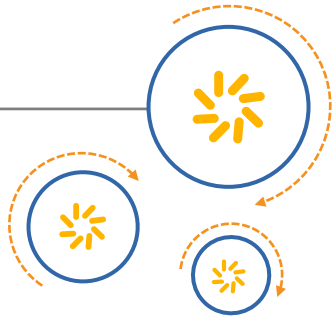
Qualcomm Technologies, Inc.



Qualcomm Snapdragon 600 Processor APQ8064

Hardware Register Description

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Revision history

Version	Date	Description
A	June 30, 2015	Initial release
B	August 25, 2015	Chapter 1: Changed name of the chipset Chapter 5: Modified CLK_BRANCH_ENA description in three places to remove reference to it being votable All: Removed references to documents that are not available to the public
C	February 8, 2016	Chapter 1: Removed Section 1.7 with architecture diagram Chapter 14: • Removed Sections 14.3 to 14.16 • Removed Sections 14.20 to 14.22 • Removed Section 14.26 to 14.32 Table 1-3 Bases in Address Order: • Removed row for OXILI_BASE • Removed row for VFE_BASE • Removed row for CSID_BASE Table 14-2 Multi_Media_Sub_System Bases: • Removed base names where OXILI_BASE was the parent • Removed base names where VFE_BASE was the parent • Removed base names where CSID_BASE was the parent Updated TOC, LOT, and index accordingly

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1 Introduction

1.1 Introduction

Customers expect their computing device to perform like a multimedia device, in addition to operating as a connectivity device. However, demand continues for increased battery life and smaller form factors. Embedded devices must continue to integrate increasingly complex functions and support more multimedia functionality, while maintaining performance and limiting board space, power consumption, and cost.

These demands are met by the Qualcomm® Snapdragon™ 600 Processor APQ8064 chipset. With its quad Krait applications processors, the 600 Processor APQ8064 device expands mass-market chipset capabilities further by making rich multimedia features accessible to more customers and end users in both developed and developing countries.

The APQ8064 device's high-level of integration significantly reduces the bill of material (BOM) to deliver board-area savings. The cost-efficient 28 nm CMOS fabrication technology significantly improves power efficiency for longer wireless connectivity, while enhancing the user's multimedia experience.

1.2 Overview

This document details the APQ8064 ARM-accessible registers. This chapter provides a register overview, along with the definitions and assumptions used. This chapter also includes a base address memory table, providing most of the major base addresses for the APQ8064 chipset. Entries in this base memory table provide links to the appropriate chapters where the register definitions at each base address are provided, in addition to the actual memory address and the top level functional area that the base address is in. See Register base address summary.

The remaining chapters are organized by core and provide detailed register information. Each core's chapter includes one or more major sections listing the core's ARM registers, as well as the address for each register, its bit assignments and bit settings. The chapter also provides an overview and detailed information on the functionality of each register. Each chapter overview starts with a more detailed base address memory table, with links to the sections within that

chapter for register definitions. In addition, the base memory addresses are provided, along with a a reference to the parent base address.

NOTE Addresses in this document are actual addresses in the total memory map, so the registers address is exactly where that register lives in memory.

NOTE The register names in this document are the complete register names with any prefixes included. The full names account for the multiple instances of register groups. Where multiple instances of register groups occur, the register names and addresses for each instance are included in this document.

This document can be used in several ways:

- If the user has the register address and wants detailed register information, the Find function of the PDF can be used to specify the address and locate the register information.
- The index at the end of the document provides an alphabetized list of all register names, with links to the appropriate register information.
- The Register Base Address Summary table in this section can be used to locate the registers at a base address location. See Register base address summary.
- The PDF bookmarks can be used to locate the registers for a specific group of registers represented by a PDF bookmark.

1.3 Definitions/guidelines

Table 1-1 offers guidance in interpreting the register definitions and covers some of the issues and assumptions made throughout this book.

Table 1-1 Register definitions

	Guidelines
Endian byte order	Endian is a term that defines the byte order to store a sequence of bytes in memory, either MSB first (big-endian) or LSB first (little endian). Hardware coding defines devide registers; in each 32-bit word, MSB = 31, LSB = 0. The chips support only little endian addressing. In little endian mode, the first byte is bits 7:0, and the fourth byte is bits 31:24.
Word addressing	All registers are word-accessible. Assume the ARM convention: a byte, 8 bits; a half-word, 16 bits; a word, 32 bits. All accesses are expected to be word size. The ARM can do byte and half-word reads, since hardware treats a read as a word access. Individual bytes accesses to a read register that triggers a hardware event will trigger an event for each read performed.
Active bit state	Unless stated otherwise, all boolean flags are active-high in register descriptions. Use a value of “1” to enable a function or indicate an event and a value of “0” do the opposite. Active-low flags are explicitly specified in the register descriptions. For example, if the BOOGA_ENA bit is set ‘1,’ it enables BOOGA mode; if cleared ‘0,’ it disables the mode.

Table 1-1 Register definitions

	Guidelines
Unused bits/ words	In the register map many bits are marked “RESERVED” or unused. Ignore undefined bits in readable registers, software cannot assume a ‘0’ upon a read. Write undefined bits with ‘0’s’ in writable registers. Bits marked “IGNORED” can be written with any desired value; in some cases this is convenient to software. Device memory and register addressing simplifies implementation and allows expansion. Many holes exist in the address space. Avoid accesses to undefined memory locations, they can cause unpredictable behavior.
Reset state	A register’s reset state is ‘unknown’ unless stated otherwise. It is better to not use a reset in hardware; it conserves area and simplifies coding and testing. Bits with a reset will be noted in the register descriptions. Assume that when a core comes out of reset, all of its programmed register bits are either in their reset state (where defined) or unknown. Do not expect a previously programmed value to be maintained.

1.4 Register categories

Most registers can be categorized using one of the types listed in Table 1-2. These categories are defined here to simplify the software interface.

Table 1-2 Register categories

	Guidelines
Write command	Command registers are always write-only, typically there is no meaningful read-back value. Use command registers to trigger events in the hardware. Often these registers serve a single purpose. You write a bit pattern to specify the desired event. Multiple events can be combined; a register may have multiple 1-bit fields, each field triggering a hardware action, such as in an interrupt clear register. A command register can also contain encoded command fields and other data fields. The bit pattern written to it is transient; i.e., there is no need to first write a value to trigger the event and another value to stop the event. If this is not the case, it will be so-stated in the register definition.
Read command	These registers return the desired data, but may also trigger a hardware event every time they are read. Often they are used to read out memory locations where each read triggers a read of the next memory location.
Control	Control registers configure the hardware to operate in a specific mode. These registers are either static or take effect at a specific time boundary (such as the next 256 chip boundary). Control bits are registered in hardware and may be readable.
Status	Status registers are read-only and reflect the current state of the hardware. There may be restrictions on when the status words can be reliably read, this ensures a self-consistent value is available. Any restrictions will be indicated in the register descriptions.
State	State registers are read/writable by the processor but also change state due to hardware events. For software to reliably read or update a state register, special “rules of engagement” may be needed to read out a self-consistent value or avoid collisions for updates by software and hardware. Each state register has these rules described in detail.
Abbreviations	
W	write register
R	read register
C	command register
X	unknown after power-on

1.5 Register base address summary

Table 1-3 Bases in Address Order

Base Name	Address	Top-Level Base
RPM_BASE	0x00000000	RPM
RPM_MSG_RAM_XPU_BASE	0x00100000	RPM
MPM_BASE	0x00200000	RPM
PA1_SSBI2_CFG_BASE	0x00300000	RPM
PA1_XPU_BASE	0x00400000	RPM
PA1_SSBI2_CMD_BASE	0x00500000	RPM
PA2_SSBI2_CFG_BASE	0x00600000	RPM
SEC_CTRL_BASE	0x00700000	Security
TLMM_BASE	0x00800000	chip_core_top
CLK_CTL_BASE	0x00900000	Clock_Controller
EBI1_CH0_BASE	0x00A00000	LPDDR
SYS_IMEM_BASE	0x00B00000	chip_core_top
PA2_SSBI2_CMD_BASE	0x00C00000	RPM
EBI1_CH1_BASE	0x00D00000	LPDDR
SFPB_WRAPPER_XPU_BASE	0x00E00000	SFPB_Wrapper
SFPB_WRAPPER_BASE	0x00F00000	SFPB_Wrapper
SPDM_BASE	0x01000000	chip_core_top
SPDM_SECURE_BASE	0x01100000	chip_core_top
SFPB_WRAPPER_MUTEX_BASE	0x01200000	SFPB_Wrapper
SFAB_BASE	0x01300000	Fabrics
AFAB_BASE	0x01400000	Fabrics
DAY_CFG_BASE	0x01500000	Fabrics
SFPB_WRAPPER_1x2_BASE	0x01600000	SFPB_Wrapper
SFPB_WRAPPER_2x1_BASE	0x01800000	SFPB_Wrapper
QDSS_DAPROM_BASE	0x01A00000	Debug_Sub_System
QDSS_ETB_BASE	0x01A01000	Debug_Sub_System
QDSS_CTI1_BASE	0x01A02000	Debug_Sub_System
QDSS_TPIU_BASE	0x01A03000	Debug_Sub_System
QDSS_TFUNNEL_BASE	0x01A04000	Debug_Sub_System
QDSS_ITM_BASE	0x01A05000	Debug_Sub_System
QDSS_STM_BASE	0x01A06000	Debug_Sub_System
QDSS_DAPM2VMT_BASE	0x01A80000	Debug_Sub_System
APCS_QGIC2_BASE	0x02000000	KraitMP_Sub_System
APCS_ACC_BASE	0x02008000	KraitMP_Sub_System
APCS_SAW2_BASE	0x02009000	KraitMP_Sub_System
APCS_TMR_BASE	0x0200A000	KraitMP_Sub_System

Table 1-3 Bases in Address Order (cont.)

Base Name	Address	Top-Level Base
APCS_GLB_BASE	0x02010000	KraitMP_Sub_System
APCS_GCC_BASE	0x02011000	KraitMP_Sub_System
APCS_L2_GDHS_BASE	0x02012000	KraitMP_Sub_System
APCS_L2_MPU_BASE	0x02013000	KraitMP_Sub_System
CPU0_APCS_ACC_BASE	0x02088000	KraitMP_Sub_System
CPU0_APCS_SAW2_BASE	0x02089000	KraitMP_Sub_System
CPU0_APCS_TMR_BASE	0x0208A000	KraitMP_Sub_System
EXT_APCS_GLB_BASE	0x02090000	KraitMP_Sub_System
EXT_APCS_GCC_BASE	0x02091000	KraitMP_Sub_System
EXT_APCS_L2_GDHS_BASE	0x02092000	KraitMP_Sub_System
EXT_APCS_L2_MPU_BASE	0x02093000	KraitMP_Sub_System
CPU1_APCS_ACC_BASE	0x02098000	KraitMP_Sub_System
CPU1_APCS_SAW2_BASE	0x02099000	KraitMP_Sub_System
CPU1_APCS_TMR_BASE	0x0209A000	KraitMP_Sub_System
CPU2_APCS_ACC_BASE	0x020A8000	KraitMP_Sub_System
CPU2_APCS_SAW2_BASE	0x020A9000	KraitMP_Sub_System
CPU2_APCS_TMR_BASE	0x020AA000	KraitMP_Sub_System
CPU3_APCS_ACC_BASE	0x020B8000	KraitMP_Sub_System
CPU3_APCS_SAW2_BASE	0x020B9000	KraitMP_Sub_System
CPU3_APCS_TMR_BASE	0x020BA000	KraitMP_Sub_System
APCS_HSEL_BASE	0x02100000	KraitMP_Sub_System
RIVA_BASE	0x03000000	RIVA
MMSS_CC_BASE	0x04000000	Multi_Media_Sub_System
MFC_BASE	0x04400000	Multi_Media_Sub_System
GEMINI_BASE	0x04600000	Multi_Media_Sub_System
MIPI_DSI_1_BASE	0x04700000	Multi_Media_Sub_System
HDMI_TX_BASE	0x04A00000	Multi_Media_Sub_System
IMEM_MMSS_BASE	0x04B00000	Multi_Media_Sub_System
ROTATOR_BASE	0x04E00000	Multi_Media_Sub_System
TV_ENC_BASE	0x04F00000	Multi_Media_Sub_System
JPEGD_BASE	0x05000000	Multi_Media_Sub_System
MDP_BASE	0x05100000	Multi_Media_Sub_System
FABRIC_MMSS_BASE	0x05200000	Fabrics
VPE_BASE	0x05300000	Multi_Media_Sub_System
MMSS_APU_BASE	0x05400000	Multi_Media_Sub_System
MMSS_SFPB_CFG_BASE	0x05700000	Multi_Media_Sub_System
MIPI_DSI_2_BASE	0x05800000	Multi_Media_Sub_System
VCAP_BASE	0x05900000	Multi_Media_Sub_System

Table 1-3 Bases in Address Order (cont.)

Base Name	Address	Top-Level Base
SMMU_VCAP_BASE	0x07200000	Multi_Media_Sub_System
SMMU_JPEGD_BASE	0x07300000	Multi_Media_Sub_System
SMMU_VPE_BASE	0x07400000	Multi_Media_Sub_System
SMMU_MDP4_0_BASE	0x07500000	Multi_Media_Sub_System
SMMU_MDP4_1_BASE	0x07600000	Multi_Media_Sub_System
SMMU_ROTATOR_BASE	0x07700000	Multi_Media_Sub_System
SMMU_JPEG_BASE	0x07800000	Multi_Media_Sub_System
SMMU_VFE_BASE	0x07900000	Multi_Media_Sub_System
SMMU_SS1080P_0_BASE	0x07A00000	Multi_Media_Sub_System
SMMU_SS1080P_1_BASE	0x07B00000	Multi_Media_Sub_System
SMMU_GFX3D_BASE	0x07C00000	Multi_Media_Sub_System
SMMU_GFX3D1_BASE	0x07D00000	Multi_Media_Sub_System
SMMU_SFPB_CFG_DUMMY_BASE	0x07F00000	Multi_Media_Sub_System
GSS_A5_CSR_BASE	0x10000000	GSS
GSS_A5_SPM_BASE	0x10001000	GSS
GSS_A5_TIMERS_BASE	0x10002000	GSS
GSS_A5_SSBI_BASE	0x10003000	GSS
GSS_A5_QGIC2_BASE	0x10008000	GSS
NAV_BASE	0x10100000	GSS
CE3_CRYPTO4_BASE	0x11000000	Security
PPSS_BASE	0x12080000	Daytona_SPS
SIC_BASE	0x120C0000	Daytona_SPS
SIC_APU_BASE	0x120C2000	Daytona_SPS
SIC_NON_SECURE_BASE	0x12100000	Daytona_SPS
INTCTL0_BASE	0x12100000	Daytona_SPS
INTCTL1_BASE	0x12100800	Daytona_SPS
INTCTL2_BASE	0x12101000	Daytona_SPS
INTCTL3_BASE	0x12101800	Daytona_SPS
INTCTL4_BASE	0x12102000	Daytona_SPS
INTCTL5_BASE	0x12102800	Daytona_SPS
INTCTL6_BASE	0x12103000	Daytona_SPS
INTCTL7_BASE	0x12103800	Daytona_SPS
SDC2_BASE	0x12140000	Daytona_SPS
SDC2_DML_BASE	0x12140800	Daytona_SPS
SDC2_BAM_BASE	0x12142000	Daytona_SPS
SDC3_BASE	0x12180000	Daytona_SPS
SDC3_DML_BASE	0x12180800	Daytona_SPS
SDC3_BAM_BASE	0x12182000	Daytona_SPS

Table 1-3 Bases in Address Order (cont.)

Base Name	Address	Top-Level Base
SDC4_BASE	0x121C0000	Daytona_SPS
SDC4_DML_BASE	0x121C0800	Daytona_SPS
SDC4_BAM_BASE	0x121C2000	Daytona_SPS
BAM_DMA_BASE	0x12240000	Daytona_SPS
BAM_DMA_BAM_BASE	0x12244000	Daytona_SPS
BAM_DMA_BAM_XPU_BASE	0x12246000	Daytona_SPS
SDC1_BASE	0x12400000	Daytona_SPS
SDC1_DML_BASE	0x12400800	Daytona_SPS
SDC1_BAM_BASE	0x12402000	Daytona_SPS
SPS_GSBI1_BASE	0x12440000	Daytona_SPS
SPS_UART1_DM_BASE	0x12450000	Daytona_SPS
SPS_QUP1_BASE	0x12460000	Daytona_SPS
SPS_GSBI2_BASE	0x12480000	Daytona_SPS
SPS_UART2_DM_BASE	0x12490000	Daytona_SPS
SPS_QUP2_BASE	0x124A0000	Daytona_SPS
USB1_HS_BASE	0x12500000	Daytona_SPS
USB1_HS_BAM_BASE	0x12502000	Daytona_SPS
USB2_HSIC_BASE	0x12510000	Daytona_SPS
USB3_HS_BASE	0x12520000	Daytona_SPS
USB3_HS_BAM_BASE	0x12522000	Daytona_SPS
USB4_HS_BASE	0x12530000	Daytona_SPS
USB4_HS_BAM_BASE	0x12532000	Daytona_SPS
CE2_CRYPTO4_BASE	0x12560000	Security
GSBI3_BASE	0x16200000	GSBIs
GSBI3_UART_DM_BASE	0x16240000	GSBIs
QUP3_BASE	0x16280000	GSBIs
GSBI4_BASE	0x16300000	GSBIs
GSBI4_UART_DM_BASE	0x16340000	GSBIs
QUP4_BASE	0x16380000	GSBIs
GSBI6_BASE	0x16500000	GSBIs
GSBI6_UART_DM_BASE	0x16540000	GSBIs
QUP6_BASE	0x16580000	GSBIs
GSBI7_BASE	0x16600000	GSBIs
GSBI7_UART_DM_BASE	0x16640000	GSBIs
QUP7_BASE	0x16680000	GSBIs
LPASS_XPU_BASE	0x17000000	chip_core_top_XPUs
KPSS_XPU_BASE	0x17100000	chip_core_top_XPUs
GSS_XPU_BASE	0x17200000	chip_core_top_XPUs

Table 1-3 Bases in Address Order (cont.)

Base Name	Address	Top-Level Base
CFPB2_XPU_CFG_BASE	0x17300000	chip_core_top_Peripherals
CSYSFPB2_BASE	0x17400000	chip_core_top_Peripherals
CE3_XPU_CFG_BASE	0x17500000	chip_core_top_XPUs
CSYSFPB_SPL_BASE	0x17F00000	chip_core_top_Peripherals
USB1_FS_BASE	0x18000000	chip_core_top_Peripherals
TSIF_BASE	0x18200000	chip_core_top_Peripherals
TSPP_BASE	0x18202000	chip_core_top_Peripherals
TSIF_BAM_BASE	0x18204000	chip_core_top_Peripherals
ADM3_0_BASE	0x18300000	chip_core_top_Peripherals
CE1_CRYPTO4_BASE	0x18500000	Security
TSSC_BASE	0x18600000	chip_core_top_Peripherals
TSSC_SSBI_BASE	0x18600000	chip_core_top_Peripherals
MSM_PDM_BASE	0x18700000	chip_core_top_Peripherals
CSYSFPB_MST_BASE	0x18D00000	chip_core_top_Peripherals
CFPB1_XPU_CFG_BASE	0x18E00000	chip_core_top_Peripherals
CSYSFPB1_BASE	0x18F00000	chip_core_top_Peripherals
GSBI5_BASE	0x1A200000	GSBIs
GSBI5_UART_DM_BASE	0x1A240000	GSBIs
QUP5_BASE	0x1A280000	GSBIs
PMEM_BASE	0x1A300000	chip_core_top_Peripherals
MSM_TCSR_BASE	0x1A400000	chip_core_top_Peripherals
PRNG_BASE	0x1A500000	chip_core_top_Peripherals
DIM_D00_REG_BASE	0x1A700000	LPDDR
DIM_BD0_REG_BASE	0x1A780000	EBI1_DIM
DIM_D01_REG_BASE	0x1A800000	LPDDR
DIM_D02_REG_BASE	0x1A900000	LPDDR
DIM_D03_REG_BASE	0x1AA00000	LPDDR
DIM_C00_REG_BASE	0x1AB00000	LPDDR
DIM_BC0_REG_BASE	0x1AB40000	EBI1_DIM
DIM_C01_REG_BASE	0x1AB80000	EBI1_DIM
DIM_D10_REG_BASE	0x1AC00000	LPDDR
DIM_BD1_REG_BASE	0x1AC80000	EBI1_DIM
DIM_D11_REG_BASE	0x1AD00000	LPDDR
DIM_D12_REG_BASE	0x1AE00000	LPDDR
DIM_D13_REG_BASE	0x1AF00000	LPDDR
DIM_C10_REG_BASE	0x1B000000	LPDDR
DIM_BC1_REG_BASE	0x1B040000	EBI1_DIM
DIM_C11_REG_BASE	0x1B080000	EBI1_DIM

Table 1-3 Bases in Address Order (cont.)

Base Name	Address	Top-Level Base
CFPB0_XPU_CFG_BASE	0x1B100000	chip_core_top_Peripherals
CSYSFPB0_BASE	0x1B200000	chip_core_top_Peripherals
SATA_XPU_CFG_BASE	0x1B300000	chip_core_top_XPUs
SATA_PHY_BASE	0x1B400000	SATA
PCIE20_BASE	0x1B500000	PCIE20
PCIE20_ELBI_BASE	0x1B502000	PCIE20
PCIE20_PARF_BASE	0x1B600000	PCIE20
LPASS_CSR_BASE	0x28000000	LP_Audio_Sub_System
LPASS_M2VMT_BASE	0x28002000	LP_Audio_Sub_System
LPASS_M2VMT_Q6SS_BASE	0x28003000	LP_Audio_Sub_System
LPASS_AHBTM_BASE	0x2800A000	LP_Audio_Sub_System
LPASS_SLIMBUS_BASE	0x28080000	LP_Audio_Sub_System
LPASS_BAM_LITE_BASE	0x28084000	LP_Audio_Sub_System
LPA_IF_BASE	0x28100000	LP_Audio_Sub_System
MIDI_BASE	0x28200000	LP_Audio_Sub_System
LPASS_QDSP6SS_PUB_BASE	0x28800000	LP_Audio_Sub_System
LPASS_QDSP6SS_CSR_BASE	0x28880000	LP_Audio_Sub_System
LPASS_QDSP6SS_L2VIC_BASE	0x28890000	LP_Audio_Sub_System
LPASS_QDSP6SS_SAW_BASE	0x288B0000	LP_Audio_Sub_System
SATA_BASE	0x29000000	SATA

1.6 Register definitions

In the register descriptions, the addresses shown are from the perspective of the ARM.

All non-command writable registers may have a reset condition as well as a time when the write takes effect. By default, writable registers do not have a reset condition, and a value written takes effect immediately. Registers not following the default behavior use the notation below:

Reset State: The value this register contains following a reset.

Each register also specifies the clock regime it is on:

Clock: <main regime>_<local regime>.

This information can be used by software to determine the main and/or local regime that a register is part of. Reads and writes to registers where the clock regime is disabled are not supported. The chip will not hang-up, but there is no guarantee the access will take place. Software can find where this may be an issue by enabling aborts for these types of accesses.

NOTE Register bit field values are represented in the register bit field Description table cells in multiple ways in this document. See the details below.

Register bit field values may be represented in the register bit field Description table cells in several ways. For example, the values for a 3-bit field with the middle bit on and the other two bits off is documented in the following ways in parts of this document:

- 0b010
- 3’b010
- 0x2
- 010:
- 010 :

Be aware of this when examining register bit fields. For larger bit fields, 0h constants also occasionally exist.

2 Chip Core Top Peripherals Registers

2.1 Overview

Table 2-1 chip_core_top_Peripherals Bases

Base Name	Parent	Address
CFPB2_XPU_APU_RGn_ACR	CFPB2_XPU_CFG_BASE	0x17300000
CSYSFPB2_CFPB2_CTRL_STATUS	CSYSFPB2_BASE	0x17400000
CSYSFPB_SPL_CFPB_SPLT_CTRL_STATUS	CSYSFPB_SPL_BASE	0x17F00000
FS1_USB_OTG_HS_ID	USB1_FS_BASE	0x18000000
TSIF_STATUS_AND_CONTROL	TSIF_BASE	0x18200000
TSPP_RST	TSPP_BASE	0x18202000
TSIF_BAM_CTRL	TSIF_BAM_BASE	0x18204000
ADM3_0_HI_CHn_CMD_PTR_SDs	ADM3_0_BASE	0x18300000
TSSC_CTL	TSSC_BASE	0x18600000
TSSC_CODEC_SSBI_CTL	TSSC_SSBI_BASE	0x18600000
TCXO_PDM_CTL	MSM_PDM_BASE	0x18700000
CSYSFPB_MST_CFPB_MASTER_CTRL_STATUS	CSYSFPB_MST_BASE	0x18D00000
CFPB1_XPU_APU_RGn_ACR	CFPB1_XPU_CFG_BASE	0x18E00000
CSYSFPB1_CFPB1_CTRL_STATUS	CSYSFPB1_BASE	0x18F00000
PMEM_IMEM_CONFIG	PMEM_BASE	0x1A300000
TCSR_PRNG_RING_OSC_DSBL	MSM_TCSR_BASE	0x1A400000
PRNG_DATA_OUT	PRNG_BASE	0x1A500000
CFPB0_XPU_APU_RGn_ACR	CFPB0_XPU_CFG_BASE	0x1B100000
CSYSFPB0_CFPB0_CTRL_STATUS	CSYSFPB0_BASE	0x1B200000

2. 2 XPU Registers (0x17300000 CFPB2_XPU_CFG_BASE)

This section contains Chip FPB 2 XPU registers.

0x17300000+4*n CFPB2_XPU_APU_RGn_ACR, n=[0..20]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type APU. These registers include a single 5 bit "owner" VMID field.

CFPB2_XPU_APU_RGn_ACR

Bits	Name	Description
31:26	RESERVED31_26	Reserved.
25	RESERVED25	Reserved
24	RESERVED24	Reserved
23:21	RESERVED23_21	Reserved
20:16	RESERVED20_16	Reserved
15:10	RESERVED15_10	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | APU_APU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a "valid" bit for the RWVMID field
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies "owner" VMID with full read/write access to the registers in the associated resource group.

0x17300F80 CFPB2_XPU_APU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

CFPB2_XPU_APU_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set APU_ESR. APU_EAR and APU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set APU_ESR. APU_EAR and APU_ESYNR0 updated with address and syndrome of error.
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x17300F84 CFPB2_XPU_APU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port.

CFPB2_XPU_APU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x17300F88 CFPB2_XPU_APU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the APU_ESYNRn registers, which are merely the "syndrome" of an error indicated by APU_ESR.

CFPB2_XPU_APU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x17300F8C CFPB2_XPU_APU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

CFPB2_XPU_APU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x17300F90 CFPB2_XPU_APU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

CFPB2_XPU_APU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x17300F94 CFPB2_XPU_APU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

CFPB2_XPU_APU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x17300FF4 CFPB2_XPU_APU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

CFPB2_XPU_APU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved

CFPB2_XPU_APU_REV (cont.)

Bits	Name	Description
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x17300FF8 CFPB2_XPU_APU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x00001014

APU ID Register: Read-only register that defines various configuration attributes of the APU instance.

CFPB2_XPU_APU_IDR

Bits	Name	Description
31:29	RESERVED31_21	Reserved
28:24	MSB	Indicates most significant address bit number used to select a resource group
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.

CFPB2_XPU_APU_IDR (cont.)

Bits	Name	Description
9	RESERVED9	Reserved
8:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

2.3 CFPB 2 Config (System FPB) Registers (0x17400000 CSYSFPB2_BASE)

This section contains System FPB 2 registers.

0x17400000 CSYSFPB2_CFPB2_CTRL_STATUS

Type: Read/Write
Clock: CC_CFPB2_CLK
Reset State: 0x00000000

This register is a general configuration register.

CSYSFPB2_CFPB2_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables Power up value is clear (0)
11	RPM_PROC_IRQ_EN	SW: RW, HW: R RPMProcInterruptEnable When set, the RPM Processor receives an interrupt whenever ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	APPS_PROC_IRQ_EN	SW: RW, HW: R AppsProcInterruptEnable When set, the Application Processor receives an interrupt whenever ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

CSYSFPB2_CFPB2_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x5: Select the S0_M0 ahb2ahb bridge test bus. 0x6: Select the S1_M1 ahb2ahb bridge test bus. 0x7: Select the M0 ahb2ahb bridge test bus. 0x8: Select the M1 ahb2ahb bridge test bus. 0x9: Select the M2 ahb2ahb bridge test bus. 0xA: Select the M3 ahb2ahb bridge test bus. 0xB: Select the M4 ahb2ahb bridge test bus. 0xC: Select the M5 ahb2ahb bridge test bus. 0xD: Select the M6 ahb2ahb bridge test bus. 0xE: Select the M7 ahb2ahb bridge test bus. 0xF: Select the M8 ahb2ahb bridge test bus. 0x10: Select the M9 ahb2ahb bridge test bus. 0x11: Select the M10 ahb2ahb bridge test bus. 0x12: Select the M11 ahb2ahb bridge test bus. 0x13: Select the M12 ahb2ahb bridge test bus. 0x14: Select the M13 ahb2ahb bridge test bus. 0x15: Select the M14 ahb2ahb bridge test bus. 0x16: Select the M15 ahb2ahb bridge test bus.

0x17400004+ 0x4*a CSYSFPB2_CFPB2_AHB2AHB_CFG_Ma, a=[0..0]

Type: Read/Write
Clock: CC_CFPB2_CLK
Reset State: 0x00000009

The CFPB2_AHB2AHB_CFG_Ma register is to configure the AHB2AHB bridge of master Ma. The AHB2AHB bridge is instantiated if the AHB interface is async (Generic: MASTER_ASYNC_IF(a) = ’1’). Otherwise this register is reserved.

CSYSFPB2_CFPB2_AHB2AHB_CFG_Ma

Bits	Name	Description
30:6	RESERVED_BITS30_6	

CSYSFPB2_CFPB2_AHB2AHB_CFG_Ma (cont.)

Bits	Name	Description
5:4	M_AHB2AHB_TEST_EN	SW: RW, HW: R Test enable for the Sa lite_bridge. Power up value is 00 0x0: DISABLED 0x1: Select slave side test signals 0x2: Select master side test signals 0x3: RESERVED_PROGRAMMING
3	M_WPOST_EN	SW: RW, HW: R MaWritePostEnable When set (1), the ahb2ahb bridge will support posting of write data. When cleared (0), each write request must complete across the bus before the next is accepted. Power up value is set (1)
2	M_HALT_ACK	SW:R, HW:W Indicates the Ma acknowledgement of halt_req asserted by software. Power up value is clear (0).
1	M_HALT_REQ	SW:RW, HW:R Software should write to this register to request the Ma lite_bridge master to cleanly halt. Power up value is clear (0).
0	M_IDLE	SW:R, HW:W Indicates that the Ma lite bridge master FSM is in IDLE state. Power up value is set (1).

0x17400044 CSYSFPB2_CFPB2_PORT_EN

Type: Read/Write
Clock: CC_CFPB2_CLK
Reset State: 0xFFFFFFFF

This register is the CFPB2 master port enable register.

CSYSFPB2_CFPB2_PORT_EN

Bits	Name	Description
31:1	RESERVED_BIT31_1	Only one master port is used.
0	M0_PORT_EN	SW: RW, HW: R M0PortEnable When cleared (0), M0 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

0x17400050 CSYSFPB2_CFPB2_ERROR_STAT

Type: Read/Write
Clock: CC_CFPB2_CLK
Reset State: 0x00000000

This register is the bus error status register.

CSYSFPB2_CFPB2_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the channel ID that caused the detected error when CID is valid for the master of the access. If not, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Master0 0x1: Master1 0x2: Master2 0x3: Master3 0x4: Master4 0x5: Master5 0x6: Master6 0x7: Master7 0x8: Master8 0x9: Master9 0xA: Master10 0xB: Master11 0xC: Master12 0xD: Master13 0xE: Master14 0xF: Master15
11:10	RESERVED_BITS11_10	

CSYSFPB2_CFPB2_ERROR_STAT (cont.)

Bits	Name	Description
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit
3:2	RESERVED_BIT3_2	
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted. Clearing (0) this bit clears any interrupts asserted as well as enables the ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x17400054 CSYSFPB2_CFPB2_ERROR_ADDR

Type: Read
Clock: CC_CFPB2_CLK
Reset State: 0x00000000

This register contains the bus error address.

CSYSFPB2_CFPB2_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x1740005C CSYSFPB2_CFPB2_XPU_ACR

Type: Read/Write
Clock: CC_CFPB2_CLK
Reset State: 0xFFFFFFFF

The CFPB2_XPU_ACR register is the CFPB2 Access Control Register for configuring register protection.

CSYSFPB2_CFPB2_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R CFPB2 XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the CFPB2 configure space, including this register itself. Power up value is set (1)

0x17400060 CSYSFPB2_CFPB2_HW_CLK_GATING_CFG

Type: Read/Write
Clock: CC_CFPB2_CLK
Reset State: 0x00000000

The CFPB2_HW_CLK_GATING_CFG register is for hardware clock gating configuration.

CSYSFPB2_CFPB2_HW_CLK_GATING_CFG

Bits	Name	Description
31:11	RESERVED_BITS31_11	

CSYSFPB2_CFPB2_HW_CLK_GATING_CFG (cont.)

Bits	Name	Description
10:4	HYSTERESIS_CNT_SW	SW: RW, HW: R Hysteresis Counter Value This field is used by SW to set the hysteresis counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)
3:0	WAKE_CNT_SW	SW: RW, HW: R Wakeup Counter Value This field is used by SW to set the wakeup counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)

2.4 USB_OTG_HS registers (0x18000000 USB1_FS_BASE)

This section contains FS USB OTG HS registers.

2.4.1 Identification registers

Identification registers are used to declare the slave interface presence and include a table of the hardware configuration parameter.

0x18000000 FS1_USB_OTG_HS_ID

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0042FA05

The USB_OTG_HS_ID register is the identification register. It provides a simple way to determine if the USB-HS USB 2.0 core is provided in the system. The ID register identifies the USB-HS USB 2.0 core and its revision.

FS1_USB_OTG_HS_ID

Bits	Name	Description
31:24	RESERVED_BITS31_24	These bits are reserved and should be set to zero.
23:16	REVISON_7_0	This field contains the revision number of the core - 0x42.
15:8	NID_5_0	This field contains the complement version of ID[7:0] - 0xFA.
7:0	ID_5_0	This field is the configuration number. This number is set to 0x05 and indicates that the peripheral is the USB-HS USB 2.0 core.

0x18000004 FS1_USB_OTG_HS_HWGENERAL

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x5C2

The USB_OTG_HS_HWGENERAL register contains the general hardware parameters.

FS1_USB_OTG_HS_HWGENERAL

Bits	Name	Description
31:10	RESERVED_BITS31_10	Clear (0) these bits.
9	SM	VUSB_HS_PHY_SERIAL = 2
8:6	PHYM	VUSB_HS_PHY_TYPE = 7
5:4	PHYW	VUSB_HS_PHY16_8 = 0

FS1_USB_OTG_HS_HWGENERAL (cont.)

Bits	Name	Description
3	BWT	This bit is reserved for internal testing = 0
2:1	CLCK	VUSB_HS_CLOCK_CONFIGURATION = 1
0	RT	VUSB_HS_RESET_TYPE = 0

0x18000008 FS1_USB_OTG_HS_HWHOST

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x10020001

The USB_OTG_HS_HWHOST register contains the host hardware parameters.

FS1_USB_OTG_HS_HWHOST

Bits	Name	Description
31:24	TTPER	VUSB_HS_TT_PERIODIC_CONTEXTS
23:16	TTASY	VUSB_HS_TT_ASYNC_CONTEXTS
15:4	RESERVED_BITS15_4	Clear (0) these bits.
3:1	NPORT	VUSB_HS_NUM_PORT-1
0	HC	VUSB_HS_HOST

0x1800000C FS1_USB_OTG_HS_HWDEVICE

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000021

The USB_OTG_HS_HWDEVICE register contains the device hardware parameters.

FS1_USB_OTG_HS_HWDEVICE

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:1	DEVEP	VUSB_HS_DEV_EP
0	DC	Device capable; [VUSB_HS_DEV/=0]

0x18000010 FS1_USB_OTG_HS_HWTXBUF

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x80070B08

The USB_OTG_HS_HWTXBUF register contains the Tx buffer hardware parameters.

FS1_USB_OTG_HS_HWTXBUF

Bits	Name	Description
31	TXLCR	This bit is fixed to 1'b1 so that the local context register's are included in the design. This means that the DMA context is implemented in FlipFlops.
30:24	RESERVED_BITS30_24	Clear (0) these bits.
23:16	TXCHANADD	VUSB_HS_TX_CHAN_ADD - Defines the number of address lines needed per Endpoint per the TX latency buffer. It's reset value is taken from a GENERIC value passed to the core.
15:8	TXADD	VUSB_HS_TX_ADD - Defines the number of address lines needed per the entire TX latency buffer. It's reset value is taken from a GENERIC value passed to the core.
7:0	TXBURST	VUSB_HS_TX_BURST - Defines the data burst length of the AHB master interface in Quad-words (4-byte increments) of the TX data. It's reset value is taken from a GENERIC value passed to the core. Note that the actual burst lengthis will depend on the settings of USB_OTG_HS_AHB_MODE and USB_OTG_HS_AHB_BURST registers.

0x18000014 FS1_USB_OTG_HS_HWRXBUF

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000808

The USB_OTG_HS_HWRXBUF register contains the Rx buffer hardware parameters.

FS1_USB_OTG_HS_HWRXBUF

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits).
15:8	RX_ADD	VUSB_HS_RX_ADD - Defines the number of address lines needed per the entire RX latency buffer. It's reset value is taken from a GENERIC value passed to the core.

FS1_USB_OTG_HS_HWRXBUF (cont.)

Bits	Name	Description
7:0	RX_BURST	VUSB_HS_RX_BURST - Defines the data burst length of the AHB master interface in Quad-words (4-byte increments) of the RX data. It's reset value is taken from a GENERIC value passed to the core. Note that the actual burst lengthis will depend on the settings of USB_OTG_HS_AHB_MODE and USB_OTG_HS_AHB_BURST registers.

0x18000040+4*n FS1_USB_OTG_HS_SCRATCH_RAMn, n=[0..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

USB_OTG_HS_SCRATCH_RAMn registers are 16 32bit scratch registers.Required for passing USB software information between different images.

FS1_USB_OTG_HS_SCRATCH_RAMn

Bits	Name	Description
31:0	SCRATCH_REGISTER	32 bit scratch register

2.4.2 Device/host timer registers

The host/device controller drivers can measure time related activities using these timer registers.

NOTE These registers are not part of the standard EHCI controller.

0x18000080 FS1_USB_OTG_HS_GPTIMER0LD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER0LD register is the general purpose timer 0 load register. This register contains the timer duration or load value. See the GPTIMER0CTRL register for a description of the timer functions.

FS1_USB_OTG_HS_GPTIMER0LD

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.

FS1_USB_OTG_HS_GPTIMER0LD (cont.)

Bits	Name	Description
23:0	GPTLD	General purpose timer load value. This field is the value to be loaded into the GPTCNT countdown timer on a reset action. This value in this register represents the time in microseconds minus 1 for the timer duration. Example: for a one millisecond timer, load 1000-1=999 or 0x0003E7. Note: Max value is 0xFFFFFF or 16.777215 seconds

0x18000084 FS1_USB_OTG_HS_GPTIMER0CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER0CTRL register is the general purpose timer 0 control register. This register contains the control for the timer and a data field can be queried to determine the running count value. This timer has a granularity of 1 ms and can be programmed to a little over 16 seconds. There are two modes supported by this timer: the first is a one-shot and the second is a looped count, which is described in the register table below. When the timer counter value transitions to zero, an interrupt can be generated though the use of the timer interrupts in the USBTS and USBINTR registers.

FS1_USB_OTG_HS_GPTIMER0CTRL

Bits	Name	Description
31	GTPRUN	General purpose timer run Read/write value 0 = Timer stop value 1 = Timer run This bit enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.
30	GPTRST	General purpose timer reset Write-only value 0 = No action value 1 = Load counter value Writing a one to this bit will reload the GPTCNT with the value in GPTLD.
29:25	RESERVED_BITS29_25	Clear (0) these bits.

FS1_USB_OTG_HS_GPTIMER0CTRL (cont.)

Bits	Name	Description
24	GPTMODE	General purpose timer mode Read/write value 0 = One shot value 1 = Repeat This bit selects between a single timer countdown and a looped count down. In the one-shot mode, the timer will count down to zero, generate an interrupt, and stop until the counter is reset by the software. In the repeat mode, the timer will count down to zero, generate an interrupt, and automatically reload the counter to begin again.
23:0	GPTCNT	General purpose timer counter Read-only This field is the value of the running timer.

0x18000088 FS1_USB_OTG_HS_GPTIMER1LD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER1LD register is the general purpose timer 1 control register. This register contains the timer duration or load value. See the GPTIMER0LD register for a description of the timer functions.

FS1_USB_OTG_HS_GPTIMER1LD

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.
23:0	GPTLD	General purpose timer load value. This field is the value to be loaded into the GPTCNT countdown timer on a reset action. This value in this register represents the time in microseconds minus 1 for the timer duration. Example: for a one millisecond timer, load 1000-1=999 or 0x0003E7. Note: Max value is 0xFFFFFF or 16.777215 seconds.

0x1800008C FS1_USB_OTG_HS_GPTIMER1CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER1CTRL register is the general purpose timer 1 control register. See the description of the USB_OTG_HS_GPTIMER0CTRL register for details about this register.

FS1_USB_OTG_HS_GPTIMER1CTRL

Bits	Name	Description
31	GTPRUN	General purpose timer run Read/write value 0 = Timer stop value 1 = Timer run This bit enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.
30	GPTRST	General purpose timer reset Write-only value 0 = No action value 1 = Load counter value Writing a one to this bit will reload the GPTCNT with the value in GPTLD.
29:25	RESERVED_BITS29_25	Clear (0) these bits.
24	GPTMODE	General purpose timer mode Read/write value 0 = One shot value 1 = Repeat This bit selects between a single timer countdown and a looped count down. In the one-shot mode, the timer will count down to zero, generate an interrupt, and stop until the counter is reset by the software. In the repeat mode, the timer will count down to zero, generate an interrupt, and automatically reload the counter to begin again.
23:0	GPTCNT	General purpose timer counter Read-only This field is the value of the running timer.

2.4.3 Wrapper operational registers

0x18000090 FS1_USB_OTG_HS_AHB_BURST

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_AHB_BURST register determines the AHB master mode of the USB HS Core.

NOTE If the USB_OTG_HS_AHB_MODE is configured to be 0x0 (the AHB Transactor is used), this register must be 0x0 as well, otherwise the AHB Master bus behavior is undefined. Use values other than 0x0 only if setting USB_OTG_HS_AHB_MODE to 0x1.

FS1_USB_OTG_HS_AHB_BURST

Bits	Name	Description
31:3	RESERVED_BITS31_3	Should be set to zero.
2:0	AHB_BURST	AMBA AHB BURST. This is a r/w field that selects the following options for the m_hburst signal of the AMBA master interface: In all cases where the unspecified length burst is allowed, singles access may also occur, this is mostly true when the transaction is not 32-bit aligned. Two consecutive single accesses should not happen. When a INCRx burst size is selected and the transfer is not multiple of the INCRx burst, the burst is decomposed in the different ways. With AHBBRST[2] = 1, the smaller bursts will be unspecified length. with AHBBRST[2] = 0, the smaller bursts will be smaller INCRx or singles. For example, lets say that it's required at a given time, to transfer 22 words of information, for the following values of AHBBRST the master sequence will be: This field after reset is set to a default value that can be configured in the file vusb_hs_cfg.vhd. The AHBBRST field is only used if the AMBA-AHB system interface has been selected. It has no effect for cores featuring BVCI interface. In the later case the read will return zeros. When this field is different from zero, the value of the fields TXBURST /RXBURST in register BURSTSIZE 160h, will be ignored by the controller. Internally the BURSTSIZE will be set to the value of the INCRx AMBA burst. Since this has a direct relation with the burst sizes you must be careful with AHB burst selected. Although the TXBURST / RXBURST are bypassed, this register can still be written / read with no effect, while the AHBBRST field is non-zero. 0x0: INCR burst of unspecified length 0x1: INCR4, non-multiple transfers of INCR4 will be decomposed into singles 0x2: INCR8, non-multiple transfers of INCR8, will be decomposed into INCR4 or singles 0x3: INCR16, non-multiple transfers of INCR16, will be decomposed into INCR8, INCR4 or singles 0x4: This value is reserved and should not be used 0x5: INCR4, non-multiple transfers of INCR4 will be decomposed into smaller unspecified length bursts 0x6: INCR8, non-multiple transfers of INCR8 will be decomposed into smaller unspecified length bursts 0x7: INCR16, non-multiple transfers of INCR16 will be decomposed into smaller unspecified length bursts 0x5: INCR4+ INCR4 +INCR4+ INCR4 +INCR4+ INCR unspec. length 0x6: INCR8+INCR8+INCR4+ INCR unspec. length 0x7: INCR16+INCR4+ INCR unspec. length 0x1: INCR4+ INCR4 +INCR4+ INCR4 +INCR4+SINGLE+SINGLE 0x2: INCR8+INCR8+INCR4+SINGLE+SINGLE 0x3: INCR16+INCR4+SINGLE+SINGLE

0x18000094 FS1_USB_OTG_HS_XTOR_STS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_XTOR_STS register is currently a placeholder for future status bits from the AHB2AHB Transactor.

FS1_USB_OTG_HS_XTOR_STS

Bits	Name	Description
31:2	RESERVED_BITS31_2	Not used currently.
1	GRANT_STOLEN	Reports whether the arbiter removed the hgrant signal prior to completing a transaction. This is currently supported in WRITES ONLY. This bit can be cleared by writing a ’1’ to the GRANT_STOLEN_CLEAR bit in the USB_OTG_HS_AHB_MODE register. To enable this bit again, write a ’0’ to he GRANT_STOLEN_CLEAR bit in the USB_OTG_HS_AHB_MODE register.
0	RESERVED_BIT0	Not used currently.

0x18000098 FS1_USB_OTG_HS_AHB_MODE

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1

FS1_USB_OTG_HS_AHB_MODE

Bits	Name	Description
31	ASYNC_BRIDGES_BYPASS	Default is ’0’. When ’0’ the asynchronous bridge on the master AHB interface issued. When ’1’, it is bypassed. The bridge on the slave AHB is always used.
30:5	RESERVED_BITS30_5	Not used currently.
4	INCR_OVERRIDE	Valid only if the Transactor is bypassed: When ’1’, all INCR bursts from the USB Core will be internally transformed into SINGLE transfers. When ’0’, if the USB Core issues an INCR burst, it will propagate to the external master AHB port.

FS1_USB_OTG_HS_AHB_MODE (cont.)

Bits	Name	Description
3:2	HPROT_MODE	When ’00’ the HPROT signal out of the USB Wrapper is ’0001’, and all transactions are non-posted. When ’01’ the HPROT signal out of the USB Wrapper is ’0101’, and all transactions are posted. When ’10’ the HPROT signal out of the USB Wrapper alternates according to the context of the AHB bus access. Control structures are non-posted while data transfer is posted. When ’11’, reserved value, but currently maps to non-posted (same as ’00’).
1	GRANT_STOLEN_CLEAR	Clears the grant stolen field of the USB_OTG_HS_XTOR_STS register. To enable this bit again, write ’0’ after clearing the GRANT_STOLEN (’1’).
0	XTOR_BYPASS	When this bit is set (1), the AHB Transactor is bypassed, and the USB HS Core’s AHB Master interface is directly connected to the AHB system. In this case, the USB_OTG_HS_AHB_BURST register value will determine the bus characteristics. When this bit is reset (0), the AHB Transactor is used to connect the USB HS Core to the AHB system.

0x1800009C FS1_USB_OTG_HS_GEN_CONFIG

Type: Read/write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXX0830

The USB_OTG_HS_GEN_CONFIG register is used to configure various features that have been added to the HS USB Core.

FS1_USB_OTG_HS_GEN_CONFIG

Bits	Name	Description
31:16	USB_OTG_HS_HW_QVERSION	HW revision of the USB OTG HS core. This version changes with every official release of USB_OTG_HS core.
15	SYS_CLK_SW_EN	This bit is applicable only in SPS Device mode. When this bit is set then USB core always voting for USB_SYSTEM_CLK. Default value is 0 - USB core doesn’t request USB_SYSTEM_CLK when in Low Power Mode.
14	TESTMUX_SEL_4	See TESTMUX_SEL_3_0 the first 4 bits of this register.
13	USB_BAM_DISABLE	This bit disables the bam logic inside the USB and makes him work in Legacy mode.
12	DMA_HPROT_CTRL	When this bit is set Link Controller always does non-posted dQH writes.
11	ISO_FIX_EN	This bit enables fix for Isochronous bug in CI core (CR--0000135251).

FS1_USB_OTG_HS_GEN_CONFIG (cont.)

Bits	Name	Description
10	DSC_PE_RST_EN	This bit enables an automatic reset of Device PE State Machine on disconnection event when operating as device. This reset is a HW fix for CR-000940.
9	HOST_SIM_TIMERS_EN_SUSP	When this bit is set (1), the timers used for the USB suspend process short for faster simulation and ATE time. When this bit is clear(0), the timers used for the USB suspend process are according to the USB specification.
8	HOST_SIM_TIMERS_EN_STD	When this bit is set (1), the timers used for the USB reset on the ULPI are short for faster simulation and ATE time. When this bit is clear(0), the timers used for the USB reset on the ULPI are according to the USB specification.
7	PE_RX_BUF_PENDING_EN	This is only valid in Device Mode. Setting this bit will cause to store a Transaction Status Tag in the Pending register instead of RX Buffer if the RX Buffer is full. The Tag will move from Pending register to RX Buffer as soon as it becomes not full.
6	STREAM_RX_BYPASS_ENABLE	This is only valid in Device Mode. If SDIS bit is set (bit 4 of USB_OTG_HS_USBMODE (0x1A8)), i.e., streaming mode is disabled, setting this bit will cause the RX traffic to override the SDIS bit, and to receive in streaming mode. TX will still be in non-streaming mode.
5	ULPI_SERIAL_EN	This bit must be set to enable operation of ULPI Serial FS/LS mode. Default state is ’1’ - ULPI Serial mode is supported.
4	PE_DP_TXFIFO_IDLE_FORCE	This is only valid in Device Mode. Setting this bit to ’1’ forces the dp_tx_fifo_cmd_dev to be equal to PE_DP_TXFIFO_IDLE when Device PE state machine in REPORT_NAK state and the RX Buffer is full. This bit is used to enable fix of CR-001612. Reset value is ’1’.

FS1_USB_OTG_HS_GEN_CONFIG (cont.)

Bits	Name	Description
3:0	TESTMUX_SEL_3_0	With TESTMUX_SEL_4 select one of the following test buses: Value 00001 Key state machines 01101 hsic_test_bus1 01110 hsic_test_bus2 10000 dma_eng_3 dma_dev_sm_2 10001 dma_eng_4 dma_traf others zeros 0x2: dma_eng_0 dma_dev_sm_1 0x3: dma_eng_1 dma_context 0x4: dma_eng_2 dma_mem_arb 0x5: prot_eng_0 0x6: prot_eng_1 0x7: prot_eng_2 0x8: port_ctrl_0 0x9: port_ctrl_1 0xA: tx_buffer 0xB: rx_buffer 0xC: otg

0x180000A0 FS1_USB_OTG_HS_GEN_CONFIG_2

Type: Read/write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0001F60

Register for the chicken bits. The USB_OTG_HS_GEN_CONFIG_2 register is used to configure various features that have been added to the HS USB Core. By default, all chicken bits are off and the fix is applicable.

FS1_USB_OTG_HS_GEN_CONFIG_2

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12	LINESTATE_DIFF_WAKEUP_EN	chicken bit for CR-0000155486.when this bit is set the USB enables the HW fix for Race condition between the attempt to enter LPM and USB bus reset.Default value is 1.
11	ULPI_LPM_PEND_EN	chicken bit for CR-0000153486.when this bit is set the USB enables the HW fix for Function Control and LPM race condition.Default value is 1.
10	RX_FULL_NAK_EN	chicken bit for CR-0000152878.when this bit is set the USB will respond with NAK's for Host Tokens with very slow AHB and when Streaming mode is enabled. Default value is 1.

FS1_USB_OTG_HS_GEN_CONFIG_2 (cont.)

Bits	Name	Description
9	ENDLESS_TD_EN	chicken bit for CR-0000152976. When this bit is set Performance enhancements for 'infinite' Producer pipe (out endpoint with eTD that points to itself) are enabled. Default value is 1.
8	SCRATCH_RAM_EN	chicken bit for CR-0000149922. When this bit is set the use of scratch ram is enabled and the SW can read/write from addresses 0x040 - 0x07c. when this bit is clear SW can no longer access those registers. Default value is 1.
7	SESS_VLD_CTRL_EN	When this bit is set then bit 25 of USBCMD register controls sess_vld signal inside the Link Controller. When this bit is clear then Link Controller receives sess_vld directly from PHY. Default value is 0.
6	CI_T_WTSUSRSTHS_EN	When this bit is 0 then Device Port Control State Machine waits 2.5 us from USB Reset detection until starting driving Chirp K. When this bit is 1 then Device Port Control State Machine waits 1.5 ms from USB Reset detection until starting driving Chirp K. Default value is 1 - legacy behavior.
5	CI_T_UCH_EN	When this bit is 0 then Device Port Control State Machine drives Chirp K for 1 ms. When this bit is 1 then Device Port Control State Machine drives Chirp K for 2ms. Default value is 1 - legacy behavior.
4	DP_RESET	chicken bit for fix CI2687: When the OTG core is acting as a Host, and VBUS is turned off, and the attached Device attempts to perform a Session Request Protocol by using Data-line Pulsing, it will not be recognized by the Host. Also, when doing HNP and becoming a Host, a SE0 is forced in the line causing the OPT TD5.4 test to fail, without the software workaround.
3	ZLP_PRIME	chicken bit for fix CI2655: When using ISO IN endpoints with MULT=3 and low bandwidth system bus access, the controller may enter into a wait loop situation without warning the software. Due to the low bandwidth the last packet from a mult3 sequence may not be fetched in time before the last token IN is received (for that uframe/endpoint). This will cause the controller to reply with a zero length packet (ZLP), breaking the prime sequence.
2	NO_SOF_RX_FIFO_FULL	chicken bit for fix CI2581: During normal operation, if the RX Fifo becomes full and the protocol engine needs to send a command to the DMA state machine, it will wait in that state until the RX Fifo becomes not full. As the protocol state machine also handles the SOF generation, the SOFs will no longer be sent. If one SOF is missed, the Host controller will issue a false babble detection. If more than 3.125ms are elapsed without SOFs the peripheral will recognize the idle bus as a USB reset.
1	WRONG_OPMODE_SUSP	chicken bit for fix CI1274: When the Controller enters a Suspend state it asserts opmode with the wrong value, according to specifications 'UTMI+ Specification, Revision 1.0, Section 3.2' and 'UTMI+ Low Pin Interface Specification, Revision 1.1, Section 3.8.5.3'. This causes no issue in actual usage.

FS1_USB_OTG_HS_GEN_CONFIG_2 (cont.)

Bits	Name	Description
0	RESUME_END_INTER	chicken bit for fix CI1179: Working as host, when doing resume a port change interrupt was fired at the end of resume. According to the EHCI spec no interrupt should be fired.

2.4.4 Device/host capability registers

0x18000100 FS1_USB_OTG_HS_CAPLENGTH

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x01000040

The USB_OTG_HS_CAPLENGTH register is the capability register length. It is used to indicate which offset to add to the register base address at the beginning of the operational register.

FS1_USB_OTG_HS_CAPLENGTH

Bits	Name	Description
31:16	HCIVERSION_15_0	BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.
7:0	CAPLENGTH_7_0	Offset at beginning of operational register

0x18000104 FS1_USB_OTG_HS_HCSPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00010011

The USB_OTG_HS_HCSPARAMS register contains the host control structural parameters. The port steering logic capabilities are described in this register.

FS1_USB_OTG_HS_HCSPARAMS

Bits	Name	Description
31:28	RESERVED_BITS31_28	Clear (0) these bits.
27:24	N_TT_3_0	Number of transaction translators This field indicates the number of embedded transaction translators associated with the USB2.0 host controller. For a multi-port host, this field will always equal 0001. For all other implementations, N_TT = 0000. This in a non-EHCI field to support embedded TT.

FS1_USB_OTG_HS_HCSPARAMS (cont.)

Bits	Name	Description
23:20	N_PTT_3_0	Number of ports per transaction translator This field indicates the number of ports assigned to each transaction translator within the USB2.0 host controller. For a multi-port host this field will always equal N_PORTS. For all other implementations, N_PTT = 0000. This in a non-EHCI field to support embedded TT.
19:17	RESERVED_BITS19_17	Clear (0) these bits.
16	PI_3_0	Port indicator This bit indicates whether the ports support port indicator control. When set (1), the port status and control registers include a read/writable field for controlling the state of the port indicator. This field will always be set (1).
15:12	N_CC_3_0	Number of companion controllers This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no internal companion controllers. Port-ownership hand-off is not supported. A value larger than zero in this field indicates that there are companion USB1.1 host controller(s). Port-ownership hand-offs are supported. High-, full-, and low-speed devices are supported on the host controller root ports. In this implementation, this field will always be clear (0).
11:8	N_PCC_3_0	Number of ports per companion controller This field indicates the number of ports supported per internal companion controller. It is used to indicate the port routing configuration to the system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2, then N_PCC could have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, and so on. In the previous example, the N_PCC could have been 4, where the first 4 are routed to companion controller 1 and the last two are routed to companion controller 2. The number in this field must be consistent with N_PORTS and N_CC. In this implementation, this field will always be clear (0).
7:5	RESERVED_BITS7_5	Clear (0) these bits.
4	PPC	Port power control This field indicates whether the host controller implementation includes port power control. Set (1) indicates that the ports have port power switches. Clear (0) indicates that the ports do not have port power switches. The value of this field affects the functionality of the port power field in each port status and control register. This bit will always be clear (0) for a device only implementation.

FS1_USB_OTG_HS_HCSPARAMS (cont.)

Bits	Name	Description
3:0	N_PORTS_3_0	Number of downstream ports This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the operational register. Valid values are in the range of 1h to Fh. A zero in this field is undefined. The number of ports for a host implementation is configurable from 1 to 8. This field will always be set (1) for device-only implementation.

0x18000108 FS1_USB_OTG_HS_HCCPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0006

The USB_OTG_HS_HCCPARAMS register contains the host control capability parameters. This register identifies multiple mode control (time-base bit functionality) addressing capability.

FS1_USB_OTG_HS_HCCPARAMS

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.
15:8	EECP_7_0	EHCI extended capabilities pointer Default = 0 This optional field indicates the existence of a capabilities list. A value of 00h indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capability. The pointer value must be 40h or greater if implemented to maintain the consistency of the PCI header defined for this class of device. For this implementation, all of these bits are clear (0).
7:4	IST_7_4	Isochronous scheduling threshold Default = implementation dependent This field indicates, relative to the current position of the executing host controller, where the software can reliably update the isochronous schedule. When bit [7] is clear (0), the value of the least significant 3 bits indicates the number of microframes a host controller can hold a set of isochronous data structures (one or more) before flushing the state. When bit [7] is set (1), then host software assumes the host controller may cache an isochronous data structure for an entire frame. All of the bits in this field will always be clear (0).
3	RESERVED_BIT3	Clear (0) this bit.

FS1_USB_OTG_HS_HCCPARAMS (cont.)

Bits	Name	Description
2	ASP	Asynchronous schedule park capability Default = 1 If this bit is set (1), then the host controller supports the park feature for high-speed queue heads in the asynchronous schedule. The feature can be disabled, or enabled and set to a specific level by using the (ASPE) and (ASP[1:0]) fields in the USB_OTG_HS_USBCMD register. This field will always be set (1).
1	PFL	Programmable frame list flag If this bit is clear (0), then the system software must use a frame list length of 1024 elements with this host controller. The FS[2:0] field in the USBCMD register is read-only and must be cleared (0). If this bit is set (1), then the system software can specify and use a smaller frame list, and configure the host controller using the FS[2:0] field in the USBCMD register. The frame list must always be aligned on a 4k-page boundary. This requirement ensures that the frame list is always physically contiguous. This bit in this field will always be set (1).
0	ADC	64-bit addressing capability This field will always be clear (0). No 64-bit addressing capability is supported.

0x18000120 FS1_USB_OTG_HS_DCIVERSION

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1

The USB_OTG_HS_DCIVERSION register contains the device interface version number. The device controller interface conforms to the two-byte BCD encoding of the interface version number contained in this register.

FS1_USB_OTG_HS_DCIVERSION

Bits	Name	Description
15:0	DCIVERSION_15_0	Device interface version number

0x18000124 FS1_USB_OTG_HS_DCCPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x190

The USB_OTG_HS_DCCPARAMS register contains the device control capability parameters. These fields describe the overall host/device capability of the controller.

FS1_USB_OTG_HS_DCCPARAMS

Bits	Name	Description
31:9	RESERVED_BITS31_9	Clear (0) these bits.
8	HC	Host capable When this bit is set (1), this controller is capable of operating as an EHCI-compatible USB 2.0 host controller.
7	DC	Device capable When this bit is set (1), this controller is capable of operating as a USB 2.0 device.
6:5	RESERVED_BITS6_5	Clear (0) these bits.
4:0	DEN_4_0	Device endpoint number This field indicates the number of endpoints build into the device controller. If this controller is not device capable, then this field will be al zeroes. Valid values for this field are 0 through 16.

2.4.5 Device/host operational registers

0x18000140 FS1_USB_OTG_HS_USBCMD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00080000

The USB_OTG_HS_USBCMD register is the USB command register. The serial bus host/device controller executes the command indicated in this register.

FS1_USB_OTG_HS_USBCMD

Bits	Name	Description
31	RST_CTRL	Default value = 0. Set to 1 to block operational reset to xcvr (ser and ulpi) clock domains.
30	ULPI_STP_CTRL	Default value = 0. Set to 1 to block the ulpi_stp signal from going out to ULPI PHY
29	ASYNC_INTR_CTRL	Default value = 0. Set to 1 to allow the async interrupt out from the HS core.
28	SE0_GLITCH_FIX_CTRL	Default value = 0. Set to 1 to activate the SE0 glitch fix mechanism
27	FS_3_WIRE_2_WIRE_SELECT	Default value = 0. Set this bit for enabling the two wire interface on the fs_dat and fs_se0 pins

FS1_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
26	ULPI_SER3_NOT6_SEL	ULPI serial 3 bits select. Read/write Read: Current status of serial data bus wide Write: SW writes ’1’ to this bit to request 3 pins ULPI data wide, or ’0’ to request 6 bit data wide in FsLsSerial Mode.
25	SESS_VLD_CTRL	Default value = 0. Set this bit to enable Link Controller operation after switching interface from Serial to ULPI.
24	RESERVED_BIT24	Clear (0) these bit
23:16	ITC_7_0	Interrupt threshold control Read/write Default 08h The system software uses this field to set the maximum rate at which the host/device controller will issue interrupts. This field contains the maximum interrupt interval measured in micro-frames. Valid values are shown below. Value Maximum interrupt interval 00h Immediate (no threshold) 01h 1 micro-frame 02h 2 micro-frames 04h 4 micro-frames 08h 8 micro-frames 10h 16 micro-frames 20h 32 micro-frames 40h 64 micro-frames
15	FS2	This field is Read/Write only if Programmable Frame List Flag in the HCCPARAMS registers is set to one. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index. Note that this field is made up from USBCMD bits 15, 3 and 2. Values meaning 000 1024 elements (4096 bytes) Default value 001 512 elements (2048 bytes) 010 256 elements (1024 bytes) 011 128 elements (512 bytes) 100 64 elements (256 bytes) 101 32 elements (128 bytes) 110 16 elements (64 bytes) 111 8 elements (32 bytes) Only the host controller uses this field.

FS1_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
14	ATDTW	Add dTD tripwire Read/write (Device mode only) This bit is used as a semaphore to ensure the proper addition of a new dTD to an active (primed) endpoint's linked list. This bit is set (1) and cleared (0) by the software. This bit shall also be cleared (0) by the hardware when the state machine is a hazard region for which adding a dTD to a primed endpoint may go unrecognized.
13	SUTW	Setup tripwire (device mode only) Read/write This bit is used as a semaphore to ensure that the setup data payload of 8 bytes is extracted from a QH by the DCD without being corrupted. If the setup lockout mode is off (see USBMODE) then there exists a hazard when new setup data arrives while the DCD is copying the setup data payload from the QH for a previous setup packet. This bit is set (1) and cleared (0) by software, and will be cleared (0) by hardware when a hazard exists.
12	RESERVED_BITS12	Clear (0) this bit
11	ASPE	Asynchronous schedule park mode enable (OPTIONAL) Read/write If the asynchronous park capability (ASP) bit in the HCCPARAMS register is set (1), then this bit defaults to a 1h and is R/W. Otherwise, the bit must be cleared (0) and is RO. The software uses this bit to enable or disable the park mode. value 1 = Park mode is enabled. value 0 = Park mode is disabled. This field is set (1) in this implementation.
10	RESERVED_BIT10	Clear (0) this bit.
9:8	ASP_1_0	Asynchronous schedule park mode count (OPTIONAL) Read/write If the Asynchronous park capability (ASP) bit in the HCCPARAMS register is set (1), then this field defaults to 3h and is R/W. Otherwise it defaults to zero and is RO. This field contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid values are 1h to 3h. The software must not clear (0) this bit when the ASPE bit in this register is set (1), as this will result in undefined behavior. This field is set to 3h in this implementation.
7	LR	Light host/device controller reset (OPTIONAL) Read only Not implemented. This bit will always be clear (0).

FS1_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
6	IAA	Interrupt on async advance doorbell Read/write This bit is used as a doorbell by the software to tell the host controller to issue an interrupt the next time it advances the asynchronous schedule. The software must set (1) this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule states, it sets (1) the interrupt on the async advance status (AAI) bit in the USBSTS register. If the interrupt on async advance enable (AAE) bit in the USBINTR register is set (1), then the host controller will assert an interrupt at the next interrupt threshold. The host controller clears (0) this bit after it has set (1) the interrupt on async advance status (AAI) bit in the USBSTS register. The software should not set (1) this bit when the asynchronous schedule is inactive. Doing so will yield undefined results. This bit is only used in the host mode. Setting (1) this bit when the device mode is selected will produce undefined results.
5	ASE	Asynchronous Schedule Enable Read/write Default = 0b This bit controls whether the host controller skips processing the asynchronous schedule. value 0 = Do not process the asynchronous schedule value 1 = Use the ASYNCLISTADDR register to access the asynchronous schedule. Only the host controller uses this bit.
4	PSE	Periodic schedule enable Read/write Default 0b This bit controls whether the host controller skips processing the periodic schedule. value 0 = Do not process the periodic schedule value 1 = Use the PERIODICLISTBASE register to access the periodic schedule. Only the host controller uses this bit.

FS1_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
3:2	FS_1_0	This field is Read/Write only if Programmable Frame List Flag in the HCCPARAMS registers is set to one. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index. Note that this field is made up from USBCMD bits 15, 3 and 2. Values meaning 000 1024 elements (4096 bytes) Default value 001 512 elements (2048 bytes) 010 256 elements (1024 bytes) 011 128 elements (512 bytes) 100 64 elements (256 bytes) 101 32 elements (128 bytes) 110 16 elements (64 bytes) 111 8 elements (32 bytes) Only the host controller uses this field.
1	RST	Controller reset (RESET) Read/write The software uses this bit to reset the controller. This bit is cleared (0) by the host/device controller when the reset process is complete. The software cannot terminate the reset process early by clearing (0) this bit. Host controller: When the software sets (1) this bit, the host controller resets its internal pipelines, timers, counters, state machines, and so on to their initial values. Any transaction currently in progress on the USB is immediately terminated. A USB reset is not driven on downstream ports. The software should not set (1) this bit when the HCHalted bit in the USBSTS register is clear (0). Attempting to reset an actively running host controller will result in undefined behavior. Device controller: When the software sets (1) this bit, the device controller resets its internal pipelines, timers, counters, state machines, and so on to their initial values. Setting this bit when the device is in the attached state is not recommended, since the effect on an attached host is undefined. In order to ensure that the device is not in an attached state before initiating a device controller reset, all primed endpoints should be flushed and the USBCMD run/stop bit should be cleared (0).

FS1_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
0	RS	Run/stop Read/Write Default 0b value 1 = Run value 0 = Stop Host controller: When this bit is set (1), the host controller proceeds with the execution of the schedule. The host controller continues execution as long as this bit remains set (1). When this bit is clear (0), the host controller completes the current transaction on the USB and then halts. The HC halted bit in the status register indicates when the host controller has finished the transaction and has entered the stopped state. The software should not set (1) this bit unless the host controller is in the halted state (that is, the HCHalted bit in the USBSTS register is set (1)). Device controller: Setting (1) this bit will cause the device controller to enable a pull-up on D+ and initiate an attach event. This control bit is not directly connected to the pull-up enable, as the pull-up will become disabled upon transitioning into high-speed mode. The software should use this bit to prevent an attach event before the device controller has been properly initialized. Clearing (0) this bit will cause a detach event.

0x18000144 FS1_USB_OTG_HS_USBSTS

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_USBSTS register is the USB status register. This register indicates various states of the host/device controller and any pending interrupts. This register does not indicate status resulting from a transaction on the serial bus. The software clears certain bits in this register by setting (1) them.

FS1_USB_OTG_HS_USBSTS

Bits	Name	Description
31	ULPI_INTR	Default value = 0.This bit is set when Interrupt during ULPI -Serial mode or ULPI Interrupt during LPM occurs. Writing a 1 to this bit will clear it.
30	PHY_SESS_VLD_CHG	This bit is set when PHY_SESS_VLD bit changes its value.
29	PHY_SESS_VLD	This bit presents the SESS_VLD status of PHY.

FS1_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
28	PHY_ALT_INT	This bit is asserted when a non-USB interrupt from PHY is detected. This interrupt is used for procedures like Battery Charging. This bit is set when bit 7 (alt_int) of RX CMD is high. Writing a 1 to this bit will clear it.
27:26	RESERVED_BITS27_26	Clear (0) these bits.
25	TI1	General purpose timer interrupt 1 (GPTINT1) Read/write control This bit is set (1) when the counter in the GPTIMER1CTRL (non-EHCI) register transitions to zero. Setting (1) this bit will clear it.
24	TI0	General purpose timer interrupt 0 (GPTINT0) Read/write control This bit is set (1) when the counter in the GPTIMER0CTRL (non-EHCI) register transitions to zero. Setting (1) this bit will clear it.
23:20	RESERVED_BITS23_20	Clear (0) these bits.
19	UPI	USB host periodic interrupt (USBHSTPERINT) Read/write control This bit is set (1) by the host controller when the cause of an interrupt is a completion of a USB transaction, where the transfer descriptor (TD) has an interrupt on complete (IOC) bit set (1) and the TD was from the periodic schedule. This bit is also set (1) by the host controller when a short packet is detected AND the packet is on the periodic schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes. This bit is not used by the device controller and will always be clear (0).
18	UAI	USB host asynchronous interrupt (USBHSTASYNCINT) Read/write control This bit is set (1) by the host controller when the cause of an interrupt is a completion of a USB transaction, where the transfer descriptor (TD) has an interrupt on complete (IOC) bit set AND the TD was from the asynchronous schedule. This bit is also set (1) by the host when a short packet is detected AND the packet is on the asynchronous schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes. This bit is not used by the device controller and will always be clear (0).
17	RESERVED_BIT17	Clear (0) these bits.
16	NAKI	NAK interrupt bit Read only This bit is set (1) by the hardware when, for a particular endpoint, both the Tx/Rx endpoint NAK bit and the corresponding Tx/Rx endpoint NAK enable bit are set (1). This bit is automatically cleared (0) by the hardware when all of the enabled Tx/Rx endpoint NAK bits are cleared (0).

FS1_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
15	AS	Asynchronous schedule status Read only Default = 0 This bit reports the current real status of the asynchronous schedule. When cleared (0), the asynchronous schedule status is disabled. And, if set (1), the status is enabled. The host controller is not required to immediately disable or enable the asynchronous schedule when software transitions the asynchronous schedule enable bit in the USBCMD register. When this bit and the asynchronous schedule enable bit are the same value, the asynchronous schedule is either enabled (1) or disabled (0). This bit is only used by the host controller.
14	PS	Periodic schedule status Read only Default = 0 This bit reports the current real status of the periodic schedule. When cleared (0), the periodic schedule is disabled. And, if set (1), the status is enabled. The host controller is not required to immediately disable or enable the periodic schedule when software transitions the periodic schedule enable bit in the USBCMD register. When this bit and the periodic schedule enable bit are the same value, the periodic schedule is either enabled (1) or disabled (0). This bit is only used by the host controller.
13	RCL	Reclamation Read only Default = 0 This is a read-only status bit that is used to detect an empty asynchronous schedule. This bit is only used by the host controller.
12	HCH	HC halted Read only Default = 1 This bit is a clear (0) whenever the run/stop bit is set (1). The host controller sets (1) this bit after it has stopped executing, because of the run/stop bit being cleared (0), either by the software or by the host controller hardware (for example, an internal error). This bit is only used by the host controller.
11	RESERVED_BIT11	Clear (0) this bit.
10	ULPII	ULPI interrupt Read/write control Default = 0 When the ULPI viewport is present in the design, an event completion will set (1) this interrupt. This bit is used by both the host and device controllers. It is only present in designs where the configuration constant VUSB_HS_PHY_ULPI = 1.

FS1_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
9	RESERVED_BIT9	Clear (0) this bit.
8	SLI	DC suspend Read/write control Default = 0 When a device controller enters a suspend state from an active state, this bit will be set (1). The device controller clears (0) the bit upon exiting from a suspend state. This bit is only used by the device controller.
7	SRI	SOF received Read/write control Default = 0 When the device controller detects a start of (micro) frame, this bit will be set (1). When a SOF is extremely late, the device controller will automatically set (1) this bit to indicate that an SOF was expected. Therefore, this bit will be set (1) roughly every 1 ms in the device FS mode and every 125 ms in the HS mode, and will be synchronized to the actual SOF that is received. Since the device controller is initialized to FS before connect, this bit will be set (1) at an interval of 1 ms during the prelude to connect and chirp. In the host mode, this bit will be set (1) every 125 us and can be used by the host controller driver as a time base. The software writes a 1 to this bit to clear it. This is a non-EHCI status bit.
6	URI	USB reset received Read/write control Default = 0 When the device controller detects a USB reset and enters the default state, this bit will be set (1). The software can set (1) this bit to clear the USB reset received status bit. This bit is only used by the device controller.
5	AAI	Interrupt on async advance Read/write control Default = 0 The system software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by setting (1) the interrupt on async advance doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source. This bit is only used by the host controller.
4	SEI	System error Read/write control This interrupt is triggered when there is an AHB error (HRESP = ERROR) on the AHB Master interface.

FS1_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
3	FRI	Frame list rollover Read/write control The host controller sets (1) this bit when the frame list index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the frame list size field of the USBCMD register) is 1024, the frame index register rolls over every time FRINDEX [1 3] toggles. Similarly, if the size is 512, the host controller sets (1) this bit to a one every time FHINDEX [12] toggles. This bit is only used by the host controller.
2	PCI	Port change detect Read/write control The host controller sets (1) this bit when a connect status occurs on any port, a port enable/disable change occurs on any port, or the force port resume bit is set (1) as the result of a J-K transition on the suspended port. The device controller sets (1) this bit when the port controller enters the full or high-speed operational state. When the port controller exits the full or high-speed operation states due to reset or suspend events, the notification mechanisms are the USB reset received bit and the DC suspend bits, respectively. This bit is not EHCI compatible.
1	UEI	USB error interrupt (USBERRINT) Read/write control When completion of a USB transaction results in an error condition, this bit is set (1) by the host/device controller. This bit is set (1) along with the USBINT bit, if the TD on which the error interrupt occurred also had its interrupt-on-complete (IOC) bit set (1). The device controller detects resume signaling only.
0	UI	USB interrupt (USBINT) Read/write control This bit is set (1) by the host/device controller when the cause of an interrupt is a completion of a USB transaction where the transfer descriptor (TD) has an interrupt-on-complete (IOC) bit set (1). This bit is also set (1) by the host/device controller when a short packet is detected. A short packet is when the actual number of bytes received was less than the expected number of bytes.

0x18000148 FS1_USB_OTG_HS_USBINTR

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_USBINTR register is the USB interrupt enable register. The interrupts to the software are enabled with this register. An interrupt is generated when a bit is set (1) and the corresponding interrupt is active. The USB status register (USBSTS) still shows interrupt sources, even if they are disabled by the USBINTR register, which allows polling of interrupt events by the software.

FS1_USB_OTG_HS_USBINTR

Bits	Name	Description
31	ULPI_INTR_EN	Default value =0.When this bit is a 1 and ULPI_INTR is a 1, the controller will issue an interrupt. The interrupt is acknowledged by software clearing the ULPI_INTR bit.
30	PHY_SESS_VLD_CHG_EN	Default value =0. When this bit is set then Link Controller will issue an interrupt when PHY_SESS_VLD changes its value.
29:26	RESERVED_BITS29_26	Clear (0) these bits.
25	TIE1	General purpose timer interrupt enable 1 When this bit is set (1), and the GPTINT1 bit in the USBSTS register is set (1), the controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the GPTINT1 bit.
24	TIE0	General purpose timer interrupt enable 0 When this bit is set (1), and the GPTINT0 bit in the USBSTS register is set (1), the controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the GPTINT0 bit.
23:20	RESERVED_BITS23_20	Clear (0) these bits.
19	UPIE	USB host periodic interrupt enable When this bit is set (1), and the USBHSTPERINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBHSTPERINT bit.
18	UAIE	USB host asynchronous interrupt enable When this bit is set (1), and the USBHSTASYNCINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBHSTASYNCINT bit.
17	RESERVED_BIT17	Clear (0) this bit.
16	NAKE	NAK interrupt enable This bit is set (1) by the software if it wants to enable the hardware interrupt for the NAK interrupt bit. If both this bit and the corresponding NAK interrupt bit are set (1), a hardware interrupt is generated.
15:11	RESERVED_BITS15_11	Clear (0) these bits.

FS1_USB_OTG_HS_USBINTR (cont.)

Bits	Name	Description
10	ULPIE	ULPI enable When this bit is set (1), and the ULPI Interrupt bit in the USBSTS register transitions, the controller will issue and interrupt. The interrupt is acknowledged by the software setting (1) the ULPI interrupt bit. This bit is used by both the host and device controllers. It is only present in designs where configuration constant VUSB_HS_PHY_ULPI = 1.
9	RESERVED_BIT9	Clear (0) this bit.
8	SLE	Sleep enable When this bit is set (1) and the DC suspend bit in the USBSTS register transitions, the device controller will issue an interrupt. The interrupt is acknowledged by the software setting (1) the DC suspend bit. This bit is only used by the device controller.
7	SRE	SOF received enable When this bit is set (1) and the SOF received bit in the USBSTS register is set (1), the device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the SOF received bit.
6	URE	USB reset enable When this bit is set (1) and the USB reset received bit in the USBSTS register is set (1), the device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the USB reset received bit.
5	AAE	Interrupt on async advance enable When this bit is set (1) and the interrupt on async advance bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the interrupt on async advance bit. This bit is only used by the host controller.
4	SEE	System error enable When this bit is set (1) and the system error bit in the USBSTS register is set (1), the host/device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the system error bit.
3	FRE	Frame list rollover enable When this bit is set (1) and the frame list rollover bit in the USBSTS register is set (1), the host controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the frame list rollover bit. This bit is only used by the host controller.

FS1_USB_OTG_HS_USBINTR (cont.)

Bits	Name	Description
2	PCE	Port change detect enable When this bit is set (1) and the port change detect bit in the USBSTS register is set (1), the host/device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the port change detect bit.
1	UEE	USB error interrupt enable When this bit is set (1) and the USBERRINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBERRINT bit in the USBSTS register.
0	UE	USB interrupt enable When this bit is set (1) and the USBINT bit in the USBSTS register is set (1), the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBINT bit.

0x1800014C FS1_USB_OTG_HS_FRINDEX

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_FRINDEX register is the USB frame index register. This register is used by the host controller to index the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits [N:3] are used to select a particular entry in the periodic frame list during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by the system software in the frame list size field in the USBCMD register.

This register must be written as a DWord. Byte writes produce-undefined results. This register cannot be written unless the host controller is in the 'halted' state, as indicated by the HC halted bit. A write to this register while the run/stop bit is set (1) produces undefined results. Writes to this register also affect the SOF value.

In the device mode, this register is read-only and the device controller updates the FRINDEX [13:3] register from the frame number indicated by the SOF marker. Whenever a SOF is received by the USB bus, FRINDEX [13:3] will be checked against the SOF marker. If FRINDEX [13:3] is different from the SOF marker, FRINDEX [13:3] will be set to the SOF value and FRINDEX [2:0] will be cleared (0) (that is, SOF for a 1-ms frame). If FRINDEX [13:3] is equal to the SOF value, FRINDEX [2:0] will be incremented (that is, SOF for 125-ms micro-frame.

FS1_USB_OTG_HS_FRINDEX

Bits	Name	Description
31:14	RESERVED_BITS31_14	Clear (0) these bits.

FS1_USB_OTG_HS_FRINDEX (cont.)

Bits	Name	Description
13:0	FRINDEX_13_0	Frame index The value in this register increments at the end of each time frame (for example, a micro-frame). Bits [N:3] are used for the frame list current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. The following data shows the values of N based on the value of the frame list size field in the USBCMD register when used in host mode. USBCMD [Frame list size] number Elements N 000b (1024) 12 001b (512) 11 010b (256) 10 011b (128) 9 100b (64) 8 101b (32) 7 110b (16) 6 111b (8) 5 In the device mode, the value is the current frame number of the last frame transmitted. It is not used as an index. In either mode, bits 2:0 indicate the current microframe.

0x18000154 FS1_USB_OTG_HS_PERIODICLISTBASE

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_PERIODICLISTBASE register is the periodic list base address register. This 32-bit register contains the beginning address of the periodic frame list in the system memory. The HCD loads this register prior to starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the frame index register (FRINDEX) to enable the host controller to step through the periodic frame list in sequence.

NOTE This device is shared between the host controller and device controller operation. For host controller operation, this is the USB_OTG_HS_ PERIODICLISTBASE register. For device controller operation, this is the USB_OTG_HS_DEVICEADDR register.

FS1_USB_OTG_HS_PERIODICLISTBASE

Bits	Name	Description
31:12	PERBASE_31_12	Base address (low) These bits correspond to memory address signals [31:12], respectively. Only used by the host controller.
11:0	RESERVED_BITS11_0	This field must be written as zeros. During runtime, the values of these bits are undefined.

0x18000154 FS1_USB_OTG_HS_DEVICEADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_DEVICEADDR register is the USB device address register. The upper seven bits of this register represent the device address. After any controller reset or a USB reset, the device address is set to the default address (0). The default address will match all incoming addresses. The software shall reprogram the address after receiving a SET_ADDRESS descriptor.

The USBADRA is used to accelerate the SET_ADDRESS sequence by allowing the DCD to preset the USBADR register before the status phase of the SET_ADDRESS descriptor.

NOTE This device is shared between the host controller and device controller operations. For host controller operation, this is the USB_OTG_HS_ PERIODICLISTBASE register. For device controller operation, this is the USB_OTG_HS_DEVICEADDR register.

FS1_USB_OTG_HS_DEVICEADDR

Bits	Name	Description
31:25	USBADR_31_25	Device address These bits correspond to the USB device address.

FS1_USB_OTG_HS_DEVICEADDR (cont.)

Bits	Name	Description
24	USBADRA	Device address advance Default = 0 When this bit is clear (0), any writes to USBADR are instantaneous. When this bit is set (1) at the same time or before USBADR is written, the write to the USBADR field is staged and held in a hidden register. After an IN occurs on endpoint 0 and is ACKed, USBADR will be loaded from the holding register. The hardware will automatically clear (0) this bit on the following conditions: 1. IN is ACKed to endpoint 0 (USBADR is updated from staging register). 2. OUT/SETUP occur to endpoint 0 (USBADR is not updated). 3. Device reset occurs (USBADR is reset to 0). Note: After the status phase of the SET_ADDRESS descriptor, the DCD has 2 ms to program the USBADR field. This mechanism will ensure this specification is met when the DCD can not write of the device address within 2 ms from the SET_ADDRESS status phase. If the DCD writes the USBADR with USBADRA = 1 after the SET_ADDRESS data phase (before the prime of the status phase), the USBADR will be programmed instantly at the correct time and meet the 2-ms USB requirement.
23:0	RESERVED_BITS23_0	These bits must be written as zeros. During runtime, the values of these bits are undefined.

0x18000158 FS1_USB_OTG_HS_ASYNCLISTADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ASYNCLISTADDR register is the next asynchronous list address register. This 32-bit register contains the address of the next asynchronous queue head to be executed by the host. Bits [4:0] of this register cannot be modified by the system software and will always return a zero when read.

NOTE The USB_OTG_HS_ASYNCLISTADDR register and the USB_OTG_HS_ENDPOINTLISTADDR register are shared between the host controller and device controller operations. For the host controller, this is the USB_OTG_HS_ASYNCLISTADDR register. For the device controller, this is the USB_OTG_HS_ENDPOINTLISTADDR register.

FS1_USB_OTG_HS_ASYNCLISTADDR

Bits	Name	Description
31:5	ASYBASE_31_15	Link pointer low (LPL). These bits correspond to memory address signals [31:5], respectively. This field may only reference a queue head (OH). This field is only used by the host controller.
4:0	RESERVED_BITS4_0	The values of these bits has no effect on circuit operation.

0x18000158 FS1_USB_OTG_HS_ENDPOINTLISTADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPOINTLISTADDR register is the endpointlist address register. In the device mode, this register contains the address of the top of the endpoint list in system memory. Bits [10:0] of this register cannot be modified by the system software and will always return a zero when read.

NOTE The USB_OTG_HS_ASYNCLISTADDR register and the USB_OTG_HS_ENDPOINTLISTADDR register are shared between the host controller and device controller operations. For the host controller, this is the USB_OTG_HS_ASYNCLISTADDR register. For the device controller, this is the USB_OTG_HS_ENDPOINTLISTADDR register.

FS1_USB_OTG_HS_ENDPOINTLISTADDR

Bits	Name	Description
31:11	EPBASE_31_11	Endpoint list pointer (low) These bits correspond to memory address signals [31:11], respectively. This field will reference a list of up to 32 queue heads (QH). That is, one queue head per endpoint & direction.
10:0	RESERVED_BITS10_0	The values of these bits has no effect on circuit operation.

0x1800015C FS1_USB_OTG_HS_TTCTRL

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_TTCTRL register is the TT status and control register. This register contains parameters needed for internal TT operations.

NOTE This register is not used in the device controller operation.

FS1_USB_OTG_HS_TTCTRL

Bits	Name	Description
31	RESERVED_BIT31	Not used.
30:24	TTHA	Not used.
23:0	RESERVED_BITS23_0	Not used.

0x18000160 FS1_USB_OTG_HS_BURSTSIZE

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1010

The USB_OTG_HS_BURSTSIZE register is the programmable burst size register. This register is used to control dynamically change the burst size used during data movement on the initiator (master) interface.

FS1_USB_OTG_HS_BURSTSIZE

Bits	Name	Description
31:16	RESERVED_BITS31_16	The value of these bits has no effect on circuit operation.
15:8	TXPBURST	Programmable Tx burst length This register represents the maximum length of a the burst in 32-bit words while moving data from system memory to the USB bus.
7:0	RXPBURST	Programmable Rx burst length This register represents the maximum length of a the burst in 32-bit words while moving data from the USB bus to system memory.

0x18000164 FS1_USB_OTG_HS_TXFILLTUNING

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_TXFILLTUNING register is the host transmit pre-buffer packet tuning register. The fields in this register control performance tuning associated with how the host controller posts data to the Tx latency FIFO before moving the data onto the USB bus. The specific areas of performance include the how much data to post into the FIFO and an estimate for how long that operation should take in the target system.

Definitions:

T0 = Standard packet overhead

T1 = Time to send data payload

Tff = Time to fetch packet into TX FIFO up to specified level.

Ts = Total packet flight time (send-only) packet

Ts = T0 + T1

Tp = Total packet time (fetch and send) packet

Tp = Tff + T0 + T1

Upon discovery of a transmit (OUT/SETUP) packet in the data structures, the host controller checks to ensure Tp remains before the end of the [micro] frame. If so it proceeds to pre-fill the TX FIFO. If at anytime during the pre-fill operation the time remaining the [micro] frame is < Ts, then the packet attempt ceases and the packet is tried at a later time. Although this is not an error condition and the host controller will eventually recover, a mark will be made the scheduler health counter to note the occurrence of a ’back-off’ event. When a back-off event is detected, the partial packet fetched may need to be discarded from the latency buffer to make room for periodic traffic that will begin after the next SOF. Too many back-off events can waste bandwidth and power on the system bus, and thus should be minimized (not necessarily eliminated). Back-offs can be minimized with use of the TSCHHEALTH (Tff), as described in the register table.

FS1_USB_OTG_HS_TXFILLTUNING

Bits	Name	Description
31:22	RESERVED_BITS31_22	The value of these bits has no effect on circuit operation.
21:16	TXFIFOTHRES	FIFO burst threshold Default = 2 This register controls the number of data bursts that are posted to the TX latency FIFO in the host mode before the packet begins on to the bus. The minimum value is 2 and this value should be a low as possible to maximize USB performance. A higher value can be used in systems with unpredictable latency and/or insufficient bandwidth, where the FIFO may underrun because the data transferred from the latency FIFO to USB occurs before it can be replenished from system memory. This value is ignored if the stream disable bit in USBMODE register is set (1).
15:13	RESERVED_BITS15_13	The value of these bits has no effect on circuit operation.

FS1_USB_OTG_HS_TXFILLTUNING (cont.)

Bits	Name	Description
12:8	TXSCHHEALTH	Scheduler health counter Read/write to clear Default = 0 This register increments when the host controller fails to fill the Tx latency FIFO to the level programmed by TXFIFOTHRES before running out of time to send the packet before the next start-of-frame. This health counter measures the number of times this occurs to provide feedback to selecting a proper TXSCHOH. Writing to this register will clear the counter and this counter will be at a maximum at 31.
7:0	TXSCHOH	Scheduler overhead Default = 0 This register adds an additional fixed offset to the schedule time estimator described above as Tff. As an approximation, the value chosen for this register should limit the number of back-off events captured in the TXSCHHEALTH to less than 10 per second in a highly-utilized bus. Choosing a value that is too high for this register is not desired, as it can needlessly reduce USB utilization. The time unit represented in this register is 1.267 ms when a device is connected in the high-speed mode for OTG and SPH. The time unit represented in this register is 6.333 ms when a device is connected in the low/full speed mode for OTG and SPH. The time unit represented in this register is always 1.267 times the MPH product.

0x18000170 FS1_USB_OTG_HS_ULPI_VIEWPORT

Type: Read/write (unless otherwise indicated)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x08000000

The USB_OTG_HS_ULPI_VIEWPORT register provides indirect access to the ULPI PHY register set. Although the core performs access to the ULPI PHY register set, there may be extraordinary circumstances where software may need direct access.

CAUTION Writes to the ULPI through the viewport can substantially harm standard USB operations. Currently, no usage model has been defined where the software should need to execute writes directly to the ULPI - see the exception regarding optional features below.

Executing read operations though the ULPI viewport should have no harmful side effects to standard USB operations.

NOTE The ULPI viewport is only synthesized in the design if the constant VUSB_HS_PHY_ULPI is set (1). If the ULPI interface is not enabled, this register will always read zeros.

Two operations can be performed with the ULPI viewport: wake-up and read/write operations. The wake-up operation is used to put the ULPI interface into normal operation mode and re-enable the clock, if necessary. A wake-up operation is required before accessing the registers when the ULPI interface is operating in the low power mode, serial mode, or car kit mode.

The ULPI state can be determined by reading the sync state bit (ULPISS). If this bit is set (1), then the ULPI interface is running in the normal operation mode and can accept read/write operations. If the ULPISS is clear (0), then read/write operations will not be able to execute. Undefined behavior will result if ULPISS = 0, and a read or write operation is performed.

To execute a wake-up operation, write all 32-bits of the ULPI Viewport where ULPIPORT is constructed appropriately, and the ULPIWU bit is set (1) and the ULPIRUN bit is clear (0). Poll the ULPI viewport until ULPIWU is zero for the operation to complete.

To execute a read or write operation, write all 32-bits of the ULPI viewport where ULPIDATWR, ULPIADDR, ULPIPORT, and ULPIRW are constructed appropriately, and the ULPIRUN bit is set (1). Poll the ULPI viewport until ULPIRUN is zero for the operation to complete. Once ULPIRUN is zero, the ULPIDATRD will be valid if the operation was a read.

The polling method above could also be replaced and an interrupt driven using the ULPI interrupt defined in the USBTS and USBINTR registers. When a wake-up or read/write operation completes, the ULPI interrupt will be set (1).

Several optional features may need to be enabled or disabled by the system software as part of system configuration. These bits are contained in the interface and OTG control registers of the ULPI PHY register set. These registers also contain bits that are controlled by the link dynamically and, therefore, should only be modified by the system software using the set/clear access method. Direct writes to these registers could have harmful side effects to the standard USB operations. The following bits are optional bits:

- Bits 3 through 7 in the interface control register
- Bits 6 and 7 in the OTG control register.

For more information on the use of the optional features, see http://www.ulpi.org/documents.html.

FS1_USB_OTG_HS_ULPI_VIEWPORT

Bits	Name	Description
31	ULPIWU	ULPI wake-up Setting (1) this bit begins the wake-up operation. The bit will automatically transition to 0 after the wake-up is complete. Once this bit is set (1), the driver can not clear it back to 0. Note: The driver must never execute a wake-up and a read/write operation at the same time.
30	ULPIRUN	ULPI read/write run Setting (1) this bit will begin the read/write operation. The bit will automatically transition to 0 after the read/write is complete. Once this bit is set (1), the driver can not clear it back to 0. Note: The driver must never execute a wakeup and a read/write operation at the same time.

FS1_USB_OTG_HS_ULPI_VIEWPORT (cont.)

Bits	Name	Description
29	ULPIRW	ULPI read/write control This bit selects between running a read or write operation. value 0 = Read value 1 = Write
28	ULPIFORCE	ULPI read/write force This bit enables forcing register access during RX packet value 0 = register access is not forced during RX packet (default) value 1 = register access is forced during RX packet reception
27	ULPISS	ULPI sync state Read Only value 1 = Normal sync state value 0 = In another state (for example, car kit, serial, low power) This bit represents the state of the ULPI interface. Before reading this bit, the ULPIPORT field should be set accordingly if used with the multi-port host. Otherwise, this field should always remain 0.
26:24	ULPIPORT	ULPI port number For the wakeup or read/write operation to be executed, this value selects the port number the ULPI PHY is attached to in the multi-port host. The valid range is 0 to 7. This field should always be written as a 0 for the non-multi port products.
23:16	ULPIADDR	ULPI data address When a read or write operation is commanded, the address of the operation is written to this field.
15:8	ULPIDATRD	ULPI data read Read only After a read operation completes, the result is placed in this field.
7:0	ULPIDATWR	ULPI data write When a write operation is commanded, the data to be sent is written to this field.

0x18000178 FS1_USB_OTG_HS_ENDPTNAK

Type: Read/write clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTNAK register is the endpoint NAK register.

FS1_USB_OTG_HS_ENDPTNAK

Bits	Name	Description
31:16	EPTN_15_0	Tx endpoint NAK Each tx endpoint has 1 bit in this field. The bit is set (1) when the device sends a NAK handshake on a received IN token for the corresponding endpoint. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0
15:0	EPRN_15_0	Rx endpoint NAK Each rx endpoint has 1 bit in this field. The bit is set (1) when the device sends a NAK handshake on a received OUT or PING token for the corresponding endpoint. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x1800017C FS1_USB_OTG_HS_ENDPTNAKEN

Type: Read/write clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTNAKEN register is the endpoint NAK enable register.

FS1_USB_OTG_HS_ENDPTNAKEN

Bits	Name	Description
31:16	EPTNE_15_0	Tx endpoint NAK enable Each bit is an enable bit for the corresponding Tx endpoint NAK bit. If this bit is set (1) and the corresponding Tx endpoint NAK bit is set (1), the NAK Interrupt bit is set (1). Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0
15:0	EPRNE_15_0	Rx endpoint NAK enable Each bit is an enable bit for the corresponding Rx endpoint NAK bit. If this bit is set (1) and the corresponding Rx endpoint NAK bit is set (1), the NAK Interrupt bit is set (1). Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x18000184 FS1_USB_OTG_HS_PORTSC

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xCC000004

This is the USB_OTG_HS_PORTSC register.

FS1_USB_OTG_HS_PORTSC

Bits	Name	Description
31:30	PTS	Parallel transceiver select Read/write This register bit pair is used in conjunction with the configuration constant VUSB_HS_PHY_TYPE to control which parallel transceiver interface is selected. If VUSB_HS_PHY_ TYPE is set for 0, 1, 2, or 3, then this bit is read only. If VUSB_HS_PHY_TYPE is 4, 5, 6, or 7, then this bit is read/write. This field is reset to the following values: 00 if VUSB_HS_PHY_TYPE = 0,4 - UTMI/UTMI+ 01 if VUSB_HS_PHY_TYPE = 1,5 - Reserved 10 if VUSB_HS_PHY_TYPE = 2,6 - ULPI 11 if VUSB_HS_PHY_TYPE = 3,7 - Serial/1.1 PHY (FS only) This bit is not defined in the EHCI specification.
29	STS	Serial transceiver select Read/write This register bit is used in conjunction with the configuration constant VUSB_HS_PHY_SERIAL to control whether the parallel or serial transceiver interface is selected for FS and LS operation. The serial interface engine can be used in combination with the UTMI+ or ULPI physical interface to provide FS/LS signaling instead of the parallel interface. ’ If VUSB_HS_PHY_SERIAL is 0 or 1, then this bit is read only. ’ If VUSB_HS_PHY_SERIAL is 2 or 3, then this bit is read/write. This bit has no effect unless the parallel transceiver select is set to UTMI+ or ULPI. The Serial/1.1 physical interface will use the serial interface engine for FS/LS signaling regardless of this bit value. Note: This bit was reserved for future operation, and is now adding for dynamic use of the serial engine in accord with UMTI+ and ULPI characterization logic. This bit is not defined in the EHCI specification.

FS1_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
28	PTW	Parallel transceiver width Read/write This register bit is used in conjunction with the configuration constant VUSB_HS_PHY16_8 to control the data bus width of the UTMI transceiver interface. ' If VUSB_HS_PHY16_8 is 0 or 1, then this bit is read only. ' If VUSB_HS_PHY16_8 is 2 or 3, then this bit is read/write. This bit is reset to 1 if VUSB_HS_PHY16_8 selects a default UTMI interface width of 16-bits, else it is reset to 0. ' Writing this bit to 0 selects the 8-bit [60MHz] UTMI interface. ' Writing this bit to 1 selects the 16-bit [30MHz] UTMI interface. This bit has no effect if the serial interface is selected. This bit is not defined in the EHCI specification.
27:26	PSPD	Port speed Read only This register field indicates the speed at which the port is operating. For HS mode operation in the host controller and HS/FS operation in the device controller, the port routing steers data to the protocol engine. For FS and LS mode operation in the host controller, the port routing steers data to the protocol engine with the embedded transaction translator. value 00 = Full speed value 01 = Low speed value 10 = High speed This bit is not defined in the EHCI specification.
25	SPRT	Short Port Reset Time. shortens port reset time for simulation.
24	PFSC	Port force full speed connect Read/write Default = 0 Setting (1) this bit will force the port to only connect at full speed. It also disables the chirp sequence that allows the port to identify itself as high speed. This is useful for testing FS configurations with a HS host, hub or device. This bit is not defined in the EHCI specification. This bit is for debugging purposes.

FS1_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
23	PHCD	PHY low power suspend - clock disable (PLPSCD) Read/write Default = 0 value 1 = Disable the PHY clock. value 0 = Enable the PHY clock. Reading this bit will indicate the status of the PHY clock. Note: The PHY clock cannot be disabled if it is being used as the system clock. In the device mode, The PHY can be put into low power suspend - clock disable when the device is not running (USBCMD run/stop = 0) or the host has signaled suspend (PORTSC SUSPEND = 1). Low power suspend will be cleared automatically when the host has signaled resume. Before forcing a resume from the device, the device controller driver must clear this bit. In the host mode, the PHY can be put into low power suspend - clock disable when the downstream device has been put into the suspend mode or when no downstream device is connected. Low power suspend is completely under the control of the software. This bit is not defined in the EHCI specification.
22	WKOC	Wake on over-current enable (WKOC_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to over-current conditions as wake-up events. This bit is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0). This bit is output from the controller as signal pwrctl_wake_ ovrcurr_en (OTG/host core only) for use by an external power control circuit.
21	WKDS	Wake on disconnect enable (WKDSCNNT_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to device disconnects as wake-up events. This field is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0) or in the device mode. This bit is output from the controller as signal pwrctl_wake_ dscnnt_en (OTG/host core only) for use by an external power control circuit.

FS1_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
20	WKCN	Wake on connect enable (WKCNNT_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to device connects as wake-up events. This field is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0) or in the device mode. This bit is output from the controller as signal pwrctl_wake_ dscnnt_en (OTG/host core only) for use by an external power control circuit.

FS1_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
19:16	PTC_3_0	Port test control Read/write Default = 0000 Any other value than zero indicates that the port is operating in the test mode. Value Specific test The FORCE_ENABLE_FS and FORCE ENABLE_LS tests are extensions to the test mode support, as specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. Note: Low speed operations are not supported as a peripheral device. 0x0: TEST_MODE_DISABLE 0x1: J_ STATE 0x8: K_STATE 0x9: SE0 (host / NAK device) 0x40: Packet 0x41: FORCE_ENABLE_HS 0x48: FORCE_ENABLE_FS 0x49: FORCE_ENABLE_LS 0x3E8: Reserved_1 0x3E9: Reserved_2 0x3EA: Reserved_3 0x3EB: Reserved_4 0x3EC: Reserved_5 0x3ED: Reserved_6 0x3EE: Reserved_7 0x3EF: Reserved_8 0x3F0: Reserved_9 0x3F1: Reserved_10 0x3F2: Reserved_11 0x3F3: Reserved_12 0x3F4: Reserved_13 0x3F5: Reserved_14 0x3F6: Reserved_15 0x3F7: Reserved_16 0x3F8: Reserved_17 0x3F9: Reserved_18 0x3FA: Reserved_19 0x3FB: Reserved_20 0x3FC: Reserved_21 0x3FD: Reserved_22 0x3FE: Reserved_23 0x3FF: Reserved_24 0x400: Reserved_25 0x401: Reserved_26 0x402: Reserved_27 0x403: Reserved_28 0x404: Reserved_29 0x405: Reserved_30 0x406: Reserved_31 0x407: Reserved_32 0x408: Reserved_33 0x409: Reserved_34 0x40A: Reserved_35 0x40B: Reserved_36 0x40C: Reserved_37 0x40D: Reserved_38 0x40E: Reserved_39 0x40F: Reserved_40 0x410: Reserved_41 0x411: Reserved_42

FS1_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
		0x412: Reserved_43 0x413: Reserved_44 0x414: Reserved_45 0x415: Reserved_46 0x416: Reserved_47 0x417: Reserved_48 0x418: Reserved_49 0x419: Reserved_50 0x41A: Reserved_51 0x41B: Reserved_52 0x41C: Reserved_53 0x41D: Reserved_54 0x41E: Reserved_55 0x41F: Reserved_56 0x420: Reserved_57 0x421: Reserved_58 0x422: Reserved_59 0x423: Reserved_60 0x424: Reserved_61 0x425: Reserved_62 0x426: Reserved_63 0x427: Reserved_64 0x428: Reserved_65 0x429: Reserved_66 0x42A: Reserved_67 0x42B: Reserved_68 0x42C: Reserved_69 0x42D: Reserved_70 0x42E: Reserved_71 0x42F: Reserved_72 0x430: Reserved_73 0x431: Reserved_74 0x432: Reserved_75 0x433: Reserved_76 0x434: Reserved_77 0x435: Reserved_78 0x436: Reserved_79 0x437: Reserved_80 0x438: Reserved_81 0x439: Reserved_82 0x43A: Reserved_83 0x43B: Reserved_84 0x43C: Reserved_85 0x43D: Reserved_86 0x43E: Reserved_87 0x43F: Reserved_88 0x440: Reserved_89 0x441: Reserved_90 0x442: Reserved_91 0x443: Reserved_92 0x444: Reserved_93 0x445: Reserved_94 0x446: Reserved_95 0x447: Reserved_96 0x448: Reserved_97 0x449: Reserved_98 0x44A: Reserved_99 0x44B: Reserved_100 0x44C: Reserved_101 0x44D: Reserved_102 0x44E: Reserved_103 0x44F: Reserved_104 0x450: Reserved_105 0x451: Reserved_106 0x452: Reserved_107 0x453: Reserved_108 0x454: Reserved_109 0x455: Reserved_110 0x456: Reserved_111 0x457: Reserved_112

FS1_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
15:14	PIC_1_0	Port indicator control Read/write Default = 0 Writing to this field has no effect if the P_INDICATOR bit in the HCSPARAMS register is a zero. If the P_INDICATOR bit is set (1), then this field has the following meanings: Bit value Meaning value 00 Port indicators are off value 01 Amber value 10 Green value 11 Undefined Refer to the USB Specification Revision 2.0 [3] for a description on how these bits are to be used. This field is output from the controller as signals port_ind_ctl_1 and port_ind_ctl_0 for use by an external LED driving circuit.
13	PO	Port owner Read only Port owner hand-off is not implemented in this design, therefore this bit will always read back as clear (0). Default = 0 The EHCI definition is include here for reference: ’ This bit unconditionally goes clear (0) when the configured bit in the CONFIGFLAG register makes a 0-to-1 transition. ’ This bit unconditionally goes set (1) whenever the configured bit is clear (0). The system software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). The software sets (1) this bit when the attached device is not a high-speed device. When this bit is set (1), it indicates that an internal companion controller owns and controls the port.

FS1_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
12	PP	Port power (PP) Read/write or read-only The function of this bit depends on the value of the port power switching (PPC) field in the HCSPARAMS register. ’ PPC = 0: PP is read-only. A device controller with no OTG capability does not have port power control switches. ’ PPC = 1: PP is read/write. The host/OTG controller requires port power control switches. This bit represents the current setting of the switch (0 = off, 1 = on). When power is not available on a port (and PP equals a 0), the port is non-functional and will not report attaches, detaches, and so on. When an over-current condition is detected on a powered port and PPC is set (1), the PP bit in each affected port may be transitioned by the host controller driver from a one to a zero, removing power from the port. This feature is implemented in the host/OTG controller (PPC = 1). In a device-only implementation, port power control is not necessary. So, PPC and PP = 0.
11:10	LS_1_0	Line status Read-only These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines: Value Meaning value 00 SE0 value 10 J-state value 01 K-state value 11 Undefined In the host mode, the use of linestate by the host controller driver is not necessary (unlike EHCI), because the port controller state machine and the port routing manage the connection of LS and FS. In the device mode, the use of linestate by the device controller driver is not necessary.
9	HSP	High-speed port Read-only Default = 0 When the bit is set (1), the host/device connected to the port is in the high-speed mode. When this bit is clear (0), the host/device connected to the port is not in a high-speed mode. Note: HSP is redundant with PSPD(27:26), but will remain in the design for compatibility. This bit is not defined in the EHCI specification.

FS1_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
8	PR	Port reset This bit is clear (0) if the port power (PP) bit (bit 12) of this register is clear (0). Host mode: ’ Read/write ’ Default = 0 When the software sets (1) this bit, the bus-reset sequence as defined in the USB Specification Revision 2.0 is started. This bit will automatically clear (go to 0) after the reset sequence is complete. Note: This behavior is different from EHCI, where the host controller driver is required to clear (0) this bit after the reset duration is timed in the driver. Device mode: This bit is a read-only status bit. Device reset from the USB bus is also indicated in the USBSTS register. 0x1: Port is in reset 0x0: Port is not in reset

FS1_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
7	SUSP	Suspend Host mode: ’ Read/write ’ Default = 0 The port enabled bit and suspend bit of this register define the port states: Bit value Port state value 0x Disable value 10 Enable value 11 Suspend When in the suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction if a transaction was in progress when this bit set (1). In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. The host controller will unconditionally clear (0) this bit when the software clears (0) the force port resume bit. The host controller ignores a write of zero to this bit. If the host software sets (1) this bit when the port is not enabled (port enabled bit is a zero), the results are undefined. This field is clear (0) if port power (PP) is clear (0) in the host mode. Device mode: ’ Read only ’ Default = 0 In the device mode, this bit is a read-only status bit. 0x1: Port in suspend state_1 0x0: Port not in suspend st_1 0x1: Port in suspend state_2 0x0: Port not in suspend st_2

FS1_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
6	FPR	Force port resume ’ Read/write ’ Default = 0 Host mode: The software sets (1) this bit to drive resume signaling. The host controller sets (1) this bit if a J-to-K transition is detected while the port is in the suspend state. When this bit transitions to a one because a J-to-K transition is detected, the port change detect bit in the USBSTS register is also set (1). This bit will automatically clear (go to 0) after the resume sequence is complete. This behavior is different from EHCI, where the host controller driver is required to clear (0) this bit after the resume duration is timed in the driver. Note that, when the host controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (full-speed 'K') is driven on the port as long as this bit remains set (1). This bit will remain set (1) until the port has switched to the high-speed idle. Clearing (0) this bit has no affect, because the port controller will time the resume operation and clear (0) the bit when the port control state switches to HS or FS idle. This bit is clear if the port power (PP) is clear (0) in the host mode. This bit is not-EHCI compatible. Device mode: After the device has been in the suspend state for 5 ms or more, the software must set (1) this bit to drive resume signaling before clearing. The device controller will set (1) this bit if a J-to-K transition is detected while the port is in the suspend state. The bit will be cleared (0) when the device returns to normal operation. Also, when this bit transitions to a one because a J-to-K transition was detected, the port change detect bit in the USBSTS register is also set (1). 0x1: Resume detected/driven on port 0x0: No resume (K-state detected/driven on port)
5	OCC	Over-current change Read/write control Default = 0 This bit gets is set (1) when there is a change to over-current active. The software clears this bit by setting (1) this bit position. For host/OTG implementations, the user can provide over-current detection to the vbus_pwr_fault input for this condition. For device-only implementations, this bit shall always be clear (0).

FS1_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
4	OCA	Over-current active Read-only Default = 0 value 1 = This port currently has an over-current condition. value 0 = This port does not have an over-current condition. This bit will automatically transition from set (1) to clear (0) when the over current condition is removed. For host/OTG implementations, the user can provide over-current detection to the vbus_pwr_fault input for this condition. For device-only implementations, this bit shall always be clear (0).
3	PEC	Port enable/disable change Read/write control value 1 = Port enabled/disabled status has changed value 0 = No change Default = 0 Host mode: For the root hub, this bit gets set (1) only when a port is disabled due to disconnect on the port or due to the appropriate conditions existing at the EOF2 point. The software clears this bit by writing a one to it. This field is clear (0) if the port power (PP) bit in the register is clear (0). Device mode: The device port is always enabled (this bit will be zero).
2	PE	Port enabled/disabled Read/write value 1 = Enable value 0 = Disable Default 0 Host mode: Ports can only be enabled by the host controller as a part of the reset and enable. The software cannot enable a port by setting (1) this field. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by the host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port, due to other host controller and bus events. When the port is disabled, (0) downstream propagation of data is blocked except for reset. This field is clear (0) if the port power (PP) bit is cleared (0) in the host mode. Device mode: The device port is always enabled (this bit will be set [1])

FS1_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
1	CSC	Connect status change Read/write control value 1 = Change in current connect status value 0 = No change Default = 0 Host mode: Indicates that a change has occurred in the port's current connect status. The host/device controller sets (1) this bit for all changes to the port device connect status, even if the system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, the hub hardware will be 'setting' an already-set bit (that is, the bit will remain set). The software clears this bit by writing a one to it. This field is zero if the port power (PP) bit in this register is zero in the host mode. Device mode: This bit is undefined in the device controller mode.
0	CCS	Current connect status Read-only Host mode: value 1 = Device is present on port value 0 = No device is present Default = 0 This value reflects the current state of the port, and may not correspond directly to the event that caused the connect status change bit (bit 1) to be set (1). This field is clear if the port power (PP) bit in this register is clear (0) in host mode. Device mode: value 1 = Attached value 0 = Not attached Default = 0 If this bit is set (1), this indicates that the device successfully attached, and is operating in either high speed or full speed, as indicated by the high speed port bit in this register. If this bit is clear (0), this indicates that the device did not attach successfully or was forcibly disconnected by the software clearing (0) the run bit in the USBCMD register. It does not state the device being disconnected or suspended.

0x180001A4 FS1_USB_OTG_HS_OTGSC

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000E20

FS1_USB_OTG_HS_OTGSC

Bits	Name	Description
31	RESERVED_BIT31	Clear (0) this bit.
30	DPIE	Data pulse interrupt enable
29	B_1MSE	1 millisecond timer interrupt enable - read/write
28	BSEIE	B session end interrupt enable Read/write Setting (1) this bit enables the B session end interrupt.
27	BSVIE	B session valid interrupt enable Read/write Setting (1) this bit enables the B session valid interrupt.
26	ASVIE	A session valid interrupt enable Read/write Setting (1) this bit enables the A session valid interrupt.
25	AVVIE	A Vbus valid interrupt enable Read/write Setting (1) this bit enables the A Vbus valid interrupt.
24	IDIE	USB ID interrupt enable Read/write Setting (1) this bit enables the USB ID interrupt.
23	RESERVED_BIT23	Clear (0) this bit.
22	DPIS	Data pulse interrupt status Read/write to clear This bit is set (1) when data bus pulsing occurs on DP or DM. Data bus pulsing is only detected when USBMODE.CM = Host (11) and PORTSC(0). PortPower = Off (0). The software must write a one to clear this bit.
21	B_1MSS	1 millisecond timer interrupt status Read/write to clear This bit is set (1) once every millisecond. The software must write a one to clear this bit.
20	BSEIS	B session end interrupt status Read/write to clear This bit is set (1) when the Vbus has fallen below the B session end threshold. The software must write a one to clear this bit
19	BSVIS	B session valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the B session valid threshold (0.8 VDC). The software must write a one to clear this bit.

FS1_USB_OTG_HS_OTGSC (cont.)

Bits	Name	Description
18	ASVIS	A session valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the A session valid threshold (0.8 VDC). The software must write a one to clear this bit.
17	AVVIS	A Vbus valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the Vbus valid threshold (4.4 VDC) on an A device. The software must write a one to clear this bit.
16	IDIS	USB ID interrupt status Read/write This bit is set (1) when a change on the ID input has been detected. The software must write a one to clear this bit.
15	RESERVED_BIT15	Clear (0) this bit.
14	DPS	Data bus pulsing status Read-only If this bit is set (1), it indicates that the data bus pulsing is being detected on the port.
13	B_1MST	1 millisecond timer toggle Read-only This bit toggles once per millisecond.
12	BSE	B session end Read-only Indicates that the Vbus is below the B session end threshold.
11	BSV	B session valid Read-only Indicates that the Vbus is above the B session valid threshold.
10	ASV	A session valid Read-only Indicates that the Vbus is above the A session valid threshold.
9	AVV	A Vbus valid Read-only Indicates that the Vbus is above the A Vbus valid threshold.
8	ID	USB ID Read-only value 0 = A device value 1 = B device

FS1_USB_OTG_HS_OTGSC (cont.)

Bits	Name	Description
7	HABA	Hardware assist B-disconnect to A-connect Read/write value 0 = Disabled value 1 = Enable automatic B-disconnect to A-connect sequence.
6	HADP	Hardware assist data-pulse Write to set
5	IDPU	ID pull-up Read/write This bit provides control over the ID pull-up register. value 0 = Off value 1 = On (default) When this bit is clear (0), the ID input will not be sampled.
4	DP	Data pulsing Read/write Setting (1) this bit causes the pull-up on DP to be asserted for data pulsing during SRP.
3	OT	OTG termination Read/write This bit must be set (1) when the OTG device is in the device mode. This controls the pull-down on DM.
2	HAAR	Hardware assist auto-reset Read/write value 0 = Disabled value 1 = Enable automatic reset after connect on host port.
1	VC	Vbus charge Read/write Setting (1) this bit causes the Vbus line to be charged. This is used for Vbus pulsing during SRP.
0	VD	Vbus discharge Read/write Setting (1) this bit causes the Vbus to discharge through a resistor.

0x180001A8 FS1_USB_OTG_HS_USBMODE

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_USBMODE register is the USB device mode register.

FS1_USB_OTG_HS_USBMODE

Bits	Name	Description
31:6	RESERVED_BITS31_6	Clear (0) these bits.
5	VBPS	Vbus power select value 0 - Output is 0 value 1 - Output is 1 This bit is connected to the vbus_pwr_select output and can be used for any generic control, but is named to be used by logic that selects between an on-chip Vbus power source (charge pump) and an off-chip source in systems when both are available.
4	SDIS	Stream disable mode value 0 = Inactive (default) value 1 = Active Device mode: Setting (1) this bit disables double priming on both the Rx and Tx for low bandwidth systems. This mode ensures that, when the Rx and Tx buffers are sufficient to contain an entire packet, the standard double buffering scheme is disabled to prevent overruns/underruns in bandwidth-limited systems. Note: In the high speed mode, a NYET handshake will respond to all packets received when the stream disable is active. Host mode: Setting (1) this bit ensures that overruns/underruns of the latency FIFO are eliminated for low bandwidth systems where the Rx and Tx buffers are sufficient to contain the entire packet. Enabling the stream disable also has the effect of ensuring that the Tx latency is filled to capacity before the packet is launched onto the USB. Note: Time duration to pre-fill the FIFO becomes significant when the stream disable is active. See TXFILLTUNING and TXTTFILLTUNING [MPH only] to characterize the adjustments needed for the scheduler when using this feature. Note: The use of this feature substantially limits of the overall USB performance.
3	SLOM	Setup lockout mode. In the device mode, this bit controls the behavior of the setup lock mechanism. value 0 = Setup lockouts on (default) value 1 = Setup lockouts off (DCD requires use of a setup data buffer tripwire in USBCMD)

FS1_USB_OTG_HS_USBMODE (cont.)

Bits	Name	Description
2	ES	Endian select Read/write This bit can change the byte ordering of the transfer buffers to match the host microprocessor bus architecture. The bit fields in the microprocessor interface and the DMA data structures (including the setup buffer within the device QH) are unaffected by the value of this bit, because they are based upon 32-bit words. value 0 = Little endian (default) - first byte referenced in the least significant byte of a 32-bit word. value 1 = Big endian - first byte referenced in most significant byte of a 32-bit word.
1:0	CM	Controller mode Read/write once The controller mode is defaulted to the proper mode for host-only and device-only implementations. For those designs that contain both host and device capability, the controller will default to an idle state and will need to be initialized to the desired operating mode after reset. For combination host/device controllers, this register can only be written once after reset. If it is necessary to switch modes, the software must reset the controller by writing to the RESET bit in the USBCMD register before reprogramming this register. value 00 = Idle [default for combination host/device] value 01 = Reserved value 10 = Device controller [default for device only controller] value 11 = Host controller [default for host only controller]

0x180001AC FS1_USB_OTG_HS_ENPDTSETUPSTAT

Type: Read/write control
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENPDTSETUPSTAT register is the endpoint set-up status register.

FS1_USB_OTG_HS_ENPDTSETUPSTAT

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.

FS1_USB_OTG_HS_ENPDTSETUPSTAT (cont.)

Bits	Name	Description
15:0	ENDPTSETUPSTAT_15_0	Set-up endpoint status For every set-up transaction that is received, a corresponding bit in this register is set (1). The software must clear or acknowledge the setup transfer by setting (1) a respective bit after it has read the setup data from the queue head. The response to a set-up packet as in the order of operations and total response time is crucial to limit bus time outs while the set-up lock-out mechanism is engaged. This register is only used in the device mode.

0x180001B0 FS1_USB_OTG_HS_ENDPTPRIME

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTPRIME register is the endpoint initialization register. This register is only used in the device mode.

FS1_USB_OTG_HS_ENDPTPRIME

Bits	Name	Description
31:16	PETB_15_0	Prime endpoint transmit buffer For each endpoint, a corresponding bit is used to request that a buffer is prepared for a transmit operation in order to respond to a USB IN/INTERRUPT transaction. The software should set (1) the corresponding bit when posting a new transfer descriptor to an endpoint. The hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a transmit buffer. The hardware will clear (0) this bit when the associated endpoint(s) is (are) successfully primed. Note: These bits will be momentarily set (1) by the hardware during hardware re-priming operations when a dTD is retired, and the dQH is updated. PETB[15] - Endpoint 15 PETB[1] - Endpoint 1 PETB[0] - Endpoint 0

FS1_USB_OTG_HS_ENDPTPRIME (cont.)

Bits	Name	Description
15:0	PERB_15_0	Prime endpoint receive buffer For each endpoint, a corresponding bit is used to request that a buffer is prepared for a receive operation for when a USB host initiates a USB OUT transaction. The software should set (1) the corresponding bit whenever posting a new transfer descriptor to an endpoint. The hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a receive buffer. The hardware will clear (0) this bit when the associated endpoint(s) is (are) successfully primed. Note: These bits will be momentarily set (1) by the hardware during hardware re-priming operations when a dTD is retired, and the dQH is updated. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x180001B4 FS1_USB_OTG_HS_ENDPTFLUSH

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTFLUSH register is the endpoint de-initialize register. This register is only used in the device mode.

FS1_USB_OTG_HS_ENDPTFLUSH

Bits	Name	Description
31:16	FETB_15_0	Flush endpoint transmit buffer Setting (1) a bit in this register will cause the associated endpoint to clear any primed buffers. If a packet is in progress for one of the associated endpoints, that transfer will continue until completion. The hardware will clear this register after the endpoint flush operation is successful. FETB[15] - Endpoint 15 FETB[1] - Endpoint 1 FETB[0] - Endpoint 0
15:0	FERB_15_0	Flush endpoint receive buffer Setting a bit (1) will cause the associated endpoint to clear any primed buffers. If a packet is in progress for one of the associated endpoints, that transfer will continue until completion. The hardware will clear this register after the endpoint flush operation is successful. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x180001B8 FS1_USB_OTG_HS_ENDPTSTAT

Type: Read-only
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTSTAT register is the endpoint status register. This register is only used in the device mode.

FS1_USB_OTG_HS_ENDPTSTAT

Bits	Name	Description
31:16	ETBR_15_0	Endpoint transmit buffer ready One bit for each endpoint indicates the status of the respective endpoint buffer. This bit is set (1) by the hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There will always be a delay between setting (1) a bit in the ENDPTPRIME register and the endpoint indicating that it is ready. This delay time varies based upon the current USB traffic and the number of bits set (1) in the ENDPTPRIME register. The buffer ready status is cleared by a USB reset, by the USB DMA system, or through the ENDPTFLUSH register. Note: These bits will be momentarily cleared by the hardware during hardware endpoint re-priming operations when a dTD is retired, and the dQH is updated. ETBR[15] - Endpoint 15 ETBR[1] - Endpoint 1 ETBR[0] - Endpoint 0
15:0	ERBR_15_0	Endpoint receive buffer ready One bit for each endpoint indicates the status of the respective endpoint buffer. This bit is set (1) by the hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There will always be a delay between setting (1) a bit in the ENDPTPRIME register and the endpoint indicating that it is ready. This delay time varies based upon the current USB traffic and the number of bits set (1) in the ENDPTPRIME register. The buffer ready status is cleared by a USB reset, by the USB DMA system, or through the ENDPTFLUSH register. Note: These bits will be momentarily cleared by the hardware during hardware endpoint re-priming operations when a dTD is retired, and the dQH is updated. ERBR[15] - Endpoint 15 ERBR[1] - Endpoint 1 ERBR[0] - Endpoint 0

0x180001BC FS1_USB_OTG_HS_ENDPTCOMPLETE

Type: Read/write control
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The register is the endpoint complete register. This register is only used in the device mode.

FS1_USB_OTG_HS_ENDPTCOMPLETE

Bits	Name	Description
31:16	ETCE_15_0	Endpoint transmit complete event Each bit indicates that a transmit event (IN/INTERRUPT) occurred and the software should read the corresponding endpoint queue to determine the endpoint status. If the corresponding IOC bit is set (1) in the transfer descriptor, then this bit will be set (1) simultaneously with the USBINT. Writing a one will clear the corresponding bit in this register. ETCE[15] - Endpoint 15 ETCE[1] - Endpoint 1 ETCE[0] - Endpoint 0
15:0	ERCE_15_0	Endpoint receive complete event Each bit indicates that a received event (OUT/SETUP) occurred and the software should read the corresponding endpoint queue to determine the transfer status. If the corresponding IOC bit is set (1) in the transfer descriptor, then this bit will be set (1) simultaneously with the USBINT. Writing a one will clear the corresponding bit in this register. ERCE[15] - Endpoint 15 ERCE[1] - Endpoint 1 ERCE[0] - Endpoint 0

0x180001C0 FS1_USB_OTG_HS_ENDPTCTRL0

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00800080

The USB_OTG_HS_ENDPTCTRL0 register is the endpoint control 0 register. Every device will implement endpoint0 as a control endpoint.

FS1_USB_OTG_HS_ENDPTCTRL0

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.

FS1_USB_OTG_HS_ENDPTCTRL0 (cont.)

Bits	Name	Description
23	TXE	Tx endpoint enable value 1 = Enabled Endpoint0 is always enabled. Read only
22:20	RESERVED_BITS22_20	Clear (0) these bits.
19:18	TXT	Tx endpoint type Read only value 00 = Control Endpoint0 is fixed as a control end point.
17	RESERVED_BIT17	Clear (0) this bit.
16	TXS	Tx endpoint stall Read/write value 0 = End point OK (default) value 1 = End point stalled The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. It will continue returning STALL until the bit is cleared (0) by the software or it will automatically be cleared (0) upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). Note: There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. In most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15:8	RESERVED_BITS15_8	Clear (0) these bits.
7	RXE	Rx endpoint enable value 1 = Enabled Endpoint0 is always enabled. Read only
6:4	RESERVED_BITS6_4	Clear (0) these bits.
3:2	RXT	Rx endpoint type Read only value 00 = Control Endpoint0 is fixed as a control end point.
1	RESERVED_BIT1	Clear (0) this bit.

FS1_USB_OTG_HS_ENDPTCTRL0 (cont.)

Bits	Name	Description
0	RXS	Rx endpoint stall Read/write value 0 = End point OK (default) value 1 = End point stalled The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. It will continue returning STALL until the bit is cleared (0) by the software or it will automatically be cleared (0) upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). Note: There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. In most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

0x180001C0+4*n FS1_USB_OTG_HS_ENDPTCTRLn, n=[1..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTCTRLn register is the endpoint control n register. There is an ENDPTCTRLn register for each endpoint in a device.

CAUTION If one endpoint direction is enabled and the paired endpoint of the opposite direction is disabled, then the unused direction type must be changed from the default control-type to any other type (such as bulk-type). Leaving an unconfigured endpoint control will cause undefined behavior for the data PID tracking on the active endpoint/direction.

FS1_USB_OTG_HS_ENDPTCTRLn

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.
23	TXE	Tx endpoint enable value 0 = Disabled (default) value 1 = Enabled An endpoint should be enabled only after it has been configured.

FS1_USB_OTG_HS_ENDPTCTRLn (cont.)

Bits	Name	Description
22	TXR	Tx data toggle reset (WS) value 1 = Reset PID sequence Whenever a configuration event is received for this endpoint, the software must set (1) this bit in order to synchronize the data PIDs between the host and device.
21	TXI	Tx data toggle inhibit value 0 = PID sequencing enabled (default) value 1 = PID sequencing disabled This bit is only used for testing and should always be cleared (0). Setting (1) this bit will cause this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.
20	RESERVED_BIT20	Clear (0) this bit.
19:18	TXT	Tx endpoint type value 00 = Control value 01 = Isochronous value 10 = Bulk value 11 = Interrupt
17	TXD	Tx endpoint data source value 0 = Dual port memory buffer/DMA engine (default) This bit should always be cleared (0).
16	TXS	Tx endpoint stall value 0 = End point OK value 1 = End point stalled This bit will be cleared (0) automatically upon receipt of a SETUP request if this endpoint is configured as a control endpoint, and this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. This control will continue to STALL until this bit is either cleared (0) by the software or automatically cleared (0) as described above for control endpoints. Note (control endpoint types only): There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. in most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15:8	RESERVED_BITS15_8	Clear (0) these bits.
7	RXE	Rx endpoint enable value 0 = Disabled (default) value 1 = Enabled An endpoint should be enabled only after it has been configured.

FS1_USB_OTG_HS_ENDPTCTRLn (cont.)

Bits	Name	Description
6	RXR	Rx data toggle reset (WS) Write 1 = Reset PID sequence Whenever a configuration event is received for this endpoint, the software must set (1) this bit in order to synchronize the data PIDs between the host and the device.
5	RXI	Rx data toggle inhibit value 0 = Disabled (default) value 1 = Enabled This bit is only used for testing and should always be cleared (0). Setting (1) this bit will cause this endpoint to ignore the data toggle sequence and always accept a data packet regardless of their data PID.
4	RESERVED_BIT4	Clear (0) this bit.
3:2	RXT	Rx endpoint type value 00 = Control value 01 = Isochronous value 10 = Bulk value 11 = Interrupt
1	RXD	Rx endpoint data sink value 0 = Dual port memory buffer/DMA engine (default) This bit should always be cleared (0).
0	RXS	Rx endpoint stall value 0 = End point OK value 1 = End point stalled This bit will be cleared (0) automatically upon receipt of a SETUP request if this endpoint is configured as a control endpoint, and this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. This control will continue to STALL until this bit is either cleared (0) by the software or automatically cleared (0) as described above for control endpoints. Note (control endpoint types only): There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. in most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

0x180001FC+4*n FS1_USB_OTG_HS_ENDPT_PIPE_IDn, n=[1..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x001F001F

The USB_OTG_HS_ENDPT_PIPE_IDn register is the endpoint pipe number register. There is an USB_OTG_HS_ENDPT_PIPE_IDn register for each endpoint in a device.

NOTE Reset value of TX_PIPE_ID and RX_PIPE_ID is 0x1F, which means that Endpoint is not mapped to any pipe.

FS1_USB_OTG_HS_ENDPT_PIPE_IDn

Bits	Name	Description
31:21	RESERVED_BITS31_21	Clear (0) these bits.
20:16	TX_PIPE_ID	This field indicate the pipe number that this tx end point (n) will use in pipe mode.
15:5	RESERVED_BITS15_5	Clear (0) these bits.
4:0	RX_PIPE_ID	This field indicate the pipe number that this rx end point (n) will use in pipe mode.

0x18000240 FS1_USB_OTG_HS_PHY_CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0b1110000111010

The USB_OTG_HS_PHY_CTRL register is used to configure various features in the Synopsys 28nm PHY.

FS1_USB_OTG_HS_PHY_CTRL

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12	USB2_PHY_IDHV_CLAMP_EN	Clamp enable for IDHV interrupt level shifter from USB VDD180 domain to VDDCX domain. When set (1), VLS is active and IDHV interrupt is translated from 1.8V domain to Vddcx domain. When clear (0), VLS is clamped high. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.
11	USB2_PHY_OTGSESSVLDHV_CLAMP_EN	Clamp enable for OTGSESSVLDHV interrupt level shifter from USB VDD180 domain to VDDCX domain. When set (1), VLS is active and OTGSESSVLDHV interrupt is translated from 1.8V domain to Vddcx domain. When clear (0), VLS is clamped to zero. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.

FS1_USB_OTG_HS_PHY_CTRL (cont.)

Bits	Name	Description
10	PHY_MPM_HV_CLAMP_EN	Clamp enable for HV interrupts level shifters from USB VDD180 domain to VDDPAD MPM in usb2 phy wrapper. When set (1), VLS is active and HV interrupts are translated from 1.8V domain to MPM Vdd domain. When clear (0), VLS is clamped to inactive state. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.
9	USB2_PHY_OTGSESSVLD HV_INTEN	Enable HV session valid interrupt from phy. This interrupt translated with level shifter for wakeup from retention when VDDCX is nominal and TCXO is running.
8	USB2_PHY_IDHV_INTEN	Enable HV id pin interrupt from phy. This interrupt translated with level shifter for wakeup from retention when VDDCX is nominal and TCXO is running.
7	USB2_PHY_ULPI_POR	Reset for ULPI PHY Wrapper and ULPI clock domain logic in usb2_phy_wrapper.
6:4	USB2_PHY_FSEL	Reference Clock Frequency Select 011 (Assumes 19.2MHz default)
3	HOST_PORTCTRL_FORCE _SUSEN	Chicken bit for CR-0000153908 - when this bit set the core will enter to low power mode when portctrl host sm enter to suspend mode. Default value is 1.
2	USB2_PHY_SIDDQ	IDDQ Test Enable.
1	USB2_PHY_RETEN	Retention mode enable/disable
0	USB2_PHY_POR	Power-On-Reset (Analog configuration needs to happen before POR is set to 0)

0x18000244 FS1_USB_OTG_HS_GENERIC1

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

The USB_OTG_HS_GENERIC1 register.

FS1_USB_OTG_HS_GENERIC1

Bits	Name	Description
31:16	USB_HS_TX_DEPTH	TX_DEPTH is the number of words in the TX buffer. This number is calculated by the number of bytes allocated per Endpoint divided by 4, times the number of endpoints. The RAM width is 36. In HS USB this value is usually 512 bytes per EP, and for FS ONLY USB it is usually 64 Bytes per EP.
15:0	USB_HS_RX_DEPTH	RX_DEPTH is the number of words in the RX buffer. This number is usually 256, but can support powers of 2 up to 4096. The RAM width is 36.

0x18000248 FS1_USB_OTG_HS_GENERIC2

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

The USB_OTG_HS_GENERIC2 register.

FS1_USB_OTG_HS_GENERIC2

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.
15	USE_SPS_AHB2AHB	USE_SPS_AHB2AHB generic specifies if AHB2AHB bridge is connected between BAM and SPS Fabric AHB.
14	LPM_SUPPORT	The LPM_SUPPORT generic specifies if USB support Link Power Management.
13:9	USB_HS_DEV_EP	The number of USB endpoints. Valid values for the number of Endpoints are 4, 8, and 16
8:3	MAX_PIPES	The number of simultaneous parallel pipes supported by the BAM. Supported values are 2 to 30
2	USE_SPS	The USE_SPS generic specifies if Bam is connected to USB core.
1	USE_HSIC	The USE_HSIC generic specifies if an HSIC is connected to USB core.
0	UTMI_PHY_SW_IF_EN	The UTMI_PHY_SW_IF_EN generic specifies if UTMI phy Register Interface is enabled

0x18000250 FS1_USB_OTG_HS_L1_EP_CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0000FFFF

The USB_OTG_HS_L1_EP_CTRL register enables/disables transition to L1 and exit from L1 state when specific TX endpoints are primed.

FS1_USB_OTG_HS_L1_EP_CTRL

Bits	Name	Description
31:16	TX_EP_PRIME_L1_EXIT	Those bit's enables Remote Wakeup in L1 state when SW starts Priming The specific Endpoint.
15:0	TX_EP_PRIME_L1_EN	Control bit's that enables/disables transition to L1 when the specific TX Endpoint is active.

0x18000254 FS1_USB_OTG_HS_L1_CONFIG

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_L1_CONFIG register is used to configure various L1 features.

FS1_USB_OTG_HS_L1_CONFIG

Bits	Name	Description
31:12	RESERVED_BITS31_12	Clear (0) these bits.
11	PLL_PWR_DWN_EN	Control bit that enables/disables power down of 480 MHZ PLL in L1 state.
10	PHY_LPM_EN	Control bit that enable/disables entering ULPI Low Power Mode in L1 state
9	GATE_AHB_CLK_EN	Control bit that enable/disables clock request signaling for usb_ahb_clk in L1 state
8	GATE_FS_XCVR_CLK_EN	Control bit that enable/disables clock gating of usb_fs_xcvr_clk in L1 state
7	GATE_SYS_CLK_EN	Control bit that enable/disables clock gating of usb_system_clk in L1 state
6	GATE_XCVR_CLK_EN	Control bit that enable/disables power-down of 480 MHz PLL in L1 state
5	L1_REMOTE_WAKEUP_EN	Control bit that enables/disables Remote Wakeup in L1 state. When this bit is low, then Link Controller never initiates Remote Wakeup in L1 state. When this bit is high, Link Controller can initiate Remote Wakeup.
4	LPM_EN	Control bit that enables/disables LPM support. When this bit is zero a full backward compatibility is ensured - no LPM support and no response for LPM Extended Transaction
3:0	PLL_TURNOFF_MIN_HIRD	Specifying a minimum expected HIRD value from Host that enables HW mechanism for turning off the 480 MHz PLL. The default value is 50us.

0x18000258 FS1_USB_OTG_HS_LPM_DEBUG_1

Type: Read/Clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_DEBUG_1 register is for debug and testing purposes mostly.

FS1_USB_OTG_HS_LPM_DEBUG_1

Bits	Name	Description
31:16	DEBUG_L1_LONG_ENT_CNT	Count number of exits from L1 where duration in L1 is > 200us. Writing to this register clears the counter.
15:0	DEBUG_L1_SHORT_ENT_CNT	Count number of exits from L1 where duration in L1 is <= 200us. Writing to this register clears the counter.

0x1800025C FS1_USB_OTG_HS_LPM_DEBUG_2

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_DEBUG_2 register is for debug and testing purposes mostly.

FS1_USB_OTG_HS_LPM_DEBUG_2

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12:9	L1_RMT_WKUP_TIME	Read/write Specifying How much time the device drives remote wakeup. The default Value is 50us for reset value. Add the value of this register (in us) to the remote wakeup time.
8	L1_FPR	Read/write L1 Force port resume, The software sets (1) this bit to drive resume signaling.
7	HSIC_CLK_PLL_BYPASSNL	Read only. Disables PLL analog logic. Active low. Connects to bypassnl input of NT_PLL.
6	HSIC_CLK_PLL_RESET	Read only. Resets all FF in PLL. Active low. Connects to reset_n input of NT_PLL.
5	HSIC_CLK_GATE	Read only. Clock gating of hsic_clk and ulpi_clk, without turning off HSIC PLL.
4	FS_XCVR_CLK_GATE	Read only. Clock gating of cc_usb_xcvr_fs_clk
3	SYS_CLK_GATE	Read only. Clock gating of cc_usb_system_clk
2	AHB_CLK_GATE	Read only. Clock gating of usb_ahb_clk

FS1_USB_OTG_HS_LPM_DEBUG_2 (cont.)

Bits	Name	Description
1	L1_STATE	Read only. Status bit indicating if Device is in L1 state. When this bit high, Link Controller and HSIC PHY are in L1 state
0	DEBUG_L1_EN	Read/write Control bit that enable/disables DEBUG counters operation.

0x18000260 FS1_USB_OTG_HS_LPM_ATTRIBUTES

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_ATTRIBUTES register store the bmAttribute Field of the LPM transaction.

FS1_USB_OTG_HS_LPM_ATTRIBUTES

Bits	Name	Description
31:5	RESERVED_BITS31_5	Clear (0) these bits.
4	BREMOTEWAKE	A value of one (1B) in this field enables the addressed device to wake the host upon any meaningful application-specific event (e.g. an interrupt for a device with one or more interrupt endpoints). A value of zero (0B) disables the device from initiating remote wake.
3:0	HIRD	Host Initiated Resume Duration.

2.5 TSIF Registers (0x18200000 TSIF_BASE)

This section contains TSIF registers.

2.5.1 TSIF status and control

0x18200000 TSIF_STATUS_AND_CONTROL

Type: Read/Write
Clock: CRIF_WR_CLK
Reset State: 0x04000000

The Status and Control Register contains six fields: Interrupt Enable, Status, Polarity, Configuration, Stop, and Start.

The Start field is located in bit[0] and controls overall operation of the TSIF. A zero value in this field indicates the TSIF is disabled and not running. A one written to this field starts the TSIF.

The Stop field is located in bit 3. Writing a one to this bit clears the Start field to zero and stops the TSIF while writing a zero has no effect. It always reads the value zero.

The EHI Configuration field is located in bits[11:9] and controls the configuration of the EHI as detailed in the description. The Internal Configuration field is located in bits[6:4] and controls internal TSIF operations.

The Polarity field is located in bits [21:16] and controls the expected polarity of signals of the EHI.

After the Start field has been written to a one, the Polarity, Configuration, and Start fields are write protected. Only the Stop field may be written. This protects the operational state of the TSIF and facilitates manipulation of the Status field when the TSIF is running.

The Status field is located in bits [27:23] and contains packet available, first packet, overflow, lost sync and timeout state respectively. The last three apply regardless of Internal Configuration. Packet available applies only when the Data Mover is not used.

Bit 28 controls the generation of interrupts. The TSIF interrupt output is a level that remains asserted as long as TSIF_EN_INTER is set and bit 27, 25, or 24 is set.

TSIF_STATUS_AND_CONTROL

Bits	Name	Description
31:29	RESERVED_1	Writes have no effect but by convention, always write zero. Reads zero.
28	TSIF_EN_INTER	Enables tsif_intr output to be asserted on an interrupt condition if high. If enabled, the interrupt level is asserted by the TSIF as the 'OR' of bits 27, 25, and 24.

TSIF_STATUS_AND_CONTROL (cont.)

Bits	Name	Description
27	TSIF_PACK_AVAIL	Set by TSIF when a 188 byte HTS packet plus four byte status are available. Only set when TSIF_EN_DM is set low. When set, it indicates that software should read 192 bytes from the Data Register. Cleared by software by writing a one. Writing zero has no effect. Never cleared by the TSIF
26	TSIF_FIRST_PACKET	Reflects the current state of the first-packet-flag. Read only from software. Never generates an interrupt.
25	TSIF_OVERFLOW	Set by TSIF when an overflow condition occurs. Cleared by software by writing a one. Writing a zero has no effect. Never cleared by the TSIF.
24	TSIF_LOST_SYNC	Set by TSIF when a lost sync condition occurs. Cleared by software by writing a one. Writing a zero has no effect. Never cleared by the TSIF.
23	TSIF_TIMEOUT	Set by TSIF when a timeout condition occurs. Cleared by software by writing a one. Writing a zero has no effect. Never cleared by the TSIF.
22	RESERVED_2	Writes have no effect but by convention, always write zero. Reads zero.
21	TSIF_INV_SYNC	Invert the external indicator tsif_sync.
20	TSIF_INV_NULL	Invert the external discrimination flag tsif_null.
19	TSIF_INV_ERROR	Invert the external error flag input tsif_error.
18	TSIF_INV_ENABLE	Invert the external enable input tsif_en.
17	TSIF_INV_DATA	Invert the external data input tsif_data.
16	TSIF_INV_CLOCK	Invert the external clock input tsif_clock.
15	SPARE_SW_BIT	programmable read/write spare SW bit
14:12	RESERVED_3	Writes have no effect but by convention, always write zero. Reads zero.
11	TSIF_EN_NULL	Enable the sample and reporting of the value of the tsif_null input.
10	TSIF_EN_ERROR	Enable the sample and reporting of the value of the tsif_error input.
9	TSIF_LAST_BIT	If high, sample tsif_null and tsif_error on the last bit of the packet.
8	TSIF_EN_TIME_LIMIT	Enables the use of the Time Limit if set.
7	TSIF_EN_TCR	Enables the TSIF Clock Reference (TCR) to run at TSIF_START.
6:5	TSIF_MODE	Set 00 - TSIF Mode 1 is used at TSIF_START. Set 01 - TSIF Mode 2 is used at TSIF_START. Set 10 - TSIF Loop-back Mode is used at TSIF_START. Set 11 - Reserved but implemented as Loop-back.

TSIF_STATUS_AND_CONTROL (cont.)

Bits	Name	Description
4	TSIF_EN_DM	Enables use of the Data Mover request acknowledge interface when set. When clear, the availability of a 188 byte HTS packet plus status is signaled via the assertion of TSIF_PACK_AVAIL.
3	TSIF_STOP	Stops the TSIF operation when written to a one. Writing a zero has no effect. Always reads zero.
2:1	RESERVED_4	Writes have no effect but by convention, always write zero. Reads zero.
0	TSIF_START	Write Operations: Set 0 - Has no effect. Set 1 - Starts the TSIF operation and begins the input of HTS packets After this field is written to a one, all bits in the range [23:0] are write-protected except bit 3. Read Operations return the current bit value.

2.5.2 TSIF time limit

0x18200004 TSIF_TIME_LIMIT

Type: Read/Write
Clock: CRIF_WR_CLK
Reset State: 0x0

The time unit of this register is the period of tsif_ref_clk. tsif_ref_clk equals 27MHz/256. This yields a 9.48 micro second period.

The LIMIT may be read or written at anytime regardless of the state of TSIF_START.

TSIF_TIME_LIMIT

Bits	Name	Description
31:29	RESERVED_1	Writes have no effect but by convention, always write zero. Reads zero.
28	TSIF_TIME_LIMIT_IMM_LOAD	When this bit is set with a write to this register, the new TSIF_TIME_LIMIT value is loaded immediately into the Time Limit Counter. Otherwise it is loaded only when TSIF_START is set, or when last bit of 'Valid Packet' is received. Setting this bit is allowed only when no packets are currently arriving. ' Write only bit.
27:24	RESERVED_2	Writes have no effect but by convention, always write zero. Reads zero.

TSIF_TIME_LIMIT (cont.)

Bits	Name	Description
23:0	TSIF_TIME_LIMIT	The time-limit indicates the amount of time which is allowed to pass between each valid-packet written to system memory (time between the END of one packet to the END of next one). If this timer expires, then a timeout-status is reported.

2.5.3 TSIF clock reference (TCR) counter

0x18200008 TSIF_CLOCK_REF_COUNTER

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x0

This counter runs off the crif_clk and may be written or read at anytime. It increments relative to a tsif_ref_clk. tsif_ref_clk is equal to 27 MHz/256. Therefore the TCR increments at a rate equal to 27 MHz/256 = 105.47 kHz. This yields a 9.48 micro second period, which is faster than the equivalent H.222.0 reference clock of 27 MHz/300 = 90 kHz with a 11.11 micro second period. Specifically, 105 kHz provides the required clock resolution but in different time units.

Bits [23:0] of the TCR are used to form the TTS provided as part of the packet status loaded into memory with each H.222.0 packet. The TTS rolls over every 159.07 seconds or approximately every 2.65 minutes. The TCR rolls over every 678.71 minutes or approximately every 11.31 hours.

- Note: Read or Write to the register should be performed at least one tsif_ref_clk cycle after the previous write to the register has been performed.

TSIF_CLOCK_REF_COUNTER

Bits	Name	Description
31:24	TSIF_TCR_HIGH	The high bits of the TCR Counter.
23:0	TSIF_TTS	The TTS provided in each packet status.

2.5.4 TSIF loop back flags

0x1820000C TSIF_LOOP_BACK_FLAGS

Type: Read/Write
Clock: CRIF_WR_CLK
Reset State: 0x0

This register is used for loop back operations.

TSIF_LOOP_BACK_FLAGS

Bits	Name	Description
31	RESERVED_1	Writes have no effect but by convention, always write zero. Reads zero.
30	TSIF_LPBK_PT_FLAG	Loop back Post tsif_en Flag.
29	TSIF_LPBK_NULL_FLAG	Loop back Null Flag.
28	TSIF_LPBK_ERROR_FLAG	Loop back Error Flag.
27:26	RESERVED_2	Writes have no effect but by convention, always write zero. Reads zero.
25	TSIF_LPBK_PKT_LAST	Loop back last packet word indicator.
24	TSIF_LPBK_PKT_START	Loop back starting packet word indicator.
23:0	RESERVED	Writes have no effect but by convention, always write zero. Reads zero.

2.5.5 TSIF loop back data

0x18200010 TSIF_LOOP_BACK_DATA

Type: Read/Write
Clock: CRIF_WR_CLK
Reset State: 0x0

This register is used for loop back operations.

TSIF_LOOP_BACK_DATA

Bits	Name	Description
31:0	TSIF_LPBK_DATA	Loop back packet data.

2.5.6 Test bus control

0x18200014 TSIF_TEST_CTRL

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x0

This register is used for test bus enable and selection.

TSIF_TEST_CTRL

Bits	Name	Description
31:5	RESERVED_1	unused.
4	TEST_BUS_EN	Test bus enable bit, if zero the test bus output is driven to zero.
3	RESERVED_2	unused.
2:0	TEST_BUS_SEL	Test bus selection: '000': control_test_bus0 '001': control_test_bus1 '010': protocol_test_bus0 '011': protocol_test_bus1 '100': testbus_out (MISR) else: test bus output is driven to zero

2.5.7 TSIF MISR test mode

0x18200018 TSIF_TEST_MODE

Type: Read/Write
Clock: CRIF_WR_CLK
Reset State: 0x0

MISR test mode register

TSIF_TEST_MODE

Bits	Name	Description
31:2	RESERVED	unused.
1:0	MODE	Set 00: Disabled Set 01: Enabled, Test Mode 1 - the input to the MISR is the data written toward the RAM Set 10: Enabled, Test Mode 2 - the input to the MISR is the data read from the RAM

2.5.8 MISR TEST MISR reset

0x1820001C TSIF_TEST_MISR_RESET

Type: Write
Clock: CRIF_WR_CLK
Reset State: Undefined

A write to this register will reset the MISR state. This need to be done after setting the test mode register to a non-zero value.

TSIF_TEST_MISR_RESET

Bits	Name	Description
31:1	RESERVED	unused.
0	RESET	

2.5.9 TSIF test export MISR

0x18200020 TSIF_TEST_EXPORT_MISR

Type: Read/Write
Clock: WR_CLK
Reset State: 0x0

This register controls what is sent on testbus. A value of '0' (reset value) will send the data that is going into the MISR on the testbus. A value of '1' will send the current MISR state onto the testbus. The latter option is typically used for debug purposes. For example, if your final MISR signature failed, you might want to know where it failed (i.e., right in the beginning or somewhere else).

TSIF_TEST_EXPORT_MISR

Bits	Name	Description
31:1	RESERVED	unused.
0	EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., what is the result of the muxing of all the input data streams with <BLOCK>_TEST_MODE) When set (1), testbus is driven by the current state of the MISR. (debug typically)

2.5.10 TSIF test MISR CURR VAL

0x18200024 TSIF_TEST_MISR_CURR_VAL

Type: Read
Clock: WR_CLK
Reset State: Undefined

A read from this address will return the current MISR state for this block. Keep in mind that this could change every cycle depending on how it is used.

TSIF_TEST_MISR_CURR_VAL

Bits	Name	Description
31:0	VAL	Current MISR state

2.5.11 TSIF data port

0x18200100 TSIF_DATA_PORT

Type: Read Only
Clock: CRIF_CLK
Reset State: Undefined

At the core level, this register has a separate select so it can be located in an address space separate from the other registers. The product specific wrapper establishes the address.

When a packet is available, 48 reads are expected to this register or data port. This provides the 188 byte Transport Stream packet followed by a four-byte status word. If additional reads are made, then the crif_error signal is asserted. Once a packet is available, it must be completely read in order for an additional packet to be made available. If too few words are read and a new packet is available, then the new packet is discarded with a resulting TSIF_OVERFLOW status condition. Writing this register also causes the crif_error signal to be asserted.

TSIF_DATA_PORT

Bits	Name	Description
31:0	TSIF_DATA	HTS packet data plus a status word.

2.6 TSPP registers (0x18202000 TSPP_BASE)

This section contains TSPP registers.

2.6.1 TSPP control, configuration and status registers (register based)

0x18202000 TSPP_RST

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

This is the SW reset register.

TSPP_RST

Bits	Name	Description
0	TSPP_SW_RESET	When set(1), all functional modules of TSPP block are reset. SW is responsible to clear(0) TSPP_SW_RESET to get TSPP block out of reset. ¨ TSPP RAM is not reset. To reset TSPP RAM SW should explicitly write the values into the RAM. ¨ All SW registers configured by SW are not reset. ¨ All SW registers including RAM may be configured when TSPP_SW_RESET is set(1).

0x18202004 TSPP_CLK_CONTROL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

This is TSPP block clock control register. It is used to disable/enable different TSPP block clocks.

TSPP_CLK_CONTROL

Bits	Name	Description
9	FORCE_CRYPTO_CLK_OPEN	When set(1), crypto_clk CGC forced open.
8	FORCE_PES_PL_CTRL_CLK_OPEN	When set(1), pes_asmb_clk CGC forced open.
7	FORCE_PES_AF_CTRL_CLK_OPEN	When set(1), pes_pre_proc_clk CGC forced open.
6	FORCE_RAW_CTRL_CLK_OPEN	When set(1), raw_ctrl_clk CGC forced open.

TSPP_CLK_CONTROL (cont.)

Bits	Name	Description
5	FORCE_PERF_CNT_CLK_OPEN	When set(1), perf_cnt_clk CGC forced open.
4	FORCE_CTX_SEARCH_CLK_OPEN	When set(1), ctx_search_clk CGC forced open.
3	FORCE_TSP_PROC_CLK_OPEN	When set(1), tsp_proc_clk CGC forced open.
2	FORCE_CONS_AHB2MEM_CLK_OPEN	When set(1), cons_ahb2mem_clk CGC forced open.
1	FORCE_TS_AHB2MEM_CLK_OPEN	When set(1), ts_ahb2mem_clk CGC forced open.
0	SET_CLKON	When set(1), tspp_clkon signal is constantly set to '1'. When clear(0), tspp_clkon signal is dynamically controlled by TSPP HW.

0x18202008 TSPP_CONFIG

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x7F

This is TSPP block configuration register. The register configures TSPP block functionality. This register value may be updated only when TSPP is not active (no TS PKTs are currently processed).

TSPP_CONFIG

Bits	Name	Description
15:8	PKT_LENGTH	Length of received packet. PKT_LENGTH = 188 + SUFFIX_LENGTH. In case of packet from consumer pipe: ¨ The packet is read from consumer pipe and only 188 bytes with 4 bytes if zero padding are written to TSPP RAM. Those 192 bytes will be parsed by TSPP. Rest of bytes are discarded. In case of packet coming from TSIF: ¨ TSIF removes the unneeded suffix, and adds its suffix. In this case PKT_LENGTH value is not used. PKT length is always multiple of 4 bytes, so the two LSB bits of PKT_LENGTH are ignored.

TSPP_CONFIG (cont.)

Bits	Name	Description
7	DUP_WITH_DISC_EN	Duplicate with discontinuity enabled bit. When this bit is clear(0): ¨ It is assumed that duplicate packets don't arrive with discontinuity_indicator set. This means that when discontinuity_indicator is set, continuity_counter is not tested, and the PKT is not considered duplicate. When this bit is set(1): ¨ It is assumed that duplicate packets may arrive with discontinuity_indicator set. This means that when discontinuity_indicator is set, and continuity_counter is the same as in the previous TS PKT, the packet is considered duplicate and discarded. ¨ In case of a duplicate TS PKT with payload_unit_start_indicator = '1', discontinuity_indicator = '1' and unspecified_pes_length = '1', In this case the duplicated PKT will be passed as a complete PES. The PKT will not be considered duplicate.
6	PES_SYNC_ERROR_MASK	When this bit is clear(0), packet_start_code_prefix (0x000001) is not tested. This means that if packet with payload_unit_start_indicator is received with wrong packet_start_code_prefix: ¨ TSP packet is not discarded. ¨ PES construction starts. ¨ PS_BROKEN interrupt is not set.
5	PS_LENGTH_ERR_AT_UNSP_MASK	This bit is related to the following error condition: ¨ payload_unit_start_indicator == 1 ¨ PS_STATE = PS_CONSTRUCTING. ¨ unsp_pes_length = '0' This error condition tells that new PES starts, before the previous PES terminated, and the previous PES is not of unspecified length. When this bit is clear(0), error condition described above is not tested. This means that: ¨ TSP packets is not discarded. ¨ Construction of the unspecified length PES completes (if there is no continuity_error). ¨ PS_BROKEN interrupt is not set.
4	PS_CONT_ERR_AT_UNSP_MASK	This bit is related to continuity_error between last TSP of unspecified length PES to the first TSP of next PES. When this bit is clear(0), continuity error described above is not tested. This means that: ¨ TSP packets is not discarded. ¨ Construction of the unspecified length PES completes. ¨ PS_BROKEN interrupt is not set.

TSPP_CONFIG (cont.)

Bits	Name	Description
3	PS_CONTINUITY_ERROR_MASK	This bit is related to continuity_error between TSPs in the same PES. When this bit is clear(0), continuity error described above is not tested. This means that: ¨ TSP packets is not discarded. ¨ Constructed PES is not discarded. ¨ PS_BROKEN interrupt is not set.
2	PS_DUPLICATE_TSP_MASK	When this bit is clear(0), while PES processing, duplicate TSP packets are not discarded.
1	TSP_ERROR_INDICATOR_MASK	When this bit is clear(0), transport_error_indicator bit is not tested.
0	TSP_SYNC_ERROR_MASK	When this bit is clear(0), sync_byte (0x47) is not tested.

0x1820200C TSPP_CONTROL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

This is TSPP block control register. The register controls TSPP block functionality. This register value may be updated while TSPP block operation.

TSPP_CONTROL

Bits	Name	Description
5	PID_FILTER_LOCK	When this bit is set(1), TSPP doesn't access PID filter table. This bit is only for test purposes, and should be always cear(0). Otherwise TS PKTs will be lost due to overflow.
4	FORCE_KEY_CALC	When this bit is clear(0): TSPP performs data key fetch only if decryption is required and data_key was changed. And as a result multi2 performs key calculation only in this case. When this bit is set(1): TSPP performs data key fetch each time decryption is required, even if the key hasn't changed.
3	TSP_CONS_SRC_DISABLE	When this bit is set(1), TS PKTs located in BAM consumer pipe are not processed, till this bit is clear(0).
2	TSP_TSIF1_SRC_DISABLE	When this bit is set(1), TS PKTs received by TSIF 1 are not processed, till this bit is clear(0).
1	TSP_TSIF0_SRC_DISABLE	When this bit is set(1), TS PKTs received by TSIF 0 are not processed, till this bit is clear(0).

TSPP_CONTROL (cont.)

Bits	Name	Description
0	PERF_COUNT_INIT	Only when this bit is asserted SW is allowed to update performance counters values. The bit insures that the HW doesn't read or write any performance counter while SW is updating their values. The SW is responsible to de assert this bit when SW finished updating performance counters values. To reset any performance counter, SW should write zero value to the corresponding performance counter register.

0x18202010 TSPP_PS_DISABLE

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

This is TSPP block PS disable register. The register is used to allow SW to reconfigure PID filter table while TSPP is active. More details exist in the following table.

TSPP_PS_DISABLE

Bits	Name	Description
15	PS_DISABLE15	PS_DISABLE for pipe number 15. Same as PS_DISABLE0.
14	PS_DISABLE14	PS_DISABLE for pipe number 14. Same as PS_DISABLE0.
13	PS_DISABLE13	PS_DISABLE for pipe number 13. Same as PS_DISABLE0.
12	PS_DISABLE12	PS_DISABLE for pipe number 12. Same as PS_DISABLE0.
11	PS_DISABLE11	PS_DISABLE for pipe number 11. Same as PS_DISABLE0.
10	PS_DISABLE10	PS_DISABLE for pipe number 10. Same as PS_DISABLE0.
9	PS_DISABLE9	PS_DISABLE for pipe number 9. Same as PS_DISABLE0.
8	PS_DISABLE8	PS_DISABLE for pipe number 8. Same as PS_DISABLE0.
7	PS_DISABLE7	PS_DISABLE for pipe number 7. Same as PS_DISABLE0.
6	PS_DISABLE6	PS_DISABLE for pipe number 6. Same as PS_DISABLE0.
5	PS_DISABLE5	PS_DISABLE for pipe number 5. Same as PS_DISABLE0.
4	PS_DISABLE4	PS_DISABLE for pipe number 4. Same as PS_DISABLE0.
3	PS_DISABLE3	PS_DISABLE for pipe number 3. Same as PS_DISABLE0.
2	PS_DISABLE2	PS_DISABLE for pipe number 2. Same as PS_DISABLE0.
1	PS_DISABLE1	PS_DISABLE for pipe number 1. Same as PS_DISABLE0.

TSPP_PS_DISABLE (cont.)

Bits	Name	Description
0	PS_DISABLE0	SW should set(1) this bit when updating PID filter entries that point to pipe number 0. In case of RAW processing, PID filter entries may be updated without setting this bit. When this bit is set(1), all TS PKTs that PID points to PID filter entry that points to pipe number 0, are ignored. When this bit is cleared(0) after it was set, the next TS PKT that is routed to pipe number 0, is retransmitted (pushed to the beginning of pipe number 0). The details regarding PID filter reconfiguration while TSPP is active, are described in SW procedures.

2.6.2 TSPP messaging interrupt registers (register based)

0x18202014 TSPP_MSG_IRQ_STATUS

Type: Read
Clock: AHB_CLK
Reset State: 0x0

This is the TSPP messaging interrupt status register.

TSPP_MSG_IRQ_STATUS

Bits	Name	Description
2	TSPP_IRQ	TSPP interrupt line value. To clear TSPP_IRQ, TSPP interrupt line should be cleared by writing to TSPP_IRQ_CLEAR register.
1	TSIF_1_IRQ	TSIF 1 interrupt line value. To clear TSIF_1_IRQ, TSIF 1 interrupt line should be cleared by writing to TSIF 1 registers.
0	TSIF_0_IRQ	TSIF 0 interrupt line value. To clear TSIF_0_IRQ, TSIF 0 interrupt line should be cleared by writing to TSIF 0 registers.

0x18202018 TSPP_MSG_IRQ_MASK

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

This is the TSPP messaging interrupt mask register.

TSPP_MSG_IRQ_MASK

Bits	Name	Description
2	TSPP_IRQ	Mask bit of TSPP_IRQ.

TSPP_MSG_IRQ_MASK (cont.)

Bits	Name	Description
1	TSIF_1_IRQ	Mask bit of TSIF_1_IRQ.
0	TSIF_0_IRQ	Mask bit of TSIF_0_IRQ.

2.6.3 TSPP interrupt registers (register based)

TSPP block interrupts are generated using only one level structure. All interrupt sources per all pipes are locate in the TSPP_IRQ_STATUS register.

0x1820201C TSPP_IRQ_STATUS

Type: Read
Clock: AHB_CLK
Reset State: 0x0

This is the TSPP interrupt status register. The bits in this register are sticky. In order to clear some bit in this register, corresponding bit should be set in the TSPP_IRQ_CLEAR register.

TSPP_IRQ_STATUS

Bits	Name	Description
19	TSP_RD_CMPL_IRQ	TS PKT read complete interrupt. The interrupt is set when TSPP has completed to fetch TS PKT from TSIF. The interrupt is only for test purposes, and it is used with TSIF loopback mode. SW sequence is as follows: ’ SW writes one TS PKT to TSIF in loopback mode. ’ TSPP fetches the PKT and sets the IRQ. ’ SW clears the IRQ and writes another TS PKT to TSIF, in parallel TSPP parses the previous TS PKT.
18	KEY_ERROR_IRQ	Key error interrupt. This interrupt is set when the required key for TS PKT decryption was not valid. In this case the TSP is discarded. TSPP_KEY_ERROR register contains the information regarding the key errors.
17	KEY_SWITCHED_ILLEGAL_IRQ	Key switched illegal interrupt is set each time when transport_scrambling_control in the TSP header is changed to non scrambled(’00’), or not defined(’01’), and the TSP contains payload. This means that adaptation_field_control is ’01’ or ’11’. When this interrupt is set, both key types, odd and even, for the selected key number, become non valid. SW should update the data key that became non valid. TSPP_KEY_VALID register contains the information regarding the valid keys.

TSPP_IRQ_STATUS (cont.)

Bits	Name	Description
16	KEY_SWITCHED_IRQ	Key switched interrupt is set each time when transport_scrambling_control in the TSP header is changed to scrambled with odd key or even key. When this interrupt is set, same key number with opposite key_type (delving) becomes non valid. SW should update the data key that became non valid. TSPP_KEY_VALID register contains the information regarding the valid keys.
15	PS_BROKEN15	PS_BROKEN interrupt for pipe number 15. Same as PS_BROKEN0.lobal interrupt.
14	PS_BROKEN14	PS_BROKEN interrupt for pipe number 14. Same as PS_BROKEN0.
13	PS_BROKEN13	PS_BROKEN interrupt for pipe number 13. Same as PS_BROKEN0.
12	PS_BROKEN12	PS_BROKEN interrupt for pipe number 12. Same as PS_BROKEN0.
11	PS_BROKEN11	PS_BROKEN interrupt for pipe number 11. Same as PS_BROKEN0.
10	PS_BROKEN10	PS_BROKEN interrupt for pipe number 10. Same as PS_BROKEN0.
9	PS_BROKEN9	PS_BROKEN interrupt for pipe number 9. Same as PS_BROKEN0.
8	PS_BROKEN8	PS_BROKEN interrupt for pipe number 8. Same as PS_BROKEN0.
7	PS_BROKEN7	PS_BROKEN interrupt for pipe number 7. Same as PS_BROKEN0.
6	PS_BROKEN6	PS_BROKEN interrupt for pipe number 6. Same as PS_BROKEN0.
5	PS_BROKEN5	PS_BROKEN interrupt for pipe number 5. Same as PS_BROKEN0.
4	PS_BROKEN4	PS_BROKEN interrupt for pipe number 4. Same as PS_BROKEN0.
3	PS_BROKEN3	PS_BROKEN interrupt for pipe number 3. Same as PS_BROKEN0.
2	PS_BROKEN2	PS_BROKEN interrupt for pipe number 2. Same as PS_BROKEN0.
1	PS_BROKEN1	PS_BROKEN interrupt for pipe number 1. Same as PS_BROKEN0.
0	PS_BROKEN0	PS_BROKEN interrupt per pipe number 0. The interrupt is set when one of the statuses in TSPP_PIPE_ERROR_STATUS0 register is set.

0x18202020 TSPP_IRQ_MASK

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

This is the TSPP interrupt mask register. This register is used to enable the corresponding functions in the TSPP_IRQ_STATUS register. Setting (1) a bit in the TSPP_IRQ_MASK register causes an interrupt to be generated, if the corresponding bit in the TSPP_IRQ_STATUS register is set. Clearing (0) a bit in the TSPP_IRQ_MASK register causes the setting of the corresponding bit in the TSPP_IRQ_STATUS register to have no effect on the interrupt.

TSPP_IRQ_MASK

Bits	Name	Description
19	TSP_RD_CMPL_IRQ	Mask bit if TSP_RD_CMPL_IRQ interrupt.
18	KEY_ERROR_IRQ	Mask bit of KEY_ERROR_IRQ interrupt.
17	KEY_SWITCHED_ILLEGAL_IRQ	Mask bit of KEY_SWITCHED_ILLEGAL_IRQ interrupt.
16	KEY_SWITCHED_IRQ	Mask bit of KEY_SWITCHED_IRQ interrupt.
15	PS_BROKEN15	Mask bit of PS_BROKEN interrupt for pipe number 15.
14	PS_BROKEN14	Mask bit of PS_BROKEN interrupt for pipe number 14.
13	PS_BROKEN13	Mask bit of PS_BROKEN interrupt for pipe number 13.
12	PS_BROKEN12	Mask bit of PS_BROKEN interrupt for pipe number 12.
11	PS_BROKEN11	Mask bit of PS_BROKEN interrupt for pipe number 11.
10	PS_BROKEN10	Mask bit of PS_BROKEN interrupt for pipe number 10.
9	PS_BROKEN9	Mask bit of PS_BROKEN interrupt for pipe number 9.
8	PS_BROKEN8	Mask bit of PS_BROKEN interrupt for pipe number 8.
7	PS_BROKEN7	Mask bit of PS_BROKEN interrupt for pipe number 7.
6	PS_BROKEN6	Mask bit of PS_BROKEN interrupt for pipe number 6.
5	PS_BROKEN5	Mask bit of PS_BROKEN interrupt for pipe number 5.
4	PS_BROKEN4	Mask bit of PS_BROKEN interrupt for pipe number 4.
3	PS_BROKEN3	Mask bit of PS_BROKEN interrupt for pipe number 3.
2	PS_BROKEN2	Mask bit of PS_BROKEN interrupt for pipe number 2.
1	PS_BROKEN1	Mask bit of PS_BROKEN interrupt for pipe number 1.
0	PS_BROKEN0	Mask bit of PS_BROKEN interrupt per pipe number 0.

0x18202024 TSPP_IRQ_CLEAR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

This is the TSPP interrupt clear register. Setting one of this register bits generates a pulse that clears corresponding bit in TSPP_IRQ_STATUS. If one of the PS_BROKEN interrupt bits is cleared, then also all the status bits in the corresponding TSPP_PIPEn_ERROR_STATUS, n = [0..15] register are cleared.

TSPP_IRQ_CLEAR

Bits	Name	Description
19	TSP_RD_CMPL_IRQ	Clear bit of TSP_RD_CMPL_IRQ interrupt.
18	KEY_ERROR_IRQ	Clear bit of KEY_ERROR_IRQ interrupt.
17	KEY_SWITCHED_ILLEGAL_IRQ	Clear bit of KEY_SWITCHED_ILLEGAL_IRQ interrupt.
16	KEY_SWITCHED_IRQ	Clear bit of KEY_SWITCHED_IRQ interrupt.
15	PS_BROKEN15	Clear bit of PS_BROKEN interrupt for pipe number 15.
14	PS_BROKEN14	Clear bit of PS_BROKEN interrupt for pipe number 14.
13	PS_BROKEN13	Clear bit of PS_BROKEN interrupt for pipe number 13.
12	PS_BROKEN12	Clear bit of PS_BROKEN interrupt for pipe number 12.
11	PS_BROKEN11	Clear bit of PS_BROKEN interrupt for pipe number 11.
10	PS_BROKEN10	Clear bit of PS_BROKEN interrupt for pipe number 10.
9	PS_BROKEN9	Clear bit of PS_BROKEN interrupt for pipe number 9.
8	PS_BROKEN8	Clear bit of PS_BROKEN interrupt for pipe number 8.
7	PS_BROKEN7	Clear bit of PS_BROKEN interrupt for pipe number 7.
6	PS_BROKEN6	Clear bit of PS_BROKEN interrupt for pipe number 6.
5	PS_BROKEN5	Clear bit of PS_BROKEN interrupt for pipe number 5.
4	PS_BROKEN4	Clear bit of PS_BROKEN interrupt for pipe number 4.
3	PS_BROKEN3	Clear bit of PS_BROKEN interrupt for pipe number 3.
2	PS_BROKEN2	Clear bit of PS_BROKEN interrupt for pipe number 2.
1	PS_BROKEN1	Clear bit of PS_BROKEN interrupt for pipe number 1.
0	PS_BROKEN0	Clear bit of PS_BROKEN interrupt per pipe number 0.

0x18202028+4*n TSPP_PIPEn_ERROR_STATUS, n=[0..15]

Type: Read
Clock: AHB_CLK
Reset State: 0x0

Those registers hold the error statuses per each pipe. Assertion of one of the error status bits of some pipe causes PS_BROKEN interrupt, which corresponds to that pipe to be set. Clearing PS_BROKEN interrupt of some pipe also clears all the status bits of the register that corresponds to that pipe.

TSPP_PIPEn_ERROR_STATUS

Bits	Name	Description
3	PES_SYNC_ERROR	PES packet didn't start with 0x000001.
2	PS_LENGTH_ERROR	PES packet discarded due to length consistency error.
1	PS_CONTINUITY_ERROR	PES packet discarded due to continuity error.
0	PS_LOST_START	PES packet discarded since the first TSP of the PES was lost.

0x18202068 TSPP_STATUS

Type: Read
Clock: AHB_CLK
Reset State: 0x0

This is a status register that is used for test purposes.

TSPP_STATUS

Bits	Name	Description
13:10	TSP_PKT_AVAIL_STATUS	When one of the bits is set, this means that pipe_number that equals to 8 subtracted from this bit number, contains at least one TS PKT.
9:6	TSIF1_DM_REQ_NUM	Number of TSIF1 DM requests that haven't been served yet.
5:2	TSIF0_DM_REQ_NUM	Number of TSIF0 DM requests that haven't been served yet.
1:0	CURR_FLTR_TABLE_NUM	The currently active PID filter table: 0b00 - Filter table0 0b01 - Filter table1 0b10 - Filter table2 0b11 - Illegal.

0x1820206C TSPP_CURR_TSP_HEADER

Type: Read
Clock: AHB_CLK
Reset State: 0x0

This is a status register that is used for test purposes.

TSPP_CURR_TSP_HEADER

Bits	Name	Description
31:0	CURR_TSP_HEADER	The TSP header of the TSP packet that is currently being processed.

0x18202070 TSPP_CURR_PID_FILTER

Type: Read
Clock: AHB_CLK
Reset State: 0x0

This is a status register that is used for test purposes.

TSPP_CURR_PID_FILTER

Bits	Name	Description
31:0	CURR_PID_FILTER	The PID_FILTER that filtered the TSP packet which is currently being processed.

2.6.4 TSPP scrambling registers

0x18202074+4*n TSPP_SYSTEM_KEY_WORDn, n=[0..7]

Type: Write
Clock: AHB_CLK
Reset State: 0x0

System key words 0 to 7.

WORD0: bits 31 down to 0

WORD1: bits 63 down to 32

WORD2: bits 95 down to 64

WORD3: bits 127 down to 96

WORD4: bits 159 down to 128

WORD5: bits 191 down to 160

WORD6: bits 223 down to 192

WORD7: bits 255 down to 224

TSPP_SYSTEM_KEY_WORDn

Bits	Name	Description
31:0	SYSTEM_KEY_BITS	System key bits.

0x18202094+4*n TSPP_CBC_INIT_VAL_WORDn, n=[0..1]

Type: Write
Clock: AHB_CLK
Reset State: 0x0

CBC initial value words 0 to 1.

WORD0: bits 31 down to 0

WORD1: bits 63 down to 32

TSPP_CBC_INIT_VAL_WORDn

Bits	Name	Description
31:0	CBC_INIT_VAL_BITS	CBC initial value bits.

0x1820209C TSPP_DATA_KEY_RESET

Type: Write
Clock: AHB_CLK
Reset State: 0x0

This is TSPP data key reset register. The reset is a pulse. SW should write to this register only during PID Filters reconfiguration. If after reconfiguration, same data key is going to be used to descramble different TS PKTs stream, SW should reset this data key by writing value of ’1’ to the corresponding bit of the TSPP_KEY_RESET register.

Writing ’1’ to a bit corresponding to specified data key does the following:

- Clears the corresponding bits in TSPP_KEY_VALID resister (both even and odd).
- Clears the corresponding bits in TSPP_KEY_ERROR register.
- Resets some other internal logic in TSPP related to data keys. This will disable KEY_SWITCHED_IRQ due to first received scrambled TS PKT.

TSPP_DATA_KEY_RESET

Bits	Name	Description
7	DATA_KEY7_RESET	Reset pulse for data key number 7.
6	DATA_KEY6_RESET	Reset pulse for data key number 6.
5	DATA_KEY5_RESET	Reset pulse for data key number 5.
4	DATA_KEY4_RESET	Reset pulse for data key number 4.
3	DATA_KEY3_RESET	Reset pulse for data key number 3.
2	DATA_KEY2_RESET	Reset pulse for data key number 2.
1	DATA_KEY1_RESET	Reset pulse for data key number 1.
0	DATA_KEY0_RESET	Reset pulse for data key number 0.

0x182020A0 TSPP_KEY_VALID

Type: Read
Clock: AHB_CLK
Reset State: 0x0

This register holds the valid bits for the data keys.

Valid bit is set(1) when SW updates the corresponding data key in the data keys table.

Valid bit is cleared(0) when the key type in the transport scrambling control is switched from even to odd or from odd to even.

TSPP_KEY_VALID

Bits	Name	Description
15	DATA_ODD_KEY7_VALID	Valid bit for data odd key number 7.
14	DATA_ODD_KEY6_VALID	Valid bit for data odd key number 6.
13	DATA_ODD_KEY5_VALID	Valid bit for data odd key number 5.
12	DATA_ODD_KEY4_VALID	Valid bit for data odd key number 4.
11	DATA_ODD_KEY3_VALID	Valid bit for data odd key number 3.
10	DATA_ODD_KEY2_VALID	Valid bit for data odd key number 2.
9	DATA_ODD_KEY1_VALID	Valid bit for data odd key number 1.
8	DATA_ODD_KEY0_VALID	Valid bit for data odd key number 0.
7	DATA_EVEN_KEY7_VALID	Valid bit for data even key number 7.
6	DATA_EVEN_KEY6_VALID	Valid bit for data even key number 6.
5	DATA_EVEN_KEY5_VALID	Valid bit for data even key number 5.

TSPP_KEY_VALID (cont.)

Bits	Name	Description
4	DATA_EVEN_KEY4_VALID	Valid bit for data even key number 4.
3	DATA_EVEN_KEY3_VALID	Valid bit for data even key number 3.
2	DATA_EVEN_KEY2_VALID	Valid bit for data even key number 2.
1	DATA_EVEN_KEY1_VALID	Valid bit for data even key number 1.
0	DATA_EVEN_KEY0_VALID	Valid bit for data even key number 0.

0x182020A4 TSPP_KEY_ERROR

Type: Read
Clock: AHB_CLK
Reset State: 0x0

This register holds the error bits for the data keys.

Error bit is set(1) when decryption is required, and the data key is not valid. This means that SW didn't update the appropriate data key in time.

Error bit is cleared(0) by SW when clearing the key_error_irq.

TSPP_KEY_ERROR

Bits	Name	Description
7	DATA_KEY7_ERROR	Error bit for data key number 7.
6	DATA_KEY6_ERROR	Error bit for data key number 6.
5	DATA_KEY5_ERROR	Error bit for data key number 5.
4	DATA_KEY4_ERROR	Error bit for data key number 4.
3	DATA_KEY3_ERROR	Error bit for data key number 3.
2	DATA_KEY2_ERROR	Error bit for data key number 2.
1	DATA_KEY1_ERROR	Error bit for data key number 1.
0	DATA_KEY0_ERROR	Error bit for data key number 0.

2.6.5 TEST bus control register

0x182020A8 TSPP_TEST_CTRL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

TSPP test bus control register.

TSPP_TEST_CTRL

Bits	Name	Description
7	TEST_BUS_EN	Test bus enable. When clear(0), tspp_test_bus is all zero.
6:0	TEST_BUS_SEL	Test bus selector: ¨ Parser test buses 0b1110010: dout_test_bus (multi2) 0b1110001: control_test_bus (multi2) 0b1110000: iif_test_bus (multi2) 0b1100111: parser_config_test_bus 0b1100110: ctx_test_bus 0b1100101: tsp2es_test_bus 0b1100100: pl_dec_test_bus 0b1100011: af_proc_test_bus 0b1100010: proc_ctrl_test_bus 0b1100001: main_ctrl_test_bus2 0b1100000: main_ctrl_test_bus1 ¨ TS ifc. test buses 0b0100101: mem2tsp_test_bus 0b0100100: cons_ahb2mem_test_bus 0b0100011:ts_ahb2mem_test_bus 0b0100010: ts_cons_arb_test_bus 0b0100001: ts_ifc_arb_test_bus 0b0100000: ts_fsms_test_bus ¨ Prod test buses 0b0010001: fifo2ahb_test_bus 0b0010000: es2fifo_test_bus ¨ Other test buses 0b0000001: mem_ctrl_test_bus 0b0000000: regs_test_bus

2.6.6 TSPP other registers

0x182020AC TSPP_VERSION

Type: Read
Clock: AHB_CLK
Reset State: 0x1

TSPP version register. The register holds current TSPP version.

TSPP_VERSION

Bits	Name	Description
7:0	TSPP_VERSION	Current TSPP version.

0x182020B0 TSPP_GENERICS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The register holds TSPP generics values. It is used to identify which generic values are used at TSPP instantiation.

TSPP_GENERICS

Bits	Name	Description
12	CRYPTO_GEN	CRYPTO_GEN generic parameter value.
11:7	MAX_CONS_PIPES	MAX_CONS_PIPES generic parameter value. Typical value 4.
6:2	MAX_PIPES	MAX_PIPES generic parameter value. Typical value 16.
1	TSIF_1_GEN	TSIF_1_GEN generic parameter value.
0	TSIF_0_GEN	TSIF_0_GEN generic parameter value.

0x182020B4 TSPP_NOP

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The register has four no operational bits. It is reserved for future use.

TSPP_NOP

Bits	Name	Description
3:0	TSPP_NOP	TSPP nop register bits.

2.6.7 TSPP PID FILTER and CONFIG registers (RAM based)

There are sixteen PID filters in each PID filter table. This allows up to sixteen different pipes to which PIDs may be routed.

Each TSP may be processed twice by the same filter. This depends on PIPE_PROCESS0, PIPE_PROCESS1 and rest of filter parameters.

After SW configured PID filter and config registers, HW operates as follows:

- New TS PKT is received, and PID is retrieved from PKT header.
- PID filter registers are registers are read from lower to higher address.
- For each filter PIPE_PROCESS0 is checked:
- When DISABLED:
- The register is skipped.
- When TSP_RAW_PROCESSING | TSP_RAW_NO_SUFFIX:
- If (PID & PID_MASK = PIPE_PID & PID_MASK):
- PID config register is read.
- The TSP packet is routed to pipe with PIPE_NUMBER0.
- RAW Processing is performed on the TSP.
- If PIPE_PROCESS1 /= DISABLED:
- The TSP is processed again based on PIPE_PROCESS1, PIPE_NUMBER1, and other filter parameters.
- ELSE
- The register is skipped.
- When PES_PROCESSING
- If (PID = PIPE_PID):
- PID config register is read.
- The TSP packet is routed to pipe with PIPE_NUMBER.
- PES Processing is performed on the TSP.
- If PIPE_PROCESS1 /= DISABLED:
- The TSP is processed again based on PIPE_PROCESS1, PIPE_NUMBER1, and other filter parameters.
- ELSE
- The register is skipped.
- If all registers were skipped, the TSP packet is ignored. Corresponding interrupt is generated, and corresponding performance counter is updated.

Notes for SW configuration.

- PID filter registers are searched till the first match. This means that PID filter registers with higher addresses have lower priority.
- All PID filter registers of PES Processing should be located at lower addresses than PID filter registers of Raw Processing, in order not to mask them mistakenly. The reason specified in the previous bullet.
- PIPE_MASK filed is used only in TSP RAW processing.
- SW may set PIPE_MASK to 0x1FFF and PIPE_PROCESS to Raw in order to rout all unmatched PIDs to some pipe and not to ignore them. PID filter search will be completed if PIPE_MASK = 0x1FFF and PIPE_PROCESS = Raw is encountered.
- If PS_DISABLE bit of the corresponding PIPE in the TSPP_PS_DISABLE register is set(1), the TS PKT is ignored.

0x18202800+ 8*n TSPP_PID_FILTERn_TABLE0, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

This is TSPP PID filter register set of PID filter table1 interface.

There are sixteen PID filters for PID filter table1. This allows up to sixteen different pipes to which PIDs may be routed.

TSPP_PID_FILTERn_TABLE0

Bits	Name	Description
31:30	PIPE_PROCESS0	Process level for the filtered PID, when TSP is processed for the first time. 0x3: TSP_RAW_NO_SUFFIX 0x2: TSP_RAW_PROCESSING 0x1: PES_PROCESSING 0x0: DISABLED
29:26	NOT_USED	Not used bits.
25:13	PIPE_PID	Collect that PID.
12:0	PID_MASK	Define don't care bits of the PIPE_PID. Note that PIPE_MASK is used only if PIPE_PROCESS = TSP_RAW_PROCESSING.

0x18202804+ 8*n TSPP_PID_CONFIGn_TABLE0, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

This is TSPP PID config register set for Filter table1.

TSPP_PID_CONFIGn_TABLE0

Bits	Name	Description
31:30	PIPE_PROCESS1	Same as PIPE_PROCESS0, only for the second time processing of the same TSP. When PIPE_PROCESS0 = DISABLED. PIPE_PROCESS1 is irrelevant.
29:24	NOT_USED1	Not used bits.
23	TSP_HEADER_ERR_MASK 1	Same as TSP_HEADER_ERR_MASK0, only for the second time processing of the TSP.
22	TRANS_END_DISABLE1	Same as TRANS_END_DISABLE0, only for the second time processing of the TSP. Relevant for PIPE_NUMBER1.
21	DEC_ON_ERR_EN1	Same as DEC_ON_ERR_EN0, only for the second time processing of the TSP.
20	SCRAMB_EN1	Same as SCRAMB_EN0, only for the second time processing of the TSP.
19:16	PIPE_NUMBER1	Same as PIPE_NUMBER0, only for the second time processing of the TSP.
15:11	NOT_USED0	Not used bits.
10:8	KEY_NUMBER	Data key number that should be used when TSP payload decryption is required.
7	TSP_HEADER_ERR_MASK 0	This bit is used when the TSP is processed for the first time. When this bit is set(1), TSP header errors are tested as usual, depending on TSP_SYNC_ERROR_MASK, and TSP_ERROR_INDICATOR_MASK. When this bit is clear(0), TSP header errors are not tested. TSP is written into the pipe if there are no other errors.
6	TRANS_END_DISABLE0	This bit controls the behavior of transaction_end output port for PIPE_NUMBER0. This control bit should be set only per pipes that were configured for Raw processing. When this bit is clear(0), each TSP, transaction_end signal is asserted. When this bit is set(1), transaction_end signal is never asserted. This control bit allows SW to allocate pipe descriptors per several TSPs, and not per each TSP. When this bit is set(1), the sizes of pipe descriptors, should be exact multiples of TSIF packet size (192 bytes).
5	DEC_ON_ERR_EN0	Decryption enabled on error. When this bit is set(1), TSPP performs TSP payload decryption when required also if there is an error in TSP header and the error is not masked (if the error is masked the packet is discarded). When this bit is clear(0), TSPP doesn’t perform TSP payload decryption when there is and error in TSP header.

TSPP_PID_CONFIGn_TABLE0 (cont.)

Bits	Name	Description
4	SCRAMB_EN0	Scrambling enable bit for the TSP when it is processed for the first time. When this bit is set(1), TSPP performs TSP payload decryption as defined by transport_scrambling_control bits in the TSP header. When this bit is clear(0), TSPP ignores the transport_scrambling_control bits in the TSP header. TS PKTs payload sent as is, without decryption.
3:0	PIPE_NUMBER0	The filtered PID will be routed to this pipe number when the TSP is processed for the first time.

0x18202880+ 8*n TSPP_PID_FILTERn_TABLE1, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

This is TSPP PID filter register set of PID filter table1 interface.

There are sixteen PID filters for PID filter table1. This allows up to sixteen different pipes to which PIDs may be routed.

TSPP_PID_FILTERn_TABLE1

Bits	Name	Description
31:30	PIPE_PROCESS0	Process level for the filtered PID, when TSP is processed for the first time. 0x3: TSP_RAW_NO_SUFFIX 0x2: TSP_RAW_PROCESSING 0x1: PES_PROCESSING 0x0: DISABLED
29:26	NOT_USED	Not used bits.
25:13	PIPE_PID	Collect that PID.
12:0	PID_MASK	Define don’t care bits of the PIPE_PID. Note that PIPE_MASK is used only if PIPE_PROCESS = TSP_RAW_PROCESSING.

0x18202884+ 8*n TSPP_PID_CONFIGn_TABLE1, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

This is TSPP PID config register set for Filter table1.

TSPP_PID_CONFIGn_TABLE1

Bits	Name	Description
31:30	PIPE_PROCESS1	Same as PIPE_PROCESS0, only for the second time processing of the same TSP. When PIPE_PROCESS0 = DISABLED. PIPE_PROCESS1 is irrelevant.
29:24	NOT_USED1	Not used bits.
23	TSP_HEADER_ERR_MASK 1	Same as TSP_HEADER_ERR_MASK0, only for the second time processing of the TSP.
22	TRANS_END_DISABLE1	Same as TRANS_END_DISABLE0, only for the second time processing of the TSP. Relevant for PIPE_NUMBER1.
21	DEC_ON_ERR_EN1	Same as DEC_ON_ERR_EN0, only for the second time processing of the TSP.
20	SCRAMB_EN1	Same as SCRAMB_EN0, only for the second time processing of the TSP.
19:16	PIPE_NUMBER1	Same as PIPE_NUMBER0, only for the second time processing of the TSP.
15:11	NOT_USED0	Not used bits.
10:8	KEY_NUMBER	Data key number that should be used when TSP payload decryption is required.
7	TSP_HEADER_ERR_MASK 0	This bit is used when the TSP is processed for the first time. When this bit is set(1), TSP header errors are tested as usual, depending on TSP_SYNC_ERROR_MASK, and TSP_ERROR_INDICATOR_MASK. When this bit is clear(0), TSP header errors are not tested. TSP is written into the pipe if there are no other errors.
6	TRANS_END_DISABLE0	This bit controls the behavior of transaction_end output port for PIPE_NUMBER0. This control bit should be set only per pipes that were configured for Raw processing. When this bit is clear(0), each TSP, transaction_end signal is asserted. When this bit is set(1), transaction_end signal is never asserted. This control bit allows SW to allocate pipe descriptors per several TSPs, and not per each TSP. When this bit is set(1), the sizes of pipe descriptors, should be exact multiples of TSIF packet size (192 bytes).
5	DEC_ON_ERR_EN0	Decryption enabled on error. When this bit is set(1), TSPP performs TSP payload decryption when required also if there is an error in TSP header and the error is not masked (if the error is masked the packet is discarded). When this bit is clear(0), TSPP doesn't perform TSP payload decryption when there is and error in TSP header.
4	SCRAMB_EN0	Scrambling enable bit for the TSP when it is processed for the first time. When this bit is set(1), TSPP performs TSP payload decryption as defined by transport_scrambling_control bits in the TSP header. When this bit is clear(0), TSPP ignores the transport_scrambling_control bits in the TSP header. TS PKTs payload sent as is, without decryption.

TSPP_PID_CONFIGn_TABLE1 (cont.)

Bits	Name	Description
3:0	PIPE_NUMBER0	The filtered PID will be routed to this pipe number when the TSP is processed for the first time.

0x18202900+ 8*n TSPP_PID_FILTERn_TABLE2, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

This is TSPP PID filter register set of PID filter table1 interface.

There are sixteen PID filters for PID filter table1. This allows up to sixteen different pipes to which PIDs may be routed.

TSPP_PID_FILTERn_TABLE2

Bits	Name	Description
31:30	PIPE_PROCESS0	Process level for the filtered PID, when TSP is processed for the first time. 0x3: TSP_RAW_NO_SUFFIX 0x2: TSP_RAW_PROCESSING 0x1: PES_PROCESSING 0x0: DISABLED
29:26	NOT_USED	Not used bits.
25:13	PIPE_PID	Collect that PID.
12:0	PID_MASK	Define don’t care bits of the PIPE_PID. Note that PIPE_MASK is used only if PIPE_PROCESS = TSP_RAW_PROCESSING.

0x18202904+ 8*n TSPP_PID_CONFIGn_TABLE2, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

This is TSPP PID config register set for Filter table1.

TSPP_PID_CONFIGn_TABLE2

Bits	Name	Description
31:30	PIPE_PROCESS1	Same as PIPE_PROCESS0, only for the second time processing of the same TSP. When PIPE_PROCESS0 = DISABLED. PIPE_PROCESS1 is irrelevant.
29:24	NOT_USED1	Not used bits.
23	TSP_HEADER_ERR_MASK 1	Same as TSP_HEADER_ERR_MASK0, only for the second time processing of the TSP.
22	TRANS_END_DISABLE1	Same as TRANS_END_DISABLE0, only for the second time processing of the TSP. Relevant for PIPE_NUMBER1.
21	DEC_ON_ERR_EN1	Same as DEC_ON_ERR_EN0, only for the second time processing of the TSP.
20	SCRAMB_EN1	Same as SCRAMB_EN0, only for the second time processing of the TSP.
19:16	PIPE_NUMBER1	Same as PIPE_NUMBER0, only for the second time processing of the TSP.
15:11	NOT_USED0	Not used bits.
10:8	KEY_NUMBER	Data key number that should be used when TSP payload decryption is required.
7	TSP_HEADER_ERR_MASK 0	This bit is used when the TSP is processed for the first time. When this bit is set(1), TSP header errors are tested as usual, depending on TSP_SYNC_ERROR_MASK, and TSP_ERROR_INDICATOR_MASK. When this bit is clear(0), TSP header errors are not tested. TSP is written into the pipe if there are no other errors.
6	TRANS_END_DISABLE0	This bit controls the behavior of transaction_end output port for PIPE_NUMBER0. This control bit should be set only per pipes that were configured for Raw processing. When this bit is clear(0), each TSP, transaction_end signal is asserted. When this bit is set(1), transaction_end signal is never asserted. This control bit allows SW to allocate pipe descriptors per several TSPs, and not per each TSP. When this bit is set(1), the sizes of pipe descriptors, should be exact multiples of TSIF packet size (192 bytes).
5	DEC_ON_ERR_EN0	Decryption enabled on error. When this bit is set(1), TSPP performs TSP payload decryption when required also if there is an error in TSP header and the error is not masked (if the error is masked the packet is discarded). When this bit is clear(0), TSPP doesn’t perform TSP payload decryption when there is and error in TSP header.
4	SCRAMB_EN0	Scrambling enable bit for the TSP when it is processed for the first time. When this bit is set(1), TSPP performs TSP payload decryption as defined by transport_scrambling_control bits in the TSP header. When this bit is clear(0), TSPP ignores the transport_scrambling_control bits in the TSP header. TS PKTs payload sent as is, without decryption.

TSPP_PID_CONFIGn_TABLE2 (cont.)

Bits	Name	Description
3:0	PIPE_NUMBER0	The filtered PID will be routed to this pipe number when the TSP is processed for the first time.

2.6.8 TSPP GLOBAL PERFORMANCE COUNTERS registers (RAM based)

TSPP performance counters are used to collect statistics of different events that occurred while TSP packets were received and processed.

TSPP global performance counters collect statistics of TSP packets before they were routed to a pipe.

Performance counters should be initialized by SW by writing values of 0x0 before TSPP block operation is started.

The counters are incremented by TSPP HW, and never reset.

Resetting performance counters should be performed by SW by writing value of 0x0 to each counter.

0x18202980 TSPP_TSP_TOTAL_NUM

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

TSPP_TSP_TOTAL_NUM

Bits	Name	Description
31:0	TSP_TOTAL_NUM	Number of all packets from HW.

0x18202984 TSPP_TSP_IGNORED_NUM

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

TSPP_TSP_IGNORED_NUM

Bits	Name	Description
31:0	TSP_IGNORED_NUM	Number of TSPs not routed to any pipe.

0x18202988 TSPP_TSP_ERROR_INDICATOR_NUM

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

TSPP_TSP_ERROR_INDICATOR_NUM

Bits	Name	Description
31:0	TSP_ERROR_INDICATOR_NUM	Number of TSPs with Reed Solomon failure.

0x1820298C TSPP_TSP_SYNC_ERROR_NUM

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

TSPP_TSP_SYNC_ERROR_NUM

Bits	Name	Description
31:0	TSP_SYNC_ERROR_NUM	Number of TSPs did not start with 0x47

2.6.9 TSPP PIPE CONTEXT registers (RAM based)

0x18202990+40*n TSPP_PIPEn_CONTEXT0, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

This is TSPP pipe context register set. Together with TSPP_PIPEn_CONTEXT1, n = [0..15] register, those registers contain pipe context information.

There are sixteen pipe context registers sets, each register per one pipe.

Notes for SW configuration:

- Most of context registers bit fields are only for test purposes.
- SW may read context registers to see context information of a pipe.
- SW should initialize PS_STATE of each context to PS_EMPTY (PS_LOST_START interrupt will be generated if in the first received TSP payload_unit_start_indicator is not set) or to PS_BROKEN_NO_RETRANS (will not generate PS_LOST_START interrupt before first PES is assembled), before activating TSPP module.

- SW may write values to context registers. SW writes to those registers while TSPP module is active, will bring to undefined results.

TSPP_PIPEn_CONTEXT0

Bits	Name	Description
31:16	PES_BYTES_LEFT	Down counter. Number of bytes that are still expected to complete PES PKT assembly. In case of UNSP_PES_LENGTH = '1', PES_BYTES_LEFT = 0x0.
15:12	CONTINUITY_COUNTER	Continuity counter of the last packet received for the PES being constructed.
11	UNSP_PES_LENGTH	Unspecified PES packet length. Asserted when PES_packet_length field in the PES header.
10:2	NOT_USED	currently not used bits.
1:0	PS_STATE	PS_STATE of the constructed PES: 0b11 - PS_BROKEN_NO_RETRANS 0b10 - PS_BROKEN_RETRANS 0b01 - PS_CONSTRUCTING 0b00 - PS_EMPTY

0x18202994+ 40*n TSPP_PIPEn_CONTEXT1, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

See description of TSPP_PIPEn_CONTEXT0, n = [0..15].

TSPP_PIPEn_CONTEXT1

Bits	Name	Description
31:0	TSIF_SUFFIX	TSIF suffix of the first TSP of the PES.

2.6.10 TSPP PIPE PERFORMANCE COUNTERS registers (RAM based)

TSPP pipe performance counters collect statistics of TSP packets after they were routed to some pipe. Pipe performance counters collect statistics per pipe.

0x18202998+ 40*n TSPP_PIPE_TSP_TOTAL_NUMn, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

TSPP_PIPE_TSP_TOTAL_NUMn

Bits	Name	Description
31:0	PIPE_TSP_TOTAL_NUM	Number of TSP routed to this pipe. Relevant to RAW and PES precessing.

0x1820299C+ 40*n TSPP_PS_DUPLICATE_TSP_NUMn, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

TSPP_PS_DUPLICATE_TSP_NUMn

Bits	Name	Description
31:0	PS_DUPLICATE_TSP_NUM	Number of duplicate TSPs. Relevant only to PES precessing.

0x182029A0+ 40*n TSPP_TSP_NO_PAYLOAD_NUMn, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

TSPP_TSP_NO_PAYLOAD_NUMn

Bits	Name	Description
31:0	TSP_NO_PAYLOAD_NUM	Number of TSPs without payload. Relevant only to PES precessing.

0x182029A4+ 40*n TSPP_TSP_BROKEN_PS_NUMn, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

TSPP_TSP_BROKEN_PS_NUMn

Bits	Name	Description
31:0	TSP_BROKEN_PS_NUM	Number of TSPs thrown since PES is broken. Relevant only to PES precessing.

0x182029A8+40*n TSPP_PS_TOTAL_NUMn, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

TSPP_PS_TOTAL_NUMn

Bits	Name	Description
31:0	PS_TOTAL_NUM	Total number of PES constructed.

0x182029AC+40*n TSPP_PS_CONTINUITY_ERROR_NUMn, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

TSPP_PS_CONTINUITY_ERROR_NUMn

Bits	Name	Description
31:0	PS_CONTINUITY_ERROR_NUM	Number of PES packets discarded due to continuity error. Relevant only to PES precessing.

0x182029B0+40*n TSPP_PS_LENGTH_ERROR_NUMn, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

TSPP_PS_LENGTH_ERROR_NUMn

Bits	Name	Description
31:0	PS_LENGTH_ERROR_NUM	Number of PES packets discarded due to length consistency error. Relevant only to PES precessing.

0x182029B4+40*n TSPP_PES_SYNC_ERROR_NUMn, n=[0..15]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

TSPP_PES_SYNC_ERROR_NUMn

Bits	Name	Description
31:0	PES_SYNC_ERROR_NUM	Number of PES packets that didn't start with 0x000001. Relevant only to PES precessing.

2.6.11 TSPP TS PKT buffer

0x18202C10+4*n TSPP_TSP_BUFF_WORDn, n=[0..47]

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

This register set points to the TS PKT that was received from BAM consumer PIPE. Those registers may be accessed by SW only for test purposes. Writing to those registers while TSPP operation will lead to undefined TSPP behavior.

TSPP_TSP_BUFF_WORDn

Bits	Name	Description
31:0	TSPP_TSP_BUFF_WORD	The register points to the TS PKT that was received from BAM consumer pipe.

2.6.12 TSPP DATA KEYS registers (RAM based)

0x18202CD0+16*n TSPP_DATA_EVEN_KEYn_LSB, n=[0..7]

Type: Write
Clock: AHB_CLK
Reset State: Undefined

Those registers hold the LSB bits of even data keys.

TSPP_DATA_EVEN_KEYn_LSB

Bits	Name	Description
31:0	DATA_EVEN_KEY_LSB	LSB bits of data even key.

0x18202CD4+16*n TSPP_DATA_EVEN_KEYn_MSB, n=[0..7]

Type: Write
Clock: AHB_CLK
Reset State: Undefined

Those registers hold the MSB bits of even data keys.

TSPP_DATA_EVEN_KEYn_MSB

Bits	Name	Description
31:0	DATA_EVEN_KEY_MSB	MSB bits of data even key.

0x18202CD8+16*n TSPP_DATA_ODD_KEYn_LSB, n=[0..7]

Type: Write
Clock: AHB_CLK
Reset State: Undefined

Those registers hold the LSB bits of odd data keys.

TSPP_DATA_ODD_KEYn_LSB

Bits	Name	Description
31:0	DATA_ODD_KEY_LSB	LSB bits of data even key.

0x18202CDC +16*n TSPP_DATA_ODD_KEYn_MSB, n=[0..7]

Type: Write
Clock: AHB_CLK
Reset State: Undefined

Those registers hold the MSB bits of odd data keys.

TSPP_DATA_ODD_KEYn_MSB

Bits	Name	Description
31:0	DATA_ODD_KEY_MSB	MSB bits of data even key.

2.7 CFPB SPLT Config (System FPB) Registers (0x17F00000 CSYSFPB_SPL_BASE)

This section contains Chip System FPB registers.

0x17F00000 CSYSFPB_SPL_CFPB_SPLT_CTRL_STATUS

Type: Read/Write
Clock: CC_CFPB_SPLT_CLK
Reset State: 0x00000000

This register is a general configuration register.

CSYSFPB_SPL_CFPB_SPLT_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables Power up value is clear (0)
11	RPM_PROC_IRQ_EN	SW: RW, HW: R RPMProcessorInterruptEnable When set, the RPM processor receives an interrupt whenever ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	APPS_PROC_IRQ_EN	SW: RW, HW: R Apps_ProcInterruptEnable When set, the Application Processor receives an interrupt whenever ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

CSYSFPB_SPL_CFPB_SPLT_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x5: Select the S0_M0 ahb2ahb bridge test bus. 0x6: Select the S1_M1 ahb2ahb bridge test bus. 0x7: Select the M0 ahb2ahb bridge test bus. 0x8: Select the M1 ahb2ahb bridge test bus. 0x9: Select the M2 ahb2ahb bridge test bus. 0xA: Select the M3 ahb2ahb bridge test bus. 0xB: Select the M4 ahb2ahb bridge test bus. 0xC: Select the M5 ahb2ahb bridge test bus. 0xD: Select the M6 ahb2ahb bridge test bus. 0xE: Select the M7 ahb2ahb bridge test bus. 0xF: Select the M8 ahb2ahb bridge test bus. 0x10: Select the M9 ahb2ahb bridge test bus. 0x11: Select the M10 ahb2ahb bridge test bus. 0x12: Select the M11 ahb2ahb bridge test bus. 0x13: Select the M12 ahb2ahb bridge test bus. 0x14: Select the M13 ahb2ahb bridge test bus. 0x15: Select the M14 ahb2ahb bridge test bus. 0x16: Select the M15 ahb2ahb bridge test bus.

0x17F00044 CSYSFPB_SPL_CFPB_SPLT_PORT_EN

Type: Read/Write
Clock: CC_CFPB_SPLT_CLK
Reset State: 0xFFFFFFFF

This register is the CFPB_SPLT master port enable register.

CSYSFPB_SPL_CFPB_SPLT_PORT_EN

Bits	Name	Description
31:1	RESERVED_BIT31_1	Only one master port is used.

CSYSFPB_SPL_CFPB_SPLT_PORT_EN (cont.)

Bits	Name	Description
0	M0_PORT_EN	SW: RW, HW: R M0PortEnable When cleared (0), M0 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

0x17F00050 CSYSFPB_SPL_CFPB_SPLT_ERROR_STAT

Type: Read/Write
Clock: CC_CFPB_SPLT_CLK
Reset State: 0x00000000

This register is the bus error status register.

CSYSFPB_SPL_CFPB_SPLT_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the channel ID that caused the detected error when CID is valid for the master of the access. If not, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	

CSYSFPB_SPL_CFPB_SPLT_ERROR_STAT (cont.)

Bits	Name	Description
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Master0 0x1: Master1 0x2: Master2 0x3: Master3 0x4: Master4 0x5: Master5 0x6: Master6 0x7: Master7 0x8: Master8 0x9: Master9 0xA: Master10 0xB: Master11 0xC: Master12 0xD: Master13 0xE: Master14 0xF: Master15
11:10	RESERVED_BITS11_10	
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit

CSYSFPB_SPL_CFPB_SPLT_ERROR_STAT (cont.)

Bits	Name	Description
3:2	RESERVED_BIT3_2	
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted. Clearing (0) this bit clears any interrupts asserted as well as enables the ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x17F00054 CSYSFPB_SPL_CFPB_SPLT_ERROR_ADDR

Type: Read
Clock: CC_CFPB_SPLT_CLK
Reset State: 0x00000000

This register contains the bus error address.

CSYSFPB_SPL_CFPB_SPLT_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x17F0005C CSYSFPB_SPL_CFPB_SPLT_XPU_ACR

Type: Read/Write
Clock: CC_CFPB_SPLT_CLK
Reset State: 0xFFFFFFFF

The CFPB_SPLT_XPU_ACR register is the CFPB_SPLT Access Control Register for configuring register protection.

CSYSFPB_SPL_CFPB_SPLT_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R CFPB_SPLT XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the CFPB_SPLT configure space, including this register itself. Power up value is set (1)

0x17F00060 CSYSFPB_SPL_CFPB_SPLT_HW_CLK_GATING_CFG

Type: Read/Write
Clock: CC_CFPB_SPLT_CLK
Reset State: 0x00000000

The CFPB_SPLT_HW_CLK_GATING_CFG register is for hardware clock gating configuration.

CSYSFPB_SPL_CFPB_SPLT_HW_CLK_GATING_CFG

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	HYSTERESIS_CNT_SW	SW: RW, HW: R Hysteresis Counter Value This field is used by SW to set the hysteresis counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)
3:0	WAKE_CNT_SW	SW: RW, HW: R Wakeup Counter Value This field is used by SW to set the wakeup counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)

2.8 BAM registers (0x18204000 TSIF_BAM_BASE)

This section contains TSIF BAM registers.

BAM supports only Word (4 byte) aligned writes and reads on the Configuration Bus interface.

BAM has MAX_PIPES hardware generic parameter defining the number of pipes it supports. Each BAM can have up to 31 pipes supported.

BAM has BAM_CONF_AHBS_ADDR_WIDTH hardware generic parameter defining the Bit Number for selecting BAM access or Peripheral access. Legal Ranges are 14 to 20. Count starts from 1, meaning a value of 17 will set BAM Base address as 0x0001_0000.

The following data applies to these registers:

- bam_addr addr range = 11:2 - At maximum (31 pipes) BAM addresses demand 11:2 bits address space. Additional BAM_CONF_AHBS_ADDR_WIDTH bit (12 or higher) selects BAM/Peripheral.

2.8.1 BAM control registers

BAM Control registers configure the BAM operational state, SW reset, interrupts and others.

0x18204F80 TSIF_BAM_CTRL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

BAM Control register allows global controls for the BAM.

TSIF_BAM_CTRL

Bits	Name	Description
31:17	RESERVED_BITS31_17	Set to Zero (0)
16	IBC_DISABLE	This Bit enables power saving by disabling the inactivity clock timer/counter. This is useful when: 1) The BAM is Enabled but idling for long periods. 2) The BAM is Enabled and running but the inactivity timers/counters are not required by the SW for operating the BAM. When the BAM is Disabled, it automatically shuts down those timers to save power. 0’b1 - Enable Power Saving Mode 0’b0 - Disable Power Saving Mode

TSIF_BAM_CTRL (cont.)

Bits	Name	Description
15	BAM_CACHED_DESC_STORE	This Bit enables storage of a cached Descriptor into RAM when doing Context Switch and loading it back when returning to this pipe. This is relevant for System Modes Only. BAM to BAM Consumer mode doesn't have this option. Enabling this makes the Context Switch process slightly longer but reduces AHB Descriptor Fetch time later on. It also reduces the number of descriptor fetches done by the BAM if BAM is treating more than 2 pipes. 1’b1 - Enabled 0x0 - Disabled Available in BAM only
14:13	BAM_DESC_CACHE_SEL	This Selector chooses which Descriptor Caching mode will be used. This is relevant for System Producer or Consumer modes only. 0x00 - Cache when current descriptor has less than 64 bytes left. 0x01 - Cache when current descriptor has less than 128 bytes left. 0x10 - Immediate Auto cache - cache will happen whenever there are no descriptors cached. This might cause unnecessary descriptors reads when switching between more than 2 pipes. It is the most effective when each pipe processes more bytes than there are in an average descriptor (small descriptors, big block size), or when working with 2 or less pipes. 0x11 - Cache when descriptor is needed only. This results in 1 descriptor present in cache at most. Available in BAM only
12	RESERVED_BITS12	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_SIC_SEL
11:5	BAM_TESTBUS_SEL	Set to Zero (0) Obsolete field
4	BAM_EN_ACCUM	When Enabled, BAM will accumulate data written by the peripheral in Direct Mode into INCR8 Bursts. This is an optimization feature for Producer Direct Mode cases. 0x1 - Enabled 0x0 - Disabled Available in BAM only
3	RESERVED_BITS3	Set to Zero (0)
2	RESERVED_BITS2	Set to Zero (0)

TSIF_BAM_CTRL (cont.)

Bits	Name	Description
1	BAM_EN	After reset the BAM wakes up in Disabled Mode. While Disabled, BAM operates in Legacy mode (all the transfers from the peripheral go around the BAM as if it doesn't exist) Software Enables this bit to allow BAM operation. This bit doesn't affect the PIPE enable bit in BAM_P_CTRL register. The only possibility to Disable the BAM after it has been enabled is by Hardware or Software reset. 0x1 - Enabled 0x0 - Disabled
0	BAM_SW_RST	This will reset the BAM & all Pipes. Software may use this to reset the BAM. As long as the bit remains high the BAM remains in reset state. Software should clear this bit 0x1 - Reset state 0x0 - Normal state

0x18204F84 TSIF_BAM_REVISION

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a hard coded revision number of the BAM RTL. This corresponds to the BAM target number in the IMS. Also additional BAM settings are reflected here.

TSIF_BAM_REVISION

Bits	Name	Description
31:24	INACTIV_TMR_BASE	This indicates the width of the inactivity timers base counter
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	NUM_INACTIV_TMRS	This bit is checked only if INACTIV_TMRS_EXST = 1. This bit indicates how many inactivity timers are implemented according to value of INACTIVITY_TIMERS_SUPPORTED generic: 0x1 - One timer for global BAM activity (INACTIVITY_TIMERS_SUPPORTED = 1) 0x0 - MAX_PIPES timers for each pipe activity (INACTIVITY_TIMERS_SUPPORTED = 2)
19	INACTIV_TMRS_EXST	This indicates BAM has inactivity timers. 0x1 - Timers available (INACTIVITY_TIMERS_SUPPORTED = 1 or 2) 0x0 - No timers available (INACTIVITY_TIMERS_SUPPORTED = 0)

TSIF_BAM_REVISION (cont.)

Bits	Name	Description
18	HIGH_FREQUENCY_BAM	This indicates BAM has Double Sampling on the Ack On Success interface. 0x1 - Ack On Success double sampled 0x0 - No double sampling of Ack On Success
17	BAM_HAS_NO_BYPASS	This field indicates BAM has no bypass on the AHB Data bus, from the Peripheral AHB Master to the fabric. When Bypass is available, it is the default routing when BAM is disabled. 0x1 - No Bypass 0x0 - Bypass Exists
16	SECURED	This field indicates BAM/BAM-Lite has security support (APU inside) 0x1 - Secured 0x0 - Not Secured
15:12	RESERVED_BITS15_12	Set to Zero (0)
11:8	NUM_EES	This indicates the Number of Interrupt Lines (Execution Environments) supported by the BAM. When 1 EE is supported, only the BAM_IRQ_SRCS*_EE0 registers exist. When 4 EEs are supported, all BAM_IRQ_SRCS*_EEn registers exist for n=[0..3].
7:0	REVISION	This field contains the revision number of the core, Hard Coded.

0x18204FBC TSIF_BAM_NUM_PIPES

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a the hard coded number of pipes in the BAM. Since each BAM may have a different number of pipes instantiated in HW, this register allows the SW to know this parameter. The reset state value doesn't have any meaning in this register since it is a constant.

TSIF_BAM_NUM_PIPES

Bits	Name	Description
31:24	BAM_NON_PIPE_GRP	This field contains the number of BAM Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
23:16	PERIPH_NON_PIPE_GRP	This field contains the number of Peripheral's Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
15:8	RESERVED_BITS15_8	Set to Zero (0)

TSIF_BAM_NUM_PIPES (cont.)

Bits	Name	Description
7:0	BAM_NUM_PIPES	This field contains the number of pipes available in this BAM

0x18204FC0 TSIF_BAM_TIMER

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the BAM (all the pipes are in idle state).

TSIF_BAM_TIMER

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x18204FC4 TSIF_BAM_TIMER_CTRL

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The register can be written and read only when INACTIVITY_TIMERS_SUPPORTED generic equals to 1.

The resolution of the BAM inactivity timer are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the TIMER_THRSHLD is 10 will indicate the 2^3*1us*10, which is 80us of inactivity in a

pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * TIMER_TRSHLD.

TSIF_BAM_TIMER_CTRL

Bits	Name	Description
31	TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1 to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the TIMER_THRESOLD value 0x1 - Active 0x0 - Reset
30	TIMER_RUN	Will be used along with TIMER_MODE Not implemented at this time. Set to zero(0)
29	TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x18204F88 TSIF_BAM_DESC_CNT_TRSHLD

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds a threshold value for the counter summing the Size of the Descriptors Provided. This value is Global for all pipes but it is relevant for System Producer BAM mode and Both Consumer modes, where Descriptors summing takes place in order to provide the information to the peripheral via pipe bytes free (producer) or pipe bytes available interfaces.

TSIF_BAM_DESC_CNT_TRSHLD

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0).
15:0	CNT_TRSHLD	Threshold value. The maximum allowed value is 32kByte. Available in BAM only

0x18204F8C TSIF_BAM_IRQ_SRCS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking out this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register points to the physical BAM_IRQ_SRCS_EE0 register.

TSIF_BAM_IRQ_SRCS

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x18204F90 TSIF_BAM_IRQ_SRCS_MSK

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register points to the physical BAM_IRQ_SRCS_MSK_EE0 register.

TSIF_BAM_IRQ_SRCS_MSK

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x18204FB0 TSIF_BAM_IRQ_SRCS_UNMASKED

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register points to the physical BAM_IRQ_SRCS_UNMASKED_EE0 register.

TSIF_BAM_IRQ_SRCS_UNMASKED

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

0x18204F94 TSIF_BAM_IRQ_STTS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only.

Clearing the interrupt bits is done by writing to BAM_IRQ_CLR register.

TSIF_BAM_IRQ_STTS

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
3	BAM_EMPTY_IRQ	This interrupt is for DEBUG purpose only. It should not be used in normal SW flows. The interrupt indicates the BAMs buffer is empty. This bit can become high only when BAM_DATA_ERASE or BAM_DATA_FLUSH is high in BAM_TEST_BUS_SEL register.
2	BAM_ERROR_IRQ	This Indicates a Fatal Error has happened in the BAM. Currently this might happen due to an UnSuccessful Pipe Reset operation.
1	BAM_HRESP_ERR_IRQ	This interrupt Indicates that an Erroneous HResponse has been received by the AHB Master. Additional Information about the error may be read at BAM_AHB_MASTER_ERR_* Registers. Clearing this interrupt also clears the BAM_AHB_MASTER_ERR_* Registers. Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x18204F98 TSIF_BAM_IRQ_CLR

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

TSIF_BAM_IRQ_CLR

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 0x1 - Clear 0x0 - Unchanged
3	BAM_EMPTY_CLR	0x1 - Clear 0x0 - Unchanged Available in BAM-Lite only
2	BAM_ERROR_CLR	0x1 - Clear 0x0 - Unchanged
1	BAM_HRESP_ERR_CLR	0x1 - Clear 0x0 - Unchanged Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x18204F9C TSIF_BAM_IRQ_EN

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the BAM Interrupt Status register.

TSIF_BAM_IRQ_EN

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_EN	Enables Inactivity timer interrupt by writing this bit 0x1 - Enable 0x0 - Disable
3	BAM_EMPTY_EN	0x1 - Enable 0x0 - Disable Available in BAM-Lite only

TSIF_BAM_IRQ_EN (cont.)

Bits	Name	Description
2	BAM_ERROR_EN	0x1 - Enable 0x0 - Disable
1	BAM_HRESP_ERR_EN	0x1 - Enable 0x0 - Disable Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x18204FA0 TSIF_BAM_RESERVED_1

Type: Read
Clock: BAM_CLK
Reset State: 0x00000000

TSIF_BAM_RESERVED_1

Bits	Name	Description
31	RESERVED_BITS31	Set to Zero (0) Obsolete field: BAM_IRQ_SIC_SEL
30:0	RESERVED_BITS30_0	Set to Zero (0) Obsolete field: P_IRQ_SIC_SEL

0x18204FA4 TSIF_BAM_AHB_MASTER_ERR_CTRLS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

TSIF_BAM_AHB_MASTER_ERR_CTRLS

Bits	Name	Description
31:23	RESERVED_BITS31_16	Set to Zero (0)
22:18	BAM_ERR_HVMID	HVMID

TSIF_BAM_AHB_MASTER_ERR_CTRLS (cont.)

Bits	Name	Description
17	BAM_ERR_DIRECT_MODE	DIRECT MODE
16:12	BAM_ERR_HCID	HCID
11:8	BAM_ERR_HPROT	HPROT
7:5	BAM_ERR_HBURST	HBURST
4:3	BAM_ERR_HSIZE	HSIZE
2	BAM_ERR_HWRITE	HWRITE
1:0	BAM_ERR_HTRANS	HTRANS

0x18204FA8 TSIF_BAM_AHB_MASTER_ERR_ADDR

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

TSIF_BAM_AHB_MASTER_ERR_ADDR

Bits	Name	Description
31:0	BAM_ERR_ADDR	HADDR

0x18204FAC TSIF_BAM_AHB_MASTER_ERR_DATA

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

TSIF_BAM_AHB_MASTER_ERR_DATA

Bits	Name	Description
31:0	BAM_ERR_DATA	HDATA

0x18204FB4 TSIF_BAM_RESERVED_2

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

TSIF_BAM_RESERVED_2

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_IRQ_DEST_ADDR

0x18204FB8 TSIF_BAM_RESERVED_3

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

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TSIF_BAM_RESERVED_3

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_DEST_ADDR

0x18204FF0 TSIF_BAM_TRUST_REG

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside - SECURED field in the BAM_REVISION register) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

TSIF_BAM_TRUST_REG

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_VMID	Those bits indicate the VMID value to be used when performing BAM type accesses to the bus. BAM Type accesses include BAM MTI (or Direct Mode accesses, not applicable for BAM Lite)
7	BAM_RST_BLOCK	When enabled, the BAM Global SW reset will not be available for usage. This is in order to deny Global SW reset requests by the Global security group. 0x1 - Enable 0x0 - Disable
6:2	RESERVED_BITS6_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_EE	This field indicates the EE (0,1,2,3) to which the BAM Interrupt belongs to. The pipe interrupts will fire on the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 0x00 - EE0 0x01 - EE1 0x10 - EE2 0x11 - EE3

0x18204FF4 TSIF_BAM_TEST_BUS_SEL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This is the testbus selector register.

Supported in releases after bam_p3q3r29 (BlackBird).

TSIF_BAM_TEST_BUS_SEL

Bits	Name	Description
31:19	RESERVED_BITS31_19	Set to Zero (0)
18	BAM_DATA_ERASE	When enabled, BAM will be instructed to erase all the data it currently has inside. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 0x1 - Enable Erase 0x0 - Disabled
17	BAM_DATA_FLUSH	When enabled, BAM will be instructed to flush all the data it currently has inside. BAM will only flush the data once it has enough data and a valid destination for it. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 0x1 - Enable Flush 0x0 - Disabled
16	BAM_CLK_ALWAYS_ON	This bit controls the BAM to issue 'always on' clock request. 0x1 - Enable Always On clock request. 0x0 - Disabled
15:7	RESERVED_BITS15_7	Set to Zero (0)
6:0	BAM_TESTBUS_SEL	Test Bus selector. Values with bit[11] set high are reserved for the BAM Lite integrator to provide testbus from outside of the BAM Lite. For example, eDML testbus may reside at X'100_0000' to X'111_1111' selector values. eDML has no registers thus has no test bus selector, so its test bus is combined with the BAM lite's. BAM provides zeroes on its testbus when external values selected. X'000_0000' - Zeros X'000_0001' - Slave test bus X'000_0010' - Pipe state machine test bus X'000_0011' - Buffer test bus X'000_0100' - Sideband test bus X'000_1101' - Bus Manager test bus X'001_0000' - Reg file test bus X'1''_''''' - BAM Lite sets zeroes on the test bus, leaving it for external use

0x18204FF8 TSIF_BAM_TEST_BUS_REG

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the value being output to the testbus of the chip. It is not intended for SW usage but for lab debugging of the BAM. Values here can change every cycle.

TSIF_BAM_TEST_BUS_REG

Bits	Name	Description
31:0	BAM_TESTBUS_REG	32 bit Testbus value. To select the Block in BAM to show here, use the BAM_TESTBUS_SEL field in BAM_CTRL register.

0x18204FFC TSIF_BAM_CNFG_BITS

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM configuration bits for bug fixes. It is highly recommended to follow the directions for each bit and set it accordingly.

TSIF_BAM_CNFG_BITS

Bits	Name	Description
31:27	RESERVED_BITS31_27	Set to Zero (0)
26	BAM_AU_ACCUMED	Recommended value: 1 This bit fixes a bug in the Ack Update state machine, where an overflow happened while counting descriptors and reaching more than 64kB of calculated sizes. 0x1 - Enable Fix 0x0 - Disable Available in BAM only
25	BAM_PSM_P_HD_DATA	Recommended value: 1 This bit allows pipe state machine to ignore retransmission requests if a pipe has just been initialized and process those as a regular fetch request. (consumer modes only). When this bit is disabled, BAM could fetch descriptors for a pipe that was reset and no descriptors were added yet, if a retransmission request followed after the reset. 0x1 - Enable Fix 0x0 - Disable Available in BAM only

TSIF_BAM_CNFG_BITS (cont.)

Bits	Name	Description
24	BAM_REG_P_EN	Recommended value: 1 This bit fixes the pipe configuration signals mux for the current active pipe in 2 pipes BAM. When disabled, internal state machines might get into enabled states while the pipe is disabled. This would typically happen after pipe reset. 0x1 - Enable 0x0 - Disable Available in BAM only
23	BAM_WB_DSC_AVL_P_RST	Recommended value: 1 This bit allows the Writeback state machine to reset the vector indicating there are available descriptors when a pipe reset occurs. If disabled, BAM might fetch descriptors after resetting and reconfiguring a pipe, even though no Event (descriptors) was provided. 0x1 - Enable 0x0 - Disable Available in BAM only
22	BAM_WB_RETR_SVPNT	Recommended value: 1 This bit fixes a bug where a pipe that was reset, still stored its retransmission savepoint, but into the illegal's pipe address space, thus hurting the last pipe of the BAM if the BAM had a total 4, 8 or 16 pipes. This is relevant for Producer to System modes only. (CR-0000151585) 0x1 - Enabled 0x0 - Disable Available in BAM only
21	BAM_WB_CSW_ACK_IDL	Recommended value: 1 This bit allows the Writeback state machine to switch into idle state prior to visiting disabled state. This is needed when context switching from mode X to another pipe of mode X is well. This is required to fix a bug in the 2 pipes BAM. 0x1 - Enable 0x0 - Disable Available in BAM only
20	BAM_WB_BLK_CSW	Recommended value: 1 When Enabled, this bit does not allow context switch to happen in the Writeback state machine until it has created a descriptor. This is relevant when the descriptor fifo is becoming full and there's no space to create a descriptor, while another pipe is context switching. This might result in the descriptor not to be created ever, if it was the last one for that pipe. Relevant for Producer BAM-to-BAM mode only. 0x1 - Enable 0x0 - Disable Available in BAM only

TSIF_BAM_CNFG_BITS (cont.)

Bits	Name	Description
19	BAM_WB_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Writeback state machine when performing pipe reset. 0x1 - 0x0 - Disable Available in BAM only
18	BAM_SI_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Sideband Inform state machine when performing pipe reset. 0x1 - Enable 0x0 - Disable Available in BAM only
17	BAM_AU_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Ack Update state machine when performing pipe reset. 0x1 - Enable 0x0 - Disable Available in BAM only
16	BAM_PSM_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Pipe state machine when performing pipe reset. 0x1 - Enable 0x0 - Disable Available in BAM only
15	BAM_PSM_CSW_REQ	Recommended value: 1 This bit forces the context switch request from pipe state machine to RAM controller not to last longer than the slave requested. (2 Pipes BAM bug fix) 0x1 - Enable 0x0 - Disable Available in BAM only
14	BAM_SB_CLK_REQ	Recommended value: 1 This bit allows the clock request from the sideband block to propagate into the BAM's common clock request. 0x1 - Propagate Sideband Clock Request 0x0 - Disable Available in BAM only
13	BAM_IBC_DISABLE	Recommended value: 1 This bit helps to save power by allowing the BAM to keep the inactivity base counter in reset when BAM is disabled or when SW configures IBC_DISABLE bit high. 0x1 - Enable Power Saving 0x0 - Disable Power Saving

TSIF_BAM_CNFG_BITS (cont.)

Bits	Name	Description
12	BAM_NO_EXT_P_RST	Recommended value: 1 This bit allows the BAM / BAM Lite to ignore the externally connected blocks (eDML) when doing pipe reset. The BAM, once instructed to pipe reset, first thing lets the externally connected block know a reset is needed. Then it waits for the externally connected block to Acknowledge it is ready for the pipe reset (meaning it doesn't push any data for the reset pipe) and then the BAM Lite completes the pipe reset operation internally. When disabled, the BAM doesn't require any Acknowledge from the external block to perform pipe reset. 0x1 - Enable external block pipe reset 0x0 - Disable - ignore external block pipe reset
11	BAM_FULL_PIPE	Recommended value: 0 This enables the BAM support for a BAM to BAM Producer that insists to write to a full pipe. When 0, BAM might issue data overflow if producers write to a full pipe. When 1 BAM will not allow this and lower HReady when peripheral tries to do so. Once space is freed in the pipe, Hready will rise and the flow will continue. This functionality has been found to be buggy and was removed from APQ8064. Bit is currently unused. 0x1 - Enable 0x0 - Disable Available in BAM only
10:4	RESERVED_BITS10_4	Set to Zero (0)
3	BAM_ADML_SYNC_BRIDGE	0x1: Use a Synchronous Configuration bridge in aDML. 0x0: Use a Asynchronous Configuration bridge in aDML.
2	BAM_PIPE_CNFG	Recommended value: 1 Pipe SM upgrade for writing EOT bit to the previous descriptor. It's invoked only when EOB arrives in the end of a descriptor. It is highly recommended to set this bit high. Leaving it low might cause incorrect Pipe Bytes Free value reported to peripheral in rare cases. 0x1 - Enable 0x0 - Disable Available in BAM only
1	BAM_ADML_DEEP_CONS_FIFO	0x1: Use a deep Consumer FIFO in aDML (16 dwords) 0x0: Use a shallow Consumer FIFO in aDML (8 dwords)
0	BAM_ADML_INCR4_EN_N	0x1: Don't allow INCR4 aDML-BAM accesses. 0x0: Allow INCR 4 aDML-BAM accesses.

0x18205800+ 128*n TSIF_BAM_IRQ_SRCS_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register has an alias - BAM_IRQ_SRCS register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

TSIF_BAM_IRQ_SRCS_EEn

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x18205804+ 128*n TSIF_BAM_IRQ_SRCS_MSK_EEn, n=[0..3]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register has an alias - BAM_IRQ_SRCS_MSK register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

TSIF_BAM_IRQ_SRCS_MSK_EEn

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x18205808+ 128*n TSIF_BAM_IRQ_SRCS_UNMASKED_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register has an alias - BAM_IRQ_SRCS_UNMASKED register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

TSIF_BAM_IRQ_SRCS_UNMASKED_EEn

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

2.8.2 BAM PIPE management registers

BAM Pipe management registers control each pipe's parameters. Those reside in physical registers.

0x18204000+ 128*n TSIF_BAM_P_CTRLn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Control register provides various controls for the pipe.

TSIF_BAM_P_CTRLn

Bits	Name	Description
31:11	RESERVED_BITS31_11	Set to Zero (0)
10:9	P_PREFETCH_LIMIT	Bam Lite feature Selects the number of bytes to be prefetched by the Bam Lite, once a peripheral requests to read data from a pipe. This feature is relevant for Consumer modes only. 0x00 - 32 bytes at most (INCR8) 0x01 - 16 bytes at most (INCR4) 0x10 - 4 bytes at most (SINGLE) Available in BAM-Lite only

TSIF_BAM_P_CTRLn (cont.)

Bits	Name	Description
8:7	P_AUTO_EOB_SEL	Bam Lite feature. Selects the number of bytes to be processed before creating End Of Block indication internally by the BAM. See P_AUTO_EOB. Descriptors generated by this feature (bam to bam producer mode) will always be of the chosen size, unless an End Of Transfer, causes a smaller descriptor to be created. 0x00 - 512 Bytes 0x01 - 256 Bytes 0x10 - 128 Bytes 0x11 - 64 Bytes Available in BAM-Lite only
6	P_AUTO_EOB	BAM Lite feature. When Enabled, the BAM Lite will ignore any incoming End Of Block indications from the peripheral (if any). Instead, the BAM Lite will generate it's own End Of Block indications internally, every P_AUTO_EOB_SEL bytes. This feature is relevant for Producer Bam 2 Bam modes only. It is a must for peripherals that are not able to produce End Of Block indications. 0x1 - Enable 0x0 - Disable Available in BAM-Lite only
5	P_SYS_MODE	This bit sets the pipe to work in System Mode, where the Software is the second side of the pipe. 0x1 - System mode. 0x0 - BAM to BAM mode.
4	P_SYS_STRM	Streaming Enable. Relevant to System Producer BAM mode only.When enabled, BAM will not close descriptors with End Of Transfer notifications received from peripheral, but continue writing the data to the same descriptor. 0x1 - Enable Streaming Mode 0x0 - None-Streaming Mode
3	P_DIRECTION	This bit denotes pipe direction. 0x1 - The pipe can be written (producer mode) 0x0 - The pipe can be read (consumer mode)
2	RESERVED_BITS2	Set to Zero (0)
1	P_EN	0x1 - Enable Pipe 0x0 - Disable Pipe
0	RESERVED_BITS0	Set to Zero (0)

0x18204004+ 128*n TSIF_BAM_P_RSTn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Reset register provides Pipe Reset ability. Software needs to write 1 to this register to make the Pipe Reset. Writing 0 to this register will finish the Pipe Reset. Writing zero is needed prior to Peripheral reconfiguration for the same pipe.

TSIF_BAM_P_RSTn

Bits	Name	Description
31:1	RESERVED_BITS31_1	Set to Zero (0)
0	P_SW_RST	This resets the pipe and its' registers, (Both Flip-Flops and RAM). 0x1 - Reset 0x0 - Do Nothing

0x18204008+ 128*n TSIF_BAM_P_HALTn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This is a self-modifying register.

TSIF_BAM_P_HALTn

Bits	Name	Description
31:2	RESERVED_BITS31_2	Set to Zero (0)
1	P_PROD_HALTED	This bit is used to inform the Consumer about the Producer being in Halt mode now. This is a part of the Halt procedure. 0x1 - Sets this bit to 1 0x0 - Does Nothing This bit will be cleared by the HW.
0	P_HALT	When Enabled, the Pipe will enter Halt Mode. 0x1 - Enable Halt 0x0 - Disable Halt For B2B Producer pipes, this bit is self modifying. It doesn't need the SW to clear it.

0x18204030+ 128*n TSIF_BAM_P_TRUST_REGn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

TSIF_BAM_P_TRUST_REGn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_P_VMID	Those bits indicate the VMID value to be used when performing Pipe type accesses to the bus. BAM Type accesses include Pipe MTI, Data and Descriptors.
7:2	RESERVED_BITS7_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_P_EE	This field indicates the EE (0,1,2,3) to which the Pipe Interrupt belongs to. The BAM interrupt will fire to the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 0x00 - EE0 0x01 - EE1 0x10 - EE2 0x11 - EE3

0x18204010+ 128*n TSIF_BAM_P_IRQ_STTSn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only. It also has informative bits that are not interrupts.

Clearing the interrupt bits is done by writing to P_IRQ_CLR register.

TSIF_BAM_P_IRQ_STTSn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_IRQ	For producer this interrupt happens whenever the last AHB burst of a transfer happens For Consumer when ack_on_success closes a transfer
4	P_ERR_IRQ	Pipe Error interrupt indicates that an error has happened. TBD: Error reason is not yet defined. Interrupt not in use.
3	P_OUT_OF_DESC_IRQ	Out of descriptors interrupt has several meanings depending on the operation mode: Producer - no free space in the descriptors fifo for adding a descriptor Consumer - no descriptors in the descriptors fifo for processing IO Vectors Producer - No descriptors to read (and therefore no space for data to write to the pipe) IO Vectors Consumer - No descriptors to read (and therefore no data to read from pipe)
2	P_WAKE_IRQ	Wake peripheral interrupt signals the driver to wake up the peripheral (USB for example) for transmission via the current pipe. This interrupt is issued whenever an Event comes to the specific pipe.
1	P_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
0	P_PRCSD_DESC_IRQ	This Interrupt rises when BAM finishes processing an IO Vector that has INT bit selected

0x18204014+128*n TSIF_BAM_P_IRQ_CLRn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

TSIF_BAM_P_IRQ_CLRn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_CLR	0x1 - Clear 0x0 - Unchanged
4	P_ERR_CLR	0x1 - Clear 0x0 - Unchanged
3	P_OUT_OF_DESC_CLR	0x1 - Clear 0x0 - Unchanged

TSIF_BAM_P_IRQ_CLRn (cont.)

Bits	Name	Description
2	P_WAKE_CLR	Clear Wake peripheral interrupt by writing this bit 0x1 - Clear 0x0 - Unchanged
1	P_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 0x1 - Clear 0x0 - Unchanged
0	P_PRCSD_DESC_CLR	Clear Descriptor Processed interrupt by writing this bit 0x1 - Clear 0x0 - Unchanged

0x18204018+ 128*n TSIF_BAM_P_IRQ_ENn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the Pipe Interrupt Status register.

TSIF_BAM_P_IRQ_ENn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_EN	0x1 - Enable 0x0 - Disable
4	P_ERR_EN	0x1 - Enable 0x0 - Disable
3	P_OUT_OF_DESC_EN	0x1 - Enable 0x0 - Disable
2	P_WAKE_EN	Enable Wake peripheral interrupt 0x1 - Enable 0x0 - Disable
1	P_TIMER_EN	Enable Inactivity timer Interrupt 0x1 - Enable 0x0 - Disable
0	P_PRCSD_DESC_EN	Enable Descriptor Processed Interrupt 0x1 - Enable 0x0 - Disable

0x1820401C+ 128*n TSIF_BAM_P_TIMERn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the pipe.

TSIF_BAM_P_TIMERn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x18204020+ 128*n TSIF_BAM_P_TIMER_CTRLn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The resolution of the pipe inactivity timers are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the P_TIMER_THRSHLD is 10 will indicate the 2^3*1us*10, which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * P_TIMER_TRSHLD.

TSIF_BAM_P_TIMER_CTRLn

Bits	Name	Description
31	P_TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the P_TIMER_THRESOLD value 0x1 - Active 0x0 - Reset
30	P_TIMER_RUN	Will be used along with P_TIMER_MODE Not implemented at this time. Set to zero(0)
29	P_TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	P_TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x18204024+ 128*n TSIF_BAM_P_PRDCR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Producer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

TSIF_BAM_P_PRDCR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_producer
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	BAM_P_TOGGLE	Pipe Bytes Free Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Free Ctrl value
15:0	BAM_P_BYTES_FREE	Pipe Bytes Free value

0x18204028+ 128*n TSIF_BAM_P_CNSMR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Consumer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

TSIF_BAM_P_CNSMR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_consumer
23	BAM_P_WAIT_4_ACK	waiting_for_ack_bytes_avail_r
22	BAM_P_ACK_TOGGLE	ack_bytes_avail_toggle
21	BAM_P_ACK_TOGGLE_R	ack_bytes_avail_toggle_r
20	BAM_P_TOGGLE	Pipe Bytes Avail Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Avail Ctrl value
15:0	BAM_P_BYTES_AVAIL	Pipe Bytes AVAIL value

2.8.3 BAM PIPE configuration registers (RAM)

BAM Pipe management registers configure each pipes' parameters.

Pipe Address span: currently defining each pipe to have 32 addresses, therefore inter pipe offset is 32*4=128=0x80 bytes.

0x1820502C+ 64*n TSIF_BAM_P_EVNT_DEST_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Event Destination Address, which is the address of BAM_P_EVNT_REG in the BAM on the other side of the Pipe.

Producer BAM will send Write Events to this address.

Consumer BAM will send Read Events to this address.

This is relevant only for BAM to BAM modes. In System modes, BAM doesn't issue Write/Read events.

TSIF_BAM_P_EVNT_DEST_ADDRn

Bits	Name	Description
31:0	P_EVNT_DEST_ADDR	Address of the Event Register in the peer BAM (second end of the pipe). Driver will configure this when initializing the pipe.

0x18205018+ 64*n TSIF_BAM_P_EVNT_REGn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register is where Read/Write events are sent to. If current BAM works as Producer, it will receive Read events into this register from the Consumer. If the Consumer is another BAM, it will write read events to this register. If the Consumer is the Software, it will prepare descriptors in the descriptor FIFO and update the DESC_FIFO_PEER_OFST value in this register.

If current BAM works as Consumer, opposite behavior is assumed.

TSIF_BAM_P_EVNT_REGn

Bits	Name	Description
31:16	P_BYTES_CONSUMED	This field is used only in the B2B mode. It indicates the number of bits consumed by the Consumer. Consumer sends this value to the Producer as a part of a read event, for the Producer to know how many bytes were consumed. When working in System mode, this value should be set to zero. BAM to BAM Producer writes zero in this value.
15:0	P_DESC_FIFO_PEER_OFST	This field indicates the Descriptor Fifo Offset Pointer of the Peer BAM (The BAM or the Software that creates descriptors). For example, when current BAM works as consumer for the current pipe, Producer BAM (or the software) updates this value to let the current pipe know about the new descriptors added in the Descriptor Fifo.

0x18205000+ 64*n TSIF_BAM_P_SW_OFSTSn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register denotes the pointer Offset of the first Not Acknowledged Descriptor. Meaning all Descriptors prior to this one have been processed by the BAM. This register is only used by the Software. After receiving an interrupt, software reads this register in order to know what descriptors has been processed.

When the BAM works as Producer, Software will usually read this value after Descriptor Processed Interrupt or after the End of Transfer Interrupt.

When the BAM works as Consumer, Software will usually read this value after Descriptor Processed Interrupt.

NOTE This is non relevant in BAM to BAM modes.

NOTE Although being Writable, Software should never write to this register.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

TSIF_BAM_P_SW_OFSTSn

Bits	Name	Description
31:16	SW_OFST_IN_DESC	Offset inside the Descriptor. This value is used by the Software only when a BAM is working as System Producer. Then the SW can read this value to know how many Bytes were written to the current descriptor if it was not closed down. This is useful for Streaming mode.
15:0	SW_DESC_OFST	Descriptor FIFO offset.

0x18205024+ 64*n TSIF_BAM_P_DATA_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Beginning of the Data Address space.

This register is non relevant in System Modes.

TSIF_BAM_P_DATA_FIFO_ADDRn

Bits	Name	Description
31:0	P_DATA_FIFO_ADDR	Data Address Space beginning.

0x1820501C+ 64*n TSIF_BAM_P_DESC_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Address of the Descriptor Fifo beginning.

NOTE This register is used by all modes.

TSIF_BAM_P_DESC_FIFO_ADDRn

Bits	Name	Description
31:0	P_DESC_FIFO_ADDR	Address of the Descriptors Fifo. This address must be 8 bytes aligned.

0x18205028+64*n TSIF_BAM_P_EVNT_GEN_TRSHLDn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register configures the threshold value for Read/Write event generation by the BAM towards another BAM. When a BAM pushes/pops this number of bytes to/from the pipe an event to the other BAM will be generated. A counter summing up the bytes pushed/popped is reset when event is issued, thus restarting count for the threshold.

Events are also issued after End Of Transfer received from the peripheral (Producer case), non regarding whether the pushed bytes count has reached the threshold or not.

This register is non relevant in System Modes.

TSIF_BAM_P_EVNT_GEN_TRSHLDn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TRSHLD	Threshold value. The maximum allowed value is 32kByte.

0x18205020+64*n TSIF_BAM_P_FIFO_SIZESn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

The least significant field is the Descriptor Fifo Size.

The most significant field is the Data Fifo Size.

NOTE This Descriptor Fifo Size is used by all modes. The Data Fifo Size is non relevant in System Modes.

TSIF_BAM_P_FIFO_SIZESn

Bits	Name	Description
31:16	P_DATA_FIFO_SIZE	Size of the Data Address Space.
15:0	P_DESC_FIFO_SIZE	Size of the Descriptors Fifo. Must be 8 byte aligned. Each descriptor is 8 bytes. Size of the descriptor fifo must contain an integer number of Descriptors.

2.8.4 BAM PIPE internal state registers (RAM)

BAM Pipe debug registers allow a software look inside on the internal parameters of the BAM State Machines stored in RAM.

Those shouldn't be normally used or altered by the software.

0x18205034+64*n TSIF_BAM_P_RETR_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context stored for retransmission.

This is being stored by Ack Update state machine in consumer mode or by the Writeback state machine in producer mode.

This is being loaded by the Writeback state machine when retransmission happens.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

TSIF_BAM_P_RETR_CNTXT_n

Bits	Name	Description
31:16	RETR_DESC_OFST	Descriptor Fifo Offset for retransmission.
15:0	RETR_OFST_IN_DESC	The Offset inside the Descriptor for retransmission.

0x18205038+64*n TSIF_BAM_P_SI_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Sideband Inform state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

TSIF_BAM_P_SI_CNTXT_n

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	SI_DESC_OFST	The Descriptor Fifo Offset pointer stored by the Sideband Inform state machine.

0x18205004+ 64*n TSIF_BAM_P_AU_PSM_CNTXT_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Ack Update state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

TSIF_BAM_P_AU_PSM_CNTXT_1_n

Bits	Name	Description
31:16	AU_PSM_ACCUMED	PSM: The acknowledged (EOB/T) number of bytes since last Write Event. AU: The accumulation of the descriptor sizes for the present ack_on_success event. This is never bigger than the ACKED field. Once the ACCUMED values are bigger than Event Threshold, an Event will be issued, the ACKED value will decrease by the ACCUMED size and this value will be zeroed. This also serves as the Bytes Consumed value in the Event.
15:0	AU_ACKED	AU: The left over of the number of bytes that were received via the ack_on_success, that did not cause a descriptor closure. This value is down counting upon issuing Read Event. PSM:

0x18205008+ 64*n TSIF_BAM_P_PSM_CNTXT_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

TSIF_BAM_P_PSM_CNTXT_2_n

Bits	Name	Description
31	PSM_DESC_VALID	The Descriptor Valid bit provided by the Writeback state machine to Pipe state machine.
30	PSM_DESC_IRQ	The Descriptor Interrupt bit provided by the Writeback state machine to pipe state machine.
29	PSM_DESC_IRQ_DONE	The Descriptor Interrupt needed selection bit.
28:25	PSM_GENERAL_BITS	General Context Switch Bits
24:22	PSM_CONS_STATE	State of the Pipe Consumer state machine.
21:19	PSM_PROD_SYS_STATE	State of the Pipe Producer System state machine.
18:16	PSM_PROD_B2B_STATE	State of the Pipe Producer BAM to BAM state machine.
15:0	PSM_DESC_SIZE	The Descriptor Size provided by the Writeback state machine to pipe state machine.

0x1820500C+ 64*n TSIF_BAM_P_PSM_CNTXT_3_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

TSIF_BAM_P_PSM_CNTXT_3_n

Bits	Name	Description
31:0	PSM_DESC_ADDR	The Data Address provided in the current descriptor from the Writeback state machine.

0x18205010+ 64*n TSIF_BAM_P_PSM_CNTXT_4_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

TSIF_BAM_P_PSM_CNTXT_4_n

Bits	Name	Description
31:16	PSM_DESC_OFST	The running Descriptor Fifo Offset of the Writeback state machine
15:0	PSM_SAVED_ACCUMED_SIZE	The Saved Accumulated Size from the Pipe state machine.

0x18205014+64*n TSIF_BAM_P_PSM_CNTXT_5_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

TSIF_BAM_P_PSM_CNTXT_5_n

Bits	Name	Description
31:16	PSM_BLOCK_BYTE_CNT	The Byte count inside the current Block.
15:0	PSM_OFST_IN_DESC	The Offset inside a register. This is used by pipe state machine to compute offset inside a register after retransmission

0x18205030+64*n TSIF_BAM_P_RESERVED_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

TSIF_BAM_P_RESERVED_1_n

Bits	Name	Description
31:0	BAM_P_RES_1	Set to zero (0) Reserved

0x1820503C+64*n TSIF_BAM_P_RESERVED_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

TSIF_BAM_P_RESERVED_2_n

Bits	Name	Description
31:0	BAM_P_RES_2	Set to zero (0) Obsolete Register: BAM_P_IRQ_DEST_ADDRn, n=[0..30]

2.9 ADM3_0 registers (0x18300000 ADM3_0_BASE)

This section contains ADM3 registers.

Table 2-2 Support for posting writes on bus

Host interface 0 (HI0)	32-bit AHB	Master on the fast peripheral bus to allow the ARM to program the DM3

Table 2-3 Client rate control interfaces (ADM3_0)

Interface	CRCI assignment	Type	Outstanding request allowed*	Purpose/properties
NULL_CRCI	0	NA	NA	NULL CRCI: choosing it indicates no throttling
CRCI1	1	Block-type	4/4	
CRCI2	2	Block-type	4/4	
CRCI3	3	Command-type	NA	
CRCI4	4	Block-type	8/4	
CRCI5	5	Block-type	8/4	
CRCI6	6	Block-type	48/4	
CRCI7	7	Block-type	4/4	
CRCI8	8	Block-type	4/4	
CRCI9	9	Block-type	4/4	
CRCI10	10	Block-type	4/4	
CRCI11	11	Block-type	4/4	
CRCI12	12	Block-type	4/4	
CRCI13	13	Block-type	4/4	
CRCI14	14	Block-type	4/4	
CRCi15	15	Command-type	NA	

Table 2-4 Client rate control interfaces (ADM3_1)

Interface	CRCI assignment	Type	Outstanding request allowed*	Purpose/properties
NULL_CRCI	0	NA	NA	NULL CRCI: choosing it indicates no throttling
CRCI1	1	Block-type	4/4	
CRCI2	2	Block-type	4/4	
CRCI3	3	Command-type	NA	
CRCI4	4	Block-type	8/4	
CRCI5	5	Block-type	8/4	
CRCI6	6	Block-type	4/4	
CRCI7	7	Block-type	4/4	
CRCI8	8	Block-type	4/4	
CRCI9	9	Block-type	4/4	
CRCI10	10	Block-type	4/4	
CRCI11	11	Block-type	4/4	
CRCI12	12	Block-type	4/4	
CRCI13	13	Block-type	4/4	
CRCI14	14	Block-type	8/4	
CRCi15	15	Command-type	NA	

In order to throttle data with the CRCI, the reset bit of corresponding CRCI control register must be cleared. All CRCIs come up in the reset state after power-up and must be enabled by software clearing these bits.

*Outstanding Request Allowed: The maximum number of the CRCI's "REQ" recognized by ADM3 at any give moment. If CRCI attempts at any given time with consecutive “REQ” the ADM3 will cease to "ACK" until the current channel "block transfer" is complete.

This section describes the various registers within the ADM3. These registers are visible from peripheral bus by the peripheral bus masters. Table 1-13 provides a summary of register accessing with respect with the security domain.

Note that the ARM and ADSP register space point to the same set of physical registers. Reserved bits must be written to as 0, and cannot be counted on to return a specific value.

For each register address, "n" denotes either the channel number (0-15) or client interface number (0-2), and ‘s’ denotes the security domain (0-7). Each security domain is 128KB+2KB apart.

Table 2-5 Host interface register accessing by the security domain summary

Address	Register name	SD Accessing Privilege
0x000+4n+0x20800s	HI_CHn_CMD_PTR	SD specific accessing
0x040+4n+0x20800s	HI_CHn_RSLT	SD specific accessing
0x080+4n+0x20800s	HI_CHn_FLUSH_STATE0	SD specific accessing
0x0C0+4n+0x20800s	HI_CHn_FLUSH_STATE1	SD specific accessing
0x100+4n+0x20800s	HI_CHn_FLUSH_STATE2	SD specific accessing
0x140+4n+0x20800s	HI_CHn_FLUSH_STATE3	SD specific accessing
0x180+4n+0x20800s	HI_CHn_FLUSH_STATE4	SD specific accessing
0x1C0+4n+0x20800s	HI_CHn_FLUSH_STATE5	SD specific accessing
0x200+4n+0x20800s	HI_CHn_STATUS	SD specific accessing
0x240+4n	HI_CHn_CONF	SD 0 only
0x280+4n	HI_CHn_DBG_0	SD 0 only
0x2C0+4n	HI_CHn_DBG_1	SD 0 only
0x300+4n+0x20800s	HI_CHn_RSLT_CONF	SD specific accessing
0x380+0x20800s	HI_SEC_DOMAIN_IRQ_STATUS	SD specific accessing*
0x390+4n	HI_CIn_CONF	SD 0 only
0x3B0+4n	HI_CIn_DBG_ERR	SD 0 only
0x3D0	HI_CRCI_CONF0	SD 0 only
0x3D4	HI_CRCI_CONF1	SD 0 only
0x3D8	HI_GP_CTL	SD 0 only
0x3E0	HI_GLBL_DBG_CMD_ENG	SD 0 only
0x3E4	HI_GLBL_DBG_REQ_ENG	SD 0 only
0x3E8	HI_GLBL_DBG_XFER_ENG	SD 0 only
0x3EC	HI_GLBL_DBG_CHAN_BLK	SD 0 only
0x3F0	HI_GLBL_DBG_CHAN_BLK_CLR	SD 0 only
0x3F4	HI_GLBL_DBG_TEST_SEL	SD 0 only
0x400+0x20800s	HI_CRCI0_CTL	SD specific accessing
0x400+4n+0x20800s	HI_CRCIn_CTL	SD specific accessing

2.9.1 Channel programming registers

0x18300000+4*n+0x20800*s **ADM3_0_HI_CHn_CMD_PTR_SDs, n=[0..15], s=[0..7]**

Type: Read/Write
Clock: DM_CORE
Reset State: 0xXXXXXXXX

The HI_CHn_CMD_PTR_SDs register is used to supply the top-level programming structure pointer to the N'th DM3 channel. This register is implemented as a FIFO that can accept two top-level pointers in addition to a third that is executing.

ADM3_0_HI_CHn_CMD_PTR_SDs

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:0	ADDR	Address (in double words) of the command structure

0x18300040+4*n+0x20800*s **ADM3_0_HI_CHn_RSLT_SDs, n=[0..15], s=[0..7]**

Type: Read
Clock: DM_CORE
Reset State: V(alid) bit=0, all other bits X

The HI_CHn_RSLT_SDs register is used to read the results produced by N'th DM3 channel.

NOTE Reading this register pops one item from the 3-deep result FIFO. The combined depth of the result FIFO and the top-level pointer FIFO is only allowed to be two deep unless there isn't already a top-level pointer executing, in which case the combined depth can be three.

There almost always is a one-to-one correspondence between the top-level pointers and the results. The only exception is when an error occurs (as indicated by ERR). In this case, all queued top-level pointers will be discarded, but only one result will be created.

ADM3_0_HI_CHn_RSLT_SDs

Bits	Name	Description
31	V	Valid - the result is valid If this bit is cleared (0), it indicates that the host has emptied the result FIFO.
3	ERR	Error - The result was generated because of an error
2	F	Flush - The result was generated because of a flush operation
1	TPD	Top pointer done - The result was generated because of the completion of the last command in the top-level programming structure
0	RESERVED_BIT0	

0x18300080+4*n+0x20800*s **ADM3_0_HI_CHn_FLUSH_STATE0_SDs, n=[0..15], s=[0..7]**

Type: Read/Write
Clock: DM_CORE
Reset State: V(alid) bit=1, FLUSH_TYPE=0, CMD_ERR=0, all other bits X

Writing to the HI_CHn_FLUSH_STATE0_SDs register clears (0) the V bit, which then causes the channel to begin a flush operation. When writing to this register, bit 31 should be set to the desired flush type (discard or graceful). Upon completion of the flush state assembly (as indicated by a set V flag), this and the other five FLUSH_STATE registers will contain the state of the channel at the time of the flush. The DM3 may also initiate a channel flush operation internally when the channel encounters an error.

NOTE If a flush is already underway for a given channel and a result from this flush has not yet been generated, then a subsequent flush to the same channel will have no impact and will not generate a second result. This can be determined by the CH_STATE after a flush request. If set to FLUSH_WAIT then this indicates that a flush is already in progress and the subsequent flush was ignored.

Also, if the NO_DATA_XFER field is set, then the flush occurred prior any data transfers occurring for the top-level pointer, and thus all other flush state registers will not contain valid data.

If the LAST_CPLE_MPU field is set then the last command list entry processed was an MPU command. As such, all other flush state registers will not contain valid data, except for the PTR_NUM field in the FLUSH_STATE5 register. In this case, PTR_NUM will point to the next CLE entry AFTER the MPU command.

If the NO_INB_INSTR field is set, then the flush occurred at a point where no INB instruction was loaded or being processed. In this case the DPH_CMD_TYPE field of FLUSH_STATE0, the SRC_REM_LEN field of FLUSH_STATE3, and the SRC_DSCR_NUM field of the FLUSH_STATE4 register provide information on the last INB operation to fully complete. This can happen between commands, between scatter/gather indices, or between scatter/gather descriptors.

If the NO_OTB_INSTR field is set, then the flush occurred at a point where no OTB instruction was loaded or being processed. In this case the DST_REM_LEN field of FLUSH_STATE3 and the DST_DSCR_NUM field of the FLUSH_STATE4 register provide information on the last OTB operation to fully complete. This can happen between commands, between scatter/gather indices, or between scatter/gather descriptors.

Also, if both the NO_INB_INSTR and NO_OTB_INSTR fields are set then the flush occurred at a time when no instructions (INB or OTB) were loaded for the channel. This can happen between commands, between scatter/gather indices, or between scatter/gather descriptors. In this case all flush state registers provide information on what just completed rather than what was next to be processed.

When following the requirement that only the FLUSH_STATE1 register, and the PTR_NUM and DSCR_INDX_NUM fields of the FLUSH_STATE5 register are used in conjunction with NO_DATA_XFER, CH_STATE, and LAST_CPLE_MPU to resubmit flushed commands, the

NO_INB_INSTR and NO_OTB_INSTR fields can be ignored and are provided for debug purposes only.

Host initiated flush operations only terminate the top-level pointer that is currently being executed. If a second top-level pointer is valid, it will not be affected by the flush. On the other hand, a flush due to an error condition will flush all top-level pointers.

ADM3_0_HI_CHn_FLUSH_STATE0_SDs

Bits	Name	Description
31	FLUSH_TYPE	Notes: 1. FLUSH_TYPE=1 is only supported for single and box mode commands. It currently is not supported for commands that are zero length, and should not be attempted on commands of zero length or unpredictable results may occur. 2. On reads, this bit indicates the type of flush that occurred based on the command type being processed at the time that the flush was requested. 3. If a graceful flush is requested just as one command is completing and another is about to start, the FLUSH_TYPE may not agree with the DPH_CMD_TYPE. This is because the FLUSH_TYPE is based on the command that is completing, while the DPH_CMD_TYPE will be based on the command that is about to start (assuming another command is loaded). This only occurs under the condition that the flush had no impact on the command completing. For example FLUSH_TYPE = 1 and DPH_CMD_TYPE = SG indicates that a single or box mode command was finishing at the time that a graceful flush was requested, but the next command is of type SG and thus only the SG command was affected by the flush. In this case graceful flush and discard flush are equivalent, since no data is buffered. 0x0: Flush should discard any data already read into data buffer 0x1: Flush should write all INB data received or requested prior to terminating the top-level command
30:21	RESERVED_BITS30_21	
20	CMD_ERR	Indicates that an error occurred when parsing a command. For example if ADDR_MODE=2 (reserved) in the first word of the command. This type of error is imprecise in that the DPH_CMD_TYPE field as well as the FLUSH_STATE1-5 registers provide details of the command that is currently in the data phase (or the last command to complete data phase processing if no commands are in the data phase) at the time that the error occurs. This is because the discard flush is applied as soon as the error is detected. The command that is in the data phase may or may not be the command to cause this type of error since up to two commands are processed at a time (one in data phase and one in command phase).
19	LAST_CPLE_MPU	The last command pointer list entry to be processed was an MPU command. As such, the DPH_CMD_TYPE field, as well as all of the other flush state registers will not contain valid data. The one exception is the PTR_NUM field in FLUSH_STATE5 which is valid.

ADM3_0_HI_CHn_FLUSH_STATE0_SDs (cont.)

Bits	Name	Description
18	NO_OTB_INSTR	Flush occurred at a time when no OTB instructions were loaded. See above for details.
17	NO_INB_INSTR	Flush occurred at a time when no INB instructions were loaded. See above for details.
16	NO_DATA_XFER	The channel had begun to process the top-level pointer for this channel, but no data transfers for the top-level pointer had yet begun. As such, all other flush state registers will not be valid. A result will be generated for this top-level pointer.
15:14	DPH_CMD_TYPE	Specifies the type of command that has been flushed (only valid if CH_STATE is not idle, NO_DATA_XFER is not set (1), and LAST_CPLE_MPU is not set (1)): 0x0: Single 0x1: Scatter/gather 0x2: Reserved_programming 0x3: Box
13	PTR_NUM_OVRFLW	Indicates that the PTR_NUM field in FLUSH_STATE5 has overflowed and is not valid (this is only a status indication, it is not a cause for a flush)
12	DSCR_INDX_OVRFLW	Indicates that the DSCR_INDX_NUM field in FLUSH_STATE5 has overflowed and is not valid (this is only a status indication, it is not a cause for a flush)
11	LEN_ERROR	A flush was triggered internally because a box mode or scatter/gather command encountered a length error.
10	MPU_ERROR	A flush was triggered internally because a command encountered an internal MPU error.
9	DPH_BUS_ERROR	A flush was triggered internally because a command encountered a bus error from one of the data transfer requests.
8	CPH_BUS_ERROR	A flush was triggered internally because a command encountered a bus error from one of the command fetch requests. This type of error is imprecise in that the DPH_CMD_TYPE field as well as the FLUSH_STATE1-5 registers provide details of the command that is currently in the data phase (or the last command to complete data phase processing if no commands are in the data phase) at the time that the error occurs. This is because the discard flush is applied as soon as the error is detected. The command that is in the data phase may or may not be the command to cause this type of error since up to two commands are processed at a time (one in data phase and one in command phase).
7:3	RESERVED_BITS7_3	

ADM3_0_HI_CHn_FLUSH_STATE0_SDs (cont.)

Bits	Name	Description
2:1	CH_STATE	Specifies the processing state of the channel at the time that the flush was requested The channel was completely idle at the time of a flush and thus the flush has been ignored and has no impact. In this case a result will not be generated for this flush request. In this case all of the other flush state registers will not update. They will continue to provide the state of the last flush (if any). The channel was processing a command at the time of the flush. A result will be generated if the flush is due to an error condition, or if flush results are enabled. The channel was already processing a flush (either host initiated or due to an error) at the time that the latest flush was requested. As such, the latest flush request will be ignored. Other flush state registers do not update and continue to correspond to the initial flush. No result will be generated for the latest flush. 0x0: IDLE 0x1: PROCESS 0x3: FLUSH_WAIT
0	V	Indicates that the flush state is now valid. If an error occurs on a top-pointer after the previous top-pointer was flushed, this bit will go low while the DM3 core gathers the flush state for the error. In this case the flush state from the previous top-pointer will be lost if it has not already been read by the host.

0x183000C0+4*n+0x20800*s ADM3_0_HI_CHn_FLUSH_STATE1_SDs, n=[0..15], s=[0..7]

Type: Read
Clock: DM_CORE
Reset State: 0xXXXXXXXX

The HI_CHn_FLUSH_STATE1_SDs register is only meaningful if CH_STATE is not idle (00), NO_DATA_XFER is not set (1), and LAST_CPLE_MPU is not set (1).

ADM3_0_HI_CHn_FLUSH_STATE1_SDs

Bits	Name	Description
31:0	CMD_ADDR	Address of the command being processed by the data phase at the time of flush operation.

0x18300100+4*n+0x20800*s ADM3_0_HI_CHn_FLUSH_STATE2_SDs, n=[0..15], s=[0..7]

Type: Read
Clock: DM_CORE
Reset State: 0xXXXXXXXX

The HI_CHn_FLUSH_STATE2_SDs register is reserved. Software should not access this register.

ADM3_0_HI_CHn_FLUSH_STATE2_SDs

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x18300140+4*n+0x20800*s ADM3_0_HI_CHn_FLUSH_STATE3_SDs, n=[0..15], s=[0..7]

Type: Read
Clock: DM_CORE
Reset State: 0xXXXXXXXX

The HI_CHn_FLUSH_STATE3_SDs register is only meaningful if CH_STATE is not idle (00), NO_DATA_XFER is not set (1), and LAST_CPLE_MPU is not set (1). This register is intended for debug purposes and should not be relied upon by software.

ADM3_0_HI_CHn_FLUSH_STATE3_SDs

Bits	Name	Description
31:16	DST_REM_LEN	Specifies the number of bytes yet to be written to the command's current destination buffer (assuming all outstanding bus requests have completed). In the case of box mode commands, this is the number of bytes remaining for the current line.
15:0	SRC_REM_LEN	Specifies the number of bytes yet to be read from the command's current source buffer (assuming all outstanding bus requests have completed). In the case of box mode commands, this is the number of bytes remaining for the current line.

0x18300180+4*n+0x20800*s ADM3_0_HI_CHn_FLUSH_STATE4_SDs, n=[0..15], s=[0..7]

Type: Read
Clock: DM_CORE
Reset State: 0xXXXXXXXX

The HI_CHn_FLUSH_STATE4_SDs register is only meaningful if CH_STATE is not idle (00), NO_DATA_XFER is not set (1), and LAST_CPLE_MPU is not set (1). This register is intended only for debug purposes and should not be relied upon for software.

ADM3_0_HI_CHn_FLUSH_STATE4_SDs

Bits	Name	Description
31:16	DST_DSCR_NUM	Box mode commands: · Specifies the number of remaining destination lines for the command, including the current line (assuming all outstanding requests completed) Scatter/gather commands: · Specifies the scatter/gather command's current destination descriptor position in the descriptor list (assuming all outstanding requests completed)
15:0	SRC_DSCR_NUM	Box mode commands: · Specifies the number of remaining source lines for the command, including the current line (assuming all outstanding requests completed) Scatter/gather commands: · Specifies the scatter/gather command's current source descriptor position in the descriptor list (assuming all outstanding requests completed)

0x183001C0+4*n+0x20800*s **ADM3_0_HI_CHn_FLUSH_STATE5_SDs, n=[0..15], s=[0..7]**

Type: Read
Clock: DM_CORE
Reset State: 0xXXXXXXXX

The HI_CHn_FLUSH_STATE5_SDs register is only meaningful if CH_STATE is not idle (00), and NO_DATA_XFER is not set (1). If LAST_CPLE_MPU is set (1), then only the PTR_NUM field in this register is valid. In this case PTR_NUM points to the command list entry AFTER the MPU command.

ADM3_0_HI_CHn_FLUSH_STATE5_SDs

Bits	Name	Description
31:24	PTR_NUM	Specifies the current command's list pointer position in the pointer list (assuming all outstanding requests completed).
23:16	DSCR_INDX_NUM	Specifies the indirect scatter/gather command's current descriptor index position in the descriptor index list (assuming all outstanding requests completed).
15:8	BUFFERED_LEN	Specifies the number of data bytes read from the source but not written to the destination (assuming all outstanding requests complete). This field is intended for debug purposes only and should not be relied upon by software.
2:0	RESERVED_BITS2_0	

2.9.2 Interrupt status registers

0x18300380+ 0x20800*s ADM3_0_HI_SEC_DOMAIN_IRQ_STATUS_SDs, s=[0..7]

Type: Read
Clock: DM_CORE
Reset State: 0x00000000

The HI_SEC_DOMAIN_IRQ_STATUS_SDs register is the N'th security domain's interrupt status register, which reflects the state of only those channels that belong to the N'th security domain. The other IRQ bits are always cleared (0). Reading the N'th security domain's interrupt status register clears (0) all of the interrupt requests from the channels belonging to the N'th security domain. The other channel interrupt requests are not affected.

ADM3_0_HI_SEC_DOMAIN_IRQ_STATUS_SDs

Bits	Name	Description
15	CH_15_IRQ	Indicates a pending interrupt request from channel 15
14	CH_14_IRQ	Indicates a pending interrupt request from channel 14
13	CH_13_IRQ	Indicates a pending interrupt request from channel 13
12	CH_12_IRQ	Indicates a pending interrupt request from channel 12
11	CH_11_IRQ	Indicates a pending interrupt request from channel 11
10	CH_10_IRQ	Indicates a pending interrupt request from channel 10
9	CH_9_IRQ	Indicates a pending interrupt request from channel 9
8	CH_8_IRQ	Indicates a pending interrupt request from channel 8
7	CH_7_IRQ	Indicates a pending interrupt request from channel 7
6	CH_6_IRQ	Indicates a pending interrupt request from channel 6
5	CH_5_IRQ	Indicates a pending interrupt request from channel 5
4	CH_4_IRQ	Indicates a pending interrupt request from channel 4
3	CH_3_IRQ	Indicates a pending interrupt request from channel 3
2	CH_2_IRQ	Indicates a pending interrupt request from channel 2
1	CH_1_IRQ	Indicates a pending interrupt request from channel 1
0	CH_0_IRQ	Indicates a pending interrupt request from channel 0

2.9.3 Channel status, configuration registers accessible to security domains

0x18300300+4*n+0x20800*s **ADM3_0_HI_CHn_RSLT_CONF_SDs, n=[0..15], s=[0..7]**

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00000002

The HI_CHn_RSLT_CONF_SDs register provides the interrupt configuration status of the indicated channel.

ADM3_0_HI_CHn_RSLT_CONF_SDs

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	FLUSH_RSLT_EN	When set (1), a result will be generated for each top-level pointer that is flushed due to a host initiated flush. Note that all top-level pointers that either fully complete or that generate an error always produce a result. This bit should be set for normal operation, since it results in a one-to-one correspondence between top-pointers and results (with the only exception being that if a top-pointer causes an error, any top pointers that are queued are discarded without a result)
0	IRQ_EN	Indicates that an interrupt should be generated when the result FIFO becomes not empty, i.e., transition from 0 valid entry to 1 valid entry.

0x18300200+4*n+0x20800*s **ADM3_0_HI_CHn_STATUS_SDs, n=[0..15], s=[0..7]**

Type: Read
Clock: DM_CORE
Reset State: 0x00000001

The HI_CHn_STATUS_SDs register provides the channel status of the indicated channel.

ADM3_0_HI_CHn_STATUS_SDs

Bits	Name	Description
31:29	RSLT_FIFO_CNTR	Number of valid entries in the result FIFO. 0-3 are supported.
28:27	CMD_PTR_FIFO_CNTR	Number of valid entries in the command pointer FIFO. Note that there may also be a command pointer already being processed.
26	CMD_IN_PROGRESS	Indicates that a top-level pointer is currently being processed.
1	RSLT_VLD	At least one valid result may be dequeued from the result FIFO

ADM3_0_HI_CHn_STATUS_SDs (cont.)

Bits	Name	Description
0	CMD_PTR_RDY	At least one command pointer may be enqueued to the command pointer FIFO. This will only assert if all of the following are true: 1. CMD_PTR_FIFO_CNTR < 2 2. (CMD_PTR_FIFO_CNTR + RSLT_FIFO_CNTR < 2) OR ((CMD_PTR_FIFO_CNTR + RSLT_FIFO_CNTR < 3) AND CMD_IN_PROGRESS = 0)

0x18300400+0x20800*s ADM3_0_HI_CRCI0_CTL_SDs, s=[0..7]

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00030000

The HI_CRCI0_CTL_SDs register provides the ready status, reset of CRCI0.

ADM3_0_HI_CRCI0_CTL_SDs

Bits	Name	Description
31:18	RESERVED_BITS31_18	
17	CRCI0_RST	When set (1), this bit resets the indicated CRCI and keeps it in the reset state. When clear(0), this bit re-enables the indicated CRCI, and it becomes `1' after reset.
16	CRCI0_RDY	This is read only bit. When (1), this bit indicates that the indicated CRCI has at least one token for sending data or a command.
15:0	RESERVED_BITS15_0	

0x18300400+4*n+0x20800*s ADM3_0_HI_CRCIn_CTL_SDs, n=[1..15], s=[0..7]

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00020000

The HI_CRCIn_CTL_SDs register provides the ready status, reset, mux select and block size of the indicated CRCI.

ADM3_0_HI_CRCIn_CTL_SDs

Bits	Name	Description
31:19	RESERVED_BITS31_19	
18	CRCIN_MUX_SEL	The mux select for indicated CRCI.

ADM3_0_HI_CRCIn_CTL_SDs (cont.)

Bits	Name	Description
17	CRCIN_RST	When set (1), this bit resets the indicated CRCI and keeps it in the reset state. When clear(0), this bit re-enables the indicated CRCI, and it becomes `1' after reset.
16	CRCIN_RDY	This is read only bit. When (1), this bit indicates that indicated CRCI has at least one token for sending data or a command.
15:3	RESERVED_BITS15_3	
2:0	CRCIN_BLOCK_SIZE	Defines the block size if indicated CRCI is Data CRCI. 0x0: 16 bytes 0x1: 32 bytes 0x2: 64 bytes 0x3: 128 bytes 0x4: 192 bytes 0x5: 256 bytes

2.9.4 Security domain 0 channel configuration and debug registers

0x18300240+4*n ADM3_0_HI_CHn_CONF, n=[0..15]

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00000081

The HI_CHn_CONF register provides the configuration status of the indicated channel and accessible through the security domain 0 only.

ADM3_0_HI_CHn_CONF

Bits	Name	Description
31:16	OTHER_CH_BLK_MASK	Each set (1) bit specifies that the corresponding channel is controlled by this channel via the OCU and OCB control field.
13	SEC_DOMAIN_2	Specifies the channel security domain (controls channel programming and status register aliasing, and selects which of the four interrupts should be used by the channel)
12	RSLT_CONF_SHADOW_EN	If set (1), the CH_CONF field IRQ_EN and FLUSH_RSLT_EN fields are set through register CHn_RSLT_CONF_SDs. During subsequent writes to CHn_CONF, writes to those fields are ignored. If clear, access to CHn_RSLT_CONF_SDs is ignored.
11	MPU_DISABLE	Disables MPU error detection
10	RESERVED_BIT10	

ADM3_0_HI_CHn_CONF (cont.)

Bits	Name	Description
9	PERM_MPU_CONF	Indicates that the MPU configuration structure pointed to by the top-level pointer will be executed. If this bit is cleared (0), all MPU structures will be silently ignored.
8	RESERVED_BIT8	
7	FLUSH_RSLT_EN	When set (1), a result will be generated for each top-level pointer that is flushed due to a host initiated flush. Note that all top-level pointers that either fully complete or that generate an error always produce a result. This bit should be set for normal operation, since it results in a one-to-one correspondence between top-pointers and results (with the only exception being that if a top-pointer causes an error, any top pointers that are queued are discarded without a result)
6	IRQ_EN	Indicates that an interrupt should be generated when the result FIFO becomes not empty, i.e., transition from 0 valid entry to 1 valid entry. if RSLT_CONF_SHADOW_EN is set (1), writes to this field will be ignored.
5:4	SEC_DOMAIN1_0	Specifies the channel security domain (controls channel programming and status register aliasing, and selects which of the four interrupts should be used by the channel)
3:0	PRIORITY	Specifies channel priority, in which 0 is the highest priority. This is the weight to the arbitration scheme. Note that assigning a channel's priority value to 0 causes the channel to stay at the highest priority, i.e., the channel will always be granted whenever there's a command to be executed, as the accumulator value is never incremented (incremented with 0). The priority can be viewed as the period between service intervals, such that a weight of 1 will be serviced twice as often as a weight of 2. Though arbitration occurs for each client interface separately, a channel's priority is common to all client interfaces. If multiple channels are configured for the same priority and are ready for access to the same client interface, round-robin servicing will be provided between these channels. The only exception to this is if more than one channel is configured as priority 0. In this case the zero-priority channel with the lowest number is always given preference.

0x18300280+4*n ADM3_0_HI_CHn_DBG_0, n=[0..15]

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00000000

The HI_CHn_DBG_0 register is used for debugging purposes for the indicated channel and accessible through the security domain 0 only.

ADM3_0_HI_CHn_DBG_0

Bits	Name	Description
3	REQ_ENG_HALT	When set (1), prevents the channel from being chosen by the arbiter for data transfers. The current operation on the channel (if already selected) will complete.
2	CMD_ENG_HALT	When set (1), prevents the channel from being chosen by the arbiter for command transfers. The current operation on the channel (if already selected) will complete.
1	CMD_PTR_FIFO_HALT	When set (1), prevents the command pointer FIFO from accepting any new command pointers from hosts. The writes to the command pointer register will be ignored.
0	ERROR	When set (1), indicates that the channel has encountered an error and is now in the stalled state. Specific error information may be obtained by reading the channel flush state registers (see Error handling section). The software must clear (0) this bit before the channel may be used again. This bit can only be cleared by S/W; it cannot be set to 1 by S/W.

0x183002C0+4*n ADM3_0_HI_CHn_DBG_1, n=[0..15]

Type: Read
Clock: DM_CORE
Reset State: 0x00000000

The HI_CHn_DBG_1 register is used for additional debugging purposes for the indicated channel and accessible through the security domain 0 only.

NOTE This register always returns "0". Writing to this register has no affect.

ADM3_0_HI_CHn_DBG_1

Bits	Name	Description
31:0	DBG_STATE	TBD

2.9.5 Global configuration, and debug registers

0x18300390+4*n ADM3_0_HI_CIn_CONF, n=[0..3]

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00010001

The HI_CIn_CONF register is the CI configuration register for the indicated client interface.

It is possible to configure two or more client interfaces to have overlapping address regions. In this case accesses to the overlapping region will be sent to the highest numbered client interface. CI0 is the default client interface, and receives accesses to addresses that have not been assigned to any client interface. Setting RANGE_END < RANGE_START will disable the client interface, with the exception of CI0. On reset only CI0 is enabled. While the CI0 RANGE_START and RANGE_END parameters can be written and read, they do not have an impact on the address decode.

ADM3_0_HI_CIn_CONF

Bits	Name	Description
31:24	RANGE_END	Specifies the end of the N'th CI address range in 16-MB blocks. Note that this is the last block within the client interface region. For example setting RANGE_START=0x00 and RANGE_END=0x00 specifies that the client interface supports the address range 0x00000000-0x00FFFFFF. APQ 7200/7500: For CI 1 (SMI), the upper bit of this field must not be set. Any addresses in the range 0x80000000-0xFFFFFFFF must go to CI 0 if unused.
23:16	RANGE_START	Specifies the start of the N'th CI address range in 16-MB blocks

ADM3_0_HI_CIn_CONF (cont.)

Bits	Name	Description
5:4	CI_WEIGHT	Specifies the relative weight that the client interface receives when arbitrating for access to the channel buffer memory. Normally this can be left at 0 for all client interfaces, which means that each CI gets 25% of the channel buffer memory BW when all client interfaces are requesting (more BW is available if not all of the client interfaces are busy). At 133MHz the channel buffer memory has a half-duplex capacity of 500MB/sec. Assuming that each client interface is performing 32-byte bursts, a weight of 0 guarantees at least 125MB/sec of half duplex channel buffer memory BW to each CI. If the CI is doing 16 byte bursts while all other client interfaces are doing 32-byte bursts, then that CI is guaranteed at least 83.3 MB/sec of half duplex BW. If more than this amount of half-duplex BW is required on a single client interface, the CI weight parameter allows for a redistribution of the channel buffer memory BW. The minimum BW that the channel buffer memory will supply to a given CIn is determined by multiplying the following ratio by the BW capacity of the channel buffer memory (500MB/sec at 133MHz) (CI_WEIGHT(CIn)+1)*MAX_BURST_LEN(CIn) --- Sum for i=0 to 3 of ((CI_WEIGHT(CIi)+1)*MAX_BURST_LEN(CIi) Assuming that all bursts are 32-bytes long, then CI_WEIGHT does not need to be set to more than 1. Setting CI_WEIGHT to 1 for a high BW CI and to 0 for the remaining three CIs will result in the channel buffer memory supporting a minimum of 200MB/sec of half-duplex BW to the high BW CI, and 100 MB/sec to each of the remaining 3 low-BW CIs. With a maximum requirement of 100MB/sec full-duplex (200MB/sec half-duplex) across all 4 CIs, this is more than sufficient. Note that this parameter only distributes the BW of the channel buffer memory. It does not ensure that the client interfaces or the command processing can keep up with these rates.
3:0	MAX_BURST_LEN	Specifies the maximum burst length in 32-bit words. Only values of 1, 4, and 8 are currently supported, which specify 1, 4, or 8 word bursts. The following are the limitations of each client interface: AHB client interfaces (CI2, CI3, CI4): 1, 4, 8 AXI client interfaces (CI0, CI1): 4, 8 The AXI client interfaces will also work with a setting of 1, but not all bursts are limited to 1 word. It is recommended that AXI client interfaces be set to 8 word bursts and AHB client interfaces be set to at least 4 word bursts for optimal system performance.

0x183003B0+ 4*n ADM3_0_HI_CIn_DBG_ERR, n=[0..3]

Type: Read
Clock: DM_CORE
Reset State: 0x00000000

The HI_CIn_DBG_ERR register is the CI debug register for the indicated client interface.

ADM3_0_HI_CIn_DBG_ERR

Bits	Name	Description
31:16	DATA_BUS_ERR	The N'th bit in the mask becomes set (1) when the N'th channel data transfer traffic causes a bus error on this interface. By clearing the ERROR bit in the HI0_CHn_DBG_0 register, the bit corresponding to the channel will be cleared in this register.
15:0	CMD_BUS_ERR	The N'th bit in the mask becomes set (1) when the N'th channel command fetch traffic causes a bus error on this interface. By clearing the ERROR bit in the HI0_CHn_DBG_0 register, the bit corresponding to the channel will be cleared in this register.

0x183003D0 ADM3_0_HI_CRCI_CONF0

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00000000

The HI_CRCI_CONF0 register is the CRCI configuration register.

ADM3_0_HI_CRCI_CONF0

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:27	CRCI9_SEC_DOMAIN	Specifies the security domain of HI_CRCI9_CTL register
26:24	CRCI8_SEC_DOMAIN	Specifies the security domain of HI_CRCI8_CTL register
23:21	CRCI7_SEC_DOMAIN	Specifies the security domain of HI_CRCI7_CTL register
20:18	CRCI6_SEC_DOMAIN	Specifies the security domain of HI_CRCI6_CTL register
17:15	CRCI5_SEC_DOMAIN	Specifies the security domain of HI_CRCI5_CTL register
14:12	CRCI4_SEC_DOMAIN	Specifies the security domain of HI_CRCI4_CTL register
11:9	CRCI3_SEC_DOMAIN	Specifies the security domain of HI_CRCI3_CTL register
8:6	CRCI2_SEC_DOMAIN	Specifies the security domain of HI_CRCI2_CTL register
5:3	CRCI1_SEC_DOMAIN	Specifies the security domain of HI_CRCI1_CTL register
2:0	CRCI0_SEC_DOMAIN	Specifies the security domain of HI_CRCI0_CTL register

0x183003D4 ADM3_0_HI_CRCI_CONF1

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00000000

The HI_CRCI_CONF1 register is the CRCI control register.

ADM3_0_HI_CRCI_CONF1

Bits	Name	Description
31:18	RESERVED_BITS31_18	
17:15	CRCI15_SEC_DOMAIN	Specifies the security domain of HI_CRCI15_CTL register
14:12	CRCI14_SEC_DOMAIN	Specifies the security domain of HI_CRCI14_CTL register
11:9	CRCI13_SEC_DOMAIN	Specifies the security domain of HI_CRCI13_CTL register
8:6	CRCI12_SEC_DOMAIN	Specifies the security domain of HI_CRCI12_CTL register
5:3	CRCI11_SEC_DOMAIN	Specifies the security domain of HI_CRCI11_CTL register
2:0	CRCI10_SEC_DOMAIN	Specifies the security domain of HI_CRCI10_CTL register

0x183003D8 ADM3_0_HI_GP_CTL

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00000000

.The HI_GP_CTL is a general purpose register that can be tailored for chip specific uses

ADM3_0_HI_GP_CTL

Bits	Name	Description
31:12	RESERVED_BITS31_12	
11:8	LP_CNT	The programmable counter is used to add more delay between AHB CI CLKON and HTRANS.
7	CI3_CLK_LP_EN	When set (1) this bit enables the corresponding CI low power feature. (CI clock gated when CI is idle). When clear (0) this bits disables the corresponding CI low power feature. (CI clock no gated).
6	CI2_CLK_LP_EN	When set (1) this bit enables the corresponding CI low power feature. (CI clock gated when CI is idle). When clear (0) this bits disables the corresponding CI low power feature. (CI clock no gated).

ADM3_0_HI_GP_CTL (cont.)

Bits	Name	Description
5	CI1_CLK_LP_EN	When set (1) this bit enables the corresponding CI low power feature. (CI clock gated when CI is idle). When clear (0) this bits disables the corresponding CI low power feature. (CI clock no gated).
4	CI0_CLK_LP_EN	When set (1) this bit enables the corresponding CI low power feature. (CI clock gated when CI is idle). When clear (0) this bits disables the corresponding CI low power feature. (CI clock no gated).
3	RESERVED_BITS3	
2	CI2_ISYNC_MODE_SEL_N	When set (1), this bit places the CI2 ISYNC AXI fifos in asynchronous operation mode. When cleared (0), this bit places the CI2 ISYNC AXI fifos in iso-synchronous operation mode. This field becomes `0' after reset.
1	CI1_ISYNC_MODE_SEL_N	When set (1), this bit places the CI1 ISYNC AXI fifos in asynchronous operation mode. When cleared (0), this bit places the CI1 ISYNC AXI fifos in iso-synchronous operation mode. This field becomes `0' after reset.
0	CI0_ISYNC_MODE_SEL_N	When set (1), this bit places the CI0 ISYNC AXI fifos in asynchronous operation mode. When cleared (0), this bit places the CI0 ISYNC AXI fifos in iso-synchronous operation mode. This field becomes `0' after reset.

0x183003E0 ADM3_0_HI_GLBL_DBG_CMD_ENG

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00000000

NOTE This register always returns "0". Writing to this register has no affect.

ADM3_0_HI_GLBL_DBG_CMD_ENG

Bits	Name	Description
31:0	DBG_STATE	TBD

0x183003E4 ADM3_0_HI_GLBL_DBG_REQ_ENG

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00000000

NOTE This register always returns "0". Writing to this register has no affect.

ADM3_0_HI_GLBL_DBG_REQ_ENG

Bits	Name	Description
31:0	DBG_STATE	TBD

0x183003E8 ADM3_0_HI_GLBL_DBG_XFR_ENG

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00000000

NOTE This register always returns "0". Writing to this register has no affect.

ADM3_0_HI_GLBL_DBG_XFR_ENG

Bits	Name	Description
31:0	DBG_STATE	TBD

0x183003EC ADM3_0_HI_GLBL_DBG_CHAN_BLK

Type: Read
Clock: DM_CORE
Reset State: 0x00000000

ADM3_0_HI_GLBL_DBG_CHAN_BLK

Bits	Name	Description
15:0	CHAN_BLK_MASK	Indicates which channel(s) are currently blocked (see other channel block or this channel block command arguments)

0x183003F0 ADM3_0_HI_GLBL_DBG_CHAN_BLK_CLR

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00000000

ADM3_0_HI_GLBL_DBG_CHAN_BLK_CLR

Bits	Name	Description
3:0	CHAN_BLK_CLR_CHAN_NNUM	Writing to this register causes the bit, corresponding to the channel number written, in GLBL_DBG_CHAN_BLK register to clear. This allows hosts to selectively clear channel block bits without relying on read-modify-write of GLBL_DBG_CHAN_BLK that would cause race-condition.

0x183003F4 ADM3_0_HI_GLBL_DBG_TEST_SEL

Type: Read/Write
Clock: DM_CORE
Reset State: 0x00000000

NOTE For the Client Interface test buses to work properly, all Client Interfaces must not be in the low power mode.

ADM3_0_HI_GLBL_DBG_TEST_SEL

Bits	Name	Description
5:0	TEST_BUS_SEL	This signal selects the signals to show on the DM3 testbus. The encoding for each set of test signal is as follows: 0x0: None (output is all zeros) 0x1: Reserved_programming_1 0x2: Reserved_programming_2 0x3: Reserved_programming_3 0x4: Command engine 0x8: Request engine 0xC: Transfer engine 0x10: Reserved_programming_4 0x20: CI0 0x24: CI1 0x28: CI2 0x2C: CI3 0x30: HI AHB2AHB BRIDGE

2.10 TSSC Registers (0x18600000 TSSC_BASE)

This section contains TSSC registers.

0x18600100 TSSC_CTL

Type: Read/Write
Clock: CC_TSSC_CLK
Reset State: 0x0000

The TSSC_CTL register is the master control register for the TSSC. Note, the ENABLE need not be reset to 0 between two TS operation unless the software wants to disable the TSSC and take over its functionality.

TSSC_CTL

Bits	Name	Description
31:13	RESERVED31_13	Reserved31_13
13	TOTAL_SSBI_CTRL_EN	If enables, blocks SSBI Master for entire duration of programmed operation(s) in Master/Slave mode 0x0: selectively reserve SSBI 0x1: reserve SSBI for all operations
12	INTR_FLAG2	This is set `1' along with PENUP_IRQ assertion.
11	DATA_FLAG	If set, indicates a valid data is present. This flag needs to be explicitly cleared by the Software (upon sample read). Collection of subsequent samples in master mode WILL NOT start unless a set DataFlag is cleared.
10	INTR_FLAG1	Set to 1 by TSSC along with SAMPLE_IRQ assertion.
9:7	DEBOUNCE_TIME	Decides the debounce time 0x0: 400 us 0x1: 800 us 0x2: 1.2 ms 0x3: 1.6 ms 0x4: 2 ms 0x5: 3 ms 0x6: 4 ms 0x7: 6 ms
6	DEBOUNCE_EN	Enables the Debounce Logic inside TSSC. 0x0: Disables TSSC Debounce Logic 0x1: Enables TSSC Debounce Logic
5	EN_AVERAGE	Enables Averaging function. In this case, the collected samples are averaged and the average value is stored in a separate register TSSC_AVG

TSSC_CTL (cont.)

Bits	Name	Description
4:3	MODE	0x0: TSSC disabled 0x1: BYPASS mode 0x2: Slave Mode 0x3: Master Mode
2	TSSC_SW_RESET	Writing a `1' to this bit resets the TSSC. The TSSC has to be enabled for this reset to take effect. This bit need not be cleared to de-assert. This is similar to a command_wr.
1	COMMAND_WR	Writing a `1' to this bit, triggers an operation in Slave/Master mode. This is optional for master (non-intr initiated) and must for slave mode.
0	ENABLE	Enables TSSC. Propagates Clock to the registers inside

0x18600104 TSSC_OPN

Type: Read/Write
Clock: CC_TSSC_CLK
Reset State: 0x0000

The TSSC_OPN holds details on the 4 different operations that the TSSC is supposed to do when in Master mode and also it tells the sequence in which the four operations are to be done.This register has four such 4-bit fields. The fields NUM_SAMPLE and RESOLUTION respectively set the number of samples and resolution for OPERATION.

TSSC_OPN

Bits	Name	Description
31:28	OPERATION4	Place Holder for Fourth Operation in Master Mode
27:24	OPERATION3	Place holder for Third operation in Master mode
23:20	OPERATION2	Place holder for second operation in Master Mode
19:16	OPERATION1	.Place holder for Slave Mode operation and first operation in Master Mode.
15:14	NUM_SAMPLE4	Number of Samples for Operation 4 0x0: One Sample 0x1: Four Samples 0x2: Eight Samples 0x3: Sixteen Samples
13:12	NUM_SAMPLE3	Number of Sample for Operation 3. Options same as above
11:10	NUM_SAMPLE2	Number of Sample for Operation 2.Options same as above
9:8	NUM_SAMPLE1	Number of Sample for Operation 1 and for slave Mode.Options same as above

TSSC_OPN (cont.)

Bits	Name	Description
7:6	RESOLUTION4	Resolution for Operation 4. 0x0: 8-bit resolution 0x1: 10-bit resolution 0x2: 12-bit resolution 0x3: reserved (if set, interpreted as 10 inside)
5:4	RESOLUTION3	Resolution setting for Operation 3
3:2	RESOLUTION2	Resolution setting for Operation 2
1:0	RESOLUTION1	Resolution setting for Operation1 and for Slave Mode.

0x18600108 TSSC_SAMPLING_INT

Type: Read/Write
Clock: CC_TSSC_CLK
Reset State: 0x0000

The TSSC_SAMPLING_INT register holds the Sampling Interval details. The SAMPLING_INT field gives the sampling interval in milliseconds. This has to be specified in unsigned binary. Hence the possible settings are 1 to 31. Note: zero is an invalid setting for this field.

TSSC_SAMPLING_INT

Bits	Name	Description
31:5	RESERVED31_5	Reserved31_5
4:0	SAMPLING_INT	Specifies (in unsigned binary) the sampling interval in millisecond units

0x1860010C TSSC_STATUS

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0b00000UU000000000

The TSSC_STATUS is a read-only register. This is updated by the TSSC and is read by software in case of interrupt from TSSC.

TSSC_STATUS

Bits	Name	Description
31:21	RESERVED31_21	Reserved31_21
20:18	TSSC_SSBI_FSM_STATE	Dynamically reflects the state of the SSBI read/write state machine inside TSSC. Used for Debugging.

TSSC_STATUS (cont.)

Bits	Name	Description
17:14	TSSC_FSM_STATE	Dynamically reflects the state of the main TSSC FSM. Used for Debugging.
13	BUSY	This bit is set to `1' when the TSSC is in the middle of a sampling operation in Slave modes. In Master mode, this bit is `1' throughout the period that SI timer is running.
12:11	ERROR_CODE	Indicates the Error details. Valid only if ERROR flag is set. 0x0: No Error 0x1: Watch Dog timed out waiting for ADC_EOC 0x2: Reserved. 0x3: Reserved
10	ADC_EOC_STATUS	The raw ADC_EOC signal synchronized to the TSSC's clock domain.
9	PENIRQ_STATUS	This is the raw PEN_IRQ_N interrupt synchronized to the TSSC's clock domain.
8:6	OPERATION	Indicates the current operation in progress. This field and the following field can become handy during error conditions. 0x0: None 0x1: First operation 0x2: Second operation 0x3: Third operation 0x4: Fourth operation
5:1	SAMPLES_COLLECTED	This field dynamically indicates the current sample number that is being collected (The sample number is in unsigned binary).
0	ERROR	If set, an ERROR has occurred. The ERROR_CODE field indicates the details.

0x18600110 TSSC_AVG_12

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "average sample" values of Operation 1 and Operation 2 as detailed in TSSC_OPN register. In slave mode, the LS field has the average value of the operation programmed in TSSC_OPN[OPERATION1] field. The number of bits valid in each of these fields depends upon the RESOLUTION setting of the concerned operation in the TSSC_OPN register.

TSSC_AVG_12

Bits	Name	Description
31:16	SAMPLES_AVG_2	Average value of samples for Operation 2 (Master mode)

TSSC_AVG_12 (cont.)

Bits	Name	Description
15:0	SAMPLES_AVG_1	Average value of samples for Operation 1 in Master mode and Average value of samples for slave mode operation

0x18600114 TSSC_AVG_34

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "average sample" values of Operation 3 and Operation 4 as detailed in TSSC_OPN register. In slave mode, this register is unused. The number of bits valid in each of these fields depends upon the RESOLUTION setting of the concerned operation in the TSSC_OPN register.

TSSC_AVG_34

Bits	Name	Description
31:16	SAMPLES_AVG_4	Average value of samples for Operation 4 (Master mode)
15:0	SAMPLES_AVG_3	Average value of samples for Operation 3(Master mode)

0x18600118 TSSC_SAMPLE_1_1

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 1 and 2 of Master Mode Operation 1 and Slave mode operation as the case may be.

TSSC_SAMPLE_1_1

Bits	Name	Description
31:16	RAW_SAMPLE_2	Raw Sample 2 of Master Mode Opn.1 and Slave Mode
15:0	RAW_SAMPLE_1	Raw Sample 1 of Master mode Opn 1 and Slave Mode

0x1860011C TSSC_SAMPLE_1_2

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 3 and 4 of Master Mode Operation 1 and Slave mode operation as the case may be.

TSSC_SAMPLE_1_2

Bits	Name	Description
31:16	RAW_SAMPLE_4	Raw Sample 4of Master Mode Opn.1 and Slave Mode
15:0	RAW_SAMPLE_3	Raw Sample 3 of Master mode Opn 1 and Slave Mode

0x18600120 TSSC_SAMPLE_1_3

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 5 and 6 of Master Mode Operation 1 and Slave mode operation as the case may be.

TSSC_SAMPLE_1_3

Bits	Name	Description
31:16	RAW_SAMPLE_6	Raw Sample 6 of Master Mode Opn.1 and Slave Mode
15:0	RAW_SAMPLE_5	Raw Sample 5 of Master mode Opn 1 and Slave Mode

0x18600124 TSSC_SAMPLE_1_4

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample7 and 8 of Master Mode Operation 1 and Slave mode operation as the case may be.

TSSC_SAMPLE_1_4

Bits	Name	Description
31:16	RAW_SAMPLE_8	Raw Sample8 of Master Mode Opn.1 and Slave Mode
15:0	RAW_SAMPLE_7	Raw Sample 7 of Master mode Opn 1 and Slave Mode

0x18600128 TSSC_SAMPLE_1_5

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 9 and 10 of Master Mode Operation 1 and Slave mode operation as the case may be.

TSSC_SAMPLE_1_5

Bits	Name	Description
31:16	RAW_SAMPLE_10	Raw Sample 10 of Master Mode Opn.1 and Slave Mode
15:0	RAW_SAMPLE_9	Raw Sample 9 of Master mode Opn 1 and Slave Mode

0x1860012C TSSC_SAMPLE_1_6

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 11 and 12 of Master Mode Operation 1 and Slave mode operation as the case may be.

TSSC_SAMPLE_1_6

Bits	Name	Description
31:16	RAW_SAMPLE_12	Raw Sample 12 of Master Mode Opn.1 and Slave Mode
15:0	RAW_SAMPLE_11	Raw Sample 11 of Master mode Opn 1 and Slave Mode

0x18600130 TSSC_SAMPLE_1_7

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 13 and 14 of Master Mode Operation 1 and Slave mode operation as the case may be.

TSSC_SAMPLE_1_7

Bits	Name	Description
31:16	RAW_SAMPLE_14	Raw Sample 14 of Master Mode Opn.1 and Slave Mode
15:0	RAW_SAMPLE_13	Raw Sample 13 of Master mode Opn 1 and Slave Mode

0x18600134 TSSC_SAMPLE_1_8

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 15 and 16 of Master Mode Operation 1 and Slave mode operation as the case may be.

TSSC_SAMPLE_1_8

Bits	Name	Description
31:16	RAW_SAMPLE_16	Raw Sample 16 of Master Mode Opn.1 and Slave Mode
15:0	RAW_SAMPLE_15	Raw Sample 15 of Master mode Opn 1 and Slave Mode

0x18600138 TSSC_SAMPLE_2_1

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 1 and 2 of Master Mode Operation 2

TSSC_SAMPLE_2_1

Bits	Name	Description
31:16	RAW_SAMPLE_2	Raw Sample 2 of Master Mode Opn.2
15:0	RAW_SAMPLE_1	Raw Sample 1 of Master mode Opn 2

0x1860013C TSSC_SAMPLE_2_2

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 3 and 4 of Master Mode Operation 2.

TSSC_SAMPLE_2_2

Bits	Name	Description
31:16	RAW_SAMPLE_4	Raw Sample 4of Master Mode Opn.2
15:0	RAW_SAMPLE_3	Raw Sample 3 of Master mode Opn 2

0x18600140 TSSC_SAMPLE_2_3

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 5 and 6 of Master Mode Operation 2

TSSC_SAMPLE_2_3

Bits	Name	Description
31:16	RAW_SAMPLE_6	Raw Sample 6 of Master Mode Opn.2
15:0	RAW_SAMPLE_5	Raw Sample 5 of Master mode Opn 2

0x18600144 TSSC_SAMPLE_2_4

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample7 and 8 of Master Mode Operation 2

TSSC_SAMPLE_2_4

Bits	Name	Description
31:16	RAW_SAMPLE_8	Raw Sample8 of Master Mode Opn.2
15:0	RAW_SAMPLE_7	Raw Sample 7 of Master mode Opn 2

0x18600148 TSSC_SAMPLE_2_5

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 9 and 10 of Master Mode Operation 2

TSSC_SAMPLE_2_5

Bits	Name	Description
31:16	RAW_SAMPLE_10	Raw Sample 10 of Master Mode Opn.2
15:0	RAW_SAMPLE_9	Raw Sample 9 of Master mode Opn 2

0x1860014C TSSC_SAMPLE_2_6

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 11 and 12 of Master Mode Operation 2.

TSSC_SAMPLE_2_6

Bits	Name	Description
31:16	RAW_SAMPLE_12	Raw Sample 12 of Master Mode Opn.2
15:0	RAW_SAMPLE_11	Raw Sample 11 of Master mode Opn 2

0x18600150 TSSC_SAMPLE_2_7

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 13 and 14 of Master Mode Operation 2.

TSSC_SAMPLE_2_7

Bits	Name	Description
31:16	RAW_SAMPLE_14	Raw Sample 14 of Master Mode Opn.2
15:0	RAW_SAMPLE_13	Raw Sample 13 of Master mode Opn 2

0x18600154 TSSC_SAMPLE_2_8

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 15 and 16 of Master Mode Operation 2

TSSC_SAMPLE_2_8

Bits	Name	Description
31:16	RAW_SAMPLE_16	Raw Sample 16 of Master Mode Opn.2
15:0	RAW_SAMPLE_15	Raw Sample 15 of Master mode Opn 2

0x18600158 TSSC_SAMPLE_3_1

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 1 and 2 of Master Mode Operation 3

TSSC_SAMPLE_3_1

Bits	Name	Description
31:16	RAW_SAMPLE_2	Raw Sample 2 of Master Mode Opn.3
15:0	RAW_SAMPLE_1	Raw Sample 1 of Master mode Opn3

0x1860015C TSSC_SAMPLE_3_2

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 3 and 4 of Master Mode Operation 3.

TSSC_SAMPLE_3_2

Bits	Name	Description
31:16	RAW_SAMPLE_4	Raw Sample 4of Master Mode Opn.3
15:0	RAW_SAMPLE_3	Raw Sample 3 of Master mode Opn 3

0x18600160 TSSC_SAMPLE_3_3

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 5 and 6 of Master Mode Operation 3

TSSC_SAMPLE_3_3

Bits	Name	Description
31:16	RAW_SAMPLE_6	Raw Sample 6 of Master Mode Opn.3
15:0	RAW_SAMPLE_5	Raw Sample 5 of Master mode Opn 3

0x18600164 TSSC_SAMPLE_3_4

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample7 and 8 of Master Mode Operation 3

TSSC_SAMPLE_3_4

Bits	Name	Description
31:16	RAW_SAMPLE_8	Raw Sample8 of Master Mode Opn.3
15:0	RAW_SAMPLE_7	Raw Sample 7 of Master mode Opn 3

0x18600168 TSSC_SAMPLE_3_5

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 9 and 10 of Master Mode Operation 3

TSSC_SAMPLE_3_5

Bits	Name	Description
31:16	RAW_SAMPLE_10	Raw Sample 10 of Master Mode Opn.3
15:0	RAW_SAMPLE_9	Raw Sample 9 of Master mode Opn 3

0x1860016C TSSC_SAMPLE_3_6

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 11 and 12 of Master Mode Operation 3.

TSSC_SAMPLE_3_6

Bits	Name	Description
31:16	RAW_SAMPLE_12	Raw Sample 12 of Master Mode Opn.3
15:0	RAW_SAMPLE_11	Raw Sample 11 of Master mode Opn 3

0x18600170 TSSC_SAMPLE_3_7

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 13 and 14 of Master Mode Operation 3.

TSSC_SAMPLE_3_7

Bits	Name	Description
31:16	RAW_SAMPLE_14	Raw Sample 14 of Master Mode Opn.3
15:0	RAW_SAMPLE_13	Raw Sample 13 of Master mode Opn 3

0x18600174 TSSC_SAMPLE_3_8

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 15 and 16 of Master Mode Operation 3

TSSC_SAMPLE_3_8

Bits	Name	Description
31:16	RAW_SAMPLE_16	Raw Sample 16 of Master Mode Opn. 3
15:0	RAW_SAMPLE_15	Raw Sample 15 of Master mode Opn 3

0x18600178 TSSC_SAMPLE_4_1

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 1 and 2 of Master Mode Operation 4

TSSC_SAMPLE_4_1

Bits	Name	Description
31:16	RAW_SAMPLE_2	Raw Sample 2 of Master Mode Opn.4
15:0	RAW_SAMPLE_1	Raw Sample 1 of Master mode Opn4

0x1860017C TSSC_SAMPLE_4_2

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 3 and 4 of Master Mode Operation 4.

TSSC_SAMPLE_4_2

Bits	Name	Description
31:16	RAW_SAMPLE_4	Raw Sample 4of Master Mode Opn.4
15:0	RAW_SAMPLE_3	Raw Sample 3 of Master mode Opn 4

0x18600180 TSSC_SAMPLE_4_3

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 5 and 6 of Master Mode Operation 4

TSSC_SAMPLE_4_3

Bits	Name	Description
31:16	RAW_SAMPLE_6	Raw Sample 6 of Master Mode Opn.4
15:0	RAW_SAMPLE_5	Raw Sample 5 of Master mode Opn 4

0x18600184 TSSC_SAMPLE_4_4

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample7 and 8 of Master Mode Operation 4

TSSC_SAMPLE_4_4

Bits	Name	Description
31:16	RAW_SAMPLE_8	Raw Sample8 of Master Mode Opn.4
15:0	RAW_SAMPLE_7	Raw Sample 7 of Master mode Opn 4

0x18600188 TSSC_SAMPLE_4_5

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 9 and 10 of Master Mode Operation 4

TSSC_SAMPLE_4_5

Bits	Name	Description
31:16	RAW_SAMPLE_10	Raw Sample 10 of Master Mode Opn.4
15:0	RAW_SAMPLE_9	Raw Sample 9 of Master mode Opn 4

0x1860018C TSSC_SAMPLE_4_6

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 11 and 12 of Master Mode Operation 4.

TSSC_SAMPLE_4_6

Bits	Name	Description
31:16	RAW_SAMPLE_12	Raw Sample 12 of Master Mode Opn.4
15:0	RAW_SAMPLE_11	Raw Sample 11 of Master mode Opn 4

0x18600190 TSSC_SAMPLE_4_7

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 13 and 14 of Master Mode Operation 4.

TSSC_SAMPLE_4_7

Bits	Name	Description
31:16	RAW_SAMPLE_14	Raw Sample 14 of Master Mode Opn.4
15:0	RAW_SAMPLE_13	Raw Sample 13 of Master mode Opn 4

0x18600194 TSSC_SAMPLE_4_8

Type: Read
Clock: CC_TSSC_CLK
Reset State: 0x0000

This register holds the "raw values" of sample 15 and 16 of Master Mode Operation 4

TSSC_SAMPLE_4_8

Bits	Name	Description
31:16	RAW_SAMPLE_16	Raw Sample 16 of Master Mode Opn. 4
15:0	RAW_SAMPLE_15	Raw Sample 15 of Master mode Opn 4

0x18600198 TSSC_TEST_1

Type: Read/Write
Clock: CC_TSSC_CLK
Reset State: 0x0001

The TSSC_TEST_1 register holds the value of ssbi_rd_data and the penirq_n signals that will be muxed into the TSSC state machine during functional test mode. Also the mode bit that controls the muxing (TEST_MODE) is also present in this register.

TSSC_TEST_1

Bits	Name	Description
31:24	TEST_SSBI_RD_DATA	The value in these bits will be muxed in as SSBI Read data when ever TEST_MODE bit is set.
23:3	RESERVED23_3	Reserved23_3
2	GATE_DEBOUNCE_EN	Selects or deselects the Gating logic in the path of penirqn signal to the debounce block. A `0' means gating logic not selected. Penirqn directly goes to debounce block. A `1' in this bit includes Gating logic in penirqn path to debounce logic.
1	TEST_MODE	This bit controls muxing of eoc, penirqn and ssbi_rd_data signals into the TSSC state machine. If 0, the functional mode inputs are muxed in. If 1, these inputs will be controlled based on description provided in the TSSC_TEST registers 1 and 2.
0	TEST_PENIRQ_N	This bit is directly muxed into penirqn debounce logic as the pen down interrupt input if TEST_MODE bit is set.

0x1860019C TSSC_TEST_2

Type: Write/Command
Clock: CC_TSSC_CLK
Reset State: 0x0000

The TSSC_TEST_2 register is a Write-only command register. A write to this register generates a pulse whose width is CC_TSSC_CLK period. If TEST_MODE bit in TSSC_TEST_1 register is set, then this pulse will be muxed into the TSSC state machine as ADC_EOC pulse.

TSSC_TEST_2

Bits	Name	Description
31:0	RESERVED31_0	Reserved31_0

2.11 TSSC Codec SSBI Registers (0x18600000 TSSC_SSBI_BASE)

This section contains TSSC Codec SSBI registers.

0x18600000 TSSC_CODEC_SSBI_CTL

Type: Read/Write
Clock: CC_TSSC_CLK
Reset State: 0x18001

Specifies various generic control information. Bits 14:7 are needed only for master interface with FTM support

TSSC_CODEC_SSBI_CTL

Bits	Name	Description
16	SSBI_DATA_PDEN	Pull down enable for SSBI_DATA pad.
15	ACTIVATE_RESERVE	Reset this bit to disable RESERVE feature in arbiter.
14	DISABLE_TERM_SYM	In FTM mode, set this bit to disable the termination symbol.
13:8	SLAVE_ID	In FTM mode, specifies the Slave ID.
7	FTM_MODE	Set this bit to force all the transfers to be in FTM mode.
6:5	SEL_RD_DATA	Specifies which RD_DATA value to select.
4	ENABLE_SSBI_INT	SSBI_INT is generated only when this bit is set.
3:2	SSBI_DATA_DEL	Specifies the number of 1/2 clock periods, SSBI_DATA will be delayed before sampling.
1:0	IDLE_SYMS	The master will ensure there are at least this number of Idle symbol periods in between the accesses. For successive writes, this value can be `0'. However if the following access is a read operation, then this value has to be greater then `0'.

0x18600004 TSSC_CODEC_SSBI_RESET

Type: Write
Clock: CC_TSSC_CLK

A write to this register resets the SSBI blocks.

TSSC_CODEC_SSBI_RESET

Bits	Name	Description
31:0	RESERVED31_0	Reserved31_0

0x18600008 TSSC_CODEC_SSBI_CMD

Type: Write
Clock: CC_TSSC_CLK

Specifies the information to use for the transfer. For both reads and writes, SW must write to this register to initiate the transfer. The REG_DATA field is ignored for reads. For a read, once it has completed, read the data through SSBI_RD. Note that, if SW initiates a read, it is expected that no subsequent access will be done until that data has been read from SSBI_RD

TSSC_CODEC_SSBI_CMD

Bits	Name	Description
27	SEND_TERM_SYM	In FTM mode, writing `1' to this bit will generate just the termination symbol without requesting for an access.
26	WAKEUP_SLAVE	When set (1), a single pulse will be send to Slave, followed by 10 idle clocks, followed by a read or write transaction.
25	USE_ENABLE	When set (1), this transaction will be stalled until the ENABLE input is set. Normally this feature is not used, hence this bit will be 0.
24	RDWRN	Denotes whether the command to perform is a register write (0) or read (1).
23:16	REG_ADD	Slave register address.
7:0	REG_DATA	Write data for a slave register. SSBI_DATA_WD can be in range 16 - 1.

0x1860000C TSSC_CODEC_SSBI_BYPASS

Type: Read/Write
Clock: CC_TSSC_CLK
Reset State: 0x0000

Allows SW to override SSBI_DATA value.

TSSC_CODEC_SSBI_BYPASS

Bits	Name	Description
1	OVR_VALUE	When OVR_MODE is 1, this bit is driven onto SSBI_DATA. This is NOT intended to enable SW to bit-bang SSBI commands. Rather, this is a safety option in case a need arises to program this bit differently in idle mode.
0	OVR_MODE	Override mode bit. When set (1), the value driven onto SSBI_DATA is given by OVR_VALUE.

0x18600010 TSSC_CODEC_SSBI_RD

Type: Read
Clock: CC_TSSC_CLK

When reading a slave register, write to SSBI_CMD (REG_DATA will be ignored). Once data is ready, read this register and it will return the returned data from the slave and the other fields filled in correctly to match. Reading from this register may clear some bits in SSBI_STATUS. Note if SW writes to SSBI_CMD before reading the contents of this register, all fields except REG_DATA may be invalid, and depending on the second access, REG_DATA may reflect the first read data or second read data

TSSC_CODEC_SSBI_RD

Bits	Name	Description
25	USE_ENABLE	Reflects how SSBI_CMD was written to initiate this read.
24	RDWRN	Reflects how SSBI_CMD was written to initiate this read.
23:16	REG_ADD	Reflects how SSBI_CMD was written to initiate this read.
7:0	REG_DATA	Returned read register data. SSBI_DATA_WD can be in range 16 - 1.

0x18600014 TSSC_CODEC_SSBI_STATUS

Type: Read
Clock: CC_TSSC_CLK

Returns information about the internal status of the SSBI master. If SW wants to perform an access, it should first ensure READY is 1. If SW wants to wait until the transfer has completed, it can poll MCHN_BUSY. If SW wants to know when read data has returned, it can poll RD_READY

TSSC_CODEC_SSBI_STATUS

Bits	Name	Description
4	SSBI_DATA_IN	Returns the instantaneous value of SSBI_DATA input. This is not affected by SSBI_DATA_DEL. This is intended as a test feature.
3	RD_CLOBBERED	This bit gets set (1) if SW initiates another access (read or write) while a SSBI read is being performed. The result of this action is that all the fields except RD_DATA in SSBI_RD will be invalid. Reads from SSBI_RD clear this bit.
2	RD_READY	Normally clear (0). If a SSBI read is performed, this bit will be set upon read completion (DONE assertion). Reads from SSBI_RD clear this bit.

TSSC_CODEC_SSBI_STATUS (cont.)

Bits	Name	Description
1	READY	Indicates that the master can accept a new transfer request. When clear (0), further writes to SSBI_CMD should not be done since the previous access may be lost. This signal will be clear for the duration from REQ assertion until ACK assertion. It also remains clear following reset, until the time SW writes to SSBI_CTL register and resets SSBI_DATA_PDEN bit.
0	MCHN_BUSY	When set (1), indicates the SSBI master is actively performing a transfer. This signal will be set for the duration from REQ assertion until DONE assertion.

0x18600018 TSSC_CODEC_SSBI_PRIORITIES

Type: Read/Write
Clock: CC_TSSC_CLK
Reset State: 0x0000

Specifies the priorities for SSBI ports. The SSBI block supports up to max. 8 ports for arbitration. Each port has 3 bits to specify its priority. Only three ports are shown here, for additional ports assume 3bits/port with priority 1 less then the port below it.

TSSC_CODEC_SSBI_PRIORITIES

Bits	Name	Description
8:6	PRIORITY2	Specifies the port of host, whose priority is 1 less then PRIORITY1
5:3	PRIORITY1	Specifies the port of host, whose priority is 1 less then PRIORITY0
2:0	PRIORITY0	Specifies the port of the highest priority host

2.12 WEB TCXO4 registers (0x18700000 MSM_PDM_BASE)

This section contains WEB TCX registers.

0x18700040 TCXO_PDM_CTL

Type: Read/Write
Clock: CC_PBUS_CLK
Reset State: 0x00

The TCXO_PDM_CTL register is used to enable/disable the PDM0 and PDM1 pins, and to configure the mode of operation for the PDM output.

TCXO_PDM_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	Reserved bits
5	PDM2_POLARITY	This bit defines the polarity of PDM2. Set (1) this bit to invert the sense of the PDM output.
4	PDM1_POLARITY	This bit defines the polarity of PDM1. Set (1) this bit to invert the sense of the PDM output.
3	PDM0_POLARITY	This bit defines the polarity of PDM0. Set (1) this bit to invert the sense of the PDM output.
2	PDM2_EN	· Setting (1) this bit enables the PDM2 pin. · Clearing (0) this bit disables PDM2 and places it in a high impedance state. This bit is cleared on RESOUT.
1	PDM1_EN	· Setting (1) this bit enables the PDM1 pin. · Clearing (0) this bit disables PDM1 and places it in a high impedance state. This bit is cleared on RESOUT.
0	PDM0_EN	· Setting (1) this bit enables the PDM0 pin. · Clearing (0) this bit disables PDM0 and places it in a high impedance state. This bit is cleared on RESOUT. This bit is WRITE ONLY in perph_web_p3q3r15

0x18700044 PDM0_CTL

Type: Read/Write
Clock: CC_PBUS_CLK
Reset State: 0x8000

The PDM0_CTL register is the pulse density modulation register number 0. This register determines the density of pulses on the PDM0 pin.

PDM0_CTL

Bits	Name	Description
15:0	PDM0_DAT	When the PDM0_POLARITY is set, the output sense is inverted and the clock source is GENERAL_CLK/4.

0x18700048 PDM1_CTL

Type: Read/Write
Clock: CC_PBUS_CLK
Reset State: 0x80

The PDM1_CTL register is the pulse density modulation register number 1. This register determines the density of pulses on the PDM1 pin.

PDM1_CTL

Bits	Name	Description
7:0	PDM1_DAT	When the PDM1_POLARITY is set, the output sense is inverted and the clock source is GENERAL_CLK/4.

0x1870004C GP_MN_CLK_MDIV

Type: Read/Write
Clock: CC_PBUS_CLK
Reset State: Undefined

The GP_MN_CLK_MDIV register is the MDIV specification register for the GP M/N clock. For all GP_MN registers, this signal is generated by dividing the frequency of the TCXO signal by an M/N counter. M and N have the following specifications:

- The maximum value of M is 511.
- The maximum value of N is 8191.
- The value of M cannot exceed the value of N.

GP_MN_CLK_MDIV

Bits	Name	Description
8:0	GP_M_VALUE	This register defines the value of M for the M/N counter, which generates the GP_MN signal.

0x18700050 GP_MN_CLK_NDIV

Type: Read/Write
Clock: CC_PBUS_CLK
Reset State: Undefined

The GP_MN_CLK_NDIV register is the NDIV specification register for the GP M/N clock.

GP_MN_CLK_NDIV

Bits	Name	Description
12:0	GP_N_VALUE	This register defines the 1'Bits complement value of N minus M for the M/N counter, which generates the GP_MN signal. Write 0x1F to this register for APQ 2.2 compatibility.

0x18700054 GP_MN_CLK_DUTY

Type: Read/Write
Clock: CC_PBUS_CLK
Reset State: Undefined

The GP_MN_CLK_DUTY register is the duty cycle specification register for the GP M/N clock.

GP_MN_CLK_DUTY

Bits	Name	Description
12:0	GP_D_VALUE	This register defines the value of D, which determines the duty cycle of the GP M/N signal. The useful value of D must be in the range of M to N minus M.

0x18700058 WEB_TCXO4_TEST

Type: Read Only
Clock: CC_PBUS_CLK
Reset State: Undefined

The WEB_TCXO4_TEST register allows the current state of the web_tcxo4 output pads to be observed for test purposes.

WEB_TCXO4_TEST

Bits	Name	Description
15:14	RESERVED15_14	
13	PDM2_EDGE	Low to high edge on tlmm_gp_pdm2 input from pad. Read to clear.

WEB_TCXO4_TEST (cont.)

Bits	Name	Description
12	PDM2	Read tlmm_gp_pdm2 input from pad.
11:10	RESERVED11_10	
9	GP_MN_EDGE	Low to high edge on tlmm_gp_mn input from pad. Read to clear.
8	GP_MN	Read tlmm_gp_mn input from pad.
7:6	RESERVED7_6	
5	PDM1_EDGE	Low to high edge on tlmm_gp_pdm1 input from pad. Read to clear.
4	PDM1	Read tlmm_gp_pdm1 input from pad.
3:2	RESERVED3_2	
1	PDM0_EDGE	Low to high edge on tlmm_gp_pdm0 input from pad. Read to clear.
0	PDM0	Read tlmm_gp_pdm0 input from pad.

0x1870005C PDM2_CTL

Type: Read/Write
Clock: CC_PBUS_CLK
Reset State: 0x8000

The PDM2_CTL register is the pulse density modulation register number 2. This register determines the density of pulses on the PDM2 pin.

PDM2_CTL

Bits	Name	Description
15:0	PDM2_DAT	When the PDM2_POLARITY is set, the output sense is inverted and the clock source is GENERAL_CLK.

2.13 Chip System FPB1 Master Registers (0x18D00000 CSYSFPB_MST_BASE)

This section contains Chip System FPB registers.

0x18D00000 CSYSFPB_MST_CFPB_MASTER_CTRL_STATUS

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: 0x00000000

This register is a general configuration register.

CSYSFPB_MST_CFPB_MASTER_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables Power up value is clear (0)
11	RPM_PROC_IRQ_EN	SW: RW, HW: R RPMProcessorInterruptEnable When set, the RPM processor receives an interrupt whenever ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	APPS_PROC_IRQ_EN	SW: RW, HW: R Apps_ProcInterruptEnable When set, the Application Processor receives an interrupt whenever ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

CSYSFPB_MST_CFPB_MASTER_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x5: Select the S0_M0 ahb2ahb bridge test bus. 0x6: Select the S1_M1 ahb2ahb bridge test bus. 0x7: Select the M0 ahb2ahb bridge test bus. 0x8: Select the M1 ahb2ahb bridge test bus. 0x9: Select the M2 ahb2ahb bridge test bus. 0xA: Select the M3 ahb2ahb bridge test bus. 0xB: Select the M4 ahb2ahb bridge test bus. 0xC: Select the M5 ahb2ahb bridge test bus. 0xD: Select the M6 ahb2ahb bridge test bus. 0xE: Select the M7 ahb2ahb bridge test bus. 0xF: Select the M8 ahb2ahb bridge test bus. 0x10: Select the M9 ahb2ahb bridge test bus. 0x11: Select the M10 ahb2ahb bridge test bus. 0x12: Select the M11 ahb2ahb bridge test bus. 0x13: Select the M12 ahb2ahb bridge test bus. 0x14: Select the M13 ahb2ahb bridge test bus. 0x15: Select the M14 ahb2ahb bridge test bus. 0x16: Select the M15 ahb2ahb bridge test bus.

0x18D00004+0x4*a CSYSFPB_MST_CFPB_MASTER_AHB2AHB_CFG_Ma, a=[0..3]

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: 0x00000009

The CFPB_MASTER_AHB2AHB_CFG_Ma register is to configure the AHB2AHB bridge of master Ma. The AHB2AHB bridge is instantiated if the AHB interface is async (Generic: MASTER_ASYNC_IF(a) = ’1’). Otherwise this register is reserved.

CSYSFPB_MST_CFPB_MASTER_AHB2AHB_CFG_Ma

Bits	Name	Description
30:6	RESERVED_BITS30_6	

CSYSFPB_MST_CFPB_MASTER_AHB2AHB_CFG_Ma (cont.)

Bits	Name	Description
5:4	M_AHB2AHB_TEST_EN	SW: RW, HW: R Test enable for the Sa lite_bridge. Power up value is 00 0x0: DISABLED 0x1: Select slave side test signals 0x2: Select master side test signals 0x3: RESERVED_PROGRAMMING
3	M_WPOST_EN	SW: RW, HW: R MaWritePostEnable When set (1), the ahb2ahb bridge will support posting of write data. When cleared (0), each write request must complete across the bus before the next is accepted. Power up value is set (1)
2	M_HALT_ACK	SW:R, HW:W Indicates the Ma acknowledgement of halt_req asserted by software. Power up value is clear (0).
1	M_HALT_REQ	SW:RW, HW:R Software should write to this register to request the Ma lite_bridge master to cleanly halt. Power up value is clear (0).
0	M_IDLE	SW:R, HW:W Indicates that the Ma lite bridge master FSM is in IDLE state. Power up value is set (1).

0x18D00044 CSYSFPB_MST_CFPB_MASTER_PORT_EN

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: 0x0000000F

This register is the CFPB_MASTER master port enable register.

CSYSFPB_MST_CFPB_MASTER_PORT_EN

Bits	Name	Description
31:4	RESERVED_BIT31_4	Not used as only 4 Master ports are used.
3	M3_PORT_EN	SW: RW, HW: R M3PortEnable When cleared (0), M3 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

CSYSFPB_MST_CFPB_MASTER_PORT_EN (cont.)

Bits	Name	Description
2	M2_PORT_EN	SW: RW, HW: R M2PortEnable When cleared (0), M2 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)
1	M1_PORT_EN	SW: RW, HW: R M1PortEnable When cleared (0), M1 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)
0	M0_PORT_EN	SW: RW, HW: R M0PortEnable When cleared (0), M0 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

0x18D00050 CSYSFPB_MST_CFPB_MASTER_ERROR_STAT

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: 0x00000000

This register is the bus error status register.

CSYSFPB_MST_CFPB_MASTER_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the channel ID that caused the detected error when CID is valid for the master of the access. If not, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	

CSYSFPB_MST_CFPB_MASTER_ERROR_STAT (cont.)

Bits	Name	Description
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Master0 0x1: Master1 0x2: Master2 0x3: Master3 0x4: Master4 0x5: Master5 0x6: Master6 0x7: Master7 0x8: Master8 0x9: Master9 0xA: Master10 0xB: Master11 0xC: Master12 0xD: Master13 0xE: Master14 0xF: Master15
11:10	RESERVED_BITS11_10	
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit

CSYSFPB_MST_CFPB_MASTER_ERROR_STAT (cont.)

Bits	Name	Description
3:2	RESERVED_BIT3_2	
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted. Clearing (0) this bit clears any interrupts asserted as well as enables the ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x18D00054 CSYSFPB_MST_CFPB_MASTER_ERROR_ADDR

Type: Read
Clock: CC_CFPB_MASTER_CLK
Reset State: 0x00000000

This register contains the bus error address.

CSYSFPB_MST_CFPB_MASTER_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x18D0005C CSYSFPB_MST_CFPB_MASTER_XPU_ACR

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: 0xFFFFFFFF

The CFPB_MASTER_XPU_ACR register is the CFPB_MASTER Access Control Register for configuring register protection.

CSYSFPB_MST_CFPB_MASTER_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R CFPB_MASTER XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the CFPB_MASTER configure space, including this register itself. Power up value is set (1)

0x18D00060 CSYSFPB_MST_CFPB_MASTER_HW_CLK_GATING_CFG

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: 0x00000000

The CFPB_MASTER_HW_CLK_GATING_CFG register is for hardware clock gating configuration.

CSYSFPB_MST_CFPB_MASTER_HW_CLK_GATING_CFG

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	HYSTERESIS_CNT_SW	SW: RW, HW: R Hysteresis Counter Value This field is used by SW to set the hysteresis counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)
3:0	WAKE_CNT_SW	SW: RW, HW: R Wakeup Counter Value This field is used by SW to set the wakeup counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)

0x18D00064 CSYSFPB_MST_CFPB_MASTER_XPU_ACR_ERR_STATUS

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: 0x00000000

The CFPB_MASTER_XPU_ACR_ERR_STATUS register is for capturing the status when there is an XPU (ACR) access error.

M2VMT (hmaster index) registers (existing when VMIDMAPPER=1)

CSYSFPB_MST_CFPB_MASTER_XPU_ACR_ERR_STATUS

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:22	HVMID	SW: RW, HW: W HVMID of the CSR access that caused an Error. Only valid when ERROR_DETECT_CSR is set (1). ERROR_DETECT_CSR must be cleared (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT_CSR has been cleared (0).
21	HWRITE	SW: RW, HW: W HVMID of the CSR access that caused an Error. Only valid when ERROR_DETECT_CSR is set (1). ERROR_DETECT_CSR must be cleared (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT_CSR has been cleared (0).
20:9	HADDR	SW: RW, HW: W HADDR of the CSR access that caused an Error. Only valid when ERROR_DETECT_CSR is set (1). ERROR_DETECT_CSR must be cleared (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT_CSR has been cleared (0).
8:6	HSIZE	SW: RW, HW: W HSIZE of the CSR access that caused an Error. Only valid when ERROR_DETECT_CSR is set (1). ERROR_DETECT_CSR must be cleared (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT_CSR has been cleared (0).
5	HPROTNS	SW: RW, HW: W HPROTNS of the CSR access that caused an Error. Only valid when ERROR_DETECT_CSR is set (1). ERROR_DETECT_CSR must be cleared (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT_CSR has been cleared (0).
4:1	HPROT	SW: RW, HW: W HPROT of the CSR access that caused an Error. Only valid when ERROR_DETECT_CSR is set (1). ERROR_DETECT_CSR must be cleared (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT_CSR has been cleared (0).
0	ERROR_DETECT_CSR	SW: RW, HW: RW ErrorDetect during CSR accesses. When set (1), a bus error has been detected and interrupts will be asserted. Clearing (0) this bit clears any interrupts asserted as well as enables this register to capture the next error detected. Power up value is clear (0)

0x18D01000+ 0x4*n CSYSFPB_MST_CFPB_MASTER_M2VMT_M2VMRn, n=[0..3]

Type: Read/Write
Clock: CC_CFPB_MASTER_CLKCC_CFPB_MASTER_CLK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where n = NUM_M2VMT_ENTRIES from the design generics and we map NUM_M2VMT_ENTRIES to NUM_MASTERS.

Since n=2 is TSIF DM master (uses CID), the set of registers starting at addr_offset 0x1000 can be ignored for the index=2. Instead, the set of registers starting at address_offset 0x2000 are to be used.

CSYSFPB_MST_CFPB_MASTER_M2VMT_M2VMRn

Bits	Name	Description
31:5	RESERVED	
4:0	VMID	Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRn address associations. n = NUM_M2VMT_ENTRIES from the design generic/parameter.

0x18D01F80 CSYSFPB_MST_CFPB_MASTER_M2VMT_CR

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: xxx0

Global configuration register.

Note: When REMOVE_M2VMT_RPU = ‘1’, this register is not available. Also, bit [2], is not valid or has no effect when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT =‘1’.

CSYSFPB_MST_CFPB_MASTER_M2VMT_CR

Bits	Name	Description
31:4	RESERVED	

CSYSFPB_MST_CFPB_MASTER_M2VMT_CR (cont.)

Bits	Name	Description
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., in valid addresses) are recorded as such. Decode error is asserted when config access to un-implemented and/or unmapped register/address are done. Also, note that decode error is never asserted for client port accesses. When value is set to ’0’, i.e., ’do not record’, decode errors do not set the M2VMT_ESR[CFG], and M2VMT_EAR & M2VMT_SYNRn is not updated. When value is set to ’1’, i.e., ’record’, decode errors set M2VMT_ESR[CFG] and M2VMT_EAR & M2VMT_SYNRn is updated with the address and the syndrome of the error. Reset State: x
2	RPUEIE	RPU error interrupt Enable: When set, configuration port errors are reported directly to the interrupt controller via the M2VMT_intr, interrupt output signal. Interrupt output is asserted if M2VMT_CR[RPUIE_EN] is ’1’ and ANY bit is set in the M2VMT_ESR register. Special Note: Not valid or has no effect on the interrupt when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT=’1’. Reset State: x
1	RPUERE	RPU error report enable: When set, M2VMT reports configuration port errors to the requesting bus master, according to the respective port’s bus protocol. All error types reported via CRIF port will use a decode error, rather than a slave error. Regardless of the value of this field, both configuration port errors are terminated by the M2VMT as RAZ/WI, and are recorded in M2VMT_ESR register. Reset State: X
0	RPUE	RPU Enable: Governs whether M2VMT_RPU_ACR is enabled to check the VMID of the configuration request. When set, all configuration port accesses are checked against M2VMT_RPU_ACR register for access permissions. It’s cleared by reset. Set once SROT configures MID->VMID mapping tables Reset State: 0

0x18D01F84 CSYSFPB_MST_CFPB_MASTER_M2VMT_EAR

Type: Read
Clock: CC_CFPB_MASTER_CLK
Reset State: unknown

When there is an error, this register holds the physical address of the errant transaction.

CSYSFPB_MST_CFPB_MASTER_M2VMT_EAR

Bits	Name	Description
31:0	PA	M2VMT Error Address Register: Physical address[31:0]. Contains the physical address of the errant request. Based on implementation, it may not contain the full 32 bits of the address. Captures the address on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. Special Note: When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT = '1', this register is not available and therefore access to this register are treated as RAZ/WI.

0x18D01F88 CSYSFPB_MST_CFPB_MASTER_M2VMT_ESR

Type: Read/Write to clear
Clock: CC_CFPB_MASTER_CLK
Reset State: Undefined

M2VMT Error Status Register:

Captures the status upon M2VMT configuration errors, as determined by the M2VMT_RPU_ACR.

This register has read/write-clear access, meaning that reads simply provide a value in the register, while writes are performed by clearing those bits corresponding to '1's in the value written data, and leaving unchanged those bits corresponding to 0s n the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old error. A write with a '1' set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

The presence of an asserted value on any bit in this register is what prompts the assertion when enabled by M2VMT_CR[RPUEIE] of the M2MVT's interrupt output. Therefore these bits must be cleared by the interrupt handler. This is contrasted with the fields in the M2VMT_ESYNRn register, which are merely the 'syndrome' of an error indicated by the M2VMT_ESR.

For M2VMT, there is only one defined error status bit in the M2VMT_SER (actually two counting multi-error).

CSYSFPB_MST_CFPB_MASTER_M2VMT_ESR

Bits	Name	Description
31	MULTI	Multi-Error: When set to '1', indicates that an additional error occurred while M2VMT_ESR is non-zero. The M2VMT_EAR,M2VMT_ESYNRn and M2VMT_ESR registers (with the exception of this bit) lock on the first error, and must be cleared to unlock. Therefore, the status and the syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., syndrome register and status register stores details of only the first error.
30:1	RESERVED	
0	CFG	Configuration Port Error: When set to '1', indicates an error associated with a configuration port request. **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this register is treated as RAZ/WI.

0x18D01F8C CSYSFPB_MST_CFPB_MASTER_M2VMT_ESRRESTORE

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: unknown

CSYSFPB_MST_CFPB_MASTER_M2VMT_ESRRESTORE

Bits	Name	Description
31:0	M2VMT_ESRRTORE	M2VMT Error Status Register Restore This is just an aliased address for M2VMT_ESR, which provides direct write access (rather than write-clear) for restoration purpose **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this register is treated as RAZ/WI.

0x18D01F90 CSYSFPB_MST_CFPB_MASTER_M2VMT_ESYNR0

Type: Read
Clock: CC_CFPB_MASTER_CLK
Reset State: undefined

Error Syndrome Register 0:

Captures the syndrome on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) 'lock' upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., the syndrome register and the status register stores details of only the first error.

CSYSFPB_MST_CFPB_MASTER_M2VMT_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request.
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request.
15:0	AMID	AMID[15:0] field of errant request. Special Note: When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT="1", this register is not available and therefore access to this register is treated as RAZ/WI.

0x18D01F94 CSYSFPB_MST_CFPB_MASTER_M2VMT_ESYNR1

Type: Read
Clock: CC_CFPB_MASTER_CLK
Reset State: Undefined

Error Syndrome Register 1:

Captures syndrome upon M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) 'lock' upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., the syndrome register and the status register stores details of only the first error.

CSYSFPB_MST_CFPB_MASTER_M2VMT_ESYNR1

Bits	Name	Description
31	DCD	Decode: Indicates configuration port error due to invalid/ unrecognized/ unmapped/ un-implemented address (e.g., a reserved register address). Includes decode errors within the global address space. Also, note that decode error is never asserted for client port accesses.
30	AC	Access control: Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED_1	

CSYSFPB_MST_CFPB_MASTER_M2VMT_ESYNR1 (cont.)

Bits	Name	Description
24	AFULL	AFULL field of the errant request
23	AOOOWR	AOOOWR field of the errant request
22	AOOORD	AOOORD field of the errant request.
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request).
19	RESERVED_2	
18:16	ASIZE	ASIZE[2:0] field of the errant request).
15:12	ALEN	ALEN[3:0] field of the errant request.
11:10	ABURST	ABURST[1:0] field of the errant request.
9	RESERVED	
8	AWRITE	AWRITE field of the errant request.
7	AINST	AINST field of the errant request.
6	APROTNS	APROTNS field of the errant request.
5	APRIV	APRIV field of the errant request.
4	AINNERSHARED	AINNERSHARED field of the errant request.
3	ASHARED	ASHARED field of the errant request.
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

0x18D01FF4 CSYSFPB_MST_CFPB_MASTER_M2VMT_REV

Type: Read
Clock: CC_CFPB_MASTER_CLK
Reset State: 0x00000010

Reports the revision information for the M2VMT core and wrapper.

CSYSFPB_MST_CFPB_MASTER_M2VMT_REV

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	Major variant field. APQ8064: MAJOR = 0001.
3:0	MINOR	Minor variant field. MINOR = 0000

0x18D01FF8 CSYSFPB_MST_CFPB_MASTER_M2VMT_IDR

Type: Read
Clock: CC_CFPB_MASTER_CLK
Reset State: Undefined

Reports the size of the M2VMT table. It is a read-only register.

CSYSFPB_MST_CFPB_MASTER_M2VMT_IDR

Bits	Name	Description
31:9	RESERVED	
8:0	M2VMTSIZE	.M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping. M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

0x18D01FFC CSYSFPB_MST_CFPB_MASTER_M2VMT_RPU_ACR

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: Undefined

Using the incoming VMID, this register controls access to the global register space.

M2VMT (hcid index) registers (existing when VMIDMAPPER=1 and MASTER_IS_DM /= x"0000")

CSYSFPB_MST_CFPB_MASTER_M2VMT_RPU_ACR

Bits	Name	Description
31:0	RWE	M2VMT local RPU Access control Register. Each bit position corresponds to a VMID. When set to '1', that VMID is granted VMID read/write access to the entire block of registers within the M2VMT's 4KB global address space, including this register itself. In practice, this register designates the VMID(s) that can act as SROT (e.g., scorpion-secure) or pseudo SROT (e.g. RPM ARM11). Special Note: When REMOVE_M2VMT_RPU='1', this register is not available and therefore access to this register is treated as RAZ/WI.

0x18D02000+ 0x4*n CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_M2VMRn, n=[0..15]

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where n = NUM_M2VMT_ENTRIES from the design generics

CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_M2VMRn

Bits	Name	Description
31:5	RESERVED	
4:0	VMID	Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRn address associations. n = NUM_M2VMT_ENTRIES from the design generic/parameter.

0x18D02F80 CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_CR

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: xxx0

Global configuration register.

Note: When REMOVE_M2VMT_RPU = ’1’, this register is not available. Also, bit [2], is not valid or has no effect when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT =’1’.

CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_CR

Bits	Name	Description
31:4	RESERVED	
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., in valid addresses) are recorded as such. Decode error is asserted when config access to un-implemented and/or unmapped register/address are done. Also, note that decode error is never asserted for client port accesses. When value is set to ’0’ i.e., ’do not record’, decode errors do not set the M2VMT_ESR[CFG], and M2VMT_EAR & M2VMT_SYNRn is not updated. When value is set to ’1’, i.e., ’record’, decode errors set M2VMT_ESR[CFG] and M2VMT_EAR & M2VMT_SYNRn is updated with the address and the syndrome of the error. Reset State: x
2	RPUEIE	RPU error interrupt Enable: When set, configuration port errors are reported directly to the interrupt controller via the M2VMT_intr, interrupt output signal. Interrupt output is asserted if M2VMT_CR[RPUIE_EN] is ’1’ and ANY bit is set in the M2VMT_ESR register. Special Note: Not valid or has no effect on the interrupt when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT=’1’. Reset State: x
1	RPUERE	RPU error report enable: When set, M2VMT reports configuration port errors to the requesting bus master, according to the respective port’s bus protocol. All error types reported via CRIF port will use a decode error, rather than a slave error. Regardless of the value of this field, both configuration port errors are terminated by the M2VMT as RAZ/WI, and are recorded in M2VMT_ESR register. Reset State: X
0	RPUE	RPU Enable: Governs whether M2VMT_RPU_ACR is enabled to check the VMID of the configuration request. When set, all configuration port accesses are checked against M2VMT_RPU_ACR register for access permissions. It’s cleared by reset. Set once SROT configures MID->VMID mapping tables Reset State: 0

0x18D02F84 CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_EAR

Type: Read
Clock: CC_CFPB_MASTER_CLK
Reset State: unknown

When there is an error, this register holds the physical address of the errant transaction.

CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_EAR

Bits	Name	Description
31:0	PA	M2VMT Error Address Register: Physical address[31:0]. Contains the physical address of the errant request. Based on implementation, it may not contain the full 32 bits of the address. Captures the address on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. Special Note: When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT = '1', this register is not available and therefore access to this register are treated as RAZ/WI.

0x18D02F88 CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_ESR

Type: Read/Write to clear
Clock: CC_CFPB_MASTER_CLK
Reset State: Undefined

M2VMT Error Status Register:

Captures the status upon M2VMT configuration errors, as determined by the M2VMT_RPU_ACR.

This register has read/write-clear access, meaning that reads simply provide a value in the register, while writes are performed by clearing those bits corresponding to '1's in the value written data, and leaving unchanged those bits corresponding to 0s n the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old error. A write with a '1' set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

The presence of an asserted value on any bit in this register is what prompts the assertion when enabled by M2VMT_CR[RPUEIE] of the M2MVT's interrupt output. Therefore these bits must be cleared by the interrupt handler. This is contrasted with the fields in the M2VMT_ESYNRn register, which are merely the 'syndrome' of an error indicated by the M2VMT_ESR.

For M2VMT, there is only one defined error status bit in the M2VMT_SER (actually two counting multi-error).

CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_ESR

Bits	Name	Description
31	MULTI	Multi-Error: When set to '1', indicates that an additional error occurred while M2VMT_ESR is non-zero. The M2VMT_EAR,M2VMT_ESYNRn and M2VMT_ESR registers (with the exception of this bit) lock on the first error, and must be cleared to unlock. Therefore, the status and the syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., syndrome register and status register stores details of only the first error.
30:1	RESERVED	
0	CFG	Configuration Port Error: When set to '1', indicates an error associated with a configuration port request. **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this register is treated as RAZ/WI.

0x18D02F8C CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_ESRRESTORE

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: unknown

CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_ESRRESTORE

Bits	Name	Description
31:0	M2VMT_ESRRTORE	M2VMT Error Status Register Restore This is just an aliased address for M2VMT_ESR, which provides direct write access (rather than write-clear) for restoration purpose **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this register is treated as RAZ/WI.

0x18D02F90 CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_ESYNR0

Type: Read
Clock: CC_CFPB_MASTER_CLK
Reset State: undefined

Error Syndrome Register 0:

Captures the syndrome on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) ‘lock’ upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is ‘1’ are lost, i.e., the syndrome register and the status register stores details of only the first error.

CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request.
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request.
15:0	AMID	AMID[15:0] field of errant request. **NOTE** When REMOVE_M2VMT_RPU=’1’ OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT=”1”, this register is not available and therefore access to this register is treated as RAZ/WI.

0x18D02F94 CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_ESYNR1

Type: Read
Clock: CC_CFPB_MASTER_CLK
Reset State: Undefined

Error Syndrome Register 1:

Captures syndrome upon M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) ‘lock’ upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is ‘1’ are lost, i.e., the syndrome register and the status register stores details of only the first error.

CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_ESYNR1

Bits	Name	Description
31	DCD	Decode: Indicates configuration port error due to invalid/ unrecognized/ unmapped/ un-implemented address (e.g., a reserved register address). Includes decode errors within the global address space. Also, note that decode error is never asserted for client port accesses.
30	AC	Access control: Indicates configuration port error due to lack of permission, as specified by the access control registers

CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_ESYNR1 (cont.)

Bits	Name	Description
29:25	RESERVED_1	
24	AFULL	AFULL field of the errant request
23	AOOOWR	AOOOWR field of the errant request
22	AOOORD	AOOORD field of the errant request.
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request).
19	RESERVED_2	
18:16	ASIZE	ASIZE[2:0] field of the errant request).
15:12	ALEN	ALEN[3:0] field of the errant request.
11:10	ABURST	ABURST[1:0] field of the errant request.
9	RESERVED	
8	AWRITE	AWRITE field of the errant request.
7	AINST	AINST field of the errant request.
6	APROTNS	APROTNS field of the errant request.
5	APRIV	APRIV field of the errant request.
4	AINNERSHARED	AINNERSHARED field of the errant request.
3	ASHARED	ASHARED field of the errant request.
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

0x18D02FF4 CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_REV

Type: Read
Clock: CC_CFPB_MASTER_CLK
Reset State: 0x00000010

Reports the revision information for the M2VMT core and wrapper.

CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_REV

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	Major variant field. APQ8064: MAJOR = 0001.
3:0	MINOR	Minor variant field. MINOR = 0000

0x18D02FF8 CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_IDR

Type: Read
Clock: CC_CFPB_MASTER_CLK
Reset State: Undefined

Reports the size of the M2VMT table. It is a read-only register.

CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_IDR

Bits	Name	Description
31:9	RESERVED	
8:0	M2VMTSIZE	.M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping. M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

0x18D02FFC CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_RPU_ACR

Type: Read/Write
Clock: CC_CFPB_MASTER_CLK
Reset State: Undefined

Using the incoming VMID, this register controls access to the global register space.

CSYSFPB_MST_CFPB_MASTER_DM_M2VMT_RPU_ACR

Bits	Name	Description
31:0	RWE	M2VMT local RPU Access control Register. Each bit position corresponds to a VMID. When set to ’1’, that VMID is granted VMID read/write access to the entire block of registers within the M2VMT’s 4KB global address space, including this register itself. In practice, this register designates the VMID(s) that can act as SROT (e.g., scorpion-secure) or pseudo SROT (e.g. RPM ARM11). Special Note: When REMOVE_M2VMT_RPU=’1’, this register is not available and therefore access to this register is treated as RAZ/WI.

2.14 Chip System FPB1 XPU Registers (0x18E00000 CFPB1_XPU_CFG_BASE)

This section contains Chip System FPB 1 XPU registers.

0x18E00000+ 4*n CFPB1_XPU_APU_RGn_ACR, n=[0..14]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type APU. These registers include a single 5 bit "owner" VMID field.

CFPB1_XPU_APU_RGn_ACR

Bits	Name	Description
31:26	RESERVED31_26	Reserved.
25	RESERVED25	Reserved
24	RESERVED24	Reserved
23:21	RESERVED23_21	Reserved
20:16	RESERVED20_16	Reserved
15:10	RESERVED15_10	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | APU_APU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a "valid" bit for the RWVMID field
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies "owner" VMID with full read/write access to the registers in the associated resource group.

0x18E00F80 CFPB1_XPU_APU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

CFPB1_XPU_APU_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set APU_ESR. APU_EAR and APU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set APU_ESR. APU_EAR and APU_ESYNR0 updated with address and syndrome of error.
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x18E00F84 CFPB1_XPU_APU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port.

CFPB1_XPU_APU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x18E00F88 CFPB1_XPU_APU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the APU_ESYNRn registers, which are merely the "syndrome" of an error indicated by APU_ESR.

CFPB1_XPU_APU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x18E00F8C CFPB1_XPU_APU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

CFPB1_XPU_APU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x18E00F90 CFPB1_XPU_APU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

CFPB1_XPU_APU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x18E00F94 CFPB1_XPU_APU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

CFPB1_XPU_APU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x18E00FF4 CFPB1_XPU_APU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

CFPB1_XPU_APU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved

CFPB1_XPU_APU_REV (cont.)

Bits	Name	Description
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x18E00FF8 CFPB1_XPU_APU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x0000100E

APU ID Register: Read-only register that defines various configuration attributes of the APU instance.

CFPB1_XPU_APU_IDR

Bits	Name	Description
31:29	RESERVED31_21	Reserved
28:24	MSB	Indicates most significant address bit number used to select a resource group
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.

CFPB1_XPU_APU_IDR (cont.)

Bits	Name	Description
9	RESERVED9	Reserved
8:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

0x18E00FFC CFPB1_XPU_APU_APU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

APU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the APU (including the APU_APU_ACR itself).

CFPB1_XPU_APU_APU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the APU's 4KB address region (including the APU_APU_ACR itself). For single VMID type APUs (APU_IDR[MV] = 0) the APU_APU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

2.15 Chip System FPB1 Config Registers (0x18F00000 CSYSFPB1_BASE)

This section contains Chip System FPB 1 registers.

0x18F00000 CSYSFPB1_CFPB1_CTRL_STATUS

Type: Read/Write
Clock: CC_CFPB1_CLK
Reset State: 0x00000000

This register is a general configuration register.

CSYSFPB1_CFPB1_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables Power up value is clear (0)
11	RPM_PROC_IRQ_EN	SW: RW, HW: R PRMProcInterruptEnable When set, the RPM Processor receives an interrupt whenever ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	APPS_PROC_IRQ_EN	SW: RW, HW: R AppsProcInterruptEnable When set, the Application Processor receives an interrupt whenever ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

CSYSFPB1_CFPB1_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x5: Select the S0_M0 ahb2ahb bridge test bus. 0x6: Select the S1_M1 ahb2ahb bridge test bus. 0x7: Select the M0 ahb2ahb bridge test bus. 0x8: Select the M1 ahb2ahb bridge test bus. 0x9: Select the M2 ahb2ahb bridge test bus. 0xA: Select the M3 ahb2ahb bridge test bus. 0xB: Select the M4 ahb2ahb bridge test bus. 0xC: Select the M5 ahb2ahb bridge test bus. 0xD: Select the M6 ahb2ahb bridge test bus. 0xE: Select the M7 ahb2ahb bridge test bus. 0xF: Select the M8 ahb2ahb bridge test bus. 0x10: Select the M9 ahb2ahb bridge test bus. 0x11: Select the M10 ahb2ahb bridge test bus. 0x12: Select the M11 ahb2ahb bridge test bus. 0x13: Select the M12 ahb2ahb bridge test bus. 0x14: Select the M13 ahb2ahb bridge test bus. 0x15: Select the M14 ahb2ahb bridge test bus. 0x16: Select the M15 ahb2ahb bridge test bus.

0x18F00004+0x4*a CSYSFPB1_CFPB1_AHB2AHB_CFG_Ma, a=[0..0]

Type: Read/Write
Clock: CC_CFPB1_CLK
Reset State: 0x00000009

The CFPB1_AHB2AHB_CFG_Ma register is to configure the AHB2AHB bridge of master Ma. The AHB2AHB bridge is instantiated if the AHB interface is async (Generic: MASTER_ASYNC_IF(a) = ’1’). Otherwise this register is reserved.

CSYSFPB1_CFPB1_AHB2AHB_CFG_Ma

Bits	Name	Description
30:6	RESERVED_BITS30_6	

CSYSFPB1_CFPB1_AHB2AHB_CFG_Ma (cont.)

Bits	Name	Description
5:4	M_AHB2AHB_TEST_EN	SW: RW, HW: R Test enable for the Sa lite_bridge. Power up value is 00 0x0: DISABLED 0x1: Select slave side test signals 0x2: Select master side test signals 0x3: RESERVED_PROGRAMMING
3	M_WPOST_EN	SW: RW, HW: R MaWritePostEnable When set (1), the ahb2ahb bridge will support posting of write data. When cleared (0), each write request must complete across the bus before the next is accepted. Power up value is set (1)
2	M_HALT_ACK	SW:R, HW:W Indicates the Ma acknowledgement of halt_req asserted by software. Power up value is clear (0).
1	M_HALT_REQ	SW:RW, HW:R Software should write to this register to request the Ma lite_bridge master to cleanly halt. Power up value is clear (0).
0	M_IDLE	SW:R, HW:W Indicates that the Ma lite bridge master FSM is in IDLE state. Power up value is set (1).

0x18F00044 CSYSFPB1_CFPB1_PORT_EN

Type: Read/Write
Clock: CC_CFPB1_CLK
Reset State: 0xFFFFFFFF

This register is the CFPB1 master port enable register.

CSYSFPB1_CFPB1_PORT_EN

Bits	Name	Description
31:1	RESERVED_BIT31_1	Only one master port is used.
0	M0_PORT_EN	SW: RW, HW: R M0PortEnable When cleared (0), M0 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

0x18F00050 CSYSFPB1_CFPB1_ERROR_STAT

Type: Read/Write
Clock: CC_CFPB1_CLK
Reset State: 0x00000000

This register is the bus error status register.

CSYSFPB1_CFPB1_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the channel ID that caused the detected error when CID is valid for the master of the access. If not, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Master0 0x1: Master1 0x2: Master2 0x3: Master3 0x4: Master4 0x5: Master5 0x6: Master6 0x7: Master7 0x8: Master8 0x9: Master9 0xA: Master10 0xB: Master11 0xC: Master12 0xD: Master13 0xE: Master14 0xF: Master15
11:10	RESERVED_BITS11_10	

CSYSFPB1_CFPB1_ERROR_STAT (cont.)

Bits	Name	Description
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit
3:2	RESERVED_BIT3_2	
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted. Clearing (0) this bit clears any interrupts asserted as well as enables the ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x18F00054 CSYSFPB1_CFPB1_ERROR_ADDR

Type: Read
Clock: CC_CFPB1_CLK
Reset State: 0x00000000

This register contains the bus error address.

CSYSFPB1_CFPB1_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x18F00058 CSYSFPB1_CFPB1_GPREG

Type: Read/Write
Clock: CC_CFPB1_CLK
Reset State: 0x00000000

This register is a configurable general purpose register. This is 9-bit register. The size of this register is defined by the generic-SFPB_GPREG_SIZE (1 - 32 bits). It is set to 9.

CSYSFPB1_CFPB1_GPREG

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8:1	MSM_TIMEOUT_VAL	SW: RW, HW: W APQ will wait for time out value for ACK to receive from the Slave if MSM_TIMEOUT_VAL is programmed and if timeout is enabled. If ACK is not received within the timeout value, APQ will respond with Error. Power up value is clear (0)
0	MSM_TIMEOUT_EN	SW: RW, HW: W Enables the time out value if set to ’1’ Power up value is clear (0)

0x18F0005C CSYSFPB1_CFPB1_XPU_ACR

Type: Read/Write
Clock: CC_CFPB1_CLK
Reset State: 0xFFFFFFFF

The CFPB1_XPU_ACR register is a SFPB Access Control Register for configuring register protection.

CSYSFPB1_CFPB1_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R CFPB1 XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the CFPB1 configure space, including this register itself. Power up value is set (1)

0x18F00060 CSYSFPB1_CFPB1_HW_CLK_GATING_CFG

Type: Read/Write
Clock: CC_CFPB1_CLK
Reset State: 0x00000000

The CFPB1_HW_CLK_GATING_CFG register is for hardware clock gating configuration.

CSYSFPB1_CFPB1_HW_CLK_GATING_CFG

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	HYSTERESIS_CNT_SW	SW: RW, HW: R Hysteresis Counter Value This field is used by SW to set the hysteresis counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)
3:0	WAKE_CNT_SW	SW: RW, HW: R Wakeup Counter Value This field is used by SW to set the wakeup counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)

2.16 IMEM Configuration Registers (0x1A300000 PMEM_BASE)

The following subsections describe the IMEM registers.

0x1A300000 PMEM_IMEM_CONFIG

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00000001

General configuration register for IMEM. This register sets the IMEM accessibility for Graphics and AXI.

Power up value is based on parameters provided

NOTE

a. All banks are 2k x 64 in size.

b. GRP and AXI memory configurations are 64 bits wide.

c. If Graphics interface is not required, set the IMEM_CONFIG_POR parameter to all AXI setting (2'b01). The sharing scheme will then not apply.

PMEM_IMEM_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	IMEM_CONFIG	(Graphics Interface = 256kbytes) (AXI Interface (and trace) = 256kbytes) (Graphics Interface = 128kbytes) (AXI Interface (and trace) = 128kbytes) Banks 0 and 1 are allocated to Graphics. Banks 2 and 3 are allocated to AXI. (Graphics Interface = 128kbytes) (AXI Interface (and trace) = 128kbytes) Banks 0 and 1 are allocated to AXI. Banks 2 and 3 are allocated to Graphics. SW : RW, HW: R 0x0: All graphics (Dedicated all to Graphics) 0x1: All axi (Dedicated all to AXI) 0x2: 0_1_Graphics_2_3_AXI 0x3: 0_1_AXI_2_3_Graphics

2.16.1 IMEM AXI Trace Configuration registers

0x1A300004 PMEM_IMEM_AXI_TRACE_CONFIG

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00000000

This register is used to enable and control the AXI trace to IMEM.

PMEM_IMEM_AXI_TRACE_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	AXI_TRACE_ADDR_WRAP_EN	1-Enables AXI trace address to wrap
0	AXI_TRACE_EN	1-Enables AXI trace to IMEM

0x1A300008 PMEM_IMEM_AXI_TRACE_ADDR_CNTR

Type: Read
Clock: CORE_CLOCK
Reset State: 0x00000000

This register is used to read the AXI Trace Address counter value.

PMEM_IMEM_AXI_TRACE_ADDR_CNTR

Bits	Name	Description
31:16	RESERVED_BITS31_16	
15:0	AXI_TRACE_ADDR_CNTR	Current AXI Trace address

0x1A30000C PMEM_IMEM_AXI_TRACE_WRAP_STATUS

Type: Read
Clock: CORE_CLOCK
Reset State: 0x00000000

This register is used to read the AXI Trace Address wrap status bit.

PMEM_IMEM_AXI_TRACE_WRAP_STATUS

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	AXI_TRACE_WRAP_STATUS	0x1: AXI trace address wrapped 0x0: AXI trace address not wrapped

0x1A300010 PMEM_IMEM_AXI_BASE_ADDR_OFFSET

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00001280

This register is used to set the AXI Base Address offset value in order to relocate the IMEM AXI memory within the space allowed by the interconnect. The POR value of this register is based on the parameter - IMEM_BASE_ADDRESS. In case of MPSS, this is set to 0x5800. This should be set to the upper 16 bits of the Imem base address. Based on the size of the Imem, the relevant bits of this register are used for decoding the address.

PMEM_IMEM_AXI_BASE_ADDR_OFFSET

Bits	Name	Description
31:16	RESERVED_BITS31_16	
15:0	IMEM_AXI_BASE_ADDRESS_OFFSET	IMEM AXI base address offset for decode

2.16.2 IMEM Syndrome registers

0x1A300020 PMEM_IMEM_ERR_ADDRESS_MS

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x000000000000

The IMEM_ERR_ADDRESS_MS register contains the upper bits of the address of the request that caused the bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, it will be locked until bit 8 of the ERR_CODE register is written to clear the error.

PMEM_IMEM_ERR_ADDRESS_MS

Bits	Name	Description
31:16	RESERVED_BITS31_16	

PMEM_IMEM_ERR_ADDRESS_MS (cont.)

Bits	Name	Description
15:0	ERROR_ADDRESS_31_16	Bits 31:16 of the address of the request that caused the bus error.

0x1A300024 PMEM_IMEM_ERR_ADDRESS_LS

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x00000000

The IMEM_ERR_ADDRESS_LS register contains the lower bits of the address of the request that caused the AXI GE bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, the register will be locked until bit 8 of the ERR_CODE register is written to clear the error.

PMEM_IMEM_ERR_ADDRESS_LS

Bits	Name	Description
31:16	RESERVED_BITS31_16	
15:3	ERROR_ADDRESS_15_3	Bits 15:3 of the address of the request that caused the bus error
2:0	RESERVED_BITS2_0	Reserved if not implemented otherwise include with error address.

0x1A300028 PMEM_IMEM_ERR_APACKET_MS

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x00000000

The IMEM_ERR_APACKET_MS register provides various data about the request that caused the AXI GE bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, it will be locked until bit 8 of the ERR_CODE register is written to clear the error.

PMEM_IMEM_ERR_APACKET_MS

Bits	Name	Description
31:20	RESERVED_BITS31_20	
19:18	ERROR_ALOCK_1_0	The ALOCK of the request that caused the bus error
17	ERROR_ABURST	The ABURST of the request that caused the bus error
16:12	ERROR_PORTID_4_0	The Port ID of the request that caused the bus error.
11:5	ERROR_ATID_6_0	The Transfer ID of the request that caused the bus error.

PMEM_IMEM_ERR_APACKET_MS (cont.)

Bits	Name	Description
4	ERROR_AWRITE	The awrite of the request that caused bus error
3:0	ERROR_ALEN	The burst length of the request that caused bus error

0x1A30002C PMEM_IMEM_ERR_APACKET_LS

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x00000000

The IMEM_ERR_APACKET_LS register provides various data about the request that caused the AXI GE bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, the register will be locked until bit 8 of the ERR_CODE register is written to clear the error.

PMEM_IMEM_ERR_APACKET_LS

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:9	ERROR_AMID_15_0	The master ID of the request that caused the bus error (The higher order bits will be set to 0 for MID width < 7)
8:5	ERROR_ATYPE_3_0	The ATYPE of the request that caused the bus error
4	ERROR_APROTNS	The APROTNS of the request that caused the bus error
3:0	RESERVED_BITS_3_0	

0x1A300030 PMEM_IMEM_ERR_CODE

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00000000

The IMEM_ERR_CODE register provides additional data about the bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, the register will be locked until bit 8 of the ERR_CODE register is written to clear the error.

Additionally, each slave or AXI interconnect that is capable of detecting an error is also required to have a single programmable register that can be used to optionally interrupt the ARM9 or Scorpion Processor core. This interrupt mechanism is required since write transfers may be posted on the bus and the AXI transfer may complete prior to the occurrence of the error in the AXI interconnect or slave device. The interrupt from the AXI interconnect and the AXI slave devices will be directed to both the modem and application processor's interrupt controllers. The interrupt output of the slave device shall be driven from bit 3 of the ERR_CODE register above. To clear the interrupt, it will be necessary to clear the ERR_CODE register by writing to bit 8

(ERROR_CLEAR) of the ERR_CODE register. This will clear the ERROR field (bit 3) and also unlock the ERR_ADDRESS, ERR_APACKET, and ERR_CODE registers so that a subsequent error can be recoded in these registers.

PMEM_IMEM_ERR_CODE

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8	ERROR_CLEAR	Writing a ’1’ to this bit will clear the bus error status bit.
7:4	RESERVED_BIT7_4	
3	ERROR	Error Status bit to indicate that an error has occurred.
2	RESERVED_BIT2	
1	MPU_ERROR	0x1: memory protection error
0	ADDRESS_DECODE_ERRO R	0x1: slave address decode error

0x1A300034 PMEM_IMEM_ERR_IRQ_MSK

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00000001

This register is used to block interrupt to ARM9 or Scorpion.

PMEM_IMEM_ERR_IRQ_MSK

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	PROCESSOR_IRQ_MASK	1 disables bus error interrupt to Processor

0x1A300040 PMEM_IMEM_CLK_ON_EN

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x00000000

This register is used to enable/disable the clock_on circuitry. If disabled, clock on is always high.

PMEM_IMEM_CLK_ON_EN

Bits	Name	Description
31:1	RESERVED_BITS31_1	

PMEM_IMEM_CLK_ON_EN (cont.)

Bits	Name	Description
0	CLK_ON_TIME	1 will enable the timer countdown

0x1A300044 PMEM_IMEM_CLK_ON_TIME

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x000003FF

This register sets the starting time for a binary countdown in clock cycles.

PMEM_IMEM_CLK_ON_TIME

Bits	Name	Description
31:10	RESERVED_BITS31_1	
9:0	CLK_ON_TIME_9_0	10 bits to count down from, for a max of 1024

0x1A300048 PMEM_IMEM_FSCGC_TIMERS

Type: Read Only
Clock: BUS_CLOCK
Reset State: 0x00000000

This register sets the starting time for a binary countdown in clock cycles.

PMEM_IMEM_FSCGC_TIMERS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	WAKEUP_COUNTER_3_0	4 bit count down, must be 20ns
3:0	TO_SLEEP_COUNTER_3_0	4 bit count down, must be 20ns

0x1A30004C PMEM_IMEM_FSCGC_CONTROL

Type: Read Only
Clock: BUS_CLOCK
Reset State: 0x00000000

Controls for head switch and perifery within IMEM.

PMEM_IMEM_FSCGC_CONTROL

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	HALT_CLOCK_23_16	Gates the clock to individual RAMS
15:8	CORE_ON_15_8	RAM Core will remain on if this is 1 (for individual rams)
7:0	PERIF_ON_7_0	RAM Perifery will remain on if this is 1 (for individual rams)

0x1A300050 PMEM_IMEM_EX_FSCGC_CONTROL

Type: Read Only
Clock: BUS_CLOCK
Reset State: 0x00000000

Controls for head switch and perifery outside of IMEM.

PMEM_IMEM_EX_FSCGC_CONTROL

Bits	Name	Description
31:22	RESERVED_BITS31_24	
23:16	HALT_CLOCK_7_0	Gates the clock to individual RAMS
15:8	CORE_ON_7_0	RAM Core will remain on if this is 1 (for individual rams)
7:0	PERIF_ON_7_0	RAM Perifery will remain on if this is 1 (for individual rams)

0x1A300054 PMEM_IMEM_RAM_CONFIG

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x00000000

This register configures the access to the external ram interface.

PMEM_IMEM_RAM_CONFIG

Bits	Name	Description
31:3	RESERVED_BITS31_3	
1:0	EX_RAM_CONFIG_1_0	External ram access configuration: 11; NO external ram allocated to AXI 0x0: No External ram allocated to AXI 0x1: 256K of external ram allocated to AXI 0x2: All external ram allocated to AXI

2.16.3 Internal Memory misc. registers

0x1A300038 PMEM_IMEM_MEM_ACC_CFG

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x00000000

This register is used to configure the acc pins of the RAM for programming the sense amp. This is not supported for APQ8064.

PMEM_IMEM_MEM_ACC_CFG

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	ACC_CFG	

2.16.4 XPU Registers

0x1A301000+ 4*n PMEM_MPU_PRTn_ACR, n=[0..15]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when MPU_IDR[MV, PT] = 10, i.e, a multi-VMID full access vs. no access permission type MPU. These registers include a single bit per VMID granting full access.

PMEM_MPU_PRTn_ACR

Bits	Name	Description
31:0	RWE	Read/Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the registers in the associated resource group.

0x1A301800+ 4*n PMEM_MPU_PRTn_START, n=[0..15]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition Start Address Register. This register contains the start address of the partition. Only the bit numbers indicated by MPU_IDR[MSb] through MPU_IDR[LSb] are valid and physically exist.

PMEM_MPU_PRTn_START

Bits	Name	Description
31:16	RESERVED_31_16	Reserved
15:7	ADDR	MPU Partition Start Address
6:0	RESERVED_6_0	Reserved

0x1A301C00+4*n PMEM_MPU_PRTn_END, n=[0..15]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition End Address Register. This register contains the start address of the partition.Only the bit numbers indicated by MPU_IDR[MSB] through MPU_IDR[LSB] are valid and physically exist.

PMEM_MPU_PRTn_END

Bits	Name	Description
31:16	RESERVED_311629	Reserved
15:7	ADDR	MPU Partition End Address
6:0	RESERVED_6_0	Reserved

0x1A301F80 PMEM_MPU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Configuration Register: This register includes fields governing various MPU behaviors.

PMEM_MPU_CR

Bits	Name	Description
31:2	RESERVED31_2	Reserved

PMEM_MPU_CR (cont.)

Bits	Name	Description
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set MPU_ESR. MPU_EAR and MPU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set MPU_ESR. MPU_EAR and MPU_ESYNR0 updated with address and syndrome of error.
2	MPUEIE	MPU Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the MPU. Interrupt output is asserted if MPU_CR[MPUEIE] = 1 and any bit is set in MPU_ESR.
1	MPUERE	MPU Error Report Enable. MPUERE = 0 causes the MPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master. MPUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective MPU port. Errors from either port are terminated by the MPU as RAZ/WI Both client and configuration port errors are recorded in MPU_ESR, independent of the value of MPU_CR[MPUERE]
0	MPUE	MPU Enable. Governs whether MPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures MPU and the MID to VMID mapping tables.

0x1A301F84 PMEM_MPU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the MPU, for both the client port and the configuration port.

PMEM_MPU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x1A301F88 PMEM_MPU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the MPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the MPU's interrupt output (when enabled by MPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the MPU_ESYNRn registers, which are merely the 'syndrome' of an error indicated by MPU_ESR.

PMEM_MPU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) 'lock' upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x1A301F8C PMEM_MPU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Restore Register. This register is an aliased address for the MPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

PMEM_MPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) 'lock' upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved

PMEM_MPU_ESRRESTORE (cont.)

Bits	Name	Description
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x1A301F90 PMEM_MPU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

PMEM_MPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x1A301F94 PMEM_MPU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

PMEM_MPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.

PMEM_MPU_ESYNR1 (cont.)

Bits	Name	Description
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x1A301FF4 PMEM_MPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

MPU Revision Register: This register provides major/minor revision codes for the implementation.

PMEM_MPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x1A301FF8 PMEM_MPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x0F07240F

MPU ID Register: Read-only register that defines various configuration attributes of the MPU instance.

PMEM_MPU_IDR

Bits	Name	Description
31:29	RESERVED31_29	Reserved
28:24	MSB	Indicates most significant address bit number used in START/END address comparisons.
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used in START/END address comparisons.
15:14	RESERVED15_12	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only MPU_PRTn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate MPU_PRTn_RACR and MPU_PRTn_WACR registers govern read vs. write access. For single VMID, MPU_PRTn_ACR registers include separate 5-bit read/write vs. read-only 'owner' VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. MPU_PRTn_ACR registers indicate single 5 bit 'owner' VMID field for governing access. MV=1 : indicates multi-VMD type access control. MPU_PRTn_xACR registers include separate bit per VMID (32 bits) for governing access.
9:8	RESERVED9_8	Reserved
7:0	NPRT	Number of partitions. Indicates the number of partitions (minus 1) supported by the MPU. Values range from 0-223 (1-224 partitions)

0x1A301FFC PMEM_MPU_MPU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

MPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the MPU (including the MPU_MPU_ACR itself).

PMEM_MPU_MPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the MPU's 4KB address region (including the MPU_MPU_ACR itself). For single VMID type MPUs (MPU_IDR[MV] = 0) the MPU_MPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

2.17 TCSR Registers (0x1A400000 MSM_TCSR_BASE)

This section contains the TCSR registers.

The registers in this section exist in the core_top_csr, which is instantiated in the core_top.

0x1A400000 TCSR_PRNG_RING_OSC_DSBL

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

No longer in use as functionality removed due to security risks.

Can be used as a 4-bit spare register, if needed.

TCSR_PRNG_RING_OSC_DSBL

Bits	Name	Description
31:4	RESERVED_31_4	
3	PRNG_RING_OSC_3_DSBL_CFG	Was controls PRNG input prng_ring_osc_3_dsbl
2	PRNG_RING_OSC_2_DSBL_CFG	Was controls PRNG input prng_ring_osc_2_dsbl
1	PRNG_RING_OSC_1_DSBL_CFG	Was controls PRNG input prng_ring_osc_1_dsbl
0	PRNG_RING_OSC_0_DSBL_CFG	Was controls PRNG input prng_ring_osc_0_dsbl

0x1A400004 TCSR_SPDM_DIAG_SW_MON_0

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register is a SW programmable bit used as inputs to either the sample or filter counters in SPDM.

TCSR_SPDM_DIAG_SW_MON_0

Bits	Name	Description
31:1	RESERVED_31_1	

TCSR_SPDM_DIAG_SW_MON_0 (cont.)

Bits	Name	Description
0	SW_BIT	SW programmable bit for off-line event counting 0x0: clear 0x1: set

0x1A400008 TCSR_SPDM_DIAG_SW_MON_1

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register is a SW programmable bit used as inputs to either the sample or filter counters in SPDM.

TCSR_SPDM_DIAG_SW_MON_1

Bits	Name	Description
31:1	RESERVED_31_1	
0	SW_BIT	SW programmable bit for off-line event counting 0x0: clear 0x1: set

0x1A40000C TCSR_SPDM_DIAG_SW_MON_2

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register is a SW programmable bit used as inputs to either the sample or filter counters in SPDM.

TCSR_SPDM_DIAG_SW_MON_2

Bits	Name	Description
31:1	RESERVED_31_1	
0	SW_BIT	SW programmable bit for off-line event counting 0x0: clear 0x1: set

0x1A400010 TCSR_SPDM_DIAG_SW_MON_3

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register was a SW programmable bit used as inputs to either the sample or filter counters in SPDM.

Not in use for APQ8064 since the SPDM port connected is connected to the 2nd LPDDR controller.

Can be used as a 1-bit spare register, if needed.

TCSR_SPDM_DIAG_SW_MON_3

Bits	Name	Description
31:1	RESERVED_31_1	
0	SW_BIT	SW programmable bit for off-line event counting 0x0: clear 0x1: set

0x1A400014 TCSR_SPDM_DLY_FIFO_EN

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

Enables delay FIFO for each offline 4bit port input. Delay FIFOs are used to transfer offline data between the source and the SPDM core pseudo-synchronously.

TCSR_SPDM_DLY_FIFO_EN

Bits	Name	Description
31:0	SPDM_DLY_FIFO_EN	Bit[0] corresponds to delay for FIFO used for offline port 0 0x0: Disable 0x1: Enable

0x1A400018 TCSR_SPDM_STG1_MUX_SEL

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

Mux selects for stage 1 MUXes to select 8 primary ports to monitor 32 offline ports. Each stage 1 MUX is 2-bits wide and selects 1 of 4 offline ports.

TCSR_SPDM_STG1_MUX_SEL

Bits	Name	Description
31:16	RESERVED_31_16	
15:14	SPDM_STG1_MUX_SEL7	Selects between Port 19, Port 23, Port 27, Port 31 to create Primary Port 7
13:12	SPDM_STG1_MUX_SEL6	Selects between Port 18, Port 22, Port 26, Port 30 to create Primary Port 6
11:10	SPDM_STG1_MUX_SEL5	Selects between Port 17, Port 21, Port 25, Port 29 to create Primary Port 5
9:8	SPDM_STG1_MUX_SEL4	Selects between Port 16, Port 20, Port 24, Port 28 to create Primary Port 4
7:6	SPDM_STG1_MUX_SEL3	Selects between Port 3, Port 7, Port 11, Port 15 to create Primary Port 3
5:4	SPDM_STG1_MUX_SEL2	Selects between Port 2, Port 6, Port 10, Port 14 to create Primary Port 2
3:2	SPDM_STG1_MUX_SEL1	Selects between Port 1, Port 5, Port 9, Port 13 to create Primary Port 1
1:0	SPDM_STG1_MUX_SEL0	Selects between Port 0, Port 4, Port 8, Port 12 to create Primary Port 0

0x1A40001C TCSR_SPDM_STG2_A_MUX_SEL

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

Mux selects for stage 2 MUXes to select one of 4 primary ports (selected in stage 1 MUX) for monitoring in an offline monitor. There is one MUX per offline monitor and each stage 2 MUX select is 2-bits wide.

TCSR_SPDM_STG2_A_MUX_SEL

Bits	Name	Description
31:30	SPDM_STG2_A_MUX_SEL15	Selects between Primary Ports 0- 3 for monitoring in offline monitor 15
29:28	SPDM_STG2_A_MUX_SEL14	Selects between Primary Ports 0- 3 for monitoring in offline monitor 14
27:26	SPDM_STG2_A_MUX_SEL13	Selects between Primary Ports 0- 3 for monitoring in offline monitor 13
25:24	SPDM_STG2_A_MUX_SEL12	Selects between Primary Ports 0- 3 for monitoring in offline monitor 12

TCSR_SPDM_STG2_A_MUX_SEL (cont.)

Bits	Name	Description
23:22	SPDM_STG2_A_MUX_SEL11	Selects between Primary Ports 0- 3 for monitoring in offline monitor 11
21:20	SPDM_STG2_A_MUX_SEL10	Selects between Primary Ports 0- 3 for monitoring in offline monitor 10
19:18	SPDM_STG2_A_MUX_SEL9	Selects between Primary Ports 0- 3 for monitoring in offline monitor 9
17:16	SPDM_STG2_A_MUX_SEL8	Selects between Primary Ports 0- 3 for monitoring in offline monitor 8
15:14	SPDM_STG2_A_MUX_SEL7	Selects between Primary Ports 0- 3 for monitoring in offline monitor 7
13:12	SPDM_STG2_A_MUX_SEL6	Selects between Primary Ports 0- 3 for monitoring in offline monitor 6
11:10	SPDM_STG2_A_MUX_SEL5	Selects between Primary Ports 0- 3 for monitoring in offline monitor 5
9:8	SPDM_STG2_A_MUX_SEL4	Selects between Primary Ports 0- 3 for monitoring in offline monitor 4
7:6	SPDM_STG2_A_MUX_SEL3	Selects between Primary Ports 0- 3 for monitoring in offline monitor 3
5:4	SPDM_STG2_A_MUX_SEL2	Selects between Primary Ports 0- 3 for monitoring in offline monitor 2
3:2	SPDM_STG2_A_MUX_SEL1	Selects between Primary Ports 0- 3 for monitoring in offline monitor 1
1:0	SPDM_STG2_A_MUX_SEL0	Selects between Primary Ports 0- 3 for monitoring in offline monitor 0

0x1A400020 TCSR_SPDM_STG2_B_MUX_SEL

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

Mux selects for stage 2 MUXes to select one of 4 primary ports (selected in stage 1 MUX) for monitoring in an offline monitor. There is one MUX per offline monitor and each stage 2 MUX select is 2-bits wide.

TCSR_SPDM_STG2_B_MUX_SEL

Bits	Name	Description
31:30	SPDM_STG2_B_MUX_SEL31	Selects between Primary Ports 4- 7 for monitoring in offline monitor 31

TCSR_SPDM_STG2_B_MUX_SEL (cont.)

Bits	Name	Description
29:28	SPDM_STG2_B_MUX_SEL30	Selects between Primary Ports 4- 7 for monitoring in offline monitor 30
27:26	SPDM_STG2_B_MUX_SEL29	Selects between Primary Ports 4- 7 for monitoring in offline monitor 29
25:24	SPDM_STG2_B_MUX_SEL28	Selects between Primary Ports 4- 7 for monitoring in offline monitor 28
23:22	SPDM_STG2_B_MUX_SEL27	Selects between Primary Ports 4- 7 for monitoring in offline monitor 27
21:20	SPDM_STG2_B_MUX_SEL26	Selects between Primary Ports 4- 7 for monitoring in offline monitor 26
19:18	SPDM_STG2_B_MUX_SEL25	Selects between Primary Ports 4- 7 for monitoring in offline monitor 25
17:16	SPDM_STG2_B_MUX_SEL24	Selects between Primary Ports 4- 7 for monitoring in offline monitor 24
15:14	SPDM_STG2_B_MUX_SEL23	Selects between Primary Ports 4- 7 for monitoring in offline monitor 23
13:12	SPDM_STG2_B_MUX_SEL22	Selects between Primary Ports 4- 7 for monitoring in offline monitor 22
11:10	SPDM_STG2_B_MUX_SEL21	Selects between Primary Ports 4- 7 for monitoring in offline monitor 21
9:8	SPDM_STG2_B_MUX_SEL20	Selects between Primary Ports 4- 7 for monitoring in offline monitor 20
7:6	SPDM_STG2_B_MUX_SEL19	Selects between Primary Ports 4- 7 for monitoring in offline monitor 19
5:4	SPDM_STG2_B_MUX_SEL18	Selects between Primary Ports 4- 7 for monitoring in offline monitor 18
3:2	SPDM_STG2_B_MUX_SEL17	Selects between Primary Ports 4- 7 for monitoring in offline monitor 17
1:0	SPDM_STG2_B_MUX_SEL16	Selects between Primary Ports 4- 7 for monitoring in offline monitor 16

0x1A400024 TCSR_SPDM_STG3_A_MUX_SEL

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

Mux selects for stage 3 multiplexors to select one bit from each port (selected in stage 2 MUX) for monitoring in an offline monitor. There is one MUX per offline monitor and each stage 3 MUX select is 2-bits wide.

TCSR_SPDM_STG3_A_MUX_SEL

Bits	Name	Description
31:30	SPDM_STG3_A_MUX_SEL15	Selects one of 4-bits from Stage 2 Mux 15 for monitoring in offline monitor 15
29:28	SPDM_STG3_A_MUX_SEL14	Selects one of 4-bits from Stage 2 Mux 14 for monitoring in offline monitor 14
27:26	SPDM_STG3_A_MUX_SEL13	Selects one of 4-bits from Stage 2 Mux 13 for monitoring in offline monitor 13
25:24	SPDM_STG3_A_MUX_SEL12	Selects one of 4-bits from Stage 2 Mux 12 for monitoring in offline monitor 12
23:22	SPDM_STG3_A_MUX_SEL11	Selects one of 4-bits from Stage 2 Mux 11 for monitoring in offline monitor 11
21:20	SPDM_STG3_A_MUX_SEL10	Selects one of 4-bits from Stage 2 Mux 10 for monitoring in offline monitor 10
19:18	SPDM_STG3_A_MUX_SEL9	Selects one of 4-bits from Stage 2 Mux 9 for monitoring in offline monitor 9
17:16	SPDM_STG3_A_MUX_SEL8	Selects one of 4-bits from Stage 2 Mux 8 for monitoring in offline monitor 8
15:14	SPDM_STG3_A_MUX_SEL7	Selects one of 4-bits from Stage 2 Mux 7 for monitoring in offline monitor 7
13:12	SPDM_STG3_A_MUX_SEL6	Selects one of 4-bits from Stage 2 Mux 6 for monitoring in offline monitor 6
11:10	SPDM_STG3_A_MUX_SEL5	Selects one of 4-bits from Stage 2 Mux 5 for monitoring in offline monitor 5
9:8	SPDM_STG3_A_MUX_SEL4	Selects one of 4-bits from Stage 2 Mux 4 for monitoring in offline monitor 4
7:6	SPDM_STG3_A_MUX_SEL3	Selects one of 4-bits from Stage 2 Mux 3 for monitoring in offline monitor 3
5:4	SPDM_STG3_A_MUX_SEL2	Selects one of 4-bits from Stage 2 Mux 2 for monitoring in offline monitor 2
3:2	SPDM_STG3_A_MUX_SEL1	Selects one of 4-bits from Stage 2 Mux 1 for monitoring in offline monitor 1
1:0	SPDM_STG3_A_MUX_SEL0	Selects one of 4-bits from Stage 2 Mux 0 for monitoring in offline monitor 0

0x1A40002C TCSR_SPDM_STG3_B_MUX_SEL

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

Mux selects for stage 3 multiplexors to select one bit from each port (selected in stage 2 MUX) for monitoring in an offline monitor. There is one MUX per offline monitor and each stage 3 MUX select is 2-bits wide.

TCSR_SPDM_STG3_B_MUX_SEL

Bits	Name	Description
31:30	SPDM_STG3_B_MUX_SEL31	Selects one of 4-bits from Stage 2 Mux 31 for monitoring in offline monitor 31
29:28	SPDM_STG3_B_MUX_SEL30	Selects one of 4-bits from Stage 2 Mux 30 for monitoring in offline monitor 30
27:26	SPDM_STG3_B_MUX_SEL29	Selects one of 4-bits from Stage 2 Mux 29 for monitoring in offline monitor 29
25:24	SPDM_STG3_B_MUX_SEL28	Selects one of 4-bits from Stage 2 Mux 28 for monitoring in offline monitor 28
23:22	SPDM_STG3_B_MUX_SEL27	Selects one of 4-bits from Stage 2 Mux 27 for monitoring in offline monitor 27
21:20	SPDM_STG3_B_MUX_SEL26	Selects one of 4-bits from Stage 2 Mux 26 for monitoring in offline monitor 26
19:18	SPDM_STG3_B_MUX_SEL25	Selects one of 4-bits from Stage 2 Mux 25 for monitoring in offline monitor 25
17:16	SPDM_STG3_B_MUX_SEL24	Selects one of 4-bits from Stage 2 Mux 24 for monitoring in offline monitor 24
15:14	SPDM_STG3_B_MUX_SEL23	Selects one of 4-bits from Stage 2 Mux 23 for monitoring in offline monitor 23
13:12	SPDM_STG3_B_MUX_SEL22	Selects one of 4-bits from Stage 2 Mux 22 for monitoring in offline monitor 22
11:10	SPDM_STG3_B_MUX_SEL21	Selects one of 4-bits from Stage 2 Mux 21 for monitoring in offline monitor 21
9:8	SPDM_STG3_B_MUX_SEL20	Selects one of 4-bits from Stage 2 Mux 20 for monitoring in offline monitor 20
7:6	SPDM_STG3_B_MUX_SEL19	Selects one of 4-bits from Stage 2 Mux 19 for monitoring in offline monitor 19
5:4	SPDM_STG3_B_MUX_SEL18	Selects one of 4-bits from Stage 2 Mux 18 for monitoring in offline monitor 18
3:2	SPDM_STG3_B_MUX_SEL17	Selects one of 4-bits from Stage 2 Mux 17 for monitoring in offline monitor 17
1:0	SPDM_STG3_B_MUX_SEL16	Selects one of 4-bits from Stage 2 Mux 16 for monitoring in offline monitor 16

0x1A400030 TCSR_SMPSS_WDOG_CFG

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register was used to enable or disable the KPSS watch-dog timer output.

In APQ8064, it is no longer in use due to security concerns.

Can be used as a spare register, if needed.

TCSR_SMPSS_WDOG_CFG

Bits	Name	Description
31:8	RESERVED_31_8	
7	SCSS_WDT1CPU3BITEEXPIRED	Used to enable/disable the SMPSS watch dog timer output. 0x0: Disable 0x1: Enable
6	SCSS_WDT1CPU2BITEEXPIRED	Used to enable/disable the SMPSS watch dog timer output. 0x0: Disable 0x1: Enable
5	SCSS_WDT0CPU3BITEEXPIRED	Used to enable/disable the SMPSS watch dog timer output. 0x0: Disable 0x1: Enable
4	SCSS_WDT0CPU2BITEEXPIRED	Used to enable/disable the SMPSS watch dog timer output. 0x0: Disable 0x1: Enable
3	SCSS_WDT1CPU1BITEEXPIRED	Used to enable/disable the SMPSS watch dog timer output. 0x0: Disable 0x1: Enable
2	SCSS_WDT1CPU0BITEEXPIRED	Used to enable/disable the SMPSS watch dog timer output. 0x0: Disable 0x1: Enable
1	SCSS_WDT0CPU1BITEEXPIRED	Used to enable/disable the SMPSS watch dog timer output. 0x0: Disable 0x1: Enable
0	SCSS_WDT0CPU0BITEEXPIRED	Used to enable/disable the SMPSS watch dog timer output. 0x0: Disable 0x1: Enable

0x1A400034 TCSR_VTG_SENSOR_STATUS

Type: Read
Clock: AXI_CLOCK
Reset State: 0x00000000

No longer in use as there is no Voltage Sensor on this device.

Can be used as a spare register, if needed.

TCSR_VTG_SENSOR_STATUS

Bits	Name	Description
31:16	STATUS_DATA	Status data from voltage sensor.
17	STATUS_MIN_MAX_ALARM	MIN-MAX alarm bit (exported to the I/O)
16	STATUS_MIN_ALARM	Minimum threshold exceeded
15	STATUS_MAX_ALARM	Maximum threshold exceeded
14:8	STATUS_MIN_VALUE	Minimum value reached
7:1	STATUS_MAX_VALUE	Maximum value reached
0	STATUS_DATA_VALID	When set as 1 by voltage sensor core, the core_top_csr latches the status data from voltage sensor in this register,

0x1A40003C TCSR_VTG_SENSOR_CONFIG

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

No longer in use as there is no Voltage Sensor on this device.

Can be used as a spare register, if needed.

TCSR_VTG_SENSOR_CONFIG

Bits	Name	Description
31:29	CONFIG_DATA	Config data for voltage sensor.
28	CONFIG_DBG_BUS_EN	Debug bus enable - gates on/off debug bus outputs (off to 0)
27	CONFIG_MODE_OPERATION	Mode of operation: serial or parallel (priority encoded 3-bit)
26:20	CONFIG_MIN_MONITOR_THRESH	Minimum monitor threshold
19:13	CONFIG_MAX_MONITOR_THRESH	Maximum monitor threshold

TCSR_VTG_SENSOR_CONFIG (cont.)

Bits	Name	Description
12:10	CONFIG_PRI_ENC_MUX_SELECT	Priority encoder MUX select (for serial mode coarse delay select)
9:6	CONFIG_FINE_DLY_LINE_SEL	Fine delay line select
5	CONFIG_DLY_LINE_DLY_DEL	Range Adjustment: Delay line delay select
4	CONFIG_PROBE_DLY_SEL	Range Adjustment: Probe delay select
3:2	CONFIG_FREQ_DIV_CTL	Frequency divider Control Register
1	DATA_REQUEST	When set as 1 by system CPU in the core_top_csr, it indicates to the voltage sensor core that valid value for config register is available from system CPU.
0	MACRO_ENABLE	When set as 1 by system CPU in the core_top_csr, it activates the voltage sensor core.

0x1A400040 TCSR_RPM_VMID_NS_CTL

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

This register is disabled by default via a FUSE - so any write to this register will not take effect. when the FUSE is blown, the functionality described below will be in effect.

For all requests presented to AHB slave port input to SMPSS, if the incoming fabric VMID matches TCSR_RPM_VMID_NS_CTL[VMID], then drive HPROTNS into SMPSS according to NSCFG as below. If the VMID does NOT match, then drive HPROTNS into SMPSS using the value supplied by the fabric AHB slave port

TCSR_RPM_VMID_NS_CTL

Bits	Name	Description
31:24	RESERVED_31_24	
23:22	NSCFG	Encoding: 0x0: pass-through HPROTNS 0x1: reserved 0x2: HPROTNS forced to 0 0x3: HPROTNS forced to 1
21:5	RESERVED_21_5	
4:0	VMID	Used to compare with incoming fabric VMID.

0x1A400044 TCSR_GSBI_IRQ_MUX_SEL_0

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register is used to select between the GSBI IRQs to output o_top_gsbi_irq_0.

TCSR_GSBI_IRQ_MUX_SEL_0

Bits	Name	Description
31:3	RESERVED_31_3	
2:0	GSBI_IRQ_MUX_SEL	Selects the GSBI IRQ corresponding to value in register

0x1A400050 TCSR_FAB_ATYPE0

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000004

This register is not being used for this device.

TCSR_FAB_ATYPE0

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	FAB_ATYPE0_CFG	FABRIC ATYPE[3:0]

0x1A400054 TCSR_FAB_ATYPE1

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000004

This register is not being used in this device.

TCSR_FAB_ATYPE1

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	FAB_ATYPE1_CFG	FABRIC ATYPE[3:0]

0x1A400058 TCSR_FAB_ATYPE2

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000004

This register is used to drive atype of M2 of system fabric in this device. ADM is connected to M2 AXI interface of system fabric.

TCSR_FAB_ATYPE2

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	FAB_ATYPE2_CFG	0x0: reserved_1 0x1: strongly ordered (non-cacheable, shared) 0x2: device, non-shared (non-cacheable) 0x3: device, shared (non-cacheable) 0x4: normal, non-cacheable, non-shared 0x5: normal, non-cacheable, shared 0x6: normal, cacheable, write-back, write-allocate. non-shared 0x7: normal, cacheable, write-back, write-allocate. shared 0x8: reserved_2 0xC: normal, cacheable, write-through, no write-allocate. non-shared 0xD: normal, cacheable, write-through, no write-allocate. shared 0xE: normal, cacheable, write-back, no write-allocate. non-shared 0xF: normal, cacheable, write-back, no write-allocate. shared

0x1A40005C TCSR_FAB_ATYPE3

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000004

This register is used to drive atype of M3 of system fabric. ADM is connected to M3 AXI interface of system fabric.

TCSR_FAB_ATYPE3

Bits	Name	Description
31:4	RESERVED_31_4	

TCSR_FAB_ATYPE3 (cont.)

Bits	Name	Description
3:0	FAB_ATYPE3_CFG	0x0: reserved_1 0x1: strongly ordered (non-cacheable, shared) 0x2: device, non-shared (non-cacheable) 0x3: device, shared (non-cacheable) 0x4: normal, non-cacheable, non-shared 0x5: normal, non-cacheable, shared 0x6: normal, cacheable, write-back, write-allocate. non-shared 0x7: normal, cacheable, write-back, write-allocate. shared 0x8: reserved_2 0xC: normal, cacheable, write-through, no write-allocate. non-shared 0xD: normal, cacheable, write-through, no write-allocate. shared 0xE: normal, cacheable, write-back, no write-allocate. non-shared 0xF: normal, cacheable, write-back, no write-allocate. shared

0x1A400060 TCSR_FAB_ATYPE4

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000004

This register is used to drive atype of M4 of system fabric. ADM is connected to M4 AXI interface of system fabric.

TCSR_FAB_ATYPE4

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	FAB_ATYPE4_CFG	0x0: reserved_1 0x1: strongly ordered (non-cacheable, shared) 0x2: device, non-shared (non-cacheable) 0x3: device, shared (non-cacheable) 0x4: normal, non-cacheable, non-shared 0x5: normal, non-cacheable, shared 0x6: normal, cacheable, write-back, write-allocate. non-shared 0x7: normal, cacheable, write-back, write-allocate. shared 0x8: reserved_2 0xC: normal, cacheable, write-through, no write-allocate. non-shared 0xD: normal, cacheable, write-through, no write-allocate. shared 0xE: normal, cacheable, write-back, no write-allocate. non-shared 0xF: normal, cacheable, write-back, no write-allocate. shared

0x1A400064 TCSR_FAB_ATYPE5

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000004

This register is used to drive atype of M5 of system fabric. ADM is connected to M5 AXI interface of system fabric.

TCSR_FAB_ATYPE5

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	FAB_ATYPE5_CFG	0x0: reserved_1 0x1: strongly ordered (non-cacheable, shared) 0x2: device, non-shared (non-cacheable) 0x3: device, shared (non-cacheable) 0x4: normal, non-cacheable, non-shared 0x5: normal, non-cacheable, shared 0x6: normal, cacheable, write-back, write-allocate. non-shared 0x7: normal, cacheable, write-back, write-allocate. shared 0x8: reserved_2 0xC: normal, cacheable, write-through, no write-allocate. non-shared 0xD: normal, cacheable, write-through, no write-allocate. shared 0xE: normal, cacheable, write-back, no write-allocate. non-shared 0xF: normal, cacheable, write-back, no write-allocate. shared

0x1A400070 TCSR_ADM_0_A_CRCI_MUX_SEL

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register is used for CRCI MUXing by ADM3.

TCSR_ADM_0_A_CRCI_MUX_SEL

Bits	Name	Description
31	ADM0_CRCI_TSIF_SEL	Select CRCI Request from TSIF 0 and 1. 0x0: TSIF 0 Req, 1 = TSIF 1 Req
30:8	RESERVED_30_8	Used by ADM
7	ADM0_CRCI_GSBI4_RX_SEL	Select CRCI req from GSBI4 UART/QUP RX req. 0 = QUP RX Req, 1 = UART RX Req

TCSR_ADM_0_A_CRCI_MUX_SEL (cont.)

Bits	Name	Description
6	ADM0_CRCI_GSBI4_TX_SEL	Select CRCI req from GSBI4 UART/QUP TX req. 0x0: QUP TX Req, 1 = UART TX Req
5	ADM0_CRCI_GSBI3_RX_SEL	Select CRCI req from GSBI3 UART/QUP RX req. 0x0: QUP RX Req, 1 = UART RX Req
4	ADM0_CRCI_GSBI3_TX_SEL	Select CRCI req from GSBI3 UART/QUP TX req. 0x0: QUP TX Req, 1 = UART TX Req
3	ADM0_CRCI_GSBI2_RX_SEL	Select CRCI req from GSBI2 UART/QUP RX req. 0x0: QUP RX Req, 1 = UART RX Req
2	ADM0_CRCI_GSBI2_TX_SEL	Select CRCI req from GSBI2 UART/QUP TX req. 0x0: QUP TX Req, 1 = UART TX Req
1	ADM0_CRCI_GSBI1_RX_SEL	Select CRCI req from GSBI1 UART/QUP RX req. 0x0: QUP RX Req, 1 = UART RX Req
0	ADM0_CRCI_GSBI1_TX_SEL	Select CRCI req from GSBI1 UART/QUP TX req. 0x0: QUP TX Req, 1 = UART TX Req

0x1A400074 TCSR_ADM_0_B_CRCI_MUX_SEL

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register is used for CRCI MUXing by ADM3.

TCSR_ADM_0_B_CRCI_MUX_SEL

Bits	Name	Description
31:11	RESERVED_31_11	
10	ADM0_CRCI_TSIF_SEL	Select CRCI Request from TSIF 0 and 1. 0x0: TSIF 0 Req, 1 = TSIF 1 Req
9:8	RESERVED_9_8	
7	ADM0_CRCI_GSBI7_TX_SEL	Select CRCI req from GSBI7 UART/QUP TX req. 0x0: QUP TX Req, 1 = UART TX Req
6	ADM0_CRCI_GSBI7_RX_SEL	Select CRCI req from GSBI7 UART/QUP RX req. 0x0: QUP RX Req, 1 = UART RX Req
5	ADM0_CRCI_GSBI6_TX_SEL	Select CRCI req from GSBI6 UART/QUP TX req. 0x0: QUP TX Req, 1 = UART TX Req
4:0	RESERVED_4_0	

0x1A400080 TCSR_CPSS_DEBUG_BUS_SEL

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register is used to select the CPSS test bus.

TCSR_CPSS_DEBUG_BUS_SEL

Bits	Name	Description
31:2	RESERVED_31_2	
1:0	CPSS_DBG_BUS_SEL	Used to select CPSS test bus. 0x0: Selects all X'00000000' on the CPSS test bus 0x1: Selects all X'55555555' on the CPSS test bus 0x2: Selects all X'AAAAAAAA' on the CPSS test bus 0x3: Selects the internal test bus

0x1A40008C TCSR_SPARE1

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

This is a 16 bit spare read/write register for possible ECO use. The bottom 3 bits are used as control inputs to the USB XO Shutdown ECO.

TCSR_SPARE1

Bits	Name	Description
31:16	RESERVED_31_16	
15:3	SPARES_15_3	Spare Reg
2	USB_XO_SD_RESET	USB XO Shutdown edge detect reset 0x1: reset 0x0: no reset
1	USB_XO_SD_FS_B_EN	USB XO Shutdown Full Speed USB B data interrupt enable 0x1: enable 0x0: disable
0	USB_XO_SD_FS_A_EN	USB XO Shutdown Full Speed USB A data interrupt enable 0x1: enable 0x0: disable

0x1A400090 TCSR_SPARE2

Type: Read/Write and Read Only
Clock: AXI_CLOCK
Reset State: 0x00000000

This is a 16 bit spare partial read/write and read only register for possible ECO use. The bottom 6 bits are used for a USB XO Shutdown ECO. The are used to read the current state of the High Speed USB DP/DM lines.

TCSR_SPARE2

Bits	Name	Description
31:16	RESERVED_31_16	
15:0	SPARES	Spare Reg

0x1A400094 TCSR_GSBI_IRQ_MUX_SEL_1

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register is used to select between the GSBI IRQs to output o_top_gsbi_irq_1.

TCSR_GSBI_IRQ_MUX_SEL_1

Bits	Name	Description
31:3	RESERVED_31_3	
2:0	GSBI_IRQ_MUX_SEL	Selects the GSBI IRQ corresponding to value in register

0x1A400098 TCSR_GSBI_IRQ_MUX_SEL_2

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register is used to select between the GSBI IRQs to output o_top_gsbi_irq_2.

TCSR_GSBI_IRQ_MUX_SEL_2

Bits	Name	Description
31:3	RESERVED_31_3	
2:0	GSBI_IRQ_MUX_SEL	Selects the GSBI IRQ corresponding to value in register

0x1A40009C TCSR_GSBI_IRQ_MUX_SEL_3

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register is used to select between the GSBI IRQs to output o_top_gsbi_irq_3.

TCSR_GSBI_IRQ_MUX_SEL_3

Bits	Name	Description
31:3	RESERVED_31_3	
2:0	GSBI_IRQ_MUX_SEL	Selects the GSBI IRQ corresponding to value in register

0x1A4000A0 TCSR_GSBI_IRQ_MUX_SEL_4

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register was used to select between the GSBI IRQs to output o_top_gsbi_irq_4.

Not in use for APQ8064 since the output of the mux selected by this register is not connected.

Due to the SPS changes from previous chips to APQ8064, there are not enough IRQ inputs available in the SPS. As such, a decision was made not to use this IRQ at all.

Can be used as a 3-bit spare register, if needed.

TCSR_GSBI_IRQ_MUX_SEL_4

Bits	Name	Description
31:3	RESERVED_31_3	
2:0	GSBI_IRQ_MUX_SEL	Selects the GSBI IRQ corresponding to value in register

0x1A4000A4 TCSR_SATA_BRIC_DEBUG_BUS_SEL

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register is used to select the SATA test bus.

TCSR_SATA_BRIC_DEBUG_BUS_SEL

Bits	Name	Description
31:3	RESERVED_31_3	
2:0	SATA_DBG_BUS_SEL	Used to select SATA test bus.

0x1A4000A8 TCSR_PCIE_BRIC_DEBUG_BUS_SEL

Type: Read/Write
Clock: AXI_CLOCK
Reset State: 0x00000000

The register is used to select the PCIE test bus.

TCSR_PCIE_BRIC_DEBUG_BUS_SEL

Bits	Name	Description
31:3	RESERVED_31_3	
2:0	PCIE_DBG_BUS_SEL	Used to select PCIE test bus.

2.18 PRNG Registers (0x1A500000 PRNG_BASE)

This section lists the registers associated with the PRNG block.

0x1A500000 PRNG_DATA_OUT

Type: Read
Reset State: 0x00000000

PRNG_DATA_OUT

Bits	Name	Description
31:0	PRNG_DATA_OUT	Pseudo Random Number output. If the FIFO is empty, reading this register will return 0.

0x1A500004 PRNG_STATUS

Type: Read
Reset State: 0x00000000

PRNG_STATUS

Bits	Name	Description
31:10	RESERVED_31_8	RESERVED
9:8	CURRENT_OPERATION	0x0: IDLE 0x1: GENERATE 0x2: INSTANTIATE 0x3: RESEED
7	GENERATE_REQUIRED	Indicates that a generate is, or soon will be occurring. This occurs when the generate counter != 0. This is only valid when the PRNG is enabled (PRNG_EN = 1)
6	RESEED_REQUIRED	Indicates that a reseed operation is, or soon will be occurring. This occurs when the reseed counter = reseed freq. This is only valid when the PRNG is enabled (PRNG_EN = 1)
5	INSTANTIATE_REQUIRED	Indicates that an instantiate operation or soon will be occurring. This occurs when the instantiate counter = 0. This is only valid when the PRNG is enabled (PRNG_EN = 1)
4	RING_OSC3_HEALTHY	Indicates that ring oscillator 3 is healthy. Only valid when RING_OSC3_CFG is set to one of the feedback settings (not valid when set to one of the FORCE inputs). When set to one of the FORCE inputs, this is reset to 0.
3	RING_OSC2_HEALTHY	Indicates that ring oscillator 2 is healthy. Only valid when RING_OSC2_CFG is set to one of the feedback settings (not valid when set to one of the FORCE inputs). When set to one of the FORCE inputs, this is reset to 0.

PRNG_STATUS (cont.)

Bits	Name	Description
2	RING_OSC1_HEALTHY	Indicates that ring oscillator 1 is healthy. Only valid when RING_OSC1_CFG is set to one of the feedback settings (not valid when set to one of the FORCE inputs).When set to one of the FORCE inputs, this is reset to 0.
1	RING_OSC0_HEALTHY	Indicates that ring oscillator 0 is healthy. Only valid when RING_OSC0_CFG is set to one of the feedback settings (not valid when set to one of the FORCE inputs). When set to one of the FORCE inputs, this is reset to 0.
0	DATA_AVAIL	Indicates that data is available on the PRNG_DATA_OUT FIFO.

0x1A500010 PRNG_ENTROPY_CNTR

Type: Read
Reset State: 0x00000000

PRNG_ENTROPY_CNTR

Bits	Name	Description
31:0	ENTROPY_CNTR	The current value of the entropy counter. Counts DOWN. Usually this is 0 except when actually doing an instantiate or reseed operation.

0x1A500014 PRNG_SAMPLE_CNTR

Type: Read
Reset State: 0x00000000

PRNG_SAMPLE_CNTR

Bits	Name	Description
31:0	SAMPLE_CNTR	The number of clocks since the last sample of the LFSRs. Counts DOWN. Usually this is 0 except when actually doing an instantiate or reseed operation.

0x1A500018 PRNG_GEN_CNTR

Type: Read
Reset State: 0x00000000

PRNG_GEN_CNTR

Bits	Name	Description
31:0	PRNG_GEN_CNTR	Current value of the generate counter

0x1A50001C PRNG_RESEED_CNTR

Type: Read
Reset State: 0x00000000

PRNG_RESEED_CNTR

Bits	Name	Description
31:0	RESEED_CNTR	Current value of the reseed counter

0x1A500020 PRNG_INSTANTIATE_CNTR

Type: Read
Reset State: 0x00000000

PRNG_INSTANTIATE_CNTR

Bits	Name	Description
31:0	INSTANTIATE_CNTR	The current number of reseed operations since the last reseed.

0x1A500024 PRNG_DEBUG

Type: Read
Reset State: 0x00000000

This register is provided to aid in debugging.

PRNG_DEBUG

Bits	Name	Description
31:14	RESERVED_31_14	RESERVED_31_14
13:10	RNG_STATE	RNG state machine state 0x0: IDLE 0x1: ENABLE_HASHGEN 0x2: ENABLE HASH DF H 0x3: UPDATE V 0x4: ENABLE HASH DF V 0x5: POP STATE COLLECTOR V 0x6: ENABLE HASH DF C 0x7: POP STATE COLLECTOR C
9:7	HASHGEN_STATE	Hash_gen states 0x0: IDLE 0x1: INITIALIZE 0x2: WAIT SHA DONE 0x3: UPDATE LOCAL V

PRNG_DEBUG (cont.)

Bits	Name	Description
6:4	HASH_DF_STATE	Hash DF states 0x0: IDLE 0x1: INITIALIZE 0x2: WAIT IDLE
3:0	PAD_STATE	Padding engine state machine 0x0: IDLE 0x1: PERSONALIZATION STRING 0x2: LOAD ENTROPY 0x3: INSERT V 0x4: LOAD STEP ID 0x5: LOAD NUM BITS 0x6: LOAD CNTR VAL 0x7: UPDATE HASHCNT 0x8: PAD FIRST 0x9: PAD ZEROES 0xA: PAD LENGTH 1 0xB: PAD LENGTH 0 0xC: WAIT SHA DONE

0x1A500100 PRNG_LFSR_CFG

Type: Read/Write
Reset State: 0x00000000

PRNG_LFSR_CFG

Bits	Name	Description
31:16	RESERVED_31_16	RESERVED
15	LFSR3_EN	Enables the output of LFSR3. When disabled, the LFSR is reset to 0 and disables the clock to the LFSR.
14:12	RING_OSC3_CFG	Configuration for Ring Oscillator 3 0x0: FORCE0. This is used for testability 0x2: FORCE1. This is used for testability. 0x4: feedback point 0 (slowest) 0x5: feedback point 1 0x6: feedback point 2 0x7: feedback point 3 (fastest)
11	LFSR2_EN	Enables the output of LFSR2. When disabled, the LFSR is reset to 0 and disables the clock to the LFSR.

PRNG_LFSR_CFG (cont.)

Bits	Name	Description
10:8	RING_OSC2_CFG	Configuration for Ring Oscillator 2 0x0: FORCE0. This is used for testability 0x2: FORCE1. This is used for testability. 0x4: feedback point 0 (slowest) 0x5: feedback point 1 0x6: feedback point 2 0x7: feedback point 3 (fastest)
7	LFSR1_EN	Enables the output of LFSR1. When disabled, the LFSR is reset to 0 and disables the clock to the LFSR.
6:4	RING_OSC1_CFG	Configuration for Ring Oscillator 1 0x0: FORCE0. This is used for testability 0x2: FORCE1. This is used for testability. 0x4: feedback point 0 (slowest) 0x5: feedback point 1 0x6: feedback point 2 0x7: feedback point 3 (fastest)
3	LFSR0_EN	Enables the output of LFSR0. When disabled, the LFSR is reset to 0 and disables the clock to the LFSR.
2:0	RING_OSC0_CFG	Configuration for Ring Oscillator 0 0x0: FORCE0. This is used for testability 0x2: FORCE1. This is used for testability. 0x4: feedback point 0 (slowest) 0x5: feedback point 1 0x6: feedback point 2 0x7: feedback point 3 (fastest)

0x1A500104 PRNG_CONFIG

Type: Read/Write
Reset State: 0x00000000

PRNG_CONFIG

Bits	Name	Description
31:6	RESERVED_31_6	RESERVED_31_6

PRNG_CONFIG (cont.)

Bits	Name	Description
5:2	TEST_OUT_SEL	Selects the appropriate test output to be put out on prng_rosc_test_out signal: 0x0: Output 0 0x8: rosc0_div_32 0x9: rosc1_div_32 0xA: rosc2_div_32 0xB: rosc3_div_32 0xC: rosc0_samp 0xD: rosc1_samp 0xE: rosc2_samp 0xF: rosc3_samp
1	PRNG_EN	Enable signal for the PRNG indicating that all setup is complete. Ring oscillators and the LFSR will still operate as per PRNG_LFSR_CFG, however when this is 0, the PRNG when the PRNG is disabled it will return to the IDLE state once its current operation has been completed, with the current operation possibly requiring space to be created in the output fifo for data that must be generated in the completion of the current operation. This space can be created by reading from the PRNG_DATA_OUT register. 0x0: disabled 0x1: enabled
0	SW_RESET	Software initiated reset. Automatically cleared when the write operation is complete. Reset is internally held for 2 clock cycles after this register is written and so no operations/accesses should be attempted until after this recovery time.

0x1A500108 PRNG_PERSONALIZATION_STRING

Type: Read/Write
Reset State: 0x00000000

PRNG_PERSONALIZATION_STRING

Bits	Name	Description
31:0	PERSONALIZATION_STRING	The personalization string. This may be all 0, but also may be obtained from other non-regular processes such as time between key presses, searcher noise (if present), or other system events.

0x1A500110 PRNG_NUM_ENTROPY

Type: Read/Write
Reset State: 0x00000400

PRNG_NUM_ENTROPY

Bits	Name	Description
31:0	NUM_ENTROPY_BYTES	Indicates the number of entropy bytes to be used during instantiate and reseed processes. Note that the minimum value of this field should be 16 for this design, although no enforcement is done in HW. Larger values provide more randomness. NIST SP800-90 specifies the maximum value to be 235 BITS.

0x1A500114 PRNG_SAMPLE_FREQ

Type: Read/Write
Reset State: 0x00000400

PRNG_SAMPLE_FREQ

Bits	Name	Description
31:0	SAMPLE_FREQ	The number of clocks between samples of the LFSR.

0x1A500118 PRNG_GEN_WORDS

Type: Read/Write
Reset State: 0x00000008

PRNG_GEN_WORDS

Bits	Name	Description
31:0	REQUESTED_WORDS	The number of words per generate operation

0x1A50011C PRNG_RESEED_FREQ

Type: Read/Write
Reset State: 0x00010000

PRNG_RESEED_FREQ

Bits	Name	Description
31:0	RESEED_FREQ	The number of generate operations before a reseed is initiated. The minimum number of generate operations before a reseed is initiated is 2.

0x1A500120 PRNG_INSTANTIATE_FREQ

Type: Read/Write
Reset State: 0x00010000

PRNG_INSTANTIATE_FREQ

Bits	Name	Description
31:0	INSTANTIATE_FREQ	The number of reseed operations before an instantiate is initiated.

2.19 Chip System FPB 0 Registers (0x1B100000 CFPB0_XPU_CFG_BASE)

This section contains the Chip FPB 0 XPU registers.

0x1B100000+ 4*n CFPB0_XPU_APU_RGn_ACR, n=[0..16]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 01, i.e., a single VMID, read/write access vs. read-only access permission type APU. These registers include 2 separate 5 bit "owner" VMID fields

CFPB0_XPU_APU_RGn_ACR

Bits	Name	Description
31:26	RESERVED31_26	Reserved.
25	ROGE	Read-only global enable: Opens up read-only access for this resource group to all VMIDs if: ROGE | (ROE & (VMID = ROVMID)) | APU_APU_ACR[VMID] = 1
24	ROE	Read-only enable. This is a "valid" bit for the ROVMID field.
23:21	RESERVED23_21	Reserved
20:16	ROVMID	Read-only VMID. Specifies "owner" VMID with read-only access to the registers in the associated resource group.
15:10	RESERVED15_10	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | APU_APU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a "valid" bit for the RWVMID field
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies "owner" VMID with full read/write access to the registers in the associated resource group.

0x1B100F80 CFPB0_XPU_APU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

CFPB0_XPU_APU_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set APU_ESR. APU_EAR and APU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set APU_ESR. APU_EAR and APU_ESYNR0 updated with address and syndrome of error.
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x1B100F84 CFPB0_XPU_APU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port.

CFPB0_XPU_APU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x1B100F88 CFPB0_XPU_APU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the APU_ESYNRn registers, which are merely the "syndrome" of an error indicated by APU_ESR.

CFPB0_XPU_APU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x1B100F8C CFPB0_XPU_APU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

CFPB0_XPU_APU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x1B100F90 CFPB0_XPU_APU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

CFPB0_XPU_APU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x1B100F94 CFPB0_XPU_APU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

CFPB0_XPU_APU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x1B100FF4 CFPB0_XPU_APU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

CFPB0_XPU_APU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved

CFPB0_XPU_APU_REV (cont.)

Bits	Name	Description
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x1B100FF8 CFPB0_XPU_APU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x00001810

APU ID Register: Read-only register that defines various configuration attributes of the APU instance.

CFPB0_XPU_APU_IDR

Bits	Name	Description
31:29	RESERVED31_21	Reserved
28:24	MSB	Indicates most significant address bit number used to select a resource group
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMIDs have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.

CFPB0_XPU_APU_IDR (cont.)

Bits	Name	Description
9	RESERVED9	Reserved
8:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

0x1B100FFC CFPB0_XPU_APU_APU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

APU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the APU (including the APU_APU_ACR itself).

CFPB0_XPU_APU_APU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the APU's 4KB address region (including the APU_APU_ACR itself). For single VMID type APUs (APU_IDR[MV] = 0) the APU_APU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

2.20 Chip System FPB0 Registers (0x1B200000 CSYSFPB0_BASE)

This section contains the Chip System FPB 0 registers.

0x1B200000 CSYSFPB0_CFPB0_CTRL_STATUS

Type: Read/Write
Clock: CC_CFPB0_CLK
Reset State: 0x00000000

This register is a general configuration register.

CSYSFPB0_CFPB0_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables Power up value is clear (0)
11	RPM_PROC_IRQ_EN	SW: RW, HW: R PRMProcInterruptEnable When set, the RPM Processor receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	APPS_PROC_IRQ_EN	SW: RW, HW: R AppsProcInterruptEnable When set, the Application Processor receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

CSYSFPB0_CFPB0_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x5: Select the S0_M0 ahb2ahb bridge test bus. 0x6: Select the S1_M1 ahb2ahb bridge test bus. 0x7: Select the M0 ahb2ahb bridge test bus. 0x8: Select the M1 ahb2ahb bridge test bus. 0x9: Select the M2 ahb2ahb bridge test bus. 0xA: Select the M3 ahb2ahb bridge test bus. 0xB: Select the M4 ahb2ahb bridge test bus. 0xC: Select the M5 ahb2ahb bridge test bus. 0xD: Select the M6 ahb2ahb bridge test bus. 0xE: Select the M7 ahb2ahb bridge test bus. 0xF: Select the M8 ahb2ahb bridge test bus. 0x10: Select the M9 ahb2ahb bridge test bus. 0x11: Select the M10 ahb2ahb bridge test bus. 0x12: Select the M11 ahb2ahb bridge test bus. 0x13: Select the M12 ahb2ahb bridge test bus. 0x14: Select the M13 ahb2ahb bridge test bus. 0x15: Select the M14 ahb2ahb bridge test bus. 0x16: Select the M15 ahb2ahb bridge test bus.

0x1B200004+ 0x4*a CSYSFPB0_CFPB0_AHB2AHB_CFG_Ma, a=[0..0]

Type: Read/Write
Clock: CC_CFPB0_CLK
Reset State: 0x00000009

The CFPB0_AHB2AHB_CFG_Ma register is to configure the AHB2AHB bridge of master Ma. The AHB2AHB bridge is instantiated if the AHB interface is async (Generic: MASTER_ASYNC_IF(a) = ’1’). Otherwise this register is reserved.

CSYSFPB0_CFPB0_AHB2AHB_CFG_Ma

Bits	Name	Description
30:6	RESERVED_BITS30_6	

CSYSFPB0_CFPB0_AHB2AHB_CFG_Ma (cont.)

Bits	Name	Description
5:4	M_AHB2AHB_TEST_EN	SW: RW, HW: R Test enable for the Sa lite_bridge. Power up value is 00 0x0: DISABLED 0x1: Select slave side test signals 0x2: Select master side test signals 0x3: RESERVED_PROGRAMMING
3	M_WPOST_EN	SW: RW, HW: R MaWritePostEnable When set (1), the ahb2ahb bridge will support posting of write data. When cleared (0), each write request must complete across the bus before the next is accepted. Power up value is set (1)
2	M_HALT_ACK	SW:R, HW:W Indicates the Ma acknowledgement of halt_req asserted by software. Power up value is clear (0).
1	M_HALT_REQ	SW:RW, HW:R Software should write to this register to request the Ma lite_bridge master to cleanly halt. Power up value is clear (0).
0	M_IDLE	SW:R, HW:W Indicates that the Ma lite bridge master FSM is in IDLE state. Power up value is set (1).

0x1B200044 CSYSFPB0_CFPB0_PORT_EN

Type: Read/Write
Clock: CC_CFPB0_CLK
Reset State: 0xFFFFFFFF

This register is the CFPB0 master port enable register.

CSYSFPB0_CFPB0_PORT_EN

Bits	Name	Description
31:1	RESERVED_BIT31_1	Only one master port is used.
0	M0_PORT_EN	SW: RW, HW: R M0PortEnable When cleared (0), M0 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

0x1B200050 CSYSFPB0_CFPB0_ERROR_STAT

Type: Read/Write
Clock: CC_CFPB0_CLK
Reset State: 0x00000000

This register is the bus error status register.

CSYSFPB0_CFPB0_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the channel ID that caused the detected error when CID is valid for the master of the access. If not, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Master0 0x1: Master1 0x2: Master2 0x3: Master3 0x4: Master4 0x5: Master5 0x6: Master6 0x7: Master7 0x8: Master8 0x9: Master9 0xA: Master10 0xB: Master11 0xC: Master12 0xD: Master13 0xE: Master14 0xF: Master15
11:10	RESERVED_BITS11_10	

CSYSFPB0_CFPB0_ERROR_STAT (cont.)

Bits	Name	Description
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit
3:2	RESERVED_BIT3_2	
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted. Clearing (0) this bit clears any interrupts asserted as well as enables the ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x1B200054 CSYSFPB0_CFPB0_ERROR_ADDR

Type: Read
Clock: CC_CFPB0_CLK
Reset State: 0x00000000

This register contains the bus error address.

CSYSFPB0_CFPB0_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x1B200058 CSYSFPB0_CFPB0_GPREG

Type: Read/Write
Clock: CC_CFPB0_CLK
Reset State: 0x00000000

This register is a configurable general purpose register. This is 9-bit register. The size of this register is defined by the generic-SFPB_GPREG_SIZE (1 - 32 bits). It is set to 9.

CSYSFPB0_CFPB0_GPREG

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8:1	MSM_TIMEOUT_VAL	SW: RW, HW: W APQ will wait for time out value for ACK to receive from the Slave if MSM_TIMEOUT_VAL is programmed and if timeout is enabled. If ACK is not received within the timeout value, APQ will respond with Error. Power up value is clear (0)
0	MSM_TIMEOUT_EN	SW: RW, HW: W Enables the time out value if set to ’1’ Power up value is clear (0)

0x1B20005C CSYSFPB0_CFPB0_XPU_ACR

Type: Read/Write
Clock: CC_CFPB0_CLK
Reset State: 0xFFFFFFFF

The CFPB0_XPU_ACR register is the CFPB0 Access Control Register for configuring register protection.

CSYSFPB0_CFPB0_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R CFPB0 XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the CFPB0 configure space, including this register itself. Power up value is set (1)

0x1B200060 CSYSFPB0_CFPB0_HW_CLK_GATING_CFG

Type: Read/Write
Clock: CC_CFPB0_CLK
Reset State: 0x00000000

The CFPB0_HW_CLK_GATING_CFG register is for hardware clock gating configuration.

CSYSFPB0_CFPB0_HW_CLK_GATING_CFG

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	HYSTERESIS_CNT_SW	SW: RW, HW: R Hysteresis Counter Value This field is used by SW to set the hysteresis counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)
3:0	WAKE_CNT_SW	SW: RW, HW: R Wakeup Counter Value This field is used by SW to set the wakeup counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)

3 Chip Core Top Registers

3.1 Overview

Table 3-1 chip_core_top Bases

Base Name	Parent	Address
TLMM_RPU_RGn_ACR	TLMM_BASE	0x00800000
SYS_IMEM_IMEM_CONFIG	SYS_IMEM_BASE	0x00B00000
SPDM_SREG_CFG0	SPDM_SECURE_BASE	0x01100000
SPDM_CREG_CFG0	SPDM_BASE	0x01000000
SPDM_OLEM_CFG0	SPDM_BASE	0x01000000
SPDM_RT_LOW_THRESH_STATUS	SPDM_BASE	0x01000000

3.2 TLMM Registers (0x00800000 TLMM_BASE)

This section contains the TLMM registers.

3.2.1 GPIO registers

3.2.1.1 Super User Only registers

The following security registers are access control registers (ACRs) that control permissions for the other registers in the TLMM. Any VMID defined as a Super User (SU) has access to all registers in the TLMM.

0x00800000+ 0x4*n TLMM_RPU_RGn_ACR, n=[0..89]

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

One per GPIO. The TLMM_RPU_RGn_ACR registers control access to a standard grouping of registers deemed to be a 'GPIO Resource.' The following registers make up a GPIO Resource: GPIO_CFGn, GPIO_IN_OUTn, GPIO_INTR_CFGn, GPIO_INTR_STATUSn. Only a single VMID can be an owner for a given GPIO Resource. Permissions are Access/No Access.

TLMM_RPU_RGn_ACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00800300 TLMM_SPARE_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The TLMM_SPARE_WACR register controls the read/write access permissions for the TLMM_SPARE register. Only a single VMID can be given read/write control of this register.

TLMM_SPARE_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00800304 TLMM_SPARE_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The TLMM_SPARE_RACR register controls the read-only access for the TLMM_SPARE register. Only a single VMID can be given read/write control of this register.

TLMM_SPARE_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x008002F0 RIVA_COEXIST_GPIO_PORT_SEL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The RIVA_COEXIST_GPIO_PORT_SEL_WACR register controls the read/write access permissions for the RIVA_COEXIST_GPIO_PORT_SEL register. Only a single VMID can be given read/write control of this register.

RIVA_COEXIST_GPIO_PORT_SEL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008002F4 RIVA_COEXIST_GPIO_PORT_SEL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The RIVA_COEXIST_GPIO_PORT_SEL_RACR register controls the read-only access for the RIVA_COEXIST_GPIO_PORT_SEL register. Only a single VMID can be given read/write control of this register.

RIVA_COEXIST_GPIO_PORT_SEL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800310 GP_PDM0_GPIO_PORT_SEL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GP_PDM0_GPIO_PORT_SEL_WACR register controls the read/write access permissions for the GP_PDM0_GPIO_PORT_SEL register. Only a single VMID can be given read/write control of this register.

GP_PDM0_GPIO_PORT_SEL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00800314 GP_PDM0_GPIO_PORT_SEL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GP_PDM0_GPIO_PORT_SEL_RACR register controls the read-only access for the GP_PDM0_GPIO_PORT_SEL register. Only a single VMID can be given read/write control of this register.

GP_PDM0_GPIO_PORT_SEL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800318 GP_PDM1_GPIO_PORT_SEL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GP_PDM1_GPIO_PORT_SEL_WACR register controls the read/write access permissions for the GP_PDM1_GPIO_PORT_SEL register. Only a single VMID can be given read/write control of this register.

GP_PDM1_GPIO_PORT_SEL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0080031C GP_PDM1_GPIO_PORT_SEL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GP_PDM1_GPIO_PORT_SEL_RACR register controls the read-only access for the GP_PDM1_GPIO_PORT_SEL register. Only a single VMID can be given read/write control of this register.

GP_PDM1_GPIO_PORT_SEL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800320 GP_PDM2_GPIO_PORT_SEL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GP_PDM2_GPIO_PORT_SEL_WACR register controls the read/write access permissions for the GP_PDM2_GPIO_PORT_SEL register. Only a single VMID can be given read/write control of this register.

GP_PDM2_GPIO_PORT_SEL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00800324 GP_PDM2_GPIO_PORT_SEL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GP_PDM2_GPIO_PORT_SEL_RACR register controls the read-only access for the GP_PDM2_GPIO_PORT_SEL register. Only a single VMID can be given read/write control of this register.

GP_PDM2_GPIO_PORT_SEL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800328 SLIMBUS1_GPIO_PORT_SEL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The SLIMBUS1_GPIO_PORT_SEL_WACR register controls the read/write access permissions for the SLIMBUS1_GPIO_PORT_SEL register. Only a single VMID can be given read/write control of this register.

SLIMBUS1_GPIO_PORT_SEL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0080032C SLIMBUS1_GPIO_PORT_SEL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The SLIMBUS1_GPIO_PORT_SEL_RACR register controls the read-only access for the SLIMBUS1_GPIO_PORT_SEL register. Only a single VMID can be given read/write control of this register.

SLIMBUS1_GPIO_PORT_SEL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800330 SLIMBUS1_A_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The SLIMBUS1_A_CTL_WACR register controls the read/write access permissions for the SLIMBUS1_A_CTL register. Only a single VMID can be given read/write control of this register.

SLIMBUS1_A_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00800334 SLIMBUS1_A_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The SLIMBUS1_A_CTL_RACR register controls the read-only access for the SLIMBUS1_A_CTL register. Only a single VMID can be given read/write control of this register.

SLIMBUS1_A_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800338 SLIMBUS1_B_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The SLIMBUS1_B_CTL_WACR register controls the read/write access permissions for the SLIMBUS1_B_CTL register. Only a single VMID can be given read/write control of this register.

SLIMBUS1_B_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0080033C SLIMBUS1_B_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The SLIMBUS1_B_CTL_RACR register controls the read-only access for the SLIMBUS1_B_CTL register. Only a single VMID can be given read/write control of this register.

SLIMBUS1_B_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800308 USB_FS1_GPIO_PORT_SEL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The USB_FS1_GPIO_PORT_SEL_WACR register controls the read/write access permissions for the USB_FS1_GPIO_PORT_SEL register. Only a single VMID can be given read/write control of this register.

USB_FS1_GPIO_PORT_SEL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0080030C USB_FS1_GPIO_PORT_SEL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The USB_FS1_GPIO_PORT_SEL_RACR register controls the read-only access for the USB_FS1_GPIO_PORT_SEL register. Only a single VMID can be given read/write control of this register.

USB_FS1_GPIO_PORT_SEL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800350+0x4*n DIR_CONN_INTRn_POLARITY_ACR, n=[0..21]

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

One per Direct Connect Interrupt. The DIR_CONN_INTRn_POLARITY_ACR registers control access to the DIR_CONN_INTRn_POLARITY registers used to configure the Direct Connect Interrupt Polarity. Each Interrupt is protected separately allowing either a SU or the owner of a particular interrupt to configure the polarity. Only a single VMID can be an owner for a given Direct Connect Interrupt.

DIR_CONN_INTRn_POLARITY_ACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008003AC RESOUT_HDRV_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The RESOUT_HDRV_CTL_WACR register controls the read/write access permissions for the RESOUT_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

RESOUT_HDRV_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008003B0 RESOUT_HDRV_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The RESOUT_HDRV_CTL_RACR register controls the read-only access for the RESOUT_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

RESOUT_HDRV_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x008003B4 JTAG_HDRV_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The JTAG_HDRV_CTL_WACR register controls the read/write access permissions for the JTAG_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

JTAG_HDRV_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008003B8 JTAG_HDRV_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The JTAG_HDRV_CTL_RACR register controls the read-only access for the JTAG_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

JTAG_HDRV_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x008003BC PMIC_HDRV_PULL_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The PMIC_HDRV_CTL_WACR register controls the read/write access permissions for the PMIC_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

PMIC_HDRV_PULL_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008003C0 PMIC_HDRV_PULL_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The PMIC_HDRV_CTL_RACR register controls the read-only access for the PMIC_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

PMIC_HDRV_PULL_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x008003C4 SDC1_HDRV_PULL_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The SDC1_HDRV_CTL_WACR register controls the read/write access permissions for the SDC1_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

SDC1_HDRV_PULL_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008003C8 SDC1_HDRV_PULL_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The SDC1_HDRV_CTL_RACR register controls the read-only access for the SDC1_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

SDC1_HDRV_PULL_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x008003CC SDC3_HDRV_PULL_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The SDC3_HDRV_CTL_WACR register controls the read/write access permissions for the SDC3_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

SDC3_HDRV_PULL_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008003D0 SDC3_HDRV_PULL_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The SDC3_HDRV_CTL_RACR register controls the read-only access for the SDC3_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

SDC3_HDRV_PULL_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x008003D8 MODE_PULL_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The MODE_HDRV_CTL_WACR register controls the read/write access permissions for the MODE_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

MODE_PULL_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008003DC MODE_PULL_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The MODE_HDRV_CTL_RACR register controls the read-only access for the MODE_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

MODE_PULL_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x008003E0 GSBI4_3D_CAM_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI4_3D_CAM_CTL_WACR register controls the read/write access permissions for the GSBI4_3D_CAM_CTL register. Only a single VMID can be given read/write control of this register.

GSBI4_3D_CAM_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008003E4 GSBI4_3D_CAM_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI4_3D_CAM_CTL_RACR register controls the read-only access for the GSBI4_3D_CAM_CTL register. Only a single VMID can be given read/write control of this register.

GSBI4_3D_CAM_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x008003E8 GSBI7_3D_CAM_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI7_3D_CAM_CTL_WACR register controls the read/write access permissions for the GSBI7_3D_CAM_CTL register. Only a single VMID can be given read/write control of this register.

GSBI7_3D_CAM_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008003EC GSBI7_3D_CAM_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI7_3D_CAM_CTL_RACR register controls the read-only access for the GSBI7_3D_CAM_CTL register. Only a single VMID can be given read/write control of this register.

GSBI7_3D_CAM_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x008003F0 HSIC_STROBE_GPIO_PAD_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The HSIC_STROBE_GPIO_PAD_CTL_WACR register controls the read/write access permissions for the HSIC_STROBE_GPIO_PAD_CTL register. Only a single VMID can be given read/write control of this register.

HSIC_STROBE_GPIO_PAD_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008003F4 HSIC_STROBE_GPIO_PAD_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The HSIC_STROBE_GPIO_PAD_CTL_RACR register controls the read-only access for the HSIC_STROBE_GPIO_PAD_CTL register. Only a single VMID can be given read/write control of this register.

HSIC_STROBE_GPIO_PAD_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x008003F8 HSIC_DATA_GPIO_PAD_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The HSIC_DATA_GPIO_PAD_CTL_WACR register controls the read/write access permissions for the HSIC_DATA_GPIO_PAD_CTL register. Only a single VMID can be given read/write control of this register.

HSIC_DATA_GPIO_PAD_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008003FC HSIC_DATA_GPIO_PAD_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The HSIC_DATA_GPIO_PAD_CTL_RACR register controls the read-only access for the HSIC_DATA_GPIO_PAD_CTL register. Only a single VMID can be given read/write control of this register.

HSIC_DATA_GPIO_PAD_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800348 HSIC_CAL_PAD_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The HSIC_CAL_PAD_CTL_WACR register controls the read/write access permissions for the HSIC_CAL_PAD_CTL register. Only a single VMID can be given read/write control of this register.

HSIC_CAL_PAD_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0080034C HSIC_CAL_PAD_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The HSIC_CAL_PAD_CTL_RACR register controls the read-only access for the HSIC_CAL_PAD_CTL register. Only a single VMID can be given read/write control of this register.

HSIC_CAL_PAD_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800340 RGB_PAD_EN_WACR

Type: Read/Write
Clock: CC_TLMM_CLK
Reset State: 0x00000000

The RGB_PAD_EN_WACR register controls the read-only access for the RGB_PAD_EN register. Only a single VMID can be given read/write control of this register.

RGB_PAD_EN_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00800344 RGB_PAD_EN_RACR

Type: Read/Write
Clock: CC_TLMM_CLK
Reset State: 0x00000000

The RGB_PAD_EN_RACR register controls the read-only access for the RGB_PAD_EN register. Only a single VMID can be given read/write control of this register.

RGB_PAD_EN_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with full read access to the registers in the associated resource group.

0x008002F8 RGB_HDRV_CTL_WACR

Type: Read/Write
Clock: CC_TLMM_CLK
Reset State: 0x00000000

The RGB_HDRV_CTL_WACR register controls the read/write access permissions for the RGB_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

RGB_HDRV_CTL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x008002FC RGB_HDRV_CTL_RACR

Type: Read/Write
Clock: CC_TLMM_CLK
Reset State: 0x00000000

The RGB_HDRV_CTL_RACR register controls the read-only access for the RGB_HDRV_CTL register. Only a single VMID can be given read/write control of this register.

RGB_HDRV_CTL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with full read access to the registers in the associated resource group.

0x00800400+ 0x4*n GPIO_INTR_CFG_SUn, n=[0..89]

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000007

The summary interrupt control registers configure which processor the summary interrupt should be routed to. In addition, they control whether the GPIO is enabled as a direct connect interrupt.

GPIO_INTR_CFG_SUn

Bits	Name	Description
31:4	RESERVED	Reserved field.
3	DIR_CONN_EN	This bit tells the TLMM that GPIO[n] is being used as a Direct Connect Interrupt. 0x1: Enable 0x0: Disable

GPIO_INTR_CFG_SUn (cont.)

Bits	Name	Description
2:0	TARGET_PROC	This a 3-bit field that determines which processor a summary interrupt from GPIO[n] should get routed to. 0x0: RIVA_PROC 0x1: SPS_PROC 0x2: LPA_DSP 0x3: RPM_PROC 0x4: APCC_PROC 0x5: GSS_PROC 0x6: Reserved 0x7: NONE

0x00800600 GSBI1_UART_I2C_SEL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI1_UART_I2C_SEL_WACR register controls the read/write access permissions for the GSBI1_UART_I2C_SEL register. Only a single VMID can be given read/write control of this register.

GSBI1_UART_I2C_SEL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00800604 GSBI1_UART_I2C_SEL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI1_UART_I2C_SEL_RACR register controls the read-only access for the GSBI1_UART_I2C_SEL register. Only a single VMID can be given read/write control of this register.

GSBI1_UART_I2C_SEL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800608 GSBI2_UART_SEL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI2_UART_SEL_WACR register controls the read/write access permissions for the GSBI2_UART_SEL register. Only a single VMID can be given read/write control of this register.

GSBI2_UART_SEL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0080060C GSBI2_UART_SEL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI2_UART_SEL_RACR register controls the read-only access for the GSBI2_UART_SEL register. Only a single VMID can be given read/write control of this register.

GSBI2_UART_SEL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800610 GSBI3_UART_SEL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI3_UART_SEL_WACR register controls the read/write access permissions for the GSBI3_UART_SEL register. Only a single VMID can be given read/write control of this register.

GSBI3_UART_SEL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00800614 GSBI3_UART_SEL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI3_UART_SEL_RACR register controls the read-only access for the GSBI3_UART_SEL register. Only a single VMID can be given read/write control of this register.

GSBI3_UART_SEL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800618 GSBI4_UART_I2C_SEL_WACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI4_UART_I2C_SEL_WACR register controls the read/write access permissions for the GSBI4_UART_I2C_SEL register. Only a single VMID can be given read/write control of this register.

GSBI4_UART_I2C_SEL_WACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field
7:5	RESERVED_2	Reserved
4:0	RWVMID_4_0	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0080061C GSBI4_UART_I2C_SEL_RACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI4_UART_I2C_SEL_RACR register controls the read-only access for the GSBI4_UART_I2C_SEL register. Only a single VMID can be given read/write control of this register.

GSBI4_UART_I2C_SEL_RACR

Bits	Name	Description
31:10	RESERVED_1	Reserved
9	RGE	Read global enable. Opens up read access for this resource group to all VMIDs if: RGE | (RE & (VMID = RVMID)) | TLMM_RPU_ACR[VMID] = 1
8	RE	Read enable. This is a 'valid' bit for the RVMID field
7:5	RESERVED_2	Reserved
4:0	RVMID_4_0	Read VMID. Specifies 'owner' VMID with read access to the registers in the associated resource group.

0x00800700+ 0x4*n DIR_CONN_INTR_CFG_SUn, n=[0..21]

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000007

The direct connect interrupt config registers configure which GPIO will be used as a direct connect interrupt. They also configure which processor a direct connect interrupt should get routed to.

NOTE In addition to selecting which GPIO will be used as a direct connect interrupt with the GPIO_SEL bit field, the DIR_CONN_EN must be set in the GPIO_INTR_CFG_SUn register.

DIR_CONN_INTR_CFG_SUn

Bits	Name	Description
31:10	RESERVED	Reserved field
9:3	GPIO_SEL	This field selects which GPIO will be used on Direct Connect Interrupt n.
2:0	TARGET_PROC	This a 3-bit field that determines which processor a Direct Connect n should get routed to. 0x0: RIVA_PROC 0x1: SPS_PROC 0x2: LPA_DSP 0x3: RPM_PROC 0x4: APCC_PROC 0x5: GSS_PROC 0x6: Reserved 0x7: NONE

0x00800800 TLMM_CLK_GATE_EN_SU

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

This register can enable the clock gating in the TLMM. By default the clock gating is disabled.

NOTE

NOTE .

TLMM_CLK_GATE_EN_SU

Bits	Name	Description
31:5	RESERVED	Reserved field
4	AHB_HCLK_EN	Enables the Clock Gating on the AHB Clock. 0x1: ENABLE 0x0: DISABLE
3	DBG_STATUS_EN	Enables the Clock Gating on the Debug Status Demets. 0x1: ENABLE 0x0: DISABLE
2	JTAG_XTRIG_EN	Enables the Clock Gating on the Debug Cross Triggering Demets. 0x1: ENABLE 0x0: DISABLE
1	SUMMARY_INTR_EN	Enables the Clock Gating on the Summary Interrupt Demets. 0x1: ENABLE 0x0: DISABLE
0	CRIF_READ_EN	Enables the Clock Gating on the Read Data Register on the CRIF interface. 0x1: ENABLE 0x0: DISABLE

0x00800810 TLMM_IE_CTRL_DISABLE_SU

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0001

This register can enable/disable control of the pad input enable within the TLMM. By default the IE control is disabled. When disabled, the IE for all GPIOs is always high and the input path is always enabled. When IE_CTRL is enabled, the input path can enabled/disabled based on the direction of the function that is configured for the GPIO. This register only affects GPIOs.

Some loopback tests require the IE to always be high. As such, this bit is required functionality for certain test modes.

TLMM_IE_CTRL_DISABLE_SU

Bits	Name	Description
31:1	RESERVED	Reserved field
0	IE_CTRL_DISABLE	Enables control of the pad IE within TLMM. When disabled, the IE is tied high. 0x1: DISABLE 0x0: ENABLE

0x00800820 PSHOLD_CTL_SU

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

This register controls the PSHOLD value when the alternate function is selected on GPIO.

NOTE In addition to SW control and the tlmm reset, this register can be reset via HW by the temperature sensor.

PSHOLD_CTL_SU

Bits	Name	Description
31:1	RESERVED	Reserved.
0	PSHOLD_VALUE	Controls the value of the PSHOLD output. 0x1: Asserted 0x0: De-asserted

0x00800840 TLMM_MPM_WAKEUP_INT_EN_0_SU

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0

This register controls the input enable for the HV input path from the pad.

NOTE Interrupt enables are present within the MPM. This register is specifically used to gate the HV path from the pad to the MPM for power savings.

TLMM_MPM_WAKEUP_INT_EN_0_SU

Bits	Name	Description
31	GPIO_75	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
30	GPIO_72	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
29	GPIO_45	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
28	GPIO_44	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
27	GPIO_41	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
26	GPIO_65	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
25	GPIO_38	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
24	GPIO_61	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
23	GPIO_58	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
22	GPIO_50	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
21	GPIO_49	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
20	GPIO_36	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
19	GPIO_34	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable

TLMM_MPM_WAKEUP_INT_EN_0_SU (cont.)

Bits	Name	Description
18	GPIO_42	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
17	GPIO_32	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
16	GPIO_39	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
15	GPIO_30	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
14	GPIO_29	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
13	GPIO_26	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
12	GPIO_22	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
11	GPIO_18	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
10	GPIO_23	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
9	GPIO_19	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
8	GPIO_15	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
7	GPIO_6	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
6	GPIO_11	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable

TLMM_MPM_WAKEUP_INT_EN_0_SU (cont.)

Bits	Name	Description
5	GPIO_10	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
4	GPIO_7	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
3	SDC3_DATA_3	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
2	SDC3_DATA_1	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
1	SDC1_DATA_3	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
0	SDC1_DATA_1	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable

0x00800844 TLMM_MPM_WAKEUP_INT_EN_1_SU

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0

This register controls the input enable for the HV input path from the pad.

NOTE Interrupt enables are present within the MPM. This register is specifically used to gate the HV path from the pad to the MPM for power savings.

TLMM_MPM_WAKEUP_INT_EN_1_SU

Bits	Name	Description
31:18	RESERVED_1	Reserved Bits
17	RESERVED_2	Reserved Bits
16	GPIO_76	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
15	RESERVED_3	Reserved Bits

TLMM_MPM_WAKEUP_INT_EN_1_SU (cont.)

Bits	Name	Description
14	GPIO_77	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
13	RESERVED_4	Reserved Bits
12	RESERVED_5	Reserved Bits
11	GPIO_78	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
10	GPIO_79	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
9	GPIO_80	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
8	GPIO_74	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
7	GPIO_73	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
6	GPIO_63	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
5	GPIO_56	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
4	GPIO_55	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
3	GPIO_83	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
2	GPIO_81	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable
1	GPIO_47	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable

TLMM_MPM_WAKEUP_INT_EN_1_SU (cont.)

Bits	Name	Description
0	SRST_N	This is used to enable the HV interrupt path to the MPM: 0x0: Disable 0x1: Enable

0x00800F80 TLMM_RPU_CR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

RPU Configuration Register: This register includes fields governing various RPU behaviors

NOTE The RPUE bit field of this register is what enables VMID checking. When this bit is ’0’, all accesses are allowed. Once the SROT defines the Super User permissions in the TLMM_RPU_ACR register, this bit should be set to ’1’ to enable the TLMM security features.

The Client Port refers to valid VMID checking. Invalid VMIDs can result in CLIENT ERRORs when this error reporting is enabled.

The Configuration Port refers to valid address checking. Invalid addresses can result in DECODE ERRORs when this error reporting is enabled.

Table 3-2 shows when CLIENT ERRORs, DECODE ERRORs, and the XPU INTR are enabled based on the register configuration values.

Table 3-2 Enablements based on register configuration values

RPUERE	DCDEE	RPUEIE	CLIENT ERROR	DECODE ERROR	XPU INTR
0	X	X	0	0	0
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

Table 3-3 shows the types of transactions that will result in CLIENT or DECODE ERRORs.

It should be noted that bitwise register accesses will not trigger a CLIENT ERROR if any of the bits have the correct permissions that match the accessing VMID.

Table 3-3 Types of transactions resulting in CLIENT or DECODE ERRORs

VALID ADDRESS	SU VMID	Correct owner VMID	CLIENT ERROR	DECODE ERROR
0	X	X	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0

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TLMM_RPU_CR

Bits	Name	Description
31:4	RESERVED	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e.invalid address) are recorded as such. Do Not Record Decode errors do not set RPU_ESR[CFG]. RPU_EAR and RPU_ESYNR0 not updated. Record Decode errors set RPU_ESR[CFG]. RPU_EAR and RPU_ESYNR0 updated with address and syndrome of error. 0x0: DCDEE_DISABLE 0x1: DCDEE_ENABLE
2	RPUEIE	Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the RPU.
1	RPUERE	Error Report Enable. Causes the RPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective RPU port. Both client and configuration port errors are recorded in RPU_EAR, RPU_ESR and RPU_ESYNRn, independent of the value of RPU_CR[ERE] 0x0: ERE_DISABLE 0x1: ERE_ENABLE
0	RPUE	RPU Enable. Governs whether RPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures RPU and the MID to VMID mapping tables.

0x00800F84 TLMM_RPU_EAR

Type: Read
Clock: CC_TLMM_HCLK
Reset State: 0x0000

Error Address Register. This register captures the address upon errors detected by the RPU, for both the client port and the configuration port.

The first error is captured and held. Subsequent errors are not captured until the TLMM_RPU_ESR register is cleared.

NOTE We are capturing address bits up to 1MB of space (19:0). This is all the TLMM decodes.

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TLMM_RPU_EAR

Bits	Name	Description
19:0	PA_19_0	The physical address of the errant request.

0x00800F88 TLMM_RPU_ESR

Type: Read/Write-Clear
Clock: CC_TLMM_HCLK
Reset State: 0x0000

Error Status Register. This register captures the status upon errors detected by the RPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old. The presence of an asserted value on any bit in this register is what prompts the assertion of the RPU's interrupt output (when enabled by RPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the RPU_ESYNRn registers, which are merely the 'syndrome' of an error indicated by RPU_ESR.

TLMM_RPU_ESR

Bits	Name	Description
31	MULTIERROR	Multi-error: Indicates additional error occurred while TLMM_RPU_ESR[CFG, CLIENT] still nonzero. TLMM_RPU_EAR and TLMM_RPU_ESYNRn registers (and TLMM_RPU_ESR itself, except for the MULTI bit) 'lock' upon first error, TLMM_RPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while TLMM_RPU_ESR is non-zero are lost.
30:2	RESERVED	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x00800F8C TLMM_RPU_ESRRESTORE

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

Error Restore Register. This register is an optional address for the TLMM_RPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes

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TLMM_RPU_ESRRESTORE

Bits	Name	Description
31	MULTIERROR	Multi-error: Indicates additional error occurred while TLMM_RPU_ESR[CFG, CLIENT] still nonzero. TLMM_RPU_EAR and TLMM_RPU_ESYNRn registers (and TLMM_RPU_ESR itself, except for the MULTI bit) 'lock' upon first error, TLMM_RPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while TLMM_RPU_ESR is non-zero are lost.
30:2	RESERVED	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x00800F90 TLMM_RPU_ESYNR0

Type: Read
Clock: CC_TLMM_HCLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the RPU, for both the client port and the configuration port.

The first error is captured and held. Subsequent errors are not captured until the TLMM_RPU_ESR register is cleared.

TLMM_RPU_ESYNR0

Bits	Name	Description
31:24	RESERVED_1	ATID field of errant request. (Not supported in the TLMM)
23:21	RESERVED_2	Reserved
20:16	AVMID_4_0	AVMID field of errant request.
15:13	RESERVED_3	ABID field of errant request. (Not supported in the TLMM)
12:8	RESERVED_4	APID field of errant request. (Not supported in the TLMM)
7:0	RESERVED	AMID field of errant request. (Not supported in the TLMM)

0x00800F94 TLMM_RPU_ESYNR1

Type: Read
Clock: CC_TLMM_HCLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the RPU, for both the client port and the configuration port.

The first error is captured and held. Subsequent errors are not captured until the TLMM_RPU_ESR register is cleared.

TLMM_RPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED_1	Reserved
24	RESERVED_2	APULL field of the errant request. (Not supported in the TLMM)
23	RESERVED_3	Reserved

TLMM_RPU_ESYNR1 (cont.)

Bits	Name	Description
22	RESERVED_4	AOOO field of the errant request. (Not supported in the TLMM)
21:20	RESERVED_5	ALOCK field of the errant request. (Not supported in the TLMM)
19	RESERVED_6	Reserved
18:16	RESERVED_7	ASIZE field of errant request. (Not supported in the TLMM)
15:12	RESERVED_8	ALEN field of the errant request. (Not supported in the TLMM)
11	RESERVED_9	Reserved
10	RESERVED_10	ABURST field of errant request. (Not supported in the TLMM)
9	RESERVED_11	Reserved
8	AWRITE	AWRITE field of errant request.
7	RESERVED_12	AINST field of the errant request. (Not supported in the TLMM)
6	RESERVED_13	APROTNS field of errant request. (Not supported in the TLMM)
5	RESERVED_14	APRIV field of the errant request. (Not supported in the TLMM)
4	RESERVED_15	AINNERSHARED field of the errant request. (Not supported in the TLMM)
3	RESERVED_16	ASHARED field of the errant request. (Not supported in the TLMM)
2:0	RESERVED	AMEMTYPE field of the errant request. (Not supported in the TLMM)

0x00800FF4 TLMM_RPU_REV

Type: Read
Clock: CC_TLMM_HCLK
Reset State: 0x00000014

RPU Revision Register: This register provides major/minor revision codes for the implementation.

TLMM_RPU_REV

Bits	Name	Description
31:8	RESERVED	Reserved
7:4	MAJOR_3_0	Major variant field
3:0	MINOR_3_0	Minor variant

0x00800FF8 TLMM_RPU_IDR

Type: Read
Clock: CC_TLMM_HCLK
Reset State: 0x000208CC

RPU ID Register: Read-only register that defines various configuration attributes of the RPU instance.

TLMM_RPU_IDR

Bits	Name	Description
31:21	RESERVED_1	Reserved
20:16	LSB_4_0	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED_2	Reserved
13:12	XPUT_1_0	Indicates type of xPU (hard wired to 0b00 for RPU) 0x0: RPU 0x1: APU 0x2: MPU 0x3: Reserved
11	PT	Permission type Indicates full access vs. no access type. Only RPU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) Indicates read/write access type vs. read-only access type. For multi-VMID, separate RPU_RGn_RACR and RPU_RGn_WACR registers govern read vs. write access. For single VMID, RPU_RGn_ACR registers include separate 5-bit read/write vs. read-only 'owner' VMID fields 0x0: PT_FULL 0x1: PT_READ_WRITE
10	MV	Multi-VMID Indicates single VMID type access control. RPU_RGn_xACR registers indicate single 5 bit 'owner' VMID field for governing access. Indicates multi-VMD type access control. RPU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access. 0x0: SINGLE_MV 0x1: MULTI_MV
9:8	RESERVED	Reserved
7:0	NRG_7_0	Number of resource groups: Indicates number of resource groups (minus 1) supported by the RPU. Value can range between 0 and 255 (1-256 resource groups).

0x00800FFC TLMM_RPU_ACR

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0xFFFFFFFF

RPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the RPU (including the TLMM_RPU_ACR itself). In other words, any VMID set to ’1’ in this register has Super User access permissions.

TLMM_RPU_ACR

Bits	Name	Description
31:0	RWE_31_0	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the RPU’s 4KB address region (including the RPU_RPU_ACR itself). For single VMID type RPUs (RPU_IDR[MV] = 0) the RPU_RPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

0x00801000+0x10*n GPIO_CFGn, n=[0..89]

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_CFG[n] controls the GPIO Output Enable, HDrive, Pull and Alternate Functions. The default pull can vary for different GPIOs and can be found in the pinout spreadsheet/chapter. The default drive setting for all GPIOs is ’000’ (2 mA).

Depending on the GPIO selected, the FUNC_SEL value determines the function output. Table 3-4 summarizes the functions and the value to set to select them.

NOTE The default drive strength for all GPIO is 2 mA (DRV_STRENGTH = 000)

For all GPIO, the default GPIO_CFG[5:2] is 0, that is, the GPIO function is selected.

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
gpio[0]				(default 01 = pd)
	GPIO_IN_OUT(0)	GPIO_CFG(0)	0	
	mdp_vsync_p	mdp_vsync_p_en	1	
	vfe_camif_timer6_b	vdd_tie	2	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	dbg_ls_out_clk	vdd_tie	3	
	aux_tms	gnd_tie	aux_jtag_mode	
	atest_usb2_hsic_ulpi_data(6)	atest_usb2_hsic_ulpi_data_en(6)	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_rst	gnd_tie	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_rst	gnd_tie	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_rst	gnd_tie	atestmode_usb4_hs	
	ebi1_ch1_smt_dq(24)	ebi1_ch1_smt_dq_en(24)	ebi1_ch1_tap_smt_mode_tdr	
gpio[1]				(default 01 = pd)
	GPIO_IN_OUT(1)	GPIO_CFG(1)	0	
	mdp_vsync_s	mdp_vsync_s_en	1	
	vfe_camif_timer7_b	vdd_tie	2	
	dbg_hs_out_clk	vdd_tie	3	
	aux_tck	gnd_tie	aux_jtag_mode	
	atest_usb2_hsic_ulpi_data(5)	atest_usb2_hsic_ulpi_data_en(5)	atestmode_hsic_gnss_wlan	
	ebi1_ch1_smt_dm(1)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[2]				(default 01 = pd)
	GPIO_IN_OUT(2)	GPIO_CFG(2)	0	
	vfe_camif_timer1_a	vdd_tie	1	
	gp_mn	gp_mn_en	2	
	la_etm_extout	gnd_tie	3	
	cam_mclk2	vdd_tie	4	
	dbg_bus_out(11)	vdd_tie	5	
	boot_from_rom	gnd_tie	msmc_gpio_sense_done_n	
	tm_bus(7)	tm_bus_en(7)	tic_mode	
	ebi1_ch0_smt_dq(19)	ebi1_ch0_smt_dq_en(19)	ebi1_ch0_tap_smt_mode_tdr	
gpio[3]				(default 01 = pd)
	GPIO_IN_OUT(3)	GPIO_CFG(3)	0	
	vfe_camif_timer2	vdd_tie	1	
	gp_clk_0a	vdd_tie	2	
	dbg_bus_out(10)	vdd_tie	3	
	adsp_etm_tracedata_b(15)	vdd_tie	4	
	qdss_tracedata_b(15)	vdd_tie	5	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	a9_riva_etm_tracepkt_b(15)	vdd_tie	6	
	wdog_disable	gnd_tie	msmc_gpio_sense_done_n	
	tm_bus(8)	tm_bus_en(8)	tic_mode	
	ebi1_ch0_smt_dq(18)	ebi1_ch0_smt_dq_en(18)	ebi1_ch0_tap_smt_mode_tdr	
gpio[4]				(default 01 = pd)
	GPIO_IN_OUT(4)	GPIO_CFG(4)	0	
	vfe_camif_timer3_a	vdd_tie	1	
	cam_mclk1	vdd_tie	2	
	gp_clk_1a	vdd_tie	3	
	boot_config(6)	gnd_tie	msmc_gpio_sense_done_n	
	tm_bus(9)	tm_bus_en(9)	tic_mode	
	ebi1_ch0_smt_dq(17)	ebi1_ch0_smt_dq_en(17)	ebi1_ch0_tap_smt_mode_tdr	
gpio[5]				(default 01 = pd)
	GPIO_IN_OUT(5)	GPIO_CFG(5)	0	
	cam_mclk0	vdd_tie	1	
	pmb_clk_ur	vdd_tie	2	
	boot_config(5)	gnd_tie	msmc_gpio_sense_done_n	
	tm_bus(12)	tm_bus_en(12)	tic_mode	
	ebi1_ch0_smt_dq(16)	ebi1_ch0_smt_dq_en(16)	ebi1_ch0_tap_smt_mode_tdr	
gpio[6]				(default 01 = pd)
	GPIO_IN_OUT(6)	GPIO_CFG(6)	0	
	gsbi3(3)	gsbi3_en(3)	1	
	ssbi_ts	ssbi_ts_en	2	
	vfe_camif_timer4_c	vdd_tie	3	
	dr_sync	vdd_tie	4	
	gps_pps_in	gnd_tie	5	
	gsbi1_spi_cs2a_n	gsbi1_spi_cs2a_n_en	6	
	riva_wcn_priority_a	vdd_tie	7	
	tm_bus(10)	tm_bus_en(10)	tic_mode	
	ebi1_ch0_smt_dq(9)	ebi1_ch0_smt_dq_en(9)	ebi1_ch0_tap_smt_mode_tdr	
gpio[7]				(default 01 = pd)

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	GPIO_IN_OUT(7)	GPIO_CFG(7)	0	
	gsbi3(2)	gsbi3_en(2)	1	
	ts_eoc	gnd_tie	2	
	gsbi1_spi_cs1a_n	gsbi1_spi_cs1a_n_en	3	
	gsbi1_spi_cs3b_n	gsbi1_spi_cs3b_n_en	4	
	adsp_etm_tracedata_b(14)	vdd_tie	5	
	qdss_tracedata_b(14)	vdd_tie	6	
	a9_riva_etm_tracepkt_b(14)	vdd_tie	7	
	tm_bus(23)	tm_bus_en(23)	tic_mode	
	ebi1_ch0_smt_dq(8)	ebi1_ch0_smt_dq_en(8)	ebi1_ch0_tap_smt_mode_tdr	
gpio[8]				(default 01 = pd)
	GPIO_IN_OUT(8)	GPIO_CFG(8)	0	
	gsbi3(1)	gsbi3_en(1)	1	
	rpm_wdog_stb	vdd_tie	2	
	pmb_ext_ctrl(1)	gnd_tie	3	
	tm_bus(24)	tm_bus_en(24)	tic_mode	
	ebi1_ch0_smt_dm(0)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
gpio[9]				(default 01 = pd)
	GPIO_IN_OUT(9)	GPIO_CFG(9)	0	
	gsbi3(0)	gsbi3_en(0)	1	
	pmb_ext_ctrl(0)	gnd_tie	2	
	tm_clk	gnd_tie	tic_clk_en	
	ebi1_ch0_smt_dqs(0)	ebi1_ch0_smt_dqs_en(0)	ebi1_ch0_tap_smt_mode_tdr	
gpio[10]				(default 01 = pd)
	GPIO_IN_OUT(10)	GPIO_CFG(10)	0	
	gsbi4(3)	gsbi4_en(3)	1	
	gsbi1_spi_cs1b_n	gsbi1_spi_cs1b_n_en	2	
	vfe_camif_timer6_c	vdd_tie	3	
	ebi1_ch0_drive_prpg	gnd_tie	4	
	adsp_etm_tracectl	vdd_tie	5	
	qdss_tracectl	vdd_tie	6	
	a9_riva_etm_pipestat(1)	vdd_tie	7	
	riva_dbg_bus(11)	vdd_tie	8	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	gsbi4_3d_cam_i2c_sda_l	gsbi4_3d_cam_i2c_sda_l_en	9	
	tm_req_b	gnd_tie	tic_mode	
	ebi1_ch0_smt_dq(7)	ebi1_ch0_smt_dq_en(7)	ebi1_ch0_tap_smt_mode_tdr	
gpio[11]				(default 01 = pd)
	GPIO_IN_OUT(11)	GPIO_CFG(11)	0	
	gsbi4(2)	gsbi4_en(2)	1	
	gsbi1_spi_cs2b_n	gsbi1_spi_cs2b_n_en	2	
	vfe_camif_timer7_c	vdd_tie	3	
	mdp_vsync_e	mdp_vsync_e_en	4	
	ebi1_ch1_drive_prpg	gnd_tie	5	
	adsp_etm_traceclk	vdd_tie	6	
	qdss_traceclk	vdd_tie	7	
	a9_riva_etm_traceclk	vdd_tie	8	
	riva_dbg_bus(10)	vdd_tie	9	
	gsbi4_3d_cam_i2c_scl_l	gsbi4_3d_cam_i2c_scl_l_en	10	
	tm_ack	vdd_tie	tic_mode	
	ebi1_ch0_smt_dq(6)	ebi1_ch0_smt_dq_en(6)	ebi1_ch0_tap_smt_mode_tdr	
gpio[12]				(default 01 = pd)
	GPIO_IN_OUT(12)	GPIO_CFG(12)	0	
	gsbi4(1)	gsbi4_en(1)	1	
	prng_rosc_test_out	vdd_tie	2	
	adsp_etm_tracedata(0)	vdd_tie	3	
	qdss_tracedata(0)	vdd_tie	4	
	a9_riva_etm_pipestat(0)	vdd_tie	5	
	gsbi4_3d_cam_i2c_sda_r	gsbi4_3d_cam_i2c_sda_r_en	6	
	tm_bus(3)	tm_bus_en(3)	tic_mode	
	ebi1_ch0_smt_dq(5)	ebi1_ch0_smt_dq_en(5)	ebi1_ch0_tap_smt_mode_tdr	
gpio[13]				(default 01 = pd)
	GPIO_IN_OUT(13)	GPIO_CFG(13)	0	
	gsbi4(0)	gsbi4_en(0)	1	
	ring_osc_clk	vdd_tie	2	
	adsp_etm_tracedata(1)	vdd_tie	3	
	qdss_tracedata_a(1)	vdd_tie	4	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	a9_riva_etm_tracepkt(1)	vdd_tie	5	
	gsbi4_3d_cam_i2c_scl_r	gsbi4_3d_cam_i2c_scl_r_en	6	
	tm_bus(4)	tm_bus_en(4)	tic_mode	
	ebi1_ch0_smt_dq(4)	ebi1_ch0_smt_dq_en(4)	ebi1_ch0_tap_smt_mode_tdr	
gpio[14]				(default 01 = pd)
	GPIO_IN_OUT(14)	GPIO_CFG(14)	0	
	riva_fm_ssbi	riva_fm_ssbi_en	1	
	gsbi6(3)	gsbi6_en(3)	2	
	adsp_etm_tracedata_a(15)	vdd_tie	3	
	qdss_tracedata_a(15)	vdd_tie	4	
	a9_riva_etm_tracepkt_a(15)	vdd_tie	5	
	aux_rtck	vdd_tie	aux_jtag_mode	
	atest_usb2_hsic_ulpi_data(4)	atest_usb2_hsic_ulpi_data_en(4)	atestmode_hsic_gnss_wlan	
	ebi1_ch1_smt_dqs(1)	ebi1_ch1_smt_dqs_en(1)	ebi1_ch1_tap_smt_mode_tdr	
gpio[15]				(default 01 = pd)
	GPIO_IN_OUT(15)	GPIO_CFG(15)	0	
	riva_fm_sdi	riva_fm_sdi_en	1	
	gsbi6(2)	gsbi6_en(2)	2	
	adsp_etm_tracedata_a(14)	vdd_tie	3	
	qdss_tracedata_a(14)	vdd_tie	4	
	a9_riva_etm_tracepkt_a(14)	vdd_tie	5	
	aux_tdo	aux_tdo_en	aux_jtag_mode	
	atest_usb2_hsic_ulpi_data(3)	atest_usb2_hsic_ulpi_data_en(3)	atestmode_hsic_gnss_wlan	
	ebi1_ch1_smt_dq(15)	ebi1_ch1_smt_dq_en(15)	ebi1_ch1_tap_smt_mode_tdr	
gpio[16]				(default 01 = pd)
	GPIO_IN_OUT(16)	GPIO_CFG(16)	0	
	riva_bt_ctl	vdd_tie	1	
	gsbi6(1)	gsbi6_en(1)	2	
	sdc1_cdc_dtest_out(1)	vdd_tie	3	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	adsp_etm_tracedata_a(13)	vdd_tie	4	
	qdss_tracedata_a(13)	vdd_tie	5	
	a9_riva_etm_tracepkt_a(13)	vdd_tie	6	
	aux_tdi	gnd_tie	aux_jtag_mode	
	atest_usb2_hsic_ulpi_data(2)	atest_usb2_hsic_ulpi_data_en(2)	atestmode_hsic_gnss_wlan	
	ebi1_ch1_smt_dq(14)	ebi1_ch1_smt_dq_en(14)	ebi1_ch1_tap_smt_mode_tdr	
gpio[17]				(default 01 = pd)
	GPIO_IN_OUT(17)	GPIO_CFG(17)	0	
	riva_bt_dat_stb	riva_bt_dat_stb_en	1	
	gsbi6(0)	gsbi6_en(0)	2	
	sdc1_cdc_dtest_out(0)	vdd_tie	3	
	sc_l2_pll_droop_test_se1	vdd_tie	4	
	adsp_etm_tracedata_a(12)	vdd_tie	5	
	qdss_tracedata_a(12)	vdd_tie	6	
	a9_riva_etm_tracepkt_a(12)	vdd_tie	7	
	aux_trst_n	gnd_tie	aux_jtag_mode	
	atest_usb2_hsic_ulpi_data(1)	atest_usb2_hsic_ulpi_data_en(1)	atestmode_hsic_gnss_wlan	
	ebi1_ch1_smt_dq(13)	ebi1_ch1_smt_dq_en(13)	ebi1_ch1_tap_smt_mode_tdr	
gpio[18]				(default 01 = pd)
	GPIO_IN_OUT(18)	GPIO_CFG(18)	0	
	gsbi1(3)	gsbi1_en(3)	1	
	gp_pdm_0b	gp_pdm_0b_en	2	
	vfe_camif_timer1_b	vdd_tie	3	
	dbg_bus_in(3)	gnd_tie	4	
	dbg_bus_out(19)	vdd_tie	5	
	adsp_etm_tracedata(5)	vdd_tie	6	
	qdss_tracedata(5)	vdd_tie	7	
	a9_riva_etm_tracepkt(5)	vdd_tie	8	
	riva_dbg_bus(19)	vdd_tie	9	
	tm_bus(27)	tm_bus_en(27)	tic_mode	
	ebi1_ch0_smt_dq(2)	ebi1_ch0_smt_dq_en(2)	ebi1_ch0_tap_smt_mode_tdr	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
gpio[19]				(default 01 = pd)
	GPIO_IN_OUT(19)	GPIO_CFG(19)	0	
	gsbi1(2)	gsbi1_en(2)	1	
	vfe_camif_timer5_b	vdd_tie	2	
	dbg_bus_in(2)	gnd_tie	3	
	dbg_bus_out(18)	vdd_tie	4	
	adsp_etm_tracedata(4)	vdd_tie	5	
	qdss_tracedata(4)	vdd_tie	6	
	a9_riva_etm_tracepkt(4)	vdd_tie	7	
	riva_dbg_bus(18)	vdd_tie	8	
	tm_bus(28)	tm_bus_en(28)	tic_mode	
	ebi1_ch0_smt_dq(1)	ebi1_ch0_smt_dq_en(1)	ebi1_ch0_tap_smt_mode_tdr	
gpio[20]				(default 01 = pd)
	GPIO_IN_OUT(20)	GPIO_CFG(20)	0	
	gsbi1(1)	gsbi1_en(1)	1	
	dbg_bus_in(1)	gnd_tie	2	
	dbg_bus_out(17)	vdd_tie	3	
	adsp_etm_tracedata(3)	vdd_tie	4	
	qdss_tracedata_a(3)	vdd_tie	5	
	a9_riva_etm_tracepkt(3)	vdd_tie	6	
	riva_dbg_bus(17)	vdd_tie	7	
	tm_bus(19)	tm_bus_en(19)	tic_mode	
	ebi1_ch0_smt_dq(0)	ebi1_ch0_smt_dq_en(0)	ebi1_ch0_tap_smt_mode_tdr	
gpio[21]				(default 01 = pd)
	GPIO_IN_OUT(21)	GPIO_CFG(21)	0	
	gsbi1(0)	gsbi1_en(0)	1	
	dbg_bus_in(0)	gnd_tie	2	
	dbg_bus_out(16)	vdd_tie	3	
	adsp_etm_tracedata(2)	vdd_tie	4	
	qdss_tracedata_a(2)	vdd_tie	5	
	a9_riva_etm_tracepkt(2)	vdd_tie	6	
	riva_dbg_bus(16)	vdd_tie	7	
	tm_bus(20)	tm_bus_en(20)	tic_mode	
	ebi1_ch0_smt_dm(2)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
gpio[22]				(default 01 = pd)

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	GPIO_IN_OUT(22)	GPIO_CFG(22)	0	
	gsbi2(3)	gsbi2_en(3)	1	
	gp_pdm_1a	gp_pdm_1a_en	2	
	tm_bus(21)	tm_bus_en(21)	tic_mode	
	ebi1_ch0_smt_dqs(2)	ebi1_ch0_smt_dqs_en(2)	ebi1_ch0_tap_smt_mode_tdr	
gpio[23]				(default 01 = pd)
	GPIO_IN_OUT(23)	GPIO_CFG(23)	0	
	gsbi2(2)	gsbi2_en(2)	1	
	adsp_ext_vfr_irq	gnd_tie	2	
	tm_bus(22)	tm_bus_en(22)	tic_mode	
	ebi1_ch0_smt_dq(23)	ebi1_ch0_smt_dq_en(23)	ebi1_ch0_tap_smt_mode_tdr	
gpio[24]				(default 01 = pd)
	GPIO_IN_OUT(24)	GPIO_CFG(24)	0	
	gsbi2(1)	gsbi2_en(1)	1	
	tm_bus(5)	tm_bus_en(5)	tic_mode	
	ebi1_ch0_smt_dq(22)	ebi1_ch0_smt_dq_en(22)	ebi1_ch0_tap_smt_mode_tdr	
gpio[25]				(default 01 = pd)
	GPIO_IN_OUT(25)	GPIO_CFG(25)	0	
	gsbi2(0)	gsbi2_en(0)	1	
	gp_clk_2b	vdd_tie	2	
	tm_bus(6)	tm_bus_en(6)	tic_mode	
	ebi1_ch0_smt_dq(21)	ebi1_ch0_smt_dq_en(21)	ebi1_ch0_tap_smt_mode_tdr	
gpio[26]				(default 11 = pu)
	GPIO_IN_OUT(26)	GPIO_CFG(26)	0	
	tm_bus(26)	tm_bus_en(26)	tic_mode	
	ebi1_ch0_smt_dq(3)	ebi1_ch0_smt_dq_en(3)	ebi1_ch0_tap_smt_mode_tdr	
gpio[27]				(default 01 = pd)
	GPIO_IN_OUT(27)	GPIO_CFG(27)	0	
	mi2s_ws	mi2s_ws_en	1	
	dbg_bus_in(7)	gnd_tie	2	
	dbg_bus_out(23)	vdd_tie	3	
	riva_dbg_bus(23)	vdd_tie	4	
	test_pcie_pipe_tx_data(3)	vdd_tie	5	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	test_pcie_pipe_rx_data(3)	vdd_tie	6	
	atest_gpsadc_yi(4)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_testdataout0(2)	vdd_tie	atestmode_usb1_hs	
	atest_usb3_hs_testdataout0(2)	vdd_tie	atestmode_usb3_hs	
	atest_usb4_hs_testdataout0(2)	vdd_tie	atestmode_usb4_hs	
	ebi1_ch0_smt_ca(5)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_ca(5)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[28]				(default 01 = pd)
	GPIO_IN_OUT(28)	GPIO_CFG(28)	0	
	mi2s_sclk	mi2s_sclk_en	1	
	dbg_bus_in(6)	gnd_tie	2	
	dbg_bus_out(22)	vdd_tie	3	
	riva_dbg_bus(22)	vdd_tie	4	
	test_pcie_pipe_tx_data(4)	vdd_tie	5	
	test_pcie_pipe_rx_data(4)	vdd_tie	6	
	hdmi_dtest_out	vdd_tie	7	
	atest_gpsadc_yi(3)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_testdataout0(1)	vdd_tie	atestmode_usb1_hs	
	atest_usb3_hs_testdataout0(1)	vdd_tie	atestmode_usb3_hs	
	atest_usb4_hs_testdataout0(1)	vdd_tie	atestmode_usb4_hs	
	ebi1_ch0_smt_ca(6)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_ca(6)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[29]				(default 01 = pd)
	GPIO_IN_OUT(29)	GPIO_CFG(29)	0	
	mi2s_fm_data_sd3	mi2s_fm_data_sd3_en	1	
	dbg_bus_in(5)	gnd_tie	2	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	dbg_bus_out(21)	vdd_tie	3	
	riva_dbg_bus(21)	vdd_tie	4	
	test_pcie_pipe_tx_data(5)	vdd_tie	5	
	test_pcie_pipe_rx_data(5)	vdd_tie	6	
	hdmi_lbk_data(9)	vdd_tie	7	
	atest_ate_gps_data_clk	gnd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_testdataout0(0)	vdd_tie	atestmode_usb1_hs	
	atest_usb3_hs_testdataout0(0)	vdd_tie	atestmode_usb3_hs	
	atest_usb4_hs_testdataout0(0)	vdd_tie	atestmode_usb4_hs	
	ebi1_ch0_smt_ca(7)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_ca(7)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[30]				(default 01 = pd)
	GPIO_IN_OUT(30)	GPIO_CFG(30)	0	
	mi2s_data_sd2	mi2s_data_sd2_en	1	
	slimbus1_data_b	slimbus1_data_b_en	2	
	gsbi5_spi_cs1a_n	gsbi5_spi_cs1a_n_en	3	
	gsbi6_spi_cs1a_n	gsbi6_spi_cs1a_n_en	4	
	gsbi7_spi_cs1a_n	gsbi7_spi_cs1a_n_en	5	
	test_pcie_pipe_tx_data(6)	vdd_tie	6	
	test_pcie_pipe_rx_data(6)	vdd_tie	7	
	hdmi_lbk_data(8)	vdd_tie	8	
	atest_gpsadc_yi(2)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_id0	vdd_tie	atestmode_usb1_hs	
	atest_usb3_hs_id0	vdd_tie	atestmode_usb3_hs	
	atest_usb4_hs_id0	vdd_tie	atestmode_usb4_hs	
	ebi1_ch0_smt_ca(8)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_ca(8)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[31]				(default 01 = pd)

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	GPIO_IN_OUT(31)	GPIO_CFG(31)	0	
	mi2s_data_sd1	mi2s_data_sd1_en	1	
	slimbus1_clk_b	slimbus1_clk_b_en	2	
	gsbi5_spi_cs2a_n	gsbi5_spi_cs2a_n_en	3	
	gsbi6_spi_cs2a_n	gsbi6_spi_cs2a_n_en	4	
	gsbi7_spi_cs2a_n	gsbi7_spi_cs2a_n_en	5	
	test_pcie_pipe_tx_data(7)	vdd_tie	6	
	test_pcie_pipe_rx_data(7)	vdd_tie	7	
	hdmi_lbk_data(7)	vdd_tie	8	
	atest_gpsadc_yi(1)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_otgsessvld0	vdd_tie	atestmode_usb1_hs	
	atest_usb3_hs_otgsessvld0	vdd_tie	atestmode_usb3_hs	
	atest_usb4_hs_otgsessvld0	vdd_tie	atestmode_usb4_hs	
	ebi1_ch0_smt_ca(9)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_ca(9)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[32]				(default 01 = pd)
	GPIO_IN_OUT(32)	GPIO_CFG(32)	0	
	mi2s_data_sd0	mi2s_data_sd0_en	1	
	gp_clk_2a	vdd_tie	2	
	dbg_bus_in(4)	gnd_tie	3	
	dbg_bus_out(20)	vdd_tie	4	
	riva_dbg_bus(20)	vdd_tie	5	
	gsbi5_spi_cs3a_n	gsbi5_spi_cs3a_n_en	6	
	gsbi6_spi_cs3a_n	gsbi6_spi_cs3a_n_en	7	
	gsbi7_spi_cs3a_n	gsbi7_spi_cs3a_n_en	8	
	test_pcie_pipe_tx_data(8)	vdd_tie	9	
	test_pcie_pipe_rx_data(8)	vdd_tie	10	
	atest_rfa_gps_clk	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_dat(7)	atest_usb1_hs_ulpi_dat_en(7)	atestmode_usb1_hs	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	atest_usb3_hs_ulpi_dat(7)	atest_usb3_hs_ulpi_dat_en(7)	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_dat(7)	atest_usb4_hs_ulpi_dat_en(7)	atestmode_usb4_hs	
gpio[33]				(default 01 = pd)
	GPIO_IN_OUT(33)	GPIO_CFG(33)	0	
	mi2s_mclk	vdd_tie	1	
	gp_pdm_2b	gp_pdm_2b_en	2	
	dbg_bus_out(15)	vdd_tie	3	
	riva_dbg_bus(15)	vdd_tie	4	
	test_pcie_pipe_tx_data(9)	vdd_tie	5	
	test_pcie_pipe_rx_data(9)	vdd_tie	6	
	hdmi_lbk_data(6)	vdd_tie	7	
	boot_config(4)	gnd_tie	msmc_gpio_sense_done_n	
	atest_gpsadc_yi(0)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_dat(6)	atest_usb1_hs_ulpi_dat_en(6)	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_dat(6)	atest_usb3_hs_ulpi_dat_en(6)	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_dat(6)	atest_usb4_hs_ulpi_dat_en(6)	atestmode_usb4_hs	
	ebi1_ch0_smt_oe_dq	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_oe_dq	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[34]				(default 01 = pd)
	GPIO_IN_OUT(34)	GPIO_CFG(34)	0	
	codec_mic_i2s_mclk	vdd_tie	1	
	gp_clk_0b	vdd_tie	2	
	sc_l2_pll_droop_test_se2	vdd_tie	3	
	dbg_bus_out(14)	vdd_tie	4	
	riva_dbg_bus(14)	vdd_tie	5	
	boot_config(3)	gnd_tie	msmc_gpio_sense_done_n	
	atest_usb2_hsic_clk	gnd_tie	atestmode_hsic_gnss_wlan	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	ebi1_ch1_smt_dq(12)	ebi1_ch1_smt_dq_en(12)	ebi1_ch1_tap_smt_mode_tdr	
gpio[35]				(default 01 = pd)
	GPIO_IN_OUT(35)	GPIO_CFG(35)	0	
	codec_mic_i2s_sck	codec_mic_i2s_sck_en	1	
	scpll0_droop_test_se1	vdd_tie	2	
	dbg_bus_in(15)	gnd_tie	3	
	dbg_bus_out(31)	vdd_tie	4	
	riva_dbg_bus(31)	vdd_tie	5	
	atest_usb2_hsic_ulpi_clk	gnd_tie	atestmode_hsic_gnss_wlan	
	ebi1_ch1_smt_dq(11)	ebi1_ch1_smt_dq_en(11)	ebi1_ch1_tap_smt_mode_tdr	
gpio[36]				(default 01 = pd)
	GPIO_IN_OUT(36)	GPIO_CFG(36)	0	
	codec_mic_i2s_ws	codec_mic_i2s_ws_en	1	
	gsbi1_spi_cs1c_n	gsbi1_spi_cs1c_n_en	2	
	usb_fs1_oe_b	vdd_tie	3	
	usb_fs1_oe_b_n	vdd_tie	4	
	scpll0_droop_test_se2	vdd_tie	5	
	dbg_bus_in(14)	gnd_tie	6	
	dbg_bus_out(30)	vdd_tie	7	
	riva_dbg_bus(30)	vdd_tie	8	
	atest_usb2_hsic_ulpi_data(0)	atest_usb2_hsic_ulpi_data_en(0)	atestmode_hsic_gnss_wlan	
	ebi1_ch1_smt_dq(10)	ebi1_ch1_smt_dq_en(10)	ebi1_ch1_tap_smt_mode_tdr	
gpio[37]				(default 01 = pd)
	GPIO_IN_OUT(37)	GPIO_CFG(37)	0	
	codec_mic_i2s_din0	gnd_tie	1	
	usb_fs1_dat_b	usb_fs1_dat_b_en	2	
	scpll1_droop_test_se1	vdd_tie	3	
	dbg_bus_in(13)	gnd_tie	4	
	dbg_bus_out(29)	vdd_tie	5	
	riva_dbg_bus(29)	vdd_tie	6	
	atest_usb2_hsic_ulpi_dir	vdd_tie	atestmode_hsic_gnss_wlan	
	ebi1_ch1_smt_dq(9)	ebi1_ch1_smt_dq_en(9)	ebi1_ch1_tap_smt_mode_tdr	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
gpio[38]				(default 01 = pd)
	GPIO_IN_OUT(38)	GPIO_CFG(38)	0	
	codec_mic_i2s_din1	gnd_tie	1	
	gp_pdm_0a	gp_pdm_0a_en	2	
	usb_fs1_se0_b	usb_fs1_se0_b_en	3	
	scpll1_droop_test_se2	vdd_tie	4	
	dbg_bus_in(12)	gnd_tie	5	
	dbg_bus_out(28)	vdd_tie	6	
	riva_dbg_bus(28)	vdd_tie	7	
	atest_usb2_hsic_ulpi_stp	gnd_tie	atestmode_hsic_gnss_wlan	
	ebi1_ch1_smt_dq(8)	ebi1_ch1_smt_dq_en(8)	ebi1_ch1_tap_smt_mode_tdr	
gpio[39]				(default 01 = pd)
	GPIO_IN_OUT(39)	GPIO_CFG(39)	0	
	codec_spkr_i2s_mclk	vdd_tie	1	
	test_pcie_pipe_tx_data(10)	vdd_tie	2	
	test_pcie_pipe_rx_data(10)	vdd_tie	3	
	hdmi_lbk_data(5)	vdd_tie	4	
	boot_config(2)	gnd_tie	msmc_gpio_sense_done_n	
	atest_gpsadc_yq(5)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_dat(5)	atest_usb1_hs_ulpi_dat_en(5)	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_dat(5)	atest_usb3_hs_ulpi_dat_en(5)	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_dat(5)	atest_usb4_hs_ulpi_dat_en(5)	atestmode_usb4_hs	
	ebi1_ch0_smt_ie_dq	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_ie_dq	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[40]				(default 01 = pd)
	GPIO_IN_OUT(40)	GPIO_CFG(40)	0	
	slimbus1_clk_a	slimbus1_clk_a_en	1	
	codec_spkr_i2s_sck	codec_spkr_i2s_sck_en	2	
	a9_riva_etm_tracesync_b	vdd_tie	3	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	test_pcie_pipe_pclk	vdd_tie	4	
	hdmi_pixel_clk	vdd_tie	5	
	atest_gpsadc_yq(4)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_utmi_clkin	gnd_tie	atestmode_usb1_hs	
	atest_usb3_hs_utmi_clkin	gnd_tie	atestmode_usb3_hs	
	atest_usb4_hs_utmi_clkin	gnd_tie	atestmode_usb4_hs	
	ebi1_ch0_smt_hiz	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_hiz	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[41]				(default 01 = pd)
	GPIO_IN_OUT(41)	GPIO_CFG(41)	0	
	slimbus1_data_a	slimbus1_data_a_en	1	
	codec_spkr_i2s_dout	vdd_tie	2	
	a9_riva_etm_pipestat_b(2)	vdd_tie	3	
	test_pcie_pipe_tx_data(11)	vdd_tie	4	
	test_pcie_pipe_rx_data(11)	vdd_tie	5	
	hdmi_rcv_det	vdd_tie	6	
	atest_gpsadc_yq(3)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_dat(4)	atest_usb1_hs_ulpi_dat_en(4)	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_dat(4)	atest_usb3_hs_ulpi_dat_en(4)	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_dat(4)	atest_usb4_hs_ulpi_dat_en(4)	atestmode_usb4_hs	
	ebi1_ch1_smt_dm(3)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[42]				(default 01 = pd)
	GPIO_IN_OUT(42)	GPIO_CFG(42)	0	
	codec_spkr_i2s_ws	codec_spkr_i2s_ws_en	1	
	a9_riva_etm_pipestat_b(1)	vdd_tie	2	
	test_pcie_pipe_tx_data(12)	vdd_tie	3	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	test_pcie_pipe_rx_data(12)	vdd_tie	4	
	hdmi_lbk_data(4)	vdd_tie	5	
	atest_gpsadc_yq(2)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_dat(3)	atest_usb1_hs_ulpi_dat_en(3)	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_dat(3)	atest_usb3_hs_ulpi_dat_en(3)	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_dat(3)	atest_usb4_hs_ulpi_dat_en(3)	atestmode_usb4_hs	
	ebi1_ch1_smt_dqs(3)	ebi1_ch1_smt_dqs_en(3)	ebi1_ch1_tap_smt_mode_tdr	
gpio[43]				(default 01 = pd)
	GPIO_IN_OUT(43)	GPIO_CFG(43)	0	
	audio_pcm_dout	audio_pcm_dout_en	1	
	dbg_bus_in(11)	gnd_tie	2	
	dbg_bus_out(27)	vdd_tie	3	
	a9_riva_etm_pipestat_b(0)	vdd_tie	4	
	riva_dbg_bus(27)	vdd_tie	5	
	test_pcie_phy_pipe_phystatus	vdd_tie	6	
	atest_wlan_adc_core_sel	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_por	gnd_tie	atestmode_usb1_hs	
	atest_usb3_hs_por	gnd_tie	atestmode_usb3_hs	
	atest_usb4_hs_por	gnd_tie	atestmode_usb4_hs	
	ebi1_ch0_smt_cs_n(1)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_cs_n(1)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[44]				(default 01 = pd)
	GPIO_IN_OUT(44)	GPIO_CFG(44)	0	
	audio_pcm_din	gnd_tie	1	
	gp_pdm_1b	gp_pdm_1b_en	2	
	dbg_bus_in(10)	gnd_tie	3	
	dbg_bus_out(26)	vdd_tie	4	
	a9_riva_etm_pipestat(2)	vdd_tie	5	
	riva_dbg_bus(26)	vdd_tie	6	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	test_pcie_pipe_tx_data(0)	vdd_tie	7	
	test_pcie_pipe_rx_data(0)	vdd_tie	8	
	atest_wlan_adc_dtestout(0)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_retenablen	gnd_tie	atestmode_usb1_hs	
	atest_usb3_hs_retenablen	gnd_tie	atestmode_usb3_hs	
	atest_usb4_hs_retenablen	gnd_tie	atestmode_usb4_hs	
	ebi1_ch0_smt_cke(0)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_cke(0)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[45]				(default 01 = pd)
	GPIO_IN_OUT(45)	GPIO_CFG(45)	0	
	audio_pcm_sync	audio_pcm_sync_en	1	
	vfe_camif_timer4_a	vdd_tie	2	
	dbg_bus_in(9)	gnd_tie	3	
	dbg_bus_out(25)	vdd_tie	4	
	a9_riva_etm_tracesync	vdd_tie	5	
	riva_dbg_bus(25)	vdd_tie	6	
	test_pcie_pipe_tx_data(1)	vdd_tie	7	
	test_pcie_pipe_rx_data(1)	vdd_tie	8	
	atest_wlan_adc_dtestout(1)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_utmi_clkin_sel	gnd_tie	atestmode_usb1_hs	
	atest_usb3_hs_utmi_clkin_sel	gnd_tie	atestmode_usb3_hs	
	atest_usb4_hs_utmi_clkin_sel	gnd_tie	atestmode_usb4_hs	
	ebi1_ch0_smt_cke(1)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_cke(1)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[46]				(default 01 = pd)
	GPIO_IN_OUT(46)	GPIO_CFG(46)	0	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	audio_pcm_clk	audio_pcm_clk_en	1	
	vfe_camif_timer5_a	vdd_tie	2	
	dbg_bus_in(8)	gnd_tie	3	
	dbg_bus_out(24)	vdd_tie	4	
	a9_riva_etm_tracepkt(0)	vdd_tie	5	
	riva_dbg_bus(24)	vdd_tie	6	
	test_pcie_pipe_tx_data(2)	vdd_tie	7	
	test_pcie_pipe_rx_data(2)	vdd_tie	8	
	atest_gpsadc_yi(5)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_testdataout0(3)	vdd_tie	atestmode_usb1_hs	
	atest_usb3_hs_testdataout0(3)	vdd_tie	atestmode_usb3_hs	
	atest_usb4_hs_testdataout0(3)	vdd_tie	atestmode_usb4_hs	
	ebi1_ch0_smt_ck	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_ck	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[47]				(default 01 = pd)
	GPIO_IN_OUT(47)	GPIO_CFG(47)	0	
	spkr_i2s_sck	spkr_i2s_sck_en	1	
	vfe_camif_timer7_a	vdd_tie	2	
	gsbi5_spi_cs1b_n	gsbi5_spi_cs1b_n_en	3	
	gsbi6_spi_cs1b_n	gsbi6_spi_cs1b_n_en	4	
	gsbi7_spi_cs1b_n	gsbi7_spi_cs1b_n_en	5	
	riva_wcn_priority_c	vdd_tie	6	
	test_pcie_pipe_tx_data(13)	vdd_tie	7	
	test_pcie_pipe_rx_data(13)	vdd_tie	8	
	hdmi_lbk_data(3)	vdd_tie	9	
	atest_gpsadc_yq(1)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_clk	vdd_tie	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_clk	vdd_tie	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_clk	vdd_tie	atestmode_usb4_hs	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	ebi1_ch1_smt_dq(31)	ebi1_ch1_smt_dq_en(31)	ebi1_ch1_tap_smt_mode_tdr	
gpio[48]				(default 01 = pd)
	GPIO_IN_OUT(48)	GPIO_CFG(48)	0	
	spkr_i2s_ws	spkr_i2s_ws_en	1	
	gsbi1_spi_cs2c_n	gsbi1_spi_cs2c_n_en	2	
	gsbi5_spi_cs2b_n	gsbi5_spi_cs2b_n_en	3	
	gsbi6_spi_cs2b_n	gsbi6_spi_cs2b_n_en	4	
	gsbi7_spi_cs2b_n	gsbi7_spi_cs2b_n_en	5	
	mdm_lte_frame_sync_c	gnd_tie	6	
	test_pcie_pipe_tx_data(14)	vdd_tie	7	
	test_pcie_pipe_rx_data(14)	vdd_tie	8	
	hdmi_lbk_data(2)	vdd_tie	9	
	atest_gpsadc_yq(0)	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_dat(2)	atest_usb1_hs_ulpi_dat_en(2)	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_dat(2)	atest_usb3_hs_ulpi_dat_en(2)	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_dat(2)	atest_usb4_hs_ulpi_dat_en(2)	atestmode_usb4_hs	
	ebi1_ch1_smt_dq(30)	ebi1_ch1_smt_dq_en(30)	ebi1_ch1_tap_smt_mode_tdr	
gpio[49]				(default 01 = pd)
	GPIO_IN_OUT(49)	GPIO_CFG(49)	0	
	spkr_i2s_dout	vdd_tie	1	
	gp_pdm_2a	gp_pdm_2a_en	2	
	adsp_etm_tracedata_a(11)	vdd_tie	3	
	qdss_tracedata_a(11)	vdd_tie	4	
	a9_riva_etm_tracepkt_a(11)	vdd_tie	5	
	gsbi5_spi_cs3b_n	gsbi5_spi_cs3b_n_en	6	
	gsbi6_spi_cs3b_n	gsbi6_spi_cs3b_n_en	7	
	gsbi7_spi_cs3b_n	gsbi7_spi_cs3b_n_en	8	
	mdm_lte_active_c	gnd_tie	9	
	atest_dac_bist_trig	gnd_tie	atestmode_hsic_gnss_wlan	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	atest_usb1_hs_ulpi_dat(1)	atest_usb1_hs_ulpi_dat_en(1)	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_dat(1)	atest_usb3_hs_ulpi_dat_en(1)	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_dat(1)	atest_usb4_hs_ulpi_dat_en(1)	atestmode_usb4_hs	
	ebi1_ch1_smt_dq(29)	ebi1_ch1_smt_dq_en(29)	ebi1_ch1_tap_smt_mode_tdr	
gpio[50]				(default 01 = pd)
	GPIO_IN_OUT(50)	GPIO_CFG(50)	0	
	spkr_i2s_mclk	vdd_tie	1	
	gp_clk_1b	vdd_tie	2	
	adsp_etm_tracedata_a(10)	vdd_tie	3	
	qdss_tracedata_a(10)	vdd_tie	4	
	a9_riva_etm_tracepkt_a(10)	vdd_tie	5	
	test_pcie_pipe_tx_data(15)	vdd_tie	6	
	test_pcie_pipe_rx_data(15)	vdd_tie	7	
	hdmi_lbk_data(1)	vdd_tie	8	
	boot_config(1)	gnd_tie	msmc_gpio_sense_done_n	
	atest_adc_bist_trig	gnd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_dat(0)	atest_usb1_hs_ulpi_dat_en(0)	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_dat(0)	atest_usb3_hs_ulpi_dat_en(0)	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_dat(0)	atest_usb4_hs_ulpi_dat_en(0)	atestmode_usb4_hs	
	ebi1_ch1_smt_dq(28)	ebi1_ch1_smt_dq_en(28)	ebi1_ch1_tap_smt_mode_tdr	
gpio[51]				(default 01 = pd)
	GPIO_IN_OUT(51)	GPIO_CFG(51)	0	
	mic_i2s_din	gnd_tie	1	
	gsbi5(3)	gsbi5_en(3)	2	
	vfe_camif_timer6_a	vdd_tie	3	
	adsp_etm_tracedata_a(9)	vdd_tie	4	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	qdss_tracedata_a(9)	vdd_tie	5	
	a9_riva_etm_tracepkt_a(9)	vdd_tie	6	
	test_pcie_pipe_tx_datak(0)	vdd_tie	7	
	test_pcie_pipe_rx_datak(0)	vdd_tie	8	
	hdmi_lbk_data(0)	vdd_tie	9	
	apcc_bist_complete	vdd_tie	apcc_bist_mode_en	
	atest_usb2_hsic_bist_status	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_dir	vdd_tie	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_dir	vdd_tie	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_dir	vdd_tie	atestmode_usb4_hs	
	ebi1_ch1_smt_dq(27)	ebi1_ch1_smt_dq_en(27)	ebi1_ch1_tap_smt_mode_tdr	
gpio[52]				(default 01 = pd)
	GPIO_IN_OUT(52)	GPIO_CFG(52)	0	
	mic_i2s_sck	mic_i2s_sck_en	1	
	gsbi5(2)	gsbi5_en(2)	2	
	usb_fs1_oe_a	vdd_tie	3	
	usb_fs1_oe_a_n	vdd_tie	4	
	adsp_etm_tracedata_a(8)	vdd_tie	5	
	qdss_tracedata_a(8)	vdd_tie	6	
	a9_riva_etm_tracepkt_a(8)	vdd_tie	7	
	test_pcie_pipe_tx_datak(1)	vdd_tie	8	
	test_pcie_pipe_rx_datak(1)	vdd_tie	9	
	apcc_bist_paused	vdd_tie	apcc_bist_mode_en	
	atest_usb2_hsic_bist_done	vdd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_stp	gnd_tie	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_stp	gnd_tie	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_stp	gnd_tie	atestmode_usb4_hs	
	ebi1_ch1_smt_dq(26)	ebi1_ch1_smt_dq_en(26)	ebi1_ch1_tap_smt_mode_tdr	
gpio[53]				(default 01 = pd)

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	GPIO_IN_OUT(53)	GPIO_CFG(53)	0	
	mic_i2s_ws	mic_i2s_ws_en	1	
	gsbi5(1)	gsbi5_en(1)	2	
	usb_fs1_dat_a	usb_fs1_dat_a_en	3	
	dbg_bus_out(13)	vdd_tie	4	
	adsp_etm_tracedata_a(7)	vdd_tie	5	
	qdss_tracedata_a(7)	vdd_tie	6	
	a9_riva_etm_tracepkt_a(7)	vdd_tie	7	
	riva_dbg_bus(13)	vdd_tie	8	
	test_pcie_phy_dtb_out(1)	vdd_tie	9	
	apcc_bist_fail	vdd_tie	apcc_bist_mode_en	
	atest_usb2_hsic_bist_start	gnd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_nxt	vdd_tie	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_nxt	vdd_tie	atestmode_usb3_hs	
	atest_usb4_hs_ulpi_nxt	vdd_tie	atestmode_usb4_hs	
gpio[54]				(default 01 = pd)
	GPIO_IN_OUT(54)	GPIO_CFG(54)	0	
	mic_i2s_mclk	vdd_tie	1	
	gsbi5(0)	gsbi5_en(0)	2	
	usb_fs1_se0_a	usb_fs1_se0_a_en	3	
	pmb_clk_ll	vdd_tie	4	
	dbg_bus_out(12)	vdd_tie	5	
	adsp_etm_tracedata_a(6)	vdd_tie	6	
	qdss_tracedata_a(6)	vdd_tie	7	
	a9_riva_etm_tracepkt_a(6)	vdd_tie	8	
	riva_dbg_bus(12)	vdd_tie	9	
	test_pcie_phy_dtb_out(0)	vdd_tie	10	
	apcc_bist_continue	gnd_tie	apcc_bist_mode_en	
	atest_usb2_hsic_ares	gnd_tie	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_ulpi_data_oe	gnd_tie	atestmode_usb1_hs	
	atest_usb3_hs_ulpi_data_oe	gnd_tie	atestmode_usb3_hs	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	atest_usb4_hs_ulpi_data_oe	gnd_tie	atestmode_usb4_hs	
gpio[55]				(default 01 = pd)
	GPIO_IN_OUT(55)	GPIO_CFG(55)	0	
	tsif1_clk	gnd_tie	1	
	pmb_clk_cn	vdd_tie	2	
	dbg_bus_out(9)	vdd_tie	3	
	adsp_etm_tracedata_b(13)	vdd_tie	4	
	qdss_tracedata_b(13)	vdd_tie	5	
	a9_riva_etm_tracepkt_b(13)	vdd_tie	6	
	riva_dbg_bus(9)	vdd_tie	7	
	tm_bus(14)	tm_bus_en(14)	tic_mode	
	ebi1_ch1_smt_dq(6)	ebi1_ch1_smt_dq_en(6)	ebi1_ch1_tap_smt_mode_tdr	
gpio[56]				(default 01 = pd)
	GPIO_IN_OUT(56)	GPIO_CFG(56)	0	
	tsif1_en	gnd_tie	1	
	gsbi1_spi_cs3a_n	gsbi1_spi_cs3a_n_en	2	
	dbg_bus_out(8)	vdd_tie	3	
	adsp_etm_tracedata_b(12)	vdd_tie	4	
	qdss_tracedata_b(12)	vdd_tie	5	
	a9_riva_etm_tracepkt_b(12)	vdd_tie	6	
	riva_dbg_bus(8)	vdd_tie	7	
	tm_bus(15)	tm_bus_en(15)	tic_mode	
	ebi1_ch1_smt_dq(5)	ebi1_ch1_smt_dq_en(5)	ebi1_ch1_tap_smt_mode_tdr	
gpio[57]				(default 01 = pd)
	GPIO_IN_OUT(57)	GPIO_CFG(57)	0	
	tsif1_data	gnd_tie	1	
	sdc2_cmd	sdc2_cmd_en	2	
	dbg_bus_out(7)	vdd_tie	3	
	adsp_etm_tracedata_b(11)	vdd_tie	4	
	qdss_tracedata_b(11)	vdd_tie	5	
	a9_riva_etm_tracepkt_b(11)	vdd_tie	6	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	riva_dbg_bus(7)	vdd_tie	7	
	tm_bus(16)	tm_bus_en(16)	tic_mode	
	ebi1_ch1_smt_dq(4)	ebi1_ch1_smt_dq_en(4)	ebi1_ch1_tap_smt_mode_tdr	
gpio[58]				(default 01 = pd)
	GPIO_IN_OUT(58)	GPIO_CFG(58)	0	
	tsif2_sync	gnd_tie	1	
	sdc2_data(3)	sdc2_data_en(3)	2	
	dbg_bus_out(6)	vdd_tie	3	
	adsp_etm_tracedata_b(10)	vdd_tie	4	
	qdss_tracedata_b(10)	vdd_tie	5	
	a9_riva_etm_tracepkt_b(10)	vdd_tie	6	
	riva_dbg_bus(6)	vdd_tie	7	
	riva_wcn_priority_b	vdd_tie	8	
	tm_bus(17)	tm_bus_en(17)	tic_mode	
	ebi1_ch0_smt_dm(3)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dq(3)	ebi1_ch1_smt_dq_en(3)	ebi1_ch1_tap_smt_mode_tdr	
gpio[59]				(default 01 = pd)
	GPIO_IN_OUT(59)	GPIO_CFG(59)	0	
	tsif2_clk	gnd_tie	1	
	sdc2_clk	sdc2_clk_en	2	
	pmb_clk_lr	vdd_tie	3	
	dbg_bus_out(5)	vdd_tie	4	
	adsp_etm_tracedata_b(9)	vdd_tie	5	
	qdss_tracedata_b(9)	vdd_tie	6	
	a9_riva_etm_tracepkt_b(9)	vdd_tie	7	
	riva_dbg_bus(5)	vdd_tie	8	
	tm_bus(18)	tm_bus_en(18)	tic_mode	
	ebi1_ch0_smt_dqs(3)	ebi1_ch0_smt_dqs_en(3)	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dq(2)	ebi1_ch1_smt_dq_en(2)	ebi1_ch1_tap_smt_mode_tdr	
gpio[60]				(default 01 = pd)
	GPIO_IN_OUT(60)	GPIO_CFG(60)	0	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	tsif2_en	gnd_tie	1	
	sdc2_data(2)	sdc2_data_en(2)	2	
	ebi1_ch1_wrcdc_dq0_osc_test	vdd_tie	3	
	dbg_bus_out(4)	vdd_tie	4	
	adsp_etm_tracedata_b(8)	vdd_tie	5	
	qdss_tracedata_b(8)	vdd_tie	6	
	a9_riva_etm_tracepkt_b(8)	vdd_tie	7	
	riva_dbg_bus(4)	vdd_tie	8	
	mdm_lte_frame_sync_b	gnd_tie	9	
	tm_req_a	gnd_tie	tic_mode	
	ebi1_ch0_smt_dq(31)	ebi1_ch0_smt_dq_en(31)	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dq(1)	ebi1_ch1_smt_dq_en(1)	ebi1_ch1_tap_smt_mode_tdr	
gpio[61]				(default 01 = pd)
	GPIO_IN_OUT(61)	GPIO_CFG(61)	0	
	tsif2_data	gnd_tie	1	
	sdc2_data(1)	sdc2_data_en(1)	2	
	sdc3_cdc_dtest_out(0)	vdd_tie	3	
	ebi1_ch1_wrcdc_dq0_test_out(1)	vdd_tie	4	
	dbg_bus_out(3)	vdd_tie	5	
	adsp_etm_tracedata_b(7)	vdd_tie	6	
	qdss_tracedata_b(7)	vdd_tie	7	
	a9_riva_etm_tracepkt_b(7)	vdd_tie	8	
	riva_dbg_bus(3)	vdd_tie	9	
	mdm_lte_active_b	gnd_tie	10	
	tm_bus(25)	tm_bus_en(25)	tic_mode	
	ebi1_ch0_smt_dq(30)	ebi1_ch0_smt_dq_en(30)	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dq(0)	ebi1_ch1_smt_dq_en(0)	ebi1_ch1_tap_smt_mode_tdr	
gpio[62]				(default 01 = pd)
	GPIO_IN_OUT(62)	GPIO_CFG(62)	0	
	tsif1_sync	gnd_tie	1	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	sdc2_data(0)	sdc2_data_en(0)	2	
	sdc3_cdc_dtest_out(1)	vdd_tie	3	
	ebi1_ch1_wrcdc_dq0_test_out(0)	vdd_tie	4	
	dbg_bus_out(2)	vdd_tie	5	
	adsp_etm_tracedata_b(6)	vdd_tie	6	
	qdss_tracedata_b(6)	vdd_tie	7	
	a9_riva_etm_tracepkt_b(6)	vdd_tie	8	
	riva_dbg_bus(2)	vdd_tie	9	
	ebi1_ch0_smt_dq(29)	ebi1_ch0_smt_dq_en(29)	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dm(2)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[63]				(default 01 = pd)
	GPIO_IN_OUT(63)	GPIO_CFG(63)	0	
	riva_bt_ssbi	riva_bt_ssbi_en	1	
	sdc4_data(3)	sdc4_data_en(3)	2	
	dbg_bus_out(1)	vdd_tie	3	
	riva_dbg_bus(1)	vdd_tie	4	
	ebi1_ch0_smt_ca(0)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_ca(0)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[64]				(default 01 = pd)
	GPIO_IN_OUT(64)	GPIO_CFG(64)	0	
	riva_wlan_data(2)	riva_wlan_data_en(2)	1	
	sdc4_data(2)	sdc4_data_en(2)	2	
	dbg_bus_out(0)	vdd_tie	3	
	riva_dbg_bus(0)	vdd_tie	4	
	ebi1_ch0_smt_ca(1)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_ca(1)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[65]				(default 01 = pd)
	GPIO_IN_OUT(65)	GPIO_CFG(65)	0	
	riva_wlan_data(1)	riva_wlan_data_en(1)	1	
	sdc4_data(1)	sdc4_data_en(1)	2	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	ebi1_ch0_smt_ca(2)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_ca(2)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[66]				(default 01 = pd)
	GPIO_IN_OUT(66)	GPIO_CFG(66)	0	
	riva_wlan_data(0)	riva_wlan_data_en(0)	1	
	sdc4_data(0)	sdc4_data_en(0)	2	
	ebi1_ch0_smt_ca(3)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_ca(3)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[67]				(default 01 = pd)
	GPIO_IN_OUT(67)	GPIO_CFG(67)	0	
	riva_wlan_set	riva_wlan_set_en	1	
	sdc4_cmd	sdc4_cmd_en	2	
	ebi1_ch0_smt_ca(4)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_ca(4)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[68]				(default 01 = pd)
	GPIO_IN_OUT(68)	GPIO_CFG(68)	0	
	riva_wlan_clk	riva_wlan_clk_en	1	
	sdc4_clk	sdc4_clk_en	2	
	pmb_clk_ul	vdd_tie	3	
	cc_tlmm_combined_pll_lock_det	vdd_tie	4	
	ebi1_ch0_smt_cs_n(0)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_cs_n(0)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[69]				(default 11 = pu)
	GPIO_IN_OUT(69)	GPIO_CFG(69)	0	
	hdmi_cec	hdmi_cec_en	1	
	scpll2_droop_test_se2	vdd_tie	2	
	atest_usb2_hsic_ulpi_nxt	vdd_tie	atestmode_hsic_gnss_wlan	
	ebi1_ch0_smt_oe_ca	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_oe_ca	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
gpio[70]				(default 11 = pu)
	GPIO_IN_OUT(70)	GPIO_CFG(70)	0	
	hdmi_ddc_clock	hdmi_ddc_clock_en	1	
	scpll2_droop_test_se1	vdd_tie	2	
	atest_usb2_hsic_ulpi_clk_out	vdd_tie	atestmode_hsic_gnss_wlan	
	ebi1_ch1_smt_dm(0)	gnd_tie	ebi1_ch1_tap_smt_mode_tdr	
gpio[71]				(default 11 = pu)
	GPIO_IN_OUT(71)	GPIO_CFG(71)	0	
	hdmi_ddc_data	hdmi_ddc_data_en	1	
	scpll3_droop_test_se1	vdd_tie	2	
	atest_usb2_hsic_ulpi_data_in_en	gnd_tie	atestmode_hsic_gnss_wlan	
	ebi1_ch1_smt_dqs(0)	ebi1_ch1_smt_dqs_en(0)	ebi1_ch1_tap_smt_mode_tdr	
gpio[72]				(default 01 = pd)
	GPIO_IN_OUT(72)	GPIO_CFG(72)	0	
	hdmi_hot_plug_detect	gnd_tie	1	
	scpll3_droop_test_se2	vdd_tie	2	
	tm_bus(13)	tm_bus_en(13)	tic_mode	
	ebi1_ch1_smt_dq(7)	ebi1_ch1_smt_dq_en(7)	ebi1_ch1_tap_smt_mode_tdr	
gpio[73]				(default 11 = pu)
	GPIO_IN_OUT(73)	GPIO_CFG(73)	0	
	atest_sub_mode(0)	gnd_tie	atestmode	
	ebi1_ch0_smt_dq(28)	ebi1_ch0_smt_dq_en(28)	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dqs(2)	ebi1_ch1_smt_dqs_en(2)	ebi1_ch1_tap_smt_mode_tdr	
gpio[74]				(default 11 = pu)
	GPIO_IN_OUT(74)	GPIO_CFG(74)	0	
	atest_sub_mode(1)	gnd_tie	atestmode	
	ebi1_ch0_smt_dq(27)	ebi1_ch0_smt_dq_en(27)	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dq(23)	ebi1_ch1_smt_dq_en(23)	ebi1_ch1_tap_smt_mode_tdr	
gpio[75]				(default 11 = pu)
	GPIO_IN_OUT(75)	GPIO_CFG(75)	0	
	atest_tic_en	gnd_tie	atestmode	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	ebi1_ch0_smt_dq(26)	ebi1_ch0_smt_dq_en(26)	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dq(22)	ebi1_ch1_smt_dq_en(22)	ebi1_ch1_tap_smt_mode_tdr	
gpio[76]				(default 11 = pu)
	GPIO_IN_OUT(76)	GPIO_CFG(76)	0	
	ebi1_ch0_smt_dq(25)	ebi1_ch0_smt_dq_en(25)	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dq(21)	ebi1_ch1_smt_dq_en(21)	ebi1_ch1_tap_smt_mode_tdr	
gpio[77]				(default 11 = pu)
	GPIO_IN_OUT(77)	GPIO_CFG(77)	0	
	ebi1_ch0_smt_dq(24)	ebi1_ch0_smt_dq_en(24)	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dq(20)	ebi1_ch1_smt_dq_en(20)	ebi1_ch1_tap_smt_mode_tdr	
gpio[78]				(default 01 = pd)
	GPIO_IN_OUT(78)	GPIO_CFG(78)	0	
	ps_hold	vdd_tie	1	
	ebi1_ch0_smt_dm(1)	gnd_tie	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dq(19)	ebi1_ch1_smt_dq_en(19)	ebi1_ch1_tap_smt_mode_tdr	
gpio[79]				(default 01 = pd)
	GPIO_IN_OUT(79)	GPIO_CFG(79)	0	
	ssbi_pmic2	ssbi_pmic2_en	1	
	ebi1_ch0_smt_dqs(1)	ebi1_ch0_smt_dqs_en(1)	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dq(18)	ebi1_ch1_smt_dq_en(18)	ebi1_ch1_tap_smt_mode_tdr	
gpio[80]				(default 01 = pd)
	GPIO_IN_OUT(80)	GPIO_CFG(80)	0	
	gps_blanking	gnd_tie	1	
	mdm_lte_frame_sync_a	gnd_tie	2	
	tm_bus(11)	tm_bus_en(11)	tic_mode	
	ebi1_ch0_smt_dq(20)	ebi1_ch0_smt_dq_en(20)	ebi1_ch0_tap_smt_mode_tdr	
gpio[81]				(default 01 = pd)
	GPIO_IN_OUT(81)	GPIO_CFG(81)	0	
	ssbi_ext_gps	ssbi_ext_gps_en	1	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
	mdm_lte_active_a	gnd_tie	2	
	atest_usb2_hsic_ulpi_data(7)	atest_usb2_hsic_ulpi_data_en(7)	atestmode_hsic_gnss_wlan	
	atest_usb1_hs_atereset	gnd_tie	atestmode_usb1_hs	
	atest_usb3_hs_atereset	gnd_tie	atestmode_usb3_hs	
	atest_usb4_hs_atereset	gnd_tie	atestmode_usb4_hs	
	ebi1_ch1_smt_dq(25)	ebi1_ch1_smt_dq_en(25)	ebi1_ch1_tap_smt_mode_tdr	
gpio[82]				(default 01 = pd)
	GPIO_IN_OUT(82)	GPIO_CFG(82)	0	
	pci_e_rst_n	vdd_tie	1	
	gsbi7(3)	gsbi7_en(3)	2	
	ebi1_ch0_wrcdc_dq1_test_out(1)	vdd_tie	3	
	gsbi7_3d_cam_i2c_sda_l	gsbi7_3d_cam_i2c_sda_l_en	4	
	tm_bus(29)	tm_bus_en(29)	tic_mode	
	ebi1_ch0_smt_dq(14)	ebi1_ch0_smt_dq_en(14)	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dq(16)	ebi1_ch1_smt_dq_en(16)	ebi1_ch1_tap_smt_mode_tdr	
gpio[83]				(default 01 = pd)
	GPIO_IN_OUT(83)	GPIO_CFG(83)	0	
	gsbi7(2)	gsbi7_en(2)	1	
	ebi1_ch0_wrcdc_dq1_test_out(0)	vdd_tie	2	
	gsbi7_3d_cam_i2c_scl_l	gsbi7_3d_cam_i2c_scl_l_en	3	
	tm_bus(2)	tm_bus_en(2)	tic_mode	
	ebi1_ch0_smt_dq(13)	ebi1_ch0_smt_dq_en(13)	ebi1_ch0_tap_smt_mode_tdr	
gpio[84]				(default 01 = pd)
	GPIO_IN_OUT(84)	GPIO_CFG(84)	0	
	pci_e_prsnt_2_n	gnd_tie	1	
	gsbi7(1)	gsbi7_en(1)	2	
	gsbi7_3d_cam_i2c_sda_r	gsbi7_3d_cam_i2c_sda_r_en	3	
	tm_bus(30)	tm_bus_en(30)	tic_mode	
	ebi1_ch0_smt_dq(12)	ebi1_ch0_smt_dq_en(12)	ebi1_ch0_tap_smt_mode_tdr	

Table 3-4 Functions and values set to select them

GPIO	Function	Output Enable (gnd_tie=input) (vdd_tie=output)	GPIO_CFG[5:2] (FUNC_SEL)	GPIO_CFG[1:0] (GPIO_PULL)
gpio[85]				(default 01 = pd)
	GPIO_IN_OUT(85)	GPIO_CFG(85)	0	
	pci_e_pwren_n	vdd_tie	1	
	pci_e_pwren	vdd_tie	2	
	gsbi7(0)	gsbi7_en(0)	3	
	gsbi7_3d_cam_i2c_scl_r	gsbi7_3d_cam_i2c_scl_r_en	4	
	tm_bus(31)	tm_bus_en(31)	tic_mode	
	ebi1_ch0_smt_dq(11)	ebi1_ch0_smt_dq_en(11)	ebi1_ch0_tap_smt_mode_tdr	
gpio[86]				(default 01 = pd)
	GPIO_IN_OUT(86)	GPIO_CFG(86)	0	
	pci_e_pwrflt_n	gnd_tie	1	
	tm_bus(0)	tm_bus_en(0)	tic_mode	
	ebi1_ch0_smt_dq(10)	ebi1_ch0_smt_dq_en(10)	ebi1_ch0_tap_smt_mode_tdr	
gpio[87]				(default 01 = pd)
	GPIO_IN_OUT(87)	GPIO_CFG(87)	0	
	sata_led	vdd_tie	1	
	ebi1_ch0_wrcdc_dq1_osc_test	vdd_tie	2	
	boot_config(0)	gnd_tie	msmc_gpio_sense_done_n	
	tm_bus(1)	tm_bus_en(1)	tic_mode	
	ebi1_ch0_smt_dq(15)	ebi1_ch0_smt_dq_en(15)	ebi1_ch0_tap_smt_mode_tdr	
	ebi1_ch1_smt_dq(17)	ebi1_ch1_smt_dq_en(17)	ebi1_ch1_tap_smt_mode_tdr	
gpio[88]				(default 01 = pd)
	GPIO_IN_OUT(88)	GPIO_CFG(88)	0	
	usb2_hsic_strobe	usb2_hsic_strobe_en	1	
	vfe_camif_timer4_b	vdd_tie	2	
gpio[89]				(default 01 = pd)
	GPIO_IN_OUT(89)	GPIO_CFG(89)	0	
	usb2_hsic_data	usb2_hsic_data_en	1	
	vfe_camif_timer3_b	vdd_tie	2	

GPIO_CFGn

Bits	Name	Description
31:10	RESERVED	Reserved field
9	GPIO_OE	1 bit that controls the OE for GPIO[n] when in GPIO mode.
8:6	DRV_STRENGTH	Controls the GPIO pad drive strength. This applies regardless of the FUNC_SEL field selection. 0x0: 2 mA 0x1: 4 mA 0x2: 6 mA 0x3: 8 mA 0x4: 10 mA 0x5: 12 mA 0x6: 14 mA 0x7: 16 mA
5:2	FUNC_SEL	Many of the GPIO pads have one or more functional hardware interfaces behind them. This field controls how the pad is used. Set this to the appropriate value for the function desired.
1:0	GPIO_PULL	The pad can be configured to employ an internal weak pull up, pull down, or keeper function. This applies regardless of the FUNC_SEL field selection. 0x0: No pull 0x1: Pull down (PD) 0x2: Keeper 0x3: Pull up (PU)

0x00801004+ 0x10*n GPIO_IN_OUTn, n=[0..89]

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_IN_OUT[n] controls the Out and In on the GPIO. The GPIO_IN bit is read-only.

GPIO_IN_OUTn

Bits	Name	Description
31:2	RESERVED	Reserved field.
1	GPIO_OUT	Controls the value of the GPIO Output
0	GPIO_IN	Allows you to read the Input value of the GPIO

0x00801008+0x10*n GPIO_INTR_CFGn, n=[0..89]

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000002

The GPIO_INTR_CFG[n] controls the summary interrupt controller for GPIO n.

GPIO_INTR_CFGn

Bits	Name	Description
31:4	RESERVED	Reserved field.
3	INTR_RAW_STATUS_EN	This enables the RAW status for the summary interrupt on this GPIO. This is a power saving mechanism. Leave this disabled unless it is needed. 0x1: Enable 0x0: Disable
2	INTR_DECT_CTL	Controls the Edge or Level Detection of the Interrupt Controller 0x1: Edge 0x0: Level
1	INTR_POL_CTL	Controls the Polarity Detection of the Interrupt Controller. Polarity 1 corresponds to active high Polarity 0 corresponds to active low. 0x1: Polarity 1 0x0: Polarity 0
0	INTR_ENABLE	Controls if this GPIO will generate a summary interrupt. 0x1: Enable 0x0: Disable

0x0080100C+0x10*n GPIO_INTR_STATUSn, n=[0..89]

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000

The GPIO_INTR_STATUS[n] controls the summary interrupt controller for GPIO n.

GPIO_INTR_STATUSn

Bits	Name	Description
31:1	RESERVED	Reserved field.
0	INTR_STATUS	When read, it returns the status for the interrupt on GPIO[n]. When written with a 1 in this position it clears the interrupt for GPIO[n].

3.2.1.2 Miscellaneous control and configuration registers

These registers control the mode MUXing outside of the GPIO. This includes the MUXing for GPIO pads used for ETM, debug, and JTAG options.

Access to these registers is determined based on the ACR registers in the previous section.

NOTE Analog test MUXing is controlled through primary pin decodes and is not covered here.

0x00802000 TLMM_INT_JTAG_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x1005

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TLMM_INT_JTAG_CTL

Bits	Name	Description
31:13	RESERVED_1	Reserved field
12	TOTAL_RTCK_ENABLE_SOFT	Enables auto RTCK generation (Default set to 1)
11:10	RTCK_SEL_SOFT	Enables manual RTCK select: 0x0: NO_RTCK_SEL 0x1: RPM_RTCK_SEL 0x2: RIVA_ARM9_RTCK_SEL 0x3: PPSS_RTCK_SEL
9	PPSS_TAP_ENA_SOFT	Enables PPSS ARM7 JTAG (RTCK dependent)
8	A9_TAP_ENA_SOFT	Enables Riva ARM9 JTAG (RTCK dependent)
7	RPM_TAP_ENA_SOFT	Enables RPM ARM7 JTAG (RTCK dependent)
6	RESERVED_2	RESERVED
5	PCIE_TAP_ENA_SOFT	Enables PCIe JTAG
4	ADSP6_TAP_ENA_SOFT	Enables LPASS QDSP6 JTAG
3	APCC_TAP_ENA_SOFT	Enables APCC JTAG
2	QDSS_TAP_ENA_SOFT	Enables QDSS JTAG
1	ACC_TAP_ENA_SOFT	Enables ACC JTAG
0	MSM_TAP_ENA_SOFT	Enables APQ JTAG (Default set to 1)

0x00802004 TLMM_AUX_JTAG

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The TLMM_AUX_JTAG register controls the enables for which processors are allowed to trigger other processors.

TLMM_AUX_JTAG

Bits	Name	Description
31:4	RESERVED	Reserved Bits
3:0	AUX_JTAG_SEL	Selects which TAP controller is connected to the auxiliary JTAG TDO pad. 0xF: Reserved_1 0xE: Reserved_2 0xD: Reserved_3 0xC: Reserved_4 0xB: Reserved_5 0xA: Reserved_6 0x9: PPSS 0x8: RIVA 0x7: RPM 0x6: Reserved_7 0x5: PCIE 0x4: AD6 0x3: APCC 0x2: Reserved_8 0x1: ACC 0x0: None

0x00802008 TLMM_ETM_XTRIG_0

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000000

The TLMM_ETM_XTRIG register controls the enables for which processors are allowed to trigger other processors.

TLMM_ETM_XTRIG_0

Bits	Name	Description
31	GSS1_TO_APC1	Permits the GSS bit 1 to trigger the APC1
30	GSS0_TO_APC1	Permits the GSS bit 0 to trigger the APC1

TLMM_ETM_XTRIG_0 (cont.)

Bits	Name	Description
29	GSS1_TO_APC0	Permits the GSS bit 1 to trigger the APC0
28	GSS0_TO_APC0	Permits the GSS bit 0 to trigger the APC0
27	QDSS_CH3_TO_APC1	Permits the QDSS CH3 to trigger the APC1
26	QDSS_CH2_TO_APC1	Permits the QDSS CH2 to trigger the APC1
25	QDSS_CH1_TO_APC1	Permits the QDSS CH1 to trigger the APC1
24	QDSS_CH0_TO_APC1	Permits the QDSSCH0 to trigger the APC1
23	APC0_TO_APC1	Permits the APC0 to trigger the APC1
22	LA_TO_APC1	Permits the Logic Analyzer to trigger the APC1
21	DAYTONA_FAB_TO_APC1	Permits the Smart Peripheral Subsystem Fabric to trigger the APC1
20	APPS_FAB_TO_APC1	Permits the Apps Fabric to trigger the APC1
19	MMSS_FAB_TO_APC1	Permits the MMSS Fabric to trigger the APC1
18	SYS_FAB_TO_APC1	Permits the System Fabric to trigger the APC1
17	APC3_TO_APC1	Permits the APC3 to trigger the APC1
16	APC2_TO_APC1	Permits the APC2 to trigger the APC1
15	AD6_TO_APC1	Permits the AD6 to trigger the APC1
14	A9_TO_APC1	Permits the ARM9RIVA to trigger the APC1
13	QDSS_CH3_TO_APC0	Permits the QDSS CH3 to trigger the APC0
12	QDSS_CH2_TO_APC0	Permits the QDSS CH2 to trigger the APC0
11	QDSS_CH1_TO_APC0	Permits the QDSS CH1 to trigger the APC0
10	QDSS_CH0_TO_APC0	Permits the QDSSCH0 to trigger the APC0
9	APC1_TO_APC0	Permits the APC1 to trigger the APC0
8	LA_TO_APC0	Permits the Logic Analyzer to trigger the APC0
7	DAYTONA_FAB_TO_APC0	Permits the Smart Peripheral Subsystem Fabric to trigger the APC0
6	APPS_FAB_TO_APC0	Permits the Apps Fabric to trigger the APC0
5	MMSS_FAB_TO_APC0	Permits the MMSS Fabric to trigger the APC0
4	SYS_FAB_TO_APC0	Permits the System Fabric to trigger the APC0
3	APC3_TO_APC0	Permits the APC3 to trigger the APC0
2	APC2_TO_APC0	Permits the APC2 to trigger the APC0
1	AD6_TO_APC0	Permits the AD6 to trigger the APC0
0	A9_TO_APC0	Permits the ARM9 RIVA to trigger the APC0

0x0080200C TLMM_ETM_XTRIG_1

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00

The TLMM_ETM_XTRIG register controls the enables for which processors are allowed to trigger other processors.

TLMM_ETM_XTRIG_1

Bits	Name	Description
31:28	RESERVED	RESERVED
27	GSS1_TO_A9	Permits the GSS bit 1 to trigger the ARM9 RIVA
26	GSS0_TO_A9	Permits the GSS bit 0 to trigger the ARM9 RIVA
25	GSS1_TO_AD6	Permits the GSS bit 1 to trigger the AD6
24	GSS0_TO_AD6	Permits the GSS bit 0 to trigger the AD6
23	QDSS_CH1_TO_A9	Permits the QDSS CH1 to trigger the ARM9 RIVA
22	QDSS_CH0_TO_A9	Permits the QDSSCH0 to trigger the ARM9 RIVA
21	LA_TO_A9	Permits the Logic Analyzer to trigger the ARM9 RIVA
20	DAYTONA_FAB_TO_A9	Permits the Smart Peripheral Subsystem Fabric to trigger the ARM9 RIVA
19	APPS_FAB_TO_A9	Permits the Apps Fabric to trigger the ARM9 RIVA
18	MMSS_FAB_TO_A9	Permits the MMSS Fabric to trigger the ARM9 RIVA
17	SYS_FAB_TO_A9	Permits the System Fabric to trigger the ARM9 RIVA
16	APC3_TO_A9	Permits the APC3 to trigger the ARM9 RIVA
15	APC2_TO_A9	Permits the APC2 to trigger the ARM9 RIVA
14	AD6_TO_A9	Permits the AD6 to trigger the ARM9 RIVA
13	APC1_TO_A9	Permits the APC1 to trigger the ARM9 RIVA
12	APC0_TO_A9	Permits the APC0 to trigger the ARM9 RIVA
11	QDSS_CH1_TO_AD6	Permits the QDSS CH1 to trigger the AD6
10	QDSS_CH0_TO_AD6	Permits the QDSSCH0 to trigger the AD6
9	LA_TO_AD6	Permits the Logic Analyzer to trigger the AD6
8	DAYTONA_FAB_TO_AD6	Permits the Smart Peripheral Subsystem Fabric to trigger the AD6
7	APPS_FAB_TO_AD6	Permits the Apps Fabric to trigger the AD6
6	MMSS_FAB_TO_AD6	Permits the MMSS Fabric to trigger the AD6
5	SYS_FAB_TO_AD6	Permits the System Fabric to trigger the AD6
4	APC3_TO_AD6	Permits the APC3 to trigger the AD6

TLMM_ETM_XTRIG_1 (cont.)

Bits	Name	Description
3	APC2_TO_AD6	Permits the APC2 to trigger the AD6
2	A9_TO_AD6	Permits the ARM9RIVA to trigger the AD6
1	APC1_TO_AD6	Permits the APC1 to trigger the AD6
0	APC0_TO_AD6	Permits the APC0 to trigger the AD6

0x00802010 TLMM_ETM_XTRIG_2

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000000

The TLMM_ETM_XTRIG register controls the enables for which processors are allowed to trigger other processors.

TLMM_ETM_XTRIG_2

Bits	Name	Description
31:28	RESERVED	RESERVED
27	GSS1_TO_MMSS_FAB_STOP	Permits the GSS bit 1 to trigger the MMSS Fabric Stop
26	GSS0_TO_MMSS_FAB_STOP	Permits the GSS bit 0 to trigger the MMSS Fabric Stop
25	GSS1_TO_MMSS_FAB_START	Permits the GSS bit 1 to trigger the MMSS Fabric Start
24	GSS0_TO_MMSS_FAB_START	Permits the GSS bit 0 to trigger the MMSS Fabric Start
23	QDSS_CH1_TO_MMSS_FAB_STOP	Permits the QDSS CH1 to trigger the MMSS_FAB_STOP
22	QDSS_CH0_TO_MMSS_FAB_STOP	Permits the QDSSCH0 to trigger the MMSS_FAB_STOP
21	LA_TO_MMSS_FAB_STOP	Permits the Logic Analyzer to trigger the MMSS Fabric Stop
20	DAYTONA_FAB_TO_MMSS_FAB_STOP	Permits the Smart Peripheral Subsystem Fabric to trigger the MMSS Fabric Stop
19	APPS_FAB_TO_MMSS_FAB_STOP	Permits the Apps Fabric to trigger the MMSS Fabric Stop
18	SYS_FAB_TO_MMSS_FAB_STOP	Permits the SYS Fabric to trigger the MMSS Fabric Stop
17	APC3_TO_MMSS_FAB_STOP	Permits the APC3 to trigger the MMSS Fabric Stop

TLMM_ETM_XTRIG_2 (cont.)

Bits	Name	Description
16	APC2_TO_MMSS_FAB_STOP	Permits the APC2 to trigger the MMSS Fabric Stop
15	AD6_TO_MMSS_FAB_STOP	Permits the AD6 to trigger the MMSS Fabric Stop
14	A9_TO_MMSS_FAB_STOP	Permits the ARM9 RIVA to trigger the MMSS Fabric Stop
13	APC1_TO_MMSS_FAB_STOP	Permits the APC1 to trigger the MMSS Fabric Stop
12	APC0_TO_MMSS_FAB_STOP	Permits the APC0 to trigger the MMSS Fabric Stop
11	QDSS_CH1_TO_MMSS_FAB_START	Permits the QDSS CH1 to trigger the MMSS_FAB_START
10	QDSS_CH0_TO_MMSS_FAB_START	Permits the QDSSCH0 to trigger the MMSS_FAB_START
9	LA_TO_MMSS_FAB_START	Permits the Logic Analyzer to trigger the MMSS Fabric Start
8	DAYTONA_FAB_TO_MMSS_FAB_START	Permits the Smart Peripheral Subsystem Fabric to trigger the MMSS Fabric Start
7	APPS_FAB_TO_MMSS_FAB_START	Permits the Apps Fabric to trigger the MMSS Fabric Start
6	SYS_FAB_TO_MMSS_FAB_START	Permits the SYS Fabric to trigger the MMSS Fabric Start
5	APC3_TO_MMSS_FAB_START	Permits the APC3 to trigger the MMSS Fabric Start
4	APC2_TO_MMSS_FAB_START	Permits the APC2 to trigger the MMSS Fabric Start
3	AD6_TO_MMSS_FAB_START	Permits the AD6 to trigger the MMSS Fabric Start
2	A9_TO_MMSS_FAB_START	Permits the ARM9 RIVA to trigger the MMSS Fabric Start
1	APC1_TO_MMSS_FAB_START	Permits the APC1 to trigger the MMSS Fabric Start
0	APC0_TO_MMSS_FAB_START	Permits the APC0 to trigger the MMSS Fabric Start

0x00802014 TLMM_ETM_XTRIG_3

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000000

The TLMM_ETM_XTRIG register controls the enables for which processors are allowed to trigger other processors.

TLMM_ETM_XTRIG_3

Bits	Name	Description
31:28	RESERVED	RESERVED
27	GSS1_TO_DAYTONA_FAB_STOP	Permits the GSS bit 1 to trigger the Smart Peripheral Subsystem Fabric Stop
26	GSS0_TO_DAYTONA_FAB_STOP	Permits the GSS bit 0 to trigger the Smart Peripheral Subsystem Fabric Stop
25	GSS1_TO_DAYTONA_FAB_START	Permits the GSS bit 1 to trigger the Smart Peripheral Subsystem Fabric Start
24	GSS0_TO_DAYTONA_FAB_START	Permits the GSS bit 0 to trigger the Smart Peripheral Subsystem Fabric Start
23	QDSS_CH1_TO_DAYTONA_FAB_STOP	Permits the QDSS CH1 to trigger the DAYTONA_FAB_STOP
22	QDSS_CH0_TO_DAYTONA_FAB_STOP	Permits the QDSSCH0 to trigger the DAYTONA_FAB_STOP
21	LA_TO_DAYTONA_FAB_STOP	Permits the Logic Analyzer to trigger the Smart Peripheral Subsystem Fabric Stop
20	APPS_FAB_TO_DAYTONA_FAB_STOP	Permits the Apps Fabric to trigger the Smart Peripheral Subsystem Fabric Stop
19	MMSS_FAB_TO_DAYTONA_FAB_STOP	Permits the MMSS Fabric to trigger the Smart Peripheral Subsystem Fabric Stop
18	SYS_FAB_TO_DAYTONA_FAB_STOP	Permits the SYS Fabric to trigger the Smart Peripheral Subsystem Fabric Stop
17	APC3_TO_DAYTONA_FAB_STOP	Permits the APC3 to trigger the Smart Peripheral Subsystem Fabric Stop
16	APC2_TO_DAYTONA_FAB_STOP	Permits the APC2 to trigger the Smart Peripheral Subsystem Fabric Stop
15	AD6_TO_DAYTONA_FAB_STOP	Permits the AD6 to trigger the Smart Peripheral Subsystem Fabric Stop
14	A9_TO_DAYTONA_FAB_STOP	Permits the ARM9 RIVA to trigger the Smart Peripheral Subsystem Fabric Stop
13	APC1_TO_DAYTONA_FAB_STOP	Permits the APC1 to trigger the Smart Peripheral Subsystem Fabric Stop
12	APC0_TO_DAYTONA_FAB_STOP	Permits the APC0 to trigger the Smart Peripheral Subsystem Fabric Stop
11	QDSS_CH1_TO_DAYTONA_FAB_START	Permits the QDSS CH1 to trigger the DAYTONA_FAB_START
10	QDSS_CH0_TO_DAYTONA_FAB_START	Permits the QDSSCH0 to trigger the DAYTONA_FAB_START
9	LA_TO_DAYTONA_FAB_START	Permits the Logic Analyzer to trigger the Smart Peripheral Subsystem Fabric Start

TLMM_ETM_XTRIG_3 (cont.)

Bits	Name	Description
8	APPS_FAB_TO_DAYTONA_FAB_START	Permits the Apps Fabric to trigger the Smart Peripheral Subsystem Fabric Start
7	MMSS_FAB_TO_DAYTONA_FAB_START	Permits the MMSS Fabric to trigger the Smart Peripheral Subsystem Fabric Start
6	SYS_FAB_TO_DAYTONA_FAB_START	Permits the SYS Fabric to trigger the Smart Peripheral Subsystem Fabric Start
5	APC3_TO_DAYTONA_FAB_START	Permits the APC3 to trigger the Smart Peripheral Subsystem Fabric Start
4	APC2_TO_DAYTONA_FAB_START	Permits the APC2 to trigger the Smart Peripheral Subsystem Fabric Start
3	AD6_TO_DAYTONA_FAB_START	Permits the AD6 to trigger the Smart Peripheral Subsystem Fabric Start
2	A9_TO_DAYTONA_FAB_START	Permits the ARM9 RIVA to trigger the Smart Peripheral Subsystem Fabric Start
1	APC1_TO_DAYTONA_FAB_START	Permits the APC1 to trigger the Smart Peripheral Subsystem Fabric Start
0	APC0_TO_DAYTONA_FAB_START	Permits the APC0 to trigger the Smart Peripheral Subsystem Fabric Start

0x00802018 TLMM_ETM_XTRIG_4

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000000

The TLMM_ETM_XTRIG register controls the enables for which processors are allowed to trigger other processors.

TLMM_ETM_XTRIG_4

Bits	Name	Description
31	GSS1_TO_APC3	Permits the GSS bit 1 to trigger the APC3
30	GSS0_TO_APC3	Permits the GSS bit 0 to trigger the APC3
29	GSS1_TO_APC2	Permits the GSS bit 1 to trigger the APC2
28	GSS0_TO_APC2	Permits the GSS bit 0 to trigger the APC2
27	QDSS_CH3_TO_APC3	Permits the QDSS CH3 to trigger the APC3
26	QDSS_CH2_TO_APC3	Permits the QDSS CH2 to trigger the APC3
25	QDSS_CH1_TO_APC3	Permits the QDSS CH1 to trigger the APC3
24	QDSS_CH0_TO_APC3	Permits the QDSSCH0 to trigger the APC3

TLMM_ETM_XTRIG_4 (cont.)

Bits	Name	Description
23	LA_TO_APC3	Permits the Logic Analyzer to trigger the APC3
22	DAYTONA_FAB_TO_APC3	Permits the Smart Peripheral Subsystem Fabric to trigger the APC3
21	APPS_FAB_TO_APC3	Permits the Apps Fabric to trigger the APC3
20	MMSS_FAB_TO_APC3	Permits the MMSS Fabric to trigger the APC3
19	SYS_FAB_TO_APC3	Permits the System Fabric to trigger the APC3
18	APC2_TO_APC3	Permits the APC2 to trigger the APC3
17	AD6_TO_APC3	Permits the AD6 to trigger the APC3
16	A9_TO_APC3	Permits the ARM9 RIVA to trigger the APC3
15	APC1_TO_APC3	Permits the APC1 to trigger the APC3
14	APC0_TO_APC3	Permits the APC0 to trigger the APC3
13	QDSS_CH3_TO_APC2	Permits the QDSS CH3 to trigger the APC2
12	QDSS_CH2_TO_APC2	Permits the QDSS CH2 to trigger the APC2
11	QDSS_CH1_TO_APC2	Permits the QDSS CH1 to trigger the APC2
10	QDSS_CH0_TO_APC2	Permits the QDSSCH0 to trigger the APC2
9	LA_TO_APC2	Permits the Logic Analyzer to trigger the APC2
8	DAYTONA_FAB_TO_APC2	Permits the Smart Peripheral Subsystem Fabric to trigger the APC2
7	APPS_FAB_TO_APC2	Permits the Apps Fabric to trigger the APC2
6	MMSS_FAB_TO_APC2	Permits the MMSS Fabric to trigger the APC2
5	SYS_FAB_TO_APC2	Permits the System Fabric to trigger the APC2
4	APC3_TO_APC2	Permits the APC3 to trigger the APC2
3	AD6_TO_APC2	Permits the AD6 to trigger the APC2
2	A9_TO_APC2	Permits the ARM9 RIVA to trigger the APC2
1	APC1_TO_APC2	Permits the APC1 to trigger the APC2
0	APC0_TO_APC2	Permits the APC0 to trigger the APC2

0x0080201C TLMM_ETM_XTRIG_5

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000000

The TLMM_ETM_XTRIG register controls the enables for which processors are allowed to trigger other processors.

TLMM_ETM_XTRIG_5

Bits	Name	Description
31:28	RESERVED	RESERVED
27	GSS1_TO_SYS_FAB_STOP	Permits the GSS bit 1 to trigger the System Fabric Stop
26	GSS0_TO_SYS_FAB_STOP	Permits the GSS bit 0 to trigger the System Fabric Stop
25	GSS1_TO_SYS_FAB_START	Permits the GSS bit 1 to trigger the System Fabric Start
24	GSS0_TO_SYS_FAB_START	Permits the GSS bit 0 to trigger the System Fabric Start
23	QDSS_CH1_TO_SYS_FAB_STOP	Permits the QDSS CH1 to trigger the SYS_FAB_STOP
22	QDSS_CH0_TO_SYS_FAB_STOP	Permits the QDSSCH0 to trigger the SYS_FAB_STOP
21	LA_TO_SYS_FAB_STOP	Permits the Logic Analyzer to trigger the System Fabric Stop
20	DAYTONA_FAB_TO_SYS_FAB_STOP	Permits the Smart Peripheral Subsystem Fabric to trigger the System Fabric Stop
19	APPS_FAB_TO_SYS_FAB_STOP	Permits the Apps Fabric to trigger the System Fabric Stop
18	MMSS_FAB_TO_SYS_FAB_STOP	Permits the MMSS Fabric to trigger the System Fabric Stop
17	APC3_TO_SYS_FAB_STOP	Permits the APC3 to trigger the System Fabric Stop
16	APC2_TO_SYS_FAB_STOP	Permits the APC2 to trigger the System Fabric Stop
15	AD6_TO_SYS_FAB_STOP	Permits the AD6 to trigger the System Fabric Stop
14	A9_TO_SYS_FAB_STOP	Permits the ARM9 RIVA to trigger the System Fabric Stop
13	APC1_TO_SYS_FAB_STOP	Permits the APC1 to trigger the System Fabric Stop
12	APC0_TO_SYS_FAB_STOP	Permits the APC0 to trigger the System Fabric Stop
11	QDSS_CH1_TO_SYS_FAB_START	Permits the QDSS CH1 to trigger the SYS_FAB_START
10	QDSS_CH0_TO_SYS_FAB_START	Permits the QDSSCH0 to trigger the SYS_FAB_START
9	LA_TO_SYS_FAB_START	Permits the Logic Analyzer to trigger the System Fabric Start
8	DAYTONA_FAB_TO_SYS_FAB_START	Permits the Smart Peripheral Subsystem Fabric to trigger the System Fabric Start
7	APPS_FAB_TO_SYS_FAB_START	Permits the Apps Fabric to trigger the System Fabric Start
6	MMSS_FAB_TO_SYS_FAB_START	Permits the MMSS Fabric to trigger the System Fabric Start
5	APC3_TO_SYS_FAB_START	Permits the APC3 to trigger the System Fabric Start

TLMM_ETM_XTRIG_5 (cont.)

Bits	Name	Description
4	APC2_TO_SYS_FAB_START	Permits the APC2 to trigger the System Fabric Start
3	AD6_TO_SYS_FAB_START	Permits the AD6 to trigger the System Fabric Start
2	A9_TO_SYS_FAB_START	Permits the ARM9 RIVA to trigger the System Fabric Start
1	APC1_TO_SYS_FAB_START	Permits the APC1 to trigger the System Fabric Start
0	APC0_TO_SYS_FAB_START	Permits the APC0 to trigger the System Fabric Start

0x00802020 TLMM_ETM_XTRIG_6

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000000

The TLMM_ETM_XTRIG register controls the enables for which processors are allowed to trigger other processors.

TLMM_ETM_XTRIG_6

Bits	Name	Description
31:28	RESERVED	RESERVED
27	GSS1_TO_APPS_FAB_STOP	Permits the GSS bit 1 to trigger the Apps Fabric Stop
26	GSS0_TO_APPS_FAB_STOP	Permits the GSS bit 0 to trigger the Apps Fabric Stop
25	GSS1_TO_APPS_FAB_START	Permits the GSS bit 1 to trigger the Apps Fabric Start
24	GSS0_TO_APPS_FAB_START	Permits the GSS bit 0 to trigger the Apps Fabric Start
23	QDSS_CH1_TO_APPS_FAB_STOP	Permits the QDSS CH1 to trigger the APPS_FAB_STOP
22	QDSS_CH0_TO_APPS_FAB_STOP	Permits the QDSSCH0 to trigger the APPS_FAB_STOP
21	LA_TO_APPS_FAB_STOP	Permits the Logic Analyzer to trigger the Apps Fabric Stop
20	DAYTONA_FAB_TO_APPS_FAB_STOP	Permits the Smart Peripheral Subsystem Fabric to trigger the Apps Fabric Stop
19	MMSS_FAB_TO_APPS_FAB_STOP	Permits the MMSS Fabric to trigger the Apps Fabric Stop

TLMM_ETM_XTRIG_6 (cont.)

Bits	Name	Description
18	SYS_FAB_TO_APPS_FAB_STOP	Permits the SYS Fabric to trigger the Apps Fabric Stop
17	APC3_TO_APPS_FAB_STOP	Permits the APC3 to trigger the Apps Fabric Stop
16	APC2_TO_APPS_FAB_STOP	Permits the APC2 to trigger the Apps Fabric Stop
15	AD6_TO_APPS_FAB_STOP	Permits the AD6 to trigger the Apps Fabric Stop
14	A9_TO_APPS_FAB_STOP	Permits the ARM9 RIVA to trigger the Apps Fabric Stop
13	APC1_TO_APPS_FAB_STOP	Permits the APC1 to trigger the Apps Fabric Stop
12	APC0_TO_APPS_FAB_STOP	Permits the APC0 to trigger the Apps Fabric Stop
11	QDSS_CH1_TO_APPS_FAB_START	Permits the QDSS CH1 to trigger the APPS_FAB_START
10	QDSS_CH0_TO_APPS_FAB_START	Permits the QDSSCH0 to trigger the APPS_FAB_START
9	LA_TO_APPS_FAB_START	Permits the Logic Analyzer to trigger the Apps Fabric Start
8	DAYTONA_FAB_TO_APPS_FAB_START	Permits the Smart Peripheral Subsystem Fabric to trigger the Apps Fabric Start
7	MMSS_FAB_TO_APPS_FAB_START	Permits the MMSS Fabric to trigger the Apps Fabric Start
6	SYS_FAB_TO_APPS_FAB_START	Permits the SYS Fabric to trigger the Apps Fabric Start
5	APC3_TO_APPS_FAB_START	Permits the APC3 to trigger the Apps Fabric Start
4	APC2_TO_APPS_FAB_START	Permits the APC2 to trigger the Apps Fabric Start
3	AD6_TO_APPS_FAB_START	Permits the AD6 to trigger the Apps Fabric Start
2	A9_TO_APPS_FAB_START	Permits the ARM9 RIVA to trigger the Apps Fabric Start
1	APC1_TO_APPS_FAB_START	Permits the APC1 to trigger the Apps Fabric Start
0	APC0_TO_APPS_FAB_START	Permits the APC0 to trigger the Apps Fabric Start

0x00802024 TLMM_ETM_XTRIG_7

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000000

The TLMM_ETM_XTRIG register controls the enables for which processors are allowed to trigger other processors.

TLMM_ETM_XTRIG_7

Bits	Name	Description
31:28	RESERVED	RESERVED
27	GSS1_TO_QDSS_CH3	Permits the GSS bit 1 to trigger the QDSS CH3
26	GSS0_TO_QDSS_CH3	Permits the GSS bit 0 to trigger the QDSS CH3
25	APC3_TO_QDSS_CH3	Permits the APC3 to trigger the QDSS CH3
24	APC2_TO_QDSS_CH3	Permits the APC2 to trigger the QDSS CH3
23	GSS1_TO_QDSS_CH2	Permits the GSS bit 1 to trigger the QDSS CH2
22	GSS0_TO_QDSS_CH2	Permits the GSS bit 0 to trigger the QDSS CH2
21	APC3_TO_QDSS_CH2	Permits the APC3 to trigger the QDSS CH2
20	APC2_TO_QDSS_CH2	Permits the APC2 to trigger the QDSS CH2
19	GSS1_TO_QDSS_CH1	Permits the GSS bit 1 to trigger the QDSS CH1
18	GSS0_TO_QDSS_CH1	Permits the GSS bit 0 to trigger the QDSS CH1
17	APC3_TO_QDSS_CH1	Permits the APC3 to trigger the QDSS CH1
16	APC2_TO_QDSS_CH1	Permits the APC2 to trigger the QDSS CH1
15	GSS1_TO_QDSS_CH0	Permits the GSS bit 1 to trigger the QDSS CH0
14	GSS0_TO_QDSS_CH0	Permits the GSS bit 0 to trigger the QDSS CH0
13	APC3_TO_QDSS_CH0	Permits the APC3 to trigger the QDSS CH0
12	APC2_TO_QDSS_CH0	Permits the APC2 to trigger the QDSS CH0
11	LA_TO_QDSS_CH3	Permits the Logic Analyzer to trigger the QDSS CH3
10	APC1_TO_QDSS_CH3	Permits the APC1 to trigger the QDSS CH3
9	APC0_TO_QDSS_CH3	Permits the APC0 to trigger the QDSS CH3
8	LA_TO_QDSS_CH2	Permits the Logic Analyzer to trigger the QDSS CH2
7	APC1_TO_QDSS_CH2	Permits the APC1 to trigger the QDSS CH2
6	APC0_TO_QDSS_CH2	Permits the APC0 to trigger the QDSS CH2
5	LA_TO_QDSS_CH1	Permits the Logic Analyzer to trigger the QDSS CH1
4	APC1_TO_QDSS_CH1	Permits the APC1 to trigger the QDSS CH1

TLMM_ETM_XTRIG_7 (cont.)

Bits	Name	Description
3	APC0_TO_QDSS_CH1	Permits the APC0 to trigger the QDSS CH1
2	LA_TO_QDSS_CH0	Permits the Logic Analyzer to trigger the QDSS CH0
1	APC1_TO_QDSS_CH0	Permits the APC1 to trigger the QDSS CH0
0	APC0_TO_QDSS_CH0	Permits the APC0 to trigger the QDSS CH0

0x00802044 TLMM_ETM_XTRIG_8

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000000

The TLMM_ETM_XTRIG register controls the enables for which processors are allowed to trigger other processors.

TLMM_ETM_XTRIG_8

Bits	Name	Description
31:30	RESERVED	RESERVED
29	QDSS_CH3_TO_GSS1	Permits the QDSS CH3 to trigger the GSS bit 1
28	QDSS_CH2_TO_GSS1	Permits the QDSS CH2 to trigger the GSS bit 1
27	QDSS_CH1_TO_GSS1	Permits the QDSS CH1 to trigger the GSS bit 1
26	QDSS_CH0_TO_GSS1	Permits the QDSSCH0 to trigger the GSS bit 1
25	LA_TO_GSS1	Permits the Logic Analyzer to trigger the GSS bit 1
24	DAYTONA_FAB_TO_GSS1	Permits the Smart Peripheral Subsystem Fabric to trigger the GSS bit 1
23	APPS_FAB_TO_GSS1	Permits the Apps Fabric to trigger the GSS bit 1
22	MMSS_FAB_TO_GSS1	Permits the MMSS Fabric to trigger the GSS bit 1
21	SYS_FAB_TO_GSS1	Permits the SYS Fabric to trigger the GSS bit 1
20	APC3_TO_GSS1	Permits the APC3 to trigger the GSS bit 1
19	APC2_TO_GSS1	Permits the APC2 to trigger the GSS bit 1
18	AD6_TO_GSS1	Permits the AD6 to trigger the GSS bit 1
17	A9_TO_GSS1	Permits the ARM9 RIVA to trigger the GSS bit 1
16	APC1_TO_GSS1	Permits the APC1 to trigger the GSS bit 1
15	APC0_TO_GSS1	Permits the APC0 to trigger the GSS bit 1
14	QDSS_CH3_TO_GSS0	Permits the QDSS CH3 to trigger the GSS bit 0

TLMM_ETM_XTRIG_8 (cont.)

Bits	Name	Description
13	QDSS_CH2_TO_GSS0	Permits the QDSS CH2 to trigger the GSS bit 0
12	QDSS_CH1_TO_GSS0	Permits the QDSS CH1 to trigger the GSS bit 0
11	QDSS_CH0_TO_GSS0	Permits the QDSSCH0 to trigger the GSS bit 0
10	LA_TO_GSS0	Permits the Logic Analyzer to trigger the GSS bit 0
9	DAYTONA_FAB_TO_GSS0	Permits the Smart Peripheral Subsystem Fabric to trigger the GSS bit 0
8	APPS_FAB_TO_GSS0	Permits the Apps Fabric to trigger the GSS bit 0
7	MMSS_FAB_TO_GSS0	Permits the MMSS Fabric to trigger the GSS bit 0
6	SYS_FAB_TO_GSS0	Permits the SYS Fabric to trigger the GSS bit 0
5	APC3_TO_GSS0	Permits the APC3 to trigger the GSS bit 0
4	APC2_TO_GSS0	Permits the APC2 to trigger the GSS bit 0
3	AD6_TO_GSS0	Permits the AD6 to trigger the GSS bit 0
2	A9_TO_GSS0	Permits the ARM9 RIVA to trigger the GSS bit 0
1	APC1_TO_GSS0	Permits the APC1 to trigger the GSS bit 0
0	APC0_TO_GSS0	Permits the APC0 to trigger the GSS bit 0

0x00802028 TLMM_DBG_HALT_XTRIG_PERM_0

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00

The TLMM_DBG_HALT_XTRIG_PERM register controls the enables for which processors are allowed to trigger other processors.

TLMM_DBG_HALT_XTRIG_PERM_0

Bits	Name	Description
31	QDMAP_TO_A9	Permits the QDMAP to trigger the ARM9 RIVA
30	APC3_TO_A9	Permits the APC3 to trigger the ARM9 RIVA
29	APC2_TO_A9	Permits the APC2 to trigger the ARM9 RIVA
28	AD6_TO_A9	Permits the AD6 to trigger the ARM9 RIVA
27	PPSS_TO_A9	Permits the PPSS to trigger the ARM9 RIVA
26	RPM_TO_A9	Permits the RPM to trigger the ARM9 RIVA
25	APC1_TO_A9	Permits the APC1 to trigger the ARM9 RIVA

TLMM_DBG_HALT_XTRIG_PERM_0 (cont.)

Bits	Name	Description
24	APC0_TO_A9	Permits the APC0 to trigger the ARM9 RIVA
23	QDMAP_TO_RPM	Permits the QDMAP to trigger the RPM
22	APC3_TO_RPM	Permits the APC3 to trigger the RPM
21	APC2_TO_RPM	Permits the APC2 to trigger the RPM
20	AD6_TO_RPM	Permits the AD6 to trigger the RPM
19	PPSS_TO_RPM	Permits the PPSS to trigger the RPM
18	A9_TO_RPM	Permits the ARM9 RIVA to trigger the RPM
17	APC1_TO_RPM	Permits the APC1 to trigger the RPM
16	APC0_TO_RPM	Permits the APC0 to trigger the RPM
15	QDMAP_TO_APC1	Permits the QDMAP to trigger the APC1
14	APC3_TO_APC1	Permits the APC3 to trigger the APC1
13	APC2_TO_APC1	Permits the APC2 to trigger the APC1
12	AD6_TO_APC1	Permits the AD6 to trigger the APC1
11	PPSS_TO_APC1	Permits the PPSS to trigger the APC1
10	A9_TO_APC1	Permits the ARM9 RIVA to trigger the APC1
9	RPM_TO_APC1	Permits the RPM to trigger the APC1
8	APC0_TO_APC1	Permits the APC0 to trigger the APC1
7	QDMAP_TO_APC0	Permits the QDMAP to trigger the APC0
6	APC3_TO_APC0	Permits the APC3 to trigger the APC0
5	APC2_TO_APC0	Permits the APC2 to trigger the APC0
4	AD6_TO_APC0	Permits the AD6 to trigger the APC0
3	PPSS_TO_APC0	Permits the PPSS to trigger the APC0
2	A9_TO_APC0	Permits the ARM9 RIVA to trigger the APC0
1	RPM_TO_APC0	Permits the RPM to trigger the APC0
0	APC1_TO_APC0	Permits the APC1 to trigger the APC0

0x0080202C TLMM_DBG_HALT_XTRIG_PERM_1

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00

Table 3-4 The TLMM_DBG_HALT_XTRIG_PERM register controls the enables for which processors are allowed to trigger other processors.

TLMM_DBG_HALT_XTRIG_PERM_1

Bits	Name	Description
31	QDMAP_TO_APC3	Permits the QDMAP to trigger the APC3
30	APC2_TO_APC3	Permits the APC2 to trigger the APC3
29	AD6_TO_APC3	Permits the AD6 to trigger the APC3
28	PPSS_TO_APC3	Permits the PPSS to trigger the APC3
27	A9_TO_APC3	Permits the ARM9 RIVA to trigger the APC3
26	RPM_TO_APC3	Permits the RPM to trigger the APC3
25	APC1_TO_APC3	Permits the APC1 to trigger the APC3
24	APC0_TO_APC3	Permits the APC0 to trigger the APC3
23	QDMAP_TO_APC2	Permits the QDMAP to trigger the APC2
22	APC3_TO_APC2	Permits the APC3 to trigger the APC2
21	AD6_TO_APC2	Permits the AD6 to trigger the APC2
20	PPSS_TO_APC2	Permits the PPSS to trigger the APC2
19	A9_TO_APC2	Permits the ARM9 RIVA to trigger the APC2
18	RPM_TO_APC2	Permits the RPM to trigger the APC2
17	APC1_TO_APC2	Permits the APC1 to trigger the APC2
16	APC0_TO_APC2	Permits the APC0 to trigger the APC2
15	QDMAP_TO_PPSS	Permits the QDMAP to trigger the PPSS
14	APC3_TO_PPSS	Permits the APC3 to trigger the PPSS
13	APC2_TO_PPSS	Permits the APC2 to trigger the PPSS
12	AD6_TO_PPSS	Permits the AD6 to trigger the PPSS
11	A9_TO_PPSS	Permits the ARM9 RIVA to trigger the PPSS
10	RPM_TO_PPSS	Permits the RPM to trigger the PPSS
9	APC1_TO_PPSS	Permits the APC1 to trigger the PPSS
8	APC0_TO_PPSS	Permits the APC0 to trigger the PPSS
7	APC3_TO_AD6	Permits the APC3 to trigger the AD6
6	APC2_TO_AD6	Permits the APC2 to trigger the AD6
5	QDMAP_TO_AD6	Permits the QDMAP to trigger the AD6
4	A9_TO_AD6	Permits the ARM9 RIVA to trigger the AD6
3	PPSS_TO_AD6	Permits the PPSS to trigger the AD6
2	RPM_TO_AD6	Permits the RPM to trigger the AD6
1	APC1_TO_AD6	Permits the APC1 to trigger the AD6

TLMM_DBG_HALT_XTRIG_PERM_1 (cont.)

Bits	Name	Description
0	APC0_TO_AD6	Permits the APC0 to trigger the AD6

0x00802050 TLMM_DBG_HALT_XTRIG_PERM_2

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000000

The TLMM_DBG_HALT_XTRIG_PERM register controls the enables for which processors are allowed to trigger other processors.

TLMM_DBG_HALT_XTRIG_PERM_2

Bits	Name	Description
31:17	RESERVED	RESERVED
16	GSS_TO_APC3	Permits the GSS to trigger the APC3
15	GSS_TO_APC2	Permits the GSS to trigger the APC2
14	GSS_TO_AD6	Permits the GSS to trigger the AD6
13	GSS_TO_A9	Permits the GSS to trigger the ARM9 RIVA
12	GSS_TO_PPSS	Permits the GSS to trigger the PPSS
11	GSS_TO_RPM	Permits the GSS to trigger the RPM
10	GSS_TO_APC1	Permits the GSS to trigger the APC1
9	GSS_TO_APC0	Permits the GSS to trigger the APC0
8	APC3_TO_GSS	Permits the APC3 to trigger the GSS
7	APC2_TO_GSS	Permits the APC2 to trigger the GSS
6	QDMAP_TO_GSS	Permits the QDMAP to trigger the GSS
5	AD6_TO_GSS	Permits the AD6 to trigger the GSS
4	A9_TO_GSS	Permits the ARM9 RIVA to trigger the GSS
3	PPSS_TO_GSS	Permits the PPSS to trigger the GSS
2	RPM_TO_GSS	Permits the RPM to trigger the GSS
1	APC1_TO_GSS	Permits the APC1 to trigger the GSS
0	APC0_TO_GSS	Permits the APC0 to trigger the GSS

0x00802030 TLMM_DBG_RESUME_XTRIG_PERM_0

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00

The TLMM_DBG_RESUME_XTRIG_PERM register controls the enables for which processors are allowed to trigger other processors.

TLMM_DBG_RESUME_XTRIG_PERM_0

Bits	Name	Description
31:27	RESERVED	Reserved Bits
26	GSS_TO_AD6	Permits the GSS to trigger the AD6
25	GSS_TO_APC1	Permits the GSS to trigger the APC1
24	GSS_TO_APC0	Permits the ARM9 RIVA to trigger the APC0
23	APC3_TO_AD6	Permits the APC3 to trigger the AD6
22	APC2_TO_AD6	Permits the APC2 to trigger the AD6
21	QDMAP_TO_AD6	Permits the QDMAP to trigger the AD6
20	A9_TO_AD6	Permits the ARM9 RIVA to trigger the AD6
19	PPSS_TO_AD6	Permits the PPSS to trigger the AD6
18	RPM_TO_AD6	Permits the RPM to trigger the AD6
17	APC1_TO_AD6	Permits the APC1 to trigger the AD6
16	APC0_TO_AD6	Permits the APC0 to trigger the AD6
15	QDMAP_TO_APC1	Permits the QDMAP to trigger the APC1
14	APC3_TO_APC1	Permits the APC3 to trigger the APC1
13	APC2_TO_APC1	Permits the APC2 to trigger the APC1
12	AD6_TO_APC1	Permits the AD6 to trigger the APC1
11	PPSS_TO_APC1	Permits the PPSS to trigger the APC1
10	A9_TO_APC1	Permits the ARM9 RIVA to trigger the APC1
9	RPM_TO_APC1	Permits the RPM to trigger the APC1
8	APC0_TO_APC1	Permits the APC0 to trigger the APC1
7	QDMAP_TO_APC0	Permits the QDMAP to trigger the APC0
6	APC3_TO_APC0	Permits the APC3 to trigger the APC0
5	APC2_TO_APC0	Permits the APC2 to trigger the APC0
4	AD6_TO_APC0	Permits the AD6 to trigger the APC0
3	PPSS_TO_APC0	Permits the PPSS to trigger the APC0

TLMM_DBG_RESUME_XTRIG_PERM_0 (cont.)

Bits	Name	Description
2	A9_TO_APC0	Permits the ARM9 RIVA to trigger the APC0
1	RPM_TO_APC0	Permits the RPM to trigger the APC0
0	APC1_TO_APC0	Permits the APC1 to trigger the APC0

0x00802034 TLMM_DBG_RESUME_XTRIG_PERM_1

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00

The TLMM_DBG_RESUME_XTRIG_PERM register controls the enables for which processors are allowed to trigger other processors.

TLMM_DBG_RESUME_XTRIG_PERM_1

Bits	Name	Description
31:27	RESERVED	Reserved Bits
26	GSS_TO_APC3	Permits the GSS to trigger the APC3
25	GSS_TO_APC2	Permits the GSS to trigger the APC2
24	QDMAP_TO_GSS	Permits the QDMAP to trigger the GSS
23	APC3_TO_GSS	Permits the APC3 to trigger the GSS
22	APC2_TO_GSS	Permits the APC2 to trigger the GSS
21	AD6_TO_GSS	Permits the AD6 to trigger the GSS
20	PPSS_TO_GSS	Permits the PPSS to trigger the GSS
19	A9_TO_GSS	Permits the ARM9 RIVA to trigger the GSS
18	RPM_TO_GSS	Permits the RPM to trigger the GSS
17	APC1_TO_GSS	Permits the APC1 to trigger the GSS
16	APC0_TO_GSS	Permits the APC0 to trigger the GSS
15	QDMAP_TO_APC3	Permits the QDMAP to trigger the APC3
14	APC2_TO_APC3	Permits the APC3 to trigger the APC3
13	AD6_TO_APC3	Permits the AD6 to trigger the APC3
12	PPSS_TO_APC3	Permits the PPSS to trigger the APC3
11	A9_TO_APC3	Permits the ARM9 RIVA to trigger the APC3
10	RPM_TO_APC3	Permits the RPM to trigger the APC3
9	APC1_TO_APC3	Permits the APC1 to trigger the APC3

TLMM_DBG_RESUME_XTRIG_PERM_1 (cont.)

Bits	Name	Description
8	APC0_TO_APC3	Permits the APC0 to trigger the APC3
7	QDMAP_TO_APC2	Permits the QDMAP to trigger the APC2
6	APC3_TO_APC2	Permits the APC3 to trigger the APC2
5	AD6_TO_APC2	Permits the AD6 to trigger the APC2
4	PPSS_TO_APC2	Permits the PPSS to trigger the APC2
3	A9_TO_APC2	Permits the ARM9 RIVA to trigger the APC2
2	RPM_TO_APC2	Permits the RPM to trigger the APC2
1	APC1_TO_APC2	Permits the APC1 to trigger the APC2
0	APC0_TO_APC2	Permits the APC0 to trigger the APC2

0x00802038 TLMM_DBG_STATUS

Type: Read
Clock: CC_TLMM_HCLK
Reset State: 0x0

The TLMM_DBG_STATUS register reflects the debug state of the RPM ARM7, PPSS ARM7, Audio QDSP6, Riva ARM9 and the APCC.

TLMM_DBG_STATUS

Bits	Name	Description
31:18	RESERVED	Reserved Bits
17	GSS_DBG_ACK	GSS debug trigger signal gss_dbg_ack
16	GSS_DBG_TRIGGER	GSS debug trigger signal gss_dbg_trigger
15	APC3_DBG_ACK	APC3 debug trigger signal apc3_dbg_ack
14	APC3_DBG_DONE	APC3 debug trigger signal apc3_dbg_done
13	APC3_DBG_TRIGGER	APC3 debug trigger signal apc3_dbg_trigger
12	APC2_DBG_ACK	APC2 debug trigger signal apc2_dbg_ack
11	APC2_DBG_DONE	APC2 debug trigger signal apc2_dbg_done
10	APC2_DBG_TRIGGER	APC2 debug trigger signal apc2_dbg_trigger
9	AD6_MCD_BREAKEVENT	Audio DSP Debug Ack signal ad6_mcd_breakevent
8	A9_DBGACK	ARM9 Debug Ack signal a9_dbgack
7	PPSS_JTAG_DBGACK	PPSS Debug Ack signal ppss_jtag_dbgack
6	RPM_DBG_ACK	RPM Debug Ack signal rpm_dbg_ack

TLMM_DBG_STATUS (cont.)

Bits	Name	Description
5	APC1_DBG_ACK	APC1 debug trigger signal apc1_dbg_ack
4	APC1_DBG_DONE	APC1 debug trigger signal apc1_dbg_done
3	APC1_DBG_TRIGGER	APC1 debug trigger signal apc1_dbg_trigger
2	APC0_DBG_ACK	APC0 debug trigger signal apc0_dbg_ack
1	APC0_DBG_DONE	APC0 debug trigger signal apc0_dbg_done
0	APC0_DBG_TRIGGER	APC0 debug trigger signal apc0_dbg_trigger

0x0080203C TLMM_ETM_MODE

Type: Read/Write
Clock: CC_TLMM_CLK
Reset State: 0x0000

The TLMM_ETM_MODE register controls the enables for which processors are allowed to trigger other processors.

TLMM_ETM_MODE

Bits	Name	Description
31:2	RESERVED	Reserved Bits
1	APC_OVER_JTAG	Configures APC ETM Mode over JTAG pins. This muxes three tracedata onto the TDI, TDO, and RTCK pins. 0x1: Enable 0x0: Disable
0	APC_OVER_SDC3	Configures 6-pin (4-bit) APC ETM Mode over SDC3 pins. 0x1: Enable 0x0: Disable

0x00802040 TLMM_DBG_BUS_OUT_SEL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0

The TLMM_DBG_BUS_OUT_SEL register selects between 4 different byte shifted versions of the dbg_bus_out. This allows critical bits to be moved to different GPIOs if concurrency issues occur. The output of this mux feeds the GPIO muxing where each bit can be enabled as an alternate function.

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TLMM_DBG_BUS_OUT_SEL

Bits	Name	Description
31:2	RESERVED	Reserved Bits
1:0	COPY_SEL	Select which byte shifted copy to output to the GPIO muxing: 0x0: COPY_A 0x1: COPY_B 0x2: COPY_C 0x3: COPY_D

0x00802048 CHIP_MODE

Type: Read
Clock: CC_TLMM_HCLK
Reset State: pin value

The APQ MODE input pad values are reflected in this register.

CHIP_MODE

Bits	Name	Description
31:2	RESERVED	Reserved field.
1	MODE1_PIN	Returns the current value of MODE[1] pin
0	MODE0_PIN	Returns the current value of MODE[0] pin

0x0080204C TLMM_SPARE

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00

The TLMM_SPARE register is a miscellaneous register for spare register bits.

TLMM_SPARE

Bits	Name	Description
31:8	RESERVED	By convention, always write zero. Reads always return zero.
7:0	MISC	

0x00802054 HW_REVISION_NUMBER

Type: Read
Clock: CC_TLMM_HCLK
Reset State: Hardcoded and PINs

The HW_REVISION_NUMBER register contains the hardware revision number for the APQ. This information is identical to that stored in JTAG ID, which contains chip revision chip ID (including 'variant'), manufacturing ID, and a start bit.

HW_REVISION_NUMBER

Bits	Name	Description
31:28	VERSION_ID	0x0: first tape-out
27:12	PARTNUM	Future variants can be created through EFUSE blowing.
11:1	QUALCOMM_MFG_ID	00001110000
0	START_BIT	Always set (1)

0x00802064 RIVA_COEXIST_GPIO_PORT_SEL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0

The GPIO_PORT_SEL register is used to control the Muxing for multiple copies of an interface on the pins.

RIVA_COEXIST_GPIO_PORT_SEL

Bits	Name	Description
31:2	RESERVED	Reserved field.
1:0	RIVA_COEXIST_SEL	Select between copy A and copy B and copy C of the interface: The signals that are part of the RIVA Coexistence Interface are: WNC_PRIORITY LTE_FRAME_SYNC LTE_ACTIVE 0x0: RIVA_COEXIST_A 0x1: RIVA_COEXIST_B 0x2: RIVA_COEXIST_C 0x3: RESERVED

0x00802068 GP_PDM0_GPIO_PORT_SEL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0

The GPIO_PORT_SEL register is used to control the Muxing for multiple copies of an interface on the pins.

GP_PDM0_GPIO_PORT_SEL

Bits	Name	Description
31:1	RESERVED	Reserved field.
0	GP_PDM0_SEL	Select between copy A and copy B of the interface: 0x0: GP_PDM0_A 0x1: GP_PDM0_B

0x0080206C GP_PDM1_GPIO_PORT_SEL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0

The GPIO_PORT_SEL register is used to control the Muxing for multiple copies of an interface on the pins.

GP_PDM1_GPIO_PORT_SEL

Bits	Name	Description
31:1	RESERVED	Reserved field.
0	GP_PDM1_SEL	Select between copy A and copy B of the interface: 0x0: GP_PDM1_A 0x1: GP_PDM1_B

0x00802070 GP_PDM2_GPIO_PORT_SEL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0

The GPIO_PORT_SEL register is used to control the Muxing for multiple copies of an interface on the pins.

GP_PDM2_GPIO_PORT_SEL

Bits	Name	Description
31:1	RESERVED	Reserved field.
0	GP_PDM2_SEL	Select between copy A and copy B of the interface: 0x0: GP_PDM2_A 0x1: GP_PDM2_B

0x00802074 SLIMBUS1_GPIO_PORT_SEL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0

The GPIO_PORT_SEL register is used to control the Muxing for multiple copies of an interface on the pins.

For slimbus1, this register serves two functions.

The first is the combining of the multiple copies of the slimbus1_clk and slimbus1_data input paths. Specifically, this register determines whether slimbus1_clk_a_in or slimbus1_clk_b_in is muxed to slimbus1_clk_in. Similarly, slimbus1_data_a_in and slimbus1_data_b_in are muxed to slimbus1_data_in.

The second function of this register is to select which copy of the early slimbus feedback clock is used. As such, the register value also determines whether slimbus1_early_fb_clk_a or slimbus1_early_fb_clk_b is muxed to slimbus1_early_fb_clk. slimbus1_early_fb_clk_a is sourced from slimbus1_clk_out when slimbus1_clk_a is selected as the alternate function for the respective GPIO. Similarly, slimbus1_early_fb_clk_b is sourced from slimbus1_clk_out when slimbus1_clk_b is selected as the alternate function for the respective GPIO. This early tapping of the output clock provides a version of the feedback clock that does not go through the pad.

SLIMBUS1_GPIO_PORT_SEL

Bits	Name	Description
31:1	RESERVED	Reserved field.
0	SLIMBUS1_SEL	Select between copy A and copy B of the interface: 0x0: SLIMBUS1_A 0x1: SLIMBUS1_B

0x0080207C SLIMBUS1_A_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0

This register controls the slimbus1_a_sr_ctl_en TLMM output.

Its purpose is to control the clock and data pads for copy A of slimbus1 on GPIO. It is used to enable/disable slew rate control for the slimbus pad. When used for slimbus, slew rate control must be enabled. When used for other purposes, slew rate control should be disabled. When disabled, the pad behaves in a similar manner to a regular GPIO pad. The default value is slew rate control disabled.

SLIMBUS1_A_CTL

Bits	Name	Description
31:1	RESERVED	Reserved field.
0	SR_CTL_EN	Select whether slew rate control is enabled/disabled: 0x0: Disable 0x1: Enable

0x00802080 SLIMBUS1_B_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0

This register controls the slimbus1_b_sr_ctl_en TLMM output.

Its purpose is to control the clock and data pads for copy B of slimbus1 on GPIO. It is used to enable/disable slew rate control for the slimbus pad. When used for slimbus, slew rate control must be enabled. When used for other purposes, slew rate control should be disabled. When disabled, the pad behaves in a similar manner to a regular GPIO pad. The default value is slew rate control disabled.

SLIMBUS1_B_CTL

Bits	Name	Description
31:1	RESERVED	Reserved field.
0	SR_CTL_EN	Select whether slew rate control is enabled/disabled: 0x0: Disable 0x1: Enable

0x00802084 RGB_PAD_EN

Type: Read/Write
Clock: CC_TLMM_CLK
Reset State: 0x00000000

This register provides an enable to the LVDS and RGB pads.

RGB_PAD_EN

Bits	Name	Description
31:1	RESERVED	Reserved
0	RGB_PAD_EN	This bit is used to provide a RGB enable to the LVDS and RGB pads. 0x1: ENABLE 0x0: DISABLE

0x00802088 USB_FS1_GPIO_PORT_SEL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0

The GPIO_PORT_SEL register is used to control the Muxing for multiple copies of an interface on the pins.

USB_FS1_GPIO_PORT_SEL

Bits	Name	Description
31:1	RESERVED	Reserved field.
0	USB_FS1_SEL	Select between copy A and copy B of the interface: 0x0: USB_FS1_A 0x1: USB_FS1_B

Table 3-5 Pull values

Value	Configuration
00	No pull (up or down)
01	Pull down
10	Keep
11	Pull up

Table 3-6 HDrive values

Value	Configuration
000	2 mA
001	4 mA
010	6 mA
011	8 mA
100	10 mA

Table 3-6 HDrive values

Value	Configuration
101	12 mA
110	14 mA
111	16 mA

0x00802090 RESOUT_HDRV_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0001

This registers controls the HDrive value for the resout pin.

RESOUT_HDRV_CTL

Bits	Name	Description
31:3	RESERVED	Reserved.
2:0	RESOUT_N_HDRV	RESOUT_N HDrive Value

0x00802094 JTAG_HDRV_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0xF0DB

This register controls the HDrive value for the JTAG pins.

JTAG_HDRV_CTL

Bits	Name	Description
31:16	RESERVED	RESERVED Bits
15:14	TDI_PULL	TDI Pull Value
13:12	TMS_PULL	TMS Pull Value
11:9	TDI_HDRV	TDI HDrive Value
8:6	TMS_HDRV	TMS HDrive Value
5:3	TDO_HDRV	TDO HDrive Value
2:0	RTCK_HDRV	RTCK HDrive Value

0x0080209C PMIC_HDRV_PULL_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x200

This register controls the HDrive and Pull values for the PMIC interfaces pins.

PMIC_HDRV_PULL_CTL

Bits	Name	Description
31:11	RESERVED	RESERVED Bits
10:9	SSBI_PMIC1_PULL	SSBI PMIC 1 Pull Value
8:6	CXO_EN_HDRV	CXO ENABLE HDrive Value
5:3	SSBI_PMIC_FWD_CLK_HDRV	SSBI PMIC FORWARD CLOCK HDrive Value
2:0	SSBI_PMIC1_HDRV	SSBI PMIC 1 HDrive Value

0x008020A0 SDC1_HDRV_PULL_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0BDB

This register controls the HDrive and Pull values for the SDC1 interface pins.

SDC1_HDRV_PULL_CTL

Bits	Name	Description
31:15	RESERVED	Reserved.
14:13	SDC1_CLK_PULL	SDC1 CLK Pull Value
12:11	SDC1_CMD_PULL	SDC1 CMD Pull Value
10:9	SDC1_DATA_PULL	SDC1 DATA Pull Value
8:6	SDC1_CLK_HDRV	SDC1 CLOCK HDrive Value
5:3	SDC1_CMD_HDRV	SDC1 CMD HDrive Value
2:0	SDC1_DATA_HDRV	SDC1 DATA HDrive Value

0x008020A4 SDC3_HDRV_PULL_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0BDB

This register controls the HDrive and Pull values for the SDC3 interface pins.

SDC3_HDRV_PULL_CTL

Bits	Name	Description
31:16	RESERVED	Reserved.
15:14	SDC3_CLK_PULL	SDC3 CLK Pull Value
13	SDC3_HYS_CTL	Enable/Disable for additional pad hysteresis. 0x0: Disable 0x1: Enable
12:11	SDC3_CMD_PULL	SDC3 CMD Pull Value
10:9	SDC3_DATA_PULL	SDC3 DATA Pull Value
8:6	SDC3_CLK_HDRV	SDC3 CLOCK HDrive Value
5:3	SDC3_CMD_HDRV	SDC3 CMD HDrive Value
2:0	SDC3_DATA_HDRV	SDC3 DATA HDrive Value

0x008020B4 MODE_PULL_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0005

This register controls the Pull values for the Mode Interface pins.

MODE_PULL_CTL

Bits	Name	Description
31:4	RESERVED	Reserved.
3:2	MODE_1_PULL	MODE 1 Pull Value
1:0	MODE_0_PULL	MODE 0 Pull Value

0x008020B8 GSBI4_3D_CAM_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

This register controls the I2C for the GSBI in 3D Camera mode.

GSBI4_3D_CAM_CTL

Bits	Name	Description
31:2	RESERVED	Reserved.
1	ENABLE_LEFT_I2C	Enable/Disable Instructions going to the Left I2C: 0x0: Disable 0x1: Enable
0	ENABLE_RIGHT_I2C	Enable/Disable Instructions going to the Right I2C: 0x0: Disable 0x1: Enable

0x008020BC GSBI7_3D_CAM_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

This register controls the I2C for the GSBI in 3D Camera mode.

GSBI7_3D_CAM_CTL

Bits	Name	Description
31:2	RESERVED	Reserved.
1	ENABLE_LEFT_I2C	Enable/Disable Instructions going to the Left I2C: 0x0: Disable 0x1: Enable
0	ENABLE_RIGHT_I2C	Enable/Disable Instructions going to the Right I2C: 0x0: Disable 0x1: Enable

0x008020C0 HSIC_STROBE_GPIO_PAD_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0002AA10

This register controls the configuration for the GPIO 81 HSIC STROBE pad, which can be configured for either HSIC or GPIO usage.

HSIC_STROBE_GPIO_PAD_CTL

Bits	Name	Description
31:28	RESERVED	Reserved.
27	CORE_CTL_EN	Control muxing between TLMM and HSIC core register control. NCNT, PCNT, and PULL control is muxed. The HSIC core controls are usb2_hsic_dat_keep_en, usb2_hsic_stb_keep_en, usb2_hsic_stb_dat_ncnt, usb2_hsic_stb_dat_pcnt. The resulting post mux pad controls are core_pull_gpio_88, gpio_88_ncnt, gpio_88_pcnt.
26	DDR_MODE	Control gpio_88_ddr_mode TLMM port.
25	LV_MODE	Control gpio_88_lv_mode TLMM port.
24	VM_SHIFT_EN	Control gpio_88_vm_shift_en TLMM port.
23	ODT_EN	Control gpio_88_odt_en TLMM port.
22:21	ODT	Control gpio_88_odt TLMM port.
20:18	DCC	Control gpio_88_dcc TLMM port.
17:16	NRXDEL	Control gpio_88_nrxdel TLMM port.
15:14	PRXDEL	Control gpio_88_prxdel TLMM port.
13:12	NSLEW	Control gpio_88_nslew TLMM port.
11:10	PSLEW	Control gpio_88_pslew TLMM port.
9:5	NCNT	Control gpio_88_ncnt TLMM port.
4:0	PCNT	Control gpio_88_pcnt TLMM port.

0x008020C4 HSIC_DATA_GPIO_PAD_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0002AA10

This register controls the configuration for the GPIO 89 HSIC DATA pad, which can be configured for either HSIC or GPIO usage.

HSIC_DATA_GPIO_PAD_CTL

Bits	Name	Description
31:28	RESERVED	Reserved.

HSIC_DATA_GPIO_PAD_CTL (cont.)

Bits	Name	Description
27	CORE_CTL_EN	Control muxing between TLMM and HSIC core register control. NCNT, PCNT, and PULL control is muxed. The HSIC core controls are usb2_hsic_dat_keep_en, usb2_hsic_stb_keep_en, usb2_hsic_stb_dat_ncnt, usb2_hsic_stb_dat_pcnt. The resulting post mux pad controls are core_pull_gpio_89, gpio_89_ncnt, gpio_89_pcnt.
26	DDR_MODE	Control gpio_89_ddr_mode TLMM port.
25	LV_MODE	Control gpio_89_lv_mode TLMM port.
24	VM_SHIFT_EN	Control gpio_89_vm_shift_en TLMM port.
23	ODT_EN	Control gpio_89_odt_en TLMM port.
22:21	ODT	Control gpio_89_odt TLMM port.
20:18	DCC	Control gpio_89_dcc TLMM port.
17:16	NRXDEL	Control gpio_89_nrxdel TLMM port.
15:14	PRXDEL	Control gpio_89_prxdel TLMM port.
13:12	NSLEW	Control gpio_89_nslew TLMM port.
11:10	PSLEW	Control gpio_89_pslew TLMM port.
9:5	NCNT	Control gpio_89_ncnt TLMM port.
4:0	PCNT	Control gpio_89_pcnt TLMM port.

0x008020C8 HSIC_CAL_PAD_CTL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x00000000

This register controls the configuration for the HSIC CAL pad.

HSIC_CAL_PAD_CTL

Bits	Name	Description
31:4	RESERVED	Reserved.
3	DDR_MODE	Control hsic_cal_ddr_mode TLMM port.
2	LV_MODE	Control hsic_cal_lv_mode TLMM port.
1:0	IMP_SEL	Control hsic_cal_imp_sel TLMM port.

0x008020CC RGB_HDRV_CTL

Type: Read/Write
Clock: CC_TLMM_CLK
Reset State: 0x00000000

This register controls the HDrive values for the LCD Interface pins.

RGB_HDRV_CTL

Bits	Name	Description
31:15	RESERVED	Reserved
14:12	RGB_CLK_HDRV	RGB CLK HDrive Value
11:9	RGB_DEN_HDRV	RGB DEN HDrive Value
8:6	RGB_VSYNC_HDRV	RGB VSYNC HDrive Value
5:3	RGB_HSYNC_HDRV	RGB HSYNC HDrive Value
2:0	RGB_DATA_HDRV	RGB Data HDrive Value

0x008020D0 GSBI1_UART_I2C_SEL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI1_UART_I2C_SEL register selects which GPIO the GSBI1 UART RX and I2C interfaces are on.

GSBI1_UART_I2C_SEL

Bits	Name	Description
31:2	RESERVED	Reserved
1	GSBI1_I2C_SEL	Select between standard GSBI1 and copy GSBI1 I2C interface on GPIO: 0x0: GSBI1 0x1: GSB1_I2C_RX
0	GSBI1_UART_SEL	Select between standard GSBI1 and copy GSBI1 UART RX interface on GPIO: 0x0: GSBI1 0x1: GSBI1_UART_RX

0x008020D4 GSBI2_UART_SEL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI2_UART_SEL register selects which GPIO the GSBI2 UART RX interface is on.

GSBI2_UART_SEL

Bits	Name	Description
31:1	RESERVED	Reserved
0	GSBI2_UART_SEL	Select between standard GSBI2 and copy GSBI2 UART RX interface on GPIO: 0x0: GSBI2 0x1: GSBI2_UART_RX

0x008020D8 GSBI3_UART_SEL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI3_UART_SEL register selects which GPIO the GSBI3 4 Wire UART interface is on.

GSBI3_UART_SEL

Bits	Name	Description
31:1	RESERVED	Reserved
0	GSBI3_UART_SEL	Select between standard GSBI3 and copy GSBI3 UART interface on GPIO: 0x0: GSBI3 0x1: GSBI3_UART

0x008020DC GSBI4_UART_I2C_SEL

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GSBI4_UART_I2C_SEL register selects which GPIO the GSBI4 2 Wire UART and I2C interfaces are on.

GSBI4_UART_I2C_SEL

Bits	Name	Description
31:2	RESERVED	Reserved
1	GSBI4_I2C_SEL	Select between standard GSBI4 and copy GSBI4 I2C interface on GPIO: 0x0: GSBI4 0x1: GSBI4_I2C
0	GSBI4_UART_SEL	Select between standard GSBI4 and copy GSBI4 UART interface on GPIO: 0x0: GSBI4 0x1: GSBI4_UART

0x00802100+ 0x4*n DIR_CONN_INTRn_POLARITY, n=[0..21]

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0001

The Direct Connect Interrupt Polarity registers control the polarity for each Direct Connect Interrupt. The polarity resets to active to high.

DIR_CONN_INTRn_POLARITY

Bits	Name	Description
31:1	RESERVED	Reserved.
0	POLARITY	Controls the Polarity Detection for the Direct Connect Interrupt. Polarity 1 corresponds to active high Polarity 0 corresponds to active low. 0x1: Polarity 1 0x0: Polarity 0

3.2.1.3 GPIO Banked registers

0x00803000 GPIO_OUT_0

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OUT_0 register controls the output values of GPIO[31:0]. This register is designed for BIT BANG or fast configuration of multiple output bits.

GPIO_OUT_0

Bits	Name	Description
31:0	GPIO_OUT_31_0	Output values for GPIO[31:0].

0x00803004 GPIO_OUT_1

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OUT_1 register controls the output values of GPIO[63:32]. This register is designed for BIT BANG or fast configuration of multiple output bits.

GPIO_OUT_1

Bits	Name	Description
31:0	GPIO_OUT_63_32	Output values for GPIO[63:32].

0x00803008 GPIO_OUT_2

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OUT_2 register controls the output values of GPIO[89:64]. This register is designed for BIT BANG or fast configuration of multiple output bits.

GPIO_OUT_2

Bits	Name	Description
25:0	GPIO_OUT_89_64	Output values for GPIO[89:64].

0x00803020 GPIO_OUT_CLR_0

Type: Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OUT_CLR_0 register bits can be used to clear (0) the output values of GPIO[31:0]. Once a CLR bit is written to ’1’, the corresponding GPIO output will be cleared to ’0’. The CLR bit will then automatically return to ’0’ so that it can be used again. This register is designed for BIT BANG or fast configuration of multiple output bits and alleviates the need for a read-modify-write operation.

GPIO_OUT_CLR_0

Bits	Name	Description
31:0	GPIO_OUT_CLR_31_0	Clear bits for GPIO[31:0] output values.

0x00803024 GPIO_OUT_CLR_1

Type: Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OUT_CLR_1 register bits can be used to clear (0) the output values of GPIO[63:32]. Once a CLR bit is written to ’1’, the corresponding GPIO output will be cleared to ’0’. The CLR bit will then automatically return to ’0’ so that it can be used again. This register is designed for BIT BANG or fast configuration of multiple output bits and alleviates the need for a read-modify-write operation.

GPIO_OUT_CLR_1

Bits	Name	Description
31:0	GPIO_OUT_CLR_63_32	Clear bits for GPIO[63:32] output values.

0x00803028 GPIO_OUT_CLR_2

Type: Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OUT_CLR_2 register bits can be used to clear (0) the output values of GPIO[89:64]. Once a CLR bit is written to ’1’, the corresponding GPIO output will be cleared to ’0’. The CLR bit will then automatically return to ’0’ so that it can be used again. This register is designed for BIT BANG or fast configuration of multiple output bits and alleviates the need for a read-modify-write operation.

GPIO_OUT_CLR_2

Bits	Name	Description
25:0	GPIO_OUT_CLR_89_64	Clear bits for GPIO[89:64] output values.

0x00803040 GPIO_OUT_SET_0

Type: Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OUT_SET_0 register bits can be used to set (1) the output values of GPIO[31:0]. Once a SET bit is written to ’1’, the corresponding GPIO output will be set to ’1’. The SET bit will then automatically return to ’0’ so that it can be used again. This register is designed for BIT BANG or fast configuration of multiple output bits and alleviates the need for a read-modify-write operation.

GPIO_OUT_SET_0

Bits	Name	Description
31:0	GPIO_OUT_SET_31_0	Set bits for GPIO[31:0] output values.

0x00803044 GPIO_OUT_SET_1

Type: Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OUT_SET_1 register bits can be used to set (1) the output values of GPIO[63:32]. Once a SET bit is written to ’1’, the corresponding GPIO output will be set to ’1’. The SET bit will then automatically return to ’0’ so that it can be used again. This register is designed for BIT BANG or fast configuration of multiple output bits and alleviates the need for a read-modify-write operation.

GPIO_OUT_SET_1

Bits	Name	Description
31:0	GPIO_OUT_SET_63_32	Set bits for GPIO[63:32] output values.

0x00803048 GPIO_OUT_SET_2

Type: Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OUT_SET_2 register bits can be used to set (1) the output values of GPIO[89:64]. Once a SET bit is written to ’1’, the corresponding GPIO output will be set to ’1’. The SET bit will then automatically return to ’0’ so that it can be used again. This register is designed for BIT BANG or fast configuration of multiple output bits and alleviates the need for a read-modify-write operation.

GPIO_OUT_SET_2

Bits	Name	Description
25:0	GPIO_OUT_SET_89_64	Set bits for GPIO[89:64] output values.

0x00803060 GPIO_IN_0

Type: Read
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_IN_0 register allows the input values for GPIO[31:0] to be read. This register is designed for reading multiple input bits.

GPIO_IN_0

Bits	Name	Description
31:0	GPIO_IN_31_0	GPIO[31:0] input values.

0x00803064 GPIO_IN_1

Type: Read
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_IN_1 register allows the input values for GPIO[63:32] to be read. This register is designed for reading multiple input bits.

GPIO_IN_1

Bits	Name	Description
31:0	GPIO_IN_63_32	GPIO[63:32] input values.

0x00803068 GPIO_IN_2

Type: Read
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_IN_2 register allows the input values for GPIO[89:64] to be read. This register is designed for reading multiple input bits.

GPIO_IN_2

Bits	Name	Description
25:0	GPIO_IN_89_64	GPIO[89:64] input values.

0x00803080 GPIO_OE_0

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OE_0 register controls the output enables of GPIO[31:0]. This register is designed for BIT BANG or fast configuration of multiple output bits.

GPIO_OE_0

Bits	Name	Description
31:0	GPIO_OE_31_0	GPIO[31:0] output enables.

0x00803084 GPIO_OE_1

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OE_1 register controls the output enables of GPIO[63:32]. This register is designed for BIT BANG or fast configuration of multiple output bits.

GPIO_OE_1

Bits	Name	Description
31:0	GPIO_OE_63_32	GPIO[63:32] output enables.

0x00803088 GPIO_OE_2

Type: Read/Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OE_2 register controls the output enables of GPIO[89:64]. This register is designed for BIT BANG or fast configuration of multiple output bits.

GPIO_OE_2

Bits	Name	Description
25:0	GPIO_OE_89_64	GPIO[89:64] output enables.

0x00803100 GPIO_OE_CLR_0

Type: Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OE_CLR_0 register bits can be used to clear (0) the output enables of GPIO[31:0]. Once a CLR bit is written to ’1’, the corresponding GPIO OE will be cleared to ’0’. The CLR bit will then automatically return to ’0’ so that it can be used again. This register is designed for BIT BANG or fast configuration of multiple OE bits and alleviates the need for a read-modify-write operation.

GPIO_OE_CLR_0

Bits	Name	Description
31:0	GPIO_OE_CLR_31_0	Clear bits for GPIO[31:0] output enables.

0x00803104 GPIO_OE_CLR_1

Type: Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OE_CLR_1 register bits can be used to clear (0) the output enables of GPIO[63:32]. Once a CLR bit is written to ’1’, the corresponding GPIO OE will be cleared to ’0’. The CLR bit will then automatically return to ’0’ so that it can be used again. This register is designed for BIT BANG or fast configuration of multiple OE bits and alleviates the need for a read-modify-write operation.

GPIO_OE_CLR_1

Bits	Name	Description
31:0	GPIO_OE_CLR_63_32	Clear bits for GPIO[63:32] output enables.

0x00803108 GPIO_OE_CLR_2

Type: Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OE_CLR_2 register bits can be used to clear (0) the output enables of GPIO[89:64]. Once a CLR bit is written to ’1’, the corresponding GPIO OE will be cleared to ’0’. The CLR bit will then automatically return to ’0’ so that it can be used again. This register is designed for BIT BANG or fast configuration of multiple OE bits and alleviates the need for a read-modify-write operation.

GPIO_OE_CLR_2

Bits	Name	Description
25:0	GPIO_OE_CLR_89_64	Clear bits for GPIO[89:64] output enables.

0x00803120 GPIO_OE_SET_0

Type: Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OE_SET_0 register bits can be used to set (1) the output enables of GPIO[31:0]. Once a SET bit is written to ’1’, the corresponding GPIO OE will be set to ’1’. The SET bit will then automatically return to ’0’ so that it can be used again. This register is designed for BIT BANG or fast configuration of multiple OE bits and alleviates the need for a read-modify-write operation.

GPIO_OE_SET_0

Bits	Name	Description
31:0	GPIO_OE_SET_31_0	Set bits for GPIO[31:0] output enables.

0x00803124 GPIO_OE_SET_1

Type: Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OE_SET_1 register bits can be used to set (1) the output enables of GPIO[63:32]. Once a SET bit is written to ’1’, the corresponding GPIO OE will be set to ’1’. The SET bit will then automatically return to ’0’ so that it can be used again. This register is designed for BIT BANG or fast configuration of multiple OE bits and alleviates the need for a read-modify-write operation.

GPIO_OE_SET_1

Bits	Name	Description
31:0	GPIO_OE_SET_63_32	Set bits for GPIO[63:32] output enables.

0x00803128 GPIO_OE_SET_2

Type: Write
Clock: CC_TLMM_HCLK
Reset State: 0x0000

The GPIO_OE_SET_2 register bits can be used to set (1) the output enables of GPIO[89:64]. Once a SET bit is written to ’1’, the corresponding GPIO OE will be set to ’1’. The SET bit will then automatically return to ’0’ so that it can be used again. This register is designed for BIT BANG or fast configuration of multiple OE bits and alleviates the need for a read-modify-write operation.

GPIO_OE_SET_2

Bits	Name	Description
25:0	GPIO_OE_SET_89_64	Set bits for GPIO[89:64] output enables.

3.3 IMEM Configuration Registers (0x00B00000 SYS_IMEM_BASE)

The following subsections describe the IMEM configuration registers.

0x00B00000 SYS_IMEM_IMEM_CONFIG

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00000001

General configuration register for IMEM. This register sets the IMEM accessibility for Graphics and AXI.

Power up value is based on parameters provided

NOTE

a. All banks are 8k x 64 in size.

b. GRP and AXI memory configurations are 64 bits wide.

c. If Graphics interface is not required, set the IMEM_CONFIG_POR parameter to all AXI setting (2'b01). The sharing scheme will then not apply.

SYS_IMEM_IMEM_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	IMEM_CONFIG	(Graphics Interface = 256kbytes) (AXI Interface (and trace) = 256kbytes) (Graphics Interface = 128kbytes) (AXI Interface (and trace) = 128kbytes) Banks 0 and 1 are allocated to Graphics. Banks 2 and 3 are allocated to AXI. (Graphics Interface = 128kbytes) (AXI Interface (and trace) = 128kbytes) Banks 0 and 1 are allocated to AXI. Banks 2 and 3 are allocated to Graphics. SW : RW, HW: R 0x0: All graphics (Dedicated all to Graphics) 0x1: All axi (Dedicated all to AXI) 0x2: 0_1_Graphics_2_3_AXI 0x3: 0_1_AXI_2_3_Graphics

3.3.1 IMEM AXI Trace Configuration registers

0x00B00004 SYS_IMEM_IMEM_AXI_TRACE_CONFIG

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00000000

This register is used to enable and control the AXI trace to IMEM.

SYS_IMEM_IMEM_AXI_TRACE_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	AXI_TRACE_ADDR_WRAP_EN	1-Enables AXI trace address to wrap
0	AXI_TRACE_EN	1-Enables AXI trace to IMEM

0x00B00008 SYS_IMEM_IMEM_AXI_TRACE_ADDR_CNTR

Type: Read
Clock: CORE_CLOCK
Reset State: 0x00000000

This register is used to read the AXI Trace Address counter value.

SYS_IMEM_IMEM_AXI_TRACE_ADDR_CNTR

Bits	Name	Description
31:16	RESERVED_BITS31_16	
15:0	AXI_TRACE_ADDR_CNTR	Current AXI Trace address

0x00B0000C SYS_IMEM_IMEM_AXI_TRACE_WRAP_STATUS

Type: Read
Clock: CORE_CLOCK
Reset State: 0x00000000

This register is used to read the AXI Trace Address wrap status bit.

SYS_IMEM_IMEM_AXI_TRACE_WRAP_STATUS

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	AXI_TRACE_WRAP_STATUS	0x1: AXI trace address wrapped 0x0: AXI trace address not wrapped

0x00B00010 SYS_IMEM_IMEM_AXI_BASE_ADDR_OFFSET

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00002A00

This register is used to set the AXI Base Address offset value in order to relocate the IMEM AXI memory within the space allowed by the interconnect. The POR value of this register is based on the parameter - IMEM_BASE_ADDRESS. In case of MPSS, this is set to 0x5800. This should be set to the upper 16 bits of the Imem base address. Based on the size of the Imem, the relevant bits of this register are used for decoding the address.

SYS_IMEM_IMEM_AXI_BASE_ADDR_OFFSET

Bits	Name	Description
31:16	RESERVED_BITS31_16	
15:0	IMEM_AXI_BASE_ADDRESS_OFFSET	IMEM AXI base address offset for decode

3.3.1.1 IMEM Syndrome registers

0x00B00020 SYS_IMEM_IMEM_ERR_ADDRESS_MS

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x000000000000

The IMEM_ERR_ADDRESS_MS register contains the upper bits of the address of the request that caused the bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, it will be locked until bit 8 of the ERR_CODE register is written to clear the error.

SYS_IMEM_IMEM_ERR_ADDRESS_MS

Bits	Name	Description
31:16	RESERVED_BITS31_16	

SYS_IMEM_IMEM_ERR_ADDRESS_MS (cont.)

Bits	Name	Description
15:0	ERROR_ADDRESS_31_16	Bits 31:16 of the address of the request that caused the bus error.

0x00B00024 SYS_IMEM_IMEM_ERR_ADDRESS_LS

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x00000000

The IMEM_ERR_ADDRESS_LS register contains the lower bits of the address of the request that caused the AXI GE bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, the register will be locked until bit 8 of the ERR_CODE register is written to clear the error.

SYS_IMEM_IMEM_ERR_ADDRESS_LS

Bits	Name	Description
31:16	RESERVED_BITS31_16	
15:3	ERROR_ADDRESS_15_3	Bits 15:3 of the address of the request that caused the bus error
2:0	RESERVED_BITS2_0	Reserved if not implemented otherwise include with error address.

0x00B00028 SYS_IMEM_IMEM_ERR_APACKET_MS

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x00000000

The IMEM_ERR_APACKET_MS register provides various data about the request that caused the AXI GE bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, it will be locked until bit 8 of the ERR_CODE register is written to clear the error.

SYS_IMEM_IMEM_ERR_APACKET_MS

Bits	Name	Description
31:20	RESERVED_BITS31_20	
19:18	ERROR_ALOCK_1_0	The ALOCK of the request that caused the bus error
17	ERROR_ABURST	The ABURST of the request that caused the bus error
16:12	ERROR_PORTID_4_0	The Port ID of the request that caused the bus error.
11:5	ERROR_ATID_6_0	The Transfer ID of the request that caused the bus error.

SYS_IMEM_IMEM_ERR_APACKET_MS (cont.)

Bits	Name	Description
4	ERROR_AWRITE	The awrite of the request that caused bus error
3:0	ERROR_ALEN	The burst length of the request that caused bus error

0x00B0002C SYS_IMEM_IMEM_ERR_APACKET_LS

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x00000000

The IMEM_ERR_APACKET_LS register provides various data about the request that caused the AXI GE bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, the register will be locked until bit 8 of the ERR_CODE register is written to clear the error.

SYS_IMEM_IMEM_ERR_APACKET_LS

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:9	ERROR_AMID_15_0	The master ID of the request that caused the bus error (The higher order bits will be set to 0 for MID width < 7)
8:5	ERROR_ATYPE_3_0	The ATYPE of the request that caused the bus error
4	ERROR_APROTNS	The APROTNS of the request that caused the bus error
3:0	RESERVED_BITS_3_0	

0x00B00030 SYS_IMEM_IMEM_ERR_CODE

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00000000

The IMEM_ERR_CODE register provides additional data about the bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, the register will be locked until bit 8 of the ERR_CODE register is written to clear the error.

Additionally, each slave or AXI interconnect which is capable of detecting an error is also required to have a single programmable register that can be used to optionally interrupt the ARM9 or Scorpion Processor core. This interrupt mechanism is required since write transfers may be posted on the bus and the AXI transfer may complete prior to the occurrence of the error in the AXI interconnect or slave device. The interrupt from the AXI interconnect and the AXI slave devices will be directed to both the ARM9 and application processor's interrupt controllers. The interrupt output of the slave device shall be driven from bit 3 of the ERR_CODE register above. To clear the interrupt, it will be necessary to clear the ERR_CODE register by writing to bit 8

(ERROR_CLEAR) of the ERR_CODE register. This will clear the ERROR field (bit 3) and also unlock the ERR_ADDRESS, ERR_APACKET, and ERR_CODE registers so that a subsequent error can be recoded in these registers.

SYS_IMEM_IMEM_ERR_CODE

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8	ERROR_CLEAR	Writing a ‘1’ to this bit will clear the bus error status bit.
7:4	RESERVED_BIT7_4	
3	ERROR	Error Status bit to indicate that an error has occurred.
2	RESERVED_BIT2	
1	MPU_ERROR	0x1: memory protection error
0	ADDRESS_DECODE_ERROR	0x1: slave address decode error

0x00B00034 SYS_IMEM_IMEM_ERR_IRQ_MSK

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00000001

This register is used to block interrupt to ARM9 or Scorpion.

SYS_IMEM_IMEM_ERR_IRQ_MSK

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	PROCESSOR_IRQ_MASK	1 disables bus error interrupt to Processor

0x00B00040 SYS_IMEM_IMEM_CLK_ON_EN

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x00000000

This register is used to enable/disable the clock_on circuitry. If disabled, clock on is always high.

SYS_IMEM_IMEM_CLK_ON_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	

SYS_IMEM_IMEM_CLK_ON_EN (cont.)

Bits	Name	Description
1	AHB_CLK_ON_EN	1 will enable AHB clock on
0	CLK_ON_EN	1 will enable the timer countdown

0x00B00044 SYS_IMEM_IMEM_CLK_ON_TIME

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x000003FF

This register sets the starting time for a binary countdown in clock cycles.

SYS_IMEM_IMEM_CLK_ON_TIME

Bits	Name	Description
31:10	RESERVED_BITS31_1	
9:0	CLK_ON_TIME_9_0	10 bits to count down from, for a max of 1024

0x00B00048 SYS_IMEM_IMEM_FSCGC_TIMERS

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x000000FF

This register sets the starting time for a binary countdown in clock cycles.

SYS_IMEM_IMEM_FSCGC_TIMERS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	WAKEUP_COUNTER_3_0	4 bit count down, must be 20ns
3:0	TO_SLEEP_COUNTER_3_0	4 bit count down, must be 20ns

0x00B0004C SYS_IMEM_IMEM_FSCGC_CONTROL

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x000000FF

Controls for head switch and periphery within IMEM.

SYS_IMEM_IMEM_FSCGC_CONTROL

Bits	Name	Description
31:12	RESERVED_BITS31_12	
11:8	HALT_CLOCK_11_8	Gates the clock to individual RAMS
7:4	CORE_ON_7_4	RAM Core will remain on if this is 1 (for individual rams)
3:0	PERIF_ON_3_0	RAM Periphery will remain on if this is 1 (for individual rams)

0x00B00050 SYS_IMEM_IMEM_EX_FSCGC_CONTROL

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x0000FFFF

Controls for head switch and perfory outside of IMEM.

SYS_IMEM_IMEM_EX_FSCGC_CONTROL

Bits	Name	Description
31:22	RESERVED_BITS31_24	
23:16	HALT_CLOCK_7_0	Gates the clock to individual RAMS
15:8	CORE_ON_7_0	RAM Core will remain on if this is 1 (for individual rams)
7:0	PERIF_ON_7_0	RAM Periphery will remain on if this is 1 (for individual rams)

0x00B00054 SYS_IMEM_IMEM_RAM_CONFIG

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x00000000

This register configures the access to the external RAM interface.

SYS_IMEM_IMEM_RAM_CONFIG

Bits	Name	Description
31:3	RESERVED_BITS31_3	
1:0	EX_RAM_CONFIG_1_0	External ram access configuration: 11: NO external RAM allocated to AXI 0x0: No External RAM allocated to AXI 0x1: 256K of external RAM allocated to AXI 0x2: All external RAM allocated to AXI

3.3.1.2 Internal Memory Misc

0x00B00038 SYS_IMEM_IMEM_MEM_ACC_CFG

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x00000000

This register is used to configure the acc pins of the RAM for programming the sense amp.

SYS_IMEM_IMEM_MEM_ACC_CFG

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	ACC_CFG	

3.3.2 XPU Registers

0x00B01000+ 4*n SYS_IMEM_MPU_PRTn_RACR, n=[0..7]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU. These registers include a single bit per VMID granting read access

SYS_IMEM_MPU_PRTn_RACR

Bits	Name	Description
31:0	RE	Read enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read access to the registers in the associated resource group.

0x00B01400+ 4*n SYS_IMEM_MPU_PRTn_WACR, n=[0..7]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

These registers exist only for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU.

SYS_IMEM_MPU_PRTn_WACR

Bits	Name	Description
31:0	WE	Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID write access to the registers in the associated resource group.

0x00B01800+4*n SYS_IMEM_MPU_PRTn_START, n=[0..7]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition Start Address Register. This register contains the start address of the partition. Only the bit numbers indicated by MPU_IDR[MSb] through MPU_IDR[LSb] are valid and physically exist.

SYS_IMEM_MPU_PRTn_START

Bits	Name	Description
31:25	RESERVED_31_25	Reserved
24:12	ADDR	MPU Partition Start Address
11:0	RESERVED_11_0	Reserved

0x00B01C00+4*n SYS_IMEM_MPU_PRTn_END, n=[0..7]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition End Address Register. This register contains the start address of the partition.Only the bit numbers indicated by MPU_IDR[MSB] through MPU_IDR[LSB] are valid and physically exist.

SYS_IMEM_MPU_PRTn_END

Bits	Name	Description
31:25	RESERVED_31_25	Reserved
24:12	ADDR	MPU Partition End Address
11:0	RESERVED_11_0	Reserved

0x00B01F80 SYS_IMEM_MPU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Configuration Register: This register includes fields governing various MPU behaviors.

SYS_IMEM_MPU_CR

Bits	Name	Description
31:2	RESERVED31_2	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set MPU_ESR. MPU_EAR and MPU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set MPU_ESR. MPU_EAR and MPU_ESYNR0 updated with address and syndrome of error.
2	MPUEIE	MPU Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the MPU. Interrupt output is asserted if MPU_CR[MPUEIE] = 1 and any bit is set in MPU_ESR.
1	MPUERE	MPU Error Report Enable. MPUERE = 0 causes the MPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master. MPUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective MPU port. Errors from either port are terminated by the MPU as RAZ/WI Both client and configuration port errors are recorded in MPU_ESR, independent of the value of MPU_CR[MPUERE]
0	MPUE	MPU Enable. Governs whether MPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures MPU and the MID to VMID mapping tables.

0x00B01F84 SYS_IMEM_MPU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the MPU, for both the client port and the configuration port.

SYS_IMEM_MPU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x00B01F88 SYS_IMEM_MPU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the MPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the MPU's interrupt output (when enabled by MPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the MPU_ESYNRn registers, which are merely the 'syndrome' of an error indicated by MPU_ESR.

SYS_IMEM_MPU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) 'lock' upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x00B01F8C SYS_IMEM_MPU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Restore Register. This register is an aliased address for the MPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

SYS_IMEM_MPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) 'lock' upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x00B01F90 SYS_IMEM_MPU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

SYS_IMEM_MPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x00B01F94 SYS_IMEM_MPU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

SYS_IMEM_MPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x00B01FF4 SYS_IMEM_MPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

MPU Revision Register: This register provides major/minor revision codes for the implementation.

SYS_IMEM_MPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x00B01FF8 SYS_IMEM_MPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x180C2C07

MPU ID Register: Read-only register that defines various configuration attributes of the MPU instance.

SYS_IMEM_MPU_IDR

Bits	Name	Description
31:29	RESERVED31_29	Reserved
28:24	MSB	Indicates most significant address bit number used in START/END address comparisons.
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used in START/END address comparisons.
15:14	RESERVED15_12	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only MPU_PRTn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate MPU_PRTn_RACR and MPU_PRTn_WACR registers govern read vs. write access. For single VMID, MPU_PRTn_ACR registers include separate 5-bit read/write vs. read-only ‘owner’ VMID fields

SYS_IMEM_MPU_IDR (cont.)

Bits	Name	Description
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. MPU_PRTn_ACR registers indicate single 5 bit 'owner' VMID field for governing access. MV=1 : indicates multi-VMD type access control. MPU_PRTn_xACR registers include separate bit per VMID (32 bits) for governing access.
9:8	RESERVED9_8	Reserved
7:0	NPRT	Number of partitions. Indicates the number of partitions (minus 1) supported by the MPU. Values range from 0-223 (1-224 partitions)

0x00B01FFC SYS_IMEM_MPU_MPU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

MPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the MPU (including the MPU_MPU_ACR itself).

SYS_IMEM_MPU_MPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the MPU's 4KB address region (including the MPU_MPU_ACR itself). For single VMID type MPUs (MPU_IDR[MV] = 0) the MPU_MPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

4 Chip Core Top XPU Registers

4.1 Overview

Table 4-1 chip_core_top_XPUs Bases

Base Name	Parent	Address
LPASS_XPU_MPU_PRTn_RACR	LPASS_XPU_BASE	0x17000000
KPSS_XPU_MPU_PRTn_RACR	KPSS_XPU_BASE	0x17100000
GSS_XPU_MPU_PRTn_RACR	GSS_XPU_BASE	0x17200000
SATA_APU_RGn_ACR	SATA_XPU_CFG_BASE	0x1B300000
CE3_APU_RGn_ACR	CE3_XPU_CFG_BASE	0x17500000

4.2 LPASS XPU Registers (0x17000000 LPASS_XPU_BASE)

This section contains the LPASS XPU registers.

0x17000000+ 4*n LPASS_XPU_MPU_PRTn_RACR, n=[0..7]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU. These registers include a single bit per VMID granting read access

LPASS_XPU_MPU_PRTn_RACR

Bits	Name	Description
31:0	RE	Read enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read access to the registers in the associated resource group.

0x17000400+ 4*n LPASS_XPU_MPU_PRTn_WACR, n=[0..7]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

These registers exist only for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU.

LPASS_XPU_MPU_PRTn_WACR

Bits	Name	Description
31:0	WE	Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID write access to the registers in the associated resource group.

0x17000800+ 4*n LPASS_XPU_MPU_PRTn_START, n=[0..7]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition Start Address Register. This register contains the start address of the partition. Only the bit numbers indicated by MPU_IDR[MSb] through MPU_IDR[LSb] are valid and physically exist.

LPASS_XPU_MPU_PRTn_START

Bits	Name	Description
31:24	RESERVED_31_24	Reserved
23:12	ADDR	MPU Partition Start Address
11:0	RESERVED_11_0	Reserved

0x17000C00+4*n LPASS_XPU_MPU_PRTn_END, n=[0..7]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition End Address Register. This register contains the start address of the partition.Only the bit numbers indicated by MPU_IDR[MSB] through MPU_IDR[LSB] are valid and physically exist.

LPASS_XPU_MPU_PRTn_END

Bits	Name	Description
31:24	RESERVED_31_24	Reserved
23:12	ADDR	MPU Partition End Address
11:0	RESERVED_11_0	Reserved

0x17000F80 LPASS_XPU_MPU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Configuration Register: This register includes fields governing various MPU behaviors.

LPASS_XPU_MPU_CR

Bits	Name	Description
31:2	RESERVED31_2	Reserved

LPASS_XPU_MPU_CR (cont.)

Bits	Name	Description
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set MPU_ESR. MPU_EAR and MPU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set MPU_ESR. MPU_EAR and MPU_ESYNR0 updated with address and syndrome of error.
2	MPUEIE	MPU Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the MPU. Interrupt output is asserted if MPU_CR[MPUEIE] = 1 and any bit is set in MPU_ESR.
1	MPUERE	MPU Error Report Enable. MPUERE = 0 causes the MPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master. MPUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective MPU port. Errors from either port are terminated by the MPU as RAZ/WI Both client and configuration port errors are recorded in MPU_ESR, independent of the value of MPU_CR[MPUERE]
0	MPUE	MPU Enable. Governs whether MPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures MPU and the MID to VMID mapping tables.

0x17000F84 LPASS_XPU_MPU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the MPU, for both the client port and the configuration port. Client port addresses are 32 bits width and configuration port addresses are 12 bits wide (the width of the configuration address port).

LPASS_XPU_MPU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x17000F88 LPASS_XPU_MPU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the MPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the MPU's interrupt output (when enabled by MPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the MPU_ESYNRn registers, which are merely the "syndrome" of an error indicated by MPU_ESR.

LPASS_XPU_MPU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x17000F8C LPASS_XPU_MPU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Restore Register. This register is an aliased address for the MPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

LPASS_XPU_MPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x17000F90 LPASS_XPU_MPU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

LPASS_XPU_MPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x17000F94 LPASS_XPU_MPU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

LPASS_XPU_MPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x17000FF4 LPASS_XPU_MPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

MPU Revision Register: This register provides major/minor revision codes for the implementation.

LPASS_XPU_MPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x17000FF8 LPASS_XPU_MPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x170C2C07

MPU ID Register: Read-only register that defines various configuration attributes of the MPU instance.

LPASS_XPU_MPU_IDR

Bits	Name	Description
31:29	RESERVED31_29	Reserved
28:24	MSB	Indicates most significant address bit number used in START/END address comparisons.
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used in START/END address comparisons.
15:14	RESERVED15_12	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only MPU_PRTn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate MPU_PRTn_RACR and MPU_PRTn_WACR registers govern read vs. write access. For single VMID, MPU_PRTn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields

LPASS_XPU_MPU_IDR (cont.)

Bits	Name	Description
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. MPU_PRTn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMD type access control. MPU_PRTn_xACR registers include separate bit per VMID (32 bits) for governing access.
9	RESERVED9	Reserved
8:0	NPRT	Number of partitions. Indicates the number of partitions (minus 1) supported by the MPU. Values range from 0-223 (1-224 partitions)

0x17000FFC LPASS_XPU_MPU_MPU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

MPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the MPU (including the MPU_MPU_ACR itself).

LPASS_XPU_MPU_MPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the MPU's 4KB address region (including the MPU_MPU_ACR itself). For single VMID type MPUs (MPU_IDR[MV] = 0) the MPU_MPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

4.3 KPSS XPU Registers (0x17100000 KPSS_XPU_BASE)

This section contains the KPSS XPU registers.

0x17100000+ 4*n KPSS_XPU_MPU_PRTn_RACR, n=[0..7]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU. These registers include a single bit per VMID granting read access

KPSS_XPU_MPU_PRTn_RACR

Bits	Name	Description
31:0	RE	Read enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read access to the registers in the associated resource group.

0x17100400+ 4*n KPSS_XPU_MPU_PRTn_WACR, n=[0..7]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

These registers exist only for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU.

KPSS_XPU_MPU_PRTn_WACR

Bits	Name	Description
31:0	WE	Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID write access to the registers in the associated resource group.

0x17100800+ 4*n KPSS_XPU_MPU_PRTn_START, n=[0..7]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition Start Address Register. This register contains the start address of the partition. Only the bit numbers indicated by MPU_IDR[MSb] through MPU_IDR[LSb] are valid and physically exist.

KPSS_XPU_MPU_PRTn_START

Bits	Name	Description
31:24	RESERVED_31_24	Reserved
23:12	ADDR	MPU Partition Start Address
11:0	RESERVED_11_0	Reserved

0x17100C00+4*n KPSS_XPU_MPU_PRTn_END, n=[0..7]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition End Address Register. This register contains the start address of the partition.Only the bit numbers indicated by MPU_IDR[MSB] through MPU_IDR[LSB] are valid and physically exist.

KPSS_XPU_MPU_PRTn_END

Bits	Name	Description
31:24	RESERVED_31_24	Reserved
23:12	ADDR	MPU Partition End Address
11:0	RESERVED_11_0	Reserved

0x17100F80 KPSS_XPU_MPU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Configuration Register: This register includes fields governing various MPU behaviors.

KPSS_XPU_MPU_CR

Bits	Name	Description
31:2	RESERVED31_2	Reserved

KPSS_XPU_MPU_CR (cont.)

Bits	Name	Description
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresse) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set MPU_ESR. MPU_EAR and MPU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set MPU_ESR. MPU_EAR and MPU_ESYNR0 updated with address and syndrome of error.
2	MPUEIE	MPU Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the MPU. Interrupt output is asserted if MPU_CR[MPUEIE] = 1 and any bit is set in MPU_ESR.
1	MPUERE	MPU Error Report Enable. MPUERE = 0 causes the MPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master. MPUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective MPU port. Errors from either port are terminated by the MPU as RAZ/WI Both client and configuration port errors are recorded in MPU_ESR, independent of the value of MPU_CR[MPUERE]
0	MPUE	MPU Enable. Governs whether MPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures MPU and the MID to VMID mapping tables.

0x17100F84 KPSS_XPU_MPU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the MPU, for both the client port and the configuration port. Client port addresses are 32 bits width and configuration port addresses are 12 bits wide (the width of the configuration address port).

KPSS_XPU_MPU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x17100F88 KPSS_XPU_MPU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the MPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the MPU's interrupt output (when enabled by MPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the MPU_ESYNRn registers, which are merely the "syndrome" of an error indicated by MPU_ESR.

KPSS_XPU_MPU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x17100F8C KPSS_XPU_MPU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Restore Register. This register is an aliased address for the MPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

KPSS_XPU_MPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x17100F90 KPSS_XPU_MPU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

KPSS_XPU_MPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x17100F94 KPSS_XPU_MPU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

KPSS_XPU_MPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant reuqest
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x17100FF4 KPSS_XPU_MPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

MPU Revision Register: This register provides major/minor revision codes for the implementation.

KPSS_XPU_MPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x17100FF8 KPSS_XPU_MPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x170C2C07

MPU ID Register: Read-only register that defines various configuration attributes of the MPU instance.

KPSS_XPU_MPU_IDR

Bits	Name	Description
31:29	RESERVED31_29	Reserved
28:24	MSB	Indicates most significant address bit number used in START/END address comparisons.
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used in START/END address comparisons.
15:14	RESERVED15_12	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full acces vs. no access type. Only MPU_PRTn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate MPU_PRTn_RACR and MPU_PRTn_WACR registers govern read vs. write access. For single VMID, MPU_PRTn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields

KPSS_XPU_MPU_IDR (cont.)

Bits	Name	Description
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. MPU_PRTn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMD type access control. MPU_PRTn_xACR registers include separate bit per VMID (32 bits) for governing access.
9	RESERVED9	Reserved
8:0	NPRT	Number of partitions. Indicates the number of partitions (minus 1) supported by the MPU. Values range from 0-223 (1-224 partitions)

0x17100FFC KPSS_XPU_MPU_MPU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

MPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the MPU (including the MPU_MPU_ACR itself).

KPSS_XPU_MPU_MPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the MPU's 4KB address region (including the MPU_MPU_ACR itself). For single VMID type MPUs (MPU_IDR[MV] = 0) the MPU_MPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

4.4 GSS XPU Registers (0x17200000 GSS_XPU_BASE)

This section contains the GSS XPU registers.

0x17200000+ 4*n GSS_XPU_MPU_PRTn_RACR, n=[0..19]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU. These registers include a single bit per VMID granting read access

GSS_XPU_MPU_PRTn_RACR

Bits	Name	Description
31:0	RE	Read enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read access to the registers in the associated resource group.

0x17200400+ 4*n GSS_XPU_MPU_PRTn_WACR, n=[0..19]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

These registers exist only for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU.

GSS_XPU_MPU_PRTn_WACR

Bits	Name	Description
31:0	WE	Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID write access to the registers in the associated resource group.

0x17200800+ 4*n GSS_XPU_MPU_PRTn_START, n=[0..19]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition Start Address Register. This register contains the start address of the partition. Only the bit numbers indicated by MPU_IDR[MSb] through MPU_IDR[LSb] are valid and physically exist.

GSS_XPU_MPU_PRTn_START

Bits	Name	Description
31:29	RESERVED_31_29	Reserved
28:10	ADDR	MPU Partition Start Address
9:0	RESERVED_9_0	Reserved

0x17200C00+4*n GSS_XPU_MPU_PRTn_END, n=[0..19]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition End Address Register. This register contains the start address of the partition.Only the bit numbers indicated by MPU_IDR[MSB] through MPU_IDR[LSB] are valid and physically exist.

GSS_XPU_MPU_PRTn_END

Bits	Name	Description
31:29	RESERVED_31_29	Reserved
28:10	ADDR	MPU Partition End Address
9:0	RESERVED_9_0	Reserved

0x17200F80 GSS_XPU_MPU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Configuration Register: This register includes fields governing various MPU behaviors.

GSS_XPU_MPU_CR

Bits	Name	Description
31:2	RESERVED31_2	Reserved

GSS_XPU_MPU_CR (cont.)

Bits	Name	Description
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set MPU_ESR. MPU_EAR and MPU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set MPU_ESR. MPU_EAR and MPU_ESYNR0 updated with address and syndrome of error.
2	MPUEIE	MPU Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the MPU. Interrupt output is asserted if MPU_CR[MPUEIE] = 1 and any bit is set in MPU_ESR.
1	MPUERE	MPU Error Report Enable. MPUERE = 0 causes the MPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master. MPUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective MPU port. Errors from either port are terminated by the MPU as RAZ/WI Both client and configuration port errors are recorded in MPU_ESR, independent of the value of MPU_CR[MPUERE]
0	MPUE	MPU Enable. Governs whether MPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures MPU and the MID to VMID mapping tables.

0x17200F84 GSS_XPU_MPU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the MPU, for both the client port and the configuration port. Client port addresses are 32 bits width and configuration port addresses are 12 bits wide (the width of the configuration address port).

GSS_XPU_MPU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x17200F88 GSS_XPU_MPU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the MPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the MPU's interrupt output (when enabled by MPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the MPU_ESYNRn registers, which are merely the "syndrome" of an error indicated by MPU_ESR.

GSS_XPU_MPU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x17200F8C GSS_XPU_MPU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Restore Register. This register is an aliased address for the MPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

GSS_XPU_MPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x17200F90 GSS_XPU_MPU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

GSS_XPU_MPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x17200F94 GSS_XPU_MPU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

GSS_XPU_MPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x17200FF4 GSS_XPU_MPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

MPU Revision Register: This register provides major/minor revision codes for the implementation.

GSS_XPU_MPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x17200FF8 GSS_XPU_MPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x1C0A2C13

MPU ID Register: Read-only register that defines various configuration attributes of the MPU instance.

GSS_XPU_MPU_IDR

Bits	Name	Description
31:29	RESERVED31_29	Reserved
28:24	MSB	Indicates most significant address bit number used in START/END address comparisons.
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used in START/END address comparisons.
15:14	RESERVED15_12	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only MPU_PRTn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate MPU_PRTn_RACR and MPU_PRTn_WACR registers govern read vs. write access. For single VMID, MPU_PRTn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields

GSS_XPU_MPU_IDR (cont.)

Bits	Name	Description
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. MPU_PRTn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMD type access control. MPU_PRTn_xACR registers include separate bit per VMID (32 bits) for governing access.
9	RESERVED9	Reserved
8:0	NPRT	Number of partitions. Indicates the number of partitions (minus 1) supported by the MPU. Values range from 0-223 (1-224 partitions)

0x17200FFC GSS_XPU_MPU_MPU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

MPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the MPU (including the MPU_MPU_ACR itself).

GSS_XPU_MPU_MPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the MPU's 4KB address region (including the MPU_MPU_ACR itself). For single VMID type MPUs (MPU_IDR[MV] = 0) the MPU_MPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

4.5 SATA XPU Registers (0x1B300000 SATA_XPU_CFG_BASE)

This section contains the SATA XPU registers.

0x1B300000+4*n SATA_APU_RGn_ACR, n=[0..0]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 01, i.e., a single VMID, read/write access vs. read-only access permission type APU. These registers include 2 separate 5 bit "owner" VMID fields

SATA_APU_RGn_ACR

Bits	Name	Description
31:26	RESERVED31_26	Reserved.
25	ROGE	Read-only global enable: Opens up read-only access for this resource group to all VMIDs if: ROGE | (ROE & (VMID = ROVMID)) | APU_APU_ACR[VMID] = 1
24	ROE	Read-only enable. This is a "valid" bit for the ROVMID field.
23:21	RESERVED23_21	Reserved
20:16	ROVMID	Read-only VMID. Specifies "owner" VMID with read-only access to the registers in the associated resource group.
15:10	RESERVED15_10	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | APU_APU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a "valid" bit for the RWVMID field
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies "owner" VMID with full read/write access to the registers in the associated resource group.

0x1B300F80 SATA_APU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

SATA_APU_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set APU_ESR. APU_EAR and APU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set APU_ESR. APU_EAR and APU_ESYNR0 updated with address and syndrome of error.
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x1B300F84 SATA_APU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port.

SATA_APU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x1B300F88 SATA_APU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the APU_ESYNRn registers, which are merely the "syndrome" of an error indicated by APU_ESR.

SATA_APU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x1B300F8C SATA_APU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

SATA_APU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x1B300F90 SATA_APU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

SATA_APU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x1B300F94 SATA_APU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

SATA_APU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x1B300FF4 SATA_APU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

SATA_APU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved

SATA_APU_REV (cont.)

Bits	Name	Description
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x1B300FF8 SATA_APU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x00001800

APU ID Register: Read-only register that defines various configuration attributes of the APU instance.

SATA_APU_IDR

Bits	Name	Description
31:29	RESERVED31_21	Reserved
28:24	MSB	Indicates most significant address bit number used to select a resource group
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.

SATA_APU_IDR (cont.)

Bits	Name	Description
9:8	RESERVED9_8	Reserved
7:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

0x1B300FFC SATA_APU_APU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

APU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the APU (including the APU_APU_ACR itself).

SATA_APU_APU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the APU's 4KB address region (including the APU_APU_ACR itself). For single VMID type APU (APU_IDR[MV] = 0) the APU_APU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

4.6 CE3 XPU Registers (0x17500000 CE3_XPU_CFG_BASE)

This section contains the CE3 XPU registers.

0x17500000+4*n CE3_APU_RGn_ACR, n=[0..0]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 01, i.e., a single VMID, read/write access vs. read-only access permission type APU. These registers include 2 separate 5 bit "owner" VMID fields

CE3_APU_RGn_ACR

Bits	Name	Description
31:26	RESERVED31_26	Reserved.
25	ROGE	Read-only global enable: Opens up read-only access for this resource group to all VMIDs if: ROGE | (ROE & (VMID = ROVMID)) | APU_APU_ACR[VMID] = 1
24	ROE	Read-only enable. This is a "valid" bit for the ROVMID field.
23:21	RESERVED23_21	Reserved
20:16	ROVMID	Read-only VMID. Specifies "owner" VMID with read-only access to the registers in the associated resource group.
15:10	RESERVED15_10	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | APU_APU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a "valid" bit for the RWVMID field
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies "owner" VMID with full read/write access to the registers in the associated resource group.

0x17500F80 CE3_APU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

CE3_APU_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set APU_ESR. APU_EAR and APU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set APU_ESR. APU_EAR and APU_ESYNR0 updated with address and syndrome of error.
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x17500F84 CE3_APU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port.

CE3_APU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x17500F88 CE3_APU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the APU_ESYNRn registers, which are merely the "syndrome" of an error indicated by APU_ESR.

CE3_APU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x17500F8C CE3_APU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

CE3_APU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x17500F90 CE3_APU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

CE3_APU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x17500F94 CE3_APU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

CE3_APU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x17500FF4 CE3_APU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

CE3_APU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved

CE3_APU_REV (cont.)

Bits	Name	Description
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x17500FF8 CE3_APU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x00001800

APU ID Register: Read-only register that defines various configuration attributes of the APU instance.

CE3_APU_IDR

Bits	Name	Description
31:29	RESERVED31_21	Reserved
28:24	MSB	Indicates most significant address bit number used to select a resource group
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.

CE3_APU_IDR (cont.)

Bits	Name	Description
9:8	RESERVED9_8	Reserved
7:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

0x17500FFC CE3_APU_APU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

APU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the APU (including the APU_APU_ACR itself).

CE3_APU_APU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the APU's 4KB address region (including the APU_APU_ACR itself). For single VMID type APUs (APU_IDR[MV] = 0) the APU_APU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

5 Clock Controller Registers

5.1 Overview

Table 5-1 Clock_Controller Bases

Base Name	Parent	Address
GCC_RPU_CR	CLK_CTL_BASE	0x00900000

5.2 GCC RPU Registers (0x00900000 CLK_CTL_BASE)

This section contains the GCC RPU registers.

0x00900F80 GCC_RPU_CR

Type: Write/Read
Clock: XPU_CLK
Reset State: 0x00000000

RPU Configuration Register: This register includes fields governing various RPU behaviors.

GCC_RPU_CR

Bits	Name	Description
31:4	RESERVED_BITS31_4	
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set RPU_ESR. RPU_EAR and RPU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set RPU_ESR. RPU_EAR and RPU_ESYNR0 updated with address and syndrome of error.
2	RPUEIE	RPU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the RPU. Interrupt output is asserted if RPU_CR[RPUEIE] = 1 and any bit is set in RPU_ESR
1	RPUERE	RPU Error Report Enable. RPUERE = 0 causes the RPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master RPUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective RPU port. Errors from either port are terminated by the RPU as RAZ/WI Both client and configuration port errors are recorded in RPU_ESR, independent of the value of RPU_CR[RPUERE]
0	RPUE	RPU Enable. Governs whether RPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures RPU and the MID to VMID mapping tables.

0x00900F84 GCC_RPU_EAR

Type: Write/Read
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the RPU, for both the client port and the configuration port.

GCC_RPU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x00900F88 GCC_RPU_ESR

Type: Write/Read
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the RPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the RPU's interrupt output (when enabled by RPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the RPU_ESYNRn registers, which are merely the 'syndrome' of an error indicated by RPU_ESR.

GCC_RPU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while RPU_ESR[CFG, CLIENT] still non-zero. RPU_EAR and RPU_ESYNRn registers (and RPU_ESR itself, except for the MULTI bit) 'lock' upon first error, RPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while RPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x00900F8C GCC_RPU_ESRRESTORE

Type: Write/Read
Clock: XPU_CLK
Reset State: 0x00000000

.Error RestoreRegister: This is just an aliased address for RPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

GCC_RPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while RPU_ESR[CFG, CLIENT] still non-zero. RPU_EAR and RPU_ESYNRn registers (and RPU_ESR itself, except for the MULTI bit) 'lock' upon first error, RPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while RPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x00900F90 GCC_RPU_ESYNR0

Type: Write/Read
Clock: XPU_CLK
Reset State: 0x00000000

.Error Syndrome Register. Captures the syndrome upon errors detected by the RPU, for both the client port and the configuration port.

GCC_RPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x00900F94 GCC_RPU_ESYNR1

Type: Write/Read
Clock: XPU_CLK
Reset State: 0x00000000

.Error Syndrome Register. Captures the syndrome upon errors detected by the RPU, for both the client port and the configuration port.

GCC_RPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x00900FF4 GCC_RPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

GCC_RPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x00900FF8 GCC_RPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x000500FF

.RPU ID Register: Read-only register that defines various configuration attributes of the RPU instance.

GCC_RPU_IDR

Bits	Name	Description
31:21	RESERVED31_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only RPU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate RPU_RGn_RACR and RPU_RGn_WACR registers govern read vs. write access. For single VMID, RPU_RGn_ACR registers include separate 5-bit read/write vs. read-only ‘owner’ VMID fields

GCC_RPU_IDR (cont.)

Bits	Name	Description
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. RPU_RGn_ACR registers indicate single 5-bit 'owner' VMID field for governing access. MV=1 : indicates multi-VMD type access control. RPU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.
9:8	RESERVED9_8	Reserved
7:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the RPU. Value can range between 0 and 255 (1-256 resource groups).

0x00900FFC GCC_RPU_RPU_ACR

Type: Write/Read
Clock: XPU_CLK
Reset State: 0x00000000

.RPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the RPU (including the RPU_RPU_ACR itself).

GCC_RPU_RPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the RPU's 4KB address region (including the RPU_RPU_ACR itself). For single VMID type RPUs (RPU_IDR[MV] = 0) the RPU_RPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

0x00901000 AFAB_CLK_SRC_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to Read and Write the AFAB_CLK_SRC0_NS, AFAB_CLK_SRC1_NS and AFAB_CLK_SRC_CTL registers.

AFAB_CLK_SRC_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0090100C QDSS_STM_CLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the QDSS_STM_CLK_CTL register.

QDSS_STM_CLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901010 AFAB_CORE_CLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the AFAB_CORE_CLK_CTL registers.

AFAB_CORE_CLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901014 SCSS_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SCCS_ACLK_CTL, SCSS_HCLK_CTL, SCCS_DBG_CLK_CTL, SCSS_XO_SRC_CLK_CTL, SCSS_RESET, SCSS_AFAB_PORT_RESET registers.

SCSS_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901018 AFAB_EBI1_S_ACLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the AFAB_EBI1_CH0_ACLK_CTL and AFAB_EBI1_CH1_ACLK_CTL

AFAB_EBI1_S_ACLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901020 AFAB_AXI_S_FCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the AFAB_AXI_S0_FCLK_CTL, AFAB_AXI_S1_FCLK_CTL, AFAB_AXI_S2_FCLK_CTL, AFAB_AXI_S3_FCLK_CTL, AFAB_AXI_S4_FCLK_CTL registers.

AFAB_AXI_S_FCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901024 SFAB_CORE_CLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SFAB_CORE_CLK_CTL register.

SFAB_CORE_CLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901028 SFAB_AXI_S_FCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SFAB_AXI_S0_FCLK_CTL, SFAB_AXI_S1_FCLK_CTL, SFAB_AXI_S2_FCLK_CTLand SFAB_AXI_S3_FCLK_CTL,SFAB_AXI_S4_FCLK_CTL, and SFAB_AXI_S5_FCLK_CTL registers.

SFAB_AXI_S_FCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved

SFAB_AXI_S_FCLK_ACR (cont.)

Bits	Name	Description
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0090102C SFAB_AHB_S_FCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SFAB_AHB_S0_FCLK_CTL, SFAB_AHB_S1_FCLK_CTL, SFAB_AHB_S2_FCLK_CTL, SFAB_AHB_S3_FCLK_CTL, SFAB_AHB_S4_FCLK_CTL, SFAB_AHB_S5_FCLK_CTL, SFAB_AHB_S6_FCLK_CTL, and SFAB_AHB_S7_FCLK_CTL registers.

SFAB_AHB_S_FCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901030 QDSS_AT_CLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the QDSS_AT_CLK_SRC0_NS, QDSS_AT_CLK_SRC1_NS, QDSS_AT_CLK_SRC_CTL, QDSS_AT_CLK_NS and QDSS_AT_CLK_FS.

QDSS_AT_CLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901034 QDSS_TRACECLKIN_CLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the QDSS_TRACECLKIN_CLK_SRC0_NS, QDSS_TRACECLKIN_CLK_SRC1_NS, QDSS_TRACECLKIN_CLK_SRC_CTL and QDSS_TRACECLKIN_CTL.

QDSS_TRACECLKIN_CLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901038 QDSS_TSCTR_CLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the QDSS_TSCTR_CLK_SRC0_NS, QDSS_TSCTR_CLK_SRC1_NS, QDSS_TSCTR_CLK_SRC_CTL and QDSS_TSCTR_CTL.

QDSS_TSCTR_CLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x0090103C SFAB_ADM0_M_ACLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SFAB_ADM0_M0_ACLK_CTL, SFAB_ADM0_M1_ACLK_CTL, SFAB_ADM0_M2_ACLK_CTL registers.

SFAB_ADM0_M_ACLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901040 ADM0_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the ADM0_CLK_CTL, ADM0_CLK_FS, ADM0_PBUS_CLK_CTL, ADM0_RESET registers.

ADM0_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x0090104C QDSS_RESETS_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the QDSS_RESETS register.

QDSS_RESETS_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901050 IMEM0_ACLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the IMEM0_ACLK_CTL, IMEM0_ACLK_FS registers.

IMEM0_ACLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901054 QDSS_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the QDSS_HCLK_CTL register.

QDSS_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901058 PCIE_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PCIE_ACLK_CTL, PCIE_ACLK_FS, PCIE_AUX_CLK_CTL_NS, PCIE_PCLK_NS, PCIE_HCLK_CTL, PCIE_SFAB_PORT_RESET registers.

PCIE_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x0090105C SFAB_CLK_SRC_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to Read and Write the SFAB_CLK_SRC0_NS, SFAB_CLK_SRC1_NS and SFAB_CLK_SRC_CTL registers.

SFAB_CLK_SRC_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved

SFAB_CLK_SRC_ACR (cont.)

Bits	Name	Description
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901074 SFAB_LPASS_Q6_ACLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SFAB_LPASS_Q6_ACLK_CTL register.

SFAB_LPASS_Q6_ACLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0090107C SFAB_AFAB_M_ACLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SFAB_AFAB_M_ACLK_CTL register.

SFAB_AFAB_M_ACLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.

SFAB_AFAB_M_ACLK_ACR (cont.)

Bits	Name	Description
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901084 AFAB_SFAB_M_ACLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE AFAB_SFAB_M0_ACLK_CTLand AFAB_SFAB_M1_ACLK_CTL registers.

AFAB_SFAB_M_ACLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901090 SFAB_SATA_S_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SFAB_SATA_S_HCLK_CTL register.

SFAB_SATA_S_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901094 DFAB_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the DFAB_CLK_SRC0_NS, DFAB_CLK_SRC1_NS, DFAB_CORE_CLK_CTL, DFAB_CLK_SRC_CTL registers.

DFAB_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010A0 SFAB_DFAB_M_ACLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the SFAB_DFAB_M_ACLK_CTL register.

SFAB_DFAB_M_ACLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009010A4 DFAB_SFAB_M_ACLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the DFAB_SFAB_M_ACLK_CTL register.

DFAB_SFAB_M_ACLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009010A8 DFAB_SWAY_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the DFAB_SWAY0_HCLK_CTL and DFAB_SWAY1_HCLK_CTL registers.

DFAB_SWAY_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009010AC DFAB_ARB_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the DFAB_ARB0_HCLK_CTL and DFAB_ARB1_HCLK_CTL registers.

DFAB_ARB_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved

DFAB_ARB_ACR (cont.)

Bits	Name	Description
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010B0 PPSS_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the PPSS_HCLK_CTL, PPSS_HCLK_FS, PPSS_PROC_CLK_CTL, PPSS_TIMER0_CLK_CTL, PPSS_TIMER1_CLK_CTL, PPSS_RESET registers.

PPSS_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010B4 PMEM_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the PMEM_ACLK_CTL, PMEM_ACLK_FS registers.

PMEM_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010B8 DMA_BAM_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the DMA_BAM_CLK_CTL, DMA_BAM_CLK_FS registers.

DMA_BAM_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010BC SIC_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the SIC_HCLK_CTL register.

SIC_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009010C0 SPS_TIC_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the SPS_TIC_HCLK_CTL register.

SPS_TIC_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009010C8 CFPB_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the CFPB_2x_CLK_SRC0_NS, CFPB_2x_CLK_SRC1_NS, CFPB_2x_CLK_SRC_CTL, CFPB_CLK_NS, CFPB0_HCLK_CTL, CFPB1_HCLK_CTL, CFPB_RESET registers.

CFPB_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009010D0 SFAB_CFPB_M_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the SFAB_CFPB_M_HCLK_CTL register.

SFAB_CFPB_M_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved

SFAB_CFPB_M_HCLK_ACR (cont.)

Bits	Name	Description
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010D4 CFPB_MASTER_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the CFPB_MASTER_HCLK_CTL register.

CFPB_MASTER_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010D8 SFAB_CFPB_S_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the SFAB_CFPB_S_HCLK_CTL register.

SFAB_CFPB_S_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.

SFAB_CFPB_S_HCLK_ACR (cont.)

Bits	Name	Description
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010DC CFPB_SPLITTER_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the CFPB_SPLITTER_HCLK_CTL register.

CFPB_SPLITTER_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010E0 TSIF_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the TSIF_HCLK_CTL, TSIF_HCLK_FS,

TSIF_INACTIVITY_TIMERS_CLK_CTL, TSIF_REF_CLK_MD, TSIF_REF_CLK_NS registers.

TSIF_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010E4 CE1_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the CE1_HCLK_CTL, CE1_CORE_CLK_CTL and CE1_SLEEP_CLK_CTL registers.

CE1_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010E8 CE2_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the CE2_HCLK_CTL and CE2_CORE_CLK_CTLregisters.

CE2_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009010EC SFPB_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the SFPB_HCLK_SRC0_NS, SFPB_HCLK_SRC1_NS, SFPB_HCLK_SRC_CTL, SFPB_HCLK_CTL registers.

SFPB_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved

SFPB_HCLK_ACR (cont.)

Bits	Name	Description
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010F0 SFAB_SFPB_M_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the SFAB_SFPB_M_HCLK_CTL register.

SFAB_SFPB_M_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010F4 SFAB_SFPB_S_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the SFAB_SFPB_S_HCLK_CTL register.

SFAB_SFPB_S_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.

SFAB_SFPB_S_HCLK_ACR (cont.)

Bits	Name	Description
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010F8 RPM_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the RPM_PROC_CLK_CTL, RPM_BUS_CLK_CTL, RPM_BUS_CLK_FS, RPM_SLEEP_CLK_CTL, RPM_TIMER_CLK_CTL registers.

RPM_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009010FC RPM_MSG_RAM_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register

that contains the VMID permitted to READ and write the RPM_MSG_RAM_HCLK_CTL, RPM_MSG_RAM_HCLK_FS registers.

RPM_MSG_RAM_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901100 PMIC_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the PMIC_ARB0_HCLK_CTL, PMIC_ARB1_HCLK_CTL, PMIC_SSBI2_NS registers.

PMIC_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901104+4*n-1 SDCn_ACR, n=[1..4]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the SDCn_HCLK_CTL, SDCn_HCLK_FS, SDCn_APPS_CLK_MD, SDCn_APPS_CLK_NS, SDCn_RESET, SDCn_APPS_CLK_FS registers.

SDCn_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x0090111C ACC_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the QMC_ACC, ACC_HPIMEM_RF8441 and ARR_STBY_N registers.

ACC_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved

ACC_ACR (cont.)

Bits	Name	Description
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901120 USB_HS1_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the USB_HS1_HCLK_CTL, USB_HS1_HCLK_FS, USB_HS1_XCVR_FS_CLK_MD, USB_HS1_XCVR_FS_CLK_NS, USB_HS1_RESET registers.

USB_HS1_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901124 USB_HSIC_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the USB_HSIC_HCLK_CTL, USB_HSIC_XCVR_FS_CLK_MD, USB_HSIC_XCVR_FS_CLK_NS, USB_HSIC_SYSTEM_CLK_CTL, USB_HSIC_SYSTEM_CLK_FS, USB_HSIC_RESET, VDD_USB_HSIC_GFS_CTL and VDD_USB_HSIC_GFS_CTL_STATUS registers.

USB_HSIC_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901128 DIM_BUS_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the CFPB0_C0_HCLK, CFPB0_D0_HCLK, CFPB0_C1_HCLK, CFPB0_D1_HCLK registers.

DIM_BUS_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0090112C USB_FS1_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register

that contains the VMID permitted to READ and write the USB_FS1_HCLK_CTL, USB_FS1_XCVR_FS_CLK_MD, USB_FS1_XCVR_FS_CLK_NS, USB_FS1_SYS_CLK_CTL, USB_FS1_SYS_CLK_FS, USB_FS1_RESET registers.

USB_FS1_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901134 GSBI_COMMON_SIM_CLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the GSBI_COMMON_SIM_CLK_NS register.

GSBI_COMMON_SIM_CLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901138+ 4*n-1 GSBIn_ACR, n=[1..7]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the GSBIn_HCLK_CTL, GSBIn_HCLK_FS, GSBIn_QUP_APPS_MD, GSBIn_QUP_APPS_NS, GSBIn_UART_APPS_MD, GSBIn_UART_APPS_NS, GSBIn_SIM_CLK_CTL, GSBIn_RESET registers.

GSBIn_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901168 USB_HSIC_HSIC_CLK_CTL_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the USB_HSIC_HSIC_CLK_SRC_CTL, USB_HSIC_HSIC_CLK_CTL, USB_HSIC_HSIO_CAL_CLK_CTL registers.

USB_HSIC_HSIC_CLK_CTL_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.

USB_HSIC_HSIC_CLK_CTL_ACR (cont.)

Bits	Name	Description
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0090116C SPDM_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the SPDM_CFG_HCLK_CTL, SPDM_MSTR_HCLK_CTL registers.

SPDM_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901170 SEC_CTRL_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the SEC_CTRL_CLK_CTL, SEC_CTRL_CLK_FS, SEC_CTRL_ACC_CLK_SRC0_NS, SEC_CTRL_ACC_CLK_SRC1_NS, SEC_CTRL_ACC_CLK_SRC_CTL, SEC_CTRL_ACC_CLK_CTL, SEC_CTRL_ACC_CLK_FS registers.

SEC_CTRL_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901174 TLMM_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the TLMM_HCLK_CTL, TLMM_CLK_CTL registers.

TLMM_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901180 SATA_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register

that contains the VMID permitted to READ and WRITE the SATA_HCLK_CTL, SATA_HCLK_FS, SATA_CLK_SRC_NS, SATA_RXOOB_CLK_CTL, SATA_PMALIVE_CLK_CTL, SATA_PHY_REF_CLK_CTL, SATA_SFAB_M_PORT_RESET, and SATA_RESET registers.

SATA_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901184 SATA_ACLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SATA_ACLK_CTL and SATA_ACLK_FS registers.

SATA_ACLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901188 SATA_PHY_CFG_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SATA_PHY_CFG_CLK_CTL registers.

SATA_PHY_CFG_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x0090118C GSS_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the GSS_SLP_CLK_CTL, GSS_RESET, GSS_CXO_SRC_CTL, and GSS_CLAMP_ENA registers.

GSS_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved

GSS_ACR (cont.)

Bits	Name	Description
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901194 TSSC_CLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the TSSC_CLK_CTL register.

TSSC_CLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901198 PDM_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PDM_CLK_N register.

PDM_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.

PDM_ACR (cont.)

Bits	Name	Description
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies owner' VMID with full read/write access to the registers in the associated resource group.

0x009011A0+4*n GPn_ACR, n=[0..2]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the GPn_MD, GPn_NS registers.

GPn_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009011B4 MPM_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the MPM_CLK_CTL, MPM_RESET registers.

MPM_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009011B8 RINGOSC_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the RINGOSC_NS, RINGOSC_TCXO_CTL, RINGOSC_CTL, RINGOSC_STATUS registers.

RINGOSC_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009011BC EBI1_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register

that contains the VMID permitted to READ and WRITE the EBI1_CLK_SRC0_NS, EBI1_CLK_SRC1_NS, EBI1_CLK_SRC_CTL, EBI1_CLK_CTL, EBI1_FRQSW_CTL, EBI1_FQSW_STATUS, EBI1_FRQSW_REQ_ACT_TIMER, EBI1_XO_SRC_CTL registers.

EBI1_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009011C0 SFAB_SMPSS_S_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SFAB_SMPSS_S_HCLK_CTL register.

SFAB_SMPSS_S_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009011CC SCSS_DBG_STATUS_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SCSS_DBG_STATUS_REQ, SCSS_DBG_STATUS_CORE_PWRUP registers.

SCSS_DBG_STATUS_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009011D0 PRNG_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PRNG_CLK_NS register.

PRNG_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009011D4 PXO_SRC_CLK_CTL_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PXO_SRC_CLK_CTL register.

PXO_SRC_CLK_CTL_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009011D8 LPASS_XO_SRC_CLK_CTL_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the LPASS_XO_SRC_CLK_CTL register.

LPASS_XO_SRC_CLK_CTL_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009011DC GLOBAL_BUS_NS_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the GLOBAL_BUS_NS register.

GLOBAL_BUS_NS_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009011E4 PLL11_DIV_SRC_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL11_DIV_SRC register.

PLL11_DIV_SRC_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009011EC SPDM_CY_CLK_CTL_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SPDM_CY_PORT0_CLK_CTL, SPDM_CY_PORT1_CLK_CTL, SPDM_CY_PORT2_CLK_CTL, SPDM_CY_PORT3_CLK_CTL, SPDM_CY_PORT4_CLK_CTL, SPDM_CY_PORT5_CLK_CTL, SPDM_CY_PORT6_CLK_CTL, SPDM_CY_PORT7_CLK_CTL registers.

SPDM_CY_CLK_CTL_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x009011F0 RESET_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the RESET_ALL and RESET_STATUS register.

RESET_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.

RESET_ACR (cont.)

Bits	Name	Description
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009011F4 CLK_DBG_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the CLK_TEST register.

CLK_DBG_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009011F8 CLK_HALT_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the CLK_HALT_AFAB_SFAB_STATEA, CLK_HALT_AFAB_SFAB_STATEB, CLK_HALT_DFAB_STATE, CLK_HALT_CFPB_STATEA, CLK_HALT_CFPB_STATEB, CLK_HALT_CFPB_STATEC, CLK_HALT_SFPB_MISC_STATE, CLK_HALT_MSS_KPSS_MISC_STATE registers.

CLK_HALT_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009011FC RPM_CLK_VOTE_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the RPM_CLK_BRANCH_ENA_VOTE and RPM_CLK_SLEEP_ENA_VOTE registers.

RPM_CLK_VOTE_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901204 LPA_Q6_CLK_VOTE_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register

that contains the VMID permitted to READ and WRITE the LPA_Q6_CLK_BRANCH_ENA_VOTE and LPA_Q6_CLK_SLEEP_ENA_VOTE registers.

LPA_Q6_CLK_VOTE_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x00901208 APCS_CLK_VOTE_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the APCS_CLK_BRANCH_ENA_VOTE and APCS_CLK_SLEEP_ENA_VOTE registers.

APCS_CLK_VOTE_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a ‘valid’ bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies ‘owner’ VMID with full read/write access to the registers in the associated resource group.

0x0090120C SPARE_CLK_VOTE_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SPARE_CLK_BRANCH_ENA_VOTE register.

SPARE_CLK_VOTE_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901210 APCS_U_CLK_VOTE_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the APCS_U_CLK_BRANCH_ENA_VOTE and APCS_U_CLK_SLEEP_ENA_VOTE registers.

APCS_U_CLK_VOTE_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved

APCS_U_CLK_VOTE_ACR (cont.)

Bits	Name	Description
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901218 PLL0_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL0_MODE, PLL0_L_VAL, PLL0_M_VAL, PLL0_N_VAL, PLL0_TEST_CTL, PLL0_CONFIG, PLL0_STATUS registers.

PLL0_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0090121C PLL5_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL5_MODE, PLL5_L_VAL, PLL5_M_VAL, PLL5_N_VAL, PLL5_TEST_CTL, PLL5_CONFIG, PLL5_STATUS registers.

PLL5_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.

PLL5_ACR (cont.)

Bits	Name	Description
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901228 PLL8_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL8_MODE, PLL8_L_VAL, PLL8_M_VAL, PLL8_N_VAL, PLL8_TEST_CTL, PLL8_CONFIG, PLL8_STATUS registers.

PLL8_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0090122C GPLL1_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the GPLL1_MODE, GPLL1_L_VAL,

GPLL1_M_VAL, GPLL1_N_VAL, GPLL1_TEST_CTL, GPLL1_CONFIG, GPLL1_STATUS registers.

GPLL1_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901230 EBI1_PLL_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the EBI1_PLL_MODE, EBI1_PLL_L_VAL, EBI1_PLL_M_VAL, EBI1_PLL_N_VAL, EBI1_PLL_TEST_CTL, EBI1_PLL_CONFIG and EBI1_PLL_STATUS registers.

EBI1_PLL_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901234 RIVA_PLL_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the RIVA_PLL_MODE, RIVA_PLL_L_VAL, RIVA_PLL_M_VAL, RIVA_PLL_N_VAL, RIVA_PLL_TEST_CTL, RIVA_PLL_CONFIG & RIVA_PLL_STATUS registers.

RIVA_PLL_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901238 PLL14_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL14_MODE, PLL14_L_VAL, PLL14_M_VAL, PLL14_N_VAL, PLL14_TEST_CTL, PLL14_CONFIG & PLL14_STATUS registers.

PLL14_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.

PLL14_ACR (cont.)

Bits	Name	Description
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901240 SC_PLL0_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SC_PLL0_MODE, SC_PLL0_CONFIG_CTL, SC_PLL0_L_VAL, SC_PLL0_M_VAL, SC_PLL0_N_VAL, SC_PLL0_DROOP, SC_PLL0_TEST_CTL and SC_PLL0_STATUS registers.

SC_PLL0_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901248 SC_PLL1_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SC_PLL1_MODE, SC_PLL1_CONFIG_CTL, SC_PLL1_L_VAL, SC_PLL1_M_VAL, SC_PLL1_N_VAL, SC_PLL1_DROOP, SC_PLL1_TEST_CTL and SC_PLL1_STATUS registers.

SC_PLL1_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901250 SC_PLL2_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SC_PLL2_MODE, SC_PLL2_CONFIG_CTL, SC_PLL2_L_VAL, SC_PLL2_M_VAL, SC_PLL2_N_VAL, SC_PLL2_DROOP, SC_PLL2_TEST_CTL and SC_PLL2_STATUS registers.

SC_PLL2_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901258 SC_PLL3_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SC_PLL3_MODE, SC_PLL3_CONFIG_CTL, SC_PLL3_L_VAL, SC_PLL3_M_VAL, SC_PLL3_N_VAL, SC_PLL3_DROOP, SC_PLL3_TEST_CTL and SC_PLL3_STATUS registers.

SC_PLL3_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901260 SC_L2_PLL_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SC_L2_PLL_MODE, SC_L2_PLL_CONFIG_CTL, SC_L2_PLL_L_VAL, SC_L2_PLL_M_VAL, SC_L2_PLL_N_VAL, SC_L2_PLL_DROOP, SC_L2_PLL_TEST_CTL and SC_L2_PLL_STATUS registers.

SC_L2_PLL_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901284 PLL_LOCK_DET_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ the PLL_LOCK_DET_STATUS and PLL_LOCK_DET_MASK register.

PLL_LOCK_DET_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0090128C PLL_ENA_SPARE_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL_ENA_SPARE register.

PLL_ENA_SPARE_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901290 PLL_ENA_GSS_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL_ENA_GSS register.

PLL_ENA_GSS_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901294 PLL_ENA_RPM_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL_ENA_RPM register.

PLL_ENA_RPM_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901298 PLL_ENA_APCS_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL_ENA_APCS register.

PLL_ENA_APCS_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0090129C PLL_ENA_APCS_U_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL_ENA_APCS_U register.

PLL_ENA_APCS_U_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012A0 PLL_ENA_RIVA_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL_ENA_RIVA register.

PLL_ENA_RIVA_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012A4 PLL_ENA_LPASS_DSP_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL_ENA_LPASS_DSP register.

PLL_ENA_LPASS_DSP_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012A8 PLL_ENA_SPS_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PLL_ENA_SPS register.

PLL_ENA_SPS_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012AC FABS_RESET_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the FABS_RESET register.

FABS_RESET_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012BC RIVA_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the RIVA_RESET registers.

RIVA_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012C0 XPU_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the XPU_RESET registers.

XPU_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012C4 TSENS_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the TSENS_CNTL, TSENS_THRESHOLD, TSENS_S0_STATUS, TSENS_S1_STATUS, TSENS_S2_STATUS, TSENS_S3_STATUS, TSENS_S4_STATUS, TSENS_INT_STATUS registers.

TSENS_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012C8 TSENS_CONFIG_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the TSENS_CONFIG and TSENS_STATUS_CNTL registers.

TSENS_CONFIG_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved

TSENS_CONFIG_ACR (cont.)

Bits	Name	Description
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012CC TSENS_STATUS_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the TSENS_STATUS_CNTL, TSENS_S5_STATUS, TSENS_S6_STATUS, TSENS_S7_STATUS, TSENS_S8_STATUS, register.

TSENS_STATUS_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012D8 CE3_HCLK_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the CE3_HCLK_CTL, CE3_CORE_CLK_CTL, and CE3_SLEEP_CLK_CTL registers.

CE3_HCLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012DC SFAB_AHB_S_FCLK2_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SFAB_AHB_S8_FCLK_CTL register.

SFAB_AHB_S_FCLK2_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012E0 USB_HS3_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register

that contains the VMID permitted to READ and write the USB_HS3_HCLK_CTL, USB_HS3_HCLK_FS, USB_HS3_XCVR_FS_CLK_MD, USB_HS3_XCVR_FS_CLK_NS, USB_HS3_RESET registers.

USB_HS3_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012E4 USB_HS4_ACR

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and write the USB_HS4_HCLK_CTL, USB_HS4_HCLK_FS, USB_HS4_XCVR_FS_CLK_MD, USB_HS4_XCVR_FS_CLK_NS, USB_HS4_RESET registers.

USB_HS4_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012E8 GSS_CLK_VOTE_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the GSS_CLK_BRANCH_ENA_VOTE and GSS_CLK_SLEEP_ENA_VOTE registers.

GSS_CLK_VOTE_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x009012FC RIVA_CLK_VOTE_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the RIVA_CLK_BRANCH_ENA_VOTE register.

RIVA_CLK_VOTE_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved

RIVA_CLK_VOTE_ACR (cont.)

Bits	Name	Description
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901300 SPDM_CY_CLK_CTL2_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SPDM_CY_PORT8_CLK_CTL register.

SPDM_CY_CLK_CTL2_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901320 APCS_WDOG_EXPIRED_ENA_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the
APCS_WDT0_CPU0_WDOG_EXPIRED_ENABLE,
APCS_WDT1_CPU0_WDOG_EXPIRED_ENABLE,
APCS_WDT0_CPU1_WDOG_EXPIRED_ENABLE,
APCS_WDT1_CPU1_WDOG_EXPIRED_ENABLE,
APCS_WDT0_CPU2_WDOG_EXPIRED_ENABLE,
APCS_WDT1_CPU2_WDOG_EXPIRED_ENABLE,

APCS_WDT0_CPU3_WDOG_EXPIRED_ENABLE,
APCS_WDT1_CPU3_WDOG_EXPIRED_ENABLE registers.

APCS_WDOG_EXPIRED_ENA_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901340 RPM_WDOG_EXPIRED_ENA_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the RPM_WDOG_EXPIRED_ENA register.

RPM_WDOG_EXPIRED_ENA_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901344 PCIE_ALT_REF_CLK_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the PCIE_ALT_REF_CLK_NS register.

PCIE_ALT_REF_CLK_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00901348 SPARE0_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and SPARE0, SPARE1, SPARE2, SPARE3 registers.

SPARE0_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x0090134C SPARE1_ACR

Type: Write/Read
Clock: SFPB_RESET
Reset State: 0x00

(Read) Access Control Registers: This description is for the case when GCC_RPU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type RPU. Access Control Register that contains the VMID permitted to READ and WRITE the SPARE4, SPARE5, SPARE6, SPARE7 registers.

SPARE1_ACR

Bits	Name	Description
31:10	RESERVED31_10	Reserved.
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a 'valid' bit for the RWVMID field.
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies 'owner' VMID with full read/write access to the registers in the associated resource group.

0x00902000 AFAB_CLK_SRC0_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The AFAB_CLK_SRC0_NS register is 1/2 of the application and system fabric only clocks selection register. Internal to the 'u_afab_sfab_clk_src' Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

AFAB_CLK_SRC0_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

AFAB_CLK_SRC0_NS (cont.)

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: pll11_out_main 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902004 AFAB_CLK_SRC1_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The AFAB_CLK_SRC1_NS register is 1/2 of the application and system fabric only clocks selection register. Internal to the 'u_afab_sfab_clk_src' Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

AFAB_CLK_SRC1_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

AFAB_CLK_SRC1_NS (cont.)

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: pll11_out_main 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902008 AFAB_CLK_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0002

The AFAB_CLK_SRC_CTL register provides control to select which asfab_only_src0/1 supplied to the arm clock. Internal to the 'u_afab_sfab_clk_src' Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16 (see descriptions above). This register also provides controls for clock root within this clock generator and provides enable to put this generator in low power state by selecting ALT_SRC which will be grounded.

NOTE The combined enable vote for the sc_hclk, sc_aclk, adm0_clk and adm1_clk branches will also enable the clock root. Therefore, the software root clock enable in this register does not have sole control for the enabling of the clock root.

AFAB_CLK_SRC_CTL

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED
2	CLK_GENERATOR_LOW_PWR_ENA	This bit put the generator in low power state by selecting the alt_src that is grounded. 0x1: Enable 0x0: Disable
1	CLK_ROOT_ENA	Enable clock source for system and application fabric. NOTE This bit does not have sole control of the disabling of the clock root. The voting of the clock branch enable for sc_hclk, sc_aclk, adm0_clk and adm1_clk also affect the enabling of the clock root. 0x1: Enable 0x0: Disable
0	NBID_SEL	This bit selects which internal divider provides the source to the global tree. 0x0: nbid0 0x1: nbid1

0x00902060 QDSS_STM_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x10

This register is used to control the QDSS_STM_CLK. It provides fabric clock gating, branch enable and clock inversion to the branch.

QDSS_STM_CLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	ASYNC_RESET	Async reset for clock domain. 0x1: Active 0x0: Not Active
5	CLK_INV	This bit is used to invert qdss_stm_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for qdss_stm_clk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902064 QDSS_REQ_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

It shows the status of three QDSS request/ack ports.

QDSS_REQ_STATUS

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED
2:0	STATUS	QDSS Status for requests and acks 0x2: qdss_cdbgrstack 0x1: qdss_cdbgrstreq 0x0: qdss_cdbgpwrupreq

0x00902080 AFAB_CORE_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the application fabric core clock branch. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

AFAB_CORE_CLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert afab_core_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for afab_core_clk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009020A0 SCSS_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The SCSS_ACLK_CTL register provides controls to the branch cell used to generate Scorpion multi-processors sub-system (SMPSS) AXI clock and the AXI clocks for the application fabric ports communicating with SMPSS. The controls include enable to fabric dynamic clock gating and inversion of these clocks. The branch enable is votable by multiple master. Therefore, this branch enable control will be located in the individual master's clock voting registers.

SCSS_ACLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_EN	Enable for dynamic clock gating. NOTE Should not be enable for both chips. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert scss_aclk. 0x1: invert 0x0: Not invert
4:0	RESERVED_BITS4_0	RESERVED

0x009020A4 SCSS_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The SCSS_HCLK_CTL register provides controls to the branch cell used to generate SMPSS AHB clock (CC_SC_HCLK). The controls include enable to fabric dynamic clock gating and inversion of CC_SC_HCLK. The branch enable of CC_SC_HCLK is votable for multiple master. Therefore, this branch enable control will be located in the individual master's clock voting registers.

SCSS_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable

SCSS_HCLK_CTL (cont.)

Bits	Name	Description
5	CLK_INV	This bit is used to invert scss_hclk. 0x1: invert 0x0: Not invert
4:0	RESERVED_BITS4_0	RESERVED

0x009020AC SCSS_XO_SRC_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x10

This register provides controls to the branch cell used to generate SMPSS XO clock (CC_SC_XO_SRC). The controls include branch enable, the clock inversion, and source selection between PXO and MXO source. MXO is not used in APQ8064.

SCSS_XO_SRC_CLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert the SC XO clock. 0x1: Inverted 0x0: Not inverted
4	CLK_BRANCH_ENA	This bit is used to enable the SC XO clock branch. 0x1: Enable 0x0: Diable
3:1	RESERVED_BITS3_1	RESERVED
0	SRC_SEL	This field selects which XO to drive SC XO src clock. 0x0: PXO 0x1: MXO

0x009020B8 SCSS_AFAB_PORT_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides software control to the application fabric ports connecting to SMPSS.

SCSS_AFAB_PORT_RESET

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED
2	AFAB_SMPSS_S_RESET	Software reset for Application fabric slave port connecting to SMPSS. 0x1: Active
1	AFAB_SMPSS_M1_RESET	Software reset for Application fabric master 1 port connecting to SMPSS. 0x1: Active
0	AFAB_SMPSS_M0_RESET	Software reset for Application fabric master 0 port connecting to SMPSS. 0x1: Active

0x009020C0 AFAB_EBI1_CH0_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the AXI clock for the application port connecting to EBI1 HSDDRX. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

AFAB_EBI1_CH0_ACLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for EBI1 application fabric AXI clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert afab_ebi1_s_aclk 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for afab_ebi1_s_sclk clock branch 0x1: Enable 0x0: Disable

AFAB_EBI1_CH0_ACLK_CTL (cont.)

Bits	Name	Description
3:0	RESERVED_BITS3_0	RESERVED

0x009020C4 AFAB_EBI1_CH1_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the AXI clock for the application port connecting to EBI1 HSDDRX. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

AFAB_EBI1_CH1_ACLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for EBI1 application fabric AXI clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert afab_ebi1_s_aclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for afab_ebi1_s_sclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902100 AFAB_AXI_S0_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the application AXI slave port 0 (cc_afab_axi_s0_fclk). It provides enable and clock inversion to the branch, and

also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

AFAB_AXI_S0_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert afab_axi_s0_fclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for afab_axi_s0_fclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902104 AFAB_AXI_S1_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the application AXI slave port 1 (cc_afab_axi_s1_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

AFAB_AXI_S1_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert afab_axi_s1_fclk. 0x1: invert 0x0: Not invert

AFAB_AXI_S1_FCLK_CTL (cont.)

Bits	Name	Description
4	CLK_BRANCH_ENA	Enable for afab_axi_s1_clk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902108 AFAB_AXI_S2_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the application AXI slave port 2 (cc_afab_axi_s2_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

AFAB_AXI_S2_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert afab_axi_s2_fclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for afab_axi_s2_fclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x0090210C AFAB_AXI_S3_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the application AXI slave port 3 (cc_afab_axi_s3_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

AFAB_AXI_S3_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert afab_axi_s3_fclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for afab_axi_s3_fclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902110 AFAB_AXI_S4_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the application AXI slave port 4 (cc_afab_axi_s4_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

AFAB_AXI_S4_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable

AFAB_AXI_S4_FCLK_CTL (cont.)

Bits	Name	Description
5	CLK_INV	This bit is used to invert afab_axi_s4_fclk. This clock is votable. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for afab_axi_s4_fclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902120 SFAB_CORE_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the sysetem fabric core clock branch. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_CORE_CLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_core_clk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_core_clk clock branch. Maybe votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902140 SFAB_AXI_S0_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AXI slave port 0 (cc_sfab_axi_s0_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AXI_S0_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_axi_s0_fclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_axi_s0_fclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902144 SFAB_AXI_S1_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AXI slave port 1 (cc_sfab_axi_s1_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AXI_S1_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_axi_s1_fclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_axi_s1_fclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902148 SFAB_AXI_S2_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AXI slave port 2 (cc_sfab_axi_s2_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AXI_S2_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_axi_s2_fclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_axi_s2_fclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable

SFAB_AXI_S2_FCLK_CTL (cont.)

Bits	Name	Description
3:0	RESERVED_BITS3_0	RESERVED

0x0090214C SFAB_AXI_S3_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AXI slave port 3 (cc_sfab_axi_s3_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AXI_S3_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_axi_s3_fclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_axi_s3_fclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902150 SFAB_AXI_S4_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This registeris used to control the branch cell used to generate the fabric clock for the system fabric AXI slave port 4 (cc_sfab_axi_s4_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the

enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AXI_S4_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_axi_s4_fclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_axi_s4_fclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902154 SFAB_AXI_S5_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AXI slave port 5 (cc_sfab_axi_s5_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AXI_S5_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_axi_s5_fclk. 0x1: invert 0x0: Not inver

SFAB_AXI_S5_FCLK_CTL (cont.)

Bits	Name	Description
4	CLK_BRANCH_ENA	Enable for sfab_axi_s5_fclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902160 SFAB_AHB_S0_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AHB slave port 0 (cc_sfab_ahb_s0_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AHB_S0_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_ahb_s0_fclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_ahb_s0_fclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902164 SFAB_AHB_S1_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AHB slave port 1 (cc_sfab_ahb_s1_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AHB_S1_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_ahb_s1_fclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_ahb_s1_fclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902168 SFAB_AHB_S2_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AHB slave port 2 (cc_sfab_ahb_s2_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AHB_S2_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable

SFAB_AHB_S2_FCLK_CTL (cont.)

Bits	Name	Description
5	CLK_INV	This bit is used to invert sfab_ahb_s2_fclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_ahb_s2_fclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x0090216C SFAB_AHB_S3_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AHB slave port 3 (cc_sfab_ahb_s3_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AHB_S3_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_ahb_s3_fclk. 0x1: Invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_ahb_s3_fclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902170 SFAB_AHB_S4_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AHB slave port 4 (cc_sfab_ahb_s4_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AHB_S4_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_ahb_s4_fclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_ahb_s4_fclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902174 SFAB_AHB_S5_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AHB slave port 5 (cc_sfab_ahb_s5_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AHB_S5_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_ahb_s5_fclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_ahb_s5_fclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902178 SFAB_AHB_S6_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AHB slave port 6 (cc_sfab_ahb_s6_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AHB_S6_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_ahb_s6_fclk. 0x1: Invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_ahb_s6_fclk clock branch. This clock is votable 0x1: Enable 0x0: Disable

SFAB_AHB_S6_FCLK_CTL (cont.)

Bits	Name	Description
3:0	RESERVED_BITS3_0	RESERVED

0x0090217C SFAB_AHB_S7_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AHB slave port 7 (cc_sfab_ahb_s7_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AHB_S7_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_ahb_s7_fclk. 0x1: Invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_ahb_s7_fclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902180 QDSS_AT_CLK_SRC0_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The QDSS_AT_CLK_SRC0_NS register is used to select the clock divisor and clock source for SRC0. Internal to the Hard-macro cell (hm_arm_crc_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

QDSS_AT_CLK_SRC0_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_main 0x3: pll8_out_main 0x4: gnd_tie 0x5: pll11_out_main 0x6: pll3_out_aux 0x7: core_bi_pll_test_se

0x00902184 QDSS_AT_CLK_SRC1_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The QDSS_AT_CLK_SRC1_NS register is used to select the clock divisor and clock source for SRC1. Internal to the Hard-macro cell (hm_arm_crc_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

QDSS_AT_CLK_SRC1_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

QDSS_AT_CLK_SRC1_NS (cont.)

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_main 0x3: pll8_out_main 0x4: gnd_tie 0x5: pll11_out_main 0x6: pll3_out_aux 0x7: core_bi_pll_test_se

0x00902188 QDSS_AT_CLK_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0002

The QDSS_AT_CLK_SRC_CTL register provides control to select between qdss_at_clk_src0/1. Internal to the Hard-macro cell (hm_arm_crc_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16 (see descriptions above). This register also provides controls for clock root within this clock generator and provides enable to put this generator in low power state by selecting ALT_SRC, which will be grounded.

QDSS_AT_CLK_SRC_CTL

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED

QDSS_AT_CLK_SRC_CTL (cont.)

Bits	Name	Description
2	CLK_GENERATOR_LOW_PWR_ENA	This bit put the generator in low power state by selecting the alt_src which is grounded. 0x1: Enable 0x0: Disable
1	CLK_ROOT_ENA	This bit is used to enable the QDSS_AT_CLK root. NOTE: The root cannot be disabled by setting this bit to 0 if the downstream CXCs (controlled by AT_CLK_BRANCH_ENA and PCLKDBG_CLK_BRANCH_ENA) are still running. 0x1: Enable 0x0: Diable
0	NBID_SEL	This bit selects which internal divider provides the source to the global tree. 0x0: nbid0 0x1: nbid1

0x0090218C QDSS_AT_CLK_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0001

This register is used to control the generation of qdss_at_clk and qdss_pclkdbg_clk.

QDSS_AT_CLK_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	AT_CLK_BRANCH_ENA	This bit is used to enable the QDSS_AT_CLK. 0x1: Enable 0x0: Disable
5	AT_CLK_INV	This bit is used to invert the QDSS_AT_CLK. 0x1: Inverted 0x0: Not inverted
4	PCLKDBG_CLK_BRANCH_ENA	This bit is used to enable the QDSS_PCLKDBG_CLK. 0x1: Enable 0x0: Diable
3	PCLKDBG_CLK_INV	This bit is used to invert the QDSS_PCLKDBG_CLK. 0x1: Inverted 0x0: Not inverted
2	DIVIDER_ASYNC_RESET	This field is used to reset the divider for qdss_pclkdbg_clk. 0x1: reset enabled 0x0: reset disabled

QDSS_AT_CLK_NS (cont.)

Bits	Name	Description
1:0	PCLKDBG_CLK_DIV	This field is used to control the divider for generating the QDSS_PCLKDBG_CLK clock. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4

0x00902190 QDSS_AT_CLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for QDSS_AT_CLK.

QDSS_AT_CLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode

QDSS_AT_CLK_FS (cont.)

Bits	Name	Description
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x009021A0 QDSS_TRACECLKIN_CLK_SRC0_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The QDSS_TRACECLKIN_CLK_SRC0_NS register is used to select the clock divisor and clock source for SRC0. Internal to the Hard-macro cell (hm_arm_crc_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

QDSS_TRACECLKIN_CLK_SRC0_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

QDSS_TRACECLKIN_CLK_SRC0_NS (cont.)

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_main 0x3: pll8_out_main 0x4: gnd_tie 0x5: pll11_out_main 0x6: pll3_out_aux 0x7: core_bi_pll_test_se

0x009021A4 QDSS_TRACECLKIN_CLK_SRC1_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The QDSS_TRACECLKIN_CLK_SRC1_NS register is used to select the clock divisor and clock source for SRC1. Internal to the Hard-macro cell (hm_arm_crc_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

QDSS_TRACECLKIN_CLK_SRC1_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

QDSS_TRACECLKIN_CLK_SRC1_NS (cont.)

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_main 0x3: pll8_out_main 0x4: gnd_tie 0x5: pll11_out_main 0x6: pll3_out_aux 0x7: core_bi_pll_test_se

0x009021A8 QDSS_TRACECLKIN_CLK_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0002

The QDSS_TRACECLKIN_CLK_SRC_CTL register provides control to select between qdss_traceclkin_clk_src0/1. Internal to the Hard-macro cell (hm_arm_crc_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16 (see descriptions above). This register also provides controls for clock root within this clock generator and provides enable to put this generator in low power state by selecting ALT_SRC, which will be grounded.

QDSS_TRACECLKIN_CLK_SRC_CTL

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED

QDSS_TRACECLKIN_CLK_SRC_CTL (cont.)

Bits	Name	Description
2	CLK_GENERATOR_LOW_PWR_ENA	This bit put the generator in low power state by selecting the alt_src which is grounded. 0x1: Enable 0x0: Disable
1	CLK_ROOT_ENA	This bit is used to enable the QDSS_TRACECLKIN_CLK root. NOTE The root cannot be disabled by setting this bit to 0 if the downstream CXC (controlled by TRACECLKIN_CLK_BRANCH_ENA) are still running. 0x1: Enable 0x0: Diable
0	NBID_SEL	This bit selects which internal divider provides the source to the global tree. 0x0: nbid0 0x1: nbid1

0x009021AC QDSS_TRACECLKIN_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register is used to control the generation of qdss_traceclkin_clk.

QDSS_TRACECLKIN_CTL

Bits	Name	Description
31:5	RESERVED_BITS31_5	RESERVED
4	CLK_BRANCH_ENA	This bit is used to enable the QDSS_TRACECLKIN_CLK. 0x1: Enable 0x0: Disable
3	CLK_INV	This bit is used to invert the QDSS_TRACECLKIN_CLK. 0x1: Inverted 0x0: Not inverted
2:0	RESERVED_BITS2_0	RESERVED

0x009021C0 QDSS_TSCTR_CLK_SRC0_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The QDSS_TSCTR_CLK_SRC0_NS register is used to select the clock divisor and clock source for SRC0. Internal to the Hard-macro cell (hm_arm_crc_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

QDSS_TSCTR_CLK_SRC0_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_main 0x3: pll8_out_main 0x4: gnd_tie 0x5: pll11_out_main 0x6: pll3_out_aux 0x7: core_bi_pll_test_se

0x009021C4 QDSS_TSCTR_CLK_SRC1_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The QDSS_TSCTR_CLK_SRC1_NS register is used to select the clock divisor and clock source for SRC1. Internal to the Hard-macro cell (hm_arm_crc_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

QDSS_TSCTR_CLK_SRC1_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_main 0x3: pll8_out_main 0x4: gnd_tie 0x5: pll11_out_main 0x6: pll3_out_aux 0x7: core_bi_pll_test_se

0x009021C8 QDSS_TSCTR_CLK_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0002

The QDSS_TSCTR_CLK_SRC_CTL register provides control to select between qdss_tsctr_clk_src0/1. Internal to the Hard-macro cell (hm_arm_crc_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16 (see descriptions above). This register also provides controls for clock root within this clock generator and provides enable to put this generator in low power state by selecting ALT_SRC which will be grounded.

QDSS_TSCTR_CLK_SRC_CTL

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED
2	CLK_GENERATOR_LOW_PWR_ENA	This bit put the generator in low power state by selecting the alt_src which is grounded. 0x1: Enable 0x0: Disable
1	CLK_ROOT_ENA	This bit is used to enable the QDSS_TSCTR_CLK root. NOTE The root cannot be disabled by setting this bit to 0 if the downstream CXC (controlled by TSCTR_CLK_BRANCH_ENA) are still running. 0x1: Enable 0x0: Diable
0	NBID_SEL	This bit selects which internal divider provides the source to the global tree. 0x0: nbid0 0x1: nbid1

0x009021CC QDSS_TSCTR_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register is used to control the generation of qdss_tsctr_clk.

QDSS_TSCTR_CTL

Bits	Name	Description
31:5	RESERVED_BITS31_5	RESERVED
4	CLK_BRANCH_ENA	This bit is used to enable the QDSS_TSCTR_CLK. 0x1: Enable 0x0: Disable
3	CLK_INV	This bit is used to invert the QDSS_TSCTR_CLK. 0x1: Inverted 0x0: Not inverted
2:0	RESERVED_BITS2_0	RESERVED

0x009021E0 SFAB_ADM0_M0_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the system fabric port connecting to ADM0 client interface 0. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_ADM0_M0_ACLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Asynchronous Software reset for ADM0 system fabric AXI master port 0. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_adm0_m0_aclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_adm0_m0_aclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009021E4 SFAB_ADM0_M1_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the system fabric port connecting to ADM0 client interface 1. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_ADM0_M1_ACLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Asynchronous Software reset for ADM0 system fabric AXI master port 1. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_adm0_m1_aclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_adm0_m1_aclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009021E8 SFAB_ADM0_M2_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the system fabric port connecting to ADM0 client interface 2. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_ADM0_M2_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Asynchronous Software reset for ADM0 system fabric AHB master port 2. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable

SFAB_ADM0_M2_HCLK_CTL (cont.)

Bits	Name	Description
5	CLK_INV	This bit is used to invert sfab_adm0_m2_hclk. 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_adm0_m2_hclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902200 ADM0_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The ADM0_CLK_CTL register provides controls to clock inversion of the branch cell used to generate ADM0 core clock (CC_ADM0_CLK). The branch enable of CC_ADM0_clk is votable for multiple master. Therefore, this branch enable control will be located in the individual master's clock voting registers.

ADM0_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert adm0_clk. 0x1: invert 0x0: Not inver
4:0	RESERVED_BITS4_0	RESERVED

0x00902204 ADM0_CLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC of the CC_ADM0_CLK.

ADM0_CLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

ADM0_CLK_FS (cont.)

Bits	Name	Description
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x00902208 ADM0_PBUS_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The ADM0_PBUS_CLK_CTL register provides controls to the branch cell used to generate CC_ADM0_PBUS_CLK. The controls include enables dynamic bus clock gating and inversion of CC_ADM0_PBUS_CLK. The branch enable of CC_ADM0_PBUS_CLK is votable for multiple master. Therefore, this branch enable control will be located in the individual master's clock voting registers.

ADM0_PBUS_CLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert ADM0_PBUS_CLK. 0x1: invert 0x0: Not invert
4:0	RESERVED_BITS4_0	RESERVED

0x0090220C ADM0_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides software control to the ADM0 resets.

ADM0_RESET

Bits	Name	Description
31:5	RESERVED_BITS31_5	RESERVED
4	ADM0_C2_RESET	Asynchronous Software reset for ADM0 Client 2 interface. 0x1: Active 0x0: Inactive
3	ADM0_C1_RESET	Asynchronous Software reset for ADM0 Client 1interface. 0x1: Active 0x0: Inactive
2	ADM0_C0_RESET	Asynchronous Software reset for ADM0 Client 0 interface. 0x1: Active 0x0: Inactive
1	ADM0_PBUS_CLK_RESET	Asynchronous Software reset for ADM0 PBUS interface. 0x1: Active 0x0: Inactive
0	ADM0_CLK_RESET	Asynchronous Software reset for ADM clock domain. 0x1: Active 0x0: Inactive

0x00902260 QDSS_RESETS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used for generating all the resets for QDSS.

QDSS_RESETS

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	QDSS_CLKS_SW_ASYNC_RESET	This bit is used for generating qdss_clks_sw_ares. 0x1: Active. 0x0: Not Active
4	QDSS_POR_ASYNC_RESET	This bit is used for generating cc_qdss_por_ares. 0x1: Active. 0x0: Not Active
3	QDSS_TSCTR_ASYNC_RESET	This bit is used for generating cc_qdss_tsctr_ares. 0x1: Active. 0x0: Not Active
2	QDSS_HRESET_ASYNC_RESET	This bit is used for generating cc_qdss_hreset_ares. 0x1: Active. 0x0: Not Active
1	QDSS_AXI_ASYNC_RESET	This bit is used for generating cc_qdss_axi_ares. 0x1: Active. 0x0: Not Active
0	QDSS_DBG_ASYNC_RESET	This bit is used for generating cc_qdss_dbg_ares. 0x1: Active. 0x0: Not Active

0x00902280 IMEM0_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AXI clock for IMEM core and system fabric port connecting to IMEM. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

IMEM0_ACLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to imem0_aclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for imem-_aclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902284 IMEM0_ACLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC of the AXI clock for IMEM and system fabric port connecting to IMEM.

IMEM0_ACLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode

IMEM0_ACLK_FS (cont.)

Bits	Name	Description
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x009022A0 QDSS_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x10

This register is used to control the clock branch for the generation of cc_qdss_hclk. It provides enable and clock inversion to the branch.

QDSS_HCLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert qdss_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for qdss_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009022C0 PCIE_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AXI clock for PCIE core and system fabric ports connecting to PCIE. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

PCIE_ACLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert pcie_aclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for pcie_aclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009022C4 PCIE_ACLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC of the AXI clock for PCIE and system fabric port connecting to PCIE.

PCIE_ACLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	Force core on.
5	FORCE_P_ON	Force peripheral on.
4	FORCE_P_OFF	Force peripheral off.

PCIE_ACLK_FS (cont.)

Bits	Name	Description
3:0	S_W_VAL	Sleep/Wake-up value.

0x009022C8 PCIE_AUX_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000

The PCIE_AUX_CLK_CTL register provides controls to the cell used to generate cc_pcie_aux_clk.

PCIE_AUX_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert pcie_aux_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for pcie_aux_clk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009022CC PCIE_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch forPCIE AHB clock. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

PCIE_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

PCIE_HCLK_CTL (cont.)

Bits	Name	Description
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert pcie_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for pcie_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009022D0 PCIE_PCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of PCLK (PCIE PHY REF CLK) clock for PCIE. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

PCIE_PCLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert pcie_aclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for pcie_aclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009022D4 PCIE_PCLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC of the PCIE PCLK (aka PCIE PHY REF CLK) clock for PCIE.

PCIE_PCLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	Force core on.
5	FORCE_P_ON	Force peripheral on.
4	FORCE_P_OFF	Force peripheral off.
3:0	S_W_VAL	Sleep/Wake-up value.

0x009022D8 PCIE_SFAB_PORT_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides software control to the system fabric ports connecting to PCIE.

PCIE_SFAB_PORT_RESET

Bits	Name	Description
31:2	RESERVED_BITS31_2	RESERVED
1	SFAB_PCIE_M_RESET	Async reset for System fabric master port connecting to PCIE. 0x1: Active 0x0: Not Active
0	SFAB_PCIE_S_RESET	Software reset for System fabric slave port connecting to PCIE. 0x1: Active

0x009022DC PCIE_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x78

This register provides centralized software resets for various PCIE clock domains and functions.

PCIE_RESET

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	EXT_PCI_RESET	Software reset routed off chip to external PCIE devices. 0x1: Active 0x0: Not Active
5	PHY_RESET	Software reset for the PCIE PHY. 0x1: Active 0x0: Not Active
4	PCI_RESET	Software reset for the PCIE core. 0x1: Active 0x0: Not Active
3	POR_RESET	Power On Reset for the PCIE core. 0x1: Active 0x0: Not Active
2	HCLK_ASYNC_RESET	Async. software reset for PCIE AHB clock. 0x1: Active 0x0: Not Active
1	RESERVED_BIT1	RESERVED
0	ACLK_ASYNC_RESET	Async. Software reset for PCIE AXI clock domain. 0x1: Active 0x0: Not Active

0x009022E0 SFAB_CLK_SRC0_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The SFAB_CLK_SRC0_NS register is 1/2 of the application and system fabric only clocks selection register. Internal to the 'u_afab_sfab_clk_src' Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

SFAB_CLK_SRC0_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

SFAB_CLK_SRC0_NS (cont.)

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_main 0x3: pll8_out_main 0x4: gnd_tie 0x5: pll11_out_main 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x009022E4 SFAB_CLK_SRC1_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The SFAB_CLK_SRC1_NS register is 1/2 of the application and system fabric only clocks selection register. Internal to the 'u_afab_sfab_clk_src' Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

SFAB_CLK_SRC1_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

SFAB_CLK_SRC1_NS (cont.)

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_main 0x3: pll8_out_main 0x4: gnd_tie 0x5: pll11_out_main 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x009022E8 SFAB_CLK_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0002

The SFAB_CLK_SRC_CTL register provides control to select which asfab_only_src0/1 supplied to the arm clock. Internal to the 'u_afab_sfab_clk_src' Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16 (see descriptions above). This register also provides controls for clock root within this clock generator and provides enable to put this generator in low power state by selecting ALT_SRC which will be grounded.

NOTE The combined enable vote for the sc_hclk, sc_aclk, adm0_clk and adm1_clk branches will also enable the clock root. Therefore, the software root clock enable in this register does not have sole control for the enabling of the clock root.

SFAB_CLK_SRC_CTL

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED
2	CLK_GENERATOR_LOW_PWR_ENA	This bit put the generator in low power state by selecting the alt_src which is grounded. 0x1: Enable 0x0: Disable
1	CLK_ROOT_ENA	Enable clock source for system and application fabric. NOTE This bit does not have sole control of the disabling of the clock root. The voting of the clock branch enable for sc_hclk, sc_aclk, adm0_clk and adm1_clk also affect the enabling of the clock root. 0x1: Enable 0x0: Disable
0	NBID_SEL	This bit selects which internal divider provides the source to the global tree. 0x0: nbid0 0x1: nbid1

0x009023A0 SFAB_LPASS_Q6_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of Low Power Audio Subsystem (LPASS) Q6 AXI clock and the AXI clock for system fabric ports connecting to LPASS Q6. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_LPASS_Q6_ACLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for System Fabric port AXI LPASS_Q6 clock domain. 0x1: Active. 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable

SFAB_LPASS_Q6_ACLK_CTL (cont.)

Bits	Name	Description
5	CLK_INV	This bit is used to invert sfab_lpass_q6_aclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sfab_lpas_q6_aclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009023E0 SFAB_AFAB_M_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AXI clock for system fabric master port connecting to application fabric and the AXI clock for application fabric slave port connecting to system fabric. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AFAB_M_ACLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for System fabric to Application fabric master port AXI clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_afab_m_aclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sfab_afab_m_aclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902420 AFAB_SFAB_M0_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AXI clock for application fabric master port 0 connecting to system fabric and the AXI clock for system fabric slave port 0 connecting to application fabric. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

AFAB_SFAB_M0_ACLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for Application fabric to System fabric master port 0 AXI clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert afab_sfab_m0_aclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for afab_sfab_m0_aclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902424 AFAB_SFAB_M1_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AXI clock for application fabric master port 1 connecting to system fabric and the AXI clock for system fabric slave port 1 connecting to application fabric. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software

clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

AFAB_SFAB_M1_ACLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for Application fabric to System fabric master port 1AXI clock domain. 0x1: Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert afab_sfab_m1_aclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for afab_sfab_m1_aclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902480 SFAB_SATA_S_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for system fabric slave port connecting to SATA. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_SATA_S_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for SATA System fabric slave port AHB clock domaindomain 0x1: Active 0x0: Not Active

SFAB_SATA_S_HCLK_CTL (cont.)

Bits	Name	Description
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_sata_s_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sfab_sata_s_hclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009024A0 DFAB_CLK_SRC0_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The DFAB_CLK_SRC0_NS register is 1/2 of the dayotona clocks selection register. This register is used to select the source clock divisor and clock source for SRC0. Internal to the 'u_dfab_clk_src' Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

DFAB_CLK_SRC0_NS

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16

DFAB_CLK_SRC0_NS (cont.)

Bits	Name	Description
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: pll11_div_src 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x009024A4 DFAB_CLK_SRC1_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The DFAB_CLK_SRC1_NS register is 1/2 of the dayotona clocks selection register. This register is used to select the source clock divisor and clock source for SRC1. Internal to the 'u_dfab_clk_src' Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

DFAB_CLK_SRC1_NS

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16

DFAB_CLK_SRC1_NS (cont.)

Bits	Name	Description
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: pll11_div_src 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x009024A8 DFAB_CLK_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0002

The DFAB_CLK_SRC_CTL register provides control to select which dfab_clk_src0/1 supplied to the arm clock. Internal to the 'u_dfab_clk_src' Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16 (see descriptions above). This register also provides controls for clock root within this clock generator and provides enable to put this generator in low power state by selecting ALT_SRC which will be grounded.

DFAB_CLK_SRC_CTL

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED
2	CLK_GENERATOR_LOW_PWR_ENA	This bit put the generator in low power state by selecting the alt_src which is grounded. 0x1: Enable 0x0: Disable
1	CLK_ROOT_ENA	Enable clock source. 0x1: Enable 0x0: Disable
0	NBID_SEL	This bit selects which internal divider provides the source to the clock tree. 0x0: nbid0 0x1: nbid1

0x009024AC DFAB_CORE_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the fabric core clock branch. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

DFAB_CORE_CLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert dfab_core_clk 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for dfab_core_clk clock branch This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902500 SFAB_DFAB_M_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AXI clock for system fabric master port connecting to Smart Peripheral Subsystem fabric and the AXI clock for Smart Peripheral Subsystem fabric slave port connecting to system fabric. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_DFAB_M_ACLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for System fabric to Smart Peripheral Subsystem fabric master port AXI clock domain. 0x1: Active
6	FABRIC_CLK_GATE_ENA	Ideal is used fabric clock gating.
5	CLK_INV	This bit is used to invert sfab_dfab_m_aclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sfab_dfab_m_aclk clock branch. This clock is votable; Should this be shared with the CLK_BRANCH_ENA voting of DFAB_SFAB_M_ACLK_CTL 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902520 DFAB_SFAB_M_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AXI clock for system fabric slave port connecting to Smart Peripheral Subsystem fabric and the AXI clock for Smart Peripheral Subsystem fabric master port connecting to system fabric. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

DFAB_SFAB_M_ACLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for Smart Peripheral Subsystem fabric to System fabric master port AXI clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable

DFAB_SFAB_M_ACLK_CTL (cont.)

Bits	Name	Description
5	CLK_INV	This bit is used to invert dfab_sfab_m_aclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for dfab_sfab_m_aclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902540 DFAB_SWAY0_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for Smart Peripheral Subsystem fabric slave way 0. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

DFAB_SWAY0_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for SWAY0 sytem fabric AHB clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert dfab0_sway0_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for dfab_sway0_hclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902544 DFAB_SWAY1_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for Smart Peripheral Subsystem fabric slave way 1. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

DFAB_SWAY1_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for SWAY1 sytem fabric AHB clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert dfab_sway1_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for dab_sway1_clk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902560 DFAB_ARB0_HCLK_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for Smart Peripheral Subsystem fabric arbitor 0. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

DFAB_ARB0_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for ARB0 Smart Peripheral Subsystem fabric AHB clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert dfab_arb0_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for dfab_arb0_hclk clock branch. Maybe votable; Consult with software 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902564 DFAB_ARB1_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for Smart Peripheral Subsystem fabric arbitor 1. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

DFAB_ARB1_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for ARB1 Smart Peripheral Subsystem fabric AHB clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable

DFAB_ARB1_HCLK_CTL (cont.)

Bits	Name	Description
5	CLK_INV	This bit is used to invert dfab_arb0_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for dfab_arb0_hclk clock branch. Maybe votable; Consult with software 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902580 PPSS_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for Peripheral Processor sub-system. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

PPSS_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert ppss_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for ppss_hclk clock branch. Maybe not votable; Consult with software. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902584 PPSS_HCLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for PPSS HCLK.

PPSS_HCLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x00902588 PPSS_PROC_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of processor clock for Peripheral Processor sub-system. It provides enable and clock inversion to the branch, and also contains enable for the hardware dynamic clock gating mode. When hardware dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on traffic.

PPSS_PROC_CLK_CTL

Bits	Name	Description
31:10	RESERVED_BITS31_10	RESERVED
9	CORE_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable. 0x1: Enable
8:7	RESERVED_BITS8_7	.
6	RESERVED_BIT6	RESERVED
5	CLK_INV	This bit is used to invert ppss_proc_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for ppss_proc_clk clock branch. Maybe votable; Consult with software. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x0090258C PPSS_TIMER0_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the generation of cc_ppss_timer0_clk. There are 2 possible sources for this clock and each source can be halted independently. This register provides controls for them as well.

PPSS_TIMER0_CLK_CTL

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12	MXO_SRC_CLK_INV	This bit is used to invert the MXO source. NOTE: MXO is not used in APQ8064. 0x1: Inverted 0x0: Not inverted
11	MXO_SRC_BRANCH_ENA	This bit is used to enable the MXO source for generating ppss timer0 clock. NOTE: MXO is not used in APQ8064. 0x1: Enable 0x0: Diable
10	PXO_SRC_CLK_INV	This bit is used to invert the PXO source. 0x1: Inverted 0x0: Not inverted
9	PXO_SRC_BRANCH_ENA	This bit is used to enable the PXO source for generating ppss timer0 clock. 0x1: Enable 0x0: Diable
8:6	RESERVED_BITS8_6	RESERVED
5	CLK_INV	This bit is used to invert the ppss timer0 clock. 0x1: Inverted 0x0: Not inverted
4	CLK_BRANCH_ENA	This bit is used to enable the ppss timer0 clock branch. 0x1: Enable 0x0: Diable
3:1	RESERVED_BITS3_1	RESERVED
0	SRC_SEL	This field selects which XO to drive ppss timer0 clock. Note: The selected source must also be enabled. 0x0: PXO 0x1: MXO

0x00902590 PPSS_TIMER1_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the generation of PPSS timer1 clock.

PPSS_TIMER1_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert ppss_timer1_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for ppss_timer1_clk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902594 PPSS_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x02

This register is used to control different resets to Peripheral Processor sub-system.

PPSS_RESET

Bits	Name	Description
31:2	RESERVED_BITS31_2	RESERVED
1	PPSS_PROC_RESET	Async reset for ppss processor clock domain. 0x1: Active 0x0: Not Active
0	PPSS_RESET	Async reset for ppss peripheral clock domain. 0x1: Active 0x0: Not Active

0x009025A0 PMEM_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of PMEM AXI clock. It provides enable and clock inversion to the branch, and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

PMEM_ACLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	CLK_GATE_ENA	Enable for dynamic clock gating. 0x1: Enable 0x0: Disable
5	CLK_INV	This bit is used to invert pmem_aclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for pmem_aclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009025A4 PMEM_ACLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for PMEM AXI clock.

PMEM_ACLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode

PMEM_ACLK_FS (cont.)

Bits	Name	Description
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x009025C0 DMA_BAM_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of DAM BAM AHB clock. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

DMA_BAM_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for the DMA_BAM AHB clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for fabric/HW dynamic clock gating. 0x1: Enable
5	CLK_INV	This bit is used to invert the DMA BAM clock 0x1: Inverted 0x0: Not inverted

DMA_BAM_HCLK_CTL (cont.)

Bits	Name	Description
4	CLK_BRANCH_ENA	This bit is used to enable the DMA BAM clock branch. 0x1: Enable 0x0: Diable
3:0	RESERVED_BITS3_0	

0x009025C4 DMA_BAM_HCLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for DMA BAM AHB clock.

DMA_BAM_HCLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode

DMA_BAM_HCLK_FS (cont.)

Bits	Name	Description
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x009025E0 SIC_HCLK_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the clock branch for the generation of SIC AHB clock. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SIC_HCLK_CTL

Bits	Name	Description
31:10	RESERVED_BITS31_10	RESERVED
9	CORE_CLK_GATE_ENA	Enable dynamic clock gating. 0x1: Enable 0x2: Disable.
8:6	RESERVED_BITS8_6	RESERVED
5	CLK_INV	This bit is used to invert sic_hclk. 0x1: invert 0x0: Not invert

SIC_HCLK_CTL (cont.)

Bits	Name	Description
4	CLK_BRANCH_ENA	Enable for sic_hclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902600 SPS_TIC_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of SPS TIC AHB clock. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SPS_TIC_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for SPS_TIC AHB clock domain. 0x1: Active
6	RESERVED_BIT6	RESERVED
5	CLK_INV	This bit is used to invert sps_tic_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sps_tic_hclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902640 CFPB_2X_CLK_SRC0_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The CFPB_2X_CLK_SRC0_NS register is 1/2 of the Chip FPB clocks selection register. This register is used to select the Smart Peripheral Subsystem source clock divisor and clock source for

SRC0. Internal to the {u_cfpb_2x_clk_src} Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

CFPB_2X_CLK_SRC0_NS

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_main 0x3: pll8_out_main 0x4: gnd_tie 0x5: pll11_div_src 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902644 CFPB_2X_CLK_SRC1_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The CFPB_2X_CLK_SRC1_NS register is 1/2 of the Chip FPB clocks selection register. This register is used to select the Smart Peripheral Subsystem source clock divisor and clock source for SRC1. Internal to the {u_cfpb_2x_clk_src} Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

CFPB_2X_CLK_SRC1_NS

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_main 0x3: pll8_out_main 0x4: gnd_tie 0x5: pll11_div_src 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902648 CFPB_2X_CLK_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0002

The CFPB_2X_CLK_SRC_CTL register provides control to select which cfpb_2x_clk_src0/1 supplied to the arm clock. Internal to the {u_cfpb_2x_clk_src} Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16 (see descriptions above). This register also provides controls for clock root within this clock generator and provides enable to put this generator in low power state by selecting ALT_SRC which will be grounded.

NOTE The combined enable vote for the adm0 and adm1 pbus clock branches will also enable the clock root. Therefore, the software root clock enable in this register does not have sole control for the enabling of the clock root.

CFPB_2X_CLK_SRC_CTL

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED
2	CLK_GENERATOR_LOW_PWR_ENA	This bit put the generator in low power state by selecting the alt_src which is grounded. 0x1: Enable 0x0: Disable
1	CLK_ROOT_ENA	Enable clock source for cfpb_2x. NOTE This bit does not have sole control of the disabling of the clock root. The voting of the clock branch enable for adm0 and adm1 pbus clocks also affect the enabling of the clock root. 0x1: Enable 0x0: Disable
0	NBID_SEL	This bit selects which internal divider provides the source to the cfpb_2x clock tree. 0x0: nbid0 0x1: nbid1

0x0090264C CFPB_CLK_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register controls the divider to divide down to CFPB 2X clock into 1X.

CFPB_CLK_NS

Bits	Name	Description
31:2	RESERVED_BITS31_2	RESERVED
1:0	CLK_DIV	This field selects the CFPB clock divisor. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4

0x00902650 CFPB0_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of cc_cfpb0_hclk. It provides enable and clock inversion to the clock branches, software control to the reset of logic clocked by these clocks and also contains enable for the dynamic clock gating for cc_cfpb0_hclk. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of cc_cfpb0_hclk. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

CFPB0_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	NOTE:This bit should be used as a static configuration. To toggle hardware clock gating for CPSS/CFPB, SW should disable the corresponding CPSS/CFPB AHB clock befor updating this bit. Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert CC_CFBP0_HCLK. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for CC_CFPB0_HCLK clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902654 CFPB1_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of cc_cfpb1_hclk . It provides enable and clock inversion to the clock branches, software control to the reset of logic clocked by these clocks and also contains enable for the dynamic clock gating for cc_cfpb1_hclk. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of cc_cfpb1_hclk. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

CFPB1_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

CFPB1_HCLK_CTL (cont.)

Bits	Name	Description
6	BUS_CLK_GATE_ENA	NOTE:This bit should be used as a static configuration. To toggle hardware clock gating for CPSS/CFPB, SW should disable the corresponding CPSS/CFPB AHB clock befor updating this bit. Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert cfbp1_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for cfpb1_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902658 CFPB2_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of cc_cfpb2_hclk. It provides enable and clock inversion to the clock branches, software control to the reset of logic clocked by these clocks and also contains enable for the dynamic clock gating for cc_cfpb2_hclk. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of cc_cfpb2_hclk. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

CFPB2_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	NOTE:This bit should be used as a static configuration. To toggle hardware clock gating for CPSS/CFPB, SW should disable the corresponding CPSS/CFPB AHB clock befor updating this bit. Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert cfpb2_hclk. 0x1: invert 0x0: Not invert

CFPB2_HCLK_CTL (cont.)

Bits	Name	Description
4	CLK_BRANCH_ENA	Enable for cfbp2_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902680 SFAB_CFPB_M_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for the system fabric master port connecting to Chip FPB. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic

SFAB_CFPB_M_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for CFPB System fabric master port AHB clock. domain 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_cfpb_m_hclk 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sfab_cfpb_m_hclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009026A0 CFPB_MASTER_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of cc_cfpb_master_hclk and cc_cfpb_master_nohwgate_hclk. It provides enable and clock inversion to the clock branches, software control to the reset of logic clocked by these clocks and also contains enable for the dynamic clock gating for cc_cfpb_master_hclk. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of cc_cfpb_master_hclk. The enabling of this clock will be done dynamically by internal hardware based on bus traffic..

CFPB_MASTER_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	NOTE:This bit should be used as a static configuration. To toggle hardware clock gating for CPSS/CFPB, SW should disable the corresponding CPSS/CFPB AHB clock befor updating this bit. Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert cfpb_master_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for cfpb_master_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009026C0 SFAB_CFPB_S_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for the system fabric slave port connecting to Chip FPB. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_CFPB_S_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for CFPB System fabric slave port AHB clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_cfpb_s_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sfab_cfpb_s_hclk clock branch This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009026E0 CFPB_SPLITTER_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of cc_cfpb_splitter_hclk. It provides enable and clock inversion to the clock branches, software control to the reset of logic clocked by these clocks and also contains enable for the dynamic clock gating for cc_cfpb_splitter_hclk. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of cc_cfpb_splitter_hclk. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

CFPB_SPLITTER_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	NOTE:This bit should be used as a static configuration. To toggle hardware clock gating for CPSS/CFPB, SW should disable the corresponding CPSS/CFPB AHB clock befor updating this bit. Enable for dynamic clock gating. 0x0: Disable 0x1: Enable

CFPB_SPLITTER_HCLK_CTL (cont.)

Bits	Name	Description
5	CLK_INV	This bit is used to invert cfpb_splitter_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for cfpb_splitter_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902700 TSIF_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for the TSIF. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

TSIF_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for TSIF AHB clock domain. 0x1: Active 0x0: Not Active
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert tsif_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for tsif_hclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902704 TSIF_HCLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for TSIF AHB clock.

TSIF_HCLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x00902708 TSIF_INACTIVITY_TIMERS_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the clock branch for the generation of cc_tsif_inactivity_timers_clk. It provides enable and clock inversion to the branch.

TSIF_INACTIVITY_TIMERS_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert tsif_inactivity_timers_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for tsif_inactivity_timers_clk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x0090270C TSIF_REF_CLK_MD

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register contains the M and D values used for the M/N:D counter of TSIF REF clock generator..

TSIF_REF_CLK_MD

Bits	Name	Description
31:16	M_VAL	This is the M value for the clock branchs M/N:D counter.
15:0	D_VAL	This is the NOT(2*D) value for the clock branchs M/N:D counter.

0x00902710 TSIF_REF_CLK_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of TSIF REF clock generator. It also contains the branch enable, root enables, clock inversion, MN counter enable and reset, MN counter mode selection, and pre divider control of the TSIF REF clock generator.

TSIF_REF_CLK_NS

Bits	Name	Description
31:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for tsif_ref_clk clock source. NOTE The root cannot be disable by setting this bit to 0 if the downstream CXC (controlled by TSIF_REF_CLK_BRANCH_ENA) is still running. 0x1: Enable 0x0: Disable
10	TSIF_REF_CLK_CLK_INV	This bit is used to invert tsif_ref_clk. 0x1: invert 0x0: Not invert
9	TSIF_REF_CLK_BRANCH_ENA	Enable for tsif_ref_clk clock branch. 0x1: Enable 0x0: Disable
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4

TSIF_REF_CLK_NS (cont.)

Bits	Name	Description
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902720 CE1_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for the Crypto engine 1. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

CE1_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for CE1 AHB clock domain. 0x1: Active 0x0: Not Active
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert ce1_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for ce1_hclk clock branch 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902724 CE1_CORE_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of core clock for the Crypto engine1 in CPSS.

CE1_CORE_CLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for CE1 Core clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert ce1_core_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for ce1_core_clk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902728 CE1_SLEEP_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the clock branch for the generation of cc_ce1_sleep_clk. It provides enable and clock inversion to the branch, and software control to the reset of logic clocked by this clock domain.

CE1_SLEEP_CLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for CE1 sleep clock domain. 0x1: Active 0x0: Not Active
6	RESERVED_BIT6	RESERVED

CE1_SLEEP_CLK_CTL (cont.)

Bits	Name	Description
5	CLK_INV	This bit is used to invert ce1_sleep_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for ce1_sleep_clk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902740 CE2_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for the Crypto engine 2. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

CE2_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for CE2 AHB clock domain. 0x1: Active 0x0: Not Active
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert ce2_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for ce2_hclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902744 CE2_CORE_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of core clock for the Crypto engine 2 in SPS. It provides enable, clock inversion to the branch and software control to the reset of logic clocked by this clock domain.

CE2_CORE_CLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for CE2 core clock domain. 0x1: Active 0x0: Not Active
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert ce2_core_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for ce2_core_clk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902760 SFPB_HCLK_SRC0_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The SFPB_CLK_SRC0_NS register is 1/2 of the System FPB clocks selection register. This register is used to select the SFPB source clock divisor and clock source for SRC0. Internal to the {u_sfpb_clk_src} Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

NOTE Due to requirement of the HFPLL that the system FPB AHB clock must always be 3X the speed of the HFPLL reference XO divided by 4, system FPB AHB clock must not be running at XO speed and can’t be sourced by CXO (19.2 Mhz) when any of the HFPLL reference XO is MXO (27 Mhz).

SFPB_HCLK_SRC0_NS

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_main 0x3: pll8_out_main 0x4: gnd_tie 0x5: pll11_div_src 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902764 SFPB_HCLK_SRC1_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The SFPB_CLK_SRC1_NS register is 1/2 of the System FPB clocks selection register. This register is used to select the SFPB source clock divisor and clock source for SRC1. Internal to the {u_sfpb_clk_src} Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

NOTE Due to requirement of the HFPLL that the system FPB AHB clock must always be 3X the speed of the HFPLL reference XO divided by 4, system FPB AHB clock must not be running at XO speed and can’t be sourced by CXO (19.2 Mhz) when any of the HFPLL reference XO is MXO (27 Mhz).

SFPB_HCLK_SRC1_NS

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_main 0x3: pll8_out_main 0x4: gnd_tie 0x5: pll11_div_src 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902768 SFPB_HCLK_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0002

The SFPB_HCLK_SRC_CTL register provides control to select which sfpb_hclk_clk_src0/1 supplied to the arm clock. Internal to the {u_sfpb_hclk_src} Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16 (see descriptions above). This register also provides controls for clock root within this clock generator.

NOTE In normal case, software should never turn off the root of sfpb clock because it will lock up the chip and can't ever turn back on this clock since clk_ctl uses sfpb_hclk. Due to requirement of the HFPLL that the system FPB AHB clock must always be 3X the speed of the HFPLL reference XO divided by 4, system FPB AHB clock must not be running at XO speed and can't be sourced by CXO (19.2 Mhz) when any of the

HFPLL reference XO is MXO (27 Mhz).

SFPB_HCLK_SRC_CTL

Bits	Name	Description
31:2	RESERVED_BITS31_2	RESERVED
1	CLK_ROOT_ENA	Enable clock source for sfpb_hclk. 0x1: Enable 0x0: Disable
0	NBID_SEL	This bit selects which internal divider provides the source to the sfpb_hclk clock tree. 0x0: nbid0 0x1: nbid1

0x0090276C SFPB_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x10

This register is used to control the clock branch for the generation of cc_sfpb_hclk and cc_sfpb_nohwgate_hclk. It provides enable and clock inversion to the clock branches, and also contains enable for the dynamic clock gating for cc_sfpb_hclk. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of cc_sfpb_hclk. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

NOTE In normal case, software should never turn off the clock branch of sfpb clock because it will lock up the chip and can’t ever turn back on this clock since clk_ctl uses sfpb_hclk.

SFPB_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfpb_hclk. 0x1: invert 0x0: Not invert

SFPB_HCLK_CTL (cont.)

Bits	Name	Description
4	CLK_BRANCH_ENA	Enable for sfpb_hclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902780 SFAB_SFPB_M_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for the system fabric master port connecting to SFPB. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_SFPB_M_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for SFPB System fabric master port AHB clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_sfpb_m_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sfab_sfpb_m_hclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009027A0 SFAB_SFPB_S_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for the system fabric slave port connecting to SFPB. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_SFPB_S_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for SFPB System fabric slave port AHB clock domain. 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_sfpb_s_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sfab_sfpb_s_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009027C0 RPM_PROC_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x10

The RPM_PROC_CLK_CTL register provides controls to the branch cell used to generate CC_RPM_PROC_CLK . The controls include branch enable and inversion of CC_RPM_PROC_CLK. This register also control software assertion of the asynchronous reset for the PRM processor. The branch enable control in this register is one of two software enable control for the RPM ARM7 processor clock. The other control comes from RPM in the form of rpm_proc_clkon signal which is also programmable by software. In addition, the enabling of rpm_proc_clk is also conditioned by the rpm_bus_hclk on/off status. Even though software

enables the rpm_proc_clk by toggling the enable bit, the rpm_proc_clk will remain off until the rpm_bus_hclk is running.

RPM_PROC_CLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for RPM_PROC clock domain. 0x1: Active 0x0: Not Active
6	RESERVED_BIT6	RESERVED
5	CLK_INV	This bit is used to invert rpm_proc_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for rpm_proc_clk clock branch. NOTE: This is one of two software controllable branch enable bits. The other branch enable control comes from a software programable register in RPM. This control comes from RPM in the form of rpm_proc_clkon which will be combined with rpm_proc_clk_sleep_ena bit (see RPM_CLK_SLEEP_ENA_VOTE register). When rpm_proc_clk_sleep_ena bit is set, this clk_branch_ena bit does not have any affect on enabling the rpm_proc_clk. In addition, enabling of the rpm_proc_clk also conditions on first turning on the rpm_bus_hclk first. Without rpm_bus_hclk being enabled, rpm_proc_clk will not turn on even though it is programmed to be enabled by setting 1 to this bit or the enable bit from RPM. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009027C4 RPM_BUS_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x10

The RPM_BUS_HCLK_CTL register provides controls to the branch cell used to generate CC_RPM_BUS_HCLK . The controls include branch enable and inversion of CC_RPM_BUS_HCLK. This register also control software assertion of the asynchronous reset for the RPM HCLK logic. The branch enable control in the register is one of two enable control for the CC_RPM_BUS_HCLK. The other control comes from RPM in the form of rpm_cc_bus_hclkon signal. This signal is conbined with the clock branch enable control from this register and if either one is asserted, the clock to the processor will be on.

RPM_BUS_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	RESERVED_BIT6	RESERVED
5	CLK_INV	This bit is used to invert rpm_bus_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for rpm_bus_hclk clock branch. NOTE: This is one of two software controllable branch enable bits. The other branch enable control comes from a software programable register in RPM. This control comes from RPM in the form of rpm_bus_hclkon. When either of the two enable is set, the rpm_bus_hclk will be running. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009027C8 RPM_BUS_HCLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for RPM bus clock.

RPM_BUS_HCLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode

RPM_BUS_HCLK_FS (cont.)

Bits	Name	Description
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x009027CC RPM_SLEEP_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the clock branch for the generation of cc_rpm_sleep_clk. It provides enable and clock inversion to the branch.

RPM_SLEEP_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert rpm_sleep_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for rpm_sleep_clk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009027D0 RPM_TIMER_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the generation of cc_rpm_timer_clk. There are 3 possible sources for this clock and each source can be halted independently. This register provides controls for them as well.

RPM_TIMER_CLK_CTL

Bits	Name	Description
31:15	RESERVED_BITS31_15	RESERVED
14	MXO_SRC_CLK_INV	This bit is used to invert the MXO source. NOTE: MXO is not used in APQ8064. 0x1: Inverted 0x0: Not inverted
13	MXO_SRC_BRANCH_ENA	This bit is used to enable the MXO source for generating rpm timer clock. NOTE: MXO is not used in APQ8064. 0x1: Enable 0x0: Diable
12	PXO_SRC_CLK_INV	This bit is used to invert the PXO source. 0x1: Inverted 0x0: Not inverted
11	PXO_SRC_BRANCH_ENA	This bit is used to enable the PXO source for generating rpm timer clock. 0x1: Enable 0x0: Diable
10	CXO_SRC_CLK_INV	This bit is used to invert the CXO source. 0x1: Inverted 0x0: Not inverted
9	CXO_SRC_BRANCH_ENA	This bit is used to enable the CXO source for generating rpm timer clock. 0x1: Enable 0x0: Diable
8:6	RESERVED_BITS8_6	RESERVED
5	CLK_INV	This bit is used to invert rpm_timer_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for rpm_timer_clk clock branch. 0x1: Enable 0x0: Disable

RPM_TIMER_CLK_CTL (cont.)

Bits	Name	Description
3:2	RESERVED_BITS3_2	RESERVED
1:0	SRC_SEL	This field selects which XO to drive rpm timer clock. Note: The selected source must also be enabled. 0x0: CXO 0x1: PXO 0x2: MXO 0x3: Ground

0x009027E0 RPM_MSG_RAM_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The RPM_MSG_RAM_HCLK_CTL register provides controls to the branch cell used to generate CC_RPM_MSG_RAM_HCLK. The controls include enable to dynamic bus clock gating and inversion of CC_RPM_MSG_RAM_HCLK. This register also control software assertion of the asynchronous reset for CC_RPM_MSG_RAM_HCLK clock domain. The branch enable of CC_RPM_MSG_RAM_HCLK is votable for multiple master. Therefore, this branch enable control will be located in the individual master's clock voting registers.

RPM_MSG_RAM_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert rpm_msg_ram_hclk. 0x1: invert 0x0: Not invert
4:0	RESERVED_BITS4_0	RESERVED

0x009027E4 RPM_MSG_RAM_HCLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for RPM message ram AHB clock.

RPM_MSG_RAM_HCLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock 0x1: Force-on mode 0x0: Normal mode
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x00902800 PMIC_ARB0_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The PMIC_ARB0_HCLK_CTL register provides controls to the branch cell used to generate CC_PMIC_ARB0_HCLK. The controls include enable to dynamic bus clock gating and inversion of CC_PMIC_ARB0_HCLK. This register also control software assertion of the asynchronous

reset for the PMIC Arbitor0 clock domain. The branch enable of PMIC Arbitor0 clock is votable for multiple master. Therefore, this branch enable control will be located in the individual master's clock voting registers.

PMIC_ARB0_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert pmic_arb0_hclk. 0x1: invert 0x0: Not invert
4:0	RESERVED_BITS4_0	RESERVED

0x00902804 PMIC_ARB1_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The PMIC_ARB0_HCLK_CTL register provides controls to the branch cell used to generate CC_PMIC_ARB1_HCLK. The controls include enable to dynamic bus clock gating and inversion of CC_PMIC_ARB1_HCLK. This register also control software assertion of the asynchronous reset for the PMIC Arbitor1 clock domain. The branch enable of PMIC Arbitor1 clock is votable for multiple master. Therefore, this branch enable control will be located in the individual master's clock voting registers.

PMIC_ARB1_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert pmic_arb1_hclk. 0x1: invert 0x0: Not invert
4:0	RESERVED_BITS4_0	RESERVED

0x0090280C PMIC_SSBI2_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0800

The PMIC_SSBI clock register provides controls to the branch cell used to generate CC_PMIC_SSBI2_CLK. The controls include root clock enable, source select, source divider value and inversion of CC_PMIC_SSBI2_CLK. This register also control software assertion of the asynchronous reset for the PMIC SSBI clock domain. The branch enable of PMIC SSBI clock is votable for multiple master. Therefore, this branch enable control will be located in the individual master's clock voting registers.

NOTE The combined enable vote for the clock branch will also enable the clock root. Therefore, the software root clock enable in this register does not have sole control for the enabling of the clock root.

PMIC_SSBI2_NS

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12	PMIC_SSBI2_RESET	Async reset for the PMIC_SSBI2 clock domain. 0x1: Active 0x0: Not Active
11	CLK_ROOT_ENA	Enable for pmic_ssbi2_clk clock source. NOTE: This bit does not have sole control of the disabling of the clock root. The voting of the clock branch enable also affects the enabling of the clock root. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert pmic_ssbi2_clk 0x1: Invert 0x0: Not Invert
9:5	RESERVED_BITS9_5	RESERVED
4:3	SRC_DIV	Select Divide ratio for pmic_ssbi clock source 0x0: Divide-1 0x1: Divide-2 0x2: Divide-3 0x3: Divide-4
2	RESERVED_BIT2	RESERVED
1:0	SRC_SEL	This field selects which XO to drive pmic_ssbi2 clock. 0x0: CXO 0x1: PXO 0x2: MXO 0x3: Ground

0x00902820+32*n-1 SDCn_HCLK_CTL, n=[1..4]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for the SDCC cores. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SDCn_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sdcn_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sdcn_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902824+32*n-1 SDCn_HCLK_FS, n=[1..4]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for SDCC AHB clocks.

SDCn_HCLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode

SDCn_HCLK_FS (cont.)

Bits	Name	Description
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x00902828+32*n-1 SDCn_APPS_CLK_MD, n=[1..4]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register contains the M and D values used for the M/N:D counter of SDCC application clock generator for each SDCC core.

SDCn_APPS_CLK_MD

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	M_VAL	This is the M value for the clock branchs M/N:D counter.
15:8	RESERVED_BITS15_8	RESERVED
7:0	D_VAL	This is the NOT(2*D) value for the clock branchs M/N:D counter.

0x0090282C+ 32*n-1 SDCn_APPS_CLK_NS, n=[1..4]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of SDCC application clock generator for each SDCC core. It also contains the branch enable, root enables, clock inversion, MN counter enable and reset, MN counter mode selection, and pre divider control of the SDCC application clock generators.

SDCn_APPS_CLK_NS

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for sdcn_apps_clk clock source. NOTE: The root cannot be disable by setting this bit to 0 if the downstream CXC (controlled by bit 9 CLK_BRANCH_ENA) is still running. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert sdcn_apps_clk 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for sdcn_apps_clk clock branch. 0x1: Enable 0x0: Disable
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode

SDCn_APPS_CLK_NS (cont.)

Bits	Name	Description
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: pll11_out_main 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902830+32*n-1 SDCn_RESET, n=[1..4]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control reset to SDCC cores.

SDCn_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	SDC_RESET	Async reset for sdc peripheral clock reset. 0x1: Active 0x0: Inactive

0x00902834+32*n-1 SDCn_APPS_CLK_FS, n=[1..4]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for SDCC AHB clocks.

SDCn_APPS_CLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x009028E0 QMC_ACC

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register contains the Compiler memory ACC values.

QMC_ACC

Bits	Name	Description
31:0	ACC	Compiler memory ACC values.

0x009028E4 ACC_HPIMEM_RF8441

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register contains the Custom memory ACC values (HPIMEM and RF8441.)

ACC_HPIMEM_RF8441

Bits	Name	Description
31:16	RESERVED_BITS31_16	RESERVED
15:8	HPIMEM	Custom memory HPIMEM ACC values.
7:0	RF8441	Custom memory RF8441 ACC values.

0x009028E8 ARR_STBY_N

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0F

This register contains the Custom memory array standby values.

ARR_STBY_N

Bits	Name	Description
31:4	RESERVED_BITS31_4	RESERVED
3:0	STBY	Array standby values.

0x00902900 USB_HS1_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock (cc_usb_hs1_hclk) for the USB_HS1 core. It provides enable and clock inversion to the branch,

and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

USB_HS1_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert usb_hs1_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for usb_hs1_hclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902904 USB_HS1_HCLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for USB high speed core AHB clock.

USB_HS1_HCLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode

USB_HS1_HCLK_FS (cont.)

Bits	Name	Description
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x00902908 USB_HS1_XCVR_FS_CLK_MD

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register contains the M and D values used for the M/N:D counter of cc_usb_hs1_xcvr_fs_clk generator.

USB_HS1_XCVR_FS_CLK_MD

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	M_VAL	This is the M value for the clock branchs M/N:D counter.
15:8	RESERVED_BITS15_8	RESERVED
7:0	D_VAL	This is the NOT(2*D) value for the clock branchs M/N:D counter.

0x0090290C USB_HS1_XCVR_FS_CLK_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of cc_usb_hs1_xcvr_fs_clk generator. It also contains the branch enable, root enables, clock inversion, MN counter enable and reset, MN counter mode selection, and pre divider control of the cc_usb_hs1_xcvr_fs_clk generator.

USB_HS1_XCVR_FS_CLK_NS

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for usb_hs1_xcvr_fs_clk clock source. NOTE: The root cannot be disable by setting this bit to 0 if the downstream CXC (controlled by bit 9 CLK_BRANCH_ENA) is still running. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert usb_hs1_xcvr_fs_clk. 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for usb_hs1_xcvr_fs_clk clock branch. 0x1: Enable 0x0: Disable
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode

USB_HS1_XCVR_FS_CLK_NS (cont.)

Bits	Name	Description
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902910 USB_HS1_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control reset to USB HS1 core..

USB_HS1_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	USB_HS1_RESET	Common USB_HS1 core reset.

0x00902920 USB_HSIC_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the clock branch for the generation of AHB clock for the USB HSIC cores. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

USB_HSIC_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert usb_hsic_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for usb_hsiic_hclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902924 USB_HSIC_XCVR_FS_CLK_MD

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register contains the M and D values used for the M/N:D counter of cc_usb_hsic_xcvr_fs_clk generator.

USB_HSIC_XCVR_FS_CLK_MD

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	M_VAL	This is the M value for the clock branchs M/N:D counter.
15:8	RESERVED_BITS15_8	RESERVED
7:0	D_VAL	This is the NOT(2*D) value for the clock branchs M/N:D counter.

0x00902928 USB_HSIC_XCVR_FS_CLK_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register contains the N values used for the M/N:D counter of cc_usb_hsic_xcvr_fs_clk generator. It also contains the branch enable, root enables, clock inversion, MN counter enable and

reset, MN counter mode selection, and pre divider control of the cc_usb_hsic_xcvr_fs_clk generator.

USB_HSIC_XCVR_FS_CLK_NS

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for usb_hsic_xcvr_fs_clk clock source. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert usb_hsic_xcvr_fs_clk. 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for usb_hsic_xcvr_fs_clk clock branch. 0x1: Enable 0x0: Disable
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4

USB_HSIC_XCVR_FS_CLK_NS (cont.)

Bits	Name	Description
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: bi_tcxo 0x2: pll0 0x3: pll8 0x4: mmcc_pll0_out_main 0x5: pll14_out_main 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x0090292C USB_HSIC_SYSTEM_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the clock branch for the generation of usb_hsic_system_clk. It provides enable and clock inversion to the branch.

USB_HSIC_SYSTEM_CLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	SYNC_HSIC_SYSTEM_CLK_ENA	This bit is used to select between the following two sources for cc_usb2_hsic_system_clk : 0x1: dfab_clk_src 0x0: usb_hsic_xcvr_fs_clk_src
5	CLK_INV	This bit is used to invert usb_hsic_system_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for usb_hsic_system_clk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902930 USB_HSIC_SYSTEM_CLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for cc_usb_hsic_system_clk.

USB_HSIC_SYSTEM_CLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	Force core on.
5	FORCE_P_ON	Force peripheral on.
4	FORCE_P_OFF	Force peripheral off.
3:0	S_W_VAL	Sleep/Wake-up value.

0x00902934 USB_HSIC_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the reset to usb hsic core.

USB_HSIC_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	USB_HSIC_RESET	Common USB_HSIC reset for HCLK and SYSTEM clock.

0x00902938 VDD_USB_HSIC_GFS_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x100

USB HSIC Power Rail control

VDD_USB_HSIC_GFS_CTL

Bits	Name	Description
9	RESERVED_BIT9	RESERVED INTERNAL only: Footswitch Retention bit for the VDD_USB_HSIC power rail. GFS_RET = 1 and GFS_EN = 0 put Macro into VDD_MIN stage (Leakage saved but logic state retained) (NOTE: This is not a supported feature in 45nm).

VDD_USB_HSIC_GFS_CTL (cont.)

Bits	Name	Description
8	VDD_USB_HSIC_GFS_EN	Footswitch enable bit for the VDD_USB_HSIC power rail.
7:6	RESERVED_BITS7_6	UNUSED
5	USB_HSIC_CLAMP	Clamp I/O bit for the Audio VDD_USB_HSIC power rail. 0x0: unclamp 0x1: clamp
4:0	VDD_USB_HSIC_GFS_CNT	This is the number of SFPB_HCLK cycles to delay the assertion of gfs_en_all after the assertion of gfs_en1 when enabling the global distributed footswitch.

0x0090293C VDD_USB_HSIC_GFS_CTL_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x1

The VDD_USB_HSIC_GFS_CTL_STATUS register hold the status of the USB HSIC global distributed footswitch control signals

VDD_USB_HSIC_GFS_CTL_STATUS

Bits	Name	Description
0	USB_HSIC_GFS_EN_ALL	Footswitch enable bit for the VDD_USB_HSIC power rail. 0x0: Disabled 0x1: Enabled

0x00902940 CFPB0_C0_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock (cc_cfpb0_c0_hclk) for the Dim Wrapper. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic

NOTE This is a spare register for any ECO purpose.

CFPB0_C0_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert usb_fs1_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for usb_fs1_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902944 CFPB0_D0_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock (cc_cfpb0_d0_hclk) for the Dim Wrapper. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic

NOTE This is a spare register for any ECO purpose.

CFPB0_D0_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable

CFPB0_D0_HCLK_CTL (cont.)

Bits	Name	Description
5	CLK_INV	This bit is used to invert usb_fs1_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for usb_fs1_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902948 CFPB0_C1_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock (cc_cfpb0_c1_hclk) for the Dim Wrapper. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic

NOTE This is a spare register for any ECO purpose.

CFPB0_C1_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert usb_fs1_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for usb_fs1_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x0090294C CFPB0_D1_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock (cc_cfpb0_d1_hclk) for the Dim Wrapper. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

NOTE This is a spare register for any ECO purpose.

CFPB0_D1_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert usb_fs1_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for usb_fs1_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902960 USB_FS1_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock (cc_usb_fs1_hclk) for the USB_FS1 core. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

USB_FS1_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert usb_fs1_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for usb_fs1_hclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902964 USB_FS1_XCVR_FS_CLK_MD

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register contains the M and D values used for the M/N:D counter of cc_usb_fs1_xcvr_fs_clk generator.

USB_FS1_XCVR_FS_CLK_MD

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	M_VAL	This is the M value for the clock branchs M/N:D counter.
15:8	RESERVED_BITS15_8	RESERVED
7:0	D_VAL	This is the NOT(2*D) value for the clock branchs M/N:D counter.

0x00902968 USB_FS1_XCVR_FS_CLK_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of cc_usb_fs1_xcvr_fs_clk generator. It also contains the branch enable, root enables, clock inversion, MN counter enable and

reset, MN counter mode selection, and pre divider control of the cc_usb_fs1_xcvr_fs_clk generator.

USB_FS1_XCVR_FS_CLK_NS

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for usb_fs1_xcvr_fs_clk clock source NOTE The root cannot be disable by setting this bit to 0 if the downstream CXCs are still running. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert usb_fs1_xcvr_fs_clk. 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for usb_fs1_xcvr_fs_clk clock branch. 0x1: Enable 0x0: Disable
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4

USB_FS1_XCVR_FS_CLK_NS (cont.)

Bits	Name	Description
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x0090296C USB_FS1_SYSTEM_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of cc_usb_fs1_system_clk. It provides enable and clock inversion to the branch.

USB_FS1_SYSTEM_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert usb_fs1_system_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for usb_fs1_system_hclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902970 USB_FS1_SYSTEM_CLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for USB FS1 core system clock.

USB_FS1_SYSTEM_CLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	Force core on.
5	FORCE_P_ON	Force peripheral on.
4	FORCE_P_OFF	Force peripheral off.
3:0	S_W_VAL	Sleep/Wake-up value.

0x00902974 USB_FS1_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the reset to usb fs1 core.

USB_FS1_RESET

Bits	Name	Description
31:2	RESERVED_BITS31_2	RESERVED
1	USB_FS1_XCVR_RESET	Async reset for usb fs1 xcvr clock domain. 0x1: Active 0x0: Inactive
0	USB_FS1_RESET	Common USB_FS1 async reset. 0x1: Active 0x0: Inactive

0x009029A0 GSBI_COMMON_SIM_CLK_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register is used to control the generation of the GSBI SIM clock source.

GSBI_COMMON_SIM_CLK_NS

Bits	Name	Description
31:12	RESERVED_BITS31_12	RESERVED

GSBI_COMMON_SIM_CLK_NS (cont.)

Bits	Name	Description
11	CLK_ROOT_ENA	This bit is used to enable the GSBI SIM clock root. NOTE The root cannot be disable by setting this bit to 0 if the downstream CXCs are still running. 0x1: Enable 0x0: Diable
10:7	RESERVED_BITS10_7	RESERVED
6:3	CLK_DIV	This field is used to control the divider for generating the GSIM SIM clock. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2	RESERVED_BIT2	RESERVED
1:0	SRC_SEL	This field selects which XO to drive GSBI SIM clock. 0x0: CXO 0x1: PXO 0x2: MXO 0x3: Ground

0x009029C0+ 32*n-1 GSBIn_HCLK_CTL, n=[1..7]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for the GSBI cores. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic

GSBIn_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert gsbin_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for gsbin_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009029C4+ 32*n-1 GSBIn_HCLK_FS, n=[1..7]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for GSBI AHB clocks.

GSBIn_HCLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode

GSBIn_HCLK_FS (cont.)

Bits	Name	Description
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x009029C8+ 32*n-1 GSBIn_QUP_APPS_MD, n=[1..7]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register contains the M and D values used for the M/N:D counter of GSBI QUP clock generator for each GSBI core.

GSBIn_QUP_APPS_MD

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	M_VAL	This is the M value for the clock branchs M/N:D counter.
15:8	RESERVED_BITS15_8	RESERVED
7:0	D_VAL	This is the NOT(2*D) value for the clock branchs M/N:D counter.

0x009029CC GSBI1_QUP_APPS_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of GSBI QUP clock generator for each GSBI core. It also contains the branch enable, root enables, clock inversion, MN counter

enable and reset, MN counter mode selection, and pre divider control of the GSBI QUP clock generators.

GSBI1_QUP_APPS_NS

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for gsbin_qup_apps_clk clock source. NOTE The root cannot be disable by setting this bit to 0 if the downstream CXCs (controlled by clk_branch_ena at bit 9) are still running. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert gsbin_qup_apps_clk. 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for gsbin_qup_apss_clk clock branch. 0x1: Enable 0x0: Disable
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4

GSBI1_QUP_APPS_NS (cont.)

Bits	Name	Description
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: core_pi_sleep_clk 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x009029EC GSBI2_QUP_APPS_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of GSBI QUP clock generator for each GSBI core. It also contains the branch enable, root enables, clock inversion, MN counter enable and reset, MN counter mode selection, and pre divider control of the GSBI QUP clock generators.

GSBI2_QUP_APPS_NS

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for gsbin_qup_apps_clk clock source. NOTE The root cannot be disable by setting this bit to 0 if the downstream CXCs (controlled by clk_branch_ena at bit 9) are still running. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert gsbin_qup_apps_clk. 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for gsbin_qup_apss_clk clock branch. 0x1: Enable 0x0: Disable

GSBI2_QUP_APPS_NS (cont.)

Bits	Name	Description
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: core_pi_sleep_clk 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x009029CC+32*n-1 GSBIn_QUP_APPS_NS, n=[3..7]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of GSBI QUP clock generator for each GSBI core. It also contains the branch enable, root enables, clock inversion, MN counter enable and reset, MN counter mode selection, and pre divider control of the GSBI QUP clock generators.

GSBIn_QUP_APPS_NS

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED

GSBIn_QUP_APPS_NS (cont.)

Bits	Name	Description
23:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for gsbin_qup_apps_clk clock source. NOTE: The root cannot be disable by setting this bit to 0 if the downstream CXCs (controlled by clk_branch_ena at bit 9) are still running. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert gsbin_qup_apps_clk. 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for gsbin_qup_apss_clk clock branch. 0x1: Enable 0x0: Disable
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x009029D0+ 32*n-1 GSBIn_UART_APPS_MD, n=[1..7]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register contains the M and D values used for the M/N:D counter of GSBI UART clock generator for each GSBI core.

GSBIn_UART_APPS_MD

Bits	Name	Description
31:16	M_VAL	This is the M value for the clock branchs M/N:D counter.
15:0	D_VAL	This is the NOT(2*D) value for the clock branchs M/N:D counter.

0x009029D4 GSBI1_UART_APPS_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of GSBI UART clock generator for each GSBI core. It also contains the branch enable, root enables, clock inversion, MN counter enable and reset, MN counter mode selection, and pre divider control of the GSBI UART clock generators.

GSBI1_UART_APPS_NS

Bits	Name	Description
31:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for gsbin_uart_apps_clk clock source. NOTE: The root cannot be disable by setting this bit to 0 if the downstream CXCs (controlled by clk_branch_ena at bit 9) are still running. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert gsbin_uart_apps_clk. 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for gsbin_uart_apss_clk clock branch. 0x1: Enable 0x0: Disable

GSBI1_UART_APPS_NS (cont.)

Bits	Name	Description
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: core_pi_sleep_clk 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x009029F4 GSBI2_UART_APPS_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of GSBI UART clock generator for each GSBI core. It also contains the branch enable, root enables, clock inversion, MN counter enable and reset, MN counter mode selection, and pre divider control of the GSBI UART clock generators.

GSBI2_UART_APPS_NS

Bits	Name	Description
31:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.

GSBI2_UART_APPS_NS (cont.)

Bits	Name	Description
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for gsbin_uart_apps_clk clock source. NOTE: The root cannot be disable by setting this bit to 0 if the downstream CXCs (controlled by clk_branch_ena at bit 9) are still running. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert gsbin_uart_apps_clk. 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for gsbin_uart_apss_clk clock branch. 0x1: Enable 0x0: Disable
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: core_pi_sleep_clk 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x009029D4+ 32*n-1 GSBIn_UART_APPS_NS, n=[3..7]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of GSBI UART clock generator for each GSBI core. It also contains the branch enable, root enables, clock inversion, MN counter enable and reset, MN counter mode selection, and pre divider control of the GSBI UART clock generators.

GSBIn_UART_APPS_NS

Bits	Name	Description
31:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for gsbin_uart_apps_clk clock source. NOTE: The root cannot be disable by setting this bit to 0 if the downstream CXCs (controlled by clk_branch_ena at bit 9) are still running. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert gsbin_uart_apps_clk. 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for gsbin_uart_apss_clk clock branch. 0x1: Enable 0x0: Disable
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode

GSBIn_UART_APPS_NS (cont.)

Bits	Name	Description
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x009029D8+ 32*n-1 GSBIn_SIM_CLK_CTL, n=[1..7]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of SIM clock for GSBI coresIt provides enable and clock inversion to the branch.

GSBIn_SIM_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert gsbin_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for gsbin_clk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009029DC+32*n-1 GSBIn_RESET, n=[1..7]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the reset to GSBI cores.

GSBIn_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	GSBI1_RESET	Reset APPS_CLK , SIM_CLK

0x00902B40 USB_HSIC_HSIC_CLK_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock source for the generation of USB HSIC HSIC clock (cc_usb_hsic_hsic_clk) for the USB HSIC. It provides enable to the source crc branch.

USB_HSIC_HSIC_CLK_SRC_CTL

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	CLK_ROOT_ENA	Enable clock source for security control. 0x1: Enable 0x0: Disable

0x00902B44 USB_HSIC_HSIC_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of USB HSIC HSIC clock (cc_usb_hsic_hsic_clk) for the USB HSIC. It provides enable and clock inversion to the branch.

USB_HSIC_HSIC_CLK_CTL

Bits	Name	Description
31:2	RESERVED_BITS31_2	RESERVED

USB_HSIC_HSIC_CLK_CTL (cont.)

Bits	Name	Description
1	CLK_INV	This bit is used to invert usb_hsic_hisc_clk. 0x1: invert 0x0: Not invert
0	CLK_BRANCH_ENA	Enable for usb_hsic_hsic_clk clock branch. 0x1: Enable 0x0: Disable

0x00902B48 USB_HSIC_HSIO_CAL_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of USB HSIC IO Calibration clock (cc_usb_hsic_hsio_cal_clk) for the USB HSIC. It provides enable and clock inversion to the branch.

USB_HSIC_HSIO_CAL_CLK_CTL

Bits	Name	Description
31:2	RESERVED_BITS31_2	RESERVED
1	CLK_INV	This bit is used to invert usb_hsic_hsio_cal_clk. 0x1: invert 0x0: Not invert
0	CLK_BRANCH_ENA	Enable for usb_hsic_hsio_cal_clk clock branch. 0x1: Enable 0x0: Disable

0x00902B60 SPDM_CFG_HCLK_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the clock branch for the generation of cc_spdm_cfg_hclk. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SPDM_CFG_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert spdm_cfg_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for spdm_cfg_hclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902B64 SPDM_MSTR_HCLK_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the clock branch for the generation of cc_spdm_mstr_hclk. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic

SPDM_MSTR_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert spdm_mstr_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for spdm_mstr_hclk clock branch 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902B68 SPDM_FF_CLK_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the generation of cc_spdm_ff_clk. There are 2 possible sources for this clock and each source can be halted independently. This register provides controls for them as well

SPDM_FF_CLK_CTL

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12	MXO_SRC_CLK_INV	This bit is used to invert the MXO source. NOTE: MXO is not used in APQ8064 0x1: Inverted 0x0: Not inverted
11	MXO_SRC_BRANCH_ENA	This bit is used to enable the MXO source for generating ppss timer0 clock. NOTE: MXO is not used in APQ8064 0x1: Enable 0x0: Diable
10	PXO_SRC_CLK_INV	This bit is used to invert the PXO source. 0x1: Inverted 0x0: Not inverted
9	PXO_SRC_BRANCH_ENA	This bit is used to enable the PXO source for generating ppss timer0 clock. 0x1: Enable 0x0: Diable
8:7	RESERVED_BITS8_7	RESERVED
6	HW_CLK_GATE_ENA	Enable dynamic clock gating. 0x1: Enable 0x0: Disable
5	CLK_INV	This bit is used to invert the ppss timer0 clock. 0x1: Inverted 0x0: Not inverted
4	CLK_BRANCH_ENA	This bit is used to enable the ppss timer0 clock branch. 0x1: Enable 0x0: Diable
3:1	RESERVED_BITS3_1	RESERVED

SPDM_FF_CLK_CTL (cont.)

Bits	Name	Description
0	SRC_SEL	This field selects which XO to drive ppss timer0 clock. Note: The selected source must also be enabled. 0x0: PXO 0x1: MXO

0x00902B6C SPDM_RESET

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the reset for the SPDM core.

SPDM_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	SPDM_RESET	ASYNC reset for SPDM 0x1: Active

0x00902B80 SEC_CTRL_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x10

This register is used to control the clock branch for the generation of cc_sec_ctrl_clk. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SEC_CTRL_CLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for Security control clock domain. 0x1: Active 0x0: Not Active

SEC_CTRL_CLK_CTL (cont.)

Bits	Name	Description
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert the sec_ctrl_clk branch. Maybe votable 0x1: Enable 0x0: Disable
4	CLK_BRANCH_ENA	RESERVED
3:0	RESERVED_BITS3_0	RESERVED

0x00902B84 SEC_CTRL_CLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for security control clock.

SEC_CTRL_CLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode

SEC_CTRL_CLK_FS (cont.)

Bits	Name	Description
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x00902B88 SEC_CTRL_ACC_CLK_SRC0_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The SEC_CTRL_ACC_CLK_SRC0_NS register is 1/2 of the Security Control ACC clock selection register. This register is used to select the cc_sec_ctrl_acc_clk source clock divisor and clock source for SRC0. Internal to the {u_sec_ctrl_acc_src} Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

SEC_CTRL_ACC_CLK_SRC0_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

SEC_CTRL_ACC_CLK_SRC0_NS (cont.)

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902B8C SEC_CTRL_ACC_CLK_SRC1_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x07

This register is used to configure the src1 divider and selection configuration. By default after reset, the source selection will be set to source 7 in order to select PLL_TEST_SE input as a clock source for chip vector so that the ACC clock can be running at a high speed.

SEC_CTRL_ACC_CLK_SRC1_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

SEC_CTRL_ACC_CLK_SRC1_NS (cont.)

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902B90 SEC_CTRL_ACC_CLK_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0002

This register provides control to select which sec_ctrl_acc_clk_src0/1 supplied to the arm clock. Internal to the {u_sec_ctrl_acc_src} Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16 (see descriptions above). This register also provides controls for clock root within this clock generator. In addition, this register contains a control bit which would like jtag to control the nbid select during production vector. By default, the control of the nbid select is under JDR register control. In production vector, jtag can select NBID1 as the source of the ACC clock which by default will get its clock from PLL_TEST_SE (see sec_ctrl_acc_clk_src1_ns register). During boot, software can switch the nbid select control back to this register by programmig the JTAG_NBID_SEL_CTRL bit.

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SEC_CTRL_ACC_CLK_SRC_CTL

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED
2	JTAG_NBID_SEL_CTRL	This field is used to select between the control of NBID_SEL coming from JTAG control or from software control by bit 0 of this register. 0x0: JDR (NBID_SEL is controlled by JDR register) 0x1: NBID_SEL (NBID_SEL is controlled by Software via configuration of bit 0 of this register)
1	CLK_ROOT_ENA	Enable clock source for security control. 0x1: Enable 0x0: Disable
0	NBID_SEL	This bit selects which internal divider provides the source to the security clock tree. 0x0: nbid0 0x1: nbid1

0x00902B94 SEC_CTRL_ACC_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x10

This register is used to control the clock branch for the generation of cc_sec_ctrl_cacc_clk. It provides enable and clock inversion to the branch.

SEC_CTRL_ACC_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert sec_ctlrl_acc_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sec_ctrl_acc_clk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902B98 SEC_CTRL_ACC_CLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for security control ACC clock.

SEC_CTRL_ACC_CLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x00902BA0 TLMM_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x10

This register is used to control the clock branch for the generation of cc_tlmm_hclk. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

TLMM_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for the TLMM AHB clock domain. 0x1: Active 0x0: Not Active
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert tlmm_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for tlmm_hclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902BA4 TLMM_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x110

This register is used to control the clock branch for the generation of cc_tlmm_clk. It provides enable and clock inversion to the branch, and software control to the reset of logic clocked by this clock domain.

TLMM_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert tlmm_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for tlmm_clk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902C00 SATA_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of cc_sata_hclk. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SATA_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sata_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sata_hclk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902C04 SATA_HCLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for SATA AHB clock.

SATA_HCLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x00902C08 SATA_CLK_SRC_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the the generation of sata_clk_src. It provides root enable, clock source divide control and clock source selection control.

SATA_CLK_SRC_NS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	CLK_ROOT_ENA	Enable sata_clk clock source. 0x1: Enable 0x0: Disable
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: gnd_1 0x2: pll0 0x3: pll8 0x4: gnd_2 0x5: pll11 0x6: pll3 0x7: core_bi_pll_test_se

0x00902C0C SATA_RXOOB_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of cc_sata_rxoob_clk. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SATA_RXOOB_CLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sata_rxoob_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sata_rxoob_clk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902C10 SATA_PMALIVE_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of cc_sata_pmalive_clk. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SATA_PMALIVE_CLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sata_pmalive_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sata_pmalive_clk clock branch. This clock votable 0x1: Enable 0x0: Disable
3:2	RESERVED_BITS3_2	RESERVED
1:0	CLK_DIV	Select divide ratio (1-4) for sata_pmalive_clk clock. 0x0: DIv-1 0x1: Div-2 0x2: Div-3 0x3: Div-4

0x00902C14 SATA_PHY_REF_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of cc_sata_phy_ref_clk. It provides source selection, enable and clock inversion to the branch.

SATA_PHY_REF_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert sata_phy_ref_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sata_phy_ref_clk clock branch. This clock is votable 0x1: Enable 0x0: Disable
3:1	RESERVED_BITS3_1	RESERVED

SATA_PHY_REF_CLK_CTL (cont.)

Bits	Name	Description
0	SRC_SEL	Selects which XO will supply the 27MHz reference for the SATA PHY PLL: 0x0: PXO (default) 0x1: MXO

0x00902C18 SATA_SFAB_M_PORT_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the reset to the system fabric master port connecting to SATA.

SATA_SFAB_M_PORT_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	SFAB_SATA_M_RESET	Async reset for System fabric sata master port. 0x1: Active 0x0: Inactive

0x00902C1C SATA_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the reset to the system fabric master port connecting to SATA.

SATA_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	ASYNC_RESET	Async reset for sata. (Resets multiple clock domains inside SATA core). 0x1: Active 0x0: Inactive

0x00902C20 SATA_ACLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AXI clock for SATA core and system fabric ports connecting to SATA. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SATA_ACLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sata_aclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sata_aclk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902C24 SATA_ACLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC of the AXI clock for SATA and system fabric port connecting to SATA.

SATA_ACLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	Force core on.
5	FORCE_P_ON	Force peripheral on.
4	FORCE_P_OFF	Force peripheral off

SATA_ACLK_FS (cont.)

Bits	Name	Description
3:0	S_W_VAL	Sleep/Wake-up value.

0x00902C40 SATA_PHY_CFG_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of cc_sata_phy_cfg_clk. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SATA_PHY_CFG_CLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	BUS_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sata_phy_cfg_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sata_phy_cfg_clk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902C60 GSS_SLP_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the clock branch for the generation of cc_gss_slp_clk. It provides enable and clock inversion to the branch, and software control to the reset of logic clocked by this clock domain.

GSS_SLP_CLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for GSS sleep clock domain. 0x1: Active 0x0: Not Active
6	RESERVED_BIT6	RESERVED
5	CLK_INV	This bit is used to invert gss_slp_clk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for gss_slp_clk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902C64 GSS_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the GSS reset.

GSS_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	ASYNC_RESET	Async reset for GSS. 0x1: Active 0x0: Inactive

0x00902C68 GSS_CLAMP_ENA

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x1

This register is used to enable the GSS clamps.

GSS_CLAMP_ENA

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	GSS_CLAMP_ENA	Clamp enable for GSS. 0x1: GSS outputs Clamped 0x0: GSS output NOT Clamped

0x00902C74 GSS_CXO_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x1

This register is used to control the clock branch for the generation of cc_gss_cxo_src. It provides enable and clock inversion.

GSS_CXO_SRC_CTL

Bits	Name	Description
31:2	RESERVED_BITS31_2	RESERVED
1	CLK_INV	This bit is used to invert cc_gss_cxo_src. 0x1: invert 0x0: Not invert
0	CLK_BRANCH_ENA	Enable for cc_gss_cxo_src clock branch. 0x1: Enable 0x0: Disable

0x00902CA0 TSSC_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the generation of cc_tssc_clk. There are 3 possible sources for this clock and each source can be halted independently. This register provides controls for them as well. This register also provides control for async reset to TSSC.

TSSC_CLK_CTL

Bits	Name	Description
31:15	RESERVED_BITS31_15	RESERVED

TSSC_CLK_CTL (cont.)

Bits	Name	Description
14	MXO_SRC_CLK_INV	This bit is used to invert the MXO source. NOTE: MXO is not used in APQ8064. 0x1: Inverted 0x0: Not inverted
13	MXO_SRC_BRANCH_ENA	This bit is used to enable the MXO source for generating tssc clock. NOTE: MXO is not used in APQ8064. 0x1: Enable 0x0: Diable
12	PXO_SRC_CLK_INV	This bit is used to invert the PXO source. 0x1: Inverted 0x0: Not inverted
11	PXO_SRC_BRANCH_ENA	This bit is used to enable the PXO source for generating tssc clock. 0x1: Enable 0x0: Diable
10	CXO_SRC_CLK_INV	This bit is used to invert the CXO source. 0x1: Inverted 0x0: Not inverted
9	CXO_SRC_BRANCH_ENA	This bit is used to enable the CXO source for generating tssc clock. 0x1: Enable 0x0: Diable
8	RESERVED_BIT8	RESERVED
7	ASYNC_RESET	Software reset for the TSSC. 0x1: Active
6	RESERVED_BIT6	RESERVED
5	CLK_INV	This bit is used to invert the tssc clk. 0x1: Inverted 0x0: Not inverted
4	CLK_BRANCH_ENA	This bit is used to enable the tssc clock branch. 0x1: Enable 0x0: Diable
3:2	RESERVED_BITS3_2	RESERVED
1:0	SRC_SEL	This field selects which XO to drive tssc clock. Note: The selected source must also be enabled. 0x0: CXO 0x1: PXO 0x2: MXO 0x3: Ground

0x00902CC0 PDM_CLK_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register is used to control the generation of cc_pdm_clk and cc_pdm_xo4_clk. There are 3 possible sources for this clock and each source can be halted independently. This register provides controls for them as well. This register also provides the control for the generation of async reset for PDM.

PDM_CLK_NS

Bits	Name	Description
31:19	RESERVED_BITS31_19	RESERVED
18	MXO_SRC_CLK_INV	This bit is used to invert the MXO source. NOTE: MXO is not used in APQ8064. 0x1: Inverted 0x0: Not inverted
17	MXO_SRC_BRANCH_ENA	This bit is used to enable the MXO source for generating pdm clock. NOTE: MXO is not used in APQ8064. 0x1: Enable 0x0: Diable
16	PXO_SRC_CLK_INV	This bit is used to invert the PXO source. 0x1: Inverted 0x0: Not inverted
15	PXO_SRC_BRANCH_ENA	This bit is used to enable the PXO source for generating pdm clock. 0x1: Enable 0x0: Diable
14	CXO_SRC_CLK_INV	This bit is used to invert the CXO source. 0x1: Inverted 0x0: Not inverted
13	CXO_SRC_BRANCH_ENA	This bit is used to enable the CXO source for generating pdm clock. 0x1: Enable 0x0: Diable
12	ASYNC_RESET	Async reset for the PDM. 0x1: Active 0x0: Not Active

PDM_CLK_NS (cont.)

Bits	Name	Description
11	CLK_ROOT_ENA	This bit is used to enable the pdm clock root. NOTE The root cannot be disable by setting this bit to 0 if the downstream CXCs (controlled by XO_CLK_BRANCH_ENA and XO4_CLK_BRANCH_ENA) are still running. 0x1: Enable 0x0: Diable
10	XO_CLK_INV	This bit is used to invert the pdm xo clock. 0x1: Inverted 0x0: Not inverted
9	XO_CLK_BRANCH_ENA	This bit is used to enable the pdm xo clock branch. 0x1: Enable 0x0: Diable
8	XO4_CLK_INV	This bit is used to invert the pdm xo4 clock. 0x1: Inverted 0x0: Not inverted
7	XO4_CLK_BRANCH_ENA	This bit is used to enable the pdm xo4 clock branch. 0x1: Enable 0x0: Diable
6:5	RESERVED_BITS6_5	RESERVED
4:3	XO4_CLK_DIV	This field is used to control the divider for generating the pdm XO4 clock. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
2	RESERVED_BIT2	RESERVED
1:0	SRC_SEL	This field selects which XO to drive PDM clock. Note: The selected source must also be enabled. 0x0: CXO 0x1: PXO 0x2: MXO 0x3: Ground

0x00902D00+ 32*n GPn_MD, n=[0..2]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register contains the M and D values used for the M/N:D counter of GP clock generators

GPn_MD

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	M_VAL	This is the M value for the clock branchs M/N:D counter.
15:8	RESERVED_BITS15_8	RESERVED
7:0	D_VAL	This is the NOT(2*D) value for the clock branchs M/N:D counter.

0x00902D24+32*n GPn_NS, n=[0..2]

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of GP clock generators. It also contains the branch enable, root enables, clock inversion, MN counter enable and reset, MN counter mode selection, and pre divider control of the GP clock generators.

GPn_NS

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for gpn_clk clock source. NOTE :The root cannot be disable by setting this bit to 0 if the downstream CXC (controlled by clk_branch_ena at bit 9) is still running. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert gpn_clk 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for gpn_clk clock branch 0x1: Enable 0x0: Disable
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable

GPn_NS (cont.)

Bits	Name	Description
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: core_pi_sleep_clk 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: cxo 0x6: mmcc_pll1 0x7: lcc_pri_pll

0x00902DA0 MPM_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x110

This register is used to control the clock branch for the generation of cc_mpm_clk. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic. This register also contains control to enable the MPM reference clock.

MPM_CLK_CTL

Bits	Name	Description
31:9	RESERVED_BITS31_9	RESERVED

MPM_CLK_CTL (cont.)

Bits	Name	Description
8	MPM_REF_CLK_ENA	Enable for mpm ref clock (in rpm block). 0x1: Enable 0x0: Disable
7	MPM_HCLK_RESET	Software reset for the MPM HCLK branch. 0x1: Active
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	MPM_HCLK_INV	This bit is used to invert mpm_clk. 0x1: invert 0x0: Not invert
4	MPM_HCLK_BRANCH_ENA	Enable for mpm_clk clock branch. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902DA4 MPM_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the reset to MPM

MPM_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	MPM_RESET	Software reset for the MPM. 0x1: Active

0x00902DC0 RINGOSC_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The RINGOSC_NS register contains control signals for the process monitors blocks and the control for the ring oscillator clock generation.

RINGOSC_NS

Bits	Name	Description
23:20	RING_MODE	This field selects the ring mode of the selected process monitor.
19:18	GROUP_ADDRESS	This field selects the group address of the selected process monitor.
17:16	RING_ADDRESS	This field selects the ring address of the selected process monitor.
15	PMBLK_LR_EN	This field enables the process monitor block (lower right). 0x1: Enabled 0x0: Not enabled
14	PMBLK_UR_EN	This field enables the process monitor block (upper right). 0x1: Enabled 0x0: Not enabled
13	PMBLK_UL_EN	This field enables the process monitor block (upper left). 0x1: Enabled 0x0: Not enabled
12	PMBLK_CN_EN	This field enables the process monitor block (central). 0x1: Enabled 0x0: Not enabled
11	RO_ROOT_ENA	This field enables the clk root signal. 0x1: Enabled 0x0: Not enabled
10	RO_CLK_INV	This field inverts the clk signal. 0x1: Inverted 0x0: Not inverted
9	RO_CLK_BRANCH_ENA	This field enables the clk branch signal. 0x1: Enabled 0x0: Not enabled
8	PMBLK_LL_EN	This field enables the process monitor block (lower left). 0x1: Enabled 0x0: Not enabled

RINGOSC_NS (cont.)

Bits	Name	Description
7:4	RING_OSC_DIV_SEL	These bits define the division ratio for the divider on the process monitor source. RING_OSC_DIV_SEL 0x0: Div1 0x1: Div2 0x2: Div3 0x3: Div4 0x4: Div5 0x5: Div6 0x6: Div7 0x7: Div8 0x8: Div9 0x9: Div10 0xA: Div11 0xB: Div12 0xC: Div13 0xD: Div14 0xE: Div15 0xF: Div16
3	UNUSED_BIT_3	UNUSED
2:0	RING_OSC_SEL	Selects the desired internal core to use as the ring_osc_clk. RING_OSC_SEL 0x0: pmblk_cn 0x1: pmblk_ul 0x2: pmblk_ur 0x3: pmblk_lr 0x4: pmblk_ll 0x5: sc_ringosc 0x6: gnd_tie_1 0x7: gnd_tie_2

0x00902DC4 RINGOSC_TCXO_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The TCXO_CNT register holds the value used to load the TCXO counter. It also contains the enable to turn on both up and down counters for DVS_CNTL circuit.

NOTE The TCXO counter uses the XO4 clock from PDM. Although the name implies the counters and logic might have a directly dependency on CXO clock but it does not. One must program the PDM_CLK_NS register to generate the corresponding XO/4

clock. See PDM_CLK_NS register for the programming need. and all the possible XO source selection available.

RINGOSC_TCXO_CTL

Bits	Name	Description
31:21	RESERVED_BITS31_21	RESERVED
20	CNT_EN	DVS_CTRL Up and down counters enable. 0x1: Enabled 0x0: Disable
19:0	TCXO_TERM_CNT	After being loaded this value is decremented and used to compare the ring oscillator frequency to the TCXO frequency and thereby estimating its frequency.

0x00902DCC RINGOSC_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0xXXXXXXXX

The RINGOSC_STATUS register is a read-only register, which contains the status of the ring oscillator counter value and the status of the tcxo counter.

RINGOSC_STATUS

Bits	Name	Description
25	TCXO_CNT_DONE	This bit is automatically set (1) when the TCXO CNT terminates. It can be polled by the microprocessor to determine when the value of RINGOSC_CNT is valid.
24:0	RINGOSC_CNT	These read only register bits hold the value stored in the ring oscillator counter, which is used to compare the ring oscillator frequency to the TCXO frequency and, thereby, estimate its frequency. This register is reset automatically by the rising edge of the ringosc_cnt_en signal.

0x00902DE0 EBI1_CLK_SRC0_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The EBI1_CLK_SRC0_NS register is 1/2 of the EBI1 clocks selection register. This register is used to select the EBI1 source clock divisor and clock source for SRC0. Internal to the {u_ebi1_async_2x_src} Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

EBI1_CLK_SRC0_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_early 0x3: pll8 0x4: gnd_tie 0x5: pll11_out_early 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902DE4 EBI1_CLK_SRC1_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The EBI1_CLK_SRC1_NS register is 1/2 of the EBI1 clocks selection register. This register is used to select the EBI1 source clock divisor and clock source for SRC1. Internal to the {u_ebi1_async_2x_src} Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16.

EBI1_CLK_SRC1_NS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

EBI1_CLK_SRC1_NS (cont.)

Bits	Name	Description
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14_out_aux 0x2: pll0_out_early 0x3: pll8 0x4: gnd_tie 0x5: pll11_out_early 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902DE8 EBI1_CLK_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x2

The EBI1_CLK_SRC_CTL register provides control to select which EBI1_CLK_SRC0/1 supplied to the arm clock. Internal to the {u_ebi1_async_2x_src} Hard-macro cell (hm_arm_clk_ctl) are two integer divider/clock selection Hard-macro cells (hm_nbid_clk_ctl). Each nbid can select from 8 sources and divide 1-16 (see descriptions above). This register also provides controls for clock root within this clock generator and provides enable to put this generator in low power state by selecting ALT_SRC which will be grounded. In addition, this register also contains control to select between asfab_only generator and ebi1_asfab generator for the source of the fabric clocks. When EBI1 frequency swtich state machine is enable (setting of the FSM_ENA bit of EBI1_FRQSW_CTl register), toggling NBID_SEL bit will trigger the state

machine to perform the EBI1 frequency switch sequence. The actual switching will not occur right away. Software must wait for the switching to complete by polling the FRQSW_CMPLT bit.

NOTE The combined enable vote for the sc_hclk, sc_aclk, adm0_clk and adm1_clk branches will also enable the clock root. Therefore, the software root clock enable in this register does not have sole control for the enabling of the clock root.

EBI1_CLK_SRC_CTL

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED
2	CLK_GENERATOR_LOW_PWR_ENA	This bit put the generator in low power state by selecting the alt_src which is grounded. 0x1: Enable 0x0: Disable
1	CLK_ROOT_ENA	Enable clock source for ebi1_clk. NOTE: This bit does not have sole control of the disabling of the clock root. The voting of the clock branch enable for sc_hclk, sc_aclk, adm0_clk and adm1_clk also affect the enabling of the clock root. 0x1: Enable 0x0: Disable
0	NBID_SEL	This bit selects which internal divider provides the source to the ebi1_clk clock tree. 0x0: nbid0 0x1: nbid1

0x00902DEC EBI1_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0xA00

The EBI1_CLK_CTL register provides controls to the branch cells used to generate all the EBI 1X clocks. The controls include enables to the branch enable(s) for the ebi1 2X clock for the EBI1 channel(s), the inversion control for the branch enable(s) and the software assertion of the asynchronous reset for the EBI1 clock domain. This register also provides control to reset all the 2X to 1X divider. In order to phase align all the 2X to 1X EBI clock dividers, assertion of the reset and deassertion of the reset should be done when the EBI1 2X clock(s) are halted. By default after chip wide reset, the branch enable(s) for the EBI 2X clock are desserted and the 2X to 1X dividers are in reset state. Prior to enabling the 2X clock branches, software should first write to this register to deassert the 2X to 1X divider reset.

The EBI1_CLK_CTL register also contains the branch enable and the inversion control for the ebi1 frequency switch FSM clock. When the branch enable for any one of the ebi1 2X clocks is set, it will enable the FSM clock as well. For this reason, in order to use the EBI1 frequency switch FSM, the ebi1 2x clock(s) must be enabled as well.

EBI1_CLK_CTL

Bits	Name	Description
31:14	RESERVED_BITS31_14	RESERVED
13	CH1_FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating for CH1 EBI1 2x clk. 0x0: Disable 0x1: Enable
12	CH0_FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating for CH0 EBI1 2x clk. 0x0: Disable 0x1: Enable
11	CH1_EBI1_1X_DIV_RESET	Async reset for reseting all the CH1 EBI1 2X to 1X dividers in the system. NOTE: The reset should be asserted when the EBI1 2X clock is not running in order to properly align all the EBI1 1X clock from each other. By default, this reset is asserted. Software needs to deassert this reset before enabling the EBI1 2X clock branches. 0x1: Active 0x0: Not Active
10	FRQSW_FSM_CLK_INV	This bit is used to invert the EBI1 frequency switch FSM clock. 0x1: invert 0x0: Not invert
9	CH0_EBI1_1X_DIV_RESET	Async reset for reseting all the CH0 EBI1 2X to 1X dividers in the system. NOTE:The reset should be asserted when the EBI1 2X clock is not running in order to properly align all the EBI1 1X clock from each other. By default, this reset is asserted. Software needs to deassert this reset before enabling the EBI1 2X clock branches. 0x1: Active 0x0: Not Active
8	CH1_CLK_BRANCH_ENA	Enable for ebi1 2X clock branch for channel 1 ebi1. Also will enable the EBI1 frequency switch FSM clock. 0x1: Enable 0x0: Disable
7	CH1_ASYNC_RESET	Async reset for EBI1 CH1 clock domain. 0x1: Active 0x0: Not Active
6	CH0_ASYNC_RESET	Async reset for EBI1 CH0 clock domain. 0x1: Active 0x0: Not Active
5	EBI1_2X_CLK_INV	This bit is used to invert ebi1 2x clock for all channels. 0x1: invert 0x0: Not invert

EBI1_CLK_CTL (cont.)

Bits	Name	Description
4	CH0_CLK_BRANCH_ENA	Enable for ebi1 2X clock branch for channel 0 ebi1. Also will enable the EBI1 frequency switch FSM clock. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902DF0 EBI1_FRQSW_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x100

This register contains controls which are specified to EBI1 frequency switching state machine and switching logic. It contains the reset and enable of the state machine and addition delay setting for the wait counter that times the actual switching of the hm_arm_clk_ctl block.

EBI1_FRQSW_CTL

Bits	Name	Description
31:10	RESERVED_BITS31_10	RESERVED
9	CH1_ENA	When this bit is set (1) the FSM will complete the frequency switch handshake with EBI1 CH1. 0x0: Disable EBI1 CH1 FRQSW 0x1: Enable EBI1 CH1 FRQSW
8	CH0_ENA	When this bit is set (1) the FSM will complete the frequency switch handshake with EBI1 CH0. 0x0: Disable EBI1 CH0 FRQSW 0x1: Enable EBI1 CH0 FRQSW
7:6	RESERVED_BITS7_6	RESERVED
5:2	ADDITION_FRQSW_WAIT_DELAY	This is an additional delay value that is added to the default delay value of 2 for the hm_arm_clk_ctl clock switching delay wait counter. A zero value means the only clock switch delay is 2 DDR 1X clock cycles.
1	FSM_RESET	EBI1 frequency switch state machine reset
0	FSM_ENA	EBI1 frequency switch state machine enable

0x00902DF4 EBI1_FRQSW_STATUS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register contains some status for the EBI1 frequency switching logic. A switch completion status and a report of the final NBID select going to hm_arm_clk_ctl can be obtained from reading this register.

NOTE Prior to issuing the next frequency switch command by toggling the NBID_SEL bit in EBI1_CLK_SRC_CTL register, Software must first write to this register to clear the FRQSW_CMPLT bit.

EBI1_FRQSW_STATUS

Bits	Name	Description
31:2	RESERVED_BITS31_2	RESERVED
1	FSM_NBID_SEL	Internal FSM nbid_sel value (Read ONLY). 0x0: nbid0 0x1: nbid1
0	FRQSW_CMPLT	Frequency switch complete frq. (Software can write this bit)

0x00902DF8 EBI1_FRQSW_REQ_ACK_TIMER

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is read only and contains the timer value for the duration betwen the rising of the REQ from the frequency switching state machine to the completion of the switching cycle via a deassertion of the ACK from the HSDDRX controller for the last switching command.

EBI1_FRQSW_REQ_ACK_TIMER

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	REQ_ACK_TIMER	Timer for REQ to ACK duration.

0x00902DFC EBI1_XO_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the generation of cc_ebi1_ch0_ca_xo_src, cc_ebi1_ch0_dq_xo_src, cc_ebi1_ch1_ca_xo_src and cc_ebi1_ch1_dq_xo_src. It provides enable and clock inversion to the branch, and also contains controls to the selection of the XO sources.

EBI1_XO_SRC_CTL

Bits	Name	Description
31:15	RESERVED_BITS31_15	RESERVED
14	CH1_CA_CLK_GATE_ENA	Enable for dynamic clock gating for EBI1 XO clock for CH1 CA. 0x0: Disable 0x1: Enable
13	CH1_CA_CLK_INV	This bit is used to invert the EBI1 XO clock for CH1 CA. 0x1: Inverted 0x0: Not inverted
12	CH1_CA_CLK_BRANCH_ENA	This bit is used to enable the EBI1 XO clock branch for CH1 CA. 0x1: Enable 0x0: Diable
11	CH1_DQ_CLK_GATE_ENA	Enable for dynamic clock gating for EBI1 XO clock for CH1 DQ. 0x0: Disable 0x1: Enable
10	CH1_DQ_CLK_INV	This bit is used to invert the EBI1 XO clock for CH1 DQ. 0x1: Inverted 0x0: Not inverted
9	CH1_DQ_CLK_BRANCH_ENA	This bit is used to enable the EBI1 XO clock branch for CH1 DQ. 0x1: Enable 0x0: Diable
8	CH0_CA_CLK_GATE_ENA	Enable for dynamic clock gating for EBI1 XO clock for CH0 CA. 0x0: Disable 0x1: Enable
7	CH0_CA_CLK_INV	This bit is used to invert the EBI1 XO clock for CH0 CA. 0x1: Inverted 0x0: Not inverted
6	CH0_CA_CLK_BRANCH_ENA	This bit is used to enable the EBI1 XO clock branch for CH0 CA. 0x1: Enable 0x0: Diable
5	CH0_DQ_CLK_GATE_ENA	Enable for dynamic clock gating for EBI1 XO clock for CH0 DQ. 0x0: Disable 0x1: Enable

EBI1_XO_SRC_CTL (cont.)

Bits	Name	Description
4	CH0_DQ_CLK_INV	This bit is used to invert the EBI1 XO clock for CH0 DQ. 0x1: Inverted 0x0: Not inverted
3	CH0_DQ_CLK_BRANCH_ENA	This bit is used to enable the EBI1 XO clock branch for CH0 DQ. 0x1: Enable 0x0: Diable
2	CLK_INV	This bit is used to invert the EBI1 XO clock. 0x1: Inverted 0x0: Not inverted
1	CLK_BRANCH_ENA	This bit is used to enable the EBI1 XO clock branch. 0x1: Enable 0x0: Diable
0	SRC_SEL	This field selects which XO to drive EBI1 XO src clock. 0x0: PXO 0x1: MXO

0x00902E00 SFAB_SMPSS_S_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of cc_sfab_smpss_s_hclk. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_SMPSS_S_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for SMPSS System fabric slave AHB port clock. domain 0x1: Active 0x0: Not Active
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable

SFAB_SMPSS_S_HCLK_CTL (cont.)

Bits	Name	Description
5	CLK_INV	This bit is used to invert sfab_smpss_s_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for sfab_smpss_s_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00902E60 SCSS_DBG_STATUS_REQ

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register constains Scorpion core debug status.

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SCSS_DBG_STATUS_REQ

Bits	Name	Description
2	SC_DBG_CPU1_CORE_PWR_UP_REQ	Request to keep Scorpion Core1 power domain up and associated clocks running. 0x1: Enable
1	SC_DBG_CPU0_CORE_PWR_UP_REQ	Request to keep Scorpion Core0 power domain up and associated clocks running. 0x1: Enable
0	SC_DBG_SYS_PWR_UP_REQ	Request to keep Scorpion system power domain up and associated clocks running. 0x1: Enable

0x00902E64 SCSS_DBG_STATUS_CORE_PWRDUP

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register contains power state of the Scorpion cores and should only be reset duirng true power on condition.

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SCSS_DBG_STATUS_CORE_PWRDUP

Bits	Name	Description
31:2	RESERVED_BITS31_2	RESERVED
1	SC_CORE1_POWER_RAIL_UP	Status which indicates the power status of Scorpion core1 power regime. 0x1: power_up (Scorpion core power rail is up.) 0x0: power_down (Scorpion core power rail is down.)
0	SC_CORE0_POWER_RAIL_UP	Status which indicates the power status of Scorpion core0 power regime. 0x1: power_up (Scorpion core power rail is up.) 0x0: power_down (Scorpion core power rail is down.)

0x00902E80 PRNG_CLK_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

The PRNG_CLK_NS register provides controls to the branch cell used to generate CC_PRNG_CLK. The controls include source select, source divide, root clock enable and inversion of CC_PRNG_CLK. This register also control software assertion of the asynchronous reset for the PRNG clock domain. The branch enable of PRNG clock is votable for multiple master. Therefore, this branch enable control will be located in the individual master's clock voting registers.

NOTE The combined enable vote for the clock branch will also enable the clock root. Therefore, the software root clock enable in this register does not have sole control for the enabling of the clock root.

PRNG_CLK_NS

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12	ASYNC_RESET	Async reset for PRNG clock domain. 0x1: Active 0x0: Not Active
11	CLK_ROOT_ENA	Enable for prng_clk clock root. NOTE: This bit does not have sole control of the disabling of the clock root. The voting of the clock branch enable also affect the enabling of the clock root. In addition, the root cannot be disabled if the downstream CXC is still running. 0x1: Enable 0x0: Disable

PRNG_CLK_NS (cont.)

Bits	Name	Description
10	CLK_INV	This bit is used to invert pprng_clk. 0x1: invert 0x0: Not invert
9:7	RESERVED_BITS9_7	RESERVED
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00902EA0 PXO_SRC_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x02

This register is used to control the XO source selection for generating the pxo_clk_src. This register must be asynchronously reset so that CXO will be default for pxo_clk_src. and the CXO branch muxed into generation of pxo_clk_src will be enabled.

PXO_SRC_CLK_CTL

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED
2	CXO_SRC_CLK_INV	This bit is used to invert the CXO branch. 0x1: Inverted 0x0: Not inverted
1	CXO_SRC_BRANCH_ENA	This bit is used to enable the CXO source for generating PXO_CLK_SRC. By default, the CXO branch is enabled. 0x1: Enable 0x0: Diable
0	CLK_SEL	Select between CXO or PXO Oscillator Output. 0x0: CXO 0x1: PXO

0x00902EC0 LPASS_XO_SRC_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x01

This register controls the XO clock sources going to low power audio sub-system.

LPASS_XO_SRC_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	LPASS_CXO_CLK_INV	This bit inverts the CXO clock to low power audio sub-system. 0x1: Inverted 0x0: Not inverted
4	LPASS_CXO_BRANCH_ENA	This bit enable the CXO clock branch for supplying CXO clock to low power audio sub-system. 0x1: Enabled 0x0: Not enabled
3	LPASS_MXO_CLK_INV	This bit inverts the MXO clock to low power audio sub-system. NOTE: MXO is not used in APQ8064. 0x1: Inverted 0x0: Not inverted
2	LPASS_MXO_BRANCH_ENA	This bit enable the MXO clock branch for supplying MXO clock to low power audio sub-system. NOTE: MXO is not used in APQ8064 0x1: Enabled 0x0: Not enabled

LPASS_XO_SRC_CLK_CTL (cont.)

Bits	Name	Description
1	LPASS_PXO_CLK_INV	This bit inverts the PXO clock to low power audio sub-system. 0x1: Inverted 0x0: Not inverted
0	LPASS_PXO_BRANCH_ENA	This bit enable the PXO clock branch for supplying PXO clock to low power audio sub-system. 0x1: Enabled 0x0: Not enabled

0x00902EE0 GLOBAL_BUS_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to globally enable/disable SFAB, AFAB, CFPB and SPS clock branches and hardware clock gating.

NOTE This register only controls clock branches that are generated within the Global Clock Controller. A number of clocks that connect to the fabrics are generated from other clock controllers and are not manipulated by this register. Additionally, some clock branches generated within the Global Clock Controller may be asynchronous to the buses and have been intentionally omitted from this feature.

NOTE The following clock branches are affected:

NOTE Apps FABRIC: afab_core_clk, cc_afab_axi_s0_fclk, cc_afab_axi_s1_fclk, cc_afab_axi_s2_fclk, cc_afab_axi_s3_fclk, cc_afab_axi_s4_fclk, afab_ebi1_ch0_aclk, afab_ebi1_ch1_aclk, spdm_cy_port0_clk_src, cc_sc_aclk

NOTE System FABRIC: sfab_core_clk, cc_sfab_axi_s0_fclk, cc_sfab_axi_s1_fclk, cc_sfab_axi_s2_fclk, cc_sfab_axi_s3_fclk, cc_sfab_axi_s4_fclk, cc_sfab_ahb_s0_fclk, cc_sfab_ahb_s1_fclk, cc_sfab_ahb_s2_fclk, cc_sfab_ahb_s3_fclk, cc_sfab_ahb_s4_fclk, cc_sfab_ahb_s5_fclk, cc_sfab_ahb_s6_fclk, cc_sfab_ahb_s7_fclk, cc_sfab_ahb_s8_fclk, afab_sfab_m0_aclk, afab_sfab_m1_aclk, sfab_afab_m_aclk, cc_sfab_adm0_m0_aclk, cc_sfab_adm0_m1_aclk, cc_sfab_adm0_m2_hclk, cc_sfab_lpass_q6_aclk, cc_sfab_mss_m_aclk, cc_sfab_mss_s_hclk, cc_mss_s_hclk, cc_sfab_mss_q6_sw_aclk, cc_sfab_mss_q6_fw_aclk, cc_sfab_usb3_m_aclk, cc_qdss_stm_clk, cc_mss_xpu_clk, spdm_cy_port1_clk_src, cc_sfab_smpss_s_hclk, cc_sc_hclk, cc_sfab_cfpb_m_hclk, cc_cfpb_master_hclk,

cc_cfpb_master_nohwgate_hclk, cc_sfab_cfpb_s_hclk, cc_cfpb_splitter_hclk, cc_adm0_clk, cc_imem0_aclk, cc_pcie_aclk, cc_sata_aclk, cc_sata_hclk

NOTE Chip Peripheral Subsystem: cfpb0_hclkc cfpb1_hclk, cfpb2_hclk, adm0_pbus_hclk, usb_fs1_hclk, gsbi3_hclk, gsbi4_hclk, gsbi5_hclk, gsbi6_hclk, gsbi7_hclk, tsif_hclk_raw, ce1_hclkce1_core_clk, sata_phy_cfg_clk, pcie_hclk

NOTE Smart Peripheral Subsystem: dfab_core_clk, sfab_dfab_m_aclk, dfab_sway0_hclk, dfab_sway1_hclk, dfab_arb0_hclk, dfab_arb1_hclk, ppss_proc_clk, sic_hclktic_hclk, pmem_aclk, ppss_hclk, usb_hs1_hclk, usb_hsic_hclk, usb_hs3_hclk, usb_hs4_hclk, dma_bam_hclk, sdc1_hclk, sdc2_hclk, sdc3_hclk, sdc4_hclk, gsbi1_hclk, gsbi2_hclk, ce2_core_clk, ce2_hclk

GLOBAL_BUS_NS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	SPS_HW_CLK_GATE	This field is used to control the HW gating for SPS* clock switches when SPS_HW_CLK_GATE is set to 1.
6	SPS_BRANCH_EN	Used to enable clocks for SPS* clock switches. 0x1: Enabled 0x0: Not enabled
5	CFPB_HW_CLK_GATE	This field is used to control the HW gating for CFPB* clock switches when CFPB_HW_CLK_GATE is set to 1.
4	CFPB_BRANCH_EN	Used to enable clocks for CFPB* clock switches. 0x1: Enabled 0x0: Not enabled
3	AFAB_HW_CLK_GATE	This field is used to control the HW gating for AFAB* clock switches when AFAB_BRANCH_EN is set to 1.
2	AFAB_BRANCH_EN	Used to enable clocks for AFAB* clock switches. 0x1: Enabled 0x0: Not enabled
1	SFAB_HW_CLK_GATE	This field is used to control the HW gating for SFAB* clock switches when SFAB_BRANCH_EN is set to 1.
0	SFAB_BRANCH_EN	Used to enable clocks for SFAB* clock switches. 0x1: Enabled 0x0: Not enabled

0x00902F20 PLL11_DIV_SRC_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x04

PLL11 (EBI1 DDR PLL) aux output will be used as a possible source for many of the clock generation. Before sending this source to all the generators, it first goes through a divider in order to divider down the frequency of this clock. This register provides the controls for this divider. This register also provides a reset to reset the divider. The proper usage of this is that the divider should be held in reset state when PLL11 aux output are being enable. Once PLL11 aux output is enabled, the reset to the divider can be removed.

PLL11_DIV_SRC_CTL

Bits	Name	Description
31:3	RESERVED_BITS31_3	RESERVED
2	DIVIDER_ASYNC_RESET	This field is used to reset the divider. 0x1: reset enabled 0x0: reset disabled
1:0	SRC_DIV	This field is used to control the divider for generating the pll11_div_src. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4

0x00902F60 SPDM_CY_PORT0_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the control for enabling and inverting the SPDM CY port0 clock.

SPDM_CY_PORT0_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert the clock. 0x1: Inverted 0x0: Not inverted
4	CLK_BRANCH_ENA	This bit is used to enable the clock branch. 0x1: Enable 0x0: Diable
3:0	RESERVED_BITS3_0	RESERVED

0x00902F64 SPDM_CY_PORT1_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the control for enabling and inverting the SPDM CY port1 clock.

SPDM_CY_PORT1_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert the clock. 0x1: Inverted 0x0: Not inverted
4	CLK_BRANCH_ENA	This bit is used to enable the clock branch. 0x1: Enable 0x0: Diable
3:0	RESERVED_BITS3_0	RESERVED

0x00902F68 SPDM_CY_PORT2_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the control for enabling and inverting the SPDM CY port2 clock.

SPDM_CY_PORT2_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert the clock. 0x1: Inverted 0x0: Not inverted
4	CLK_BRANCH_ENA	This bit is used to enable the clock branch. 0x1: Enable 0x0: Diable
3:0	RESERVED_BITS3_0	RESERVED

0x00902F6C SPDM_CY_PORT3_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the control for enabling and inverting the SPDM CY port3 clock.

SPDM_CY_PORT3_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert the clock. 0x1: Inverted 0x0: Not inverted
4	CLK_BRANCH_ENA	This bit is used to enable the clock branch. 0x1: Enable 0x0: Diable
3:0	RESERVED_BITS3_0	RESERVED

0x00902F70 SPDM_CY_PORT4_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the control for enabling and inverting the SPDM CY port4 clock. SPDM CY port 4 clock is a divided version of SMPSS L2 PLL aux output clock. We must enable the AUX source output of SMPSS L2 PLL as well in order to see this clock properly.

SPDM_CY_PORT4_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert the clock. 0x1: Inverted 0x0: Not inverted
4	CLK_BRANCH_ENA	This bit is used to enable the clock branch. 0x1: Enable 0x0: Diable
3:1	RESERVED_BITS3_1	RESERVED
0	SRC_SEL	This bit selects between SC_L2_PLL aux output or PXO clock. 0x1: SC_L2_PLL aux 0x0: PXO (default)

0x00902F74 SPDM_CY_PORT5_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the control for enabling and inverting the SPDM CY port5 clock. SPDM CY port 5 clock is a divided version of SCPLL0 aux output clock. We must enable the AUX source output of SCPLL0 as well in order to see this clock properly.

SPDM_CY_PORT5_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert the clock. 0x1: Inverted 0x0: Not inverted
4	CLK_BRANCH_ENA	This bit is used to enable the clock branch. 0x1: Enable 0x0: Diable
3:1	RESERVED_BITS3_1	RESERVED
0	SRC_SEL	This bit selects between SCPLL0 aux output or PXO clock. 0x1: SCPLL0_aux 0x0: PXO (default)

0x00902F78 SPDM_CY_PORT6_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the control for enabling and inverting the SPDM CY port6 clock. SPDM CY port 6 clock is a divided version of SCPLL1 aux output clock. We must enable the AUX source output of SCPLL1 as well in order to see this clock properly.

SPDM_CY_PORT6_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert the clock. 0x1: Inverted 0x0: Not inverted

SPDM_CY_PORT6_CLK_CTL (cont.)

Bits	Name	Description
4	CLK_BRANCH_ENA	This bit is used to enable the clock branch. 0x1: Enable 0x0: Diable
3:1	RESERVED_BITS3_1	RESERVED
0	SRC_SEL	This bit selects between SCPLL1 aux output or PXO clock. 0x1: SCPLL1_aux 0x0: PXO (default)

0x00902F7C SPDM_CY_PORT7_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the control for enabling and inverting the SPDM CY port7 clock. SPDM CY port 7 clock is a divided version of SCPLL2 aux output clock. We must enable the AUX source output of SCPLL2 as well in order to see this clock properly.

SPDM_CY_PORT7_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert the clock. 0x1: Inverted 0x0: Not inverted
4	CLK_BRANCH_ENA	This bit is used to enable the clock branch. 0x1: Enable 0x0: Diable
3:1	RESERVED_BITS3_1	RESERVED
0	SRC_SEL	This bit selects between SCPLL2 aux output or PXO clock. 0x1: SCPLL2_aux 0x0: PXO (default)

0x00902F80 RESET_ALL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0

This register controls the sw_ares_all. "sw_ares_all" is a means for SW to assert all "reset" bits for various blocks/bridges/cores which are under SW control in one-shot WITHOUT impacting the clock control's internal reset. With this bit, we can maintain mission mode speeds while reseting.

RESET_ALL

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	RESET_ALL	Setting this bit will trigger software reset to everything on chip 0x1: Active

0x00902F84 RESET_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: X

The RESET_STATUS register indicates the source of the last reset.

NOTE Since this register reflects the source of the last reset, its Reset State cannot be defined since the source of the reset can not be known before it occurs. Typically, the RESET_STATUS value will be 0x4 indicating that the Security Control module was the last element to trigger a Power On Reset.

RESET_STATUS

Bits	Name	Description
31:4	RESERVED_BITS31_4	RESERVED
3:0	STATUS	The source fo the last reset. 0x0: RESIN_N 0x1: WDOG_EXPIRED 0x2: MPM_PU_RESET 0x3: SRST (pi_srst_n NAND qdss_srst_n) 0x4: Security control power on reset 0x8: QDSS_SRST_N

0x00902FA0 CLK_TEST

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x00

The CLK_TEST register is used for conrotrolling the clock debug bus and generation of the debug clocks.

CLK_TEST

Bits	Name	Description
31:29	RESERVED_BITS31_29	RESERVED
28:27	HS_DBG_OUTPUT_DIV	Select Divide ratio for high speed debug clock output divide. 0x0: Divide-1 0x1: Divide-2 0x2: Divide-3 0x3: Divide-4
26	RING_OSC_DBG_SEL	Select between ring_osc_clk or dbg_hs_clk Set (1) to this bit to enable the test TCXO counter and test clock counter to check the function of the high speed debug clock. Clear (0) to this bit to select the ring oscillator clock source instead. 0x1: cc_dbg_hs_clk 0x0: cc_ringosc_clk
25	SC_LEAF_CLK_INV	Set (1) this bit to invert the Scorpion high-speed leaf debug clock. 0x1: Inverted 0x0: Not inverted
24	SC_LEAF_CLK_ENA	This bit is used to enable the SMPSS debug clocks. Set (1) this bit to enable the Scorpion high-speed leaf debug cloc. 0x1: Enable 0x0: Diable
23	TEST_BUS_ENA	This bit is used to enable the debug bus. When disable, the debug bus coming out of clock control will be zero. 0x1: Enable 0x0: Diable

CLK_TEST (cont.)

Bits	Name	Description
22:19	TEST_BUS_SEL	This field is used to configure clk_dbg_bus: Bit 31 qdss_at_clk_slp_ret_n Bit 30 qdss_at_clk_slp_nret_n Bit 29 GND Bit 28 GND Bit 27 GND_TIE Bit 26 GND_TIE Bit 25- sdc1_hclk_slp_ret_n Bit 24- sdc1_hclk_slp_nret_n Bit 23- sdc2_hclk_slp_ret_n Bit 22- sdc2_hclk_slp_nret_n Bit 21- sdc3_hclk_slp_ret_n Bit 20- sdc3_hclk_slp_nret_n Bit 19- sdc4_hclk_slp_ret_n Bit 18- sdc4_hclk_slp_nret_n Bit 17- GND Bit 16- GND Bit 15- pmem_aclk_slp_ret_n Bit 14- pmem_aclk_slp_nret_n Bit 13- ppss_hclk_slp_ret_n Bit 12- ppss_hclk_slp_nret_n Bit 11- dma_bam_hclk_slp_ret_n Bit 10- dma_bam_hclk_slp_nret_n Bit 09- gsbi1_hclk_slp_ret_n Bit 08- gsbi1_hclk_slp_nret_n Bit 07- gsbi2_hclk_slp_ret_n Bit 06- gsbi2_hclk_slp_nret_n Bit 05- gsbi3_hclk_slp_ret_n Bit 04- gsbi3_hclk_slp_nret_n Bit 03- gsbi4_hclk_slp_ret_n Bit 02- gsbi4_hclk_slp_nret_n Bit 01- gsbi5_hclk_slp_ret_n Bit 00- gsbi5_hclk_slp_nret_n Bit 31- gsbi6_hclk_slp_ret_n Bit 30- gsbi6_hclk_slp_nret_n Bit 29- gsbi7_hclk_slp_ret_n Bit 28- gsbi7_hclk_slp_nret_n Bit 27- sata_aclk_slp_ret_n Bit 26- sata_aclk_slp_nret_n Bit 25- sata_hclk_slp_ret_n Bit 24- sata_hclk_slp_nret_n Bit 23- pcie_aclk_slp_ret_n Bit 22- pcie_aclk_slp_ret_n Bit 21- pcie_pclk_slp_ret_n Bit 20- pcie_pclk_slp_ret_n Bit 19- GND Bit 18- GND

CLK_TEST (cont.)

Bits	Name	Description
		Bit 17- rpm_bus_hclk_slp_ret_n Bit 16- rpm_bus_hclk_slp_nret_n Bit 15- qfprom_slp_n Bit 14- acc_rom_slp_n Bit 13- acc_ram_slp_ret_n Bit 12- acc_ram_slp_nret_n Bit 11- rpm_msg_ram_hclk_slp_ret_n Bit 10- rpm_msg_ram_hclk_slp_nret_n Bit 09- adm0_clk_slp_ret_n Bit 08- adm0_clk_slp_nret_n Bit 07- adm1_clk_slp_ret_n Bit 06- adm1_clk_slp_nret_n Bit 05- GND_TIE Bit 04- GND_TIE Bit 03- imem0_aclk_slp_ret_n Bit 02- imem0_aclk_slp_nret_n Bit 01- usb_hs1_hclk_slp_ret_n Bit 00- usb_hs1_hclk_slp_nret_n Bit 19- sdc1_apps_clk_slp_nret_n Bit 18- sdc1_apps_clk_slp_ret_n Bit 17- sdc2_apps_clk_slp_nret_n Bit 16- sdc2_apps_clk_slp_ret_n Bit 15- sdc3_apps_clk_slp_nret_n Bit 14- sdc3_apps_clk_slp_ret_n Bit 13- sdc4_apps_clk_slp_nret_n Bit 12- sdc4_apps_clk_slp_ret_n Bit 11- GND Bit 10- GND Bit 09- usb_hsic_system_clk_slp_ret_n Bit 08- usb_hsic_system_clk_slp_nret_n Bit 07- usb_fs1_system_clk_slp_ret_n Bit 06- usb_fs1_system_clk_slp_nret_n Bit 05- usb_fs2_system_clk_slp_ret_n Bit 04- usb_fs2_system_clk_slp_nret_n Bit 03- tsif_hclk_slp_ret_n Bit 02- tsif_hclk_slp_nret_n Bit 01- GND_TIE Bit 00- GND_TIE 0x0: CLK_HALT_AFAB_SFAB_STATEA (Application and system fabric group A clock off) 0x1: CLK_HALT_AFAB_SFAB_STATEB (Application and system fabric group B clock off) 0x2: CLK_HALT_DFAB_STATE (Smart Peripheral Subsystem SPS clock off) 0x3: CLK_HALT_CFPB_STATEA (Chip Fast Perpherial group A clock off) 0x4: CLK_HALT_CFPB_STATEB (Chip Fast Perpherial group B clock off)

CLK_TEST (cont.)

Bits	Name	Description
		0x5: CLK_HALT_CFPB_STATEC (Chip Fast Perpherial group C clock off) 0x6: CLK_HALT_SFPB_MISC_STATE (System Fast Perpherial and miscellaneous clock off) 0x7: CLK_HALT_MSS_KPSS_MISC_STATE (MSS KPSS and miscellaneous clock off) 0x8: PLL test out (scpll0_droop_cal_done, scpll1_droop_cal_done, sc_l2_pll_droop_cal_done, pll0, mmcc_pll0, mmcc_pll1, gpll1, lcc_pri_pll, pll5, pll8, scpll0, scpll1, pll11, sc_l2_pll, pll13, pll14) 0x9: Clock Memory FS Status 1 0xA: Clock Memory FS Status 2 0xB: Clock Memory FS Status 3
18	RESERVED_BIT18	RESERVED
17	HS_DBG_CLK_BRANCH_ENA	Enable for high speed debug clock. 0x1: Enable

CLK_TEST (cont.)

Bits	Name	Description
16:10	DBG_CLK_HS_SEL	Debug clock selection 0x0: afab_ebi1_ch0_aclk 0x1: afab_kpss_m0_aclk 0x2: afab_kpss_m1_aclk 0x3: afab_sfab_m0_aclk 0x4: afab_sfab_m1_aclk 0x5: afab_smpss_s_aclk 0x6: afab_sfab_s_aclk 0x7: afab_core_clk 0x8: afab_axi_s0_fclk 0x9: afab_axi_s1_fclk 0xA: afab_axi_s2_fclk 0xB: afab_axi_s3_fclk 0xC: afab_axi_s4_fclk 0xD: sfab_afab_m_aclk 0xE: sfab_adm0_m0_aclk 0xF: sfab_adm0_m1_aclk 0x10: sfab_adm0_m2_hclk 0x11: GND_1 0x12: GND_2 0x13: ebi1_ch0_2x 0x14: ebi1_ch1_2x 0x15: sfab_lpass_q6_aclk 0x16: sfab_afab_s0_aclk 0x17: sfab_afab_s1_aclk 0x18: sfab_core_clk 0x19: sfab_axi_s0_fclk 0x1A: sfab_axi_s1_fclk 0x1B: sfab_axi_s2_fclk 0x1C: sfab_axi_s3_fclk 0x1D: sfab_axi_s4_fclk 0x1E: sfab_ahb_s0_fclk 0x1F: sfab_ahb_s1_fclk 0x20: sfab_ahb_s2_fclk 0x21: sfab_ahb_s3_fclk 0x22: sfab_ahb_s4_fclk 0x23: sfab_ahb_s5_fclk 0x24: sfab_ahb_s6_fclk 0x25: sfab_ahb_s7_fclk 0x26: GND_3 0x27: GND_4 0x28: sc_aclk 0x29: sc_dbg_clk 0x2A: adm0_clk_raw 0x2B: pcie_aux_clk 0x2C: imem0_aclk 0x2D: pcie_pclk

CLK_TEST (cont.)

Bits	Name	Description
		0x2E: mmss_cc_dbg_hs_in_clk 0x2F: lpass_cc_dbg_hs_in_clk 0x30: lpass_q6_cc_dbg_hs_in_clk 0x31: sata_aclk 0x32: pcie_aclk 0x33: ebi1_clk_src 0x34: ddr_clk 0x35: ebi1_ch0_cc_dbg_hs_clk 0x36: ebi1_ch1_cc_dbg_hs_clk 0x37: spdm_cy_port0_clk 0x38: spdm_cy_port1_clk 0x39: spdm_cy_port2_clk 0x3A: spdm_cy_port4_clk 0x3B: spdm_cy_port5_clk 0x3C: spdm_cy_port6_clk 0x3D: spdm_cy_port7_clk 0x3E: spdm_cy_port8_clk 0x3F: sc_l2_clk (Aux output of l2 PLL divided by 2 This shares the same clock as SPDM CY PORT4 clock source. In order to see this clock, we need to config to the right source by programming spdm_cy_port4_clk_ctl register.) 0x40: sc_dbg_hs0_clk 0x41: sc_dbg_hs1_clk 0x42: GND_5 0x43: Low Speed debug clock (cc_dbg_ls_out_clk) 0x44: sec_ctrl_acc_clk 0x45: GND_6 0x46: GND_7 0x47: GND_8 0x48: qdss_at_clk 0x49: qdss_pclkdbg_clk 0x4A: qdss_traceclkin_clk 0x4B: qdss_tsctr_clk 0x4C: GND_9 0x4D: GND_10 0x4E: GND_11 0x4F: qdss_stm_clk 0x50: usb_hsic_hsic_clk 0x51: riva_cc_dbg_clk_hs 0x52: afab_ebi1_ch1_aclk 0x53: sfab_axi_s5_fclk 0x54: sfab_ahb_s8_fclk
9	RESERVED_BIT9	RESERVED
8	LS_DBG_CLK_BRANCH_ENA	Enable for low speed debug clock. 0x1: Enable

CLK_TEST (cont.)

Bits	Name	Description
7:0	DBG_CLK_LS_SEL	Debug clock selection 0x0: sfab_dfab_m_aclk 0x1: sfab_cfpb_m_hclk 0x2: sfab_sfpb_m_hclk 0x3: sfab_dfab_s_aclk 0x4: sfab_smpss_s_hclk 0x5: qdss_hclk 0x6: sfab_cfpb_s_hclk 0x7: sfab_sfpb_s_hclk 0x8: GND_1 0x9: gnd_tie_1 0xA: gss_slp_clk 0xB: GND_2 0xC: GND_3 0xD: sc_hclk 0xE: sc_xo_src 0xF: lpass_cxo_src 0x10: lpass_pxo_src 0x11: lpass_mxo_src 0x12: sdc1_hclk 0x13: sdc1_apps_clk 0x14: sdc2_hclk 0x15: sdc2_apps_clk 0x16: sdc3_hclk 0x17: sdc3_apps_clk 0x18: sdc4_hclk 0x19: sdc4_apps_clk 0x1A: GND_4 0x1B: GND_5 0x1C: ebi1_xo_src 0x1D: gss_cxo_src 0x1E: GND_6 0x1F: gp0_clk 0x20: gp1_clk 0x21: gp2_clk 0x22: ring_osc_clk 0x23: dfab_sfab_m_aclk 0x24: dfab_sfab_s_aclk 0x25: dfab_core_clk 0x26: pmem_aclk 0x27: dfab_sway0_hclk 0x28: dfab_sway1_hclk 0x29: dfab_arb0_hclk 0x2A: dfab_arb1_hclk 0x2B: ppss_hclk 0x2C: ppss_proc_clk 0x2D: ppss_timer0_clk

CLK_TEST (cont.)

Bits	Name	Description
		0x2E: ppss_timer1_clk 0x2F: sps_tic_hclk 0x30: GND_7 0x31: sic_hclk 0x32: dma_bam_hclk 0x33: cfpb0_hclk 0x34: gnd_tie_2 0x35: cfpb1_hclk 0x36: gnd_tie_3 0x37: cfpb2_hclk 0x38: gnd_tie_4 0x39: gnd_tie_5 0x3A: cfpb_splitter_hclk 0x3B: cfpb_master_nohwgate_hclk 0x3C: cfpb_master_hclk 0x3D: gsbi1_hclk 0x3E: gsbi1_uart_apps_clk 0x3F: gsbi1_qup_apps_clk 0x40: gsbi1_sim_clk_src 0x41: gsbi2_hclk 0x42: gsbi2_uart_apps_clk 0x43: gsbi2_sim_clk_src 0x44: gsbi2_qup_apps_clk 0x45: gsbi3_hclk 0x46: gsbi3_uart_apps_clk 0x47: gsbi3_sim_clk_src 0x48: gsbi3_qup_apps_clk 0x49: gsbi4_hclk 0x4A: gsbi4_uart_apps_clk 0x4B: gsbi4_sim_clk_src 0x4C: gsbi4_qup_apps_clk 0x4D: gsbi5_hclk 0x4E: gsbi5_uart_apps_clk 0x4F: gsbi5_sim_clk_src 0x50: gsbi5_qup_apps_clk 0x51: gsbi6_hclk 0x52: gsbi6_uart_apps_clk 0x53: gsbi6_sim_clk_src 0x54: gsbi6_qup_apps_clk 0x55: gsbi7_hclk 0x56: gsbi7_uart_apps_clk 0x57: gsbi7_sim_clk_src 0x58: gsbi7_qup_apps_clk 0x59: sfab_sata_s_hclk 0x5A: sata_hclk 0x5B: sata_rxoob_clk 0x5C: sata_pmalive_clk 0x5D: pcie_alt_ref_clk

CLK_TEST (cont.)

Bits	Name	Description
		0x5E: pcie_hclk 0x5F: ce3_hclk 0x60: ce3_core_clk 0x61: ce3_sleep_clk 0x62: GND_8 0x63: usb_hs3_hclk 0x64: usb_hs3_xcvr_fs_clk 0x65: usb_hs4_hclk 0x66: usb_hs4_xcvr_fs_clk 0x67: GND_9 0x68: GND_10 0x69: GND_11 0x6A: GND_12 0x6B: sata_phy_ref_clk 0x6C: sata_phy_cfg_clk 0x6D: mpm_hclk 0x6E: bbrx_ssbi_clk 0x6F: tlmm_hclk 0x70: tlmm_clk 0x71: spdm_cfg_hclk 0x72: spdm_mstr_hclk 0x73: spdm_ff_clk 0x74: rpm_sleep_clk 0x75: rpm_proc_clk 0x76: rpm_bus_hclk 0x77: rpm_timer_clk 0x78: sfpb_nohwgate_hclk 0x79: sfpb_hclk 0x7A: pmic_ssbi2_clk 0x7B: pmic_arb0_hclk 0x7C: pmic_arb1_hclk 0x7D: prng_clk 0x7E: sec_ctrl_clk 0x7F: rpm_msg_ram_hclk 0x80: adm0_pbus_hclk 0x81: GND_TIE_1 0x82: pdm_clk 0x83: pdm_xo4_clk 0x84: usb_hs1_hclk 0x85: usb_hs1_xcvr_fs_clk 0x86: usb_hsic_hclk 0x87: usb_hsic_system_clk 0x88: usb_hsic_xcvr_fs_clk 0x89: usb_fs1_hclk 0x8A: usb_fs1_system_clk 0x8B: usb_fs1_xcvr_fs_clk 0x8C: GND_13 0x8D: GND_14

CLK_TEST (cont.)

Bits	Name	Description
		0x8E: GND_15 0x8F: tsif_hclk_raw 0x90: tsif_inactivity_timers_clk 0x91: tsif_ref_clk 0x92: ce1_hclk 0x93: ce2_hclk 0x94: tssc_clk 0x95: GND_16 0x96: sc_cc_dbg_ls_clk 0x97: mmss_cc_dbg_ls_in_clk 0x98: lpass_cc_dbg_ls_in_clk 0x99: lpass_q6_cc_dbg_ls_in_clk 0x9A: gss_cc_dbg_hs_clk 0x9B: gss_cc_dbg_ls_clk 0x9C: ce2_core_clk 0x9D: usb_hsic_hsio_io_cal_clk 0x9E: GND_TIE_2 0x9F: GND_TIE_3 0xA0: spdm_cy_port3_clk 0xA1: Voltage_sensor debug clock 0xA2: mmss_pxo_src 0xA3: GND_17 0xA4: ce1_core_clk 0xA5: ce1_sleep_clk 0xA6: riva_cc_dbg_clk_ls 0xA7: GND_18 0xA8: cfpb0_c0_hclk 0xA9: cfpb0_d0_hclk 0xAA: cfpb0_c1_hclk 0xAB: cfpb0_d1_hclk 0xAC: ebi1_ch0_ca_xo_src 0xAD: ebi1_ch0_dq_xo_src 0xAE: ebi1_ch1_ca_xo_src 0xAF: ebi1_ch1_dq_xo_src

0x00902FA4 PLLTEST_PAD_CFG

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x058016

The PLLTEST_PAD_CFG register is used to configure the PLLTEST DE pad. By default, CORE_IE_N is set as enabled so that a test clock can be driven into the chip for sourcing the ACC clock in production vector.

PLLTEST_PAD_CFG

Bits	Name	Description
31:27	RESERVED_BITS31_27	RESERVED
26:24	DROOP_SEL	These values are selected when 0x0: scpll0_droop_test_se1 0x1: scpll0_droop_test_se2 0x2: scpll1_droop_test_se1 0x3: scpll1_droop_test_se2 0x4: sc_l2_pll_droop_test_se1 0x5: sc_l2_pll_droop_test_se2 0x6: scpll2_droop_test_se1 0x7: scpll2_droop_test_se2
23:21	OUT_SEL2	0x0: This selects all the signals given under OUT_SEL and OUT_SEL1 0x1: afab_core_clk_src 0x2: afab_core_clk 0x3: sfab_core_clk_src 0x4: sfab_core_clk 0x5: qdss_at_clk 0x6: GND_TIE_1 0x7: GND_TIE_2
20	RT_EN	This bit is used to enable termination resistor on the transmitter side. 0x1: Enable 0x0: Disable
19:18	PULL_INPUT_N	These bits are used to control the pull-state of input path of padsig_n. 0x0: None 0x1: Pulldown 0x2: Keep 0x3: Pull Up
17:16	PULL_INPUT_P	These bits are used to control the pull-state of input path of padsig_p. 0x0: None 0x1: Pulldown 0x2: Keep 0x3: Pull Up
15	CORE_IE_N	This bit is used to enable the single-ended input path of padsig_n. 0x1: Enabled 0x0: Disable
14	CORE_IE_P	This bit is used to enable the single-ended input path of padsig_p. 0x1: Enabled 0x0: Disable

PLLTEST_PAD_CFG (cont.)

Bits	Name	Description
13	CORE_OE	This bit is used to enable the output pad. 0x1: Enabled 0x0: Disable
12	MUX_EN	This bit is used to enable the high voltage mux which muxes together the pllout_hv signals of each PLL. 0x1: Enabled 0x0: Disable
11:5	OUT_SEL	These bits are used to select the output signal. All the test clocks are gated at the source. It must be enabled before the clock can be propagated to be muxed out. NOTE: The signals below are selected when OUT_SEL1 and OUT_SEL2 are '000' PLLTEST output muxing 0x0: sc_l2_pll_out_test 0x1: mmcc_pll0_out_test 0x2: scpll1_out_test 0x3: scpll0_out_test 0x4: scpll2_out_test 0x5: scpll3_out_test 0x6: scpll3_droop_test_se1 0x7: scpll3_droop_test_se2 0x20: ebi1_ch0_cc_dbg_hs_clk 0x21: lpass_q6_cc_dbg_hs_in_clk 0x22: sc_dbg_hs0_clk (div2 version) 0x23: sc_dbg_hs1_clk (div2 version) 0x24: sc_dbg_hs2_clk (div2 version) 0x25: usb_phy0_clockout 0x26: mmss_cc_dbg_hs_in_clk 0x27: dbg_ls_clk (see CLK_TEST for configuration) 0x40: pll0_out_test 0x41: cc_mmcc_pll1_out_test 0x42: cc_gpll1_out_test 0x43: cc_lcc_pri_pll_out_test, 0x44: pll5_out_test 0x45: GND_TIE 0x46: pll8_out_test 0x47: dbg_hs_clk (see CLK_TEST for configuration) 0x60: pll11_out_test
4:3	CORE_DRIVE	These bits are used to configure the output driver output amplitude. 0x3: 300 mV (single ended) 0x2: 250 mV (single ended) 0x1: 200 mV (single ended) 0x0: 150 mV (single ended.)

PLLTEST_PAD_CFG (cont.)

Bits	Name	Description
2:0	OUT_SEL1	NOTE: The signals below are selected when OUT_SEL2 and OUT_SEL are '000' PLLTEST output muxing 0x0: This selects all the signals given under OUT_SEL 0x1: GND_TIE_1 0x2: pll13_out_test 0x3: pxo_clk_src 0x4: GND_TIE_2 0x5: scpll_droop_test_se (selected by DROOP_SEL) 0x6: pll14_out_test 0x7: mmcc_pll3_out_test

0x00902FA8 CLKTEST_PAD_CFG

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x08000

The CLKTEST_PAD_CFG register is used to configure the CLKTEST pad.

CLKTEST_PAD_CFG

Bits	Name	Description
31:17	RESERVED_BITS31_17	RESERVED
16:15	PULL_SE	These bits are used to set the single-ended pad pull-state. 0x0: None 0x1: Pulldown 0x2: Keep 0x3: Pull Up
14	CORE_IE	This bit is used to enable the single-ended input path. 0x1: Enabled 0x0: Disable
13	SE_OE	This bit is used to enable the single-ended output pad. 0x1: Enabled 0x0: Disable
12	RESERVED_BIT12	RESERVED
11:9	OUT_SEL_SINGLE	These bits are used to select the single-ended output signal.
8:5	RESERVED_BITS8_5	RESERVED
4:2	CORE_HDRIVE	These bits are used to configure the output drive strength. This is hard-wired to 24 mA drive strength.
1:0	RESERVED_BITS1_0	RESERVED

0x00902FAC JITTER_PROBE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0xFF

Jitter probe enable and init counter value. See PLLTEST_PAD_CFG for Jitter probe reference clock selection.

JITTER_PROBE

Bits	Name	Description
31:9	RESERVED_BITS31_9	RESERVED
8	EN	Enable of the jitter probe macro. 0x1: Enabled 0x0: Disabled
7:0	INIT_COUNTER	Initial value of bit 8 counter.

0x00902FB0 JITTER_PROBE_VAL

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

Jitter probe read value

JITTER_PROBE_VAL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	COUNT_VALUE	8 bit value represents the reference clock period in terms of half FO 1.3 inv delay under the operating PVT condition.

0x00902FC0 CLK_HALT_AFAB_SFAB_STATEA

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The CLK_HALT_AFAB_SFAB_STATEA is used to indicate the halt state of the Application and system clocks. There are 2 parts, A and B. Each bit indicates the halt state of the corresponding clock branch. A set (1) bit indicates that the clock branch is halted (disabled or *_clk_off=1).

CLK_HALT_AFAB_SFAB_STATEA

Bits	Name	Description
31	AFAB_SMPSS_M0_ACLK	0x1: Halted 0x0: Not Halted
30	AFAB_SMPSS_M1_ACLK	0x1: Halted 0x0: Not Halted
29	AFAB_SFAB_M0_ACLK	0x1: Halted 0x0: Not Halted
28	AFAB_SFAB_M1_ACLK	0x1: Halted 0x0: Not Halted
27	AFAB_SMPSS_S_ACLK	0x1: Halted 0x0: Not Halted
26	AFAB_SFAB_S_ACLK	0x1: Halted 0x0: Not Halted
25	AFAB_CORE_CLK	0x1: Halted 0x0: Not Halted
24	AFAB_EBI1_CH0_ACLK	Clock Halt state for AFAB_EBI1_CH0_ACLK and EBI1_CH0_ACLK. 0x1: Halted 0x0: Not Halted
23	AFAB_AXI_S0_FCLK	0x1: Halted 0x0: Not Halted
22	AFAB_AXI_S1_FCLK	0x1: Halted 0x0: Not Halted
21	AFAB_AXI_S2_FCLK	0x1: Halted 0x0: Not Halted
20	AFAB_AXI_S3_FCLK	0x1: Halted 0x0: Not Halted
19	AFAB_AXI_S4_FCLK	0x1: Halted 0x0: Not Halted
18	SFAB_AFAB_M_ACLK	0x1: Halted 0x0: Not Halted
17	SFAB_DFAB_M_ACLK	0x1: Halted 0x0: Not Halted
16	SFAB_ADM0_M0_ACLK	0x1: Halted 0x0: Not Halted
15	SFAB_ADM0_M1_ACLK	0x1: Halted 0x0: Not Halted
14	SFAB_ADM0_M2_HCLK	0x1: Halted 0x0: Not Halted

CLK_HALT_AFAB_SFAB_STATEA (cont.)

Bits	Name	Description
13	PCIE_ACLK	Clock Halt state for PCIE_ACLK, SFAB_PCIE_M_ACLK and SFAB_PCIE_S_ACLK. 0x1: Halted 0x0: Not Halted
12	SATA_ACLK	Clock Halt state for SATA_ACLK and SFAB_SATA_M_ACLK. 0x1: Halted 0x0: Not Halted
11	RESERVED_BIT11	RESERVED
10	SFAB_LPASS_Q6_ACLK	0x1: Halted 0x0: Not Halte
9	AFAB_EBI1_CH1_ACLK	Clock Halt state for AFAB_EBI1_CH1_ACLK and EBI1_CH1_ACLK. 0x1: Halted 0x0: Not Halted
8	SFAB_CFPB_M_HCLK	0x1: Halted 0x0: Not Halted
7	SFAB_SFPB_M_HCLK	0x1: Halted 0x0: Not Halted
6	SFAB_AFAB_S0_ACLK	0x1: Halted 0x0: Not Halted
5	SFAB_AFAB_S1_ACLK	0x1: Halted 0x0: Not Halted
4	SFAB_DFAB_S_ACLK	0x1: Halted 0x0: Not Halted
3	IMEM_ACLK	Clock Halt state for IMEM0_ACLK and SFAB_IMEM_S0_ACLK 0x1: Halted 0x0: Not Halted
2	SFAB_SMPSS_S_HCLK	0x1: Halted 0x0: Not Halted
1	RESEVED_BIT1	RESERVED
0	SFAB_CORE_CLK	0x1: Halted 0x0: Not Halted

0x00902FC4 CLK_HALT_AFAB_SFAB_STATEB

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The CLK_HALT_AFAB_SFAB_STATEB is used to indicate the halt state of the Application and system clocks. There are 2 parts, A and B. Each bit indicates the halt state of the corresponding clock branch. A set (1) bit indicates that the clock branch is halted (disabled or *_clk_off=1).

CLK_HALT_AFAB_SFAB_STATEB

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23	SFAB_AXI_S5_FCLK	0x1: Halted 0x0: Not Halted
22:21	RESERVED_BITS22_21	RESERVED
20	QDSS_STM_CLK	0x1: Halted 0x0: Not Halted
19	SFAB_AHB_S7_FCLK	0x1: Halted 0x0: Not Halted
18	SFAB_AHB_S8_FCLK	0x1: Halted 0x0: Not Halted
17	RESERVED_BIT17	RESERVED
16	CE3_HCLK	Clock Halt state for CE3_HCLK, SFAB_CE3_M_HCLK, and SFAB_CE3_S_HCLK.
15	RESERVED_BIT15	RESERVED
14	SFAB_SATA_S_HCLK	0x1: Halted 0x0: Not Halted
13	SFAB_CFPB_S_HCLK	0x1: Halted 0x0: Not Halted
12	SFAB_SFPB_S_HCLK	0x1: Halted 0x0: Not Halted
11	SFAB_AXI_S0_FCLK	0x1: Halted 0x0: Not Halted
10	SFAB_AXI_S1_FCLK	0x1: Halted 0x0: Not Halted
9	SFAB_AXI_S2_FCLK	0x1: Halted 0x0: Not Halted
8	SFAB_AXI_S3_FCLK	0x1: Halted 0x0: Not Halted
7	SFAB_AXI_S4_FCLK	0x1: Halted 0x0: Not Halted
6	SFAB_AHB_S0_FCLK	0x1: Halted 0x0: Not Halted
5	SFAB_AHB_S1_FCLK	0x1: Halted 0x0: Not Halted

CLK_HALT_AFAB_SFAB_STATEB (cont.)

Bits	Name	Description
4	SFAB_AHB_S2_FCLK	0x1: Halted 0x0: Not Halted
3	SFAB_AHB_S3_FCLK	0x1: Halted 0x0: Not Halted
2	SFAB_AHB_S4_FCLK	0x1: Halted 0x0: Not Halted
1	SFAB_AHB_S5_FCLK	0x1: Halted 0x0: Not Halted
0	SFAB_AHB_S6_FCLK	0x1: Halted 0x0: Not Halted

0x00902FC8 CLK_HALT_DFAB_STATE

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The CLK_HALT_DFAB_STATE is used to indicate the halt state of all the Smart Peripheral Subsystem fabric and peripheral clocks. Each bit indicates the halt state of the corresponding clock branch. A set (1) bit indicates that the clock branch is halted (disabled or *_clk_off=1).

CLK_HALT_DFAB_STATE

Bits	Name	Description
31	USB_HS3_HCLK	0x1: Halted 0x0: Not Halted
30	USB_HS3_XCVR_FS_CLK	0x1: Halted 0x0: Not Halted
29	RESERVED_BIT29	RESERVED
28	RESERVED_BIT28	RESERVED
27	DFAB_SFAB_M_ACLK	0x1: Halted 0x0: Not Halted
26	DFAB_SFAB_S_ACLK	0x1: Halted 0x0: Not Halted
25	DFAB_CORE_CLK	0x1: Halted 0x0: Not Halted
24	DFAB_SWAY0_HCLK	0x1: Halted 0x0: Not Halted

CLK_HALT_DFAB_STATE (cont.)

Bits	Name	Description
23	DFAB_SWAY1_HCLK	0x1: Halted 0x0: Not Halted
22	DFAB_ARB0_HCLK	0x1: Halted 0x0: Not Halted
21	DFAB_ARB1_HCLK	0x1: Halted 0x0: Not Halted
20	PMEM_ACLK	0x1: Halted 0x0: Not Halted
19	PPSS_HCLK	0x1: Halted 0x0: Not Halted
18	PPSS_PROC_CLK	0x1: Halted 0x0: Not Halted
17	PPSS_TIMER0_CLK	0x1: Halted 0x0: Not Halted
16	PPSS_TIMER1_CLK	0x1: Halted 0x0: Not Halted
15	SPS_TIC_HCLK	0x1: Halted 0x0: Not Halted
14	RESERVED_BIT14	RESERVED
13	SIC_HCLK	0x1: Halted 0x0: Not Halted
12	DMA_BAM_HCLK	0x1: Halted 0x0: Not Halted
11	SDC1_HCLK	0x1: Halted 0x0: Not Halted
10	SDC2_HCLK	0x1: Halted 0x0: Not Halted
9	SDC3_HCLK	0x1: Halted 0x0: Not Halted
8	SDC4_HCLK	0x1: Halted 0x0: Not Halted
7	USB_HS4_HCLK	0x1: Halted 0x0: Not Halted
6	SDC1_APPS_CLK	0x1: Halted 0x0: Not Halted
5	SDC2_APPS_CLK	0x1: Halted 0x0: Not Halted

CLK_HALT_DFAB_STATE (cont.)

Bits	Name	Description
4	SDC3_APPS_CLK	0x1: Halted 0x0: Not Halted
3	SDC4_APPS_CLK	0x1: Halted 0x0: Not Halted
2	USB_HS4_XCVR_FS_CLK	0x1: Halted 0x0: Not Halted
1	USB_HS1_HCLK	0x1: Halted 0x0: Not Halted
0	USB_HS1_XCVR_FS_CLK	0x1: Halted 0x0: Not Halted

0x00902FCC CLK_HALT_CFPB_STATEA

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The CLK_HALT_CFPB_STATEA is used to indicate the halt state of all the Chip Fast Peripheral Bus and its peripheral clocks. There are 3 parts, A, B and C. Each bit indicates the halt state of the corresponding clock branch. A set (1) bit indicates that the clock branch is halted (disabled or *_clk_off=1).

CLK_HALT_CFPB_STATEA

Bits	Name	Description
31:30	RESERVED_BITS31_30	RESERVED
29	CFPB0_HCLK	0x1: Halted 0x0: Not Halted
28	USB_HSIC_HCLK	0x1: Halted 0x0: Not Halted
27	CFPB1_HCLK	0x1: Halted 0x0: Not Halted
26	USB_HSIC_XCVR_FS_CLK	0x1: Halted 0x0: Not Halted
25	CFPB2_HCLK	0x1: Halted 0x0: Not Halted
24	USB_HSIC_SYSTEM_CLK	0x1: Halted 0x0: Not Halted

CLK_HALT_CFPB_STATEA (cont.)

Bits	Name	Description
23	USB_HSIC_HSIO_IO_CAL_CLK	0x1: Halted 0x0: Not Halted
22	CFPB_SPLITTER_HCLK	0x1: Halted 0x0: Not Halted
21	CFPB_MASTER_NOHWGATE_HCLK	0x1: Halted 0x0: Not Halted
20	CFPB_MASTER_HCLK	0x1: Halted 0x0: Not Halted
19	USB_HSIC_HSIC_CLK	0x1: Halted 0x0: Not Halted
18	RESERVED_BITS18	RESERVED
17	USB_FS1_HCLK	0x1: Halted 0x0: Not Halted
16	USB_FS1_SYSTEM_CLK	0x1: Halted 0x0: Not Halted
15	USB_FS1_XCVR_FS_CLK	0x1: Halted 0x0: Not Halted
14:13	RESERVED_BITS14_13	RESERVED
12	SATA_PHY_CFG_CLK	0x1: Halted 0x0: Not Halted
11	GSBI1_HCLK	0x1: Halted 0x0: Not Halted
10	GSBI1_UART_APPS_CLK	0x1: Halted 0x0: Not Halted
9	GSBI1_QUP_APPS_CLK	0x1: Halted 0x0: Not Halted
8	GSBI1_SIM_CLK_SRC	0x1: Halted 0x0: Not Halted
7	GSBI2_HCLK	0x1: Halted 0x0: Not Halted
6	GSBI2_UART_APPS_CLK	0x1: Halted 0x0: Not Halted
5	GSBI2_SIM_CLK_SRC	0x1: Halted 0x0: Not Halted
4	GSBI2_QUP_APPS_CLK	0x1: Halted 0x0: Not Halted
3	GSBI3_HCLK	0x1: Halted 0x0: Not Halted

CLK_HALT_CFPB_STATEA (cont.)

Bits	Name	Description
2	GSBI3_UART_APPS_CLK	0x1: Halted 0x0: Not Halted
1	GSBI3_SIM_CLK_SRC	0x1: Halted 0x0: Not Halted
0	GSBI3_QUP_APPS_CLK	0x1: Halted 0x0: Not Halted

0x00902FD0 CLK_HALT_CFPB_STATEB

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The CLK_HALT_CFPB_STATEB is used to indicate the halt state of all the Chip Fast Peripheral Bus and its peripheral clocks. There are 3 parts, A, B and C. Each bit indicates the halt state of the corresponding clock branch. A set (1) bit indicates that the clock branch is halted (disabled or *_clk_off=1).

CLK_HALT_CFPB_STATEB

Bits	Name	Description
31:29	RESERVED_BITS31_29	RESERVED
28	CE2_CORE_CLK	0x1: Halted 0x0: Not Halted
27	GSBI4_HCLK	0x1: Halted 0x0: Not Halted
26	GSBI4_UART_APPS_CLK	0x1: Halted 0x0: Not Halted
25	GSBI4_SIM_CLK_SRC	0x1: Halted 0x0: Not Halted
24	GSBI4_QUP_APPS_CLK	0x1: Halted 0x0: Not Halted
23	GSBI5_HCLK	0x1: Halted 0x0: Not Halted
22	GSBI5_UART_APPS_CLK	0x1: Halted 0x0: Not Halted
21	GSBI5_SIM_CLK_SRC	0x1: Halted 0x0: Not Halted

CLK_HALT_CFPB_STATEB (cont.)

Bits	Name	Description
20	GSBI5_QUP_APPS_CLK	0x1: Halted 0x0: Not Halted
19	GSBI6_HCLK	0x1: Halted 0x0: Not Halted
18	GSBI6_UART_APPS_CLK	0x1: Halted 0x0: Not Halted
17	GSBI6_SIM_CLK_SRC	0x1: Halted 0x0: Not Halted
16	GSBI6_QUP_APPS_CLK	0x1: Halted 0x0: Not Halted
15	GSBI7_HCLK	0x1: Halted 0x0: Not Halted
14	GSBI7_UART_APPS_CLK	0x1: Halted 0x0: Not Halted
13	GSBI7_SIM_CLK_SRC	0x1: Halted 0x0: Not Halted
12	GSBI7_QUP_APPS_CLK	0x1: Halted 0x0: Not Halted
11:0	RESERVED_BITS11_0	RESERVED

0x00902FD4 CLK_HALT_CFPB_STATEC

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The CLK_HALT_CFPB_STATEC is used to indicate the halt state of all the Chip Fast Peripheral Bus and its peripheral clocks. There are 3 parts, A, B and C. Each bit indicates the halt state of the corresponding clock branch. In addition to part C of the CFPB related clocks, it also reports the halt state of the 8 SPDM CY port clocks. A set (1) bit indicates that the clock branch is halted (disabled or *_clk_off=1).

CLK_HALT_CFPB_STATEC

Bits	Name	Description
31	CFPB0_C0_HCLK	0x1: Halted 0x0: Not Halted
30	CFPB0_D0_HCLK	0x1: Halted 0x0: Not Halted

CLK_HALT_CFPB_STATEC (cont.)

Bits	Name	Description
29	CFPB0_C1_HCLK	0x1: Halted 0x0: Not Halted
28	CFPB0_D1_HCLK	0x1: Halted 0x0: Not Halted
27	CE1_CORE_CLK	0x1: Halted 0x0: Not Halted
26	SPDM_CY_PORT7_CLK	0x1: Halted 0x0: Not Halted
25	SPDM_CY_PORT6_CLK	0x1: Halted 0x0: Not Halted
24	SPDM_CY_PORT5_CLK	0x1: Halted 0x0: Not Halted
23	SPDM_CY_PORT4_CLK	0x1: Halted 0x0: Not Halted
22	SPDM_CY_PORT3_CLK	0x1: Halted 0x0: Not Halted
21	SPDM_CY_PORT2_CLK	0x1: Halted 0x0: Not Halted
20	SPDM_CY_PORT1_CLK	0x1: Halted 0x0: Not Halted
19	SPDM_CY_PORT0_CLK	0x1: Halted 0x0: Not Halted
18	SPDM_CY_PORT8_CLK	0x1: Halted 0x0: Not Halted
17:9	RESERVED_BITS17_9	RESERVED
8	PCIE_HCLK	0x1: Halted 0x0: Not Halted
7	TSIF_HCLK_RAW	0x1: Halted 0x0: Not Halted
6	TSIF_INACTIVITY_TIMERS_CLK	0x1: Halted 0x0: Not Halted
5	TSIF_REF_CLK	0x1: Halted 0x0: Not Halted
4	TSSC_CLK	0x1: Halted 0x0: Not Halted
3	PDM_CLK	0x1: Halted 0x0: Not Halted

CLK_HALT_CFPB_STATEC (cont.)

Bits	Name	Description
2	PDM_XO4_CLK	0x1: Halted 0x0: Not Halted
1	CE1_HCLK	0x1: Halted 0x0: Not Halted
0	CE2_HCLK	0x1: Halted 0x0: Not Halted

0x00902FD8 CLK_HALT_SFPB_MISC_STATE

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The CLK_HALT_SFPB_MISC_STATE is used to indicate the halt state of all the System Fast Peripheral Bus, its peripheral clocks and some miscellaneous clocks. Each bit indicates the halt state of the corresponding clock branch. A set (1) bit indicates that the clock branch is halted (disabled or *_clk_off=1).

CLK_HALT_SFPB_MISC_STATE

Bits	Name	Description
31:30	RESERVED_BITS31_30	RESERVED
29	RPM_SLEEP_CLK	0x1: Halted 0x0: Not Halted
28	RPM_PROC_CLK	0x1: Halted 0x0: Not Halted
27	RPM_BUS_HCLK	0x1: Halted 0x0: Not Halted
26	RPM_TIMER_CLK	0x1: Halted 0x0: Not Halted
25	SFPB_NOHWGATE_HCLK	0x1: Halted 0x0: Not Halted
24	SFPB_HCLK	0x1: Halted 0x0: Not Halted
23	PMIC_SSBI2_CLK	0x1: Halted 0x0: Not Halted
22	PMIC_ARB0_HCLK	0x1: Halted 0x0: Not Halted

CLK_HALT_SFPB_MISC_STATE (cont.)

Bits	Name	Description
21	PMIC_ARB1_HCLK	0x1: Halted 0x0: Not Halted
20	SPDM_CFG_HCLK	0x1: Halted 0x0: Not Halted
19	SPDM_MSTR_HCLK	0x1: Halted 0x0: Not Halted
18	SPDM_FF_CLK	0x1: Halted 0x0: Not Halted
17	TLMM_HCLK	0x1: Halted 0x0: Not Halted
16	TLMM_CLK	0x1: Halted 0x0: Not Halted
15	MPM_HCLK	0x1: Halted 0x0: Not Halted
14	SEC_CTRL_CLK	0x1: Halted 0x0: Not Halted
13	SEC_CTRL_ACC_CLK	0x1: Halted 0x0: Not Halted
12	RPM_MSG_RAM_HCLK	0x1: Halted 0x0: Not Halted
11	QDSS_HCLK	0x1: Halted 0x0: Not Halted
10	PRNG_CLK	0x1: Halted 0x0: Not Halted
9	RING_OSC_CLK	0x1: Halted 0x0: Not Halted
8	BBRX_SSBI_CLK	0x1: Halted 0x0: Not Halted
7	GP0_CLK	0x1: Halted 0x0: Not Halted
6	GP1_CLK	0x1: Halted 0x0: Not Halted
5	GP2_CLK	0x1: Halted 0x0: Not Halted
4	MMSS_PXO_SRC	0x1: Halted 0x0: Not Halted
3	MMSS_MXO_SRC	0x1: Halted 0x0: Not Halted

CLK_HALT_SFPB_MISC_STATE (cont.)

Bits	Name	Description
2	LPASS_CXO_SRC	0x1: Halted 0x0: Not Halted
1	LPASS_PXO_SRC	0x1: Halted 0x0: Not Halted
0	LPASS_MXO_SRC	0x1: Halted 0x0: Not Halted

0x00902FDC CLK_HALT_GSS_KPSS_MISC_STATE

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The CLK_HALT_GSS_KPSS_MISC_STATE is used to indicate the halt state of the Scorpion sub-system and some miscellaneous clocks. Each bit indicates the halt state of the corresponding clock branch. A set (1) bit indicates that the clock branch is halted (disabled or *_clk_off=1).

CLK_HALT_GSS_KPSS_MISC_STATE

Bits	Name	Description
31	PCIE_AUX_CLK	0x1: Halted 0x0: Not Halted
30	PCIE_ALT_REF_CLK	0x1: Halted 0x0: Not Halted
29	PCIE_PCLK	0x1: Halted 0x0: Not Halted
28	EBI1_2X_DDR_CLK_SRC	0x1: Halted 0x0: Not Halted
27	SATA_HCLK	0x1: Halted 0x0: Not Halted
26	SATA_RXOOB_CLK	0x1: Halted 0x0: Not Halted
25	SATA_PMALIVE_CLK	0x1: Halted 0x0: Not Halted
24	SATA_PHY_REF_CLK	0x1: Halted 0x0: Not Halted
23	TSENS_SLP_CLK	0x1: Halted 0x0: Not Halted

CLK_HALT_GSS_KPSS_MISC_STATE (cont.)

Bits	Name	Description
22	EBI1_CH0_CA_XO_SRC	0x1: Halted 0x0: Not Halted
21	EBI1_CH0_DQ_XO_SRC	0x1: Halted 0x0: Not Halted
20	EBI1_CH1_CA_XO_SRC	0x1: Halted 0x0: Not Halted
19	EBI1_CH1_DQ_XO_SRC	0x1: Halted 0x0: Not Halted
18	GSS_CXO_SRC	0x1: Halted 0x0: Not Halted
17	EBI1_XO_SRC	0x1: Halted 0x0: Not Halted
16	EBI1_2X_CH0_CLK_SRC	0x1: Halted 0x0: Not Halted
15	EBI1_2X_CH1_CLK_SRC	0x1: Halted 0x0: Not Halted
14	ADM0_CLK	0x1: Halted 0x0: Not Halted
13	ADM0_PBUS_HCLK	0x1: Halted 0x0: Not Halted
12	RESERVED_BIT12	RESERVED
11	CE1_SLEEP_CLK	0x1: Halted 0x0: Not Halted
10	QDSS_AT_CLK	0x1: Halted 0x0: Not Halted
9	QDSS_PCLKDBG_CLK	0x1: Halted 0x0: Not Halted
8	QDSS_TRACECLKIN_CLK	0x1: Halted 0x0: Not Halted
7	QDSS_TSCTR_CLK	0x1: Halted 0x0: Not Halted
6	GSS_SLP_CLK	0x1: Halted 0x0: Not Halted
5	CE3_CORE_CLK	0x1: Halted 0x0: Not Halted
4	CE3_SLEEP_CLK	0x1: Halted 0x0: Not Halted

CLK_HALT_GSS_KPSS_MISC_STATE (cont.)

Bits	Name	Description
3	SC_ACLK	0x1: Halted 0x0: Not Halted
2	SC_HCLK	0x1: Halted 0x0: Not Halted
1	RESERVED_BIT1	RESERVED
0	SC_XO_SRC	0x1: Halted 0x0: Not Halted

0x00902FE0 RPM_CLK_BRANCH_ENA_VOTE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0380

The RPM_CLK_BRANCH_ENA_VOTE register is the clock enable votes dedicated to RPM ARM7 for clocks that are votable. The vote for clock branch enables is only a vote for ON scheme (The clock will be disabled only if all Masters vote for OFF). RPM ARM7 votes are considered to be the main vote for all the votable clocks.

The votable clocks include:

- Scorpion AXI and AHB clocks -- Voting only with RPM, and Scorpion Core 0 and 1
- ADM0 and ADM1 core clocks and pbus clocks
- RPM message ram clock
- PMIC SSBI2, arbitor 0 and 1 hclk
- PRNG clock

Some bits in this register are set (1) on RESOUT to allow the chip to function only at a basic start-up level. All clock branches are enabled (active) and operating at the CXO frequency during RESOUT. The enable signals do not take effect until the RESOUT is de-asserted.

Set (1) enables the corresponding clock branch.

Clear (0) disables the corresponding clock branch.

RPM_CLK_BRANCH_ENA_VOTE

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12	SC_HCLK_ENA	Enable SMPSS AHB clock. 0x1: Enabled

RPM_CLK_BRANCH_ENA_VOTE (cont.)

Bits	Name	Description
11	SC_ACLK_ENA	Enable SMPSS AXI clock. This also enables the clocks for the 3 fabric axi ports interfacing with SMPSS. 0x1: Enabled
10	PRNG_CLK_ENA	Enable for PRNG clock. 0x1: Enable
9	PMIC_ARB1_HCLK_ENA	Enable PMIC Arbiter 1 clock. 0x1: Enabled
8	PMIC_ARB0_HCLK_ENA	Enable PMIC Arbiter 0 clock. 0x1: Enabled
7	PMIC_SSBI2_CLK_ENA	Enable for PMIC SSBI2 clock. 0x1: Enable
6	RPM_MSG_RAM_HCLK_ENA	Enable for RPM message ram clock. 0x1: Enable
5:4	RESERVED_BITS5_4	RESERVED
3	ADM0_PBUS_CLK_ENA	Enable for ADM0 PBUS clock 0x1: Enable
2	ADM0_CLK_ENA	Enable ADM0 clock 0x1: Enabled
1:0	RESERVED_BITS1_0	RESERVED

0x00902FE4 RPM_CLK_SLEEP_ENA_VOTE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

The RPM_CLK_SLEEP_ENA_VOTE register is used to halt the corresponding clock signals when the RPM ARM7 processor goes to standby by deasserting rpm_proc_clkon signal. The value of each bit is correspondingly combined with the bit in RPM_CLK_BRANCH_ENA_VOTE register. If clock is not enabled in RPM_CLK_BRANCH_ENA register, it will NOT enable upon interrupt.

- Set (1) allows the clock to halt when RPM ARM7 goes to standby mode.
- Clear (0) does not allow the clock to halt when RPM ARM7 goes to standby mode.

RPM_CLK_SLEEP_ENA_VOTE

Bits	Name	Description
31	RPM_PROC_CLK_PRE	This field selects if RPM ARM7 clock is halted before halting others. 0x1: Enabled
30	RPM_PROC_CLK_SLEEP_ENA	Halt RPM ARM7 processor clock upon standby. When this bit is set, the clk_branch_ena bit in rpm_proc_clk_ctl register will have no affect in turning on the rpm_proc_clk. With this bit set, the rpm_proc_clk can only be turned on by programming the appropiate register in RPM to enable its processor clock. Please note that rpm_proc_clk is also conditioned on the enabling of rpm_bus_hclk first. 0x1: Enabled
29:13	RESERVED_BITS29_13	RESERVED
12	SC_HCLK_SLEEP_ENA	Halt SMPSS AHB clock upon standby. 0x1: Enabled
11	SC_ACLK_SLEEP_ENA	Halt SMPSS AXI clock upon standby. This also halts the clocks for the 3 fabric axi ports interfacing with SMPSS. 0x1: Enabled
10	PRNG_CLK_SLEEP_ENA	Haltr PRNG clock upon standby. 0x1: Enable
9	PMIC_ARB1_HCLK_SLEEP_ENA	Halt PMIC Arbiter 1 clock upon standby. 0x1: Enabled
8	PMIC_ARB0_HCLK_SLEEP_ENA	Halt PMIC Arbiter 0 clock upon standby. 0x1: Enabled
7	PMIC_SSBI2_CLK_SLEEP_ENA	Halt PMIC SSBI2 clock upon standby. 0x1: Enable
6	RPM_MSG_RAM_HCLK_SLEEP_ENA	Halt RPM message ram clock upon standby. 0x1: Enable
5:4	RESERVED_BITS5_4	RESERVED
3	ADM0_PBUS_CLK_SLEEP_ENA	Halt ADM0 PBUS clock upon standby. 0x1: Enable
2	ADM0_CLK_SLEEP_ENA	halt ADM0 clock upon standby. 0x1: Enabled
1:0	RESERVED_BITS1_0	RESERVED

0x00903020 LPA_Q6_CLK_BRANCH_ENA_VOTE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

The LPA_Q6_CLK_BRANCH_ENA_VOTE register is the clock enable votes dedicated to LPASS Q6 for clocks that are votable. The vote for clock branch enables is only a vote for ON scheme (The clock will be disabled only if all Masters vote for OFF).

The votable clocks include:

- Scorpion AXI and AHB clocks -- Voting only with RPM, and Scorpion Core 0 and 1
- ADM0 and ADM1 core clocks and pbus clocks
- RPM message ram clock.
- PMIC SSBI2, arbitor 0 and 1 hclk
- PRNG clock

Some bits in this register are set (1) on RESOUT to allow the chip to function only at a basic start-up level. All clock branches are enabled (active) and operating at the CXO frequency during RESOUT. The enable signals do not take effect until the RESOUT is de-asserted.

Set (1) enables the corresponding clock branch.

Clear (0) disables the corresponding clock branch.

LPA_Q6_CLK_BRANCH_ENA_VOTE

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12:11	RESERVED_BITS12_11	RESERVED
10	PRNG_CLK_ENA	Enable for PRNG clock. 0x1: Enable
9	PMIC_ARB1_HCLK_ENA	Enable PMIC Arbiter 1 clock. 0x1: Enabled
8	PMIC_ARB0_HCLK_ENA	Enable PMIC Arbiter 0 clock. 0x1: Enabled
7	PMIC_SSBI2_CLK_ENA	Enable for PMIC SSBI2 clock. 0x1: Enable
6	RPM_MSG_RAM_HCLK_ENA	Enable for RPM message ram clock. 0x1: Enable
5:4	RESERVED_BITS5_4	RESERVED
3	ADM0_PBUS_CLK_ENA	Enable for ADM0 PBUS clock. 0x1: Enable
2	ADM0_CLK_ENA	Enable ADM0 clock. 0x1: Enabled
1:0	RESERVED_BITS1_0	RESERVED

0x00903024 LPA_Q6_CLK_SLEEP_ENA_VOTE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

The LPA_Q6_CLK_SLEEP_ENA_VOTE register is used to halt the corresponding clock signals when the LPA_Q6 processor goes to standby by asserting lpass_cc_qdsp6_core_idle signal. The value of each bit is correspondingly combined with the bit in LPA_Q6_CLK_BRANCH_ENA_VOTE register. If clock is not enabled in LPA_Q6_CLK_BRANCH_ENA register, it will NOT enable upon interrupt.

- Set (1) allows the clock to halt when LPASS Q6 goes to standby mode.
- Clear (0) does not allow the clock to halt when LPASS Q6 goes to standby mode.

LPA_Q6_CLK_SLEEP_ENA_VOTE

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12:11	RESERVED_BITS12_11	RESERVED
10	PRNG_CLK_SLEEP_ENA	Halt PRNG clock upon standby. 0x1: Enable
9	PMIC_ARB1_HCLK_SLEEP_ENA	Halt PMIC Arbiter 1 clock upon standby. 0x1: Enabled
8	PMIC_ARB0_HCLK_SLEEP_ENA	Halt PMIC Arbiter 0 clock upon standby. 0x1: Enabled
7	PMIC_SSBI2_CLK_SLEEP_ENA	Halt PMIC SSBI2 clock upon standby. 0x1: Enable
6	RPM_MSG_RAM_HCLK_SLEEP_ENA	Halt RPM message ram clock upon standby. 0x1: Enable
5:4	RESERVED_BITS5_4	RESERVED
3	ADM0_PBUS_CLK_SLEEP_ENA	Halt ADM0 PBUS clock upon standby. 0x1: Enable
2	ADM0_CLK_SLEEP_ENA	halt ADM0 clock upon standby. 0x1: Enabled
1:0	RESERVED_BITS1_0	RESERVED

0x00903040 APCS_CLK_BRANCH_ENA_VOTE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

The APCS_CLK_BRANCH_ENA_VOTE register is the clock enable votes dedicated to trusted side of Scorpion core0 for clocks that are votable. The vote for clock branch enables is only a vote for ON scheme (The clock will be disabled only if all Masters vote for OFF).

The votable clocks include:

- Scorpion AXI and AHB clocks -- Voting only with RPM, and Scorpion Core 0 and 1
- ADM0 and ADM1 core clocks and pbus clocks
- RPM message ram clock
- PMIC SSBI2, arbitor 0 and 1 hclk
- PRNG clock

Some bits in this register are set (1) on RESOUT to allow the chip to function only at a basic start-up level. All clock branches are enabled (active) and operating at the CXO frequency during RESOUT. The enable signals do not take effect until the RESOUT is de-asserted.

Set (1) enables the corresponding clock branch.

Clear (0) disables the corresponding clock branch.

APCS_CLK_BRANCH_ENA_VOTE

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12	SC_HCLK_ENA	Enable SMPSS AHB clock. 0x1: Enabled
11	SC_ACLK_ENA	Enable SMPSS AXI clock. This also enables the clocks for the 3 fabric axi ports interfacing with SMPSS. 0x1: Enabled
10	PRNG_CLK_ENA	Enable for PRNG clock. 0x1: Enable
9	PMIC_ARB1_HCLK_ENA	Enable PMIC Arbiter 1 clock. 0x1: Enabled
8	PMIC_ARB0_HCLK_ENA	Enable PMIC Arbiter 0 clock. 0x1: Enabled
7	PMIC_SSBI2_CLK_ENA	Enable for PMIC SSBI2 clock. 0x1: Enable
6	RPM_MSG_RAM_HCLK_ENA	Enable for RPM message ram clock. 0x1: Enable
5:4	RESERVED_BITS5_4	RESERVED
3	ADM0_PBUS_CLK_ENA	Enable for ADM0 PBUS clock. 0x1: Enable

APCS_CLK_BRANCH_ENA_VOTE (cont.)

Bits	Name	Description
2	ADM0_CLK_ENA	Enable ADM0 clock. 0x1: Enabled
1:0	RESERVED_BITS1_0	RESERVED

0x00903044 APCS_CLK_SLEEP_ENA_VOTE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

The APCS_CLK_SLEEP_ENA_VOTE register is used to halt the corresponding clock signals when the Trusted side of Scorpion core 0 processor goes to standby by deasserting SCSS_stdbyClkEnable signal. The value of each bit is correspondingly combined with the bit in APCS_CLK_BRANCH_ENA_VOTE register. If clock is not enabled in APCS_CLK_BRANCH_ENA register, it will NOT enable upon interrupt.

- Set (1) allows the clock to halt when Trusted side of Scorpion core 0 goes to standby mode.
- Clear (0) does not allow the clock to halt when Trusted side of Scorpion core 0 goes to standby mode.

APCS_CLK_SLEEP_ENA_VOTE

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12	SC_HCLK_SLEEP_ENA	Halt SMPSS AHB clock upon standby. 0x1: Enabled
11	SC_ACLK_SLEEP_ENA	Halt SMPSS AXI clock upon standby. This also halts the clocks for the 3 fabric axi ports interfacing with SMPSS. 0x1: Enabled
10	PRNG_CLK_SLEEP_ENA	Haltr PRNG clock upon standby. 0x1: Enable
9	PMIC_ARB1_HCLK_SLEEP_ENA	Halt PMIC Arbiter 1 clock upon standby. 0x1: Enabled
8	PMIC_ARB0_HCLK_SLEEP_ENA	Halt PMIC Arbiter 0 clock upon standby. 0x1: Enabled
7	PMIC_SSBI2_CLK_SLEEP_ENA	Halt PMIC SSBI2 clock upon standby. 0x1: Enable
6	RPM_MSG_RAM_HCLK_SLEEP_ENA	Halt RPM message ram clock upon standby. 0x1: Enable
5:4	RESERVED_BITS5_4	RESERVED

APCS_CLK_SLEEP_ENA_VOTE (cont.)

Bits	Name	Description
3	ADM0_PBUS_CLK_SLEEP_ENA	Halt ADM0 PBUS clock upon standby. 0x1: Enable
2	ADM0_CLK_SLEEP_ENA	halt ADM0 clock upon standby. 0x1: Enabled
1:0	RESERVED_BITS1_0	RESERVED

0x00903060 SPARE_CLK_BRANCH_ENA_VOTE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

The SPARE_CLK_BRANCH_ENA_VOTE register is the clock enable votes dedicated as spare for clocks that are votable. The vote for clock branch enables is only a vote for ON scheme (The clock will be disabled only if all Masters vote for OFF).

The votable clocks include:

- Scorpion AXI and AHB clocks -- Voting only with RPM, and Scorpion Core 0 and 1
- ADM0 and ADM1 core clocks and pbus clocks
- RPM message ram clock
- PMIC SSBI2, arbitor 0 and 1 hclk
- PRNG clock

Some bits in this register are set (1) on RESOUT to allow the chip to function only at a basic start-up level. All clock branches are enabled (active) and operating at the CXO frequency during RESOUT. The enable signals do not take effect until the RESOUT is de-asserted.

Set (1) enables the corresponding clock branch.

Clear (0) disables the corresponding clock branch.

SPARE_CLK_BRANCH_ENA_VOTE

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12	SC_HCLK_ENA	Enable SMPSS AHB clock. 0x1: Enabled
11	SC_ACLK_ENA	Enable SMPSS AXI clock. This also enables the clocks for the 3 fabric axi ports interfacing with SMPSS. 0x1: Enabled

SPARE_CLK_BRANCH_ENA_VOTE (cont.)

Bits	Name	Description
10	PRNG_CLK_ENA	Enable for PRNG clock. 0x1: Enable
9	PMIC_ARB1_HCLK_ENA	Enable PMIC Arbiter 1 clock. 0x1: Enabled
8	PMIC_ARB0_HCLK_ENA	Enable PMIC Arbiter 0 clock. 0x1: Enabled
7	PMIC_SSBI2_CLK_ENA	Enable for PMIC SSBI2 clock. 0x1: Enable
6	RPM_MSG_RAM_HCLK_ENA	Enable for RPM message ram clock. 0x1: Enable
5:4	RESERVED_BITS5_4	RESERVED
3	ADM0_PBUS_CLK_ENA	Enable for ADM0 PBUS clock. 0x1: Enable
2	ADM0_CLK_ENA	Enable ADM0 clock. 0x1: Enabled
1:0	RESERVED_BITS1_0	RESERVED

0x00903080 APCS_U_CLK_BRANCH_ENA_VOTE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

The APCS_U_CLK_BRANCH_ENA_VOTE register is the clock enable votes dedicated to untrusted side of Scorpion core0 for clocks that are votable. The vote for clock branch enables is only a vote for ON scheme (The clock will be disabled only if all Masters vote for OFF).

The votable clocks include:

- Scorpion AXI and AHB clocks -- Voting only with RPM, and Scorpion Core 0 and 1
- ADM0 and ADM1 core clocks and pbus clocks
- RPM message ram clock
- PMIC SSBI2, arbitor 0 and 1 hclk
- PRNG clock

Some bits in this register are set (1) on RESOUT to allow the chip to function only at a basic start-up level. All clock branches are enabled (active) and operating at the CXO frequency during RESOUT. The enable signals do not take effect until the RESOUT is de-asserted.

Set (1) enables the corresponding clock branch.

Clear (0) disables the corresponding clock branch.

APCS_U_CLK_BRANCH_ENA_VOTE

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12	SC_HCLK_ENA	Enable SMPSS AHB clock. 0x1: Enabled
11	SC_ACLK_ENA	Enable SMPSS AXI clock. This also enables the clocks for the 3 fabric axi ports interfacing with SMPSS. 0x1: Enabled
10	PRNG_CLK_ENA	Enable for PRNG clock. 0x1: Enable
9	PMIC_ARB1_HCLK_ENA	Enable PMIC Arbiter 1 clock. 0x1: Enabled
8	PMIC_ARB0_HCLK_ENA	Enable PMIC Arbiter 0 clock. 0x1: Enabled
7	PMIC_SSBI2_CLK_ENA	Enable for PMIC SSBI2 clock. 0x1: Enable
6	RPM_MSG_RAM_HCLK_ENA	Enable for RPM message ram clock. 0x1: Enable
5:4	RESERVED_BITS5_4	RESERVED
3	ADM0_PBUS_CLK_ENA	Enable for ADM0 PBUS clock. 0x1: Enable
2	ADM0_CLK_ENA	Enable ADM0 clock. 0x1: Enabled
1:0	RESERVED_BITS1_0	RESERVED

0x00903084 APCS_U_CLK_SLEEP_ENA_VOTE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

The APCS_U_CLK_SLEEP_ENA_VOTE register is used to halt the corresponding clock signals when the untrusted side of Scorpion core 0 processor goes to standby by deasserting SCSS_stdbyClkEnable signal. The value of each bit is correspondingly combined with the bit in APCS_U_CLK_BRANCH_ENA_VOTE register. If clock is not enabled in APCS_U_CLK_BRANCH_ENA register, it will NOT enable upon interrupt.

- Set (1) allows the clock to halt when untrusted side of Scorpion core 0 goes to standby mode.

- Clear (0) does not allow the clock to halt when untrusted side of Scorpion core 0 goes to standby mode.

APCS_U_CLK_SLEEP_ENA_VOTE

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12	SC_HCLK_SLEEP_ENA	Halt SMPSS AHB clock upon standby. 0x1: Enabled
11	SC_ACLK_SLEEP_ENA	Halt SMPSS AXI clock upon standby. This also halts the clocks for the 3 fabric axi ports interfacing with SMPSS. 0x1: Enabled
10	PRNG_CLK_SLEEP_ENA	Haltr PRNG clock upon standby. 0x1: Enable
9	PMIC_ARB1_HCLK_SLEEP_ENA	Halt PMIC Arbiter 1 clock upon standby. 0x1: Enabled
8	PMIC_ARB0_HCLK_SLEEP_ENA	Halt PMIC Arbiter 0 clock upon standby. 0x1: Enabled
7	PMIC_SSBI2_CLK_SLEEP_ENA	Halt PMIC SSBI2 clock upon standby. 0x1: Enable
6	RPM_MSG_RAM_HCLK_SLEEP_ENA	Halt RPM message ram clock upon standby. 0x1: Enable
5:4	RESERVED_BITS5_4	RESERVED
3	ADM0_PBUS_CLK_SLEEP_ENA	Halt ADM0 PBUS clock upon standby. 0x1: Enable
2	ADM0_CLK_SLEEP_ENA	halt ADM0 clock upon standby. 0x1: Enabled
1:0	RESERVED_BITS1_0	RESERVED

0x009030C0 PLL0_MODE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The PLL0_MODE register configures and controls PLL0 (SVS. Global Bus PLL - SR) . All register bits are cleared (0) on RESOUT.

PLL0_MODE

Bits	Name	Description
31:22	RESERVED_BITS31_22	RESERVED

PLL0_MODE (cont.)

Bits	Name	Description
21	PLL_VOTE_FSM_RESET	Resets PLL voting FSM. 0x0: De-asserts Reset to PLL voting FSM 0x1: Resets PLL voting FSM
20	PLL_VOTE_FSM_ENA	Enables PLL voting FSM. 0x0: Disabled 0x1: Enabled
19:14	PLL_BIAS_COUNT	Sets PLL bias count of PLL voting FSM.
13:8	PLL_LOCK_COUNT	Sets PLL lock time of PLL voting FSM.
7:5	RESERVED_BITS_7_5	RESERVED
4	PLL_REF_XO_SEL	Specify the reference XO to be used. 0x0: PXO (27MHz) 0x1: GND
3	PLL_PLLTEST	Set (1) this bit to enter the PLL test mode. Clear (0) this bit for the normal mode.
2	PLL_RESET_N	Low asserted reset for the digital logic in the PLL. This includes the MND counters and integer divider.
1	PLL_BYPASSNL	Clear (0) to bypass the PLL (PLLOUT is then identical to the input reference). Set (1) to use the PLL. Default is clear (0) at RESOUT (different from previous APQs).
0	PLL_OUTCTRL	Set (1) to activate the PLL's outputs (the analog circuitry is active but the output is not). Set (1) will enable the following PLL's outputs: PLLOUT_LV_MAIN (if MAIN output enabled PLL0_CONFIG[23]) PLLOUT_LV_BIST (If BIST output enabled PLL0_TEST_CTL[13]) PLLOUT_LV_AUX (If AUX output enabled PLL0_TEST_CTL[12]) Clear (0) to disable the PLL's output and save power. Clears (0) at RESOUT.

0x009030C4 PLL0_L_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The following equation (fractional division ratio) is used to calculate the PLL0 (NT PLL) output frequency:

VCO = REF * [L+(M/N)] / (R * P)

Where:

- R represents the predivider of 2
- P represents the post divider

The value of the PLL0_L_VAL register is the given value of L for that equation.

PLL0_L_VAL

Bits	Name	Description
31:10	RESERVED_BITS31_10	UNUSED (This is the original assignment before CR154463.)
31	ICP_TST_EN	PLL_TEST_CTL(9) Charge pump test current control. 0x0: Disable 0x1: Enable
27:26	NMOSC_FREQ_CTL	PLL_CONFIG_CTL(27:26) 0x0: Highest (2.8 GHz at TT / 1.05V /40C) 0x1: 1/2 highest 0x2: 1/3 highest 0x3: 1/4 highest
25:24	PFD_DZSEL	PLL_CONFIG_CTL(25:24) PFD reset pulse width adjustment 0x0: 1x delay 0x1: 2x delay 0x2: 3x delay 0x3: 4x delay
23	NMOSC_EN	PLL_CONFIG_CTL(23) Noise measurement oscillator control. 0x0: Disable 0x1: Enable

PLL0_L_VAL (cont.)

Bits	Name	Description
21:20	ICP_DIV	PLL_CONFIG_CTL(21:20) Charge pump bias mirror multiplication factor. 0x0: 1 0x1: 3/2 0x2: 7/4 0x3: 9/4
19:18	IREG_DIV	PLL_CONFIG_CTL(19:18) Regulator bias mirror multiplication factor. 0x0: 1 0x1: 7/5 0x2: 9/5 0x3: 11/5
17:16	CUSEL	PLL_CONFIG_CTL(17:16) VCO decoupling cap unit size. 0x0: 125 fF 0x1: 250 fF 0x2: 375 fF 0x3: 500 fF
15	REF_MODE	PLL_CONFIG_CTL(15) Reference circuit mode. 0x0: Bandgap mode (seed currents sourced from bandgap circuit and Nwell reference circuit active). 0x1: Supply independent mode (seed currents sourced from supply independent circuit amd Nwell reference pulled to VDDA).
14	PLLOUT_LV_TEST	PLL_TEST_CTL(14) PLLOUT_LV_TEST source selection 0x0: PLL output clock 0x1: Noise measurement oscillator
13:12	CFG_LOCKDET	PLL_CONFIG_CTL(13:12) Lock detector phase error threshold. 0x0: 2 pi /7 0x1: 2 pi /15 0x2: 2 pi /23 0x3: 2 pi /31
11	FORCE_ISEED	PLL_CONFIG_CTL(11) Seed current control 0x0: Turn off seed currents when clock is detected 0x1: Keep seed currents on at all times
9:0	PLL_L	This register contains the 10-bit L value in the PLL0’s fractional division ratio.

0x009030C8 PLL0_M_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The value of the PLL0_M_VAL register is the given value of M for the fractional division ratio.

PLL0_M_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED
18:0	PLL_M	This register contains the 19-bit M value of the PLLn's numerator value in the fractional division ratio.

0x009030CC PLL0_N_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x1

The value of the PLL0_N_VAL register is the given value of N for the fractional division ratio.

PLL0_N_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED
18:0	PLL_N	This register contains the 19-bit N value of the PLLn's denominator value in the fractional division ratio.

0x009030D0 PLL0_TEST_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The PLL0_TEST_CTL register is used to enable the TEST, BIST and AUX outputs of PLL0 (NT PLL)

PLL0_TEST_CTL

Bits	Name	Description
31:19	RESERVED_BITS31_19	RESERVED

PLL0_TEST_CTL (cont.)

Bits	Name	Description
18:17	INTERNAL_BITS18_17	Mux selectors for TESTOUT (NOTE: Set PLLTEST to enable TESTOUT). 0x0: select DN_TEST 0x1: select NOCLK 0x2: select UP_TEST 0x3: select VSIG (output of high speed divider)
16	INTERNAL_BIT16	0x0: Direct PLL output 0x1: Inverted PLL output. (test feature to evaluate clock tree duty cycle distortion)
15	INTERNAL_BIT15	0x0: Disable PLLOUT_LV_TEST output 0x1: Enable PLLOUT_LV_TEST output (if outctrl=1)
14	RESERVED_BIT14	RESERVED
13	PLLOUT_BIST_ENABLE	0x0: Disable PLLOUT_LV_BIST output. 0x1: Enable PLLOUT_LV_BIST output (if outctrl=1)
12	PLLOUT_AUX_ENABLE	0x0: Disable PLLOUT_LV_AUX output. 0x1: Enable PLLOUT_LV_AUX output (if outctrl=1)
11:0	INTERNAL_BIT11_0	Bits used for PLL testing.

0x009030D4 PLL0_CONFIG

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0084248B

The PLL0_CONFIG register is used for the PLL0 (NT PLL) for:

- Enable the main output
- Set up integer or fractional mode
- Set up the Post divider ratio
- Set up the Pre-divider ratio
- Select the appropriate VCO depending on the generated frequency

PLL0_CONFIG

Bits	Name	Description
31:28	RESERVED_BITS31_28	PLL0_CONFIG(31:30) : Not Used See PLL0_L_VAL(27:26) that maps to PLL_CONFIG_CTL(27:26) PLL0_CONFIG(29) : Not Used See PLL0_L_VAL(23) that maps to PLL_CONFIG_CTL(23) PLL0_CONFIG(28) : Not Used See PLL0_L_VAL(15) that maps to PLL_CONFIG_CTL(15)
27	EARLY_OUT_ENA	PLL0_CONFIG(27) maps to PLL_CONFIG_CTL(3) PLLOUT_LV_EARLY enable 0x0: Disable 0x1: Enable
26	CLK33_OUT_SEL	Not Used
25	CLK33_OUT_ENA	Not Used
24	OUT_SEL	Not Used
23	MAIN_OUT_ENA	PLL0_CONFIG(23) maps to PLL_CONFIG_CTL(0) PLLOUT_LV_MAIN enable 0x0: Disable 0x1: Enable
22	MN_ACCUM_ENA	PLL0_CONFIG(22) maps to PLL_CONFIG_CTL(14) PLL fractional mode control 0x0: Disable 0x1: Enable
21:20	PLLOUT_DIVIDE	PLL0_CONFIG(21:20) maps to PLL_CONFIG_CTL(8:7) PLL Post-divider control 0x0: Divide by 1 (use this setting when sending reference clock to output) 0x1: Divide by 2 0x2: Divide by 4 0x3: Invalid
19	PRE_DIVIDE	PLL0_CONFIG(19) maps to PLL_CONFIG_CTL(6) PLL pre-divider control 0x0: Divide by 1 0x1: Divide by 2
18	INTERNAL_BIT18	Not Used
17:16	VCO	PLL0_CONFIG(17) maps to PLL_CONFIG_CTL(9) VCO Selection PLL0_CONFIG(16) : Not Used 0x0: Select 100 - 500 MHz VCO 0x1: Select 400 - 1400 MHz VCO

PLL0_CONFIG (cont.)

Bits	Name	Description
15	INTERNAL_BIT15	Not Used
14:0	INTERNAL_BITS14_0	Not Used

0x009030D8 PLL0_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The PLL0_STATUS register is used for reporting PLL state.

NOTE PLLs 1-2 are programmed by registers within MMSS. PLL4 is programmed by registers in LPASS.

PLL0_STATUS

Bits	Name	Description
31:17	RESERVED_BITS31_17	RESERVED
16	PLL_ACTIVE_FLAG	pll_active_flag from PLL voting FSM. It indicates when FSM has enabled the PLL and PLL should be locked.
15:0	PLL_D	PLL0_STATUS(15:1) : Unused and shorted to VSSD PLL0_STATUS(0) : Clock detect

0x009030E0 PLL5_MODE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x20

The PLL5_MODE register configures and controls PLL5 (Modem PLL0 - SR PLL). All register bits are cleared (0) on RESOUT.

PLL5_MODE

Bits	Name	Description
31:22	RESERVED_BITS31_22	RESERVED
21	PLL_VOTE_FSM_RESET	Resets PLL voting FSM 0x0: De-asserts Reset to PLL voting FSM 0x1: Resets PLL voting FSM

PLL5_MODE (cont.)

Bits	Name	Description
20	PLL_VOTE_FSM_ENA	Enables PLL voting FSM 0x0: Disabled 0x1: Enabled
19:14	PLL_BIAS_COUNT	Sets PLL bias count of PLL voting FSM
13:8	PLL_LOCK_COUNT	Sets PLL lock time of PLL voting FSM
7:6	RESERVED_BITS7_6	RESERVED
5:4	PLL_REF_XO_SEL	Specify the reference XO to be used. 0x0: PXO 0x1: GND 0x2: CXO 0x3: GND_TIE
3	PLL_PLLTEST	Set(1) this bit to enter the PLL test mode. Clear (0) this bit for the normal mode.
2	PLL_RESET_N	Low asserted reset for the digital logic in the PLL. This includes the MND counters and integer divider.
1	PLL_BYPASSNL	lear (0) at RESOUT (different from previous APQs).
0	PLL_OUTCTRL	Set (1) to activate the PLL's outputs (the analog circuitry is active but the output is not). Set (1) will enable the following PLL's outputs: PLLOUT_LV_MAIN (if MAIN output enabled PLL5_CONFIG[23]) PLLOUT_LV_BIST (If BIST output enabled PLL5_TEST_CTL[13]) PLLOUT_LV_AUX (If AUX output enabled PLL5_TEST_CTL[12]) Clear (0) to disable the PLL's output and save power. Clears (0) at RESOUT.

0x009030E4 PLL5_L_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The following equation (fractional division ratio) is used to calculate the PLL5 (NT PLL) output frequency:

VCO = REF * [L+(M/N)] / (R * P)

Where:

- R represents the predivider of 2
- P represents the post divider

The value of the PLL5_L_VAL register is the given value of L for that equation.

PLL5_L_VAL

Bits	Name	Description
31:10	RESERVED_BITS31_10	UNUSED (This is the original assignment before CR154463.)
31	ICP_TST_EN	PLL_TEST_CTL(9) Charge pump test current control. 0x0: Disable 0x1: Enable
27:26	NMOSC_FREQ_CTL	PLL_CONFIG_CTL(27:26) 0x0: Highest (2.8 GHz at TT / 1.05V /40C) 0x1: 1/2 highest 0x2: 1/3 highest 0x3: 1/4 highest
25:24	PFD_DZSEL	PLL_CONFIG_CTL(25:24) PFD reset pulse width adjustment. 0x0: 1x delay 0x1: 2x delay 0x2: 3x delay 0x3: 4x delay
23	NMOSC_EN	PLL_CONFIG_CTL(23) Noise measurement oscillator control. 0x0: Disable 0x1: Enable
21:20	ICP_DIV	PLL_CONFIG_CTL(21:20) Charge pump bias mirror multiplication factor. 0x0: 1 0x1: 3/2 0x2: 7/4 0x3: 9/4
19:18	IREG_DIV	PLL_CONFIG_CTL(19:18) Regulator bias mirror multiplication factor. 0x0: 1 0x1: 7/5 0x2: 9/5 0x3: 11/5
17:16	CUSEL	PLL_CONFIG_CTL(17:16) VCO decoupling cap unit size. 0x0: 125 fF 0x1: 250 fF 0x2: 375 fF 0x3: 500 fF

PLL5_L_VAL (cont.)

Bits	Name	Description
15	REF_MODE	PLL_CONFIG_CTL(15) Reference circuit mode 0x0: Bandgap mode (seed currents sourced from bandgap circuit and Nwell reference circuit active). 0x1: Supply independent mode (seed currents sourced from supply independent circuit amd Nwell reference pulled to VDDA)
14	PLLOUT_LV_TEST	PLL_TEST_CTL(14) PLLOUT_LV_TEST source selection 0x0: PLL output clock 0x1: Noise measurement oscillator
13:12	CFG_LOCKDET	PLL_CONFIG_CTL(13:12) Lock detector phase error threshold 0x0: 2 pi /7 0x1: 2 pi /15 0x2: 2 pi /23 0x3: 2 pi /31
11	FORCE_ISEED	PLL_CONFIG_CTL(11) Seed current control 0x0: Turn off seed currents when clock is detected 0x1: Keep seed currents on at all times
9:0	PLL_L	This register contains the 10-bit L value in the PLL0's fractional division ratio.

0x009030E8 PLL5_M_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The value of the PLL5_M_VAL register is the given value of M for the fractional division ratio.

PLL5_M_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED
18:0	PLL_M	This register contains the 19-bit M value of the PLLn's numerator value in the fractional division ratio.

0x009030EC PLL5_N_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x1

The value of the PLL5_N_VAL register is the given value of N for the fractional division ratio.

PLL5_N_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED
18:0	PLL_N	This register contains the 19-bit N value of the PLLn's denominator value in the fractional division ratio.

0x009030F0 PLL5_TEST_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The PLL5_TEST_CTL register is used to enable the TEST, BIST and AUX outputs of PLL5 (SR PLL). The field descriptions show the mapping from 45nm NT wrapper PLL5_TEST_CTL register to SR PLL inputs, PLL_TEST_CTL and PLL_CONFIG_CTL. Some bits of PLL_TEST_CTL and PLL_CONFIG_CTL come from PLL5_L_VAL (CR154463).

PLL5_TEST_CTL

Bits	Name	Description
31:19	RESERVED_BITS31_19	PLL5_TEST_CTL(31:30) : Not Used See PLL5_L_VAL(25:24) that maps to PLL_CONFIG_CTL(25:24) PLL5_TEST_CTL(29:28) : Not Used See PLL5_L_VAL(21:20) that maps to PLL_CONFIG_CTL(21:20) PLL5_TEST_CTL(27:26) : Not Used See PLL5_L_VAL(19:18) that maps to PLL_CONFIG_CTL(19:18) PLL5_TEST_CTL(25:24) : Not Used See PLL5_L_VAL(17:16) that maps to PLL_CONFIG_CTL(17:16) PLL5_TEST_CTL(23:22) : Not Used See PLL5_L_VAL(13:12) that maps to PLL_CONFIG_CTL(13:12) PLL5_TEST_CTL(21) : Not Used See PLL5_L_VAL(11) that maps to PLL_CONFIG_CTL(11) PLL5_TEST_CTL(20) : Not Used. See PLL5_L_VAL(31) that maps to PLL_TEST_CTL(9) PLL5_TEST_CTL(19) : Not Used
18:17	INTERNAL_BITS18_17	PLL5_TEST_CTL(18:17) : Not Used
16	INTERNAL_BIT16	PLL5_TEST_CTL(16) maps to PLL_CONFIG_CTL(5) Output clock polarity 0x0: Do not invert output 0x1: Invert output
15	INTERNAL_BIT15	PLL5_TEST_CTL(15) maps to PLL_CONFIG_CTL(4) PLLOUT_LV_TEST enable 0x0: Disable 0x1: Enable
14	RESERVED_BIT14	PLL5_TEST_CTL(14) : Not used. See PLL5_L_VAL(14) that maps to PLL_TEST_CTL(14)
13	PLLOUT_BIST_ENABLE	PLL5_TEST_CTL(13) maps to PLL_CONFIG_CTL(2) PLLOUT_LV_BIST enable 0x0: Disable 0x1: Enable (must be enabled to use noise generator)
12	PLLOUT_AUX_ENABLE	PLL5_TEST_CTL(12) maps to PLL_CONFIG_CTL(1) PLLOUT_LV_AUX enable 0x0: Disable 0x1: Enable

PLL5_TEST_CTL (cont.)

Bits	Name	Description
11:0	INTERNAL_BIT11_0	PLL5_TEST_CTL(11) : Not Used PLL5_TEST_CTL(10) maps to PLL_TEST_CTL(8) Charge pump external bias control PLL5_TEST_CTL(9:8) maps to PLL_CONFIG_CTL(29:28) PFD force bits PLL5_TEST_CTL(9) = Force PFD up PLL5_TEST_CTL(8) = Force PFD down PLL5_TEST_CTL(7) maps to PLL_TEST_CTL(7) DTEST signal select PLL5_TEST_CTL(6) maps to PLL_TEST_CTL(6) ATEST amplifier bypass control PLL5_TEST_CTL(5:4) maps to PLL_TEST_CTL(5:4) ATEST1 signal select Force PLL filter voltage externally (set PLL_TEST_CTL(6) to 1) PLL5_TEST_CTL(3:2) maps to PLL_TEST_CTL(3:2) ATEST0 signal select PLL5_TEST_CTL(1) maps to PLL_TEST_CTL(1) ATEST1 Control PLL5_TEST_CTL(0) maps to PLL_TEST_CTL(0) ATEST0 Control 0x0: Disable 0x1: Enable 0x0: Normal operation_1 0x1: Force PFD UP -> 1 0x0: Normal operation_2 0x1: Force PFD DN -> 1 0x0: Select clock detect signal 0x1: Select feedback divider output signal 0x0: Do not bypass ATEST buffer amplifier 0x1: Bypass ATEST buffer amplifier 0x0: Observe Nwell reference (set PLL_TEST_CTL6 to 0) 0x1: Observe regulator output (set PLL_TEST_CTL6 to 0) 0x2: Observe PLL filter voltage (set PLL_TEST_CTL6 to 0) 0x3: Supply noise measurement mode

PLL5_TEST_CTL (cont.)

Bits	Name	Description
		0x0: Provide external bias current to charge pump (set PLL_TEST_CTL8 to 1) 0x1: Observe ICO test current (set PLL_TEST_CTL9 to 1) 0x2: Observe bandgap test current 0x3: VSSA 0x0: Disable ATEST1 0x1: Enable ATEST1 0x0: Disable ATEST0 0x1: Enable ATEST0

0x009030F4 PLL5_CONFIG

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0084248B

- The PLL5_CONFIG register is used for the PLL5 (NT PLL) for:
- Enable the main output
- Set up integer or fractional mode
- Set up the Post divider ratio
- Set up the Pre-divider ratio
- Select the appropriate VCO depending on the generated frequency

The field descriptions show the mapping from 45nm NT wrapper PLL5_CONFIG register to SR PLL input, PLL_CONFIG_CTL. Some bits of PLL_CONFIG_CTL come from PLL5_TEST_CTL and PLL5_L_VAL (CR154463).

PLL5_CONFIG

Bits	Name	Description
31:28	RESERVED_BITS31_28	PLL5_CONFIG(31:30) : Not Used See PLL5_L_VAL(27:26) that maps to PLL_CONFIG_CTL(27:26) PLL5_CONFIG(29) : Not Used See PLL5_L_VAL(23) that maps to PLL_CONFIG_CTL(23) PLL5_CONFIG(28) : Not Used See PLL5_L_VAL(15) that maps to PLL_CONFIG_CTL(15)
27	EARLY_OUT_ENA	PLL5_CONFIG(27) maps to PLL_CONFIG_CTL(3) PLLOUT_LV_EARLY enable 0x0: Disable 0x1: Enable

PLL5_CONFIG (cont.)

Bits	Name	Description
26	CLK33_OUT_SEL	Not Used
25	CLK33_OUT_ENA	Not Used
24	OUT_SEL	Not Used
23	MAIN_OUT_ENA	PLL5_CONFIG(23) maps to PLL_CONFIG_CTL(0) PLLOUT_LV_MAIN enable 0x0: Disable 0x1: Enable
22	MN_ACCUM_ENA	PLL5_CONFIG(22) maps to PLL_CONFIG_CTL(14) PLL fractional mode control 0x0: Disable 0x1: Enable
21:20	PLLOUT_DIVIDE	PLL5_CONFIG(21:20) maps to PLL_CONFIG_CTL(8:7) PLL Post-divider control 0x0: Divide by 1 (use this setting when sending reference clock to output) 0x1: Divide by 2 0x2: Divide by 4 0x3: Invalid
19	PRE_DIVIDE	PLL5_CONFIG(19) maps to PLL_CONFIG_CTL(6) PLL pre-divider control 0x0: Divide by 1 0x1: Divide by 2
18	INTERNAL_BIT18	Not Used
17:16	VCO	PLL5_CONFIG(17) maps to PLL_CONFIG_CTL(9) VCO Selection PLL5_CONFIG(16) : Not Used 0x0: Select 100 - 500 MHz VCO 0x1: Select 400 - 1400 MHz VCO
15	INTERNAL_BIT15	Not Used
14:0	INTERNAL_BITS14_0	Not Used

0x009030F8 PLL5_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

the PLL5_STATUS register is used for reporting PLL state.

PLL5_STATUS

Bits	Name	Description
31:17	RESERVED_BITS31_17	RESERVED
16	PLL_ACTIVE_FLAG	pll_active_flag from PLL voting FSM. It indicates when FSM has enabled the PLL and PLL should be locked.
15:0	PLL_D	PLL5_STATUS(15:1) : Unused and shorted to VSSD PLL5_STATUS(0) : Clock detect

0x00903140 PLL8_MODE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The PLL8_MODE register configures and controls PLL8 (SPS PLL - SR PLL). All register bits are cleared (0) on RESOUT.

PLL8_MODE

Bits	Name	Description
31:22	RESERVED_BITS31_22	RESERVED
21	PLL_VOTE_FSM_RESET	Resets PLL voting FSM. 0x0: De-asserts Reset to PLL voting FSM 0x1: Resets PLL voting FSM
20	PLL_VOTE_FSM_ENA	Enables PLL voting FSM. 0x0: Disabled 0x1: Enabled
19:14	PLL_BIAS_COUNT	Sets PLL bias count of PLL voting FSM.
13:8	PLL_LOCK_COUNT	Sets PLL lock time of PLL voting FSM.
7:5	RESERVED_BITS_7_5	RESERVED
4	PLL_REF_XO_SEL	Specify the reference XO to be used. 0x0: PXO (27MHz) 0x1: GND
3	PLL_PLLTEST	Set (1) this bit to enter the PLL test mode. Clear (0) this bit for the normal mode.
2	PLL_RESET_N	Low asserted reset for the digital logic in the PLL. This includes the MND counters and integer divider.
1	PLL_BYPASSNL	Clear (0) to bypass the PLL (PLLOUT is then identical to the input reference). Set (1) to use the PLL. Default is clear (0) at RESOUT (different from previous APQs)

PLL8_MODE (cont.)

Bits	Name	Description
0	PLL_OUTCTRL	Set (1) to activate the PLL's outputs (the analog circuitry is active - but the output is not). Set (1) will enable the following PLL's outputs: PLLOUT_LV_MAIN (if MAIN output enabled PLL8_CONFIG[23])PLLOUT_LV_BIST (If BIST output enabled PLL8_TEST_CTL[13]) PLLOUT_LV_AUX (If AUX output enabled PLL8_TEST_CTL[12]) Clear (0) to disable the PLL's output and save power. Clears (0) at RESOUT.

0x00903144 PLL8_L_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The following equation (fractional division ratio) is used to calculate the PLL8 (NT PLL) output frequency:

VCO = REF * [L+(M/N)] / (R * P)

Where:

- R represents the predivider of 2
- P represents the post divider

The value of the PLL8_L_VAL register is the given value of L for that equation.

PLL8_L_VAL

Bits	Name	Description
31:10	RESERVED_BITS31_10	UNUSED (This is the original assignment before CR154463.)
31	ICP_TST_EN	PLL_TEST_CTL(9) Charge pump test current control 0x0: Disable 0x1: Enable
27:26	NMOSC_FREQ_CTL	PLL_CONFIG_CTL(27:26) 0x0: Highest (2.8 GHz at TT / 1.05V /40C) 0x1: 1/2 highest 0x2: 1/3 highest 0x3: 1/4 highest

PLL8_L_VAL (cont.)

Bits	Name	Description
25:24	PFD_DZSEL	PLL_CONFIG_CTL(25:24) PFD reset pulse width adjustment 0x0: 1x delay 0x1: 2x delay 0x2: 3x delay 0x3: 4x delay
23	NMOSC_EN	PLL_CONFIG_CTL(23) Noise measurement oscillator control. 0x0: Disable 0x1: Enable
21:20	ICP_DIV	PLL_CONFIG_CTL(21:20) Charge pump bias mirror multiplication factor. 0x0: 1 0x1: 3/2 0x2: 7/4 0x3: 9/4
19:18	IREG_DIV	PLL_CONFIG_CTL(19:18) Regulator bias mirror multiplication factor. 0x0: 1 0x1: 7/5 0x2: 9/5 0x3: 11/5
17:16	CUSEL	PLL_CONFIG_CTL(17:16) VCO decoupling cap unit size. 0x0: 125 fF 0x1: 250 fF 0x2: 375 fF 0x3: 500 fF
15	REF_MODE	PLL_CONFIG_CTL(15) Reference circuit mode. 0x0: Bandgap mode (seed currents sourced from bandgap circuit and Nwell reference circuit active) 0x1: Supply independent mode (seed currents sourced from supply independent circuit amd Nwell reference pulled to VDDA)
14	PLLOUT_LV_TEST	PLL_TEST_CTL(14) PLLOUT_LV_TEST source selection 0x0: PLL output clock 0x1: Noise measurement oscillator

PLL8_L_VAL (cont.)

Bits	Name	Description
13:12	CFG_LOCKDET	PLL_CONFIG_CTL(13:12) Lock detector phase error threshold. 0x0: 2 pi /7 0x1: 2 pi /15 0x2: 2 pi /23 0x3: 2 pi /31
11	FORCE_ISEED	PLL_CONFIG_CTL(11) Seed current control. 0x0: Turn off seed currents when clock is detected 0x1: Keep seed currents on at all times
9:0	PLL_L	This register contains the 10-bit L value in the PLL0's fractional division ratio.

0x00903148 PLL8_M_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The value of the PLL8_M_VAL register is the given value of M for the fractional division ratio.

PLL8_M_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED
18:0	PLL_M	This register contains the 19-bit M value of the PLLn's numerator value in the fractional division ratio.

0x0090314C PLL8_N_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x1

The value of the PLL8_N_VAL register is the given value of N for the fractional division ratio.

PLL8_N_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED

PLL8_N_VAL (cont.)

Bits	Name	Description
18:0	PLL_N	This register contains the 19-bit N value of the PLLn's denominator value in the fractional division ratio.

0x00903150 PLL8_TEST_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The PLL8_TEST_CTL register is used to enable the TEST, BIST and AUX outputs of PLL8 (SR PLL). The field descriptions show the mapping from 45nm NT wrapper PLL8_TEST_CTL register to SR PLL inputs, PLL_TEST_CTL and PLL_CONFIG_CTL. Some bits of PLL_TEST_CTL and PLL_CONFIG_CTL come from PLL8_L_VAL (CR154463).

PLL8_TEST_CTL

Bits	Name	Description
31:19	RESERVED_BITS31_19	PLL8_TEST_CTL(31:30) : Not Used See PLL8_L_VAL(25:24) that maps to PLL_CONFIG_CTL(25:24) PLL8_TEST_CTL(29:28) : Not Used See PLL8_L_VAL(21:20) that maps to PLL_CONFIG_CTL(21:20) PLL8_TEST_CTL(27:26) : Not Used See PLL8_L_VAL(19:18) that maps to PLL_CONFIG_CTL(19:18) PLL8_TEST_CTL(25:24) : Not Used See PLL8_L_VAL(17:16) that maps to PLL_CONFIG_CTL(17:16) PLL8_TEST_CTL(23:22) : Not Used See PLL8_L_VAL(13:12) that maps to PLL_CONFIG_CTL(13:12) PLL8_TEST_CTL(21) : Not Used See PLL8_L_VAL(11) that maps to PLL_CONFIG_CTL(11) PLL8_TEST_CTL(20) : Not Used. See PLL8_L_VAL(31) that maps to PLL_TEST_CTL(9) PLL8_TEST_CTL(19) : Not Used
18:17	INTERNAL_BITS18_17	PLL8_TEST_CTL(18:17) : Not Used
16	INTERNAL_BIT16	PLL8_TEST_CTL(16) maps to PLL_CONFIG_CTL(5) Output clock polarity. 0x0: Do not invert output 0x1: Invert output

PLL8_TEST_CTL (cont.)

Bits	Name	Description
15	INTERNAL_BIT15	PLL8_TEST_CTL(15) maps to PLL_CONFIG_CTL(4) PLLOUT_LV_TEST enable 0x0: Disable 0x1: Enable
14	RESERVED_BIT14	PLL8_TEST_CTL(14) : Not used. See PLL8_L_VAL(14) that maps to PLL_TEST_CTL(14)
13	PLLOUT_BIST_ENABLE	PLL8_TEST_CTL(13) maps to PLL_CONFIG_CTL(2) PLLOUT_LV_BIST enable 0x0: Disable 0x1: Enable (must be enabled to use noise generator)
12	PLLOUT_AUX_ENABLE	PLL8_TEST_CTL(12) maps to PLL_CONFIG_CTL(1) PLLOUT_LV_AUX enable 0x0: Disable 0x1: Enable

PLL8_TEST_CTL (cont.)

Bits	Name	Description
11:0	INTERNAL_BIT11_0	PLL8_TEST_CTL(11) : Not Used PLL8_TEST_CTL(10) maps to PLL_TEST_CTL(8) Charge pump external bias control PLL8_TEST_CTL(9:8) maps to PLL_CONFIG_CTL(29:28) PFD force bits PLL8_TEST_CTL(9) = Force PFD up PLL8_TEST_CTL(8) = Force PFD down PLL8_TEST_CTL(7) maps to PLL_TEST_CTL(7) DTEST signal select PLL8_TEST_CTL(6) maps to PLL_TEST_CTL(6) ATEST amplifier bypass control PLL8_TEST_CTL(5:4) maps to PLL_TEST_CTL(5:4) ATEST1 signal select Force PLL filter voltage externally (set PLL_TEST_CTL(6) to 1) PLL8_TEST_CTL(3:2) maps to PLL_TEST_CTL(3:2) ATEST0 signal select PLL8_TEST_CTL(1) maps to PLL_TEST_CTL(1) ATEST1 Control PLL8_TEST_CTL(0) maps to PLL_TEST_CTL(0) ATEST0 Control 0x0: Disable 0x1: Enable 0x0: Normal operation_1 0x1: Force PFD UP -> 1 0x0: Normal operation_2 0x1: Force PFD DN -> 1 0x0: Select clock detect signal 0x1: Select feedback divider output signal 0x0: Do not bypass ATEST buffer amplifier 0x1: Bypass ATEST buffer amplifier 0x0: Observe Nwell reference (set PLL_TEST_CTL6 to 0) 0x1: Observe regulator output (set PLL_TEST_CTL6 to 0) 0x2: Observe PLL filter voltage (set PLL_TEST_CTL6 to 0) 0x3: Supply noise measurement mode

PLL8_TEST_CTL (cont.)

Bits	Name	Description
		0x0: Provide external bias current to charge pump (set PLL_TEST_CTL8 to 1) 0x1: Observe ICO test current (set PLL_TEST_CTL9 to 1) 0x2: Observe bandgap test current 0x3: VSSA 0x0: Disable ATEST1 0x1: Enable ATEST1 0x0: Disable ATEST0 0x1: Enable ATEST0

0x00903154 PLL8_CONFIG

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0084248B

The PLL8_CONFIG register is used for the PLL8 (NT PLL) to:

- Enable the main output
- Setup integer or fractional mode
- Setup the Post divider ratio
- Setup the Pre-divider ratio
- Select the appropriate VCO depending on the generated frequency

The field descriptions show the mapping from 45nm NT wrapper PLL8_CONFIG register to SR PLL input, PLL_CONFIG_CTL. Some bits of PLL_CONFIG_CTL come from PLL8_TEST_CTL and PLL8_L_VAL (CR154463).

PLL8_CONFIG

Bits	Name	Description
31:28	RESERVED_BITS31_28	PLL8_CONFIG(31:30) : Not Used See PLL8_L_VAL(27:26) that maps to PLL_CONFIG_CTL(27:26) PLL8_CONFIG(29) : Not Used See PLL8_L_VAL(23) that maps to PLL_CONFIG_CTL(23) PLL8_CONFIG(28) : Not Used See PLL8_L_VAL(15) that maps to PLL_CONFIG_CTL(15)

PLL8_CONFIG (cont.)

Bits	Name	Description
27	EARLY_OUT_ENA	PLL8_CONFIG(27) maps to PLL_CONFIG_CTL(3) PLLOUT_LV_EARLY enable 0x0: Disable 0x1: Enable
26	CLK33_OUT_SEL	Not Used
25	CLK33_OUT_ENA	Not Used
24	OUT_SEL	Not Used
23	MAIN_OUT_ENA	PLL8_CONFIG(23) maps to PLL_CONFIG_CTL(0) PLLOUT_LV_MAIN enable 0x0: Disable 0x1: Enable
22	MN_ACCUM_ENA	PLL8_CONFIG(22) maps to PLL_CONFIG_CTL(14) PLL fractional mode control 0x0: Disable 0x1: Enable
21:20	PLLOUT_DIVIDE	PLL8_CONFIG(21:20) maps to PLL_CONFIG_CTL(8:7) PLL Post-divider control 0x0: Divide by 1 (use this setting when sending reference clock to output) 0x1: Divide by 2 0x2: Divide by 4 0x3: Invalid
19	PRE_DIVIDE	PLL8_CONFIG(19) maps to PLL_CONFIG_CTL(6) PLL pre-divider control 0x0: Divide by 1 0x1: Divide by 2
18	INTERNAL_BIT18	Not Used
17:16	VCO	PLL8_CONFIG(17) maps to PLL_CONFIG_CTL(9) VCO Selection PLL8_CONFIG(16) : Not Used 0x0: Select 100 - 500 MHz VCO 0x1: Select 400 - 1400 MHz VCO
15	INTERNAL_BIT15	Not Used
14:0	INTERNAL_BITS14_0	Not Used

0x00903158 PLL8_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The PLL8_STATUS register is used to report the PLL state.

PLL8_STATUS

Bits	Name	Description
31:17	RESERVED_BITS31_17	RESERVED
16	PLL_ACTIVE_FLAG	pll_active_flag from PLL voting FSM. It indicates when FSM has enabled the PLL and PLL should be locked.
15:0	PLL_D	PLL8_STATUS(15:1) : Unused and shorted to VSSD PLL8_STATUS(0) : Clock detect

0x00903160 GPLL1_MODE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The GPLL1_MODE register configures and controls GPLL1. All register bits are cleared (0) on RESOUT.

GPLL1_MODE

Bits	Name	Description
31:22	RESERVED_BITS31_22	RESERVED
21	PLL_VOTE_FSM_RESET	Resets PLL voting FSM. 0x0: De-asserts Reset to PLL voting FSM 0x1: Resets PLL voting FSM
20	PLL_VOTE_FSM_ENA	Enables PLL voting FSM. 0x0: Disabled 0x1: Enabled
19:14	PLL_BIAS_COUNT	Sets PLL bias count of PLL voting FSM.
13:8	PLL_LOCK_COUNT	Sets PLL lock time of PLL voting FSM.
7:5	RESERVED_BITS_7_5	RESERVED
4	PLL_REF_XO_SEL	Specify the reference XO to be used. 0x0: PXO 0x1: MXO

GPLL1_MODE (cont.)

Bits	Name	Description
3	PLL_PLLTEST	Set(1) this bit to enter the PLL test mode. Clear (0) this bit for the normal mode.
2	PLL_RESET_N	Low asserted reset for the digital logic in the PLL. This includes the MND counters and integer divider.
1	PLL_BYPASSNL	Clear (0) to bypass the PLL (PLLOUT is then identical to the input reference). Set (1) to use the PLL. Default is clear (0) at RESOUT (different from previous APQs)
0	PLL_OUTCTRL	Set (1) to activate the PLL's outputs (the analog circuitry is active but the output is not). Set (1) will enable the following PLL's outputs: PLLOUT_LV_MAIN (if MAIN output enabled GPLL1_CONFIG[24]) PLLOUT_LV_BIST (If BIST output enabled GPLL1_TEST_CTL[13]) PLLOUT_LV_AUX (If AUX output enabled GPLL1_TEST_CTL[12]) Clear (0) to disable the PLL's output and save power. Clears (0) at RESOUT.

0x00903164 GPLL1_L_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The following equation (fractional division ratio) is used to calculate the GPLL1 (SR2 PLL) output frequency:

VCO = REF * [L+(M/N)] / (R * P)

Where:

- R represents the predivider of 2
- P represents the post divider.

The value of the GPLL1_L_VAL register is the given value of L for that equation.

GPLL1_L_VAL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED (this is the original assignment before CR154463)

GPLL1_L_VAL (cont.)

Bits	Name	Description
31	LFSR_DITHER_EN	PLL_CONFIG_CTL(31) 0x0: LFSR dither disabled 0x1: LFSR dither enabled (use this in conjunction with MASH11fracN mode)
30:29	LOCK_DET_CFG	PLL_CONFIG_CTL(30:29) Lock detection circuit configuration 0x0: Threshold = 2 pi / 7 0x1: Threshold = 2 pi / 15 0x2: Threshold = 2 pi / 23 0x3: Threshold = 2 pi / 31
28	FRACN_MODE_CTL	PLL_CONFIG_CTL(24) Frac-N mode control 0x0: MN- Accumulator FracN mode (legacy) 0x1: Mash11 FracN mode (Use PLL_N_val = 19'hFFFF in this mode for lowest inband dither power. Use PLL_CONFIG_CTL3:2 = 2'b0 in this mode for best quantization noise filtering)
27:26	OVER_VOLTAGE_CFG	PLL_CONFIG_CTL(27:26) Over voltage detect counter configuration 0x0: Detect at count = 0 0x1: Detect at count = 4 0x2: Detect at count = 8 0x3: Detect at count = 32
25	OVER_VOLTAGE_EN	PLL_CONFIG_CTL(25) 0x0: Over voltage detect counter is enabled 0x1: Over voltage detect counter is disabled
16:14	RESERVED_16_14	PLL_TEST_CTL (31:29) RESERVED
13	VCO_DCAPS_EN	PLL_CONFIG_CTL(13) Disable internally programmed VCO decoupling caps 0x0: Automatically controlled programmable VCO dcaps 0x1: Disable programmable VCO dcaps
11	REG_BIAS_CFG_B1	PLL_CONFIG_CTL(11) Bit1 of regulator stage 2 bias current setting
10	ADZ_CFG_B0	PLL_CONFIG_CTL(6) Bit0 of anti dead zone programmable input /filter phase offset control
8	VREG_ATEST_CTL	PLL_TEST_CTL (0) 0x0: Disconnect VREG to test op amp input 0x1: Connect VREG to test op amp input - observed on ATEST0
7:0	PLL_L	This register contains the 10-bit L value in the PLL's fractional division ratio.

0x00903168 GPLL1_M_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The value of the GPLL1_M_VAL register is the given value of M for the fractional division ratio.

GPLL1_M_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED (This is the original assignment before CR154463.)
31:30	NMOSC_FREQ_CTL	PLL_CONFIG_CTL(27:26) for LPA PLL - Pll4 0x0: Highest (2.8 GHz at TT / 1.05V /40C) 0x1: 1/2 highest 0x2: 1/3 highest 0x3: 1/4 highest
29	NMOSC_EN	PLL_CONFIG_CTL(23) for LPA PLL - Pll4 Noise measurement oscillator control 0x0: Disable 0x1: Enable
28	REF_MODE	PLL_CONFIG_CTL(15) for LPA PLL - Pll4 Reference circuit mode 0x0: Bandgap mode (seed currents sourced from bandgap circuit and Nwell reference circuit active) 0x1: Supply independent mode (seed currents sourced from supply independent circuit amd Nwell reference pulled to VDDA)
27	LVEARLY_EN	PLL_CONFIG_CTL(3) for LPA PLL - Pll4 PLLOUT_LV_EARLY enable 0x0: Disable 0x1: Enable
26	PLLOUT_LV_TEST	PLL_TEST_CTL(14) for LPA PLL - Pll4 PLLOUT_LV_TEST source selection 0x0: PLL output clock 0x1: Noise measurement oscillator
25	DTEST_SEL	PLL_TEST_CTL(7) for LPA PLL - Pll4 DTEST signal select 0x0: Select clock detect signal 0x1: Select feedback divider output signal
24	BYP_TESTAMP	PLL_TEST_CTL(6) for LPA PLL - Pll4 ATEST amplifier bypass control 0x0: Do not bypass ATEST buffer amplifier 0x1: Bypass ATEST buffer amplifier

GPLL1_M_VAL (cont.)

Bits	Name	Description
18:0	PLL_M	This register contains the 19-bit M value of the PLLn's numerator value in the fractional division ratio.

0x0090316C GPLL1_N_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x01

The value of the GPLL1_N_VAL register is the given value of N for the fractional division ratio.

GPLL1_N_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED (This is the original assignment before CR154463.)
31:30	PFD_DZSEL	PLL_CONFIG_CTL(25:24) for LPA PLL - Pll4 PFD reset pulse width adjustment 0x0: 1x delay 0x1: 2x delay 0x2: 3x delay 0x3: 4x delay
29:28	ICP_DIV	PLL_CONFIG_CTL(21:20) for LPA PLL - Pll4 Charge pump bias mirror multiplication factor. 0x0: 1 0x1: 3/2 0x2: 7/4 0x3: 9/4
27:26	IREG_DIV	PLL_CONFIG_CTL(19:18) for LPA PLL - Pll4 Regulator bias mirror multiplication factor. 0x0: 1 0x1: 7/5 0x2: 9/5 0x3: 11/5
25:24	CUSEL	PLL_CONFIG_CTL(17:16) for LPA PLL - Pll4 VCO decoupling cap unit size. 0x0: 125 fF 0x1: 250 fF 0x2: 375 fF 0x3: 500 fF

GPLL1_N_VAL (cont.)

Bits	Name	Description
23:22	CFG_LOCKDET	PLL_CONFIG_CTL(13:12) for LPA PLL - Pll4 Lock detector phase error threshold. 0x0: 2 pi /7 0x1: 2 pi /15 0x2: 2 pi /23 0x3: 2 pi /31
21	FORCE_ISEED	PLL_CONFIG_CTL(11) for LPA PLL - Pll4 Seed current control 0x0: Turn off seed currents when clock is detected 0x1: Keep seed currents on at all times
20	ICP_TST_EN	PLL_TEST_CTL(9) for LPA PLL - Pll4 Charge pump test current control 0x0: Disable 0x1: Enable
18:0	PLL_N	This register contains the 19-bit N value of the PLLn's denominator value in the fractional division ratio.

0x00903170 GPLL1_TEST_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The GPLL1_TEST_CTL register is used to enable the TEST, BIST and AUX outputs of this PLL (SR2 PLL). The field descriptions show the mapping from 45nm NT wrapper GPLL1_TEST_CTL register to SR2 PLL inputs, PLL_TEST_CTL. Some bits of PLL_TEST_CTL and PLL_CONFIG_CTL come from GPLL1_L_VAL (CR154463).

GPLL1_TEST_CTL

Bits	Name	Description
31:29	RESERVED_BITS31_29	MMCC_PLL2_TEST_CTL(31:29) : Not Used See MMCC_PLL2_L_VAL(16:14) that maps to PLL_TEST_CTL(31:29)
28:25	INTERNAL_BITS28_25	Not Used
24	INTERNAL_BIT24	MMCC_PLL2_TEST_CTL(24) maps to PLL_TEST_CTL(11) 0x0: Output invert disabled 0x1: Output invert enabled
23:22	INTERNAL_BITS23_22	MMCC_PLL2_TEST_CTL(23) : Not Used MMCC_PLL2_TEST_CTL(22) maps to PLL_TEST_CTL(22) See MMCC_PLL2_TEST_CTL(22:20) together below.

GPLL1_TEST_CTL (cont.)

Bits	Name	Description
21	INTERNAL_BIT21	MMCC_PLL2_TEST_CTL(21) maps to PLL_TEST_CTL(21) See MMCC_PLL2_TEST_CTL(22:20) together below.
20:19	INTERNAL_BITS20_19	MMCC_PLL2_TEST_CTL(20:19) maps to PLL_TEST_CTL(20:19) MMCC_PLL2_TEST_CTL(22:20) Select current sink in noise generator resistor dac MMCC_PLL2_TEST_CTL(19) Enable for supply noise generator circuit. 0x0: Zero 0x1: Max 2 mA 0x2: Max 4 mA 0x3: Max 6 mA 0x4: Max 8 mA 0x5: Max 10 mA 0x6: Max 12 mA 0x7: Max 14 mA 0x0: Disable 0x1: Enable
18	INTERNAL_BIT18	MMCC_PLL2_TEST_CTL(18) maps to PLL_TEST_CTL(18) See MMCC_PLL2_TEST_CTL(18:17) together below.
17:16	INTERNAL_BITS17_16	MMCC_PLL2_TEST_CTL(17:16) maps to PLL_TEST_CTL(17:16) MMCC_PLL2_TEST_CTL(18:17) MMCC_PLL2_TEST_CTL(16) 0x0: Disable analog supply measurement oscillator 0x1: Enable row0 of oscillator drivers (slowest frequency of oscillation) 0x2: Enable row0, row1 of oscillator drivers (mid frequency of oscillator) 0x3: Enable row0, row1, row2, row3 of oscillator drivers (highest frequency of oscillator) 0x0: Connect PLL clock path to pllout_lv_test output 0x1: Connect analog supply measurement oscillator path to pllout_lv_test output
15	INTERNAL_BIT15	MMCC_PLL2_TEST_CTL(15) maps to PLL_TEST_CTL(13) When set to â□□1â□□ connect FILT_INT to test op amp input - observed on ATEST0
14	INTERNAL_BIT14	MMCC_PLL2_TEST_CTL(14) maps to PLL_TEST_CTL(10) 0x0: Disable PLLOUT_LV_TEST 0x1: Enable PLLOUT_LV_TEST
13	PLLOUT_BIST_ENABLE	MMCC_PLL2_TEST_CTL(13) maps to PLL_TEST_CTL(8) 0x0: Disable PLLOUT_LV_BIST 0x1: Enable PLLOUT_LV_BIST

GPLL1_TEST_CTL (cont.)

Bits	Name	Description
12	PLLOUT_AUX_ENABLE	MMCC_PLL2_TEST_CTL(12) maps to PLL_TEST_CTL(9) 0x0: Disable PLLOUT_LV_AUX 0x1: Enable PLLOUT_LV_AUX
11	INTERNAL_BIT11	Not Used
10	INTERNAL_BIT10	Not Used
9:8	RESERVED_BITS9_8	MMCC_PLL2_TEST_CTL(9) : Not Used MMCC_PLL2_TEST_CTL(8) : Not Used See MMCC_PLL2_L_VAL(8) that maps to PLL_TEST_CTL(0)
7	INTERNAL_BIT7	MMCC_PLL2_TEST_CTL(7) maps to PLL_TEST_CTL(7) 0x0: Disable PLLOUT_HV 0x1: Enable PLLOUT_HV
6	INTERNAL_BIT6	MMCC_PLL2_TEST_CTL(6) maps to PLL_TEST_CTL(6) Current flows from VDDA (should terminate to VSSA on board) 0x0: Open test switch 0x1: Enable vco current div-8 output to ATEST0 pin
5	INTERNAL_BIT5	MMCC_PLL2_TEST_CTL(5) maps to PLL_TEST_CTL(5) Current flows from AVDD (should terminate to AVSS on board) 0x0: Open test switch 0x1: Bypass ico current with external input from ATEST1 pin to bias the cp
4:1	INTERNAL_BITS4_1	MMCC_PLL2_TEST_CTL(4:1) maps to PLL_TEST_CTL(4:1) MMCC_PLL2_TEST_CTL(4) Current flows from VDDA (should terminate to VSSA on board) MMCC_PLL2_TEST_CTL(3) MMCC_PLL2_TEST_CTL(2) When set to â□□1â□□ enable switch to force external voltages from ATEST0 MMCC_PLL2_TEST_CTL(1) When set to â□□1â□□ connect VINT to test op amp input - observed on ATEST0 MMCC_PLL2_TEST_CTL(0) When set to â□□1â□□ connect VREG to test op amp input - observed on ATEST0 0x0: Open test switch 0x1: Enable bias circuit current to ATEST1 pin 0x0: Filter test op amp disabled 0x1: Enable the filter test opamp

GPLL1_TEST_CTL (cont.)

Bits	Name	Description
0	INTERNAL_BIT0	MMCC_PLL2_TEST_CTL(0) maps to PLL_TEST_CTL(12) Mux selectors for DTEST 0x0: Select C_MVAL (carry input for M-val: +1 dither) 0x1: Select NOCLKB

0x00903174 GPLL1_CONFIG

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00010401

Some bits of the PLLn_CONFIG register are used for test purposes. The field descriptions show the mapping from 45nm GP3 wrapper GPLL1_CONFIG register to SR2 PLL input, PLL_CONFIG_CTL. Some bits of PLL_CONFIG_CTL come from GPLL1_L_VAL.

GPLL1_CONFIG

Bits	Name	Description
31:25	RESERVED_BITS31_25	MMCC_PLL2_CONFIG(31:25) : Not Used See MMCC_PLL2_L_VAL(31:25) that maps to PLL_CONFIG_CTL(31:25).
24	INTERNAL_BIT24	MMCC_PLL2_CONFIG(24) maps to PLL_CONFIG_CTL(21) 0x0: Disable PLLOUT_LV_MAIN 0x1: Enable PLLOUT_LV_MAIN
23:22	INTERNALBITS23_22	MMCC_PLL2_CONFIG(23) maps to PLL_CONFIG_CTL(18) Filter timing configuration MMCC_PLL2_CONFIG(22) maps to PLL_CONFIG_CTL(22) 0x0: Filter timing driven by early reference clock 0x1: Filter timing driven by the edge that arrives first - reference / divider output 0x0: Disable PLLOUT_LV_EARLY 0x1: Enable PLLOUT_LV_EARLY
21:20	INTERNALBITS21_20	MMCC_PLL2_CONFIG(21) maps to PLL_CONFIG_CTL(17) Filter timing configuration Phase offset magnitude is controlled using ADZ config bits. MMCC_PLL2_CONFIG(20) maps to PLL_CONFIG_CTL(20) MSB (Bit1) for output clock post divide ratio. (MMCC_PLL2_CONFIG(20) and MMCC_PLL2_CONFIG(16) are used together) 0x0: Conventional sample reset filter - double sampling disabled 0x1: Enable double sampled filter on opposite reference clock edge, enable filter phase offset circuit.

GPLL1_CONFIG (cont.)

Bits	Name	Description
19:18	PLLOUT_HV_DIVIDE	MMCC_PLL2_CONFIG(19:18) maps to PLL_CONFIG_CTL(16:15) Regulator stage-1 output voltage setting. 0x0: Vfilt *_1 (1.4 / 1) 0x1: Vfilt *_2 (1.35 / 1) 0x2: Vfilt *_3 (1.3 / 1) 0x3: Vfilt *_4 (1.25 / 1)
17	INTERNAL_BIT17	MMCC_PLL2_CONFIG(17) maps to PLL_CONFIG_CTL(28) MN accumulator 0x0: Disable 0x1: Enable
16	POST_DIVIDE	MMCC_PLL2_CONFIG(16) maps to PLL_CONFIG_CTL(19) LSB (Bit0) for output clock post divide ratio MMCC_PLL2_CONFIG(20) : MMCC_PLL2_CONFIG(16) = PLL_CONFIG_CTL(20:19) 0x0: 1 (Use this setting when bypassing reference clock to PLL output) 0x1: 2 0x2: 4 0x3: Unused, Reserved
15	PRE_DIVIDE	MMCC_PLL2_CONFIG(15) maps to PLL_CONFIG_CTL(23) CLK_REF pre-divide ratio 0x0: 1 0x1: 2
14	PLLOUT_HV_ENABLE	MMCC_PLL2_CONFIG(14) maps to PLL_CONFIG_CTL(14) 0x0: Disable iseed gating 0x1: Enables no_clock signal to gate iseed current in the charge pump
13	RESERVED_BIT13	MMCC_PLL2_CONFIG(13) : Not Used See MMCC_PLL2_L_VAL(13) that maps to PLL_CONFIG_CTL(13).
12	INTERNAL_BIT12	MMCC_PLL2_CONFIG(12) maps to PLL_CONFIG_CTL(12) Enable / Bypass for stage 1 regulator 0x0: Enable 0x1: Bypass
11	RESERVED_BIT11	MMCC_PLL2_CONFIG(11) : Not Used See MMCC_PLL2_L_VAL(11) that maps to PLL_CONFIG_CTL(11). (MMCC_PLL2_L_VAL(11) and MMCC_PLL2_CONFIG(10) are used together)

GPLL1_CONFIG (cont.)

Bits	Name	Description
10:9	INTERNAL_BITS10_9	MMCC_PLL2_CONFIG(10:9) maps to PLL_CONFIG_CTL(10:9) MMCC_PLL2_CONFIG(10) is LSB (Bit0) of regulator stage 2 Bias current setting MMCC_PLL2_L_VAL(11) : MMCC_PLL2_CONFIG(10) maps to PLL_CONFIG_CTL(11:10) (MMCC_PLL2_CONFIG(9:8) are used together) 0x0: 1x Ivco / L 0x1: 2x Ivco / L 0x2: 3x Ivco / L 0x3: 4x Ivco / L
8:7	VCO	MMCC_PLL2_CONFIG(8:7) maps to PLL_CONFIG_CTL(8:7) MMCC_PLL2_CONFIG(9:8) maps to PLL_CONFIG_CTL(9:8) Reference voltage setting for over voltage detection on stage 2 regulator output MMCC_PLL2_CONFIG(7) MMCC_PLL2_CONFIG(7) is MSB (bit1) of Anti dead zone programmable input / Filter phase offset control and LSB (bit0) is MMCC_PLL2_L_VAL(10). MMCC_PLL2_CONFIG(7) : MMCC_PLL2_L_VAL(10) maps to PLL_CONFIG_CTL(7:6) 0x0: Power down over voltage detection 0x1: 1.15 / 1.8 0x2: 1.2 / 1.8 0x3: 1.25 / 1.8 0x0: 1 delay elements / Icpoffset = 0 (Tcpoffset = 0, Filter offset disabled) 0x1: 2 delay elements / Icpoffset = 0.6uA @ Fref = 20MHz, Fo = 1GHz (Tcpoffset = 250 ps) 0x2: 3 delay elements / Icpoffset = 1.2uA @ Fref = 20MHz, Fo = 1GHz (Tcpoffset = 500 ps) 0x3: 4 delay elements / Icpoffset = 4.2uA @ Fref = 20MHz, Fo = 1GHz (Tcpoffset = 1750 ps)
6	RESERVED_BIT6	MMCC_PLL2_CONFIG(6) : Not Used See MMCC_PLL2_L_VAL(10) that maps to PLL_CONFIG_CTL(6). (MMCC_PLL2_CONFIG(7) and MMCC_PLL2_L_VAL(10) are used together)

GPLL1_CONFIG (cont.)

Bits	Name	Description
5:2	INTERNAL_BITS5_2	MMCC_PLL2_CONFIG(5:4) maps to PLL_CONFIG_CTL(5:4) Iseed control for Charge pump MMCC_PLL2_CONFIG(3:2) maps to PLL_CONFIG_CTL(1:0) Setting for delay in reference path. Delta t (nominal values) 0x0: 0.5x Iseed 0x1: 1x Iseed 0x2: 2x Iseed 0x3: 4x Iseed 0x0: 200 ps 0x1: 400 ps 0x2: 800 ps 0x3: 1200 ps
1:0	INTERNAL_BITS1_0	MMCC_PLL2_CONFIG(1:0) maps to PLL_CONFIG_CTL(3:2) Current mirror for charge pump current fixed divider ratio Iout / Ivco 0x0: 1 / L (may need to use this setting at low end of VCO range) 0x1: 2 / L 0x2: 3 / L 0x3: 5 / L

0x00903178

GPLL1_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The GPLL1_STATUS register is used for test purposes to report PLL state.

GPLL1_STATUS

Bits	Name	Description
31:16	RESERVED_BITS31_16	RESERVED
15:0	PLL_AUTOCAL_VAL	MMCC_PLL2_STATUS(15:6) : Unused, driven low (vssd domain) MMCC_PLL2_STATUS(5:2) : Over voltage counter status MMCC_PLL2_STATUS(1) : Over voltage detect flag MMCC_PLL2_STATUS(0) : Negated of no_clock (if clock is detected, output is high)

0x00903180 EBI1_PLL_MODE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The EBI1_PLL_MODE register configures and controls EBI1_PLL (EBI1_PLL - GP3 PLL). All register bits are cleared (0) on RESOUT.

EBI1_PLL_MODE

Bits	Name	Description
31:5	RESERVED_BITS31_5	RESERVED
4	PLL_REF_XO_SEL	Specify the reference XO to be used 0x0: PXO (27MHz) 0x1: GND
3	PLL_PLLTEST	Set(1) this bit to enter the PLL test mode. Clear (0) this bit for the normal mode.
2	PLL_RESET_N	Low asserted reset for the digital logic in the PLL. This includes the MND counters and integer divider.
1	PLL_BYPASSNL	Clear (0) to bypass the PLL (PLLOUT is then identical to the input reference). Set (1) to use the PLL. Default is clear (0) at RESOUT (different from previous APQs)
0	PLL_OUTCTRL	Set (1) to activate the PLL's outputs (the analog circuitry is active but the output is not). Set (1) will enable the following PLL's outputs: PLLOUT_LV_MAIN (if MAIN output enabled EBI1_PLL_CONFIG[24]) PLLOUT_LV_BIST (If BIST output enabled EBI1_PLL_TEST_CTL[13]) PLLOUT_LV_AUX (If AUX output enabled EBI1_PLL_TEST_CTL[12]) Clear (0) to disable the PLL's output and save power. Clears (0) at RESOUT.

0x00903184 EBI1_PLL_L_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The following equation (fractional division ratio) is used to calculate the EBI1_PLL (GP3 PLL) output frequency:

VCO = REF * [L+(M/N)] / (R * P)

Where:

- R represents the predivider of 2
- P represents the post divider

The value of the EBI1_PLL_L_VAL register is the given value of L for that equation.

EBI1_PLL_L_VAL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED (This is the original assignment before CR154463.)
31	LFSR_DITHER_EN	PLL_CONFIG_CTL(31) 0x0: LFSR dither disabled 0x1: LFSR dither enabled (use this in conjunction with MASH11fracN mode)
30:29	LOCK_DET_CFG	PLL_CONFIG_CTL(30:29) Lock detection circuit configuration 0x0: Threshold = 2 pi / 7 0x1: Threshold = 2 pi / 15 0x2: Threshold = 2 pi / 23 0x3: Threshold = 2 pi / 31
28	FRACN_MODE_CTL	PLL_CONFIG_CTL(24) Frac-N mode control 0x0: MN- Accumulator FracN mode (legacy) 0x1: Mash11 FracN mode (Use PLL_N_val = 19'hFFFF in this mode for lowest inband dither power. Use PLL_CONFIG_CTL3:2 = 2'b0 in this mode for best quantization noise filtering)
27:26	OVER_VOLTAGE_CFG	PLL_CONFIG_CTL(27:26) Over voltage detect counter configuration 0x0: Detect at count = 0 0x1: Detect at count = 4 0x2: Detect at count = 8 0x3: Detect at count = 32

EBI1_PLL_L_VAL (cont.)

Bits	Name	Description
25	OVER_VOLTAGE_EN	PLL_CONFIG_CTL(25) 0x0: Over voltage detect counter is enabled 0x1: Over voltage detect counter is disabled
16:14	RESERVED_16_14	PLL_TEST_CTL (31:29) RESERVED
13	VCO_DCAPS_EN	PLL_CONFIG_CTL(13) Disable internally programmed VCO decoupling caps 0x0: Automatically controlled programmable VCO dcaps 0x1: Disable programmable VCO dcaps
11	REG_BIAS_CFG_B1	PLL_CONFIG_CTL(11) Bit1 of regulator stage 2 bias current setting
10	ADZ_CFG_B0	PLL_CONFIG_CTL(6) Bit0 of anti dead zone programmable input /filter phase offset control
8	VREG_ATEST_CTL	PLL_TEST_CTL (0) 0x0: Disconnect VREG to test op amp input 0x1: Connect VREG to test op amp input - observed on ATEST0
7:0	PLL_L	This register contains the 10-bit L value in the PLL's fractional division ratio.

0x00903188 EBI1_PLL_M_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The value of the EBI1_PLL_M_VAL register is the given value of M for the fractional division ratio.

EBI1_PLL_M_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED
18:0	PLL_M	This register contains the 19-bit M value of the PLLn's numerator value in the fractional division ratio.

0x0090318C EBI1_PLL_N_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x01

The value of the EBI1_PLL_N_VAL register is the given value of N for the fractional division ratio.

EBI1_PLL_N_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED
18:0	PLL_N	This register contains the 19-bit N value of the PLLn's denominator value in the fractional division ratio.

0x00903190 EBI1_PLL_TEST_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The EBI1_PLL_TEST_CTL register is used to enable the TEST, BIST and AUX outputs of PLL11 (SR2 PLL). The field descriptions show the mapping from 45nm NT wrapper EBI1_PLL_TEST_CTL register to SR2 PLL inputs, PLL_TEST_CTL. Some bits of PLL_TEST_CTL and PLL_CONFIG_CTL come from EBI1_PLL_L_VAL (CR154463).

EBI1_PLL_TEST_CTL

Bits	Name	Description
31:29	RESERVED_BITS31_29	EBI1_PLL_TEST_CTL(31:29) : Not Used See EBI1_PLL_L_VAL(16:14) that maps to PLL_TEST_CTL(31:29)
28:25	INTERNAL_BITS28_25	Not Used
24	INTERNAL_BIT24	EBI1_PLL_TEST_CTL(24) maps to PLL_TEST_CTL(11) 0x0: Output invert disabled 0x1: Output invert enabled
23:22	INTERNAL_BITS23_22	EBI1_PLL_TEST_CTL(23) : Not Used EBI1_PLL_TEST_CTL(22) maps to PLL_TEST_CTL(22) See EBI1_PLL_TEST_CTL(22:20) together below.
21	INTERNAL_BIT21	EBI1_PLL_TEST_CTL(21) maps to PLL_TEST_CTL(21) See EBI1_PLL_TEST_CTL(22:20) together below.

EBI1_PLL_TEST_CTL (cont.)

Bits	Name	Description
20:19	INTERNAL_BITS20_19	EBI1_PLL_TEST_CTL(20:19) maps to PLL_TEST_CTL(20:19) EBI1_PLL_TEST_CTL(22:20) Select current sink in noise generator resistor dac, EBI1_PLL_TEST_CTL(19) Enable for supply noise generator circuit 0x0: Zero 0x1: Max 2 mA 0x2: Max 4 mA 0x3: Max 6 mA 0x4: Max 8 mA 0x5: Max 10 mA 0x6: Max 12 mA 0x7: Max 14 mA 0x0: Disable 0x1: Enable
18	INTERNAL_BIT18	EBI1_PLL_TEST_CTL(18) maps to PLL_TEST_CTL(18) See EBI1_PLL_TEST_CTL(18:17) together below.
17:16	INTERNAL_BITS17_16	EBI1_PLL_TEST_CTL(17:16) maps to PLL_TEST_CTL(17:16) EBI1_PLL_TEST_CTL(18:17) EBI1_PLL_TEST_CTL(16) 0x0: Disable analog supply measurement oscillator 0x1: Enable row0 of oscillator drivers (slowest frequency of oscillation) 0x2: Enable row0, row1 of oscillator drivers (mid frequency of oscillator) 0x3: Enable row0, row1, row2, row3 of oscillator drivers (highest frequency of oscillator) 0x0: Connect PLL clock path to pllout_lv_test output 0x1: Connect analog supply measurement oscillator path to pllout_lv_test output
15	INTERNAL_BIT15	EBI1_PLL_TEST_CTL(15) maps to PLL_TEST_CTL(13) When set to â□□1â□□ connect FILT_INT to test op amp input - observed on ATEST0
14	INTERNAL_BIT14	EBI1_PLL_TEST_CTL(14) maps to PLL_TEST_CTL(10) 0x0: Disable PLLOUT_LV_TEST 0x1: Enable PLLOUT_LV_TEST
13	PLLOUT_BIST_ENABLE	EBI1_PLL_TEST_CTL(13) maps to PLL_TEST_CTL(8) 0x0: Disable PLLOUT_LV_BIST 0x1: Enable PLLOUT_LV_BIST
12	PLLOUT_AUX_ENABLE	EBI1_PLL_TEST_CTL(12) maps to PLL_TEST_CTL(9) 0x0: Disable PLLOUT_LV_AUX 0x1: Enable PLLOUT_LV_AUX

EBI1_PLL_TEST_CTL (cont.)

Bits	Name	Description
11	INTERNAL_BIT11	Not Used
10	INTERNAL_BIT10	Not Used
9:8	RESERVED_BITS9_8	EBI1_PLL_TEST_CTL(9) : Not Used EBI1_PLL_TEST_CTL(8) : Not Used See EBI1_PLL_L_VAL(8) that maps to PLL_TEST_CTL(0)
7	INTERNAL_BIT7	EBI1_PLL_TEST_CTL(7) maps to PLL_TEST_CTL(7) 0x0: Disable PLLOUT_HV 0x1: Enable PLLOUT_HV
6	INTERNAL_BIT6	EBI1_PLL_TEST_CTL(6) maps to PLL_TEST_CTL(6) Current flows from VDDA (should terminate to VSSA on board) 0x0: Open test switch 0x1: Enable vco current div-8 output to ATEST0 pin
5	INTERNAL_BIT5	EBI1_PLL_TEST_CTL(5) maps to PLL_TEST_CTL(5) Current flows from AVDD (should terminate to AVSS on board) 0x0: Open test switch 0x1: Bypass ico current with external input from ATEST1 pin to bias the cp
4:1	INTERNAL_BITS4_1	EBI1_PLL_TEST_CTL(4:1) maps to PLL_TEST_CTL(4:1) EBI1_PLL_TEST_CTL(4) Current flows from VDDA (should terminate to VSSA on board) EBI1_PLL_TEST_CTL(3) EBI1_PLL_TEST_CTL(2) When set to â□□1â□□ enable switch to force external voltages from ATEST0 EBI1_PLL_TEST_CTL(1) When set to â□□1â□□ connect VINT to test op amp input - observed on ATEST0 EBI1_PLL_TEST_CTL(0) When set to â□□1â□□ connect VREG to test op amp input - observed on ATEST0 0x0: Open test switch 0x1: Enable bias circuit current to ATEST1 pin 0x0: Filter test op amp disabled 0x1: Enable the filter test opamp
0	INTERNAL_BIT0	EBI1_PLL_TEST_CTL(0) maps to PLL_TEST_CTL(12) Mux selectors for DTEST 0x0: Select C_MVAL (carry input for M-val: +1 dither) 0x1: Select NOCLKB

0x00903194 EBI1_PLL_CONFIG

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00010401

Some bits of the EBI1_PLL_CONFIG register are used for test purposes. The field descriptions show the mapping from 45nm GP3 wrapper EBI1_PLL_CONFIG register to SR2 PLL input, PLL_CONFIG_CTL. Some bits of PLL_CONFIG_CTL come from EBI1_PLL_L_VAL (CR154463).

EBI1_PLL_CONFIG

Bits	Name	Description
31:25	RESERVED_BITS31_25	EBI1_PLL_CONFIG(31:25) : Not Used See EBI1_PLL_L_VAL(31:25) that maps to PLL_CONFIG_CTL(31:25).
24	INTERNAL_BIT24	EBI1_PLL_CONFIG(24) maps to PLL_CONFIG_CTL(21) 0x0: Disable PLLOUT_LV_MAIN 0x1: Enable PLLOUT_LV_MAIN
23:22	INTERNALBITS23_22	EBI1_PLL_CONFIG(23) maps to PLL_CONFIG_CTL(18) Filter timing configuration EBI1_PLL_CONFIG(22) maps to PLL_CONFIG_CTL(22) 0x0: Filter timing driven by early reference clock 0x1: Filter timing driven by the edge that arrives first - reference / divider output 0x0: Disable PLLOUT_LV_EARLY 0x1: Enable PLLOUT_LV_EARLY
21:20	INTERNALBITS21_20	EBI1_PLL_CONFIG(21) maps to PLL_CONFIG_CTL(17) Filter timing configuration EBI1_PLL_CONFIG(20) maps to PLL_CONFIG_CTL(20) MSB (Bit1) for output clock post divide ratio. (EBI1_PLL_CONFIG(20) and EBI1_PLL_CONFIG(16) are used together) 0x0: Conventional sample reset filter - double sampling disabled 0x1: Enable double sampled filter on opposite reference clock edge, enable filter phase offset circuit. Phase offset magnitude is controlled using ADZ config bits
19:18	PLLOUT_HV_DIVIDE	EBI1_PLL_CONFIG(19:18) maps to PLL_CONFIG_CTL(16:15) Regulator stage-1 output voltage setting 0x0: Vfilt *_1 (1.4 / 1) 0x1: Vfilt *_2 (1.35 / 1) 0x2: Vfilt *_3 (1.3 / 1) 0x3: Vfilt *_4 (1.25 / 1)

EBI1_PLL_CONFIG (cont.)

Bits	Name	Description
17	INTERNAL_BIT17	EBI1_PLL_CONFIG(17) maps to PLL_CONFIG_CTL(28) MN accumulator 0x0: Disable 0x1: Enable
16	POST_DIVIDE	EBI1_PLL_CONFIG(16) maps to PLL_CONFIG_CTL(19) LSB (Bit0) for output clock post divide ratio EBI1_PLL_CONFIG(20) : EBI1_PLL_CONFIG(16) maps to PLL_CONFIG_CTL(20:19) 0x0: 1 (Use this setting when bypassing reference clock to PLL output) 0x1: 2 0x2: 4 0x3: Unused, Reserved
15	PRE_DIVIDE	EBI1_PLL_CONFIG(15) maps to PLL_CONFIG_CTL(23) CLK_REF pre-divide ratio 0x0: 1 0x1: 2
14	PLLOUT_HV_ENABLE	EBI1_PLL_CONFIG(14) maps to PLL_CONFIG_CTL(14) 0x0: Disable iseed gating 0x1: Enables no_clock signal to gate iseed current in the charge pump
13	RESERVED_BIT13	EBI1_PLL_CONFIG(13) : Not Used See EBI1_PLL_L_VAL(13) that maps to PLL_CONFIG_CTL(13).
12	INTERNAL_BIT12	EBI1_PLL_CONFIG(12) maps to PLL_CONFIG_CTL(12) Enable / Bypass for stage 1 regulator 0x0: Enable 0x1: Bypass
11	RESERVED_BIT11	EBI1_PLL_CONFIG(11) : Not Used See EBI1_PLL_L_VAL(11) that maps to PLL_CONFIG_CTL(11). (EBI1_PLL_L_VAL(11) and EBI1_PLL_CONFIG(10) are used together)
10:9	INTERNAL_BITS10_9	EBI1_PLL_CONFIG(10:9) maps to PLL_CONFIG_CTL(10:9) EBI1_PLL_CONFIG(10) is LSB (Bit0) of regulator stage 2 Bias current setting EBI1_PLL_L_VAL(11) : EBI1_PLL_CONFIG(10) maps to PLL_CONFIG_CTL(11:10) (EBI1_PLL_CONFIG(9:8) are used together) 0x0: 1x Ivco / L 0x1: 2x Ivco / L 0x2: 3x Ivco / L 0x3: 4x Ivco / L

EBI1_PLL_CONFIG (cont.)

Bits	Name	Description
8:7	VCO	EBI1_PLL_CONFIG(8:7) maps to PLL_CONFIG_CTL(8:7) EBI1_PLL_CONFIG(9:8) maps to PLL_CONFIG_CTL(9:8) Reference voltage setting for over voltage detection on stage 2 regulator output EBI1_PLL_CONFIG(7) EBI1_PLL_CONFIG(7) is MSB (bit1) of Anti dead zone programmable input / Filter phase offset control and LSB (bit0) is EBI1_PLL_L_VAL(10). EBI1_PLL_CONFIG(7) : EBI1_PLL_L_VAL(10) maps to PLL_CONFIG_CTL(7:6) 0x0: Power down over voltage detection 0x1: 1.15 / 1.8 0x2: 1.2 / 1.8 0x3: 1.25 / 1.8 0x0: 1 delay elements / Icpoffset = 0 (Tcpoffset = 0, Filter offset disabled) 0x1: 2 delay elements / Icpoffset = 0.6uA @ Fref = 20MHz, Fo = 1GHz (Tcpoffset = 250 ps) 0x2: 3 delay elements / Icpoffset = 1.2uA @ Fref = 20MHz, Fo = 1GHz (Tcpoffset = 500 ps) 0x3: 4 delay elements / Icpoffset = 4.2uA @ Fref = 20MHz, Fo = 1GHz (Tcpoffset = 1750 ps)
6	RESERVED_BIT6	EBI1_PLL_CONFIG(6) : Not Used See EBI1_PLL_L_VAL(10) that maps to PLL_CONFIG_CTL(6). (EBI1_PLL_CONFIG(7) and EBI1_PLL_L_VAL(10) are used together)
5:2	INTERNAL_BITS5_2	EBI1_PLL_CONFIG(5:4) maps to PLL_CONFIG_CTL(5:4) Iseed control for Charge pump EBI1_PLL_CONFIG(3:2) maps to PLL_CONFIG_CTL(1:0) Setting for delay in reference path. Delta t (nominal values) 0x0: 0.5x Iseed 0x1: 1x Iseed 0x2: 2x Iseed 0x3: 4x Iseed 0x0: 200 ps 0x1: 400 ps 0x2: 800 ps 0x3: 1200 ps

EBI1_PLL_CONFIG (cont.)

Bits	Name	Description
1:0	INTERNAL_BITS1_0	EBI1_PLL_CONFIG(1:0) maps to PLL_CONFIG_CTL(3:2) Current mirror for charge pump current fixed divider ratio Iout / Ivco 0x0: 1 / L (may need to use this setting at low end of VCO range) 0x1: 2 / L 0x2: 3 / L 0x3: 5 / L

0x00903198 EBI1_PLL_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The EBI1_PLL_STATUS register is used for test purposes to report PLL state.

EBI1_PLL_STATUS

Bits	Name	Description
31:16	RESERVED_BITS31_16	RESERVED
15:0	PLL_AUTOCAL_VAL	EBI1_PLL_STATUS(15:6) : Unused, driven low (vssd domain) EBI1_PLL_STATUS(5:2) : Over voltage counter status EBI1_PLL_STATUS(1) : Over voltage detect flag EBI1_PLL_STATUS(0) : Negated of no_clock (if clock is detected, output is high))

0x009031A0 RIVA_PLL_MODE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The RIVA_PLL_MODE register configures and controls RIVA_PLL (SR2 PLL). All register bits are cleared (0) on RESOUT.

RIVA_PLL_MODE

Bits	Name	Description
31:6	RESERVED_BITS31_5	RESERVED

RIVA_PLL_MODE (cont.)

Bits	Name	Description
5:4	PLL_REF_XO_SEL	Specify the reference XO to be used 0x0: PXO (27MHz) 0x1: GND 0x2: CXO 0x3: RF_24MHZ_XO_SRC
3	PLL_PLLTEST	Set (1) this bit to enter the PLL test mode. Clear (0) this bit for the normal mode.
2	PLL_RESET_N	Low asserted reset for the digital logic in the PLL. This includes the MND counters and integer divider.
1	PLL_BYPASSNL	Clear (0) to bypass the PLL (PLLOUT is then identical to the input reference). Set (1) to use the PLL. Default is clear (0) at RESOUT (different from previous APQs)
0	PLL_OUTCTRL	Set (1) to activate the PLL's outputs (the analog circuitry is active but the output is not). Set (1) will enable the following PLL's outputs: PLLOUT_LV_MAIN (if MAIN output enabled RIVA_PLL_CONFIG[24]) PLLOUT_LV_BIST (If BIST output enabled RIVA_PLL_TEST_CTL[13]) PLLOUT_LV_AUX (If AUX output enabled RIVA_PLL_TEST_CTL[12]) Clear (0) to disable the PLL's output and save power. Clears (0) at RESOUT.

0x009031A4 RIVA_PLL_L_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The following equation (fractional division ratio) is used to calculate the RIVA_PLL output frequency:

VCO = REF * [L+(M/N)] / (R * P)

Where:

- R represents the predivider of 2
- P represents the post divider

The value of the RIVA_PLL_L_VAL register is the given value of L for that equation.

RIVA_PLL_L_VAL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED (This is the original assignment before CR154463.)
31	LFSR_DITHER_EN	PLL_CONFIG_CTL(31) 0x0: LFSR dither disabled 0x1: LFSR dither enabled (use this in conjunction with MASH11fracN mode)
30:29	LOCK_DET_CFG	PLL_CONFIG_CTL(30:29) Lock detection circuit configuration 0x0: Threshold = 2 pi / 7 0x1: Threshold = 2 pi / 15 0x2: Threshold = 2 pi / 23 0x3: Threshold = 2 pi / 31
28	FRACN_MODE_CTL	PLL_CONFIG_CTL(24) Frac-N mode control 0x0: MN- Accumulator FracN mode (legacy) 0x1: Mash11 FracN mode (Use PLL_N_val = 19'hFFFF in this mode for lowest inband dither power. Use PLL_CONFIG_CTL3:2 = 2'b0 in this mode for best quantization noise filtering)
27:26	OVER_VOLTAGE_CFG	PLL_CONFIG_CTL(27:26) Over voltage detect counter configuration 0x0: Detect at count = 0 0x1: Detect at count = 4 0x2: Detect at count = 8 0x3: Detect at count = 32
25	OVER_VOLTAGE_EN	PLL_CONFIG_CTL(25) 0x0: Over voltage detect counter is enabled 0x1: Over voltage detect counter is disabled
16:14	RESERVED_16_14	PLL_TEST_CTL (31:29) RESERVED
13	VCO_DCAPS_EN	PLL_CONFIG_CTL(13) Disable internally programmed VCO decoupling caps 0x0: Automatically controlled programmable VCO dcaps 0x1: Disable programmable VCO dcaps
11	REG_BIAS_CFG_B1	PLL_CONFIG_CTL(11) Bit1 of regulator stage 2 bias current setting
10	ADZ_CFG_B0	PLL_CONFIG_CTL(6) Bit0 of anti dead zone programmable input /filter phase offset control
8	VREG_ATEST_CTL	PLL_TEST_CTL (0) 0x0: Disconnect VREG to test op amp input 0x1: Connect VREG to test op amp input - observed on ATEST0

RIVA_PLL_L_VAL (cont.)

Bits	Name	Description
7:0	PLL_L	This register contains the 10-bit L value in the PLL's fractional division ratio.

0x009031A8 RIVA_PLL_M_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The value of the RIVA_PLL_M_VAL register is the given value of M for the fractional division ratio.

RIVA_PLL_M_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED
18:0	PLL_M	This register contains the 19-bit M value of the PLLn's numerator value in the fractional division ratio.

0x009031AC RIVA_PLL_N_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x01

The value of the RIVA_PLL_N_VAL register is the given value of N for the fractional division ratio.

RIVA_PLL_N_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED
18:0	PLL_N	This register contains the 19-bit N value of the PLLn's denominator value in the fractional division ratio.

0x009031B0 RIVA_PLL_TEST_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The RIVA_PLL_TEST_CTL register is used to enable the TEST, BIST and AUX outputs of PLL11 (SR2 PLL). The field descriptions show the mapping from 45nm NT wrapper RIVA_PLL_TEST_CTL register to SR2 PLL inputs, PLL_TEST_CTL. Some bits of PLL_TEST_CTL and PLL_CONFIG_CTL come from RIVA_PLL_L_VAL (CR154463).

RIVA_PLL_TEST_CTL

Bits	Name	Description
31:29	RESERVED_BITS31_29	RIVA_PLL_TEST_CTL(31:29) : Not Used See RIVA_PLL_L_VAL(16:14) that maps to PLL_TEST_CTL(31:29)
28:25	INTERNAL_BITS28_25	Not Used
24	INTERNAL_BIT24	RIVA_PLL_TEST_CTL(24) maps to PLL_TEST_CTL(11) 0x0: Output invert disabled 0x1: Output invert enabled
23:22	INTERNAL_BITS23_22	RIVA_PLL_TEST_CTL(23) : Not Used RIVA_PLL_TEST_CTL(22) maps to PLL_TEST_CTL(22) See RIVA_PLL_TEST_CTL(22:20) together below.
21	INTERNAL_BIT21	RIVA_PLL_TEST_CTL(21) maps to PLL_TEST_CTL(21) See RIVA_PLL_TEST_CTL(22:20) together below.
20:19	INTERNAL_BITS20_19	RIVA_PLL_TEST_CTL(20:19) maps to PLL_TEST_CTL(20:19) RIVA_PLL_TEST_CTL(22:20) Select current sink in noise generator resistor dac RIVA_PLL_TEST_CTL(19) Enable for supply noise generator circuit 0x0: Zero 0x1: Max 2 mA 0x2: Max 4 mA 0x3: Max 6 mA 0x4: Max 8 mA 0x5: Max 10 mA 0x6: Max 12 mA 0x7: Max 14 mA 0x0: Disable 0x1: Enable
18	INTERNAL_BIT18	RIVA_PLL_TEST_CTL(18) maps to PLL_TEST_CTL(18) See RIVA_PLL_TEST_CTL(18:17) together below.

RIVA_PLL_TEST_CTL (cont.)

Bits	Name	Description
17:16	INTERNAL_BITS17_16	RIVA_PLL_TEST_CTL(17:16) maps to PLL_TEST_CTL(17:16) RIVA_PLL_TEST_CTL(18:17) RIVA_PLL_TEST_CTL(16) 0x0: Disable analog supply measurement oscillator 0x1: Enable row0 of oscillator drivers (slowest frequency of oscillation) 0x2: Enable row0, row1 of oscillator drivers (mid frequency of oscillator) 0x3: Enable row0, row1, row2, row3 of oscillator drivers (highest frequency of oscillator) 0x0: Connect PLL clock path to pllout_lv_test output 0x1: Connect analog supply measurement oscillator path to pllout_lv_test output
15	INTERNAL_BIT15	RIVA_PLL_TEST_CTL(15) maps to PLL_TEST_CTL(13) When set to â□□1â□□ connect FILT_INT to test op amp input - observed on ATEST0
14	INTERNAL_BIT14	RIVA_PLL_TEST_CTL(14) maps to PLL_TEST_CTL(10) 0x0: Disable PLLOUT_LV_TEST 0x1: Enable PLLOUT_LV_TEST
13	PLLOUT_BIST_ENABLE	RIVA_PLL_TEST_CTL(13) maps to PLL_TEST_CTL(8) 0x0: Disable PLLOUT_LV_BIST 0x1: Enable PLLOUT_LV_BIST
12	PLLOUT_AUX_ENABLE	RIVA_PLL_TEST_CTL(12) maps to PLL_TEST_CTL(9) 0x0: Disable PLLOUT_LV_AUX 0x1: Enable PLLOUT_LV_AUX
11	INTERNAL_BIT11	Not Used
10	INTERNAL_BIT10	Not Used
9:8	RESERVED_BITS9_8	RIVA_PLL_TEST_CTL(9) : Not Used RIVA_PLL_TEST_CTL(8) : Not Used See RIVA_PLL_L_VAL(8) that maps to PLL_TEST_CTL(0)
7	INTERNAL_BIT7	RIVA_PLL_TEST_CTL(7) maps to PLL_TEST_CTL(7) 0x0: Disable PLLOUT_HV 0x1: Enable PLLOUT_HV
6	INTERNAL_BIT6	RIVA_PLL_TEST_CTL(6) maps to PLL_TEST_CTL(6) Current flows from VDDA (should terminate to VSSA on board) 0x0: Open test switch 0x1: Enable vco current div-8 output to ATEST0 pin

RIVA_PLL_TEST_CTL (cont.)

Bits	Name	Description
5	INTERNAL_BIT5	RIVA_PLL_TEST_CTL(5) maps to PLL_TEST_CTL(5) Current flows from AVDD (should terminate to AVSS on board). 0x0: Open test switch 0x1: Bypass ico current with external input from ATEST1 pin to bias the cp
4:1	INTERNAL_BITS4_1	RIVA_PLL_TEST_CTL(4:1) maps to PLL_TEST_CTL(4:1) RIVA_PLL_TEST_CTL(4) Current flows from VDDA (should terminate to VSSA on board). RIVA_PLL_TEST_CTL(3) RIVA_PLL_TEST_CTL(2) When set to â□□1â□□ enable switch to force external voltages from ATEST0 RIVA_PLL_TEST_CTL(1) When set to â□□1â□□ connect VINT to test op amp input - observed on ATEST0 RIVA_PLL_TEST_CTL(0) When set to â□□1â□□ connect VREG to test op amp input - observed on ATEST0 0x0: Open test switch 0x1: Enable bias circuit current to ATEST1 pin 0x0: Filter test op amp disabled 0x1: Enable the filter test opamp
0	INTERNAL_BIT0	RIVA_PLL_TEST_CTL(0) maps to PLL_TEST_CTL(12) Mux selectors for DTEST 0x0: Select C_MVAL (carry input for M-val: +1 dither) 0x1: Select NOCLKB

0x009031B4 RIVA_PLL_CONFIG

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00010401

Some bits of the RIVA_PLL_CONFIG register are used for test purposes. The field descriptions show the mapping from 45nm GP3 wrapper RIVA_PLL_CONFIG register to SR2 PLL input, PLL_CONFIG_CTL. Some bits of PLL_CONFIG_CTL come from RIVA_PLL_L_VAL (CR154463).

RIVA_PLL_CONFIG

Bits	Name	Description
31:25	RESERVED_BITS31_25	RIVA_PLL_CONFIG(31:25) : Not Used See RIVA_PLL_L_VAL(31:25) that maps to PLL_CONFIG_CTL(31:25).
24	INTERNAL_BIT24	RIVA_PLL_CONFIG(24) maps to PLL_CONFIG_CTL(21) 0x0: Disable PLLOUT_LV_MAIN 0x1: Enable PLLOUT_LV_MAIN
23:22	INTERNALBITS23_22	RIVA_PLL_CONFIG(23) maps to PLL_CONFIG_CTL(18) Filter timing configuration RIVA_PLL_CONFIG(22) maps to PLL_CONFIG_CTL(22) 0x0: Filter timing driven by early reference clock 0x1: Filter timing driven by the edge that arrives first - reference / divider output 0x0: Disable PLLOUT_LV_EARLY 0x1: Enable PLLOUT_LV_EARLY
21:20	INTERNALBITS21_20	RIVA_PLL_CONFIG(21) maps to PLL_CONFIG_CTL(17) Filter timing configuration RIVA_PLL_CONFIG(20) maps to PLL_CONFIG_CTL(20) MSB (Bit1) for output clock post divide ratio. (RIVA_PLL_CONFIG(20) and RIVA_PLL_CONFIG(16) are used together) 0x0: Conventional sample reset filter - double sampling disabled 0x1: Enable double sampled filter on opposite reference clock edge, enable filter phase offset circuit. Phase offset magnitude is controlled using ADZ config bits
19:18	PLLOUT_HV_DIVIDE	RIVA_PLL_CONFIG(19:18) maps to PLL_CONFIG_CTL(16:15) Regulator stage-1 output voltage setting 0x0: Vfilt *_1 (1.4 / 1) 0x1: Vfilt *_2 (1.35 / 1) 0x2: Vfilt *_3 (1.3 / 1) 0x3: Vfilt *_4 (1.25 / 1)
17	INTERNAL_BIT17	RIVA_PLL_CONFIG(17) maps to PLL_CONFIG_CTL(28) MN accumulator 0x0: Disable 0x1: Enable

RIVA_PLL_CONFIG (cont.)

Bits	Name	Description
16	POST_DIVIDE	RIVA_PLL_CONFIG(16) maps to PLL_CONFIG_CTL(19) LSB (Bit0) for output clock post divide ratio RIVA_PLL_CONFIG(20) : RIVA_PLL_CONFIG(16) maps to PLL_CONFIG_CTL(20:19) 0x0: 1 (Use this setting when bypassing reference clock to PLL output) 0x1: 2 0x2: 4 0x3: Unused, Reserved
15	PRE_DIVIDE	RIVA_PLL_CONFIG(15) maps to PLL_CONFIG_CTL(23) CLK_REF pre-divide ratio 0x0: 1 0x1: 2
14	PLLOUT_HV_ENABLE	RIVA_PLL_CONFIG(14) maps to PLL_CONFIG_CTL(14) 0x0: Disable iseed gating 0x1: Enables no_clock signal to gate iseed current in the charge pump
13	RESERVED_BIT13	RIVA_PLL_CONFIG(13) : Not Used See RIVA_PLL_L_VAL(13) that maps to PLL_CONFIG_CTL(13).
12	INTERNAL_BIT12	RIVA_PLL_CONFIG(12) maps to PLL_CONFIG_CTL(12) Enable / Bypass for stage 1 regulator 0x0: Enable 0x1: Bypass
11	RESERVED_BIT11	RIVA_PLL_CONFIG(11) : Not Used See RIVA_PLL_L_VAL(11) that maps to PLL_CONFIG_CTL(11). (RIVA_PLL_L_VAL(11) and RIVA_PLL_CONFIG(10) are used together)
10:9	INTERNAL_BITS10_9	RIVA_PLL_CONFIG(10:9) maps to PLL_CONFIG_CTL(10:9) RIVA_PLL_CONFIG(10) is LSB (Bit0) of regulator stage 2 Bias current setting RIVA_PLL_L_VAL(11) : RIVA_PLL_CONFIG(10) maps to PLL_CONFIG_CTL(11:10) (RIVA_PLL_CONFIG(9:8) are used together) 0x0: 1x Ivco / L 0x1: 2x Ivco / L 0x2: 3x Ivco / L 0x3: 4x Ivco / L

RIVA_PLL_CONFIG (cont.)

Bits	Name	Description
8:7	VCO	RIVA_PLL_CONFIG(8:7) maps to PLL_CONFIG_CTL(8:7) RIVA_PLL_CONFIG(9:8) maps to PLL_CONFIG_CTL(9:8) Reference voltage setting for over voltage detection on stage 2 regulator output RIVA_PLL_CONFIG(7) RIVA_PLL_CONFIG(7) is MSB (bit1) of Anti dead zone programmable input / Filter phase offset control and LSB (bit0) is RIVA_PLL_L_VAL(10) RIVA_PLL_CONFIG(7) : RIVA_PLL_L_VAL(10) maps to PLL_CONFIG_CTL(7:6) 0x0: Power down over voltage detection 0x1: 1.15 / 1.8 0x2: 1.2 / 1.8 0x3: 1.25 / 1.8 0x0: 1 delay elements / Icpoffset = 0 (Tcpoffset = 0, Filter offset disabled) 0x1: 2 delay elements / Icpoffset = 0.6uA @ Fref = 20MHz, Fo = 1GHz (Tcpoffset = 250 ps) 0x2: 3 delay elements / Icpoffset = 1.2uA @ Fref = 20MHz, Fo = 1GHz (Tcpoffset = 500 ps) 0x3: 4 delay elements / Icpoffset = 4.2uA @ Fref = 20MHz, Fo = 1GHz (Tcpoffset = 1750 ps)
6	RESERVED_BIT6	RIVA_PLL_CONFIG(6) : Not Used See RIVA_PLL_L_VAL(10) that maps to PLL_CONFIG_CTL(6). (RIVA_PLL_CONFIG(7) and RIVA_PLL_L_VAL(10) are used together)
5:2	INTERNAL_BITS5_2	RIVA_PLL_CONFIG(5:4) maps to PLL_CONFIG_CTL(5:4) Iseed control for Charge pump RIVA_PLL_CONFIG(3:2) maps to PLL_CONFIG_CTL(1:0) Setting for delay in reference path. Delta t (nominal values) 0x0: 0.5x Iseed 0x1: 1x Iseed 0x2: 2x Iseed 0x3: 4x Iseed 0x0: 200 ps 0x1: 400 ps 0x2: 800 ps 0x3: 1200 ps

RIVA_PLL_CONFIG (cont.)

Bits	Name	Description
1:0	INTERNAL_BITS1_0	RIVA_PLL_CONFIG(1:0) maps to PLL_CONFIG_CTL(3:2) Current mirror for charge pump current fixed divider ratio Iout / Ivco 0x0: 1 / L (may need to use this setting at low end of VCO range) 0x1: 2 / L 0x2: 3 / L 0x3: 5 / L

0x009031B8 RIVA_PLL_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The RIVA_PLL_STATUS register is used for test purposes to report PLL state.

RIVA_PLL_STATUS

Bits	Name	Description
31:16	RESERVED_BITS31_16	RESERVED
15:0	PLL_AUTOCAL_VAL	RIVA_PLL_STATUS(15:6) : Unused, driven low (vssd domain) RIVA_PLL_STATUS(5:2) : Over voltage counter status RIVA_PLL_STATUS(1) : Over voltage detect flag RIVA_PLL_STATUS(0) : Negated of no_clock (if clock is detected, output is high)

0x009031C0 PLL14_MODE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The PLL14_MODE register configures and controls PLL14_ (SRPLL). All register bits are cleared (0) on RESOUT.

PLL14_MODE

Bits	Name	Description
31:22	RESERVED_BITS31_22	RESERVED
21	PLL_VOTE_FSM_RESET	Resets PLL voting FSM 0x0: De-asserts Reset to PLL voting FSM 0x1: Resets PLL voting FSM

PLL14_MODE (cont.)

Bits	Name	Description
20	PLL_VOTE_FSM_ENA	Enables PLL voting FSM 0x0: Disabled 0x1: Enabled
19:14	PLL_BIAS_COUNT	Sets PLL bias count of PLL voting FSM
13:8	PLL_LOCK_COUNT	Sets PLL lock time of PLL voting FSM
7:5	RESERVED_BITS_7_5	RESERVED
4	PLL_REF_XO_SEL	Specify the reference XO to be used. 0x0: PXO 0x1: CXO
3	PLL_PLLTEST	Set(1) this bit to enter the PLL test mode. Clear (0) this bit for the normal mode.
2	PLL_RESET_N	Low asserted reset for the digital logic in the PLL. This includes the MND counters and integer divider.
1	PLL_BYPASSNL	Clear (0) to bypass the PLL (PLLOUT is then identical to the input reference). Set (1) to use the PLL. Default is clear (0) at RESOUT (different from previous APQs)
0	PLL_OUTCTRL	Set (1) to activate the PLL's outputs (the analog circuitry is active but the output is not). Set (1) will enable the following PLL's outputs: PLLOUT_LV_MAIN (if MAIN output enabled PLL14_CONFIG[24]) PLLOUT_LV_BIST (If BIST output enabled PLL14_TEST_CTL[13]) PLLOUT_LV_AUX (If AUX output enabled PLL14_TEST_CTL[12]) Clear (0) to disable the PLL's output and save power. Clears (0) at RESOUT.

0x009031C4 PLL14_L_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The following equation (fractional division ratio) is used to calculate the PLL14 (SR PLL) output frequency:

VCO = REF * [L+(M/N)] / (R * P)

Where:

- R represents the predivider of 2
- P represents the post divider

The value of the PLL14_L_VAL register is the given value of L for that equation.

PLL14_L_VAL

Bits	Name	Description
31:10	RESERVED_BITS31_10	UNUSED (this is the original assignment before CR154463)
31	ICP_TST_EN	PLL_TEST_CTL(9) Charge pump test current control 0x0: Disable 0x1: Enable
27:26	NMOSC_FREQ_CTL	PLL_CONFIG_CTL(27:26) 0x0: Highest (2.8 GHz at TT / 1.05V /40C) 0x1: 1/2 highest 0x2: 1/3 highest 0x3: 1/4 highest
25:24	PFD_DZSEL	PLL_CONFIG_CTL(25:24) PFD reset pulse width adjustment 0x0: 1x delay 0x1: 2x delay 0x2: 3x delay 0x3: 4x delay
23	NMOSC_EN	PLL_CONFIG_CTL(23) Noise measurement oscillator control 0x0: Disable 0x1: Enable
21:20	ICP_DIV	PLL_CONFIG_CTL(21:20) Charge pump bias mirror multiplication factor 0x0: 1 0x1: 3/2 0x2: 7/4 0x3: 9/4
19:18	IREG_DIV	PLL_CONFIG_CTL(19:18) Regulator bias mirror multiplication factor 0x0: 1 0x1: 7/5 0x2: 9/5 0x3: 11/5
17:16	CUSEL	PLL_CONFIG_CTL(17:16) VCO decoupling cap unit size 0x0: 125 fF 0x1: 250 fF 0x2: 375 fF 0x3: 500 fF

PLL14_L_VAL (cont.)

Bits	Name	Description
15	REF_MODE	PLL_CONFIG_CTL(15) Reference circuit mode 0x0: Bandgap mode (seed currents sourced from bandgap circuit and Nwell reference circuit active) 0x1: Supply independent mode (seed currents sourced from supply independent circuit amd Nwell reference pulled to VDDA)
14	PLLOUT_LV_TEST	PLL_TEST_CTL(14) PLLOUT_LV_TEST source selection 0x0: PLL output clock 0x1: Noise measurement oscillator
13:12	CFG_LOCKDET	PLL_CONFIG_CTL(13:12) Lock detector phase error threshold 0x0: 2 pi /7 0x1: 2 pi /15 0x2: 2 pi /23 0x3: 2 pi /31
11	FORCE_ISEED	PLL_CONFIG_CTL(11) Seed current control 0x0: Turn off seed currents when clock is detected 0x1: Keep seed currents on at all times
9:0	PLL_L	This register contains the 10-bit L value in the PLL0's fractional division ratio.

0x009031C8 PLL14_M_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

The value of the PLL14_M_VAL register is the given value of M for the fractional division ratio.

PLL14_M_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED
18:0	PLL_M	This register contains the 19-bit M value of the PLLn's numerator value in the fractional division ratio.

0x009031CC PLL14_N_VAL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x01

The value of the PLL14_N_VAL register is the given value of N for the fractional division ratio.

PLL14_N_VAL

Bits	Name	Description
31:19	RESERVED_BITS31_19	UNUSED
18:0	PLL_N	This register contains the 19-bit N value of the PLLn's denominator value in the fractional division ratio.

0x009031D0 PLL14_TEST_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

The PLL14_TEST_CTL register is used to enable the TEST, BIST and AUX outputs of PLL14 (SR PLL). The field descriptions show the mapping from 45nm NT wrapper PLL14_TEST_CTL register to SR PLL inputs, PLL_TEST_CTL and PLL_CONFIG_CTL. Some bits of PLL_TEST_CTL and PLL_CONFIG_CTL come from PLL14_L_VAL (CR154463).

PLL14_TEST_CTL

Bits	Name	Description
31:19	RESERVED_BITS31_19	PLL14_TEST_CTL(31:30) : Not Used See PLL14_L_VAL(25:24) that maps to PLL_CONFIG_CTL(25:24) PLL14_TEST_CTL(29:28) : Not Used See PLL14_L_VAL(21:20) that maps to PLL_CONFIG_CTL(21:20) PLL14_TEST_CTL(27:26) : Not Used See PLL14_L_VAL(19:18) that maps to PLL_CONFIG_CTL(19:18) PLL14_TEST_CTL(25:24) : Not Used See PLL14_L_VAL(17:16) that maps to PLL_CONFIG_CTL(17:16) PLL14_TEST_CTL(23:22) : Not Used See PLL14_L_VAL(13:12) that maps to PLL_CONFIG_CTL(13:12) PLL14_TEST_CTL(21) : Not Used See PLL14_L_VAL(11) that maps to PLL_CONFIG_CTL(11) PLL14_TEST_CTL(20) : Not Used. See PLL14_L_VAL(31) that maps to PLL_TEST_CTL(9) PLL14_TEST_CTL(19) : Not Used
18:17	INTERNAL_BITS18_17	PLL14_TEST_CTL(18:17) : Not Used
16	INTERNAL_BIT16	PLL14_TEST_CTL(16) maps to PLL_CONFIG_CTL(5) Output clock polarity 0x0: Do not invert output 0x1: Invert output
15	INTERNAL_BIT15	PLL14_TEST_CTL(15) maps to PLL_CONFIG_CTL(4) PLLOUT_LV_TEST enable 0x0: Disable 0x1: Enable
14	RESERVED_BIT14	PLL14_TEST_CTL(14) : Not used. See PLL14_L_VAL(14) that maps to PLL_TEST_CTL(14)
13	PLLOUT_BIST_ENABLE	PLL14_TEST_CTL(13) maps to PLL_CONFIG_CTL(2) PLLOUT_LV_BIST enable 0x0: Disable 0x1: Enable (must be enabled to use noise generator)
12	PLLOUT_AUX_ENABLE	PLL14_TEST_CTL(12) maps to PLL_CONFIG_CTL(1) PLLOUT_LV_AUX enable 0x0: Disable 0x1: Enable

PLL14_TEST_CTL (cont.)

Bits	Name	Description
11:0	INTERNAL_BIT11_0	PLL14_TEST_CTL(11) : Not Used PLL14_TEST_CTL(10) maps to PLL_TEST_CTL(8) Charge pump external bias control PLL14_TEST_CTL(9:8) maps to PLL_CONFIG_CTL(29:28) PFD force bits PLL14_TEST_CTL(9) = Force PFD up PLL14_TEST_CTL(8) = Force PFD down PLL14_TEST_CTL(7) maps to PLL_TEST_CTL(7) DTEST signal select PLL14_TEST_CTL(6) maps to PLL_TEST_CTL(6) ATEST amplifier bypass control PLL14_TEST_CTL(5:4) maps to PLL_TEST_CTL(5:4) ATEST1 signal select Force PLL filter voltage externally (set PLL_TEST_CTL(6) to 1) PLL14_TEST_CTL(3:2) maps to PLL_TEST_CTL(3:2) ATEST0 signal select PLL14_TEST_CTL(1) maps to PLL_TEST_CTL(1) ATEST1 Control PLL14_TEST_CTL(0) maps to PLL_TEST_CTL(0) ATEST0 Control 0x0: Disable 0x1: Enable 0x0: Normal operation_1 0x1: Force PFD UP -> 1 0x0: Normal operation_2 0x1: Force PFD DN -> 1 0x0: Select clock detect signal 0x1: Select feedback divider output signal 0x0: Do not bypass ATEST buffer amplifier 0x1: Bypass ATEST buffer amplifier 0x0: Observe Nwell reference (set PLL_TEST_CTL6 to 0) 0x1: Observe regulator output (set PLL_TEST_CTL6 to 0) 0x2: Observe PLL filter voltage (set PLL_TEST_CTL6 to 0) 0x3: Supply noise measurement mode

PLL14_TEST_CTL (cont.)

Bits	Name	Description
		0x0: Provide external bias current to charge pump (set PLL_TEST_CTL8 to 1) 0x1: Observe ICO test current (set PLL_TEST_CTL9 to 1) 0x2: Observe bandgap test current 0x3: VSSA 0x0: Disable ATEST1 0x1: Enable ATEST1 0x0: Disable ATEST0 0x1: Enable ATEST0

0x009031D4 PLL14_CONFIG

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0084248B

The field descriptions show the mapping from 45nm NT wrapper PLL14_CONFIG register to SR PLL input, PLL_CONFIG_CTL. Some bits of PLL_CONFIG_CTL come from PLL14_TEST_CTL and PLL14_L_VAL (CR154463).

PLL14_CONFIG

Bits	Name	Description
31:28	RESERVED_BITS31_28	PLL14_CONFIG(31:30) : Not Used See PLL14_L_VAL(27:26) that maps to PLL_CONFIG_CTL(27:26) PLL14_CONFIG(29) : Not Used See PLL14_L_VAL(23) that maps to PLL_CONFIG_CTL(23) PLL14_CONFIG(28) : Not Used See PLL14_L_VAL(15) that maps to PLL_CONFIG_CTL(15)
27	EARLY_OUT_ENA	PLL14_CONFIG(27) maps to PLL_CONFIG_CTL(3) PLLOUT_LV_EARLY enable 0x0: Disable 0x1: Enable
26	CLK33_OUT_SEL	Not Used
25	CLK33_OUT_ENA	Not Used
24	OUT_SEL	Not Used
23	MAIN_OUT_ENA	PLL14_CONFIG(23) maps to PLL_CONFIG_CTL(0) PLLOUT_LV_MAIN enable 0x0: Disable 0x1: Enable

PLL14_CONFIG (cont.)

Bits	Name	Description
22	MN_ACCUM_ENA	PLL14_CONFIG(22) maps to PLL_CONFIG_CTL(14) PLL fractional mode control 0x0: Disable 0x1: Enable
21:20	PLLOUT_DIVIDE	PLL14_CONFIG(21:20) maps to PLL_CONFIG_CTL(8:7) PLL Post-divider control 0x0: Divide by 1 (use this setting when sending reference clock to output) 0x1: Divide by 2 0x2: Divide by 4 0x3: Invalid
19	PRE_DIVIDE	PLL14_CONFIG(19) maps to PLL_CONFIG_CTL(6) PLL pre-divider control 0x0: Divide by 1 0x1: Divide by 2
18	INTERNAL_BIT18	Not Used
17:16	VCO	PLL14_CONFIG(17) maps to PLL_CONFIG_CTL(9) VCO Selection PLL14_CONFIG(16) : Not Used 0x0: Select 100 - 500 MHz VCO 0x1: Select 400 - 1400 MHz VCO
15	INTERNAL_BIT15	Not Used
14:0	INTERNAL_BITS14_0	Not Used

0x009031D8 PLL14_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x00

The PLL14_STATUS register is used for test purposes to report PLL state.

PLL14_STATUS

Bits	Name	Description
31:17	RESERVED_BITS31_17	RESERVED
16	PLL_ACTIVE_FLAG	pll_active_flag from PLL voting FSM. It indicates when FSM has enabled the PLL and PLL should be locked.
15:0	PLL_D	PLL14_STATUS(15:1) : Unused and shorted to VSSD PLL14_STATUS(0) : Clock detect

0x00903200 SC_PLL0_MODE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Mode register.

SC_PLL0_MODE

Bits	Name	Description
31:4	RESERVED_BITS_31_4	
3	PLLTEST	pll mode bits
2	RESET_N	pll mode bits
1	BYPASSNL	pll mode bits
0	OUTCTRL	pll mode bits

0x00903204 SC_PLL0_CONFIG_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x7805c665

PLL Config control register.

SC_PLL0_CONFIG_CTL

Bits	Name	Description
31:30	INJECTION_MODE	Injection Mode control for VCO 0x0: No caps on injection node 0x1: 18fF cap 0x2: 36fF cap 0x3: 54 fF cap
29:28	WINDOW_SIZE	Window Size for phase detector used in injection locked VCO 0x0: 50ps window size 0x1: 67ps window size 0x2: 83ps window size 0x3: 100ps window size
27:26	LOCK_DET_CFG	Lock detection circuit configuration 0x0: Threshold = 2pi/7 0x1: Threshold = 2pi/15 0x2: Threshold = 2pi/23 0x3: Threshold = 2pi/31

SC_PLL0_CONFIG_CTL (cont.)

Bits	Name	Description
25	MN_ACCUMULATOR	0x0: Disable MN accumulator 0x1: Enable MN accumulator
24:23	PRE_DIVIDE_RATIO	SC_PLL0_CONFIG_CTL(24) : Enable/ Disable for PLLOUT_LV_MASTER. SC_PLL0_CONFIG_CTL(23) : CLK_REF pre divide ratio 0x0: Disable 0x1: Enable 0x0: Predivide by 1 0x1: Predivide by 2
22	PLLOUT_EARLY	0x0: Disable PLLOUT_LV_EARLY 0x1: Enable PLLOUT_LV_EARLY
21	PLLOUT_MAIN	0x0: Disable PLLOUT_LV_MAIN 0x1: Enable PLLOUT_LV_MAIN
20:19	POST_DIVIDE_RATIO	Output clock post divide ratio 0x0: 1 0x1: 2 0x2: 4 0x3: Reserved
18:17	LEFT_SHIFT	Left shift operation configuration on droop control bits. Offset1, Offset0 bits are set using config_ctl[9:8]. Slave VCO Throttle control = 00 : {offset1, offset0, droopcontrol[2:0]} 01 : {offset1, droopcontrol[2:0], offset0} 10 : {droopcontrol[2:0], offset1, offset0} 0x3: Reserved
16:15	INJECTION_STRENGTH	Configure injection strength for slave VCO 0x0: 1/4th of Islave 0x1: 1/2 of Islave 0x2: 3/4 of Islave 0x3: Islave
14	ISEED_GATING	0x0: Disable iseed gating 0x1: Enables no_clock signal to gate iseed current in the charge pump
13:12	SLAVE_VCO_DCAPS	Configure slave VCO dcaps 0x0: Default; 4pF + 187.5fFper unit L value 0x1: 4pF + 113fF per unit L value 0x2: 4pF + 62.5fF per unit L value 0x3: Fixed 4pF total cap

SC_PLL0_CONFIG_CTL (cont.)

Bits	Name	Description
11:10	REGULATOR_BIAS	Regulator Bias current setting 0x0: 0.5 x Ivco/L 0x1: 1 x Ivco/L 0x2: 2 x Ivco/L 0x3: 4 x Ivco/L
9:8	DROOP_OFFSET	External droop offset to convert 3 bit TDC droop code to 5 bit regulator throttle 0x0: offset bits set to 00 0x1: offset bits set to 01 0x2: offset bits set to 10 0x3: offset bits set to 11
7:6	ANTI_DEAD_ZONE	Anti dead zone programmable input 0x0: 1 delay elements 0x1: 2 delay elements 0x2: 3 delay elements 0x3: 4 delay elements
5:4	ISEED_CTL	Iseed control for charge pump 0x0: 0.5 x Iseed 0x1: 1 x Iseed 0x2: 2 x Iseed 0x3: 4 x Iseed
3:2	CURRENT_MIRROR	Current mirror for charge pump current fixed divider ratio. Iout / Iin = 0x0: 1/ 2L 0x1: 1/L 0x2: 2/L 0x3: 4/L
1:0	DELTA_T	Setting for delay in reference path 0x0: 200ps 0x1: 400ps 0x2: 800 ps 0x3: 1200 ps

0x00903208 SC_PLL0_L_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL L Val register.

SC_PLL0_L_VAL

Bits	Name	Description
31:7	RESERVED_BITS_31_7	RESERVED
6:0	L_VAL	L value

0x0090320C SC_PLL0_M_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL M Val register.

SC_PLL0_M_VAL

Bits	Name	Description
31:19	RESERVED_BITS_31_19	RESERVED
18:0	M_VAL	M value

0x00903210 SC_PLL0_N_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL N Val register.

SC_PLL0_N_VAL

Bits	Name	Description
31:19	RESERVED_BITS_31_19	RESERVED
18:0	N_VAL	N value

0x00903214 SC_PLL0_DROOP_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0xc000

PLL Droop register.

SC_PLL0_DROOP_CTL

Bits	Name	Description
31	NOISE_PATTERN_SHIFT	Control pattern shifting operation in vddd_scorpion droop pattern generator 0x0: Disable 0x1: Enable
30:29	LOAD_ADDRESS	Load address for vddd_scorpion droop pattern generator 0x0: Address 3:0 bits for pattern LSB 0x1: Address 8:4 bits for pattern LSB 0x2: Address 3:0 bits for pattern MSB 0x3: Address 8:4 bits for pattern MSB
28:25	DROOP_PATTERN_DATA	4 bits of pattern data for vddd_scorpion droop pattern generator
24:23	RESET_CNT_TIMER_CFG	Reset counter timer configuration 0x0: Count 2049 cycles of input clock 0x1: Count 4097cycles of input clock 0x2: Count 8193 cycles of input clock 0x3: Count 16385 cycles of input clock
22	DROOP_DET_CLK_SEL	Clock select for droop detector 0x0: Use HF PLL clock 0x1: Use droop_clk_in
21:20	OUTPUT_SER_DATA_DIV	Clock divider control for output serialized data 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: RESERVED
19:18	DROOP_DET_CLK_DIV	Clock divider control for droop detection clock 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: RESERVED
17	ATEST_MODE	Atest mode for pulse generation circuit 0x0: Disable 0x1: Enable
16	BYPASS_MODE	Bypass mode for pulse generation circuit 0x0: Internally generated pulse control current 0x1: Bypass with external control current
15	PULSE_GENERATION	For controling pulse generation circuit 0x0: Disable 0x1: Enable

SC_PLL0_DROOP_CTL (cont.)

Bits	Name	Description
14:13	PULSE_WIDTH_CTL	Pulse width control 0x0: 140 ps 0x1: 270 ps 0x2: 390 ps 0x3: 470 ps
12:10	EXTERNAL_DROOP_CTL0	External droop control 0 0x0: No droop detected 0x7: Maximum droop detected
9:7	EXTERNAL_DROOP_CTL1	External droop control 1 0x0: No droop detected 0x7: Maximum droop detected
6	EXTERNAL_DROOP_DET0	External droop detect 0 0x0: No droop detected 0x1: Droop detected
5	EXTERNAL_DROOP_DET1	External droop detect 1 0x0: No droop detected 0x1: Droop detected
4	EXTERNAL_DROOP_CODE	Select external droop code, droop detect 0x0: Select external droop code 0 0x1: Select external droop code 1
3	DROOP_CODE_DETECT	Control external droop code, droop detect mode 0x0: Disable 0x1: Enable
2:1	DROOP_CONTROL_SE	Select output signal on droop_control_se lines For droop_test_se1, For droop_test_se2, 0x0: Pulse width control 0 0x1: Divided reference cloc_2 0x2: Inverter chain latching clock 0x3: Reference clock 0x0: Pulse width control 1 0x1: Pulse Generator output 0x2: Output from last stage in inverter chain 0x3: Serialized droop control output
0	OUTPUT_DRIVER	Output driver control on droop_control_se 0x0: Disable 0x1: Enable

0x00903218 SC_PLL0_TEST_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Test control register.

SC_PLL0_TEST_CTL

Bits	Name	Description
31:30	RESERVED_BITS_31_30	RESERVED
29	SLAVE_VCO_INJECTION	0x0: Slave VCO injection is disabled during droop 0x1: Slave VCO injection lock is always enabled
28	SYNC_MODE	0x0: Slave re-locking is synchronized 0x1: Slave re-locking is asynchronous
27:25	RESERVED_BITS_27_25	RESERVED
24:23	NOISE_OSC_CTL_VDDD_SCORPION	Control for noise measurement oscillator on VDDD_SCORPION supply 0x0: Highest frequency of oscillation 0x1: 1/2 Highest frequency 0x2: 1/3 Highest frequency 0x3: 1/4 Highest frequency
22:20	NOISE_GEN_CFG_VDDA	VDDA Noise Generator configuration. Current sink in noise generator resistor dac, 0x0: 0 0x1: Max 2 mA 0x2: Max 4 mA 0x3: Max 6 mA 0x4: Max 8 mA 0x5: Max 10 mA 0x6: Max 12 mA 0x7: Max 14 mA
19	SUPPLY_NOISE_GEN	To control the supply noise generator circuit 0x0: Disable 0x1: Enable
18:17	NOISE_OSC_CTL_VDDA	Control for noise measurement oscillator on VDDA supply 0x0: Disable analog supply measurement oscillator 0x1: Slowest frequency of oscillation 0x2: Mid frequency of oscillation 0x3: Highest frequency of oscillation

SC_PLL0_TEST_CTL (cont.)

Bits	Name	Description
16:15	CONNECT_PLL_LV_TEST	0x0: Connect PLL clock path to pllout_lv_test output 0x1: Connect vddd_scorpion supply noise measurement oscillator path to pllout_lv_test output 0x2: Connect analog supply noise measurement oscillator path to pllout_lv_test output 0x3: RESERVED
14	NOISE_OSC_EN	Used to control the noise measurement oscillator on VDDD_SCORPION supply 0x0: Disable 0x1: Enable
13	FILT_INT	0x0: Disconnect 0x1: Connect FILT_INT to test op amp input - observed on ATEST0
12	DTEST_MUX_SEL	Mux selectors for DTEST(note: set PLLTEST to enable DTEST) 0x0: Reserved 0x1: Select NOCLK
11	OUTPUT_INVERT	0x0: Disable 0x1: Enable
10	PLLOUT_LV_TEST	0x0: Disable 0x1: Enable
9	PLLOUT_LV_AUX	0x0: Disable 0x1: Enable
8	PLLOUT_LV_BIST	0x0: Disable 0x1: Enable
7	PLLOUT_HV	0x0: Disable 0x1: Enable
6	VCO_CURRENT_ATEST0	current flows from VDDA (should terminate to VSSA on board) 0x0: Open test switch 0x1: Enable VCO current div-16 output to ATEST0 pin
5	ICO_CURRENT_ATEST1	Current flows from AVDD (should terminate to AVSS on board) 0x0: Open test switch 0x1: Bypass ICO current with external input from ATEST1 pin to bias the cp
4	BIAS_CURRENT_ATEST1	Current flows from VDDA (should terminate to VSSA on Board) 0x0: Open test switch 0x1: Enable bias circuit current to ATEST1 pin
3	FILTER_TEST_OPAMP	0x0: Disable 0x1: Enable
2	SWITCH_ATEST0	0x0: Disabled 0x1: Enables switch to force external voltages from ATEST0

SC_PLL0_TEST_CTL (cont.)

Bits	Name	Description
1	VREG_SLAVE_ATEST0	0x0: Disconnect 0x1: Connect VREG_SLAVE to test op amp input -observed on ATEST0
0	VREG_MST_ATEST0	0x0: Disconnect 0x1: Connect VREG_MST to test op amp input -observed on ATEST0

0x0090321C SC_PLL0_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Status register.

SC_PLL0_STATUS

Bits	Name	Description
31:16	RESERVED_BITS_31_16	RESERVED
15:0	PLL_STATUS	SC_PLL0_STATUS(15:6) : Unused, driven low (vssd domain) SC_PLL0_STATUS(5:2) : Over voltage counter status SC_PLL0_STATUS(1) : Over voltage detect flag SC_PLL0_STATUS(0) : Negated of no_clock (if clock is detected, output is high)

0x00903240 SC_PLL1_MODE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Mode register.

SC_PLL1_MODE

Bits	Name	Description
31:4	RESERVED_BITS_31_4	
3	PLLTEST	pll mode bits
2	RESET_N	pll mode bits
1	BYPASSNL	pll mode bits

SC_PLL1_MODE (cont.)

Bits	Name	Description
0	OUTCTRL	pll mode bits

0x00903244 SC_PLL1_CONFIG_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x7805c665

PLL Config control register.

SC_PLL1_CONFIG_CTL

Bits	Name	Description
31:30	INJECTION_MODE	Injection Mode control for VCO 0x0: No caps on injection node 0x1: 18fF cap 0x2: 36fF cap 0x3: 54 fF cap
29:28	WINDOW_SIZE	Window Size for phase detector used in injection locked VCO 0x0: 50ps window size 0x1: 67ps window size 0x2: 83ps window size 0x3: 100ps window size
27:26	LOCK_DET_CFG	Lock detection circuit configuration 0x0: Threshold = 2pi/7 0x1: Threshold = 2pi/15 0x2: Threshold = 2pi/23 0x3: Threshold = 2pi/31
25	MN_ACCUMULATOR	0x0: Disable MN accumulator 0x1: Enable MN accumulator
24:23	PRE_DIVIDE_RATIO	SC_PLL0_CONFIG_CTL(24) : Enable/ Disable for PLLOUT_LV_MASTER. SC_PLL0_CONFIG_CTL(23) : CLK_REF pre divide ratio 0x0: Disable 0x1: Enable 0x0: Predivide by 1 0x1: Predivide by 2
22	PLLOUT_EARLY	0x0: Disable PLLOUT_LV_EARLY 0x1: Enable PLLOUT_LV_EARLY
21	PLLOUT_MAIN	0x0: Disable PLLOUT_LV_MAIN 0x1: Enable PLLOUT_LV_MAIN

SC_PLL1_CONFIG_CTL (cont.)

Bits	Name	Description
20:19	POST_DIVIDE_RATIO	Output clock post divide ratio 0x0: 1 0x1: 2 0x2: 4 0x3: Reserved
18:17	LEFT_SHIFT	Left shift operation configuration on droop control bits. Offset1, Offset0 bits are set using config_ctl[9:8]. Slave VCO Throttle control = 00 : {offset1, offset0, droopcontrol[2:0]} 01 : {offset1, droopcontrol[2:0], offset0} 10 : {droopcontrol[2:0], offset1, offset0} 0x3: Reserved
16:15	INJECTION_STRENGTH	Configure injection strength for slave VCO 0x0: 1/4th of Islave 0x1: 1/2 of Islave 0x2: 3/4 of Islave 0x3: Islave
14	ISEED_GATING	0x0: Disable iseed gating 0x1: Enables no_clock signal to gate iseed current in the charge pump
13:12	SLAVE_VCO_DCAPS	Configure slave VCO dcaps 0x0: Default; 4pF + 187.5fFper unit L value 0x1: 4pF + 113fF per unit L value 0x2: 4pF + 62.5fF per unit L value 0x3: Fixed 4pF total cap
11:10	REGULATOR_BIAS	Regulator Bias current setting 0x0: 0.5 x Ivco/L 0x1: 1 x Ivco/L 0x2: 2 x Ivco/L 0x3: 4 x Ivco/L
9:8	DROOP_OFFSET	External droop offset to convert 3 bit TDC droop code to 5 bit regulator throttle 0x0: offset bits set to 00 0x1: offset bits set to 01 0x2: offset bits set to 10 0x3: offset bits set to 11
7:6	ANTI_DEAD_ZONE	Anti dead zone programmable input 0x0: 1 delay elements 0x1: 2 delay elements 0x2: 3 delay elements 0x3: 4 delay elements

SC_PLL1_CONFIG_CTL (cont.)

Bits	Name	Description
5:4	ISEED_CTL	Iseed control for charge pump 0x0: 0.5 x Iseed 0x1: 1 x Iseed 0x2: 2 x Iseed 0x3: 4 x Iseed
3:2	CURRENT_MIRROR	Current mirror for charge pump current fixed divider ratio. Iout / Iin = 0x0: 1/ 2L 0x1: 1/L 0x2: 2/L 0x3: 4/L
1:0	DELTA_T	Setting for delay in reference path 0x0: 200ps 0x1: 400ps 0x2: 800 ps 0x3: 1200 ps

0x00903248 SC_PLL1_L_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL L Val register.

SC_PLL1_L_VAL

Bits	Name	Description
31:7	RESERVED_BITS_31_7	RESERVED
6:0	L_VAL	L value

0x0090324C SC_PLL1_M_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL M Val register.

SC_PLL1_M_VAL

Bits	Name	Description
31:19	RESERVED_BITS_31_19	RESERVED
18:0	M_VAL	M value

0x00903250 SC_PLL1_N_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL N Val register.

SC_PLL1_N_VAL

Bits	Name	Description
31:19	RESERVED_BITS_31_19	RESERVED
18:0	N_VAL	N value

0x00903254 SC_PLL1_DROOP_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0xc000

PLL Droop register.

SC_PLL1_DROOP_CTL

Bits	Name	Description
31	NOISE_PATTERN_SHIFT	Control pattern shifting operation in vddd_scorpion droop pattern generator 0x0: Disable 0x1: Enable
30:29	LOAD_ADDRESS	Load address for vddd_scorpion droop pattern generator 0x0: Address 3:0 bits for pattern LSB 0x1: Address 8:4 bits for pattern LSB 0x2: Address 3:0 bits for pattern MSB 0x3: Address 8:4 bits for pattern MSB
28:25	DROOP_PATTERN_DATA	4 bits of pattern data for vddd_Krait droop pattern generator

SC_PLL1_DROOP_CTL (cont.)

Bits	Name	Description
24:23	RESET_CNT_TIMER_CFG	Reset counter timer configuration 0x0: Count 2049 cycles of input clock 0x1: Count 4097cycles of input clock 0x2: Count 8193 cycles of input clock 0x3: Count 16385 cycles of input clock
22	DROOP_DET_CLK_SEL	Clock select for droop detector 0x0: Use HF PLL clock 0x1: Use droop_clk_in
21:20	OUTPUT_SER_DATA_DIV	Clock divider control for output serialized data 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: RESERVED
19:18	DROOP_DET_CLK_DIV	Clock divider control for droop detection clock 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: RESERVED
17	ATEST_MODE	Atest mode for pulse generation circuit 0x0: Disable 0x1: Enable
16	BYPASS_MODE	Bypass mode for pulse generation circuit 0x0: Internally generated pulse control current 0x1: Bypass with external control current
15	PULSE_GENERATION	For controling pulse generation circuit 0x0: Disable 0x1: Enable
14:13	PULSE_WIDTH_CTL	Pulse width control 0x0: 140 ps 0x1: 270 ps 0x2: 390 ps 0x3: 470 ps
12:10	EXTERNAL_DROOP_CTL0	External droop control 0 0x0: No droop detected 0x7: Maximum droop detected
9:7	EXTERNAL_DROOP_CTL1	External droop control 1 0x0: No droop detected 0x7: Maximum droop detected
6	EXTERNAL_DROOP_DET0	External droop detect 0 0x0: No droop detected 0x1: Droop detected

SC_PLL1_DROOP_CTL (cont.)

Bits	Name	Description
24:23	RESET_CNT_TIMER_CFG	Reset counter timer configuration 0x0: Count 2049 cycles of input clock 0x1: Count 4097cycles of input clock 0x2: Count 8193 cycles of input clock 0x3: Count 16385 cycles of input clock
22	DROOP_DET_CLK_SEL	Clock select for droop detector 0x0: Use HF PLL clock 0x1: Use droop_clk_in
21:20	OUTPUT_SER_DATA_DIV	Clock divider control for output serialized data 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: RESERVED
19:18	DROOP_DET_CLK_DIV	Clock divider control for droop detection clock 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: RESERVED
17	ATEST_MODE	Atest mode for pulse generation circuit 0x0: Disable 0x1: Enable
16	BYPASS_MODE	Bypass mode for pulse generation circuit 0x0: Internally generated pulse control current 0x1: Bypass with external control current
15	PULSE_GENERATION	For controling pulse generation circuit 0x0: Disable 0x1: Enable
14:13	PULSE_WIDTH_CTL	Pulse width control 0x0: 140 ps 0x1: 270 ps 0x2: 390 ps 0x3: 470 ps
12:10	EXTERNAL_DROOP_CTL0	External droop control 0 0x0: No droop detected 0x7: Maximum droop detected
9:7	EXTERNAL_DROOP_CTL1	External droop control 1 0x0: No droop detected 0x7: Maximum droop detected
6	EXTERNAL_DROOP_DET0	External droop detect 0 0x0: No droop detected 0x1: Droop detected

SC_PLL1_DROOP_CTL (cont.)

Bits	Name	Description
5	EXTERNAL_DROOP_DET1	External droop detect 1 0x0: No droop detected 0x1: Droop detected
4	EXTERNAL_DROOP_CODE	Select external droop code, droop detect 0x0: Select external droop code 0 0x1: Select external droop code 1
3	DROOP_CODE_DETECT	Control external droop code, droop detect mode 0x0: Disable 0x1: Enable
2:1	DROOP_CONTROL_SE	Select output signal on droop_control_se lines For droop_test_se1, For droop_test_se2, 0x0: Pulse width control 0 0x1: Divided reference cloc_2 0x2: Inverter chain latching clock 0x3: Reference clock 0x0: Pulse width control 1 0x1: Pulse Generator output 0x2: Output from last stage in inverter chain 0x3: Serialized droop control output
0	OUTPUT_DRIVER	Output driver control on droop_control_se 0x0: Disable 0x1: Enable

0x00903258 SC_PLL1_TEST_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Test control register.

SC_PLL1_TEST_CTL

Bits	Name	Description
31:30	RESERVED_BITS_31_30	RESERVED
29	SLAVE_VCO_INJECTION	0x0: Slave VCO injection is disabled during droop 0x1: Slave VCO injection lock is always enabled
28	SYNC_MODE	0x0: Slave re-locking is synchronized 0x1: Slave re-locking is asynchronous
27:25	RESERVED_BITS_27_25	RESERVED

SC_PLL1_TEST_CTL (cont.)

Bits	Name	Description
24:23	NOISE_OSC_CTL_VDDD_SCORPION	Control for noise measurement oscillator on VDDD_SCORPION supply 0x0: Highest frequency of oscillation 0x1: 1/2 Highest frequency 0x2: 1/3 Highest frequency 0x3: 1/4 Highest frequency
22:20	NOISE_GEN_CFG_VDDA	VDDA Noise Generator configuration. Current sink in noise generator resistor dac, 0x0: 0 0x1: Max 2 mA 0x2: Max 4 mA 0x3: Max 6 mA 0x4: Max 8 mA 0x5: Max 10 mA 0x6: Max 12 mA 0x7: Max 14 mA
19	SUPPLY_NOISE_GEN	To control the supply noise generator circuit 0x0: Disable 0x1: Enable
18:17	NOISE_OSC_CTL_VDDA	Control for noise measurement oscillator on VDDA supply 0x0: Disable analog supply measurement oscillator 0x1: Slowest frequency of oscillation 0x2: Mid frequency of oscillation 0x3: Highest frequency of oscillation
16:15	CONNECT_PLL_LV_TEST	0x0: Connect PLL clock path to pllout_lv_test output 0x1: Connect vddd_scorpion supply noise measurement oscillator path to pllout_lv_test output 0x2: Connect analog supply noise measurement oscillator path to pllout_lv_test output 0x3: RESERVED
14	NOISE_OSC_EN	Used to control the noise measurement oscillator on VDDD_SCORPION supply 0x0: Disable 0x1: Enable
13	FILT_INT	0x0: Disconnect 0x1: Connect FILT_INT to test op amp input - observed on ATEST0
12	DTEST_MUX_SEL	Mux selectors for DTEST(note: set PLLTEST to enable DTEST) 0x0: Reserved 0x1: Select NOCLK
11	OUTPUT_INVERT	0x0: Disable 0x1: Enable

SC_PLL1_TEST_CTL (cont.)

Bits	Name	Description
10	PLLOUT_LV_TEST	0x0: Disable 0x1: Enable
9	PLLOUT_LV_AUX	0x0: Disable 0x1: Enable
8	PLLOUT_LV_BIST	0x0: Disable 0x1: Enable
7	PLLOUT_HV	0x0: Disable 0x1: Enable
6	VCO_CURRENT_ATEST0	Current flows from VDDA (should terminate to VSSA on board) 0x0: Open test switch 0x1: Enable VCO current div-16 output to ATEST0 pin
5	ICO_CURRENT_ATEST1	Current flows from AVDD (should terminate to AVSS on board) 0x0: Open test switch 0x1: Bypass ICO current with external input from ATEST1 pin to bias the cp
4	BIAS_CURRENT_ATEST1	Current flows from VDDA (should terminate to VSSA on Board) 0x0: Open test switch 0x1: Enable bias circuit current to ATEST1 pin
3	FILTER_TEST_OPAMP	0x0: Disable 0x1: Enable
2	SWITCH_ATEST0	0x0: Disabled 0x1: Enables switch to force external voltages from ATEST0
1	VREG_SLAVE_ATEST0	0x0: Disconnect 0x1: Connect VREG_SLAVE to test op amp input -observed on ATEST0
0	VREG_MST_ATEST0	0x0: Disconnect 0x1: Connect VREG_MST to test op amp input -observed on ATEST0

0x0090325C SC_PLL1_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Status register.

SC_PLL1_STATUS

Bits	Name	Description
31:16	RESERVED_BITS_31_16	RESERVED
15:0	PLL_STATUS	SC_PLL1_STATUS(15:6) : Unused, driven low (vssd domain) SC_PLL1_STATUS(5:2) : Over voltage counter status SC_PLL1_STATUS(1) : Over voltage detect flag SC_PLL1_STATUS(0) : Negated of no_clock (if clock is detected, output is high)

0x00903280 SC_PLL2_MODE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Mode register.

SC_PLL2_MODE

Bits	Name	Description
31:4	RESERVED_BITS_31_4	
3	PLLTEST	pll mode bits
2	RESET_N	pll mode bits
1	BYPASSNL	pll mode bits
0	OUTCTRL	pll mode bits

0x00903284 SC_PLL2_CONFIG_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x7805c665

PLL Config control register.

SC_PLL2_CONFIG_CTL

Bits	Name	Description
31:30	INJECTION_MODE	Injection Mode control for VCO 0x0: No caps on injection node 0x1: 18fF cap 0x2: 36fF cap 0x3: 54 fF cap

SC_PLL2_CONFIG_CTL (cont.)

Bits	Name	Description
29:28	WINDOW_SIZE	Window Size for phase detector used in injection locked VCO 0x0: 50ps window size 0x1: 67ps window size 0x2: 83ps window size 0x3: 100ps window size
27:26	LOCK_DET_CFG	Lock detection circuit configuration 0x0: Threshold = 2pi/7 0x1: Threshold = 2pi/15 0x2: Threshold = 2pi/23 0x3: Threshold = 2pi/31
25	MN_ACCUMULATOR	0x0: Disable MN accumulator 0x1: Enable MN accumulator
24:23	PRE_DIVIDE_RATIO	SC_PLL0_CONFIG_CTL(24) : Enable/ Disable for PLLOUT_LV_MASTER. SC_PLL0_CONFIG_CTL(23) : CLK_REF pre divide ratio 0x0: Disable 0x1: Enable 0x0: Predivide by 1 0x1: Predivide by 2
22	PLLOUT_EARLY	0x0: Disable PLLOUT_LV_EARLY 0x1: Enable PLLOUT_LV_EARLY
21	PLLOUT_MAIN	0x0: Disable PLLOUT_LV_MAIN 0x1: Enable PLLOUT_LV_MAIN
20:19	POST_DIVIDE_RATIO	Output clock post divide ratio 0x0: 1 0x1: 2 0x2: 4 0x3: Reserved
18:17	LEFT_SHIFT	Left shift operation configuration on droop control bits. Offset1, Offset0 bits are set using config_ctl[9:8]. Slave VCO Throttle control = 00 : {offset1, offset0, droopcontrol[2:0]} 01 : {offset1, droopcontrol[2:0], offset0} 10 : {droopcontrol[2:0], offset1, offset0} 0x3: Reserved
16:15	INJECTION_STRENGTH	Configure injection strength for slave VCO 0x0: 1/4th of Islave 0x1: 1/2 of Islave 0x2: 3/4 of Islave 0x3: Islave

SC_PLL2_CONFIG_CTL (cont.)

Bits	Name	Description
14	ISEED_GATING	0x0: Disable iseed gating 0x1: Enables no_clock signal to gate iseed current in the charge pump
13:12	SLAVE_VCO_DCAPS	Configure slave VCO dcaps 0x0: Default; 4pF + 187.5fFper unit L value 0x1: 4pF + 113fF per unit L value 0x2: 4pF + 62.5fF per unit L value 0x3: Fixed 4pF total cap
11:10	REGULATOR_BIAS	Regulator Bias current setting 0x0: 0.5 x Ivco/L 0x1: 1 x Ivco/L 0x2: 2 x Ivco/L 0x3: 4 x Ivco/L
9:8	DROOP_OFFSET	External droop offset to convert 3 bit TDC droop code to 5 bit regulator throttle 0x0: offset bits set to 00 0x1: offset bits set to 01 0x2: offset bits set to 10 0x3: offset bits set to 11
7:6	ANTI_DEAD_ZONE	Anti dead zone programmable input 0x0: 1 delay elements 0x1: 2 delay elements 0x2: 3 delay elements 0x3: 4 delay elements
5:4	ISEED_CTL	Iseed control for charge pump 0x0: 0.5 x Iseed 0x1: 1 x Iseed 0x2: 2 x Iseed 0x3: 4 x Iseed
3:2	CURRENT_MIRROR	Current mirror for charge pump current fixed divider ratio. Iout / Iin = 0x0: 1/ 2L 0x1: 1/L 0x2: 2/L 0x3: 4/L
1:0	DELTA_T	Setting for delay in reference path 0x0: 200ps 0x1: 400ps 0x2: 800 ps 0x3: 1200 ps

0x00903288 SC_PLL2_L_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL L Val register.

SC_PLL2_L_VAL

Bits	Name	Description
31:7	RESERVED_BITS_31_7	RESERVED
6:0	L_VAL	L value

0x0090328C SC_PLL2_M_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL M Val register.

SC_PLL2_M_VAL

Bits	Name	Description
31:19	RESERVED_BITS_31_19	RESERVED
18:0	M_VAL	M value

0x00903290 SC_PLL2_N_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL N Val register.

SC_PLL2_N_VAL

Bits	Name	Description
31:19	RESERVED_BITS_31_19	RESERVED
18:0	N_VAL	N value

0x00903294 SC_PLL2_DROOP_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0xc000

PLL Droop register.

SC_PLL2_DROOP_CTL

Bits	Name	Description
31	NOISE_PATTERN_SHIFT	Control pattern shifting operation in vddd_scorpion droop pattern generator 0x0: Disable 0x1: Enable
30:29	LOAD_ADDRESS	Load address for vddd_scorpion droop pattern generator 0x0: Address 3:0 bits for pattern LSB 0x1: Address 8:4 bits for pattern LSB 0x2: Address 3:0 bits for pattern MSB 0x3: Address 8:4 bits for pattern MSB
28:25	DROOP_PATTERN_DATA	4 bits of pattern data for vddd_scorpion droop pattern generator
24:23	RESET_CNT_TIMER_CFG	0x0: Count 2049 cycles of input clock 0x1: Count 4097cycles of input clock 0x2: Count 8193 cycles of input clock 0x3: Count 16385 cycles of input clock
22	DROOP_DET_CLK_SEL	Clock select for droop detector 0x0: Use HF PLL clock 0x1: Use droop_clk_in
21:20	OUTPUT_SER_DATA_DIV	Clock divider control for output serialized data 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: RESERVED
19:18	DROOP_DET_CLK_DIV	Clock divider control for droop detection clock 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: RESERVED
17	ATEST_MODE	Atest mode for pulse generation circuit 0x0: Disable 0x1: Enable
16	BYPASS_MODE	Bypass mode for pulse generation circuit 0x0: Internally generated pulse control current 0x1: Bypass with external control current

SC_PLL2_DROOP_CTL (cont.)

Bits	Name	Description
15	PULSE_GENERATION	For controling pulse generation circuit 0x0: Disable 0x1: Enable
14:13	PULSE_WIDTH_CTL	Pulse width control 0x0: 140 ps 0x1: 270 ps 0x2: 390 ps 0x3: 470 ps
12:10	EXTERNAL_DROOP_CTL0	External droop control 0 0x0: No droop detected 0x7: Maximum droop detected
9:7	EXTERNAL_DROOP_CTL1	External droop control 1 0x0: No droop detected 0x7: Maximum droop detected
6	EXTERNAL_DROOP_DET0	External droop detect 0 0x0: No droop detected 0x1: Droop detected
5	EXTERNAL_DROOP_DET1	External droop detect 1 0x0: No droop detected 0x1: Droop detected
4	EXTERNAL_DROOP_CODE	Select external droop code, droop detect 0x0: Select external droop code 0 0x1: Select external droop code 1
3	DROOP_CODE_DETECT	Control external droop code, droop detect mode 0x0: Disable 0x1: Enable
2:1	DROOP_CONTROL_SE	Select output signal on droop_control_se lines For droop_test_se1, For droop_test_se2, 0x0: Pulse width control 0 0x1: Divided reference clock 0x2: Inverter chain latching clock 0x3: Reference clock 0x0: Pulse width control 1 0x1: Pulse Generator output 0x2: Output from last stage in inverter chain 0x3: Serialized droop control output
0	OUTPUT_DRIVER	Output driver control on droop_control_se 0x0: Disable 0x1: Enable

0x00903298 SC_PLL2_TEST_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Test control register.

SC_PLL2_TEST_CTL

Bits	Name	Description
31:30	RESERVED_BITS_31_30	RESERVED
29	SLAVE_VCO_INJECTION	0x0: Slave VCO injection is disabled during droop 0x1: Slave VCO injection lock is always enabled
28	SYNC_MODE	0x0: Slave re-locking is synchronized 0x1: Slave re-locking is asynchronous
27:25	RESERVED_BITS_27_25	RESERVED
24:23	NOISE_OSC_CTL_VDDD_SCORPION	Control for noise measurement oscillator on VDDD_SCORPION supply 0x0: Highest frequency of oscillation 0x1: 1/2 Highest frequency 0x2: 1/3 Highest frequency 0x3: 1/4 Highest frequency
22:20	NOISE_GEN_CFG_VDDA	VDDA Noise Generator configuration. Current sink in noise generator resistor dac, 0x0: 0 0x1: Max 2 mA 0x2: Max 4 mA 0x3: Max 6 mA 0x4: Max 8 mA 0x5: Max 10 mA 0x6: Max 12 mA 0x7: Max 14 mA
19	SUPPLY_NOISE_GEN	To control the supply noise generator circuit 0x0: Disable 0x1: Enable
18:17	NOISE_OSC_CTL_VDDA	Control for noise measurement oscillator on VDDA supply 0x0: Disable analog supply measurement oscillator 0x1: Slowest frequency of oscillation 0x2: Mid frequency of oscillation 0x3: Highest frequency of oscillation

SC_PLL2_TEST_CTL (cont.)

Bits	Name	Description
16:15	CONNECT_PLL_LV_TEST	0x0: Connect PLL clock path to pllout_lv_test output 0x1: Connect vddd_scorpion supply noise measurement oscillator path to pllout_lv_test output 0x2: Connect analog supply noise measurement oscillator path to pllout_lv_test output 0x3: RESERVED
14	NOISE_OSC_EN	Used to control the noise measurement oscillator on VDDD_SCORPION supply. 0x0: Disable 0x1: Enable
13	FILT_INT	0x0: Disconnect 0x1: Connect FILT_INT to test op amp input - observed on ATEST0
12	DTEST_MUX_SEL	Mux selectors for DTEST(note: set PLLTEST to enable DTEST) 0x0: Reserved 0x1: Select NOCLK
11	OUTPUT_INVERT	0x0: Disable 0x1: Enable
10	PLLOUT_LV_TEST	0x0: Disable 0x1: Enable
9	PLLOUT_LV_AUX	0x0: Disable 0x1: Enable
8	PLLOUT_LV_BIST	0x0: Disable 0x1: Enable
7	PLLOUT_HV	0x0: Disable 0x1: Enable
6	VCO_CURRENT_ATEST0	Current flows from VDDA (should terminate to VSSA on board). 0x0: Open test switch 0x1: Enable VCO current div-16 output to ATEST0 pin
5	ICO_CURRENT_ATEST1	Current flows from AVDD (should terminate to AVSS on board). 0x0: Open test switch 0x1: Bypass ICO current with external input from ATEST1 pin to bias the cp
4	BIAS_CURRENT_ATEST1	Current flows from VDDA (should terminate to VSSA on Board). 0x0: Open test switch 0x1: Enable bias circuit current to ATEST1 pin
3	FILTER_TEST_OPAMP	0x0: Disable 0x1: Enable
2	SWITCH_ATEST0	0x0: Disabled 0x1: Enables switch to force external voltages from ATEST0

SC_PLL2_TEST_CTL (cont.)

Bits	Name	Description
1	VREG_SLAVE_ATEST0	0x0: Disconnect 0x1: Connect VREG_SLAVE to test op amp input -observed on ATEST0
0	VREG_MST_ATEST0	0x0: Disconnect 0x1: Connect VREG_MST to test op amp input -observed on ATEST0

0x0090329C SC_PLL2_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Status register.

SC_PLL2_STATUS

Bits	Name	Description
31:16	RESERVED_BITS_31_16	RESERVED
15:0	PLL_STATUS	SC_PLL2_STATUS(15:6) : Unused, driven low (vssd domain) SC_PLL2_STATUS(5:2) : Over voltage counter status SC_PLL2_STATUS(1) : Over voltage detect flag SC_PLL2_STATUS(0) : Negated of no_clock (if clock is detected, output is high)

0x009032C0 SC_PLL3_MODE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Mode register.

SC_PLL3_MODE

Bits	Name	Description
31:4	RESERVED_BITS_31_4	
3	PLLTEST	pll mode bits
2	RESET_N	pll mode bits
1	BYPASSNL	pll mode bits

SC_PLL3_MODE (cont.)

Bits	Name	Description
0	OUTCTRL	pll mode bits

0x009032C4 SC_PLL3_CONFIG_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x7805c665

PLL Config control register.

SC_PLL3_CONFIG_CTL

Bits	Name	Description
31:30	INJECTION_MODE	Injection Mode control for VCO. 0x0: No caps on injection node 0x1: 18fF cap 0x2: 36fF cap 0x3: 54 fF cap
29:28	WINDOW_SIZE	Window Size for phase detector used in injection locked VCO. 0x0: 50ps window size 0x1: 67ps window size 0x2: 83ps window size 0x3: 100ps window size
27:26	LOCK_DET_CFG	Lock detection circuit configuration. 0x0: Threshold = 2pi/7 0x1: Threshold = 2pi/15 0x2: Threshold = 2pi/23 0x3: Threshold = 2pi/31
25	MN_ACCUMULATOR	0x0: Disable MN accumulator 0x1: Enable MN accumulator
24:23	PRE_DIVIDE_RATIO	SC_PLL0_CONFIG_CTL(24) : Enable/ Disable for PLLOUT_LV_MASTER. SC_PLL0_CONFIG_CTL(23) : CLK_REF pre divide ratio 0x0: Disable 0x1: Enable 0x0: Predivide by 1 0x1: Predivide by 2
22	PLLOUT_EARLY	0x0: Disable PLLOUT_LV_EARLY 0x1: Enable PLLOUT_LV_EARLY
21	PLLOUT_MAIN	0x0: Disable PLLOUT_LV_MAIN 0x1: Enable PLLOUT_LV_MAIN

SC_PLL3_CONFIG_CTL (cont.)

Bits	Name	Description
20:19	POST_DIVIDE_RATIO	Output clock post divide ratio. 0x0: 1 0x1: 2 0x2: 4 0x3: Reserved
18:17	LEFT_SHIFT	Left shift operation configuration on droop control bits. Offset1, Offset0 bits are set using config_ctl[9:8]. Slave VCO Throttle control = 00 : {offset1, offset0, droopcontrol[2:0]} 01 : {offset1, droopcontrol[2:0], offset0} 10 : {droopcontrol[2:0], offset1, offset0} 0x3: Reserved
16:15	INJECTION_STRENGTH	Configure injection strength for slave VCO. 0x0: 1/4th of Islave 0x1: 1/2 of Islave 0x2: 3/4 of Islave 0x3: Islave
14	ISEED_GATING	0x0: Disable iseed gating 0x1: Enables no_clock signal to gate iseed current in the charge pump
13:12	SLAVE_VCO_DCAPS	Configure slave VCO dcaps 0x0: Default; 4pF + 187.5fFper unit L value 0x1: 4pF + 113fF per unit L value 0x2: 4pF + 62.5fF per unit L value 0x3: Fixed 4pF total cap
11:10	REGULATOR_BIAS	Regulator Bias current setting. 0x0: 0.5 x Ivco/L 0x1: 1 x Ivco/L 0x2: 2 x Ivco/L 0x3: 4 x Ivco/L
9:8	DROOP_OFFSET	External droop offset to convert 3 bit TDC droop code to 5 bit regulator throttle. 0x0: offset bits set to 00 0x1: offset bits set to 01 0x2: offset bits set to 10 0x3: offset bits set to 11
7:6	ANTI_DEAD_ZONE	Anti dead zone programmable input. 0x0: 1 delay elements 0x1: 2 delay elements 0x2: 3 delay elements 0x3: 4 delay elements

SC_PLL3_CONFIG_CTL (cont.)

Bits	Name	Description
5:4	ISEED_CTL	Iseed control for charge pump. 0x0: 0.5 x Iseed 0x1: 1 x Iseed 0x2: 2 x Iseed 0x3: 4 x Iseed
3:2	CURRENT_MIRROR	Current mirror for charge pump current fixed divider ratio. Iout / Iin = 0x0: 1/ 2L 0x1: 1/L 0x2: 2/L 0x3: 4/L
1:0	DELTA_T	Setting for delay in reference path 0x0: 200ps 0x1: 400ps 0x2: 800 ps 0x3: 1200 ps

0x009032C8 SC_PLL3_L_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL L Val register.

SC_PLL3_L_VAL

Bits	Name	Description
31:7	RESERVED_BITS_31_7	RESERVED
6:0	L_VAL	L value

0x009032CC SC_PLL3_M_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL M Val register.

SC_PLL3_M_VAL

Bits	Name	Description
31:19	RESERVED_BITS_31_19	RESERVED
18:0	M_VAL	M value

0x009032D0 SC_PLL3_N_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL N Val register.

SC_PLL3_N_VAL

Bits	Name	Description
31:19	RESERVED_BITS_31_19	RESERVED
18:0	N_VAL	N value

0x009032D4 SC_PLL3_DROOP_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0xc000

PLL Droop register.

SC_PLL3_DROOP_CTL

Bits	Name	Description
31	NOISE_PATTERN_SHIFT	Control pattern shifting operation in vddd_scorpion droop pattern generator 0x0: Disable 0x1: Enable
30:29	LOAD_ADDRESS	Load address for vddd_scorpion droop pattern generator 0x0: Address 3:0 bits for pattern LSB 0x1: Address 8:4 bits for pattern LSB 0x2: Address 3:0 bits for pattern MSB 0x3: Address 8:4 bits for pattern MSB
28:25	DROOP_PATTERN_DATA	4 bits of pattern data for vddd_scorpion droop pattern generator

SC_PLL3_DROOP_CTL (cont.)

Bits	Name	Description
24:23	RESET_CNT_TIMER_CFG	Reset counter timer configuration 0x0: Count 2049 cycles of input clock 0x1: Count 4097cycles of input clock 0x2: Count 8193 cycles of input clock 0x3: Count 16385 cycles of input clock
22	DROOP_DET_CLK_SEL	Clock select for droop detector 0x0: Use HF PLL clock 0x1: Use droop_clk_in
21:20	OUTPUT_SER_DATA_DIV	Clock divider control for output serialized data 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: RESERVED
19:18	DROOP_DET_CLK_DIV	Clock divider control for droop detection clock 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: RESERVED
17	ATEST_MODE	Atest mode for pulse generation circuit 0x0: Disable 0x1: Enable
16	BYPASS_MODE	Bypass mode for pulse generation circuit 0x0: Internally generated pulse control current 0x1: Bypass with external control current
15	PULSE_GENERATION	For controling pulse generation circuit 0x0: Disable 0x1: Enable
14:13	PULSE_WIDTH_CTL	Pulse width control 0x0: 140 ps 0x1: 270 ps 0x2: 390 ps 0x3: 470 ps
12:10	EXTERNAL_DROOP_CTL0	External droop control 0 0x0: No droop detected 0x7: Maximum droop detected
9:7	EXTERNAL_DROOP_CTL1	External droop control 1 0x0: No droop detected 0x7: Maximum droop detected
6	EXTERNAL_DROOP_DET0	External droop detect 0 0x0: No droop detected 0x1: Droop detected

SC_PLL3_DROOP_CTL (cont.)

Bits	Name	Description
5	EXTERNAL_DROOP_DET1	External droop detect 1 0x0: No droop detected 0x1: Droop detected
4	EXTERNAL_DROOP_CODE	Select external droop code, droop detect 0x0: Select external droop code 0 0x1: Select external droop code 1
3	DROOP_CODE_DETECT	Control external droop code, droop detect mode 0x0: Disable 0x1: Enable
2:1	DROOP_CONTROL_SE	Select output signal on droop_control_se lines For droop_test_se1, For droop_test_se2, 0x0: Pulse width control 0 0x1: Divided reference clock 0x2: Inverter chain latching clock 0x3: Reference clock 0x0: Pulse width control 1 0x1: Pulse Generator output 0x2: Output from last stage in inverter chain 0x3: Serialized droop control output
0	OUTPUT_DRIVER	Output driver control on droop_control_se 0x0: Disable 0x1: Enable

0x009032D8 SC_PLL3_TEST_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Test control register.

SC_PLL3_TEST_CTL

Bits	Name	Description
31:30	RESERVED_BITS_31_30	RESERVED
29	SLAVE_VCO_INJECTION	0x0: Slave VCO injection is disabled during droop 0x1: Slave VCO injection lock is always enabled
28	SYNC_MODE	0x0: Slave re-locking is synchronized 0x1: Slave re-locking is asynchronous
27:25	RESERVED_BITS_27_25	RESERVED

SC_PLL3_TEST_CTL (cont.)

Bits	Name	Description
24:23	NOISE_OSC_CTL_VDDD_SCORPION	Control for noise measurement oscillator on VDDD_SCORPION supply 0x0: Highest frequency of oscillation 0x1: 1/2 Highest frequency 0x2: 1/3 Highest frequency 0x3: 1/4 Highest frequency
22:20	NOISE_GEN_CFG_VDDA	VDDA Noise Generator configuration. Current sink in noise generator resistor dac, 0x0: 0 0x1: Max 2 mA 0x2: Max 4 mA 0x3: Max 6 mA 0x4: Max 8 mA 0x5: Max 10 mA 0x6: Max 12 mA 0x7: Max 14 mA
19	SUPPLY_NOISE_GEN	To control the supply noise generator circuit 0x0: Disable 0x1: Enable
18:17	NOISE_OSC_CTL_VDDA	Control for noise measurement oscillator on VDDA supply 0x0: Disable analog supply measurement oscillator 0x1: Slowest frequency of oscillation 0x2: Mid frequency of oscillation 0x3: Highest frequency of oscillation
16:15	CONNECT_PLL_LV_TEST	0x0: Connect PLL clock path to pllout_lv_test output 0x1: Connect vddd_scorpion supply noise measurement oscillator path to pllout_lv_test output 0x2: Connect analog supply noise measurement oscillator path to pllout_lv_test output 0x3: RESERVED
14	NOISE_OSC_EN	Used to control the noise measurement oscillator on VDDD_SCORPION supply 0x0: Disable 0x1: Enable
13	FILT_INT	0x0: Disconnect 0x1: Connect FILT_INT to test op amp input - observed on ATEST0
12	DTEST_MUX_SEL	Mux selectors for DTEST(note: set PLLTEST to enable DTEST) 0x0: Reserved 0x1: Select NOCLK
11	OUTPUT_INVERT	0x0: Disable 0x1: Enable

SC_PLL3_TEST_CTL (cont.)

Bits	Name	Description
10	PLLOUT_LV_TEST	0x0: Disable 0x1: Enable
9	PLLOUT_LV_AUX	0x0: Disable 0x1: Enable
8	PLLOUT_LV_BIST	0x0: Disable 0x1: Enable
7	PLLOUT_HV	0x0: Disable 0x1: Enable
6	VCO_CURRENT_ATEST0	Current flows from VDDA (should terminate to VSSA on board) 0x0: Open test switch 0x1: Enable VCO current div-16 output to ATEST0 pin
5	ICO_CURRENT_ATEST1	Current flows from AVDD (should terminate to AVSS on board) 0x0: Open test switch 0x1: Bypass ICO current with external input from ATEST1 pin to bias the cp
4	BIAS_CURRENT_ATEST1	Current flows from VDDA (should terminate to VSSA on Board) 0x0: Open test switch 0x1: Enable bias circuit current to ATEST1 pin
3	FILTER_TEST_OPAMP	0x0: Disable 0x1: Enable
2	SWITCH_ATEST0	0x0: Disabled 0x1: Enables switch to force external voltages from ATEST0
1	VREG_SLAVE_ATEST0	0x0: Disconnect 0x1: Connect VREG_SLAVE to test op amp input -observed on ATEST0
0	VREG_MST_ATEST0	0x0: Disconnect 0x1: Connect VREG_MST to test op amp input -observed on ATEST0

0x009032DC SC_PLL3_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Status register.

SC_PLL3_STATUS

Bits	Name	Description
31:16	RESERVED_BITS_31_16	RESERVED
15:0	PLL_STATUS	SC_PLL3_STATUS(15:6) : Unused, driven low (vssd domain) SC_PLL3_STATUS(5:2) : Over voltage counter status SC_PLL3_STATUS(1) : Over voltage detect flag SC_PLL3_STATUS(0) : Negated of no_clock (if clock is detected, output is high)

0x00903300 SC_L2_PLL_MODE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Mode register.

SC_L2_PLL_MODE

Bits	Name	Description
31:4	RESERVED_BITS_31_4	
3	PLLTEST	pll mode bits
2	RESET_N	pll mode bits
1	BYPASSNL	pll mode bits
0	OUTCTRL	pll mode bits

0x00903304 SC_L2_PLL_CONFIG_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x7805c665

PLL Config control register.

SC_L2_PLL_CONFIG_CTL

Bits	Name	Description
31:30	INJECTION_MODE	Injection Mode control for VCO 0x0: No caps on injection node 0x1: 18fF cap 0x2: 36fF cap 0x3: 54 fF cap

SC_L2_PLL_CONFIG_CTL (cont.)

Bits	Name	Description
29:28	WINDOW_SIZE	Window Size for phase detector used in injection locked VCO 0x0: 50ps window size 0x1: 67ps window size 0x2: 83ps window size 0x3: 100ps window size
27:26	LOCK_DET_CFG	Lock detection circuit configuration 0x0: Threshold = 2pi/7 0x1: Threshold = 2pi/15 0x2: Threshold = 2pi/23 0x3: Threshold = 2pi/31
25	MN_ACCUMULATOR	0x0: Disable MN accumulator 0x1: Enable MN accumulator
24:23	PRE_DIVIDE_RATIO	SC_PLL0_CONFIG_CTL(24) : Enable/ Disable for PLLOUT_LV_MASTER. SC_PLL0_CONFIG_CTL(23) : CLK_REF pre divide ratio 0x0: Disable 0x1: Enable 0x0: Predivide by 1 0x1: Predivide by 2
22	PLLOUT_EARLY	0x0: Disable PLLOUT_LV_EARLY 0x1: Enable PLLOUT_LV_EARLY
21	PLLOUT_MAIN	0x0: Disable PLLOUT_LV_MAIN 0x1: Enable PLLOUT_LV_MAIN
20:19	POST_DIVIDE_RATIO	Output clock post divide ratio 0x0: 1 0x1: 2 0x2: 4 0x3: Reserved
18:17	LEFT_SHIFT	Left shift operation configuration on droop control bits. Offset1, Offset0 bits are set using config_ctl[9:8]. Slave VCO Throttle control = 00 : {offset1, offset0, droopcontrol[2:0]} 01 : {offset1, droopcontrol[2:0], offset0} 10 : {droopcontrol[2:0], offset1, offset0} 0x3: Reserved
16:15	INJECTION_STRENGTH	Configure injection strength for slave VCO 0x0: 1/4th of Islave 0x1: 1/2 of Islave 0x2: 3/4 of Islave 0x3: Islave

SC_L2_PLL_CONFIG_CTL (cont.)

Bits	Name	Description
14	ISEED_GATING	0x0: Disable iseed gating 0x1: Enables no_clock signal to gate iseed current in the charge pump
13:12	SLAVE_VCO_DCAPS	Configure slave VCO dcaps 0x0: Default; 4pF + 187.5fFper unit L value 0x1: 4pF + 113fF per unit L value 0x2: 4pF + 62.5fF per unit L value 0x3: Fixed 4pF total cap
11:10	REGULATOR_BIAS	Regulator Bias current setting 0x0: 0.5 x Ivco/L 0x1: 1 x Ivco/L 0x2: 2 x Ivco/L 0x3: 4 x Ivco/L
9:8	DROOP_OFFSET	External droop offset to convert 3 bit TDC droop code to 5 bit regulator throttle 0x0: offset bits set to 00 0x1: offset bits set to 01 0x2: offset bits set to 10 0x3: offset bits set to 11
7:6	ANTI_DEAD_ZONE	Anti dead zone programmable input 0x0: 1 delay elements 0x1: 2 delay elements 0x2: 3 delay elements 0x3: 4 delay elements
5:4	ISEED_CTL	Iseed control for charge pump 0x0: 0.5 x Iseed 0x1: 1 x Iseed 0x2: 2 x Iseed 0x3: 4 x Iseed
3:2	CURRENT_MIRROR	Current mirror for charge pump current fixed divider ratio. Iout / Iin = 0x0: 1/ 2L 0x1: 1/L 0x2: 2/L 0x3: 4/L
1:0	DELTA_T	Setting for delay in reference path 0x0: 200ps 0x1: 400ps 0x2: 800 ps 0x3: 1200 ps

0x00903308 SC_L2_PLL_L_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL L Val register.

SC_L2_PLL_L_VAL

Bits	Name	Description
31:7	RESERVED_BITS_31_7	RESERVED
6:0	L_VAL	L value

0x0090330C SC_L2_PLL_M_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL M Val register.

SC_L2_PLL_M_VAL

Bits	Name	Description
31:19	RESERVED_BITS_31_19	RESERVED
18:0	M_VAL	M value

0x00903310 SC_L2_PLL_N_VAL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL N Val register.

SC_L2_PLL_N_VAL

Bits	Name	Description
31:19	RESERVED_BITS_31_19	RESERVED
18:0	N_VAL	N value

0x00903314 SC_L2_PLL_DROOP_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0xc000

PLL Droop register.

SC_L2_PLL_DROOP_CTL

Bits	Name	Description
31	NOISE_PATTERN_SHIFT	Control pattern shifting operation in vddd_scorpion droop pattern generator 0x0: Disable 0x1: Enable
30:29	LOAD_ADDRESS	Load address for vddd_scorpion droop pattern generator 0x0: Address 3:0 bits for pattern LSB 0x1: Address 8:4 bits for pattern LSB 0x2: Address 3:0 bits for pattern MSB 0x3: Address 8:4 bits for pattern MSB
28:25	DROOP_PATTERN_DATA	4 bits of pattern data for vddd_scorpion droop pattern generator
24:23	RESET_CNT_TIMER_CFG	Reset counter timer configuration 0x0: Count 2049 cycles of input clock 0x1: Count 4097cycles of input clock 0x2: Count 8193 cycles of input clock 0x3: Count 16385 cycles of input clock
22	DROOP_DET_CLK_SEL	Clock select for droop detector 0x0: Use HF PLL clock 0x1: Use droop_clk_in
21:20	OUTPUT_SER_DATA_DIV	Clock divider control for output serialized data 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: RESERVED
19:18	DROOP_DET_CLK_DIV	Clock divider control for droop detection clock 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: RESERVED
17	ATEST_MODE	Atest mode for pulse generation circuit 0x0: Disable 0x1: Enable
16	BYPASS_MODE	Bypass mode for pulse generation circuit 0x0: Internally generated pulse control current 0x1: Bypass with external control current

SC_L2_PLL_DROOP_CTL (cont.)

Bits	Name	Description
15	PULSE_GENERATION	For controling pulse generation circuit 0x0: Disable 0x1: Enable
14:13	PULSE_WIDTH_CTL	Pulse width control 0x0: 140 ps 0x1: 270 ps 0x2: 390 ps 0x3: 470 ps
12:10	EXTERNAL_DROOP_CTL0	External droop control 0 0x0: No droop detected 0x7: Maximum droop detected
9:7	EXTERNAL_DROOP_CTL1	External droop control 1 0x0: No droop detected 0x7: Maximum droop detected
6	EXTERNAL_DROOP_DET0	External droop detect 0 0x0: No droop detected 0x1: Droop detected
5	EXTERNAL_DROOP_DET1	External droop detect 1 0x0: No droop detected 0x1: Droop detected
4	EXTERNAL_DROOP_CODE	Select external droop code, droop detect 0x0: Select external droop code 0 0x1: Select external droop code 1
3	DROOP_CODE_DETECT	Control external droop code, droop detect mode 0x0: Disable 0x1: Enable
2:1	DROOP_CONTROL_SE	Select output signal on droop_control_se lines For droop_test_se1, For droop_test_se2, 0x0: Pulse width control 0 0x1: Divided reference clock 0x2: Inverter chain latching clock 0x3: Reference clock 0x0: Pulse width control 1 0x1: Pulse Generator output 0x2: Output from last stage in inverter chain 0x3: Serialized droop control output
0	OUTPUT_DRIVER	Output driver control on droop_control_se 0x0: Disable 0x1: Enable

0x00903318 SC_L2_PLL_TEST_CTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Test control register.

SC_L2_PLL_TEST_CTL

Bits	Name	Description
31:30	RESERVED_BITS_31_30	RESERVED
29	SLAVE_VCO_INJECTION	0x0: Slave VCO injection is disabled during droop 0x1: Slave VCO injection lock is always enabled
28	SYNC_MODE	0x0: Slave re-locking is synchronized 0x1: Slave re-locking is asynchronous
27:25	RESERVED_BITS_27_25	RESERVED
24:23	NOISE_OSC_CTL_VDDD_SCORPION	Control for noise measurement oscillator on VDDD_SCORPION supply 0x0: Highest frequency of oscillation 0x1: 1/2 Highest frequency 0x2: 1/3 Highest frequency 0x3: 1/4 Highest frequency
22:20	NOISE_GEN_CFG_VDDA	VDDA Noise Generator configuration. Current sink in noise generator resistor dac, 0x0: 0 0x1: Max 2 mA 0x2: Max 4 mA 0x3: Max 6 mA 0x4: Max 8 mA 0x5: Max 10 mA 0x6: Max 12 mA 0x7: Max 14 mA
19	SUPPLY_NOISE_GEN	To control the supply noise generator circuit 0x0: Disable 0x1: Enable
18:17	NOISE_OSC_CTL_VDDA	Control for noise measurement oscillator on VDDA supply 0x0: Disable analog supply measurement oscillator 0x1: Slowest frequency of oscillation 0x2: Mid frequency of oscillation 0x3: Highest frequency of oscillation

SC_L2_PLL_TEST_CTL (cont.)

Bits	Name	Description
16:15	CONNECT_PLL_LV_TEST	0x0: Connect PLL clock path to pllout_lv_test output 0x1: Connect vddd_scorpion supply noise measurement oscillator path to pllout_lv_test output 0x2: Connect analog supply noise measurement oscillator path to pllout_lv_test output 0x3: RESERVED
14	NOISE_OSC_EN	Used to control the noise measurement oscillator on VDDD_SCORPION supply 0x0: Disable 0x1: Enable
13	FILT_INT	0x0: Disconnect 0x1: Connect FILT_INT to test op amp input - observed on ATEST0
12	DTEST_MUX_SEL	Mux selectors for DTEST(note: set PLLTEST to enable DTEST) 0x0: Reserved 0x1: Select NOCLK
11	OUTPUT_INVERT	0x0: Disable 0x1: Enable
10	PLLOUT_LV_TEST	0x0: Disable 0x1: Enable
9	PLLOUT_LV_AUX	0x0: Disable 0x1: Enable
8	PLLOUT_LV_BIST	0x0: Disable 0x1: Enable
7	PLLOUT_HV	0x0: Disable 0x1: Enable
6	VCO_CURRENT_ATEST0	current flows from VDDA (should terminate to VSSA on board) 0x0: Open test switch 0x1: Enable VCO current div-16 output to ATEST0 pin
5	ICO_CURRENT_ATEST1	Current flows from AVDD (should terminate to AVSS on board) 0x0: Open test switch 0x1: Bypass ICO current with external input from ATEST1 pin to bias the cp
4	BIAS_CURRENT_ATEST1	Current flows from VDDA (should terminate to VSSA on Board) 0x0: Open test switch 0x1: Enable bias circuit current to ATEST1 pin
3	FILTER_TEST_OPAMP	0x0: Disable 0x1: Enable
2	SWITCH_ATEST0	0x0: Disabled 0x1: Enables switch to force external voltages from ATEST0

SC_L2_PLL_TEST_CTL (cont.)

Bits	Name	Description
1	VREG_SLAVE_ATEST0	0x0: Disconnect 0x1: Connect VREG_SLAVE to test op amp input -observed on ATEST0
0	VREG_MST_ATEST0	0x0: Disconnect 0x1: Connect VREG_MST to test op amp input -observed on ATEST0

0x0090331C SC_L2_PLL_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0000

PLL Status register.

SC_L2_PLL_STATUS

Bits	Name	Description
31:16	RESERVED_BITS_31_16	RESERVED
15:0	PLL_STATUS	SC_L2_PLL_STATUS(15:6) : Unused, driven low (vssd domain) SC_L2_PLL_STATUS(5:2) : Over voltage counter status SC_L2_PLL_STATUS(1) : Over voltage detect flag SC_L2_PLL_STATUS(0) : Negated of no_clock (if clock is detected, output is high)

0x00903420 PLL_LOCK_DET_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0000

PLL lock detect status register.

PLL_LOCK_DET_STATUS

Bits	Name	Description
31:18	RESERVED_BITS_31_18	RESERVED
17	PLL17_LOCK_DET	Pll17 lock detect status
16	PLL16_LOCK_DET	Pll16 lock detect status
15	PLL15_LOCK_DET	Pll15 lock detect status

PLL_LOCK_DET_STATUS (cont.)

Bits	Name	Description
14	PLL14_LOCK_DET	Pll14 lock detect status
13	PLL13_LOCK_DET	Pll13 lock detect status
12	PLL12_LOCK_DET	Pll12 lock detect status
11	PLL11_LOCK_DET	Pll11 lock detect status
10	PLL10_LOCK_DET	Pll10 lock detect status
9	PLL9_LOCK_DET	Pll9 lock detect status
8	PLL8_LOCK_DET	Pll8 lock detect status
7:6	RESERVED_BITS7_6	RESERVED
5	PLL5_LOCK_DET	Pll5 lock detect status
4	PLL4_LOCK_DET	Pll4 lock detect status
3	PLL3_LOCK_DET	Pll3 lock detect status
2	PLL2_LOCK_DET	Pll2 lock detect status
1	PLL1_LOCK_DET	Pll1 lock detect status
0	PLL0_LOCK_DET	Pll0 lock detect status

0x00903424 PLL_LOCK_DET_MASK

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000

PLL lock detect status register mask. This mask can be set to selectively export a combined PLL lock detection status. This combined PLL lock detection status is intended to be used during manufacturing testing. The combined status is not viewable through the software interface.

Setting a bit to 1'b1 will enable the real time monitoring of the corresponding PLL's lock detect status.

NOTE This register’s reset value of 0x0 must be adjusted before use. The reset value of 0x0 indicates the LOCK_DET status for ALL PLLs are ignored, and thus the combined PLL lock detect output will report that all PLLs are locked.

PLL_LOCK_DET_MASK

Bits	Name	Description
31:18	RESERVED_BITS_31_18	RESERVED
17	PLL17_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored

PLL_LOCK_DET_MASK (cont.)

Bits	Name	Description
16	PLL16_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
15	PLL15_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
14	PLL14_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
13	PLL13_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
12	PLL12_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
11	PLL11_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
10	PLL10_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
9	PLL9_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
8	PLL8_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
7:6	RESERVED_BITS7_6	RESERVED
5	PLL5_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
4	PLL4_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
3	PLL3_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
2	PLL2_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
1	PLL1_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored
0	PLL0_LOCK_DET	0x0: lock detect status ignored 0x1: lock detect status monitored

0x00903460 PLL_ENA_SPARE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register allows a spare entity to enable a limited set of shared PLLs without incurring any messaging overhead with the RPM. The PLLs are programmed to a static frequency and setting a bit in this register only enables or disables the PLL to run at that predetermined static frequency.

Enabling the PLL starts off the automated FSM which paces the PLL through the warmup routine. The FSM status bits, located in the PLLn_MODE registers, for each PLL featuring automatic enables should be consulted to determine if the PLL is locked and running.

PLL_ENA_SPARE

Bits	Name	Description
31:15	RESERVED_BITS31_15	RESERVED
14	PLL14	Enable for PLL14 0x0: PLL not required and disabled 0x1: PLL required and enabled
13:9	RESERVED_BITS13_9	RESERVED
8	PLL8	Enable for PLL8 0x0: PLL not required and disabled 0x1: PLL required and enabled
7:6	RESERVED_BITS7_6	RESERVED
5	PLL5	Enable for PLL5 0x0: PLL not required and disabled 0x1: PLL required and enabled
4	PLL4	Enable for PLL4 0x0: PLL not required and disabled 0x1: PLL required and enabled
3	PLL3	Enable for PLL3 0x0: PLL not required and disabled 0x1: PLL required and enabled
2:1	RESERVED_BITS2_1	RESERVED
0	PLL0	Enable for PLL0 0x0: PLL not required and disabled 0x1: PLL required and enabled

0x00903480 PLL_ENA_GSS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register allows the GPS Subsystem to enable a limited set of shared PLLs without incurring any messaging overhead with the RPM. The PLLs are programmed to a static frequency and setting a bit in this register only enables or disables the PLL to run at that predetermined static frequency.

Enabling the PLL starts off the automated FSM which paces the PLL through the warmup routine. The FSM status bits, located in the PLLn_MODE registers, for each PLL featuring automatic enables should be consulted to determine if the PLL is locked and running.

PLL_ENA_GSS

Bits	Name	Description
31:15	RESERVED_BITS31_15	RESERVED
14	PLL14	Enable for PLL14 0x0: PLL not required and disabled 0x1: PLL required and enabled
13:9	RESERVED_BITS13_9	RESERVED
8	PLL8	Enable for PLL8 0x0: PLL not required and disabled 0x1: PLL required and enabled
7:6	RESERVED_BITS7_6	RESERVED
5	PLL5	Enable for PLL5 0x0: PLL not required and disabled 0x1: PLL required and enabled
4	PLL4	Enable for PLL4 0x0: PLL not required and disabled 0x1: PLL required and enabled
3	PLL3	Enable for PLL3 0x0: PLL not required and disabled 0x1: PLL required and enabled
2:1	RESERVED_BITS2_1	RESERVED
0	PLL0	Enable for PLL0 0x0: PLL not required and disabled 0x1: PLL required and enabled

0x009034A0 PLL_ENA_RPM

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register allows the RPM to enable a limited set of shared PLLs without incurring any messaging overhead with the RPM. The PLLs are programmed to a static frequency and setting a bit in this register only enables or disables the PLL to run at that predetermined static frequency.

Enabling the PLL starts off the automated FSM which paces the PLL through the warmup routine. The FSM status bits, located in the PLLn_MODE registers, for each PLL featuring automatic enables should be consulted to determine if the PLL is locked and running.

PLL_ENA_RPM

Bits	Name	Description
31:15	RESERVED_BITS31_15	RESERVED
14	PLL14	Enable for PLL14 0x0: PLL not required and disabled 0x1: PLL required and enabled
13:9	RESERVED_BITS13_9	RESERVED
8	PLL8	Enable for PLL8 0x0: PLL not required and disabled 0x1: PLL required and enabled
7:6	RESERVED_BITS7_6	RESERVED
5	PLL5	Enable for PLL5 0x0: PLL not required and disabled 0x1: PLL required and enabled
4	PLL4	Enable for PLL4 0x0: PLL not required and disabled 0x1: PLL required and enabled
3	PLL3	Enable for PLL3 0x0: PLL not required and disabled 0x1: PLL required and enabled
2:1	RESERVED_BITS2_1	RESERVED
0	PLL0	Enable for PLL0 0x0: PLL not required and disabled 0x1: PLL required and enabled

0x009034C0 PLL_ENA_APCS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register allows the Scorpion Core 0 to enable a limited set of shared PLLs without incurring any messaging overhead with the RPM. The PLLs are programmed to a static frequency and setting a bit in this register only enables or disables the PLL to run at that predetermined static frequency.

Enabling the PLL starts off the automated FSM which paces the PLL through the warmup routine. The FSM status bits, located in the PLLn_MODE registers, for each PLL featuring automatic enables should be consulted to determine if the PLL is locked and running.

PLL_ENA_APCS

Bits	Name	Description
31:15	RESERVED_BITS31_15	RESERVED
14	PLL14	Enable for PLL14 0x0: PLL not required and disabled 0x1: PLL required and enabled
13:9	RESERVED_BITS13_9	RESERVED
8	PLL8	Enable for PLL8 0x0: PLL not required and disabled 0x1: PLL required and enabled
7:6	RESERVED_BITS7_6	RESERVED
5	PLL5	Enable for PLL5 0x0: PLL not required and disabled 0x1: PLL required and enabled
4	PLL4	Enable for PLL4 0x0: PLL not required and disabled 0x1: PLL required and enabled
3	PLL3	Enable for PLL3 0x0: PLL not required and disabled 0x1: PLL required and enabled
2:1	RESERVED_BITS2_1	RESERVED
0	PLL0	Enable for PLL0 0x0: PLL not required and disabled 0x1: PLL required and enabled

0x009034E0 PLL_ENA_APCS_U

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register allows the Scorpion Core 1 to enable a limited set of shared PLLs without incurring any messaging overhead with the RPM. The PLLs are programmed to a static frequency and setting a bit in this register only enables or disables the PLL to run at that predetermined static frequency.

Enabling the PLL starts off the automated FSM which paces the PLL through the warmup routine. The FSM status bits, located in the PLLn_MODE registers, for each PLL featuring automatic enables should be consulted to determine if the PLL is locked and running.

PLL_ENA_APCS_U

Bits	Name	Description
31:15	RESERVED_BITS31_15	RESERVED
14	PLL14	Enable for PLL14 0x0: PLL not required and disabled 0x1: PLL required and enabled
13:9	RESERVED_BITS13_9	RESERVED
8	PLL8	Enable for PLL8 0x0: PLL not required and disabled 0x1: PLL required and enabled
7:6	RESERVED_BITS7_6	RESERVED
5	PLL5	Enable for PLL5 0x0: PLL not required and disabled 0x1: PLL required and enabled
4	PLL4	Enable for PLL4 0x0: PLL not required and disabled 0x1: PLL required and enabled
3	PLL3	Enable for PLL3 0x0: PLL not required and disabled 0x1: PLL required and enabled
2:1	RESERVED_BITS2_1	RESERVED
0	PLL0	Enable for PLL0 0x0: PLL not required and disabled 0x1: PLL required and enabled

0x00903500 PLL_ENA_RIVA

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register allows the Riva processor to enable a limited set of shared PLLs without incurring any messaging overhead with the RPM. The PLLs are programmed to a static frequency and setting a bit in this register only enables or disables the PLL to run at that predetermined static frequency.

Enabling the PLL starts off the automated FSM which paces the PLL through the warmup routine. The FSM status bits, located in the PLLn_MODE registers, for each PLL featuring automatic enables should be consulted to determine if the PLL is locked and running.

PLL_ENA_RIVA

Bits	Name	Description
31:15	RESERVED_BITS31_15	RESERVED
14	PLL14	Enable for PLL14 0x0: PLL not required and disabled 0x1: PLL required and enabled
13:9	RESERVED_BITS13_9	RESERVED
8	PLL8	Enable for PLL8 0x0: PLL not required and disabled 0x1: PLL required and enabled
7:6	RESERVED_BITS7_6	RESERVED
5	PLL5	Enable for PLL5 0x0: PLL not required and disabled 0x1: PLL required and enabled
4	PLL4	Enable for PLL4 0x0: PLL not required and disabled 0x1: PLL required and enabled
3	PLL3	Enable for PLL3 0x0: PLL not required and disabled 0x1: PLL required and enabled
2:1	RESERVED_BITS2_1	RESERVED
0	PLL0	Enable for PLL0 0x0: PLL not required and disabled 0x1: PLL required and enabled

0x00903520 PLL_ENA_LPASS_DSP

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register allows the LPASS DSP to enable a limited set of shared PLLs without incurring any messaging overhead with the RPM. The PLLs are programmed to a static frequency and setting a bit in this register only enables or disables the PLL to run at that predetermined static frequency.

Enabling the PLL starts off the automated FSM which paces the PLL through the warmup routine. The FSM status bits, located in the PLLn_MODE registers, for each PLL featuring automatic enables should be consulted to determine if the PLL is locked and running.

PLL_ENA_LPASS_DSP

Bits	Name	Description
31:15	RESERVED_BITS31_15	RESERVED
14	PLL14	Enable for PLL14 0x0: PLL not required and disabled 0x1: PLL required and enabled
13:9	RESERVED_BITS13_9	RESERVED
8	PLL8	Enable for PLL8 0x0: PLL not required and disabled 0x1: PLL required and enabled
7:6	RESERVED_BITS7_6	RESERVED
5	PLL5	Enable for PLL5 0x0: PLL not required and disabled 0x1: PLL required and enabled
4	PLL4	Enable for PLL4 0x0: PLL not required and disabled 0x1: PLL required and enabled
3	PLL3	Enable for PLL3 0x0: PLL not required and disabled 0x1: PLL required and enabled
2:1	RESERVED_BITS2_1	RESERVED
0	PLL0	Enable for PLL0 0x0: PLL not required and disabled 0x1: PLL required and enabled

0x00903540 PLL_ENA_SPS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register allows the Smart Peripheral SubSystem to enable a limited set of shared PLLs without incurring any messaging overhead with the RPM. The PLLs are programmed to a static frequency and setting a bit in this register only enables or disables the PLL to run at that predetermined static frequency.

Enabling the PLL starts off the automated FSM which paces the PLL through the warmup routine. The FSM status bits, located in the PLLn_MODE registers, for each PLL featuring automatic enables should be consulted to determine if the PLL is locked and running.

PLL_ENA_SPS

Bits	Name	Description
31:15	RESERVED_BITS31_15	RESERVED
14	PLL14	Enable for PLL14 0x0: PLL not required and disabled 0x1: PLL required and enabled
13:9	RESERVED_BITS13_9	RESERVED
8	PLL8	Enable for PLL8 0x0: PLL not required and disabled 0x1: PLL required and enabled
7:6	RESERVED_BITS7_6	RESERVED
5	PLL5	Enable for PLL5 0x0: PLL not required and disabled 0x1: PLL required and enabled
4	PLL4	Enable for PLL4 0x0: PLL not required and disabled 0x1: PLL required and enabled
3	PLL3	Enable for PLL3 0x0: PLL not required and disabled 0x1: PLL required and enabled
2:1	RESERVED_BITS2_1	RESERVED
0	PLL0	Enable for PLL0 0x0: PLL not required and disabled 0x1: PLL required and enabled

0x00903560 FABS_RESET

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

Reset for all the MMSS Fab.

FABS_RESET

Bits	Name	Description
31:4	RESERVED_BITS31_4	
3	DFAB_CORE_ASYNC_RESET	Async reset for Smart Peripheral Subsystem fabric core clock domain 0x1: Active. 0x0: Not Active

FABS_RESET (cont.)

Bits	Name	Description
2	SFAB_CORE_ASYNC_RESET	Async reset for System fabric core clock domain 0x1: Active 0x0: Not Active
1	AFAB_CORE_ASYNC_RESET	Async reset for Apps. fabric core clock domain 0x1: Active 0x0: Not Active
0	MMSS_ASYNC_RESET	Async reset for MMSS 0x1: Active. 0x0: Not Active

0x009035E0 RIVA_RESET

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

RIVA reset register.

RIVA_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	ASYNC_RESET	Async reset for RIVA 0x1: Active. 0x0: Not Active

0x00903600 XPU_RESET

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

Reset for all the XPUs

XPU_RESET

Bits	Name	Description
31:18	RESERVED_BITS31_18	RESERVED
17	CFPB2_ASYNC_RESET	Async reset for the CFPB2 AHB clock domain. 0x1: Active 0x0: Not Active

XPU_RESET (cont.)

Bits	Name	Description
16	CFPB1_ASYNC_RESET	Async reset for the CFPB1 AHB clock domain. 0x1: Active 0x0: Not Active
15	CFPB0_ASYNC_RESET	Async reset for the CFPB0 AHB clock domain. 0x1: Active 0x0: Not Active
14	SCSS_SYS_POR_ASYNC_RESET	Software reset for Scorpion system wide POR. 0x1: Active
13	SCSS_SYS_ASYNC_RESET	Software reset for Scorpion system wide warm reset. 0x1: Active
12	CFPB_SPLITTER_ASYNC_RESET	Async reset for CFPB splitter AHB clock domain 0x1: Active 0x0: Not Active.
11	CFPB_MASTER_ASYNC_RESET	Async reset for CFPB master AHB clock domain 0x1: Active 0x0: Not Active
10	PMIC_ARB1_ASYNC_RESET	Async reset for PMIC_ARB1 AHB clock domain 0x1: Active 0x0: Not Active
9	PMIC_ARB0_ASYNC_RESET	Async reset for PMIC_ARB0 AHB clock domain 0x1: Active 0x0: Not Active
8	RPM_BUS_ASYNC_RESET	Async reset for RPM BUS AHB clock domain 0x1: Active 0x0: Not Active
7	RPM_MSG_RAM_ASYNC_RESET	Async reset for RPM_MSG_RAM AHB clock domain 0x1: Active 0x0: Not Active
6	PMEM_ASYNC_RESET	Async reset for PME AXI clock domain 0x1: Active 0x0: Not Active
5	SIC_ASYNC_RESET	Async reset for SIC AHB clock domain 0x1: Active 0x0: Not Active
4	TLMM_ASYNC_RESET	Async reset for the TLMM clock domain. 0x1: Active 0x0: Not Active
3	MMSS_SMMU_ASYNC_RESET	Async reset for MMSS SMMU 0x1: Active. 0x0: Not Active

XPU_RESET (cont.)

Bits	Name	Description
2	MMSS_IMEM_ASYNC_RESET	Async reset for MMSS Imem 0x1: Active. 0x0: Not Active
1	IMEM0_ASYNC_RESET	Async reset for Imem0 0x1: Active. 0x0: Not Active
0	GLOBAL_XPU_ASYNC_RESET	Async reset for all the XPUs in the chip 0x1: Active. 0x0: Not Active

0x00903620 TSENS_CNTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

TSENS control register.

TSENS_CNTL

Bits	Name	Description
31:27	RESERVED_BITS31_27	RESERVED
26	TSENS_SLP_CLK_ENA	Enable to tsens slp clock 0x1: Enable
25:18	MEASURE_PERIOD	Periodic Temperature measurement period
17:14	RESERVED_BITS17_14	RESERVED
13	SENSOR10_EN	Remote temperature sensor 10 enable 0x0: Disabled 0x1: Enabled
12	SENSOR9_EN	Remote temperature sensor 9 enable 0x0: Disabled 0x1: Enabled
11	SENSOR8_EN	Remote temperature sensor 8 enable 0x0: Disabled 0x1: Enabled
10	SENSOR7_EN	Remote temperature sensor 7 enable 0x0: Disabled 0x1: Enabled

TSENS_CNTL (cont.)

Bits	Name	Description
9	SENSOR6_EN	Remote temperature sensor 6 enable 0x0: Disabled 0x1: Enabled
8	SENSOR5_EN	Remote temperature sensor 5 enable 0x0: Disabled 0x1: Enabled
7	SENSOR4_EN	Remote temperature sensor 4 enable 0x0: Disabled 0x1: Enabled
6	SENSOR3_EN	Remote temperature sensor 3 enable 0x0: Disabled 0x1: Enabled
5	SENSOR2_EN	Remote temperature sensor 2 enable 0x0: Disabled 0x1: Enabled
4	SENSOR1_EN	Remote temperature sensor 1 enable 0x0: Disabled 0x1: Enabled
3	SENSOR0_EN	Remote temperature sensor 0 enable (this is the central temperature sensor) 0x0: Disabled 0x1: Enabled
2	TSENS_ADC_CLK_SEL	ADC clock select 0x0: Internal oscillator 0x1: External clock source
1	SENS_SW_RST	Software reset bit 0x0: Reset de-asserted 0x1: Reset asserted
0	TSENS_EN	Temperature sensor monitoring enable 0x0: Disabled (default) 0x1: Enabled

0x00903624 TSENS_THRESHOLD

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

TSENS Limit Value register.

TSENS_THRESHOLD

Bits	Name	Description
31:24	MAX_LIMIT_TH	The Max temperature limit threshold is calculated with the following equation: 0000 0000 = -57.17C 1110 1111 = +125.02C 1111 1111 = +137.22C
23:16	MIN_LIMIT_TH	The Min temperature limit threshold is calculated with the following equation: 0001 0111 = -39.64C 0x0: -57.17C 0xFF: +137.22C
15:8	UPPER_LIMIT_TH	The Upper temperature limit threshold is calculated with the following equation: 0000 0000 = -57.17C 1100 1110 = +99.86C 1111 1111 = +137.22C
7:0	LOWER_LIMIT_TH	The Lower temperature threshold is calculated with the following equation: 0000 0000 = -57.17C 0011 0000 = -20.58C 1111 1111 = +137.22C

0x00903628 TSENS_S0_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

TSENS_S0_Status register.

TSENS_S0_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	LAST_TEMP0	The last temperature measured is calculated with the following equation: 0x0: -57.17C 0xFF: +137.22C

0x0090362C TSENS_S1_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

TSENS_S1_Status register.

TSENS_S1_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	LAST_TEMP1	The last temperature measured is calculated with the following equation: 0x0: -57.17C 0xFF: +137.22C

0x00903630 TSENS_S2_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

TSENS_S2_Status register.

TSENS_S2_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	LAST_TEMP2	The last temperature measured is calculated with the following equation: 0x0: -57.17C 0xFF: +137.22C

0x00903634 TSENS_S3_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

TSENS_S3_Status register.

TSENS_S3_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	LAST_TEMP3	The last temperature measured is calculated with the following equation: 0x0: -57.17C 0xFF: +137.22C

0x00903638 TSENS_S4_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

TSENS_S0_Status register.

TSENS_S4_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	LAST_TEMP4	The last temperature measured is calculated with the following equation: 0x0: -57.17C 0xFF: +137.22C

0x0090363C TSENS_INT_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

TSENS_INT_Status register.

TSENS_INT_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	TRDY	Temperature measurement is complete and temperature values are stored in LAST_TEMP[4:0] 0x0: Temperature measurement is not valid (default) 0x1: Last temperature reading is stored in LAST_TEMP[4:0]
6:4	RESERVED_BITS6_4	RESERVED

TSENS_INT_STATUS (cont.)

Bits	Name	Description
3	MAX_INT	Temperature in higher than MAX_LIMIT_TH 0x0: Temperature is lower than MAX_LIMIT_TH (default) 0x1: Temperature is equal to or higher than MAX_LIMIT_TH
2	UPPER_INT	Temperature is higher than UPPER_LIMIT_TH 0x0: Temperature is lower than UPPER_LIMIT_TH (default) 0x1: Temperature is higher than UPPER_LIMIT_TH but lower than MAX_LIM_TH
1	LOWER_INT	Temperature is lower than LOWER_LIMIT_TH 0x0: Temperature is higher than LOWER_LIMIT_TH (default) 0x1: Temperature is lower than LOWER_LIMIT_TH but higher than MIN_LIMIT_TH
0	MIN_INT	Temperature in lower than MIN_LIMIT_TH 0x0: Temperature is higher than MIN_LIMIT_TH (default) 0x1: Temperature is equal to or lower than MIN_LIMIT_TH

0x00903640 TSENS_CONFIG

Type: Read
Clock: SFPB_HCLK
Reset State: 0x9B

TSENS_CONFIG is used for fine tuning central sensor current magnitude.

TSENS_CONFIG

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	TSENS_CONFIG	Tsens config: [7:6] control internal clock frequency. [5:3] control Iref magnitude. [2:0] control Iin.

0x00903644 TSENS_TEST_CNTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

TSENS control register for test related functions

TSENS_TEST_CNTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	TSENS_TEST_SEL	Used for muxing out appropriate current or voltage to tsens_test_out in test mode. When TSENS_TEST_EN is '1', tsens_test_out gets, When TSENS_TEST_EN = 0, TSENS_TEST_SEL(3:0) is don't care and tsens_test_out is in Hi-Z state 0x0: Vref of Sensor 0 0x1: Iptat of Sensor 0 0x2: Ictat of Sensor 0 0x3: Iin of Sensor 0 (controlled by TSENS_CONFIG to change slope) 0x4: Iin of Sensor 1 0x5: Iin of Sensor 2 0x6: Iin of Sensor 3 0x7: Iin of Sensor 4 0x8: Iin of Sensor 5 0x9: Iin of Sensor 6 0xA: Iin of Sensor 7 0xB: Iin of Sensor 8 0xC: Iin of Sensor 9 0xD: Iin of Sensor 10
3:2	RESERVED_BITS3_2	RESERVED
1	TSENS_TEST_EN	Test enable 0x0: Test disabled (default) 0x1: Test enabled
0	TSENS_ADC_TEST_SEL	ADC test select 0x0: ADC uses temperature sensor outputs (default) 0x1: ADC uses analog test input signals

0x00903660 TSENS_STATUS_CNTL

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

TSENS control register.

TSENS_STATUS_CNTL

Bits	Name	Description
31:4	RESERVED_BITS31_4	

TSENS_STATUS_CNTL (cont.)

Bits	Name	Description
3	TSENS_MAX_STATUS_MASK	MASK MAX status to PSHOLD 0x0: Normal operation 0x1: Mask off Max interrupt operation to PSHOLD
2	TSENS_UPPER_STATUS_CLR	Clear UPPER_INT status bit 0x0: Normal operation 0x1: Clear (logic 0 UPPER_INT bit in the TSENS_INT_STATUS register)
1	TSENS_LOWER_STATUS_CLR	Clear LOWER_INT status bit 0x0: Normal operation 0x1: Clear (logic 0 LOWER_INT bit in the TSENS_INT_STATUS register)
0	TSENS_MIN_STATUS_MASK	MASK MIN status to PSHOLD 0x0: Normal operation 0x1: Mask off Min interrupt operation to PSHOLD

0x00903664 TSENS_S5_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

TSENS_S5_Status register.

TSENS_S5_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	LAST_TEMP5	The last temperature measured is calculated with the following equation: 0x0: -57.17C 0xFF: +137.22C

0x00903668 TSENS_S6_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

TSENS_S6_Status register.

TSENS_S6_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	LAST_TEMP6	The last temperature measured is calculated with the following equation: 0x0: -57.17C 0xFF: +137.22C

0x0090366C TSENS_S7_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

TSENS_S7_Status register.

TSENS_S7_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	LAST_TEMP7	The last temperature measured is calculated with the following equation: 0x0: -57.17C 0xFF: +137.22C

0x00903670 TSENS_S8_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

TSENS_S8_Status register.

TSENS_S8_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	LAST_TEMP8	The last temperature measured is calculated with the following equation: 0x0: -57.17C 0xFF: +137.22C

0x00903674 TSENS_S9_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

TSENS_S9_Status register.

TSENS_S9_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	LAST_TEMP9	The last temperature measured is calculated with the following equation: 0x0: -57.17C 0xFF: +137.22C

0x00903678 TSENS_S10_STATUS

Type: Read
Clock: SFPB_HCLK
Reset State: 0x0

TSENS_S10_Status register.

TSENS_S10_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	LAST_TEMP9	The last temperature measured is calculated with the following equation: 0x0: -57.17C 0xFF: +137.22C

0x009036C0 CE3_CLK_SRC_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the the generation of ce3_clk_src. It provides root enable, clock source divide control and clock source selection control.

CE3_CLK_SRC_NS

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	CLK_ROOT_ENA	Enable ce3_clk clock source 0x1: Enable 0x0: Disable
6:3	SRC_DIV	This field selects to activate or bypass the modulo divider. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: pll14 0x2: pll0 0x3: pll8 0x4: gnd 0x5: pll11 0x6: pll3 0x7: core_bi_pll_test_se

0x009036C4 CE3_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock for the Crypto engine 3. It provides enable and clock inversion to the branch, software control to the reset of logic clocked by this clock domain and also contains enable for the dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

CE3_HCLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for CE3 AHB clock domain. 0x1: Active 0x0: Not Active
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. (This feature is for future usage only. Setting this bit will have the same effect of enabling the clock.) 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert ce2_hclk 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for ce2_hclk clock branch 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009036C8 CE3_SFAB_PORT_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides software control to the system fabric ports connecting to CE3.

CE3_SFAB_PORT_RESET

Bits	Name	Description
31:2	RESERVED_BITS31_2	RESERVED
1	SFAB_CE3_M_RESET	Async reset for System fabric master port connecting to CE3. 0x1: Active 0x0: Not Active
0	SFAB_CE3_S_RESET	Software reset for System fabric slave port connecting to CE3. 0x1: Active

0x009036CC CE3_CORE_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of core clock for the Crypto engine 3 on the System FABRIC. It provides enable, clock inversion to the branch and software control to the reset of logic clocked by this clock domain.

CE3_CORE_CLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7	ASYNC_RESET	Async reset for CE3 core clock domain 0x1: Active 0x0: Not Active
6	BUS_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert ce3_core_clk 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for ce3_core_clk clock branch 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009036D0 CE3_SLEEP_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control the clock branch for the generation of cc_ce3_sleep_clk. It provides enable and clock inversion to the branch, and software control to the reset of logic clocked by this clock domain.

CE3_SLEEP_CLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED

CE3_SLEEP_CLK_CTL (cont.)

Bits	Name	Description
7	ASYNC_RESET	Async reset for CE3 sleep clock domain. 0x1: Active 0x0: Not Active
6	RESERVED_BIT6	RESERVED
5	CLK_INV	This bit is used to invert ce3_sleep_clk 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for ce3_sleep_clk clock branch This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x009036E0 SFAB_AHB_S8_FCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the branch cell used to generate the fabric clock for the system fabric AHB slave port 8 (cc_sfab_ahb_s8_fclk). It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When fabric dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

SFAB_AHB_S8_FCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert sfab_ahb_s7_fclk 0x1: invert 0x0: Not inver
4	CLK_BRANCH_ENA	Enable for sfab_ahb_s7_fclk clock branch This clock is votable 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00903700 USB_HS3_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock (cc_USB_HS3_hclk) for the USB_HS3 core. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

USB_HS3_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert usb_hs3_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for usb_hs3_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00903704 USB_HS3_HCLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for USB high speed core AHB clock.

USB_HS3_HCLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED

USB_HS3_HCLK_FS (cont.)

Bits	Name	Description
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock 0x1: Force-on mode 0x0: Normal mode
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock 0x1: Force-on mode 0x0: Normal mode
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x00903708 USB_HS3_XCVR_FS_CLK_MD

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register contains the M and D values used for the M/N:D counter of cc_usb_hs3_xcvr_fs_clk generator.

USB_HS3_XCVR_FS_CLK_MD

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED

USB_HS3_XCVR_FS_CLK_MD (cont.)

Bits	Name	Description
23:16	M_VAL	This is the M value for the clock branchs M/N:D counter.
15:8	RESERVED_BITS15_8	RESERVED
7:0	D_VAL	This is the NOT(2*D) value for the clock branchs M/N:D counter.

0x0090370C USB_HS3_XCVR_FS_CLK_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of cc_usb_hs3_xcvr_fs_clk generator. It also contains the branch enable, root enables, clock inversion, MN counter enable and reset, MN counter mode selection, and pre divider control of the cc_usb_hs3_xcvr_fs_clk generator.

USB_HS3_XCVR_FS_CLK_NS

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for usb_hs3_xcvr_fs_clk clock source. NOTE The root cannot be disable by setting this bit to 0 if the downstream CXC (controlled by bit 9 CLK_BRANCH_ENA) is still running. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert usb_hs3_xcvr_fs_clk. 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for usb_hs3_xcvr_fs_clk clock branch. 0x1: Enable 0x0: Disable
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active

USB_HS3_XCVR_FS_CLK_NS (cont.)

Bits	Name	Description
6:5	MNCNTR_MODE	Define M/N counter mode 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00903710 USB_HS3_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control reset to USB HS1 core..

USB_HS3_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	USB_HS3_RESET	Common USB_HS3 core reset

0x00903720 USB_HS4_HCLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is used to control the clock branch for the generation of AHB clock (cc_USB_HS4_hclk) for the USB_HS4 core. It provides enable and clock inversion to the branch, and also contains enable for the fabric dynamic clock gating mode. When dynamic clock gating mode is enabled, the software clock branch enable bit will not have direct control over the enabling of this clock. The enabling of this clock will be done dynamically by internal hardware based on bus traffic.

USB_HS4_HCLK_CTL

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FABRIC_CLK_GATE_ENA	Enable for dynamic clock gating. 0x0: Disable 0x1: Enable
5	CLK_INV	This bit is used to invert usb_hs4_hclk. 0x1: invert 0x0: Not invert
4	CLK_BRANCH_ENA	Enable for usb_hs4_hclk clock branch. This clock is votable. 0x1: Enable 0x0: Disable
3:0	RESERVED_BITS3_0	RESERVED

0x00903724 USB_HS4_HCLK_FS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x4F

This register is used for the sleep and wake-up values of the footswitch controller CXC for USB high speed core AHB clock.

USB_HS4_HCLK_FS

Bits	Name	Description
31:7	RESERVED_BITS31_7	RESERVED
6	FORCE_C_ON	This bit force the core on signal to remain active during halt state of the clk. 0x1: Force-on mode 0x0: Normal mode
5	FORCE_P_ON	This bit force the periph_on signal to remain active during halt state of the clock 0x1: Force-on mode 0x0: Normal mode

USB_HS4_HCLK_FS (cont.)

Bits	Name	Description
4	FORCE_P_OFF	This bit force the perif_off signal to remain active during halt state of the clock. 0x1: Force-on mode 0x0: Normal mode
3:0	S_W_VAL	These bits will set the wake-up and sleep value of the clock. 0x0: Clocks-0 0x1: Clocks-1 0x2: Clocks-2 0x3: Clocks-3 0x4: Clocks-4 0x5: Clocks-5 0x6: Clocks-6 0x7: Clocks-7 0x8: Clocks-8 0x9: Clocks-9 0xA: Clocks-10 0xB: Clocks-11 0xC: Clocks-12 0xD: Clocks-13 0xE: Clocks-14 0xF: Clocks-15

0x00903728 USB_HS4_XCVR_FS_CLK_MD

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register contains the M and D values used for the M/N:D counter of cc_usb_hs4_xcvr_fs_clk generator.

USB_HS4_XCVR_FS_CLK_MD

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	M_VAL	This is the M value for the clock branchs M/N:D counter.
15:8	RESERVED_BITS15_8	RESERVED
7:0	D_VAL	This is the NOT(2*D) value for the clock branchs M/N:D counter.

0x0090372C USB_HS4_XCVR_FS_CLK_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000_0000

This register contains the N values used for the M/N:D counter of cc_usb_hs4_xcvr_fs_clk generator. It also contains the branch enable, root enables, clock inversion, MN counter enable and reset, MN counter mode selection, and pre divider control of the cc_usb_hs4_xcvr_fs_clk generator.

USB_HS4_XCVR_FS_CLK_NS

Bits	Name	Description
31:24	RESERVED_BITS31_24	RESERVED
23:16	N_VAL	This is the NOT(N-M) value of the clock branchs M/N:D counter when it is used as either modulo-N counter or as full M/N:D counter.
15:12	RESERVED_BITS15_12	RESERVED
11	CLK_ROOT_ENA	Enable for usb_hs4_xcvr_fs_clk clock source. NOTE: The root cannot be disable by setting this bit to 0 if the downstream CXC (controlled by bit 9 CLK_BRANCH_ENA) is still running. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert usb_hs4_xcvr_fs_clk. 0x1: invert 0x0: Not invert
9	CLK_BRANCH_ENA	Enable for usb_hs4_xcvr_fs_clk clock branch. 0x1: Enable 0x0: Disable
8	MNCNTR_EN	Enable for the M/N counter. 0x1: Enable 0x0: Disable
7	MNCNTR_RST	Activate the reset for the M/N counter. 0x1: Active 0x0: Not Active
6:5	MNCNTR_MODE	Define M/N counter mode 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode

USB_HS4_XCVR_FS_CLK_NS (cont.)

Bits	Name	Description
4:3	PRE_DIV_SEL	Select to activate or bypass the modulo divider before the M/N counter. 0x0: Bypass 0x1: Div-2 0x2: Div-3 0x3: Div-4
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mxo 0x2: pll0 0x3: pll8 0x4: gnd_tie 0x5: GND 0x6: core_bi_clk_test_se 0x7: core_bi_pll_test_se

0x00903730 USB_HS4_RESET

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0

This register is used to control reset to USB HS1 core.

USB_HS4_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	USB_HS4_RESET	Common USB_HS4 core reset

0x00903740 GSS_CLK_BRANCH_ENA_VOTE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

The GSS_CLK_BRANCH_ENA_VOTE register is the clock enable votes dedicated to LPASS Q6 for clocks that are votable. The vote for clock branch enables is only a vote for ON scheme (The clock will be disabled only if all Masters vote for OFF).

The votable clocks include:

- Scorpion AXI and AHB clocks -- Voting only with RPM, and Scorpion Core 0 and 1

- ADM0 and ADM1 core clocks and pbus clocks
- RPM message ram clock
- PMIC SSBI2, arbitor 0 and 1 hclk
- PRNG clock

Some bits in this register are set (1) on RESOUT to allow the chip to function only at a basic start-up level. All clock branches are enabled (active) and operating at the CXO frequency during RESOUT. The enable signals do not take effect until the RESOUT is de-asserted.

Set (1) enables the corresponding clock branch.

Clear (0) disables the corresponding clock branch.

GSS_CLK_BRANCH_ENA_VOTE

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12:11	RESERVED_BITS12_11	RESERVED
10	PRNG_CLK_ENA	Enable for PRNG clock 0x1: Enable
9	PMIC_ARB1_HCLK_ENA	Enable PMIC Arbiter 1 clock 0x1: Enabled
8	PMIC_ARB0_HCLK_ENA	Enable PMIC Arbiter 0 clock 0x1: Enabled
7	PMIC_SSBI2_CLK_ENA	Enable for PMIC SSBI2 clock 0x1: Enable
6	RPM_MSG_RAM_HCLK_ENA	Enable for RPM message ram clock 0x1: Enable
5:4	RESERVED_BITS5_4	RESERVED
3	ADM0_PBUS_CLK_ENA	Enable for ADM0 PBUS clock 0x1: Enable
2	ADM0_CLK_ENA	Enable ADM0 clock 0x1: Enabled
1:0	RESERVED_BITS1_0	RESERVED

0x00903744 GSS_CLK_SLEEP_ENA_VOTE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

The GSS_CLK_SLEEP_ENA_VOTE register is used to halt the corresponding clock signals when the LPA_Q6 processor goes to standby by asserting lpass_cc_qdsp6_core_idle signal. The value of each bit is correspondingly combined with the bit in GSS_CLK_BRANCH_ENA_VOTE register. If clock is not enabled in GSS_CLK_BRANCH_ENA register, it will NOT enable upon interrupt.

- Set (1) allows the clock to halt when LPASS Q6 goes to standby mode.
- Clear (0) does not allow the clock to halt when LPASS Q6 goes to standby mode.

GSS_CLK_SLEEP_ENA_VOTE

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12:11	RESERVED_BITS12_11	RESERVED
10	PRNG_CLK_SLEEP_ENA	Halt PRNG clock upon standby 0x1: Enable
9	PMIC_ARB1_HCLK_SLEEP_ENA	Halt PMIC Arbiter 1 clock upon standby 0x1: Enabled
8	PMIC_ARB0_HCLK_SLEEP_ENA	Halt PMIC Arbiter 0 clock upon standby 0x1: Enabled
7	PMIC_SSBI2_CLK_SLEEP_ENA	Halt PMIC SSBI2 clock upon standby 0x1: Enable
6	RPM_MSG_RAM_HCLK_SLEEP_ENA	Halt RPM message ram clock upon standby 0x1: Enable
5:4	RESERVED_BITS5_4	RESERVED
3	ADM0_PBUS_CLK_SLEEP_ENA	Halt ADM0 PBUS clock upon standby 0x1: Enable
2	ADM0_CLK_SLEEP_ENA	halt ADM0 clock upon standby. 0x1: Enabled
1:0	RESERVED_BITS1_0	RESERVED

0x009037E4 RIVA_CLK_BRANCH_ENA_VOTE

Type: Read/Write
Clock: SFPB_HCLK
Reset State: 0x0

The RIVA_CLK_BRANCH_ENA_VOTE register is the clock enable votes dedicated to untrusted side of Scorpion core1 for clocks that are votable. The vote for clock branch enables is only a vote for ON scheme (The clock will be disabled only if all Masters vote for OFF).

The votable clocks include:

- Scorpion AXI and AHB clocks -- Voting only with RPM, and Scorpion Core 0 and 1
- ADM0 and ADM1 core clocks and pbus clocks
- RPM message ram clock
- PMIC SSBI2, arbitor 0 and 1 hclk
- PRNG clock

Some bits in this register are set (1) on RESOUT to allow the chip to function only at a basic start-up level. All clock branches are enabled (active) and operating at the CXO frequency during RESOUT. The enable signals do not take effect until the RESOUT is de-asserted.

Set (1) enables the corresponding clock branch.

Clear (0) disables the corresponding clock branch.

RIVA_CLK_BRANCH_ENA_VOTE

Bits	Name	Description
31:13	RESERVED_BITS31_13	RESERVED
12:11	RESERVED_BITS12_11	RESERVED
10	PRNG_CLK_ENA	Enable for PRNG clock 0x1: Enable
9	PMIC_ARB1_HCLK_ENA	Enable PMIC Arbiter 1 clock 0x1: Enabled
8	PMIC_ARB0_HCLK_ENA	Enable PMIC Arbiter 0 clock 0x1: Enabled
7	PMIC_SSBI2_CLK_ENA	Enable for PMIC SSBI2 clock 0x1: Enable
6	RPM_MSG_RAM_HCLK_ENA	Enable for RPM message ram clock 0x1: Enable
5:4	RESERVED_BITS5_4	RESERVED
3	ADM0_PBUS_CLK_ENA	Enable for ADM0 PBUS clock 0x1: Enable
2	ADM0_CLK_ENA	Enable ADM0 clock 0x1: Enabled
1:0	RESERVED_BITS1_0	RESERVED

0x00903800 SPDM_CY_PORT8_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the control for enabling and inverting the SPDM CY port8 clock. SPDM CY port 8 clock is a divided version of SCPLL3 aux output clock. We must enable the AUX source output of SCPLL3 as well in order to see this clock properly.

SPDM_CY_PORT8_CLK_CTL

Bits	Name	Description
31:6	RESERVED_BITS31_6	RESERVED
5	CLK_INV	This bit is used to invert the clock. 0x1: Inverted 0x0: Not inverted
4	CLK_BRANCH_ENA	This bit is used to enable the clock branch. 0x1: Enable 0x0: Diable
3:1	RESERVED_BITS3_1	RESERVED
0	SRC_SEL	This bit selects between SCPLL3 aux output or PXO clock. 0x1: SCPLL3_aux 0x0: PXO (default)

0x00903820 APCS_WDT0_CPU0_WDOG_EXPIRED_ENABLE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the enable for allowing the APCS CPU0's WDOG timer0's expiration to trigger a reset.

APCS_WDT0_CPU0_WDOG_EXPIRED_ENABLE

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	WDOG_ENA	This bit enables the WDOG timer's expiration to trigger a reset: 0x0: not enabled 0x1: enabled

0x00903824 APCS_WDT1_CPU0_WDOG_EXPIRED_ENABLE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the enable for allowing the APCS CPU0's WDOG timer1's expiration to trigger a reset.

APCS_WDT1_CPU0_WDOG_EXPIRED_ENABLE

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	WDOG_ENA	This bit enables the WDOG timer's expiration to trigger a reset: 0x0: not enabled 0x1: enabled

0x00903828 APCS_WDT0_CPU1_WDOG_EXPIRED_ENABLE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the enable for allowing the APCS CPU1's WDOG timer0's expiration to trigger a reset.

APCS_WDT0_CPU1_WDOG_EXPIRED_ENABLE

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	WDOG_ENA	This bit enables the WDOG timer's expiration to trigger a reset: 0x0: not enabled 0x1: enabled

0x0090382C APCS_WDT1_CPU1_WDOG_EXPIRED_ENABLE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the enable for allowing the APCS CPU1's WDOG timer1's expiration to trigger a reset.

APCS_WDT1_CPU1_WDOG_EXPIRED_ENABLE

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	WDOG_ENA	This bit enables the WDOG timer's expiration to trigger a reset: 0x0: not enabled 0x1: enabled

0x00903830 APCS_WDT0_CPU2_WDOG_EXPIRED_ENABLE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the enable for allowing the APCS CPU2's WDOG timer0's expiration to trigger a reset.

APCS_WDT0_CPU2_WDOG_EXPIRED_ENABLE

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	WDOG_ENA	This bit enables the WDOG timer's expiration to trigger a reset: 0x0: not enabled 0x1: enabled

0x00903834 APCS_WDT1_CPU2_WDOG_EXPIRED_ENABLE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the enable for allowing the APCS CPU2's WDOG timer1's expiration to trigger a reset.

APCS_WDT1_CPU2_WDOG_EXPIRED_ENABLE

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	WDOG_ENA	This bit enables the WDOG timer's expiration to trigger a reset: 0x0: not enabled 0x1: enabled

0x00903838 APCS_WDT0_CPU3_WDOG_EXPIRED_ENABLE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the enable for allowing the APCS CPU3's WDOG timer0's expiration to trigger a reset.

APCS_WDT0_CPU3_WDOG_EXPIRED_ENABLE

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	WDOG_ENA	This bit enables the WDOG timer's expiration to trigger a reset: 0x0: not enabled 0x1: enabled

0x0090383C APCS_WDT1_CPU3_WDOG_EXPIRED_ENABLE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register provides the enable for allowing the APCS CPU3's WDOG timer1's expiration to trigger a reset.

APCS_WDT1_CPU3_WDOG_EXPIRED_ENABLE

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	WDOG_ENA	This bit enables the WDOG timer's expiration to trigger a reset: 0x0: not enabled 0x1: enabled

0x00903840 RPM_WDOG_EXPIRED_ENABLE

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x01

This register provides the enable for allowing the RPM's WDOG timer's expiration to trigger a reset.

RPM_WDOG_EXPIRED_ENABLE

Bits	Name	Description
31:1	RESERVED_BITS31_1	RESERVED
0	WDOG_ENA	This bit enables the WDOG timer's expiration to trigger a reset: 0x0: not enabled 0x1: enabled

0x00903860 PCIE_ALT_REF_CLK_NS

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x0000

The PCIE_ALT_REF_CLK_NS register provides controls to the cell used to generate cc_pcie_alt_ref_clk. The controls include root clock enable, source select, source divider value and inversion of cc_pcie_alt_ref_clk.

PCIE_ALT_REF_CLK_NS

Bits	Name	Description
31:12	RESERVED_BITS31_12	RESERVED
11	CLK_ROOT_ENA	Enable for pcie_alt_ref_clk clock source. 0x1: Enable 0x0: Disable
10	CLK_INV	This bit is used to invert pcie_alt_ref_clk 0x1: Invert 0x0: Not Invert
9	CLK_BRANCH_ENA	Enable for pcie_alt_ref_clk clock branch 0x1: Enable 0x0: Disable
8:7	RESERVED_BITS8_7	RESERVED

PCIE_ALT_REF_CLK_NS (cont.)

Bits	Name	Description
6:3	CLK_DIV	This field is used to control the divider for generating the pcie_alt_ref_clk. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
2:1	RESERVED_BITS2_1	RESERVED
0	SRC_SEL	This field selects which source to drive pcie_alt_ref_clk. 0x0: PXO 0x1: PLL3

0x00903880 RIVA_XO_SRC_CLK_CTL

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is a spare.

RIVA_XO_SRC_CLK_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:4	NOT_USED_BITS7_4	NOT USED
3	RIVA_XO_INV	This bit is used to invert riva_clk_pxo_src 0x1: invert 0x0: Not invert
2	RIVA_XO_SELECT	Select between CXO and PXO sources 0x1: Select PXO 0x0: Select CXO

RIVA_XO_SRC_CLK_CTL (cont.)

Bits	Name	Description
1	RIVA_XO_SWITCH_DISABLE	Disables the CXC switch 0x1: XOOFF 0x0: XO ON
0	NOT_USED_BIT0	NOT USED

0x00903884 SPARE1

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is a spare.

SPARE1

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	SPARE_BITS	Spare bits

0x00903888 SPARE2

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is a spare.

SPARE2

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	SPARE_BITS	Spare bits

0x0090388C SPARE3

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is a spare.

SPARE3

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	SPARE_BITS	Spare bits

0x009038A0 SPARE4

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is a spare.

SPARE4

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	SPARE_BITS	Spare bits

0x009038A4 SPARE5

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is a spare.

SPARE5

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	SPARE_BITS	Spare bits

0x009038A8 SPARE6

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is a spare.

SPARE6

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	SPARE_BITS	Spare bits

0x009038AC SPARE7

Type: Write/Read
Clock: SFPB_HCLK
Reset State: 0x00

This register is a spare.

SPARE7

Bits	Name	Description
31:8	RESERVED_BITS31_8	RESERVED
7:0	SPARE_BITS	Spare bits

6 Debug Subsystem Registers

6.1 Overview

Table 6-1 Debug_Sub_System

Bases

Base Name	Parent	Address
QDSS_ETB_ROM_WORD	QDSS_DAPROM_BASE	0x01A00000
QDSS_ETB_RAM_DEPTH_REG	QDSS_ETB_BASE	0x01A01000
QDSS_CTI1_CONTROL	QDSS_CTI1_BASE	0x01A02000
QDSS_TPIU_SUPPORTED_PORT_SIZE	QDSS_TPIU_BASE	0x01A03000
QDSS_CS_TFUNNEL_FUNCTL	QDSS_TFUNNEL_BASE	0x01A04000
QDSS_ITM_STIMULUS_PORT_REGn	QDSS_ITM_BASE	0x01A05000
QDSS_STMDMASTARTR	QDSS_STM_BASE	0x01A06000
QDSS_M2VMT_M2VMRn	QDSS_DAPM2VMT_BASE	0x01A80000

6.2 QDSS DAPROM Registers (0x01A00000 QDSS_DAPROM_BASE)

This section contains the QDSS DAPROM registers.

The DAPROM contains the base address location information for all the CoreSight compliant components as well as the CoreSight management registers of the debug system implemented in APQ8064. Address range 0x000 - 0xFFC follows the entry format shown in the DDIO314H ARM specification. This format contains the APB address offset of one CoreSight component such as the ETB. All of the registers in DAPROM are READ-ONLY.

NOTE For more detailed information about these registers, see ARM documentation at http://infocenter.arm.com/help/index.jsp.

0x01A00000 QDSS_ETB_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00001003

QDSS_ETB_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x01000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00004 QDSS_CTI1_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00002003

QDSS_CTI1_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x02000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00008 QDSS_TPIU_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00003003

QDSS_TPIU_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x03000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A0000C QDSS_FUNNEL_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00004003

QDSS_FUNNEL_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x04000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00010 QDSS_ITM_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00005003

QDSS_ITM_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x05000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word

QDSS_ITM_ROM_WORD (cont.)

Bits	Name	Description
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00014 QDSS_STM_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00006003

QDSS_STM_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x06000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00018 QDSS_CA5_DBG_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00007003

QDSS_CA5_DBG_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x10000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A0001C QDSS_CA5_PMU_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00008003

QDSS_CA5_PMU_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x10000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00020 QDSS_CA5_ETM_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00009003

QDSS_CA5_ETM_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x10000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00024 QDSS_KRAIT0_DBG_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00010003

QDSS_KRAIT0_DBG_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x10000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00028 QDSS_KRAIT0_PM_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00011003

QDSS_KRAIT0_PM_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x11000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A0002C QDSS_KRAIT1_DBG_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00012003

QDSS_KRAIT1_DBG_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x12000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00030 QDSS_KRAIT1_PM_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00013003

QDSS_KRAIT1_PM_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x13000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word

QDSS_KRAIT1_PM_ROM_WORD (cont.)

Bits	Name	Description
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00034 QDSS_KRAIT2_DBG_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00014003

QDSS_KRAIT2_DBG_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x12000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00038 QDSS_KRAIT2_PM_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00015003

QDSS_KRAIT2_PM_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x13000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A0003C QDSS_KRAIT3_DBG_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00016003

QDSS_KRAIT3_DBG_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x12000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00040 QDSS_KRAIT3_PM_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x00017003

QDSS_KRAIT3_PM_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x13000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00044 QDSS_KRAIT0_PFT_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x0001C003

QDSS_KRAIT0_PFT_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x1C000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00048 QDSS_KRAIT1_PFT_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x0001D003

QDSS_KRAIT1_PFT_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x1D000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A0004C QDSS_KRAIT2_PFT_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x0001E003

QDSS_KRAIT2_PFT_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x1D000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00050 QDSS_KRAIT3_PFT_ROM_WORD

Type: Read
Clock: PCLKDBG
Reset State: 0x0001F003

QDSS_KRAIT3_PFT_ROM_WORD

Bits	Name	Description
31:12	ADDR_OFFSET	0x1D000 Address offset relative to the base address of this ROM Table
11:2	RESERVED	0x0000
1	FORMAT	0b1 The '1' value signifies a 32-bit ROM word

QDSS_KRAIT3_PFT_ROM_WORD (cont.)

Bits	Name	Description
0	PRESENT	0b1 The '1' value signifies a non-empty ROM word

0x01A00FD0 QDSS_DAPROM_PERIPHERAL_ID4

Type: Read
Clock: PCLKDBG
Reset State: 0x00000000

QDSS_DAPROM_PERIPHERAL_ID4

Bits	Name	Description
31:8	RESERVED	0x000000
7:4	B_4KB_COUNT	Log2 of the number of 4KB blocks occupied by the device. Hence the value of "0" indicates one 4KB block for this ROM table.
3:0	JEP106_CC	This is bits [10:7] of JEP106 Identity Code. This field must have the same value as DAP input port TARGETID[11:8].

0x01A00FD4 QDSS_DAPROM_PERIPHERAL_ID5

Type: Read
Clock: PCLKDBG
Reset State: 0x00000000

QDSS_DAPROM_PERIPHERAL_ID5

Bits	Name	Description
31:1	RESERVED	0x000000
0	RESERVED_SBZ	0x00

0x01A00FD8 QDSS_DAPROM_PERIPHERAL_ID6

Type: Read
Clock: PCLKDBG
Reset State: 0x00000000

QDSS_DAPROM_PERIPHERAL_ID6

Bits	Name	Description
31:8	RESERVED	0x000000
7:0	RESERVED_SBZ	0x00

0x01A00FDC QDSS_DAPROM_PERIPHERAL_ID7

Type: Read
Clock: PCLKDBG
Reset State: 0x00000000

QDSS_DAPROM_PERIPHERAL_ID7

Bits	Name	Description
31:8	RESERVED	0x000000
7:0	RESERVED_SBZ	0x00

0x01A00FE0 QDSS_DAPROM_PERIPHERAL_ID0

Type: Read
Clock: PCLKDBG
Reset State: 0x00000071

QDSS_DAPROM_PERIPHERAL_ID0

Bits	Name	Description
31:8	RESERVED	0x000000
7:0	PART_NUM	Part number for the device. A database must be established to ensure that each Coresight-equipped chip gets a unique 12-bit number. This field must have the same value as DAP input port TARGETID[23:16].

0x01A00FE4 QDSS_DAPROM_PERIPHERAL_ID1

Type: Read
Clock: PCLKDBG
Reset State: 0x00000000

QDSS_DAPROM_PERIPHERAL_ID1

Bits	Name	Description
31:8	RESERVED	0x000000
7:4	JEP106_ID	This is bits [3:0] of JEP106 Identity Code. This field must have the same value as DAP input port TARGETID[4:1].
3:0	PART_NUM	Part number for the device. A database must be established to ensure that each Coresight-equipped chip gets a unique 12-bit number. This field must have the same value as DAP input port TARGETID[27:24].

0x01A00FE8 QDSS_DAPROM_PERIPHERAL_ID2

Type: Read
Clock: PCLKDBG
Reset State: 0x0000000F

QDSS_DAPROM_PERIPHERAL_ID2

Bits	Name	Description
31:8	RESERVED	0x000000
7:4	PERIPH_REV	Revision number of the peripheral (this ROM table). Starts at 0 and increments by 1 for each revision. This field must have the same value as DAP input port TARGETID[31:28].
3	JEP106_ASS	This bit is set to 1 when a JEP 106 Identity Code is used. This bit must be 1 on new implementations
2:0	JEP106_ID	This is bits [6:4] of JEP106 Identity Code.This field must have the same value as DAP input port TARGETID[7:5].

0x01A00FEC QDSS_DAPROM_PERIPHERAL_ID3

Type: Read
Clock: PCLKDBG
Reset State: 0x00000000

QDSS_DAPROM_PERIPHERAL_ID3

Bits	Name	Description
31:8	RESERVED	0x000000
7:4	REV_AND	Manufacturer Revision Number. This field must have the same value as DAP input port TARGETID[15:12].
3:0	MODIFIED	Customer modified, implementation defined.

0x01A00FF0 QDSS_DAPROM_COMPONENT_ID0

Type: Read
Clock: PCLKDBG
Reset State: 0x0000000D

QDSS_DAPROM_COMPONENT_ID0

Bits	Name	Description
31:8	RESERVED	0x000000
7:0	PREAMBLE_7_0	0x0D

0x01A00FF4 QDSS_DAPROM_COMPONENT_ID1

Type: Read
Clock: PCLKDBG
Reset State: 0x00000010

QDSS_DAPROM_COMPONENT_ID1

Bits	Name	Description
31:8	RESERVED	0x000000
7:4	PREAMBLE_15_12	0x1 (aka Component class) 0x1 says ROM table
3:0	PREAMBLE_11_8	0x0

0x01A00FF8 QDSS_DAPROM_COMPONENT_ID2

Type: Read
Clock: PCLKDBG
Reset State: 0x00000005

QDSS_DAPROM_COMPONENT_ID2

Bits	Name	Description
31:8	RESERVED	0x000000
7:0	PREAMBLE_23_16	0x05

0x01A00FFC QDSS_DAPROM_COMPONENT_ID3

Type: Read
Clock: PCLKDBG
Reset State: 0x000000B1

QDSS_DAPROM_COMPONENT_ID3

Bits	Name	Description
31:8	RESERVED	0x000000
7:0	PREAMBLE_31_24	0xB1

6.3 QDSS ETB Registers (0x01A01000 QDSS_ETB_BASE)

This section contains the QDSS ETB registers.

6.3.1 CoreSight Component Registers

This section describes the CS component registers. This includes device specific registers, CS management registers, peripheral ID registers, and component ID registers. It is provided below for QCSR and FLAT file generation. However, the details of the registers can be found in the ARM documents, which provide more detailed information about these registers, such as their usage and descriptive register bits information. See: http://infocenter.arm.com/help/index.jsp.

6.3.1.1 CoreSight ETB Registers Summary

Table 6-2 contains a summary of ETB registers.

Table 6-2 Summary of ETB registers

Offset	Type	Width	Reset value	Name	Reference Section
0x004	Read	32	0x1000	RAM Depth Register, RDP	ETB RAM Depth Register, RDP, 0x004
0x00C	Read	32	0x1000	Status Register, STS	ETB Status Register, STS, 0x00C
0x010	Read	32	0x00000000	RAM Read Data Register, RRD	ETB RAM Read Data Register, RRD, 0x010
0x014	Read/Write	32	0x00000000	RAM Read Pointer Register, RRP	ETB RAM Read Pointer Register, RRP, 0x014
0x018	Read/Write	32	0x00000000	RAM Write Pointer Register, RWP	ETB RAM Write Pointer Register, RWP, 0x018
0x01C	Read/Write	32	0x00000000	Trigger Counter Register, TRG	ETB Trigger Counter Register, TRG, 0x01C
0x020	Read/Write	32	0x00000000	Control Register, CTL	ETB Control Register, CTL, 0x020
0x024	Write	32	0x00000000	RAM Write Data Register, RWD	ETB RAM Write Data Register, RWD, 0x024
0x300	Read	2	0x02	Formatter and Flush Status Register, FFSR	ETB Formatter and Flush Status Register, FFSR, 0x300
0x304	Read/Write	13	0x0200	Formatter and Flush Control Register, FFCR	ETB Formatter and Flush Control Register, FFCR, 0x304
0xEE0	Write	2	-	Integration Register, ITMISCOP0	ETB Integration Test Registers
0xEE4	Write	2	-	Integration Register, ITTRFLINACK	Integration Test Trigger In and Flush In Acknowledge Register, ITTRFLINACK, 0xEE4
0xEE8	Read	2	Undefined	Integration Register, ITTRFLIN	Integration Test Trigger In and Flush In Register, ITTRFLIN, 0xEE8

Table 6-2 Summary of ETB registers

Offset	Type	Width	Reset value	Name	Reference Section
0xEEC	Read	5	Undefined	Integration Register, ITATBDATA0	Integration Test ATB Data Register 0, ITATBDATA0, 0xEEC
0xEF0	Write	2	-	Integration Register, ITATBCTR2	Integration Test ATB Control Register 2, ITATBCTR2, 0xEF0
0xEF4	Read	7	Undefined	Integration Register, ITATBCTR1	Integration Test ATB Control Register 1, ITATBCTR1, 0xEF4
0xEF8	Read	10	Undefined	Integration Register, ITATBCTR0	Integration Test ATB Control Register 0, ITATBCTR0, 0xEF8
0xF00	Read/Write	1	0x0	Integration Mode Control Register	ETB CoreSight management registers
0xFA0	Read/Write	4	0xF	Claim Tag Set Register	
0xFA4	Read/Write	4	0x0	Claim Tag Clear Register	
0xFB0	Write	32	-	Lock Access Register	
0xFB4	Read	3	0x0/0x3	Lock Status Register	
0xFB8	Read	8	0x00	Authentication Status Register	
0xFC8	Read	32	0x00	Device ID	
0xFCC	Read	8	0x21	Device Type Identifier Register	
0xFD0	Read	8	0x04	Peripheral ID4	
0xFD4	Read	8	0x00 (reserved)	Peripheral ID5	
0xFD8	Read	8	0x00 (reserved)	Peripheral ID6	
0xFDC	Read	8	0x00 (reserved)	Peripheral ID7	
0xFE0	Read	8	0x07	Peripheral ID0	
0xFE4	Read	8	0xB9	Peripheral ID1	
0xFE8	Read	8	0x2B	Peripheral ID2	ETB CoreSight management registers
0xFEC	Read	8	0x00	Peripheral ID3	
0xFF0	Read	8	0x0D	Component ID0	
0xFF4	Read	8	0x90	Component ID1	
0xFF8	Read	8	0x05	Component ID2	
0xFFC	Read	8	0xB1	Component ID3	

6.3.1.2 ETB Registers

0x01A01004 QDSS_ETB_RAM_DEPTH_REG

Type: Read
Reset State: 0x1000

ETB RAM Depth Register, RDP, 0x004

QDSS_ETB_RAM_DEPTH_REG

Bits	Name	Description
31:0	RAM_DEPTH_REGISTER	Defines the depth, in words, of the trace RAM. This value is configurable in the RTL, but fixed at synthesis. Supported depth in powers of 2 only. Reset value = Ram Depth that is given by a Verilog tick define. = 0x1000 = 16KB ETB

0x01A0100C QDSS_ETB_STATUS_REG

Type: Read
Reset State: 0x0008

ETB Status Register, STS, 0x00C

QDSS_ETB_STATUS_REG

Bits	Name	Description
31:4	RESERVED	Reserved.
3	FTEMPTY	Formatter pipeline empty. All data stored to RAM.
2	ACQCOMP	Acquisition complete. The acquisition complete flag indicates that capture has been completed when the formatter stops because of any of the methods defined in the Formatter and Flush Control Register, or TraceCaptEn = 0. This also results in FtStopped in the Formatter and Flush Status Register going HIGH.
1	TRIGGERED	The Triggered bit is set when a trigger has been observed. This does not indicate that a trigger has been embedded in the trace data by the formatter, but is determined by the programming of the Formatter and Flush Control Register.
0	FULL	RAM Full. The flag indicates when the RAM write pointer has wrapped around.

0x01A01010 QDSS_ETB_RAM_READ_DATA_REG

Type: Read
Reset State: 0x00000000

ETB RAM Read Data Register, RRD, 0x010

0x01A01014 QDSS_ETB_RAM_READ_POINTER

Type: Read/Write
Reset State: 0x00000000

ETB RAM Read Pointer Register, RRP, 0x014

QDSS_ETB_RAM_READ_POINTER

Bits	Name	Description
1:0	CSETB_ADDR_WIDTH	Sets the read pointer used to read entries from the Trace RAM over the APB interface.

0x01A01018 QDSS_ETB_RAM_WRITE_POINTER

Type: Read/Write
Reset State: 0x00000000

ETB RAM Write Pointer Register, RWP, 0x018

QDSS_ETB_RAM_WRITE_POINTER

Bits	Name	Description
1:0	CSETB_ADDR_WIDTH	Sets the write pointer used to write entries from the CoreSight bus into the Trace RAM

0x01A0101C QDSS_ETB_TRG

Type: Read/Write
Reset State: 0x00000000

ETB Trigger Counter Register, TRG, 0x01C

0x01A01020 QDSS_ETB_CTL_REG

Type: Read/Write
Reset State: 0x00000000

ETB Control Register, CTL, 0x020

QDSS_ETB_CTL_REG

Bits	Name	Description
31:1	RESERVED	Reserved
0	TRACECAPTEN	ETB Trace Capture Enable. This is the master enable bit forcing FtStopped HIGH when TraceCaptEn is LOW. When capture is disabled, any remaining data in the ATB formatter is stored to RAM. When all data is stored the formatter outputs FtStopped. Capture is fully disabled, or complete, when FtStopped goes HIGH. See ETB Formatter and Flush Status Register, FFSR, 0x300. 0x1: enable trace capture 0x0: disable trace capture.

0x01A01024 QDSS_ETB_RWD_REG

Type: Write
Reset State: 0x00000000

ETB RAM Write Data Register, RWD, 0x024

QDSS_ETB_RWD_REG

Bits	Name	Description
31:0	RAM_WRITE_DATA_REGISTER	Data written to the ETB Trace RAM. When trace capture is disabled, the contents of this register are placed into the ETB Trace RAM when this register is written to. Writing to this register increments the RAM Write Pointer Register. If trace capture is enabled, and this register is accessed, then a read from this register outputs 0xFFFFFFFF. Reads of this register never increment the RAM Write Pointer Register. A constant stream of 1s being output corresponds to a synchronization output from the ETB. If a write access is attempted, the data is not written into Trace RAM.

0x01A01300 QDSS_ETB_FFSR

Type: Read
Reset State: 0x00000002

ETB Formatter and Flush Status Register, FFSR, 0x300

QDSS_ETB_FFSR

Bits	Name	Description
31:2	RESERVED	Reserved RAZ/SBZP.
1	FTSTOPPED	Formatter stopped. The formatter has received a stop request signal and all trace data and post-amble has been output. Any more trace data on the ATB interface is ignored and ATREADYS goes HIGH.
0	FLINPROG	Flush In Progress. This is an indication of the current state of AFVALIDS.

0x01A01304 QDSS_ETB_FFCR

Type: Read/Write
Reset State: 0x0000

ETB Formatter and Flush Control Register, FFCR, 0x304

QDSS_ETB_FFCR

Bits	Name	Description
31:14	RESERVED_1	Reserved RAZ/SBZP.
13	STOPTRIG	Stop the formatter when a Trigger Event has been observed. Reset to disabled (zero).
12	STOPFL	Stop the formatter when a flush has completed (return of AFREADYS). This forces the FIFO to drain off any part-completed packets. Setting this bit enables this function but this is clear on reset (disabled).
11	RESERVED_2	Reserved RAZ/SBZP.
10	TRIGFL	Indicate a trigger on Flush completion (AFREADYS being returned).
9	TRIGEVT	Indicate a trigger on a Trigger Event.
8	TRIGIN	Indicate a trigger on TRIGIN being asserted
7	RESERVED_3	Reserved RAZ/SBZP.
6	FONMAN	Manually generate a flush of the system. Setting this bit causes a flush to be generated. This is cleared when this flush has been serviced. This bit is clear on reset.
5	FONTRIG	Generate flush using Trigger event. Set this bit to cause a flush of data in the system when a Trigger Event occurs. This bit is clear on reset.
4	FONFLIN	Generate flush using the FLUSHIN interface. Set this bit to enable use of the FLUSHIN connection. This bit is clear on reset.
3:2	RESERVED_4	Reserved RAZ/SBZP.

QDSS_ETB_FFCR (cont.)

Bits	Name	Description
1	ENFCONT	Continuous Formatting. Continuous mode in the ETB corresponds to normal mode with the embedding of triggers. Can only be changed when FtStopped is HIGH. This bit is clear on reset.
0	ENFTC	Enable Formatting. Do not embed Triggers into the formatted stream. Trace disable cycles and triggers are indicated by TRACECTL, where fitted. Can only be changed when FtStopped is HIGH. This bit is clear on reset.

0x01A01EE0 QDSS_ETB_ITMISCOP0

Type: Write
Reset State: Not readable

ETB Integration Test Registers

QDSS_ETB_ITMISCOP0

Bits	Name	Description
31:2	RESERVED	Reserved
1	FULL	Set the value of FULL
0	ACQCOMP	Set the value of ACQCOMP

0x01A01EE4 QDSS_ETB_ITTRFLINACK

Type: Write
Reset State: Not readable

Integration Test Trigger In and Flush In Acknowledge Register, ITTRFLINACK, 0xEE4

QDSS_ETB_ITTRFLINACK

Bits	Name	Description
31:2	RESERVED	Reserved
1	FLUSHINACK	Set the value of FLUSHINACK
0	TRIGINACK	Set the value of TRIGINACK

0x01A01EE8 QDSS_ETB_ITTRFLIN

Type: Read
Reset State: Undefined

Integration Test Trigger In and Flush In Register, ITTRFLIN, 0xEE8

QDSS_ETB_ITTRFLIN

Bits	Name	Description
31:2	RESERVED	Reserved
1	FLUSHIN	Read the value of FLUSHIN
0	TRIGIN	Read the value of TRIGIN

0x01A01EEC QDSS_ETB_ITATBDATA0

Type: Read
Reset State: Undefined

Integration Test ATB Data Register 0, ITATBDATA0, 0xEEC

QDSS_ETB_ITATBDATA0

Bits	Name	Description
31:5	RESERVED	Reserved
4	ATDATA_31	Read the value of ATDATAS[31]
3	ATDATA_23	Read the value of ATDATAS[23]
2	ATDATA_15	Read the value of ATDATAS[15]
1	ATDATA_7	Read the value of ATDATAS[7]
0	ATDATA_0	Read the value of ATDATAS[0]

0x01A01EF0 QDSS_ETB_ITATBCTR2

Type: Write
Reset State: Not readable

Integration Test ATB Control Register 2, ITATBCTR2, 0xEF0

QDSS_ETB_ITATBCTR2

Bits	Name	Description
31:2	RESERVED	Reserved
1	AFVALIDS	Set the value of AFVALIDS
0	ATREADYS	Set the value of ATREADYS

0x01A01EF4 QDSS_ETB_ITATBCTR1

Type: Read
Reset State: Undefined

Integration Test ATB Control Register 1, ITATBCTR1, 0xEF4

QDSS_ETB_ITATBCTR1

Bits	Name	Description
31:7	RESERVED	Reserved
6:0	ATID	Read the value of ATIDS

0x01A01EF8 QDSS_ETB_ITATBCTR0

Type: Read
Reset State: Undefined

Integration Test ATB Control Register 0, ITATBCTR0, 0xEF8

QDSS_ETB_ITATBCTR0

Bits	Name	Description
31:10	RESERVED_1	Reserved
9:8	ATBYTES	Read the value of ATBYTESS
7:2	RESERVED_2	Reserved
1	AFREADY	Read the value of AFREADYS
0	ATVALID	Read the value of ATVALIDS

0x01A01F00 QDSS_ETB_INTG_MODE_CTL

Type: Read/Write
Reset State: 0x0

ETB CoreSight management registers

0x01A01FA0 QDSS_ETB_CLAIM_TAG_SET

Type: Read/Write
Reset State: 0xF

0x01A01FA4 QDSS_ETB_CLAIM_TAG_CLR

Type: Read/Write
Reset State: 0x0

0x01A01FB0 QDSS_ETB_LOCK_ACCESS

Type: Write
Reset State: Not readable

0x01A01FB4 QDSS_ETB_LOCK_STATUS

Type: Read
Reset State: 0x0/0x3

0x01A01FB8 QDSS_ETB_AUTH_STATUS

Type: Read
Reset State: 0x00

0x01A01FC8 QDSS_ETB_DEVICE_ID

Type: Read
Reset State: 0x00

0x01A01FCC QDSS_ETB_DEVICE_TYPE_ID

Type: Read
Reset State: 0x21

0x01A01FD0 QDSS_ETB_PID4

Type: Read
Reset State: 0x04

0x01A01FE0 QDSS_ETB_PID0

Type: Read
Reset State: 0x07

0x01A01FE4 QDSS_ETB_PID1

Type: Read
Reset State: 0xB9

0x01A01FE8 QDSS_ETB_PID2

Type: Read
Reset State: 0x3B

ETB CoreSight management registers

0x01A01FEC QDSS_ETB_PID3

Type: Read
Reset State: 0x00

0x01A01FF0 QDSS_ETB_CID0

Type: Read
Reset State: 0x0D

0x01A01FF4 QDSS_ETB_CID1

Type: Read
Reset State: 0x90

0x01A01FF8 QDSS_ETB_CID2

Type: Read
Reset State: 0x05

0x01A01FFC QDSS_ETB_CID3

Type: Read
Reset State: 0xB1

6.4 QDSS CTI1 Registers (0x01A02000 QDSS_CTI1_BASE)

This section contains the QDSS CTI1 registers.

6.4.1 CoreSight Component Registers

This section describes the CS component registers. This includes device specific registers, CS management registers, peripheral ID registers, and component ID registers. It is provided below for QCSR and FLAT file generation. However, the details of the registers can be found in the ARM documents, which provide more detailed information about these registers, such as their usage and descriptive register bits information. See: http://infocenter.arm.com/help/index.jsp.

6.4.1.1 CoreSight CTI Registers Summary

Table 6-3 is the summary of CTI registers.

Table 6-3 Summary of CTI registers

Offset	Name	Type	Width	Reset value	Description
0x000	CTI1_CONTROL	Read/Write	1	0x0	See CTI Control Register, CTICONTROL, 0x000
0x010	CTI1_INTACK	Write	8	-	See CTI Interrupt Acknowledge Register, CTIINTACK, 0x010
0x014	CTI1_APPSET	Read/Write	4	0x0	See CTI Application Trigger Set Register, CTIAPPSET, 0x014
0x018	CTI1_APPCLEAR	Write	4	0x0	See CTI Application Trigger Clear Register, CTIAPPCLEAR, 0x018
0x01C	CTI1_APPPULSE	Write	4	0x0	See CTI Application Pulse Register, CTIAPPPULSE, 0x01C
0x020-0x03C	CTI1_INEN	Read/Write	4	0x00	See CTI Trigger to Channel Enable Registers, CTIINEN0-7, 0x020-0x03C
0x0A0-0x0BC	CTI1_OUTEN	Read/Write	4	0x00	See CTI Channel to Trigger Enable Registers, CTIOUTEN0-7, 0x0A0-0x0BC
0x130	CTI1_TRIGINSTATUS	Read	8	-	See CTI Trigger In Status Register, CTITRIGINSTATUS, 0x130
0x134	CTI1_TRIGOUTSTATUS	Read	8	0x00	See CTI Trigger Out Status Register, CTITRIGOUTSTATUS, 0x134
0x138	CTI1_CHINSTATUS	Read	4	-	See CTI Channel In Status Register, CTICHINSTATUS, 0x138
0x13C	CTI1_CHOUTSTATUS	Read	4	0x0	See CTI Channel Out Status Register, CTICHOUTSTATUS, 0x13C
0x140	CTI1_GATE	Read/Write	4	0xF	See Enable CTI Channel Gate Register, CTIGATE, 0x140
0x144	CTI1_ASICCTL	Read/Write	8	0x00	See External Multiplexor Control Register, ASICCTL, 0x144

Table 6-3 Summary of CTI registers

Offset	Name	Type	Width	Reset value	Description
0xEDC	CTI1_ITCHINACK	Write	4	0x0	See ITCHINACK Register, 0xEDC
0xEE0	CTI1_ITTRIGINACK	Write	8	0x00	See ITTRIGINACK Register, 0xEE0
0xEE4	CTI1_ITCHOUT	Write	4	0x0	See ITCHOUT Register, 0xEE4
0xEE8	CTI1_ITTRIGOUT	Write	8	0x00	See ITTRIGOUT Register, 0xEE8
0xEEC	CTI1_ITCHOUTACK	Read	4	0x0	See ITCHOUTACK Register, 0xEEC
0xEF0	CTI1_ITTRIGOUTACK	Read	8	0x00	See ITTRIGOUTACK Register, 0xEF0
0xEF4	CTI1_ITCHIN	Read	4	0x0	See ITCHIN Register, 0xEF4
0xEF8	CTI1_ITTRIGIN	Read	8	0x00	See ITTRIGIN Register, 0xEF8
0xEFC -0xF7C	-	-	-	-	Reserved
0xF00	CTI1_ITCTRL	Read/Write	1	0x0	See ECT CoreSight defined registers
0xFA0	CTI1_CLAIMSET	Read/Write	4	0xF	
0xFA4	CTI1_CLAIMCLR	Read/Write	4	0x0	
0xFB0	CTI1_LAR	Write	32	-	
0xFB4	CTI1_LSR	Read	2	0x0/0x3	
0xFB8	CTI1_AUTHSTATUS	Read	4	0x5	
0xFC0-0xFC4	-	-	-	-	Reserved
0xFC8	CTI1_DEVID	Read	20	0x40800	See ECT CoreSight defined registers
0xFCC	CTI1_DEVTYPE	Read	8	0x14	See ECT CoreSight defined registers
0xFD0	CTI1_PIDR4	Read	8	0x04	
0xFD4	PeripheralID5	-	-	-	Reserved
0xFD8	PeripheralID6	-	-	-	Reserved
0xFDC	PeripheralID7	-	-	-	Reserved
0xFE0	CTI1_PIDR0	Read	8	0x06	See ECT CoreSight defined registers
0xFE4	CTI1_PIDR1	Read	8	0xB9	
0xFE8	CTI1_PIDR2	Read	8	0x2B	
0xFEC	CTI1_PIDR3	Read	8	0x00	
0xFF0	CTI1_CIDR0	Read	8	0x0D	
0xFF4	CTI1_CIDR1	Read	8	0x90	
0xFF8	CTI1_CIDR2	Read	8	0x05	
0xFFC	CTI1_CIDR3	Read	8	0xB1	

6.4.1.2 CTI1 Registers

0x01A02000 QDSS_CTI1_CONTROL

Type: Read/Write
Reset State: 0x0

CTI control register enables the CTI

QDSS_CTI1_CONTROL

Bits	Name	Description
31:1	RESERVED_31_1	Reserved RAZ DNM.
0	GLBEN	Enables or disables the ECT: When disabled, all cross triggering mapping logic functionality is disabled for this processor. 0x0: disabled (reset) 0x1: enabled.

0x01A02010 QDSS_CTI1_INTACK

Type: Write
Reset State: Not readable

QDSS_CTI1_INTACK

Bits	Name	Description
31:8	RESERVED_31_8	Reserved RAZ DNM.
7:0	INTACK	Acknowledges the corresponding CTITRIGOUT output: There is one bit of the register for each CTITRIGOUT output. 0x1: CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW. 0x0: no effect.

0x01A02014 QDSS_CTI1_APPSET

Type: Read/Write
Reset State: 0x0

QDSS_CTI1_APPSET

Bits	Name	Description
31:4	RESERVED_31_4	Reserved RAZ DNM.

QDSS_CTI1_APPSET (cont.)

Bits	Name	Description
3:0	APPSET	Setting a bit HIGH generates a channel event for the selected channel. Read: Write: There is one bit of the register for each channel. 0x0: application trigger inactive (reset) 0x1: application trigger active. 0x0: no effect 0x1: generate channel event.

0x01A02018 QDSS_CTI1_APPCLEAR

Type: Write
Reset State: 0x0

QDSS_CTI1_APPCLEAR

Bits	Name	Description
31:4	RESERVED_31_4	Reserved RAZ DNM.
3:0	APPCLEAR	Clears corresponding bits in the CTIAPPSET register. There is one bit of the register for each channel. 0x1: application trigger disabled in the CTIAPPSET register 0x0: no effect.

0x01A0201C QDSS_CTI1_APPPULSE

Type: Write
Reset State: 0x0

QDSS_CTI1_APPPULSE

Bits	Name	Description
31:4	RESERVED	Reserved RAZ DNM.
3:0	APPULSE	Setting a bit HIGH generates a channel event pulse for the selected channel. Write: There is one bit of the register for each channel. 0x1: channel event pulse generated for one CTICLK period 0x0: no effect.

0x01A02020+ 0x4*n QDSS_CTI1_INENn, n=[0..7]

Type: Read/Write
Reset State: 0x00

NOTE 8 registers

QDSS_CTI1_INENn

Bits	Name	Description
31:4	RESERVED	Reserved RAZ DNM.
3:0	TRIGINEN	Enables a cross trigger event to the corresponding channel when an CTITRIGIN is activated. There is one bit of the register for each of the four channels. For example in register CTIINEN0, TRIGINEN0 set to 1 enables CTITRIGIN onto channel 0. 0x1: enables the CTITRIGIN signal to generate an event on the respective channel of the CTM. 0x0: disables the CTITRIGIN signal from generating an event on the respective channel of the CTM.

0x01A020A0+ 0x4*n QDSS_CTI1_OUTENn, n=[0..7]

Type: Read/Write
Reset State: 0x00

NOTE 8 registers

QDSS_CTI1_OUTENn

Bits	Name	Description
31:4	RESERVED	Reserved RAZ DNM.
3:0	TRIGOUTEN	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate an CTITRIGOUT output: There is one bit for each of the four channels. For example in register CTIOUTEN0, enabling bit 0 enables CTICHIN0 to cause a trigger event on the CTITRIGOUT0 output. 0x0: the channel input_1 (CTICHIN from the CTM is not routed to the CTITRIGOUT output) 0x1: the channel input_2 (CTICHIN from the CTM is routed to the CTITRIGOUT output.)

0x01A02130 QDSS_CTI1_TRIGINSTATUS

Type: Read
Reset State: Undefined

QDSS_CTI1_TRIGINSTATUS

Bits	Name	Description
31:8	RESERVED	Reserved RAZ DNM.
7:0	TRIGINSTATUS	Shows the status of the CTITRIGIN inputs: Because the register provides a view of the raw CTITRIGIN inputs, the reset value is unknown. There is one bit of the register for each trigger input. 0x1: CTITRIGIN is active 0x0: CTITRIGIN is inactive.

0x01A02134 QDSS_CTI1_TRIGOUTSTATUS

Type: Read
Reset State: 0x00

QDSS_CTI1_TRIGOUTSTATUS

Bits	Name	Description
31:8	RESERVED	Reserved RAZ DNM.
7:0	TRIGOUTSTATUS	Shows the status of the CTITRIGOUT outputs. There is one bit of the register for each trigger output. 0x1: CTITRIGOUT is active 0x0: CTITRIGOUT is inactive (reset.)

0x01A02138 QDSS_CTI1_CHINSTATUS

Type: Read
Reset State: Undefined

QDSS_CTI1_CHINSTATUS

Bits	Name	Description
31:4	RESERVED	Reserved RAZ DNM.
3:0	CTICHINSTATUS	Shows the status of the CTICHIN inputs: Because the register provides a view of the raw CTICHIN inputs from the CTM, the reset value is unknown. There is one bit of the register for each channel input. 0x1: CTICHIN is active 0x0: CTICHIN is inactive.

0x01A0213C QDSS_CTI1_CHOUTSTATUS

Type: Read
Reset State: 0x0

QDSS_CTI1_CHOUTSTATUS

Bits	Name	Description
31:4	RESERVED	Reserved RAZ DNM.
3:0	CTICHOUTSTATUS	Shows the status of the CTICHOUT outputs. There is one bit of the register for each channel output. 0x1: CTICHOUT is active 0x0: CTICHOUT is inactive (reset.)

0x01A02140 QDSS_CTI1_GATE

Type: Read/Write
Reset State: 0xF

QDSS_CTI1_GATE

Bits	Name	Description
31:4	RESERVED	Reserved RAZ DNM.
3	CTIGATEEN3	Enable CTICHOUT3. Set to 0 to disable channel propagation.
2	CTIGATEEN2	Enable CTICHOUT2. Set to 0 to disable channel propagation.
1	CTIGATEEN1	Enable CTICHOUT1. Set to 0 to disable channel propagation.
0	CTIGATEEN0	Enable CTICHOUT0. Set to 0 to disable channel propagation.

0x01A02144 QDSS_CTI1_ASICCTL

Type: Read/Write
Reset State: 0x00

QDSS_CTI1_ASICCTL

Bits	Name	Description
31:8	RESERVED	Reserved RAZ DNM.
7:0	ASICCTL	Implementation-defined ASIC control, value written to the register is output on ASICCTL7:0. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM.

0x01A02EDC QDSS_CTI1_ITCHINACK

Type: Write
Reset State: 0x0

QDSS_CTI1_ITCHINACK

Bits	Name	Description
31:4	RESERVED	Reserved
3:0	CTCHINACK	Set the value of the CTCHINACK outputs

0x01A02EE0 QDSS_CTI1_ITTRIGINACK

Type: Write
Reset State: 0x00

QDSS_CTI1_ITTRIGINACK

Bits	Name	Description
31:8	RESERVED	Reserved
7:0	CTTRIGINACK	Set the value of the CTTRIGINACK outputs

0x01A02EE4 QDSS_CTI1_ITCHOUT

Type: Write
Reset State: 0x0

QDSS_CTI1_ITCHOUT

Bits	Name	Description
31:4	RESERVED	Reserved
3:0	CTCHOUT	Set the value of the CTCHOUT outputs

0x01A02EE8 QDSS_CTI1_ITTRIGOUT

Type: Write
Reset State: 0x00

QDSS_CTI1_ITTRIGOUT

Bits	Name	Description
31:8	RESERVED	Reserved
7:0	CTTRIGOUT	Set the value of the CTTRIGOUT outputs

0x01A02EEC QDSS_CTI1_ITCHOUTACK

Type: Read
Reset State: 0x0

QDSS_CTI1_ITCHOUTACK

Bits	Name	Description
31:4	RESERVED	Reserved
3:0	CTCHOUTACK	Read the values of the CTCHOUTACK inputs

0x01A02EF0 QDSS_CTI1_ITTRIGOUTACK

Type: Read
Reset State: 0x00

QDSS_CTI1_ITTRIGOUTACK

Bits	Name	Description
31:8	RESERVED	Reserved
7:0	CTTRIGOUTACK	Read the values of the CTTRIGOUTACK inputs

0x01A02EF4 QDSS_CTI1_ITCHIN

Type: Read
Reset State: 0x0

QDSS_CTI1_ITCHIN

Bits	Name	Description
31:4	RESERVED	Reserved
3:0	CTCHIN	Read the values of the CTCHIN inputs

0x01A02EF8 QDSS_CTI1_ITTRIGIN

Type: Read
Reset State: 0x00

QDSS_CTI1_ITTRIGIN

Bits	Name	Description
31:8	RESERVED	Reserved
7:0	CTTRIGIN	Read the values of the CTTRIGIN inputs

0x01A02F00 QDSS_CTI1_ITCTRL

Type: Read/Write
Reset State: 0x0

Reset Mask: 0x00000001

Used to enable topology detection. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for integration testing and topology solving. Refer to the CoreSight Architecture Specification for more information, at http://www.arm.com/products/system-ip/coresight/index.php.

NOTE When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

QDSS_CTI1_ITCTRL

Bits	Name	Description
31:1	RESERVED	Reserved
0	INTEGRATION_MODE	Enables the component to switch from functional mode to integration mode and back. If no integration functionality is implemented, this register must read as zero. 0x1: INTEGRATION_MODE (Enable integration mode.) 0x0: FUNCTIONAL_MODE (Disable integration mode.)

0x01A02FA0 QDSS_CTI1_CLAIMSET

Type: Read/Write
Reset State: 0xF

This is used in conjunction with Claim Tag Clear Register, CTICLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

QDSS_CTI1_CLAIMSET

Bits	Name	Description
3:0	CLAIMSET	On write: Each bit is considered separately: 0 = no effect, 1 = set this bit in the claim tag. On Read: This claim tag bit is implemented 0xF: CLAIM_TAG_IMPLEMENTED_BITS (These bits are present within the claim tag field)

0x01A02FA4 QDSS_CTI1_CLAIMCLR

Type: Read/Write
Reset State: 0x0

This register is used in conjunction with Claim Tag Set Register, CTICLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

QDSS_CTI1_CLAIMCLR

Bits	Name	Description
3:0	CLAIMCLR	On Write: Each bit is considered separately: 0 = no effect, 1 = clear this bit in the claim tag. On Read: The value present reflects the current setting of the Claim Tag.

0x01A02FB0 QDSS_CTI1_LAR

Type: Write
Reset State: Not readable

This register is used to enable write access to device registers.

QDSS_CTI1_LAR

Bits	Name	Description
31:0	ACCESS_W	A write of 0xC5ACCE55 enables further write access to this device. An invalid write has the effect of removing write access. 0xC5ACCE55: UNLOCK (unlock the protection register to enable write access)

0x01A02FB4 QDSS_CTI1_LSR

Type: Read
Reset State: 0x0/0x3

This indicates the status of the lock control mechanism. This lock prevents accidental writes by code under debug. This register must always be present although there might not be any lock access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register, 0xFB0.

QDSS_CTI1_LSR

Bits	Name	Description
2	LOCKTYPE	Indicates if the Lock Access Register, 0xFB0, is implemented as 8-bit or 32-bit. 0x0: V_32_BIT (This component implements a 32-bit Lock Access Register.)
1	LOCKGRANT	Returns the current status of the Lock. 0x0: ACCESS_PERMITTED (Write access is allowed to this device.) 0x1: DEVICE_LOCKED (Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted.)
0	LOCKEXIST	Indicates that a lock control mechanism exists for this device. 0x0: LOCK_NOT_PRESENT (No lock control mechanism exists, writes to the Lock Access Register, 0xFB0, are ignored.) 0x1: LOCK_PRESENT (Lock control mechanism is present.)

0x01A02FB8 QDSS_CTI1_AUTHSTATUS

Type: Read
Reset State: 0x5

Reports the required security level and current status of those enables. Where functionality changes on a given security level, this change in status must be reported in this register.

QDSS_CTI1_AUTHSTATUS

Bits	Name	Description
7:6	SNID	Indicates the security level for secure non-invasive debug: 0x0: V_2_B10 (Functionality disabled) 0x3: V_2_B11 (Functionality enabled.)
5:4	SID	Indicates the security level for secure invasive debug: 0x0: V_2_B10 (Functionality disabled) 0x3: V_2_B11 (Functionality enabled.)
3:2	NSNID	Indicates the security level for non-secure non-invasive debug: 0x0: V_2_B10 (Functionality disabled) 0x3: V_2_B11 (Functionality enabled.)
1:0	NSID	Indicates the security level for non-secure invasive debug: 0x0: V_2_B10 (Functionality disabled) 0x3: V_2_B11 (Functionality enabled.)

0x01A02FC8 QDSS_CTI1_DEVID

Type: Read
Reset State: 0x40800

QDSS_CTI1_DEVID

Bits	Name	Description
31:20	RESERVED_31_20	Reserved.
19:16	NUMECTCHN	Number of ECT channels available. Always reads 0x4
15:8	NUMECTTRIG	Number of ECT triggers available. Always reads 0x08
7:5	RESERVED_7_5	Reserved.
4:0	EXTMUXNUM	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly.

0x01A02FCC QDSS_CTI1_DEVTYPE

Type: Read
Reset State: 0x14

Provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

QDSS_CTI1_DEVTYPE

Bits	Name	Description
7:4	SUB_TYPE	Sub-classification within the major category: 0x1: TRIGGER_MATRIX
3:0	MAJOR_TYPE	Major classification grouping for this debug or trace component: 0x4: DEBUG_CONTROL

0x01A02FD0 QDSS_CTI1_PIDR4

Type: Read
Reset State: 0x04

Part of the set of peripheral identification registers. Contains part of the designer identity and the memory footprint indicator.

QDSS_CTI1_PIDR4

Bits	Name	Description
7:4	FOURKB_COUNT	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB, this must read as 0x0, 4KB only. For 8KB set to 0x1, for 16KB set to 0x, for 32KB set to 0x3, and so on. 0x0: V_4KB (Indicates that the device only occupies 4KB of memory.)
3:0	JEP106_CONT	JEDEC continuation code indicating the designer of the component, together with the identity code. 0x4: ARM_JEP106_CONTINUATION_CODE (Indicates that ARMs JEDEC identity code is on the 5th bank.)

0x01A02FD4 QDSS_CTI1_PIDR5

Type: Read
Reset State: 0x00

Part of the set of peripheral identification registers.

QDSS_CTI1_PIDR5

Bits	Name	Description
7:0	RESERVED	Reserved RAZ/SBZP

0x01A02FD8 QDSS_CTI1_PIDR6

Type: Read
Reset State: 0x00

Part of the set of peripheral identification registers.

QDSS_CTI1_PIDR6

Bits	Name	Description
7:0	RESERVED	Reserved RAZ/SBZP

0x01A02FDC QDSS_CTI1_PIDR7

Type: Read
Reset State: 0x00

Part of the set of peripheral identification registers.

QDSS_CTI1_PIDR7

Bits	Name	Description
7:0	RESERVED	Reserved RAZ/SBZP

0x01A02FE0 QDSS_CTI1_PIDR0

Type: Read
Reset State: 0x06

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

QDSS_CTI1_PIDR0

Bits	Name	Description
7:0	PART_NUMBER_BITS7TO0	Bits [7:0] of the component part number. This is selected by the designer of the component. 0x62: CORESIGHT_STM_PART_NUMBER_7_0 (Lowest 8 bits of the Part Number, 0x962.)

0x01A02FE4 QDSS_CTI1_PIDR1

Type: Read
Reset State: 0xB9

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

QDSS_CTI1_PIDR1

Bits	Name	Description
7:4	JEP106_BITS3TO0	Bits [3:0] of the JEDEC identity code indicating the designer of the component, together with the continuation code. 0xB: ARM_JEP106_IDENTITY_CODE_7_0 (Lowest 4 bits of the JEP106 Identity Code.)
3:0	PART_NUMBER_BITS11TO8	Bits [11:8] of the component part number. This is selected by the designer of the component. 0x9: CORESIGHT_STM_PART_NUMBER_11_8 (Upper 4 bits of the Part Number, 0x907.)

0x01A02FE8 QDSS_CTI1_PIDR2

Type: Read
Reset State: 0x3B

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

QDSS_CTI1_PIDR2

Bits	Name	Description
7:4	REVISION	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is used as a look-up to establish the exact major and minor revision. 0x0: R0P0 (This device is at r0p0.)
3	JEDEC	Always set. Indicates that a JEDEC assigned value is used. 0x1: JEDEC_IDENTITY (The designer ID is specified by JEDEC http://www.jedec.org.)
2:0	JEP106_BITS6TO4	Bits [6:4] of the JEDEC identity code indicating the designer of the component, together with the continuation code. 0x3: ARM_JEP106_IDENTITY_CODE_6_4 (Upper 3 bits of the JEP106 Identity Code.)

0x01A02FEC QDSS_CTI1_PIDR3

Type: Read
Reset State: 0x00

Part of the set of Peripheral Identification registers. Contains the Rev and customer modified fields.

QDSS_CTI1_PIDR3

Bits	Name	Description
7:4	REVAND	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero. 0x0: NO_MODS (Indicates that there have been no metal fixes to this component.)
3:0	CUSTOMER_MODIFIED	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero. 0x0: NO_MODS (Indicates that there have been no modifications made.)

0x01A02FF0 QDSS_CTI1_CIDR0

Type: Read
Reset State: 0x0D

A component identification register, that indicates that the identification registers are present.

QDSS_CTI1_CIDR0

Bits	Name	Description
7:0	PREAMBLE	Contains bits [24:31] of the component identification. 0xD: V_0D (Identification value.)

0x01A02FF4 QDSS_CTI1_CIDR1

Type: Read
Reset State: 0x90

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

QDSS_CTI1_CIDR1

Bits	Name	Description
7:4	CLASS	Class of the component, for example, ROM table or CoreSight component. 0x9: CORESIGHT_COMPONENT (Indicates the component is a CoreSight component.)
3:0	PREAMBLE	Contains bits [19:16] of the component identification. 0x0: V_0 (Identification value.)

0x01A02FF8 QDSS_CTI1_CIDR2

Type: Read
Reset State: 0x05

A component identification register that indicates the identification registers are present.

QDSS_CTI1_CIDR2

Bits	Name	Description
7:0	PREAMBLE	Contains bits [15:8] of the component identification. 0x5: V_05 (Identification value.)

0x01A02FFC QDSS_CTI1_CIDR3

Type: Read
Reset State: 0xB1

A component identification register, that indicates that the identification registers are present.

QDSS_CTI1_CIDR3

Bits	Name	Description
7:0	PREAMBLE	Contains bits [7:0] of the component identification. 0xB1: B1 (Identification value.)

6.5 QDSS TPIU Registers (0x01A03000 QDSS_TPIU_BASE)

This section contains the QDSS TPIU registers.

6.5.1 CoreSight Component Registers

This section describes the CS component registers. This includes device specific registers, CS management registers, peripheral ID registers, and component ID registers. It is provided below for QCSR and FLAT file generation. However, the details of the registers can be found in the ARM documents, which provide more detailed information about these registeres, such as their usage and descriptive register bits information. You can find ARM documentation at http://infocenter.arm.com/help/index.jsp.

6.5.1.1 TPIU Registers

0x01A03000 QDSS_TPIU_SUPPORTED_PORT_SIZE

Type: Read
Reset State: 0xFFFFFFF

See Supported Port Size Register, 0x000

QDSS_TPIU_SUPPORTED_PORT_SIZE

Bits	Name	Description
31:0	DATA	

0x01A03004 QDSS_TPIU_CURRENT_PORT_SIZE

Type: Read/Write
Reset State: 0x0000001

See Current Port Size Register, 0x004

QDSS_TPIU_CURRENT_PORT_SIZE

Bits	Name	Description
31:0	DATA	

0x01A03100 QDSS_TPIU_SUPPORTED_TRIGGER_MODES

Type: Read
Reset State: 0x11F

See Supported Trigger Modes Register, 0x100

QDSS_TPIU_SUPPORTED_TRIGGER_MODES

Bits	Name	Description
31:18	RESERVED_1	Reserved RAZ/SBZP
17	TRGRUN	Trigger Counter running. A trigger has occurred but the counter is not at zero.
16	TRIGGERED	Triggered. A trigger has occurred and the counter has reached zero.
15:9	RESERVED_2	Reserved RAZ/SBZP
8	TCOUNT8	8-bit wide counter register implemented.
7:5	RESERVED	Reserved RAZ/SBZP
4	MULT64K	Multiply the Trigger Counter by 65536 supported.
3	MULT256	Multiply the Trigger Counter by 256 supported.
2	MULT16	Multiply the Trigger Counter by 16 supported.
1	MULT4	Multiply the Trigger Counter by 4 supported.
0	MULT2	Multiply the Trigger Counter by 2 supported.

0x01A03104 QDSS_TPIU_TRIGGER_COUNTER_VALUE

Type: Read/Write
Reset State: 0x00

See Trigger Counter Register, 0x104

QDSS_TPIU_TRIGGER_COUNTER_VALUE

Bits	Name	Description
31:8	RESERVED	Reserved RAZ/SBZP
7:0	TRIGCOUNT	8-bit counter value for the number of words to be output from the formatter before a trigger is inserted. Reset value is 0x00.

0x01A03108 QDSS_TPIU_TRIGGER_MULTIPLIER

Type: Read/Write
Reset State: 0x00

See Trigger Multiplier Register, 0x108

QDSS_TPIU_TRIGGER_MULTIPLIER

Bits	Name	Description
31:5	RESERVED	Reserved RAZ/SBZP
4	MULT64K	Multiply the Trigger Counter by 65536 (216)
3	MULT256	Multiply the Trigger Counter by 256 (28)
2	MULT16	Multiply the Trigger Counter by 16 (24)
1	MULT4	Multiply the Trigger Counter by 4 (22)
0	MULT2	Multiply the Trigger Counter by 2 (21)

0x01A03200 QDSS_TPIU_SUPPORTED_TEST_PATTERNM

Type: Read
Reset State: 0x3000F

See Supported Test Patterns/Modes Register, 0x200

QDSS_TPIU_SUPPORTED_TEST_PATTERNM

Bits	Name	Description
31:18	RESERVED_1	Reserved RAZ/SBZP
17	PCONTEN	Continuous mode
16	PTIMEEN	Timed mode
15:4	RESERVED_2	Reserved RAZ/SBZP
3	PATF0	FF/00 Pattern
2	PATA5	AA/55 Pattern
1	PATW0	Walking 0s Pattern
0	PATW1	Walking 1s Pattern

0x01A03204 QDSS_TPIU_CURRENT_TEST_PATTERNM

Type: Read/Write
Reset State: 0x00000

See Current Test Patterns/Modes Register, 0x204

QDSS_TPIU_CURRENT_TEST_PATTERNM

Bits	Name	Description
31:0	DATA	

0x01A03208 QDSS_TPIU_TEST_PATTERN_REPEAT_COUNTER

Type: Read/Write
Reset State: 0x00

See TPIU Test Pattern Repeat Counter Register, 0x208

QDSS_TPIU_TEST_PATTERN_REPEAT_COUNTER

Bits	Name	Description
31:8	RESERVED	Reserved RAZ/SBZP
7:0	PATTCOUNT	8-bit counter value to indicate the number of TRACECLKIN cycles that a pattern runs for before switching to the next pattern. Default value is 0.

0x01A03300 QDSS_TPIU_FORMATTER_AND_FLUSH_STATUS

Type: Read
Reset State: 0x2 or 0x6

See Formatter and Flush Status Register, 0x300

QDSS_TPIU_FORMATTER_AND_FLUSH_STATUS

Bits	Name	Description
31:3	RESERVED	Reserved RAZ/SBZP.
2	TCPRESENT	If this bit is set then TRACECTL is present. If no TRACECTL pin is available, that is, this bit is zero, then the data formatter must be used and only in continuous mode. This is constrained by the CSTPIU_TRACECTL_VAL Verilog define, which is not user modifiable, and the external tie-off TPCTL. If either constraint reports zero/LOW then no TRACECTL is present and this inability to use the pin is reflected in this register. See TRACECTL removal for more information.
1	FTSTOPPED	Formatter stopped. The formatter has received a stop request signal and all trace data and post-amble has been output. Any more trace data on the ATB interface is ignored and ATREADYS goes HIGH.
0	FLINPROG	Flush In Progress. This is an indication of the current state of AFVALIDS.

0x01A03304 QDSS_TPIU_FORMATTER_AND_FLUSH_CONTROL

Type: Read/Write
Reset State: 0x0000

See Formatter and Flush Control Register, 0x304

QDSS_TPIU_FORMATTER_AND_FLUSH_CONTROL

Bits	Name	Description
31:14	RESERVED_1	Reserved RAZ/SBZP.
13	STOPTRIG	Stop the formatter after a Trigger Event is observed. Reset to disabled, or zero.
12	STOPFL	Stop the formatter after a flush completes (return of AFREADYS). This forces the FIFO to drain off any part-completed packets. Setting this bit enables this function but this is clear on reset, or disabled.
11	RESERVED_2	Reserved RAZ/SBZP.
10	TRIGFL	Indicates a trigger on Flush completion on AFREADYS being returned.
9	TRIGEVT	Indicate a trigger on a Trigger Eventa.
8	TRIGIN	Indicate a trigger on TRIGIN being asserted.
7	RESERVED_3	Reserved RAZ/SBZP.
6	FONMAN	Manually generate a flush of the system. Setting this bit causes a flush to be generated. This is cleared when this flush has been serviced. This bit is clear on reset.
5	FONTRIG	Generate flush using Trigger event. Set this bit to cause a flush of data in the system when a Trigger Eventa occurs. Reset value is this bit clear.
4	FONFLIN	Generate flush using the FLUSHIN interface. Set this bit to enable use of the FLUSHIN connection. This is clear on reset.
3:2	RESERVED_4	Reserved RAZ/SBZP.
1	ENFCONT	Continuous Formatting, no TRACECTL. Embed in trigger packets and indicate null cycles using Sync packets. Reset value is this bit clear. Can only be changed when FtStopped is HIGH.
0	ENFTC	Enable Formatting. Do not embed Triggers into the formatted stream. Trace disable cycles and triggers are indicated by TRACECTL, where fitted. Reset value is this bit clear. Can only be changed when FtStopped is HIGH.

0x01A03308 QDSS_TPIU_FORMATTER_SYNCHRONIZATION_COUNTER

Type: Read/Write
Reset State: 0x040

See Formatter Synchronization Counter Register, 0x308

QDSS_TPIU_FORMATTER_SYNCHRONIZATION_COUNTER

Bits	Name	Description
31:12	RESERVED	Reserved RAZ/SBZP.
11:0	CYCCOUNT	12-bit counter value to indicate the number of complete frames between full synchronization packets. Default value is 64 (0x40).

0x01A03400 QDSS_TPIU_EXTCTL_IN_PORT

Type: Read
Reset State: Undefined

See TPIU EXCTL Port Registers

0x01A03404 QDSS_TPIU_EXTCTL_OUT_PORT

Type: Read/Write
Reset State: 0x00

See TPIU EXCTL Port Registers

0x01A03EE4 QDSS_TPIU_ITTRFLINACK

Type: Write
Reset State: Not readable

See Integration Test Trigger In and Flush In Acknowledge Register, ITTRFLINACK, 0xEE4

0x01A03EE8 QDSS_TPIU_ITTRFLIN

Type: Read
Reset State: Undefined

See Integration Test Trigger In and Flush In Register, ITTRFLIN, 0xEE8.

QDSS_TPIU_ITTRFLIN

Bits	Name	Description
31:2	RESERVED	Reserved RAZ/SBZP.
1	FLUSHIN	Read the value of FLUSHIN
0	TRIGIN	Read the value of TRIGIN

0x01A03EEC QDSS_TPIU_ITATBDATA0

Type: Read
Reset State: Undefined

See Integration Test ATB Data Register 0, ITATBDATA0, 0xEEC.

QDSS_TPIU_ITATBDATA0

Bits	Name	Description
31:5	B_1	Reserved
4	ATDATA_31	Read the value of ATDATAS[31]
3	ATDATA_23	Read the value of ATDATAS[23]
2	ATDATA_15	Read the value of ATDATAS[15]
1	ATDATA_7	Read the value of ATDATAS[7]
0	ATDATA_0	Read the value of ATDATAS[0]

0x01A03EF0 QDSS_TPIU_ITATBCTR2

Type: Write
Reset State: Not readable

See Integration Test ATB Control Register 2, ITATBCTR2, 0xEF0

0x01A03EF4 QDSS_TPIU_ITATBCTR1

Type: Read
Reset State: Undefined

See Integration Test ATB Control Register 1, ITATBCTR1, 0xEF4

0x01A03EF8 QDSS_TPIU_ITATBCTR0

Type: Read
Reset State: Undefined

See Integration Test ATB Control Register 0, ITATBCTR0, 0xEF8

0x01A03F00 QDSS_TPIU_ITMR

Type: Read/Write
Reset State: 0x0

See TPIU CoreSight management registers

0x01A03FA0 QDSS_TPIU_CLAIM_TAG_SET

Type: Read/Write
Reset State: 0xF

0x01A03FA4 QDSS_TPIU_CLAIM_TAG_CLR

Type: Read/Write
Reset State: 0x0

0x01A03FB4 QDSS_TPIU_LOCK_STATUS

Type: Read
Reset State: 0x0/0x3

0x01A03FB0 QDSS_TPIU_LOCK_ACCESS

Type: Write
Reset State: Not readable

0x01A03FB8 QDSS_TPIU_AUTH_STATUS

Type: Read
Reset State: 0x00

0x01A03FC8 QDSS_TPIU_DEVID

Type: Read
Reset State: 0x0A0

0x01A03FCC QDSS_TPIU_DEVTYPE_ID

Type: Read
Reset State: 0x11

0x01A03FD0 QDSS_TPIU_PID4

Type: Read
Reset State: 0x04

0x01A03FD4 QDSS_TPIU_PID5

Type: Read
Reset State: 0xXX (unused)

0x01A03FD8 QDSS_TPIU_PID6

Type: Read
Reset State: 0xXX (unused)

0x01A03FDC QDSS_TPIU_PID7

Type: Read
Reset State: 0xXX (unused)

0x01A03FE0 QDSS_TPIU_PID0

Type: Read
Reset State: 0x12

See TPIU CoreSight management registers

0x01A03FE4 QDSS_TPIU_PID1

Type: Read
Reset State: 0xB9

0x01A03FE8 QDSS_TPIU_PID2

Type: Read
Reset State: 0x4B

0x01A03FEC QDSS_TPIU_PID3

Type: Read
Reset State: 0x00

0x01A03FF0 QDSS_TPIU_CID0

Type: Read
Reset State: 0x0D

0x01A03FF4 QDSS_TPIU_CID1

Type: Read
Reset State: 0x90

0x01A03FF8 QDSS_TPIU_CID2

Type: Read
Reset State: 0x05

0x01A03FFC QDSS_TPIU_CID3

Type: Read
Reset State: 0xB1

6.6 QDSS TFUNNEL Registers (0x01A04000 QDSS_TFUNNEL_BASE)

QDSS TFUNNEL Registers
(0x01A04000 QDSS_TFUNNEL_BASE)

This section contains the QDSS Tfunnel registers.

6.6.1 CoreSight Component Registers

This section describes the CS component registers. This includes device specific registers, CS management registers, peripheral ID registers, and component ID registers. It is provided below for QCSR and FLAT file generation. However, the details of the registers can be found in the ARM documents, which provide more detailed information about these registers, such as their usage and descriptive register bits information. You can find ARM documentation at http://infocenter.arm.com/help/index.jsp.

6.6.1.1 CoreSight trace funnel registers summary

Table 6-4 is the summary of Trace Funnel registers.

Table 6-4 Trace Funnel registers summary

Offset	Type	Width	Reset value	Name	Description
0x000	Read/Write	12	0x300	CS_TFUNNEL_FUNCTL	CSTF Control Register, 0x000
0x004	Read/Write	24	0xFAC688	CS_TFUNNEL_PRICTL	CSTF Priority Control Register, 0x004
0xEEC	Read/Write	5	0x00	CS_TFUNNEL_ITATBDATA0	CSTF Integration Test Registers
0xEF0	Read/Write	2	0x0	CS_TFUNNEL_ITATBCTR2	CSTF Integration Test Registers
0xEF4	Read/Write	7	0x00	CS_TFUNNEL_ITATBCTR1	CSTF Integration Test Registers
0xEF8	Read/Write	10	0x000	CS_TFUNNEL_ITATBCTR0	CSTF Integration Test Registers
0xF00	Read/Write	1	0x0	CS_TFUNNEL_ITCTL	CoreSight management registers for CSTF
0xFA0	Read/Write	4	0xF	CS_TFUNNEL_CLAIMSET	
0xFA4	Read/Write	4	0x0	CS_TFUNNEL_CLAIMCLR	
0xFB0	Write	32	Not readable	CS_TFUNNEL_LOCKACCESS	
0xFB4	Read	3	0x0/0x3	CS_TFUNNEL_LOCKSTATUS	
0xFB8	Read	8	0x00	CS_TFUNNEL_AUTHSTATUS	
0xFC8	Read	8	0x28	CS_TFUNNEL_DEVICEID	
0xFCC	Read	8	0x12	CS_TFUNNEL_DEVICETYPE	
0xFD0	Read	8	0x04	CS_TFUNNEL_PERIPHID4	

Table 6-4 Trace Funnel registers summary

Offset	Type	Width	Reset value	Name	Description
0xFD4	Read	8	0x00	CS_TFUNNEL_PERIPHID5	
0xFD8	Read	8	0x00	CS_TFUNNEL_PERIPHID6	
0xFDC	Read	8	0x00	CS_TFUNNEL_PERIPHID7	
0xFE0	Read	8	0x08	CS_TFUNNEL_PERIPHID0	
0xFE4	Read	8	0xB9	CS_TFUNNEL_PERIPHID1	CoreSight management registers for CSTF
0xFE8	Read	8	0x1B	CS_TFUNNEL_PERIPHID2	
0xFEC	Read	8	0x00	CS_TFUNNEL_PERIPHID3	
0xFF0	Read	8	0x0D	CS_TFUNNEL_COMPID0	
0xFF4	Read	8	0x90	CS_TFUNNEL_COMPID1	
0xFF8	Read	8	0x05	CS_TFUNNEL_COMPID2	
0xFFC	Read	8	0xB1	CS_TFUNNEL_COMPID3	

6.6.1.2 CSTF Registers

This section describes the coresight trace funnel (CSTF) specific registers:

- CSTF control register
- CSTF priority control register

The CSTF control register and the CSTF priority control register can only be changed when the whole trace system is stopped.

0x01A04000 QDSS_CS_TFUNNEL_FUNCTL

Type: Read/Write
Clock: PCLKDBG
Reset State: 0x300

The coresight funnel control register enables the slave ports and defines the hold time of the slave ports. Hold time refers to the number of transactions that are output on the funnel master port from the same slave while that slave port ATVALIDSx is HIGH. Hold time does not refer to clock cycles in this context.

QDSS_CS_TFUNNEL_FUNCTL

Bits	Name	Description
31:12	RESERVED	

QDSS_CS_TFUNNEL_FUNCTL (cont.)

Bits	Name	Description
11:8	MINIMUM_HOLD_TIME	The formatting scheme can easily become inefficient if fast switching occurs, so, where possible, this must be minimized. If a source has nothing to transmit, then another source is selected irrespective of the minimum number of cycles. Reset is 0x3. The CSTF holds for the minimum hold time and one additional cycle.The maximum value that can be entered is 0xE and this equates to 15 cycles. 0xF is reserved.
7	ENABLE_SLAVE_PORT_7	Setting this bit enables slave, port 7. If the bit is not set, this has the effect of excluding the port from the priority selection scheme. The port is disabled on reset.
6	ENABLE_SLAVE_PORT_6	Setting this bit enables slave, port 6. If the bit is not set then this has the effect of excluding the port from the priority selection scheme. The port is disabled on reset.
5	ENABLE_SLAVE_PORT_5	Setting this bit enables slave, port 5. If the bit is not set then this has the effect of excluding the port from the priority selection scheme. The port is disabled on reset.
4	ENALBE_SLAVE_PORT_4	Setting this bit enables slave, port 4. If the bit is not set then this has the effect of excluding the port from the priority selection scheme. The port is disabled on reset.
3	ENABLE_SLAVE_PORT_3	Setting this bit enables slave, port 3. If the bit is not set then this has the effect of excluding the port from the priority selection scheme. The port is disabled on reset.
2	ENABLE_SLAVE_PORT_2	Setting this bit enables slave, port 2. If the bit is not set then this has the effect of excluding the port from the priority selection scheme. The port is disabled on reset.
1	ENABLE_SLAVE_PORT_1	Setting this bit enables slave, port 1. If the bit is not set then this has the effect of excluding the port from the priority selection scheme. The port is disabled on reset.
0	ENABLE_SLAVE_PORT_0	Setting this bit enables slave, port 0. If the bit is not set then this has the effect of excluding the port from the priority selection scheme. The port is disabled on reset.

0x01A04004 QDSS_CS_TFUNNEL_PRICTL

Type: Read/Write
Clock: PCLKDBG
Reset State: 0xFAC688

At reset the default configuration assigns priority 0 to port 0, and priority 1 to port 1. If the highest priority is given to a particular slave port, the corresponding port must be programmed with the lowest value. Typically this is likely to be a port that has more important data or that has a small FIFO and is, therefore, likely to overflow. If the lowest priority is given to a particular slave port, the corresponding slave port must be programmed with the highest value. Typically this is likely to be a device that has a large FIFO that is less likely to overflow, or a source that has information that is of lower importance. A port programmed with value 0 gets the highest priority. A port

programmed with value 7 gets the lowest priority. Priority must always go to the highest priority source that has valid data available, if enabled. If a priority value has been entered for multiple different slave ports, then the arbitration logic selects the lowest port number of them.

QDSS_CS_TFUNNEL_PRICTL

Bits	Name	Description
31:24	RESERVED	Reserved
23:21	PRIORITY_PORT7	Port7 priority value.
20:18	PRIORITY_PORT6	Port6 priority value.
17:15	PRIORITY_PORT5	Port5 priority value.
14:12	PRIORITY_PORT4	Port4 priority value.
11:9	PRIORITY_PORT3	Port3 priority value.
8:6	PRIORITY_PORT2	Port2 priority value.
5:3	PRIORITY_PORT1	Port1 priority value.
2:0	PRIORITY_PORT0	Priority value of the slave port 0. The value written into this location is the value that is assigned to the first slave port.

0x01A04EEC QDSS_CS_TFUNNEL_ITATBDATA0

Type: Read/Write
Clock: PDBGCLK
Reset State: 0x00

The integration test ATB Data 0 register performs different functions depending on whether the access is a read or a write.

- A write outputs data on ATDATAM
- A read returns the data from ATDATAS<n>, where <n> is defined by the status of the CSTF control register at 0x000. The read data is only valid when ATVALIDS<n> is HIGH

QDSS_CS_TFUNNEL_ITATBDATA0

Bits	Name	Description
31:5	RESERVED	Reserved
4	ATDATA_31	WRITE: When this bit is written, it sets the value of ATDATAM bit[31] READ : When this bit is read, it returns the value of ATDATAS<n> bit[31]
3	ATDATA_23	WRITE: When this bit is written, it sets the value of ATDATAM bit[23] READ : When this bit is read, it returns the value of ATDATAS<n> bit[23]
2	ATDATA_15	WRITE: When this bit is written, it sets the value of ATDATAM bit[15] READ : When this bit is read, it returns the value of ATDATAS<n> bit[15]

QDSS_CS_TFUNNEL_ITATBDATA0 (cont.)

Bits	Name	Description
1	ATDATA_7	WRITE: When this bit is written, it sets the value of ATDATAM bit[7] READ : When this bit is read, it returns the value of ATDATAS<n> bit[7]
0	ATDATA_0	WRITE: When this bit is written, it sets the value of ATDATAM bit[0] READ : When this bit is read, it returns the value of ATDATAS<n> bit[0] where <n> refers to the selected slave port that is achieved by programming the CSTF control register.

0x01A04EF0 QDSS_CS_TFUNNEL_ITATBCTR2

Type: Read/Write
Clock: PCLKDBG
Reset State: 0x0

The integration test ATB Control 2 register performs different functions depending on whether the access is a read or a write.

- A write outputs data on ATREADYS<n> and AFVALIDS<n>, where <n> is defined by the status of the CSTF Control Register at 0x00
- A read returns the data from ATREADYM and AFVALIDM

QDSS_CS_TFUNNEL_ITATBCTR2

Bits	Name	Description
31:2	RESERVED	Reserved
1	AFVALID	WRITE: When this bit is written, it sets the value of AFVALIDS<n> READ : When this bit is read, it returns the value of AFVALIDM
0	ATREADY	WRITE: When this bit is written, it sets the value of AFREADYS<n> READ : When this bit is read, it returns the value of ATREADYM where <n> refers to the selected slave port that is achieved by programming the CSTF control register.

0x01A04EF4 QDSS_CS_TFUNNEL_ITATBCTR1

Type: Read/Write
Clock: PDBGCLK
Reset State: 0x00

The integration test ATB Control 1 register performs different functions depending on whether the access is a read or a write.

- A write outputs data on ATIDM

- A read returns the data from ATIDS<n>, where <n> is defined by the status of the CSTF Control register at 0x000. The read data is only valid when ATVALIDS<n> is HIGH

QDSS_CS_TFUNNEL_ITATBCTR1

Bits	Name	Description
31:7	RESERVED	Reserved
6:0	ATID	WRITE: When this bit is written, it sets the value of ATIDM READ : When this bit is read, it returns the value of ATIDS<n> where <n> refers to the selected slave port that is achieved by programming the CSTF control register.

0x01A04EF8 QDSS_CS_TFUNNEL_ITATBCTR0

Type: Read/Write
Clock: PDBGCLK
Reset State: 0x000

The integration test ATB Control 0 register performs different functions depending on whether the access is a read or a write.

- Write sets the value of the ATVALIDM, AFREADYM, and ATBYTESM signals
- Read returns the value of the ATVALIDS<n>, AFREADYS<n>, and ATBYTESS<n> signals, where <n> is defined by the status of the CSTF Control register at 0x000. The read value of ATBYTESS<n> is only valid when ATVALIDS<n> is HIGH.

QDSS_CS_TFUNNEL_ITATBCTR0

Bits	Name	Description
31:10	RESERVED_1	
9:8	ATBYTES	WRITE: When this bit is written, it sets the value of ATBYTESM READ : When this bit is read, it returns the value of ATBYTESS<n>
7:2	RESERVED_2	
1	AFREADYS	WRITE: When this bit is written, it sets the value of AFREADYM READ : When this bit is read, it returns the value of AFREADYS<n>
0	ATVALID	WRITE: When this bit is written, it sets the value of ATVALIDM READ : When this bit is read, it returns the value of ATVALIDS<n> where <n> refers to the selected slave port that is achieved by programming the CSTF control register.

0x01A04F00 QDSS_CS_TFUNNEL_ITCTL

Type: Read/Write
Clock: PDBGCLK
Reset State: 0x0

QDSS_CS_TFUNNEL_ITCTL

Bits	Name	Description
31:1	RESERVED	
0	INTEGRATION_MODE	Integration Mode Control Register. 0x1: Integration Mode 0x0: Not in Integration Mode

6.6.1.3 CoreSight management registers for CSTF

0x01A04FA0 QDSS_CS_TFUNNEL_CLAIMSET

Type: Read/Write
Clock: PDBGCLK
Reset State: 0xF

This is used in conjunction with Claim Tag Clear Register, CS_TFUNNEL_CLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

QDSS_CS_TFUNNEL_CLAIMSET

Bits	Name	Description
3:0	CLAIMSET	

0x01A04FA4 QDSS_CS_TFUNNEL_CLAIMCLR

Type: Read/Write
Clock: PDBGCLK
Reset State: 0x0

This register is used in conjunction with Claim Tag Set Register. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

QDSS_CS_TFUNNEL_CLAIMCLR

Bits	Name	Description
3:0	CLAIMCLR	

6.6.1.4 Lock Registers

The Lock Registers prevent accidental access to the registers of CoreSight components. Software that is being debugged might accidentally write to memory used by CoreSight components. This might disable those components, making the software impossible to debug. The CoreSight programmer's model includes a Lock Status Register and a Lock Access Register to control software access to CoreSight components to ensure that the likelihood of accidental access to CoreSight components is extremely small.

0x01A04FB0 QDSS_CS_TFUNNEL_LOCKACCESS

Type: Write ONLY
Clock: PDBGCLK

QDSS_CS_TFUNNEL_LOCKACCESS

Bits	Name	Description
31:0	LOCKACCESS	

0x01A04FB4 QDSS_CS_TFUNNEL_LOCKSTATUS

Type: Read ONLY
Clock: PDBGCLK
Reset State: 0x3

QDSS_CS_TFUNNEL_LOCKSTATUS

Bits	Name	Description
31:3	RESERVED	
2	B_8_BIT_LOCK	
1	ACCESS	
0	LOCK_CONTROL	

6.6.1.5 Authentication Status Register

0x01A04FB8 QDSS_CS_TFUNNEL_AUTHSTATUS

Type: Read Only
Clock: PDBGCLK
Reset State: 0x00

QDSS_CS_TFUNNEL_AUTHSTATUS

Bits	Name	Description
31:0	RESERVED	

6.6.1.6 Identification Registers

0x01A04FC8 QDSS_CS_TFUNNEL_DEVICEID

Type: Read Only
Clock: PDBGCLK
Reset State: 0x28

QDSS_CS_TFUNNEL_DEVICEID

Bits	Name	Description
31:8	RESERVED	
7:4	PRIORITY_SCHEME	The CSTF implements a static priority scheme.
3:0	PORTCOUNT	This is the value of the Verilog define PORTCOUNT and represents the number of input ports connected. By default all 8 ports are connected. 0x0 and 0x1 are illegal values.

0x01A04FCC QDSS_CS_TFUNNEL_DEVICETYPE

Type: Read Only
Clock: PDBGCLK
Reset State: 0x12

QDSS_CS_TFUNNEL_DEVICETYPE

Bits	Name	Description
7:0	DEVICE_TYPE	

0x01A04FD0 QDSS_CS_TFUNNEL_PERIPHID4

Type: Read Only
Clock: PDBGCLK
Reset State: 0x04

QDSS_CS_TFUNNEL_PERIPHID4

Bits	Name	Description
7:4	B_4KB_COUNT	
3:0	JEP106_CONTINUATION	

0x01A04FD4 QDSS_CS_TFUNNEL_PERIPHID5

Type: Read Only
Clock: PDBGCLK
Reset State: 0x00

QDSS_CS_TFUNNEL_PERIPHID5

Bits	Name	Description
7:0	RESERVED	

0x01A04FD8 QDSS_CS_TFUNNEL_PERIPHID6

Type: Read Only
Clock: PDBGCLK
Reset State: 0x00

QDSS_CS_TFUNNEL_PERIPHID6

Bits	Name	Description
7:0	RESERVED	

0x01A04FDC QDSS_CS_TFUNNEL_PERIPHID7

Type: Read Only
Clock: PDBGCLK
Reset State: 0x00

QDSS_CS_TFUNNEL_PERIPHID7

Bits	Name	Description
7:0	RESERVED	

0x01A04FE0 QDSS_CS_TFUNNEL_PERIPHID0

Type: Read Only
Clock: PDBGCLK
Reset State: 0x08

QDSS_CS_TFUNNEL_PERIPHID0

Bits	Name	Description
7:0	DEVICE_NUM_7_0	

0x01A04FE4 QDSS_CS_TFUNNEL_PERIPHID1

Type: Read Only
Clock: PDBGCLK
Reset State: 0xB9

QDSS_CS_TFUNNEL_PERIPHID1

Bits	Name	Description
7:4	JEP106_IDENTITY_3_0	
3:0	DEVICE_NUM_11_8	

0x01A04FE8 QDSS_CS_TFUNNEL_PERIPHID2

Type: Read Only
Clock: PDBGCLK
Reset State: 0x1B

QDSS_CS_TFUNNEL_PERIPHID2

Bits	Name	Description
7:4	REVISION	
3	JEDEC	
2:0	JEP106_IDENTITY_6_4	

0x01A04FEC QDSS_CS_TFUNNEL_PERIPHID3

Type: Read Only
Clock: PDBGCLK
Reset State: 0x00

QDSS_CS_TFUNNEL_PERIPHID3

Bits	Name	Description
7:4	REV_AND	
3:0	CUSTOMER_MODIFIED	

0x01A04FF0 QDSS_CS_TFUNNEL_COMPID0

Type: Read Only
Clock: PDBGCLK
Reset State: 0x0D

QDSS_CS_TFUNNEL_COMPID0

Bits	Name	Description
7:0	PREAMBLE_7_0	

0x01A04FF4 QDSS_CS_TFUNNEL_COMPID1

Type: Read Only
Clock: PDBGCLK
Reset State: 0x90

QDSS_CS_TFUNNEL_COMPID1

Bits	Name	Description
7:4	PREAMBLE_15_12	
3:0	PREAMBLE_11_8	

0x01A04FF8 QDSS_CS_TFUNNEL_COMPID2

Type: Read Only
Clock: PDBGCLK
Reset State: 0x05

QDSS_CS_TFUNNEL_COMPID2

Bits	Name	Description
7:0	PREAMBLE_23_16	

0x01A04FFC QDSS_CS_TFUNNEL_COMPID3

Type: Read Only
Clock: PDBGCLK
Reset State: 0xB1

QDSS_CS_TFUNNEL_COMPID3

Bits	Name	Description
7:0	PREAMBLE_31_24	

6.7 QDSS ITM Registers (0x01A05000 QDSS_ITM_BASE)

This section contains the QDSS ITM registers.

6.7.1 CoreSight Component Registers

This section describes the CS component registers. This includes device specific registers, CS management registers, peripheral ID registers, and component ID registers. It is provided below for QCSR and FLAT file generation. However, the details of the registers can be found in the ARM documents, which provide more detailed information about these registers, such as their usage and descriptive register bits information. You can find ARM documentation at http://infocenter.arm.com/help/index.jsp.

6.7.1.1 CoreSight ITM Registers Summary

Table 6-5 is the summary of ITM registers.

NOTE ITM is for integration testing only.

Table 6-5 ITM register summary

Offset	Type	Width	Reset value	Name	Description
0x000-0x07C	Read/Write	32	0x00000000	ITM_STIMULUS_PORT_REGn n=[0..31]	See Stimulus registers
0xE00	Read/Write	32	0x00000000	ITM_TER	See Trace registers
0xE20	Read/Write	32	0x00000000	ITM_TTR	
0xE80	Read/Write	32	0x00000004	ITM_CR	See Control registers
0xE90	Read/Write	12	0x00000400	ITM_SCR	
0xEE4	Read	1	0x00000000	ITM_ITTRIGOUTACK	See Integration test registers
0xEE8	Write	1	Not readable	ITM_ITTRIGOUT	
0xEEC	Write	2	Not readable	ITM_IITATDATA	
0xEF0	R0	1	0x00000000	ITM_ITATCTL2	
0xEF4	Write	7	Not readable	ITM_ITATCTL1	
0xEF8	Write	2	Not readable	ITM_ITATCTL0	
0xF00	Read/Write	1	0x0	ITM_ITMODE_CONTROL_REGISTER	See CoreSight defined registers
0xFA0	Read/Write	4	0xFF	ITM_CLAIM_TAG_SET	
0xFA4	Read/Write	4	0x00	ITM_CLAIM_TAG_CLEAR	
0xFB0	Write	32	Not readable	ITM_LOCK_ACCESS	
0xFB4	Read	3	0x0/0x3	LOCK_STATUS	
0xFB8	Read	8	Not readable	ITM_AUTHENTICATION_STATUS	

Table 6-5 ITM register summary

Offset	Type	Width	Reset value	Name	Description
0xFC8	Read	13	0x20	ITM_DEVICE_ID	
0xFCC	Read	8	0x43	ITM_DEVICE_TYPE_IDENTIFIER	
0xFD0	Read	8	0x04	ITM_PERIPHERAL_ID4	See CoreSight defined registers
0xFD4	Read	8	0x00	ITM_PERIPHERAL_ID5	
0xFD8	Read	8	0x00	ITM_PERIPHERAL_ID6	
0xFDC	Read	8	0x00	ITM_PERIPHERAL_ID7	
0xFE0	Read	8	0x14	ITM_PERIPHERAL_ID0	
0xFE4	Read	8	0xB9	ITM_PERIPHERAL_ID1	
0xFE8	Read	8	0x1B	ITM_PERIPHERAL_ID2	
0xFEC	Read	8	0x00	ITM_PERIPHERAL_ID3	
0xFF0	Read	8	0x0D	ITM_CID0	
0xFF4	Read	8	0x90	ITM_CID1	
0xFF8	Read	8	0x05	ITM_CID2	
0xFFC	Read	8	0xB1	ITM_CID3	

7.7.1.2 ITM Registers

0x01A05000+ 0x04*n QDSS_ITM_STIMULUS_PORT_REGn, n=[0..31]

Type: Read/Write
Reset State: 0x00000000

See Stimulus registers

NOTE n=32

QDSS_ITM_STIMULUS_PORT_REGn

Bits	Name	Description
31:0	DATA	

0x01A05E00 QDSS_ITM_TER

Type: Read/Write
Reset State: 0x00000000

See Trace registers

QDSS_ITM_TER

Bits	Name	Description
31:0	TRACE_ENABLE_REG	Bit mask to enable tracing on ITM stimulus port

0x01A05E20 QDSS_ITM_TTR

Type: Read/Write
Reset State: 0x00000000

QDSS_ITM_TTR

Bits	Name	Description
31:0	TRIGGER_MASK	Bit mask to trigger generation, TRIGOUT, on selected writes to the stimulus registers

0x01A05E80 QDSS_ITM_CR

Type: Read/Write
Reset State: 0x00000004

See Control registers

QDSS_ITM_CR

Bits	Name	Description
31:24	RESERVED_1	Reserved RAZ/SBZP
23	ITMBUSY	ITM is transmitting trace and FIFO is not empty
22:16	TRACEID	ATIDM[6:0] value
15:10	RESERVED_2	Reserved RAZ/SBZP
9:8	TSPRESCALE	Timestamp Prescaler, 0b00=/1, 0b01=/4, 0b10=/16, 0b11=/64
7:4	RESERVED	Reserved RAZ/SBZP
3	DWTEN	Enable DWT input port
2	SYNCEN	Enable sync packets
1	TSSEN	Enable timestamps, delta
0	ITMEN	Enable ITM stimulus, also acts as a global enable

0x01A05E90 QDSS_ITM_SCR

Type: Read/Write
Reset State: 0x00000400

QDSS_ITM_SCR

Bits	Name	Description
31:12	RESERVED	Reserved RAZ/SBZP
11:0	SYNC_COUNT	Counter value for time between synchronization markers

0x01A05EE4 QDSS_ITM_ITTRIGOUTACK

Type: Read
Reset State: 0x00000000

See Integration test registers

QDSS_ITM_ITTRIGOUTACK

Bits	Name	Description
31:1	RESERVED	Reserved RAZ/SBZP
0	ITTRIGOUTACK	Read the value of TRIGOUTACK

0x01A05EE8 QDSS_ITM_ITTRIGOUT

Type: Write
Reset State: Not readable

Integration Test Trigger Out Register

QDSS_ITM_ITTRIGOUT

Bits	Name	Description
31:1	RESERVED	Reserved RAZ/SBZP
0	ITTRIGOUT	Set the value of TRIGOUT

0x01A05EEC QDSS_ITM_IITATDATA

Type: Write
Reset State: Not readable

Integration Test ATB Data Register 0

QDSS_ITM_IITATDATA

Bits	Name	Description
31:2	RESERVED	Reserved RAZ/SBZP
1	ITATDATAM7	Set the value of ATDATAM7
0	ITATDATAM0	Set the value of ATDATAM0

0x01A05EF0 QDSS_ITM_ITATCTL2

Type: Read
Reset State: 0x00000000

Integration Test ATB Control Register 2

QDSS_ITM_ITATCTL2

Bits	Name	Description
31:1	RESERVED	Reserved RAZ/SBZP
0	ITATREADYM	Read the value of ATREADYM

0x01A05EF4 QDSS_ITM_ITATCTL1

Type: Write
Reset State: Not readable

Integration Test ATB Control Register 1

QDSS_ITM_ITATCTL1

Bits	Name	Description
31:7	RESERVED	Reserved RAZ/SBZP
6:0	ITATIDM	Set the value of ATIDM6:0

0x01A05EF8 QDSS_ITM_ITATCTL0

Type: Write
Reset State: Not readable

Integration Test ATB Control Register 0

QDSS_ITM_ITATCTL0

Bits	Name	Description
31:2	RESERVED	Reserved RAZ/SBZP
1	ITAFREADYM	Set the value of AFREADYM
0	ITATVALIDM	Set the value of ATVALIDM

0x01A05F00 QDSS_ITM_ITMODE_CONTROL_REGISTER

Type: Read/Write
Reset State: 0x0

See CoreSight defined registers

QDSS_ITM_ITMODE_CONTROL_REGISTER

Bits	Name	Description
31:0	DATA	

0x01A05FA0 QDSS_ITM_CLAIM_TAG_SET

Type: Read/Write
Reset State: 0xFF

QDSS_ITM_CLAIM_TAG_SET

Bits	Name	Description
31:0	DATA	

0x01A05FA4 QDSS_ITM_CLAIM_TAG_CLEAR

Type: Read/Write
Reset State: 0x00

QDSS_ITM_CLAIM_TAG_CLEAR

Bits	Name	Description
31:0	DATA	

0x01A05FB0 QDSS_ITM_LOCK_ACCESS

Type: Write
Reset State: Not readable

QDSS_ITM_LOCK_ACCESS

Bits	Name	Description
31:0	DATA	

0x01A05FB4 QDSS_LOCK_STATUS

Type: Read
Reset State: 0x0/0x3

QDSS_LOCK_STATUS

Bits	Name	Description
31:0	DATA	

0x01A05FB8 QDSS_ITM_AUTHENTICATION_STATUS

Type: Read
Reset State: Not readable

QDSS_ITM_AUTHENTICATION_STATUS

Bits	Name	Description
31:0	DATA	

0x01A05FC8 QDSS_ITM_DEVICE_ID

Type: Read
Reset State: 0x20

QDSS_ITM_DEVICE_ID

Bits	Name	Description
31:0	DATA	

0x01A05FCC QDSS_ITM_DEVICE_TYPE_IDENTIFIER

Type: Read
Reset State: 0x43

QDSS_ITM_DEVICE_TYPE_IDENTIFIER

Bits	Name	Description
31:0	DATA	

0x01A05FD0 QDSS_ITM_PERIPHERAL_ID4

Type: Read
Reset State: 0x04

See CoreSight defined registers

QDSS_ITM_PERIPHERAL_ID4

Bits	Name	Description
31:0	DATA	

0x01A05FD4 QDSS_ITM_PERIPHERAL_ID5

Type: Read
Reset State: 0x00

QDSS_ITM_PERIPHERAL_ID5

Bits	Name	Description
31:0	RESERVED	

0x01A05FD8 QDSS_ITM_PERIPHERAL_ID6

Type: Read
Reset State: 0x00

QDSS_ITM_PERIPHERAL_ID6

Bits	Name	Description
31:0	RESERVED	

0x01A05FDC QDSS_ITM_PERIPHERAL_ID7

Type: Read
Reset State: 0x00

QDSS_ITM_PERIPHERAL_ID7

Bits	Name	Description
31:0	RESERVED	

0x01A05FE0 QDSS_ITM_PERIPHERAL_ID0

Type: Read
Reset State: 0x13

0x01A05FE4 QDSS_ITM_PERIPHERAL_ID1

Type: Read
Reset State: 0xB9

0x01A05FE8 QDSS_ITM_PERIPHERAL_ID2

Type: Read
Reset State: 0x2B

0x01A05FEC QDSS_ITM_PERIPHERAL_ID3

Type: Read
Reset State: 0x00

0x01A05FF0 QDSS_ITM_CID0

Type: Read
Reset State: 0x0D

0x01A05FF4 QDSS_ITM_CID1

Type: Read
Reset State: 0x90

0x01A05FF8 QDSS_ITM_CID2

Type: Read
Reset State: 0x05

0x01A05FFC QDSS_ITM_CID3

Type: Read
Reset State: 0xB1

6.8 QDSS STM Registers (0x01A06000 QDSS_STM_BASE)

This section contains the QDSS STM registers.

6.8.1 CoreSight Component Registers

This section describes the CS component registers. This includes device specific registers, CS management registers, peripheral ID registers, and component ID registers. It is provided below for QCSR and FLAT file generation. However, the details of the registers can be found in the ARM documents, which provide more detailed information about these registers, such as their usage and descriptive register bits information. You can find ARM documentation at http://infocenter.arm.com/help/index.jsp.

6.8.1.1 CoreSight STM registers overview

System Trace Macrocell (STM) is a recently added CoreSight component from the ARM IP technology.

6.8.1.2 STM Registers

0x01A06C04 QDSS_STMDMASTARTR

Type: Write
Reset State: Not readable

This Write register is used to start a DMA transfer.

A write of one when the DMA peripheral request interface is idle starts a DMA transfer. A write of zero has no effect. A write of one when the DMA peripheral request interface is active has no effect.

QDSS_STMDMASTARTR

Bits	Name	Description
0	START	Start a DMA transfer 0x1: START (Start a DMA transfer)

0x01A06C08 QDSS_STMDMASTOPR

Type: Write
Reset State: Not readable

This Write register is used to stop a DMA transfer.

A write of one stops an active DMA transfer. A write of zero has no effect. A write of one when the DMA peripheral request interface is idle has no effect.

QDSS_STMDMASTOPR

Bits	Name	Description
0	STOP	Stop an active DMA transfer 0x1: STOP (Stop an active DMA transfer)

0x01A06C0C QDSS_STMDMASTATR

Type: Read
Reset State: Undefined

This Read register is used to determine the status of the DMA peripheral request interface.

QDSS_STMDMASTATR

Bits	Name	Description
0	STATUS	Stop an active DMA transfer 0x0: IDLE (interface is idle) 0x1: ACTIVE (interface is active)

0x01A06C10 QDSS_STMDMACTLR

Type: Read/Write
Reset State: 0x00000000

Controls the DMA transfer request mechanism.

QDSS_STMDMACTLR

Bits	Name	Description
3:2	SENS	Determines the sensitivity of the DMA request to the current buffer level in the STM: 0x0: EMPTY (FIFO is less than 25% full) 0x1: V_25 (FIFO is less than 50% full) 0x2: V_50 (FIFO is less than 75% full) 0x3: V_75 (FIFO is less than 100% full)

0x01A06CFC QDSS_STMDMAIDR

Type: Read
Reset State: Undefined

This Read register indicates the DMA features of the STM.

QDSS_STMDMAIDR

Bits	Name	Description
11:8	VENDSPEC	The VENDSPEC field identifies any vendor specific modifications or mappings. 0x0: VENDSPEC (Vendor specific information.)
7:4	CLASSREV	The CLASSREV field identifies the revision of the programmers model. 0x0: REVISION_CONTROL (Revision.)
3:0	CLASS	The CLASS field identifies the programmers model. 0x2: CONTROL (DMA Control.)

0x01A06E00 QDSS_STMSPER

Type: Read/Write
Reset State: Undefined

This read/write only register is used to enable the stimulus registers to generate trace.

The register defines one bit per stimulus register. Writing 1 enables the appropriate stimulus port, writing 0 disables the appropriate stimulus port. This register is used in conjunction with the Software Enable Bank Select Register.

QDSS_STMSPER

Bits	Name	Description
31:0	SPE	Stimulus port enable, with one bit per stimulus port 0x0: stimulus port disabled 0x1: stimulus port enabled

0x01A06E20 QDSS_STMSPTER

Type: Read/Write
Reset State: Undefined

This register is used to enable trigger generation on writes to enabled stimulus port registers.

QDSS_STMSPTER

Bits	Name	Description
31:0	SPTE	Bit mask to enable trigger generation from the stimulus port registers, with one bit per stimulus port register 0x0: disabled 0x1: enabled

0x01A06E60 QDSS_STMSPSCR

Type: Read/Write
Reset State: Undefined

This register allows a debugger to program which stimulus ports the STMSPER and STMSPTER apply to.

QDSS_STMSPSCR

Bits	Name	Description
31:20	PORTSEL	This field defines which stimulus ports the STMSPTER and/or STMSPER apply to
1:0	PORTCTL	This defines how the port selection is applied: 0x0: NOT_USED (Port selection not used) 0x1: STMSPTER_ONLY (Port selection applies only to the STMSPTER) 0x2: RESERVED (Reserved) 0x3: STMSPER_AND_STMSPTER (Port selection applies to both the STMSPER and STMSPTER)

0x01A06E64 QDSS_STMSPMSCR

Type: Read/Write
Reset State: Undefined

This register allows a debugger to program which masters the STMSPSCR applies to.

QDSS_STMSPMSCR

Bits	Name	Description
22:15	MASTSEL	This field defines which master the STMSPSCR applies to
0	MASTCTL	This defines how the master is applied: 0x0: NOT_USED (Master selection not used) 0x1: STMSPSCR (Port selection applies to the STMSPSCR)

0x01A06E68 QDSS_STMSPOVERRIDER

Type: Read/Write
Reset State: Undefined

This register allows a debugger to override various features of the STM.

QDSS_STMSPOVERRIDER

Bits	Name	Description
31:15	PORTSEL	This field defines which stimulus ports the override controls apply to. This size of this field is defined by the number of implemented stimulus ports
2	OVERTS	This override requests all stimulus port writes that cause trace to be traced with a timestamp (where possible). As with normal operation, this does not ensure all packets are generated with timestamps. This field is independent of OVERCTL and PORTSEL. 0x0: DISABLED (Override not enabled) 0x1: ENABLED (Override enabled)
1:0	OVERCTL	This defines how the port selection is applied: 0x0: DISABLED (Override controls disabled) 0x1: GUARANTEED (Ports selected by PORTSEL always behave as Guaranteed transactions) 0x2: INVARIANT_TIMING (Ports selected by PORTSEL always behave as Invariant Timing transactions) 0x3: RESERVED (Reserved)

0x01A06E6C QDSS_STMSPMOVERRIDER

Type: Read/Write
Reset State: Undefined

This register allows a debugger to choose which masters the STMSPOVERRIDERR applies to.

QDSS_STMSPMOVERRIDER

Bits	Name	Description
22:15	MASTSEL	This field defines which master ports the override controls apply to. This size of this field is defined by the number of implemented masters
0	MASTCTL	This defines how the master selection is applied: 0x0: DISABLED (Override controls disabled. STMSPOVERRIDERR applies equally to all masters) 0x1: ENABLED (Master selection enabled. STMSPOVERRIDERR applies to the masters selected by MASTSEL)

0x01A06E70 QDSS_STMSPTRIGCSR

Type: Read/Write
Reset State: Undefined

This register is used to control the STM triggers caused by STMSPTER.

QDSS_STMSPTRIGCSR

Bits	Name	Description
4	ATBTRIGEN_DIR	When set, this bit enables the STM to use the ATID value of 0x7D when a Trigger Event on writes to TRIG location occurs. 0x0: DISABLE (Do not output ATB trace triggers on write to TRIG location) 0x1: ENABLE (Output ATB trace trigger for trigger on write to TRIG location)
3	ATBTRIGEN_TE	When set, this bit enables the STM to use the ATID value of 0x7D when a Trigger Event on match using STMSPTER occurs. 0x0: DISABLE (Do not output ATB trace trigger for trigger on match using STMSPTER) 0x1: ENABLE (Output ATB trace trigger for trigger on match using STMSPTER)
2	TRIGCLEAR	When TRIGCTL indicates single-shot mode, this bit is used to clear TRIGSTATUS. Writing a b1 to this bit when in multi-shot mode is Unpredictable. 0x0: NO_EFFECT (No effect) 0x1: CLEAR (Clears TRIGSTATUS if TRIGSTATUS is b1)
1	TRIGSTATUS	When TRIGCTL indicates single-shot mode, this indicates whether the single trigger has occurred: 0x0: NOT_OCCURRED (Trigger has not occurred) 0x1: OCCURRED (Trigger has occurred)
0	TRIGCTL	Trigger Control. 0x0: MULTI_SHOT (Triggers are multi-shot) 0x1: SINGLE_SHOT (Triggers are single-shot)

0x01A06E80 QDSS_STMTCSR

Type: Read/Write
Reset State: 0x00000004

Controls the STM settings.

QDSS_STMTCSR

Bits	Name	Description
23	BUSY	STM is busy, for example the STM trace FIFO is not empty: 0x0: IDLE (STM is not busy.) 0x1: BUSY (STM is busy.)

QDSS_STMTCSR (cont.)

Bits	Name	Description
22:16	TRACEID	ATB Trace ID.
5	COMPEN	Compression Enable for Stimulus Ports: 0x0: DISABLED (Compression disabled, data transfers are transmitted at the size of the transaction.) 0x1: ENABLED (Compression enabled, data transfers are compressed to save bandwidth.)
2	SYNCEN	STMSYNCR is implemented so this value is RAO. 0x1: RAO (STMSYNCR implemented.)
1	TSEN	This bit controls if timestamp requests are ignored or not: 0x0: DISABLE (Timestamping disabled. Requests for timestamp generation are ignored, and stimulus port writes selecting timestamping are treated as if it were not selected.) 0x1: ENABLE (Timestamping enabled. If stimulus writes select timestamping, a timestamp is output according to STPv2.)
0	EN	Global STM enable: 0x0: DISABLE (STM disabled) 0x1: ENABLE (STM enabled)

0x01A06E84 QDSS_STMTSSTIMR

Type: Write
Reset State: Not readable

This Write register is used to force the next packet caused by a stimulus port write to have a timestamp output.

QDSS_STMTSSTIMR

Bits	Name	Description
0	FORCETS	Force Timestamp Stimulus. A write to this register with this bit as b1 requests the next stimulus port write which causes trace to be upgraded to have a timestamp. Writes with this bit b0 are ignored. 0x1: FORCETS (Force Timestamp Stimulus)

0x01A06E8C QDSS_STMTSFREQR

Type: Read/Write
Reset State: Undefined

This Read/Write register is used to indicate the frequency of the timestamp counter. The unit of measurement is increments per second. When the STPv2 protocol is used, this register contains the

value output in the FREQ and FREQ_TS packets. The timestamp frequency is output in the STPv2 protocol at every synchronization point when STMTCSR.TSEN is b1.

QDSS_STMTSFREQR

Bits	Name	Description
31:0	FREQ	The timestamp frequency in Hz

0x01A06E90 QDSS_STMSYNCR

Type: Read/Write
Reset State: Undefined

This register controls the interval between synchronization packets, in terms of the number of bytes of trace generated.

This register only provides a hint of the desired synchronization frequency; implementations are permitted to be inaccurate.

Writing a value of 0x00000000 to this register disables the synchronization counter. However, any other IMPLEMENTATION DEFINED synchronizations mechanism continue to operate independently.

QDSS_STMSYNCR

Bits	Name	Description
12	MODE	Mode control: 0x0: N_BYTES (COUNT[11:0] defines a value N. Synchronization period is N bytes) 0x1: V_2_N_BYTES (COUNT[11:7] defines a value N. Synchronization period is 2^N bytes. N must be in the range of 12 to 27 inclusive and other values are Unpredictable)
11:2	COUNT	Counter value for the number of bytes between synchronization packets. Reads return the value of this register.

0x01A06E94 QDSS_STMAUXCR

Type: Read/Write
Reset State: 0x00000000

Used for IMPLEMENTATION DEFINED STM controls.

QDSS_STMAUXCR

Bits	Name	Description
4	AFREADYHIGH	Provides override control for the AFREADY output: 0x0: NO_OVERRIDE (No override, AFREADY is controlled by the state of the STM.) 0x1: OVERRIDE (Override, AFREADY is driven HIGH.)
3	CLKON	Provides override control for architectural clock gate enable: 0x0: NO_OVERRIDE (No override, clock gate is controlled by the state of STM.) 0x1: OVERRIDE (Override, clock is enabled.)
2	PRIORINVDIS	Controls arbitration between AXI and HW during flush: 0x0: INVERSION_ENABLED (Priority inversion, when AXI flush is finished, HW gets priority until HW flush is done) 0x1: INVERSION_DISABLED (Priority inversion disabled, AXI always has priority over HW.)
1	ASYNCPE	ASYNC priority: 0x0: DISABLE (ASYNC priority is always lower than trace.) 0x1: ENABLE (ASYNC priority escalates on second synchronization request.)
0	FIFOAF	Auto-flush: 0x0: DISABLED (Auto-flush disabled.) 0x1: ENABLED (Auto-flush enabled.)

0x01A06EA0 QDSS_STMSPFEAT1R

Type: Read
Reset State: 0x006587D1

Indicates the features of the STM.

QDSS_STMSPFEAT1R

Bits	Name	Description
23:22	SWOEN	STMTCSR.SWOEN support. 0x1: NOT_IMPLEMENTED (STMTCSR.SWOEN not implemented.)
21:20	SYNCEN	STMTCSR.SYNCEN support. 0x2: RAO (STMTCSR.SYNCEN implemented but always reads as b1.)
19:18	HWTEN	STMTCSR.HWTEN support. 0x1: NOT_IMPLEMENTED (STMTCSR.HWTEN not implemented.)
17:16	TSPRESCALE	Timestamp prescale support. 0x1: NOT_IMPLEMENTED (Timestamp prescale not implemented.)

QDSS_STMSPFEAT1R (cont.)

Bits	Name	Description
15:14	TRIGCTL	Trigger control support. 0x2: MULTI_SHOT_AND_SINGLE_SHOT (Multi-shot and single-shot triggers supported. STMTRIGCSR implemented.)
13:10	TRACEBUS	Trace bus support. 0x1: ATB_WITH_TRIGGER (CoreSight ATB plus ATB trigger support implemented. STMTCSR.TRACEID and STMTRIGCSR.ATBTRIGEN implemented.)
9:8	SYNC	STMSYNCR support 0x3: MODE (STMSYNCR implemented with MODE control.)
7	FORCETS	STMTSSTIMR support. 0x1: IMPLEMENTED (STMTSSTIMR bit implemented.)
6	TSFREQ	Timestamp frequency indication configuration. 0x1: RW (STMTSFREQR is Read/Write.)
5:4	TS	Timestamp support. 0x1: ABSOLUT (Absolute timestamps implemented.)
3:0	PROT	Protocol 0x1: STPV2 (STPv2 protocol.)

0x01A06EA4 QDSS_STMSPFEAT2R

Type: Read
Reset State: 0x000104F2

Indicates the features of the STM.

QDSS_STMSPFEAT2R

Bits	Name	Description
17:16	SPTYPE	Stimulus port type support. 0x1: EXTENDED_ONLY (Only Extended Stimulus Ports implemented.)
15:12	DSIZE	Fundamental data size. 0x0: V_32_BIT (32-bit data.)
10:9	SPTRTYPE	Stimulus port transaction type support. 0x2: INVARIANT_TIMING_AND_GUARANTEED (Both invariant timing and guaranteed transactions are supported)
8:7	PRIVMASK	STMPRIVMASKR support. 0x1: NOT_IMPLEMENTED (STMPRIVMASKR not implemented.)
6	SPOVERRIDE	STMOVERRIDER support. 0x1: IMPLEMENTED (STMSPOVERRIDER and STMSPMOVERRIDER implemented.)

QDSS_STMSPFEAT2R (cont.)

Bits	Name	Description
5:4	SPCOMP	Data compression on stimulus ports support. 0x3: PROGRAMMABLE (Data compression support is programmable. STMTCSR.COMPEN is implemented.)
2	SPER	STMSPER presence. 0x0: IMPLEMENTED (STMSPER is implemented.)
1:0	SPTER	STMSPTER support. 0x2: IMPLEMENTED (STMSPTER is implemented.)

0x01A06EA8 QDSS_STMSPFEAT3R

Type: Read
Reset State: 0x0000007F

Indicates the features of the STM.

QDSS_STMSPFEAT3R

Bits	Name	Description
6:0	NUMMAST	The number of stimulus ports masters implemented, minus 1. 0x7F: NUMMAST (128 masters are implemented.)

0x01A06EE8 QDSS_STMITTRIGGER

Type: Write
Reset State: Not readable

Integration Test for Cross-Trigger Outputs Register.

QDSS_STMITTRIGGER

Bits	Name	Description
3	ASYNCOUT_W	Sets the value of the ASYNCOUT output in integration mode: 0x1: HIGH (Drive logic 1 on ASYNCOUT output.) 0x0: LOW (Drive logic 0 on ASYNCOUT output.)
2	TRIGOUTHETE_W	Sets the value of the TRIGOUTHETE output in integration mode: 0x1: HIGH (Drive logic 1 on TRIGOUTHETE output.) 0x0: LOW (Drive logic 0 on TRIGOUTHETE output.)
1	TRIGOUTSW_W	Sets the value of the TRIGOUTSW output in integration mode: 0x1: HIGH (Drive logic 1 on TRIGOUTSW output.) 0x0: LOW (Drive logic 0 on TRIGOUTSW output.)

QDSS_STMITTRIGGER (cont.)

Bits	Name	Description
0	TRIGOUTSPTE_W	Sets the value of the TRIGOUTSPTE output in integration mode: 0x1: HIGH (Drive logic 1 on TRIGOUTSPTE output.) 0x0: LOW (Drive logic 0 on TRIGOUTSPTE output.)

0x01A06EEC QDSS_STMITATBDATA0

Type: Write
Reset State: Not readable

Controls the value of the ATDATAM output in integration mode:

QDSS_STMITATBDATA0

Bits	Name	Description
4	ATDATAM31_W	Set the value of the ATDATAM[31] output: 0x1: HIGH (Drive logic 1 on ATDATAM output.) 0x0: LOW (Drive logic 0 on ATDATAM output.)
3	ATDATAM23_W	Set the value of the ATDATAM[23] output: 0x1: HIGH (Drive logic 1 on ATDATAM output.) 0x0: LOW (Drive logic 0 on ATDATAM output.)
2	ATDATAM15_W	Set the value of the ATDATAM[15] output: 0x1: HIGH (Drive logic 1 on ATDATAM output.) 0x0: LOW (Drive logic 0 on ATDATAM output.)
1	ATDATAM7_W	Set the value of the ATDATAM[7] output: 0x1: HIGH (Drive logic 1 on ATDATAM output.) 0x0: LOW (Drive logic 0 on ATDATAM output.)
0	ATDATAM0_W	Set the value of the ATDATAM[0] output: 0x1: HIGH (Drive logic 1 on ATDATAM output.) 0x0: LOW (Drive logic 0 on ATDATAM output.)

0x01A06EF0 QDSS_STMITATBCTR2

Type: Read
Reset State: Undefined

Returns the value of the ATREADYM and AFVALIDM inputs in integration mode.

QDSS_STMITATBCTR2

Bits	Name	Description
1	AFVALIDM_R	Reads the value of the AFVALIDM input: 0x1: HIGH (Pin is at logic 1.) 0x0: LOW (Pin is at logic 0.)
0	ATREADYM_R	Reads the value of the ATREADYM input: 0x1: HIGH (Pin is at logic 1.) 0x0: LOW (Pin is at logic 0.)

0x01A06EF4 QDSS_STMITATBID

Type: Write
Reset State: Not readable

Controls the value of the ATIDM output in integration mode.

QDSS_STMITATBID

Bits	Name	Description
6:0	ATIDM_W	Sets the value of the ATIDM output.

0x01A06EF8 QDSS_STMITATBCTR0

Type: Write
Reset State: Not readable

Controls the value of the ATVALIDM, AFREADYM, and ATBYTESM outputs in integration mode.

QDSS_STMITATBCTR0

Bits	Name	Description
9:8	ATBYTESM_W	Sets the value of the ATBYTESM output: 0x3: V_11 (Drive logic 2b11 on the ATBYTESM output.) 0x2: V_10 (Drive logic 2b10 on the ATBYTESM output.) 0x1: V_01 (Drive logic 2b01 on the ATBYTESM output.) 0x0: V_00 (Drive logic 2b00 on the ATBYTESM output.)
1	AFREADYM_W	Sets the value of the AFREADYM output: 0x1: HIGH (Drive logic 1 on the AFREADYM output.) 0x0: LOW (Drive logic 0 on the AFREADYM output.)

QDSS_STMITATBCTR0 (cont.)

Bits	Name	Description
0	ATVALIDM_W	Sets the value of the ATVALIDM output: 0x1: HIGH (Drive logic 1 on the ATVALIDM output.) 0x0: LOW (Drive logic 0 on the ATVALIDM output.)

0x01A06F00 QDSS_STMITCTRL

Type: Read/Write
Reset State: 0x00000000

Used to enable topology detection. See the CoreSight Architecture Specification for more information. This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for integration testing and topology solving.

NOTE When a device has been in integration mode, it might not function with the original behavior. After performing integration or topology detection, you must reset the system to ensure correct behavior of CoreSight and other connected system components that are affected by the integration or topology detection.

QDSS_STMITCTRL

Bits	Name	Description
0	INTEGRATION_MODE	Enables the component to switch from functional mode to integration mode and back. If no integration functionality is implemented, this register must read as zero. 0x1: INTEGRATION_MODE (Enable integration mode.) 0x0: FUNCTIONAL_MODE (Disable integration mode.)

0x01A06FA0 QDSS_STMCLAIMSET

Type: Read/Write
Reset State: Undefined

This is used in conjunction with Claim Tag Clear Register, STMCLAIMCLR. This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.

QDSS_STMCLAIMSET

Bits	Name	Description
3:0	CLAIMSET	On write: Each bit is considered separately: 0 = no effect, 1 = set this bit in the claim tag. On Read: This claim tag bit is implemented 0xF: CLAIM_TAG_IMPLEMENTED_BITS (These bits are present within the claim tag field)

0x01A06FA4 QDSS_STMCLAIMCLR

Type: Read/Write
Reset State: Undefined

This register is used in conjunction with Claim Tag Set Register, STMCLAIMSET. This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read.

QDSS_STMCLAIMCLR

Bits	Name	Description
3:0	CLAIMCLR	On Write: Each bit is considered separately: 0 = no effect, 1 = clear this bit in the claim tag. On Read: The value present reflects the current setting of the Claim Tag.

0x01A06FB0 QDSS_STMLAR

Type: Write
Reset State: Not readable

This is used to enable write access to device registers.

QDSS_STMLAR

Bits	Name	Description
31:0	ACCESS_W	A write of 0xC5ACCE55 enables further write access to this device. An invalid write has the effect of removing write access. 0xC5ACCE55: UNLOCK (unlock the protection register to enable write access)

0x01A06FB4 QDSS_STMLSR

Type: Read
Reset State: Undefined (Value depends on PADDRDBG31)

This indicates the status of the lock control mechanism. This lock prevents accidental writes by code under debug. This register must always be present although there might not be any lock access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register, 0xFB0.

QDSS_STMLSR

Bits	Name	Description
2	LOCKTYPE	Indicates if the Lock Access Register, 0xFB0, is implemented as 8-bit or 32-bit. 0x0: V_32_BIT (This component implements a 32-bit Lock Access Register.)
1	LOCKGRANT	Returns the current status of the Lock. 0x0: ACCESS_PERMITTED (Write access is allowed to this device.) 0x1: DEVICE_LOCKED (Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted.)
0	LOCKEXIST	Indicates that a lock control mechanism exists for this device. 0x0: LOCK_NOT_PRESENT (No lock control mechanism exists, writes to the Lock Access Register, 0xFB0, are ignored.) 0x1: LOCK_PRESENT (Lock control mechanism is present.)

0x01A06FB8 QDSS_STMAUTHSTATUS

Type: Read
Reset State: 0x000000AA

Reports the required security level and current status of those enables. Where functionality changes on a given security level, this change in status must be reported in this register.

QDSS_STMAUTHSTATUS

Bits	Name	Description
7:6	SNID	Indicates the security level for secure non-invasive debug: 0x2: V_2_B10 (Functionality disabled) 0x3: V_2_B11 (Functionality enabled.)
5:4	SID	Indicates the security level for secure invasive debug: 0x2: V_2_B10 (Functionality disabled) 0x3: V_2_B11 (Functionality enabled.)

QDSS_STMAUTHSTATUS (cont.)

Bits	Name	Description
3:2	NSNID	Indicates the security level for non-secure non-invasive debug: 0x2: V_2_B10 (Functionality disabled) 0x3: V_2_B11 (Functionality enabled.)
1:0	NSID	Indicates the security level for non-secure invasive debug: 0x2: V_2_B10 (Functionality disabled) 0x3: V_2_B11 (Functionality enabled.)

0x01A06FC8 QDSS_STMDEVID

Type: Read
Reset State: 0x00010000

Indicates the capabilities of the CoreSight STM.

QDSS_STMDEVID

Bits	Name	Description
16:0	NUMSP	This value indicates the number of stimulus ports implemented. 0x10000: NUMBER_OF_PORTS (65536 stimulus ports implemented.)

0x01A06FCC QDSS_STMDEVTYPE

Type: Read
Reset State: 0x00000063

Provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

QDSS_STMDEVTYPE

Bits	Name	Description
7:4	SUB_TYPE	Sub-classification within the major category: 0x6: CORESIGHT_STM (This component generates trace based on software and hardware stimulus.)
3:0	MAJOR_TYPE	Major classification grouping for this debug or trace component: 0x3: TRACE_SOURCE (This component has ATB output.)

0x01A06FE0 QDSS_STMPIDR0

Type: Read
Reset State: 0x00000062

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number.

QDSS_STMPIDR0

Bits	Name	Description
7:0	PART_NUMBER_BITS7TO0	Bits [7:0] of the component part number. This is selected by the designer of the component. 0x62: CORESIGHT_STM_PART_NUMBER_7_0 (Lowest 8 bits of the Part Number, 0x962.)

0x01A06FE4 QDSS_STMPIDR1

Type: Read
Reset State: 0x000000B9

Part of the set of Peripheral Identification registers. Contains part of the designer specific part number and part of the designer identity.

QDSS_STMPIDR1

Bits	Name	Description
7:4	JEP106_BITS3TO0	Bits [3:0] of the JEDEC identity code indicating the designer of the component, together with the continuation code. 0xB: ARM_JEP106_IDENTITY_CODE_7_0 (Lowest 4 bits of the JEP106 Identity Code.)
3:0	PART_NUMBER_BITS11TO8	Bits [11:8] of the component part number. This is selected by the designer of the component. 0x9: CORESIGHT_STM_PART_NUMBER_11_8 (Upper 4 bits of the Part Number, 0x907.)

0x01A06FE8 QDSS_STMPIDR2

Type: Read
Reset State: 0x0000000B

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the product revision.

QDSS_STMPIDR2

Bits	Name	Description
7:4	REVISION	The Revision field is an incremental value starting at 0x0 for the first design of this component. This only increases by 1 for both major and minor revisions and is used as a look-up to establish the exact major and minor revision. 0x0: R0P0 (This device is at r0p0.)
3	JEDEC	Always set. Indicates that a JEDEC assigned value is used. 0x1: JEDEC_IDENTITY (The designer ID is specified by JEDEC http://www.jedec.org.)
2:0	JEP106_BITS6TO4	Bits [6:4] of the JEDEC identity code indicating the designer of the component, together with the continuation code. 0x3: ARM_JEP106_IDENTITY_CODE_6_4 (Upper 3 bits of the JEP106 Identity Code.)

0x01A06FEC QDSS_STMPIDR3

Type: Read
Reset State: 0x00000000

Part of the set of Peripheral Identification registers. Contains the RevAnd and Customer Modified fields.

QDSS_STMPIDR3

Bits	Name	Description
7:4	REVAND	This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is zero. It is recommended that component designers ensure this field can be changed by a metal fix if required, for example by driving it from registers that reset to zero. 0x0: NO_MODS (Indicates that there have been no metal fixes to this component.)
3:0	CUSTOMER_MODIFIED	Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is zero. 0x0: NO_MODS (Indicates that there have been no modifications made.)

0x01A06FD0 QDSS_STMPIDR4

Type: Read
Reset State: 0x00000004

Part of the set of Peripheral Identification registers. Contains part of the designer identity and the memory footprint indicator.

QDSS_STMPIDR4

Bits	Name	Description
7:4	FOURKB_COUNT	This is a 4-bit value that indicates the total contiguous size of the memory window used by this component in powers of 2 from the standard 4KB. If a component only requires the standard 4KB, this must read as 0x0, 4KB only. For 8KB set to 0x1, for 16KB set to 0x2, for 32KB set to 0x3, and so on. 0x0: V_4KB (Indicates that the device only occupies 4KB of memory.)
3:0	JEP106_CONT	JEDEC continuation code indicating the designer of the component, together with the identity code. 0x4: ARM_JEP106_CONTINUATION_CODE (Indicates that ARMs JEDEC identity code is on the 5th bank.)

0x01A06FF0 QDSS_STMCIDR0

Type: Read
Reset State: 0x0000000D

A component identification register, that indicates that the identification registers are present.

QDSS_STMCIDR0

Bits	Name	Description
7:0	PREAMBLE	Contains bits [24:31] of the component identification. 0xD: V_0D (Identification value.)

0x01A06FF4 QDSS_STMCIDR1

Type: Read
Reset State: 0x00000090

A component identification register, that indicates that the identification registers are present. This register also indicates the component class.

QDSS_STMCIDR1

Bits	Name	Description
7:4	CLASS	Class of the component, for example, ROM table or CoreSight component. 0x9: CORESIGHT_COMPONENT (Indicates the component is a CoreSight component.)
3:0	PREAMBLE	Contains bits [19:16] of the component identification. 0x0: V_0 (Identification value.)

0x01A06FF8 QDSS_STMCIDR2

Type: Read
Reset State: 0x00000005

A component identification register, that indicates that the identification registers are present.

QDSS_STMCIDR2

Bits	Name	Description
7:0	PREAMBLE	Contains bits [15:8] of the component identification. 0x5: V_05 (Identification value.)

0x01A06FFC QDSS_STMCIDR3

Type: Read
Reset State: 0x000000B1

A component identification register, that indicates that the identification registers are present.

QDSS_STMCIDR3

Bits	Name	Description
7:0	PREAMBLE	Contains bits [7:0] of the component identification. 0xB1: B1 (Identification value.)

6.9 QDSS M2VMT Registers (0x01A80000 QDSS_DAPM2VMT_BASE)

This section contains the QDSS M2VMT registers.

6.9.1 CoreSight Component Registers

This section describes the CS component registers. This includes device specific registers, CS management registers, peripheral ID registers, and component ID registers. It is provided below for QCSR and FLAT file generation. However, the details of the registers can be found in the ARM documents, which provide more detailed information about these registers, such as their usage and descriptive register bits information. You can find ARM documentation at http://infocenter.arm.com/help/index.jsp.

6.9.1.1 M2VMT Registers

NOTE These registers are independent of the DAP ROM Table.

0x01A80000+ 0x4*n QDSS_M2VMT_M2VMRn, n=[0..1]

Type: Read/Write
Clock: CC_QDSS_H_CLK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where n = NUM_M2VMT_ENTRIES from the design generics.

QDSS_M2VMT_M2VMRn

Bits	Name	Description
31:5	RESERVED	
4:0	VMID	Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRn address associations. n = NUM_M2VMT_ENTRIES from the design generic/parameter.

0x01A80F80 QDSS_M2VMT_CR

Type: Read/Write
Clock: CC_QDSS_H_CLK
Reset State: xxx0

Global configuration register.

Note: When REMOVE_M2VMT_RPU = ’1’, this register is not available. Also, bit [2], is not valid or has no effect when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT =’1’.

QDSS_M2VMT_CR

Bits	Name	Description
31:4	RESERVED	
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., in valid addresses) are recorded as such. Decode error is asserted when config access to un-implemented and/or unmapped register/address are done. Also, note that decode error is never asserted for client port accesses. When value is set to ’0’, i.e., ’do not record’, decode errors do not set the M2VMT_ESR[CFG], and M2VMT_EAR & M2VMT_SYNRn is not updated. When value is set to ‘1’, i.e., ’record’, decode errors set M2VMT_ESR[CFG] and M2VMT_EAR & M2VMT_SYNRn is updated with the address and the syndrome of the error. Reset State: x
2	RPUEIE	RPU error interrupt Enable: When set, configuration port errors are reported directly to the interrupt controller via the M2VMT_intr, interrupt output signal. Interrupt output is asserted if M2VMT_CR[RPUIE_EN] is ’1’ and ANY bit is set in the M2VMT_ESR register. **NOTE** Not valid or has no effect on the interrupt when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT=’1’. Reset State: x
1	RPUERE	RPU error report enable: When set, M2VMT reports configuration port errors to the requesting bus master, according to the respective port bus protocol. All error types reported via CRIF port uses a decode error, rather than a slave error. Regardless of the value of this field, both configuration port errors are terminated by the M2VMT as RAZ/WI, and are recorded in M2VMT_ESR register. Reset State: X

QDSS_M2VMT_CR (cont.)

Bits	Name	Description
0	RPUE	RPU Enable: Governs whether M2VMT_RPU_ACR is enabled to check the VMID of the configuration request. When set, all configuration port accesses are checked against M2VMT_RPU_ACR register for access permissions. It is cleared by reset. Set once SROT configures MID->VMID mapping tables. Reset State: 0

0x01A80F84 QDSS_M2VMT_EAR

Type: Read/Write
Clock: CC_QDSS_H_CLK
Reset State: unknown

When there is an error, this register holds the physical address of the errant transaction.

QDSS_M2VMT_EAR

Bits	Name	Description
31:0	PA	M2VMT Error Address Register: Physical address[31:0]. Contains the physical address of the errant request. Based on implementation, it may not contain the full 32 bits of the address. Captures the address on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. NOTE When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT = '1', this register is not available; and, therefore, access to this register are treated as RAZ/WI.

0x01A80F88 QDSS_M2VMT_ESR

Type: Read/Write to clear
Clock: CC_QDSS_H_CLK
Reset State: Undefined

M2VMT Error Status Register:

Captures the status upon M2VMT configuration errors, as determined by the M2VMT_RPU_ACR.

This register has read/write-clear access, meaning that reads simply provide a value in the register, while writes are performed by clearing those bits corresponding to '1's in the value written data, and leaving unchanged those bits corresponding to 0s n the written data. This prevents inadvertent

clearing of new errors when writing the register to clear an old error. A write with a ‘1’ set in a bit field results in clearing that bit. Writes with a 0 have no effect.

The presence of an asserted value on any bit in this register is what prompts the assertion when enabled by M2VMT_CR[RPUEIE] of the M2MVT’s interrupt output. Therefore these bits must be cleared by the interrupt handler. This is contrasted with the fields in the M2VMT_ESYNRn register, which are merely the ’syndrome’ of an error indicated by the M2VMT_ESR.

For M2VMT, there is only one defined error status bit in the M2VMT_SER (actually two counting multi-error).

QDSS_M2VMT_ESR

Bits	Name	Description
31	MULTI	Multi-Error: When set to ’1’, indicates that an additional error occurred while M2VMT_ESR is non-zero. The M2VMT_EAR,M2VMT_ESYNRn and M2VMT_ESR registers (with the exception of this bit) lock on the first error, and must be cleared to unlock. Therefore, the status and the syndrome of errors that occurred while M2VMT_ESR[CFG] is ’1’ are lost, i.e., syndrome register and status register only stores details of the first error.
30:1	RESERVED	
0	CFG	Configuration Port Error: When set to ’1’, indicates an error associated with a configuration port request. NOTE When REMOVE_M2VMT_RPU=’1’ OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT=’1’, this register is not available; and, therefore, access to this register is treated as RAZ/WI.

0x01A80F8C QDSS_M2VMT_ESRRESTORE

Type: Write Only/reads ignored
Clock: CC_QDSS_H_CLK
Reset State: unknown

QDSS_M2VMT_ESRRESTORE

Bits	Name	Description
31:0	M2VMT_ESRRTORE	M2VMT Error Status Register Restore This is just an aliased address for M2VMT_ESR, which provides direct write access (rather than write-clear) for restoration purpose NOTE When REMOVE_M2VMT_RPU=’1’ OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT=’1’, this register is not available; and, therefore, access to this register is treated as RAZ/WI.

0x01A80F90 QDSS_M2VMT_ESYNR0

Type: Read/Write
Clock: CC_QDSS_H_CLK
Reset State: undefined

Error Syndrome Register 0:

Captures the syndrome on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) ‘lock’ upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is ‘1’ are lost, i.e., the syndrome register and the status register only stores details of the first error.

QDSS_M2VMT_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request.
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request.
15:0	AMID	AMID[15:0] field of errant request. NOTE When REMOVE_M2VMT_RPU=’1’ OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT=”1”, this register is not available; and, therefore, access to this register is treated as RAZ/WI.

0x01A80F94 QDSS_M2VMT_ESYNR1

Type: Read/Write
Clock: CC_QDSS_H_CLK
Reset State: Undefined

Error Syndrome Register 1:

Captures syndrome upon M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) ‘lock’ upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is ‘1’ are lost., i.e., the syndrome register and the status register only stores details of the first error.

QDSS_M2VMT_ESYNR1

Bits	Name	Description
31	DCD	Decode: Indicates configuration port error due to invalid/ unrecognized/ unmapped/ unimplemented address (e.g., a reserved register address). Includes decode errors within the global address space. Also, note that decode error is never asserted for client port accesses.
30	AC	Access control: Indicates configuration port error due to lack of permission, as specified by the access control registers.
29:25	RESERVED_1	
24	AFULL	AFULL field of the errant request
23	AOOOWR	AOOOWR field of the errant request
22	AOOORD	AOOORD field of the errant request.
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request).
19	RESERVED_2	Reserved
18:16	ASIZE	ASIZE[2:0] field of the errant request).
15:12	ALEN	ALEN[3:0] field of the errant request.
11:10	ABURST	ABURST[1:0] field of the errant request.
9	RESERVED	Reserved
8	AWRITE	AWRITE field of the errant request.
7	AINST	AINST field of the errant request.
6	APROTNS	APROTNS field of the errant request.
5	APRIV	APRIV field of the errant request.
4	AINNERSHARED	AINNERSHARED field of the errant request.
3	ASHARED	ASHARED field of the errant request.
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

0x01A80FF4 QDSS_M2VMT_REV

Type: Read
Clock: CC_QDSS_H_CLK
Reset State: ’00010000’b

Reports the revision information for the M2VMT core and wrapper.

QDSS_M2VMT_REV

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	Major variant field. APQ8064: MAJOR = 0001.
3:0	MINOR	Minor variant field. MINOR = 0000.

0x01A80FF8 QDSS_M2VMT_IDR

Type: Read
Clock: CC_QDSS_H_CLK
Reset State: 0x2

Reports the size of the M2VMT table. It is a read-only register.

QDSS_M2VMT_IDR

Bits	Name	Description
31:9	RESERVED	
8:0	M2VMTSIZE	M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of Read/Write or other fields used to select mapping. M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

0x01A80FFC QDSS_M2VMT_RPU_ACR

Type: Read/Write
Clock: CC_QDSS_H_CLK
Reset State: Undefined

Using the incoming VMID, this register controls access to the global register space.

QDSS_M2VMT_RPU_ACR

Bits	Name	Description
31:0	RWE	M2VMT local RPU Access control Register. Each bit position corresponds to a VMID. When set to ‘1’, that VMID is granted VMID read/write access to the entire block of registers within the M2VMT 4 Kb global address space, including this register itself. In practice, this register designates the VMID(s) that can act as SROT (e.g., scorpion-secure) or pseudo SROT (e.g., RPM ARM11). NOTE When REMOVE_M2VMT_RPU=’1’, this register is not available; and, therefore, access to this register is treated as RAZ/WI.

7 EBI1 DIM Registers

7.1 Overview

Table 7-1 EBI1_DIM Bases

Base Name	Parent	Address
DIM_BD0_DIM_DQ_TOP_CFG	DIM_BD0_REG_BASE	0x1A780000
DIM_BC0_DIM_CA_TOP_CFG	DIM_BC0_REG_BASE	0x1AB40000
DIM_C01_DIM_CA_TOP_CFG	DIM_C01_REG_BASE	0x1AB80000
DIM_BD1_DIM_DQ_TOP_CFG	DIM_BD1_REG_BASE	0x1AC80000
DIM_BC1_DIM_CA_TOP_CFG	DIM_BC1_REG_BASE	0x1B040000
DIM_C11_DIM_CA_TOP_CFG	DIM_C11_REG_BASE	0x1B080000

7.2 DIM BD0 DQ Top Configuration Registers (0x1A780000 DIM_BD0_REG_BASE)

This section describes the BD0 DIM DQ TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1A780000 DIM_BD0_DIM_DQ_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_DQ_TOP_CFG register configures the following:

DIM_DQ_TOP_CFG

DIM_BD0_DIM_DQ_TOP_CFG

Bits	Name	Description
26	CDC_LDO_EN	Enablement of CDC LDO 1’b1 : Enabled 1’b0 : Disabled LDO and power provided from switches (default)
25	CDC_SWITCH_RC_EN	Enablement of CDC power RC (LPF) switch 1’b1 : Enabled 1’b0 : Disabled (default)
24	CDC_SWITCH_BYPASS_OFF	Enablement of CDC power bypass switch 1’b1 : Disabled 1’b0 : Enabled (default)
16	RCW_EN	Enablement of the Read Capture Window 1’b1 : Enable the RCW 1’b0 : Disabled (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1 : from Read CDCCAL 1’b0 : from Write CDCCAL (default)
12	DEBUG_BUS_EN	1’b1 : Enables the debug bus functionality 1’b0 : Disables the debug bus and drives all ’0’s on debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_dq[5:0] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend

DIM_BD0_DIM_DQ_TOP_CFG (cont.)

Bits	Name	Description
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1'b0) 1'b1 : with pipe extend (default) 1'b0 : without pipe extend
0	WR_CLK_SEL	Write clock select 1'b1 : With write CDC (default) 1'b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1A780004 DIM_BD0_DIM_DQ_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_DQ_HW_INFO register configures the following:

DIM_DQ_HW_INFO

DIM_BD0_DIM_DQ_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1A780008 DIM_BD0_DIM_DQ_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_DQ_HW_VERSION register configures the following:

DIM_DQ_HW_VERSION

DIM_BD0_DIM_DQ_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.

DIM_BD0_DIM_DQ_HW_VERSION (cont.)

Bits	Name	Description
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1A780010 DIM_BD0_DIM_DQ_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG0 register configures the following:

DIM_DQ_PAD_CFG0

DIM_BD0_DIM_DQ_PAD_CFG0

Bits	Name	Description
31	DQ_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	DQ_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	DQ_LV_MODE	Mode select for high/low voltage regime
28	DQ_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQ_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQ_PULL_B	Input pull control
21:20	DQ_NSLEW	Slew rate control bits for output path NMOS
17:16	DQ_PSLEW	Slew rate control bits for output path PMOS
13:12	DQ_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQ_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	DQ_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQ_ROUT	Impedance control bit settings for output driver
2:0	DQ_DCC	Duty cycle correction bits for output path

0x1A780014 DIM_BD0_DIM_DQ_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG1 register configures the following:

DIM_DQ_PAD_CFG1

DIM_BD0_DIM_DQ_PAD_CFG1

Bits	Name	Description
31	DQS_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
30	DQS_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	DQS_LV_MODE	Mode select for high/low voltage regime
28	DQS_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQS_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQS_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	DQS_NSLEW	Slew rate control bits for output path NMOS
17:16	DQS_PSLEW	Slew rate control bits for output path PMOS
13:12	DQS_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQS_PRXDEL	Delay control bits to increase strength of PMOS input drive
7	DQS_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQS_ROUT	Impedance control bit settings for output driver
2:0	DQS_DCC	Duty cycle correction bits for output path

0x1A780018 DIM_BD0_DIM_DQ_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_DQ_PAD_CFG2 register configures the DIM_DQ_PAD_CFG2.

DIM_BD0_DIM_DQ_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1A780020 DIM_BD0_DIM_DQ_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x1000FF11

The DIM_DQ_PAD_CFG3 register configures the DIM_DQ_PAD_CFG3.

DIM_BD0_DIM_DQ_PAD_CFG3

Bits	Name	Description
28	DQS_DIFF_MODE	DQS output mode control 1'b1 : differential output (default) 1'b0 : single-ended output; _n output is HIZ
27	RCW_ODT_ENA1	Enable ODT for RCW pad (when hp_mode=1)
26	RCW_ODT_ENA0	Enable ODT for RCW pad (when hp_mode=0)
25:24	RCW_ODT	Impedance control for on-die termination on RCW pad
23	DQ_ODT_ENA1	Enable ODT for DQ pads (when hp_mode=1)
22	DQ_ODT_ENA0	Enable ODT for DQ pads (when hp_mode=0)

DIM_BD0_DIM_DQ_PAD_CFG3 (cont.)

Bits	Name	Description
21:20	DQ_ODT	Impedance control for on-die termination on DQ pads
19	DQS_ODT_ENA1	Enable ODT for DQS pad (when hp_mode=1)
18	DQS_ODT_ENA0	Enable ODT for DQS pad (when hp_mode=0)
17:16	DQS_ODT	Impedance control for on-die termination on DQS pad
15:8	DQ_IE_OE	Enable both input receiver and output driver for all DQ pads
5	RCW_IE_OE	Enable both input receiver and output driver for RCW pad
4	DQS_IE_OE	Enable both input receiver and output driver for DQS pad
1	DM_IE	Input received enable for DM pad
0	DM_OE	Output driver enable for DM pad

0x1A780024 DIM_BD0_DIM_DQ_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG4 register configures the DIM_DQ_PAD_CFG4.

DIM_BD0_DIM_DQ_PAD_CFG4

Bits	Name	Description
31	RCW_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	RCW_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	RCW_LV_MODE	Mode select for high/low voltage regime
25:24	RCW_PULL_B	Input pull control
21:20	RCW_NSLEW	Slew rate control bits for output path NMOS
17:16	RCW_PSLEW	Slew rate control bits for output path PMOS
13:12	RCW_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	RCW_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	RCW_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	RCW_ROUT	Impedance control bit settings for output driver
2:0	RCW_DCC	Duty cycle correction bits for output path

0x1A780030 DIM_BD0_DIM_DQ_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG0 register configures the DIM_DQ_CDC_CTLR_CFG0.

DIM_BD0_DIM_DQ_CDC_CTLR_CFG0

Bits	Name	Description
25	STAGGER_CAL_ENA	1'b1: Stagger calibration of write and read CDCs once after the other to reduce peak voltage drop. 1'b0: Both write and read CDCs calibrated simultaneously This bit is introduced on the x2 core, so not present on x0 and x1 versions of DIM/PHY.
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1A780034 DIM_BD0_DIM_DQ_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG1 register configures the DIM_DQ_CDC_CTLR_CFG1.

DIM_BD0_DIM_DQ_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used.
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1.
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1.
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1.
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1.

0x1A780038 DIM_BD0_DIM_DQ_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG0 register configures the DIM_DQ_CDC_CAL_TIMER_CFG0.

DIM_BD0_DIM_DQ_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1A78003C DIM_BD0_DIM_DQ_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG1 register configures the DIM_DQ_CDC_CAL_TIMER_CFG1

DIM_BD0_DIM_DQ_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1A780040 DIM_BD0_DIM_DQ_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_REFCOUNT_CFG register configures DIM_DQ_CDC_REFCOUNT_CFG.

DIM_BD0_DIM_DQ_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1A780044 DIM_BD0_DIM_DQ_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_DQ_CDC_COARSE_CAL_CFG configures the DIM_DQ_CDC_COARSE_CAL_CFG

DIM_BD0_DIM_DQ_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1A780048 DIM_BD0_DIM_DQ_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_RSVD_CFG register configures the DIM_DQ_CDC_RSVD_CFG.

DIM_BD0_DIM_DQ_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1A78004C DIM_BD0_DIM_DQ_RD_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_OFFSET_CFG register configures the DIM_DQ_RD_CDC_OFFSET_CFG

DIM_BD0_DIM_DQ_RD_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1A780050 DIM_BD0_DIM_DQ_RD_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_DELAY_CFG register configures the DIM_DQ_RD_CDC_DELAY_CFG

DIM_BD0_DIM_DQ_RD_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1A780054 DIM_BD0_DIM_DQ_RD_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_MODE_CFG register configures the DIM_DQ_RD_CDC_SW_MODE_CFG.

DIM_BD0_DIM_DQ_RD_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1’b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1A780058 DIM_BD0_DIM_DQ_RD_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_TEST_CFG register configures the following:

DIM_DQ_RD_CDC_TEST_CFG

DIM_BD0_DIM_DQ_RD_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1’b1: Test outputs from the main DDA are connected to the CDC test ports 1’b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1’b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1’b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.

DIM_BD0_DIM_DQ_RD_CDC_TEST_CFG (cont.)

Bits	Name	Description
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1A78005C DIM_BD0_DIM_DQ_RD_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_RD_CDC_SW_OVRD_CFG

DIM_BD0_DIM_DQ_RD_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1A780060 DIM_BD0_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SLAVE_DDA_CFG register configures the following:

DIM_DQ_RD_CDC_SLAVE_DDA_CFG

DIM_BD0_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Bits	Name	Description
17	SLAV_DDA_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit-step count 1'b0: Programmed offset is added/subtracted from the unit-step count
16	SLAV_DDA_OFFSET_SIGN	1'b1: Offset is subtracted from the unit-step count. This subtraction feature is not supported on x0 and x1 PHY cores (bit RESERVED). Supported on the x2 core version. 1'b0: Offset is added to the unit-step count
15:12	SLAVE_DDA_OFFSET	unit-step offset for slave DDA.
10:0	SLAVE_DDA_DELAY	Delay required from slave DDA programmed in pico seconds.

0x1A780070 DIM_BD0_DIM_DQ_RD_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_RD_CDC_STATUS0 register configures the DIM_DQ_RD_CDC_STATUS0.

DIM_BD0_DIM_DQ_RD_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. **NOTE** The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.

DIM_BD0_DIM_DQ_RD_CDC_STATUS0 (cont.)

Bits	Name	Description
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1A780074 DIM_BD0_DIM_DQ_RD_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS1 register configures the following:

DIM_DQ_RD_CDC_STATUS1

DIM_BD0_DIM_DQ_RD_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1A780078 DIM_BD0_DIM_DQ_RD_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_RD_CDC_STATUS2 register configures the DIM_DQ_RD_CDC_STATUS2.

DIM_BD0_DIM_DQ_RD_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1A78007C DIM_BD0_DIM_DQ_RD_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS3 register configures the DIM_DQ_RD_CDC_STATUS3.

DIM_BD0_DIM_DQ_RD_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1A780080 DIM_BD0_DIM_DQ_RD_CDC_STATUS4

Type: Read
Clock: HCLK
Reset State: 0x000000FF

The DIM_DQ_RD_CDC_STATUS4 register configures the DIM_DQ_RD_CDC_STATUS4.

DIM_BD0_DIM_DQ_RD_CDC_STATUS4

Bits	Name	Description
7:4	SLAVE_DDA_DA1_TAPS	Number if unit taps applied to delay array 1 of slave DDA
3:0	SLAVE_DDA_DA0_TAPS	Number if unit taps applied to delay array 0 of slave DDA

0x1A7800AC DIM_BD0_DIM_DQ_WR_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_OFFSET_CFG register configures the DIM_DQ_WR_CDC_OFFSET_CFG.

DIM_BD0_DIM_DQ_WR_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1A7800B0 DIM_BD0_DIM_DQ_WR_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_DELAY_CFG register configures the DIM_DQ_WR_CDC_DELAY_CFG.

DIM_BD0_DIM_DQ_WR_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1A7800B4 DIM_BD0_DIM_DQ_WR_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_MODE_CFG register configures the DIM_DQ_WR_CDC_SW_MODE_CFG.

DIM_BD0_DIM_DQ_WR_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1’b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1A7800B8 DIM_BD0_DIM_DQ_WR_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_TEST_CFG register configures the DIM_DQ_WR_CDC_TEST_CFG.

DIM_BD0_DIM_DQ_WR_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1’b1: Test outputs from the main DDA are connected to the CDC test ports 1’b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1’b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1’b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1’b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1’b0 : CDC test ports disabled

DIM_BD0_DIM_DQ_WR_CDC_TEST_CFG (cont.)

Bits	Name	Description
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1A7800BC DIM_BD0_DIM_DQ_WR_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_OVRD_CFG register configures the DIM_DQ_WR_CDC_SW_OVRD_CFG.

DIM_BD0_DIM_DQ_WR_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1A7800D0 DIM_BD0_DIM_DQ_WR_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_WR_CDC_STATUS0 register configures the DIM_DQ_WR_CDC_STATUS0.

DIM_BD0_DIM_DQ_WR_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. **NOTE** The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1A7800D4 DIM_BD0_DIM_DQ_WR_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS1 register configures the DIM_DQ_WR_CDC_STATUS1.

DIM_BD0_DIM_DQ_WR_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1A7800D8 DIM_BD0_DIM_DQ_WR_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_WR_CDC_STATUS2 register configures the DIM_DQ_WR_CDC_STATUS2.

DIM_BD0_DIM_DQ_WR_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1A7800DC DIM_BD0_DIM_DQ_WR_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS3 register configures the DIM_DQ_WR_CDC_STATUS3.

DIM_BD0_DIM_DQ_WR_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1A780100 DIM_BD0_DIM_DQ_DQ_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQ_IOC_SLV_CFG register configures the DIM_DQ_DQ_IOC_SLV_CFG.

DIM_BD0_DIM_DQ_DQ_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1A780104 DIM_BD0_DIM_DQ_DQ_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQ_IOC_SLV_STATUS register configures the DIM_CA_CA_IOC_SLV_STATUS.

DIM_BD0_DIM_DQ_DQ_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

0x1A780110 DIM_BD0_DIM_DQ_DQS_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQS_IOC_SLV_CFG register configures the DIM_DQ_DQS_IOC_SLV_CFG.

DIM_BD0_DIM_DQ_DQS_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1A780114 DIM_BD0_DIM_DQ_DQS_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQS_IOC_SLV_STATUS register configures the DIM_DQ_DQS_IOC_SLV_STATUS.

DIM_BD0_DIM_DQ_DQS_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

7.3 DIM BC0 CA Top Configuration Registers (0x1AB40000 DIM_BC0_REG_BASE)

This section describes the BC0 DIM CA TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1AB40000 DIM_BC0_DIM_CA_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_CA_TOP_CFG register configures the DIM_CA_TOP_CFG.

DIM_BC0_DIM_CA_TOP_CFG

Bits	Name	Description
20	IOCAL_CTLR_SEL	Select source of PCNT/NCNT/PNCNT_VALID 1’b1: external 1’b0: internal (default)
16	SDR_MODE_EN	1’b1 : Enables SDR mode on address bus 1’b0 : Enables DDR mode on address bus (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1: From IOCAL 1’b0: From CDCCAL (default)
12	DEBUG_BUS_EN	1’b1: Enables the debug bus functionality 1’b0: Disables the debug bus and drives all ’0’s on the debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_ca[7:5] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1’b0) 1’b1 : with pipe extend (default) 1’b0: without pipe extend
0	WR_CLK_SEL	Write clock select 1’b1 : With write CDC (default) 1’b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1AB40004 DIM_BC0_DIM_CA_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_CA_HW_INFO register configures the DIM_CA_HW_INFO.

DIM_BC0_DIM_CA_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1AB40008 DIM_BC0_DIM_CA_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_CA_HW_VERSION register configures the DIM_CA_HW_VERSION.

DIM_BC0_DIM_CA_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1AB40010 DIM_BC0_DIM_CA_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_CA_PAD_CFG0 register configures the DIM_CA_PAD_CFG0.

DIM_BC0_DIM_CA_PAD_CFG0

Bits	Name	Description
31	CA_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	CA_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	CA_LV_MODE	Mode pin for high/low voltage regime
28	CA_ODT_ENA	Enable bit for on-die termination
27:26	CA_ODT	Impedance control bit settings for on-die termination
25:24	CA_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	CA_NSLEW	Slew rate control bits for output path NMOS
17:16	CA_PSLEW	Slew rate control bits for output path PMOS
13:12	CA_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	CA_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	CA_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	CA_ROUT	Impedance control bit settings for output driver
2:0	CA_DCC	Duty cycle correction bits for output path

0x1AB40014 DIM_BC0_DIM_CA_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0220440

The DIM_CA_PAD_CFG1 register configures the DIM_CA_PAD_CFG1.

DIM_BC0_DIM_CA_PAD_CFG1

Bits	Name	Description
31	CK_DDR_MODE1	Mode select for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes

DIM_BC0_DIM_CA_PAD_CFG1 (cont.)

Bits	Name	Description
30	CK_DDR_MODE0	Mode select for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	CK_LV_MODE	Mode select for high/low voltage regime
28	CK_CMFB_ENA	Common mode feedback loop enable
27	CK_ODT_ENA1	Enable bit for on-die termination (when hp_mode = 1'b1)
26	CK_ODT_ENA	Enable bit for on-die termination (when hp_mode = 1'b0) Bit field name missing '0' for APQ8064 SW compatibility.
25:24	CK_ODT	Impedance control bit settings for on-die termination
21:20	CK_NSLEW	Slew rate control bits for output path NMOS
17:16	CK_PSLEW	Slew rate control bits for output path PMOS
13	CK_CUR_MODE1	Current/Voltage mode selection (when hp_mode = 1'b1) 1'b1 : Current mode 1'b0 : Voltage mode (default)
12	CK_CUR_MODE0	Current/Voltage mode selection (when hp_mode = 1'b0) 1'b1 : Current mode 1'b0 : Voltage mode (default)
10:8	CK_I_DRV	Control bit settings for bias current
7	CK_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	CK_ROUT	Impedance control bit settings for output driver
2:0	CK_DCC	Duty cycle correction bits for output path

0x1AB40018 DIM_BC0_DIM_CA_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_CA_PAD_CFG2 register configures the DIM_CA_PAD_CFG2.

DIM_BC0_DIM_CA_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused

DIM_BC0_DIM_CA_PAD_CFG2 (cont.)

Bits	Name	Description
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1AB4001C DIM_BC0_DIM_CA_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x00300000

The DIM_CA_PAD_CFG3 register configures the DIM_CA_PAD_CFG3.

DIM_BC0_DIM_CA_PAD_CFG3

Bits	Name	Description
31:30	CS_N_IE	
29:28	CS_N_OE	
25	CK_IE	
24	CK_OE	
23:22	CKE_IE	
21:20	CKE_OE	
19:10	CA_IE	
9:0	CA_OE	

0x1AB40020 DIM_BC0_DIM_CA_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_PAD_CFG4 register configures the DIM_CA_PAD_CFG4.

DIM_BC0_DIM_CA_PAD_CFG4

Bits	Name	Description
31:30	CS_N_OE_DYN_ENA	Enable dynamic control of CS_N OE 1'b1: Dynamic control enabled and CS_N_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CS_N OE gated by CA_PAD_CFG3 bits **NOTE** This register should not be set in external loopback mode since it will change the IE contol source.
29:28	CS_N_OE_DYN	Dynamic OE control for each of the CS_N outputs, OR-ed with common controller OE.
25	RESERVED_1	
24	RESERVED_2	
23:22	CKE_OE_DYN_ENA	Enable dynamic control of CKE OE 1'b1: Dynamic control enabled and CKE_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CKE OE gated by CA_PAD_CFG3 bits
21:20	CKE_OE_DYN	Dynamic OE control for each of the CA outputs, OR-ed with common controller OE.
19:10	CA_OE_DYN_ENA	Enable dynamic control of CA OE 1'b1: Dynamic control enabled and CA_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CA OE gated by CA_PAD_CFG3 bits
9:0	CA_OE_DYN	Dynamic OE control for each of the CA outputs, OR-ed with common controller OE.

0x1AB40030 DIM_BC0_DIM_CA_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CTLR_CFG0 register configures the DIM_CA_CDC_CTLR_CFG0.

DIM_BC0_DIM_CA_CDC_CTLR_CFG0

Bits	Name	Description
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration

DIM_BC0_DIM_CA_CDC_CTLR_CFG0 (cont.)

Bits	Name	Description
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. Example: if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1AB40034 DIM_BC0_DIM_CA_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CTLR_CFG1 register configures the DIM_CA_CDC_CTLR_CFG1.

DIM_BC0_DIM_CA_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.

DIM_BC0_DIM_CA_CDC_CTLR_CFG1 (cont.)

Bits	Name	Description
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used.
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1.
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1.
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1.
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1.

0x1AB40038 DIM_BC0_DIM_CA_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CAL_TIMER_CFG0 register configures the DIM_CA_CDC_CAL_TIMER_CFG0.

DIM_BC0_DIM_CA_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.

DIM_BC0_DIM_CA_CDC_CAL_TIMER_CFG0 (cont.)

Bits	Name	Description
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1AB4003C DIM_BC0_DIM_CA_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CAL_TIMER_CFG1 register configures the DIM_CA_CDC_CAL_TIMER_CFG1.

DIM_BC0_DIM_CA_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1AB40040 DIM_BC0_DIM_CA_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_REFCOUNT_CFG register configures the DIM_CA_CDC_REFCOUNT_CFG.

DIM_BC0_DIM_CA_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.

DIM_BC0_DIM_CA_CDC_REFCOUNT_CFG (cont.)

Bits	Name	Description
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1AB40044 DIM_BC0_DIM_CA_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_CA_CDC_COARSE_CAL_CFG configures the DIM_CA_CDC_COARSE_CAL_CFG.

DIM_BC0_DIM_CA_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1AB40048 DIM_BC0_DIM_CA_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_RSVD_CFG register configures the DIM_CA_CDC_RSVD_CFG.

DIM_BC0_DIM_CA_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1AB4004C DIM_BC0_DIM_CA_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_OFFSET_CFG register configures the DIM_CA_CDC_OFFSET_CFG.

DIM_BC0_DIM_CA_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AB40050 DIM_BC0_DIM_CA_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_DELAY_CFG register configures the DIM_CA_CDC_DELAY_CFG.

DIM_BC0_DIM_CA_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AB40054 DIM_BC0_DIM_CA_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_SW_MODE_CFG register configures the DIM_CA_CDC_SW_MODE_CFG.

DIM_BC0_DIM_CA_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AB40058 DIM_BC0_DIM_CA_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_TEST_CFG register configures the DIM_CA_CDC_TEST_CFG.

DIM_BC0_DIM_CA_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AB4005C DIM_BC0_DIM_CA_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_TEST_CFG register configures the DIM_CA_CDC_SW_OVRD_CFG.

DIM_BC0_DIM_CA_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AB40070 DIM_BC0_DIM_CA_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_CA_CDC_STATUS0 register configures the DIM_CA_CDC_STATUS0.

DIM_BC0_DIM_CA_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. **NOTE** The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy.
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AB40074 DIM_BC0_DIM_CA_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_STATUS1 register configures the DIM_CA_CDC_STATUS1.

DIM_BC0_DIM_CA_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.

DIM_BC0_DIM_CA_CDC_STATUS1 (cont.)

Bits	Name	Description
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AB40078 DIM_BC0_DIM_CA_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_CA_CDC_STATUS2 register configures the DIM_CA_CDC_STATUS2.

DIM_BC0_DIM_CA_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AB4007C DIM_BC0_DIM_CA_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_STATUS3 register configures the DIM_CA_CDC_STATUS3.

DIM_BC0_DIM_CA_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AB400E0 DIM_BC0_DIM_CA_IOC_CTLR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_CFG register configures the DIM_CA_IOC_CTLR_CFG.

DIM_BC0_DIM_CA_IOC_CTLR_CFG

Bits	Name	Description
31	CAL_NOW	SW : RW Set this bit to 1'b1 will cause the IO calibration starts immediately. This bit has to be cleared after the calibration has been done. 0x0: no-op 0x1: start IOCal immediately
30	IO_CAL_AUTO	Periodic auto calibration mode. Writing a '1' to this bit will trigger periodic auto calibration with the period specified in IOC_CTLR_TIMER_CFG register. If '0', it disables the timer based on sleep clock. Note that this does not impact the timer based on fixed frequency clock (ffclk).
29	IO_CAL_FF_TIMER_EN	Fixed Frequency Timer mode. Writing a '1' to this bit will set the timer running off tcxo clock. If '0', it disables the timer based on fixed frequency clock.
28	IO_CAL_BANDGAP_DYN_CTRL	Enable dynamic control of the bandgap element: This low-power feature is only available on x2 core. Bit reserved for x0/x1 cores. 1'b1: Enabled - bandgap element turned on only during IO calibration or when current mode is enabled. 1'b0: Disabled (default) - bandgap element turned on/off statically based on BANDHGAP_ENA0/1 bits.
25	SW_FFCLK_ON	Writing a '1' to this field will turn on the fixed frequency (xo) clock on signal
24	LV_MODE	SW: RW Enable/Disable low-voltage mode (MIF2 pad only) 0x0: 1.8V 0x1: non-1.8V
20:16	MARGIN_LOAD	SW: RW If the difference between the current IOCal result is greater than the last result by the number specified here, then the IOCal controller will request value update to DDR controller. 0x0: always update
13:12	IMP_SEL	SW : RW Select bits to choose which impedance to calibrate to

DIM_BC0_DIM_CA_IOC_CTLR_CFG (cont.)

Bits	Name	Description
10	PN_SEL_CA	SW: RW Enables loading of HW calibrated values for ca pads. Writing a ’1’ to this bit would let the IOCAL to request traffic stall on ca pads when it is time to update the pads with the new value.
9	PN_SEL_DATA	SW: RW Enables loading of HW calibrated values for dq/dqs pads. Writing a ’1’ to this bit would let the IOCAL to request traffic stall on data pads when it is time to update the pads with the new value.
8	CAL_USE_LAST	SW: RW Select the initial value to start IO calibration 0x0: start from a fixed values specified in IOC_CTLR_PNCNT_CFG (default) 0x1: start from previous IOCal PNCNT results
6:4	SAMPLE_POINT	SW: RW Specify number of samples per measure point 0x0: 1 0x1: 3 0x2: 5 0x3: 7 0x4: 9 0x5: 11 0x6: 13 0x7: 15
3	DDR_MODE1	
2	DDR_MODE0	
1	BANDGAP_ENA1	SW: RW Pin to enable bandgap independent of diff_ctl 0x0: disable 0x1: enable
0	BANDGAP_ENA0	SW: RW Pin to enable bandgap independent of diff_ctl 0x0: disable 0x1: enable

0x1AB400E4 DIM_BC0_DIM_CA_IOC_CTLR_PNCNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_CFG register configures the DIM_CA_IOC_CTLR_CFG.

This register contains the initial value for the next calibration to start from. Softwave can set the hardware to start calibration either from a fixed value or from previous results. If software chooses to use fixed value by setting CAN_USE_LAST in register IOC_CTLR_CFG to be 0, then the values in this register will be used.

DIM_BC0_DIM_CA_IOC_CTLR_PNCNT_CFG

Bits	Name	Description
12:8	NCNT_INIT_CSR	SW: RW Starting PCNT value used in calibration. Only take effect when CAN_USE_LAST is asserted
4:0	PCNT_INIT_CSR	SW: RW Starting NCNT value used in calibration. Only take effect when CAN_USE_LAST is asserted

0x1AB400E8 DIM_BC0_DIM_CA_IOC_CTLR_TIMER_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_TIMER_CFG register configures the DIM_CA_IOC_CTLR_TIMER_CFG.

DIM_BC0_DIM_CA_IOC_CTLR_TIMER_CFG

Bits	Name	Description
31:16	TIMER_PERIOD	SW: RW Recalibration Period. The period is measured in timer clock cycles. Typically it's a 32kHz clock. The minimum period that can be programmed is 3. 0,1,2: Invalid values
15:0	FF_TIMER_PERIOD	SW: RW Recalibration Period for the timer running of xo clock. 0x0: Invalid

0x1AB400EC DIM_BC0_DIM_CA_IOC_CTLR_TIMER_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_TIMER_STATUS register configures the DIM_CA_IOC_CTLR_TIMER_STATUS.

DIM_BC0_DIM_CA_IOC_CTLR_TIMER_STATUS

Bits	Name	Description
15:0	TIMER_STATUS	Current Auto Calibration Timer value. As this register is written in sleep clock domain and read in xo clock domain and no hardware synchronization in place, It is required by the software to read this register 4 times to get the correct value.

0x1AB400F0 DIM_BC0_DIM_CA_IOC_CTLR_CHAR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_ CHAR_CFG register configures the IDIM_CA_IOC_CTLR_CHAR_CFG.

This register is used by hardware verification software only. It provides a mechanism to allow software to bypass the internal calibration state machine and directly access the IOCAL pad inputs.

DIM_BC0_DIM_CA_IOC_CTLR_CHAR_CFG

Bits	Name	Description
16	SM_BYP_ENA	SW: RW Characterization Bypass Path Enable 0x0: Non-bypass: State Machine Controls IOCAL pad inputs (default) 0x1: bypass: This register controls IOCal pad inputs
15	SM_BYP_N_ENA	SW: RW IO CAL Characterization n_enable: 0x0: de-asserted (default) 0x1: asserted
12:8	SM_BYP_NCNT	SW: RW IO CAL Characterization ncnt value. 0x0: count 0 (default)
7	SM_BYP_P_ENA	SW: RW IO CAL Characterization p_enable: 0x0: de-asserted (default) 0x1: asserted
4:0	SM_BYP_PCNT	SW: RW IO CAL Characterization pcnt value. 0x0: count 0 (default)

0x1AB400F4 DIM_BC0_DIM_CA_IOC_CTLR_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00011010

The DIM_CA_IOC_CTLR_STATUS register configures the following:

DIM_CA_IOC_CTLR_STATUS

DIM_BC0_DIM_CA_IOC_CTLR_STATUS

Bits	Name	Description
31	INIT_IOCAL_DONE	SW : R The very first IO Calibration is finished This bit is stiky. once it becomes 1’b1 until software writes it back to 0. 0x0: Init-cal never done 0x1: Init-cal finished
18	IOCAL_DONE_D	SW : R IO Calibration is finished 0x0: in progress 0x1: finished
17	IOCAL_BUSY	SW : R Status of calibration State machine 0x0: idle 0x1: busy
16	SYNC_COMP	SW : R comp value from IOCal pad
12:8	NCNT_HOLD	SW : R Current NCNT value used
4:0	PCNT_HOLD	SW : R Current PCNT value used

0x1AB40100 DIM_BC0_DIM_CA_CA_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_CA_CA_IOC_SLV_CFG register configures the following:

This register specifies the overriding pcnt and ncnt values. Overriding mode is controlled by PNCNT_HW_LOAD_EN bit in this register.

DIM_CA_CA_IOC_SLV_CFG

DIM_BC0_DIM_CA_CA_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	Select PCNT/NCNT Source for pads. This is the mux control that chooses either auto calibrated value or the software override value. 0x0: override (default) 0x1: auto cal
28:24	NCNT_SW_VAL	SW: RW NCNT Override Value for the pads
20:16	PCNT_SW_VAL	SW: RW PCNT Override Value for the pads
15	NCNT_OFFSET_SIGN	Controls if the NOFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
12:8	NCNT_SW_OFFSET	SW: RW The offiset applied on top of NCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)
7	PCNT_OFFSET_SIGN	Controls if the POFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
4:0	PCNT_SW_OFFSET	SW: RW The offiset applied on top of PCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)

0x1AB40104 DIM_BC0_DIM_CA_CA_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_CA_CA_IOC_SLV_STATUS register configures the following:

DIM_CA_CA_IOC_SLV_STATUS

DIM_BC0_DIM_CA_CA_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	The final NCNT value that is applied to the pads.
4:0	PAD_PCNT	The final PCNT value that is applied to the pads.

0x1AB40110 DIM_BC0_DIM_CA_CK_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_CA_CK_IOC_SLV_CFG register configures the following:

DIM_CA_CK_IOC_SLV_CFG

DIM_BC0_DIM_CA_CK_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	Select PCNT/NCNT Source for pads. This is the mux control that chooses either auto calibrated value or the software override value. 0x0: override (default) 0x1: auto cal
28:24	NCNT_SW_VAL	SW: RW NCNT Override Value for the pads
20:16	PCNT_SW_VAL	SW: RW PCNT Override Value for the pads
15	NCNT_OFFSET_SIGN	Controls if the NOFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
12:8	NCNT_SW_OFFSET	SW: RW The offiset applied on top of NCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)
7	PCNT_OFFSET_SIGN	Controls if the POFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
4:0	PCNT_SW_OFFSET	SW: RW The offiset applied on top of PCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)

0x1AB40114 DIM_BC0_DIM_CA_CK_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_CA_CK_IOC_SLV_STATUS register configures DIM_CA_CK_IOC_SLV_STATUS.

DIM_BC0_DIM_CA_CK_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	The final NCNT value that is applied to the pads.
4:0	PAD_PCNT	The final PCNT value that is applied to the pads.

7.4 DIM C01 CA Top Configuration Registers (0x1AB80000 DIM_C01_REG_BASE)

This section describes the C01 DIM CA TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1AB80000 DIM_C01_DIM_CA_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_CA_TOP_CFG register configures DIM_CA_TOP_CFG.

DIM_C01_DIM_CA_TOP_CFG

Bits	Name	Description
20	IOCAL_CTLR_SEL	Select source of PCNT/NCNT/PNCNT_VALID 1’b1: external 1’b0: internal (default)
16	SDR_MODE_EN	1’b1 : Enables SDR mode on address bus 1’b0 : Enables DDR mode on address bus (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1: From IOCAL 1’b0: From CDCCAL (default)
12	DEBUG_BUS_EN	1’b1: Enables the debug bus functionality 1’b0: Disables the debug bus and drives all ’0’s on the debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_ca[7:5] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1’b0) 1’b1 : with pipe extend (default) 1’b0: without pipe extend
0	WR_CLK_SEL	Write clock select 1’b1 : With write CDC (default) 1’b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1AB80004 DIM_C01_DIM_CA_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_CA_HW_INFO register configures DIM_CA_HW_INFO.

DIM_C01_DIM_CA_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1AB80008 DIM_C01_DIM_CA_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_CA_HW_VERSION register configures DIM_CA_HW_VERSION.

DIM_C01_DIM_CA_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1AB80010 DIM_C01_DIM_CA_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_CA_PAD_CFG0 register configures DIM_CA_PAD_CFG0.

DIM_C01_DIM_CA_PAD_CFG0

Bits	Name	Description
31	CA_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	CA_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	CA_LV_MODE	Mode pin for high/low voltage regime
28	CA_ODT_ENA	Enable bit for on-die termination
27:26	CA_ODT	Impedance control bit settings for on-die termination
25:24	CA_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	CA_NSLEW	Slew rate control bits for output path NMOS
17:16	CA_PSLEW	Slew rate control bits for output path PMOS
13:12	CA_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	CA_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	CA_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	CA_ROUT	Impedance control bit settings for output driver
2:0	CA_DCC	Duty cycle correction bits for output path

0x1AB80014 DIM_C01_DIM_CA_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0220440

The DIM_CA_PAD_CFG1 register configures DIM_CA_PAD_CFG1.

DIM_C01_DIM_CA_PAD_CFG1

Bits	Name	Description
31	CK_DDR_MODE1	Mode select for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes

DIM_C01_DIM_CA_PAD_CFG1 (cont.)

Bits	Name	Description
30	CK_DDR_MODE0	Mode select for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	CK_LV_MODE	Mode select for high/low voltage regime
28	CK_CMFB_ENA	Common mode feedback loop enable
27	CK_ODT_ENA1	Enable bit for on-die termination (when hp_mode = 1'b1)
26	CK_ODT_ENA	Enable bit for on-die termination (when hp_mode = 1'b0) Bit field name missing '0' for APQ8064 SW compatibility.
25:24	CK_ODT	Impedance control bit settings for on-die termination
21:20	CK_NSLEW	Slew rate control bits for output path NMOS
17:16	CK_PSLEW	Slew rate control bits for output path PMOS
13	CK_CUR_MODE1	Current/Voltage mode selection (when hp_mode = 1'b1) 1'b1 : Current mode 1'b0 : Voltage mode (default)
12	CK_CUR_MODE0	Current/Voltage mode selection (when hp_mode = 1'b0) 1'b1 : Current mode 1'b0 : Voltage mode (default)
10:8	CK_I_DRV	Control bit settings for bias current
7	CK_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	CK_ROUT	Impedance control bit settings for output driver
2:0	CK_DCC	Duty cycle correction bits for output path

0x1AB80018 DIM_C01_DIM_CA_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_CA_PAD_CFG2 register configures DIM_CA_PAD_CFG2.

DIM_C01_DIM_CA_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused

DIM_C01_DIM_CA_PAD_CFG2 (cont.)

Bits	Name	Description
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1AB8001C DIM_C01_DIM_CA_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x00300000

The DIM_CA_PAD_CFG3 register configures DIM_CA_PAD_CFG3.

DIM_C01_DIM_CA_PAD_CFG3

Bits	Name	Description
31:30	CS_N_IE	
29:28	CS_N_OE	
25	CK_IE	
24	CK_OE	
23:22	CKE_IE	
21:20	CKE_OE	
19:10	CA_IE	
9:0	CA_OE	

0x1AB80020 DIM_C01_DIM_CA_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_PAD_CFG4 register configures DIM_CA_PAD_CFG4.

DIM_C01_DIM_CA_PAD_CFG4

Bits	Name	Description
31:30	CS_N_OE_DYN_ENA	Enable dynamic control of CS_N OE 1'b1: Dynamic control enabled and CS_N_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CS_N OE gated by CA_PAD_CFG3 bits **NOTE** This register should not be set in external loopback mode since it will change the IE contol source.
29:28	CS_N_OE_DYN	Dynamic OE control for each of the CS_N outputs, OR-ed with common controller OE.
25	RESERVED_1	
24	RESERVED_2	
23:22	CKE_OE_DYN_ENA	Enable dynamic control of CKE OE 1'b1: Dynamic control enabled and CKE_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CKE OE gated by CA_PAD_CFG3 bits
21:20	CKE_OE_DYN	Dynamic OE control for each of the CA outputs, OR-ed with common controller OE.
19:10	CA_OE_DYN_ENA	Enable dynamic control of CA OE 1'b1: Dynamic control enabled and CA_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CA OE gated by CA_PAD_CFG3 bits
9:0	CA_OE_DYN	Dynamic OE control for each of the CA outputs, OR-ed with common controller OE.

0x1AB80030 DIM_C01_DIM_CA_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CTLR_CFG0 register configures DIM_CA_CDC_CTLR_CFG0.

DIM_C01_DIM_CA_CDC_CTLR_CFG0

Bits	Name	Description
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration

DIM_C01_DIM_CA_CDC_CTLR_CFG0 (cont.)

Bits	Name	Description
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1AB80034 DIM_C01_DIM_CA_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CTLR_CFG1 register configures DIM_CA_CDC_CTLR_CFG1.

DIM_C01_DIM_CA_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.

DIM_C01_DIM_CA_CDC_CTLR_CFG1 (cont.)

Bits	Name	Description
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used.
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1.
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1.
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1.
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1.

0x1AB80038 DIM_C01_DIM_CA_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CAL_TIMER_CFG0 register configures the following:

DIM_CA_CDC_CAL_TIMER_CFG0

DIM_C01_DIM_CA_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.

DIM_C01_DIM_CA_CDC_CAL_TIMER_CFG0 (cont.)

Bits	Name	Description
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1AB8003C DIM_C01_DIM_CA_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CAL_TIMER_CFG1 register configures DIM_CA_CDC_CAL_TIMER_CFG1.

DIM_C01_DIM_CA_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1AB80040 DIM_C01_DIM_CA_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_REFCOUNT_CFG register configures DIM_CA_CDC_REFCOUNT_CFG.

DIM_C01_DIM_CA_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.

DIM_C01_DIM_CA_CDC_REFCOUNT_CFG (cont.)

Bits	Name	Description
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1AB80044 DIM_C01_DIM_CA_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_CA_CDC_COARSE_CAL_CFG configures DIM_CA_CDC_COARSE_CAL_CFG.

DIM_C01_DIM_CA_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	Unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1AB80048 DIM_C01_DIM_CA_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_RSVD_CFG register configures DIM_CA_CDC_RSVD_CFG.

DIM_C01_DIM_CA_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1AB8004C DIM_C01_DIM_CA_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_OFFSET_CFG register configures DIM_CA_CDC_OFFSET_CFG.

DIM_C01_DIM_CA_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AB80050 DIM_C01_DIM_CA_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_DELAY_CFG register configures DIM_CA_CDC_DELAY_CFG.

DIM_C01_DIM_CA_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AB80054 DIM_C01_DIM_CA_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_SW_MODE_CFG register configures DIM_CA_CDC_SW_MODE_CFG.

DIM_C01_DIM_CA_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AB80058 DIM_C01_DIM_CA_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_TEST_CFG register configures DIM_CA_CDC_TEST_CFG.

DIM_C01_DIM_CA_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AB8005C DIM_C01_DIM_CA_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_TEST_CFG register configures DIM_CA_CDC_SW_OVRD_CFG.

DIM_C01_DIM_CA_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AB80070 DIM_C01_DIM_CA_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_CA_CDC_STATUS0 register configures DIM_CA_CDC_STATUS0.

DIM_C01_DIM_CA_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. **NOTE** The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AB80074 DIM_C01_DIM_CA_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_STATUS1 register configures DIM_CA_CDC_STATUS1.

DIM_C01_DIM_CA_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.

DIM_C01_DIM_CA_CDC_STATUS1 (cont.)

Bits	Name	Description
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AB80078 DIM_C01_DIM_CA_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_CA_CDC_STATUS2 register configures DIM_CA_CDC_STATUS2.

DIM_C01_DIM_CA_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AB8007C DIM_C01_DIM_CA_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_STATUS3 register configures DIM_CA_CDC_STATUS3.

DIM_C01_DIM_CA_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AB800E0 DIM_C01_DIM_CA_IOC_CTLR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_CFG register configures DIM_CA_IOC_CTLR_CFG.

DIM_C01_DIM_CA_IOC_CTLR_CFG

Bits	Name	Description
31	CAL_NOW	SW : RW Set this bit to 1'b1 will cause the IO calibration starts immediately. This bit has to be cleared after the calibration has been done. 0x0: no-op 0x1: start IOCal immediately
30	IO_CAL_AUTO	Periodic auto calibration mode. Writing a '1' to this bit will trigger periodic auto calibration with the period specified in IOC_CTLR_TIMER_CFG register. If '0', it disables the timer based on sleep clock. Note that this does not impact the timer based on fixed frequency clock (ffclk).
29	IO_CAL_FF_TIMER_EN	Fixed Frequency Timer mode. Writing a '1' to this bit will set the timer running off tcxo clock. If '0', it disables the timer based on fixed frequency clock.
28	IO_CAL_BANDGAP_DYN_CTRL	Enable dynamic control of the bandgap element: This low-power feature is only available on x2 core. Bit reserved for x0/x1 cores. 1'b1: Enabled - bandgap element turned on only during IO calibration or when current mode is enabled. 1'b0: Disabled (default) - bandgap element turned on/off statically based on BANDHGAP_ENA0/1 bits.
25	SW_FFCLK_ON	Writing a '1' to this field will turn on the fixed frequency (xo) clock on signal
24	LV_MODE	SW: RW Enable/Disable low-voltage mode (MIF2 pad only) 0x0: 1.8V 0x1: non-1.8V
20:16	MARGIN_LOAD	SW: RW If the difference between the current IOCal result is greater than the last result by the number specified here, then the IOCal controller will request value update to DDR controller. 0x0: always update
13:12	IMP_SEL	SW: RW Select bits to choose which impedance to calibrate to

DIM_C01_DIM_CA_IOC_CTLR_CFG (cont.)

Bits	Name	Description
10	PN_SEL_CA	SW: RW Enables loading of HW calibrated values for ca pads. Writing a ‘1’ to this bit would let the IOCAL to request traffic stall on ca pads when it is time to update the pads with the new value.
9	PN_SEL_DATA	SW: RW Enables loading of HW calibrated values for dq/dqs pads. Writing a ’1’ to this bit would let the IOCAL to request traffic stall on data pads when it is time to update the pads with the new value.
8	CAL_USE_LAST	SW: RW Select the initial value to start IO calibration 0x0: start from a fixed values specified in IOC_CTLR_PNCNT_CFG (default) 0x1: start from previous IOCal PNCNT results
6:4	SAMPLE_POINT	SW: RW Specify number of samples per measure point 0x0: 1 0x1: 3 0x2: 5 0x3: 7 0x4: 9 0x5: 11 0x6: 13 0x7: 15
3	DDR_MODE1	
2	DDR_MODE0	
1	BANDGAP_ENA1	SW: RW Pin to enable bandgap independent of diff_ctl 0x0: disable 0x1: enable
0	BANDGAP_ENA0	SW: RW Pin to enable bandgap independent of diff_ctl 0x0: disable 0x1: enable

0x1AB800E4 DIM_C01_DIM_CA_IOC_CTLR_PNCNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_CFG register configures DIM_CA_IOC_CTLR_CFG.

This register contains the initial value for the next calibration to start from. Softwave can set the hardware to either start calibration from a fixed value or from previous results. If software chooses to use fixed value by setting CAN_USE_LAST in register IOC_CTLR_CFG to be 0, then the values in this register will be used.

DIM_C01_DIM_CA_IOC_CTLR_PNCNT_CFG

Bits	Name	Description
12:8	NCNT_INIT_CSR	SW : RW Starting PCNT value used in calibration. Only take effect when CAN_USE_LAST is asserted
4:0	PCNT_INIT_CSR	SW : RW Starting NCNT value used in calibration. Only take effect when CAN_USE_LAST is asserted

0x1AB800E8 DIM_C01_DIM_CA_IOC_CTLR_TIMER_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_TIMER_CFG register configures DIM_CA_IOC_CTLR_TIMER_CFG.

DIM_C01_DIM_CA_IOC_CTLR_TIMER_CFG

Bits	Name	Description
31:16	TIMER_PERIOD	SW: RW Recalibration Period. The period is measured in timer clock cycles. Typically it's a 32kHz clock. The minimum period that can be programmed is 3. 0,1,2: Invalid values
15:0	FF_TIMER_PERIOD	SW: RW Recalibration Period for the timer running of xo clock. 0x0: Invalid

0x1AB800EC DIM_C01_DIM_CA_IOC_CTLR_TIMER_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_TIMER_STATUS register configures DIM_CA_IOC_CTLR_TIMER_STATUS.

DIM_C01_DIM_CA_IOC_CTLR_TIMER_STATUS

Bits	Name	Description
15:0	TIMER_STATUS	Current Auto Calibration Timer value. As this register is written in sleep clock domain and read in xo clock domain and no hardware synchronization in place, It is required by the software to read this register 4 times to get the correct value.

0x1AB800F0 DIM_C01_DIM_CA_IOC_CTLR_CHAR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_ CHAR_CFGregister configures IDIM_CA_IOC_CTLR_CHAR_CFG.

This register is used by hardware verification software only. It provides a mechanism to allow software to bypass the internal calibration state machine and directly access the IOCAL pad inputs.

DIM_C01_DIM_CA_IOC_CTLR_CHAR_CFG

Bits	Name	Description
16	SM_BYP_ENA	SW: RW Characterization Bypass Path Enable 0x0: Non-bypass: State Machine Controls IOCAL pad inputs (default) 0x1: bypass: This register controls IOCal pad inputs
15	SM_BYP_N_ENA	SW: RW IO CAL Characterization n_enable: 0x0: de-asserted (default) 0x1: asserted
12:8	SM_BYP_NCNT	SW: RW IO CAL Characterization ncnt value. 0x0: count 0 (default)
7	SM_BYP_P_ENA	SW: RW IO CAL Characterization p_enable: 0x0: de-asserted (default) 0x1: asserted
4:0	SM_BYP_PCNT	SW: RW IO CAL Characterization pcnt value. 0x0: count 0 (default)

0x1AB800F4 DIM_C01_DIM_CA_IOC_CTLR_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00011010

The DIM_CA_IOC_CTLR_STATUS register configures DIM_CA_IOC_CTLR_STATUS.

DIM_C01_DIM_CA_IOC_CTLR_STATUS

Bits	Name	Description
31	INIT_IOCAL_DONE	SW: R The very first IO Calibration is finished This bit is stiky. once it becomes 1’b1 until software writes it back to 0. 0x0: Init-cal never done 0x1: Init-cal finished
18	IOCAL_DONE_D	SW: R IO Calibration is finished 0x0: in progress 0x1: finished
17	IOCAL_BUSY	SW: R Status of calibration State machine 0x0: idle 0x1: busy
16	SYNC_COMP	SW: R comp value from IOCal pad
12:8	NCNT_HOLD	SW: R Current NCNT value used
4:0	PCNT_HOLD	SW: R Current PCNT value used

0x1AB80100 DIM_C01_DIM_CA_CA_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_CA_CA_IOC_SLV_CFG register configures DIM_CA_CA_IOC_SLV_CFG.

This register specifies the overriding pcnt and ncnt values. Overriding mode is controlled by PNCNT_HW_LOAD_EN bit in this register.

DIM_C01_DIM_CA_CA_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	Select PCNT/NCNT Source for pads. This is the mux control that chooses either auto calibrated value or the software override value. 0x0: override (default) 0x1: auto cal
28:24	NCNT_SW_VAL	SW: RW NCNT Override Value for the pads
20:16	PCNT_SW_VAL	SW: RW PCNT Override Value for the pads
15	NCNT_OFFSET_SIGN	Controls if the NOFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
12:8	NCNT_SW_OFFSET	SW: RW The offiset applied on top of NCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)
7	PCNT_OFFSET_SIGN	Controls if the POFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
4:0	PCNT_SW_OFFSET	SW: RW The offiset applied on top of PCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)

0x1AB80104 DIM_C01_DIM_CA_CA_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_CA_CA_IOC_SLV_STATUS register configures DIM_CA_CA_IOC_SLV_STATUS.

DIM_C01_DIM_CA_CA_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	The final NCNT value that is applied to the pads.
4:0	PAD_PCNT	The final PCNT value that is applied to the pads.

0x1AB80110 DIM_C01_DIM_CA_CK_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_CA_CK_IOC_SLV_CFG register configures DIM_CA_CK_IOC_SLV_CFG.

DIM_C01_DIM_CA_CK_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	Select PCNT/NCNT Source for pads. This is the mux control that chooses either auto calibrated value or the software override value. 0x0: override (default) 0x1: auto cal
28:24	NCNT_SW_VAL	SW: RW NCNT Override Value for the pads
20:16	PCNT_SW_VAL	SW : RW PCNT Override Value for the pads
15	NCNT_OFFSET_SIGN	Controls if the NOFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
12:8	NCNT_SW_OFFSET	SW: RW The offiset applied on top of NCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)
7	PCNT_OFFSET_SIGN	Controls if the POFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
4:0	PCNT_SW_OFFSET	SW: RW The offiset applied on top of PCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)

0x1AB80114 DIM_C01_DIM_CA_CK_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_CA_CK_IOC_SLV_STATUS register configures DIM_CA_CK_IOC_SLV_STATUS.

DIM_C01_DIM_CA_CK_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	The final NCNT value that is applied to the pads.
4:0	PAD_PCNT	The final PCNT value that is applied to the pads.

7.5 DIM BD1 DQ Top Configuration Registers (0x1AC80000 DIM_BD1_REG_BASE)

This section describes the BD1 DIM DQ TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1AC80000 DIM_BD1_DIM_DQ_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_DQ_TOP_CFG register configures DIM_DQ_TOP_CFG.

DIM_BD1_DIM_DQ_TOP_CFG

Bits	Name	Description
26	CDC_LDO_EN	Enablement of CDC LDO 1’b1 : Enabled 1’b0 : Disabled LDO and power provided from switches (default)
25	CDC_SWITCH_RC_EN	Enablement of CDC power RC (LPF) switch 1’b1 : Enabled 1’b0 : Disabled (default)
24	CDC_SWITCH_BYPASS_OFF	Enablement of CDC power bypass switch 1’b1 : Disabled 1’b0 : Enabled (default)
16	RCW_EN	Enablement of the Read Capture Window 1’b1 : Enable the RCW 1’b0 : Disabled (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1 : from Read CDCCAL 1’b0 : from Write CDCCAL (default)
12	DEBUG_BUS_EN	1’b1 : Enables the debug bus functionality 1’b0 : Disables the debug bus and drives all ’0’s on debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_dq[5:0] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend

DIM_BD1_DIM_DQ_TOP_CFG (cont.)

Bits	Name	Description
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1'b0) 1'b1 : with pipe extend (default) 1'b0 : without pipe extend
0	WR_CLK_SEL	Write clock select 1'b1 : With write CDC (default) 1'b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1AC80004 DIM_BD1_DIM_DQ_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_DQ_HW_INFO register configures DIM_DQ_HW_INFO.

DIM_BD1_DIM_DQ_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1AC80008 DIM_BD1_DIM_DQ_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_DQ_HW_VERSION register configures DIM_DQ_HW_VERSION.

DIM_BD1_DIM_DQ_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.

DIM_BD1_DIM_DQ_HW_VERSION (cont.)

Bits	Name	Description
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1AC80010 DIM_BD1_DIM_DQ_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG0 register configures DIM_DQ_PAD_CFG0.

DIM_BD1_DIM_DQ_PAD_CFG0

Bits	Name	Description
31	DQ_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	DQ_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	DQ_LV_MODE	Mode select for high/low voltage regime
28	DQ_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQ_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQ_PULL_B	Input pull control
21:20	DQ_NSLEW	Slew rate control bits for output path NMOS
17:16	DQ_PSLEW	Slew rate control bits for output path PMOS
13:12	DQ_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQ_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	DQ_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQ_ROUT	Impedance control bit settings for output driver
2:0	DQ_DCC	Duty cycle correction bits for output path

0x1AC80014 DIM_BD1_DIM_DQ_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG1 register configures DIM_DQ_PAD_CFG1.

DIM_BD1_DIM_DQ_PAD_CFG1

Bits	Name	Description
31	DQS_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
30	DQS_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	DQS_LV_MODE	Mode select for high/low voltage regime
28	DQS_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQS_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQS_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	DQS_NSLEW	Slew rate control bits for output path NMOS
17:16	DQS_PSLEW	Slew rate control bits for output path PMOS
13:12	DQS_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQS_PRXDEL	Delay control bits to increase strength of PMOS input drive
7	DQS_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQS_ROUT	Impedance control bit settings for output driver
2:0	DQS_DCC	Duty cycle correction bits for output path

0x1AC80018 DIM_BD1_DIM_DQ_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_DQ_PAD_CFG2 register configures DIM_DQ_PAD_CFG2.

DIM_BD1_DIM_DQ_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)

DIM_BD1_DIM_DQ_PAD_CFG2 (cont.)

Bits	Name	Description
27:24	VREF_SP_OUT	Unused
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1AC80020 DIM_BD1_DIM_DQ_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x1000FF11

The DIM_DQ_PAD_CFG3 register configures DIM_DQ_PAD_CFG3.

DIM_BD1_DIM_DQ_PAD_CFG3

Bits	Name	Description
28	DQS_DIFF_MODE	DQS output mode control 1'b1 : differential output (default) 1'b0 : single-ended output; _n output is HIZ
27	RCW_ODT_ENA1	Enable ODT for RCW pad (when hp_mode=1)
26	RCW_ODT_ENA0	Enable ODT for RCW pad (when hp_mode=0)
25:24	RCW_ODT	Impedance control for on-die termination on RCW pad
23	DQ_ODT_ENA1	Enable ODT for DQ pads (when hp_mode=1)
22	DQ_ODT_ENA0	Enable ODT for DQ pads (when hp_mode=0)
21:20	DQ_ODT	Impedance control for on-die termination on DQ pads
19	DQS_ODT_ENA1	Enable ODT for DQS pad (when hp_mode=1)
18	DQS_ODT_ENA0	Enable ODT for DQS pad (when hp_mode=0)
17:16	DQS_ODT	Impedance control for on-die termination on DQS pad
15:8	DQ_IE_OE	Enable both input receiver and output driver for all DQ pads
5	RCW_IE_OE	Enable both input receiver and output driver for RCW pad
4	DQS_IE_OE	Enable both input receiver and output driver for DQS pad
1	DM_IE	Input received enable for DM pad
0	DM_OE	Output driver enable for DM pad

0x1AC80024 DIM_BD1_DIM_DQ_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG4 register configures DIM_DQ_PAD_CFG4.

DIM_BD1_DIM_DQ_PAD_CFG4

Bits	Name	Description
31	RCW_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	RCW_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	RCW_LV_MODE	Mode select for high/low voltage regime
25:24	RCW_PULL_B	Input pull control
21:20	RCW_NSLEW	Slew rate control bits for output path NMOS
17:16	RCW_PSLEW	Slew rate control bits for output path PMOS
13:12	RCW_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	RCW_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	RCW_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	RCW_ROUT	Impedance control bit settings for output driver
2:0	RCW_DCC	Duty cycle correction bits for output path

0x1AC80030 DIM_BD1_DIM_DQ_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG0 register configures DIM_DQ_CDC_CTLR_CFG0.

DIM_BD1_DIM_DQ_CDC_CTLR_CFG0

Bits	Name	Description
25	STAGGER_CAL_ENA	1'b1: Stagger calibration of write and read CDCs once after the other to reduce peak voltage drop. 1'b0: Both write and read CDCs calibrated simultaneously This bit is introduced on the x2 core, so not present on x0 and x1 versions of DIM/PHY.
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. Example: if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1AC80034 DIM_BD1_DIM_DQ_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG1 register configures DIM_DQ_CDC_CTLR_CFG1.

DIM_BD1_DIM_DQ_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used.
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1.
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1.
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1.
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1.

0x1AC80038 DIM_BD1_DIM_DQ_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG0 register configures DIM_DQ_CDC_CAL_TIMER_CFG0.

DIM_BD1_DIM_DQ_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.

DIM_BD1_DIM_DQ_CDC_CAL_TIMER_CFG0 (cont.)

Bits	Name	Description
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1AC8003C DIM_BD1_DIM_DQ_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG1 register configures DIM_DQ_CDC_CAL_TIMER_CFG1.

DIM_BD1_DIM_DQ_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1AC80040 DIM_BD1_DIM_DQ_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_REFCOUNT_CFG register configures DIM_DQ_CDC_REFCOUNT_CFG.

DIM_BD1_DIM_DQ_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.

DIM_BD1_DIM_DQ_CDC_REFCOUNT_CFG (cont.)

Bits	Name	Description
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1AC80044 DIM_BD1_DIM_DQ_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_DQ_CDC_COARSE_CAL_CFG configures DIM_DQ_CDC_COARSE_CAL_CFG.

DIM_BD1_DIM_DQ_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	Unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1AC80048 DIM_BD1_DIM_DQ_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_RSVD_CFG register configures DIM_DQ_CDC_RSVD_CFG.

DIM_BD1_DIM_DQ_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1AC8004C DIM_BD1_DIM_DQ_RD_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_OFFSET_CFG register configures DIM_DQ_RD_CDC_OFFSET_CFG.

DIM_BD1_DIM_DQ_RD_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AC80050 DIM_BD1_DIM_DQ_RD_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_DELAY_CFG register configures DIM_DQ_RD_CDC_DELAY_CFG.

DIM_BD1_DIM_DQ_RD_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AC80054 DIM_BD1_DIM_DQ_RD_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_MODE_CFG register configures DIM_DQ_RD_CDC_SW_MODE_CFG.

DIM_BD1_DIM_DQ_RD_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AC80058 DIM_BD1_DIM_DQ_RD_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_TEST_CFG register configures DIM_DQ_RD_CDC_TEST_CFG.

DIM_BD1_DIM_DQ_RD_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AC8005C DIM_BD1_DIM_DQ_RD_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_OVRD_CFG register configures DIM_DQ_RD_CDC_SW_OVRD_CFG.

DIM_BD1_DIM_DQ_RD_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AC80060 DIM_BD1_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SLAVE_DDA_CFG register configures DIM_DQ_RD_CDC_SLAVE_DDA_CFG.

DIM_BD1_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Bits	Name	Description
17	SLAV_DDA_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit-step count 1'b0: Programmed offset is added/subtracted from the unit-step count
16	SLAV_DDA_OFFSET_SIGN	1'b1: Offset is subtracted from the unit-step count. This subtraction feature is not supported on x0 and x1 PHY cores (bit RESERVED). Supported on the x2 core version. 1'b0: Offset is added to the unit-step count
15:12	SLAVE_DDA_OFFSET	unit-step offset for slave DDA.
10:0	SLAVE_DDA_DELAY	Delay required from slave DDA programmed in pico seconds.

0x1AC80070 DIM_BD1_DIM_DQ_RD_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_RD_CDC_STATUS0 register configures DIM_DQ_RD_CDC_STATUS0.

DIM_BD1_DIM_DQ_RD_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. **NOTE** The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected

DIM_BD1_DIM_DQ_RD_CDC_STATUS0 (cont.)

Bits	Name	Description
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AC80074 DIM_BD1_DIM_DQ_RD_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS1 register configures DIM_DQ_RD_CDC_STATUS1.

DIM_BD1_DIM_DQ_RD_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AC80078 DIM_BD1_DIM_DQ_RD_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_RD_CDC_STATUS2 register configures DIM_DQ_RD_CDC_STATUS2.

DIM_BD1_DIM_DQ_RD_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AC8007C DIM_BD1_DIM_DQ_RD_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS3 register configures DIM_DQ_RD_CDC_STATUS3.

DIM_BD1_DIM_DQ_RD_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AC80080 DIM_BD1_DIM_DQ_RD_CDC_STATUS4

Type: Read
Clock: HCLK
Reset State: 0x000000FF

The DIM_DQ_RD_CDC_STATUS4 register configures DIM_DQ_RD_CDC_STATUS4.

DIM_BD1_DIM_DQ_RD_CDC_STATUS4

Bits	Name	Description
7:4	SLAVE_DDA_DA1_TAPS	Number if unit taps applied to delay array 1 of slave DDA
3:0	SLAVE_DDA_DA0_TAPS	Number if unit taps applied to delay array 0 of slave DDA

0x1AC800AC DIM_BD1_DIM_DQ_WR_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_OFFSET_CFG register configures DIM_DQ_WR_CDC_OFFSET_CFG.

DIM_BD1_DIM_DQ_WR_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AC800B0 DIM_BD1_DIM_DQ_WR_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_DELAY_CFG register configures DIM_DQ_WR_CDC_DELAY_CFG.

DIM_BD1_DIM_DQ_WR_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AC800B4 DIM_BD1_DIM_DQ_WR_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_MODE_CFG register configures DIM_DQ_WR_CDC_SW_MODE_CFG.

DIM_BD1_DIM_DQ_WR_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AC800B8 DIM_BD1_DIM_DQ_WR_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_TEST_CFG register configures DIM_DQ_WR_CDC_TEST_CFG.

DIM_BD1_DIM_DQ_WR_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AC800BC DIM_BD1_DIM_DQ_WR_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_OVRD_CFG register configures DIM_DQ_WR_CDC_SW_OVRD_CFG.

DIM_BD1_DIM_DQ_WR_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AC800D0 DIM_BD1_DIM_DQ_WR_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_WR_CDC_STATUS0 register configures DIM_DQ_WR_CDC_STATUS0.

DIM_BD1_DIM_DQ_WR_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. **NOTE** The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AC800D4 DIM_BD1_DIM_DQ_WR_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS1 register configures DIM_DQ_WR_CDC_STATUS1.

DIM_BD1_DIM_DQ_WR_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.

DIM_BD1_DIM_DQ_WR_CDC_STATUS1 (cont.)

Bits	Name	Description
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AC800D8 DIM_BD1_DIM_DQ_WR_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_WR_CDC_STATUS2 register configures DIM_DQ_WR_CDC_STATUS2.

DIM_BD1_DIM_DQ_WR_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AC800DC DIM_BD1_DIM_DQ_WR_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS3 register configures DIM_DQ_WR_CDC_STATUS3.

DIM_BD1_DIM_DQ_WR_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AC80100 DIM_BD1_DIM_DQ_DQ_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQ_IOC_SLV_CFG register configures DIM_DQ_DQ_IOC_SLV_CFG.

DIM_BD1_DIM_DQ_DQ_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1AC80104 DIM_BD1_DIM_DQ_DQ_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQ_IOC_SLV_STATUS register configures DIM_CA_CA_IOC_SLV_STATUS.

DIM_BD1_DIM_DQ_DQ_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

0x1AC80110 DIM_BD1_DIM_DQ_DQS_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQS_IOC_SLV_CFG register configures DIM_DQ_DQS_IOC_SLV_CFG.

DIM_BD1_DIM_DQ_DQS_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1AC80114 DIM_BD1_DIM_DQ_DQS_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQS_IOC_SLV_STATUS register configures DIM_DQ_DQS_IOC_SLV_STATUS.

DIM_BD1_DIM_DQ_DQS_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

7.6 DIM BC1 CA Top Configuration Registers (0x1B040000 DIM_BC1_REG_BASE)

This section describes the BC1 DIM CA TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1B040000 DIM_BC1_DIM_CA_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_CA_TOP_CFG register configures DIM_CA_TOP_CFG.

DIM_BC1_DIM_CA_TOP_CFG

Bits	Name	Description
20	IOCAL_CTLR_SEL	Select source of PCNT/NCNT/PNCNT_VALID 1’b1: external 1’b0: internal (default)
16	SDR_MODE_EN	1’b1 : Enables SDR mode on address bus 1’b0 : Enables DDR mode on address bus (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1: From IOCAL 1’b0: From CDCCAL (default)
12	DEBUG_BUS_EN	1’b1: Enables the debug bus functionality 1’b0: Disables the debug bus and drives all ’0’s on the debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_ca[7:5] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1’b0) 1’b1 : with pipe extend (default) 1’b0: without pipe extend
0	WR_CLK_SEL	Write clock select 1’b1 : With write CDC (default) 1’b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1B040004 DIM_BC1_DIM_CA_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_CA_HW_INFO register configures DIM_CA_HW_INFO.

DIM_BC1_DIM_CA_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1B040008 DIM_BC1_DIM_CA_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_CA_HW_VERSION register configures DIM_CA_HW_VERSION.

DIM_BC1_DIM_CA_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1B040010 DIM_BC1_DIM_CA_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_CA_PAD_CFG0 register configures DIM_CA_PAD_CFG0.

DIM_BC1_DIM_CA_PAD_CFG0

Bits	Name	Description
31	CA_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	CA_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	CA_LV_MODE	Mode pin for high/low voltage regime
28	CA_ODT_ENA	Enable bit for on-die termination
27:26	CA_ODT	Impedance control bit settings for on-die termination
25:24	CA_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	CA_NSLEW	Slew rate control bits for output path NMOS
17:16	CA_PSLEW	Slew rate control bits for output path PMOS
13:12	CA_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	CA_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	CA_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	CA_ROUT	Impedance control bit settings for output driver
2:0	CA_DCC	Duty cycle correction bits for output path

0x1B040014 DIM_BC1_DIM_CA_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0220440

The DIM_CA_PAD_CFG1 register configures DIM_CA_PAD_CFG1.

DIM_BC1_DIM_CA_PAD_CFG1

Bits	Name	Description
31	CK_DDR_MODE1	Mode select for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes

DIM_BC1_DIM_CA_PAD_CFG1 (cont.)

Bits	Name	Description
30	CK_DDR_MODE0	Mode select for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	CK_LV_MODE	Mode select for high/low voltage regime
28	CK_CMFB_ENA	Common mode feedback loop enable
27	CK_ODT_ENA1	Enable bit for on-die termination (when hp_mode = 1'b1)
26	CK_ODT_ENA	Enable bit for on-die termination (when hp_mode = 1'b0) Bit field name missing '0' for APQ8064 SW compatibility.
25:24	CK_ODT	Impedance control bit settings for on-die termination
21:20	CK_NSLEW	Slew rate control bits for output path NMOS
17:16	CK_PSLEW	Slew rate control bits for output path PMOS
13	CK_CUR_MODE1	Current/Voltage mode selection (when hp_mode = 1'b1) 1'b1 : Current mode 1'b0 : Voltage mode (default)
12	CK_CUR_MODE0	Current/Voltage mode selection (when hp_mode = 1'b0) 1'b1 : Current mode 1'b0 : Voltage mode (default)
10:8	CK_I_DRV	Control bit settings for bias current
7	CK_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	CK_ROUT	Impedance control bit settings for output driver
2:0	CK_DCC	Duty cycle correction bits for output path

0x1B040018 DIM_BC1_DIM_CA_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_CA_PAD_CFG2 register configures DIM_CA_PAD_CFG2.

DIM_BC1_DIM_CA_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused

DIM_BC1_DIM_CA_PAD_CFG2 (cont.)

Bits	Name	Description
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1B04001C DIM_BC1_DIM_CA_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x00300000

The DIM_CA_PAD_CFG3 register configures DIM_CA_PAD_CFG3.

DIM_BC1_DIM_CA_PAD_CFG3

Bits	Name	Description
31:30	CS_N_IE	
29:28	CS_N_OE	
25	CK_IE	
24	CK_OE	
23:22	CKE_IE	
21:20	CKE_OE	
19:10	CA_IE	
9:0	CA_OE	

0x1B040020 DIM_BC1_DIM_CA_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_PAD_CFG4 register configures DIM_CA_PAD_CFG4.

DIM_BC1_DIM_CA_PAD_CFG4

Bits	Name	Description
31:30	CS_N_OE_DYN_ENA	Enable dynamic control of CS_N OE 1'b1: Dynamic control enabled and CS_N_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CS_N OE gated by CA_PAD_CFG3 bits **NOTE** This register should not be set in external loopback mode since it will change the IE contol source.
29:28	CS_N_OE_DYN	Dynamic OE control for each of the CS_N outputs, OR-ed with common controller OE.
25	RESERVED_1	
24	RESERVED_2	
23:22	CKE_OE_DYN_ENA	Enable dynamic control of CKE OE 1'b1: Dynamic control enabled and CKE_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CKE OE gated by CA_PAD_CFG3 bits
21:20	CKE_OE_DYN	Dynamic OE control for each of the CA outputs, OR-ed with common controller OE.
19:10	CA_OE_DYN_ENA	Enable dynamic control of CA OE 1'b1: Dynamic control enabled and CA_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CA OE gated by CA_PAD_CFG3 bits
9:0	CA_OE_DYN	Dynamic OE control for each of the CA outputs, OR-ed with common controller OE.

0x1B040030 DIM_BC1_DIM_CA_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CTLR_CFG0 register configures DIM_CA_CDC_CTLR_CFG0.

DIM_BC1_DIM_CA_CDC_CTLR_CFG0

Bits	Name	Description
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration

DIM_BC1_DIM_CA_CDC_CTLR_CFG0 (cont.)

Bits	Name	Description
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1B040034 DIM_BC1_DIM_CA_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CTLR_CFG1 register configures DIM_CA_CDC_CTLR_CFG1.

DIM_BC1_DIM_CA_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.

DIM_BC1_DIM_CA_CDC_CTLR_CFG1 (cont.)

Bits	Name	Description
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used.
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1.
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1.
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1.
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1.

0x1B040038 DIM_BC1_DIM_CA_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CAL_TIMER_CFG0 register configures DIM_CA_CDC_CAL_TIMER_CFG0.

DIM_BC1_DIM_CA_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.

DIM_BC1_DIM_CA_CDC_CAL_TIMER_CFG0 (cont.)

Bits	Name	Description
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1B04003C DIM_BC1_DIM_CA_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CAL_TIMER_CFG1 register configures DIM_CA_CDC_CAL_TIMER_CFG1.

DIM_BC1_DIM_CA_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1B040040 DIM_BC1_DIM_CA_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_REFCOUNT_CFG register configures DIM_CA_CDC_REFCOUNT_CFG.

DIM_BC1_DIM_CA_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.

DIM_BC1_DIM_CA_CDC_REFCOUNT_CFG (cont.)

Bits	Name	Description
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1B040044 DIM_BC1_DIM_CA_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_CA_CDC_COARSE_CAL_CFG configures DIM_CA_CDC_COARSE_CAL_CFG.

DIM_BC1_DIM_CA_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	Unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1B040048 DIM_BC1_DIM_CA_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_RSVD_CFG register configures DIM_CA_CDC_RSVD_CFG.

DIM_BC1_DIM_CA_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1B04004C DIM_BC1_DIM_CA_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_OFFSET_CFG register configures DIM_CA_CDC_OFFSET_CFG.

DIM_BC1_DIM_CA_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1B040050 DIM_BC1_DIM_CA_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_DELAY_CFG register configures DIM_CA_CDC_DELAY_CFG.

DIM_BC1_DIM_CA_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1B040054 DIM_BC1_DIM_CA_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_SW_MODE_CFG register configures DIM_CA_CDC_SW_MODE_CFG.

DIM_BC1_DIM_CA_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1B040058 DIM_BC1_DIM_CA_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_TEST_CFG register configures DIM_CA_CDC_TEST_CFG.

DIM_BC1_DIM_CA_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1B04005C DIM_BC1_DIM_CA_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_TEST_CFG register configures DIM_CA_CDC_SW_OVRD_CFG.

DIM_BC1_DIM_CA_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1B040070 DIM_BC1_DIM_CA_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_CA_CDC_STATUS0 register configures DIM_CA_CDC_STATUS0.

DIM_BC1_DIM_CA_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. **NOTE** The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1B040074 DIM_BC1_DIM_CA_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_STATUS1 register configures DIM_CA_CDC_STATUS1.

DIM_BC1_DIM_CA_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.

DIM_BC1_DIM_CA_CDC_STATUS1 (cont.)

Bits	Name	Description
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1B040078 DIM_BC1_DIM_CA_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_CA_CDC_STATUS2 register configures DIM_CA_CDC_STATUS2.

DIM_BC1_DIM_CA_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1B04007C DIM_BC1_DIM_CA_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_STATUS3 register configures DIM_CA_CDC_STATUS3.

DIM_BC1_DIM_CA_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking.
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration.
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1B0400E0 DIM_BC1_DIM_CA_IOC_CTLR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_CFG register configures DIM_CA_IOC_CTLR_CFG.

DIM_BC1_DIM_CA_IOC_CTLR_CFG

Bits	Name	Description
31	CAL_NOW	SW: RW Set this bit to 1'b1 will cause the IO calibration starts immediately. This bit has to be cleared after the calibration has been done. 0x0: no-op 0x1: start IOCal immediately
30	IO_CAL_AUTO	Periodic auto calibration mode. Writing a '1' to this bit will trigger periodic auto calibration with the period specified in IOC_CTLR_TIMER_CFG register. If '0', it disables the timer based on sleep clock. Note that this does not impact the timer based on fixed frequency clock (ffclk).
29	IO_CAL_FF_TIMER_EN	Fixed Frequency Timer mode. Writing a '1' to this bit will set the timer running off tcxo clock. If '0', it disables the timer based on fixed frequency clock.
28	IO_CAL_BANDGAP_DYN_CTRL	Enable dynamic control of the bandgap element: This low-power feature is only available on x2 core. Bit reserved for x0/x1 cores. 1'b1: Enabled - bandgap element turned on only during IO calibration or when current mode is enabled. 1'b0: Disabled (default) - bandgap element turned on/off statically based on BANDHGAP_ENA0/1 bits.
25	SW_FFCLK_ON	Writing a '1' to this field will turn on the fixed frequency (xo) clock on signal
24	LV_MODE	SW: RW Enable/Disable low-voltage mode (MIF2 pad only) 0x0: 1.8V 0x1: non-1.8V
20:16	MARGIN_LOAD	SW: RW If the difference between the current IOCal result is greater than the last result by the number specified here, then the IOCal controller will request value update to DDR controller. 0x0: always update
13:12	IMP_SEL	SW: RW Select bits to choose which impedance to calibrate to.

DIM_BC1_DIM_CA_IOC_CTLR_CFG (cont.)

Bits	Name	Description
10	PN_SEL_CA	SW: RW Enables loading of HW calibrated values for ca pads. Writing a ’1’ to this bit would let the IOCAL to request traffic stall on ca pads when it is time to update the pads with the new value.
9	PN_SEL_DATA	SW: RW Enables loading of HW calibrated values for dq/dqs pads. Writing a ’1’ to this bit would let the IOCAL to request traffic stall on data pads when it is time to update the pads with the new value.
8	CAL_USE_LAST	SW: RW Select the initial value to start IO calibration 0x0: start from a fixed values specified in IOC_CTLR_PNCNT_CFG (default) 0x1: start from previous IOCal PNCNT results
6:4	SAMPLE_POINT	SW: RW Specify number of samples per measure point 0x0: 1 0x1: 3 0x2: 5 0x3: 7 0x4: 9 0x5: 11 0x6: 13 0x7: 15
3	DDR_MODE1	
2	DDR_MODE0	
1	BANDGAP_ENA1	SW : RW Pin to enable bandgap independent of diff_ctl 0x0: disable 0x1: enable
0	BANDGAP_ENA0	SW : RW Pin to enable bandgap independent of diff_ctl 0x0: disable 0x1: enable

0x1B0400E4 DIM_BC1_DIM_CA_IOC_CTLR_PNCNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_CFG register configures DIM_CA_IOC_CTLR_CFG.

This register contains the initial value for the next calibration to start from. Softwave can set the hardware to either start calibration from a fixed value or from previous results. If software chooses to use fixed value by setting CAN_USE_LAST in register IOC_CTLR_CFG to be 0, then the values in this register will be used.

DIM_BC1_DIM_CA_IOC_CTLR_PNCNT_CFG

Bits	Name	Description
12:8	NCNT_INIT_CSR	SW: RW Starting PCNT value used in calibration. Only take effect when CAN_USE_LAST is asserted
4:0	PCNT_INIT_CSR	SW: RW Starting NCNT value used in calibration. Only take effect when CAN_USE_LAST is asserted

0x1B0400E8 DIM_BC1_DIM_CA_IOC_CTLR_TIMER_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_TIMER_CFG register configures DIM_CA_IOC_CTLR_TIMER_CFG.

DIM_BC1_DIM_CA_IOC_CTLR_TIMER_CFG

Bits	Name	Description
31:16	TIMER_PERIOD	SW: RW Recalibration Period. The period is measured in timer clock cycles. Typically it's a 32kHz clock. The minimum period that can be programmed is 3. 0,1,2: Invalid values
15:0	FF_TIMER_PERIOD	SW: RW Recalibration Period for the timer running of xo clock. 0x0: Invalid

0x1B0400EC DIM_BC1_DIM_CA_IOC_CTLR_TIMER_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_TIMER_STATUS register configures DIM_CA_IOC_CTLR_TIMER_STATUS.

DIM_BC1_DIM_CA_IOC_CTLR_TIMER_STATUS

Bits	Name	Description
15:0	TIMER_STATUS	Current Auto Calibration Timer value. As this register is written in sleep clock domain and read in xo clock domain and no hardware synchronization in place, It is required by the software to read this register 4 times to get the correct value.

0x1B0400F0 DIM_BC1_DIM_CA_IOC_CTLR_CHAR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_ CHAR_CFG register configures IDIM_CA_IOC_CTLR_CHAR_CFG.

This register is used by hardware verification software only. It provides a mechanism to allow software to bypass the internal calibration state machine and directly access the IOCAL pad inputs.

DIM_BC1_DIM_CA_IOC_CTLR_CHAR_CFG

Bits	Name	Description
16	SM_BYP_ENA	SW : RW Characterization Bypass Path Enable 0x0: Non-bypass: State Machine Controls IOCAL pad inputs (default) 0x1: bypass: This register controls IOCal pad inputs
15	SM_BYP_N_ENA	SW: RW IO CAL Characterization n_enable: 0x0: de-asserted (default) 0x1: asserted
12:8	SM_BYP_NCNT	SW: RW IO CAL Characterization ncnt value. 0x0: count 0 (default)
7	SM_BYP_P_ENA	SW: RW IO CAL Characterization p_enable: 0x0: de-asserted (default) 0x1: asserted
4:0	SM_BYP_PCNT	SW: RW IO CAL Characterization pcnt value. 0x0: count 0 (default)

0x1B0400F4 DIM_BC1_DIM_CA_IOC_CTLR_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00011010

The DIM_CA_IOC_CTLR_STATUS register configures DIM_CA_IOC_CTLR_STATUS.

DIM_BC1_DIM_CA_IOC_CTLR_STATUS

Bits	Name	Description
31	INIT_IOCAL_DONE	SW: R The very first IO Calibration is finished This bit is stiky. once it becomes 1’b1 until software writes it back to 0. 0x0: Init-cal never done 0x1: Init-cal finished
18	IOCAL_DONE_D	SW: R IO Calibration is finished 0x0: in progress 0x1: finished
17	IOCAL_BUSY	SW: R Status of calibration State machine 0x0: idle 0x1: busy
16	SYNC_COMP	SW: R comp value from IOCal pad
12:8	NCNT_HOLD	SW: R Current NCNT value used
4:0	PCNT_HOLD	SW: R Current PCNT value used

0x1B040100 DIM_BC1_DIM_CA_CA_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_CA_CA_IOC_SLV_CFG register configures DIM_CA_CA_IOC_SLV_CFG.

This register specifies the overriding pcnt and ncnt values. Overriding mode is controlled by PNCNT_HW_LOAD_EN bit in this register.

DIM_BC1_DIM_CA_CA_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	Select PCNT/NCNT Source for pads. This is the mux control that chooses either auto calibrated value or the software override value. 0x0: override (default) 0x1: auto cal
28:24	NCNT_SW_VAL	SW: RW NCNT Override Value for the pads
20:16	PCNT_SW_VAL	SW: RW PCNT Override Value for the pads
15	NCNT_OFFSET_SIGN	Controls if the NOFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
12:8	NCNT_SW_OFFSET	SW: RW The offiset applied on top of NCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)
7	PCNT_OFFSET_SIGN	Controls if the POFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
4:0	PCNT_SW_OFFSET	SW: RW The offiset applied on top of PCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)

0x1B040104 DIM_BC1_DIM_CA_CA_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_CA_CA_IOC_SLV_STATUS register configures DIM_CA_CA_IOC_SLV_STATUS.

DIM_BC1_DIM_CA_CA_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	The final NCNT value that is applied to the pads.
4:0	PAD_PCNT	The final PCNT value that is applied to the pads.

0x1B040110 DIM_BC1_DIM_CA_CK_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_CA_CK_IOC_SLV_CFG register configures DIM_CA_CK_IOC_SLV_CFG.

DIM_BC1_DIM_CA_CK_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	Select PCNT/NCNT Source for pads. This is the mux control that chooses either auto calibrated value or the software override value. 0x0: override (default) 0x1: auto cal
28:24	NCNT_SW_VAL	SW: RW NCNT Override Value for the pads
20:16	PCNT_SW_VAL	SW: RW PCNT Override Value for the pads
15	NCNT_OFFSET_SIGN	Controls if the NOFFSET is added for subtracted on top of calibration result. 0x0: Add 0x1: Subtract
12:8	NCNT_SW_OFFSET	SW: RW The offiset applied on top of NCNT value from calibration before it gets sent to IO pads. 0x0: count 0 (default)
7	PCNT_OFFSET_SIGN	Controls if the POFFSET is added for subtracted on top of calibration result. 0x0: Add 0x1: Subtract
4:0	PCNT_SW_OFFSET	SW: RW The offiset applied on top of PCNT value from calibration before it gets sent to IO pads. 0x0: count 0 (default)

0x1B040114 DIM_BC1_DIM_CA_CK_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_CA_CK_IOC_SLV_STATUS register configures DIM_CA_CK_IOC_SLV_STATUS.

DIM_BC1_DIM_CA_CK_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	The final NCNT value that is applied to the pads.
4:0	PAD_PCNT	The final PCNT value that is applied to the pads.

7.7 DIM C11 CA Top Configuration Registers (0x1B080000 DIM_C11_REG_BASE)

This section describes the C11 DIM CA TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1B080000 DIM_C11_DIM_CA_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_CA_TOP_CFG register configures DIM_CA_TOP_CFG.

DIM_C11_DIM_CA_TOP_CFG

Bits	Name	Description
20	IOCAL_CTLR_SEL	Select source of PCNT/NCNT/PNCNT_VALID 1’b1: external 1’b0: internal (default)
16	SDR_MODE_EN	1’b1 : Enables SDR mode on address bus 1’b0 : Enables DDR mode on address bus (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1: From IOCAL 1’b0: From CDCCAL (default)
12	DEBUG_BUS_EN	1’b1: Enables the debug bus functionality 1’b0: Disables the debug bus and drives all ’0’s on the debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_ca[7:5] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1’b0) 1’b1 : with pipe extend (default) 1’b0: without pipe extend
0	WR_CLK_SEL	Write clock select 1’b1 : With write CDC (default) 1’b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1B080004 DIM_C11_DIM_CA_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_CA_HW_INFO register configures DIM_CA_HW_INFO.

DIM_C11_DIM_CA_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1B080008 DIM_C11_DIM_CA_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_CA_HW_VERSION register configures DIM_CA_HW_VERSION.

DIM_C11_DIM_CA_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1B080010 DIM_C11_DIM_CA_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_CA_PAD_CFG0 register configures DIM_CA_PAD_CFG0.

DIM_C11_DIM_CA_PAD_CFG0

Bits	Name	Description
31	CA_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	CA_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	CA_LV_MODE	Mode pin for high/low voltage regime
28	CA_ODT_ENA	Enable bit for on-die termination
27:26	CA_ODT	Impedance control bit settings for on-die termination
25:24	CA_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	CA_NSLEW	Slew rate control bits for output path NMOS
17:16	CA_PSLEW	Slew rate control bits for output path PMOS
13:12	CA_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	CA_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	CA_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	CA_ROUT	Impedance control bit settings for output driver
2:0	CA_DCC	Duty cycle correction bits for output path

0x1B080014 DIM_C11_DIM_CA_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0220440

The DIM_CA_PAD_CFG1 register configures DIM_CA_PAD_CFG1.

DIM_C11_DIM_CA_PAD_CFG1

Bits	Name	Description
31	CK_DDR_MODE1	Mode select for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes

DIM_C11_DIM_CA_PAD_CFG1 (cont.)

Bits	Name	Description
30	CK_DDR_MODE0	Mode select for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	CK_LV_MODE	Mode select for high/low voltage regime
28	CK_CMFB_ENA	Common mode feedback loop enable
27	CK_ODT_ENA1	Enable bit for on-die termination (when hp_mode = 1'b1)
26	CK_ODT_ENA	Enable bit for on-die termination (when hp_mode = 1'b0) Bit field name missing '0' for APQ8064 SW compatibility.
25:24	CK_ODT	Impedance control bit settings for on-die termination
21:20	CK_NSLEW	Slew rate control bits for output path NMOS
17:16	CK_PSLEW	Slew rate control bits for output path PMOS
13	CK_CUR_MODE1	Current/Voltage mode selection (when hp_mode = 1'b1) 1'b1 : Current mode 1'b0 : Voltage mode (default)
12	CK_CUR_MODE0	Current/Voltage mode selection (when hp_mode = 1'b0) 1'b1 : Current mode 1'b0 : Voltage mode (default)
10:8	CK_I_DRV	Control bit settings for bias current
7	CK_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	CK_ROUT	Impedance control bit settings for output driver
2:0	CK_DCC	Duty cycle correction bits for output path

0x1B080018 DIM_C11_DIM_CA_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_CA_PAD_CFG2 register configures DIM_CA_PAD_CFG2.

DIM_C11_DIM_CA_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused

DIM_C11_DIM_CA_PAD_CFG2 (cont.)

Bits	Name	Description
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1B08001C DIM_C11_DIM_CA_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x00300000

The DIM_CA_PAD_CFG3 register configures DIM_CA_PAD_CFG3.

DIM_C11_DIM_CA_PAD_CFG3

Bits	Name	Description
31:30	CS_N_IE	
29:28	CS_N_OE	
25	CK_IE	
24	CK_OE	
23:22	CKE_IE	
21:20	CKE_OE	
19:10	CA_IE	
9:0	CA_OE	

0x1B080020 DIM_C11_DIM_CA_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_PAD_CFG4 register configures DIM_CA_PAD_CFG4.

DIM_C11_DIM_CA_PAD_CFG4

Bits	Name	Description
31:30	CS_N_OE_DYN_ENA	Enable dynamic control of CS_N OE 1'b1: Dynamic control enabled and CS_N_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CS_N OE gated by CA_PAD_CFG3 bits **NOTE** This register should not be set in external loopback mode since it will change the IE contol source.
29:28	CS_N_OE_DYN	Dynamic OE control for each of the CS_N outputs, OR-ed with common controller OE.
25	RESERVED_1	
24	RESERVED_2	
23:22	CKE_OE_DYN_ENA	Enable dynamic control of CKE OE 1'b1: Dynamic control enabled and CKE_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CKE OE gated by CA_PAD_CFG3 bits
21:20	CKE_OE_DYN	Dynamic OE control for each of the CA outputs, OR-ed with common controller OE.
19:10	CA_OE_DYN_ENA	Enable dynamic control of CA OE 1'b1: Dynamic control enabled and CA_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CA OE gated by CA_PAD_CFG3 bits
9:0	CA_OE_DYN	Dynamic OE control for each of the CA outputs, OR-ed with common controller OE.

0x1B080030 DIM_C11_DIM_CA_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CTLR_CFG0 register configures DIM_CA_CDC_CTLR_CFG0.

DIM_C11_DIM_CA_CDC_CTLR_CFG0

Bits	Name	Description
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration

DIM_C11_DIM_CA_CDC_CTLR_CFG0 (cont.)

Bits	Name	Description
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1B080034 DIM_C11_DIM_CA_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CTLR_CFG1 register configuresDIM_CA_CDC_CTLR_CFG1.

DIM_C11_DIM_CA_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.

DIM_C11_DIM_CA_CDC_CTLR_CFG1 (cont.)

Bits	Name	Description
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used.
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1.
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1.
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1.
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1.

0x1B080038 DIM_C11_DIM_CA_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CAL_TIMER_CFG0 register configures DIM_CA_CDC_CAL_TIMER_CFG0.

DIM_C11_DIM_CA_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.

DIM_C11_DIM_CA_CDC_CAL_TIMER_CFG0 (cont.)

Bits	Name	Description
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1B08003C DIM_C11_DIM_CA_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CAL_TIMER_CFG1 register configures DIM_CA_CDC_CAL_TIMER_CFG1.

DIM_C11_DIM_CA_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1B080040 DIM_C11_DIM_CA_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_REFCOUNT_CFG register configures DIM_CA_CDC_REFCOUNT_CFG.

DIM_C11_DIM_CA_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.

DIM_C11_DIM_CA_CDC_REFCOUNT_CFG (cont.)

Bits	Name	Description
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1B080044 DIM_C11_DIM_CA_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_CA_CDC_COARSE_CAL_CFG configures DIM_CA_CDC_COARSE_CAL_CFG.

DIM_C11_DIM_CA_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	Unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1B080048 DIM_C11_DIM_CA_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_RSVD_CFG register configures DIM_CA_CDC_RSVD_CFG.

DIM_C11_DIM_CA_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1B08004C DIM_C11_DIM_CA_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_OFFSET_CFG register configures DIM_CA_CDC_OFFSET_CFG.

DIM_C11_DIM_CA_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1B080050 DIM_C11_DIM_CA_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_DELAY_CFG register configures DIM_CA_CDC_DELAY_CFG.

DIM_C11_DIM_CA_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1B080054 DIM_C11_DIM_CA_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_SW_MODE_CFG register configures DIM_CA_CDC_SW_MODE_CFG.

DIM_C11_DIM_CA_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1B080058 DIM_C11_DIM_CA_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_TEST_CFG register configures DIM_CA_CDC_TEST_CFG.

DIM_C11_DIM_CA_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1B08005C DIM_C11_DIM_CA_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_TEST_CFG register configures DIM_CA_CDC_SW_OVRD_CFG.

DIM_C11_DIM_CA_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1B080070 DIM_C11_DIM_CA_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_CA_CDC_STATUS0 register configures DIM_CA_CDC_STATUS0.

DIM_C11_DIM_CA_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. **NOTE** The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1B080074 DIM_C11_DIM_CA_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_STATUS1 register configures DIM_CA_CDC_STATUS1.

DIM_C11_DIM_CA_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.

DIM_C11_DIM_CA_CDC_STATUS1 (cont.)

Bits	Name	Description
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1B080078 DIM_C11_DIM_CA_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_CA_CDC_STATUS2 register configures DIM_CA_CDC_STATUS2.

DIM_C11_DIM_CA_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1B08007C DIM_C11_DIM_CA_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_STATUS3 register configures DIM_CA_CDC_STATUS3.

DIM_C11_DIM_CA_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1B0800E0 DIM_C11_DIM_CA_IOC_CTLR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_CFG register configures DIM_CA_IOC_CTLR_CFG.

DIM_C11_DIM_CA_IOC_CTLR_CFG

Bits	Name	Description
31	CAL_NOW	SW: RW Set this bit to 1'b1 will cause the IO calibration starts immediately. This bit has to be cleared after the calibration has been done. 0x0: no-op 0x1: start IOCal immediately
30	IO_CAL_AUTO	Periodic auto calibration mode. Writing a '1' to this bit will trigger periodic auto calibration with the period specified in IOC_CTLR_TIMER_CFG register. If '0', it disables the timer based on sleep clock. Note that this does not impact the timer based on fixed frequency clock (ffclk).
29	IO_CAL_FF_TIMER_EN	Fixed Frequency Timer mode. Writing a '1' to this bit will set the timer running off tcxo clock. If '0', it disables the timer based on fixed frequency clock.
28	IO_CAL_BANDGAP_DYN_CTRL	Enable dynamic control of the bandgap element: This low-power feature is only available on x2 core. Bit reserved for x0/x1 cores. 1'b1: Enabled - bandgap element turned on only during IO calibration or when current mode is enabled. 1'b0: Disabled (default) - bandgap element turned on/off statically based on BANDHGAP_ENA0/1 bits.
25	SW_FFCLK_ON	Writing a '1' to this field will turn on the fixed frequency (xo) clock on signal
24	LV_MODE	SW: RW Enable/Disable low-voltage mode (MIF2 pad only) 0x0: 1.8V 0x1: non-1.8V
20:16	MARGIN_LOAD	SW: RW If the difference between the current IOCal result is greater than the last result by the number specified here, then the IOCal controller will request value update to DDR controller. 0x0: always update
13:12	IMP_SEL	SW: RW Select bits to choose which impedance to calibrate to

DIM_C11_DIM_CA_IOC_CTLR_CFG (cont.)

Bits	Name	Description
10	PN_SEL_CA	SW: RW Enables loading of HW calibrated values for ca pads. Writing a ’1’ to this bit would let the IOCAL to request traffic stall on ca pads when it is time to update the pads with the new value.
9	PN_SEL_DATA	SW: RW Enables loading of HW calibrated values for dq/dqs pads. Writing a ’1’ to this bit would let the IOCAL to request traffic stall on data pads when it is time to update the pads with the new value.
8	CAL_USE_LAST	SW: RW Select the initial value to start IO calibration 0x0: start from a fixed values specified in IOC_CTLR_PNCNT_CFG (default) 0x1: start from previous IOCal PNCNT results
6:4	SAMPLE_POINT	SW: RW Specify number of samples per measure point 0x0: 1 0x1: 3 0x2: 5 0x3: 7 0x4: 9 0x5: 11 0x6: 13 0x7: 15
3	DDR_MODE1	
2	DDR_MODE0	
1	BANDGAP_ENA1	SW: RW Pin to enable bandgap independent of diff_ctl 0x0: disable 0x1: enable
0	BANDGAP_ENA0	SW: RW Pin to enable bandgap independent of diff_ctl 0x0: disable 0x1: enable

0x1B0800E4 DIM_C11_DIM_CA_IOC_CTLR_PNCNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_CFG register configures DIM_CA_IOC_CTLR_CFG.

This register contains the initial value for the next calibration to start from. Softwave can set the hardware to either start calibration from a fixed value or from previous results. If software chooses to use fixed value by setting CAN_USE_LAST in register IOC_CTLR_CFG to be 0, then the values in this register will be used.

DIM_C11_DIM_CA_IOC_CTLR_PNCNT_CFG

Bits	Name	Description
12:8	NCNT_INIT_CSR	SW : RW Starting PCNT value used in calibration. Only take effect when CAN_USE_LAST is asserted
4:0	PCNT_INIT_CSR	SW : RW Starting NCNT value used in calibration. Only take effect when CAN_USE_LAST is asserted

0x1B0800E8 DIM_C11_DIM_CA_IOC_CTLR_TIMER_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_TIMER_CFG register configures DIM_CA_IOC_CTLR_TIMER_CFG.

DIM_C11_DIM_CA_IOC_CTLR_TIMER_CFG

Bits	Name	Description
31:16	TIMER_PERIOD	SW : RW Recalibration Period. The period is measured in timer clock cycles. Typically it's a 32kHz clock. The minimum period that can be programmed is 3. 0,1,2: Invalid values
15:0	FF_TIMER_PERIOD	SW : RW Recalibration Period for the timer running of xo clock. 0x0: Invalid

0x1B0800EC DIM_C11_DIM_CA_IOC_CTLR_TIMER_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_TIMER_STATUS register configures DIM_CA_IOC_CTLR_TIMER_STATUS.

DIM_C11_DIM_CA_IOC_CTLR_TIMER_STATUS

Bits	Name	Description
15:0	TIMER_STATUS	Current Auto Calibration Timer value. As this register is written in sleep clock domain and read in xo clock domain and no hardware synchronization in place, It is required by the software to read this register 4 times to get the correct value.

0x1B0800F0 DIM_C11_DIM_CA_IOC_CTLR_CHAR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_ CHAR_CFGregister configures IDIM_CA_IOC_CTLR_CHAR_CFG.

This register is used by hardware verification software only. It provides a mechanism to allow software to bypass the internal calibration state machine and directly access the IOCAL pad inputs.

DIM_C11_DIM_CA_IOC_CTLR_CHAR_CFG

Bits	Name	Description
16	SM_BYP_ENA	SW: RW Characterization Bypass Path Enable 0x0: Non-bypass: State Machine Controls IOCAL pad inputs (default) 0x1: bypass: This register controls IOCal pad inputs
15	SM_BYP_N_ENA	SW: RW IO CAL Characterization n_enable: 0x0: de-asserted (default) 0x1: asserted
12:8	SM_BYP_NCNT	SW: RW IO CAL Characterization ncnt value. 0x0: count 0 (default)
7	SM_BYP_P_ENA	SW: RW IO CAL Characterization p_enable: 0x0: de-asserted (default) 0x1: asserted
4:0	SM_BYP_PCNT	SW: RW IO CAL Characterization pcnt value. 0x0: count 0 (default)

0x1B0800F4 DIM_C11_DIM_CA_IOC_CTLR_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00011010

The DIM_CA_IOC_CTLR_STATUS register configures DIM_CA_IOC_CTLR_STATUS.

DIM_C11_DIM_CA_IOC_CTLR_STATUS

Bits	Name	Description
31	INIT_IOCAL_DONE	SW: R The very first IO Calibration is finished This bit is stiky. once it becomes 1'b1 until software writes it back to 0. 0x0: Init-cal never done 0x1: Init-cal finished
18	IOCAL_DONE_D	SW: R IO Calibration is finished 0x0: in progress 0x1: finished
17	IOCAL_BUSY	SW: R Status of calibration State machine 0x0: idle 0x1: busy
16	SYNC_COMP	SW: R comp value from IOCal pad
12:8	NCNT_HOLD	SW: R Current NCNT value used
4:0	PCNT_HOLD	SW: R Current PCNT value used

0x1B080100 DIM_C11_DIM_CA_CA_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_CA_CA_IOC_SLV_CFG register configures DIM_CA_CA_IOC_SLV_CFG.

This register specifies the overriding pcnt and ncnt values. Overriding mode is controlled by PNCNT_HW_LOAD_EN bit in this register.

DIM_C11_DIM_CA_CA_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	Select PCNT/NCNT Source for pads. This is the mux control that chooses either auto calibrated value or the software override value. 0x0: override (default) 0x1: auto cal
28:24	NCNT_SW_VAL	SW: RW NCNT Override Value for the pads
20:16	PCNT_SW_VAL	SW: RW PCNT Override Value for the pads
15	NCNT_OFFSET_SIGN	Controls if the NOFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
12:8	NCNT_SW_OFFSET	SW: RW The offiset applied on top of NCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)
7	PCNT_OFFSET_SIGN	Controls if the POFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
4:0	PCNT_SW_OFFSET	SW: RW The offiset applied on top of PCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)

0x1B080104 DIM_C11_DIM_CA_CA_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_CA_CA_IOC_SLV_STATUS register configures DIM_CA_CA_IOC_SLV_STATUS.

DIM_C11_DIM_CA_CA_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	The final NCNT value that is applied to the pads.
4:0	PAD_PCNT	The final PCNT value that is applied to the pads.

0x1B080110 DIM_C11_DIM_CA_CK_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_CA_CK_IOC_SLV_CFG register configures DIM_CA_CK_IOC_SLV_CFG.

DIM_C11_DIM_CA_CK_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	Select PCNT/NCNT Source for pads. This is the mux control that chooses either auto calibrated value or the software override value. 0x0: override (default) 0x1: auto cal
28:24	NCNT_SW_VAL	SW : RW NCNT Override Value for the pads
20:16	PCNT_SW_VAL	SW: RW PCNT Override Value for the pads
15	NCNT_OFFSET_SIGN	Controls if the NOFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
12:8	NCNT_SW_OFFSET	SW: RW The offiset applied on top of NCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)
7	PCNT_OFFSET_SIGN	Controls if the POFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
4:0	PCNT_SW_OFFSET	SW: RW The offiset applied on top of PCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)

0x1B080114 DIM_C11_DIM_CA_CK_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_CA_CK_IOC_SLV_STATUS register configures DIM_CA_CK_IOC_SLV_STATUS.

DIM_C11_DIM_CA_CK_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	The final NCNT value that is applied to the pads.
4:0	PAD_PCNT	The final PCNT value that is applied to the pads.

8 Fabrics Registers

8.1 Overview

Table 8-1 Fabrics Bases

Base Name	Parent	Address
SFAB_FABRIC_ID_REVISION_REG0	SFAB_BASE	0x01300000
SFAB_M2VMT_M2VMRv_2	SFAB_BASE	0x01300000
AFAB_FABRIC_ID_REVISION_REG0	AFAB_BASE	0x01400000
AFAB_M2VMT_M2VMRv_0	AFAB_BASE	0x01400000
DAY_CFG_FABRIC_ID_REVISION_REG0	DAY_CFG_BASE	0x01500000
FABRIC_ID_REVISION_REG0	FABRIC_MMSS_BASE	0x05200000

8.2 System Fabric Registers (0x01300000 SFAB_BASE)

This section contains the System Fabric registers.

0x01300000 SFAB_FABRIC_ID_REVISION_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x2C40

This register contains the upper 16-bits of the core ID and revision number and contains the Major/Minor Revision information as well as the site ID where the core was developed.

SFAB_FABRIC_ID_REVISION_REG0

Bits	Name	Description
15:13	MAJ	SW: R Major Revision 0x1: Initial Release
12:10	MIN	SW: R Minor Revision 0x3: APQ8064
9:6	SITE	SW: R Site ID 0x1: RTP
5:0	RESERVED_BITS_5_0	

0x01300004 SFAB_FABRIC_ID_REVISION_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0001

This register contains the lower 16-bits of the core ID and revision number and contains the Core ID number.

SFAB_FABRIC_ID_REVISION_REG1

Bits	Name	Description
15:8	RESERVED_BITS_3_2	
7:0	ID	SW : R Core ID 0x1: FABRIC

0x01300008 SFAB_FABRIC_CONFIGURATION_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0002

This register defines the operating frequency, power down mode for the performance monitor, as well as the decode error and performance monitor cycle counter interrupts. It also has the control bit to globally disable redirection in Fabric.

The ISYND bits contain the interrupt syndrome. If more than one interrupt type occurs, more than one bit will be set. For example, if a decode error occurs and the performance monitor cycle-counter expires, the ISYND field will contain the value 3'b101. Performance monitor interrupts are only generated when the interrupt enable (PMIE) bit is set for the interrupt type.

If multiple decode errors occur, only the first error is recorded. If multiple decode errors occur at the same clock cycle, only a single error is considered, with Master 0 having the highest priority and Master 14 the lowest priority.

The determination of the time an error is recorded in the Fabric Error Status Register (FESR) is based on the following criteria:

For Reads: When Mn_RLAST is asserted.

For Writes: When Mn_BRESP is asserted.

Therefore, if two different masters make requests with invalid addresses to the FABRIC, the master which receives the RLAST or BRESP first for the invalid transaction, is recorded in the FESR. See FABRIC_ERROR_STATUS_REG_1 for information that is captured when a decode error occurs. The address of the request which caused a decode error is captured in the FABRIC_ERROR_UPPER_ADDR_REG and the FABRIC_ERROR_LOWER_ADDR_REG. If they happen simultaneously, the master priority is used to resolve which error is recorded in a fixed priority scheme. Master 0 has highest priority and Master 31 has the lowest priority.

NOTE If the master does not have RREADY or BREADY asserted by default (i.e., it is not able to receive all responses for outstanding requests and may throttle the FABRIC), the FABRIC_Interrupt generation may precede the return of the last read data beat or the write response.

To clear the interrupt, the ISYND bits are required to be written to 3'b000.

The performance monitor event/tenure overflow condition is indicated when the ISYND value is 010. An event overflow occurs when the event counter has reached its maximum value. A tenure overflow condition occurs:

When the tenure counter has reached its maximum value

OR

More than 16 tenures are outstanding, since the performance monitor implements only 16 counters for tenure tracking. Note that if the tenure overflows, values read from the performance monitors

for min/max/total/last tenure will no longer be valid as values recorded after the overflow will be incorrect.

SFAB_FABRIC_CONFIGURATION_REG

Bits	Name	Description
15:7	RESERVED_BITS_15_7	Reserved Bits
6:4	ISYND	SW : RW Interrupt syndrome* 0x0: No/Clear (interrupt) 0x1: Cycle counter expired (Perfmon) 0x2: Event/tenure overflow (Perfmon) 0x4: Decode error detected 0x5: MPU Error 0x6: Timeout Error (SPB)
3	RESERVED_BITS_3	
2	CSPDM	SW:RW CSR block power down mode 0x0: Disable Dynamic Clock Gating 0x1: Enable Dynamic Clock Gating
1	PPDM	SW : RW Performance monitor power down/disable mode 0x0: Monitor Enabled 0x1: Monitor Disabled (Gates clocks to performance monitor registers)
0	PMIE	SW : RW Perfmon interrupt enable

0x01300100+4*n SFAB_FABRIC_SEGMENT_UADDR_0_REG_n, n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the upper and lower address ranges for a particular slave segment (n).If this slave segment (n) is a link then this register defines the first address range for the slave link.

NOTE A segmentation address register is required for each slave segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

SFAB_FABRIC_SEGMENT_UADDR_0_REG_n

Bits	Name	Description
15:10	RESERVED_15_10	
9:0	SUA	SW: RW Segment 'n' upper address (based on parameter- up to 10-bits)

0x01300200+4*n SFAB_FABRIC_SEGMENT_LADDR_0_REG_n, n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the upper and lower address ranges for a particular slave segment (n). If this slave segment (n) is a link then this register defines the first address range for the slave link.

NOTE A segmentation address register is required for each slave segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

SFAB_FABRIC_SEGMENT_LADDR_0_REG_n

Bits	Name	Description
15	SSE	SW: RW Slave segment n enable

SFAB_FABRIC_SEGMENT_LADDR_0_REG_n (cont.)

Bits	Name	Description
14	SSIE	SW: RW Slave segment "n" & "n+1" nterleave enable
13:10	RESERVED_13_10	
9:0	SLA	SW: RW Segment n lower address (based on parameter- up to 10-bits)

0x01300300+4*n SFAB_FABRIC_SEGMENT_UADDR_1_REG_n, n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the upper address for a particular slave link segment (n) if it's a link. A link segment can have up to two separate address ranges. This register defines the second address range for the slave link.

NOTE A link segmentation address register is required for each slave link segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

SFAB_FABRIC_SEGMENT_UADDR_1_REG_n

Bits	Name	Description
15:10	RESERVED_15_10	
9:0	SUA	SW : RW Segment 'n' upper address (based on parameter- up to 10-bits)

0x01300400+4*n SFAB_FABRIC_SEGMENT_LADDR_1_REG_n, n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the lower address range for a particular slave link segment (n). A link segment can have up to two separate address ranges. This register defines the second address range for the slave link.

NOTE A segmentation link address register is required for each slave link segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

SFAB_FABRIC_SEGMENT_LADDR_1_REG_n

Bits	Name	Description
15:10	RESERVED_15_10	
9:0	SLA	SW: RW Segment n lower address (based on parameter- up to 10-bits)

0x01301000+0x0100*n+4*m SFAB_FABRIC_m_WEIGHTING_REG_n, m=[0..14], n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

The values programmed into this register determine the Tier 2 weight for each master under the Tier Based Arbitration Scheme.

NOTE This register is required for each master and each slave segment supported by the FABRIC .

SFAB_FABRIC_m_WEIGHTING_REG_n

Bits	Name	Description
15:8	RESERVED_BITS_15_8	
7:0	M_M_W	SW: RW Master 'm' Weight

0x01302000+0x0100*n+4*m SFAB_FABRIC_m_QOS_REG_n, m=[0..3], n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

The values programmed into this register determine the Tier 1 weight for each master under the Tier Based Arbitration Scheme. Only 4 master ports can be configured as Tier 1. The QMC bits are used to configure a master port as Tier 1.

NOTE If more than one of these QOS Control registers are set to the same master port, unpredictable behavior will occur.

Set-up procedure:

1. Set the QOS enable bit.
2. Set the arbitration mode to Scheduled Access Time in the FABRIC arbitration configuration register FACR (See FABRIC_ARBITRATION_CONTROL_REG_n, n=[0..14]).
3. Configure the master port that needs to be set to Tier1.
4. Set the appropriate number of tokens/weight.
5. Set the MLT value (default is zero clock cycles).

NOTE Four of these registers are required for each slave segment supported by the FABRIC .

SFAB_FABRIC_m_QOS_REG_n

Bits	Name	Description
15:14	RESERVED_BITS15_13	
13:10	MLT	SW: RW MLT Value
9	QE	SW: RW QOS Enable

SFAB_FABRIC_m_QOS_REG_n (cont.)

Bits	Name	Description
8:4	QMC	SW: RW QOS Master Configuration 0x0: Master Port 0 0x1: Master Port 1 0x2: Master Port 2 0x3: Master Port 3 0x4: Master Port 4 0x5: Master Port 5 0x6: Master Port 6 0x7: Master Port 7 0x8: Master Port 8 0x9: Master Port 9 0xA: Master Port 10 0xB: Master Port 11 0xC: Master Port 12 0xD: Master Port 13 0xE: Master Port 14 0xF: Master Port 15 0x10: Master Port 16 0x11: Master Port 17 0x12: Master Port 18 0x13: Master Port 19 0x14: Master Port 20 0x15: Master Port 21 0x16: Master Port 22 0x17: Master Port 23 0x18: Master Port 24 0x19: Master Port 25 0x1A: Master Port 26 0x1B: Master Port 27 0x1C: Master Port 28 0x1D: Master Port 29 0x1E: Master Port 30 0x1F: Master Port 31
3:0	M_M_QW	SW : RW Master 'm' QOS Weight

0x01303000+4*n SFAB_FABRIC_BUS_INTERVAL_REG_n, n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register sets the bus interval value for Tier 2 masters.

NOTE A control register is implemented for each slave segment supported by the FABRIC .

SFAB_FABRIC_BUS_INTERVAL_REG_n

Bits	Name	Description
15:0	IBI	SW : RW Intct bus interval (in clock cycles)

0x01303100+4*n SFAB_FABRIC_QOS_INTERVAL_REG_n, n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register sets the QOS interval value for Tier 1 masters..

NOTE A control register is required for each slave segment supported by the FABRIC .

SFAB_FABRIC_QOS_INTERVAL_REG_n

Bits	Name	Description
15:8	RESERVED_BITS15_8	
7:0	QBI	SW : RW QOS bus interval (in clock cycles)

0x01303200+4*n SFAB_FABRIC_ARBITRATION_CONTROL_REG_n, n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x00FF

This register controls the arbitration mode and the pipeline depth of a particular slave segment.

NOTE A control register is implemented for each slave segment supported by the FABRIC .

SFAB_FABRIC_ARBITRATION_CONTROL_REG_n

Bits	Name	Description
15	QLP	SW: RW QOS Timer Low Power Mode 0x1: Enable 0x0: Disable
14:13	QHI	SW: RW QOS Timer Halt Interval 0x0: Stop after 1 interval of inactivity 0x1: Stop after 2 intervals of inactivity 0x2: Stop after 4 intervals of inactivity 0x3: Stop after 8 intervals of inactivity
12	BLP	SW: RW Bus Interval Low Power Mode 0x1: Enable 0x0: Disable
11:10	BHI	SW: RW Bus Interval Halt Interval 0x0: Stop after 1 interval of inactivity 0x1: Stop after 2 intervals of inactivity 0x2: Stop after 4 intervals of inactivity 0x3: Stop after 8 intervals of inactivity
9	QCE	SW : RW QoS Channel Enable 0x0: Disable (default) 0x1: Enable
8	IAM	SW : RW FABRIC arbitration mode 0x0: Fair round-robin (default) 0x1: Scheduled access time

SFAB_FABRIC_ARBITRATION_CONTROL_REG_n (cont.)

Bits	Name	Description
7:4	IRPD	SW : RW FABRIC read pipeline depth 0x0: Pipeline depth = 1 0x1: Pipeline depth = 2 0x2: Pipeline depth = 3 0x3: Pipeline depth = 4 0x4: Pipeline depth = 5 0x5: Pipeline depth = 6 0x6: Pipeline depth = 7 0x7: Pipeline depth = 8 0x8: Pipeline depth = 9 0x9: Pipeline depth = 10 0xA: Pipeline depth = 11 0xB: Pipeline depth = 12 0xC: Pipeline depth = 13 0xD: Pipeline depth = 14 0xE: Pipeline depth = 15 0xF: Pipeline depth = 16
3:0	IWPD	SW : RW FABRIC Write Pipeline Depth 0x0: Pipeline depth = 1 0x1: Pipeline depth = 2 0x2: Pipeline depth = 3 0x3: Pipeline depth = 4 0x4: Pipeline depth = 5 0x5: Pipeline depth = 6 0x6: Pipeline depth = 7 0x7: Pipeline depth = 8 0x8: Pipeline depth = 9 0x9: Pipeline depth = 10 0xA: Pipeline depth = 11 0xB: Pipeline depth = 12 0xC: Pipeline depth = 13 0xD: Pipeline depth = 14 0xE: Pipeline depth = 15 0xF: Pipeline depth = 16

0x01303300+4*n SFAB_FABRIC_MASTER_INTERFACE_REG_n, n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0084

This register controls the following master port attributes:

- whether the master request priority signals are used by the internal arbiter
- the redirection of cacheable coherent requests
- write gathering on AXI
- write packing on AHB

This register also controls a particular master's halt interface and for AHB master interfaces, it enables write packing functionality for posted writes.

When the MHR bit is set, the FABRIC_MnHALTREQ signal is asserted. The MHA and MHI fields capture the state of the FABRIC_MnHALTACK and FABRIC_MnIDLE signals at every clock cycle.

NOTE A register is implemented for each master interface supported by the FABRIC

SFAB_FABRIC_MASTER_INTERFACE_REG_n

Bits	Name	Description
15	RESERVED_BIT_15	
14	OWGM	SW : RW Enable optimized write gathering mode. SW should disable for AXI Ports
13	DBW	SW : RW Disable Bufferable writes. Treats Bufferable writes as Non Bufferable writes (AHB only)
12	PRIEN	SW : RW Enable Request Priority Lets the slave way arbiter consider the master request priority AREQPRIORITY[1:0] signal that is driven with each transaction
11	RCOSH	SW : RW Redirect Cacheable-outer-sharable Governs whether or not cacheable accesses that are outer-sharable are redirected to the Scorpion-MP L2 slave port
10	RCISH	SW : RW Redirect Cacheable-inner-sharable Governs whether or not cacheable accesses that are inner-sharable are redirected to the Scorpion-MP L2 slave port
9	RCNSH	SW : RW Redirect Cacheable-non-sharable Governs whether or not cacheable accesses that are non-sharable are redirected to the Scorpion-MP L2 slave port
8	CRE	SW : RW Enable redirection of cachable coherent requests

SFAB_FABRIC_MASTER_INTERFACE_REG_n (cont.)

Bits	Name	Description
7	WGE	SW : RW Write Gathering Enable (AXI only)
6	WPE	SW : RW Write Packing Enable (AHB Only) When enabled, the master port will pack indeterminate INCR burst writes, if disabled, the master port will break indeterminate INCR burst writes into SINGLES. 0x1: Enable 0x0: Disable
5:4	IIIW	SW : RW Bufferable Indeterminate INCR WR packing (AHB only): 0x0: break into INCR4 0x1: break into INCR8 0x3: break into INCR16
3	MID	SW : RW Master Interface Disable. SW diable of Master interface.
2	MI	SW : R Master Idle. Indicates that the Master does not have any pending bus transactions. For AHB busses, this bit is set internally by the FABRIC AHB Master port. For AXI masters, this value is driven by the master that is connected to the port.
1	MHA	SW : R Master halt acknowledge. Only valid for AXI masters. This bit is 0 on AHB master ports.
0	MHR	SW : RW Master halt request. Only valid for AXI masters. Writing this bit has no effect for AHB masters.

0x01303430 SFAB_FABRIC_SLAVE_ARBITRATION_DISABLE_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is RESERVED.

SFAB_FABRIC_SLAVE_ARBITRATION_DISABLE_REG

Bits	Name	Description
15	S15AD	SW : R RESERVED

SFAB_FABRIC_SLAVE_ARBITRATION_DISABLE_REG (cont.)

Bits	Name	Description
14	S14AD	SW : R RESERVED
13	S13AD	SW : R RESERVED
12	S12AD	SW : R RESERVED
11	S11AD	SW : R RESERVED
10	S10AD	SW : R RESERVED
9	S9AD	SW : R RESERVED
8	S8AD	SW : R RESERVED
7	S7AD	SW : R RESERVED
6	S6AD	SW : R RESERVED
5	S5AD	SW : R RESERVED
4	S4AD	SW : R RESERVED
3	S3AD	SW : R RESERVED
2	S2AD	SW : R RESERVED
1	S1AD	SW : R RESERVED
0	S0AD	SW : R RESERVED

0x01303434 SFAB_FABRIC_SLAVE_BYPASS_BUFFER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register enables the bypass buffer functionality in a slave way (if implemented).

SFAB_FABRIC_SLAVE_BYPASS_BUFFER_REG

Bits	Name	Description
15	S15BE	SW : RW Slave 15 Bypass Buffer Enable
14	S14BE	SW : RW Slave 14 Bypass Buffer Enable
13	S13BE	SW : RW Slave 13 Bypass Buffer Enable
12	S12BE	SW : RW Slave 12 Bypass Buffer Enable
11	S11BE	SW : RW Slave 11 Bypass Buffer Enable
10	S10BE	SW : RW Slave 10 Bypass Buffer Enable
9	S9BE	SW : RW Slave 9 Bypass Buffer Enable
8	S8BE	SW : RW Slave 8 Bypass Buffer Enable
7	S7BE	SW : RW Slave 7 Bypass Buffer Enable
6	S6BE	SW : RW Slave 6 Bypass Buffer Enable
5	S5BE	SW : RW Slave 5 Bypass Buffer Enable
4	S4BE	SW : RW Slave 4 Bypass Buffer Enable
3	S3BE	SW : RW Slave 3 Bypass Buffer Enable
2	S2BE	SW : RW Slave 2 Bypass Buffer Enable

SFAB_FABRIC_SLAVE_BYPASS_BUFFER_REG (cont.)

Bits	Name	Description
1	S1BE	SW : RW Slave 1 Bypass Buffer Enable
0	S0BE	SW : RW Slave 0 Bypass Buffer Enable

0x01303438 SFAB_FABRIC_SLAVE_STATUS_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the status of each slave.

- A 1 indicates that the slave is idle.
- A 0 indicates that the slave is busy processing a transfer and/or the FABRIC is has not completed sending transactions to the slave.

SFAB_FABRIC_SLAVE_STATUS_REG

Bits	Name	Description
15	S15S	SW : R Slave 15 Status
14	S14S	SW : R Slave 14 Status
13	S13S	SW : R Slave 13 Status
12	S12S	SW : R Slave 12 Status
11	S11S	SW : R Slave 11 Status
10	S10S	SW : R Slave 10 Status
9	S9S	SW : R Slave 9 Status
8	S8S	SW : R Slave 8 Status
7	S7S	SW : R Slave 7 Status

SFAB_FABRIC_SLAVE_STATUS_REG (cont.)

Bits	Name	Description
6	S6S	SW : R Slave 6 Status
5	S5S	SW : R Slave 5 Status
4	S4S	SW : R Slave 4 Status
3	S3S	SW : R Slave 3 Status
2	S2S	SW : R Slave 2 Status
1	S1S	SW : R Slave 1 Status
0	S0S	SW : R Slave 0 Status

0x01303500 SFAB_FABRIC_TEST_INTERFACE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls:

- the grouping of signals that are driven out on the test bus (FABRIC_TESTBUS[31:0])
- Selection of MISR slave way and channel input

MEN: Selects which MISR output is driven onto the test-bus. For example, setting MEN to 00010 selects the MISR in slave segment 2. The MEN bits are only valid when the testmode (TMODE) is set to 000000 and test-enable is set (TEN)

TMODE: Selects the various test-bus modes

TEN: Test-enable. Must be set for values to be driven onto the test-bus OR for MISR to be enabled.

SFAB_FABRIC_TEST_INTERFACE_REG

Bits	Name	Description
15:14	RESERVED_BITS15_14	

SFAB_FABRIC_TEST_INTERFACE_REG (cont.)

Bits	Name	Description
13:12	MSEL	SW : RW MISR input selection: 0x0: Address channel 0x1: Write channel 0x2: Read channel 0x3: Write response channel
11:7	MEN	SW : RW MISR Enable 0x1: Slave Segment 0 0x2: Slave Segment 1 0x3: Slave Segment 2 0x4: Slave Segment 3 0x5: Slave Segment 4 0x6: Slave Segment 5 0x7: Slave Segment 6 0x8: Slave Segment 7 0x9: Slave Segment 8 0xA: Slave Segment 9 0xB: Slave Segment 10 0xC: Slave Segment 11 0xD: Slave Segment 12 0xE: Slave Segment 13 0xF: Slave Segment 14 0x10: Slave Segment 15

SFAB_FABRIC_TEST_INTERFACE_REG (cont.)

Bits	Name	Description
6:1	TMODE	SW : RW Test Mode: 0x0: Testbus M0 0x1: Testbus M1 0x2: Testbus M2 0x3: Testbus M3 0x4: Testbus M4 0x5: Testbus M5 0x6: Testbus M6 0x7: Testbus M7 0x8: Testbus M8 0x9: Testbus M9 0xA: Testbus M10 0xB: Testbus M11 0xC: Testbus M12 0xD: Testbus M13 0xE: Testbus M14 0xF: Testbus M15 0x10: Testbus M16 0x11: Testbus M17 0x12: Testbus M18 0x13: Testbus M19 0x14: Testbus M20 0x15: Testbus M21 0x16: Testbus M22 0x17: Testbus M23 0x18: Testbus M24 0x19: Testbus M25 0x1A: Testbus M26 0x1B: Testbus M27 0x1C: Testbus M28 0x1D: Testbus M29 0x1E: Testbus M30 0x1F: Testbus M31 0x20: Testbus S0 0x21: Testbus S1 0x22: Testbus S2 0x23: Testbus S3 0x24: Testbus S4 0x25: Testbus S5 0x26: Testbus S6 0x27: Testbus S7 0x28: Testbus S8 0x29: Testbus S9 0x2A: Testbus S10 0x2B: Testbus S11 0x2C: Testbus S12

SFAB_FABRIC_TEST_INTERFACE_REG (cont.)

Bits	Name	Description
		0x2D: Testbus S13 0x2E: Testbus S14 0x2F: Testbus S15 0x30: Reserved_1 0x31: Reserved_2 0x32: Reserved_3 0x33: Reserved_4 0x34: Reserved_5 0x35: Reserved_6 0x36: Reserved_7 0x37: Reserved_8 0x38: Reserved_9 0x39: Reserved_10 0x3A: Reserved_11 0x3B: Reserved_12 0x3C: Reserved_13 0x3D: Reserved_14 0x3E: Reserved_15 0x3F: Reserved_16
0	TEN	SW : RW Test Enable

0x01303504 SFAB_FABRIC_ERROR_STATUS_REG_0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

SFAB_FABRIC_ERROR_STATUS_REG_0

Bits	Name	Description
15:0	MID	SW : R AMID for AXI port HMID for AHB port

0x01303508 SFAB_FABRIC_ERROR_STATUS_REG_1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one. (See FABRIC_CONFIGURATION_REG)

SFAB_FABRIC_ERROR_STATUS_REG_1

Bits	Name	Description
15:8	TID	SW : R Transaction ID Only Applicable for AXI Transfers ZERO for AHB Transfers
7:6	RESERVED_BITS_7_6	Reserved
5:0	MPORT	SW : R Master port that generated the error

0x0130350C SFAB_FABRIC_ERROR_STATUS_REG_2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

SFAB_FABRIC_ERROR_STATUS_REG_2

Bits	Name	Description
15:12	RESERVED_BITS_15_12	Reserved
11	BURST	SW : R Burst transfer
10	OOOWR	SW : R OOO write response Only Applicable for AXI
9	OOORD	SW : R OOO read response Only Applicable for AXI

SFAB_FABRIC_ERROR_STATUS_REG_2 (cont.)

Bits	Name	Description
8:7	LOCK	SW : R Lock Transfer
6:4	SIZE	SW : R Transfer Size
3:0	TYPE	SW : R Transfer Type Only Applicable for AXI

0x01303510 SFAB_FABRIC_ERROR_STATUS_REG_3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

SFAB_FABRIC_ERROR_STATUS_REG_3

Bits	Name	Description
15:8	RESERVED_BITS_15_8	Reserved
7	PROTNS	SW : R APROTNS/HPROTNS
6	PROTIND	SW : R PROTIND
5	AISH	SW : R Inner Shared
4	WRITE	SW : R Write transfer
3:0	LEN	SW : R Transfer Length

0x01303514 SFAB_FABRIC_ERROR_UPPER_ADDR_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address of the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

SFAB_FABRIC_ERROR_UPPER_ADDR_REG

Bits	Name	Description
15:0	EUA	SW : R Bits [31:16] of the address which generated a decode error

0x01303518 SFAB_FABRIC_ERROR_LOWER_ADDR_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address of the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

SFAB_FABRIC_ERROR_LOWER_ADDR_REG

Bits	Name	Description
15:0	ELR	SW : R Bits [15:0] of the address which generated a decode error

0x0130351C SFAB_FABRIC_MISR_SIGNATURE_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG.

SFAB_FABRIC_MISR_SIGNATURE_REG0

Bits	Name	Description
15:0	SIG0	SW : R Bits [15:0] of 64-bit MISR signature

0x01303520 SFAB_FABRIC_MISR_SIGNATURE_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG

SFAB_FABRIC_MISR_SIGNATURE_REG1

Bits	Name	Description
15:0	SIG1	SW : R Bits [31:16] of 64-bit MISR signature

0x01303524 SFAB_FABRIC_MISR_SIGNATURE_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 47:32 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG

SFAB_FABRIC_MISR_SIGNATURE_REG2

Bits	Name	Description
15:0	SIG2	SW : R Bits [47:32] of 64-bit MISR signature

0x01303528 SFAB_FABRIC_MISR_SIGNATURE_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 63:48 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG

SFAB_FABRIC_MISR_SIGNATURE_REG3

Bits	Name	Description
15:0	SIG3	SW : R Bits [63:48] of 64-bit MISR signature

0x0130352C SFAB_FTMR_TESTBUS_MODE_REGISTER

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

For the testbus selected of master or slave port in FABRIC_TEST_INTERFACE_REG, user can program the testbus mode via this register

SFAB_FTMR_TESTBUS_MODE_REGISTER

Bits	Name	Description
15:3	RESERVED_BITS15_3	Reserved
2:0	MODE	0x0: Default Mode 0x1: Address channel attributes at the interface 0x2: Address at the interface 0x3: Misc 0x4: Write data Lower 32 bits at interface 0x5: Write data Upper 32 bits at interface 0x6: Read data Lower 32 bits at interface 0x7: Read data Upper 32 bits at interface

0x01303600+4*n SFAB_FABRIC_MASTER_CLOCK_HALT_REG_n, n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt & change functionality within the FABRIC master ports. To enable the clock halting functionality, the clock halt enable bit (CHTEN) needs to be set. The hysteresis timer value is a 10-bit timer (running on FCLK) value that is set using the CHTMR bits. The clock change and MODE bits are used to change the interface between sync/async/isosync modes.

NOTE A register is implemented for each master interface supported by the FABRIC .

SFAB_FABRIC_MASTER_CLOCK_HALT_REG_n

Bits	Name	Description
15	CHTEN	SW : RW Clock halt enable. Enables clock halt functionality for this port.
14	CCDONE	SW : RW Clock mode change completed/done
13	CCACK	SW : R Clock mode change acknowledge
12	CCREQ	SW : RW Clock mode change request
11:10	MODE	SW : RW Master clock interface mode 0x0: ASYNC 0x1: SYNC 0x2: ISOSYNC port clk slower. 0x3: ISOSYNC port clk faster.
9:0	CHTMR	SW : RW Master clock halt timer: # clock cycles of inactivity that should pass before clock is halted

0x01303800+4*n SFAB_FABRIC_SLAVE_CLOCK_HALT_REG_n, n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt & change functionality within the FABRIC slave ways. To enable the clock halting functionality, the clock halt enable bit (CHTEN) needs to be set. The hysteresis timer value is a 10-bit timer (running on FCLK) value that is set using the CHTMR bits. The clock change and MODE bits are used to change the interface between sync/async/isosync modes.

NOTE A register is implemented for each slave interface supported by the FABRIC .

SFAB_FABRIC_SLAVE_CLOCK_HALT_REG_n

Bits	Name	Description
15	CHTEN	SW : RW Clock halt enable. Enables clock halt functionality for this port.

SFAB_FABRIC_SLAVE_CLOCK_HALT_REG_n (cont.)

Bits	Name	Description
14	CCDONE	SW : RW Cock mode change completed/done
13	CCACK	SW : RW Clock mode change acknowledge
12	CCREQ	SW : RW Clock mode change request
11:10	MODE	SW : RW Slave clock interface mode 0x0: ASYNC 0x1: SYNC 0x2: ISOSYNC port clk slower. 0x3: ISOSYNC port clk faster.
9:0	CHTMR	SW : RW Slave clock halt timer: clock cycles of inactivity that should pass before clock is halted

0x01303880 SFAB_FABRIC_SLAVE_ARBITER_CLOCK_HALT_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt functionality within the FABRIC slave ways arbiter.

SFAB_FABRIC_SLAVE_ARBITER_CLOCK_HALT_REG

Bits	Name	Description
15	S15CHTEN	SW : RW S15 Arbiter Clock halt enable.
14	S14CHTEN	SW : RW S14 Arbiter Clock halt enable.
13	S13CHTEN	SW : RW S13 Arbiter Clock halt enable.
12	S12CHTEN	SW : RW S12 Arbiter Clock halt enable.

SFAB_FABRIC_SLAVE_ARBITER_CLOCK_HALT_REG (cont.)

Bits	Name	Description
11	S11CHTEN	SW : RW S11 Arbiter Clock halt enable.
10	S10CHTEN	SW : RW S10 Arbiter Clock halt enable.
9	S9CHTEN	SW : RW S9 Arbiter Clock halt enable.
8	S8CHTEN	SW : RW S8 Arbiter Clock halt enable.
7	S7CHTEN	SW : RW S7 Arbiter Clock halt enable.
6	S6CHTEN	SW : RW S6 Arbiter Clock halt enable.
5	S5CHTEN	SW : RW S5 Arbiter Clock halt enable.
4	S4CHTEN	SW : RW S4 Arbiter Clock halt enable.
3	S3CHTEN	SW : RW S3 Arbiter Clock halt enable.
2	S2CHTEN	SW : RW S2 Arbiter Clock halt enable.
1	S1CHTEN	SW : RW S1 Arbiter Clock halt enable.
0	S0CHTEN	SW : RW S0 Arbiter Clock halt enable.

0x01303884+4*n SFAB_FABRIC_SLAVE_CLOCK_ON_CFG_REG_n, n=[0..14]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to set wake-up timer values durin g HW clock gating functionality for the Fabric slave ways arbiter and AHB/AXI slaves connected to Fabric.

SFAB_FABRIC_SLAVE_CLOCK_ON_CFG_REG_n

Bits	Name	Description
15:4	RESERVED_BITS_15_4	Reserved

SFAB_FABRIC_SLAVE_CLOCK_ON_CFG_REG_n (cont.)

Bits	Name	Description
3:0	COD	SW : RW Slave Way Clock On Delay

0x013038F8 SFAB_FABRIC_MONITOR_ENABLE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the trigger selection and enabling of event and cycle counters.

NOTE When PTRIG is set to use any of the external trigger signals, the external triggers incur a 2 cycle delay from the positive edge assertion of the signal to when the actual counters are enabled in the performance monitor. This allows synchronization of the external signals into the FABRIC clock domain.

SFAB_FABRIC_MONITOR_ENABLE_REG

Bits	Name	Description
15:13	PTRIG	SW : RW 0x5: Manual Enable/ Manual Disable 0x4: Int Trig/Ext Trig 0x3: Ext Trig 0x2: Ext Trig/CC expire 0x1: Int Trig/CC expire 0x0: Manual enable/CC expire (No trigger)
12	ECC	SW : RW Enable cycle counter
11:8	RESERVED_BITS_11_8	Reserved
7	EEC7	SW : RW Enable event counter 7
6	EEC6	SW : RW Enable event counter 6
5	EEC5	SW : RW Enable event counter 5
4	EEC4	SW : RW Enable event counter 4
3	EEC3	SW : RW Enable event counter 3

SFAB_FABRIC_MONITOR_ENABLE_REG (cont.)

Bits	Name	Description
2	EEC2	SW : RW Enable event counter 2
1	EEC1	SW : RW Enable event counter 1
0	EEC0	SW : RW Enable event counter 0

0x013038FC SFAB_FABRIC_MONITOR_RESET_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the resets for event and cycle counters.

SFAB_FABRIC_MONITOR_RESET_REG

Bits	Name	Description
15:8	RESERVED_BITS_15_8	Reserved
7	REC7	SW : RW Reset event counter 7 (automatically resets the cycle-counter as well)
6	REC6	SW : RW Reset event counter 6 (automatically resets the cycle-counter as well)
5	REC5	SW : RW Reset event counter 5 (automatically resets the cycle-counter as well)
4	REC4	SW : RW Reset event counter 4 (automatically resets the cycle-counter as well)
3	REC3	SW : RW Reset event counter 3 (automatically resets the cycle-counter as well)
2	REC2	SW : RW Reset event counter 2 (automatically resets the cycle-counter as well)
1	REC1	SW : RW Reset event counter 1 (automatically resets the cycle-counter as well)

SFAB_FABRIC_MONITOR_RESET_REG (cont.)

Bits	Name	Description
0	REC0	SW : RW Reset event counter 0 (automatically resets the cycle-counter as well)

0x01303900 SFAB_FABRIC_MONITOR_TENURE_ENABLE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the trigger selection and enabling of tenure counters.

NOTE When PTRIG is set to use any of the external trigger signals, the external triggers incur a 2 cycle delay from the positive edge assertion of the signal to when the actual counters are enabled in the performance monitor. This allows synchronization of the external signals into the FABRIC clock domain.

SFAB_FABRIC_MONITOR_TENURE_ENABLE_REG

Bits	Name	Description
15:5	RESERVED_BITS_15_5	Reserved
4	ETTF	SW : RW Enable tenure table fix This bit, when set, enables a the following feature: The tenure table for each tenure counter will track atleast 16 tenures properly without overflowing
3	ETC3	SW : RW Enable tenure counter 3
2	ETC2	SW : RW Enable tenure counter 2
1	ETC1	SW : RW Enable tenure counter 1
0	ETC0	SW : RW Enable tenure counter 0

0x01303904 SFAB_FABRIC_MONITOR_TENURE_RESET_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the resets for tenure counters and cycle counters.

SFAB_FABRIC_MONITOR_TENURE_RESET_REG

Bits	Name	Description
15:4	RESERVED_BITS_15_4	Reserved
3	RTC3	SW : RW Reset tenure counter 3 (automatically resets the cycle-counter as well)
2	RTC2	SW : RW Reset tenure counter 2 (automatically resets the cycle-counter as well)
1	RTC1	SW : RW Reset tenure counter 1 (automatically resets the cycle-counter as well)
0	RTC0	SW : RW Reset tenure counter 0 (automatically resets the cycle-counter as well)

0x01303908 SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 0.

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG0

Bits	Name	Description
15:13	E0ES	SW : RW Event counter 0 event selection 0x0: Read burst 0 (Master/slave) 0x1: Write burst 0 (Master/slave) 0x2: Address transfer count 0 (Master/slave) 0x3: Read transfer count 0 (Master/slave) 0x4: Write transfer count 0 (Master/slave) 0x5: Write (bufferable burst 0 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E0MIDFEN	SW : RW Event counter 0 MID Filtering enable 0x0: Disabled 0x1: Enabled

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
10	E0INDFEN	SW : RW Event counter 0 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E0IND	SW : RW Event counter 0 Instruction/Data selection 0x0: Data 0x1: Instruction
8:4	E0MPS	SW : RW Event counter 0 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
3:0	E0SWS	SW : RW Event counter 0 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0130390C SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 0.

SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG0

Bits	Name	Description
15:0	E0MID	SW : RW Event counter 0 MID selection (If MID filtering enabled)

0x01303910 SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 1.

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG1

Bits	Name	Description
15:13	E1ES	SW : RW Event counter 1event selection 0x0: Read burst 1 (Master/slave) 0x1: Write burst 1 (Master/slave) 0x2: Address transfer count 1 (Master/slave) 0x3: Read transfer count 1 (Master/slave) 0x4: Write transfer count 1 (Master/slave) 0x5: Write (bufferable burst 1 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E1MIDFEN	SW : RW Event counter 1 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E1INDFEN	SW : RW Event counter 1Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E1IND	SW : RW Event counter 1Instruction/Data selection 0x0: Data 0x1: Instruction

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
8:4	E1MPS	SW : RW Event counter 1Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
3:0	E1SWS	SW : RW Event counter 1Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01303914 SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 1.

SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG1

Bits	Name	Description
15:0	E1MID	SW : RW Event counter 1MID selection (If MID filtering enabled)

0x01303918 SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 2.

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG2

Bits	Name	Description
15:13	E2ES	SW : RW Event counter 2event selection 0x0: Read burst 2 (Master/slave) 0x1: Write burst 2 (Master/slave) 0x2: Address transfer count 2 (Master/slave) 0x3: Read transfer count 2 (Master/slave) 0x4: Write transfer count 2 (Master/slave) 0x5: Write (bufferable burst 2 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E2MIDFEN	SW : RW Event counter 2MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E2INDFEN	SW : RW Event counter 2Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E2IND	SW : RW Event counter 2Instruction/Data selection 0x0: Data 0x1: Instruction

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
8:4	E2MPS	SW : RW Event counter 2Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
3:0	E2SWS	SW : RW Event counter 2Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0130391C SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 2.

SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG2

Bits	Name	Description
15:0	E2MID	SW : RW Event counter 2 MID selection (If MID filtering enabled)

0x01303920 SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 3.

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG3

Bits	Name	Description
15:13	E3ES	SW : RW Event counter 3event selection 0x0: Read burst 3 (Master/slave) 0x1: Write burst 3 (Master/slave) 0x2: Address transfer count 3 (Master/slave) 0x3: Read transfer count 3 (Master/slave) 0x4: Write transfer count 3 (Master/slave) 0x5: Write (bufferable burst 3 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E3MIDFEN	SW : RW Event counter 3MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E3INDFEN	SW : RW Event counter 3Instruction/Data Filtering enable 0x0: Disabled 0x1: Enable
9	E3IND	SW : RW Event counter 3Instruction/Data selection 0x0: Data 0x1: Instruction

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
8:4	E3MPS	SW : RW Event counter 3Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
3:0	E3SWS	SW : RW Event counter 3 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01303924 SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 3.

SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG3

Bits	Name	Description
15:0	E3MID	SW : RW Event counter 3 MID selection (If MID filtering enabled)

0x01303928 SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 4.

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG4

Bits	Name	Description
15:13	E4ES	SW : RW Event counter 4event selection 0x0: Read burst 4 (Master/slave) 0x1: Write burst 4 (Master/slave) 0x2: Address transfer count 4 (Master/slave) 0x3: Read transfer count 4 (Master/slave) 0x4: Write transfer count 4 (Master/slave) 0x5: Write (bufferable burst 4AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	SEL_SPDM_OUT0	SW : RW 0x0: Send total tenure overflow infor (for tenure counter 0 to SPDM) 0x1: Send individual counter overflow info (for tenure counter 0 to SPDM)
11	E4MIDFEN	SW : RW Event counter 4 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E4INDFEN	SW : RW Event counter 4 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E4IND	SW : RW Event counter 4 Instruction/Data selection 0x0: Data 0x1: Instruction

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG4 (cont.)

Bits	Name	Description
8:4	E4MPS	SW : RW Event counter 4 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG4 (cont.)

Bits	Name	Description
3:0	E4SWS	SW : RW Event counter 4 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0130392C SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 4.

SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG4

Bits	Name	Description
15:0	E4MID	SW : RW Event counter 4 MID selection (If MID filtering enabled)

0x01303930 SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 5.

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG5

Bits	Name	Description
15:13	E5ES	SW : RW Event counter 5 event selection 0x0: Read burst 5 (Master/slave) 0x1: Write burst 5 (Master/slave) 0x2: Address transfer count 5 (Master/slave) 0x3: Read transfer count 5 (Master/slave) 0x4: Write transfer count 5 (Master/slave) 0x5: Write (bufferable burst 5 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	SEL_SPDM_OUT1	SW : RW 0x0: Send total tenure overflow infor (for tenure counter 1 to SPDM) 0x1: Send individual counter overflow info (for tenure counter 1 to SPDM)
11	E5MIDFEN	SW : RW Event counter 5 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E5INDFEN	SW : RW Event counter 5 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E5IND	SW : RW Event counter 5 Instruction/Data selection 0x0: Data 0x1: Instruction

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG5 (cont.)

Bits	Name	Description
8:4	E5MPS	SW : RW Event counter 5 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG5 (cont.)

Bits	Name	Description
3:0	E5SWS	SW : RW Event counter 5 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01303934 SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 5.

SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG5

Bits	Name	Description
15:0	E5MID	SW : RW Event counter 5 MID selection (If MID filtering enabled)

0x01303938 SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 6.

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG6

Bits	Name	Description
15:13	E6ES	SW : RW Event counter 6 event selection 0x0: Read burst 6 (Master/slave) 0x1: Write burst 6 (Master/slave) 0x2: Address transfer count 6 (Master/slave) 0x3: Read transfer count 6 (Master/slave) 0x4: Write transfer count 6 (Master/slave) 0x5: Write (bufferable burst 6 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	SEL_SPDM_OUT2	SW : RW 0x0: Send total tenure overflow infor (for tenure counter 2 to SPDM) 0x1: Send individual counter overflow info (for tenure counter 2 to SPDM)
11	E6MIDFEN	SW : RW Event counter 6 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E6INDFEN	SW : RW Event counter 6 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E6IND	SW : RW Event counter 6 Instruction/Data selection 0x0: Data 0x1: Instruction

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG6 (cont.)

Bits	Name	Description
8:4	E6MPS	SW : RW Event counter 6 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG6 (cont.)

Bits	Name	Description
3:0	E6SWS	SW : RW Event counter 6 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0130393C SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 6.

SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG6

Bits	Name	Description
15:0	E6MID	SW : RW Event counter 6 MID selection (If MID filtering enabled)

0x01303940 SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 7.

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG7

Bits	Name	Description
15:13	E7ES	SW : RW Event counter 7 event selection 0x0: Read burst 7 (Master/slave) 0x1: Write burst 7 (Master/slave) 0x2: Address transfer count 7 (Master/slave) 0x3: Read transfer count 7 (Master/slave) 0x4: Write transfer count 7 (Master/slave) 0x5: Write (bufferable burst 7 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	SEL_SPDM_OUT3	SW : RW 0x0: Send total tenure overflow infor (for tenure counter 3 to SPDM) 0x1: Send individual counter overflow info (for tenure counter 3 to SPDM)
11	E7MIDFEN	SW : RW Event counter 7 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E7INDFEN	SW : RW Event counter 7 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E7IND	SW : RW Event counter 7 Instruction/Data selection 0x0: Data 0x1: Instruction

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG7 (cont.)

Bits	Name	Description
8:4	E7MPS	SW : RW Event counter 7 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

SFAB_FABRIC_MONITOR_SELECTION_LOWER_REG7 (cont.)

Bits	Name	Description
3:0	E7SWS	SW : RW Event counter 7 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01303944 SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 7.

SFAB_FABRIC_MONITOR_SELECTION_UPPER_REG7

Bits	Name	Description
15:0	E7MID	SW : RW Event counter 7 MID selection (If MID filtering enabled)

0x01303948 SFAB_FABRIC_MONITOR_PICK_PORTS_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the main port and other port selection for the 8 event counters.

SFAB_FABRIC_MONITOR_PICK_PORTS_REG

Bits	Name	Description
15:14	E7PP	SW : RW Event counter 7 port combination selection 0x0: Master port selected by E7MPS, filtering based on slave port disabled 0x1: Master port selected by E7MPS, filtering based on slave way selected by E7SWS 0x2: Slave way selected by E7SWS, filtering based on master port disabled 0x3: Slave way selected by E7SWS, filtering based on master port selected by E7MPS
13:12	E6PP	SW : RW Event counter 6 port combination selection 0x0: Master port selected by E6MPS, filtering based on slave port disabled 0x1: Master port selected by E6MPS, filtering based on slave way selected by E6SWS 0x2: Slave way selected by E6SWS, filtering based on master port disabled 0x3: Slave way selected by E6SWS, filtering based on master port selected by E6MPS
11:10	E5PP	SW : RW Event counter 5 port combination selection 0x0: Master port selected by E5MPS, filtering based on slave port disabled 0x1: Master port selected by E5MPS, filtering based on slave way selected by E5SWS 0x2: Slave way selected by E5SWS, filtering based on master port disabled 0x3: Slave way selected by E5SWS, filtering based on master port selected by E5MPS
9:8	E4PP	SW : RW Event counter 4 port combination selection 0x0: Master port selected by E4MPS, filtering based on slave port disabled 0x1: Master port selected by E4MPS, filtering based on slave way selected by E4SWS 0x2: Slave way selected by E4SWS, filtering based on master port disabled 0x3: Slave way selected by E4SWS, filtering based on master port selected by E4MPS

SFAB_FABRIC_MONITOR_PICK_PORTS_REG (cont.)

Bits	Name	Description
7:6	E3PP	SW : RW Event counter 3 port combination selection 0x0: Master port selected by E3MPS, filtering based on slave port disabled 0x1: Master port selected by E3MPS, filtering based on slave way selected by E3SWS 0x2: Slave way selected by E3SWS, filtering based on master port disabled 0x3: Slave way selected by E3SWS, filtering based on master port selected by E3MPS
5:4	E2PP	SW : RW Event counter 2 port combination selection 0x0: Master port selected by E2MPS, filtering based on slave port disabled 0x1: Master port selected by E2MPS, filtering based on slave way selected by E2SWS 0x2: Slave way selected by E2SWS, filtering based on master port disabled 0x3: Slave way selected by E2SWS, filtering based on master port selected by E2MPS
3:2	E1PP	SW : RW Event counter 1 port combination selection 0x0: Master port selected by E1MPS, filtering based on slave port disabled 0x1: Master port selected by E1MPS, filtering based on slave way selected by E1SWS 0x2: Slave way selected by E1SWS, filtering based on master port disabled 0x3: Slave way selected by E1SWS, filtering based on master port selected by E1MPS
1:0	E0PP	SW : RW Event counter 0 port combination selection 0x0: Master port selected by E0MPS, filtering based on slave port disabled 0x1: Master port selected by E0MPS, filtering based on slave way selected by E0SWS 0x2: Slave way selected by E0SWS, filtering based on master port disabled 0x3: Slave way selected by E0SWS, filtering based on master port selected by E0MPS

0x01303950 SFAB_FABRIC_MONITOR_CYCLE_COUNT_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the performance monitor cycle counter.

SFAB_FABRIC_MONITOR_CYCLE_COUNT_UPPER_REG

Bits	Name	Description
15:0	UCC	SW : RW MSB cycle count value The cycle count value is decremented once per FABRIC clock. The counter stops decrementing once the CC value equals 32:h0.

0x01303954 SFAB_FABRIC_MONITOR_CYCLE_COUNT_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the performance monitor cycle counter. If SW requires that the values when read do not change, when it reads this register, the value for all 32 bits of the cycle counter is stored. This allows for SW to read the lower reg and have the value match the exact cycle in which the upper reg was read.

SFAB_FABRIC_MONITOR_CYCLE_COUNT_LOWER_REG

Bits	Name	Description
15:0	LCC	SW : RW LSB cycle count value The cycle count value is decremented once per FABRIC clock. The counter stops decrementing once the CC value equals 32:h0.

0x01303958 SFAB_FABRIC_MONITOR_EVENT_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 0. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_LOWER_REG0

Bits	Name	Description
15:0	ECLT0	SW : RW Total # events (lower 16-bit value)

0x0130395C SFAB_FABRIC_MONITOR_EVENT_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 0. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_UPPER_REG0

Bits	Name	Description
15:0	ECUT0	SW : RW Total # events (upper 16-bit value)

0x01303960 SFAB_FABRIC_MONITOR_EVENT_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 1. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_LOWER_REG1

Bits	Name	Description
15:0	ECLT1	SW : RW Total # events (lower 16-bit value)

0x01303964 SFAB_FABRIC_MONITOR_EVENT_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 1. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_UPPER_REG1

Bits	Name	Description
15:0	ECUT1	SW : RW Total # events (upper 16-bit value)

0x01303968 SFAB_FABRIC_MONITOR_EVENT_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 2. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_LOWER_REG2

Bits	Name	Description
15:0	ECLT2	SW : RW Total # events (lower 16-bit value)

0x0130396C SFAB_FABRIC_MONITOR_EVENT_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 2. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_UPPER_REG2

Bits	Name	Description
15:0	ECUT2	SW : RW Total # events (upper 16-bit value)

0x01303970 SFAB_FABRIC_MONITOR_EVENT_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 3. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_LOWER_REG3

Bits	Name	Description
15:0	ECLT3	SW : RW Total # events (lower 16-bit value)

0x01303974 SFAB_FABRIC_MONITOR_EVENT_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 3. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_UPPER_REG3

Bits	Name	Description
15:0	ECUT3	SW : RW Total # events (upper 16-bit value)

0x01303978 SFAB_FABRIC_MONITOR_EVENT_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 4. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_LOWER_REG4

Bits	Name	Description
15:0	ECLT4	SW : RW Total # events (lower 16-bit value)

0x0130397C SFAB_FABRIC_MONITOR_EVENT_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 4. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_UPPER_REG4

Bits	Name	Description
15:0	ECUT4	SW : RW Total # events (upper 16-bit value)

0x01303980 SFAB_FABRIC_MONITOR_EVENT_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 5. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_LOWER_REG5

Bits	Name	Description
15:0	ECLT5	SW : RW Total # events (lower 16-bit value)

0x01303984 SFAB_FABRIC_MONITOR_EVENT_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 5. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_UPPER_REG5

Bits	Name	Description
15:0	ECUT5	SW : RW Total # events (upper 16-bit value)

0x01303988 SFAB_FABRIC_MONITOR_EVENT_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 6. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_LOWER_REG6

Bits	Name	Description
15:0	ECLT6	SW : RW Total # events (lower 16-bit value)

0x0130398C SFAB_FABRIC_MONITOR_EVENT_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 6. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_UPPER_REG6

Bits	Name	Description
15:0	ECUT6	SW : RW Total # events (upper 16-bit value)

0x01303990 SFAB_FABRIC_MONITOR_EVENT_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 7. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_LOWER_REG7

Bits	Name	Description
15:0	ECLT7	SW : RW Total # events (lower 16-bit value)

0x01303994 SFAB_FABRIC_MONITOR_EVENT_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 7. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_UPPER_REG7

Bits	Name	Description
15:0	ECUT7	SW : RW Total # events (upper 16-bit value)

0x013039A4 SFAB_FABRIC_TRIGGER_CONFIGURATION_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register configures the interface in which the trigger comparison is done on the address channel.

TAMS: Selects one of the 32 interfaces from which the address channel transfer qualifiers are used to enable trigger matching.

SFAB_FABRIC_TRIGGER_CONFIGURATION_REG

Bits	Name	Description
15:7	RESERVED_BITS15_6	

SFAB_FABRIC_TRIGGER_CONFIGURATION_REG (cont.)

Bits	Name	Description
6	TRGEN	SW : RW Trigger enable 1'b0 -disabled 0x1: enabled

SFAB_FABRIC_TRIGGER_CONFIGURATION_REG (cont.)

Bits	Name	Description
5:0	TAMS	SW : RW Trigger based on address channel on M/S Port #: 0x0: Master Port 0 0x1: Master Port 1 0x2: Master Port 2 0x3: Master Port 3 0x4: Master Port 4 0x5: Master Port 5 0x6: Master Port 6 0x7: Master Port 7 0x8: Master Port 8 0x9: Master Port 9 0xA: Master Port 10 0xB: Master Port 11 0xC: Master Port 12 0xD: Master Port 13 0xE: Master Port 14 0xF: Master Port 15 0x10: Master Port 16 0x11: Master Port 17 0x12: Master Port 18 0x13: Master Port 19 0x14: Master Port 20 0x15: Master Port 21 0x16: Master Port 22 0x17: Master Port 23 0x18: Master Port 24 0x19: Master Port 25 0x1A: Master Port 26 0x1B: Master Port 27 0x1C: Master Port 28 0x1D: Master Port 29 0x1E: Master Port 30 0x1F: Master Port 31 0x20: Slave Port 0 0x21: Slave Port 1 0x22: Slave Port 2 0x23: Slave Port 3 0x24: Slave Port 4 0x25: Slave Port 5 0x26: Slave Port 6 0x27: Slave Port 7 0x28: Slave Port 8 0x29: Slave Port 9 0x2A: Slave Port 10 0x2B: Slave Port 11

SFAB_FABRIC_TRIGGER_CONFIGURATION_REG (cont.)

Bits	Name	Description
5:0	TAMS (CONT'D)	0x2C: Slave Port 12 0x2D: Slave Port 13 0x2E: Slave Port 14 0x2F: Slave Port 15

0x013039AC SFAB_FABRIC_TRIGGER_REG_0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the upper address which is used as comparison for the trigger feature of the on-chip trace or performance monitor function. TUADDR[15:0] will be compared against Address[31:16].

SFAB_FABRIC_TRIGGER_REG_0

Bits	Name	Description
15:0	TUADDR	SW : RW Address bits[31:16]

0x013039B0 SFAB_FABRIC_TRIGGER_REG_1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the lower address which is used as comparison for the trigger feature of the performance monitor function. TLADDR[15:0] will be compared against Address[15:0].

SFAB_FABRIC_TRIGGER_REG_1

Bits	Name	Description
15:0	TLADDR	SW : RW Address bits[15:0]

0x013039B4 SFAB_FABRIC_TRIGGER_REG_2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the lower address which is used as comparison for the trigger feature of the performance monitor function..

SFAB_FABRIC_TRIGGER_REG_2

Bits	Name	Description
15:0	AMID	SW : RW AMID / HMID

0x013039B8 SFAB_FABRIC_TRIGGER_REG_3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the address channel transfer qualifiers which are used as comparison for the trigger feature of the performance monitor function.

SFAB_FABRIC_TRIGGER_REG_3

Bits	Name	Description
15:12	RESERVED_BITS15_12	
11	AOOOWR	SW : RW Out-of-order write
10	AOOORD	SW : RW Out-of-order read
9:3	ATID	SW : RW Address TID (If ATID is less than 7 bits, the upper bits must be set to 0)
2	AFULL	SW : RW Full Transfer
1	RESERVED_BIT1	
0	APROTNS	SW : RW Protection level

0x013039BC SFAB_FABRIC_TRIGGER_REG_4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the address channel transfer qualifiers which are used as comparison for the trigger feature of the performance monitor function.

SFAB_FABRIC_TRIGGER_REG_4

Bits	Name	Description
15:12	ATYPE	SW : RW Memory type attributes
11:10	ALOCK	SW : RW Lock type
9	RESERVED_BITS9	
8	ABURST	SW : RW Burst type
7:5	ASIZE	Burst size
4:1	ALEN	Burst length
0	AWRITE	Burst direction

0x013039C0 SFAB_FABRIC_TRIGGER_MASK_REG_0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR0.

SFAB_FABRIC_TRIGGER_MASK_REG_0

Bits	Name	Description
15:0	FTTR0_MASK	SW : RW Bit mask field for FTTR0 Enable: 1 Disable: 0

0x013039C4 SFAB_FABRIC_TRIGGER_MASK_REG_1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR1.

SFAB_FABRIC_TRIGGER_MASK_REG_1

Bits	Name	Description
15:0	FTTR1_MASK	SW : RW Bit mask field for FTTR1 Enable: 1 Disable: 0

0x013039C8 SFAB_FABRIC_TRIGGER_MASK_REG_2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR2.

SFAB_FABRIC_TRIGGER_MASK_REG_2

Bits	Name	Description
15:0	FTTR2_MASK	SW : RW Bit mask field for FTTR2 Enable: 1 Disable: 0

0x013039CC SFAB_FABRIC_TRIGGER_MASK_REG_3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR3.

SFAB_FABRIC_TRIGGER_MASK_REG_3

Bits	Name	Description
15:0	FTTR3_MASK	SW : RW Bit mask field for FTTR3 Enable: 1 Disable: 0

0x013039D0 SFAB_FABRIC_TRIGGER_MASK_REG_4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR4.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR4.

SFAB_FABRIC_TRIGGER_MASK_REG_4

Bits	Name	Description
15:0	FTTR4_MASK	SW : RW Bit mask field for FTTR4 Enable: 1 Disable: 0

0x013039D4 SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter0.

SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG0

Bits	Name	Description
15:0	E0AL	SW : RW LSB address value Event counter 0 address selection (if address range filtering enabled)

0x013039D8 SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter0.

SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG0

Bits	Name	Description
15:0	E0AU	SW : RW MSB address value Event counter 0 address selection (if address range filtering enabled)

0x013039DC SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter1.

SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG1

Bits	Name	Description
15:0	E1AL	SW : RW LSB address value Event counter 1address selection (if address range filtering enabled)

0x013039E0 SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter1.

SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG1

Bits	Name	Description
15:0	E1AU	SW : RW MSB address value Event counter 1address selection (if address range filtering enabled)

0x013039E4 SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter2

SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG2

Bits	Name	Description
15:0	E2AL	SW : RW LSB address value Event counter 2 address selection (if address range filtering enabled)

0x013039E8 SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter2.

SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG2

Bits	Name	Description
15:0	E2AU	SW : RW MSB address value Event counter 2 address selection (if address range filtering enabled)

0x013039EC SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter3

SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG3

Bits	Name	Description
15:0	E3AL	SW : RW LSB address value Event counter 3 address selection (if address range filtering enabled)

0x013039F0 SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter3.

SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG3

Bits	Name	Description
15:0	E3AU	SW : RW MSB address value Event counter 3 address selection (if address range filtering enabled)

0x013039F4 SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter4.

SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG4

Bits	Name	Description
15:0	E4AL	SW : RW LSB address value Event counter 4 address selection (if address range filtering enabled)

0x013039F8 SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter4.

SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG4

Bits	Name	Description
15:0	E4AU	SW : RW MSB address value Event counter 4address selection (if address range filtering enabled)

0x013039FC SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter5.

SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG5

Bits	Name	Description
15:0	E5AL	SW : RW LSB address value Event counter 5 address selection (if address range filtering enabled)

0x01303A00 SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter4.

SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG5

Bits	Name	Description
15:0	E5AU	SW : RW MSB address value Event counter 5 address selection (if address range filtering enabled)

0x01303A04 SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter 6.

SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG6

Bits	Name	Description
15:0	E6AL	SW : RW LSB address value Event counter 6 address selection (if address range filtering enabled)

0x01303A08 SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 6.

SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG6

Bits	Name	Description
15:0	E6AU	SW : RW MSB address value Event counter 6 address selection (if address range filtering enabled)

0x01303A0C SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter 7.

SFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG7

Bits	Name	Description
15:0	E7AL	SW : RW LSB address value Event counter 7 address selection (if address range filtering enabled)

0x01303A10 SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 7.

SFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG7

Bits	Name	Description
15:0	E7AU	SW : RW MSB address value Event counter 7 address selection (if address range filtering enabled)

0x01303A14 SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR0.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG0

Bits	Name	Description
15:0	E0AML	SW : RW LSB address value Event counter 0 address mask

0x01303A18 SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR0.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG0

Bits	Name	Description
15:0	E0AMU	SW : RW MSB address value Event counter 0 address mask

0x01303A1C SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR1.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG1

Bits	Name	Description
15:0	E1AML	SW : RW LSB address value Event counter 1 address mask

0x01303A20 SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR1.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG1

Bits	Name	Description
15:0	E1AMU	SW : RW MSB address value Event counter address mask

0x01303A24 SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR2.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG2

Bits	Name	Description
15:0	E2AML	SW : RW LSB address value Event counter 2 address mask

0x01303A28 SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR2.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG2

Bits	Name	Description
15:0	E2AMU	SW : RW MSB address value Event counter 2 address mask

0x01303A2C SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR3.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG3

Bits	Name	Description
15:0	E3AML	SW : RW LSB address value Event counter 3 address mask

0x01303A30 SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR3.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG3

Bits	Name	Description
15:0	E3AMU	SW : RW MSB address value Event counter 3 address mask

0x01303A34 SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 4.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR4.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG4

Bits	Name	Description
15:0	E4AML	SW : RW LSB address value Event counter 4 address mask

0x01303A38 SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 4.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR4.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG4

Bits	Name	Description
15:0	E4AMU	SW : RW MSB address value Event counter 4 address mask

0x01303A3C SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 5.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR5.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG5

Bits	Name	Description
15:0	E5AML	SW : RW LSB address value Event counter 5 address mask

0x01303A40 SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 5.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR5.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG5

Bits	Name	Description
15:0	E5AMU	SW : RW MSB address value Event counter 5 address mask

0x01303A44 SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 6.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR6.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG6

Bits	Name	Description
15:0	E6AML	SW : RW LSB address value Event counter 6 address mask

0x01303A48 SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 6.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR6.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG6

Bits	Name	Description
15:0	E6AMU	SW : RW MSB address value Event counter 6 address mask

0x01303A4C SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 7.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR7.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG7

Bits	Name	Description
15:0	E7AML	SW : RW LSB address value Event counter 7 address mask

0x01303A50 SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 7.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR7.

SFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG7

Bits	Name	Description
15:0	E7AMU	SW : RW MSB address value Event counter 7 address mask

0x01303A70 SFAB_FABRIC_MONITOR_MID_MASK_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 0

SFAB_FABRIC_MONITOR_MID_MASK_REG0

Bits	Name	Description
15:0	E0MM	SW : RW MID Mask value for event counter 0

0x01303A74 SFAB_FABRIC_MONITOR_MID_MASK_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 1

SFAB_FABRIC_MONITOR_MID_MASK_REG1

Bits	Name	Description
15:0	E1MM	SW : RW MID Mask value for event counter 1

0x01303A78 SFAB_FABRIC_MONITOR_MID_MASK_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 2

SFAB_FABRIC_MONITOR_MID_MASK_REG2

Bits	Name	Description
15:0	E2MM	SW : RW MID Mask value for event counter 2

0x01303A7C SFAB_FABRIC_MONITOR_MID_MASK_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 3

SFAB_FABRIC_MONITOR_MID_MASK_REG3

Bits	Name	Description
15:0	E3MM	SW : RW MID Mask value for event counter 3

0x01303A80 SFAB_FABRIC_MONITOR_MID_MASK_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 4

SFAB_FABRIC_MONITOR_MID_MASK_REG4

Bits	Name	Description
15:0	E4MM	SW : RW MID Mask value for event counter 4

0x01303A84 SFAB_FABRIC_MONITOR_MID_MASK_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 15

SFAB_FABRIC_MONITOR_MID_MASK_REG5

Bits	Name	Description
15:0	E5MM	SW : RW MID Mask value for event counter 5

0x01303A88 SFAB_FABRIC_MONITOR_MID_MASK_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 6

SFAB_FABRIC_MONITOR_MID_MASK_REG6

Bits	Name	Description
15:0	E6MM	SW : RW MID Mask value for event counter 6

0x01303A8C SFAB_FABRIC_MONITOR_MID_MASK_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 7

SFAB_FABRIC_MONITOR_MID_MASK_REG7

Bits	Name	Description
15:0	E7MM	SW : RW MID Mask value for event counter 7

0x01303AA0 SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG0

Bits	Name	Description
15:0	EBTL0	SW : RW Total # beats (lower 16-bit value)

0x01303AA4 SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG0

Bits	Name	Description
15:0	EBTM0	SW : RW Total # beats (middle 16-bit value)

0x01303AA8 SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG0

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU0	SW : RW Total # beats (upper 4-bit value)

0x01303AAC SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG1

Bits	Name	Description
15:0	EBTL1	SW : RW Total # beats (lower 16-bit value)

0x01303AB0 SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG1

Bits	Name	Description
15:0	EBTM1	SW : RW Total # beats (middle 16-bit value)

0x01303AB4 SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG1

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU1	SW : RW Total # beats (upper 4-bit value)

0x01303AB8 SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG2

Bits	Name	Description
15:0	EBTL2	SW : RW Total # beats (lower 16-bit value)

0x01303ABC SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG2

Bits	Name	Description
15:0	EBTM2	SW : RW Total # beats (middle 16-bit value)

0x01303AC0 SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG2

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU2	SW : RW Total # beats (upper 4-bit value)

0x01303AC4 SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG3

Bits	Name	Description
15:0	EBTL3	SW : RW Total # beats (lower 16-bit value)

0x01303AC8 SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write

Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG3

Bits	Name	Description
15:0	EBTM3	SW : RW Total # beats (middle 16-bit value)

0x01303ACC SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG3

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU3	SW : RW Total # beats (upper 4-bit value)

0x01303AD0 SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG4

Bits	Name	Description
15:0	EBTL4	SW : RW Total # beats (lower 16-bit value)

0x01303AD4 SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG4

Bits	Name	Description
15:0	EBTM4	SW : RW Total # beats (middle 16-bit value)

0x01303AD8 SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG4

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU4	SW : RW Total # beats (upper 4-bit value)

0x01303ADC SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write

Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG5

Bits	Name	Description
15:0	EBTL5	SW : RW Total # beats (lower 16-bit value)

0x01303AE0 SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG5

Bits	Name	Description
15:0	EBTM5	SW : RW Total # beats (middle 16-bit value)

0x01303AE4 SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG5

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU5	SW : RW Total # beats (upper 4-bit value)

0x01303AE8 SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG6

Bits	Name	Description
15:0	EBTL6	SW : RW Total # beats (lower 16-bit value)

0x01303AEC SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG6

Bits	Name	Description
15:0	EBTM6	SW : RW Total # beats (middle 16-bit value)

0x01303AF0 SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG6

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU6	SW : RW Total # beats (upper 4-bit value)

0x01303AF4 SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG7

Bits	Name	Description
15:0	EBTL7	SW : RW Total # beats (lower 16-bit value)

0x01303AF8 SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG7

Bits	Name	Description
15:0	EBTM7	SW : RW Total # beats (middle 16-bit value)

0x01303AFC SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG7

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU7	SW : RW Total # beats (upper 4-bit value)

0x01303B00 SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG0

Bits	Name	Description
15:0	EBYL0	SW : RW Total bytes (lower 16-bit value)

0x01303B04 SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG0

Bits	Name	Description
15:0	EBYM0	SW : RW Total bytes (middle 16-bit value)

0x01303B08 SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG0

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU0	SW : RW Total bytes (upper 11-bit value)

0x01303B0C SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG1

Bits	Name	Description
15:0	EBYL1	SW : RW Total bytes (lower 16-bit value)

0x01303B10 SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG1

Bits	Name	Description
15:0	EBYM1	SW : RW Total bytes (middle 16-bit value)

0x01303B14 SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG1

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU1	SW : RW Total bytes (upper 11-bit value)

0x01303B18 SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG2

Bits	Name	Description
15:0	EBYL2	SW : RW Total bytes (lower 16-bit value)

0x01303B1C SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG2

Bits	Name	Description
15:0	EBYM2	SW : RW Total bytes (middle 16-bit value)

0x01303B20 SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG2

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU2	SW : RW Total bytes (upper 11-bit value)

0x01303B24 SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG3

Bits	Name	Description
15:0	EBYL3	SW : RW Total bytes (lower 16-bit value)

0x01303B28 SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG3

Bits	Name	Description
15:0	EBYM3	SW : RW Total bytes (middle 16-bit value)

0x01303B2C SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG3

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU3	SW : RW Total bytes (upper 11-bit value)

0x01303B30 SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG4

Bits	Name	Description
15:0	EBYL4	SW : RW Total bytes (lower 16-bit value)

0x01303B34 SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG4

Bits	Name	Description
15:0	EBYM4	SW : RW Total bytes (middle 16-bit value)

0x01303B38 SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG4

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU4	SW : RW Total bytes (upper 11-bit value)

0x01303B3C SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG5

Bits	Name	Description
15:0	EBYL5	SW : RW Total bytes (lower 16-bit value)

0x01303B40 SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG5

Bits	Name	Description
15:0	EBYM5	SW : RW Total bytes (middle 16-bit value)

0x01303B44 SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG5

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU5	SW : RW Total bytes (upper 11-bit value)

0x01303B48 SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG6

Bits	Name	Description
15:0	EBYL6	SW : RW Total bytes (lower 16-bit value)

0x01303B4C SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG6

Bits	Name	Description
15:0	EBYM6	SW : RW Total bytes (middle 16-bit value)

0x01303B50 SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG6

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU6	SW : RW Total bytes (upper 11-bit value)

0x01303B54 SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG7

Bits	Name	Description
15:0	EBYL7	SW : RW Total bytes (lower 16-bit value)

0x01303B58 SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG7

Bits	Name	Description
15:0	EBYM7	SW : RW Total bytes (middle 16-bit value)

0x01303B5C SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

SFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG7

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU7	SW : RW Total bytes (upper 11-bit value)

0x01303B60 SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 0.

SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0

Bits	Name	Description
15:14	T0SR	SW : RW Tenure selection for tenure counter 0 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T0MIDFEN	SW : RW Tenure counter 0 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T0INDFEN	SW : RW Tenure counter 0 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T0IND	SW : RW Tenure counter 0 Instruction/Data selection 0x0: Data 0x1: Instruction

SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
8:4	T0MP	SW : RW Tenure master port selection register for tenure counter 0 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
3:0	T0SW	SW : RW Tenure slave way selection register for tenure counter 0 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01303B64 SFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 0.

SFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG0

Bits	Name	Description
15:0	T0MID	SW : RW Tenure counter 0 MID selection (If MID filtering enabled)

0x01303B68 SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 1.

SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1

Bits	Name	Description
15:14	T1SR	SW : RW Tenure selection for tenure counter 1 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T1MIDFEN	SW : RW Tenure counter 1MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T1INDFEN	SW : RW Tenure counter 1Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T1IND	SW : RW Tenure counter 1Instruction/Data selection 0x0: Data 0x1: Instruction

SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
8:4	T1MP	SW : RW Tenure master port selection register for tenure counter 1 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
3:0	T1SW	SW : RW Tenure slave way selection register for tenure counter 1 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01303B6C SFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 1.

SFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG1

Bits	Name	Description
15:0	T1MID	SW : RW Tenure counter 1MID selection (If MID filtering enabled)

0x01303B70 SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 2.

SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2

Bits	Name	Description
15:14	T2SR	SW : RW Tenure selection for tenure counter 2 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T2MIDFEN	SW : RW Tenure counter 2 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T2INDFEN	SW : RW Tenure counter 2 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T2IND	SW : RW Tenure counter 2 Instruction/Data selection 0x0: Data 0x1: Instruction

SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
8:4	T2MP	SW : RW Tenure master port selection register for tenure counter 2 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
3:0	T2SW	SW : RW Tenure slave way selection register for tenure counter 2 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01303B74 SFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 2.

SFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG2

Bits	Name	Description
15:0	T2MID	SW : RW Tenure counter 2 MID selection (If MID filtering enabled)

0x01303B78 SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 3.

SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3

Bits	Name	Description
15:14	T3SR	SW : RW Tenure selection for tenure counter 3 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T3MIDFEN	SW : RW Tenure counter 3 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T3INDFEN	SW : RW Tenure counter 3 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T3IND	SW : RW Tenure counter 3 Instruction/Data selection 0x0: Data 0x1: Instruction

SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
8:4	T3MP	SW : RW Tenure master port selection register for tenure counter 3 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

SFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
3:0	T3SW	SW : RW Tenure slave way selection register for tenure counter 3 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01303B7C SFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 3.

SFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG3

Bits	Name	Description
15:0	T3MID	SW : RW Tenure counter 3 MID selection (If MID filtering enabled)

0x01303B80 SFAB_FABRIC_MONITOR_MIN_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x01FF

This register contains the minimum value of the tenure that is selected using FPTSLR0 and measured in tenure counter 0.

NOTE The reset value for this register is set to 0x01FF, equivalent to 8191 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at 0x01FF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

SFAB_FABRIC_MONITOR_MIN_REG0

Bits	Name	Description
15:0	MIN0	SW : R Minimum value of tenure, in tenure counter 0

0x01303B84 SFAB_FABRIC_MONITOR_MIN_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x01FF

This register contains the minimum value of the tenure that is selected using FPTSLR1 and measured in tenure counter 1.

NOTE The reset value for this register is set to 0x01FF, equivalent to 8191 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at 0x01FF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

SFAB_FABRIC_MONITOR_MIN_REG1

Bits	Name	Description
15:0	MIN1	SW : R Minimum value of tenure, in tenure counter 1

0x01303B88 SFAB_FABRIC_MONITOR_MIN_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x01FF

This register contains the minimum value of the tenure that is selected using FPTSLR2 and measured in tenure counter 2.

NOTE The reset value for this register is set to 0x01FF, equivalent to 8191 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at 0x01FF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

SFAB_FABRIC_MONITOR_MIN_REG2

Bits	Name	Description
15:0	MIN2	SW : R Minimum value of tenure, in tenure counter 2

0x01303B8C SFAB_FABRIC_MONITOR_MIN_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x01FF

This register contains the minimum value of the tenure that is selected using FPTSLR3 and measured in tenure counter 3.

NOTE The reset value for this register is set to 0x01FF, equivalent to 8191 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at 0x01FF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

SFAB_FABRIC_MONITOR_MIN_REG3

Bits	Name	Description
15:0	MIN3	SW : R Minimum value of tenure, in tenure counter 3

0x01303B90 SFAB_FABRIC_MONITOR_MAX_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR0 and measured in tenure counter 0.

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

SFAB_FABRIC_MONITOR_MAX_REG0

Bits	Name	Description
15:0	MAX0	SW : R Maximum value of tenure, in tenure counter 0

0x01303B94 SFAB_FABRIC_MONITOR_MAX_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR1and measured in tenure counter 1

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

SFAB_FABRIC_MONITOR_MAX_REG1

Bits	Name	Description
15:0	MAX1	SW : R Maximum value of tenure, in tenure counter 1

0x01303B98 SFAB_FABRIC_MONITOR_MAX_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR2 and measured in tenure counter 2

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

SFAB_FABRIC_MONITOR_MAX_REG2

Bits	Name	Description
15:0	MAX2	SW : R Maximum value of tenure, in tenure counter 2

0x01303B9C SFAB_FABRIC_MONITOR_MAX_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR3 and measured in tenure counter 3

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

SFAB_FABRIC_MONITOR_MAX_REG3

Bits	Name	Description
15:0	MAX3	SW : R Maximum value of tenure, in tenure counter 3

0x01303BA0 SFAB_FABRIC_MONITOR_TENURE_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 0

SFAB_FABRIC_MONITOR_TENURE_LOWER_REG0

Bits	Name	Description
15:0	LTOT0	SW : RW LSB total value of tenure, in tenure counter 0

0x01303BA4 SFAB_FABRIC_MONITOR_TENURE_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 0.

SFAB_FABRIC_MONITOR_TENURE_UPPER_REG0

Bits	Name	Description
15:0	UTOT0	SW : RW MSB total value of tenure, in tenure counter 0

0x01303BA8 SFAB_FABRIC_MONITOR_TENURE_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 1

SFAB_FABRIC_MONITOR_TENURE_LOWER_REG1

Bits	Name	Description
15:0	LTOT1	SW : RW LSB total value of tenure, in tenure counter 1

0x01303BAC SFAB_FABRIC_MONITOR_TENURE_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 1.

SFAB_FABRIC_MONITOR_TENURE_UPPER_REG1

Bits	Name	Description
15:0	UTOT1	SW : RW MSB total value of tenure, in tenure counter 1

0x01303BB0 SFAB_FABRIC_MONITOR_TENURE_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 2

SFAB_FABRIC_MONITOR_TENURE_LOWER_REG2

Bits	Name	Description
15:0	LTOT2	SW : RW LSB total value of tenure, in tenure counter 2

0x01303BB4 SFAB_FABRIC_MONITOR_TENURE_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 2.

SFAB_FABRIC_MONITOR_TENURE_UPPER_REG2

Bits	Name	Description
15:0	UTOT2	SW : RW MSB total value of tenure, in tenure counter 2

0x01303BB8 SFAB_FABRIC_MONITOR_TENURE_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 3

SFAB_FABRIC_MONITOR_TENURE_LOWER_REG3

Bits	Name	Description
15:0	LTOT3	SW : RW LSB total value of tenure, in tenure counter 3

0x01303BBC SFAB_FABRIC_MONITOR_TENURE_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 3.

SFAB_FABRIC_MONITOR_TENURE_UPPER_REG3

Bits	Name	Description
15:0	UTOT3	SW : RW MSB total value of tenure, in tenure counter 3

0x01303BC0 SFAB_FABRIC_MONITOR_LAST_TENURE_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 0

SFAB_FABRIC_MONITOR_LAST_TENURE_REG0

Bits	Name	Description
15:0	LASTT0	SW : R Last tenure value in tenure counter 0

0x01303BC4 SFAB_FABRIC_MONITOR_LAST_TENURE_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 1

SFAB_FABRIC_MONITOR_LAST_TENURE_REG1

Bits	Name	Description
15:0	LASTT1	SW : R Last tenure value in tenure counter 1

0x01303BC8 SFAB_FABRIC_MONITOR_LAST_TENURE_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 2

SFAB_FABRIC_MONITOR_LAST_TENURE_REG2

Bits	Name	Description
15:0	LASTT2	SW : R Last tenure value in tenure counter 2

0x01303BCC SFAB_FABRIC_MONITOR_LAST_TENURE_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 3

SFAB_FABRIC_MONITOR_LAST_TENURE_REG3

Bits	Name	Description
15:0	LASTT0	SW : R Last tenure value in tenure counter 3

0x01303BD0 SFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 0.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG0

Bits	Name	Description
15:0	T0AL	SW : RW LSB address value Tenure counter 0 address mask

0x01303BD4 SFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 0.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG0

Bits	Name	Description
15:0	T0AU	SW : RW MSB address value Tenure counter 0 address mask

0x01303BD8 SFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 1.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG1

Bits	Name	Description
15:0	T1AL	SW : RW LSB address value Tenure counter 1 address mask

0x01303BDC SFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 1.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG1

Bits	Name	Description
15:0	T1AU	SW : RW MSB address value Tenure counter 1 address mask

0x01303BE0 SFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 2.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG2

Bits	Name	Description
15:0	T2AL	SW : RW LSB address value Tenure counter 2 address mask

0x01303BE4 SFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 2.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG2

Bits	Name	Description
15:0	T2AU	SW : RW MSB address value Tenure counter 2 address mask

0x01303BE8 SFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 3.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG3

Bits	Name	Description
15:0	T3AL	SW : RW LSB address value Tenure counter 3 address mask

0x01303BEC SFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 3.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG3

Bits	Name	Description
15:0	T3AU	SW : RW MSB address value Tenure counter 3 address mask

0x01303BF0 SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 0

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR0.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG0

Bits	Name	Description
15:0	T0AML	SW : RW LSB address value Tenure counter 0 address mask

0x01303BF4 SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 0

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR0.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG0

Bits	Name	Description
15:0	T0AMU	SW : RW MSB address mask value Tenure counter 0 address mask

0x01303BF8 SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 1

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR1.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG1

Bits	Name	Description
15:0	T1AML	SW : RW LSB address value Tenure counter 1 address mask

0x01303BFC SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 1

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR1.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG1

Bits	Name	Description
15:0	T1AMU	SW : RW MSB address mask value Tenure counter 1 address mask

0x01303C00 SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 2

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR2.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG2

Bits	Name	Description
15:0	T2AML	SW : RW LSB address value Tenure counter 2 address mask

0x01303C04 SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 2

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR2.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG2

Bits	Name	Description
15:0	T2AMU	SW : RW MSB address mask value Tenure counter 2 address mask

0x01303C08 SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 3

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR3.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG3

Bits	Name	Description
15:0	T3AML	SW : RW LSB address value Tenure counter 3 address mask

0x01303C0C SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 3

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR3.

SFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG3

Bits	Name	Description
15:0	T3AMU	SW : RW MSB address mask value Tenure counter 3 address mask

0x01303C10 SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG 0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 0 that were longer than the specified threshold for tenure counter 0

SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG0

Bits	Name	Description
15:0	T0ATCL	SW : R LSB count value

0x01303C14 SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 0 that were longer than the specified threshold for tenure counter 0

SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG0

Bits	Name	Description
15:0	T0ATCU	SW : R MSB count value

0x01303C18 SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG 1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 1 that were longer than the specified threshold for tenure counter 1

SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG1

Bits	Name	Description
15:0	T1ATCL	SW : R LSB count value

0x01303C1C SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 1 that were longer than the specified threshold for tenure counter 1

SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG1

Bits	Name	Description
15:0	T1ATCU	SW : R MSB count value

0x01303C20 SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 2 that were longer than the specified threshold for tenure counter 2

SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG2

Bits	Name	Description
15:0	T2ATCL	SW : R LSB count value

0x01303C24 SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 2 that were longer than the specified threshold for tenure counter 2

SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG2

Bits	Name	Description
15:0	T2ATCU	SW : R MSB count value

0x01303C28 SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG 3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 3 that were longer than the specified threshold for tenure counter 3

SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG3

Bits	Name	Description
15:0	T3ATCL	SW : R LSB count value

0x01303C2C SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 3 that were longer than the specified threshold for tenure counter 3

SFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG3

Bits	Name	Description
15:0	T3ATCU	SW : R MSB count value

0x01303C30 SFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 0 are measured.

SFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG0

Bits	Name	Description
12:0	T0TV	SW : RW Tenure counter 0 threshold value

0x01303C34 SFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 1 are measured.

SFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG1

Bits	Name	Description
12:0	T1TV	SW : RW Tenure counter 1 threshold value

0x01303C38 SFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 2 are measured.

SFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG2

Bits	Name	Description
12:0	T2TV	SW : RW Tenure counter 2 threshold value

0x01303C3C SFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 3 are measured.

SFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG3

Bits	Name	Description
12:0	T3TV	SW : RW Tenure counter 3 threshold value

0x01303C40 SFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 0

SFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG0

Bits	Name	Description
15:0	T0MM	SW : RW MID Mask value

0x01303C44 SFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 1

SFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG1

Bits	Name	Description
15:0	T1MM	SW : RW MID Mask value

0x01303C48 SFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 2

SFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG2

Bits	Name	Description
15:0	T2MM	SW : RW MID Mask value

0x01303C4C SFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 3

SFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG3

Bits	Name	Description
15:0	T3MM	SW : RW MID Mask value

0x01303C50 SFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure0 register.

SFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG0

Bits	Name	Description
15:0	TLC0	SW : R LSB count value Incremented every time a tenure under observation completes in tenure counter 0

0x01303C54 SFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure0 register.

SFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG0

Bits	Name	Description
15:0	TUC0	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 0

0x01303C58 SFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure1 register.

SFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG1

Bits	Name	Description

0x01303C5C SFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure1 register.

SFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG1

Bits	Name	Description
15:0	TUC1	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 1

0x01303C60 SFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure2 register.

SFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG2

Bits	Name	Description
15:0	TLC2	SW : R LSB count value Incremented every time a tenure under observation completes in tenure counter 2

0x01303C64 SFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure2 register.

SFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG2

Bits	Name	Description
15:0	TUC2	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 2

0x01303C68 SFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure3 register.

SFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG3

Bits	Name	Description
15:0	TLC3	SW : R LSB count value Incremented every time a tenure under observation completes in tenure counter 3

0x01303C6C SFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure3 register.

SFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG3

Bits	Name	Description
15:0	TUC3	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 3

0x01303C70 SFAB_FABRIC_MONITOR_TENURE_PICK_PORTS_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the main port and other port selection for the 4 event counters.

SFAB_FABRIC_MONITOR_TENURE_PICK_PORTS_REG

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3	T3PP	SW : RW Tenure counter 3 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T3MP or T3SW
2	T2PP	SW : RW Tenure counter 2 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T2MP or T2SW

SFAB_FABRIC_MONITOR_TENURE_PICK_PORTS_REG (cont.)

Bits	Name	Description
1	T1PP	SW : RW Tenure counter 1 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T1MP or T1SW
0	T0PP	SW : RW Tenure counter 0 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T0MP or T0SW

0x01303C80 SFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 0

SFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG0

Bits	Name	Description
15:0	LTOTU0	SW : RW LSB total union value of tenure, in tenure counter 0

0x01303C84 SFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 0.

SFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG0

Bits	Name	Description
15:0	UTOTU0	SW : RW MSB total union value of tenure, in tenure counter 0

0x01303C88 SFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 1

SFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG1

Bits	Name	Description
15:0	LTOTU1	SW : RW LSB total union value of tenure, in tenure counter 1

0x01303C8C SFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 1.

SFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG1

Bits	Name	Description
15:0	UTOTU1	SW : RW MSB total union value of tenure, in tenure counter 1

0x01303C90 SFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 2

SFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG2

Bits	Name	Description
15:0	LTOTU2	SW : RW LSB total union value of tenure, in tenure counter 2

0x01303C94 SFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 2.

SFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG2

Bits	Name	Description
15:0	UTOTU2	SW : RW MSB total union value of tenure, in tenure counter 2

0x01303C98 SFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 3

SFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG3

Bits	Name	Description
15:0	LTOTU3	SW : RW LSB total union value of tenure, in tenure counter 3

0x01303C9C SFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 3.

SFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG3

Bits	Name	Description
15:0	UTOTU3	SW : RW MSB total union value of tenure, in tenure counter 3

0x01303CA0 SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 0, that were pipelined.

SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG0

Bits	Name	Description

0x01303CA4 SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 0, that were pipelined.

SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG0

Bits	Name	Description
15:0	TUCP0	SW : R MSB count value TUCP0,TLCP0 value incremented every time a pipelined tenure completes in tenure counter 0

0x01303CA8 SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 1, that were pipelined.

SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG1

Bits	Name	Description

0x01303CAC SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 1, that were pipelined.

SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG1

Bits	Name	Description
15:0	TUCP1	SW : R MSB count value TUCP1,TLCP1 value incremented every time a pipelined tenure completes in tenure counter 1

0x01303CB0 SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 2, that were pipelined.

SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG2

Bits	Name	Description

0x01303CB4 SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 2, that were pipelined.

SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG2

Bits	Name	Description
15:0	TUCP2	SW : R MSB count value TUCP1,TLCP1 value incremented every time a pipelined tenure completes in tenure counter 2

0x01303CB8 SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 3, that were pipelined.

SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG3

Bits	Name	Description

0x01303CBC SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 3, that were pipelined.

SFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG3

Bits	Name	Description
15:0	TUCP3	SW : R MSB count value TUCP3,TLCP3 value incremented every time a pipelined tenure completes in tenure counter 3

0x01303CC0 SFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the max number of tenures pipelined at any point during the monitoring window for tenure counter 0

SFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG0

Bits	Name	Description
15:0	TMCP0	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 0

0x01303CC4 SFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the max number of tenures pipelined at any point during the monitoring window for tenure counter 1

SFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG1

Bits	Name	Description
15:0	TMCP1	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 1

0x01303CC8 SFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the max number of tenures pipelined at any point during the monitoring window for tenure counter 2

SFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG2

Bits	Name	Description
15:0	TMCP2	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 2

0x01303CCC SFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the max number of tenures pipelined at any point during the monitoring window for tenure counter 3

SFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG3

Bits	Name	Description
15:0	TMCP3	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 3

0x01303CD0 SFAB_FABRIC_MONITOR_INFLIGHT_TENURE_CORRECTION_MODE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the facility to correlate a particular event counter to a tenure counter. When the tenure results of a counter are reset during a monitoring window (to account for errors due to starting the monitor in the middle of traffic), the event counters too get reset if the correlation between them is enabled.

NOTE PCORR bit (bit 0) should not be set for APQ8064.

SFAB_FABRIC_MONITOR_INFLIGHT_TENURE_CORRECTION_MODE_REG

Bits	Name	Description
15:9	RESERVED_15_9	Reserved Bits
8	EC7COR	SW : RW 0x1: Link Event Counter 7 to Tenure Counter 3 0x0: Event Counter 7 is independent

SFAB_FABRIC_MONITOR_INFLIGHT_TENURE_CORRECTION_MODE_REG (cont.)

Bits	Name	Description
7	EC6COR	SW : RW 0x1: Link Event Counter 6 to Tenure Counter 2 0x0: Event Counter 6 is independent
6	EC5COR	SW : RW 0x1: Link Event Counter 5 to Tenure Counter 1 0x0: Event Counter 5 is independent
5	EC4COR	SW : RW 0x1: Link Event Counter 4 to Tenure Counter 0 0x0: Event Counter 4 is independent
4	EC3COR	SW : RW 0x1: Link Event Counter 3 to Tenure Counter 3 0x0: Event Counter 3 is independent
3	EC2COR	SW : RW 0x1: Link Event Counter 2 to Tenure Counter 2 0x0: Event Counter 2 is independent
2	EC1COR	SW : RW 0x1: Link Event Counter 1 to Tenure Counter 1 0x0: Event Counter 1 is independent
1	EC0COR	SW : RW 0x1: Link Event Counter 0 to Tenure Counter 0 0x0: Event Counter 0 is independent
0	PCORR	SW : RW This is the enable for tenure correction mode This bit SHOULD NOT be set for APQ8064 and newer configs.

0x01303CE0 SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures counted by tenure counter 0 that correspond to out-of-order transactions.

SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG0

Bits	Name	Description
15:0	TOLC0	SW : R LSB count value Incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 0

0x01303CE4 SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures counted by tenure counter 0 that correspond to out-of-order transactions

SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG0

Bits	Name	Description
15:0	TOUC0	SW : R MSB count value TOUC,TOLC value incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 0

0x01303CE8 SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures counted by tenure counter 1 that correspond to out-of-order transactions.

SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG1

Bits	Name	Description
15:0	TOLC1	SW : R LSB count value Incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 1

0x01303CEC SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures counted by tenure counter 1 that correspond to out-of-order transactions

SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG1

Bits	Name	Description
15:0	TOUC1	SW : R MSB count value TOUC,TOLC value incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 1

0x01303CF0 SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures counted by tenure counter 2 that correspond to out-of-order transactions.

SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG2

Bits	Name	Description
15:0	TOLC2	SW : R LSB count value Incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 2

0x01303CF4 SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures counted by tenure counter 2 that correspond to out-of-order transactions

SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG2

Bits	Name	Description
15:0	TOUC2	SW : R MSB count value TOUC,TOLC value incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 2

0x01303CF8 SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures counted by tenure counter 3 that correspond to out-of-order transactions.

SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG3

Bits	Name	Description
15:0	TOLC3	SW : R LSB count value Incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 3

0x01303CFC SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures counted by tenure counter 3 that correspond to out-of-order transactions

SFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG3

Bits	Name	Description
15:0	TOUC3	SW : R MSB count value TOUC,TOLC value incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 3

0x01303D00 SFAB_FABRIC_MONITOR_RTR_STATUS_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains 4 status bits (one for each performance monitor tenure counter). Each bit indicates whether the monitoring results pertaining to the associated tenure counter have been reset (to account for errors due to starting the monitor in the middle of traffic) or not.

SFAB_FABRIC_MONITOR_RTR_STATUS_REG

Bits	Name	Description
15:4	RESERVED15_4	Reserved
3	TC3_RESET	SW: R When set, this bit indicates that tenure counter 3 results have been reset by the design during the monitoring window, to account for errors due to starting the monitor in the middle of traffic
2	TC2_RESET	SW: R When set, this bit indicates that tenure counter 2 results have been reset by the design during the monitoring window, to account for errors due to starting the monitor in the middle of traffic
1	TC1_RESET	SW: R When set, this bit indicates that tenure counter 1 results have been reset by the design during the monitoring window, to account for errors due to starting the monitor in the middle of traffic
0	TC0_RESET	SW: R When set, this bit indicates that tenure counter 0 results have been reset by the design during the monitoring window, to account for errors due to starting the monitor in the middle of traffic

0x01303D04 SFAB_FABRIC_MONITOR_IDLE_INTERNAL_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 0 to Master 15). A value of 1 indicates that the internally generated idle status is to be used to determine when to reset the performance monitor tenure counter results (resetting the tenure counter results is needed to compensate for errors due to enabling the tenure counters in the middle of traffic). A value of 0 will indicate that the primary idle input is to be used instead.

NOTE These settings will have an effect only in case of AXI master ports.

SFAB_FABRIC_MONITOR_IDLE_INTERNAL_LOWER_REG

Bits	Name	Description
15	M15_PII	SW : RW 0x1: The internally generated idle status for Master 15 will be used by the performance monitor 0x0: Primary input I_AXI_M15_IDLE is used by the performance monitor

SFAB_FABRIC_MONITOR_IDLE_INTERNAL_LOWER_REG (cont.)

Bits	Name	Description
14	M14_PII	SW : RW 0x1: The internally generated idle status for Master 14 will be used by the performance monitor 0x0: Primary input I_AXI_M14_IDLE is used by the performance monitor
13	M13_PII	SW : RW 0x1: The internally generated idle status for Master 13 will be used by the performance monitor 0x0: Primary input I_AXI_M13_IDLE is used by the performance monitor
12	M12_PII	SW : RW 0x1: The internally generated idle status for Master 12 will be used by the performance monitor 0x0: Primary input I_AXI_M12_IDLE is used by the performance monitor
11	M11_PII	SW : RW 0x1: The internally generated idle status for Master 11 will be used by the performance monitor 0x0: Primary input I_AXI_M11_IDLE is used by the performance monitor
10	M10_PII	SW : RW 0x1: The internally generated idle status for Master 10 will be used by the performance monitor 0x0: Primary input I_AXI_M10_IDLE is used by the performance monitor
9	M9_PII	SW : RW 0x1: The internally generated idle status for Master 9 will be used by the performance monitor 0x0: Primary input I_AXI_M9_IDLE is used by the performance monitor
8	M8_PII	SW : RW 0x1: The internally generated idle status for Master 8 will be used by the performance monitor 0x0: Primary input I_AXI_M8_IDLE is used by the performance monitor
7	M7_PII	SW : RW 0x1: The internally generated idle status for Master 7 will be used by the performance monitor 0x0: Primary input I_AXI_M7_IDLE is used by the performance monitor
6	M6_PII	SW : RW 0x1: The internally generated idle status for Master 6 will be used by the performance monitor 0x0: Primary input I_AXI_M6_IDLE is used by the performance monitor

SFAB_FABRIC_MONITOR_IDLE_INTERNAL_LOWER_REG (cont.)

Bits	Name	Description
5	M5_PII	SW : RW 0x1: The internally generated idle status for Master 5 will be used by the performance monitor 0x0: Primary input I_AXI_M5_IDLE is used by the performance monitor
4	M4_PII	SW : RW 0x1: The internally generated idle status for Master 4 will be used by the performance monitor 0x0: Primary input I_AXI_M4_IDLE is used by the performance monitor
3	M3_PII	SW : RW 0x1: The internally generated idle status for Master 3 will be used by the performance monitor 0x0: Primary input I_AXI_M3_IDLE is used by the performance monitor
2	M2_PII	SW : RW 0x1: The internally generated idle status for Master 2 will be used by the performance monitor 0x0: Primary input I_AXI_M2_IDLE is used by the performance monitor
1	M1_PII	SW : RW 0x1: The internally generated idle status for Master 1 will be used by the performance monitor 0x0: Primary input I_AXI_M1_IDLE is used by the performance monitor
0	M0_PII	SW : RW 0x1: The internally generated idle status for Master 0 will be used by the performance monitor 0x0: Primary input I_AXI_M0_IDLE is used by the performance monitor

0x01303D08 SFAB_FABRIC_MONITOR_IDLE_INTERNAL_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 16 to Master 31). A value of 1 indicates that the internally generated idle status is to be used to determine when to reset the performance monitor tenure counter results (resetting the tenure counter results is needed to compensate for errors due to enabling the tenure counters in the middle of traffic). A value of 0 will indicate that the primary idle input is to be used instead.

NOTE These settings will have an effect only in case of AXI master ports.

SFAB_FABRIC_MONITOR_IDLE_INTERNAL_UPPER_REG

Bits	Name	Description
31	M31_PII	SW : RW 0x1: The internally generated idle status for Master 31 will be used by the performance monitor 0x0: Primary input I_AXI_M31_IDLE is used by the performance monitor
30	M30_PII	SW : RW 0x1: The internally generated idle status for Master 30 will be used by the performance monitor 0x0: Primary input I_AXI_M30_IDLE is used by the performance monitor
29	M29_PII	SW : RW 0x1: The internally generated idle status for Master 29 will be used by the performance monitor 0x0: Primary input I_AXI_M29_IDLE is used by the performance monitor
28	M28_PII	SW : RW 0x1: The internally generated idle status for Master 28 will be used by the performance monitor 0x0: Primary input I_AXI_M28_IDLE is used by the performance monitor
27	M27_PII	SW : RW 0x1: The internally generated idle status for Master 27 will be used by the performance monitor 0x0: Primary input I_AXI_M27_IDLE is used by the performance monitor
26	M26_PII	SW : RW 0x1: The internally generated idle status for Master 26 will be used by the performance monitor 0x0: Primary input I_AXI_M26_IDLE is used by the performance monitor
25	M25_PII	SW : RW 0x1: The internally generated idle status for Master 25 will be used by the performance monitor 0x0: Primary input I_AXI_M25_IDLE is used by the performance monitor
24	M24_PII	SW : RW 0x1: The internally generated idle status for Master 24 will be used by the performance monitor 0x0: Primary input I_AXI_M24_IDLE is used by the performance monitor

SFAB_FABRIC_MONITOR_IDLE_INTERNAL_UPPER_REG (cont.)

Bits	Name	Description
23	M23_PII	SW : RW 0x1: The internally generated idle status for Master 23 will be used by the performance monitor 0x0: Primary input I_AXI_M23_IDLE is used by the performance monitor
22	M22_PII	SW : RW 0x1: The internally generated idle status for Master 22 will be used by the performance monitor 0x0: Primary input I_AXI_M22_IDLE is used by the performance monitor
21	M21_PII	SW : RW 0x1: The internally generated idle status for Master 21 will be used by the performance monitor 0x0: Primary input I_AXI_M21_IDLE is used by the performance monitor
20	M20_PII	SW : RW 0x1: The internally generated idle status for Master 20 will be used by the performance monitor 0x0: Primary input I_AXI_M20_IDLE is used by the performance monitor
19	M19_PII	SW : RW 0x1: The internally generated idle status for Master 19 will be used by the performance monitor 0x0: Primary input I_AXI_M19_IDLE is used by the performance monitor
18	M18_PII	SW : RW 0x1: The internally generated idle status for Master 18 will be used by the performance monitor 0x0: Primary input I_AXI_M18_IDLE is used by the performance monitor
17	M17_PII	SW : RW 0x1: The internally generated idle status for Master 17 will be used by the performance monitor 0x0: Primary input I_AXI_M17_IDLE is used by the performance monitor
16	M16_PII	SW : RW 0x1: The internally generated idle status for Master 16 will be used by the performance monitor 0x0: Primary input I_AXI_M16_IDLE is used by the performance monitor

0x01303D0C SFAB_FABRIC_MONITOR_RTR_MASK_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains 1 bit for each of the tenure counters that controls the RTR assertion and clearing of the monitoring results pertaining to the associated tenure counter to account for errors due to starting the monitor in the middle of traffic. A value of 1 indicates that RTR will not be asserted.

SFAB_FABRIC_MONITOR_RTR_MASK_REG

Bits	Name	Description
31:4	RESERVED_31_4	Reserved
3	RTR_MASK_3	SW : RW 0x1: No RTR will be asserted for Tenure Counter 3 0x0: The design is allowed to assert RTR for Tenure Counter 3
2	RTR_MASK_2	SW : RW 0x1: No RTR will be asserted for Tenure Counter 2 0x0: The design is allowed to assert RTR for Tenure Counter 2
1	RTR_MASK_1	SW : RW 0x1: No RTR will be asserted for Tenure Counter 1 0x0: The design is allowed to assert RTR for Tenure Counter 1
0	RTR_MASK_0	SW : RW 0x1: No RTR will be asserted for Tenure Counter 0 0x0: The design is allowed to assert RTR for Tenure Counter 0

0x01303D10 SFAB_FABRIC_MASTER_SELECT_HYST_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 0 to Master 15). A value of 1 indicates that the hysteresis timer value is used to keep the master segmented clock on. A value of 0 indicates that the hysteresis timer will not be used in the master segmented clock on.

SFAB_FABRIC_MASTER_SELECT_HYST_LOWER_REG

Bits	Name	Description
15	M15_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

SFAB_FABRIC_MASTER_SELECT_HYST_LOWER_REG (cont.)

Bits	Name	Description
14	M14_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
13	M13_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
12	M12_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
11	M11_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
10	M10_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
9	M9_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
8	M8_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
7	M7_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
6	M6_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
5	M5_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

SFAB_FABRIC_MASTER_SELECT_HYST_LOWER_REG (cont.)

Bits	Name	Description
4	M4_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
3	M3_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
2	M2_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
1	M1_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
0	M0_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

0x01303D14 SFAB_FABRIC_MASTER_SELECT_HYST_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 16to Master 31). A value of 1 indicates that the hysteresis timer value is used to keep the master segmented clock on. A value of 0 indicates that the hysteresis timer will not be used in the master segmented clock on.

SFAB_FABRIC_MASTER_SELECT_HYST_UPPER_REG

Bits	Name	Description
15	M31_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
14	M30_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

SFAB_FABRIC_MASTER_SELECT_HYST_UPPER_REG (cont.)

Bits	Name	Description
13	M29_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
12	M28_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
11	M27_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
10	M26_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
9	M25_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
8	M24_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
7	M23_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
6	M22_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
5	M21_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
4	M20_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

SFAB_FABRIC_MASTER_SELECT_HYST_UPPER_REG (cont.)

Bits	Name	Description
3	M19_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
2	M18_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
1	M17_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
0	M16_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

0x01303D18 SFAB_FABRIC_MASTER_USE_CG_DISABLE_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 0 to Master 15). A value of 1 indicates that the FMCHR bit 15 can be used to always keep the master segmented clock on, hence disabling HW dynamic clock gating. A value of 0 indicates that the FMCHR bit cannot be used to disable HW dynamic clock gating.

SFAB_FABRIC_MASTER_USE_CG_DISABLE_LOWER_REG

Bits	Name	Description
15	M15_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 15 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
14	M14_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 14 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

SFAB_FABRIC_MASTER_USE_CG_DISABLE_LOWER_REG (cont.)

Bits	Name	Description
13	M13_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 13 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
12	M12_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 12 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
11	M11_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 11 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
10	M10_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 10 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
9	M9_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 9 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
8	M8_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 8 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
7	M7_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 7 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
6	M6_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 6 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
5	M5_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 5 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

SFAB_FABRIC_MASTER_USE_CG_DISABLE_LOWER_REG (cont.)

Bits	Name	Description
4	M4_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 4 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
3	M3_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 3 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
2	M2_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 2 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
1	M1_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 1 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
0	M0_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 0 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

0x01303D1C SFAB_FABRIC_MASTER_USE_CG_DISABLE_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 16 to Master 31). A value of 1 indicates that the FMCHR bit 15 can be used to always keep the master segmented clock on, hence disabling HW dynamic clock gating. A value of 0 indicates that the FMCHR bit cannot be used to disable HW dynamic clock gating.

SFAB_FABRIC_MASTER_USE_CG_DISABLE_UPPER_REG

Bits	Name	Description
15	M31_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 31 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

SFAB_FABRIC_MASTER_USE_CG_DISABLE_UPPER_REG (cont.)

Bits	Name	Description
14	M30_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 30 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
13	M29_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 29 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
12	M28_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 28 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
11	M27_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 27 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
10	M26_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 26 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
9	M25_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 25 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
8	M24_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 24 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
7	M23_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 23 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
6	M22_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 22 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

SFAB_FABRIC_MASTER_USE_CG_DISABLE_UPPER_REG (cont.)

Bits	Name	Description
5	M21_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 21 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
4	M20_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 20 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
3	M19_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 19 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
2	M18_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 18 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
1	M17_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 17 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
0	M16_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 16 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

0x01303D20 SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter0.

SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG0

Bits	Name	Description
15:0	RTENL0	SW : RW Contains the LSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked bytenure counter 0

0x01303D24 SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter0.

SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG0

Bits	Name	Description
15:0	RTENU0	SW : RW Contains the MSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 0

0x01303D28 SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter1.

SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG1

Bits	Name	Description
15:0	RTENL1	SW : RW Contains the LSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 1

0x01303D2C SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter1.

SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG1

Bits	Name	Description
15:0	RTENU1	SW : RW Contains the MSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 1

0x01303D30 SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter2.

SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG2

Bits	Name	Description
15:0	RTENL2	SW : RW Contains the LSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 2

0x01303D34 SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter2.

SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG2

Bits	Name	Description
15:0	RTENU2	SW : RW Contains the MSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 2

0x01303D38 SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter3.

SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG3

Bits	Name	Description
15:0	RTENL3	SW : RW Contains the LSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 3

0x01303D3C SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter3.

SFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG3

Bits	Name	Description
15:0	RTENU3	SW : RW Contains the MSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 3

8.3 System Fabric M2MVT Registers (0x01300000 SFAB_BASE)

This section contains the System Fabric M2MVT registers.

8.3.1 M2VMT registers map with generic permutations

See Table 8-2.

Table 8-2 System Fabric M2VMT Registers Table

Register	Address / Range	Description	Type	Default
M2VMT_M2VRv [4:0]	x000 to x7FC	Defines VMID value associated with the M2VMT index:		
Where v = NUM_M2VMT_ENTRIES from the design generic	R/W	x		
Reserved	x800 to xFF0	Reserved	X	X
M2VMT_REV	xFF4	M2VMT Revision Register	RO	'10000000'b
M2VMT_IDR [8:0]	xFF8	ID Register	RO	NUM_M2VMT_ENTRIES
Reserved	xFFC	Reserved	X	x

REMOVE_M2VMT_RPU = '0' &
REMOVE_M2VMT_SYND_REG_IF_RPU_IS_PRESENT='0'

The normal default use model uses M2VMT_RPU='0' and REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT= '0'. In this default configuration, local RPU and associated syndrome registers and interrupt support registers are available.

0x01306000+ 0x4*v SFAB_M2VMT_M2VMRv_2, v=[0..15]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics

SFAB_M2VMT_M2VMRv_2

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9-bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRv address associations.

0x01306FF4 SFAB_M2VMT_REV_2

Type: Read
Clock: FABRIC_CLOCK
Reset State: '10000000'b

Reports the revision information for the M2VMT core and wrapper.

SFAB_M2VMT_REV_2

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

0x01306FF8 SFAB_M2VMT_IDR_2

Type: Read
Clock: FABRIC_CLOCK
Reset State: M2VMTSIZE

Reports the size of the M2VMT table. It is a read-only register.

SFAB_M2VMT_IDR_2

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

SFAB_M2VMT_IDR_2 (cont.)

Bits	Name	Description
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x01307000+0x4*v SFAB_M2VMT_M2VMRv_3, v=[0..15]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics

SFAB_M2VMT_M2VMRv_3

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRv address associations.

0x01307FF4 SFAB_M2VMT_REV_3

Type: Read
Clock: FABRIC_CLOCK
Reset State: '10000000'b

Reports the revision information for the M2VMT core and wrapper.

SFAB_M2VMT_REV_3

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

Clock: FABRIC_CLOCK
Reset State: M2VMTSIZE

Reports the size of the M2VMT table. It is a read-only register.

SFAB_M2VMT_IDR_3

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x01308000+0x4*v SFAB_M2VMT_M2VMRv_4, v=[0..0]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics.

SFAB_M2VMT_M2VMRv_4

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRv address associations.

0x01308FF4 SFAB_M2VMT_REV_4

Type: Read
Clock: FABRIC_CLOCK
Reset State: '10000000'b

Reports the revision information for the M2VMT core and wrapper.

SFAB_M2VMT_REV_4

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

0x01308FF8 SFAB_M2VMT_IDR_4

Type: Read
Clock: FABRIC_CLOCK
Reset State: M2VMTSIZE

Reports the size of the M2VMT table. It is a read-only register.

SFAB_M2VMT_IDR_4

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

SFAB_M2VMT_IDR_4 (cont.)

Bits	Name	Description
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x01309000+0x4*v SFAB_M2VMT_M2VMRv_5, v=[0..1]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics

SFAB_M2VMT_M2VMRv_5

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRv address associations.

0x01309FF4 SFAB_M2VMT_REV_5

Type: Read
Clock: FABRIC_CLOCK
Reset State: '10000000'b

Reports the revision information for the M2VMT core and wrapper.

SFAB_M2VMT_REV_5

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

0x01309FF8 SFAB_M2VMT_IDR_5

Type: Read
Clock: FABRIC_CLOCK
Reset State: M2VMTSIZE

Reports the size of the M2VMT table. It is a read-only register.

SFAB_M2VMT_IDR_5

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x0130A000+0x4*v SFAB_M2VMT_M2VMRv_6, v=[0..3]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics

SFAB_M2VMT_M2VMRv_6

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index to make the proper master to M2VMT_M2VRv address associations.

0x0130AFF4 SFAB_M2VMT_REV_6

Type: Read
Clock: FABRIC_CLOCK
Reset State: '10000000'b

Reports the revision information for the M2VMT core and wrapper.

SFAB_M2VMT_REV_6

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

SFAB_M2VMT_IDR_6

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

SFAB_M2VMT_IDR_6 (cont.)

Bits	Name	Description
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics

SFAB_M2VMT_M2VMRv_8

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRv address associations.

0x0130CFF4 SFAB_M2VMT_REV_8

Type: Read
Clock: FABRIC_CLOCK
Reset State: '10000000'b

Reports the revision information for the M2VMT core and wrapper.

SFAB_M2VMT_REV_8

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

0x0130CFF8 SFAB_M2VMT_IDR_8

Type: Read
Clock: FABRIC_CLOCK
Reset State: M2VMTSIZE

Reports the size of the M2VMT table. It is a read-only register.

SFAB_M2VMT_IDR_8

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x01310000+0x4*v SFAB_M2VMT_M2VMRv_12, v=[0..1]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics

SFAB_M2VMT_M2VMRv_12

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRv address associations.

0x01310FF4 SFAB_M2VMT_REV_12

Type: Read
Clock: FABRIC_CLOCK
Reset State: '10000000'b

Reports the revision information for the M2VMT core and wrapper.

SFAB_M2VMT_REV_12

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

0x01310FF8 SFAB_M2VMT_IDR_12

Type: Read
Clock: FABRIC_CLOCK
Reset State: M2VMTSIZE

Reports the size of the M2VMT table. It is a read-only register.

SFAB_M2VMT_IDR_12

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

SFAB_M2VMT_IDR_12 (cont.)

Bits	Name	Description
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x01311000+0x4*v SFAB_M2VMT_M2VMRv_13, v=[0..15]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics

SFAB_M2VMT_M2VMRv_13

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRv address associations.

0x01311FF4 SFAB_M2VMT_REV_13

Type: Read
Clock: FABRIC_CLOCK
Reset State: '10000000'b

Reports the revision information for the M2VMT core and wrapper.

SFAB_M2VMT_REV_13

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

0x01311FF8 SFAB_M2VMT_IDR_13

Type: Read
Clock: FABRIC_CLOCK
Reset State: M2VMTSIZE

Reports the size of the M2VMT table. It is a read-only register.

SFAB_M2VMT_IDR_13

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x01312000+0x4*v SFAB_M2VMT_M2VMRv_14, v=[0..0]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics

SFAB_M2VMT_M2VMRv_14

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRv address associations.

0x01312FF4 SFAB_M2VMT_REV_14

Type: Read
Clock: FABRIC_CLOCK
Reset State: '10000000'b

Reports the revision information for the M2VMT core and wrapper.

SFAB_M2VMT_REV_14

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

0x01312FF8 SFAB_M2VMT_IDR_14

Type: Read
Clock: FABRIC_CLOCK
Reset State: M2VMTSIZE

Reports the size of the M2VMT table. It is a read-only register.

SFAB_M2VMT_IDR_14

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

SFAB_M2VMT_IDR_14 (cont.)

Bits	Name	Description
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

8.4 Application Fabric Registers (0x01400000 AFAB_BASE)

This section contains the Application Fabric registers.

0x01400000 AFAB_FABRIC_ID_REVISION_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x2C40

This register contains the upper 16-bits of the core ID and revision number and contains the Major/Minor Revision information as well as the site ID where the core was developed.

AFAB_FABRIC_ID_REVISION_REG0

Bits	Name	Description
15:13	MAJ	SW : R Major Revision 0x1: Initial Release
12:10	MIN	SW : R Minor Revision 0x3: APQ8064
9:6	SITE	SW : R Site ID 0x1: RTP
5:0	RESERVED_BITS_5_0	

0x01400004 AFAB_FABRIC_ID_REVISION_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0001

This register contains the lower 16-bits of the core ID and revision number and contains the Core ID number.

AFAB_FABRIC_ID_REVISION_REG1

Bits	Name	Description
15:8	RESERVED_BITS_3_2	
7:0	ID	SW : R Core ID 0x1: FABRIC

0x01400008 AFAB_FABRIC_CONFIGURATION_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0002

This register defines the operating frequency, power down mode for the performance monitor, as well as the decode error and performance monitor cycle counter interrupts. It also has the control bit to globally disable redirection in Fabric.

The ISYND bits contain the interrupt syndrome. If more than one interrupt type occurs, more than one bit will be set. For example, if a decode error occurs and the performance monitor cycle-counter expires, the ISYND field will contain the value 3'b101. Performance monitor interrupts are only generated when the interrupt enable (PMIE) bit is set for the interrupt type.

If multiple decode errors occur, only the first error is recorded. If multiple decode errors occur at the same clock cycle, only a single error is considered, with Master 0 having the highest priority and Master 5 the lowest priority.

The determination of the time an error is recorded in the Fabric Error Status Register (FESR) is based on the following criteria:

For Reads: When Mn_RLAST is asserted.

For Writes: When Mn_BRESP is asserted.

Therefore, if two different masters make requests with invalid addresses to the FABRIC, the master which receives the RLAST or BRESP first for the invalid transaction, is recorded in the FESR. See FABRIC_ERROR_STATUS_REG_1 for information that is captured when a decode error occurs. The address of the request which caused a decode error is captured in the FABRIC_ERROR_UPPER_ADDR_REG and the FABRIC_ERROR_LOWER_ADDR_REG. If they happen simultaneously, the master priority is used to resolve which error is recorded in a fixed priority scheme. Master 0 has highest priority and Master 31 has the lowest priority.

NOTE If the master does not have RREADY or BREADY asserted by default (i.e., it is not able to receive all responses for outstanding requests and may throttle the FABRIC), the FABRIC_Interrupt generation may precede the return of the last read data beat or the write response.

To clear the interrupt, the ISYND bits are required to be written to 3'b000.

The performance monitor event/tenure overflow condition is indicated when the ISYND value is 010. An event overflow occurs when the event counter has reached its maximum value. A tenure overflow condition occurs:

When the tenure counter has reached its maximum value

OR

More than 16 tenures are outstanding, since the performance monitor implements only 16 counters for tenure tracking. Note that if the tenure overflows, values read from the performance monitors

for min/max/total/last tenure will no longer be valid as values recorded after the overflow will be incorrect.

AFAB_FABRIC_CONFIGURATION_REG

Bits	Name	Description
15:7	RESERVED_BITS_15_7	Reserved Bits
6:4	ISYND	SW : RW Interrupt syndrome* 0x0: No/Clear (interrupt) 0x1: Cycle counter expired (Perfmon) 0x2: Event/tenure overflow (Perfmon) 0x4: Decode error detected 0x5: MPU Error 0x6: Timeout Error (SPB)
3	RESERVED_BITS_3	
2	CSPDM	SW:RW CSR block power down mode 0x0: Disable Dynamic Clock Gating 0x1: Enable Dynamic Clock Gating
1	PPDM	SW : RW Performance monitor power down/disable mode 0x0: Monitor Enabled 0x1: Monitor Disabled (Gates clocks to performance monitor registers)
0	PMIE	SW : RW Perfmon interrupt enable

0x01400100+4*n AFAB_FABRIC_SEGMENT_UADDR_0_REG_n, n=[0..4]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the upper and lower address ranges for a particular slave segment (n).If this slave segment (n) is a link then this register defines the first address range for the slave link.

NOTE A segmentation address register is required for each slave segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

AFAB_FABRIC_SEGMENT_UADDR_0_REG_n

Bits	Name	Description
15:10	RESERVED_15_10	
9:0	SUA	SW : RW Segment 'n' upper address (based on parameter- up to 10-bits)

0x01400200+4*n AFAB_FABRIC_SEGMENT_LADDR_0_REG_n, n=[0..4]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the upper and lower address ranges for a particular slave segment (n). If this slave segment (n) is a link then this register defines the first address range for the slave link.

NOTE A segmentation address register is required for each slave segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

AFAB_FABRIC_SEGMENT_LADDR_0_REG_n

Bits	Name	Description
15	SSE	SW : RW Slave segment n enable

AFAB_FABRIC_SEGMENT_LADDR_0_REG_n (cont.)

Bits	Name	Description
14	SSIE	SW : RW Slave segment "n" & "n+1" nterleave enable
13:10	RESERVED_13_10	
9:0	SLA	SW : RW Segment n lower address (based on parameter- up to 10-bits)

0x01400300+4*n AFAB_FABRIC_SEGMENT_UADDR_1_REG_n, n=[0..4]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the upper address for a particular slave link segment (n) if it's a link. A link segment can have up to two separate address ranges. This register defines the second address range for the slave link.

NOTE A link segmentation address register is required for each slave link segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

AFAB_FABRIC_SEGMENT_UADDR_1_REG_n

Bits	Name	Description
15:10	RESERVED_15_10	
9:0	SUA	SW : RW Segment 'n' upper address (based on parameter- up to 10-bits)

0x01400400+4*n AFAB_FABRIC_SEGMENT_LADDR_1_REG_n, n=[0..4]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the lower address range for a particular slave link segment (n). A link segment can have up to two separate address ranges. This register defines the second address range for the slave link.

NOTE A segmentation link address register is required for each slave link segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

AFAB_FABRIC_SEGMENT_LADDR_1_REG_n

Bits	Name	Description
15:10	RESERVED_15_10	
9:0	SLA	SW : RW Segment n lower address (based on parameter- up to 10-bits)

0x01401000+0x0100*n+4*m AFAB_FABRIC_m_WEIGHTING_REG_n, m=[0..5], n=[0..4]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

The values programmed into this register determine the Tier 2 weight for each master under the Tier Based Arbitration Scheme.

NOTE This register is required for each master and each slave segment supported by the FABRIC .

AFAB_FABRIC_m_WEIGHTING_REG_n

Bits	Name	Description
15:8	RESERVED_BITS_15_8	
7:0	M_M_W	SW : RW Master 'm' Weight

0x01402000+0x0100*n+4*m AFAB_FABRIC_m_QOS_REG_n, m=[0..3], n=[0..4]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

The values programmed into this register determine the Tier 1 weight for each master under the Tier Based Arbitration Scheme. Only 4 master ports can be configured as Tier 1. The QMC bits are used to configure a master port as Tier 1.

NOTE If more than one of these QOS Control registers are set to the same master port, unpredictable behavior will occur.

Set-up procedure:

1. Set the QOS enable bit.
2. Set the arbitration mode to Scheduled Access Time in the FABRIC arbitration configuration register FACR (See FABRIC_ARBITRATION_CONTROL_REG_n, n=[0..4]).
3. Configure the master port that needs to be set to Tier1.
4. Set the appropriate number of tokens/weight.
5. Set the MLT value (default is zero clock cycles).

NOTE Four of these registers are required for each slave segment supported by the FABRIC .

AFAB_FABRIC_m_QOS_REG_n

Bits	Name	Description
15:14	RESERVED_BITS15_13	
13:10	MLT	SW : RW MLT Value
9	QE	SW : RW QOS Enable

AFAB_FABRIC_m_QOS_REG_n (cont.)

Bits	Name	Description
8:4	QMC	SW : RW QOS Master Configuration 0x0: Master Port 0 0x1: Master Port 1 0x2: Master Port 2 0x3: Master Port 3 0x4: Master Port 4 0x5: Master Port 5 0x6: Master Port 6 0x7: Master Port 7 0x8: Master Port 8 0x9: Master Port 9 0xA: Master Port 10 0xB: Master Port 11 0xC: Master Port 12 0xD: Master Port 13 0xE: Master Port 14 0xF: Master Port 15 0x10: Master Port 16 0x11: Master Port 17 0x12: Master Port 18 0x13: Master Port 19 0x14: Master Port 20 0x15: Master Port 21 0x16: Master Port 22 0x17: Master Port 23 0x18: Master Port 24 0x19: Master Port 25 0x1A: Master Port 26 0x1B: Master Port 27 0x1C: Master Port 28 0x1D: Master Port 29 0x1E: Master Port 30 0x1F: Master Port 31
3:0	M_M_QW	SW : RW Master 'm' QOS Weight

0x01403000+4*n AFAB_FABRIC_BUS_INTERVAL_REG_n, n=[0..4]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register sets the bus interval value for Tier 2 masters.

NOTE A control register is implemented for each slave segment supported by the FABRIC .

AFAB_FABRIC_BUS_INTERVAL_REG_n

Bits	Name	Description
15:0	IBI	SW : RW Intct bus interval (in clock cycles)

0x01403100+4*n AFAB_FABRIC_QOS_INTERVAL_REG_n, n=[0..4]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register sets the QOS interval value for Tier 1 masters.

NOTE A control register is required for each slave segment supported by the FABRIC .

AFAB_FABRIC_QOS_INTERVAL_REG_n

Bits	Name	Description
15:8	RESERVED_BITS15_8	
7:0	QBI	SW : RW QOS bus interval (in clock cycles)

0x01403200+4*n AFAB_FABRIC_ARBITRATION_CONTROL_REG_n, n=[0..4]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x00FF

This register controls the arbitration mode and the pipeline depth of a particular slave segment.

NOTE A control register is implemented for each slave segment supported by the FABRIC .

AFAB_FABRIC_ARBITRATION_CONTROL_REG_n

Bits	Name	Description
15	QLP	SW : RW QOS Timer Low Power Mode 0x1: Enable 0x0: Disable
14:13	QHI	SW : RW QOS Timer Halt Interval 0x0: Stop after 1 interval of inactivity 0x1: Stop after 2 intervals of inactivity 0x2: Stop after 4 intervals of inactivity 0x3: Stop after 8 intervals of inactivity
12	BLP	SW : RW Bus Interval Low Power Mode 0x1: Enable 0x0: Disable
11:10	BHI	SW : RW Bus Interval Halt Interval 0x0: Stop after 1 interval of inactivity 0x1: Stop after 2 intervals of inactivity 0x2: Stop after 4 intervals of inactivity 0x3: Stop after 8 intervals of inactivity
9	QCE	SW : RW QoS Channel Enable 0x0: Disable (default) 0x1: Enable
8	IAM	SW : RW FABRIC arbitration mode 0x0: Fair round-robin (default) 0x1: Scheduled access time

AFAB_FABRIC_ARBITRATION_CONTROL_REG_n (cont.)

Bits	Name	Description
7:4	IRPD	SW : RW FABRIC read pipeline depth 0x0: Pipeline depth = 1 0x1: Pipeline depth = 2 0x2: Pipeline depth = 3 0x3: Pipeline depth = 4 0x4: Pipeline depth = 5 0x5: Pipeline depth = 6 0x6: Pipeline depth = 7 0x7: Pipeline depth = 8 0x8: Pipeline depth = 9 0x9: Pipeline depth = 10 0xA: Pipeline depth = 11 0xB: Pipeline depth = 12 0xC: Pipeline depth = 13 0xD: Pipeline depth = 14 0xE: Pipeline depth = 15 0xF: Pipeline depth = 16
3:0	IWPD	SW : RW FABRIC Write Pipeline Depth 0x0: Pipeline depth = 1 0x1: Pipeline depth = 2 0x2: Pipeline depth = 3 0x3: Pipeline depth = 4 0x4: Pipeline depth = 5 0x5: Pipeline depth = 6 0x6: Pipeline depth = 7 0x7: Pipeline depth = 8 0x8: Pipeline depth = 9 0x9: Pipeline depth = 10 0xA: Pipeline depth = 11 0xB: Pipeline depth = 12 0xC: Pipeline depth = 13 0xD: Pipeline depth = 14 0xE: Pipeline depth = 15 0xF: Pipeline depth = 16

0x01403300+4*n AFAB_FABRIC_MASTER_INTERFACE_REG_n, n=[0..5]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0084

This register controls the following master port attributes:

- whether the master request priority signals are used by the internal arbiter
- the redirection of cacheable coherent requests
- write gathering on AXI
- write packing on AHB

This register also controls a particular master's halt interface and for AHB master interfaces, it enables write packing functionality for posted writes.

When the MHR bit is set, the FABRIC_MnHALTREQ signal is asserted. The MHA and MHI fields capture the state of the FABRIC_MnHALTACK and FABRIC_MnIDLE signals at every clock cycle.

NOTE A register is implemented for each master interface supported by the FABRIC

AFAB_FABRIC_MASTER_INTERFACE_REG_n

Bits	Name	Description
15	RESERVED_BIT_15	
14	OWGM	SW : RW Enable optimized write gathering mode. SW should disable for AXI Ports
13	DBW	SW : RW Disable Bufferable writes. Treats Bufferable writes as Non Bufferable writes (AHB only)
12	PRIEN	SW : RW Enable Request Priority Lets the slave way arbiter consider the master request priority AREQPRIORITY[1:0] signal that is driven with each transaction
11	RCOSH	SW : RW Redirect Cacheable-outer-sharable Governs whether or not cacheable accesses that are outer-sharable are redirected to the Scorpion-MP L2 slave port
10	RCISH	SW : RW Redirect Cacheable-inner-sharable Governs whether or not cacheable accesses that are inner-sharable are redirected to the Scorpion-MP L2 slave port
9	RCNSH	SW : RW Redirect Cacheable-non-sharable Governs whether or not cacheable accesses that are non-sharable are redirected to the Scorpion-MP L2 slave port
8	CRE	SW : RW Enable redirection of cachable coherent requests

AFAB_FABRIC_MASTER_INTERFACE_REG_n (cont.)

Bits	Name	Description
7	WGE	SW : RW Write Gathering Enable (AXI only)
6	WPE	SW : RW Write Packing Enable (AHB Only) When enabled, the master port will pack indeterminate INCR burst writes, if disabled, the master port will break indeterminate INCR burst writes into SINGLES. 0x1: Enable 0x0: Disable
5:4	IIIW	SW : RW Bufferable Indeterminate INCR WR packing (AHB only): 0x0: break into INCR4 0x1: break into INCR8 0x3: break into INCR16
3	MID	SW : RW Master Interface Disable. SW diable of Master interface.
2	MI	SW : R Master Idle. Indicates that the Master does not have any pending bus transactions. For AHB busses, this bit is set internally by the FABRIC AHB Master port. For AXI masters, this value is driven by the master that is connected to the port.
1	MHA	SW : R Master halt acknowledge. Only valid for AXI masters. This bit is 0 on AHB master ports.
0	MHR	SW : RW Master halt request. Only valid for AXI masters. Writing this bit has no effect for AHB masters.

0x01403430 AFAB_FABRIC_SLAVE_ARBITRATION_DISABLE_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is RESERVED.

AFAB_FABRIC_SLAVE_ARBITRATION_DISABLE_REG

Bits	Name	Description
15	S15AD	SW : R RESERVED

AFAB_FABRIC_SLAVE_ARBITRATION_DISABLE_REG (cont.)

Bits	Name	Description
14	S14AD	SW : R RESERVED
13	S13AD	SW : R RESERVED
12	S12AD	SW : R RESERVED
11	S11AD	SW : R RESERVED
10	S10AD	SW : R RESERVED
9	S9AD	SW : R RESERVED
8	S8AD	SW : R RESERVED
7	S7AD	SW : R RESERVED
6	S6AD	SW : R RESERVED
5	S5AD	SW : R RESERVED
4	S4AD	SW : R RESERVED
3	S3AD	SW : R RESERVED
2	S2AD	SW : R RESERVED
1	S1AD	SW : R RESERVED
0	S0AD	SW : R RESERVED

0x01403434 AFAB_FABRIC_SLAVE_BYPASS_BUFFER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register enables the bypass buffer functionality in a slave way (if implemented).

AFAB_FABRIC_SLAVE_BYPASS_BUFFER_REG

Bits	Name	Description
15	S15BE	SW : RW Slave 15 Bypass Buffer Enable
14	S14BE	SW : RW Slave 14 Bypass Buffer Enable
13	S13BE	SW : RW Slave 13 Bypass Buffer Enable
12	S12BE	SW : RW Slave 12 Bypass Buffer Enable
11	S11BE	SW : RW Slave 11 Bypass Buffer Enable
10	S10BE	SW : RW Slave 10 Bypass Buffer Enable
9	S9BE	SW : RW Slave 9 Bypass Buffer Enable
8	S8BE	SW : RW Slave 8 Bypass Buffer Enable
7	S7BE	SW : RW Slave 7 Bypass Buffer Enable
6	S6BE	SW : RW Slave 6 Bypass Buffer Enable
5	S5BE	SW : RW Slave 5 Bypass Buffer Enable
4	S4BE	SW : RW Slave 4 Bypass Buffer Enable
3	S3BE	SW : RW Slave 3 Bypass Buffer Enable
2	S2BE	SW : RW Slave 2 Bypass Buffer Enable
1	S1BE	SW : RW Slave 1 Bypass Buffer Enable
0	S0BE	SW : RW Slave 0 Bypass Buffer Enable

0x01403438 AFAB_FABRIC_SLAVE_STATUS_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the status of each slave.

- A 1 indicates that the slave is idle.
- A 0 indicates that the slave is busy processing a transfer and/or the FABRIC has not completed sending transactions to the slave.

AFAB_FABRIC_SLAVE_STATUS_REG

Bits	Name	Description
15	S15S	SW : R Slave 15 Status
14	S14S	SW : R Slave 14 Status
13	S13S	SW : R Slave 13 Status
12	S12S	SW : R Slave 12 Status
11	S11S	SW : R Slave 11 Status
10	S10S	SW : R Slave 10 Status
9	S9S	SW : R Slave 9 Status
8	S8S	SW : R Slave 8 Status
7	S7S	SW : R Slave 7 Status
6	S6S	SW : R Slave 6 Status
5	S5S	SW : R Slave 5 Status
4	S4S	SW : R Slave 4 Status
3	S3S	SW : R Slave 3 Status

AFAB_FABRIC_SLAVE_STATUS_REG (cont.)

Bits	Name	Description
2	S2S	SW : R Slave 2 Status
1	S1S	SW : R Slave 1 Status
0	S0S	SW : R Slave 0 Status

0x01403500 AFAB_FABRIC_TEST_INTERFACE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls:

- the grouping of signals that are driven out on the test bus (FABRIC_TESTBUS[31:0])
- Selection of MISR slave way and channel input

MEN: Selects which MISR output is driven onto the test-bus. For example, setting MEN to 00010 selects the MISR in slave segment 2. The MEN bits are only valid when the testmode (TMODE) is set to 000000 and test-enable is set (TEN)

TMODE: Selects the various test-bus modes

TEN: Test-enable. Must be set for values to be driven onto the test-bus OR for MISR to be enabled.

AFAB_FABRIC_TEST_INTERFACE_REG

Bits	Name	Description
15:14	RESERVED_BITS15_14	
13:12	MSEL	SW : RW MISR input selection: 0x0: Address channel 0x1: Write channel 0x2: Read channel 0x3: Write response channel

AFAB_FABRIC_TEST_INTERFACE_REG (cont.)

Bits	Name	Description
11:7	MEN	SW : RW MISR Enable 0x1: Slave Segment 0 0x2: Slave Segment 1 0x3: Slave Segment 2 0x4: Slave Segment 3 0x5: Slave Segment 4 0x6: Slave Segment 5 0x7: Slave Segment 6 0x8: Slave Segment 7 0x9: Slave Segment 8 0xA: Slave Segment 9 0xB: Slave Segment 10 0xC: Slave Segment 11 0xD: Slave Segment 12 0xE: Slave Segment 13 0xF: Slave Segment 14 0x10: Slave Segment 15

AFAB_FABRIC_TEST_INTERFACE_REG (cont.)

Bits	Name	Description
6:1	TMODE	SW : RW Test Mode: 0x0: Testbus M0 0x1: Testbus M1 0x2: Testbus M2 0x3: Testbus M3 0x4: Testbus M4 0x5: Testbus M5 0x6: Testbus M6 0x7: Testbus M7 0x8: Testbus M8 0x9: Testbus M9 0xA: Testbus M10 0xB: Testbus M11 0xC: Testbus M12 0xD: Testbus M13 0xE: Testbus M14 0xF: Testbus M15 0x10: Testbus M16 0x11: Testbus M17 0x12: Testbus M18 0x13: Testbus M19 0x14: Testbus M20 0x15: Testbus M21 0x16: Testbus M22 0x17: Testbus M23 0x18: Testbus M24 0x19: Testbus M25 0x1A: Testbus M26 0x1B: Testbus M27 0x1C: Testbus M28 0x1D: Testbus M29 0x1E: Testbus M30 0x1F: Testbus M31 0x20: Testbus S0 0x21: Testbus S1 0x22: Testbus S2 0x23: Testbus S3 0x24: Testbus S4 0x25: Testbus S5 0x26: Testbus S6 0x27: Testbus S7 0x28: Testbus S8 0x29: Testbus S9 0x2A: Testbus S10 0x2B: Testbus S11 0x2C: Testbus S12

AFAB_FABRIC_TEST_INTERFACE_REG (cont.)

Bits	Name	Description
6:1	TMODE (CONT'D)	0x2D: Testbus S13 0x2E: Testbus S14 0x2F: Testbus S15 0x30: Reserved_1 0x31: Reserved_2 0x32: Reserved_3 0x33: Reserved_4 0x34: Reserved_5 0x35: Reserved_6 0x36: Reserved_7 0x37: Reserved_8 0x38: Reserved_9 0x39: Reserved_10 0x3A: Reserved_11 0x3B: Reserved_12 0x3C: Reserved_13 0x3D: Reserved_14 0x3E: Reserved_15 0x3F: Reserved_16
0	TEN	SW : RW Test Enable

0x01403504 AFAB_FABRIC_ERROR_STATUS_REG_0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCRis set to one (See FABRIC_CONFIGURATION_REG).

AFAB_FABRIC_ERROR_STATUS_REG_0

Bits	Name	Description
15:0	MID	SW : R AMID for AXI port HMID for AHB port

0x01403508 AFAB_FABRIC_ERROR_STATUS_REG_1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

AFAB_FABRIC_ERROR_STATUS_REG_1

Bits	Name	Description
15:8	TID	SW : R Transaction ID Only Applicable for AXI Transfers ZERO for AHB Transfers
7:6	RESERVED_BITS_7_6	Reserved
5:0	MPORT	SW : R Master port that generated the error

0x0140350C AFAB_FABRIC_ERROR_STATUS_REG_2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

AFAB_FABRIC_ERROR_STATUS_REG_2

Bits	Name	Description
15:12	RESERVED_BITS_15_12	Reserved
11	BURST	SW : R Burst transfer
10	OOOWR	SW : R OOO write response Only Applicable for AXI
9	OOORD	SW : R OOO read response Only Applicable for AXI

AFAB_FABRIC_ERROR_STATUS_REG_2 (cont.)

Bits	Name	Description
8:7	LOCK	SW : R Lock Transfer
6:4	SIZE	SW : R Transfer Size
3:0	TYPE	SW : R Transfer Type Only Applicable for AXI

0x01403510 AFAB_FABRIC_ERROR_STATUS_REG_3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

AFAB_FABRIC_ERROR_STATUS_REG_3

Bits	Name	Description
15:8	RESERVED_BITS_15_8	Reserved
7	PROTNS	SW : R APROTNS/HPROTNS
6	PROTIND	SW : R PROTIND
5	AISH	SW : R Inner Shared
4	WRITE	SW : R Write transfer
3:0	LEN	SW : R Transfer Length

0x01403514 AFAB_FABRIC_ERROR_UPPER_ADDR_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address of the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

AFAB_FABRIC_ERROR_UPPER_ADDR_REG

Bits	Name	Description
15:0	EUA	SW : R Bits [31:16] of the address which generated a decode error

0x01403518 AFAB_FABRIC_ERROR_LOWER_ADDR_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address of the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

AFAB_FABRIC_ERROR_LOWER_ADDR_REG

Bits	Name	Description
15:0	ELR	SW : R Bits [15:0] of the address which generated a decode error

0x0140351C AFAB_FABRIC_MISR_SIGNATURE_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG.

AFAB_FABRIC_MISR_SIGNATURE_REG0

Bits	Name	Description
15:0	SIG0	SW : R Bits [15:0] of 64-bit MISR signature

0x01403520 AFAB_FABRIC_MISR_SIGNATURE_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG

AFAB_FABRIC_MISR_SIGNATURE_REG1

Bits	Name	Description
15:0	SIG1	SW : R Bits [31:16] of 64-bit MISR signature

0x01403524 AFAB_FABRIC_MISR_SIGNATURE_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 47:32 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG.

AFAB_FABRIC_MISR_SIGNATURE_REG2

Bits	Name	Description
15:0	SIG2	SW : R Bits [47:32] of 64-bit MISR signature

0x01403528 AFAB_FABRIC_MISR_SIGNATURE_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 63:48 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG.

AFAB_FABRIC_MISR_SIGNATURE_REG3

Bits	Name	Description
15:0	SIG3	SW : R Bits [63:48] of 64-bit MISR signature

0x0140352C AFAB_FTMR_TESTBUS_MODE_REGISTER

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

For the testbus selected of master or slave port in FABRIC_TEST_INTERFACE_REG, user can program the testbus mode via this register.

AFAB_FTMR_TESTBUS_MODE_REGISTER

Bits	Name	Description
15:3	RESERVED_BITS15_3	Reserved
2:0	MODE	0x0: Default Mode 0x1: Address channel attributes at the interface 0x2: Address at the interface 0x3: Misc 0x4: Write data Lower 32 bits at interface 0x5: Write data Upper 32 bits at interface 0x6: Read data Lower 32 bits at interface 0x7: Read data Upper 32 bits at interface

0x01403600+4*n AFAB_FABRIC_MASTER_CLOCK_HALT_REG_n, n=[0..5]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt & change functionality within the FABRIC master ports. To enable the clock halting functionality, the clock halt enable bit (CHTEN) needs to be set. The hysteresis timer value is a 10-bit timer (running on FCLK) value that is set using the CHTMR bits.

NOTE The register bits related to clock mode changing that exist in other fabrics are disabled in this fabric, in order to increase performance. These bits are marked as reserved and should not be modified by software.

NOTE A register is implemented for each master interface supported by the FABRIC .

AFAB_FABRIC_MASTER_CLOCK_HALT_REG_n

Bits	Name	Description
15	CHTEN	SW : RW Clock halt enable. Enables clock halt functionality for this port.
14	CCDONE	SW : RW RESERVED
13	CCACK	SW : R RESERVED
12	CCREQ	SW:RW RESERVED
11:10	MODE	SW : RW Reserved - Master clock interface mode SOFTWARE SHOULD NOT MODIFY THIS FIELD. 0x0: ASYNC 0x1: SYNC 0x2: ISOSYNC port clk slower 0x3: ISOSYNC port clk faster.
9:0	CHTMR	SW : RW Master clock halt timer: clock cycles of inactivity that should pass before clock is halted

0x01403800+4*n AFAB_FABRIC_SLAVE_CLOCK_HALT_REG_n, n=[0..4]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt & change functionality within the FABRIC slave ways. To enable the clock halting functionality, the clock halt enable bit (CHTEN) needs to be set. The hysteresis timer value is a 10-bit timer (running on FCLK) value that is set using the CHTMR bits.

NOTE The register bits related to clock mode changing that exist in other fabrics are disabled in this fabric, in order to increase performance. These bits are marked as reserved and should not be modified by software.

NOTE A register is implemented for each slave interface supported by the FABRIC .

AFAB_FABRIC_SLAVE_CLOCK_HALT_REG_n

Bits	Name	Description
15	CHTEN	SW : RW Clock halt enable. Enables clock halt functionality for this port.

AFAB_FABRIC_SLAVE_CLOCK_HALT_REG_n (cont.)

Bits	Name	Description
14	CCDONE	SW : RW Reserved
13	CCACK	SW : RW Reserved
12	CCREQ	SW : RW Reserved
11:10	MODE	SW : RW Reserved - Slave clock interface mode - Software should not modify this field 0x0: ASYNC 0x1: SYNC 0x2: ISOSYNC port clk slower. 0x3: ISOSYNC port clk faster.
9:0	CHTMR	SW : RW Slave clock halt timer: clock cycles of inactivity that should pass before clock is halted

0x01403880 AFAB_FABRIC_SLAVE_ARBITER_CLOCK_HALT_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt functionality within the FABRIC slave ways arbiter.

AFAB_FABRIC_SLAVE_ARBITER_CLOCK_HALT_REG

Bits	Name	Description
15	S15CHTEN	SW : RW S15 Arbiter Clock halt enable.
14	S14CHTEN	SW : RW S14 Arbiter Clock halt enable.
13	S13CHTEN	SW : RW S13 Arbiter Clock halt enable.
12	S12CHTEN	SW : RW S12 Arbiter Clock halt enable.
11	S11CHTEN	SW : RW S11 Arbiter Clock halt enable.
10	S10CHTEN	SW : RW S10 Arbiter Clock halt enable.

AFAB_FABRIC_SLAVE_ARBITER_CLOCK_HALT_REG (cont.)

Bits	Name	Description
9	S9CHTEN	SW : RW S9 Arbiter Clock halt enable.
8	S8CHTEN	SW : RW S8 Arbiter Clock halt enable.
7	S7CHTEN	SW : RW S7 Arbiter Clock halt enable.
6	S6CHTEN	SW : RW S6 Arbiter Clock halt enable.
5	S5CHTEN	SW : RW S5 Arbiter Clock halt enable.
4	S4CHTEN	SW : RW S4 Arbiter Clock halt enable.
3	S3CHTEN	SW : RW S3 Arbiter Clock halt enable.
2	S2CHTEN	SW : RW S2 Arbiter Clock halt enable.
1	S1CHTEN	SW : RW S1 Arbiter Clock halt enable.
0	S0CHTEN	SW : RW S0 Arbiter Clock halt enable.

0x01403884+4*n AFAB_FABRIC_SLAVE_CLOCK_ON_CFG_REG_n, n=[0..4]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to set wake-up timer values during HW clock gating functionality for the Fabric slave ways arbiter and AHB/AXI slaves connected to Fabric.

AFAB_FABRIC_SLAVE_CLOCK_ON_CFG_REG_n

Bits	Name	Description
15:4	RESERVED_BITS_15_4	Reserved
3:0	COD	SW : RW Slave Way Clock On Delay)

0x014038F8 AFAB_FABRIC_MONITOR_ENABLE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the trigger selection and enabling of event and cycle counters.

NOTE When PTRIG is set to use any of the external trigger signals, the external triggers incur a 2 cycle delay from the positive edge assertion of the signal to when the actual counters are enabled in the performance monitor. This allows synchronization of the external signals into the FABRIC clock domain.

AFAB_FABRIC_MONITOR_ENABLE_REG

Bits	Name	Description
15:13	PTRIG	SW : RW 0x5: Manual Enable/ Manual Disable 0x4: Int Trig/Ext Trig 0x3: Ext Trig 0x2: Ext Trig/CC expire 0x1: Int Trig/CC expire 0x0: Manual enable/CC expire (No trigger)
12	ECC	SW : RW Enable cycle counter
11:8	RESERVED_BITS_11_8	Reserved
7	EEC7	SW : RW Enable event counter 7
6	EEC6	SW : RW Enable event counter 6
5	EEC5	SW : RW Enable event counter 5
4	EEC4	SW : RW Enable event counter 4
3	EEC3	SW : RW Enable event counter 3
2	EEC2	SW : RW Enable event counter 2
1	EEC1	SW : RW Enable event counter 1
0	EEC0	SW : RW Enable event counter 0

0x014038FC AFAB_FABRIC_MONITOR_RESET_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the resets for event and cycle counters.

AFAB_FABRIC_MONITOR_RESET_REG

Bits	Name	Description
15:8	RESERVED_BITS_15_8	Reserved
7	REC7	SW : RW Reset event counter 7 (automatically resets the cycle-counter as well)
6	REC6	SW : RW Reset event counter 6 (automatically resets the cycle-counter as well)
5	REC5	SW : RW Reset event counter 5 (automatically resets the cycle-counter as well)
4	REC4	SW : RW Reset event counter 4 (automatically resets the cycle-counter as well)
3	REC3	SW : RW Reset event counter 3 (automatically resets the cycle-counter as well)
2	REC2	SW : RW Reset event counter 2 (automatically resets the cycle-counter as well)
1	REC1	SW : RW Reset event counter 1 (automatically resets the cycle-counter as well)
0	REC0	SW : RW Reset event counter 0 (automatically resets the cycle-counter as well)

0x01403900 AFAB_FABRIC_MONITOR_TENURE_ENABLE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the trigger selection and enabling of tenure counters.

NOTE When PTRIG is set to use any of the external trigger signals, the external triggers incur a 2 cycle delay from the positive edge assertion of the signal to when the actual counters are enabled in the performance monitor. This allows synchronization of the external signals into the FABRIC clock domain.

AFAB_FABRIC_MONITOR_TENURE_ENABLE_REG

Bits	Name	Description
15:5	RESERVED_BITS_15_5	Reserved
4	ETTF	SW : RW Enable tenure table fix This bit, when set, enables a the following feature: The tenure table for each tenure counter will track atleast 16 tenures properly without overflowing.
3	ETC3	SW : RW Enable tenure counter 3
2	ETC2	SW : RW Enable tenure counter 2
1	ETC1	SW : RW Enable tenure counter 1
0	ETC0	SW : RW Enable tenure counter 0

0x01403904 AFAB_FABRIC_MONITOR_TENURE_RESET_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the resets for tenure counters and cycle counters.

AFAB_FABRIC_MONITOR_TENURE_RESET_REG

Bits	Name	Description
15:4	RESERVED_BITS_15_4	Reserved
3	RTC3	SW : RW Reset tenure counter 3 (automatically resets the cycle-counter as well)
2	RTC2	SW : RW Reset tenure counter 2 (automatically resets the cycle-counter as well)

AFAB_FABRIC_MONITOR_TENURE_RESET_REG (cont.)

Bits	Name	Description
1	RTC1	SW : RW Reset tenure counter 1 (automatically resets the cycle-counter as well)
0	RTC0	SW : RW Reset tenure counter 0 (automatically resets the cycle-counter as well)

0x01403908 AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 0.

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG0

Bits	Name	Description
15:13	E0ES	SW : RW Event counter 0 event selection 0x0: Read burst 0 (Master/slave) 0x1: Write burst 0 (Master/slave) 0x2: Address transfer count 0 (Master/slave) 0x3: Read transfer count 0 (Master/slave) 0x4: Write transfer count 0 (Master/slave) 0x5: Write (bufferable burst 0 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E0MIDFEN	SW : RW Event counter 0 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E0INDFEN	SW : RW Event counter 0 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E0IND	SW : RW Event counter 0 Instruction/Data selection 0x0: Data 0x1: Instruction

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
8:4	E0MPS	SW : RW Event counter 0 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
3:0	E0SWS	SW : RW Event counter 0 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0140390C AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 0.

AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG0

Bits	Name	Description
15:0	E0MID	SW : RW Event counter 0 MID selection (If MID filtering enabled)

0x01403910 AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 1.

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG1

Bits	Name	Description
15:13	E1ES	SW : RW Event counter 1event selection 0x0: Read burst 1 (Master/slave) 0x1: Write burst 1 (Master/slave) 0x2: Address transfer count 1 (Master/slave) 0x3: Read transfer count 1 (Master/slave) 0x4: Write transfer count 1 (Master/slave) 0x5: Write (bufferable burst 1 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E1MIDFEN	SW : RW Event counter 1 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E1INDFEN	SW : RW Event counter 1Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E1IND	SW : RW Event counter 1Instruction/Data selection 0x0: Data 0x1: Instruction

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
8:4	E1MPS	SW : RW Event counter 1Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
3:0	E1SWS	SW : RW Event counter 1Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01403914 AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 1.

AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG1

Bits	Name	Description
15:0	E1MID	SW : RW Event counter 1MID selection (If MID filtering enabled)

0x01403918 AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 2.

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG2

Bits	Name	Description
15:13	E2ES	SW : RW Event counter 2event selection 0x0: Read burst 2 (Master/slave) 0x1: Write burst 2 (Master/slave) 0x2: Address transfer count 2 (Master/slave) 0x3: Read transfer count 2 (Master/slave) 0x4: Write transfer count 2 (Master/slave) 0x5: Write (bufferable burst 2 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E2MIDFEN	SW : RW Event counter 2MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E2INDFEN	SW : RW Event counter 2Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E2IND	SW : RW Event counter 2Instruction/Data selection 0x0: Data 0x1: Instruction

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
8:4	E2MPS	SW : RW Event counter 2Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
3:0	E2SWS	SW : RW Event counter 2Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0140391C AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 2.

AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG2

Bits	Name	Description
15:0	E2MID	SW : RW Event counter 2 MID selection (If MID filtering enabled)

0x01403920 AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 3.

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG3

Bits	Name	Description
15:13	E3ES	SW : RW Event counter 3event selection 0x0: Read burst 3 (Master/slave) 0x1: Write burst 3 (Master/slave) 0x2: Address transfer count 3 (Master/slave) 0x3: Read transfer count 3 (Master/slave) 0x4: Write transfer count 3 (Master/slave) 0x5: Write (bufferable burst 3 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E3MIDFEN	SW : RW Event counter 3MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E3INDFEN	SW : RW Event counter 3Instruction/Data Filtering enable 0x0: Disabled 0x1: Enable
9	E3IND	SW : RW Event counter 3Instruction/Data selection 0x0: Data 0x1: Instruction

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
8:4	E3MPS	SW : RW Event counter 3Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
3:0	E3SWS	SW : RW Event counter 3 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01403924 AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 3.

AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG3

Bits	Name	Description
15:0	E3MID	SW : RW Event counter 3 MID selection (If MID filtering enabled)

0x01403928 AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 4.

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG4

Bits	Name	Description
15:13	E4ES	SW : RW Event counter 4event selection 0x0: Read burst 4 (Master/slave) 0x1: Write burst 4 (Master/slave) 0x2: Address transfer count 4 (Master/slave) 0x3: Read transfer count 4 (Master/slave) 0x4: Write transfer count 4 (Master/slave) 0x5: Write (bufferable burst 4AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	SEL_SPDM_OUT0	SW : RW 0x0: Send total tenure overflow info (for tenure counter 0 to SPDM) 0x1: Send individual counter overflow info (for tenure counter 0 to SPDM)
11	E4MIDFEN	SW : RW Event counter 4 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E4INDFEN	SW : RW Event counter 4 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E4IND	SW : RW Event counter 4 Instruction/Data selection 0x0: Data 0x1: Instruction

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG4 (cont.)

Bits	Name	Description
8:4	E4MPS	SW : RW Event counter 4 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG4 (cont.)

Bits	Name	Description
3:0	E4SWS	SW : RW Event counter 4 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0140392C AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 4.

AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG4

Bits	Name	Description
15:0	E4MID	SW : RW Event counter 4 MID selection (If MID filtering enabled)

0x01403930 AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 5.

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG5

Bits	Name	Description
15:13	E5ES	SW : RW Event counter 5 event selection 0x0: Read burst 5 (Master/slave) 0x1: Write burst 5 (Master/slave) 0x2: Address transfer count 5 (Master/slave) 0x3: Read transfer count 5 (Master/slave) 0x4: Write transfer count 5 (Master/slave) 0x5: Write (bufferable burst 5 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	SEL_SPDM_OUT1	SW : RW 0x0: Send total tenure overflow info (for tenure counter 1 to SPDM) 0x1: Send individual counter overflow info (for tenure counter 1 to SPDM)
11	E5MIDFEN	SW : RW Event counter 5 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E5INDFEN	SW : RW Event counter 5 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E5IND	SW : RW Event counter 5 Instruction/Data selection 0x0: Data 0x1: Instruction

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG5 (cont.)

Bits	Name	Description
8:4	E5MPS	SW : RW Event counter 5 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG5 (cont.)

Bits	Name	Description
3:0	E5SWS	SW : RW Event counter 5 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01403934 AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 5.

AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG5

Bits	Name	Description
15:0	E5MID	SW : RW Event counter 5 MID selection (If MID filtering enabled)

0x01403938 AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 6.

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG6

Bits	Name	Description
15:13	E6ES	SW : RW Event counter 6 event selection 0x0: Read burst 6 (Master/slave) 0x1: Write burst 6 (Master/slave) 0x2: Address transfer count 6 (Master/slave) 0x3: Read transfer count 6 (Master/slave) 0x4: Write transfer count 6 (Master/slave) 0x5: Write (bufferable burst 6 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	SEL_SPDM_OUT2	SW : RW 0x0: Send total tenure overflow info (for tenure counter 2 to SPDM) 0x1: Send individual counter overflow info (for tenure counter 2 to SPDM)
11	E6MIDFEN	SW : RW Event counter 6 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E6INDFEN	SW : RW Event counter 6 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E6IND	SW : RW Event counter 6 Instruction/Data selection 0x0: Data 0x1: Instruction

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG6 (cont.)

Bits	Name	Description
8:4	E6MPS	SW : RW Event counter 6 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG6 (cont.)

Bits	Name	Description
3:0	E6SWS	SW : RW Event counter 6 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0140393C AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 6.

AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG6

Bits	Name	Description
15:0	E6MID	SW : RW Event counter 6 MID selection (If MID filtering enabled)

0x01403940 AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 7.

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG7

Bits	Name	Description
15:13	E7ES	SW : RW Event counter 7 event selection 0x0: Read burst 7 (Master/slave) 0x1: Write burst 7 (Master/slave) 0x2: Address transfer count 7 (Master/slave) 0x3: Read transfer count 7 (Master/slave) 0x4: Write transfer count 7 (Master/slave) 0x5: Write (bufferable burst 7 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	SEL_SPDM_OUT3	SW : RW 0x0: Send total tenure overflow info (for tenure counter 3 to SPDM) 0x1: Send individual counter overflow info (for tenure counter 3 to SPDM)
11	E7MIDFEN	SW : RW Event counter 7 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E7INDFEN	SW : RW Event counter 7 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E7IND	SW : RW Event counter 7 Instruction/Data selection 0x0: Data 0x1: Instruction

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG7 (cont.)

Bits	Name	Description
8:4	E7MPS	SW : RW Event counter 7 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

AFAB_FABRIC_MONITOR_SELECTION_LOWER_REG7 (cont.)

Bits	Name	Description
3:0	E7SWS	SW : RW Event counter 7 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01403944 AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 7.

AFAB_FABRIC_MONITOR_SELECTION_UPPER_REG7

Bits	Name	Description
15:0	E7MID	SW : RW Event counter 7 MID selection (If MID filtering enabled)

0x01403948 AFAB_FABRIC_MONITOR_PICK_PORTS_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the main port and other port selection for the 8 event counters.

AFAB_FABRIC_MONITOR_PICK_PORTS_REG

Bits	Name	Description
15:14	E7PP	SW : RW Event counter 7 port combination selection 0x0: Master port selected by E7MPS, filtering based on slave port disabled 0x1: Master port selected by E7MPS, filtering based on slave way selected by E7SWS 0x2: Slave way selected by E7SWS, filtering based on master port disabled 0x3: Slave way selected by E7SWS, filtering based on master port selected by E7MPS
13:12	E6PP	SW : RW Event counter 6 port combination selection 0x0: Master port selected by E6MPS, filtering based on slave port disabled 0x1: Master port selected by E6MPS, filtering based on slave way selected by E6SWS 0x2: Slave way selected by E6SWS, filtering based on master port disabled 0x3: Slave way selected by E6SWS, filtering based on master port selected by E6MPS
11:10	E5PP	SW : RW Event counter 5 port combination selection 0x0: Master port selected by E5MPS, filtering based on slave port disabled 0x1: Master port selected by E5MPS, filtering based on slave way selected by E5SWS 0x2: Slave way selected by E5SWS, filtering based on master port disabled 0x3: Slave way selected by E5SWS, filtering based on master port selected by E5MPS
9:8	E4PP	SW : RW Event counter 4 port combination selection 0x0: Master port selected by E4MPS, filtering based on slave port disabled 0x1: Master port selected by E4MPS, filtering based on slave way selected by E4SWS 0x2: Slave way selected by E4SWS, filtering based on master port disabled 0x3: Slave way selected by E4SWS, filtering based on master port selected by E4MPS

AFAB_FABRIC_MONITOR_PICK_PORTS_REG (cont.)

Bits	Name	Description
7:6	E3PP	SW : RW Event counter 3 port combination selection 0x0: Master port selected by E3MPS, filtering based on slave port disabled 0x1: Master port selected by E3MPS, filtering based on slave way selected by E3SWS 0x2: Slave way selected by E3SWS, filtering based on master port disabled 0x3: Slave way selected by E3SWS, filtering based on master port selected by E3MPS
5:4	E2PP	SW : RW Event counter 2 port combination selection 0x0: Master port selected by E2MPS, filtering based on slave port disabled 0x1: Master port selected by E2MPS, filtering based on slave way selected by E2SWS 0x2: Slave way selected by E2SWS, filtering based on master port disabled 0x3: Slave way selected by E2SWS, filtering based on master port selected by E2MPS
3:2	E1PP	SW : RW Event counter 1 port combination selection 0x0: Master port selected by E1MPS, filtering based on slave port disabled 0x1: Master port selected by E1MPS, filtering based on slave way selected by E1SWS 0x2: Slave way selected by E1SWS, filtering based on master port disabled 0x3: Slave way selected by E1SWS, filtering based on master port selected by E1MPS
1:0	E0PP	SW : RW Event counter 0 port combination selection 0x0: Master port selected by E0MPS, filtering based on slave port disabled 0x1: Master port selected by E0MPS, filtering based on slave way selected by E0SWS 0x2: Slave way selected by E0SWS, filtering based on master port disabled 0x3: Slave way selected by E0SWS, filtering based on master port selected by E0MPS

0x01403950 AFAB_FABRIC_MONITOR_CYCLE_COUNT_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the performance monitor cycle counter.

AFAB_FABRIC_MONITOR_CYCLE_COUNT_UPPER_REG

Bits	Name	Description
15:0	UCC	SW : RW MSB cycle count value The cycle count value is decremented once per FABRIC clock. The counter stops decrementing once the CC value equals 32:h0.

0x01403954 AFAB_FABRIC_MONITOR_CYCLE_COUNT_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the performance monitor cycle counter. If SW requires that the values when read do not change, when it reads this register, the value for all 32 bits of the cycle counter is stored. This allows for SW to read the lower reg and have the value match the exact cycle in which the upper reg was read.

AFAB_FABRIC_MONITOR_CYCLE_COUNT_LOWER_REG

Bits	Name	Description
15:0	LCC	SW : RW LSB cycle count value The cycle count value is decremented once per FABRIC clock. The counter stops decrementing once the CC value equals 32:h0.

0x01403958 AFAB_FABRIC_MONITOR_EVENT_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 0. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_LOWER_REG0

Bits	Name	Description
15:0	ECLT0	SW : RW Total events (lower 16-bit value)

0x0140395C AFAB_FABRIC_MONITOR_EVENT_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 0. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_UPPER_REG0

Bits	Name	Description
15:0	ECUT0	SW : RW Total events (upper 16-bit value)

0x01403960 AFAB_FABRIC_MONITOR_EVENT_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 1. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_LOWER_REG1

Bits	Name	Description
15:0	ECLT1	SW : RW Total events (lower 16-bit value)

0x01403964 AFAB_FABRIC_MONITOR_EVENT_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 1. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_UPPER_REG1

Bits	Name	Description
15:0	ECUT1	SW : RW Total events (upper 16-bit value)

0x01403968 AFAB_FABRIC_MONITOR_EVENT_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 2. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_LOWER_REG2

Bits	Name	Description
15:0	ECLT2	SW : RW Total events (lower 16-bit value)

0x0140396C AFAB_FABRIC_MONITOR_EVENT_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 2. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_UPPER_REG2

Bits	Name	Description
15:0	ECUT2	SW : RW Total events (upper 16-bit value)

0x01403970 AFAB_FABRIC_MONITOR_EVENT_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 3. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_LOWER_REG3

Bits	Name	Description
15:0	ECLT3	SW : RW Total events (lower 16-bit value)

0x01403974 AFAB_FABRIC_MONITOR_EVENT_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 3. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_UPPER_REG3

Bits	Name	Description
15:0	ECUT3	SW : RW Total events (upper 16-bit value)

0x01403978 AFAB_FABRIC_MONITOR_EVENT_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 4. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_LOWER_REG4

Bits	Name	Description
15:0	ECLT4	SW : RW Total events (lower 16-bit value)

0x0140397C AFAB_FABRIC_MONITOR_EVENT_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 4. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_UPPER_REG4

Bits	Name	Description
15:0	ECUT4	SW : RW Total events (upper 16-bit value)

0x01403980 AFAB_FABRIC_MONITOR_EVENT_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 5. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_LOWER_REG5

Bits	Name	Description
15:0	ECLT5	SW : RW Total events (lower 16-bit value)

0x01403984 AFAB_FABRIC_MONITOR_EVENT_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 5. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_UPPER_REG5

Bits	Name	Description
15:0	ECUT5	SW : RW Total events (upper 16-bit value)

0x01403988 AFAB_FABRIC_MONITOR_EVENT_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 6. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_LOWER_REG6

Bits	Name	Description
15:0	ECLT6	SW : RW Total events (lower 16-bit value)

0x0140398C AFAB_FABRIC_MONITOR_EVENT_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 6. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_UPPER_REG6

Bits	Name	Description
15:0	ECUT6	SW : RW Total events (upper 16-bit value)

0x01403990 AFAB_FABRIC_MONITOR_EVENT_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 7. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_LOWER_REG7

Bits	Name	Description
15:0	ECLT7	SW : RW Total events (lower 16-bit value)

0x01403994 AFAB_FABRIC_MONITOR_EVENT_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 7. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_UPPER_REG7

Bits	Name	Description
15:0	ECUT7	SW : RW Total events (upper 16-bit value)

0x014039A4 AFAB_FABRIC_TRIGGER_CONFIGURATION_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register configures the interface in which the trigger comparison is done on the address channel. TAMS: Selects one of the 32 interfaces from which the address channel transfer qualifiers are used to enable trigger matching.

AFAB_FABRIC_TRIGGER_CONFIGURATION_REG

Bits	Name	Description
15:7	RESERVED_BITS15_6	
6	TRGEN	SW : RW Trigger enable 1'b0 -disabled 0x1: enabled

AFAB_FABRIC_TRIGGER_CONFIGURATION_REG (cont.)

Bits	Name	Description
5:0	TAMS	SW : RW Trigger based on address channel on M/S Port #: 0x0: Master Port 0 0x1: Master Port 1 0x2: Master Port 2 0x3: Master Port 3 0x4: Master Port 4 0x5: Master Port 5 0x6: Master Port 6 0x7: Master Port 7 0x8: Master Port 8 0x9: Master Port 9 0xA: Master Port 10 0xB: Master Port 11 0xC: Master Port 12 0xD: Master Port 13 0xE: Master Port 14 0xF: Master Port 15 0x10: Master Port 16 0x11: Master Port 17 0x12: Master Port 18 0x13: Master Port 19 0x14: Master Port 20 0x15: Master Port 21 0x16: Master Port 22 0x17: Master Port 23 0x18: Master Port 24 0x19: Master Port 25 0x1A: Master Port 26 0x1B: Master Port 27 0x1C: Master Port 28 0x1D: Master Port 29 0x1E: Master Port 30 0x1F: Master Port 31 0x20: Slave Port 0 0x21: Slave Port 1 0x22: Slave Port 2 0x23: Slave Port 3 0x24: Slave Port 4 0x25: Slave Port 5 0x26: Slave Port 6 0x27: Slave Port 7 0x28: Slave Port 8 0x29: Slave Port 9 0x2A: Slave Port 10 0x2B: Slave Port 11 0x2C: Slave Port 12

AFAB_FABRIC_TRIGGER_CONFIGURATION_REG (cont.)

Bits	Name	Description
5:0	TAMS (CONT'D)	0x2D: Slave Port 13 0x2E: Slave Port 14 0x2F: Slave Port 15

0x014039AC AFAB_FABRIC_TRIGGER_REG_0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the upper address which is used as comparison for the trigger feature of the on-chip trace or performance monitor function. TUADDR[15:0] will be compared against Address[31:16].

AFAB_FABRIC_TRIGGER_REG_0

Bits	Name	Description
15:0	TUADDR	SW : RW Address bits[31:16]

0x014039B0 AFAB_FABRIC_TRIGGER_REG_1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the lower address which is used as comparison for the trigger feature of the performance monitor function. TLADDR[15:0] will be compared against Address[15:0].

AFAB_FABRIC_TRIGGER_REG_1

Bits	Name	Description
15:0	TLADDR	SW : RW Address bits[15:0]

0x014039B4 AFAB_FABRIC_TRIGGER_REG_2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the lower address which is used as comparison for the trigger feature of the performance monitor function.

AFAB_FABRIC_TRIGGER_REG_2

Bits	Name	Description
15:0	AMID	SW : RW AMID / HMID

0x014039B8 AFAB_FABRIC_TRIGGER_REG_3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the address channel transfer qualifiers which are used as comparison for the trigger feature of the performance monitor function.

AFAB_FABRIC_TRIGGER_REG_3

Bits	Name	Description
15:12	RESERVED_BITS15_12	
11	AOOOWR	SW : RW Out-of-order write
10	AOOORD	SW : RW Out-of-order read
9:3	ATID	SW : RW Address TID (If ATID is less than 7 bits, the upper bits must be set to 0)
2	AFULL	SW : RW Full Transfer
1	RESERVED_BIT1	
0	APROTNS	SW : RW Protection level

0x014039BC AFAB_FABRIC_TRIGGER_REG_4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the address channel transfer qualifiers which are used as comparison for the trigger feature of the performance monitor function.

AFAB_FABRIC_TRIGGER_REG_4

Bits	Name	Description
15:12	ATYPE	SW : RW Memory type attributes
11:10	ALOCK	SW : RW Lock type
9	RESERVED_BITS9	
8	ABURST	SW : RW Burst type
7:5	ASIZE	Burst size
4:1	ALEN	Burst length
0	AWRITE	Burst direction

0x014039C0 AFAB_FABRIC_TRIGGER_MASK_REG_0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR0.

AFAB_FABRIC_TRIGGER_MASK_REG_0

Bits	Name	Description
15:0	FTTR0_MASK	SW : RW Bit mask field for FTTR0 Enable: 1 Disable: 0

0x014039C4 AFAB_FABRIC_TRIGGER_MASK_REG_1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR1.

AFAB_FABRIC_TRIGGER_MASK_REG_1

Bits	Name	Description
15:0	FTTR1_MASK	SW : RW Bit mask field for FTTR1 Enable: 1 Disable: 0

0x014039C8 AFAB_FABRIC_TRIGGER_MASK_REG_2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR2.

AFAB_FABRIC_TRIGGER_MASK_REG_2

Bits	Name	Description
15:0	FTTR2_MASK	SW : RW Bit mask field for FTTR2 Enable: 1 Disable: 0

0x014039CC AFAB_FABRIC_TRIGGER_MASK_REG_3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR3.

AFAB_FABRIC_TRIGGER_MASK_REG_3

Bits	Name	Description
15:0	FTTR3_MASK	SW : RW Bit mask field for FTTR3 Enable: 1 Disable: 0

0x014039D0 AFAB_FABRIC_TRIGGER_MASK_REG_4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR4.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR4.

AFAB_FABRIC_TRIGGER_MASK_REG_4

Bits	Name	Description
15:0	FTTR4_MASK	SW : RW Bit mask field for FTTR4 Enable: 1 Disable: 0

0x014039D4 AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter0.

AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG0

Bits	Name	Description
15:0	E0AL	SW : RW LSB address value Event counter 0 address selection (if address range filtering enabled)

0x014039D8 AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter0.

AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG0

Bits	Name	Description
15:0	E0AU	SW : RW MSB address value Event counter 0 address selection (if address range filtering enabled)

0x014039DC AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter1.

AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG1

Bits	Name	Description
15:0	E1AL	SW : RW LSB address value Event counter 1address selection (if address range filtering enabled)

0x014039E0 AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter1.

AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG1

Bits	Name	Description
15:0	E1AU	SW : RW MSB address value Event counter 1address selection (if address range filtering enabled)

0x014039E4 AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter2.

AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG2

Bits	Name	Description
15:0	E2AL	SW : RW LSB address value Event counter 2 address selection (if address range filtering enabled)

0x014039E8 AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter2.

AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG2

Bits	Name	Description
15:0	E2AU	SW : RW MSB address value Event counter 2 address selection (if address range filtering enabled)

0x014039EC AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter3.

AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG3

Bits	Name	Description
15:0	E3AL	SW : RW LSB address value Event counter 3 address selection (if address range filtering enabled)

0x014039F0 AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter3.

AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG3

Bits	Name	Description
15:0	E3AU	SW : RW MSB address value Event counter 3 address selection (if address range filtering enabled)

0x014039F4 AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter4.

AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG4

Bits	Name	Description
15:0	E4AL	SW : RW LSB address value Event counter 4 address selection (if address range filtering enabled)

0x014039F8 AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter4.

AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG4

Bits	Name	Description
15:0	E4AU	SW : RW MSB address value Event counter 4address selection (if address range filtering enabled)

0x014039FC AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter5.

AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG5

Bits	Name	Description
15:0	E5AL	SW : RW LSB address value Event counter 5 address selection (if address range filtering enabled)

0x01403A00 AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter4.

AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG5

Bits	Name	Description
15:0	E5AU	SW : RW MSB address value Event counter 5 address selection (if address range filtering enabled)

0x01403A04 AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter 6.

AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG6

Bits	Name	Description
15:0	E6AL	SW : RW LSB address value Event counter 6 address selection (if address range filtering enabled)

0x01403A08 AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 6.

AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG6

Bits	Name	Description
15:0	E6AU	SW : RW MSB address value Event counter 6 address selection (if address range filtering enabled)

0x01403A0C AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter 7.

AFAB_FABRIC_MONITOR_ADDRESS_LOWER_REG7

Bits	Name	Description
15:0	E7AL	SW : RW LSB address value Event counter 7 address selection (if address range filtering enabled)

0x01403A10 AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 7.

AFAB_FABRIC_MONITOR_ADDRESS_UPPER_REG7

Bits	Name	Description
15:0	E7AU	SW : RW MSB address value Event counter 7 address selection (if address range filtering enabled)

0x01403A14 AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR0.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG0

Bits	Name	Description
15:0	E0AML	SW : RW LSB address value Event counter 0 address mask

0x01403A18 AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR0.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG0

Bits	Name	Description
15:0	E0AMU	SW : RW MSB address value Event counter 0 address mask

0x01403A1C AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR1.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG1

Bits	Name	Description
15:0	E1AML	SW : RW LSB address value Event counter 1 address mask

0x01403A20 AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR1.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG1

Bits	Name	Description
15:0	E1AMU	SW : RW MSB address value Event counter address mask

0x01403A24 AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR2.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG2

Bits	Name	Description
15:0	E2AML	SW : RW LSB address value Event counter 2 address mask

0x01403A28 AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR2.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG2

Bits	Name	Description
15:0	E2AMU	SW : RW MSB address value Event counter 2 address mask

0x01403A2C AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR3.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG3

Bits	Name	Description
15:0	E3AML	SW : RW LSB address value Event counter 3 address mask

0x01403A30 AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR3.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG3

Bits	Name	Description
15:0	E3AMU	SW : RW MSB address value Event counter 3 address mask

0x01403A34 AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 4.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR4.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG4

Bits	Name	Description
15:0	E4AML	SW : RW LSB address value Event counter 4 address mask

0x01403A38 AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 4.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR4.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG4

Bits	Name	Description
15:0	E4AMU	SW : RW MSB address value Event counter 4 address mask

0x01403A3C AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 5.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR5.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG5

Bits	Name	Description
15:0	E5AML	SW : RW LSB address value Event counter 5 address mask

0x01403A40 AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 5.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR5.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG5

Bits	Name	Description
15:0	E5AMU	SW : RW MSB address value Event counter 5 address mask

0x01403A44 AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 6.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR6.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG6

Bits	Name	Description
15:0	E6AML	SW : RW LSB address value Event counter 6 address mask

0x01403A48 AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 6.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR6.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG6

Bits	Name	Description
15:0	E6AMU	SW : RW MSB address value Event counter 6 address mask

0x01403A4C AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 7.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR7.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG7

Bits	Name	Description
15:0	E7AML	SW : RW LSB address value Event counter 7 address mask

0x01403A50 AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 7.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR7.

AFAB_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG7

Bits	Name	Description
15:0	E7AMU	SW : RW MSB address value Event counter 7 address mask

0x01403A70 AFAB_FABRIC_MONITOR_MID_MASK_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 0.

AFAB_FABRIC_MONITOR_MID_MASK_REG0

Bits	Name	Description
15:0	E0MM	SW : RW MID Mask value for event counter 0

0x01403A74 AFAB_FABRIC_MONITOR_MID_MASK_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 1.

AFAB_FABRIC_MONITOR_MID_MASK_REG1

Bits	Name	Description
15:0	E1MM	SW : RW MID Mask value for event counter 1

0x01403A78 AFAB_FABRIC_MONITOR_MID_MASK_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 2.

AFAB_FABRIC_MONITOR_MID_MASK_REG2

Bits	Name	Description
15:0	E2MM	SW : RW MID Mask value for event counter 2

0x01403A7C AFAB_FABRIC_MONITOR_MID_MASK_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 3.

AFAB_FABRIC_MONITOR_MID_MASK_REG3

Bits	Name	Description
15:0	E3MM	SW : RW MID Mask value for event counter 3

0x01403A80 AFAB_FABRIC_MONITOR_MID_MASK_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 4.

AFAB_FABRIC_MONITOR_MID_MASK_REG4

Bits	Name	Description
15:0	E4MM	SW : RW MID Mask value for event counter 4

0x01403A84 AFAB_FABRIC_MONITOR_MID_MASK_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 15.

AFAB_FABRIC_MONITOR_MID_MASK_REG5

Bits	Name	Description
15:0	E5MM	SW : RW MID Mask value for event counter 5

0x01403A88 AFAB_FABRIC_MONITOR_MID_MASK_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 6.

AFAB_FABRIC_MONITOR_MID_MASK_REG6

Bits	Name	Description
15:0	E6MM	SW : RW MID Mask value for event counter 6

0x01403A8C AFAB_FABRIC_MONITOR_MID_MASK_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 7.

AFAB_FABRIC_MONITOR_MID_MASK_REG7

Bits	Name	Description
15:0	E7MM	SW : RW MID Mask value for event counter 7

0x01403AA0 AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG0

Bits	Name	Description
15:0	EBTL0	SW : RW Total # beats (lower 16-bit value)

0x01403AA4 AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG0

Bits	Name	Description
15:0	EBTM0	SW : RW Total # beats (middle 16-bit value)

0x01403AA8 AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG0

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU0	SW : RW Total # beats (upper 4-bit value)

0x01403AAC AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG1

Bits	Name	Description
15:0	EBTL1	SW : RW Total # beats (lower 16-bit value)

0x01403AB0 AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG1

Bits	Name	Description
15:0	EBTM1	SW : RW Total # beats (middle 16-bit value)

0x01403AB4 AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG1

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU1	SW : RW Total # beats (upper 4-bit value)

0x01403AB8 AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG2

Bits	Name	Description
15:0	EBTL2	SW : RW Total # beats (lower 16-bit value)

0x01403ABC AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG2

Bits	Name	Description
15:0	EBTM2	SW : RW Total # beats (middle 16-bit value)

0x01403AC0 AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG2

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU2	SW : RW Total # beats (upper 4-bit value)

0x01403AC4 AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG3

Bits	Name	Description
15:0	EBTL3	SW : RW Total # beats (lower 16-bit value)

0x01403AC8 AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write

Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG3

Bits	Name	Description
15:0	EBTM3	SW : RW Total # beats (middle 16-bit value)

0x01403ACC AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG3

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU3	SW : RW Total # beats (upper 4-bit value)

0x01403AD0 AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG4

Bits	Name	Description
15:0	EBTL4	SW : RW Total # beats (lower 16-bit value)

0x01403AD4 AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG4

Bits	Name	Description
15:0	EBTM4	SW : RW Total # beats (middle 16-bit value)

0x01403AD8 AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG4

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU4	SW : RW Total # beats (upper 4-bit value)

0x01403ADC AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write

Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG5

Bits	Name	Description
15:0	EBTL5	SW : RW Total # beats (lower 16-bit value)

0x01403AE0 AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG5

Bits	Name	Description
15:0	EBTM5	SW : RW Total # beats (middle 16-bit value)

0x01403AE4 AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG5

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU5	SW : RW Total # beats (upper 4-bit value)

0x01403AE8 AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG6

Bits	Name	Description
15:0	EBTL6	SW : RW Total # beats (lower 16-bit value)

0x01403AEC AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG6

Bits	Name	Description
15:0	EBTM6	SW : RW Total # beats (middle 16-bit value)

0x01403AF0 AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG6

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU6	SW : RW Total # beats (upper 4-bit value)

0x01403AF4 AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG7

Bits	Name	Description
15:0	EBTL7	SW : RW Total # beats (lower 16-bit value)

0x01403AF8 AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_MID_REG7

Bits	Name	Description
15:0	EBTM7	SW : RW Total # beats (middle 16-bit value)

0x01403AFC AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG7

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU7	SW : RW Total # beats (upper 4-bit value)

0x01403B00 AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG0

Bits	Name	Description
15:0	EBYL0	SW : RW Total bytes (lower 16-bit value)

0x01403B04 AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG0

Bits	Name	Description
15:0	EBYM0	SW : RW Total bytes (middle 16-bit value)

0x01403B08 AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG0

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU0	SW : RW Total bytes (upper 11-bit value)

0x01403B0C AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG1

Bits	Name	Description
15:0	EBYL1	SW : RW Total bytes (lower 16-bit value)

0x01403B10 AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG1

Bits	Name	Description
15:0	EBYM1	SW : RW Total bytes (middle 16-bit value)

0x01403B14 AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG1

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU1	SW : RW Total bytes (upper 11-bit value)

0x01403B18 AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG2

Bits	Name	Description
15:0	EBYL2	SW : RW Total bytes (lower 16-bit value)

0x01403B1C AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG2

Bits	Name	Description
15:0	EBYM2	SW : RW Total bytes (middle 16-bit value)

0x01403B20 AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG2

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU2	SW : RW Total bytes (upper 11-bit value)

0x01403B24 AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG3

Bits	Name	Description
15:0	EBYL3	SW : RW Total bytes (lower 16-bit value)

0x01403B28 AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG3

Bits	Name	Description
15:0	EBYM3	SW : RW Total bytes (middle 16-bit value)

0x01403B2C AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG3

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU3	SW : RW Total bytes (upper 11-bit value)

0x01403B30 AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG4

Bits	Name	Description
15:0	EBYL4	SW : RW Total bytes (lower 16-bit value)

0x01403B34 AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG4

Bits	Name	Description
15:0	EBYM4	SW : RW Total bytes (middle 16-bit value)

0x01403B38 AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG4

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU4	SW : RW Total bytes (upper 11-bit value)

0x01403B3C AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG5

Bits	Name	Description
15:0	EBYL5	SW : RW Total bytes (lower 16-bit value)

0x01403B40 AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG5

Bits	Name	Description
15:0	EBYM5	SW : RW Total bytes (middle 16-bit value)

0x01403B44 AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG5

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU5	SW : RW Total bytes (upper 11-bit value)

0x01403B48 AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG6

Bits	Name	Description
15:0	EBYL6	SW : RW Total bytes (lower 16-bit value)

0x01403B4C AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG6

Bits	Name	Description
15:0	EBYM6	SW : RW Total bytes (middle 16-bit value)

0x01403B50 AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG6

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU6	SW : RW Total bytes (upper 11-bit value)

0x01403B54 AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG7

Bits	Name	Description
15:0	EBYL7	SW : RW Total bytes (lower 16-bit value)

0x01403B58 AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_MID_REG7

Bits	Name	Description
15:0	EBYM7	SW : RW Total bytes (middle 16-bit value)

0x01403B5C AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

AFAB_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG7

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU7	SW : RW Total bytes (upper 11-bit value)

0x01403B60 AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 0.

AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0

Bits	Name	Description
15:14	T0SR	SW : RW Tenure selection for tenure counter 0 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T0MIDFEN	SW : RW Tenure counter 0 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T0INDFEN	SW : RW Tenure counter 0 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T0IND	SW : RW Tenure counter 0 Instruction/Data selection 0x0: Data 0x1: Instruction

AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
8:4	T0MP	SW : RW Tenure master port selection register for tenure counter 0 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
3:0	T0SW	SW : RW Tenure slave way selection register for tenure counter 0 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01403B64 AFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 0.

AFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG0

Bits	Name	Description
15:0	T0MID	SW : RW Tenure counter 0 MID selection (If MID filtering enabled)

0x01403B68 AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 1.

AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1

Bits	Name	Description
15:14	T1SR	SW : RW Tenure selection for tenure counter 1 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T1MIDFEN	SW : RW Tenure counter 1MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T1INDFEN	SW : RW Tenure counter 1Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T1IND	SW : RW Tenure counter 1Instruction/Data selection 0x0: Data 0x1: Instruction

AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
8:4	T1MP	SW : RW Tenure master port selection register for tenure counter 1 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
3:0	T1SW	SW : RW Tenure slave way selection register for tenure counter 1 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01403B6C AFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 1.

AFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG1

Bits	Name	Description
15:0	T1MID	SW : RW Tenure counter 1MID selection (If MID filtering enabled)

0x01403B70 AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 2.

AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2

Bits	Name	Description
15:14	T2SR	SW : RW Tenure selection for tenure counter 2 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T2MIDFEN	SW : RW Tenure counter 2 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T2INDFEN	SW : RW Tenure counter 2 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T2IND	SW : RW Tenure counter 2 Instruction/Data selection 0x0: Data 0x1: Instruction

AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
8:4	T2MP	SW : RW Tenure master port selection register for tenure counter 2 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
3:0	T2SW	SW : RW Tenure slave way selection register for tenure counter 2 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01403B74 AFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 2.

AFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG2

Bits	Name	Description
15:0	T2MID	SW : RW Tenure counter 2 MID selection (If MID filtering enabled)

0x01403B78 AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 3.

AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3

Bits	Name	Description
15:14	T3SR	SW : RW Tenure selection for tenure counter 3 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T3MIDFEN	SW : RW Tenure counter 3 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T3INDFEN	SW : RW Tenure counter 3 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T3IND	SW : RW Tenure counter 3 Instruction/Data selection 0x0: Data 0x1: Instruction

AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
8:4	T3MP	SW : RW Tenure master port selection register for tenure counter 3 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

AFAB_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
3:0	T3SW	SW : RW Tenure slave way selection register for tenure counter 3 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01403B7C AFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 3.

AFAB_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG3

Bits	Name	Description
15:0	T3MID	SW : RW Tenure counter 3 MID selection (If MID filtering enabled)

0x01403B80 AFAB_FABRIC_MONITOR_MIN_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x01FF

This register contains the minimum value of the tenure that is selected using FPTSLR0 and measured in tenure counter 0.

NOTE The reset value for this register is set to 0x01FF, equivalent to 8191 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at 0x01FF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

AFAB_FABRIC_MONITOR_MIN_REG0

Bits	Name	Description
15:0	MIN0	SW : R Minimum value of tenure, in tenure counter 0

0x01403B84 AFAB_FABRIC_MONITOR_MIN_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x01FF

This register contains the minimum value of the tenure that is selected using FPTSLR1 and measured in tenure counter 1.

NOTE The reset value for this register is set to 0x01FF, equivalent to 8191 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at 0x01FF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

AFAB_FABRIC_MONITOR_MIN_REG1

Bits	Name	Description
15:0	MIN1	SW : R Minimum value of tenure, in tenure counter 1

0x01403B88 AFAB_FABRIC_MONITOR_MIN_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x01FF

This register contains the minimum value of the tenure that is selected using FPTSLR2 and measured in tenure counter 2.

NOTE The reset value for this register is set to 0x01FF, equivalent to 8191 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at 0x01FF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

AFAB_FABRIC_MONITOR_MIN_REG2

Bits	Name	Description
15:0	MIN2	SW : R Minimum value of tenure, in tenure counter 2

0x01403B8C AFAB_FABRIC_MONITOR_MIN_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x01FF

This register contains the minimum value of the tenure that is selected using FPTSLR3 and measured in tenure counter 3.

NOTE The reset value for this register is set to 0x01FF, equivalent to 8191 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at 0x01FF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

AFAB_FABRIC_MONITOR_MIN_REG3

Bits	Name	Description
15:0	MIN3	SW : R Minimum value of tenure, in tenure counter 3

0x01403B90 AFAB_FABRIC_MONITOR_MAX_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR0 and measured in tenure counter 0.

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

AFAB_FABRIC_MONITOR_MAX_REG0

Bits	Name	Description
15:0	MAX0	SW : R Maximum value of tenure, in tenure counter 0

0x01403B94 AFAB_FABRIC_MONITOR_MAX_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR1and measured in tenure counter 1.

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

AFAB_FABRIC_MONITOR_MAX_REG1

Bits	Name	Description
15:0	MAX1	SW : R Maximum value of tenure, in tenure counter 1

0x01403B98 AFAB_FABRIC_MONITOR_MAX_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR2 and measured in tenure counter 2.

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

AFAB_FABRIC_MONITOR_MAX_REG2

Bits	Name	Description
15:0	MAX2	SW : R Maximum value of tenure, in tenure counter 2

0x01403B9C AFAB_FABRIC_MONITOR_MAX_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR3 and measured in tenure counter 3.

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

AFAB_FABRIC_MONITOR_MAX_REG3

Bits	Name	Description
15:0	MAX3	SW : R Maximum value of tenure, in tenure counter 3

0x01403BA0 AFAB_FABRIC_MONITOR_TENURE_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 0.

AFAB_FABRIC_MONITOR_TENURE_LOWER_REG0

Bits	Name	Description
15:0	LTOT0	SW : RW LSB total value of tenure, in tenure counter 0

0x01403BA4 AFAB_FABRIC_MONITOR_TENURE_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 0.

AFAB_FABRIC_MONITOR_TENURE_UPPER_REG0

Bits	Name	Description
15:0	UTOT0	SW : RW MSB total value of tenure, in tenure counter 0

0x01403BA8 AFAB_FABRIC_MONITOR_TENURE_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 1.

AFAB_FABRIC_MONITOR_TENURE_LOWER_REG1

Bits	Name	Description
15:0	LTOT1	SW : RW LSB total value of tenure, in tenure counter 1

0x01403BAC AFAB_FABRIC_MONITOR_TENURE_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 1.

AFAB_FABRIC_MONITOR_TENURE_UPPER_REG1

Bits	Name	Description
15:0	UTOT1	SW : RW MSB total value of tenure, in tenure counter 1

0x01403BB0 AFAB_FABRIC_MONITOR_TENURE_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 2.

AFAB_FABRIC_MONITOR_TENURE_LOWER_REG2

Bits	Name	Description
15:0	LTOT2	SW : RW LSB total value of tenure, in tenure counter 2

0x01403BB4 AFAB_FABRIC_MONITOR_TENURE_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 2.

AFAB_FABRIC_MONITOR_TENURE_UPPER_REG2

Bits	Name	Description
15:0	UTOT2	SW : RW MSB total value of tenure, in tenure counter 2

0x01403BB8 AFAB_FABRIC_MONITOR_TENURE_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 3.

AFAB_FABRIC_MONITOR_TENURE_LOWER_REG3

Bits	Name	Description
15:0	LTOT3	SW : RW LSB total value of tenure, in tenure counter 3

0x01403BBC AFAB_FABRIC_MONITOR_TENURE_UPPER_REG3.

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 3.

AFAB_FABRIC_MONITOR_TENURE_UPPER_REG3

Bits	Name	Description
15:0	UTOT3	SW : RW MSB total value of tenure, in tenure counter 3

0x01403BC0 AFAB_FABRIC_MONITOR_LAST_TENURE_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 0.

AFAB_FABRIC_MONITOR_LAST_TENURE_REG0

Bits	Name	Description
15:0	LASTT0	SW : R Last tenure value in tenure counter 0

0x01403BC4 AFAB_FABRIC_MONITOR_LAST_TENURE_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 1.

AFAB_FABRIC_MONITOR_LAST_TENURE_REG1

Bits	Name	Description
15:0	LASTT1	SW : R Last tenure value in tenure counter 1

0x01403BC8 AFAB_FABRIC_MONITOR_LAST_TENURE_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 2.

AFAB_FABRIC_MONITOR_LAST_TENURE_REG2

Bits	Name	Description
15:0	LASTT2	SW : R Last tenure value in tenure counter 2

0x01403BCC AFAB_FABRIC_MONITOR_LAST_TENURE_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 3.

AFAB_FABRIC_MONITOR_LAST_TENURE_REG3

Bits	Name	Description
15:0	LASTT0	SW : R Last tenure value in tenure counter 3

0x01403BD0 AFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 0.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG0

Bits	Name	Description
15:0	T0AL	SW : RW LSB address value Tenure counter 0 address mask

0x01403BD4 AFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 0.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG0

Bits	Name	Description
15:0	T0AU	SW : RW MSB address value Tenure counter 0 address mask

0x01403BD8 AFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 1.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG1

Bits	Name	Description
15:0	T1AL	SW : RW LSB address value Tenure counter 1 address mask

0x01403BDC AFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 1.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG1

Bits	Name	Description
15:0	T1AU	SW : RW MSB address value Tenure counter 1 address mask

0x01403BE0 AFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 2.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG2

Bits	Name	Description
15:0	T2AL	SW : RW LSB address value Tenure counter 2 address mask

0x01403BE4 AFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 2.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG2

Bits	Name	Description
15:0	T2AU	SW : RW MSB address value Tenure counter 2 address mask

0x01403BE8 AFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 3.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG3

Bits	Name	Description
15:0	T3AL	SW : RW LSB address value Tenure counter 3 address mask

0x01403BEC AFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 3.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG3

Bits	Name	Description
15:0	T3AU	SW : RW MSB address value Tenure counter 3 address mask

0x01403BF0 AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR0.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG0

Bits	Name	Description
15:0	T0AML	SW : RW LSB address value Tenure counter 0 address mask

0x01403BF4 AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR0.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG0

Bits	Name	Description
15:0	T0AMU	SW : RW MSB address mask value Tenure counter 0 address mask

0x01403BF8 AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR1.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG1

Bits	Name	Description
15:0	T1AML	SW : RW LSB address value Tenure counter 1 address mask

0x01403BFC AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR1.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG1

Bits	Name	Description
15:0	T1AMU	SW : RW MSB address mask value Tenure counter 1 address mask

0x01403C00 AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR2.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG2

Bits	Name	Description
15:0	T2AML	SW : RW LSB address value Tenure counter 2 address mask

0x01403C04 AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR2.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG2

Bits	Name	Description
15:0	T2AMU	SW : RW MSB address mask value Tenure counter 2 address mask

0x01403C08 AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR3.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG3

Bits	Name	Description
15:0	T3AML	SW : RW LSB address value Tenure counter 3 address mask

0x01403C0C AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR3.

AFAB_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG3

Bits	Name	Description
15:0	T3AMU	SW : RW MSB address mask value Tenure counter 3 address mask

0x01403C10 AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG 0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 0 that were longer than the specified threshold for tenure counter 0.

AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG0

Bits	Name	Description
15:0	T0ATCL	SW : R LSB count value

0x01403C14 AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 0 that were longer than the specified threshold for tenure counter 0.

AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG0

Bits	Name	Description
15:0	T0ATCU	SW : R MSB count value

0x01403C18 AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG 1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 1 that were longer than the specified threshold for tenure counter 1.

AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG1

Bits	Name	Description
15:0	T1ATCL	SW : R LSB count value

0x01403C1C AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 1 that were longer than the specified threshold for tenure counter 1.

AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG1

Bits	Name	Description
15:0	T1ATCU	SW : R MSB count value

0x01403C20 AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 2 that were longer than the specified threshold for tenure counter 2.

AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG2

Bits	Name	Description
15:0	T2ATCL	SW : R LSB count value

0x01403C24 AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 2 that were longer than the specified threshold for tenure counter 2.

AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG2

Bits	Name	Description
15:0	T2ATCU	SW : R MSB count value

0x01403C28 AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG 3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 3 that were longer than the specified threshold for tenure counter 3.

AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG3

Bits	Name	Description
15:0	T3ATCL	SW : R LSB count value

0x01403C2C AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 3 that were longer than the specified threshold for tenure counter 3.

AFAB_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG3

Bits	Name	Description
15:0	T3ATCU	SW : R MSB count value

0x01403C30 AFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 0 are measured.

AFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG0

Bits	Name	Description
12:0	T0TV	SW : RW Tenure counter 0 threshold value

0x01403C34 AFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 1 are measured.

AFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG1

Bits	Name	Description
12:0	T1TV	SW : RW Tenure counter 1 threshold value

0x01403C38 AFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 2 are measured.

AFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG2

Bits	Name	Description
12:0	T2TV	SW : RW Tenure counter 2 threshold value

0x01403C3C AFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 3 are measured.

AFAB_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG3

Bits	Name	Description
12:0	T3TV	SW : RW Tenure counter 3 threshold value

0x01403C40 AFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 0.

AFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG0

Bits	Name	Description
15:0	T0MM	SW : RW MID Mask value

0x01403C44 AFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 1.

AFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG1

Bits	Name	Description
15:0	T1MM	SW : RW MID Mask value

0x01403C48 AFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 2.

AFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG2

Bits	Name	Description
15:0	T2MM	SW : RW MID Mask value

0x01403C4C AFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 3.

AFAB_FABRIC_MONITOR_TENURE_MID_MASK_REG3

Bits	Name	Description
15:0	T3MM	SW : RW MID Mask value

0x01403C50 AFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure0 register.

AFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG0

Bits	Name	Description
15:0	TLC0	SW : R LSB count value Incremented every time a tenure under observation completes in tenure counter 0

0x01403C54 AFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure0 register.

AFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG0

Bits	Name	Description
15:0	TUC0	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 0

0x01403C58 AFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure1 register.

AFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG1

Bits	Name	Description

0x01403C5C AFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure1 register.

AFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG1

Bits	Name	Description
15:0	TUC1	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 1

0x01403C60 AFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure2 register.

AFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG2

Bits	Name	Description
15:0	TLC2	SW : R LSB count value Incremented every time a tenure under observation completes in tenure counter 2

0x01403C64 AFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure2 register.

AFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG2

Bits	Name	Description
15:0	TUC2	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 2

0x01403C68 AFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure3 register.

AFAB_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG3

Bits	Name	Description
15:0	TLC3	SW : R LSB count value Incremented every time a tenure under observation completes in tenure counter 3

0x01403C6C AFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure3 register.

AFAB_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG3

Bits	Name	Description
15:0	TUC3	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 3

0x01403C70 AFAB_FABRIC_MONITOR_TENURE_PICK_PORTS_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the main port and other port selection for the 4 event counters.

AFAB_FABRIC_MONITOR_TENURE_PICK_PORTS_REG

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3	T3PP	SW : RW Tenure counter 3 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T3MP or T3SW
2	T2PP	SW : RW Tenure counter 2 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T2MP or T2SW

AFAB_FABRIC_MONITOR_TENURE_PICK_PORTS_REG (cont.)

Bits	Name	Description
1	T1PP	SW : RW Tenure counter 1 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T1MP or T1SW
0	T0PP	SW : RW Tenure counter 0 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T0MP or T0SW

0x01403C80 AFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 0.

AFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG0

Bits	Name	Description
15:0	LTOTU0	SW : RW LSB total union value of tenure, in tenure counter 0

0x01403C84 AFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 0.

AFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG0

Bits	Name	Description
15:0	UTOTU0	SW : RW MSB total union value of tenure, in tenure counter 0

0x01403C88 AFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 1.

AFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG1

Bits	Name	Description
15:0	LTOTU1	SW : RW LSB total union value of tenure, in tenure counter 1

0x01403C8C AFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 1.

AFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG1

Bits	Name	Description
15:0	UTOTU1	SW : RW MSB total union value of tenure, in tenure counter 1

0x01403C90 AFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 2.

AFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG2

Bits	Name	Description
15:0	LTOTU2	SW : RW LSB total union value of tenure, in tenure counter 2

0x01403C94 AFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 2.

AFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG2

Bits	Name	Description
15:0	UTOTU2	SW : RW MSB total union value of tenure, in tenure counter 2

0x01403C98 AFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 3.

AFAB_FABRIC_MONITOR_TENURE_UNION_LOWER_REG3

Bits	Name	Description
15:0	LTOTU3	SW : RW LSB total union value of tenure, in tenure counter 3

0x01403C9C AFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 3.

AFAB_FABRIC_MONITOR_TENURE_UNION_UPPER_REG3

Bits	Name	Description
15:0	UTOTU3	SW : RW MSB total union value of tenure, in tenure counter 3

0x01403CA0 AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 0, that were pipelined.

AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG0

Bits	Name	Description

0x01403CA4 AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 0, that were pipelined.

AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG0

Bits	Name	Description
15:0	TUCP0	SW : R MSB count value TUCP0,TLCP0 value incremented every time a pipelined tenure completes in tenure counter 0

0x01403CA8 AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 1, that were pipelined.

AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG1

Bits	Name	Description

0x01403CAC AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 1, that were pipelined.

AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG1

Bits	Name	Description
15:0	TUCP1	SW : R MSB count value TUCP1,TLCP1 value incremented every time a pipelined tenure completes in tenure counter 1

0x01403CB0 AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 2, that were pipelined.

AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG2

Bits	Name	Description

0x01403CB4 AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 2, that were pipelined.

AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG2

Bits	Name	Description
15:0	TUCP2	SW : R MSB count value TUCP1,TLCP1 value incremented every time a pipelined tenure completes in tenure counter 2

0x01403CB8 AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 3, that were pipelined.

AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG3

Bits	Name	Description

0x01403CBC AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 3, that were pipelined.

AFAB_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG3

Bits	Name	Description
15:0	TUCP3	SW : R MSB count value TUCP3,TLCP3 value incremented every time a pipelined tenure completes in tenure counter 3

0x01403CC0 AFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the max number of tenures pipelined at any point during the monitoring window for tenure counter 0.

AFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG0

Bits	Name	Description
15:0	TMCP0	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 0

0x01403CC4 AFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the max number of tenures pipelined at any point during the monitoring window for tenure counter 1

AFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG1

Bits	Name	Description
15:0	TMCP1	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 1

0x01403CC8 AFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the max number of tenures pipelined at any point during the monitoring window for tenure counter 2.

AFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG2

Bits	Name	Description
15:0	TMCP2	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 2

0x01403CCC AFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the max number of tenures pipelined at any point during the monitoring window for tenure counter 3.

AFAB_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG3

Bits	Name	Description
15:0	TMCP3	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 3

0x01403CD0 AFAB_FABRIC_MONITOR_INFLIGHT_TENURE_CORRECTION_MODE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the facility to correlate a particular event counter to a tenure counter. When the tenure results of a counter are reset during a monitoring window (to account for errors due to starting the monitor in the middle of traffic), the event counters too get reset if the correlation between them is enabled.

NOTE PCORR bit (bit 0) should not be set for APQ8064.

AFAB_FABRIC_MONITOR_INFLIGHT_TENURE_CORRECTION_MODE_REG

Bits	Name	Description
15:9	RESERVED_15_9	Reserved Bits
8	EC7COR	SW : RW 0x1: Link Event Counter 7 to Tenure Counter 3 0x0: Event Counter 7 is independent

AFAB_FABRIC_MONITOR_INFLIGHT_TENURE_CORRECTION_MODE_REG (cont.)

Bits	Name	Description
7	EC6COR	SW : RW 0x1: Link Event Counter 6 to Tenure Counter 2 0x0: Event Counter 6 is independent
6	EC5COR	SW : RW 0x1: Link Event Counter 5 to Tenure Counter 1 0x0: Event Counter 5 is independent
5	EC4COR	SW : RW 0x1: Link Event Counter 4 to Tenure Counter 0 0x0: Event Counter 4 is independent
4	EC3COR	SW : RW 0x1: Link Event Counter 3 to Tenure Counter 3 0x0: Event Counter 3 is independent
3	EC2COR	SW : RW 0x1: Link Event Counter 2 to Tenure Counter 2 0x0: Event Counter 2 is independent
2	EC1COR	SW : RW 0x1: Link Event Counter 1 to Tenure Counter 1 0x0: Event Counter 1 is independent
1	EC0COR	SW : RW 0x1: Link Event Counter 0 to Tenure Counter 0 0x0: Event Counter 0 is independent
0	PCORR	SW : RW This is the enable for tenure correction mode This bit SHOULD NOT be set for APQ8064.

0x01403CE0 AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures counted by tenure counter 0 that correspond to out-of-order transactions.

AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG0

Bits	Name	Description
15:0	TOLC0	SW : R LSB count value Incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 0

0x01403CE4 AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures counted by tenure counter 0 that correspond to out-of-order transactions.

AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG0

Bits	Name	Description
15:0	TOUC0	SW : R MSB count value TOUC,TOLC value incremented every time a tenure (of an out-of-order transaction) under observation completes in tenure counter 0

0x01403CE8 AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures counted by tenure counter 1 that correspond to out-of-order transactions.

AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG1

Bits	Name	Description
15:0	TOLC1	SW : R LSB count value Incremented every time a tenure (of an out-of-order transaction) under observation completes in tenure counter 1

0x01403CEC AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures counted by tenure counter 1 that correspond to out-of-order transactions.

AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG1

Bits	Name	Description
15:0	TOUC1	SW : R MSB count value TOUC,TOLC value incremented every time a tenure (of an out-of-order transaction) under observation completes in tenure counter 1

0x01403CF0 AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures counted by tenure counter 2 that correspond to out-of-order transactions.

AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG2

Bits	Name	Description
15:0	TOLC2	SW : R LSB count value Incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 2

0x01403CF4 AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures counted by tenure counter 2 that correspond to out-of-order transactions.

AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG2

Bits	Name	Description
15:0	TOUC2	SW : R MSB count value TOUC,TOLC value incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 2

0x01403CF8 AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures counted by tenure counter 3 that correspond to out-of-order transactions.

AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG3

Bits	Name	Description
15:0	TOLC3	SW : R LSB count value Incremented every time a tenure (of an out-of-order transaction) under observation completes in tenure counter 3

0x01403CFC AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures counted by tenure counter 3 that correspond to out-of-order transactions

AFAB_FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG3

Bits	Name	Description
15:0	TOUC3	SW : R MSB count value TOUC,TOLC value incremented every time a tenure (of an out-of-order transaction) under observation completes in tenure counter 3

0x01403D00 AFAB_FABRIC_MONITOR_RTR_STATUS_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains 4 status bits (one for each performance monitor tenure counter). Each bit indicates whether the monitoring results pertaining to the associated tenure counter have been reset (to account for errors due to starting the monitor in the middle of traffic) or not.

AFAB_FABRIC_MONITOR_RTR_STATUS_REG

Bits	Name	Description
15:4	RESERVED15_4	Reserved
3	TC3_RESET	SW: R When set, this bit indicates that tenure counter 3 results have been reset by the design during the monitoring window, to account for errors due to starting the monitor in the middle of traffic
2	TC2_RESET	SW: R When set, this bit indicates that tenure counter 2 results have been reset by the design during the monitoring window, to account for errors due to starting the monitor in the middle of traffic
1	TC1_RESET	SW: R When set, this bit indicates that tenure counter 1 results have been reset by the design during the monitoring window, to account for errors due to starting the monitor in the middle of traffic
0	TC0_RESET	SW: R When set, this bit indicates that tenure counter 0 results have been reset by the design during the monitoring window, to account for errors due to starting the monitor in the middle of traffic

0x01403D04 AFAB_FABRIC_MONITOR_IDLE_INTERNAL_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 0 to Master 15). A value of 1 indicates that the internally generated idle status is to be used to determine when to reset the performance monitor tenure counter results (resetting the tenure counter results is needed to compensate for errors due to enabling the tenure counters in the middle of traffic). A value of 0 will indicate that the primary idle input is to be used instead.

NOTE These settings will have an effect only in case of AXI master ports.

AFAB_FABRIC_MONITOR_IDLE_INTERNAL_LOWER_REG

Bits	Name	Description
15	M15_PII	SW : RW 0x1: The internally generated idle status for Master 15 will be used by the performance monitor 0x0: Primary input I_AXI_M15_IDLE is used by the performance monitor

AFAB_FABRIC_MONITOR_IDLE_INTERNAL_LOWER_REG (cont.)

Bits	Name	Description
14	M14_PII	SW : RW 0x1: The internally generated idle status for Master 14 will be used by the performance monitor 0x0: Primary input I_AXI_M14_IDLE is used by the performance monitor
13	M13_PII	SW : RW 0x1: The internally generated idle status for Master 13 will be used by the performance monitor 0x0: Primary input I_AXI_M13_IDLE is used by the performance monitor
12	M12_PII	SW : RW 0x1: The internally generated idle status for Master 12 will be used by the performance monitor 0x0: Primary input I_AXI_M12_IDLE is used by the performance monitor
11	M11_PII	SW : RW 0x1: The internally generated idle status for Master 11 will be used by the performance monitor 0x0: Primary input I_AXI_M11_IDLE is used by the performance monitor
10	M10_PII	SW : RW 0x1: The internally generated idle status for Master 10 will be used by the performance monitor 0x0: Primary input I_AXI_M10_IDLE is used by the performance monitor
9	M9_PII	SW : RW 0x1: The internally generated idle status for Master 9 will be used by the performance monitor 0x0: Primary input I_AXI_M9_IDLE is used by the performance monitor
8	M8_PII	SW : RW 0x1: The internally generated idle status for Master 8 will be used by the performance monitor 0x0: Primary input I_AXI_M8_IDLE is used by the performance monitor
7	M7_PII	SW : RW 0x1: The internally generated idle status for Master 7 will be used by the performance monitor 0x0: Primary input I_AXI_M7_IDLE is used by the performance monitor
6	M6_PII	SW : RW 0x1: The internally generated idle status for Master 6 will be used by the performance monitor 0x0: Primary input I_AXI_M6_IDLE is used by the performance monitor

AFAB_FABRIC_MONITOR_IDLE_INTERNAL_LOWER_REG (cont.)

Bits	Name	Description
5	M5_PII	SW : RW 0x1: The internally generated idle status for Master 5 will be used by the performance monitor 0x0: Primary input I_AXI_M5_IDLE is used by the performance monitor
4	M4_PII	SW : RW 0x1: The internally generated idle status for Master 4 will be used by the performance monitor 0x0: Primary input I_AXI_M4_IDLE is used by the performance monitor
3	M3_PII	SW : RW 0x1: The internally generated idle status for Master 3 will be used by the performance monitor 0x0: Primary input I_AXI_M3_IDLE is used by the performance monitor
2	M2_PII	SW : RW 0x1: The internally generated idle status for Master 2 will be used by the performance monitor 0x0: Primary input I_AXI_M2_IDLE is used by the performance monitor
1	M1_PII	SW : RW 0x1: The internally generated idle status for Master 1 will be used by the performance monitor 0x0: Primary input I_AXI_M1_IDLE is used by the performance monitor
0	M0_PII	SW : RW 0x1: The internally generated idle status for Master 0 will be used by the performance monitor 0x0: Primary input I_AXI_M0_IDLE is used by the performance monitor

0x01403D08 AFAB_FABRIC_MONITOR_IDLE_INTERNAL_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 16 to Master 31). A value of 1 indicates that the internally generated idle status is to be used to determine when to reset the performance monitor tenure counter results (resetting the tenure counter results is needed to compensate for errors due to enabling the tenure counters in the middle of traffic). A value of 0 will indicate that the primary idle input is to be used instead.

NOTE These settings will have an effect only in case of AXI master ports.

AFAB_FABRIC_MONITOR_IDLE_INTERNAL_UPPER_REG

Bits	Name	Description
15	M31_PII	SW : RW 0x1: The internally generated idle status for Master 31 will be used by the performance monitor 0x0: Primary input I_AXI_M31_IDLE is used by the performance monitor
14	M30_PII	SW : RW 0x1: The internally generated idle status for Master 30 will be used by the performance monitor 0x0: Primary input I_AXI_M30_IDLE is used by the performance monitor
13	M29_PII	SW : RW 0x1: The internally generated idle status for Master 29 will be used by the performance monitor 0x0: Primary input I_AXI_M29_IDLE is used by the performance monitor
12	M28_PII	SW : RW 0x1: The internally generated idle status for Master 28 will be used by the performance monitor 0x0: Primary input I_AXI_M28_IDLE is used by the performance monitor
11	M27_PII	SW : RW 0x1: The internally generated idle status for Master 27 will be used by the performance monitor 0x0: Primary input I_AXI_M27_IDLE is used by the performance monitor
10	M26_PII	SW : RW 0x1: The internally generated idle status for Master 26 will be used by the performance monitor 0x0: Primary input I_AXI_M26_IDLE is used by the performance monitor
9	M25_PII	SW : RW 0x1: The internally generated idle status for Master 25 will be used by the performance monitor 0x0: Primary input I_AXI_M25_IDLE is used by the performance monitor
8	M24_PII	SW : RW 0x1: The internally generated idle status for Master 24 will be used by the performance monitor 0x0: Primary input I_AXI_M24_IDLE is used by the performance monitor

AFAB_FABRIC_MONITOR_IDLE_INTERNAL_UPPER_REG (cont.)

Bits	Name	Description
7	M23_PII	SW : RW 0x1: The internally generated idle status for Master 23 will be used by the performance monitor 0x0: Primary input I_AXI_M23_IDLE is used by the performance monitor
6	M22_PII	SW : RW 0x1: The internally generated idle status for Master 22 will be used by the performance monitor 0x0: Primary input I_AXI_M22_IDLE is used by the performance monitor
5	M21_PII	SW : RW 0x1: The internally generated idle status for Master 21 will be used by the performance monitor 0x0: Primary input I_AXI_M21_IDLE is used by the performance monitor
4	M20_PII	SW : RW 0x1: The internally generated idle status for Master 20 will be used by the performance monitor 0x0: Primary input I_AXI_M20_IDLE is used by the performance monitor
3	M19_PII	SW : RW 0x1: The internally generated idle status for Master 19 will be used by the performance monitor 0x0: Primary input I_AXI_M19_IDLE is used by the performance monitor
2	M18_PII	SW : RW 0x1: The internally generated idle status for Master 18 will be used by the performance monitor 0x0: Primary input I_AXI_M18_IDLE is used by the performance monitor
1	M17_PII	SW : RW 0x1: The internally generated idle status for Master 17 will be used by the performance monitor 0x0: Primary input I_AXI_M17_IDLE is used by the performance monitor
0	M16_PII	SW : RW 0x1: The internally generated idle status for Master 16 will be used by the performance monitor 0x0: Primary input I_AXI_M16_IDLE is used by the performance monitor

0x01403D0C AFAB_FABRIC_MONITOR_RTR_MASK_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains 1 bit for each of the tenure counters that controls the RTR assertion and clearing of the monitoring results pertaining to the associated tenure counter to account for errors due to starting the monitor in the middle of traffic. A value of 1 indicates that RTR will not be asserted.

AFAB_FABRIC_MONITOR_RTR_MASK_REG

Bits	Name	Description
31:4	RESERVED_31_4	Reserved
3	RTR_MASK_3	SW : RW 0x1: No RTR will be asserted for Tenure Counter 3 0x0: The design is allowed to assert RTR for Tenure Counter 3
2	RTR_MASK_2	SW : RW 0x1: No RTR will be asserted for Tenure Counter 2 0x0: The design is allowed to assert RTR for Tenure Counter 2
1	RTR_MASK_1	SW : RW 0x1: No RTR will be asserted for Tenure Counter 1 0x0: The design is allowed to assert RTR for Tenure Counter 1
0	RTR_MASK_0	SW : RW 0x1: No RTR will be asserted for Tenure Counter 0 0x0: The design is allowed to assert RTR for Tenure Counter 0

0x01403D10 AFAB_FABRIC_MASTER_SELECT_HYST_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 0 to Master 15). A value of 1 indicates that the hysteresis timer value is used to keep the master segmented clock on. A value of 0 indicates that the hysteresis timer will not be used in the master segmented clock on.

AFAB_FABRIC_MASTER_SELECT_HYST_LOWER_REG

Bits	Name	Description
15	M15_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

AFAB_FABRIC_MASTER_SELECT_HYST_LOWER_REG (cont.)

Bits	Name	Description
14	M14_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
13	M13_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
12	M12_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
11	M11_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
10	M10_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
9	M9_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
8	M8_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
7	M7_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
6	M6_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
5	M5_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

AFAB_FABRIC_MASTER_SELECT_HYST_LOWER_REG (cont.)

Bits	Name	Description
4	M4_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
3	M3_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
2	M2_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
1	M1_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
0	M0_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

0x01403D14 AFAB_FABRIC_MASTER_SELECT_HYST_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 16to Master 31). A value of 1 indicates that the hysteresis timer value is used to keep the master segmented clock on. A value of 0 indicates that the hysteresis timer will not be used in the master segmented clock on.

AFAB_FABRIC_MASTER_SELECT_HYST_UPPER_REG

Bits	Name	Description
15	M31_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
14	M30_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

AFAB_FABRIC_MASTER_SELECT_HYST_UPPER_REG (cont.)

Bits	Name	Description
13	M29_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
12	M28_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
11	M27_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
10	M26_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
9	M25_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
8	M24_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
7	M23_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
6	M22_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
5	M21_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
4	M20_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

AFAB_FABRIC_MASTER_SELECT_HYST_UPPER_REG (cont.)

Bits	Name	Description
3	M19_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
2	M18_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
1	M17_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
0	M16_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

0x01403D18 AFAB_FABRIC_MASTER_USE_CG_DISABLE_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 0 to Master 15). A value of 1 indicates that the FMCHR bit 15 can be used to always keep the master segmented clock on, hence disabling HW dynamic clock gating. A value of 0 indicates that the FMCHR bit cannot be used to disable HW dynamic clock gating.

AFAB_FABRIC_MASTER_USE_CG_DISABLE_LOWER_REG

Bits	Name	Description
15	M15_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 15 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
14	M14_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 14 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

AFAB_FABRIC_MASTER_USE_CG_DISABLE_LOWER_REG (cont.)

Bits	Name	Description
13	M13_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 13 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
12	M12_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 12 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
11	M11_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 11 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
10	M10_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 10 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
9	M9_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 9 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
8	M8_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 8 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
7	M7_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 7 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
6	M6_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 6 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
5	M5_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 5 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

AFAB_FABRIC_MASTER_USE_CG_DISABLE_LOWER_REG (cont.)

Bits	Name	Description
4	M4_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 4 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
3	M3_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 3 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
2	M2_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 2 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
1	M1_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 1 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
0	M0_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 0 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

0x01403D1C AFAB_FABRIC_MASTER_USE_CG_DISABLE_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 16 to Master 31). A value of 1 indicates that the FMCHR bit 15 can be used to always keep the master segmented clock on, hence disabling HW dynamic clock gating. A value of 0 indicates that the FMCHR bit cannot be used to disable HW dynamic clock gating.

AFAB_FABRIC_MASTER_USE_CG_DISABLE_UPPER_REG

Bits	Name	Description
15	M31_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 31 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

AFAB_FABRIC_MASTER_USE_CG_DISABLE_UPPER_REG (cont.)

Bits	Name	Description
14	M30_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 30 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
13	M29_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 29 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
12	M28_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 28 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
11	M27_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 27 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
10	M26_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 26 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
9	M25_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 25 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
8	M24_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 24 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
7	M23_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 23 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
6	M22_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 22 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

AFAB_FABRIC_MASTER_USE_CG_DISABLE_UPPER_REG (cont.)

Bits	Name	Description
5	M21_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 21 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
4	M20_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 20 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
3	M19_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 19 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
2	M18_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 18 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
1	M17_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 17 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
0	M16_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 16 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

0x01403D20 AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter0.

AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG0

Bits	Name	Description
15:0	RTENL0	SW : RW Contains the LSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked bytenure counter 0

0x01403D24 AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter0.

AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG0

Bits	Name	Description
15:0	RTENU0	SW : RW Contains the MSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 0

0x01403D28 AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter1.

AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG1

Bits	Name	Description
15:0	RTENL1	SW : RW Contains the LSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 1.

0x01403D2C AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter1.

AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG1

Bits	Name	Description
15:0	RTENU1	SW : RW Contains the MSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 1.

0x01403D30 AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter2.

AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG2

Bits	Name	Description
15:0	RTENL2	SW : RW Contains the LSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 2

0x01403D34 AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter2.

AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG2

Bits	Name	Description
15:0	RTENU2	SW : RW Contains the MSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 2

0x01403D38 AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter3.

AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG3

Bits	Name	Description
15:0	RTENL3	SW : RW Contains the LSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 3

0x01403D3C AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter3.

AFAB_FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG3

Bits	Name	Description
15:0	RTENU3	SW : RW Contains the MSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 3

8.5 Application Fabric M2VMT Registers (0x01400000 AFAB_BASE)

This section contains the Application Fabric M2VMT registers.

8.5.1 M2VMT registers map with generic permutations

REMOVE_M2VMT_RPU = '0' &
REMOVE_M2VMT_SYND_REG_IF_RPU_IS_PRESENT='0'

The normal default use model uses M2VMT_RPU='0' and REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT= '0'. In this default configuration, local RPU and associated syndrome registers and interrupt support registers are available.

See Table 1-3 Bases in Address Order

Table 8-3 Application Fabric M2VMT Registers Table

Register	Address / Range	Description	Type	Default
M2VMT_M2VRv [4:0]	x000 to x7FC	Defines VMID value associated with the M2VMT index:		
Where v = NUM_M2VMT_ENTRIES from the design generic	R/W	x		
Reserved	x800 to xFF0	Reserved	X	X
M2VMT_REV	xFF4	M2VMT Revision Register	RO	'10000000'b
M2VMT_IDR [8:0]	xFF8	ID Register	RO	NUM_M2VMT_ENTRIES
Reserved	xFFC	Reserved	X	x

8.5.2 M2VMT VMID mapping registers

0x01404000+ 0x4*v AFAB_M2VMT_M2VMRv_0, v=[0..1]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics

AFAB_M2VMT_M2VMRv_0

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRv address associations.

0x01404FF4 AFAB_M2VMT_REV_0

Type: Read
Clock: FABRIC_CLOCK
Reset State: '10000000'b

Reports the revision information for the M2VMT core and wrapper.

AFAB_M2VMT_REV_0

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

0x01404FF8 AFAB_M2VMT_IDR_0

Type: Read
Clock: FABRIC_CLOCK
Reset State: M2VMTSIZE

Reports the size of the M2VMT table. It is a read-only register.

AFAB_M2VMT_IDR_0

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

AFAB_M2VMT_IDR_0 (cont.)

Bits	Name	Description
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x01405000+0x4*v AFAB_M2VMT_M2VMRv_1, v=[0..1]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics

AFAB_M2VMT_M2VMRv_1

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRv address associations.

0x01405FF4 AFAB_M2VMT_REV_1

Type: Read
Clock: FABRIC_CLOCK
Reset State: '10000000'b

Reports the revision information for the M2VMT core and wrapper.

AFAB_M2VMT_REV_1

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

0x01405FF8 AFAB_M2VMT_IDR_1

Type: Read
Clock: FABRIC_CLOCK
Reset State: M2VMTSIZE

Reports the size of the M2VMT table. It is a read-only register.

AFAB_M2VMT_IDR_1

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

8.6 Smart Peripheral Subsystem Fabric Registers (0x01500000 DAY_CFG_BASE)

This section contains the Smart Peripheral Subsystem Fabric registers.

8.6.1 Smart Peripheral Subsystem Configuration Registers

0x01500000 DAY_CFG_FABRIC_ID_REVISION_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x2840

This register contains the upper 16-bits of the core ID and revision number and contains the Major/Minor Revision information, as well as the site ID where the core was developed.

DAY_CFG_FABRIC_ID_REVISION_REG0

Bits	Name	Description
15:13	MAJ	SW : R Major Revision 0x1: Initial Release
12:10	MIN	SW : R Minor Revision 0x0: Voyager 0x1: Phantom 0x2: Blackbird Rev2.0
9:6	SITE	SW : R Site ID 0x1: RTP
5:0	RESERVED_BITS_5_0	

0x01500004 DAY_CFG_FABRIC_ID_REVISION_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0001

This register contains the lower 16-bits of the core ID and revision number and contains the Core ID number.

DAY_CFG_FABRIC_ID_REVISION_REG1

Bits	Name	Description
15:8	RESERVED_BITS_3_2	

DAY_CFG_FABRIC_ID_REVISION_REG1 (cont.)

Bits	Name	Description
7:0	ID	SW : R Core ID 0x1: FABRIC

0x01500008 DAY_CFG_FABRIC_CONFIGURATION_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0002

This register defines the operating frequency, power down mode for the performance monitor, as well as the decode error and performance monitor cycle counter interrupts.

The ISYND bits contain the interrupt syndrome. If more than one interrupt type occurs, more than one bit will be set. For example, if a decode error occurs and the performance monitor cycle-counter expires, the ISYND field will contain the value 3'b101. Performance monitor interrupts are only generated when the interrupt enable (PMIE) bit is set for the interrupt type.

If multiple decode errors occur, only the first error is recorded. If multiple decode errors occur at the same clock cycle, only a single error is considered, with Master 0 having the highest priority and Master 2 the lowest priority.

The determination of the time an error is recorded in the Fabric Error Status Register (FESR) is based on the following criteria:

For Reads: When Mn_RLAST is asserted.

For Writes: When Mn_BRESP is asserted.

Therefore, if two different masters make requests with invalid addresses to the FABRIC, the master which receives the RLAST or BRESP first for the invalid transaction, is recorded in the FESR. See FABRIC_ERROR_STATUS_REG_1 for information that is captured when a decode error occurs. The address of the request which caused a decode error is captured in the FABRIC_ERROR_UPPER_ADDR_REG and the FABRIC_ERROR_LOWER_ADDR_REG. If they happen simultaneously, the master priority is used to resolve which error is recorded in a fixed priority scheme. Master 0 has highest priority and Master 31 has the lowest priority.

NOTE If the master does not have RREADY or BREADY asserted by default (i.e., it is not able to receive all responses for outstanding requests and may throttle the FABRIC), the FABRIC_Interrupt generation may precede the return of the last read data beat or the write response.

To clear the interrupt, the ISYND bits are required to be written to 3'b000.

The performance monitor event/tenure overflow condition is indicated when the ISYND value is 010. An event overflow occurs when the event counter has reached its maximum value. A tenure overflow condition occurs:

When the tenure counter has reached its maximum value

OR

More than 16 tenures are outstanding, since the performance monitor implements only 16 counters for tenure tracking. Note that if the tenure overflows, values read from the performance monitors for min/max/total/last tenure will no longer be valid as values recorded after the overflow will be incorrect.

DAY_CFG_FABRIC_CONFIGURATION_REG

Bits	Name	Description
15:7	RESERVED_BITS_15_7	Reserved Bits
6:4	ISYND	SW : RW Interrupt syndrome* 0x0: No/Clear (interrupt) 0x1: Cycle counter expired (Perfmon) 0x2: Event/tenure overflow (Perfmon) 0x4: Decode error detected 0x5: MPU Error 0x6: Timeout Error (SPB)
3:2	RESERVED_BITS_3_2	
1	PPDM	SW : RW Performance monitor power down/disable mode 0x0: Monitor Enabled 0x1: Monitor Disabled (Gates clocks to performance monitor registers)
0	PMIE	SW : RW Perfmon interrupt enable

0x01500100+4*n DAY_CFG_FABRIC_SEGMENT_UADDR_0_REG_n, n=[0..3]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the upper and lower address ranges for a particular slave segment (n).If this slave segment (n) is a link then this register defines the first address range for the slave link.

NOTE A segmentation address register is required for each slave segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

DAY_CFG_FABRIC_SEGMENT_UADDR_0_REG_n

Bits	Name	Description
15:10	RESERVED_15_10	
9:0	SUA	SW : RW Segment 'n' upper address (based on parameter- up to 10-bits)

0x01500200+4*n DAY_CFG_FABRIC_SEGMENT_LADDR_0_REG_n, n=[0..3]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the upper and lower address ranges for a particular slave segment (n). If this slave segment (n) is a link then this register defines the first address range for the slave link.

NOTE A segmentation address register is required for each slave segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

DAY_CFG_FABRIC_SEGMENT_LADDR_0_REG_n

Bits	Name	Description
15	SSE	SW : RW Slave segment n enable

DAY_CFG_FABRIC_SEGMENT_LADDR_0_REG_n (cont.)

Bits	Name	Description
14	SSIE	SW : RW Slave segment 'n' & 'n+1' nterleave enable
13:10	RESERVED_13_10	
9:0	SLA	SW : RW Segment n lower address (based on parameter- up to 10-bits)

0x01500300+4*n DAY_CFG_FABRIC_SEGMENT_UADDR_1_REG_n, n=[0..3]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the upper address for a particular slave link segment (n) if it's a link. A link segment can have up to two separate address ranges. This register defines the second address range for the slave link.

NOTE A link segmentation address register is required for each slave link segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

DAY_CFG_FABRIC_SEGMENT_UADDR_1_REG_n

Bits	Name	Description
15:10	RESERVED_15_10	
9:0	SUA	SW : RW Segment 'n' upper address (based on parameter- up to 10-bits)

0x01500400+4*n DAY_CFG_FABRIC_SEGMENT_LADDR_1_REG_n, n=[0..3]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the lower address range for a particular slave link segment (n). A link segment can have up to two separate address ranges. This register defines the second address range for the slave link.

NOTE A segmentation link address register is required for each slave link segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

DAY_CFG_FABRIC_SEGMENT_LADDR_1_REG_n

Bits	Name	Description
15:10	RESERVED_15_10	
9:0	SLA	SW : RW Segment n lower address (based on parameter- up to 10-bits)

0x01501000+0x0100*n+4*m DAY_CFG_FABRIC_m_WEIGHTING_REG_n, m=[0..2], n=[0..3]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

The values programmed into this register determine the Tier 2 weight for each master under the Tier Based Arbitration Scheme.

NOTE This register is required for each master and each slave segment supported by the FABRIC .

DAY_CFG_FABRIC_m_WEIGHTING_REG_n

Bits	Name	Description
15:8	RESERVED_BITS_15_8	
7:0	M_M_W	SW : RW Master 'm' Weight

0x01502000+ 0x0100*n+4* m **DAY_CFG_FABRIC_m_QOS_REG_n, m=[0..3], n=[0..3]**

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

The values programmed into this register determine the Tier 1 weight for each master under the Tier Based Arbitration Scheme. Only 4 master ports can be configured as Tier 1. The QMC bits are used to configure a master port as Tier 1.

NOTE If more than one of these QOS Control registers are set to the same master port, unpredictable behavior will occur.

Set-up procedure:

1. Set the QOS enable bit.
2. Set the arbitration mode to Scheduled Access Time in the FABRIC arbitration configuration register FACR (See FABRIC_ARBITRATION_CONTROL_REG_n, n=[0..3]).
3. Configure the master port that needs to be set to Tier1.
4. Set the appropriate number of tokens/weight.
5. Set the MLT value (default is zero clock cycles).

NOTE Four of these registers are required for each slave segment supported by the FABRIC .

DAY_CFG_FABRIC_m_QOS_REG_n

Bits	Name	Description
15:14	RESERVED_BITS15_13	
13:10	MLT	SW : RW MLT Value
9	QE	SW : RW QOS Enable

DAY_CFG_FABRIC_m_QOS_REG_n (cont.)

Bits	Name	Description
8:4	QMC	SW : RW QOS Master Configuration 0x0: Master Port 0 0x1: Master Port 1 0x2: Master Port 2 0x3: Master Port 3 0x4: Master Port 4 0x5: Master Port 5 0x6: Master Port 6 0x7: Master Port 7 0x8: Master Port 8 0x9: Master Port 9 0xA: Master Port 10 0xB: Master Port 11 0xC: Master Port 12 0xD: Master Port 13 0xE: Master Port 14 0xF: Master Port 15 0x10: Master Port 16 0x11: Master Port 17 0x12: Master Port 18 0x13: Master Port 19 0x14: Master Port 20 0x15: Master Port 21 0x16: Master Port 22 0x17: Master Port 23 0x18: Master Port 24 0x19: Master Port 25 0x1A: Master Port 26 0x1B: Master Port 27 0x1C: Master Port 28 0x1D: Master Port 29 0x1E: Master Port 30 0x1F: Master Port 31
3:0	M_M_QW	SW : RW Master 'm' QOS Weight

0x01503000+4*n DAY_CFG_FABRIC_BUS_INTERVAL_REG_n, n=[0..3]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register sets the bus interval value for Tier 2 masters.

NOTE A control register is implemented for each slave segment supported by the FABRIC .

DAY_CFG_FABRIC_BUS_INTERVAL_REG_n

Bits	Name	Description
15:0	IBI	SW : RW Intct bus interval (in clock cycles)

0x01503100+4*n DAY_CFG_FABRIC_QOS_INTERVAL_REG_n, n=[0..3]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register sets the QOS interval value for Tier 1 masters.

NOTE A control register is required for each slave segment supported by the FABRIC .

DAY_CFG_FABRIC_QOS_INTERVAL_REG_n

Bits	Name	Description
15:8	RESERVED_BITS15_8	
7:0	QBI	SW : RW QOS bus interval (in clock cycles)

0x01503200+4*n DAY_CFG_FABRIC_ARBITRATION_CONTROL_REG_n, n=[0..3]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x00FF

This register controls the arbitration mode and the pipeline depth of a particular slave segment.

NOTE A control register is implemented for each slave segment supported by the FABRIC .

DAY_CFG_FABRIC_ARBITRATION_CONTROL_REG_n

Bits	Name	Description
15	QLP	SW : RW QOS Timer Low Power Mode 0x1: Enable 0x0: Disable
14:13	QHI	SW : RW QOS Timer Halt Interval 0x0: Stop after 1 interval of inactivity 0x1: Stop after 2 intervals of inactivity 0x2: Stop after 4 intervals of inactivity 0x3: Stop after 8 intervals of inactivity
12	BLP	SW : RW Bus Interval Low Power Mode 0x1: Enable 0x0: Disable
11:10	BHI	SW : RW Bus Interval Halt Interval 0x0: Stop after 1 interval of inactivity 0x1: Stop after 2 intervals of inactivity 0x2: Stop after 4 intervals of inactivity 0x3: Stop after 8 intervals of inactivity
9	QCE	SW : RW QoS Channel Enable 0x0: Disable (default) 0x1: Enable
8	IAM	SW : RW FABRIC arbitration mode 0x0: Fair round-robin (default) 0x1: Scheduled access time

DAY_CFG_FABRIC_ARBITRATION_CONTROL_REG_n (cont.)

Bits	Name	Description
7:4	IRPD	SW : RW FABRIC read pipeline depth 0x0: Pipeline depth = 1 0x1: Pipeline depth = 2 0x2: Pipeline depth = 3 0x3: Pipeline depth = 4 0x4: Pipeline depth = 5 0x5: Pipeline depth = 6 0x6: Pipeline depth = 7 0x7: Pipeline depth = 8 0x8: Pipeline depth = 9 0x9: Pipeline depth = 10 0xA: Pipeline depth = 11 0xB: Pipeline depth = 12 0xC: Pipeline depth = 13 0xD: Pipeline depth = 14 0xE: Pipeline depth = 15 0xF: Pipeline depth = 16
3:0	IWPD	SW : RW FABRIC Write Pipeline Depth 0x0: Pipeline depth = 1 0x1: Pipeline depth = 2 0x2: Pipeline depth = 3 0x3: Pipeline depth = 4 0x4: Pipeline depth = 5 0x5: Pipeline depth = 6 0x6: Pipeline depth = 7 0x7: Pipeline depth = 8 0x8: Pipeline depth = 9 0x9: Pipeline depth = 10 0xA: Pipeline depth = 11 0xB: Pipeline depth = 12 0xC: Pipeline depth = 13 0xD: Pipeline depth = 14 0xE: Pipeline depth = 15 0xF: Pipeline depth = 16

0x01503300+4*n DAY_CFG_FABRIC_MASTER_INTERFACE_REG_n, n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x4084

This register controls the following master port attributes:

- whether the master request priority signals are used by the internal arbiter
- the redirection of cacheable coherent requests
- write gathering on AXI
- write packing on AHB

This register also controls a particular master's halt interface and for AHB master interfaces, it enables write packing functionality for posted writes.

When the MHR bit is set, the FABRIC_MnHALTREQ signal is asserted. The MHA and MHI fields capture the state of the FABRIC_MnHALTACK and FABRIC_MnIDLE signals at every clock cycle.

NOTE A register is implemented for each master interface supported by the FABRIC .SW should disable OWGM bit for AXI ports .

DAY_CFG_FABRIC_MASTER_INTERFACE_REG_n

Bits	Name	Description
15	RESERVED_BIT_15	
14	OWGM	SW : RW Enable optimized write gathering mode
13	DBW	SW : RW Disable Bufferable writes. Treats Bufferable writes as Non Bufferable writes (AHB only)
12	PRIEN	SW : RW Enable Request Priority Lets the slave way arbiter consider the master request priority AREQPRIORITY[1:0] signal that is driven with each transaction
11	RCOSH	SW : RW Redirect Cacheable-outer-sharable Governs whether or not cacheable accesses that are outer-sharable are redirected to the Scorpion-MP L2 slave port
10	RCISH	SW : RW Redirect Cacheable-inner-sharable Governs whether or not cacheable accesses that are inner-sharable are redirected to the Scorpion-MP L2 slave port
9	RCNSH	SW : RW Redirect Cacheable-non-sharable Governs whether or not cacheable accesses that are non-sharable are redirected to the Scorpion-MP L2 slave port
8	CRE	SW : RW Enable redirection of cachable coherent requests
7	WGE	SW : RW Write Gathering Enable (AXI only)

DAY_CFG_FABRIC_MASTER_INTERFACE_REG_n (cont.)

Bits	Name	Description
6	WPE	SW : RW Write Packing Enable (AHB Only) When enabled, the master port will pack indeterminate INCR burst writes, if disabled, the master port will break indeterminate INCR burst writes into SINGLES. 0x1: Enable 0x0: Disable
5:4	IIIW	SW : RW Bufferable Indeterminate INCR WR packing (AHB only): 0x0: break into INCR4 0x1: break into INCR8 0x3: break into INCR16
3	MID	SW : RW Master Interface Disable. SW diable of Master interface.
2	MI	SW : R Master Idle. Indicates that the Master does not have any pending bus transactions. For AHB busses, this bit is set internally by the FABRIC AHB Master port. For AXI masters, this value is driven by the master that is connected to the port.
1	MHA	SW : R Master halt acknowledge. Only valid for AXI masters. This bit is 0 on AHB master ports.
0	MHR	SW : RW Master halt request. Only valid for AXI masters. Writing this bit has no effect for AHB masters.

0x01503430 DAY_CFG_FABRIC_SLAVE_ARBITRATION_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register disables the arbiter on a particular slave segment. The arbiter stalls and stops granting requests to a slave until the arbiter is re-enabled. These registers allow for the slave way to be stalled while reconfiguring a slave device or frequency scaling the slave way.

DAY_CFG_FABRIC_SLAVE_ARBITRATION_REG

Bits	Name	Description
15	S15AD	SW : R Slave 15 Arbitration Disable 0x1: Disables slave segment arbiter 0x0: Enables slave segment arbiter

DAY_CFG_FABRIC_SLAVE_ARBITRATION_REG (cont.)

Bits	Name	Description
14	S14AD	SW : R Slave 14 Arbitration Disable
13	S13AD	SW : R Slave 13 Arbitration Disable
12	S12AD	SW : R Slave 12 Arbitration Disable
11	S11AD	SW : R Slave 11 Arbitration Disable
10	S10AD	SW : R Slave 10 Arbitration Disable
9	S9AD	SW : R Slave 9 Arbitration Disable
8	S8AD	SW : R Slave 8 Arbitration Disable
7	S7AD	SW : R Slave 7 Arbitration Disable
6	S6AD	SW : R Slave 6 Arbitration Disable
5	S5AD	SW : R Slave 5 Arbitration Disable
4	S4AD	SW : R Slave 4 Arbitration Disable
3	S3AD	SW : R Slave 3 Arbitration Disable
2	S2AD	SW : R Slave 2 Arbitration Disable
1	S1AD	SW : R Slave 1 Arbitration Disable
0	S0AD	SW : R Slave 0 Arbitration Disable

0x01503434 DAY_CFG_FABRIC_SLAVE_BYPASS_BUFFER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register enables the bypass buffer functionality in a slave way (if implemented).

DAY_CFG_FABRIC_SLAVE_BYPASS_BUFFER_REG

Bits	Name	Description
15	S15BE	SW : RW Slave 15 Bypass Buffer Enable
14	S14BE	SW : RW Slave 14 Bypass Buffer Enable
13	S13BE	SW : RW Slave 13 Bypass Buffer Enable
12	S12BE	SW : RW Slave 12 Bypass Buffer Enable
11	S11BE	SW : RW Slave 11 Bypass Buffer Enable
10	S10BE	SW : RW Slave 10 Bypass Buffer Enable
9	S9BE	SW : RW Slave 9 Bypass Buffer Enable
8	S8BE	SW : RW Slave 8 Bypass Buffer Enable
7	S7BE	SW : RW Slave 7 Bypass Buffer Enable
6	S6BE	SW : RW Slave 6 Bypass Buffer Enable
5	S5BE	SW : RW Slave 5 Bypass Buffer Enable
4	S4BE	SW : RW Slave 4 Bypass Buffer Enable
3	S3BE	SW : RW Slave 3 Bypass Buffer Enable
2	S2BE	SW : RW Slave 2 Bypass Buffer Enable

DAY_CFG_FABRIC_SLAVE_BYPASS_BUFFER_REG (cont.)

Bits	Name	Description
1	S1BE	SW : RW Slave 1 Bypass Buffer Enable
0	S0BE	SW : RW Slave 0 Bypass Buffer Enable

0x01503438 DAY_CFG_FABRIC_SLAVE_STATUS_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the status of each slave.

- A 1 indicates that the slave is idle.
- A 0 indicates that the slave is busy processing a transfer and/or the FABRIC is has not completed sending transactions to the slave.

DAY_CFG_FABRIC_SLAVE_STATUS_REG

Bits	Name	Description
15	S15S	SW : R Slave 15 Status
14	S14S	SW : R Slave 14 Status
13	S13S	SW : R Slave 13 Status
12	S12S	SW : R Slave 12 Status
11	S11S	SW : R Slave 11 Status
10	S10S	SW : R Slave 10 Status
9	S9S	SW : R Slave 9 Status
8	S8S	SW : R Slave 8 Status
7	S7S	SW : R Slave 7 Status

DAY_CFG_FABRIC_SLAVE_STATUS_REG (cont.)

Bits	Name	Description
6	S6S	SW : R Slave 6 Status
5	S5S	SW : R Slave 5 Status
4	S4S	SW : R Slave 4 Status
3	S3S	SW : R Slave 3 Status
2	S2S	SW : R Slave 2 Status
1	S1S	SW : R Slave 1 Status
0	S0S	SW : R Slave 0 Status

0x01503500 DAY_CFG_FABRIC_TEST_INTERFACE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls:

- the grouping of signals that are driven out on the test bus (FABRIC_TESTBUS[31:0])
- Selection of MISR slave way and channel input

MEN: Selects which MISR output is driven onto the test-bus. For example, setting MEN to 00010 selects the MISR in slave segment 2. The MEN bits are only valid when the testmode (TMODE) is set to 000000 and test-enable is set (TEN)

TMODE: Selects the various test-bus modes

TEN: Test-enable. Must be set for values to be driven onto the test-bus OR for MISR to be enabled.

DAY_CFG_FABRIC_TEST_INTERFACE_REG

Bits	Name	Description
15:14	RESERVED_BITS15_14	

DAY_CFG_FABRIC_TEST_INTERFACE_REG (cont.)

Bits	Name	Description
13:12	MSEL	SW : RW MISR input selection: 0x0: Address channel 0x1: Write channel 0x2: Read channel 0x3: Write response channel
11:7	MEN	SW : RW MISR Enable 0x1: Slave Segment 0 0x2: Slave Segment 1 0x3: Slave Segment 2 0x4: Slave Segment 3 0x5: Slave Segment 4 0x6: Slave Segment 5 0x7: Slave Segment 6 0x8: Slave Segment 7 0x9: Slave Segment 8 0xA: Slave Segment 9 0xB: Slave Segment 10 0xC: Slave Segment 11 0xD: Slave Segment 12 0xE: Slave Segment 13 0xF: Slave Segment 14 0x10: Slave Segment 15

DAY_CFG_FABRIC_TEST_INTERFACE_REG (cont.)

Bits	Name	Description
6:1	TMODE	SW : RW Test Mode: 0x0: Testbus M0 0x1: Testbus M1 0x2: Testbus M2 0x3: Testbus M3 0x4: Testbus M4 0x5: Testbus M5 0x6: Testbus M6 0x7: Testbus M7 0x8: Testbus M8 0x9: Testbus M9 0xA: Testbus M10 0xB: Testbus M11 0xC: Testbus M12 0xD: Testbus M13 0xE: Testbus M14 0xF: Testbus M15 0x10: Testbus M16 0x11: Testbus M17 0x12: Testbus M18 0x13: Testbus M19 0x14: Testbus M20 0x15: Testbus M21 0x16: Testbus M22 0x17: Testbus M23 0x18: Testbus M24 0x19: Testbus M25 0x1A: Testbus M26 0x1B: Testbus M27 0x1C: Testbus M28 0x1D: Testbus M29 0x1E: Testbus M30 0x1F: Testbus M31 0x20: Testbus S0 0x21: Testbus S1 0x22: Testbus S2 0x23: Testbus S3 0x24: Testbus S4 0x25: Testbus S5 0x26: Testbus S6 0x27: Testbus S7 0x28: Testbus S8 0x29: Testbus S9 0x2A: Testbus S10 0x2B: Testbus S11 0x2C: Testbus S12

DAY_CFG_FABRIC_TEST_INTERFACE_REG (cont.)

Bits	Name	Description
		0x2D: Testbus S13 0x2E: Testbus S14 0x2F: Testbus S15 0x30: Reserved_1 0x31: Reserved_2 0x32: Reserved_3 0x33: Reserved_4 0x34: Reserved_5 0x35: Reserved_6 0x36: Reserved_7 0x37: Reserved_8 0x38: Reserved_9 0x39: Reserved_10 0x3A: Reserved_11 0x3B: Reserved_12 0x3C: Reserved_13 0x3D: Reserved_14 0x3E: Reserved_15 0x3F: Reserved_16
0	TEN	SW : RW Test Enable

0x01503504 DAY_CFG_FABRIC_ERROR_STATUS_REG_0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

DAY_CFG_FABRIC_ERROR_STATUS_REG_0

Bits	Name	Description
15:0	MID	SW : R AMID for AXI port HMID for AHB port

0x01503508 DAY_CFG_FABRIC_ERROR_STATUS_REG_1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

DAY_CFG_FABRIC_ERROR_STATUS_REG_1

Bits	Name	Description
15:8	TID	SW : R Transaction ID Only Applicable for AXI Transfers ZERO for AHB Transfers
7:6	RESERVED_BITS_7_6	Reserved
5:0	MPORT	SW : R Master port that generated the error

0x0150350C DAY_CFG_FABRIC_ERROR_STATUS_REG_2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

DAY_CFG_FABRIC_ERROR_STATUS_REG_2

Bits	Name	Description
15:12	RESERVED_BITS_15_12	Reserved
11	BURST	SW : R Burst transfer
10	OOOWR	SW : R OOO write response Only Applicable for AXI
9	OOORD	SW : R OOO read response Only Applicable for AXI

DAY_CFG_FABRIC_ERROR_STATUS_REG_2 (cont.)

Bits	Name	Description
8:7	LOCK	SW : R Lock Transfer
6:4	SIZE	SW : R Transfer Size
3:0	TYPE	SW : R Transfer Type Only Applicable for AXI

0x01503510 DAY_CFG_FABRIC_ERROR_STATUS_REG_3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

DAY_CFG_FABRIC_ERROR_STATUS_REG_3

Bits	Name	Description
15:8	RESERVED_BITS_15_8	Reserved
7	PROTNS	SW : R APROTNS/HPROTNS
6	PROTIND	SW : R PROTIND
5	AISH	SW : R Inner Shared
4	WRITE	SW : R Write transfer
3:0	LEN	SW : R Transfer Length

0x01503514 DAY_CFG_FABRIC_ERROR_UPPER_ADDR_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address of the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

DAY_CFG_FABRIC_ERROR_UPPER_ADDR_REG

Bits	Name	Description
15:0	EUA	SW : R Bits [31:16] of the address which generated a decode error

0x01503518 DAY_CFG_FABRIC_ERROR_LOWER_ADDR_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address of the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

DAY_CFG_FABRIC_ERROR_LOWER_ADDR_REG

Bits	Name	Description
15:0	ELR	SW : R Bits [15:0] of the address which generated a decode error

0x0150351C DAY_CFG_FABRIC_MISR_SIGNATURE_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG.

DAY_CFG_FABRIC_MISR_SIGNATURE_REG0

Bits	Name	Description
15:0	SIG0	SW : R Bits [15:0] of 64-bit MISR signature

0x01503520 DAY_CFG_FABRIC_MISR_SIGNATURE_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG

DAY_CFG_FABRIC_MISR_SIGNATURE_REG1

Bits	Name	Description
15:0	SIG1	SW : R Bits [31:16] of 64-bit MISR signature

0x01503524 DAY_CFG_FABRIC_MISR_SIGNATURE_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 47:32 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG

DAY_CFG_FABRIC_MISR_SIGNATURE_REG2

Bits	Name	Description
15:0	SIG2	SW : R Bits [47:32] of 64-bit MISR signature

0x01503528 DAY_CFG_FABRIC_MISR_SIGNATURE_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 63:48 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG

DAY_CFG_FABRIC_MISR_SIGNATURE_REG3

Bits	Name	Description
15:0	SIG3	SW : R Bits [63:48] of 64-bit MISR signature

0x01503600+4*n DAY_CFG_FABRIC_MASTER_CLOCK_HALT_REG_n, n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt & change functionality within the FABRIC master ports. To enable the clock halting functionality, the clock halt enable bit (CHTEN) needs to be set. The hysteresis timer value is a 10-bit timer (running on FCLK) value that is set using the CHTMR bits. The clock change and MODE bits are used to change the interface between sync/async/isosync modes.

NOTE A register is implemented for each master interface supported by the FABRIC .

DAY_CFG_FABRIC_MASTER_CLOCK_HALT_REG_n

Bits	Name	Description
15	CHTEN	SW : RW Clock halt enable. Enables clock halt functionality for this port.
14	CCDONE	SW : RW Clock mode change completed/done
13	CCACK	SW : R Clock mode change acknowledge
12	CCREQ	SW : RW Clock mode change request
11:10	MODE	SW : RW Master clock interface mode 0x0: ASYNC 0x1: SYNC 0x2: ISOSYNC port clk slower. 0x3: ISOSYNC port clk faster.
9:0	CHTMR	SW : RW Master clock halt timer: clock cycles of inactivity that should pass before clock is halted

0x01503800+4*n DAY_CFG_FABRIC_SLAVE_CLOCK_HALT_REG_n, n=[0..3]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt & change functionality within the FABRIC slave ways. To enable the clock halting functionality, the clock halt enable bit (CHTEN) needs to be set. The hysteresis timer value is a 10-bit timer (running on FCLK) value that is set using the CHTMR bits. The clock change and MODE bits are used to change the interface between sync/async/isosync modes.

NOTE A register is implemented for each slave interface supported by the FABRIC .

DAY_CFG_FABRIC_SLAVE_CLOCK_HALT_REG_n

Bits	Name	Description
15	CHTEN	SW : RW Clock halt enable. Enables clock halt functionality for this port.
14	CCDONE	SW : RW Cock mode change completed/done
13	CCACK	SW : RW Clock mode change acknowledge
12	CCREQ	SW : RW Clock mode change request
11:10	MODE	SW : RW Slave clock interface mode 0x0: ASYNC 0x1: SYNC 0x2: ISOSYNC port clk slower. 0x3: ISOSYNC port clk faster.
9:0	CHTMR	SW : RW Slave clock halt timer: clock cycles of inactivity that should pass before clock is halted

0x01503880 DAY_CFG_FABRIC_SLAVE_ARBITER_CLOCK_HALT_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt functionality within the FABRIC slave ways arbiter.

DAY_CFG_FABRIC_SLAVE_ARBITER_CLOCK_HALT_REG

Bits	Name	Description
15	S15CHTEN	SW : RW S15 Arbiter Clock halt enable.
14	S14CHTEN	SW : RW S14 Arbiter Clock halt enable.
13	S13CHTEN	SW : RW S13 Arbiter Clock halt enable.
12	S12CHTEN	SW : RW S12 Arbiter Clock halt enable.
11	S11CHTEN	SW : RW S11 Arbiter Clock halt enable.
10	S10CHTEN	SW : RW S10 Arbiter Clock halt enable.
9	S9CHTEN	SW : RW S9 Arbiter Clock halt enable.
8	S8CHTEN	SW : RW S8 Arbiter Clock halt enable.
7	S7CHTEN	SW : RW S7 Arbiter Clock halt enable.
6	S6CHTEN	SW : RW S6 Arbiter Clock halt enable.
5	S5CHTEN	SW : RW S5 Arbiter Clock halt enable.
4	S4CHTEN	SW : RW S4 Arbiter Clock halt enable.
3	S3CHTEN	SW : RW S3 Arbiter Clock halt enable.
2	S2CHTEN	SW : RW S2 Arbiter Clock halt enable.
1	S1CHTEN	SW : RW S1 Arbiter Clock halt enable.
0	S0CHTEN	SW : RW S0 Arbiter Clock halt enable.

0x01503884+4*n DAY_CFG_FABRIC_SLAVE_CLOCK_ON_CFG_REG_n, n=[0..3]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt functionality within the FABRIC slave ways arbiter.

DAY_CFG_FABRIC_SLAVE_CLOCK_ON_CFG_REG_n

Bits	Name	Description
15:4	RESERVED_BITS_15_4	Reserved
3:0	COD	SW : RW AHB Slave Way Clock On Delay (in FCLK cycles)

0x015038F8 DAY_CFG_FABRIC_MONITOR_ENABLE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the trigger selection and enabling of event and cycle counters.

NOTE When PTRIG is set to use any of the external trigger signals, the external triggers incur a 2 cycle delay from the positive edge assertion of the signal to when the actual counters are enabled in the performance monitor. This allows synchronization of the external signals into the FABRIC clock domain.

DAY_CFG_FABRIC_MONITOR_ENABLE_REG

Bits	Name	Description
15:13	PTRIG	SW : RW 0x4: Int Trig/Ext Trig 0x3: Ext Trig 0x2: Ext Trig/CC expire 0x1: Int Trig/CC expire 0x0: Manual enable/CC expire (No trigger)
12	ECC	SW : RW Enable cycle counter
11:8	RESERVED_BITS_11_8	Reserved
7	EEC7	SW : RW Enable event counter 7

DAY_CFG_FABRIC_MONITOR_ENABLE_REG (cont.)

Bits	Name	Description
6	EEC6	SW : RW Enable event counter 6
5	EEC5	SW : RW Enable event counter 5
4	EEC4	SW : RW Enable event counter 4
3	EEC3	SW : RW Enable event counter 3
2	EEC2	SW : RW Enable event counter 2
1	EEC1	SW : RW Enable event counter 1
0	EEC0	SW : RW Enable event counter 0

0x015038FC DAY_CFG_FABRIC_MONITOR_RESET_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the resets for event and cycle counters.

DAY_CFG_FABRIC_MONITOR_RESET_REG

Bits	Name	Description
15:8	RESERVED_BITS_15_8	Reserved
7	REC7	SW : RW Reset event counter 7 (automatically resets the cycle-counter as well)
6	REC6	SW : RW Reset event counter 6 (automatically resets the cycle-counter as well)
5	REC5	SW : RW Reset event counter 5 (automatically resets the cycle-counter as well)
4	REC4	SW : RW Reset event counter 4 (automatically resets the cycle-counter as well)

DAY_CFG_FABRIC_MONITOR_RESET_REG (cont.)

Bits	Name	Description
3	REC3	SW : RW Reset event counter 3 (automatically resets the cycle-counter as well)
2	REC2	SW : RW Reset event counter 2 (automatically resets the cycle-counter as well)
1	REC1	SW : RW Reset event counter 1 (automatically resets the cycle-counter as well)
0	REC0	SW : RW Reset event counter 0 (automatically resets the cycle-counter as well)

0x01503900 DAY_CFG_FABRIC_MONITOR_TENURE_ENABLE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the trigger selection and enabling of tenure counters.

NOTE When PTRIG is set to use any of the external trigger signals, the external triggers incur a 2 cycle delay from the positive edge assertion of the signal to when the actual counters are enabled in the performance monitor. This allows synchronization of the external signals into the FABRIC clock domain.

DAY_CFG_FABRIC_MONITOR_TENURE_ENABLE_REG

Bits	Name	Description
15:4	RESERVED_BITS_15_4	Reserved
3	ETC3	SW : RW Enable tenure counter 3
2	ETC2	SW : RW Enable tenure counter 2
1	ETC1	SW : RW Enable tenure counter 1
0	ETC0	SW : RW Enable tenure counter 0

0x01503904 DAY_CFG_FABRIC_MONITOR_TENURE_RESET_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the resets for tenure counters and cycle counters.

DAY_CFG_FABRIC_MONITOR_TENURE_RESET_REG

Bits	Name	Description
15:4	RESERVED_BITS_15_4	Reserved
3	RTC3	SW : RW Reset tenure counter 3 (automatically resets the cycle-counter as well)
2	RTC2	SW : RW Reset tenure counter 2 (automatically resets the cycle-counter as well)
1	RTC1	SW : RW Reset tenure counter 1 (automatically resets the cycle-counter as well)
0	RTC0	SW : RW Reset tenure counter 0 (automatically resets the cycle-counter as well)

0x01503908 DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 0.

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG0

Bits	Name	Description
15:13	E0ES	SW : RW Event counter 0 event selection 0x0: Read burst 0 (Master/slave) 0x1: Write burst 0 (Master/slave) 0x2: Address transfer count 0 (Master/slave) 0x3: Read transfer count 0 (Master/slave) 0x4: Write transfer count 0 (Master/slave) 0x5: Write (bufferable burst 0 AHB Master only) 0x3: b110 ’ 3:b111: Reserved

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
12	RESERVED_BIT_12	Reserved
11	E0MIDFEN	SW : RW Event counter 0 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E0INDFEN	SW : RW Event counter 0 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E0IND	SW : RW Event counter 0 Instruction/Data selection 0x0: Data 0x1: Instruction

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
8:4	E0MPS	SW : RW Event counter 0 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
3:0	E0SWS	SW : RW Event counter 0 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0150390C DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 0.

DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG0

Bits	Name	Description
15:0	E0MID	SW : RW Event counter 0 MID selection (If MID filtering enabled)

0x01503910 DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 1.

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG1

Bits	Name	Description
15:13	E1ES	SW : RW Event counter 1event selection 0x0: Read burst 1 (Master/slave) 0x1: Write burst 1 (Master/slave) 0x2: Address transfer count 1 (Master/slave) 0x3: Read transfer count 1 (Master/slave) 0x4: Write transfer count 1 (Master/slave) 0x5: Write (bufferable burst 1 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E1MIDFEN	SW : RW Event counter 1 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E1INDFEN	SW : RW Event counter 1Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E1IND	SW : RW Event counter 1Instruction/Data selection 0x0: Data 0x1: Instruction

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
8:4	E1MPS	SW : RW Event counter 1Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
3:0	E1SWS	SW : RW Event counter 1Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01503914 DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 1.

DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG1

Bits	Name	Description
15:0	E1MID	SW : RW Event counter 1MID selection (If MID filtering enabled)

0x01503918 DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 2.

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG2

Bits	Name	Description
15:13	E2ES	SW : RW Event counter 2event selection 0x0: Read burst 2 (Master/slave) 0x1: Write burst 2 (Master/slave) 0x2: Address transfer count 2 (Master/slave) 0x3: Read transfer count 2 (Master/slave) 0x4: Write transfer count 2 (Master/slave) 0x5: Write (bufferable burst 2 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E2MIDFEN	SW : RW Event counter 2MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E2INDFEN	SW : RW Event counter 2Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E2IND	SW : RW Event counter 2Instruction/Data selection 0x0: Data 0x1: Instruction

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
8:4	E2MPS	SW : RW Event counter 2Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
3:0	E2SWS	SW : RW Event counter 2Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0150391C DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 2.

DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG2

Bits	Name	Description
15:0	E2MID	SW : RW Event counter 2 MID selection (If MID filtering enabled)

0x01503920 DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 3.

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG3

Bits	Name	Description
15:13	E3ES	SW : RW Event counter 3event selection 0x0: Read burst 3 (Master/slave) 0x1: Write burst 3 (Master/slave) 0x2: Address transfer count 3 (Master/slave) 0x3: Read transfer count 3 (Master/slave) 0x4: Write transfer count 3 (Master/slave) 0x5: Write (bufferable burst 3 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E3MIDFEN	SW : RW Event counter 3MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E3INDFEN	SW : RW Event counter 3Instruction/Data Filtering enable 0x0: Disabled 0x1: Enable
9	E3IND	SW : RW Event counter 3Instruction/Data selection 0x0: Data 0x1: Instruction

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
8:4	E3MPS	SW : RW Event counter 3Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
3:0	E3SWS	SW : RW Event counter 3 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01503924 DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 3.

DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG3

Bits	Name	Description
15:0	E3MID	SW : RW Event counter 3 MID selection (If MID filtering enabled)

0x01503928 DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 4.

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG4

Bits	Name	Description
15:13	E4ES	SW : RW Event counter 4event selection 0x0: Read burst 4 (Master/slave) 0x1: Write burst 4 (Master/slave) 0x2: Address transfer count 4 (Master/slave) 0x3: Read transfer count 4 (Master/slave) 0x4: Write transfer count 4 (Master/slave) 0x5: Write (bufferable burst 4AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E4MIDFEN	SW : RW Event counter 4 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E4INDFEN	SW : RW Event counter 4 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E4IND	SW : RW Event counter 4 Instruction/Data selection 0x0: Data 0x1: Instruction

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG4 (cont.)

Bits	Name	Description
8:4	E4MPS	SW : RW Event counter 4 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG4 (cont.)

Bits	Name	Description
3:0	E4SWS	SW : RW Event counter 4 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0150392C DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 4.

DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG4

Bits	Name	Description
15:0	E4MID	SW : RW Event counter 4 MID selection (If MID filtering enabled)

0x01503930 DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 5.

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG5

Bits	Name	Description
15:13	E5ES	SW : RW Event counter 5 event selection 0x0: Read burst 5 (Master/slave) 0x1: Write burst 5 (Master/slave) 0x2: Address transfer count 5 (Master/slave) 0x3: Read transfer count 5 (Master/slave) 0x4: Write transfer count 5 (Master/slave) 0x5: Write (bufferable burst 5 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E5MIDFEN	SW : RW Event counter 5 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E5INDFEN	SW : RW Event counter 5 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E5IND	SW : RW Event counter 5 Instruction/Data selection 0x0: Data 0x1: Instruction

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG5 (cont.)

Bits	Name	Description
8:4	E5MPS	SW : RW Event counter 5 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG5 (cont.)

Bits	Name	Description
3:0	E5SWS	SW : RW Event counter 5 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01503934 DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 5.

DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG5

Bits	Name	Description
15:0	E5MID	SW : RW Event counter 5 MID selection (If MID filtering enabled)

0x01503938 DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 6.

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG6

Bits	Name	Description
15:13	E6ES	SW : RW Event counter 6 event selection 0x0: Read burst 6 (Master/slave) 0x1: Write burst 6 (Master/slave) 0x2: Address transfer count 6 (Master/slave) 0x3: Read transfer count 6 (Master/slave) 0x4: Write transfer count 6 (Master/slave) 0x5: Write (bufferable burst 6 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E6MIDFEN	SW : RW Event counter 6 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E6INDFEN	SW : RW Event counter 6 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E6IND	SW : RW Event counter 6 Instruction/Data selection 0x0: Data 0x1: Instruction

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG6 (cont.)

Bits	Name	Description
8:4	E6MPS	SW : RW Event counter 6 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG6 (cont.)

Bits	Name	Description
3:0	E6SWS	SW : RW Event counter 6 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0150393C DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 6.

DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG6

Bits	Name	Description
15:0	E6MID	SW : RW Event counter 6 MID selection (If MID filtering enabled)

0x01503940 DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 7.

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG7

Bits	Name	Description
15:13	E7ES	SW : RW Event counter 7 event selection 0x0: Read burst 7 (Master/slave) 0x1: Write burst 7 (Master/slave) 0x2: Address transfer count 7 (Master/slave) 0x3: Read transfer count 7 (Master/slave) 0x4: Write transfer count 7 (Master/slave) 0x5: Write (bufferable burst 7 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E7MIDFEN	SW : RW Event counter 7 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E7INDFEN	SW : RW Event counter 7 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E7IND	SW : RW Event counter 7 Instruction/Data selection 0x0: Data 0x1: Instruction

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG7 (cont.)

Bits	Name	Description
8:4	E7MPS	SW : RW Event counter 7 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

DAY_CFG_FABRIC_MONITOR_SELECTION_LOWER_REG7 (cont.)

Bits	Name	Description
3:0	E7SWS	SW : RW Event counter 7 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01503944 DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 7.

DAY_CFG_FABRIC_MONITOR_SELECTION_UPPER_REG7

Bits	Name	Description
15:0	E7MID	SW : RW Event counter 7 MID selection (If MID filtering enabled)

0x01503948 DAY_CFG_FABRIC_MONITOR_PICK_PORTS_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the main port and other port selection for the eight event counters. Due to a bug in the design, these fields should not be set for Smart Peripheral Subsystem Fabric.

DAY_CFG_FABRIC_MONITOR_PICK_PORTS_REG

Bits	Name	Description
15:14	E7PP	SW : RW Event counter 7 port combination selection 0x0: Master port selected by E7MPS, filtering based on slave port disabled 0x1: Master port selected by E7MPS, filtering based on slave way selected by E7SWS 0x2: Slave way selected by E7SWS, filtering based on master port disabled 0x3: Slave way selected by E7SWS, filtering based on master port selected by E7MPS
13:12	E6PP	SW : RW Event counter 6 port combination selection 0x0: Master port selected by E6MPS, filtering based on slave port disabled 0x1: Master port selected by E6MPS, filtering based on slave way selected by E6SWS 0x2: Slave way selected by E6SWS, filtering based on master port disabled 0x3: Slave way selected by E6SWS, filtering based on master port selected by E6MPS
11:10	E5PP	SW : RW Event counter 5 port combination selection 0x0: Master port selected by E5MPS, filtering based on slave port disabled 0x1: Master port selected by E5MPS, filtering based on slave way selected by E5SWS 0x2: Slave way selected by E5SWS, filtering based on master port disabled 0x3: Slave way selected by E5SWS, filtering based on master port selected by E5MPS
9:8	E4PP	SW : RW Event counter 4 port combination selection 0x0: Master port selected by E4MPS, filtering based on slave port disabled 0x1: Master port selected by E4MPS, filtering based on slave way selected by E4SWS 0x2: Slave way selected by E4SWS, filtering based on master port disabled 0x3: Slave way selected by E4SWS, filtering based on master port selected by E4MPS

DAY_CFG_FABRIC_MONITOR_PICK_PORTS_REG (cont.)

Bits	Name	Description
7:6	E3PP	SW : RW Event counter 3 port combination selection 0x0: Master port selected by E3MPS, filtering based on slave port disabled 0x1: Master port selected by E3MPS, filtering based on slave way selected by E3SWS 0x2: Slave way selected by E3SWS, filtering based on master port disabled 0x3: Slave way selected by E3SWS, filtering based on master port selected by E3MPS
5:4	E2PP	SW : RW Event counter 2 port combination selection 0x0: Master port selected by E2MPS, filtering based on slave port disabled 0x1: Master port selected by E2MPS, filtering based on slave way selected by E2SWS 0x2: Slave way selected by E2SWS, filtering based on master port disabled 0x3: Slave way selected by E2SWS, filtering based on master port selected by E2MPS
3:2	E1PP	SW : RW Event counter 1 port combination selection 0x0: Master port selected by E1MPS, filtering based on slave port disabled 0x1: Master port selected by E1MPS, filtering based on slave way selected by E1SWS 0x2: Slave way selected by E1SWS, filtering based on master port disabled 0x3: Slave way selected by E1SWS, filtering based on master port selected by E1MPS
1:0	E0PP	SW : RW Event counter 0 port combination selection 0x0: Master port selected by E0MPS, filtering based on slave port disabled 0x1: Master port selected by E0MPS, filtering based on slave way selected by E0SWS 0x2: Slave way selected by E0SWS, filtering based on master port disabled 0x3: Slave way selected by E0SWS, filtering based on master port selected by E0MPS

0x01503950 DAY_CFG_FABRIC_MONITOR_CYCLE_COUNT_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the performance monitor cycle counter.

DAY_CFG_FABRIC_MONITOR_CYCLE_COUNT_UPPER_REG

Bits	Name	Description
15:0	UCC	SW : RW MSB cycle count value The cycle count value is decremented once per FABRIC clock. The counter stops decrementing once the CC value equals 32:h0.

0x01503954 DAY_CFG_FABRIC_MONITOR_CYCLE_COUNT_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the performance monitor cycle counter. If SW requires that the values when read do not change, when it reads this register, the value for all 32 bits of the cycle counter is stored. This allows for SW to read the lower reg and have the value match the exact cycle in which the upper reg was read.

DAY_CFG_FABRIC_MONITOR_CYCLE_COUNT_LOWER_REG

Bits	Name	Description
15:0	LCC	SW : RW LSB cycle count value The cycle count value is decremented once per FABRIC clock. The counter stops decrementing once the CC value equals 32:h0.

0x01503958 DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 0. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG0

Bits	Name	Description
15:0	ECLT0	SW : RW Total events (lower 16-bit value)

0x0150395C DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 0. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG0

Bits	Name	Description
15:0	ECUT0	SW : RW Total events (upper 16-bit value)

0x01503960 DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 1. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG1

Bits	Name	Description
15:0	ECLT1	SW : RW Total events (lower 16-bit value)

0x01503964 DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 1. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG1

Bits	Name	Description
15:0	ECUT1	SW : RW Total events (upper 16-bit value)

0x01503968 DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 2. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG2

Bits	Name	Description
15:0	ECLT2	SW : RW Total events (lower 16-bit value)

0x0150396C DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 2. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG2

Bits	Name	Description
15:0	ECUT2	SW : RW Total events (upper 16-bit value)

0x01503970 DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 3. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG3

Bits	Name	Description
15:0	ECLT3	SW : RW Total events (lower 16-bit value)

0x01503974 DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 3. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG3

Bits	Name	Description
15:0	ECUT3	SW : RW Total events (upper 16-bit value)

0x01503978 DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 4. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG4

Bits	Name	Description
15:0	ECLT4	SW : RW Total events (lower 16-bit value)

0x0150397C DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 4. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG4

Bits	Name	Description
15:0	ECUT4	SW : RW Total events (upper 16-bit value)

0x01503980 DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 5. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG5

Bits	Name	Description
15:0	ECLT5	SW : RW Total events (lower 16-bit value)

0x01503984 DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 5. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG5

Bits	Name	Description
15:0	ECUT5	SW : RW Total events (upper 16-bit value)

0x01503988 DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 6. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG6

Bits	Name	Description
15:0	ECLT6	SW : RW Total events (lower 16-bit value)

0x0150398C DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 6. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG6

Bits	Name	Description
15:0	ECUT6	SW : RW Total events (upper 16-bit value)

0x01503990 DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 7. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_LOWER_REG7

Bits	Name	Description
15:0	ECLT7	SW : RW Total events (lower 16-bit value)

0x01503994 DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 7. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_UPPER_REG7

Bits	Name	Description
15:0	ECUT7	SW : RW Total events (upper 16-bit value)

0x015039A4 DAY_CFG_FABRIC_TRIGGER_CONFIGURATION_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register configures the interface in which the trigger comparison is done on the address channel.

TAMS: Selects one of the 32 interfaces from which the address channel transfer qualifiers are used to enable trigger matching.

DAY_CFG_FABRIC_TRIGGER_CONFIGURATION_REG

Bits	Name	Description
15:7	RESERVED_BITS15_6	

DAY_CFG_FABRIC_TRIGGER_CONFIGURATION_REG (cont.)

Bits	Name	Description
6	TRGEN	SW : RW Trigger enable 1'b0 -disabled 1'b1 - enabled
5:0	TAMS	SW : RW Trigger based on address channel on M/S Port : 0x0: Master Port 0 0x1: Master Port 1 0x2: Master Port 2 0x3: Master Port 3 0x4: Master Port 4 0x5: Master Port 5 0x6: Master Port 6 0x7: Master Port 7 0x8: Master Port 8 0x9: Master Port 9 0xA: Master Port 10 0xB: Master Port 11 0xC: Master Port 12 0xD: Master Port 13 0xE: Master Port 14 0xF: Master Port 15 0x10: Master Port 16 0x11: Master Port 17 0x12: Master Port 18 0x13: Master Port 19 0x14: Master Port 20 0x15: Master Port 21 0x16: Master Port 22 0x17: Master Port 23 0x18: Master Port 24 0x19: Master Port 25 0x1A: Master Port 26 0x1B: Master Port 27 0x1C: Master Port 28 0x1D: Master Port 29 0x1E: Master Port 30 0x1F: Master Port 31

DAY_CFG_FABRIC_TRIGGER_CONFIGURATION_REG (cont.)

Bits	Name	Description
5:0	TAMS	0x20: Slave Port 0 0x21: Slave Port 1 0x22: Slave Port 2 0x23: Slave Port 3 0x24: Slave Port 4 0x25: Slave Port 5 0x26: Slave Port 6 0x27: Slave Port 7 0x28: Slave Port 8 0x29: Slave Port 9 0x2A: Slave Port 10 0x2B: Slave Port 11 0x2C: Slave Port 12 0x2D: Slave Port 13 0x2E: Slave Port 14 0x2F: Slave Port 15

0x015039AC DAY_CFG_FABRIC_TRIGGER_REG_0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the upper address which is used as comparison for the trigger feature of the on-chip trace or performance monitor function. TUADDR[15:0] will be compared against Address[31:16].

DAY_CFG_FABRIC_TRIGGER_REG_0

Bits	Name	Description
15:0	TUADDR	SW : RW Address bits[31:16]

0x015039B0 DAY_CFG_FABRIC_TRIGGER_REG_1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the lower address which is used as comparison for the trigger feature of the performance monitor function. TLADDR[15:0] will be compared against Address[15:0].

DAY_CFG_FABRIC_TRIGGER_REG_1

Bits	Name	Description
15:0	TLADDR	SW : RW Address bits[15:0]

0x015039B4 DAY_CFG_FABRIC_TRIGGER_REG_2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the lower address which is used as comparison for the trigger feature of the performance monitor function..

DAY_CFG_FABRIC_TRIGGER_REG_2

Bits	Name	Description
15:0	AMID	SW : RW AMID / HMID

0x015039B8 DAY_CFG_FABRIC_TRIGGER_REG_3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the address channel transfer qualifiers which are used as comparison for the trigger feature of the performance monitor function.

DAY_CFG_FABRIC_TRIGGER_REG_3

Bits	Name	Description
15:12	RESERVED_BITS15_12	
11	AOOOWR	SW : RW Out-of-order write
10	AOOORD	SW : RW Out-of-order read
9:3	ATID	SW : RW Address TID (If ATID is less than 7 bits, the upper bits must be set to 0)
2	AFULL	SW : RW Full Transfer

DAY_CFG_FABRIC_TRIGGER_REG_3 (cont.)

Bits	Name	Description
1	RESERVED_BIT1	
0	APROTNS	SW : RW Protection level

0x015039BC DAY_CFG_FABRIC_TRIGGER_REG_4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the address channel transfer qualifiers which are used as comparison for the trigger feature of the performance monitor function.

DAY_CFG_FABRIC_TRIGGER_REG_4

Bits	Name	Description
15:12	ATYPE	SW : RW Memory type attributes
11:10	ALOCK	SW : RW Lock type
9	RESERVED_BITS9	
8	ABURST	SW : RW Burst type
7:5	ASIZE	Burst size
4:1	ALEN	Burst length
0	AWRITE	Burst direction

0x015039C0 DAY_CFG_FABRIC_TRIGGER_MASK_REG_0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR0.

Setting a mask bit to 1’b1 indicates that the selected field is not matched against the corresponding bit in FTTR0.

DAY_CFG_FABRIC_TRIGGER_MASK_REG_0

Bits	Name	Description
15:0	FTTR0_MASK	SW : RW Bit mask field for FTTR0 Enable: 1 Disable: 0

0x015039C4 DAY_CFG_FABRIC_TRIGGER_MASK_REG_1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR1.

DAY_CFG_FABRIC_TRIGGER_MASK_REG_1

Bits	Name	Description
15:0	FTTR1_MASK	SW : RW Bit mask field for FTTR1 Enable: 1 Disable: 0

0x015039C8 DAY_CFG_FABRIC_TRIGGER_MASK_REG_2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR2.

DAY_CFG_FABRIC_TRIGGER_MASK_REG_2

Bits	Name	Description
15:0	FTTR2_MASK	SW : RW Bit mask field for FTTR2 Enable: 1 Disable: 0

0x015039CC DAY_CFG_FABRIC_TRIGGER_MASK_REG_3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR3.

DAY_CFG_FABRIC_TRIGGER_MASK_REG_3

Bits	Name	Description
15:0	FTTR3_MASK	SW : RW Bit mask field for FTTR3 Enable: 1 Disable: 0

0x015039D0 DAY_CFG_FABRIC_TRIGGER_MASK_REG_4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR4.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR4.

DAY_CFG_FABRIC_TRIGGER_MASK_REG_4

Bits	Name	Description
15:0	FTTR4_MASK	SW : RW Bit mask field for FTTR4 Enable: 1 Disable: 0

0x015039D4 DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter0.

DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG0

Bits	Name	Description
15:0	E0AL	SW : RW LSB address value Event counter 0 address selection (if address range filtering enabled)

0x015039D8 DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter0.

DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG0

Bits	Name	Description
15:0	E0AU	SW : RW MSB address value Event counter 0 address selection (if address range filtering enabled)

0x015039DC DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter1.

DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG1

Bits	Name	Description
15:0	E1AL	SW : RW LSB address value Event counter 1address selection (if address range filtering enabled)

0x015039E0 DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter1.

DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG1

Bits	Name	Description
15:0	E1AU	SW : RW MSB address value Event counter 1address selection (if address range filtering enabled)

0x015039E4 DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter2

DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG2

Bits	Name	Description
15:0	E2AL	SW : RW LSB address value Event counter 2 address selection (if address range filtering enabled)

0x015039E8 DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter2.

DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG2

Bits	Name	Description
15:0	E2AU	SW : RW MSB address value Event counter 2 address selection (if address range filtering enabled)

0x015039EC DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter3

DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG3

Bits	Name	Description
15:0	E3AL	SW : RW LSB address value Event counter 3 address selection (if address range filtering enabled)

0x015039F0 DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter3.

DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG3

Bits	Name	Description
15:0	E3AU	SW : RW MSB address value Event counter 3 address selection (if address range filtering enabled)

0x015039F4 DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter4.

DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG4

Bits	Name	Description
15:0	E4AL	SW : RW LSB address value Event counter 4 address selection (if address range filtering enabled)

0x015039F8 DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter4.

DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG4

Bits	Name	Description
15:0	E4AU	SW : RW MSB address value Event counter 4address selection (if address range filtering enabled)

0x015039FC DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter5.

DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG5

Bits	Name	Description
15:0	E5AL	SW : RW LSB address value Event counter 5 address selection (if address range filtering enabled)

0x01503A00 DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter4.

DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG5

Bits	Name	Description
15:0	E5AU	SW : RW MSB address value Event counter 5 address selection (if address range filtering enabled)

0x01503A04 DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter 6.

DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG6

Bits	Name	Description
15:0	E6AL	SW : RW LSB address value Event counter 6 address selection (if address range filtering enabled)

0x01503A08 DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 6.

DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG6

Bits	Name	Description
15:0	E6AU	SW : RW MSB address value Event counter 6 address selection (if address range filtering enabled)

0x01503A0C DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter 7.

DAY_CFG_FABRIC_MONITOR_ADDRESS_LOWER_REG7

Bits	Name	Description
15:0	E7AL	SW : RW LSB address value Event counter 7 address selection (if address range filtering enabled)

0x01503A10 DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 7.

DAY_CFG_FABRIC_MONITOR_ADDRESS_UPPER_REG7

Bits	Name	Description
15:0	E7AU	SW : RW MSB address value Event counter 7 address selection (if address range filtering enabled)

0x01503A14 DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR0.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG0

Bits	Name	Description
15:0	E0AML	SW : RW LSB address value Event counter 0 address mask

0x01503A18 DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR0.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG0

Bits	Name	Description
15:0	E0AMU	SW : RW MSB address value Event counter 0 address mask

0x01503A1C DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR1.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG1

Bits	Name	Description
15:0	E1AML	SW : RW LSB address value Event counter 1 address mask

0x01503A20 DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR1.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG1

Bits	Name	Description
15:0	E1AMU	SW : RW MSB address value Event counter address mask

0x01503A24 DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR2.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG2

Bits	Name	Description
15:0	E2AML	SW : RW LSB address value Event counter 2 address mask

0x01503A28 DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR2.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG2

Bits	Name	Description
15:0	E2AMU	SW : RW MSB address value Event counter 2 address mask

0x01503A2C DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR3.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG3

Bits	Name	Description
15:0	E3AML	SW : RW LSB address value Event counter 3 address mask

0x01503A30 DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR3.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG3

Bits	Name	Description
15:0	E3AMU	SW : RW MSB address value Event counter 3 address mask

0x01503A34 DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 4.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR4.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG4

Bits	Name	Description
15:0	E4AML	SW : RW LSB address value Event counter 4 address mask

0x01503A38 DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 4.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR4.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG4

Bits	Name	Description
15:0	E4AMU	SW : RW MSB address value Event counter 4 address mask

0x01503A3C DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 5.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR5.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG5

Bits	Name	Description
15:0	E5AML	SW : RW LSB address value Event counter 5 address mask

0x01503A40 DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 5.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR5.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG5

Bits	Name	Description
15:0	E5AMU	SW : RW MSB address value Event counter 5 address mask

0x01503A44 DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 6.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR6.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG6

Bits	Name	Description
15:0	E6AML	SW : RW LSB address value Event counter 6 address mask

0x01503A48 DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 6.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR6.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG6

Bits	Name	Description
15:0	E6AMU	SW : RW MSB address value Event counter 6 address mask

0x01503A4C DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 7.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR7.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG7

Bits	Name	Description
15:0	E7AML	SW : RW LSB address value Event counter 7 address mask

0x01503A50 DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 7.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR7.

DAY_CFG_FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG7

Bits	Name	Description
15:0	E7AMU	SW : RW MSB address value Event counter 7 address mask

0x01503A70 DAY_CFG_FABRIC_MONITOR_MID_MASK_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 0

DAY_CFG_FABRIC_MONITOR_MID_MASK_REG0

Bits	Name	Description
15:0	E0MM	SW : RW MID Mask value for event counter 0

0x01503A74 DAY_CFG_FABRIC_MONITOR_MID_MASK_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 1

DAY_CFG_FABRIC_MONITOR_MID_MASK_REG1

Bits	Name	Description
15:0	E1MM	SW : RW MID Mask value for event counter 1

0x01503A78 DAY_CFG_FABRIC_MONITOR_MID_MASK_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 2

DAY_CFG_FABRIC_MONITOR_MID_MASK_REG2

Bits	Name	Description
15:0	E2MM	SW : RW MID Mask value for event counter 2

0x01503A7C DAY_CFG_FABRIC_MONITOR_MID_MASK_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 3

DAY_CFG_FABRIC_MONITOR_MID_MASK_REG3

Bits	Name	Description
15:0	E3MM	SW : RW MID Mask value for event counter 3

0x01503A80 DAY_CFG_FABRIC_MONITOR_MID_MASK_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 4

DAY_CFG_FABRIC_MONITOR_MID_MASK_REG4

Bits	Name	Description
15:0	E4MM	SW : RW MID Mask value for event counter 4

0x01503A84 DAY_CFG_FABRIC_MONITOR_MID_MASK_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 15

DAY_CFG_FABRIC_MONITOR_MID_MASK_REG5

Bits	Name	Description
15:0	E5MM	SW : RW MID Mask value for event counter 5

0x01503A88 DAY_CFG_FABRIC_MONITOR_MID_MASK_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 6

DAY_CFG_FABRIC_MONITOR_MID_MASK_REG6

Bits	Name	Description
15:0	E6MM	SW : RW MID Mask value for event counter 6

0x01503A8C DAY_CFG_FABRIC_MONITOR_MID_MASK_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 7

DAY_CFG_FABRIC_MONITOR_MID_MASK_REG7

Bits	Name	Description
15:0	E7MM	SW : RW MID Mask value for event counter 7

0x01503AA0 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG0

Bits	Name	Description
15:0	EBTL0	SW : RW Total beats (lower 16-bit value)

0x01503AA4 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG0

Bits	Name	Description
15:0	EBTM0	SW : RW Total beats (middle 16-bit value)

0x01503AA8 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG0

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU0	SW : RW Total beats (upper 4-bit value)

0x01503AAC DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG1

Bits	Name	Description
15:0	EBTL1	SW : RW Total beats (lower 16-bit value)

0x01503AB0 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG1

Bits	Name	Description
15:0	EBTM1	SW : RW Total beats (middle 16-bit value)

0x01503AB4 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG1

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU1	SW : RW Total beats (upper 4-bit value)

0x01503AB8 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write

Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG2

Bits	Name	Description
15:0	EBTL2	SW : RW Total beats (lower 16-bit value)

0x01503ABC DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG2

Bits	Name	Description
15:0	EBTM2	SW : RW Total beats (middle 16-bit value)

0x01503AC0 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG2

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU2	SW : RW Total beats (upper 4-bit value)

0x01503AC4 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG3

Bits	Name	Description
15:0	EBTL3	SW : RW Total beats (lower 16-bit value)

0x01503AC8 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG3

Bits	Name	Description
15:0	EBTM3	SW : RW Total beats (middle 16-bit value)

0x01503ACC DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG3

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU3	SW : RW Total beats (upper 4-bit value)

0x01503AD0 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG4

Bits	Name	Description
15:0	EBTL4	SW : RW Total beats (lower 16-bit value)

0x01503AD4 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG4

Bits	Name	Description
15:0	EBTM4	SW : RW Total beats (middle 16-bit value)

0x01503AD8 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG4

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU4	SW : RW Total beats (upper 4-bit value)

0x01503ADC DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG5

Bits	Name	Description
15:0	EBTL5	SW : RW Total beats (lower 16-bit value)

0x01503AE0 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write

Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG5

Bits	Name	Description
15:0	EBTM5	SW : RW Total beats (middle 16-bit value)

0x01503AE4 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG5

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU5	SW : RW Total beats (upper 4-bit value)

0x01503AE8 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG6

Bits	Name	Description
15:0	EBTL6	SW : RW Total beats (lower 16-bit value)

0x01503AEC DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG6

Bits	Name	Description
15:0	EBTM6	SW : RW Total beats (middle 16-bit value)

0x01503AF0 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG6

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU6	SW : RW Total beats (upper 4-bit value)

0x01503AF4 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write

Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_LOWER_REG7

Bits	Name	Description
15:0	EBTL7	SW : RW Total beats (lower 16-bit value)

0x01503AF8 DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_MID_REG7

Bits	Name	Description
15:0	EBTM7	SW : RW Total beats (middle 16-bit value)

0x01503AFC DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BEATS_UPPER_REG7

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU7	SW : RW Total beats (upper 4-bit value)

0x01503B00 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG0

Bits	Name	Description
15:0	EBYL0	SW : RW Total bytes (lower 16-bit value)

0x01503B04 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG0

Bits	Name	Description
15:0	EBYM0	SW : RW Total bytes (middle 16-bit value)

0x01503B08 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG0

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU0	SW : RW Total bytes (upper 11-bit value)

0x01503B0C DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG1

Bits	Name	Description
15:0	EBYL1	SW : RW Total bytes (lower 16-bit value)

0x01503B10 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG1

Bits	Name	Description
15:0	EBYM1	SW : RW Total bytes (middle 16-bit value)

0x01503B14 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG1

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU1	SW : RW Total bytes (upper 11-bit value)

0x01503B18 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG2

Bits	Name	Description
15:0	EBYL2	SW : RW Total bytes (lower 16-bit value)

0x01503B1C DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG2

Bits	Name	Description
15:0	EBYM2	SW : RW Total bytes (middle 16-bit value)

0x01503B20 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG2

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU2	SW : RW Total bytes (upper 11-bit value)

0x01503B24 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG3

Bits	Name	Description
15:0	EBYL3	SW : RW Total bytes (lower 16-bit value)

0x01503B28 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG3

Bits	Name	Description
15:0	EBYM3	SW : RW Total bytes (middle 16-bit value)

0x01503B2C DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG3

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU3	SW : RW Total bytes (upper 11-bit value)

0x01503B30 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG4

Bits	Name	Description
15:0	EBYL4	SW : RW Total bytes (lower 16-bit value)

0x01503B34 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG4

Bits	Name	Description
15:0	EBYM4	SW : RW Total bytes (middle 16-bit value)

0x01503B38 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG4

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU4	SW : RW Total bytes (upper 11-bit value)

0x01503B3C DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG5

Bits	Name	Description
15:0	EBYL5	SW : RW Total bytes (lower 16-bit value)

0x01503B40 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG5

Bits	Name	Description
15:0	EBYM5	SW : RW Total bytes (middle 16-bit value)

0x01503B44 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG5

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU5	SW : RW Total bytes (upper 11-bit value)

0x01503B48 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG6

Bits	Name	Description
15:0	EBYL6	SW : RW Total bytes (lower 16-bit value)

0x01503B4C DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG6

Bits	Name	Description
15:0	EBYM6	SW : RW Total bytes (middle 16-bit value)

0x01503B50 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG6

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU6	SW : RW Total bytes (upper 11-bit value)

0x01503B54 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_LOWER_REG7

Bits	Name	Description
15:0	EBYL7	SW : RW Total bytes (lower 16-bit value)

0x01503B58 DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_MID_REG7

Bits	Name	Description
15:0	EBYM7	SW : RW Total bytes (middle 16-bit value)

0x01503B5C DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

DAY_CFG_FABRIC_MONITOR_EVENT_BYTES_UPPER_REG7

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU7	SW : RW Total bytes (upper 11-bit value)

0x01503B60 DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 0.

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0

Bits	Name	Description
15:14	T0SR	SW : RW Tenure selection for tenure counter 0 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T0MIDFEN	SW : RW Tenure counter 0 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T0INDFEN	SW : RW Tenure counter 0 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T0IND	SW : RW Tenure counter 0 Instruction/Data selection 0x0: Data 0x1: Instruction

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
8:4	T0MP	SW : RW Tenure master port selection register for tenure counter 0 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
3:0	T0SW	SW : RW Tenure slave way selection register for tenure counter 0 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01503B64 DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 0.

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG0

Bits	Name	Description
15:0	T0MID	SW : RW Tenure counter 0 MID selection (If MID filtering enabled)

0x01503B68 DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 1.

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1

Bits	Name	Description
15:14	T1SR	SW : RW Tenure selection for tenure counter 1 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T1MIDFEN	SW : RW Tenure counter 1MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T1INDFEN	SW : RW Tenure counter 1Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T1IND	SW : RW Tenure counter 1Instruction/Data selection 0x0: Data 0x1: Instruction

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
8:4	T1MP	SW : RW Tenure master port selection register for tenure counter 1 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
3:0	T1SW	SW : RW Tenure slave way selection register for tenure counter 1 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01503B6C DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 1.

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG1

Bits	Name	Description
15:0	T1MID	SW : RW Tenure counter 1MID selection (If MID filtering enabled)

0x01503B70 DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 2.

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2

Bits	Name	Description
15:14	T2SR	SW : RW Tenure selection for tenure counter 2 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T2MIDFEN	SW : RW Tenure counter 2 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T2INDFEN	SW : RW Tenure counter 2 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T2IND	SW : RW Tenure counter 2 Instruction/Data selection 0x0: Data 0x1: Instruction

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
8:4	T2MP	SW : RW Tenure master port selection register for tenure counter 2 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
3:0	T2SW	SW : RW Tenure slave way selection register for tenure counter 2 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01503B74 DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 2.

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG2

Bits	Name	Description
15:0	T2MID	SW : RW Tenure counter 2 MID selection (If MID filtering enabled)

0x01503B78 DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 3.

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3

Bits	Name	Description
15:14	T3SR	SW : RW Tenure selection for tenure counter 3 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T3MIDFEN	SW : RW Tenure counter 3 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T3INDFEN	SW : RW Tenure counter 3 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T3IND	SW : RW Tenure counter 3 Instruction/Data selection 0x0: Data 0x1: Instruction

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
8:4	T3MP	SW : RW Tenure master port selection register for tenure counter 3 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
3:0	T3SW	SW : RW Tenure slave way selection register for tenure counter 3 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x01503B7C DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 3.

DAY_CFG_FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG3

Bits	Name	Description
15:0	T3MID	SW : RW Tenure counter 3 MID selection (If MID filtering enabled)

0x01503B80 DAY_CFG_FABRIC_MONITOR_MIN_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains the minimum value of the tenure that is selected using FPTSLR0 and measured in tenure counter 0.

NOTE The reset value for this register is set to h'FFFF, equivalent to 65535 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'FFFF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

DAY_CFG_FABRIC_MONITOR_MIN_REG0

Bits	Name	Description
15:0	MIN0	SW : R Minimum value of tenure, in tenure counter 0

0x01503B84 DAY_CFG_FABRIC_MONITOR_MIN_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains the minimum value of the tenure that is selected using FPTSLR1 and measured in tenure counter 1.

NOTE The reset value for this register is set to h'FFFF, equivalent to 65535 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'FFFF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

DAY_CFG_FABRIC_MONITOR_MIN_REG1

Bits	Name	Description
15:0	MIN1	SW : R Minimum value of tenure, in tenure counter 1

0x01503B88 DAY_CFG_FABRIC_MONITOR_MIN_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains the minimum value of the tenure that is selected using FPTSLR2 and measured in tenure counter 2.

NOTE The reset value for this register is set to h'FFFF, equivalent to 65535 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'FFFF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

DAY_CFG_FABRIC_MONITOR_MIN_REG2

Bits	Name	Description
15:0	MIN2	SW : R Minimum value of tenure, in tenure counter 2

0x01503B8C DAY_CFG_FABRIC_MONITOR_MIN_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains the minimum value of the tenure that is selected using FPTSLR3 and measured in tenure counter 3.

NOTE The reset value for this register is set to h'FFFF, equivalent to 65535 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'FFFF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

DAY_CFG_FABRIC_MONITOR_MIN_REG3

Bits	Name	Description
15:0	MIN3	SW : R Minimum value of tenure, in tenure counter 3

0x01503B90 DAY_CFG_FABRIC_MONITOR_MAX_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR0 and measured in tenure counter 0.

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

DAY_CFG_FABRIC_MONITOR_MAX_REG0

Bits	Name	Description
15:0	MAX0	SW : R Maximum value of tenure, in tenure counter 0

0x01503B94 DAY_CFG_FABRIC_MONITOR_MAX_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR1and measured in tenure counter 1

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be ’hFFFF.

DAY_CFG_FABRIC_MONITOR_MAX_REG1

Bits	Name	Description
15:0	MAX1	SW : R Maximum value of tenure, in tenure counter 1

0x01503B98 DAY_CFG_FABRIC_MONITOR_MAX_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR2 and measured in tenure counter 2

NOTE The reset value for this register is set to h’0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h’0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be ’hFFFF.

DAY_CFG_FABRIC_MONITOR_MAX_REG2

Bits	Name	Description
15:0	MAX2	SW : R Maximum value of tenure, in tenure counter 2

0x01503B9C DAY_CFG_FABRIC_MONITOR_MAX_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR3 and measured in tenure counter 3

NOTE The reset value for this register is set to h’0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h’0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be ’hFFFF.

DAY_CFG_FABRIC_MONITOR_MAX_REG3

Bits	Name	Description
15:0	MAX3	SW : R Maximum value of tenure, in tenure counter 3

0x01503BA0 DAY_CFG_FABRIC_MONITOR_TENURE_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 0

DAY_CFG_FABRIC_MONITOR_TENURE_LOWER_REG0

Bits	Name	Description
15:0	LTOT0	SW : RW LSB total value of tenure, in tenure counter 0

0x01503BA4 DAY_CFG_FABRIC_MONITOR_TENURE_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 0.

DAY_CFG_FABRIC_MONITOR_TENURE_UPPER_REG0

Bits	Name	Description
15:0	UTOT0	SW : RW MSB total value of tenure, in tenure counter 0

0x01503BA8 DAY_CFG_FABRIC_MONITOR_TENURE_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 1

DAY_CFG_FABRIC_MONITOR_TENURE_LOWER_REG1

Bits	Name	Description
15:0	LTOT1	SW : RW LSB total value of tenure, in tenure counter 1

0x01503BAC DAY_CFG_FABRIC_MONITOR_TENURE_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 1.

DAY_CFG_FABRIC_MONITOR_TENURE_UPPER_REG1

Bits	Name	Description
15:0	UTOT1	SW : RW MSB total value of tenure, in tenure counter 1

0x01503BB0 DAY_CFG_FABRIC_MONITOR_TENURE_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 2

DAY_CFG_FABRIC_MONITOR_TENURE_LOWER_REG2

Bits	Name	Description
15:0	LTOT2	SW : RW LSB total value of tenure, in tenure counter 2

0x01503BB4 DAY_CFG_FABRIC_MONITOR_TENURE_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 2.

DAY_CFG_FABRIC_MONITOR_TENURE_UPPER_REG2

Bits	Name	Description
15:0	UTOT2	SW : RW MSB total value of tenure, in tenure counter 2

0x01503BB8 DAY_CFG_FABRIC_MONITOR_TENURE_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 3

DAY_CFG_FABRIC_MONITOR_TENURE_LOWER_REG3

Bits	Name	Description
15:0	LTOT3	SW : RW LSB total value of tenure, in tenure counter 3

0x01503BBC DAY_CFG_FABRIC_MONITOR_TENURE_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 3.

DAY_CFG_FABRIC_MONITOR_TENURE_UPPER_REG3

Bits	Name	Description
15:0	UTOT3	SW : RW MSB total value of tenure, in tenure counter 3

0x01503BC0 DAY_CFG_FABRIC_MONITOR_LAST_TENURE_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 0

DAY_CFG_FABRIC_MONITOR_LAST_TENURE_REG0

Bits	Name	Description
15:0	LASTT0	SW : R Last tenure value in tenure counter 0

0x01503BC4 DAY_CFG_FABRIC_MONITOR_LAST_TENURE_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 1

DAY_CFG_FABRIC_MONITOR_LAST_TENURE_REG1

Bits	Name	Description
15:0	LASTT1	SW : R Last tenure value in tenure counter 1

0x01503BC8 DAY_CFG_FABRIC_MONITOR_LAST_TENURE_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 2

DAY_CFG_FABRIC_MONITOR_LAST_TENURE_REG2

Bits	Name	Description
15:0	LASTT2	SW : R Last tenure value in tenure counter 2

0x01503BCC DAY_CFG_FABRIC_MONITOR_LAST_TENURE_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 3

DAY_CFG_FABRIC_MONITOR_LAST_TENURE_REG3

Bits	Name	Description
15:0	LASTT0	SW : R Last tenure value in tenure counter 3

0x01503BD0 DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 0.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG0

Bits	Name	Description
15:0	T0AL	SW : RW LSB address value Tenure counter 0 address mask

0x01503BD4 DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 0.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG0

Bits	Name	Description
15:0	T0AU	SW : RW MSB address value Tenure counter 0 address mask

0x01503BD8 DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 1.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG1

Bits	Name	Description
15:0	T1AL	SW : RW LSB address value Tenure counter 1 address mask

0x01503BDC DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 1.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG1

Bits	Name	Description
15:0	T1AU	SW : RW MSB address value Tenure counter 1 address mask

0x01503BE0 DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 2.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG2

Bits	Name	Description
15:0	T2AL	SW : RW LSB address value Tenure counter 2 address mask

0x01503BE4 DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 2.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG2

Bits	Name	Description
15:0	T2AU	SW : RW MSB address value Tenure counter 2 address mask

0x01503BE8 DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 3.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG3

Bits	Name	Description
15:0	T3AL	SW : RW LSB address value Tenure counter 3 address mask

0x01503BEC DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 3.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG3

Bits	Name	Description
15:0	T3AU	SW : RW MSB address value Tenure counter 3 address mask

0x01503BF0 DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 0

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR0.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG0

Bits	Name	Description
15:0	T0AML	SW : RW LSB address value Tenure counter 0 address mask

0x01503BF4 DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 0

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR0.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG0

Bits	Name	Description
15:0	T0AMU	SW : RW MSB address mask value Tenure counter 0 address mask

0x01503BF8 DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 1

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR1.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG1

Bits	Name	Description
15:0	T1AML	SW : RW LSB address value Tenure counter 1 address mask

0x01503BFC DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 1

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR1.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG1

Bits	Name	Description
15:0	T1AMU	SW : RW MSB address mask value Tenure counter 1 address mask

0x01503C00 DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 2

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR2.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG2

Bits	Name	Description
15:0	T2AML	SW : RW LSB address value Tenure counter 2 address mask

0x01503C04 DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 2

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR2.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG2

Bits	Name	Description
15:0	T2AMU	SW : RW MSB address mask value Tenure counter 2 address mask

0x01503C08 DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 3

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR3.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG3

Bits	Name	Description
15:0	T3AML	SW : RW LSB address value Tenure counter 3 address mask

0x01503C0C DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 3

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR3.

DAY_CFG_FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG3

Bits	Name	Description
15:0	T3AMU	SW : RW MSB address mask value Tenure counter 3 address mask

0x01503C10 DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 0 that were longer than the specified threshold for tenure counter 0

DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG0

Bits	Name	Description
15:0	T0ATCL	SW : R LSB count value

0x01503C14 DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 0 that were longer than the specified threshold for tenure counter 0

DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG0

Bits	Name	Description
15:0	T0ATCU	SW : R MSB count value

0x01503C18 DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 1 that were longer than the specified threshold for tenure counter 1

DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG1

Bits	Name	Description
15:0	T1ATCL	SW : R LSB count value

0x01503C1C DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 1 that were longer than the specified threshold for tenure counter 1

DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG1

Bits	Name	Description
15:0	T1ATCU	SW : R MSB count value

0x01503C20 DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 2 that were longer than the specified threshold for tenure counter 2

DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG2

Bits	Name	Description
15:0	T2ATCL	SW : R LSB count value

0x01503C24 DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 2 that were longer than the specified threshold for tenure counter 2

DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG2

Bits	Name	Description
15:0	T2ATCU	SW : R MSB count value

0x01503C28 DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 3 that were longer than the specified threshold for tenure counter 3

DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG3

Bits	Name	Description
15:0	T3ATCL	SW : R LSB count value

0x01503C2C DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 3 that were longer than the specified threshold for tenure counter 3

DAY_CFG_FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG3

Bits	Name	Description
15:0	T3ATCU	SW : R MSB count value

0x01503C30 DAY_CFG_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 0 are measured.

DAY_CFG_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG0

Bits	Name	Description
15:0	T0TV	SW : RW Tenure counter 0 threshold value

0x01503C34 DAY_CFG_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 1 are measured.

DAY_CFG_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG1

Bits	Name	Description
15:0	T1TV	SW : RW Tenure counter 1 threshold value

0x01503C38 DAY_CFG_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 2 are measured.

DAY_CFG_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG2

Bits	Name	Description
15:0	T2TV	SW : RW Tenure counter 2 threshold value

0x01503C3C DAY_CFG_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 3 are measured.

DAY_CFG_FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG3

Bits	Name	Description
15:0	T3TV	SW : RW Tenure counter 3 threshold value

0x01503C40 DAY_CFG_FABRIC_MONITOR_TENURE_MID_MASK_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 0

DAY_CFG_FABRIC_MONITOR_TENURE_MID_MASK_REG0

Bits	Name	Description
15:0	T0MM	SW : RW MID Mask value

0x01503C44 DAY_CFG_FABRIC_MONITOR_TENURE_MID_MASK_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 1

DAY_CFG_FABRIC_MONITOR_TENURE_MID_MASK_REG1

Bits	Name	Description
15:0	T1MM	SW : RW MID Mask value

0x01503C48 DAY_CFG_FABRIC_MONITOR_TENURE_MID_MASK_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 2

DAY_CFG_FABRIC_MONITOR_TENURE_MID_MASK_REG2

Bits	Name	Description
15:0	T2MM	SW : RW MID Mask value

0x01503C4C DAY_CFG_FABRIC_MONITOR_TENURE_MID_MASK_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 3

DAY_CFG_FABRIC_MONITOR_TENURE_MID_MASK_REG3

Bits	Name	Description
15:0	T3MM	SW : RW MID Mask value

0x01503C50 DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure0 register.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG0

Bits	Name	Description
15:0	TLC0	SW : R LSB count value Incremented every time a tenure under observation completes in tenure counter 0

0x01503C54 DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure0 register.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG0

Bits	Name	Description
15:0	TUC0	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 0

0x01503C58 DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure1 register.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG1

Bits	Name	Description

0x01503C5C DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure1 register.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG1

Bits	Name	Description
15:0	TUC1	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 1

0x01503C60 DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure2 register.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG2

Bits	Name	Description
15:0	TLC2	SW : R LSB count value Incremented every time a tenure under observation completes in tenure counter 2

0x01503C64 DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure2 register.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG2

Bits	Name	Description
15:0	TUC2	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 2

0x01503C68 DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure3 register.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_LOWER_REG3

Bits	Name	Description
15:0	TLC3	SW : R LSB count value Incremented every time a tenure under observation completes in tenure counter 3

0x01503C6C DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure3 register.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_UPPER_REG3

Bits	Name	Description
15:0	TUC3	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 3

0x01503C70 DAY_CFG_FABRIC_MONITOR_TENURE_PICK_PORTS_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the main port and other port selection for the 4 event counters. Due to a bug in the design, these fields should not be set for Smart Peripheral Subsystem Fabric.

DAY_CFG_FABRIC_MONITOR_TENURE_PICK_PORTS_REG

Bits	Name	Description
15:4	RESERVED_15_4	Reserved

DAY_CFG_FABRIC_MONITOR_TENURE_PICK_PORTS_REG (cont.)

Bits	Name	Description
3	T3PP	SW : RW Tenure counter 3 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T3MP or T3SW
2	T2PP	SW : RW Tenure counter 2 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T2MP or T2SW
1	T1PP	SW : RW Tenure counter 1 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T1MP or T1SW
0	T0PP	SW : RW Tenure counter 0 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T0MP or T0SW

0x01503C80 DAY_CFG_FABRIC_MONITOR_TENURE_UNION_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 0

DAY_CFG_FABRIC_MONITOR_TENURE_UNION_LOWER_REG0

Bits	Name	Description
15:0	LTOTU0	SW : RW LSB total union value of tenure, in tenure counter 0

0x01503C84 DAY_CFG_FABRIC_MONITOR_TENURE_UNION_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 0.

DAY_CFG_FABRIC_MONITOR_TENURE_UNION_UPPER_REG0

Bits	Name	Description
15:0	UTOTU0	SW : RW MSB total union value of tenure, in tenure counter 0

0x01503C88 DAY_CFG_FABRIC_MONITOR_TENURE_UNION_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 1

DAY_CFG_FABRIC_MONITOR_TENURE_UNION_LOWER_REG1

Bits	Name	Description
15:0	LTOTU1	SW : RW LSB total union value of tenure, in tenure counter 1

0x01503C8C DAY_CFG_FABRIC_MONITOR_TENURE_UNION_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 1.

DAY_CFG_FABRIC_MONITOR_TENURE_UNION_UPPER_REG1

Bits	Name	Description
15:0	UTOTU1	SW : RW MSB total union value of tenure, in tenure counter 1

0x01503C90 DAY_CFG_FABRIC_MONITOR_TENURE_UNION_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 2

DAY_CFG_FABRIC_MONITOR_TENURE_UNION_LOWER_REG2

Bits	Name	Description
15:0	LTOTU2	SW : RW LSB total union value of tenure, in tenure counter 2

0x01503C94 DAY_CFG_FABRIC_MONITOR_TENURE_UNION_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 2.

DAY_CFG_FABRIC_MONITOR_TENURE_UNION_UPPER_REG2

Bits	Name	Description
15:0	UTOTU2	SW : RW MSB total union value of tenure, in tenure counter 2

0x01503C98 DAY_CFG_FABRIC_MONITOR_TENURE_UNION_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 3

DAY_CFG_FABRIC_MONITOR_TENURE_UNION_LOWER_REG3

Bits	Name	Description
15:0	LTOTU3	SW : RW LSB total union value of tenure, in tenure counter 3

0x01503C9C DAY_CFG_FABRIC_MONITOR_TENURE_UNION_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 3.

DAY_CFG_FABRIC_MONITOR_TENURE_UNION_UPPER_REG3

Bits	Name	Description
15:0	UTOTU3	SW : RW MSB total union value of tenure, in tenure counter 3

0x01503CA0 DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 0, that were pipelined.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG0

Bits	Name	Description

0x01503CA4 DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 0, that were pipelined.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG0

Bits	Name	Description
15:0	TUCP0	SW : R MSB count value TUCP0,TLCP0 value incremented every time a pipelined tenure completes in tenure counter 0

0x01503CA8 DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 1, that were pipelined.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG1

Bits	Name	Description

0x01503CAC DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 1, that were pipelined.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG1

Bits	Name	Description
15:0	TUCP1	SW : R MSB count value TUCP1,TLCP1 value incremented every time a pipelined tenure completes in tenure counter 1

0x01503CB0 DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 2, that were pipelined.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG2

Bits	Name	Description

0x01503CB4 DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 2, that were pipelined.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG2

Bits	Name	Description
15:0	TUCP2	SW : R MSB count value TUCP1,TLCP1 value incremented every time a pipelined tenure completes in tenure counter 2

0x01503CB8 DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 3, that were pipelined.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG3

Bits	Name	Description

0x01503CBC DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 3, that were pipelined.

DAY_CFG_FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG3

Bits	Name	Description
15:0	TUCP3	SW : R MSB count value TUCP3,TLCP3 value incremented every time a pipelined tenure completes in tenure counter 3

0x01503CC0 DAY_CFG_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum number of tenures pipelined at any point during the monitoring window for tenure counter 0.

DAY_CFG_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG0

Bits	Name	Description
15:0	TMCP0	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 0

0x01503CC4 DAY_CFG_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum number of tenures pipelined at any point during the monitoring window for tenure counter 1.

DAY_CFG_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG1

Bits	Name	Description
15:0	TMCP1	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 1

0x01503CC8 DAY_CFG_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum number of tenures pipelined at any point during the monitoring window for tenure counter 2.

DAY_CFG_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG2

Bits	Name	Description
15:0	TMCP2	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 2

0x01503CCC DAY_CFG_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum number of tenures pipelined at any point during the monitoring window for tenure counter 3.

DAY_CFG_FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG3

Bits	Name	Description
15:0	TMCP3	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 3

0x01503CD0 DAY_CFG_FABRIC_MONITOR_INFLIGHT_TENURE_CORRECTION_MODE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the activation of tenure correction mode wherein the monitors are not enabled until all outstanding transactions have been completed. This also controls the facility to correlate the enabling of a particular event counter to a tenure counter.

DAY_CFG_FABRIC_MONITOR_INFLIGHT_TENURE_CORRECTION_MODE_REG

Bits	Name	Description
15:9	RESERVED_15_9	Reserved Bits
8	EC7COR	SW : RW 1'b1: Link enable of Event Counter 7 to Tenure Counter 3 1'b0: Event Counter 7 enable is independent
7	EC6COR	SW : RW 1'b1: Link enable of Event Counter 6 to Tenure Counter 2 1'b0: Event Counter 6 enable is independent
6	EC5COR	SW : RW 1'b1: Link enable of Event Counter 5 to Tenure Counter 1 1'b0: Event Counter 5 enable is independent
5	EC4COR	SW : RW 1'b1: Link enable of Event Counter 4 to Tenure Counter 0 1'b0: Event Counter 4 enable is independent
4	EC3COR	SW : RW 1'b1: Link enable of Event Counter 3 to Tenure Counter 3 1'b0: Event Counter 3 enable is independent
3	EC2COR	SW : RW 1'b1: Link enable of Event Counter 2 to Tenure Counter 2 1'b0: Event Counter 2 enable is independent
2	EC1COR	SW : RW 1'b1: Link enable of Event Counter 1 to Tenure Counter 1 1'b0: Event Counter 1 enable is independent
1	EC0COR	SW : RW 1'b1: Link enable of Event Counter 0 to Tenure Counter 0 1'b0: Event Counter 0 enable is independent
0	PCORR	SW : RW This is the enable for tenure correction mode

0x01505000+ 0x4*v DAY_CFG_M2VMT_M2VMRv_1, v=[0..7]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics.

DAY_CFG_M2VMT_M2VMRv_1

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRv address associations.

0x01505FF4 DAY_CFG_M2VMT_REV_1

Type: Read
Clock: FABRIC_CLOCK
Reset State: ’10000000’b

Reports the revision information for the M2VMT core and wrapper.

DAY_CFG_M2VMT_REV_1

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

0x01505FF8 DAY_CFG_M2VMT_IDR_1

Type: Read
Clock: FABRIC_CLOCK
Reset State: M2VMTSIZE

Reports the size of the M2VMT table. It is a read-only register.

DAY_CFG_M2VMT_IDR_1

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

DAY_CFG_M2VMT_IDR_1 (cont.)

Bits	Name	Description
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x01506000+0x4*v DAY_CFG_M2VMT_M2VMRv_2, v=[0..7]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where v= NUM_M2VMT_ENTRIES from the design generics.

DAY_CFG_M2VMT_M2VMRv_2

Bits	Name	Description
31:5	RESERVED	v= NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	SW : RW Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRv address associations.

0x01506FF4 DAY_CFG_M2VMT_REV_2

Type: Read
Clock: FABRIC_CLOCK
Reset State: ’10000000’b

Reports the revision information for the M2VMT core and wrapper.

DAY_CFG_M2VMT_REV_2

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	SW : R Major variant field
3:0	MINOR	SW : R Minor variant field.

0x01506FF8 DAY_CFG_M2VMT_IDR_2

Type: Read
Clock: FABRIC_CLOCK
Reset State: M2VMTSIZE

Reports the size of the M2VMT table. It is a read-only register.

DAY_CFG_M2VMT_IDR_2

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.
8:0	M2VMTSIZE	SW : R M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x01510000+4*n DAY_CFG_APU0_RGn_ACR, n=[0..9]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 10, i.e, a multi-VMID full access vs. no access permission type APU. These registers include a single bit per VMID granting full access

n	
9	BAM_DMA
8	SDC5
7	SDC4
6	SDC3
5	SDC2
4	SIC_CPUI
3	SIC_DIST
2	UPRP
1	UBUF
0	UCODE

DAY_CFG_APU0_RGn_ACR

Bits	Name	Description
31:0	RWE_31_0	Read/Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the registers in the associated resource group.

0x01510F80 DAY_CFG_APU0_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

DAY_CFG_APU0_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresse) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set APU_ESR. APU_EAR and APU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set APU_ESR. APU_EAR and APU_ESYNR0 updated with address and syndrome of error.

DAY_CFG_APU0_CR (cont.)

Bits	Name	Description
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x01510F84 DAY_CFG_APU0_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port.

DAY_CFG_APU0_EAR

Bits	Name	Description
31:0	PA_31_0	The physical address of the errant request.

0x01510F88 DAY_CFG_APU0_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent

clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the APU_ESYNRn registers, which are merely the 'syndrome' of an error indicated by APU_ESR.

DAY_CFG_APU0_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) 'lock' upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x01510F8C DAY_CFG_APU0_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

DAY_CFG_APU0_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) 'lock' upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x01510F90 DAY_CFG_APU0_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

DAY_CFG_APU0_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x01510F94 DAY_CFG_APU0_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

DAY_CFG_APU0_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant reuqest
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved

DAY_CFG_APU0_ESYNR1 (cont.)

Bits	Name	Description
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x01510FF4 DAY_CFG_APU0_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

DAY_CFG_APU0_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR_3_0	Major variant field
3:0	MINOR_3_0	Minor variant field

0x01510FF8 DAY_CFG_APU0_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x00001409

APU ID Register: Read-only register that defines various configuration attributes of the APU iinstance.

DAY_CFG_APU0_IDR

Bits	Name	Description
31:29	RESERVED31_29	Reserved
28:24	MSB	Indicates most significant address bit number used to select a resource group
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full acces vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only 'owner' VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit 'owner' VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.
9:8	RESERVED9_8	Reserved
7:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

0x01510FFC DAY_CFG_APU0_APU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

APU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the APU (including the APU_APU_ACR itself).

DAY_CFG_APU0_APU_ACR

Bits	Name	Description
31:0	RWE_31_0	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the APU's 4KB address region (including the APU_APU_ACR itself). For single VMID type APUs (APU_IDR[MV] = 0) the APU_APU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

0x01520000+4*n DAY_CFG_APU1_RGn_ACR, n=[0..13]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 10, i.e, a multi-VMID full access vs. no access permission type APU. These registers include a single bit per VMID granting full access.

n	
13	USB4_HS
12	USB3_HS
11	USB2 HSIC
10	Crypto4
9	SlimBus
8	USB1 HS
7	A2 BAM
6	QUP2
5	UART2
4	GSBI2
3	QUP1
2	UART1
1	GSBI1
0	SDC1

DAY_CFG_APU1_RGn_ACR

Bits	Name	Description
31:0	RWE_31_0	Read/Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the registers in the associated resource group.

0x01520F80 DAY_CFG_APU1_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

DAY_CFG_APU1_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresse) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set APU_ESR. APU_EAR and APU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set APU_ESR. APU_EAR and APU_ESYNR0 updated with address and syndrome of error.
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x01520F84 DAY_CFG_APU1_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port. Client port addresses are 32 bits width and configuration port addresses are 12 bits wide (the width of the configuration address port).

DAY_CFG_APU1_EAR

Bits	Name	Description
31:0	PA_31_0	The physical address of the errant request.

0x01520F88 DAY_CFG_APU1_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the APU_ESYNRn registers, which are merely the 'syndrome' of an error indicated by APU_ESR.

DAY_CFG_APU1_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) 'lock' upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x01520F8C DAY_CFG_APU1_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

DAY_CFG_APU1_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) 'lock' upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x01520F90 DAY_CFG_APU1_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

DAY_CFG_APU1_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x01520F94 DAY_CFG_APU1_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

DAY_CFG_APU1_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant reuqest
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x01520FF4 DAY_CFG_APU1_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

DAY_CFG_APU1_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR_3_0	Major variant field
3:0	MINOR_3_0	Minor variant field

0x01520FF8 DAY_CFG_APU1_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x0000140D

APU ID Register: Read-only register that defines various configuration attributes of the APU iinstance.

DAY_CFG_APU1_IDR

Bits	Name	Description
31:29	RESERVED31_29	Reserved
28:24	MSB_4_0	Indicates most significant address bit number used to select a resource group
23:21	RESERVED23_21	Reserved
20:16	LSB_4_0	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT_1_0	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved

DAY_CFG_APU1_IDR (cont.)

Bits	Name	Description
11	PT	Permission type PT=0 : indicates full acces vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only 'owner' VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit 'owner' VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.
9:8	RESERVED9_8	Reserved
7:0	NRG_7_0	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

0x01520FFC DAY_CFG_APU1_APU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

APU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the APU (including the APU_APU_ACR itself).

DAY_CFG_APU1_APU_ACR

Bits	Name	Description
31:0	RWE_31_0	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the APU's 4KB address region (including the APU_APU_ACR itself). For single VMID type APUs (APU_IDR[MV] = 0) the APU_APU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

0x01530000 DAY_CFG_DAYTONA_TEST_BUS_SEL

Type: Read/Write
Clock: DFAB_CLK
Reset State: 0x00000000

Smart Peripheral Subsystem test bus selection register: this register selects whether the test bus should be disabled (default), show a pattern, or allow the core test bus to be enabled.

DAY_CFG_DAYTONA_TEST_BUS_SEL

Bits	Name	Description
31:2	RESERVED31_2	Reserved
1:0	RWE_1_0	2 bits select which test bus output to enable: select = 00 => disabled (all zeroes) select = 01 => 5 pattern (0x55555555) select = 10 => A pattern (0xAAAAAAAA) select = 11 => enable Smart Peripheral Subsystem core test bus

8.7 Multi-Media Fabric Registers (0x05200000 FABRIC_MMSS_BASE)

This section contains the Multimedia Fabric registers.

0x05200000 FABRIC_ID_REVISION_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x2C40

This register contains the upper 16-bits of the core ID and revision number and contains the Major/Minor Revision information as well as the site ID where the core was developed.

FABRIC_ID_REVISION_REG0

Bits	Name	Description
15:13	MAJ	SW : R Major Revision 0x1: Initial Release
12:10	MIN	SW : R Minor Revision 0x3: APQ8064
9:6	SITE	SW : R Site ID 0x1: RTP
5:0	RESERVED_BITS_5_0	

0x05200004 FABRIC_ID_REVISION_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0001

This register contains the lower 16-bits of the core ID and revision number and contains the Core ID number.

FABRIC_ID_REVISION_REG1

Bits	Name	Description
15:8	RESERVED_BITS_3_2	
7:0	ID	SW : R Core ID 0x1: FABRIC

0x05200008 FABRIC_CONFIGURATION_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0002

This register defines the operating frequency, power down mode for the performance monitor, as well as the decode error and performance monitor cycle counter interrupts. It also has the control bit to globally disable redirection in Fabric.

The ISYND bits contain the interrupt syndrome. If more than one interrupt type occurs, more than one bit will be set. For example, if a decode error occurs and the performance monitor cycle-counter expires, the ISYND field will contain the value 3'b101. Performance monitor interrupts are only generated when the interrupt enable (PMIE) bit is set for the interrupt type.

If multiple decode errors occur, only the first error is recorded. If multiple decode errors occur at the same clock cycle, only a single error is considered, with Master 0 having the highest priority and Master 12 the lowest priority.

The determination of the time an error is recorded in the Fabric Error Status Register (FESR) is based on the following criteria:

For Reads: When Mn_RLAST is asserted.

For Writes: When Mn_BRESP is asserted.

Therefore, if two different masters make requests with invalid addresses to the FABRIC, the master which receives the RLAST or BRESP first for the invalid transaction, is recorded in the FESR. See FABRIC_ERROR_STATUS_REG_1 for information that is captured when a decode error occurs. The address of the request which caused a decode error is captured in the FABRIC_ERROR_UPPER_ADDR_REG and the FABRIC_ERROR_LOWER_ADDR_REG. If they happen simultaneously, the master priority is used to resolve which error is recorded in a fixed priority scheme. Master 0 has highest priority and Master 31 has the lowest priority.

NOTE If the master does not have RREADY or BREADY asserted by default (i.e., it is not able to receive all responses for outstanding requests and may throttle the FABRIC), the FABRIC_Interrupt generation may precede the return of the last read data beat or the write response.

To clear the interrupt, the ISYND bits are required to be written to 3'b000.

The performance monitor event/tenure overflow condition is indicated when the ISYND value is 010. An event overflow occurs when the event counter has reached its maximum value. A tenure overflow condition occurs:

When the tenure counter has reached its maximum value

OR

More than 16 tenures are outstanding, since the performance monitor implements only 16 counters for tenure tracking. Note that if the tenure overflows, values read from the performance monitors

for min/max/total/last tenure will no longer be valid as values recorded after the overflow will be incorrect.

FABRIC_CONFIGURATION_REG

Bits	Name	Description
15:7	RESERVED_BITS_15_7	Reserved Bits
6:4	ISYND	SW : RW Interrupt syndrome* 0x0: No/Clear (interrupt) 0x1: Cycle counter expired (Perfmon) 0x2: Event/tenure overflow (Perfmon) 0x4: Decode error detected 0x5: MPU Error 0x6: Timeout Error (SPB)
3	RESERVED_BITS_3	
2	CSPDM	SW:RW CSR block power down mode 0x0: Disable Dynamic Clock Gating 0x1: Enable Dynamic Clock Gating
1	PPDM	SW : RW Performance monitor power down/disable mode 0x0: Monitor Enabled 0x1: Monitor Disabled (Gates clocks to performance monitor registers)
0	PMIE	SW : RW Perfmon interrupt enable

0x05200100+4*n FABRIC_SEGMENT_UADDR_0_REG_n, n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the upper and lower address ranges for a particular slave segment (n).If this slave segment (n) is a link then this register defines the first address range for the slave link.

NOTE A segmentation address register is required for each slave segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

FABRIC_SEGMENT_UADDR_0_REG_n

Bits	Name	Description
15:10	RESERVED_15_10	
9:0	SUA	SW : RW Segment 'n' upper address (based on parameter- up to 10-bits)

0x05200200+4*n FABRIC_SEGMENT_LADDR_0_REG_n, n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the upper and lower address ranges for a particular slave segment (n). If this slave segment (n) is a link then this register defines the first address range for the slave link.

NOTE A segmentation address register is required for each slave segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

FABRIC_SEGMENT_LADDR_0_REG_n

Bits	Name	Description
15	SSE	SW : RW Slave segment n enable

FABRIC_SEGMENT_LADDR_0_REG_n (cont.)

Bits	Name	Description
14	SSIE	SW : RW Slave segment "n" & "n+1" nterleave enable
13:10	RESERVED_13_10	
9:0	SLA	SW : RW Segment n lower address (based on parameter- up to 10-bits)

0x05200300+4*n FABRIC_SEGMENT_UADDR_1_REG_n, n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the upper address for a particular slave link segment (n) if it's a link. A link segment can have up to two separate address ranges. This register defines the second address range for the slave link.

NOTE A link segmentation address register is required for each slave link segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

FABRIC_SEGMENT_UADDR_1_REG_n

Bits	Name	Description
15:10	RESERVED_15_10	
9:0	SUA	SW : RW Segment 'n' upper address (based on parameter- up to 10-bits)

0x05200400+4*n FABRIC_SEGMENT_LADDR_1_REG_n, n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: Based on parameters passed

This register defines the lower address range for a particular slave link segment (n). A link segment can have up to two separate address ranges. This register defines the second address range for the slave link.

NOTE A segmentation link address register is required for each slave link segment supported by the FABRIC.The reset values for each of these registers is set by top-level input ports which are strapped to a value determined from a configuration file

The address decode range is based on the value of the SEG_ADDR_DECODE_SHIFT & NUM_ADDR_DECODE_BITS parameters:

A request is generated to the slave segment if the address falls within the following range:

SLA[(NUM_ADDR_DEC_BITS-1):0]

<= ADDR[MSB-(SEG_ADDR_DECODE_SHIFT):MSB-((NUM_ADDR_DEC_BITS-1)+SEG_ADDR_DECODE_SHIFT)]

<= SUA[(NUM_ADDR_DEC_BITS-1):0]

and the slave segment enable (SSE) bit is set and the slave is present (Sn_NOTPRESENT = 0).

FABRIC_SEGMENT_LADDR_1_REG_n

Bits	Name	Description
15:10	RESERVED_15_10	
9:0	SLA	SW : RW Segment n lower address (based on parameter- up to 10-bits)

0x05201000+0x0100*n+4*m FABRIC_m_WEIGHTING_REG_n, m=[0..12], n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

The values programmed into this register determine the Tier 2 weight for each master under the Tier Based Arbitration Scheme.

NOTE This register is required for each master and each slave segment supported by the FABRIC .

FABRIC_m_WEIGHTING_REG_n

Bits	Name	Description
15:8	RESERVED_BITS_15_8	
7:0	M_M_W	SW : RW Master 'm' Weight

0x05202000+0x0100*n+4*m FABRIC_m_QOS_REG_n, m=[0..3], n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

The values programmed into this register determine the Tier 1 weight for each master under the Tier Based Arbitration Scheme. Only 4 master ports can be configured as Tier 1. The QMC bits are used to configure a master port as Tier 1.

NOTE If more than one of these QOS Control registers are set to the same master port, unpredictable behavior will occur.

Set-up procedure:

1. Set the QOS enable bit.
2. Set the arbitration mode to Scheduled Access Time in the FABRIC arbitration configuration register FACR (See FABRIC_ARBITRATION_CONTROL_REG_n=[0..2]).
3. Configure the master port that needs to be set to Tier1.
4. Set the appropriate number of tokens/weight.
5. Set the MLT value (default is zero clock cycles).

NOTE Four of these registers are required for each slave segment supported by the FABRIC .

FABRIC_m_QOS_REG_n

Bits	Name	Description
15:14	RESERVED_BITS15_13	
13:10	MLT	SW : RW MLT Value
9	QE	SW : RW QOS Enable

FABRIC_m_QOS_REG_n (cont.)

Bits	Name	Description
8:4	QMC	SW : RW QOS Master Configuration 0x0: Master Port 0 0x1: Master Port 1 0x2: Master Port 2 0x3: Master Port 3 0x4: Master Port 4 0x5: Master Port 5 0x6: Master Port 6 0x7: Master Port 7 0x8: Master Port 8 0x9: Master Port 9 0xA: Master Port 10 0xB: Master Port 11 0xC: Master Port 12 0xD: Master Port 13 0xE: Master Port 14 0xF: Master Port 15 0x10: Master Port 16 0x11: Master Port 17 0x12: Master Port 18 0x13: Master Port 19 0x14: Master Port 20 0x15: Master Port 21 0x16: Master Port 22 0x17: Master Port 23 0x18: Master Port 24 0x19: Master Port 25 0x1A: Master Port 26 0x1B: Master Port 27 0x1C: Master Port 28 0x1D: Master Port 29 0x1E: Master Port 30 0x1F: Master Port 31
3:0	M_M_QW	SW : RW Master 'm' QOS Weight

0x05203000+4*n FABRIC_BUS_INTERVAL_REG_n, n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register sets the bus interval value for Tier 2 masters.

NOTE A control register is implemented for each slave segment supported by the FABRIC .

FABRIC_BUS_INTERVAL_REG_n

Bits	Name	Description
15:0	IBI	SW : RW Intct bus interval (in clock cycles)

0x05203100+ 4*n FABRIC_QOS_INTERVAL_REG_n, n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register sets the QOS interval value for Tier 1 masters.

NOTE A control register is required for each slave segment supported by the FABRIC .

FABRIC_QOS_INTERVAL_REG_n

Bits	Name	Description
15:8	RESERVED_BITS15_8	
7:0	QBI	SW : RW QOS bus interval (in clock cycles)

0x05203200+ 4*n FABRIC_ARBITRATION_CONTROL_REG_n, n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x00FF

This register controls the arbitration mode and the pipeline depth of a particular slave segment.

NOTE A control register is implemented for each slave segment supported by the FABRIC .

FABRIC_ARBITRATION_CONTROL_REG_n

Bits	Name	Description
15	QLP	SW : RW QOS Timer Low Power Mode 0x1: Enable 0x0: Disable
14:13	QHI	SW : RW QOS Timer Halt Interval 0x0: Stop after 1 interval of inactivity 0x1: Stop after 2 intervals of inactivity 0x2: Stop after 4 intervals of inactivity 0x3: Stop after 8 intervals of inactivity
12	BLP	SW : RW Bus Interval Low Power Mode 0x1: Enable 0x0: Disable
11:10	BHI	SW : RW Bus Interval Halt Interval 0x0: Stop after 1 interval of inactivity 0x1: Stop after 2 intervals of inactivity 0x2: Stop after 4 intervals of inactivity 0x3: Stop after 8 intervals of inactivity
9	QCE	SW : RW QoS Channel Enable 0x0: Disable (default) 0x1: Enable
8	IAM	SW : RW FABRIC arbitration mode 0x0: Fair round-robin (default) 0x1: Scheduled access time

FABRIC_ARBITRATION_CONTROL_REG_n (cont.)

Bits	Name	Description
7:4	IRPD	SW : RW FABRIC read pipeline depth 0x0: Pipeline depth = 1 0x1: Pipeline depth = 2 0x2: Pipeline depth = 3 0x3: Pipeline depth = 4 0x4: Pipeline depth = 5 0x5: Pipeline depth = 6 0x6: Pipeline depth = 7 0x7: Pipeline depth = 8 0x8: Pipeline depth = 9 0x9: Pipeline depth = 10 0xA: Pipeline depth = 11 0xB: Pipeline depth = 12 0xC: Pipeline depth = 13 0xD: Pipeline depth = 14 0xE: Pipeline depth = 15 0xF: Pipeline depth = 16
3:0	IWPD	SW : RW FABRIC Write Pipeline Depth 0x0: Pipeline depth = 1 0x1: Pipeline depth = 2 0x2: Pipeline depth = 3 0x3: Pipeline depth = 4 0x4: Pipeline depth = 5 0x5: Pipeline depth = 6 0x6: Pipeline depth = 7 0x7: Pipeline depth = 8 0x8: Pipeline depth = 9 0x9: Pipeline depth = 10 0xA: Pipeline depth = 11 0xB: Pipeline depth = 12 0xC: Pipeline depth = 13 0xD: Pipeline depth = 14 0xE: Pipeline depth = 15 0xF: Pipeline depth = 16

0x05203300+4*n FABRIC_MASTER_INTERFACE_REG_n, n=[0..12]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0084

This register controls the following master port attributes:

- whether the master request priority signals are used by the internal arbiter
- the redirection of cacheable coherent requests
- write gathering on AXI
- write packing on AHB

This register also controls a particular master's halt interface and for AHB master interfaces, it enables write packing functionality for posted writes.

When the MHR bit is set, the FABRIC_MnHALTREQ signal is asserted. The MHA and MHI fields capture the state of the FABRIC_MnHALTACK and FABRIC_MnIDLE signals at every clock cycle.

NOTE A register is implemented for each master interface supported by the FABRIC

FABRIC_MASTER_INTERFACE_REG_n

Bits	Name	Description
15	RESERVED_BIT_15	
14	OWGM	SW : RW Enable optimized write gathering mode. SW should disable for AXI Ports
13	DBW	SW : RW Disable Bufferable writes. Treats Bufferable writes as Non Bufferable writes (AHB only)
12	PRIEN	SW : RW Enable Request Priority Lets the slave way arbiter consider the master request priority AREQPRIORITY[1:0] signal that is driven with each transaction
11	RCOSH	SW : RW Redirect Cacheable-outer-sharable Governs whether or not cacheable accesses that are outer-sharable are redirected to the Scorpion-MP L2 slave port
10	RCISH	SW : RW Redirect Cacheable-inner-sharable Governs whether or not cacheable accesses that are inner-sharable are redirected to the Scorpion-MP L2 slave port
9	RCNSH	SW : RW Redirect Cacheable-non-sharable Governs whether or not cacheable accesses that are non-sharable are redirected to the Scorpion-MP L2 slave port
8	CRE	SW : RW Enable redirection of cachable coherent requests

FABRIC_MASTER_INTERFACE_REG_n (cont.)

Bits	Name	Description
7	WGE	SW : RW Write Gathering Enable (AXI only)
6	WPE	SW : RW Write Packing Enable (AHB Only) When enabled, the master port will pack indeterminate INCR burst writes, if disabled, the master port will break indeterminate INCR burst writes into SINGLES. 0x1: Enable 0x0: Disable
5:4	IIIW	SW : RW Bufferable Indeterminate INCR WR packing (AHB only): 0x0: break into INCR4 0x1: break into INCR8 0x3: break into INCR16
3	MID	SW : RW Master Interface Disable. SW diable of Master interface.
2	MI	SW : R Master Idle. Indicates that the Master does not have any pending bus transactions. For AHB busses, this bit is set internally by the FABRIC AHB Master port. For AXI masters, this value is driven by the master that is connected to the port.
1	MHA	SW : R Master halt acknowledge. Only valid for AXI masters. This bit is 0 on AHB master ports.
0	MHR	SW : RW Master halt request. Only valid for AXI masters. Writing this bit has no effect for AHB masters.

0x05203430 FABRIC_SLAVE_ARBITRATION_DISABLE_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is RESERVED.

FABRIC_SLAVE_ARBITRATION_DISABLE_REG

Bits	Name	Description
15	S15AD	SW : R RESERVED

FABRIC_SLAVE_ARBITRATION_DISABLE_REG (cont.)

Bits	Name	Description
14	S14AD	SW : R RESERVED
13	S13AD	SW : R RESERVED
12	S12AD	SW : R RESERVED
11	S11AD	SW : R RESERVED
10	S10AD	SW : R RESERVED
9	S9AD	SW : R RESERVED
8	S8AD	SW : R RESERVED
7	S7AD	SW : R RESERVED
6	S6AD	SW : R RESERVED
5	S5AD	SW : R RESERVED
4	S4AD	SW : R RESERVED
3	S3AD	SW : R RESERVED
2	S2AD	SW : R RESERVED
1	S1AD	SW : R RESERVED
0	S0AD	SW : R RESERVED

0x05203434 FABRIC_SLAVE_BYPASS_BUFFER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register enables the bypass buffer functionality in a slave way (if implemented).

FABRIC_SLAVE_BYPASS_BUFFER_REG

Bits	Name	Description
15	S15BE	SW : RW Slave 15 Bypass Buffer Enable
14	S14BE	SW : RW Slave 14 Bypass Buffer Enable
13	S13BE	SW : RW Slave 13 Bypass Buffer Enable
12	S12BE	SW : RW Slave 12 Bypass Buffer Enable
11	S11BE	SW : RW Slave 11 Bypass Buffer Enable
10	S10BE	SW : RW Slave 10 Bypass Buffer Enable
9	S9BE	SW : RW Slave 9 Bypass Buffer Enable
8	S8BE	SW : RW Slave 8 Bypass Buffer Enable
7	S7BE	SW : RW Slave 7 Bypass Buffer Enable
6	S6BE	SW : RW Slave 6 Bypass Buffer Enable
5	S5BE	SW : RW Slave 5 Bypass Buffer Enable
4	S4BE	SW : RW Slave 4 Bypass Buffer Enable
3	S3BE	SW : RW Slave 3 Bypass Buffer Enable
2	S2BE	SW : RW Slave 2 Bypass Buffer Enable
1	S1BE	SW : RW Slave 1 Bypass Buffer Enable
0	S0BE	SW : RW Slave 0 Bypass BufferBuffer Enable

0x05203438 FABRIC_SLAVE_STATUS_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the status of each slave.

- A 1 indicates that the slave is idle.
- A 0 indicates that the slave is busy processing a transfer and/or the FABRIC is has not completed sending transactions to the slave.

FABRIC_SLAVE_STATUS_REG

Bits	Name	Description
15	S15S	SW : R Slave 15 Status
14	S14S	SW : R Slave 14 Status
13	S13S	SW : R Slave 13 Status
12	S12S	SW : R Slave 12 Status
11	S11S	SW : R Slave 11 Status
10	S10S	SW : R Slave 10 Status
9	S9S	SW : R Slave 9 Status
8	S8S	SW : R Slave 8 Status
7	S7S	SW : R Slave 7 Status
6	S6S	SW : R Slave 6 Status
5	S5S	SW : R Slave 5 Status
4	S4S	SW : R Slave 4 Status

FABRIC_SLAVE_STATUS_REG (cont.)

Bits	Name	Description
3	S3S	SW : R Slave 3 Status
2	S2S	SW : R Slave 2 Status
1	S1S	SW : R Slave 1 Status
0	S0S	SW : R Slave 0 Status

0x05203500 FABRIC_TEST_INTERFACE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls:

- the grouping of signals that are driven out on the test bus (FABRIC_TESTBUS[31:0])
- Selection of MISR slave way and channel input

MEN: Selects which MISR output is driven onto the test-bus. For example, setting MEN to 00010 selects the MISR in slave segment 2. The MEN bits are only valid when the testmode (TMODE) is set to 000000 and test-enable is set (TEN)

TMODE: Selects the various test-bus modes

TEN: Test-enable. Must be set for values to be driven onto the test-bus OR for MISR to be enabled.

FABRIC_TEST_INTERFACE_REG

Bits	Name	Description
15:14	RESERVED_BITS15_14	
13:12	MSEL	SW : RW MISR input selection: 0x0: Address channel 0x1: Write channel 0x2: Read channel 0x3: Write response channel

FABRIC_TEST_INTERFACE_REG (cont.)

Bits	Name	Description
11:7	MEN	SW : RW MISR Enable 0x1: Slave Segment 0 0x2: Slave Segment 1 0x3: Slave Segment 2 0x4: Slave Segment 3 0x5: Slave Segment 4 0x6: Slave Segment 5 0x7: Slave Segment 6 0x8: Slave Segment 7 0x9: Slave Segment 8 0xA: Slave Segment 9 0xB: Slave Segment 10 0xC: Slave Segment 11 0xD: Slave Segment 12 0xE: Slave Segment 13 0xF: Slave Segment 14 0x10: Slave Segment 15

FABRIC_TEST_INTERFACE_REG (cont.)

Bits	Name	Description
6:1	TMODE	SW : RW Test Mode: 0x0: Testbus M0 0x1: Testbus M1 0x2: Testbus M2 0x3: Testbus M3 0x4: Testbus M4 0x5: Testbus M5 0x6: Testbus M6 0x7: Testbus M7 0x8: Testbus M8 0x9: Testbus M9 0xA: Testbus M10 0xB: Testbus M11 0xC: Testbus M12 0xD: Testbus M13 0xE: Testbus M14 0xF: Testbus M15 0x10: Testbus M16 0x11: Testbus M17 0x12: Testbus M18 0x13: Testbus M19 0x14: Testbus M20 0x15: Testbus M21 0x16: Testbus M22 0x17: Testbus M23 0x18: Testbus M24 0x19: Testbus M25 0x1A: Testbus M26 0x1B: Testbus M27 0x1C: Testbus M28 0x1D: Testbus M29 0x1E: Testbus M30 0x1F: Testbus M31 0x20: Testbus S0 0x21: Testbus S1 0x22: Testbus S2 0x23: Testbus S3 0x24: Testbus S4 0x25: Testbus S5 0x26: Testbus S6 0x27: Testbus S7 0x28: Testbus S8 0x29: Testbus S9 0x2A: Testbus S10 0x2B: Testbus S11 0x2C: Testbus S12

FABRIC_TEST_INTERFACE_REG (cont.)

Bits	Name	Description
6:1	TMODE (CONT'D)	0x2D: Testbus S13 0x2E: Testbus S14 0x2F: Testbus S15 0x30: Reserved_1 0x31: Reserved_2 0x32: Reserved_3 0x33: Reserved_4 0x34: Reserved_5 0x35: Reserved_6 0x36: Reserved_7 0x37: Reserved_8 0x38: Reserved_9 0x39: Reserved_10 0x3A: Reserved_11 0x3B: Reserved_12 0x3C: Reserved_13 0x3D: Reserved_14 0x3E: Reserved_15 0x3F: Reserved_16
0	TEN	SW : RW Test Enable

0x05203504 FABRIC_ERROR_STATUS_REG_0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

FABRIC_ERROR_STATUS_REG_0

Bits	Name	Description
15:0	MID	SW : R AMID for AXI port HMID for AHB port

0x05203508 FABRIC_ERROR_STATUS_REG_1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

FABRIC_ERROR_STATUS_REG_1

Bits	Name	Description
15:8	TID	SW : R Transaction ID Only Applicable for AXI Transfers ZERO for AHB Transfers
7:6	RESERVED_BITS_7_6	Reserved
5:0	MPORT	SW : R Master port that generated the error

0x0520350C FABRIC_ERROR_STATUS_REG_2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

FABRIC_ERROR_STATUS_REG_2

Bits	Name	Description
15:12	RESERVED_BITS_15_12	Reserved
11	BURST	SW : R Burst transfer
10	OOOWR	SW : R OOO write response Only Applicable for AXI
9	OOORD	SW : R OOO read response Only Applicable for AXI

FABRIC_ERROR_STATUS_REG_2 (cont.)

Bits	Name	Description
8:7	LOCK	SW : R Lock Transfer
6:4	SIZE	SW : R Transfer Size
3:0	TYPE	SW : R Transfer Type Only Applicable for AXI

0x05203510 FABRIC_ERROR_STATUS_REG_3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the address channel transfer qualifiers for the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

FABRIC_ERROR_STATUS_REG_3

Bits	Name	Description
15:8	RESERVED_BITS_15_8	Reserved
7	PROTNS	SW : R APROTNS/HPROTNS
6	PROTIND	SW : R PROTIND
5	AISH	SW : R Inner Shared
4	WRITE	SW : R Write transfer
3:0	LEN	SW : R Transfer Length

0x05203514 FABRIC_ERROR_UPPER_ADDR_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address of the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

FABRIC_ERROR_UPPER_ADDR_REG

Bits	Name	Description
15:0	EUA	SW : R Bits [31:16] of the address which generated a decode error

0x05203518 FABRIC_ERROR_LOWER_ADDR_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address of the request which generated a decode error. The value of the register is valid only when the FABRIC_Interrupt signal is asserted and ISYND in the FCR is set to one (See FABRIC_CONFIGURATION_REG).

FABRIC_ERROR_LOWER_ADDR_REG

Bits	Name	Description
15:0	ELR	SW : R Bits [15:0] of the address which generated a decode error

0x0520351C FABRIC_MISR_SIGNATURE_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG.

FABRIC_MISR_SIGNATURE_REG0

Bits	Name	Description
15:0	SIG0	SW : R Bits [15:0] of 64-bit MISR signature

0x05203520 FABRIC_MISR_SIGNATURE_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG

FABRIC_MISR_SIGNATURE_REG1

Bits	Name	Description
15:0	SIG1	SW : R Bits [31:16] of 64-bit MISR signature

0x05203524 FABRIC_MISR_SIGNATURE_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 47:32 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG

FABRIC_MISR_SIGNATURE_REG2

Bits	Name	Description
15:0	SIG2	SW : R Bits [47:32] of 64-bit MISR signature

0x05203528 FABRIC_MISR_SIGNATURE_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 63:48 of the MISR signature. This register's contents are valid only when the TMODE and TEN fields in the FABRIC_TEST_INTERFACE_REG are set to 000000 and 1 respectively. The value that is stored in these registers is selected based on the channel selection and the slave way that is configured in the FABRIC_TEST_INTERFACE_REG

FABRIC_MISR_SIGNATURE_REG3

Bits	Name	Description
15:0	SIG3	SW : R Bits [63:48] of 64-bit MISR signature

0x0520352C FTMR_TESTBUS_MODE_REGISTER

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

For the testbus selected of master or slave port in FABRIC_TEST_INTERFACE_REG, user can program the testbus mode via this register

FTMR_TESTBUS_MODE_REGISTER

Bits	Name	Description
15:3	RESERVED_BITS15_3	Reserved
2:0	MODE	0x0: Default Mode 0x1: Address channel attributes at the interface 0x2: Address at the interface 0x3: Misc 0x4: Write data Lower 32 bits at interface 0x5: Write data Upper 32 bits at interface 0x6: Read data Lower 32 bits at interface 0x7: Read data Upper 32 bits at interface

0x05203600+4*n FABRIC_MASTER_CLOCK_HALT_REG_n, n=[0..12]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt & change functionality within the FABRIC master ports. To enable the clock halting functionality, the clock halt enable bit (CHTEN) needs to be set. The hysteresis timer value is a 10-bit timer (running on FCLK) value that is set using the CHTMR bits. The clock change and MODE bits are used to change the interface between sync/async/isosync modes.

NOTE A register is implemented for each master interface supported by the FABRIC .

FABRIC_MASTER_CLOCK_HALT_REG_n

Bits	Name	Description
15	CHTEN	SW : RW Clock halt enable. Enables clock halt functionality for this port.
14	CCDONE	SW : RW Clock mode change completed/done
13	CCACK	SW : R Clock mode change acknowledge
12	CCREQ	SW : RW Clock mode change request
11:10	MODE	SW : RW Master clock interface mode 0x0: ASYNC 0x1: SYNC 0x2: ISOSYNC port clk slower. 0x3: ISOSYNC port clk faster.
9:0	CHTMR	SW : RW Master clock halt timer: clock cycles of inactivity that should pass before clock is halted

0x05203800+4*n FABRIC_SLAVE_CLOCK_HALT_REG_n, n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt & change functionality within the FABRIC slave ways. To enable the clock halting functionality, the clock halt enable bit (CHTEN) needs to be set. The hysteresis timer value is a 10-bit timer (running on FCLK) value that is set using the CHTMR bits. The clock change and MODE bits are used to change the interface between sync/async/isosync modes.

NOTE A register is implemented for each slave interface supported by the FABRIC .

FABRIC_SLAVE_CLOCK_HALT_REG_n

Bits	Name	Description
15	CHTEN	SW : RW Clock halt enable. Enables clock halt functionality for this port.

FABRIC_SLAVE_CLOCK_HALT_REG_n (cont.)

Bits	Name	Description
14	CCDONE	SW : RW Cock mode change completed/done
13	CCACK	SW : RW Clock mode change acknowledge
12	CCREQ	SW : RW Clock mode change request
11:10	MODE	SW : RW Slave clock interface mode 0x0: ASYNC 0x1: SYNC 0x2: ISOSYNC port clk slower. 0x3: ISOSYNC port clk faster.
9:0	CHTMR	SW : RW Slave clock halt timer: clock cycles of inactivity that should pass before clock is halted

0x05203880 FABRIC_SLAVE_ARBITER_CLOCK_HALT_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to enable the low power mode clock halt functionality within the FABRIC slave ways arbiter.

FABRIC_SLAVE_ARBITER_CLOCK_HALT_REG

Bits	Name	Description
15	S15CHTEN	SW : RW S15 Arbiter Clock halt enable.
14	S14CHTEN	SW : RW S14 Arbiter Clock halt enable.
13	S13CHTEN	SW : RW S13 Arbiter Clock halt enable.
12	S12CHTEN	SW : RW S12 Arbiter Clock halt enable.

FABRIC_SLAVE_ARBITER_CLOCK_HALT_REG (cont.)

Bits	Name	Description
11	S11CHTEN	SW : RW S11 Arbiter Clock halt enable.
10	S10CHTEN	SW : RW S10 Arbiter Clock halt enable.
9	S9CHTEN	SW : RW S9 Arbiter Clock halt enable.
8	S8CHTEN	SW : RW S8 Arbiter Clock halt enable.
7	S7CHTEN	SW : RW S7 Arbiter Clock halt enable.
6	S6CHTEN	SW : RW S6 Arbiter Clock halt enable.
5	S5CHTEN	SW : RW S5 Arbiter Clock halt enable.
4	S4CHTEN	SW : RW S4 Arbiter Clock halt enable.
3	S3CHTEN	SW : RW S3 Arbiter Clock halt enable.
2	S2CHTEN	SW : RW S2 Arbiter Clock halt enable.
1	S1CHTEN	SW : RW S1 Arbiter Clock halt enable.
0	S0CHTEN	SW : RW S0 Arbiter Clock halt enable.

0x05203884+4*n FABRIC_SLAVE_CLOCK_ON_CFG_REG_n, n=[0..2]

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register is used to set wake-up timer values durin g HW clock gating functionality for the Fabric slave ways arbiter and AHB/AXI slaves connected to Fabric.

FABRIC_SLAVE_CLOCK_ON_CFG_REG_n

Bits	Name	Description
15:4	RESERVED_BITS_15_4	Reserved

FABRIC_SLAVE_CLOCK_ON_CFG_REG_n (cont.)

Bits	Name	Description
3:0	COD	SW : RW Slave Way Clock On Delay

0x052038F8 FABRIC_MONITOR_ENABLE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the trigger selection and enabling of event and cycle counters.

NOTE When PTRIG is set to use any of the external trigger signals, the external triggers incur a 2 cycle delay from the positive edge assertion of the signal to when the actual counters are enabled in the performance monitor. This allows synchronization of the external signals into the FABRIC clock domain.

FABRIC_MONITOR_ENABLE_REG

Bits	Name	Description
15:13	PTRIG	SW : RW 0x5: Manual Enable/ Manual Disable 0x4: Int Trig/Ext Trig 0x3: Ext Trig 0x2: Ext Trig/CC expire 0x1: Int Trig/CC expire 0x0: Manual enable/CC expire (No trigger)
12	ECC	SW : RW Enable cycle counter
11:8	RESERVED_BITS_11_8	Reserved
7	EEC7	SW : RW Enable event counter 7
6	EEC6	SW : RW Enable event counter 6
5	EEC5	SW : RW Enable event counter 5
4	EEC4	SW : RW Enable event counter 4
3	EEC3	SW : RW Enable event counter 3

FABRIC_MONITOR_ENABLE_REG (cont.)

Bits	Name	Description
2	EEC2	SW : RW Enable event counter 2
1	EEC1	SW : RW Enable event counter 1
0	EEC0	SW : RW Enable event counter 0

0x052038FC FABRIC_MONITOR_RESET_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the resets for event and cycle counters.

FABRIC_MONITOR_RESET_REG

Bits	Name	Description
15:8	RESERVED_BITS_15_8	Reserved
7	REC7	SW : RW Reset event counter 7 (automatically resets the cycle-counter as well)
6	REC6	SW : RW Reset event counter 6 (automatically resets the cycle-counter as well)
5	REC5	SW : RW Reset event counter 5 (automatically resets the cycle-counter as well)
4	REC4	SW : RW Reset event counter 4 (automatically resets the cycle-counter as well)
3	REC3	SW : RW Reset event counter 3 (automatically resets the cycle-counter as well)
2	REC2	SW : RW Reset event counter 2 (automatically resets the cycle-counter as well)
1	REC1	SW : RW Reset event counter 1 (automatically resets the cycle-counter as well)

FABRIC_MONITOR_RESET_REG (cont.)

Bits	Name	Description
0	REC0	SW : RW Reset event counter 0 (automatically resets the cycle-counter as well)

0x05203900 FABRIC_MONITOR_TENURE_ENABLE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the trigger selection and enabling of tenure counters.

NOTE When PTRIG is set to use any of the external trigger signals, the external triggers incur a 2 cycle delay from the positive edge assertion of the signal to when the actual counters are enabled in the performance monitor. This allows synchronization of the external signals into the FABRIC clock domain.

FABRIC_MONITOR_TENURE_ENABLE_REG

Bits	Name	Description
15:5	RESERVED_BITS_15_5	Reserved
4	ETTF	SW : RW Enable tenure table fix This bit, when set, enables a the following feature: The tenure table for each tenure counter will track atleast 16 tenures properly without overflowing
3	ETC3	SW : RW Enable tenure counter 3
2	ETC2	SW : RW Enable tenure counter 2
1	ETC1	SW : RW Enable tenure counter 1
0	ETC0	SW : RW Enable tenure counter 0

0x05203904 FABRIC_MONITOR_TENURE_RESET_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the resets for tenure counters and cycle counters.

FABRIC_MONITOR_TENURE_RESET_REG

Bits	Name	Description
15:4	RESERVED_BITS_15_4	Reserved
3	RTC3	SW : RW Reset tenure counter 3 (automatically resets the cycle-counter as well)
2	RTC2	SW : RW Reset tenure counter 2 (automatically resets the cycle-counter as well)
1	RTC1	SW : RW Reset tenure counter 1 (automatically resets the cycle-counter as well)
0	RTC0	SW : RW Reset tenure counter 0 (automatically resets the cycle-counter as well)

0x05203908 FABRIC_MONITOR_SELECTION_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 0.

FABRIC_MONITOR_SELECTION_LOWER_REG0

Bits	Name	Description
15:13	E0ES	SW : RW Event counter 0 event selection 0x0: Read burst 0 (Master/slave) 0x1: Write burst 0 (Master/slave) 0x2: Address transfer count 0 (Master/slave) 0x3: Read transfer count 0 (Master/slave) 0x4: Write transfer count 0 (Master/slave) 0x5: Write (bufferable burst 0 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E0MIDFEN	SW : RW Event counter 0 MID Filtering enable 0x0: Disabled 0x1: Enabled

FABRIC_MONITOR_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
10	E0INDFEN	SW : RW Event counter 0 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E0IND	SW : RW Event counter 0 Instruction/Data selection 0x0: Data 0x1: Instruction
8:4	E0MPS	SW : RW Event counter 0 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

FABRIC_MONITOR_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
3:0	E0SWS	SW : RW Event counter 0 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0520390C FABRIC_MONITOR_SELECTION_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 0.

FABRIC_MONITOR_SELECTION_UPPER_REG0

Bits	Name	Description
15:0	E0MID	SW : RW Event counter 0 MID selection (If MID filtering enabled)

0x05203910 FABRIC_MONITOR_SELECTION_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 1.

FABRIC_MONITOR_SELECTION_LOWER_REG1

Bits	Name	Description
15:13	E1ES	SW : RW Event counter 1event selection 0x0: Read burst 1 (Master/slave) 0x1: Write burst 1 (Master/slave) 0x2: Address transfer count 1 (Master/slave) 0x3: Read transfer count 1 (Master/slave) 0x4: Write transfer count 1 (Master/slave) 0x5: Write (bufferable burst 1 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E1MIDFEN	SW : RW Event counter 1 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E1INDFEN	SW : RW Event counter 1Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E1IND	SW : RW Event counter 1Instruction/Data selection 0x0: Data 0x1: Instruction

FABRIC_MONITOR_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
8:4	E1MPS	SW : RW Event counter 1Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

FABRIC_MONITOR_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
3:0	E1SWS	SW : RW Event counter 1Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x05203914 FABRIC_MONITOR_SELECTION_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 1.

FABRIC_MONITOR_SELECTION_UPPER_REG1

Bits	Name	Description
15:0	E1MID	SW : RW Event counter 1MID selection (If MID filtering enabled)

0x05203918 FABRIC_MONITOR_SELECTION_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 2.

FABRIC_MONITOR_SELECTION_LOWER_REG2

Bits	Name	Description
15:13	E2ES	SW : RW Event counter 2event selection 0x0: Read burst 2 (Master/slave) 0x1: Write burst 2 (Master/slave) 0x2: Address transfer count 2 (Master/slave) 0x3: Read transfer count 2 (Master/slave) 0x4: Write transfer count 2 (Master/slave) 0x5: Write (bufferable burst 2 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E2MIDFEN	SW : RW Event counter 2MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E2INDFEN	SW : RW Event counter 2Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E2IND	SW : RW Event counter 2Instruction/Data selection 0x0: Data 0x1: Instruction

FABRIC_MONITOR_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
8:4	E2MPS	SW : RW Event counter 2Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

FABRIC_MONITOR_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
3:0	E2SWS	SW : RW Event counter 2Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0520391C FABRIC_MONITOR_SELECTION_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 2.

FABRIC_MONITOR_SELECTION_UPPER_REG2

Bits	Name	Description
15:0	E2MID	SW : RW Event counter 2 MID selection (If MID filtering enabled)

0x05203920 FABRIC_MONITOR_SELECTION_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 3.

FABRIC_MONITOR_SELECTION_LOWER_REG3

Bits	Name	Description
15:13	E3ES	SW : RW Event counter 3event selection 0x0: Read burst 3 (Master/slave) 0x1: Write burst 3 (Master/slave) 0x2: Address transfer count 3 (Master/slave) 0x3: Read transfer count 3 (Master/slave) 0x4: Write transfer count 3 (Master/slave) 0x5: Write (bufferable burst 3 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	RESERVED_BIT_12	Reserved
11	E3MIDFEN	SW : RW Event counter 3MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E3INDFEN	SW : RW Event counter 3Instruction/Data Filtering enable 0x0: Disabled 0x1: Enable
9	E3IND	SW : RW Event counter 3Instruction/Data selection 0x0: Data 0x1: Instruction

FABRIC_MONITOR_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
8:4	E3MPS	SW : RW Event counter 3Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

FABRIC_MONITOR_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
3:0	E3SWS	SW : RW Event counter 3 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x05203924 FABRIC_MONITOR_SELECTION_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 3.

FABRIC_MONITOR_SELECTION_UPPER_REG3

Bits	Name	Description
15:0	E3MID	SW : RW Event counter 3 MID selection (If MID filtering enabled)

0x05203928 FABRIC_MONITOR_SELECTION_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 4.

FABRIC_MONITOR_SELECTION_LOWER_REG4

Bits	Name	Description
15:13	E4ES	SW : RW Event counter 4event selection 0x0: Read burst 4 (Master/slave) 0x1: Write burst 4 (Master/slave) 0x2: Address transfer count 4 (Master/slave) 0x3: Read transfer count 4 (Master/slave) 0x4: Write transfer count 4 (Master/slave) 0x5: Write (bufferable burst 4AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	SEL_SPDM_OUT0	SW : RW 0x0: Send total tenure overflow info (for tenure counter 0 to SPDM) 0x1: Send individual counter overflow info (for tenure counter 0 to SPDM)
11	E4MIDFEN	SW : RW Event counter 4 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E4INDFEN	SW : RW Event counter 4 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E4IND	SW : RW Event counter 4 Instruction/Data selection 0x0: Data 0x1: Instruction

FABRIC_MONITOR_SELECTION_LOWER_REG4 (cont.)

Bits	Name	Description
8:4	E4MPS	SW : RW Event counter 4 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

FABRIC_MONITOR_SELECTION_LOWER_REG4 (cont.)

Bits	Name	Description
3:0	E4SWS	SW : RW Event counter 4 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0520392C FABRIC_MONITOR_SELECTION_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 4.

FABRIC_MONITOR_SELECTION_UPPER_REG4

Bits	Name	Description
15:0	E4MID	SW : RW Event counter 4 MID selection (If MID filtering enabled)

0x05203930 FABRIC_MONITOR_SELECTION_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 5.

FABRIC_MONITOR_SELECTION_LOWER_REG5

Bits	Name	Description
15:13	E5ES	SW : RW Event counter 5 event selection 0x0: Read burst 5 (Master/slave) 0x1: Write burst 5 (Master/slave) 0x2: Address transfer count 5 (Master/slave) 0x3: Read transfer count 5 (Master/slave) 0x4: Write transfer count 5 (Master/slave) 0x5: Write (bufferable burst 5 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	SEL_SPDM_OUT1	SW : RW 0x0: Send total tenure overflow info (for tenure counter 1 to SPDM) 0x1: Send individual counter overflow info (for tenure counter 1 to SPDM)
11	E5MIDFEN	SW : RW Event counter 5 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E5INDFEN	SW : RW Event counter 5 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E5IND	SW : RW Event counter 5 Instruction/Data selection 0x0: Data 0x1: Instruction

FABRIC_MONITOR_SELECTION_LOWER_REG5 (cont.)

Bits	Name	Description
8:4	E5MPS	SW : RW Event counter 5 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

FABRIC_MONITOR_SELECTION_LOWER_REG5 (cont.)

Bits	Name	Description
3:0	E5SWS	SW : RW Event counter 5 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x05203934 FABRIC_MONITOR_SELECTION_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 5.

FABRIC_MONITOR_SELECTION_UPPER_REG5

Bits	Name	Description
15:0	E5MID	SW : RW Event counter 5 MID selection (If MID filtering enabled)

0x05203938 FABRIC_MONITOR_SELECTION_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 6.

FABRIC_MONITOR_SELECTION_LOWER_REG6

Bits	Name	Description
15:13	E6ES	SW : RW Event counter 6 event selection 0x0: Read burst 6 (Master/slave) 0x1: Write burst 6 (Master/slave) 0x2: Address transfer count 6 (Master/slave) 0x3: Read transfer count 6 (Master/slave) 0x4: Write transfer count 6 (Master/slave) 0x5: Write (bufferable burst 6 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	SEL_SPDM_OUT2	SW : RW 0x0: Send total tenure overflow info (for tenure counter 2 to SPDM) 0x1: Send individual counter overflow info (for tenure counter 2 to SPDM)
11	E6MIDFEN	SW : RW Event counter 6 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E6INDFEN	SW : RW Event counter 6 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E6IND	SW : RW Event counter 6 Instruction/Data selection 0x0: Data 0x1: Instruction

FABRIC_MONITOR_SELECTION_LOWER_REG6 (cont.)

Bits	Name	Description
8:4	E6MPS	SW : RW Event counter 6 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

FABRIC_MONITOR_SELECTION_LOWER_REG6 (cont.)

Bits	Name	Description
3:0	E6SWS	SW : RW Event counter 6 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x0520393C FABRIC_MONITOR_SELECTION_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 6.

FABRIC_MONITOR_SELECTION_UPPER_REG6

Bits	Name	Description
15:0	E6MID	SW : RW Event counter 6 MID selection (If MID filtering enabled)

0x05203940 FABRIC_MONITOR_SELECTION_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the event and port selection and filtering criteria for event counter 7.

FABRIC_MONITOR_SELECTION_LOWER_REG7

Bits	Name	Description
15:13	E7ES	SW : RW Event counter 7 event selection 0x0: Read burst 7 (Master/slave) 0x1: Write burst 7 (Master/slave) 0x2: Address transfer count 7 (Master/slave) 0x3: Read transfer count 7 (Master/slave) 0x4: Write transfer count 7 (Master/slave) 0x5: Write (bufferable burst 7 AHB Master only) 0x3: b110 ’ 3:b111: Reserved
12	SEL_SPDM_OUT3	SW : RW 0x0: Send total tenure overflow info (for tenure counter 3 to SPDM) 0x1: Send individual counter overflow info (for tenure counter 3 to SPDM)
11	E7MIDFEN	SW : RW Event counter 7 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	E7INDFEN	SW : RW Event counter 7 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	E7IND	SW : RW Event counter 7 Instruction/Data selection 0x0: Data 0x1: Instruction

FABRIC_MONITOR_SELECTION_LOWER_REG7 (cont.)

Bits	Name	Description
8:4	E7MPS	SW : RW Event counter 7 Master port selection 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

FABRIC_MONITOR_SELECTION_LOWER_REG7 (cont.)

Bits	Name	Description
3:0	E7SWS	SW : RW Event counter 7 Slave way selection 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x05203944 FABRIC_MONITOR_SELECTION_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for event counter 7.

FABRIC_MONITOR_SELECTION_UPPER_REG7

Bits	Name	Description
15:0	E7MID	SW : RW Event counter 7 MID selection (If MID filtering enabled)

0x05203948 FABRIC_MONITOR_PICK_PORTS_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the main port and other port selection for the 8 event counters.

FABRIC_MONITOR_PICK_PORTS_REG

Bits	Name	Description
15:14	E7PP	SW : RW Event counter 7 port combination selection 0x0: Master port selected by E7MPS, filtering based on slave port disabled 0x1: Master port selected by E7MPS, filtering based on slave way selected by E7SWS 0x2: Slave way selected by E7SWS, filtering based on master port disabled 0x3: Slave way selected by E7SWS, filtering based on master port selected by E7MPS
13:12	E6PP	SW : RW Event counter 6 port combination selection 0x0: Master port selected by E6MPS, filtering based on slave port disabled 0x1: Master port selected by E6MPS, filtering based on slave way selected by E6SWS 0x2: Slave way selected by E6SWS, filtering based on master port disabled 0x3: Slave way selected by E6SWS, filtering based on master port selected by E6MPS
11:10	E5PP	SW : RW Event counter 5 port combination selection 0x0: Master port selected by E5MPS, filtering based on slave port disabled 0x1: Master port selected by E5MPS, filtering based on slave way selected by E5SWS 0x2: Slave way selected by E5SWS, filtering based on master port disabled 0x3: Slave way selected by E5SWS, filtering based on master port selected by E5MPS
9:8	E4PP	SW : RW Event counter 4 port combination selection 0x0: Master port selected by E4MPS, filtering based on slave port disabled 0x1: Master port selected by E4MPS, filtering based on slave way selected by E4SWS 0x2: Slave way selected by E4SWS, filtering based on master port disabled 0x3: Slave way selected by E4SWS, filtering based on master port selected by E4MPS

FABRIC_MONITOR_PICK_PORTS_REG (cont.)

Bits	Name	Description
7:6	E3PP	SW : RW Event counter 3 port combination selection 0x0: Master port selected by E3MPS, filtering based on slave port disabled 0x1: Master port selected by E3MPS, filtering based on slave way selected by E3SWS 0x2: Slave way selected by E3SWS, filtering based on master port disabled 0x3: Slave way selected by E3SWS, filtering based on master port selected by E3MPS
5:4	E2PP	SW : RW Event counter 2 port combination selection 0x0: Master port selected by E2MPS, filtering based on slave port disabled 0x1: Master port selected by E2MPS, filtering based on slave way selected by E2SWS 0x2: Slave way selected by E2SWS, filtering based on master port disabled 0x3: Slave way selected by E2SWS, filtering based on master port selected by E2MPS
3:2	E1PP	SW : RW Event counter 1 port combination selection 0x0: Master port selected by E1MPS, filtering based on slave port disabled 0x1: Master port selected by E1MPS, filtering based on slave way selected by E1SWS 0x2: Slave way selected by E1SWS, filtering based on master port disabled 0x3: Slave way selected by E1SWS, filtering based on master port selected by E1MPS
1:0	E0PP	SW : RW Event counter 0 port combination selection 0x0: Master port selected by E0MPS, filtering based on slave port disabled 0x1: Master port selected by E0MPS, filtering based on slave way selected by E0SWS 0x2: Slave way selected by E0SWS, filtering based on master port disabled 0x3: Slave way selected by E0SWS, filtering based on master port selected by E0MPS

0x05203950 FABRIC_MONITOR_CYCLE_COUNT_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the performance monitor cycle counter.

FABRIC_MONITOR_CYCLE_COUNT_UPPER_REG

Bits	Name	Description
15:0	UCC	SW : RW MSB cycle count value The cycle count value is decremented once per FABRIC clock. The counter stops decrementing once the CC value equals 32:h0.

0x05203954 FABRIC_MONITOR_CYCLE_COUNT_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the performance monitor cycle counter. If SW requires that the values when read do not change, when it reads this register, the value for all 32 bits of the cycle counter is stored. This allows for SW to read the lower reg and have the value match the exact cycle in which the upper reg was read.

FABRIC_MONITOR_CYCLE_COUNT_LOWER_REG

Bits	Name	Description
15:0	LCC	SW : RW LSB cycle count value The cycle count value is decremented once per FABRIC clock. The counter stops decrementing once the CC value equals 32:h0.

0x05203958 FABRIC_MONITOR_EVENT_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 0. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_LOWER_REG0

Bits	Name	Description
15:0	ECLT0	SW : RW Total # events (lower 16-bit value)

0x0520395C FABRIC_MONITOR_EVENT_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 0. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_UPPER_REG0

Bits	Name	Description
15:0	ECUT0	SW : RW Total # events (upper 16-bit value)

0x05203960 FABRIC_MONITOR_EVENT_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 1. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_LOWER_REG1

Bits	Name	Description
15:0	ECLT1	SW : RW Total # events (lower 16-bit value)

0x05203964 FABRIC_MONITOR_EVENT_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 1. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_UPPER_REG1

Bits	Name	Description
15:0	ECUT1	SW : RW Total # events (upper 16-bit value)

0x05203968 FABRIC_MONITOR_EVENT_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 2. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_LOWER_REG2

Bits	Name	Description
15:0	ECLT2	SW : RW Total # events (lower 16-bit value)

0x0520396C FABRIC_MONITOR_EVENT_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 2. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_UPPER_REG2

Bits	Name	Description
15:0	ECUT2	SW : RW Total # events (upper 16-bit value)

0x05203970 FABRIC_MONITOR_EVENT_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 3. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_LOWER_REG3

Bits	Name	Description
15:0	ECLT3	SW : RW Total # events (lower 16-bit value)

0x05203974 FABRIC_MONITOR_EVENT_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 3. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_UPPER_REG3

Bits	Name	Description
15:0	ECUT3	SW : RW Total # events (upper 16-bit value)

0x05203978 FABRIC_MONITOR_EVENT_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 4. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_LOWER_REG4

Bits	Name	Description
15:0	ECLT4	SW : RW Total # events (lower 16-bit value)

0x0520397C FABRIC_MONITOR_EVENT_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 4. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_UPPER_REG4

Bits	Name	Description
15:0	ECUT4	SW : RW Total # events (upper 16-bit value)

0x05203980 FABRIC_MONITOR_EVENT_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 5. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_LOWER_REG5

Bits	Name	Description
15:0	ECLT5	SW : RW Total # events (lower 16-bit value)

0x05203984 FABRIC_MONITOR_EVENT_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 5. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_UPPER_REG5

Bits	Name	Description
15:0	ECUT5	SW : RW Total # events (upper 16-bit value)

0x05203988 FABRIC_MONITOR_EVENT_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 6. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_LOWER_REG6

Bits	Name	Description
15:0	ECLT6	SW : RW Total # events (lower 16-bit value)

0x0520398C FABRIC_MONITOR_EVENT_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 6. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_UPPER_REG6

Bits	Name	Description
15:0	ECUT6	SW : RW Total # events (upper 16-bit value)

0x05203990 FABRIC_MONITOR_EVENT_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (lower 16-bits) for event counter 7. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_LOWER_REG7

Bits	Name	Description
15:0	ECLT7	SW : RW Total # events (lower 16-bit value)

0x05203994 FABRIC_MONITOR_EVENT_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of events (upper 16-bits) for event counter 7. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_UPPER_REG7

Bits	Name	Description
15:0	ECUT7	SW : RW Total # events (upper 16-bit value)

0x052039A4 FABRIC_TRIGGER_CONFIGURATION_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register configures the interface in which the trigger comparison is done on the address channel.

TAMS: Selects one of the 32 interfaces from which the address channel transfer qualifiers are used to enable trigger matching.

FABRIC_TRIGGER_CONFIGURATION_REG

Bits	Name	Description
15:7	RESERVED_BITS15_6	

FABRIC_TRIGGER_CONFIGURATION_REG (cont.)

Bits	Name	Description
6	TRGEN	SW : RW Trigger enable 1'b0 -disabled 0x1: enabled

FABRIC_TRIGGER_CONFIGURATION_REG (cont.)

Bits	Name	Description
5:0	TAMS	SW : RW Trigger based on address channel on M/S Port #: 0x0: Master Port 0 0x1: Master Port 1 0x2: Master Port 2 0x3: Master Port 3 0x4: Master Port 4 0x5: Master Port 5 0x6: Master Port 6 0x7: Master Port 7 0x8: Master Port 8 0x9: Master Port 9 0xA: Master Port 10 0xB: Master Port 11 0xC: Master Port 12 0xD: Master Port 13 0xE: Master Port 14 0xF: Master Port 15 0x10: Master Port 16 0x11: Master Port 17 0x12: Master Port 18 0x13: Master Port 19 0x14: Master Port 20 0x15: Master Port 21 0x16: Master Port 22 0x17: Master Port 23 0x18: Master Port 24 0x19: Master Port 25 0x1A: Master Port 26 0x1B: Master Port 27 0x1C: Master Port 28 0x1D: Master Port 29 0x1E: Master Port 30 0x1F: Master Port 31 0x20: Slave Port 0 0x21: Slave Port 1 0x22: Slave Port 2 0x23: Slave Port 3 0x24: Slave Port 4 0x25: Slave Port 5 0x26: Slave Port 6 0x27: Slave Port 7 0x28: Slave Port 8 0x29: Slave Port 9 0x2A: Slave Port 10 0x2B: Slave Port 11 0x2C: Slave Port 12

FABRIC_TRIGGER_CONFIGURATION_REG (cont.)

Bits	Name	Description
5:0	TAMS (CONT'D)	0x2D: Slave Port 13 0x2E: Slave Port 14 0x2F: Slave Port 15

0x052039AC FABRIC_TRIGGER_REG_0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the upper address which is used as comparison for the trigger feature of the on-chip trace or performance monitor function. TUADDR[15:0] will be compared against Address[31:16].

FABRIC_TRIGGER_REG_0

Bits	Name	Description
15:0	TUADDR	SW : RW Address bits[31:16]

0x052039B0 FABRIC_TRIGGER_REG_1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the lower address which is used as comparison for the trigger feature of the performance monitor function. TLADDR[15:0] will be compared against Address[15:0].

FABRIC_TRIGGER_REG_1

Bits	Name	Description
15:0	TLADDR	SW : RW Address bits[15:0]

0x052039B4 FABRIC_TRIGGER_REG_2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the lower address which is used as comparison for the trigger feature of the performance monitor function..

FABRIC_TRIGGER_REG_2

Bits	Name	Description
15:0	AMID	SW : RW AMID / HMID

0x052039B8 FABRIC_TRIGGER_REG_3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the address channel transfer qualifiers which are used as comparison for the trigger feature of the performance monitor function.

FABRIC_TRIGGER_REG_3

Bits	Name	Description
15:12	RESERVED_BITS15_12	
11	AOOOWR	SW : RW Out-of-order write
10	AOOORD	SW : RW Out-of-order read
9:3	ATID	SW : RW Address TID (If ATID is less than 7 bits, the upper bits must be set to 0)
2	AFULL	SW : RW Full Transfer
1	RESERVED_BIT1	
0	APROTNS	SW : RW Protection level

0x052039BC FABRIC_TRIGGER_REG_4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register defines the address channel transfer qualifiers which are used as comparison for the trigger feature of the performance monitor function.

FABRIC_TRIGGER_REG_4

Bits	Name	Description
15:12	ATYPE	SW : RW Memory type attributes
11:10	ALOCK	SW : RW Lock type
9	RESERVED_BITS9	
8	ABURST	SW : RW Burst type
7:5	ASIZE	Burst size
4:1	ALEN	Burst length
0	AWRITE	Burst direction

0x052039C0 FABRIC_TRIGGER_MASK_REG_0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR0.

FABRIC_TRIGGER_MASK_REG_0

Bits	Name	Description
15:0	FTTR0_MASK	SW : RW Bit mask field for FTTR0 Enable: 1 Disable: 0

0x052039C4 FABRIC_TRIGGER_MASK_REG_1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR1.

FABRIC_TRIGGER_MASK_REG_1

Bits	Name	Description
15:0	FTTR1_MASK	SW : RW Bit mask field for FTTR1 Enable: 1 Disable: 0

0x052039C8 FABRIC_TRIGGER_MASK_REG_2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR2.

FABRIC_TRIGGER_MASK_REG_2

Bits	Name	Description
15:0	FTTR2_MASK	SW : RW Bit mask field for FTTR2 Enable: 1 Disable: 0

0x052039CC FABRIC_TRIGGER_MASK_REG_3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR3.

FABRIC_TRIGGER_MASK_REG_3

Bits	Name	Description
15:0	FTTR3_MASK	SW : RW Bit mask field for FTTR3 Enable: 1 Disable: 0

0x052039D0 FABRIC_TRIGGER_MASK_REG_4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the mask field for FTTR4.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FTTR4.

FABRIC_TRIGGER_MASK_REG_4

Bits	Name	Description
15:0	FTTR4_MASK	SW : RW Bit mask field for FTTR4 Enable: 1 Disable: 0

0x052039D4 FABRIC_MONITOR_ADDRESS_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter0.

FABRIC_MONITOR_ADDRESS_LOWER_REG0

Bits	Name	Description
15:0	E0AL	SW : RW LSB address value Event counter 0 address selection (if address range filtering enabled)

0x052039D8 FABRIC_MONITOR_ADDRESS_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter0.

FABRIC_MONITOR_ADDRESS_UPPER_REG0

Bits	Name	Description
15:0	E0AU	SW : RW MSB address value Event counter 0 address selection (if address range filtering enabled)

0x052039DC FABRIC_MONITOR_ADDRESS_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter1.

FABRIC_MONITOR_ADDRESS_LOWER_REG1

Bits	Name	Description
15:0	E1AL	SW : RW LSB address value Event counter 1address selection (if address range filtering enabled)

0x052039E0 FABRIC_MONITOR_ADDRESS_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter1.

FABRIC_MONITOR_ADDRESS_UPPER_REG1

Bits	Name	Description
15:0	E1AU	SW : RW MSB address value Event counter 1address selection (if address range filtering enabled)

0x052039E4 FABRIC_MONITOR_ADDRESS_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter2

FABRIC_MONITOR_ADDRESS_LOWER_REG2

Bits	Name	Description
15:0	E2AL	SW : RW LSB address value Event counter 2 address selection (if address range filtering enabled)

0x052039E8 FABRIC_MONITOR_ADDRESS_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter2.

FABRIC_MONITOR_ADDRESS_UPPER_REG2

Bits	Name	Description
15:0	E2AU	SW : RW MSB address value Event counter 2 address selection (if address range filtering enabled)

0x052039EC FABRIC_MONITOR_ADDRESS_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter3

FABRIC_MONITOR_ADDRESS_LOWER_REG3

Bits	Name	Description
15:0	E3AL	SW : RW LSB address value Event counter 3 address selection (if address range filtering enabled)

0x052039F0 FABRIC_MONITOR_ADDRESS_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter3.

FABRIC_MONITOR_ADDRESS_UPPER_REG3

Bits	Name	Description
15:0	E3AU	SW : RW MSB address value Event counter 3 address selection (if address range filtering enabled)

0x052039F4 FABRIC_MONITOR_ADDRESS_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter4.

FABRIC_MONITOR_ADDRESS_LOWER_REG4

Bits	Name	Description
15:0	E4AL	SW : RW LSB address value Event counter 4 address selection (if address range filtering enabled)

0x052039F8 FABRIC_MONITOR_ADDRESS_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter4.

FABRIC_MONITOR_ADDRESS_UPPER_REG4

Bits	Name	Description
15:0	E4AU	SW : RW MSB address value Event counter 4address selection (if address range filtering enabled)

0x052039FC FABRIC_MONITOR_ADDRESS_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter5.

FABRIC_MONITOR_ADDRESS_LOWER_REG5

Bits	Name	Description
15:0	E5AL	SW : RW LSB address value Event counter 5 address selection (if address range filtering enabled)

0x05203A00 FABRIC_MONITOR_ADDRESS_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter4.

FABRIC_MONITOR_ADDRESS_UPPER_REG5

Bits	Name	Description
15:0	E5AU	SW : RW MSB address value Event counter 5 address selection (if address range filtering enabled)

0x05203A04 FABRIC_MONITOR_ADDRESS_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter 6.

FABRIC_MONITOR_ADDRESS_LOWER_REG6

Bits	Name	Description
15:0	E6AL	SW : RW LSB address value Event counter 6 address selection (if address range filtering enabled)

0x05203A08 FABRIC_MONITOR_ADDRESS_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 6.

FABRIC_MONITOR_ADDRESS_UPPER_REG6

Bits	Name	Description
15:0	E6AU	SW : RW MSB address value Event counter 6 address selection (if address range filtering enabled)

0x05203A0C FABRIC_MONITOR_ADDRESS_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address filter value for event counter 7.

FABRIC_MONITOR_ADDRESS_LOWER_REG7

Bits	Name	Description
15:0	E7AL	SW : RW LSB address value Event counter 7 address selection (if address range filtering enabled)

0x05203A10 FABRIC_MONITOR_ADDRESS_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 7.

FABRIC_MONITOR_ADDRESS_UPPER_REG7

Bits	Name	Description
15:0	E7AU	SW : RW MSB address value Event counter 7 address selection (if address range filtering enabled)

0x05203A14 FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR0.

FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG0

Bits	Name	Description
15:0	E0AML	SW : RW LSB address value Event counter 0 address mask

0x05203A18 FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 0.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR0.

FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG0

Bits	Name	Description
15:0	E0AMU	SW : RW MSB address value Event counter 0 address mask

0x05203A1C FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR1.

FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG1

Bits	Name	Description
15:0	E1AML	SW : RW LSB address value Event counter 1 address mask

0x05203A20 FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 1.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR1.

FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG1

Bits	Name	Description
15:0	E1AMU	SW : RW MSB address value Event counter address mask

0x05203A24 FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR2.

FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG2

Bits	Name	Description
15:0	E2AML	SW : RW LSB address value Event counter 2 address mask

0x05203A28 FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 2.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR2.

FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG2

Bits	Name	Description
15:0	E2AMU	SW : RW MSB address value Event counter 2 address mask

0x05203A2C FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR3.

FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG3

Bits	Name	Description
15:0	E3AML	SW : RW LSB address value Event counter 3 address mask

0x05203A30 FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 3.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR3.

FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG3

Bits	Name	Description
15:0	E3AMU	SW : RW MSB address value Event counter 3 address mask

0x05203A34 FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 4.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR4.

FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG4

Bits	Name	Description
15:0	E4AML	SW : RW LSB address value Event counter 4 address mask

0x05203A38 FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 4.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR4.

FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG4

Bits	Name	Description
15:0	E4AMU	SW : RW MSB address value Event counter 4 address mask

0x05203A3C FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 5.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR5.

FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG5

Bits	Name	Description
15:0	E5AML	SW : RW LSB address value Event counter 5 address mask

0x05203A40 FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 5.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR5.

FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG5

Bits	Name	Description
15:0	E5AMU	SW : RW MSB address value Event counter 5 address mask

0x05203A44 FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 6.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR6.

FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG6

Bits	Name	Description
15:0	E6AML	SW : RW LSB address value Event counter 6 address mask

0x05203A48 FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 6.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR6.

FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG6

Bits	Name	Description
15:0	E6AMU	SW : RW MSB address value Event counter 6 address mask

0x05203A4C FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for event counter 7.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPALR7.

FABRIC_MONITOR_ADDRESS_MASK_LOWER_REG7

Bits	Name	Description
15:0	E7AML	SW : RW LSB address value Event counter 7 address mask

0x05203A50 FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for event counter 7.

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPAUR7.

FABRIC_MONITOR_ADDRESS_MASK_UPPER_REG7

Bits	Name	Description
15:0	E7AMU	SW : RW MSB address value Event counter 7 address mask

0x05203A70 FABRIC_MONITOR_MID_MASK_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 0

FABRIC_MONITOR_MID_MASK_REG0

Bits	Name	Description
15:0	E0MM	SW : RW MID Mask value for event counter 0

0x05203A74 FABRIC_MONITOR_MID_MASK_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 1

FABRIC_MONITOR_MID_MASK_REG1

Bits	Name	Description
15:0	E1MM	SW : RW MID Mask value for event counter 1

0x05203A78 FABRIC_MONITOR_MID_MASK_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 2

FABRIC_MONITOR_MID_MASK_REG2

Bits	Name	Description
15:0	E2MM	SW : RW MID Mask value for event counter 2

0x05203A7C FABRIC_MONITOR_MID_MASK_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 3

FABRIC_MONITOR_MID_MASK_REG3

Bits	Name	Description
15:0	E3MM	SW : RW MID Mask value for event counter 3

0x05203A80 FABRIC_MONITOR_MID_MASK_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 4

FABRIC_MONITOR_MID_MASK_REG4

Bits	Name	Description
15:0	E4MM	SW : RW MID Mask value for event counter 4

0x05203A84 FABRIC_MONITOR_MID_MASK_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 15

FABRIC_MONITOR_MID_MASK_REG5

Bits	Name	Description
15:0	E5MM	SW : RW MID Mask value for event counter 5

0x05203A88 FABRIC_MONITOR_MID_MASK_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 6

FABRIC_MONITOR_MID_MASK_REG6

Bits	Name	Description
15:0	E6MM	SW : RW MID Mask value for event counter 6

0x05203A8C FABRIC_MONITOR_MID_MASK_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for event counter 7

FABRIC_MONITOR_MID_MASK_REG7

Bits	Name	Description
15:0	E7MM	SW : RW MID Mask value for event counter 7

0x05203AA0 FABRIC_MONITOR_EVENT_BEATS_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_LOWER_REG0

Bits	Name	Description
15:0	EBTL0	SW : RW Total # beats (lower 16-bit value)

0x05203AA4 FABRIC_MONITOR_EVENT_BEATS_MID_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_MID_REG0

Bits	Name	Description
15:0	EBTM0	SW : RW Total # beats (middle 16-bit value)

0x05203AA8 FABRIC_MONITOR_EVENT_BEATS_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_UPPER_REG0

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU0	SW : RW Total # beats (upper 4-bit value)

0x05203AAC FABRIC_MONITOR_EVENT_BEATS_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_LOWER_REG1

Bits	Name	Description
15:0	EBTL1	SW : RW Total # beats (lower 16-bit value)

0x05203AB0 FABRIC_MONITOR_EVENT_BEATS_MID_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_MID_REG1

Bits	Name	Description
15:0	EBTM1	SW : RW Total # beats (middle 16-bit value)

0x05203AB4 FABRIC_MONITOR_EVENT_BEATS_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_UPPER_REG1

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU1	SW : RW Total # beats (upper 4-bit value)

0x05203AB8 FABRIC_MONITOR_EVENT_BEATS_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_LOWER_REG2

Bits	Name	Description
15:0	EBTL2	SW : RW Total # beats (lower 16-bit value)

0x05203ABC FABRIC_MONITOR_EVENT_BEATS_MID_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_MID_REG2

Bits	Name	Description
15:0	EBTM2	SW : RW Total # beats (middle 16-bit value)

0x05203AC0 FABRIC_MONITOR_EVENT_BEATS_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_UPPER_REG2

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU2	SW : RW Total # beats (upper 4-bit value)

0x05203AC4 FABRIC_MONITOR_EVENT_BEATS_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_LOWER_REG3

Bits	Name	Description
15:0	EBTL3	SW : RW Total # beats (lower 16-bit value)

0x05203AC8 FABRIC_MONITOR_EVENT_BEATS_MID_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write

Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_MID_REG3

Bits	Name	Description
15:0	EBTM3	SW : RW Total # beats (middle 16-bit value)

0x05203ACC FABRIC_MONITOR_EVENT_BEATS_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_UPPER_REG3

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU3	SW : RW Total # beats (upper 4-bit value)

0x05203AD0 FABRIC_MONITOR_EVENT_BEATS_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_LOWER_REG4

Bits	Name	Description
15:0	EBTL4	SW : RW Total # beats (lower 16-bit value)

0x05203AD4 FABRIC_MONITOR_EVENT_BEATS_MID_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_MID_REG4

Bits	Name	Description
15:0	EBTM4	SW : RW Total # beats (middle 16-bit value)

0x05203AD8 FABRIC_MONITOR_EVENT_BEATS_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_UPPER_REG4

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU4	SW : RW Total # beats (upper 4-bit value)

0x05203ADC FABRIC_MONITOR_EVENT_BEATS_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write

Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_LOWER_REG5

Bits	Name	Description
15:0	EBTL5	SW : RW Total # beats (lower 16-bit value)

0x05203AE0 FABRIC_MONITOR_EVENT_BEATS_MID_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_MID_REG5

Bits	Name	Description
15:0	EBTM5	SW : RW Total # beats (middle 16-bit value)

0x05203AE4 FABRIC_MONITOR_EVENT_BEATS_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_UPPER_REG5

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU5	SW : RW Total # beats (upper 4-bit value)

0x05203AE8 FABRIC_MONITOR_EVENT_BEATS_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_LOWER_REG6

Bits	Name	Description
15:0	EBTL6	SW : RW Total # beats (lower 16-bit value)

0x05203AEC FABRIC_MONITOR_EVENT_BEATS_MID_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_MID_REG6

Bits	Name	Description
15:0	EBTM6	SW : RW Total # beats (middle 16-bit value)

0x05203AF0 FABRIC_MONITOR_EVENT_BEATS_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_UPPER_REG6

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU6	SW : RW Total # beats (upper 4-bit value)

0x05203AF4 FABRIC_MONITOR_EVENT_BEATS_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (lower 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_LOWER_REG7

Bits	Name	Description
15:0	EBTL7	SW : RW Total # beats (lower 16-bit value)

0x05203AF8 FABRIC_MONITOR_EVENT_BEATS_MID_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (mid 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events. Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_MID_REG7

Bits	Name	Description
15:0	EBTM7	SW : RW Total # beats (middle 16-bit value)

0x05203AFC FABRIC_MONITOR_EVENT_BEATS_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of beats (upper 4-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BEATS_UPPER_REG7

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3:0	EBTU7	SW : RW Total # beats (upper 4-bit value)

0x05203B00 FABRIC_MONITOR_EVENT_BYTES_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_LOWER_REG0

Bits	Name	Description
15:0	EBYL0	SW : RW Total bytes (lower 16-bit value)

0x05203B04 FABRIC_MONITOR_EVENT_BYTES_MID_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_MID_REG0

Bits	Name	Description
15:0	EBYM0	SW : RW Total bytes (middle 16-bit value)

0x05203B08 FABRIC_MONITOR_EVENT_BYTES_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 0. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_UPPER_REG0

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU0	SW : RW Total bytes (upper 11-bit value)

0x05203B0C FABRIC_MONITOR_EVENT_BYTES_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_LOWER_REG1

Bits	Name	Description
15:0	EBYL1	SW : RW Total bytes (lower 16-bit value)

0x05203B10 FABRIC_MONITOR_EVENT_BYTES_MID_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_MID_REG1

Bits	Name	Description
15:0	EBYM1	SW : RW Total bytes (middle 16-bit value)

0x05203B14 FABRIC_MONITOR_EVENT_BYTES_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 1. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_UPPER_REG1

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU1	SW : RW Total bytes (upper 11-bit value)

0x05203B18 FABRIC_MONITOR_EVENT_BYTES_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_LOWER_REG2

Bits	Name	Description
15:0	EBYL2	SW : RW Total bytes (lower 16-bit value)

0x05203B1C FABRIC_MONITOR_EVENT_BYTES_MID_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_MID_REG2

Bits	Name	Description
15:0	EBYM2	SW : RW Total bytes (middle 16-bit value)

0x05203B20 FABRIC_MONITOR_EVENT_BYTES_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 2. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_UPPER_REG2

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU2	SW : RW Total bytes (upper 11-bit value)

0x05203B24 FABRIC_MONITOR_EVENT_BYTES_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_LOWER_REG3

Bits	Name	Description
15:0	EBYL3	SW : RW Total bytes (lower 16-bit value)

0x05203B28 FABRIC_MONITOR_EVENT_BYTES_MID_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_MID_REG3

Bits	Name	Description
15:0	EBYM3	SW : RW Total bytes (middle 16-bit value)

0x05203B2C FABRIC_MONITOR_EVENT_BYTES_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 3. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_UPPER_REG3

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU3	SW : RW Total bytes (upper 11-bit value)

0x05203B30 FABRIC_MONITOR_EVENT_BYTES_LOWER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_LOWER_REG4

Bits	Name	Description
15:0	EBYL4	SW : RW Total bytes (lower 16-bit value)

0x05203B34 FABRIC_MONITOR_EVENT_BYTES_MID_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_MID_REG4

Bits	Name	Description
15:0	EBYM4	SW : RW Total bytes (middle 16-bit value)

0x05203B38 FABRIC_MONITOR_EVENT_BYTES_UPPER_REG4

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 4. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_UPPER_REG4

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU4	SW : RW Total bytes (upper 11-bit value)

0x05203B3C FABRIC_MONITOR_EVENT_BYTES_LOWER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_LOWER_REG5

Bits	Name	Description
15:0	EBYL5	SW : RW Total bytes (lower 16-bit value)

0x05203B40 FABRIC_MONITOR_EVENT_BYTES_MID_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_MID_REG5

Bits	Name	Description
15:0	EBYM5	SW : RW Total bytes (middle 16-bit value)

0x05203B44 FABRIC_MONITOR_EVENT_BYTES_UPPER_REG5

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 5. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_UPPER_REG5

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU5	SW : RW Total bytes (upper 11-bit value)

0x05203B48 FABRIC_MONITOR_EVENT_BYTES_LOWER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_LOWER_REG6

Bits	Name	Description
15:0	EBYL6	SW : RW Total bytes (lower 16-bit value)

0x05203B4C FABRIC_MONITOR_EVENT_BYTES_MID_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_MID_REG6

Bits	Name	Description
15:0	EBYM6	SW : RW Total bytes (middle 16-bit value)

0x05203B50 FABRIC_MONITOR_EVENT_BYTES_UPPER_REG6

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 6. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_UPPER_REG6

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU6	SW : RW Total bytes (upper 11-bit value)

0x05203B54 FABRIC_MONITOR_EVENT_BYTES_LOWER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (lower 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_LOWER_REG7

Bits	Name	Description
15:0	EBYL7	SW : RW Total bytes (lower 16-bit value)

0x05203B58 FABRIC_MONITOR_EVENT_BYTES_MID_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (mid 16-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_MID_REG7

Bits	Name	Description
15:0	EBYM7	SW : RW Total bytes (middle 16-bit value)

0x05203B5C FABRIC_MONITOR_EVENT_BYTES_UPPER_REG7

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the total number of bytes (upper 11-bits) associated with events for event counter 7. This value is valid only for Address Transfer Count event, Read Burst event and Write Burst events.

Note that although the register is writable, SW should not write this field. The field is made writable only for HW debug/verification.

FABRIC_MONITOR_EVENT_BYTES_UPPER_REG7

Bits	Name	Description
15:11	RESERVED_15_11	Reserved
10:0	EBYU7	SW : RW Total bytes (upper 11-bit value)

0x05203B60 FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 0.

FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0

Bits	Name	Description
15:14	T0SR	SW : RW Tenure selection for tenure counter 0 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T0MIDFEN	SW : RW Tenure counter 0 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T0INDFEN	SW : RW Tenure counter 0 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T0IND	SW : RW Tenure counter 0 Instruction/Data selection 0x0: Data 0x1: Instruction

FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
8:4	T0MP	SW : RW Tenure master port selection register for tenure counter 0 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG0 (cont.)

Bits	Name	Description
3:0	T0SW	SW : RW Tenure slave way selection register for tenure counter 0 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x05203B64 FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 0.

FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG0

Bits	Name	Description
15:0	T0MID	SW : RW Tenure counter 0 MID selection (If MID filtering enabled)

0x05203B68 FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 1.

FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1

Bits	Name	Description
15:14	T1SR	SW : RW Tenure selection for tenure counter 1 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T1MIDFEN	SW : RW Tenure counter 1MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T1INDFEN	SW : RW Tenure counter 1Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T1IND	SW : RW Tenure counter 1Instruction/Data selection 0x0: Data 0x1: Instruction

FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
8:4	T1MP	SW : RW Tenure master port selection register for tenure counter 1 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG1 (cont.)

Bits	Name	Description
3:0	T1SW	SW : RW Tenure slave way selection register for tenure counter 1 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x05203B6C FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 1.

FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG1

Bits	Name	Description
15:0	T1MID	SW : RW Tenure counter 1MID selection (If MID filtering enabled)

0x05203B70 FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 2.

FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2

Bits	Name	Description
15:14	T2SR	SW : RW Tenure selection for tenure counter 2 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T2MIDFEN	SW : RW Tenure counter 2 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T2INDFEN	SW : RW Tenure counter 2 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T2IND	SW : RW Tenure counter 2 Instruction/Data selection 0x0: Data 0x1: Instruction

FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
8:4	T2MP	SW : RW Tenure master port selection register for tenure counter 2 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG2 (cont.)

Bits	Name	Description
3:0	T2SW	SW : RW Tenure slave way selection register for tenure counter 2 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x05203B74 FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 2.

FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG2

Bits	Name	Description
15:0	T2MID	SW : RW Tenure counter 2 MID selection (If MID filtering enabled)

0x05203B78 FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the tenure selection, port selection and filtering criteria for the performance monitor tenure counter 3.

FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3

Bits	Name	Description
15:14	T3SR	SW : RW Tenure selection for tenure counter 3 0x0: Master addr hndshk interval 0x1: Slave addr hndshk interval 0x2: Bresp interval 0x3: Read data tenure
13:12	RESERVED_BITS_13_12	Reserved
11	T3MIDFEN	SW : RW Tenure counter 3 MID Filtering enable 0x0: Disabled 0x1: Enabled
10	T3INDFEN	SW : RW Tenure counter 3 Instruction/Data Filtering enable 0x0: Disabled 0x1: Enabled
9	T3IND	SW : RW Tenure counter 3 Instruction/Data selection 0x0: Data 0x1: Instruction

FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
8:4	T3MP	SW : RW Tenure master port selection register for tenure counter 3 0x0: Selects Master 0 0x1: Selects Master 1 0x2: Selects Master 2 0x3: Selects Master 3 0x4: Selects Master 4 0x5: Selects Master 5 0x6: Selects Master 6 0x7: Selects Master 7 0x8: Selects Master 8 0x9: Selects Master 9 0xA: Selects Master 10 0xB: Selects Master 11 0xC: Selects Master 12 0xD: Selects Master 13 0xE: Selects Master 14 0xF: Selects Master 15 0x10: Selects Master 16 0x11: Selects Master 17 0x12: Selects Master 18 0x13: Selects Master 19 0x14: Selects Master 20 0x15: Selects Master 21 0x16: Selects Master 22 0x17: Selects Master 23 0x18: Selects Master 24 0x19: Selects Master 25 0x1A: Selects Master 26 0x1B: Selects Master 27 0x1C: Selects Master 28 0x1D: Selects Master 29 0x1E: Selects Master 30 0x1F: Selects Master 31

FABRIC_MONITOR_TENURE_SELECTION_LOWER_REG3 (cont.)

Bits	Name	Description
3:0	T3SW	SW : RW Tenure slave way selection register for tenure counter 3 0x0: Selects Slave 0 0x1: Selects Slave 1 0x2: Selects Slave 2 0x3: Selects Slave 3 0x4: Selects Slave 4 0x5: Selects Slave 5 0x6: Selects Slave 6 0x7: Selects Slave 7 0x8: Selects Slave 8 0x9: Selects Slave 9 0xA: Selects Slave 10 0xB: Selects Slave 11 0xC: Selects Slave 12 0xD: Selects Slave 13 0xE: Selects Slave 14 0xF: Selects Slave 15

0x05203B7C FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the MID selection for tenure counter 3.

FABRIC_MONITOR_TENURE_SELECTION_UPPER_REG3

Bits	Name	Description
15:0	T3MID	SW : RW Tenure counter 3 MID selection (If MID filtering enabled)

0x05203B80 FABRIC_MONITOR_MIN_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x01FF

This register contains the minimum value of the tenure that is selected using FPTSLR0 and measured in tenure counter 0.

NOTE The reset value for this register is set to 0x01FF, equivalent to 8191 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at 0x01FF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

FABRIC_MONITOR_MIN_REG0

Bits	Name	Description
15:0	MIN0	SW : R Minimum value of tenure, in tenure counter 0

0x05203B84 FABRIC_MONITOR_MIN_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x01FF

This register contains the minimum value of the tenure that is selected using FPTSLR1 and measured in tenure counter 1.

NOTE The reset value for this register is set to 0x01FF, equivalent to 8191 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at 0x01FF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

FABRIC_MONITOR_MIN_REG1

Bits	Name	Description
15:0	MIN1	SW : R Minimum value of tenure, in tenure counter 1

0x05203B88 FABRIC_MONITOR_MIN_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x01FF

This register contains the minimum value of the tenure that is selected using FPTSLR2 and measured in tenure counter 2.

NOTE The reset value for this register is set to 0x01FF, equivalent to 8191 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at 0x01FF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

FABRIC_MONITOR_MIN_REG2

Bits	Name	Description
15:0	MIN2	SW : R Minimum value of tenure, in tenure counter 2

0x05203B8C FABRIC_MONITOR_MIN_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x01FF

This register contains the minimum value of the tenure that is selected using FPTSLR3 and measured in tenure counter 3.

NOTE The reset value for this register is set to 0x01FF, equivalent to 8191 clock cycles (which is the maximum tenure value that can be captured by the performance monitor). The value is used as an initial comparison against the captured tenure. If the value of this register remains at 0x01FF after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

The tenure values cannot be relied on to be accurate if an overflow condition occurs.

FABRIC_MONITOR_MIN_REG3

Bits	Name	Description
15:0	MIN3	SW : R Minimum value of tenure, in tenure counter 3

0x05203B90 FABRIC_MONITOR_MAX_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR0 and measured in tenure counter 0.

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

FABRIC_MONITOR_MAX_REG0

Bits	Name	Description
15:0	MAX0	SW : R Maximum value of tenure, in tenure counter 0

0x05203B94 FABRIC_MONITOR_MAX_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR1and measured in tenure counter 1

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

FABRIC_MONITOR_MAX_REG1

Bits	Name	Description
15:0	MAX1	SW : R Maximum value of tenure, in tenure counter 1

0x05203B98 FABRIC_MONITOR_MAX_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR2 and measured in tenure counter 2

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

FABRIC_MONITOR_MAX_REG2

Bits	Name	Description
15:0	MAX2	SW : R Maximum value of tenure, in tenure counter 2

0x05203B9C FABRIC_MONITOR_MAX_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the maximum value of the tenure that is selected using FPTSLR3 and measured in tenure counter 3

NOTE The reset value for this register is set to h'0000, equivalent to 0 clock cycles.The value is used as an initial comparison against the captured tenure. If the value of this register remains at h'0000 after the performance monitor has been set-up and tenure measurements have been completed, it indicates that no tenures have occurred.

If an overflow condition occurs, the tenure values cannot be relied on to be accurate.

The maximum tenure value can only be 'hFFFF.

FABRIC_MONITOR_MAX_REG3

Bits	Name	Description
15:0	MAX3	SW : R Maximum value of tenure, in tenure counter 3

0x05203BA0 FABRIC_MONITOR_TENURE_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 0

FABRIC_MONITOR_TENURE_LOWER_REG0

Bits	Name	Description
15:0	LTOT0	SW : RW LSB total value of tenure, in tenure counter 0

0x05203BA4 FABRIC_MONITOR_TENURE_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 0.

FABRIC_MONITOR_TENURE_UPPER_REG0

Bits	Name	Description
15:0	UTOT0	SW : RW MSB total value of tenure, in tenure counter 0

0x05203BA8 FABRIC_MONITOR_TENURE_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 1

FABRIC_MONITOR_TENURE_LOWER_REG1

Bits	Name	Description
15:0	LTOT1	SW : RW LSB total value of tenure, in tenure counter 1

0x05203BAC FABRIC_MONITOR_TENURE_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 1.

FABRIC_MONITOR_TENURE_UPPER_REG1

Bits	Name	Description
15:0	UTOT1	SW : RW MSB total value of tenure, in tenure counter 1

0x05203BB0 FABRIC_MONITOR_TENURE_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 2

FABRIC_MONITOR_TENURE_LOWER_REG2

Bits	Name	Description
15:0	LTOT2	SW : RW LSB total value of tenure, in tenure counter 2

0x05203BB4 FABRIC_MONITOR_TENURE_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 2.

FABRIC_MONITOR_TENURE_UPPER_REG2

Bits	Name	Description
15:0	UTOT2	SW : RW MSB total value of tenure, in tenure counter 2

0x05203BB8 FABRIC_MONITOR_TENURE_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure in tenure counter 3

FABRIC_MONITOR_TENURE_LOWER_REG3

Bits	Name	Description
15:0	LTOT3	SW : RW LSB total value of tenure, in tenure counter 3

0x05203BBC FABRIC_MONITOR_TENURE_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure in tenure counter 3.

FABRIC_MONITOR_TENURE_UPPER_REG3

Bits	Name	Description
15:0	UTOT3	SW : RW MSB total value of tenure, in tenure counter 3

0x05203BC0 FABRIC_MONITOR_LAST_TENURE_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 0

FABRIC_MONITOR_LAST_TENURE_REG0

Bits	Name	Description
15:0	LASTT0	SW : R Last tenure value in tenure counter 0

0x05203BC4 FABRIC_MONITOR_LAST_TENURE_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 1

FABRIC_MONITOR_LAST_TENURE_REG1

Bits	Name	Description
15:0	LASTT1	SW : R Last tenure value in tenure counter 1

0x05203BC8 FABRIC_MONITOR_LAST_TENURE_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 2

FABRIC_MONITOR_LAST_TENURE_REG2

Bits	Name	Description
15:0	LASTT2	SW : R Last tenure value in tenure counter 2

0x05203BCC FABRIC_MONITOR_LAST_TENURE_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the value of the last tenure in tenure counter 3

FABRIC_MONITOR_LAST_TENURE_REG3

Bits	Name	Description
15:0	LASTT0	SW : R Last tenure value in tenure counter 3

0x05203BD0 FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 0.

FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG0

Bits	Name	Description
15:0	T0AL	SW : RW LSB address value Tenure counter 0 address mask

0x05203BD4 FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 0.

FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG0

Bits	Name	Description
15:0	T0AU	SW : RW MSB address value Tenure counter 0 address mask

0x05203BD8 FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 1.

FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG1

Bits	Name	Description
15:0	T1AL	SW : RW LSB address value Tenure counter 1 address mask

0x05203BDC FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 1.

FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG1

Bits	Name	Description
15:0	T1AU	SW : RW MSB address value Tenure counter 1 address mask

0x05203BE0 FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 2.

FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG2

Bits	Name	Description
15:0	T2AL	SW : RW LSB address value Tenure counter 2 address mask

0x05203BE4 FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 2.

FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG2

Bits	Name	Description
15:0	T2AU	SW : RW MSB address value Tenure counter 2 address mask

0x05203BE8 FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 3.

FABRIC_MONITOR_TENURE_ADDRESS_LOWER_REG3

Bits	Name	Description
15:0	T3AL	SW : RW LSB address value Tenure counter 3 address mask

0x05203BEC FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address filter value for tenure counter 3.

FABRIC_MONITOR_TENURE_ADDRESS_UPPER_REG3

Bits	Name	Description
15:0	T3AU	SW : RW MSB address value Tenure counter 3 address mask

0x05203BF0 FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 0

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR0.

FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG0

Bits	Name	Description
15:0	T0AML	SW : RW LSB address value Tenure counter 0 address mask

0x05203BF4 FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 0

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR0.

FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG0

Bits	Name	Description
15:0	T0AMU	SW : RW MSB address mask value Tenure counter 0 address mask

0x05203BF8 FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 1

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR1.

FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG1

Bits	Name	Description
15:0	T1AML	SW : RW LSB address value Tenure counter 1 address mask

0x05203BFC FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 1

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR1.

FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG1

Bits	Name	Description
15:0	T1AMU	SW : RW MSB address mask value Tenure counter 1 address mask

0x05203C00 FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 2

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR2.

FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG2

Bits	Name	Description
15:0	T2AML	SW : RW LSB address value Tenure counter 2 address mask

0x05203C04 FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 2

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR2.

FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG2

Bits	Name	Description
15:0	T2AMU	SW : RW MSB address mask value Tenure counter 2 address mask

0x05203C08 FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the address mask value for tenure counter 3

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTALR3.

FABRIC_MONITOR_TENURE_ADDRESS_MASK_LOWER_REG3

Bits	Name	Description
15:0	T3AML	SW : RW LSB address value Tenure counter 3 address mask

0x05203C0C FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the address mask value for tenure counter 3

Setting a mask bit to 1'b1 indicates that the selected field is not matched against the corresponding bit in FPTAUR3.

FABRIC_MONITOR_TENURE_ADDRESS_MASK_UPPER_REG3

Bits	Name	Description
15:0	T3AMU	SW : RW MSB address mask value Tenure counter 3 address mask

0x05203C10 FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 0 that were longer than the specified threshold for tenure counter 0

FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG0

Bits	Name	Description
15:0	T0ATCL	SW : R LSB count value

0x05203C14 FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 0 that were longer than the specified threshold for tenure counter 0

FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG0

Bits	Name	Description
15:0	T0ATCU	SW : R MSB count value

0x05203C18 FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 1 that were longer than the specified threshold for tenure counter 1

FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG1

Bits	Name	Description
15:0	T1ATCL	SW : R LSB count value

0x05203C1C FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 1 that were longer than the specified threshold for tenure counter 1

FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG1

Bits	Name	Description
15:0	T1ATCU	SW : R MSB count value

0x05203C20 FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 2 that were longer than the specified threshold for tenure counter 2

FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG2

Bits	Name	Description
15:0	T2ATCL	SW : R LSB count value

0x05203C24 FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 2 that were longer than the specified threshold for tenure counter 2

FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG2

Bits	Name	Description
15:0	T2ATCU	SW : R MSB count value

0x05203C28 FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the count of tenures measures in tenure counter 3 that were longer than the specified threshold for tenure counter 3

FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_LOWER_REG3

Bits	Name	Description
15:0	T3ATCL	SW : R LSB count value

0x05203C2C FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the count of tenures measured in tenure counter 3 that were longer than the specified threshold for tenure counter 3

FABRIC_MONITOR_TENURE_ABOVE_THRESHOLD_COUNT_UPPER_REG3

Bits	Name	Description
15:0	T3ATCU	SW : R MSB count value

0x05203C30 FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 0 are measured.

FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG0

Bits	Name	Description
12:0	T0TV	SW : RW Tenure counter 0 threshold value

0x05203C34 FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 1 are measured.

FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG1

Bits	Name	Description
12:0	T1TV	SW : RW Tenure counter 1 threshold value

0x05203C38 FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 2 are measured.

FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG2

Bits	Name	Description
12:0	T2TV	SW : RW Tenure counter 2 threshold value

0x05203C3C FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the threshold against which all tenure values in tenure counter 3 are measured.

FABRIC_MONITOR_TENURE_THRESHOLD_VALUE_REG3

Bits	Name	Description
12:0	T3TV	SW : RW Tenure counter 3 threshold value

0x05203C40 FABRIC_MONITOR_TENURE_MID_MASK_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 0

FABRIC_MONITOR_TENURE_MID_MASK_REG0

Bits	Name	Description
15:0	T0MM	SW : RW MID Mask value

0x05203C44 FABRIC_MONITOR_TENURE_MID_MASK_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 1

FABRIC_MONITOR_TENURE_MID_MASK_REG1

Bits	Name	Description
15:0	T1MM	SW : RW MID Mask value

0x05203C48 FABRIC_MONITOR_TENURE_MID_MASK_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 2

FABRIC_MONITOR_TENURE_MID_MASK_REG2

Bits	Name	Description
15:0	T2MM	SW : RW MID Mask value

0x05203C4C FABRIC_MONITOR_TENURE_MID_MASK_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains MID mask value for tenure counter 3

FABRIC_MONITOR_TENURE_MID_MASK_REG3

Bits	Name	Description
15:0	T3MM	SW : RW MID Mask value

0x05203C50 FABRIC_MONITOR_TENURE_COUNT_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure0 register.

FABRIC_MONITOR_TENURE_COUNT_LOWER_REG0

Bits	Name	Description
15:0	TLC0	SW : R LSB count value Incremented every time a tenure under observation completes in tenure counter 0

0x05203C54 FABRIC_MONITOR_TENURE_COUNT_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure0 register.

FABRIC_MONITOR_TENURE_COUNT_UPPER_REG0

Bits	Name	Description
15:0	TUC0	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 0

0x05203C58 FABRIC_MONITOR_TENURE_COUNT_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure1 register.

FABRIC_MONITOR_TENURE_COUNT_LOWER_REG1

Bits	Name	Description

0x05203C5C FABRIC_MONITOR_TENURE_COUNT_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure1 register.

FABRIC_MONITOR_TENURE_COUNT_UPPER_REG1

Bits	Name	Description
15:0	TUC1	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 1

0x05203C60 FABRIC_MONITOR_TENURE_COUNT_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure2 register.

FABRIC_MONITOR_TENURE_COUNT_LOWER_REG2

Bits	Name	Description
15:0	TLC2	SW : R LSB count value Incremented every time a tenure under observation completes in tenure counter 2

0x05203C64 FABRIC_MONITOR_TENURE_COUNT_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure2 register.

FABRIC_MONITOR_TENURE_COUNT_UPPER_REG2

Bits	Name	Description
15:0	TUC2	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 2

0x05203C68 FABRIC_MONITOR_TENURE_COUNT_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenure updations to total_tenure3 register.

FABRIC_MONITOR_TENURE_COUNT_LOWER_REG3

Bits	Name	Description
15:0	TLC3	SW : R LSB count value Incremented every time a tenure under observation completes in tenure counter 3

0x05203C6C FABRIC_MONITOR_TENURE_COUNT_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenure updations to total_tenure3 register.

FABRIC_MONITOR_TENURE_COUNT_UPPER_REG3

Bits	Name	Description
15:0	TUC3	SW : R MSB count value TUC,TLC value incremented every time a tenure under observation completes in tenure counter 3

0x05203C70 FABRIC_MONITOR_TENURE_PICK_PORTS_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the main port and other port selection for the 4 event counters.

FABRIC_MONITOR_TENURE_PICK_PORTS_REG

Bits	Name	Description
15:4	RESERVED_15_4	Reserved
3	T3PP	SW : RW Tenure counter 3 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T3MP or T3SW
2	T2PP	SW : RW Tenure counter 2 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T2MP or T2SW
1	T1PP	SW : RW Tenure counter 1 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T1MP or T1SW
0	T0PP	SW : RW Tenure counter 0 port combination selection 0x0: Filtering based on other port disabled 0x1: Filtering based on other port selected by T0MP or T0SW

0x05203C80 FABRIC_MONITOR_TENURE_UNION_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 0

FABRIC_MONITOR_TENURE_UNION_LOWER_REG0

Bits	Name	Description
15:0	LTOTU0	SW : RW LSB total union value of tenure, in tenure counter 0

0x05203C84 FABRIC_MONITOR_TENURE_UNION_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 0.

FABRIC_MONITOR_TENURE_UNION_UPPER_REG0

Bits	Name	Description
15:0	UTOTU0	SW : RW MSB total union value of tenure, in tenure counter 0

0x05203C88 FABRIC_MONITOR_TENURE_UNION_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 1

FABRIC_MONITOR_TENURE_UNION_LOWER_REG1

Bits	Name	Description
15:0	LTOTU1	SW : RW LSB total union value of tenure, in tenure counter 1

0x05203C8C FABRIC_MONITOR_TENURE_UNION_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 1.

FABRIC_MONITOR_TENURE_UNION_UPPER_REG1

Bits	Name	Description
15:0	UTOTU1	SW : RW MSB total union value of tenure, in tenure counter 1

0x05203C90 FABRIC_MONITOR_TENURE_UNION_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 2

FABRIC_MONITOR_TENURE_UNION_LOWER_REG2

Bits	Name	Description
15:0	LTOTU2	SW : RW LSB total union value of tenure, in tenure counter 2

0x05203C94 FABRIC_MONITOR_TENURE_UNION_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 2.

FABRIC_MONITOR_TENURE_UNION_UPPER_REG2

Bits	Name	Description
15:0	UTOTU2	SW : RW MSB total union value of tenure, in tenure counter 2

0x05203C98 FABRIC_MONITOR_TENURE_UNION_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total tenure (considering pipelining) in tenure counter 3

FABRIC_MONITOR_TENURE_UNION_LOWER_REG3

Bits	Name	Description
15:0	LTOTU3	SW : RW LSB total union value of tenure, in tenure counter 3

0x05203C9C FABRIC_MONITOR_TENURE_UNION_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total tenure (considering pipelining) in tenure counter 3.

FABRIC_MONITOR_TENURE_UNION_UPPER_REG3

Bits	Name	Description
15:0	UTOTU3	SW : RW MSB total union value of tenure, in tenure counter 3

0x05203CA0 FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 0, that were pipelined.

FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG0

Bits	Name	Description

0x05203CA4 FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 0, that were pipelined.

FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG0

Bits	Name	Description
15:0	TUCP0	SW : R MSB count value TUCP0,TLCP0 value incremented every time a pipelined tenure completes in tenure counter 0

0x05203CA8 FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 1, that were pipelined.

FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG1

Bits	Name	Description

0x05203CAC FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 1, that were pipelined.

FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG1

Bits	Name	Description
15:0	TUCP1	SW : R MSB count value TUCP1,TLCP1 value incremented every time a pipelined tenure completes in tenure counter 1

0x05203CB0 FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 2, that were pipelined.

FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG2

Bits	Name	Description

0x05203CB4 FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 2, that were pipelined.

FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG2

Bits	Name	Description
15:0	TUCP2	SW : R MSB count value TUCP1,TLCP1 value incremented every time a pipelined tenure completes in tenure counter 2

0x05203CB8 FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures measured in tenure counter 3, that were pipelined.

FABRIC_MONITOR_TENURE_COUNT_PIPELINED_LOWER_REG3

Bits	Name	Description

0x05203CBC FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures measured in tenure counter 3, that were pipelined.

FABRIC_MONITOR_TENURE_COUNT_PIPELINED_UPPER_REG3

Bits	Name	Description
15:0	TUCP3	SW : R MSB count value TUCP3,TLCP3 value incremented every time a pipelined tenure completes in tenure counter 3

0x05203CC0 FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the max number of tenures pipelined at any point during the monitoring window for tenure counter 0

FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG0

Bits	Name	Description
15:0	TMCP0	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 0

0x05203CC4 FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the max number of tenures pipelined at any point during the monitoring window for tenure counter 1

FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG1

Bits	Name	Description
15:0	TMCP1	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 1

0x05203CC8 FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the max number of tenures pipelined at any point during the monitoring window for tenure counter 2

FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG2

Bits	Name	Description
15:0	TMCP2	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 2

0x05203CCC FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains the max number of tenures pipelined at any point during the monitoring window for tenure counter 3

FABRIC_MONITOR_TENURE_MAX_COUNT_PIPELINED_REG3

Bits	Name	Description
15:0	TMCP3	SW : R This is the maximum number of tenures pipelined at the same time in tenure counter 3

0x05203CD0 FABRIC_MONITOR_INFLIGHT_TENURE_CORRECTION_MODE_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register controls the facility to correlate a particular event counter to a tenure counter. When the tenure results of a counter are reset during a monitoring window (to account for errors due to starting the monitor in the middle of traffic), the event counters too get reset if the correlation between them is enabled.

NOTE PCORR bit (bit 0) should not be set for APQ8064.

FABRIC_MONITOR_INFLIGHT_TENURE_CORRECTION_MODE_REG

Bits	Name	Description
15:9	RESERVED_15_9	Reserved Bits
8	EC7COR	SW : RW 0x1: Link Event Counter 7 to Tenure Counter 3 0x0: Event Counter 7 is independent
7	EC6COR	SW : RW 0x1: Link Event Counter 6 to Tenure Counter 2 0x0: Event Counter 6 is independent
6	EC5COR	SW : RW 0x1: Link Event Counter 5 to Tenure Counter 1 0x0: Event Counter 5 is independent
5	EC4COR	SW : RW 0x1: Link Event Counter 4 to Tenure Counter 0 0x0: Event Counter 4 is independent
4	EC3COR	SW : RW 0x1: Link Event Counter 3 to Tenure Counter 3 0x0: Event Counter 3 is independent
3	EC2COR	SW : RW 0x1: Link Event Counter 2 to Tenure Counter 2 0x0: Event Counter 2 is independent
2	EC1COR	SW : RW 0x1: Link Event Counter 1 to Tenure Counter 1 0x0: Event Counter 1 is independent
1	EC0COR	SW : RW 0x1: Link Event Counter 0 to Tenure Counter 0 0x0: Event Counter 0 is independent
0	PCORR	SW : RW This is the enable for tenure correction mode This bit SHOULD NOT be set for APQ8064.

0x05203CE0 FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures counted by tenure counter 0 that correspond to out-of-order transactions.

FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG0

Bits	Name	Description
15:0	TOLC0	SW : R LSB count value Incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 0

0x05203CE4 FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG0

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures counted by tenure counter 0 that correspond to out-of-order transactions

FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG0

Bits	Name	Description
15:0	TOUC0	SW : R MSB count value TOUC,TOLC value incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 0

0x05203CE8 FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures counted by tenure counter 1 that correspond to out-of-order transactions.

FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG1

Bits	Name	Description
15:0	TOLC1	SW : R LSB count value Incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 1

0x05203CEC FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG1

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures counted by tenure counter 1 that correspond to out-of-order transactions

FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG1

Bits	Name	Description
15:0	TOUC1	SW : R MSB count value TOUC,TOLC value incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 1

0x05203CF0 FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures counted by tenure counter 2 that correspond to out-of-order transactions.

FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG2

Bits	Name	Description
15:0	TOLC2	SW : R LSB count value Incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 2

0x05203CF4 FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG2

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures counted by tenure counter 2 that correspond to out-of-order transactions

FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG2

Bits	Name	Description
15:0	TOUC2	SW : R MSB count value TOUC,TOLC value incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 2

0x05203CF8 FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the total count of tenures counted by tenure counter 3 that correspond to out-of-order transactions.

FABRIC_MONITOR_TENURE_COUNT_OOO_LOWER_REG3

Bits	Name	Description
15:0	TOLC3	SW : R LSB count value Incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 3

0x05203CFC FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG3

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the total count of tenures counted by tenure counter 3 that correspond to out-of-order transactions

FABRIC_MONITOR_TENURE_COUNT_OOO_UPPER_REG3

Bits	Name	Description
15:0	TOUC3	SW : R MSB count value TOUC,TOLC value incremented every time a tenure (of an out of order transaction) under observation completes in tenure counter 3

0x05203D00 FABRIC_MONITOR_RTR_STATUS_REG

Type: Read
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains 4 status bits (one for each performance monitor tenure counter). Each bit indicates whether the monitoring results pertaining to the associated tenure counter have been reset (to account for errors due to starting the monitor in the middle of traffic) or not.

FABRIC_MONITOR_RTR_STATUS_REG

Bits	Name	Description
15:4	RESERVED15_4	Reserved
3	TC3_RESET	SW: R When set, this bit indicates that tenure counter 3 results have been reset by the design during the monitoring window, to account for errors due to starting the monitor in the middle of traffic
2	TC2_RESET	SW: R When set, this bit indicates that tenure counter 2 results have been reset by the design during the monitoring window, to account for errors due to starting the monitor in the middle of traffic
1	TC1_RESET	SW: R When set, this bit indicates that tenure counter 1 results have been reset by the design during the monitoring window, to account for errors due to starting the monitor in the middle of traffic
0	TC0_RESET	SW: R When set, this bit indicates that tenure counter 0 results have been reset by the design during the monitoring window, to account for errors due to starting the monitor in the middle of traffic

0x05203D04 FABRIC_MONITOR_IDLE_INTERNAL_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 0 to Master 15). A value of 1 indicates that the internally generated idle status is to be used to determine when to reset the performance monitor tenure counter results (resetting the tenure counter results is needed to compensate for errors due to enabling the tenure counters in the middle of traffic). A value of 0 will indicate that the primary idle input is to be used instead.

NOTE These settings will have an effect only in case of AXI master ports.

FABRIC_MONITOR_IDLE_INTERNAL_LOWER_REG

Bits	Name	Description
15	M15_PII	SW : RW 0x1: The internally generated idle status for Master 15 will be used by the performance monitor 0x0: Primary input I_AXI_M15_IDLE is used by the performance monitor
14	M14_PII	SW : RW 0x1: The internally generated idle status for Master 14 will be used by the performance monitor 0x0: Primary input I_AXI_M14_IDLE is used by the performance monitor
13	M13_PII	SW : RW 0x1: The internally generated idle status for Master 13 will be used by the performance monitor 0x0: Primary input I_AXI_M13_IDLE is used by the performance monitor
12	M12_PII	SW : RW 0x1: The internally generated idle status for Master 12 will be used by the performance monitor 0x0: Primary input I_AXI_M12_IDLE is used by the performance monitor
11	M11_PII	SW : RW 0x1: The internally generated idle status for Master 11 will be used by the performance monitor 0x0: Primary input I_AXI_M11_IDLE is used by the performance monitor
10	M10_PII	SW : RW 0x1: The internally generated idle status for Master 10 will be used by the performance monitor 0x0: Primary input I_AXI_M10_IDLE is used by the performance monitor
9	M9_PII	SW : RW 0x1: The internally generated idle status for Master 9 will be used by the performance monitor 0x0: Primary input I_AXI_M9_IDLE is used by the performance monitor

FABRIC_MONITOR_IDLE_INTERNAL_LOWER_REG (cont.)

Bits	Name	Description
8	M8_PII	SW : RW 0x1: The internally generated idle status for Master 8 will be used by the performance monitor 0x0: Primary input I_AXI_M8_IDLE is used by the performance monitor
7	M7_PII	SW : RW 0x1: The internally generated idle status for Master 7 will be used by the performance monitor 0x0: Primary input I_AXI_M7_IDLE is used by the performance monitor
6	M6_PII	SW : RW 0x1: The internally generated idle status for Master 6 will be used by the performance monitor 0x0: Primary input I_AXI_M6_IDLE is used by the performance monitor
5	M5_PII	SW : RW 0x1: The internally generated idle status for Master 5 will be used by the performance monitor 0x0: Primary input I_AXI_M5_IDLE is used by the performance monitor
4	M4_PII	SW : RW 0x1: The internally generated idle status for Master 4 will be used by the performance monitor 0x0: Primary input I_AXI_M4_IDLE is used by the performance monitor
3	M3_PII	SW : RW 0x1: The internally generated idle status for Master 3 will be used by the performance monitor 0x0: Primary input I_AXI_M3_IDLE is used by the performance monitor
2	M2_PII	SW : RW 0x1: The internally generated idle status for Master 2 will be used by the performance monitor 0x0: Primary input I_AXI_M2_IDLE is used by the performance monitor
1	M1_PII	SW : RW 0x1: The internally generated idle status for Master 1 will be used by the performance monitor 0x0: Primary input I_AXI_M1_IDLE is used by the performance monitor
0	M0_PII	SW : RW 0x1: The internally generated idle status for Master 0 will be used by the performance monitor 0x0: Primary input I_AXI_M0_IDLE is used by the performance monitor

0x05203D08 FABRIC_MONITOR_IDLE_INTERNAL_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 16 to Master 31). A value of 1 indicates that the internally generated idle status is to be used to determine when to reset the performance monitor tenure counter results (resetting the tenure counter results is needed to compensate for errors due to enabling the tenure counters in the middle of traffic). A value of 0 will indicate that the primary idle input is to be used instead.

NOTE These settings will have an effect only in case of AXI master ports.

FABRIC_MONITOR_IDLE_INTERNAL_UPPER_REG

Bits	Name	Description
31	M31_PII	SW : RW 0x1: The internally generated idle status for Master 31 will be used by the performance monitor 0x0: Primary input I_AXI_M31_IDLE is used by the performance monitor
30	M30_PII	SW : RW 0x1: The internally generated idle status for Master 30 will be used by the performance monitor 0x0: Primary input I_AXI_M30_IDLE is used by the performance monitor
29	M29_PII	SW : RW 0x1: The internally generated idle status for Master 29 will be used by the performance monitor 0x0: Primary input I_AXI_M29_IDLE is used by the performance monitor
28	M28_PII	SW : RW 0x1: The internally generated idle status for Master 28 will be used by the performance monitor 0x0: Primary input I_AXI_M28_IDLE is used by the performance monitor
27	M27_PII	SW : RW 0x1: The internally generated idle status for Master 27 will be used by the performance monitor 0x0: Primary input I_AXI_M27_IDLE is used by the performance monitor
26	M26_PII	SW : RW 0x1: The internally generated idle status for Master 26 will be used by the performance monitor 0x0: Primary input I_AXI_M26_IDLE is used by the performance monitor

FABRIC_MONITOR_IDLE_INTERNAL_UPPER_REG (cont.)

Bits	Name	Description
25	M25_PII	SW : RW 0x1: The internally generated idle status for Master 25 will be used by the performance monitor 0x0: Primary input I_AXI_M25_IDLE is used by the performance monitor
24	M24_PII	SW : RW 0x1: The internally generated idle status for Master 24 will be used by the performance monitor 0x0: Primary input I_AXI_M24_IDLE is used by the performance monitor
23	M23_PII	SW : RW 0x1: The internally generated idle status for Master 23 will be used by the performance monitor 0x0: Primary input I_AXI_M23_IDLE is used by the performance monitor
22	M22_PII	SW : RW 0x1: The internally generated idle status for Master 22 will be used by the performance monitor 0x0: Primary input I_AXI_M22_IDLE is used by the performance monitor
21	M21_PII	SW : RW 0x1: The internally generated idle status for Master 21 will be used by the performance monitor 0x0: Primary input I_AXI_M21_IDLE is used by the performance monitor
20	M20_PII	SW : RW 0x1: The internally generated idle status for Master 20 will be used by the performance monitor 0x0: Primary input I_AXI_M20_IDLE is used by the performance monitor
19	M19_PII	SW : RW 0x1: The internally generated idle status for Master 19 will be used by the performance monitor 0x0: Primary input I_AXI_M19_IDLE is used by the performance monitor
18	M18_PII	SW : RW 0x1: The internally generated idle status for Master 18 will be used by the performance monitor 0x0: Primary input I_AXI_M18_IDLE is used by the performance monitor
17	M17_PII	SW : RW 0x1: The internally generated idle status for Master 17 will be used by the performance monitor 0x0: Primary input I_AXI_M17_IDLE is used by the performance monitor

FABRIC_MONITOR_IDLE_INTERNAL_UPPER_REG (cont.)

Bits	Name	Description
16	M16_PII	SW : RW 0x1: The internally generated idle status for Master 16 will be used by the performance monitor 0x0: Primary input I_AXI_M16_IDLE is used by the performance monitor

0x05203D0C FABRIC_MONITOR_RTR_MASK_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains 1 bit for each of the tenure counters that controls the RTR assertion and clearing of the monitoring results pertaining to the associated tenure counter to account for errors due to starting the monitor in the middle of traffic. A value of 1 indicates that RTR will not be asserted.

FABRIC_MONITOR_RTR_MASK_REG

Bits	Name	Description
31:4	RESERVED_31_4	Reserved
3	RTR_MASK_3	SW : RW 0x1: No RTR will be asserted for Tenure Counter 3 0x0: The design is allowed to assert RTR for Tenure Counter 3
2	RTR_MASK_2	SW : RW 0x1: No RTR will be asserted for Tenure Counter 2 0x0: The design is allowed to assert RTR for Tenure Counter 2
1	RTR_MASK_1	SW : RW 0x1: No RTR will be asserted for Tenure Counter 1 0x0: The design is allowed to assert RTR for Tenure Counter 1
0	RTR_MASK_0	SW : RW 0x1: No RTR will be asserted for Tenure Counter 0 0x0: The design is allowed to assert RTR for Tenure Counter 0

0x05203D10 FABRIC_MASTER_SELECT_HYST_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 0 to Master 15). A value of 1 indicates that the hysteresis timer value is used to keep the master segmented clock on. A value of 0 indicates that the hysteresis timer will not be used in the master segmented clock on.

FABRIC_MASTER_SELECT_HYST_LOWER_REG

Bits	Name	Description
15	M15_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
14	M14_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
13	M13_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
12	M12_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
11	M11_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
10	M10_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
9	M9_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
8	M8_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
7	M7_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
6	M6_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

FABRIC_MASTER_SELECT_HYST_LOWER_REG (cont.)

Bits	Name	Description
5	M5_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
4	M4_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
3	M3_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
2	M2_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
1	M1_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
0	M0_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

0x05203D14 FABRIC_MASTER_SELECT_HYST_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 16to Master 31). A value of 1 indicates that the hysteresis timer value is used to keep the master segmented clock on. A value of 0 indicates that the hysteresis timer will not be used in the master segmented clock on.

FABRIC_MASTER_SELECT_HYST_UPPER_REG

Bits	Name	Description
15	M31_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

FABRIC_MASTER_SELECT_HYST_UPPER_REG (cont.)

Bits	Name	Description
14	M30_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
13	M29_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
12	M28_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
11	M27_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
10	M26_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
9	M25_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
8	M24_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
7	M23_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
6	M22_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
5	M21_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

FABRIC_MASTER_SELECT_HYST_UPPER_REG (cont.)

Bits	Name	Description
4	M20_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
3	M19_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
2	M18_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
1	M17_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.
0	M16_SEL_HYST	SW : RW 0x1: Hysteresis timer is used to keep segmented FCLK on for this master 0x0: Hysteresis timer is not used for this master.

0x05203D18 FABRIC_MASTER_USE_CG_DISABLE_LOWER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 0 to Master 15). A value of 1 indicates that the FMCHR bit 15 can be used to always keep the master segmented clock on, hence disabling HW dynamic clock gating. A value of 0 indicates that the FMCHR bit cannot be used to disable HW dynamic clock gating.

FABRIC_MASTER_USE_CG_DISABLE_LOWER_REG

Bits	Name	Description
15	M15_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 15 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

FABRIC_MASTER_USE_CG_DISABLE_LOWER_REG (cont.)

Bits	Name	Description
14	M14_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 14 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
13	M13_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 13 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
12	M12_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 12 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
11	M11_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 11 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
10	M10_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 10 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
9	M9_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 9 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
8	M8_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 8 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
7	M7_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 7 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
6	M6_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 6 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

FABRIC_MASTER_USE_CG_DISABLE_LOWER_REG (cont.)

Bits	Name	Description
5	M5_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 5 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
4	M4_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 4 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
3	M3_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 3 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
2	M2_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 2 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
1	M1_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 1 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
0	M0_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 0 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

0x05203D1C FABRIC_MASTER_USE_CG_DISABLE_UPPER_REG

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0xFFFF

This register contains 1 bit for each of the masters (Master 16 to Master 31). A value of 1 indicates that the FMCHR bit 15 can be used to always keep the master segmented clock on, hence disabling HW dynamic clock gating. A value of 0 indicates that the FMCHR bit cannot be used to disable HW dynamic clock gating.

FABRIC_MASTER_USE_CG_DISABLE_UPPER_REG

Bits	Name	Description
15	M31_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 31 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
14	M30_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 30 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
13	M29_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 29 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
12	M28_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 28 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
11	M27_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 27 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
10	M26_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 26 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
9	M25_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 25 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
8	M24_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 24 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

FABRIC_MASTER_USE_CG_DISABLE_UPPER_REG (cont.)

Bits	Name	Description
7	M23_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 23 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
6	M22_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 22 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
5	M21_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 21 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
4	M20_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 20 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
3	M19_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 19 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
2	M18_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 18 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
1	M17_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 17 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating
0	M16_USE_CG_DISABLE	SW : RW 0x1: FMCHR bit can be used to disable HW dynamic clock gating for master 16 0x0: FMCHR bit cannot be used to disable HW dynamic clock gating

0x05203D20 FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter0.

FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG0

Bits	Name	Description
15:0	RTENL0	SW : RW Contains the LSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked bytenure counter 0

0x05203D24 FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG0

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter0.

FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG0

Bits	Name	Description
15:0	RTENU0	SW : RW Contains the MSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 0

0x05203D28 FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter1.

FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG1

Bits	Name	Description
15:0	RTENL1	SW : RW Contains the LSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 1

0x05203D2C FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG1

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter1.

FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG1

Bits	Name	Description
15:0	RTENU1	SW : RW Contains the MSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 1

0x05203D30 FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter2.

FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG2

Bits	Name	Description
15:0	RTENL2	SW : RW Contains the LSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 2

0x05203D34 FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG2

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter2.

FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG2

Bits	Name	Description
15:0	RTENU2	SW : RW Contains the MSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 2

0x05203D38 FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 15:0 of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter3.

FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_LOWER_REG3

Bits	Name	Description
15:0	RTENL3	SW : RW Contains the LSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 3

0x05203D3C FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG3

Type: Read/Write
Clock: FABRIC_CLOCK
Reset State: 0x0000

This register contains bits 31:16of the number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter3.

FABRIC_MONITOR_CYCLECOUNT_TENURES_ABV16_UPPER_REG3

Bits	Name	Description
15:0	RTENU3	SW : RW Contains the MSB of number of cycles for which there were more than 16 outstanding tenures for the port tracked by tenure counter 3

9 GSBI Registers

9.1 Overview

Table 9-1 GSBIs Bases

Base Name	Parent	Address
GSBI3_GSBI_CTRL_REG	GSBI3_BASE	0x16200000
GSBI3_UART_DM_MR1	GSBI3_UART_DM_BASE	0x16240000
GSBI3_QUP_CONFIG	QUP3_BASE	0x16280000
GSBI4_GSBI_CTRL_REG	GSBI4_BASE	0x16300000
GSBI4_UART_DM_MR1	GSBI4_UART_DM_BASE	0x16340000
GSBI4_QUP_CONFIG	QUP4_BASE	0x16380000
GSBI5_GSBI_CTRL_REG	GSBI5_BASE	0x1A200000
GSBI5_UART_DM_MR1	GSBI5_UART_DM_BASE	0x1A240000
GSBI5_QUP_CONFIG	QUP5_BASE	0x1A280000
GSBI6_GSBI_CTRL_REG	GSBI6_BASE	0x16500000
GSBI6_UART_DM_MR1	GSBI6_UART_DM_BASE	0x16540000
GSBI6_QUP_CONFIG	QUP6_BASE	0x16580000
GSBI7_GSBI_CTRL_REG	GSBI7_BASE	0x16600000
GSBI7_UART_DM_MR1	GSBI7_UART_DM_BASE	0x16640000
GSBI7_QUP_CONFIG	QUP7_BASE	0x16680000

9.2 GSBI3 Registers (0x16200000 GSBI3_BASE)

This section contains the GSBI3 registers.

9.2.1 GSBI CTRL Registers

0x16200000 GSBI3_GSBI_CTRL_REG

Type: Read/write
Clock: HCLK
Reset State: 0x00000000

GSBI3_GSBI_CTRL_REG

Bits	Name	Description
15:12	RESERVED	reserved
11:8	WRAPPER_CTRL	This field has no predefined use. When a wrapper is constructed around one or more GSBIs there may be a need to configure it. E.g., to select which of several GSBIs will be connected to a particular I2S block. All bits of this field emerge from GSBI as output ports which can be used for any such configuration task.
7	RESERVED_7	Reserved. The host can write and read this field, but its state has no effect on anything.
6:4	PROTOCOL_CODE	This field controls which protocol, if any, is applied to the GSBI's four I/O ports Most codes assign a single protocol, but codes of "001" and "110" assigns I2C to two of the ports and UART (without flow control signals) or SIM to the other two. 0x0: Idle (null values are applied to all four GSBI I/Os) 0x1: I2C on 2 ports, SIM/R-UIM on other 2 0x2: I2C 0x3: SPI 0x4: UART with flow control (or IRDA) 0x5: SIM/R-UIM 0x6: I2C on 2 ports, UART (without HS flow ctrl on other 2) 0x7: Undefined
3:1	RESERVED_3_1	Reserved. The host can write and read this field, but its state has no effect on anything.
0	CRCI_MUX_CTRL	While this bit is low QUP CRCI ports are connected to the GSBI ports nominally for QUP and UART_DM CRCI ports are connected to the GSBI ports nominally for UART_DM. While this bit is high QUP CRCI ports are connected to the GSBI ports nominally for UART_DM and UART_DM CRCI ports are connected to nothing.

0x16200004 GSBI3_GSBI_DBG0_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI3_GSBI_DBG0_REG

Bits	Name	Description
1:0	GSBI_PLAY0	This field has no function beyond the fact that the ARM can write to it and read from it.

0x16200008 GSBI3_GSBI_DBG1_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI3_GSBI_DBG1_REG

Bits	Name	Description
1:0	GSBI_PLAY1	This field has no function beyond the fact that the ARM can write to it and read from it.

0x1620000C GSBI3_GSBI_DBG2_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI3_GSBI_DBG2_REG

Bits	Name	Description
1:0	GSBI_PLAY2	This field has no function beyond the fact that the ARM can write to it and read from it.

0x16200010 GSBI3_GSBI_DBG3_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI3_GSBI_DBG3_REG

Bits	Name	Description
1:0	GSBI_PLAY3	This field has no function beyond the fact that the ARM can write to it and read from it.

9.3 GSBI3 UART DM Registers (0x16240000 GSBI3_UART_DM_BASE)

This section contains the GSBI3 UART DM registers.

9.3.1 Write and read/write registers

0x16240000 GSBI3_UART_DM_MR1

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_MR1 register is the UART mode register 1. It is used, along with UART_DM_MR2, to configure the operational mode of the UART.

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GSBI3_UART_DM_MR1

Bits	Name	Description
31:8	AUTO_RFR_LEVEL1	These bits are used, along with bits 5:0 (AUTO_RFR_LEVEL0) to program the level in the receive FIFO at which the RFR_N signal is de-asserted, if programmed to do so (see RX_RDY_CTL field of this register). The level counts the number of words inside the RX FIFO. It doesn't count the character that is being received (shift register) or characters in the packing buffer. This value is programmed from 1 to 2^RAM_ADDR_WIDTH. The RFR_N signal is de-asserted when the RX FIFO level (the number of characters remaining in the RX FIFO) is greater than the level that is programmed into this register. · Only RAM_ADDR_WIDTH +1:8 bits are generated.
7	RX_RDY_CTL	Setting (1) this bit enables the automatic ready-for-receiving (RFR_N) control for the receiver. RFR_N is turned off, or set (1), when a valid start bit is received and the channel FIFO is at the level programmed in bits 4 through 0 of this mode register. When the FIFO level falls back to the programmed level, the RFR_N signal is turned on, or clear (0). When this feature is off, the RFR_N signal can be used by normal signal port bit manipulation (see UART_DM_CR register).
6	CTS_CTL	When this bit is set(1), the transmitter checks the CTS_N input to determine whether to begin transmission of a new character. If CTS_N is low, the character is sent. Otherwise the transmitter continues marking until CTS_N goes low, then the next character is transmitted. A change on CTS_N during the transmission of a character has no effect on that character. When this bit is clear(0), the CTS_N input for the channel has no effect on the transmitter.

GSBI3_UART_DM_MR1 (cont.)

Bits	Name	Description
5:0	AUTO_RFR_LEVEL0	See the description of bit 8 (AUTO_RFR_LEVEL1).

0x16240004 GSBI3_UART_DM_MR2

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI3_UART_DM_MR2

Bits	Name	Description
9	RX_ERROR_CHAR_OFF	When this bit is asserted, characters with parity or framing errors don't enter RX FIFO. Otherwise they enter RX FIFO.
8	RX_BREAK_ZERO_CHAR_OFF	When this bit is asserted, the zero character received at rx_break doesn't enter RX FIFO. Otherwise it enters RX FIFO.
7	LOOPBACK	Internal use only
6	ERROR_MODE	This bit controls the operation of the two FIFO status bits for the channel (parity or framing error and received break). • When clear (0), the UART operates in character mode and the status bits apply only to the character at the top of the FIFO. • When set (1), the UART operates in block mode and both bits are the "OR" of the status for all previously received characters arriving after the last `reset error status' command was issued (see CR register).
5:4	BITS_PER_CHAR	These bits determine how many bits are transmitted or received per character, not including the start, stop, and parity bits. 0x0: 5 bits 0x1: 6 bits 0x2: 7 bits 0x3: 8 bits
3:2	STOP_BIT_LEN	This field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 9/16, 1, 1+ 9/16, and 2 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. 0x0: 0.563 (9/16 bit times) 0x1: 1.000 bit time 0x2: 1.563 (1+9/16 bit times) 0x3: 2.000 bit times

GSBI3_UART_DM_MR2 (cont.)

Bits	Name	Description
1:0	PARITY_MODE	These bits determine which parity mode is used. The user can select between odd, even, space, or no parity. 0x0: no parity 0x1: odd parity 0x2: even parity 0x3: space parity

0x16240008 GSBI3_UART_DM_CSR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_CSR register is the UART clock selection register. This register is used in conjunction with the UART M/N counter registers to determine the bit rate for the transmitter and receiver. The transmitter and receiver can be clocked at different rates.

The rates below are based on a uart_dm_clk rate of 1.8432 MHz (115.2 * 16).

Table 9-2 lists the hexadecimal values for the clock select field and the corresponding data rates.

Table 9-2 Hexadecimal values and data rates for clock select field

CLK SEL value	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Bit rate (b/sec)	75	150	300	600	1200	2400	3600	4800	7200	9600	14.4k	19.2k	28.8k	38.4k	57.6k	115.2k

GSBI3_UART_DM_CSR

Bits	Name	Description
7:4	UART_RX_CLK_SEL	Use the CLK SEL values in Table 28-12 to select the appropriate receive and transmit bit rates.
3:0	UART_TX_CLK_SEL	

0x16240070 GSBI3_UART_DM_TF

Type: Write
Clock: AHB_CLK
Reset State: Undefined

In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM TX FIFO.

GSBI3_UART_DM_TF

Bits	Name	Description
31:0	UART_TF	The UART_TF register is the UART transmit FIFO register. This register is used to access the channel transmit FIFO. If the FIFO is full at the time of writing, the character is lost and an interrupt is generated (see UART_DM_IMR register).

0x16240074 GSBI3_UART_DM_TF_2

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI3_UART_DM_TF_2

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x16240078 GSBI3_UART_DM_TF_3

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI3_UART_DM_TF_3

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x1624007C GSBI3_UART_DM_TF_4

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI3_UART_DM_TF_4

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x16240010 GSBI3_UART_DM_CR

Type: Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_CR register is the UART command register. This register is used to issue specific commands to the UART subsystem. This register is updated asynchronously.

CAUTION Do not reset the transmitter and disable it at the same time. Do not reset the receiver and disable it at the same time.

Table 9-3 UART DM commands

Value	Description	Result
0	Null command	Does nothing.
1	Reset receiver	Resets the receiver as if a hardware reset were issued. The receiver is disabled and the FIFO, packing buffer and shift registers are flushed.
2	Reset transmitter	Resets the transmitter as if a hardware reset were issued. The transmitter signal goes high (marking) and the FIFO, unpacking register and shift register are flushed.
3	Reset error status	Clears the overrun error and hunt char received status bits in both the character and block error modes. In the block error mode, it clears the error status and received break.
4	Reset break change interrupt	Clears the break change interrupt status bit.
5	Start break	Forces the transmitter signal low. The transmitter must be enabled. If the transmitter is busy, the break is started when all characters in the transmit FIFO and the transmit shift register have been completely sent.
6	Stop break	If executed while channel is breaking, this command causes the transmitter signal to go high. The signal remains high for at least one bit time before sending out a new character.
7	Reset CTS_N	Clears ISR bit 5.
8	Reset stale interrupt	Clears the stale interrupt.
9	Packet mode	Turns on the sample data mode, which causes the receiver to sample the receive data stream at 16 times the programmed baud rate. The data is sampled with the start of the start bit, or the first data bit, and continued until the marking state. To exit this state, write 1100 in the command field.
A	test_parity_on	Internal use only.
B	test_frame_on	Internal use only.
C	Mode reset	Turns off the sample data mode.
D	Set RFR_N	Asserts the ready for receiving signal (active low).
E	Reset RFR_N	De-asserts the ready for receiving signal.
F	uart_reset_int	Internal use only.

Table 9-3 UART DM commands

Value	Description	Result
10	Reset TX_ERROR	Clears TX_ERROR
11	Clear TX_DONE	Clears the TX_DONE interrupt (ISR bit 9)
12	Reset break start interrupt	Clears the break start interrupt status bit.
13	Reset break end interrupt	Clears the break end interrupt status bit.
14	Reset par_frame_err interrupt	Clears the par_frame_err interrupt status bit.

Table 9-4 UART DM commands

Value	Description	Result
0	Null command	Does nothing.
1	CR Protection Enable	Enables CR HW protection. When two consecutive writes to the CR are detected, the second write is delayed until the command of the first write is finished. The delay is done by de-asserting the AHB ready and this ensures that the first command completes and the second one will be executed right afterward.
2	CR Protection Disable	Disables CR HW protection. SW is responsible for managing delay between writes to the CR register.
3	Reset TX-Ready interrupt	Clears the TX_READY interrupt.
5	Enable Stale Event	Enables the `stale event' mechanism. .
6	Disable Stale Event	Disables the `stale event' mechanism.
4	SW Force Stale	Causes a `stale event' (even if `stale event' is disabled).
7	RESERVED	

GSBI3_UART_DM_CR

Bits	Name	Description
11	CHANNEL_COMMAND_MSB	This is the msb of the CHANNEL_COMMAND bit field.
10:8	GENERAL_COMMAND	Writing the appropriate value to these bits executes the commands that are listed in Table.
7:4	CHANNEL_COMMAND_LSB	Writing the appropriate value to these bits along with bit 11,executes the commands that are listed in Table 28-13.
3	UART_TX_DISABLE	This command terminates the operation of the transmitter after any character in the transmit shift register is sent.
2	UART_TX_EN	This command enables the operation of the transmitter.
1	UART_RX_DISABLE	This command immediately terminates the operation of the channel receiver and any incoming characters are lost. None of the receiver status bits are affected by this command and characters that are already in the receive FIFO remain there.

GSBI3_UART_DM_CR (cont.)

Bits	Name	Description
0	UART_RX_EN	This command enables the channel receiver.

0x16240014 GSBI3_UART_DM_IMR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IMR register is the UART interrupt mask register. This register is used to enable the corresponding functions in the UART_DM_ISR register. Setting (1) a bit in the UART_DM_IMR register causes an interrupt to be generated, if the corresponding bit in the UART_DM_ISR register is set. Clearing (0) a bit in the UART_DM_IMR register causes the setting of the corresponding bit in the UART_DM_ISR register to have no effect on the interrupt signal.

Bit 6 of the UART_DM_IMR register, CURRENT_CTS, is slightly different. If the current value of the CTS is one (1), no interrupt is generated. However, the user can use bit 6 in this register to mask the CTS value when reading the UART_DM_MISR register or as a general-purpose bit.

GSBI3_UART_DM_IMR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	This bit is asserted in the same condition at which PAR_FRAME_ERR status bit is asserted. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x14.
11	RXBREAK_END	This bit is set (1) if the end of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x13.
10	RXBREAK_START	This bit is set (1) if the start of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x12.
9	TX_DONE	This bit is used only in UIM/SIM_IF mode. Set (1) this bit when the last byte in the transmitter has been sent. This bit is generated only when SIM_GLUE_GEN generic equals 1.
8	TX_ERROR	Only used in UIM_IF mode. Set (1) this bit to indicate that there has been parity error during transmission. To clear the detection logic associated with this function, write CR[11;7:4]=0x10. This bit is generated only when SIM_GLUE_GEN generic equals 1.

GSBI3_UART_DM_IMR (cont.)

Bits	Name	Description
7	TX_READY	This bit, when set(1), indicates that: 1. TX FIFO is empty. 2. The value written in NO_CHARS_FOR_TX register equals the number of bytes written to the TX FIFO since the register was updated. **NOTE** There may be characters in the unpack buffer or in the shift register. This bit is cleared by issuing `clear TX ready' command (see UART_DM_CR register).
6	CURRENT_CTS	This bit indicates the current state of the CTS input. It never generates an interrupt.
5	DELTA_CTS	This bit, when set (1), indicates that the CTS input has changed states. To clear the detection logic associated with this function, write CR[7:4]=0x7.
4	RXLEV	This bit is set when a character is loaded into the receive FIFO that brings the total number of characters in the FIFO above the programmed watermark level in the FIFO watermark register (RFWR). This bit is cleared after enough characters have been read to bring the level equal to or below the programmed watermark level.
3	RXSTALE	This bit indicates that a `stale event' occurred. It is cleared by issuing a reset-stale command (see CR register).
2	RXBREAK_CHANGE	This bit is set (1) if the start or end of a break condition is detected. The logic associated with this condition is cleared (0) by writing CR[7:4]=0x4. A detected break is defined as an all-zeros character with an invalid stop bit AND LOW PARITY. The end of a break is defined as a mark condition (1) at least 1/2 bit width. A detected break occupies one position in the Rx FIFO.
1	RXHUNT	This bit is set (1) when an incoming character matches the value programmed into the UART_DM_HCR register. This condition is cleared (0) by issuing a reset error status command (CR[7:4]=0x3).
0	TXLEV	This bit is set (1) when a character which is transferred from the transmit FIFO to the transmit shift register brings the total number of characters in the FIFO below or equal to the programmed watermark level in the UART_DM_TFWR register. This bit is cleared (0) after enough characters have been written to the FIFO to bring the level above the programmed watermark level.

0x16240018 GSBI3_UART_DM_IPR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0xffffff9f

The UART_DM_IPR register is the UART interrupt programming register.

GSBI3_UART_DM_IPR

Bits	Name	Description
31:7	STALE_TIMEOUT_MSB	These bits are the STALE_TIMEOUT bit field. The stale character time-out duration field contains a number from 1 to 2^30 -1. This number determines how many character times must elapse before a `stale event' is generated. This character time is defined as 10 times the bit rate. It is reset whenever a data bit is received. Do not clear (0) this register if the stale character time-out interrupt is enabled. Note the discontinuity in the bit assignments.
6	SAMPLE_DATA	Setting (1) this bit enables the new sample data mode, which means that the start bit is sampled as well as the rest, when in sample data mode. See the CR register, CHANNEL_COMMAND bit for more information.
5	RESERVED	
4:0	STALE_TIMEOUT_LSB	This bit field is the LSbits of the STALE_TIMEOUT bitfield.

0x1624001C GSBI3_UART_DM_TFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_TFWR register is the UART transmit FIFO watermark register.

GSBI3_UART_DM_TFWR

Bits	Name	Description
31:0	TFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the transmit FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of TX words in the FIFO) is less than or equal to the value in TFWR. See UART_DM_IMR register. Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x16240020 GSBI3_UART_DM_RFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RFWR register is the UART receive FIFO watermark register.

GSBI3_UART_DM_RFWR

Bits	Name	Description
31:0	RFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the receive FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of words in the RX FIFO) is greater than the value in RFWR. Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x16240024 GSBI3_UART_DM_HCR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI3_UART_DM_HCR

Bits	Name	Description
7:0	DATA	The UART_DM_HCR register is the UART hunt character register, which contains the character for which the receiver looks to assert a hunt character received interrupt.

0x16240034 GSBI3_UART_DM_DMRX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI3_UART_DM_DMRX

Bits	Name	Description
24:0	RX_DM_CRCI_CHARS	In the DM mode, the number of chars in the Rx FIFO that are used for CRCI handshake with the DM. The written value of RX_DM_CRCI_ CHARS must be a multiple of 16(bits [3:0] are treated as 0x0). After a value is written, the UART will generate CRCI requests as long as RX_DM_CRCI_CHARS is non zero. Read of DMRX register gives the number of characters that were received since the end of the last transfer. It is reset at the end of each Rx transfer Also is used by the software to indicate `transfer initialization'.

0x16240038 GSBI3_UART_DM_IRDA

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IRDA register enables the IRDA function, selects a loopback, and allows inversion of RX and TX data. This register also controls the IRDA transceiver that optionally interfaces between the UART and the DP_RX_DATA and DP_TX_DATA pins.

The UART proper is a standard RX/TX configuration that converts the serial pin input and output lines to 8-bit data for the microprocessor. The configuration contains receive and transmit blocks, a control block, a bit rate generator for RX and TX, and FIFO interfaces with the microprocessor data bus. The IRDA register provides the means of switching IRDA circuits into the serial I/O lines and the IRDA function is normally switched out. The IRDA modulator/demodulator may be enabled or disabled under microprocessor control. When enabled, the RX and TX data pathis have individual inversion select bits, so external true or inverted drivers may be used in the signal path.

- The register is generated only when IRDA_IFC_GEN generic equals 1.

GSBI3_UART_DM_IRDA

Bits	Name	Description
4	MEDIUM_RATE_EN	• Set (1) for 1/4 bit-time pulse length (Medium rate) • Clear (0) for 3/16 bit-time pulse length (Low rate)
3	IRDA_LOOPBACK	This bit loops the IRDA modulated TX line back into the IRDA RX line. The normal UART loopback mode must be off in order to see this effect.
2	INVERT_IRDA_TX	This bit inverts the polarity of the IRDA modulated signal on the DP_TX_DATA pin. • Set (1) this bit for an inverted polarity. • Clear (0) this bit for a non-inverted polarity.
1	INVERT_IRDA_RX	This bit inverts the polarity of the IRDA received signal on the DP_RX_DATA pin. • Set (1) this bit for inverted the polarity. • Clear (0) this bit for non-inverted polarity.
0	IRDA_EN	• Set (1) this bit to enable the IRDA transceiver. • Clear (0) this bit to bypass the IRDA transceiver and ignore the other bits of this register.

0x1624003C GSBI3_UART_DM_DMEN

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_DMEN register indicates if Data Mover is enabled for TX and RX channels.

GSBI3_UART_DM_DMEN

Bits	Name	Description
1	RX_DM_EN	· Set (1) this bit to enable RX DM interface. · Clear (0) this bit to disable RX DM interface. Clearing this bit requires resetting the receiver (see UART_DM_CR register).
0	TX_DM_EN	Set (1) this bit to enable TX DM interface. Clear (0) this bit to disable TX DM interface.

0x16240040 GSBI3_UART_DM_NO_CHARS_FOR_TX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI3_UART_DM_NO_CHARS_FOR_TX

Bits	Name	Description
23:0	TX_TOTAL_TRANS_LEN	The total number of characters for transmission. Before writing a new value, the TX FIFO must be empty (as indicated by TX_READY interrupt in IMR register or after a reset). It is used by the transmitter to calculate how many characters to transmit in the last word. In DM mode, it is also used for the CRCI mechanism. Any additional writes to the TX FIFO above TX_TOTAL_TRANS_LEN will be discarded. A TX_READY interrupt is triggered after TX_TOTAL_TRANS_LEN number of characters were moved from the TX FIFO to the unpacking register (not all may have been sent).

0x16240044 GSBI3_UART_DM_BADR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

GSBI3_UART_DM_BADR

Bits	Name	Description
31:2	RX_BASE_ADDR	RX FIFO base address. Both FIFOs use the same RAM (2^RAM_ADDR_WIDTH, 32-bit entries). This register controls the division of the memory to the RX and TX FIFOs. The division is a multiple of 4 entries, since the DM's burst length is 4. The size of the TX FIFO equals RX_BASE_ADDR. The size of the RX FIFO is 2^RAM_ADDR_WIDTH - RX_BASE_ADDR. ® The default is RX_BASE_ADDR = 2^(RAM_ADDR_WIDTH - 1) ® Only RAM_ADDR_WIDTH -1:2 bits are generated.
1:0	UNUSED	

0x16240048 GSBI3_UART_DM_TESTSL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI3_UART_DM_TESTSL

Bits	Name	Description
4	TEST_EN	Test bus enable
3:0	TEST_SEL	Test bus selector

0x16240060 GSBI3_UART_DM_MISR_MODE

Type: Read/Write
Clock: WR_CLK

GSBI3_UART_DM_MISR_MODE

Bits	Name	Description
31:2	RESERVED	unused.
1:0	MODE	0x0: Disabled 0x1: Enabled,TX test 0x2: Enabled, RX test

0x16240064 GSBI3_UART_DM_MISR_RESET

Type: Write
Clock: WR_CLK
Reset State: Undefined

GSBI3_UART_DM_MISR_RESET

Bits	Name	Description
31:1	RESERVED	unused.
0	RESET	

0x16240068 GSBI3_UART_DM_MISR_EXPORT

Type: Read/Write
Clock: WR_CLK
Reset State: Undefined

GSBI3_UART_DM_MISR_EXPORT

Bits	Name	Description
31:1	RESERVED	unused.
0	EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., what is the result of the muxing of all the input data streams with <BLOCK>_TEST_MODE) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x1624006C GSBI3_UART_DM_MISR_VAL

Type: Read
Clock: WR_CLK
Reset State: Undefined

GSBI3_UART_DM_MISR_VAL

Bits	Name	Description
9:0	VAL	Current MISR state

0x16240080 GSBI3_UART_DM_SIM_CFG

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_SIM_CFG register is used to configure the SIM interface for the UART.

- The register is generated only when SIM_GLUE_GEN generic equals 1.

GSBI3_UART_DM_SIM_CFG

Bits	Name	Description
17	UIM_TX_MODE	When this bit is set (1), the transmission portion of the SIM interface operates in block mode (T=1). When clear (0), the transmission portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.
16	UIM_RX_MODE	When this bit is set (1), the receive portion of the SIM interface operates in block mode (T=1). When clear (0), the receive portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.
15:8	SIM_STOP_BIT_LEN	In UIM_IF mode, this field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 1 to 254 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. ..... 11 111110: 254 bit times 0x1: 1 bit times 0x2: 2 bit times
7	SIM_CLK_ON	When this bit is set(1), the UIM_CLK is turned on at either the TD8 or TD4 frequency, as indicated by bit6(UIM_CLK_TD8_SEL). When this bit is cleared, the UIM_CLK is stopped either LOW or HIGH, as indicated by bit 5(UIM_CLK_STOP_HIGH).
6	SIM_CLK_TD8_SEL	This bit selects the UIM_CLK frequency at which the UIM_CLK is turned on. 0x1: TD8 (the UIM_CLK runs at the TD8 frequency) 0x0: TD4 (the UIM_CLK runs at the TD4 frequency)
5	SIM_CLK_STOP_HIGH	This bit indicates at what point - high or low - the UIM_CLK will stop. 0x1: high 0x0: low
4	SIM_CLK_SEL	unused
3	MASK_RX	Setting (1) this bit masks off any 0 on the RX line, which prevents the receiver from seeing the START bit. Set (1) this bit if you do not want to receive the data you transmit.
2	SWAP_D	Setting (1) this bit causes the UIM_IF to swap the 8 data bits (making MSB into LSB, bit 6 into bit1, and so on) before it is read by the microprocessor.
1	INV_D	Set (1) this bit to cause the UIM_IF to invert the 8 data bit before it is read by the microprocessor.
0	SIM_SEL	Set (1) this bit to designate the UIM_IF mode of operation.

0x16240084 GSBI3_UART_DM_TEST_WR_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI3_UART_DM_TEST_WR_ADDR

Bits	Name	Description
31:0	TEST_WR_ADDR	RAM address at which to write the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x16240088 GSBI3_UART_DM_TEST_WR_DATA

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI3_UART_DM_TEST_WR_DATA

Bits	Name	Description
31:0	TEST_WR_DATA	The test data to be written to the RAM. Write to this register triggers the write to the RAM, to TEST_WR_ADDR address.

0x1624008C GSBI3_UART_DM_TEST_RD_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI3_UART_DM_TEST_RD_ADDR

Bits	Name	Description
31:0	TEST_RD_ADDR	RAM address from which to read the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

9.3.2 Read registers

NOTE The addresses of the read-only registers are mapped into the same addresses of the four write-only registers in the section above this one. They are: UART_DM_CSR, UART_DM_TF, UART_DM_CR, and UART_DM_IMR, respectively.

0x16240008 GSBI3_UART_DM_SR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_SR register is the UART status register. This register is used to obtain the current state of the UART subsystem. This register is updated asynchronously.

GSBI3_UART_DM_SR

Bits	Name	Description
8	RX_BREAK_START_LAST	When break start is detected, this bit is set (1). When break end was detected, this bit is reset (0).
7	HUNT_CHAR	When set (1), this bit indicates that the programmed character in the UART_DM_HCR register was received. If programmed, this condition causes the RXHUNT bit to be set (1) in the UART_DM_ISR register. This bit is cleared by issuing a reset error status command.
6	RX_BREAK	When set (1), this bit indicates that an all-zero character of the programmed length was received without a stop bit. If a break begins in the middle of a character, it is detected if the condition remains until the end of the next character time. Only one all zero character is written into the FIFO upon receiving the break. After the RX input returns high for at least half a bit time, then more characters are accepted by the receiver. Whenever the break condition starts or stops as defined above, the RXBREAK bit is set (1) in the UART_DM_ISR register. This bit is appended to the character in the receive FIFO.
5	PAR_FRAME_ERR	A parity error occurs if parity is programmed to be checked and an incoming character is received with incorrect parity. A framing error occurs when the RX input is low while the stop bit is being sampled. This bit is sampled in the middle of the first stop bit position, regardless of the programmed length of the stop bit. This error bit is appended to the character in the receive FIFO.
4	UART_OVERRUN	An overrun error occurs if one or more incoming characters are lost. This happens when the receive FIFO is full, the packing buffer is full and another character has been received in the shift register. The character in the receive shift register is lost. Upon overrun, this status bit remains high until cleared by a reset error status command.
3	TXEMT	This bit is set (1) when the transmitter under-runs. It is set after the transmission of the stop bit at the end of a character, if there are no characters waiting to be sent. It is reset when a character is written to the transmit FIFO.
2	TXRDY	This bit indicates that the transmit FIFO has space in it. It is reset when the FIFO becomes full and set when space becomes available again. Any characters that are written to the FIFO while this bit is low is lost.

GSBI3_UART_DM_SR (cont.)

Bits	Name	Description
1	RXFULL	This bit is set (1) when the receive FIFO becomes full. It is reset when the CPU reads a word.
0	RXRDY	This bit is set (1) when there is a word in the receive FIFO waiting to be read. It is reset when the last word currently stored in the FIFO is read.

0x16240070 GSBI3_UART_DM_RF

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RF register is the UART receive FIFO register, which is used to access the channel receive FIFO. In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM RX FIFO.

GSBI3_UART_DM_RF

Bits	Name	Description
31:0	UART_RF	This register returns the next value in the receive FIFO. After the read is completed, the FIFO read pointer is updated to make the next character available.

0x16240074 GSBI3_UART_DM_RF_2

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI3_UART_DM_RF_2

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x16240078 GSBI3_UART_DM_RF_3

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI3_UART_DM_RF_3

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x1624007C GSBI3_UART_DM_RF_4

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI3_UART_DM_RF_4

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x16240010 GSBI3_UART_DM_MISR

Type: Read
Clock: AHB_CLK
Reset State: 0x0

GSBI3_UART_DM_MISR

Bits	Name	Description
12:0	UART_MISR	The UART_DM_MISR register is the masked interrupt status register. A read from this register returns the "AND" of the UART_DM_ISR and the UART_DM_IMR registers. This register is updated asynchronously. This bit field is misr <= (isr(12 DOWNTO 7) AND imr(12 DOWNTO 7)) & '0' & (isr(5 DOWNTO 0) AND imr(5 DOWNTO 0)).

0x16240014 GSBI3_UART_DM_ISR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_ISR register is the UART interrupt status register. This register provides the current status of the possible interrupt conditions. If one of these bits is set (1), and the corresponding bit in the UART_DM_IMR register is set (1), an interrupt is generated (with the exception of bit 6, CURRENT_CTS - see the description of the UART_DM_IMR register). If the corresponding bit in the UART_DM_IMR register is clear (0), setting one of these bits has no effect on the UART interrupt request signal. This register is updated asynchronously.

GSBI3_UART_DM_ISR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	See UART_DM_IMR on page 28-9
11	RXBREAK_END	See UART_DM_IMR on page 28-9
10	RXBREAK_START	See UART_DM_IMR on page 28-9
9	TX_DONE	Bit 9 generated only when SIM_GLUE_GEN generic equals 1
8	TX_ERROR	Bit 9 generated only when SIM_GLUE_GEN generic equals 1
7	TX_READY	See UART_DM_IMR on page 28-9, for descriptions of the UART_DM_ISR bits.
6	CURRENT_CTS	
5	DELTA_CTS	
4	RXLEV	
3	RXSTALE	
2	RXBREAK	
1	RXHUNT	
0	TXLEV	

0x16240038 GSBI3_UART_DM_RX_TOTAL_SNAP

Type: Read
Clock: AHB_CLK
Reset State: 0x0

GSBI3_UART_DM_RX_TOTAL_SNAP

Bits	Name	Description
23:0	RX_TOTAL_BYTES	'RX_TOTAL_SNAP register holds the number of characters received since the end of last Rx transfer. It is updated at the end of an Rx transfer. Rx transfer ends when one of the conditions is met: · The number of characters which were received since the end of the previous transfer equals the value which was written to DMRX at "Transfer initialization". · A stale event occurred (flush operation already performed if was needed).

0x1624004C GSBI3_UART_DM_TXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI3_UART_DM_TXFS

Bits	Name	Description
31:14	TX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bit field. · Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	TX_ASYNC_FIFO_STATE	TX asynchronous fifo status - number of characters in the TX asynchronous FIFO.
9:7	TX_BUFFER_STATE	TX unpacking buffer status - number of bytes in the unpacking buffer
6:0	TX_FIFO_STATE_LSB	TX FIFO status - number of words in the TX FIFO

0x16240050 GSBI3_UART_DM_RXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI3_UART_DM_RXFS

Bits	Name	Description
31:14	RX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bit field. Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	RX_ASYNC_FIFO_STATE	RX asynchronous fifo status - number of characters in the RX asynchronous FIFO.
9:7	RX_BUFFER_STATE	RX packing buffer status - number of bytes in the packing buffer
6:0	RX_FIFO_STATE_LSB	The number of entries in the RX FIFO that have at least one valid character. It is incremented each time a word is moved from the packing register to the RX FIFO. It is decremented each time a word is read from the RX FIFO. **NOTE** The Uart does not keep track of non-valid characters in each word.

0x16240090 GSBI3_UART_DM_TEST_RD_DATA

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI3_UART_DM_TEST_RD_DATA

Bits	Name	Description
31:0	TEST_RD_DATA	Read from this register triggers the read from the RAM. The register will hold, after read access, data which is found at TEST_RD_ADDR address in the RAM.

9.4 GSBI3 QUP Registers (0x16280000 QUP3_BASE)

This section contains the GSBI3 QUP registers.

0x16280000 GSBI3_QUP_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

a. The contents of this register should only be changed when in the RESET_STATE (see the QUP_STATE register).

b. The value written to the QUP output FIFO, is shifted left toward the MSB before passing it to the mini-core as follows:

- N equals 8 or less - shift 24
- N equals 16 to 9 - shift 16
- N equals 24 to 17 - shift 8
- N equals 32 to 25 - no shift

The MINI_CORE clock selected is as follows:

Null: cc_qup_core_clk

SPI: cc_spi_master_clk

I2C: cc_I2C_clk		

GSBI3_QUP_CONFIG

Bits	Name	Description
31:14	RESERVED_1	reserved
13	CORE_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).
12	APP_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).

GSBI3_QUP_CONFIG (cont.)

Bits	Name	Description
11:8	MINI_CORE	value: 0000 Null core value: 0001 SPI core value: 0010 I2C master controller value: 0011 I2C slave controller value: 0100 Reserved (I2C master & slave for loop back operation) value: 0101 Reserved (map to null core) value: 0110 Reserved (map to null core value: 0111 Reserved (map to null core) See Note 1.
7	NO_INPUT	qup_data_in is not used and the value is a "don't care". The QUP input FIFO is always empty. The input service interrupt and INPUT_SERVICE_FLAG bit are never set. See notes (a) and (b) above.
6	NO_OUTPUT	qup_data_out is not used and is held at the value zero. The QUP output FIFO is always empty. The output service flag and OUTPUT_SERVICE_FLAG bit are never set. qup_data_out is still driven when SPI_CS _N is asserted. The setting for NO_TRI_STATE still applies. See notes (a) and (b) above.
5	RESERVED_2	Reserved.
4:0	N	Number of logical bits N in the mini-core that constitutes a single transfer. The value zero indicates N equals one. The value of all ones indicates N equals 32. The value in this register must be 3 (i.e., N is 4 or higher in order for the STATE field to be set to RUN_STATE). See note (a) above.

0x16280004 GSBI3_QUP_STATE

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b0000000000000000_00000000000XX100

GSBI3_QUP_STATE

Bits	Name	Description
31:5	RESERVED	reserved.
4	I2C_MAST_GEN	Read only. Reflects the RTL generic setting for GEN_I2C_MASTER_MINI_CORE.
3	SPI_GEN	Read only. Reflects the RTL generic setting for GEN_SPI_MINI_CORE.
2	STATE_VALID	Read only. If and only if set to one, writes to the STATE field is allowed or reads from the STATE field is valid. Writes to this bit is ignored.

GSBI3_QUP_STATE (cont.)

Bits	Name	Description
1:0	STATE	When clear (00), the mini-core and related logic is held in RESET_STATE. When set to "01", the mini-core and related logic is released from reset and enters the RUN_STATE. When set to "11", the mini-core and related logic enters the PAUSE_STATE at the next appropriate point in time. Writing (10) to this field clears these two bits. For PAUSE_STATE to RESET_STATE transition, two writes of (10) are required for the transition to complete. See notes 1 and 2. Note 1: SPI - the "next appropriate point in time" is the next time SPI_CS _N de-asserts. If SPI_CS _N is not asserted when the PAUSE_STATE is entered, the SPI_CS _N is maintained in the not asserted state. The PAUSE_STATE is not available for SLAVE operation. Note 2: I2C -

0x16280008 GSBI3_QUP_IO_MODES

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b000000000000000_00000000XXXXXXXX

Unless otherwise stated, register bits written return the value when read.

Notes:

a. "Packing" occurs as follows:

- N equals 8 or less - pack four values into each QUP input FIFO word.
- N equals 16 to 9 - pack two values into each QUP input FIFO word.
- N equals 32 to 17 - no packing. Each mini-core value is moved to an QUP input FIFO word.

b. "Un-Packing" occurs as follows:

- N equals 8 or less - unpack four values from each QUP output FIFO word.
- N equals 16 to 9 - unpack two values from each QUP output FIFO word.
- N equals 32 to 17 - no packing. Each QUP output FIFO value is moved to the mini-core.

GSBI3_QUP_IO_MODES

Bits	Name	Description
31:17	RESERVED	reserved
16	OUTPUT_BIT_SHIFT_EN	If set, enables the QUP output FIFO block to do bit shifting on the output data.

GSBI3_QUP_IO_MODES (cont.)

Bits	Name	Description
15	PACK_EN	Indicates data values from the mini-core are to be packed before placement in the QUP input FIFO. See note (a) above.
14	UNPACK_EN	Indicates data values taken from the QUP output FIFO should be unpacked before passing to the mini-core. See note (b) above.
13:12	INPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_INPUT = 0, then only FIFO_Mode is available)
11:10	OUTPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_OUTPUT = 0, then only FIFO_Mode is available)
9:7	INPUT_FIFO_SIZE	Read only, actual value set by RTL generic. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 6x BLOCK_SIZE
6:5	INPUT_BLOCK_SIZE	Read only. Actual value set by RTL generic. Indicates the block size associated with Block_Mode and Data_Mover_Mode for input. Value 00: 4 Bytes (FIFO_Mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved
4:2	OUTPUT_FIFO_SIZE	Read only. Actual value set by RTL GENERIC. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 16 BLOCK_SIZE
1:0	OUTPUT_BLOCK_SIZE	Read only. Actual value set by RTL GENERIC. Value 00: 04 Bytes (FIFO mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved

0x1628000C GSBI3_QUP_SW_RESET

Type: Write/cmd
Clock: CRIF_CLK
Reset State: 0x0000

A write to this register resets the entire QUP core and all mini-cores. The internal registers are brought back to their reset values. Reading of this register returns zero.

GSBI3_QUP_SW_RESET

Bits	Name	Description
31:0	RESERVED	NA

0x16280010 GSBI3_QUP_TIME_OUT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies if the QUP_MX_OUTPUT_COUNT register and/or QUP_MX_INPUT_COUNT register are enabled. Additionally, this register only applies to Block_Mode and Data_Mover_Mode. The timer starts "ticking" when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The timer pauses for the PAUSE_STATE. If the timer expires before the QUP_MX_OUTPUT_COUNT and/or QUP_MX_INPUT_COUNT are exhausted, then the TIME_OUT_ERR flag is set in the QUP_ERROR_FLAGS register and the interrupt gsbi_qup_irq may be asserted.

GSBI3_QUP_TIME_OUT

Bits	Name	Description
15:0	TIME_OUT_VALUE	Specifies time out value in units of cc_qup_app clock ticks. A value of zero indicates the timer function is not enabled for use. See QUP_CONFIG register for information on clocks.

0x16280014 GSBI3_QUP_TIME_OUT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI3_QUP_TIME_OUT_CURRENT

Bits	Name	Description
31:0	TIME_OUT_CURRENT	Current value of time-out counter.

0x16280018 GSBI3_QUP_OPERATIONAL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0080

GSBI3_QUP_OPERATIONAL

Bits	Name	Description
31:10	RESERVED_1	reserved.
13	IN_BLOCK_READ_REQ	Read only. When set by hardware, indicates QUP input FIFO has BLOCK_SIZE_INPUT amount of data ready for reading. Valid only in Block_Mode.
12	OUT_BLOCK_WRITE_REQ	Read only. When set by hardware, indicates QUP output FIFO needs BLOCK_SIZE_OUTPUT amount of data to be written. Valid only in Block_Mode.
11	MAX_INPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP input FIFO has reached the programmed QUP_MX_INPUT_COUNT value. Valid in FIFO_Mode (only if MX_READ_COUNT is non-zero), Block_Mode and Data_Mover_Mode.
10	MAX_OUTPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP output FIFO has reached the programmed QUP_MX_OUTPUT_COUNT value. Valid in Block_Mode and Data_Mover_Mode.
9	INPUT_SERVICE_FLAG	When set by hardware, indicates QUP input FIFO has an outstanding input service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowleges software has or will read the data. Valid only in all modes.
8	OUTPUT_SERVICE_FLAG	When set by hardware, indicates QUP output FIFO has an outstanding output service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowledges software has or will read the data. Valid only in all modes.
7	INPUT_FIFO_FULL	Read only. When set, indicates the input FIFO is full and can accept no more data from the QUP mini-core.
6	OUTPUT_FIFO_FULL	Read only. When set, indicates the output FIFO is full and can accept no more CRIF writes.
5	INPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the input FIFO has at least one value in it to be read. When clear, indicates the input FIFO is empty.
4	OUTPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the output FIFO has at least one value in it to be shifted out. When clear, indicates the output FIFO is empty.
3:0	RESERVED_2	reserved.

0x1628001C GSBI3_QUP_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

GSBI3_QUP_ERROR_FLAGS

Bits	Name	Description
31:7	RESERVED_1	reserved.
6	TIME_OUT_ERR	The time out limit for a given transfer has been reached.
5	OUTPUT_OVER_RUN_ERR	Indicates the output FIFO was full when a CRIF write was attempted to the FIFO. The write is discarded.
4	INPUT_UNDER_RUN_ERR	Indicates the input FIFO was empty when a CRIF read was attempted to the FIFO. The read value returns is indeterminate.
3	OUTPUT_UNDER_RUN_ER R	Indicates the output FIFO was empty when an output shift operation required a value.
2	INPUT_OVER_RUN_ERR	Indicates the input FIFO was full when an input shift operation provided a new value. When this happens, the new value is discarded.
1:0	RESERVED_2	reserved

0x16280020 GSBI3_QUP_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x007C

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of gsbi_qup_irq and the setting of the corresponding error flag in the QUP_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

GSBI3_QUP_ERROR_FLAGS_EN

Bits	Name	Description
31:7	RESERVED_1	reserved
6	TIME_OUT_ERR_EN	If set, enables time out error generation.
5	OUTPUT_OVER_RUN_ERR _EN	If set, enables output over run error generation.

GSBI3_QUP_ERROR_FLAGS_EN (cont.)

Bits	Name	Description
4	INPUT_UNDER_RUN_ERR_EN	If set, enables input under run error generation.
3	OUTPUT_UNDER_RUN_ERR_EN	If set, enables output under run error generation.
2	INPUT_OVER_RUN_ERR_EN	If set, enables input over run error generation.
1:0	RESERVED_2	reserved

0x16280024 GSBI3_QUP_TEST_CTRL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register enables QUP test bus to be actively driven by QUP core signals.

GSBI3_QUP_TEST_CTRL

Bits	Name	Description
31:1	RESERVED	reserved
0	QUP_TEST_BUS_EN	If set, enables QUP core to actively drive test bus. If zero, the core drives the test bus to all zeros.

9.4.1 QUP output FIFO registers

0x16280100 GSBI3_QUP_MX_OUTPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each output transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not effect the count.

Notes:

a. Allows the total number of Mini Core transfers to be less than an exact multiple of OUTPUT_BLOCK_SIZE. Any additional outputs are discarded.

GSBI3_QUP_MX_OUTPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_COUNT	Number of writes of size N to the mini-core per RUN_STATE. A value of zero indicates the output count function is not enabled for use. See note (a) above.

0x16280104 GSBI3_QUP_MX_OUTPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI3_QUP_MX_OUTPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_CNT_CURRENT	Current value of QUP_MX_OUTPUT_COUNT.

0x16280108 GSBI3_QUP_OUTPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

This register holds the output data hanging out of the QUP output FIFO ready be loaded into the mini-core for the next load operation. This corresponds to signal qup_data_out going into the mini-core block.

GSBI3_QUP_OUTPUT_DEBUG

Bits	Name	Description
31:0	OUTPUT_DEBUG_DATA	Value waiting at the exit of output FIFO.

0x1628010C GSBI3_QUP_OUTPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the output FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the

value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

GSBI3_QUP_OUTPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	OUTPUT_FIFO_WORD_CNT	Number of words in the output FIFO.

0x16280110+4*c GSBI3_QUP_OUTPUT_FIFOc, c=[0..15]

Type: Write
Clock: CRIF_CLK
Reset State: 0x0000

Note that consecutive writes to this address keeps filling up the output FIFO. The max address to address the output FIFO is 0x14C.

GSBI3_QUP_OUTPUT_FIFOc

Bits	Name	Description
31:0	OUTPUT	Value to be shifted out.

0x16280150 GSBI3_QUP_MX_WRITE_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_OUTPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the gsbi_qup_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_OUTPUT_COUNT register case, the SW should not program the QUP_MX_WRITE_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_OUTPUT * FIFO_SIZE_OUTPUT).

GSBI3_QUP_MX_WRITE_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_COUNT	The number of "writes" of size N. This is used only if the core is in FIFO_Mode.

0x16280154 GSBI3_QUP_MX_WRITE_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI3_QUP_MX_WRITE_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_CNT_CURRENT	Current value of QUP_MX_WRITE_COUNT counter.

9.4.2 QUP input FIFO registers

0x16280200 GSBI3_QUP_MX_INPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each input transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not affect the count.

Notes:

a. Allows the number of shift register transfers to be less than an exact multiple of INPUT_BLOCK_SIZE. When count reached, remainder of INPUT_BLOCK_SIZE is filled with zeroes.

GSBI3_QUP_MX_INPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_COUNT	Number of reads of size N from the mini-core per RUN_STATE. A value of zero indicates the input count function is not enabled for use. See note (a) above.

0x16280204 GSBI3_QUP_MX_INPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI3_QUP_MX_INPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_CNT_CURRENT	Current value of QUP_MX_INPUT_COUNT.

0x16280208 GSBI3_QUP_MX_READ_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_INPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the qup_input_service_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_INPUT_COUNT register case, the SW should not program the QUP_MX_READ_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_INPUT * FIFO_SIZE_INPUT). If the SPI mini-core and slave operation is enabled, then an InputOverRun error will result.

GSBI3_QUP_MX_READ_COUNT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_COUNT	The number of "reads" of size N. This is used only if the core is in FIFO_Mode.

0x1628020C GSBI3_QUP_MX_READ_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI3_QUP_MX_READ_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_CNT_CURRENT	Current value of QUP_MX_READ_COUNT counter.

0x16280210 GSBI3_QUP_INPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the value of the last loaded in known-good-data into the QUP input FIFO. May be different from what the actual read of input FIFO will return because of packing enabled at the input side. This corresponds to signal qup_data_in coming from the mini-core block synchronized to the crif_clk.

GSBI3_QUP_INPUT_DEBUG

Bits	Name	Description
31:0	INPUT_DEBUG_DATA	Last known good value shifted into the input FIFO.

0x16280214 GSBI3_QUP_INPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the input FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

GSBI3_QUP_INPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	INPUT_FIFO_WORD_CNT	Number of words in the input FIFO.

0x16280218+4*c GSBI3_QUP_INPUT_FIFOc, c=[0..15]

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

Consecutive reads to this address reads the input FIFO contents on a FIFO basis.The max address to read the input FIFO is 0x254.

GSBI3_QUP_INPUT_FIFOc

Bits	Name	Description
31:0	INPUT	Value shifted in.

9.4.3 SPI mini-core registers

0x16280300 GSBI3_SPI_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register. Both NO_OUTPUT and NO_INPUT set to zero provides default full duplex operation. Setting both these bits to one is not a legal operational state.

GSBI3_SPI_CONFIG

Bits	Name	Description
31:11	RESERVED_1	Reserved.
10	HS_MODE	When set, SPI HS_MODE is enabled. When clear, SPI HS_MODE is disabled.
9	INPUT_FIRST	When set, INPUT FIRST SPI protocol is used. When clear, OUTPUT FIRST SPI protocol is used.
8	LOOP_BACK	Loopback is only valid in non-HS mode. Always clear for normal operation. If set, loop back on SPI_DATA_MO_SI under MASTER operation or SPI_DATA_MI_SO under SLAVE operation.
7:6	RESERVED_2	Reserved.
5	SLAVE_OPERATION	This register is writable only when the hardware signal spi_slave_en is asserted. When set, the SPI is configured for SLAVE operation. Zero indicates MASTER operation.
4:0	RESERVED	Reserved.

0x16280304 GSBI3_SPI_IO_CONTROL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register.

Unless otherwise stated, register bits written return the value when read.

GSBI3_SPI_IO_CONTROL

Bits	Name	Description
31:11	RESERVED	Reserved.
10	CLK_IDLE_HIGH	Use SPI_CLK_IDLE_HIGH when set.
9	CLK_ALWAYS_ON	When MASTER operation is used, run SPI_CLK during IDLE.
8	MX_CS_MODE	If this bit is set, then for a given RUN state, the associated chip select will be asserted for the first N-bit transfer and will be kept asserted till the last programmed transfer. Applies only in MASTER mode. The number of transfers is determined by SPI_MX_OUTPUT_COUNT and/or SPI_MX_INPUT_COUNT registers.
7:4	CS_N_POLARITY	These four bits control the polarity of four SPI_CS _N respectively. Setting any of this bit to '1', makes the associated SPI_CS _N active HIGH. This field is a "don't care" in SLAVE operation.
3:2	CS_SELECT	When MASTER operation is used, controls the assertion of SPI_CS_ N pins. Selects SPI_CS_N if 00, SPI_CS1_N if 01, SPI_CS2_N if 10, or SPI_CS3_N if 11. The deselected ChipSelects will be driven to inactive state dictated by the field CS_N_POLARITY. This field is a "don't care" in SLAVE operation.
1	TRISTATE_CS	When set, drives Z on all SPI_CS _N lines. When clear, enables normal functionality on these lines. This bit can be used to support deployment of the core as one of the masters in a multi-master configuration.
0	NO_TRI_STATE	When set, spi_data_out is not taken tri-state when SPI_CS _N is de-asserted. This bit is normally set for MASTER operation but may be optionally left cleared.

0x16280308 GSBI3_SPI_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

GSBI3_SPI_ERROR_FLAGS

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.

GSBI3_SPI_ERROR_FLAGS (cont.)

Bits	Name	Description
1	SPI_SLV_CLK_OVER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was greater than the programmed value of N. When this happens, only the first N bits are passed to the SPI input FIFO and the output shift value is held at zero.
0	SPI_SLV_CLK_UNDER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was less than the programmed value of N. When this occurs, the bits which were received are passed to the SPI input FIFO and the CURRENT output bit is forced to zero.

0x1628030C GSBI3_SPI_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0003

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of spi_error_irq and the setting of the corresponding error flag in the SPI_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

GSBI3_SPI_ERROR_FLAGS_EN

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.
1	SPI_SLV_CLK_OVER_RUN_ERR_EN	If set, enables clock over run error generation.
0	SPI_SLV_CLK_UNDER_RUN_ERR_EN	If set, enables clock under run error generation.

0x16280310 GSBI3_SPI_DEASSERT_WAIT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the de-assertion wait time of SPI_CS _N between consecutive N-bit transfers in MASTER operation. The wait time is specified in number of cycles of cc_spi_master_clk.

GSBI3_SPI_DEASSERT_WAIT

Bits	Name	Description
31:6	RESERVED	Reserved.

GSBI3_SPI_DEASSERT_WAIT (cont.)

Bits	Name	Description
5:0	DEASSERT_WAIT	Number cc_spi_master_clk ticks associated with the de-asserted time of SPI_CS _N. Only applies to MASTER operation. For SLAVE operation, this field is a "don't care". A value of zero indicates SPI_CS _N remains de-asserted for exactly one clock tick. A value of one, indicates two ticks, etc. All ones indicates 64 ticks.

9.4.4 I2C master mini-core registers

0x16280400 GSBI3_I2C_MASTER_CLK_CTL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_CLK_CTL register is a read/write register that controls clock divider values. This register should only be written to after it is confirmed that the I2C master mini-core is not longer in RESET state (QUP_STATE register).

GSBI3_I2C_MASTER_CLK_CTL

Bits	Name	Description
31:11	RESERVED	Reserved.
10:8	HS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in high-speed (HS) mode. The minimum value should be 3 hex (4 I2C_clk clocks per period) to ensure proper sampling of the bus. For a maximum high speed bit rate of 3.4 Mb/s (high speed mode), this would require a minimum 40.8 MHz I2C_clk clock. The maximum I2C_clk is 81.6 MHz. This register is reset to a maximum value of 7 hex. I2C_HS_CLK = I2C_CLK/(3*(HS_DIVIDER_VALUE+1)
7:0	FS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in fast/standard (FS) mode. The minimum value should be 3 hex to ensure proper sampling of the bus. For a maximum bit rate of 400 kb/s (fast mode), this would require a 4.8 MHz I2C_clk clock. For a maximum bit rate of 100 kb/s (standard mode), this would require a 1.2 MHz I2C_clk clock. Maximum I2C_clk for fast and standard modes are 206.4 MHz and 51.6 MHz respectively. This register is reset to a maximum value of 255 hex. I2C_FS_CLK = I2C_CLK/(2*(FS_DIVIDER_VALUE+3)

0x16280404 GSBI3_I2C_MASTER_STATUS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_STATUS is a status register. Writing a one clears the status bits.

GSBI3_I2C_MASTER_STATUS

Bits	Name	Description
31:26	RESERVED_1	Reserved.
25	INVALID_READ_SEQ	This bit is set (1) when a MI_REC tag does not follow a START tag for an I2C READ. Not applicable for Halcyon.
24	INVALID_READ_ADDR	This bit is set (1) when the I2C controller is trying to receive data from a non-existent I2C slave (address).
23	INVALID_TAG	This bit is set (1) when the I2C controller is trying to process data from the output FIFO that is improperly tagged.
22:20	INPUT_FSM_STATE	This 3-bit field informs the microprocessor of the state of the I2C MASTER INPUT FSM block. Reset, read_last_byte, mi_rec, dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: READ_LAST_BYTE_STATE Value 0x3: MI_REC_STATE Value 0x4: DEC_STATE Value 0x5: STORE_STATE
19:16	OUTPUT_FSM_STATE	This 4-bit field informs the microprocessor of the state of the I2C MASTER OUTPUT FSM block. Reset, decode, send, mi_red, nop, nop_dec, invalid, invalid_dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: DECODE_STATE Value 0x3: SEND_STATE Value 0x4: MI_REC_STATE Value 0x5: NOP_STATE Value 0x6: INVALID_STATE Value 0x7: PEEK_STATE Value 0x8: SEND_R_STATE

GSBI3_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
15:13	CLK_STATE	This 3-bit field informs the microprocessor of the state of the I2C clk_control block. Reset_busidle, not_master, high, low, high_wait, forced_low, hs_addr_low or double_buffer_wait. Value 0x0: RESET_BUSIDLE_STATE Value 0x1: NOT_MASTER_STATE Value 0x2: HIGH_STATE Value 0x3: LOW_STATE Value 0x4: HIGH_WAIT_STATE Value 0x5: FORCED_LOW_STATE Value 0x6: HS_ADDR_LOW_STATE Value 0x7: DOUBLE_BUFFER_WAIT_STATE
12:10	DATA_STATE	This 3-bit field informs the microprocessor of the state of the I2C data_control block. Reset, Tx addr, Tx HS addr, Tx 10-bit addr, Tx 2nd 10-bit addr byte, Tx data and Rx data. Value 0x0: RESET_WAIT_STATE Value 0x1: TX_ADDR_STATE Value 0x2: TX_DATA_STATE Value 0x3: TX_HS_ADDR_STATE Value 0x4: TX_10_BIT_ADDR_STATE Value 0x5: TX_2ND_BYTE_STATE Value 0x6: RX_DATA_STATE
9	BUS_MASTER	This bit is set (1) when the I2C controller is the present bus master.
8	BUS_ACTIVE	This bit is set (1) when the bus is in use by this, or any other controller.
7:6	FAILED	This 2-bit field contains the failure information of the present I2C transfers. If transmitting, failed[1] contains the information regarding the byte that has been transmitted. Failed[0] contains the information of the byte awaiting transmission if there is a byte pipelined. If no byte is pipelined, ignore this bit. If receiving, failed[1] contains the information of the byte received and stored in the buffer, and failed[0] should be ignored. For example: Value 00: Byte n transmitted successfully, byte n+1 to begin transmission Value 01: Byte n transmitted successfully, byte n+1 errored: type of error indicated in other STATUS bits. (queued invalid write, for example) Value 10: Byte n errored: type of error indicated in other STATUS bits, byte n+1 to begin transmission (byte n+1 would have to be a valid address byte for this condition to occur) Value 11: Byte n errored: type of error indicated in other STATUS bits, byte n+1 discarded as well (if the byte was a data byte destined for a NACKed address, data is useless, therefore discarded)
5	INVALID_WRITE	This bit is set (1) when software writes data to the I2C_DATA register that should be flagged as an address but is not.

GSBI3_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
4	ARB_LOST	This bit is set (1) when the controller loses arbitration for the bus. If this bit gets set (1) during the transmission, all data has been lost, and the microprocessor must re-request its transmission.
3	PACKET_NACKED	This bit is set high when a NACK is received from a slave. If a high speed master code is sent and there is an ACK from a slave, then this bit is set (1) to indicate that the high speed mode can not be entered. If the high speed mode is accepted by the slave, then a NACK is performed and this bit is not set (1).
2	BUS_ERROR	This bit is set (1) when an unexpected START or STOP condition is detected. This returns the controller to its reset state.
1:0	RESERVED_2	Reserved.

9.5 GSBI4 Registers (0x16300000 GSBI4_BASE)

This section contains the GSBI4 registers.

9.5.1 GSBI CTRL Registers

0x16300000 GSBI4_GSBI_CTRL_REG

Type: Read/write
Clock: HCLK
Reset State: 0x00000000

GSBI4_GSBI_CTRL_REG

Bits	Name	Description
15:12	RESERVED	reserved
11:8	WRAPPER_CTRL	This field has no predefined use. When a wrapper is constructed around one or more GSBIs there may be a need to configure it. E.g., to select which of several GSBIs will be connected to a particular I2S block. All bits of this field emerge from GSBI as output ports which can be used for any such configuration task.
7	RESERVED_7	Reserved. The host can write and read this field, but its state has no effect on anything.
6:4	PROTOCOL_CODE	This field controls which protocol, if any, is applied to the GSBI's four I/O ports. Most codes assign a single protocol, but codes of "001" and "110" assigns I2C to two of the ports and UART (without flow control signals) or SIM to the other two. 0x0: Idle (null values are applied to all four GSBI I/Os) 0x1: I2C on 2 ports, SIM/R-UIM on other 2 0x2: I2C 0x3: SPI 0x4: UART with flow control (or IRDA) 0x5: SIM/R-UIM 0x6: I2C on 2 ports, UART (without HS flow ctrl on other 2) 0x7: Undefined
3:1	RESERVED_3_1	Reserved. The host can write and read this field, but its state has no effect on anything.
0	CRCI_MUX_CTRL	While this bit is low QUP CRCI ports are connected to the GSBI ports nominally for QUP and UART_DM CRCI ports are connected to the GSBI ports nominally for UART_DM. While this bit is high QUP CRCI ports are connected to the GSBI ports nominally for UART_DM and UART_DM CRCI ports are connected to nothing.

0x16300004 GSBI4_GSBI_DBG0_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI4_GSBI_DBG0_REG

Bits	Name	Description
1:0	GSBI_PLAY0	This field has no function beyond the fact that the ARM can write to it and read from it.

0x16300008 GSBI4_GSBI_DBG1_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI4_GSBI_DBG1_REG

Bits	Name	Description
1:0	GSBI_PLAY1	This field has no function beyond the fact that the ARM can write to it and read from it.

0x1630000C GSBI4_GSBI_DBG2_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI4_GSBI_DBG2_REG

Bits	Name	Description
1:0	GSBI_PLAY2	This field has no function beyond the fact that the ARM can write to it and read from it.

0x16300010 GSBI4_GSBI_DBG3_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI4_GSBI_DBG3_REG

Bits	Name	Description
1:0	GSBI_PLAY3	This field has no function beyond the fact that the ARM can write to it and read from it.

9.6 GSBI4 UART DM Registers (0x16340000 GSBI4_UART_DM_BASE)

This section contains the GSBI4 UART DM registers.

9.6.1 UART_DM registers

This section contains the read and write registers for UART1.

9.6.1.1 Write and read/write registers

0x16340000 GSBI4_UART_DM_MR1

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_MR1 register is the UART mode register 1. It is used, along with UART_DM_MR2, to configure the operational mode of the UART.

GSBI4_UART_DM_MR1

Bits	Name	Description
31:8	AUTO_RFR_LEVEL1	These bits are used, along with bits 5:0 (AUTO_RFR_LEVEL0) to program the level in the receive FIFO at which the RFR_N signal is de-asserted, if programmed to do so (see RX_RDY_CTL field of this register). The level counts the number of words inside the RX FIFO. It doesn't count the character that is being received (shift register) or characters in the packing buffer. This value is programmed from 1 to 2^RAM_ADDR_WIDTH. The RFR_N signal is de-asserted when the RX FIFO level (the number of characters remaining in the RX FIFO) is greater than the level that is programmed into this register. · Only RAM_ADDR_WIDTH +1:8 bits are generated.
7	RX_RDY_CTL	Setting (1) this bit enables the automatic ready-for-receiving (RFR_N) control for the receiver. RFR_N is turned off, or set (1), when a valid start bit is received and the channel FIFO is at the level programmed in bits 4 through 0 of this mode register. When the FIFO level falls back to the programmed level, the RFR_N signal is turned on, or clear (0). When this feature is off, the RFR_N signal can be used by normal signal port bit manipulation (see UART_DM_CR register).

GSBI4_UART_DM_MR1 (cont.)

Bits	Name	Description
6	CTS_CTL	When this bit is set(1), the transmitter checks the CTS_N input to determine whether to begin transmission of a new character. If CTS_N is low, the character is sent. Otherwise the transmitter continues marking until CTS_N goes low, then the next character is transmitted. A change on CTS_N during the transmission of a character has no effect on that character. When this bit is clear(0), the CTS_N input for the channel has no effect on the transmitter.
5:0	AUTO_RFR_LEVEL0	See the description of bit 8 (AUTO_RFR_LEVEL1).

0x16340004 GSBI4_UART_DM_MR2

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI4_UART_DM_MR2

Bits	Name	Description
9	RX_ERROR_CHAR_OFF	When this bit is asserted, characters with parity or framing errors don't enter RX FIFO. Otherwise they enter RX FIFO.
8	RX_BREAK_ZERO_CHAR_OFF	When this bit is asserted, the zero character received at rx_break doesn't enter RX FIFO. Otherwise it enters RX FIFO.
7	LOOPBACK	Internal use only
6	ERROR_MODE	This bit controls the operation of the two FIFO status bits for the channel (parity or framing error and received break). · When clear (0), the UART operates in character mode and the status bits apply only to the character at the top of the FIFO. · When set (1), the UART operates in block mode and both bits are the "OR" of the status for all previously received characters arriving after the last `reset error status' command was issued (see CR register).
5:4	BITS_PER_CHAR	These bits determine how many bits are transmitted or received per character, not including the start, stop, and parity bits. 0x0: 5 bits 0x1: 6 bits 0x2: 7 bits 0x3: 8 bits

GSBI4_UART_DM_MR2 (cont.)

Bits	Name	Description
3:2	STOP_BIT_LEN	This field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 9/16, 1, 1+ 9/16, and 2 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. 0x0: 0.563 (9/16 bit times) 0x1: 1.000 bit time 0x2: 1.563 (1+9/16 bit times) 0x3: 2.000 bit times
1:0	PARITY_MODE	These bits determine which parity mode is used. The user can select between odd, even, space, or no parity. 0x0: no parity 0x1: odd parity 0x2: even parity 0x3: space parity

0x16340008 GSBI4_UART_DM_CSR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_CSR register is the UART clock selection register. This register is used in conjunction with the UART M/N counter registers to determine the bit rate for the transmitter and receiver. The transmitter and receiver can be clocked at different rates.

The rates below are based on a uart_dm_clk rate of 1.8432 MHz (115.2 * 16).

Table 9-5 lists the hexadecimal values for the clock select field and the corresponding data rates.

Table 9-5 Hexadecimal values and data rates for clock select field

CLK SEL value	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Bit rate (b/sec)	75	150	300	600	1200	2400	3600	4800	7200	9600	14.4k	19.2k	28.8k	38.4k	57.6k	115.2k

GSBI4_UART_DM_CSR

Bits	Name	Description
7:4	UART_RX_CLK_SEL	Use the CLK SEL values in Table 28-12 to select the appropriate receive and transmit bit rates.
3:0	UART_TX_CLK_SEL	

0x16340070 GSBI4_UART_DM_TF

Type: Write
Clock: AHB_CLK
Reset State: Undefined

In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM TX FIFO.

GSBI4_UART_DM_TF

Bits	Name	Description
31:0	UART_TF	The UART_TF register is the UART transmit FIFO register. This register is used to access the channel transmit FIFO. If the FIFO is full at the time of writing, the character is lost and an interrupt is generated (see UART_DM_IMR register).

0x16340074 GSBI4_UART_DM_TF_2

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI4_UART_DM_TF_2

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x16340078 GSBI4_UART_DM_TF_3

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI4_UART_DM_TF_3

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x1634007C GSBI4_UART_DM_TF_4

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI4_UART_DM_TF_4

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x16340010 GSBI4_UART_DM_CR

Type: Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_CR register is the UART command register. This register is used to issue specific commands to the UART subsystem. This register is updated asynchronously.

CAUTION Do not reset the transmitter and disable it at the same time. Do not reset the receiver and disable it at the same time.

Table 9-6 UART DM commands

Value	Description	Result
0	Null command	Does nothing.
1	Reset receiver	Resets the receiver as if a hardware reset were issued. The receiver is disabled and the FIFO, packing buffer and shift registers are flushed.
2	Reset transmitter	Resets the transmitter as if a hardware reset were issued. The transmitter signal goes high (marking) and the FIFO, unpacking register and shift register are flushed.
3	Reset error status	Clears the overrun error and hunt char received status bits in both the character and block error modes. In the block error mode, it clears the error status and received break.
4	Reset break change interrupt	Clears the break change interrupt status bit.
5	Start break	Forces the transmitter signal low. The transmitter must be enabled. If the transmitter is busy, the break is started when all characters in the transmit FIFO and the transmit shift register have been completely sent.
6	Stop break	If executed while channel is breaking, this command causes the transmitter signal to go high. The signal remains high for at least one bit time before sending out a new character.
7	Reset CTS_N	Clears ISR bit 5.
8	Reset stale interrupt	Clears the stale interrupt.
9	Packet mode	Turns on the sample data mode, which causes the receiver to sample the receive data stream at 16 times the programmed baud rate. The data is sampled with the start of the start bit, or the first data bit, and continued until the marking state. To exit this state, write 1100 in the command field.
A	test_parity_on	Internal use only.

Table 9-6 UART DM commands

Value	Description	Result
B	test_frame_on	Internal use only.
C	Mode reset	Turns off the sample data mode.
D	Set RFR_N	Asserts the ready for receiving signal (active low).
E	Reset RFR_N	De-asserts the ready for receiving signal.
F	uart_reset_int	Internal use only.
10	Reset TX_ERROR	Clears TX_ERROR
11	Clear TX_DONE	Clears the TX_DONE interrupt (ISR bit 9)
12	Reset break start interrupt	Clears the break start interrupt status bit.
13	Reset break end interrupt	Clears the break end interrupt status bit.
14	Reset par_frame_err interrupt	Clears the par_frame_err interrupt status bit.

Table 9-7 UART DM command values

Value	Description	Result
0	Null command	Does nothing.
1	CR Protection Enable	Enables CR HW protection. When two consecutive writes to the CR are detected, the second write is delayed until the command of the first write is finished. The delay is done by de-asserting the AHB ready and this ensures that the first command completes and the second one will be executed right afterward.
2	CR Protection Disable	Disables CR HW protection. SW is responsible for managing delay between writes to the CR register.
3	Reset TX-Ready interrupt	Clears the TX_READY interrupt.
5	Enable Stale Event	Enables the `stale event' mechanism. See Software Procedures.
6	Disable Stale Event	Disables the `stale event' mechanism. See Software Procedures.
4	SW Force Stale	Causes a `stale event' (even if `stale event' is disabled). See Software Procedures.
7	RESERVED	

GSBI4_UART_DM_CR

Bits	Name	Description
11	CHANNEL_COMMAND_MSB	This is the msb of the CHANNEL_COMMAND bitfield.
10:8	GENERAL_COMMAND	Writing the appropriate value to these bits executes the commands that are listed in Table .
7:4	CHANNEL_COMMAND_LSB	Writing the appropriate value to these bits along with bit 11,executes the commands that are listed in Table 28-13.
3	UART_TX_DISABLE	This command terminates the operation of the transmitter after any character in the transmit shift register is sent.

GSBI4_UART_DM_CR (cont.)

Bits	Name	Description
2	UART_TX_EN	This command enables the operation of the transmitter.
1	UART_RX_DISABLE	This command immediately terminates the operation of the channel receiver and any incoming characters are lost. None of the receiver status bits are affected by this command and characters that are already in the receive FIFO remain there.
0	UART_RX_EN	This command enables the channel receiver.

0x16340014 GSBI4_UART_DM_IMR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IMR register is the UART interrupt mask register. This register is used to enable the corresponding functions in the UART_DM_ISR register. Setting (1) a bit in the UART_DM_IMR register causes an interrupt to be generated, if the corresponding bit in the UART_DM_ISR register is set. Clearing (0) a bit in the UART_DM_IMR register causes the setting of the corresponding bit in the UART_DM_ISR register to have no effect on the interrupt signal.

Bit 6 of the UART_DM_IMR register, CURRENT_CTS, is slightly different. If the current value of the CTS is one (1), no interrupt is generated. However, the user can use bit 6 in this register to mask the CTS value when reading the UART_DM_MISR register or as a general-purpose bit.

GSBI4_UART_DM_IMR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	This bit is asserted in the same condition at which PAR_FRAME_ERR status bit is asserted. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x14.
11	RXBREAK_END	This bit is set (1) if the end of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x13.
10	RXBREAK_START	This bit is set (1) if the start of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x12.
9	TX_DONE	This bit is used only in UIM/SIM_IF mode. Set (1) this bit when the last byte in the transmitter has been sent. This bit is generated only when SIM_GLUE_GEN generic equals 1.

GSBI4_UART_DM_IMR (cont.)

Bits	Name	Description
8	TX_ERROR	Only used in UIM_IF mode. Set (1) this bit to indicate that there has been parity error during transmission. To clear the detection logic associated with this function, write CR[11;7:4]=0x10. This bit is generated only when SIM_GLUE_GEN generic equals 1.
7	TX_READY	This bit, when set(1), indicates that: 1. TX FIFO is empty. 2. The value written in NO_CHARS_FOR_TX register equals the number of bytes written to the TX FIFO since the register was updated. **NOTE** There may be characters in the unpack buffer or in the shift register. This bit is cleared by issuing `clear TX ready' command (see UART_DM_CR register).
6	CURRENT_CTS	This bit indicates the current state of the CTS input. It never generates an interrupt.
5	DELTA_CTS	This bit, when set (1), indicates that the CTS input has changed states. To clear the detection logic associated with this function, write CR[7:4]=0x7.
4	RXLEV	This bit is set when a character is loaded into the receive FIFO that brings the total number of characters in the FIFO above the programmed watermark level in the FIFO watermark register (RFWR). This bit is cleared after enough characters have been read to bring the level equal to or below the programmed watermark level.
3	RXSTALE	This bit indicates that a `stale event' occurred. See Software procedures for the exact timing of this interrupt. It is cleared by issuing a reset-stale command (see CR register).
2	RXBREAK_CHANGE	This bit is set (1) if the start or end of a break condition is detected. The logic associated with this condition is cleared (0) by writing CR[7:4]=0x4. A detected break is defined as an all-zeros character with an invalid stop bit AND LOW PARITY. The end of a break is defined as a mark condition (1) at least 1/2 bit width. A detected break occupies one position in the Rx FIFO.
1	RXHUNT	This bit is set (1) when an incoming character matches the value programmed into the UART_DM_HCR register. This condition is cleared (0) by issuing a reset error status command (CR[7:4]=0x3).
0	TXLEV	This bit is set (1) when a character which is transferred from the transmit FIFO to the transmit shift register brings the total number of characters in the FIFO below or equal to the programmed watermark level in the UART_DM_TFWR register. This bit is cleared (0) after enough characters have been written to the FIFO to bring the level above the programmed watermark level.

0x16340018 GSBI4_UART_DM_IPR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0xffffff9f

The UART_DM_IPR register is the UART interrupt programming register.

GSBI4_UART_DM_IPR

Bits	Name	Description
31:7	STALE_TIMEOUT_MSB	These bits are the STALE_TIMEOUT bitfield. The stale character time-out duration field contains a number from 1 to 2^30 -1. This number determines how many character times must elapse before a `stale event' is generated. This character time is defined as 10 times the bit rate. It is reset whenever a data bit is received. Do not clear (0) this register if the stale character time-out interrupt is enabled. Note the discontinuity in the bit assignments.
6	SAMPLE_DATA	Setting (1) this bit enables the new sample data mode, which means that the start bit is sampled as well as the rest, when in sample data mode. See the CR register, CHANNEL_COMMAND bit for more information.
5	RESERVED	
4:0	STALE_TIMEOUT_LSB	This bitfield is the LSbits of the STALE_TIMEOUT bitfield.

0x1634001C GSBI4_UART_DM_TFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_TFWR register is the UART transmit FIFO watermark register.

GSBI4_UART_DM_TFWR

Bits	Name	Description
31:0	TFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the transmit FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of TX words in the FIFO) is less than or equal to the value in TFWR. See UART_DM_IMR register. Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x16340020 GSBI4_UART_DM_RFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RFWR register is the UART receive FIFO watermark register.

GSBI4_UART_DM_RFWR

Bits	Name	Description
31:0	RFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the receive FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of words in the RX FIFO) is greater than the value in RFWR. Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x16340024 GSBI4_UART_DM_HCR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI4_UART_DM_HCR

Bits	Name	Description
7:0	DATA	The UART_DM_HCR register is the UART hunt character register, which contains the character for which the receiver looks to assert a hunt character received interrupt.

0x16340034 GSBI4_UART_DM_DMRX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI4_UART_DM_DMRX

Bits	Name	Description
24:0	RX_DM_CRCI_CHARS	In the DM mode, the number of chars in the Rx FIFO that are used for CRCI handshake with the DM. The written value of RX_DM_CRCI_ CHARS must be a multiple of 16(bits [3:0] are treated as 0x0). After a value is written, the UART will generate CRCI requests as long as RX_DM_CRCI_CHARS is non zero. Read of DMRX register gives the number of characters that were received since the end of the last transfer. It is reset at the end of each Rx transfer Also is used by the software to indicate `transfer initialization'. See Software procedures.

0x16340038 GSBI4_UART_DM_IRDA

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IRDA register enables the IRDA function, selects a loopback, and allows inversion of RX and TX data. This register also controls the IRDA transceiver that optionally interfaces between the UART and the DP_RX_DATA and DP_TX_DATA pins.

The UART proper is a standard RX/TX configuration that converts the serial pin input and output lines to 8-bit data for the microprocessor. The configuration contains receive and transmit blocks, a control block, a bit rate generator for RX and TX, and FIFO interfaces with the microprocessor data bus. The IRDA register provides the means of switching IRDA circuits into the serial I/O lines and the IRDA function is normally switched out. The IRDA modulator/demodulator may be enabled or disabled under microprocessor control. When enabled, the RX and TX data pathis have individual inversion select bits, so external true or inverted drivers may be used in the signal path.

- The register is generated only when IRDA_IFC_GEN generic equals 1.

GSBI4_UART_DM_IRDA

Bits	Name	Description
4	MEDIUM_RATE_EN	Set (1) for 1/4 bit-time pulse length (Medium rate) Clear (0) for 3/16 bit-time pulse length (Low rate)
3	IRDA_LOOPBACK	This bit loops the IRDA modulated TX line back into the IRDA RX line. The normal UART loopback mode must be off in order to see this effect.
2	INVERT_IRDA_TX	This bit inverts the polarity of the IRDA modulated signal on the DP_TX_DATA pin. - Set (1) this bit for an inverted polarity. - Clear (0) this bit for a non-inverted polarity.

GSBI4_UART_DM_IRDA (cont.)

Bits	Name	Description
1	INVERT_IRDA_RX	This bit inverts the polarity of the IRDA received signal on the DP_RX_DATA pin. nSet (1) this bit for inverted the polarity. nClear (0) this bit for non-inverted polarity.
0	IRDA_EN	Set (1) this bit to enable the IRDA transceiver. Clear (0) this bit to bypass the IRDA transceiver and ignore the other bits of this register.

0x1634003C GSBI4_UART_DM_DMEN

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_DMEN register indicates if Data Mover is enabled for TX and RX channels.

GSBI4_UART_DM_DMEN

Bits	Name	Description
1	RX_DM_EN	Set (1) this bit to enable RX DM interface. Clear (0) this bit to disable RX DM interface. Clearing this bit requires resetting the receiver (see UART_DM_CR register).
0	TX_DM_EN	Set (1) this bit to enable TX DM interface. Clear (0) this bit to disable TX DM interface.

0x16340040 GSBI4_UART_DM_NO_CHARS_FOR_TX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI4_UART_DM_NO_CHARS_FOR_TX

Bits	Name	Description
23:0	TX_TOTAL_TRANS_LEN	The total number of characters for transmission. Before writing a new value, the TX FIFO must be empty (as indicated by TX_READY interrupt in IMR register or after a reset). It is used by the transmitter to calculate how many characters to transmit in the last word. In DM mode, it is also used for the CRCI mechanism. Any additional writes to the TX FIFO above TX_TOTAL_TRANS_LEN will be discarded. A TX_READY interrupt is triggered after TX_TOTAL_TRANS_LEN number of characters were moved from the TX FIFO to the unpacking register (not all may have been sent).

0x16340044 GSBI4_UART_DM_BADR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

GSBI4_UART_DM_BADR

Bits	Name	Description
31:2	RX_BASE_ADDR	RX FIFO base address. Both FIFOs use the same RAM (2^RAM_ADDR_WIDTH, 32-bit entries). This register controls the division of the memory to the RX and TX FIFOs. The division is a multiple of 4 entries, since the DM's burst length is 4. The size of the TX FIFO equals RX_BASE_ADDR. The size of the RX FIFO is 2^RAM_ADDR_WIDTH - RX_BASE_ADDR. ® The default is RX_BASE_ADDR = 2^(RAM_ADDR_WIDTH - 1) ® Only RAM_ADDR_WIDTH -1:2 bits are generated.
1:0	UNUSED	

0x16340048 GSBI4_UART_DM_TESTSL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI4_UART_DM_TESTSL

Bits	Name	Description
4	TEST_EN	Test bus enable
3:0	TEST_SEL	Test bus selector

0x16340060 GSBI4_UART_DM_MISR_MODE

Type: Read/Write
Clock: WR_CLK

GSBI4_UART_DM_MISR_MODE

Bits	Name	Description
31:2	RESERVED	unused.
1:0	MODE	0x0: Disabled 0x1: Enabled,TX test 0x2: Enabled, RX test

0x16340064 GSBI4_UART_DM_MISR_RESET

Type: Write
Clock: WR_CLK
Reset State: Undefined

GSBI4_UART_DM_MISR_RESET

Bits	Name	Description
31:1	RESERVED	unused.
0	RESET	

0x16340068 GSBI4_UART_DM_MISR_EXPORT

Type: Read/Write
Clock: WR_CLK
Reset State: Undefined

GSBI4_UART_DM_MISR_EXPORT

Bits	Name	Description
31:1	RESERVED	unused.
0	EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., what is the result of the muxing of all the input data streams with <BLOCK>_TEST_MODE) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x1634006C GSBI4_UART_DM_MISR_VAL

Type: Read
Clock: WR_CLK
Reset State: Undefined

GSBI4_UART_DM_MISR_VAL

Bits	Name	Description
9:0	VAL	Current MISR state

0x16340080 GSBI4_UART_DM_SIM_CFG

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_SIM_CFG register is used to configure the SIM interface for the UART.

- The register is generated only when SIM_GLUE_GEN generic equals 1.

GSBI4_UART_DM_SIM_CFG

Bits	Name	Description
17	UIM_TX_MODE	When this bit is set (1), the transmission portion of the SIM interface operates in block mode (T=1). When clear (0), the transmission portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.
16	UIM_RX_MODE	When this bit is set (1), the receive portion of the SIM interface operates in block mode (T=1). When clear (0), the receive portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.
15:8	SIM_STOP_BIT_LEN	In UIM_IF mode, this field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 1 to 254 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. ..... 11 111110: 254 bit times 0x1: 1 bit times 0x2: 2 bit times
7	SIM_CLK_ON	When this bit is set(1), the UIM_CLK is turned on at either the TD8 or TD4 frequency, as indicated by bit6(UIM_CLK_TD8_SEL). When this bit is cleared, the UIM_CLK is stopped either LOW or HIGH, as indicated by bit 5(UIM_CLK_STOP_HIGH).

GSBI4_UART_DM_SIM_CFG (cont.)

Bits	Name	Description
6	SIM_CLK_TD8_SEL	This bit selects the UIM_CLK frequency at which the UIM_CLK is turned on. 0x1: TD8 (the UIM_CLK runs at the TD8 frequency) 0x0: TD4 (the UIM_CLK runs at the TD4 frequency)
5	SIM_CLK_STOP_HIGH	This bit indicates at what point - high or low - the UIM_CLK will stop. 0x1: high 0x0: low
4	SIM_CLK_SEL	unused
3	MASK_RX	Setting (1) this bit masks off any 0 on the RX line, which prevents the receiver from seeing the START bit. Set (1) this bit if you do not want to receive the data you transmit.
2	SWAP_D	Setting (1) this bit causes the UIM_IF to swap the 8 data bits (making MSB into LSB, bit 6 into bit1, and so on) before it is read by the microprocessor.
1	INV_D	Set (1) this bit to cause the UIM_IF to invert the 8 data bit before it is read by the microprocessor.
0	SIM_SEL	Set (1) this bit to designate the UIM_IF mode of operation.

0x16340084 GSBI4_UART_DM_TEST_WR_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI4_UART_DM_TEST_WR_ADDR

Bits	Name	Description
31:0	TEST_WR_ADDR	RAM address at which to write the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x16340088 GSBI4_UART_DM_TEST_WR_DATA

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI4_UART_DM_TEST_WR_DATA

Bits	Name	Description
31:0	TEST_WR_DATA	The test data to be written to the RAM. Write to this register triggers the write to the RAM, to TEST_WR_ADDR address.

0x1634008C GSBI4_UART_DM_TEST_RD_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI4_UART_DM_TEST_RD_ADDR

Bits	Name	Description
31:0	TEST_RD_ADDR	RAM address from which to read the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

9.6.1.2 Read registers

NOTE The addresses of the read-only registers are mapped into the same addresses of the four write-only registers in the section above this one. They are: UART_DM_CSR, UART_DM_TF, UART_DM_CR, and UART_DM_IMR, respectively.

0x16340008 GSBI4_UART_DM_SR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_SR register is the UART status register. This register is used to obtain the current state of the UART subsystem. This register is updated asynchronously.

GSBI4_UART_DM_SR

Bits	Name	Description
8	RX_BREAK_START_LAST	When break start is detected, this bit is set (1). When break end was detected, this bit is reset (0).
7	HUNT_CHAR	When set (1), this bit indicates that the programmed character in the UART_DM_HCR register was received. If programmed, this condition causes the RXHUNT bit to be set (1) in the UART_DM_ISR register. This bit is cleared by issuing a reset error status command.
6	RX_BREAK	When set (1), this bit indicates that an all-zero character of the programmed length was received without a stop bit. If a break begins in the middle of a character, it is detected if the condition remains until the end of the next character time. Only one all zero character is written into the FIFO upon receiving the break. After the RX input returns high for at least half a bit time, then more characters are accepted by the receiver. Whenever the break condition starts or stops as defined above, the RXBREAK bit is set (1) in the UART_DM_ISR register. This bit is appended to the character in the receive FIFO.

GSBI4_UART_DM_SR (cont.)

Bits	Name	Description
5	PAR_FRAME_ERR	A parity error occurs if parity is programmed to be checked and an incoming character is received with incorrect parity. A framing error occurs when the RX input is low while the stop bit is being sampled. This bit is sampled in the middle of the first stop bit position, regardless of the programmed length of the stop bit. This error bit is appended to the character in the receive FIFO.
4	UART_OVERRUN	An overrun error occurs if one or more incoming characters are lost. This happens when the receive FIFO is full, the packing buffer is full and another character has been received in the shift register. The character in the receive shift register is lost. Upon overrun, this status bit remains high until cleared by a reset error status command.
3	TXEMT	This bit is set (1) when the transmitter under-runs. It is set after the transmission of the stop bit at the end of a character, if there are no characters waiting to be sent. It is reset when a character is written to the transmit FIFO.
2	TXRDY	This bit indicates that the transmit FIFO has space in it. It is reset when the FIFO becomes full and set when space becomes available again. Any characters that are written to the FIFO while this bit is low is lost.
1	RXFULL	This bit is set (1) when the receive FIFO becomes full. It is reset when the CPU reads a word.
0	RXRDY	This bit is set (1) when there is a word in the receive FIFO waiting to be read. It is reset when the last word currently stored in the FIFO is read.

0x16340070 GSBI4_UART_DM_RF

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RF register is the UART receive FIFO register, which is used to access the channel receive FIFO. In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM RX FIFO.

GSBI4_UART_DM_RF

Bits	Name	Description
31:0	UART_RF	This register returns the next value in the receive FIFO. After the read is completed, the FIFO read pointer is updated to make the next character available.

0x16340074 GSBI4_UART_DM_RF_2

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI4_UART_DM_RF_2

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x16340078 GSBI4_UART_DM_RF_3

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI4_UART_DM_RF_3

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x1634007C GSBI4_UART_DM_RF_4

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI4_UART_DM_RF_4

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x16340010 GSBI4_UART_DM_MISR

Type: Read
Clock: AHB_CLK
Reset State: 0x0

GSBI4_UART_DM_MISR

Bits	Name	Description
12:0	UART_MISR	The UART_DM_MISR register is the masked interrupt status register. A read from this register returns the "AND" of the UART_DM_ISR and the UART_DM_IMR registers. This register is updated asynchronously. This bit field is misr <= (isr(12 DOWNTO 7) AND imr(12 DOWNTO 7)) & '0' & (isr(5 DOWNTO 0) AND imr(5 DOWNTO 0)).

0x16340014 GSBI4_UART_DM_ISR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_ISR register is the UART interrupt status register. This register provides the current status of the possible interrupt conditions. If one of these bits is set (1), and the corresponding bit in the UART_DM_IMR register is set (1), an interrupt is generated (with the exception of bit 6, CURRENT_CTS - see the description of the UART_DM_IMR register). If the corresponding bit in the UART_DM_IMR register is clear (0), setting one of these bits has no effect on the UART interrupt request signal. This register is updated asynchronously.

GSBI4_UART_DM_ISR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	· See UART_DM_IMR on page 28-9
11	RXBREAK_END	· See UART_DM_IMR on page 28-9
10	RXBREAK_START	· See UART_DM_IMR on page 28-9
9	TX_DONE	· Bit 9 generated only when SIM_GLUE_GEN generic equals 1
8	TX_ERROR	· Bit 9 generated only when SIM_GLUE_GEN generic equals 1
7	TX_READY	See UART_DM_IMR on page 28-9, for descriptions of the UART_DM_ISR bits.
6	CURRENT_CTS	
5	DELTA_CTS	
4	RXLEV	
3	RXSTALE	
2	RXBREAK	
1	RXHUNT	
0	TXLEV	

0x16340038 GSBI4_UART_DM_RX_TOTAL_SNAP

Type: Read
Clock: AHB_CLK
Reset State: 0x0

GSBI4_UART_DM_RX_TOTAL_SNAP

Bits	Name	Description
23:0	RX_TOTAL_BYTES	'RX_TOTAL_SNAP register holds the number of characters received since the end of last Rx transfer. It is updated at the end of an Rx transfer (see Software procedures). Rx transfer ends when one of the conditions is met: · The number of characters which were received since the end of the previous transfer equals the value which was written to DMRX at "Transfer initialization". · A stale event occurred (flush operation already performed if was needed).

0x1634004C GSBI4_UART_DM_TXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI4_UART_DM_TXFS

Bits	Name	Description
31:14	TX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bitfield. · Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	TX_ASYNC_FIFO_STATE	TX asynchronous fifo status - number of characters in the TX asynchronous FIFO.
9:7	TX_BUFFER_STATE	TX unpacking buffer status - number of bytes in the unpacking buffer
6:0	TX_FIFO_STATE_LSB	TX FIFO status - number of words in the TX FIFO

0x16340050 GSBI4_UART_DM_RXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI4_UART_DM_RXFS

Bits	Name	Description
31:14	RX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bitfield. Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	RX_ASYNC_FIFO_STATE	RX asynchronous fifo status - number of characters in the RX asynchronous FIFO.
9:7	RX_BUFFER_STATE	RX packing buffer status - number of bytes in the packing buffer
6:0	RX_FIFO_STATE_LSB	The number of entries in the RX FIFO that have at least one valid character. It is incremented each time a word is moved from the packing register to the RX FIFO. It is decremented each time a word is read from the RX FIFO. **NOTE** The Uart does not keep track of non-valid characters in each word. (See Software procedures).

0x16340090 GSBI4_UART_DM_TEST_RD_DATA

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI4_UART_DM_TEST_RD_DATA

Bits	Name	Description
31:0	TEST_RD_DATA	Read from this register triggers the read from the RAM. The register will hold, after read access, data which is found at TEST_RD_ADDR address in the RAM.

9.7 GSBI4 QUP Registers (0x16380000 QUP4_BASE)

This section contains the GSBI4 QUP registers.

0x16380000 GSBI4_QUP_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

a. The contents of this register should only be changed when in the RESET_STATE (see the QUP_STATE register).

b. The value written to the QUP output FIFO, is shifted left toward the MSB before passing it to the mini-core as follows:

- N equals 8 or less - shift 24
- N equals 16 to 9 - shift 16
- N equals 24 to 17 - shift 8
- N equals 32 to 25 - no shift

The MINI_CORE clock selected is as follows:

Null: cc_qup_core_clk

SPI: cc_spi_master_clk

I2C: cc_I2C_clk		

GSBI4_QUP_CONFIG

Bits	Name	Description
31:14	RESERVED_1	reserved
13	CORE_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).
12	APP_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).

GSBI4_QUP_CONFIG (cont.)

Bits	Name	Description
11:8	MINI_CORE	value: 0000 Null core value: 0001 SPI core value: 0010 I2C master controller value: 0011 I2C slave controller value: 0100 Reserved (I2C master & slave for loop back operation) value: 0101 Reserved (map to null core) value: 0110 Reserved (map to null core value: 0111 Reserved (map to null core) See Note 1.
7	NO_INPUT	qup_data_in is not used and the value is a "don't care". The QUP input FIFO is always empty. The input service interrupt and INPUT_SERVICE_FLAG bit are never set. See notes (a) and (b) above.
6	NO_OUTPUT	qup_data_out is not used and is held at the value zero. The QUP output FIFO is always empty. The output service flag and OUTPUT_SERVICE_FLAG bit are never set. qup_data_out is still driven when SPI_CS _N is asserted. The setting for NO_TRI_STATE still applies. See notes (a) and (b) above.
5	RESERVED_2	Reserved.
4:0	N	Number of logical bits N in the mini-core that constitutes a single transfer. The value zero indicates N equals one. The value of all ones indicates N equals 32. The value in this register must be 3 (i.e., N is 4 or higher in order for the STATE field to be set to RUN_STATE). See note (a) above.

0x16380004 GSBI4_QUP_STATE

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b0000000000000000_00000000000XX100

GSBI4_QUP_STATE

Bits	Name	Description
31:5	RESERVED	reserved.
4	I2C_MAST_GEN	Read only. Reflects the RTL generic setting for GEN_I2C_MASTER_MINI_CORE.
3	SPI_GEN	Read only. Reflects the RTL generic setting for GEN_SPI_MINI_CORE.
2	STATE_VALID	Read only. If and only if set to one, writes to the STATE field is allowed or reads from the STATE field is valid. Writes to this bit is ignored.

GSBI4_QUP_STATE (cont.)

Bits	Name	Description
1:0	STATE	When clear (00), the mini-core and related logic is held in RESET_STATE. When set to "01", the mini-core and related logic is released from reset and enters the RUN_STATE. When set to "11", the mini-core and related logic enters the PAUSE_STATE at the next appropriate point in time. Writing (10) to this field clears these two bits. For PAUSE_STATE to RESET_STATE transition, two writes of (10) are required for the transition to complete. . See notes 1 and 2. Note 1: SPI - the "next appropriate point in time" is the next time SPI_CS _N de-asserts. If SPI_CS _N is not asserted when the PAUSE_STATE is entered, the SPI_CS _N is maintained in the not asserted state. The PAUSE_STATE is not available for SLAVE operation. Note 2: I2C -

0x16380008 GSBI4_QUP_IO_MODES

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b000000000000000_00000000XXXXXXXX

Unless otherwise stated, register bits written return the value when read.

Notes:

a. "Packing" occurs as follows:

- N equals 8 or less - pack four values into each QUP input FIFO word.
- N equals 16 to 9 - pack two values into each QUP input FIFO word.
- N equals 32 to 17 - no packing. Each mini-core value is moved to an QUP input FIFO word.

b. "Un-Packing" occurs as follows:

- N equals 8 or less - un-pack four values from each QUP output FIFO word.
- N equals 16 to 9 - un-pack two values from each QUP output FIFO word.
- N equals 32 to 17 - no packing. Each QUP output FIFO value is moved to the mini-core.

GSBI4_QUP_IO_MODES

Bits	Name	Description
31:17	RESERVED	reserved
16	OUTPUT_BIT_SHIFT_EN	If set, enables the QUP output FIFO block to do bit shifting on the output data.

GSBI4_QUP_IO_MODES (cont.)

Bits	Name	Description
15	PACK_EN	Indicates data values from the mini-core are to be packed before placement in the QUP input FIFO. See note (a) above.
14	UNPACK_EN	Indicates data values taken from the QUP output FIFO should be unpacked before passing to the mini-core. See note (b) above.
13:12	INPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_INPUT = 0, then only FIFO_Mode is available)
11:10	OUTPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_OUTPUT = 0, then only FIFO_Mode is available)
9:7	INPUT_FIFO_SIZE	Read only, actual value set by RTL generic. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 6x BLOCK_SIZE
6:5	INPUT_BLOCK_SIZE	Read only. Actual value set by RTL generic. Indicates the block size associated with Block_Mode and Data_Mover_Mode for input. Value 00: 4 Bytes (FIFO_Mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved
4:2	OUTPUT_FIFO_SIZE	Read only. Actual value set by RTL GENERIC. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 16 BLOCK_SIZE
1:0	OUTPUT_BLOCK_SIZE	Read only. Actual value set by RTL GENERIC. Value 00: 04 Bytes (FIFO mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved

0x1638000C GSBI4_QUP_SW_RESET

Type: Write/cmd
Clock: CRIF_CLK
Reset State: 0x0000

A write to this register resets the entire QUP core and all mini-cores. The internal registers are brought back to their reset values. Reading of this register returns zero.

GSBI4_QUP_SW_RESET

Bits	Name	Description
31:0	RESERVED	NA

0x16380010 GSBI4_QUP_TIME_OUT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies if the QUP_MX_OUTPUT_COUNT register and/or QUP_MX_INPUT_COUNT register are enabled. Additionally, this register only applies to Block_Mode and Data_Mover_Mode. The timer starts "ticking" when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The timer pauses for the PAUSE_STATE. If the timer expires before the QUP_MX_OUTPUT_COUNT and/or QUP_MX_INPUT_COUNT are exhausted, then the TIME_OUT_ERR flag is set in the QUP_ERROR_FLAGS register and the interrupt gsbi_qup_irq may be asserted.

GSBI4_QUP_TIME_OUT

Bits	Name	Description
15:0	TIME_OUT_VALUE	Specifies time out value in units of cc_qup_app clock ticks. A value of zero indicates the timer function is not enabled for use. See QUP_CONFIG register for information on clocks.

0x16380014 GSBI4_QUP_TIME_OUT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI4_QUP_TIME_OUT_CURRENT

Bits	Name	Description
31:0	TIME_OUT_CURRENT	Current value of time-out counter.

0x16380018 GSBI4_QUP_OPERATIONAL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0080

GSBI4_QUP_OPERATIONAL

Bits	Name	Description
31:10	RESERVED_1	reserved.
13	IN_BLOCK_READ_REQ	Read only. When set by hardware, indicates QUP input FIFO has BLOCK_SIZE_INPUT amount of data ready for reading. Valid only in Block_Mode.
12	OUT_BLOCK_WRITE_REQ	Read only. When set by hardware, indicates QUP output FIFO needs BLOCK_SIZE_OUTPUT amount of data to be written. Valid only in Block_Mode.
11	MAX_INPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP input FIFO has reached the programmed QUP_MX_INPUT_COUNT value. Valid in FIFO_Mode (only if MX_READ_COUNT is non-zero), Block_Mode and Data_Mover_Mode.
10	MAX_OUTPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP output FIFO has reached the programmed QUP_MX_OUTPUT_COUNT value. Valid in Block_Mode and Data_Mover_Mode.
9	INPUT_SERVICE_FLAG	When set by hardware, indicates QUP input FIFO has an outstanding input service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowleges software has or will read the data. Valid only in all modes.
8	OUTPUT_SERVICE_FLAG	When set by hardware, indicates QUP output FIFO has an outstanding output service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowledges software has or will read the data. Valid only in all modes.
7	INPUT_FIFO_FULL	Read only. When set, indicates the input FIFO is full and can accept no more data from the QUP mini-core.
6	OUTPUT_FIFO_FULL	Read only. When set, indicates the output FIFO is full and can accept no more CRIF writes.
5	INPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the input FIFO has at least one value in it to be read. When clear, indicates the input FIFO is empty.
4	OUTPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the output FIFO has at least one value in it to be shifted out. When clear, indicates the output FIFO is empty.
3:0	RESERVED_2	reserved.

0x1638001C GSBI4_QUP_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

GSBI4_QUP_ERROR_FLAGS

Bits	Name	Description
31:7	RESERVED_1	reserved.
6	TIME_OUT_ERR	The time out limit for a given transfer has been reached.
5	OUTPUT_OVER_RUN_ERR	Indicates the output FIFO was full when a CRIF write was attempted to the FIFO. The write is discarded.
4	INPUT_UNDER_RUN_ERR	Indicates the input FIFO was empty when a CRIF read was attempted to the FIFO. The read value returns is indeterminate.
3	OUTPUT_UNDER_RUN_ER R	Indicates the output FIFO was empty when an output shift operation required a value.
2	INPUT_OVER_RUN_ERR	Indicates the input FIFO was full when an input shift operation provided a new value. When this happens, the new value is discarded.
1:0	RESERVED_2	reserved

0x16380020 GSBI4_QUP_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x007C

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of gsbi_qup_irq and the setting of the corresponding error flag in the QUP_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

GSBI4_QUP_ERROR_FLAGS_EN

Bits	Name	Description
31:7	RESERVED_1	reserved
6	TIME_OUT_ERR_EN	If set, enables time out error generation.
5	OUTPUT_OVER_RUN_ERR _EN	If set, enables output over run error generation.

GSBI4_QUP_ERROR_FLAGS_EN (cont.)

Bits	Name	Description
4	INPUT_UNDER_RUN_ERR_EN	If set, enables input under run error generation.
3	OUTPUT_UNDER_RUN_ERR_EN	If set, enables output under run error generation.
2	INPUT_OVER_RUN_ERR_EN	If set, enables input over run error generation.
1:0	RESERVED_2	reserved

0x16380024 GSBI4_QUP_TEST_CTRL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register enables QUP test bus to be actively driven by QUP core signals.

GSBI4_QUP_TEST_CTRL

Bits	Name	Description
31:1	RESERVED	reserved
0	QUP_TEST_BUS_EN	If set, enables QUP core to actively drive test bus. If zero, the core drives the test bus to all zeros.

9.7.1 QUP output FIFO registers

0x16380100 GSBI4_QUP_MX_OUTPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each output transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not effect the count.

Notes:

a. Allows the total number of Mini Core transfers to be less than an exact multiple of OUTPUT_BLOCK_SIZE. Any additional outputs are discarded.

GSBI4_QUP_MX_OUTPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_COUNT	Number of writes of size N to the mini-core per RUN_STATE. A value of zero indicates the output count function is not enabled for use. See note (a) above.

0x16380104 GSBI4_QUP_MX_OUTPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI4_QUP_MX_OUTPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_CNT_CURRENT	Current value of QUP_MX_OUTPUT_COUNT.

0x16380108 GSBI4_QUP_OUTPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

This register holds the output data hanging out of the QUP output FIFO ready be loaded into the mini-core for the next load operation. This corresponds to signal qup_data_out going into the mini-core block.

GSBI4_QUP_OUTPUT_DEBUG

Bits	Name	Description
31:0	OUTPUT_DEBUG_DATA	Value waiting at the exit of output FIFO.

0x1638010C GSBI4_QUP_OUTPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the output FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the

value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

GSBI4_QUP_OUTPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	OUTPUT_FIFO_WORD_CNT	Number of words in the output FIFO.

0x16380110+4*c GSBI4_QUP_OUTPUT_FIFOc, c=[0..15]

Type: Write
Clock: CRIF_CLK
Reset State: 0x0000

Note that consecutive writes to this address keeps filling up the output FIFO. The max address to address the output FIFO is 0x14C.

GSBI4_QUP_OUTPUT_FIFOc

Bits	Name	Description
31:0	OUTPUT	Value to be shifted out.

0x16380150 GSBI4_QUP_MX_WRITE_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_OUTPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the gsbi_qup_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_OUTPUT_COUNT register case, the SW should not program the QUP_MX_WRITE_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_OUTPUT * FIFO_SIZE_OUTPUT).

GSBI4_QUP_MX_WRITE_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_COUNT	The number of "writes" of size N. This is used only if the core is in FIFO_Mode.

0x16380154 GSBI4_QUP_MX_WRITE_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI4_QUP_MX_WRITE_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_CNT_CURRENT	Current value of QUP_MX_WRITE_COUNT counter.

9.7.2 QUP input FIFO registers

0x16380200 GSBI4_QUP_MX_INPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each input transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not affect the count.

Notes:

a. Allows the number of shift register transfers to be less than an exact multiple of INPUT_BLOCK_SIZE. When count reached, remainder of INPUT_BLOCK_SIZE is filled with zeroes.

GSBI4_QUP_MX_INPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_COUNT	Number of reads of size N from the mini-core per RUN_STATE. A value of zero indicates the input count function is not enabled for use. See note (a) above.

0x16380204 GSBI4_QUP_MX_INPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI4_QUP_MX_INPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_CNT_CURRENT	Current value of QUP_MX_INPUT_COUNT.

0x16380208 GSBI4_QUP_MX_READ_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_INPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the qup_input_service_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_INPUT_COUNT register case, the SW should not program the QUP_MX_READ_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_INPUT * FIFO_SIZE_INPUT). If the SPI mini-core and slave operation is enabled, then an InputOverRun error will result.

GSBI4_QUP_MX_READ_COUNT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_COUNT	The number of "reads" of size N. This is used only if the core is in FIFO_Mode.

0x1638020C GSBI4_QUP_MX_READ_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI4_QUP_MX_READ_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_CNT_CURRENT	Current value of QUP_MX_READ_COUNT counter.

0x16380210 GSBI4_QUP_INPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the value of the last loaded in known-good-data into the QUP input FIFO. May be different from what the actual read of input FIFO will return because of packing enabled at the input side. This corresponds to signal qup_data_in coming from the mini-core block synchronized to the crif_clk.

GSBI4_QUP_INPUT_DEBUG

Bits	Name	Description
31:0	INPUT_DEBUG_DATA	Last known good value shifted into the input FIFO.

0x16380214 GSBI4_QUP_INPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the input FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

GSBI4_QUP_INPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	INPUT_FIFO_WORD_CNT	Number of words in the input FIFO.

0x16380218+4*c GSBI4_QUP_INPUT_FIFOc, c=[0..15]

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

Consecutive reads to this address reads the input FIFO contents on a FIFO basis.The max address to read the input FIFO is 0x254.

GSBI4_QUP_INPUT_FIFOc

Bits	Name	Description
31:0	INPUT	Value shifted in.

9.7.3 SPI mini-core registers

0x16380300 GSBI4_SPI_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register. Both NO_OUTPUT and NO_INPUT set to zero provides default full duplex operation. Setting both these bits to one is not a legal operational state.

GSBI4_SPI_CONFIG

Bits	Name	Description
31:11	RESERVED_1	Reserved.
10	HS_MODE	When set, SPI HS_MODE is enabled. When clear, SPI HS_MODE is disabled.
9	INPUT_FIRST	When set, INPUT FIRST SPI protocol is used. When clear, OUTPUT FIRST SPI protocol is used.
8	LOOP_BACK	Loopback is only valid in non-HS mode. Always clear for normal operation. If set, loop back on SPI_DATA_MO_SI under MASTER operation or SPI_DATA_MI_SO under SLAVE operation.
7:6	RESERVED_2	Reserved.
5	SLAVE_OPERATION	This register is writable only when the hardware signal spi_slave_en is asserted. When set, the SPI is configured for SLAVE operation. Zero indicates MASTER operation.
4:0	RESERVED	Reserved.

0x16380304 GSBI4_SPI_IO_CONTROL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register.

Unless otherwise stated, register bits written return the value when read.

GSBI4_SPI_IO_CONTROL

Bits	Name	Description
31:11	RESERVED	Reserved.
10	CLK_IDLE_HIGH	Use SPI_CLK_IDLE_HIGH when set.
9	CLK_ALWAYS_ON	When MASTER operation is used, run SPI_CLK during IDLE.
8	MX_CS_MODE	If this bit is set, then for a given RUN state, the associated chip select will be asserted for the first N-bit transfer and will be kept asserted till the last programmed transfer. Applies only in MASTER mode. The number of transfers is determined by SPI_MX_OUTPUT_COUNT and/or SPI_MX_INPUT_COUNT registers.
7:4	CS_N_POLARITY	These four bits control the polarity of four SPI_CS _N respectively. Setting any of this bit to '1', makes the associated SPI_CS _N active HIGH. This field is a "don't care" in SLAVE operation.
3:2	CS_SELECT	When MASTER operation is used, controls the assertion of SPI_CS_ N pins. Selects SPI_CS_N if 00, SPI_CS1_N if 01, SPI_CS2_N if 10, or SPI_CS3_N if 11. The deselected ChipSelects will be driven to inactive state dictated by the field CS_N_POLARITY. This field is a "don't care" in SLAVE operation.
1	TRISTATE_CS	When set, drives Z on all SPI_CS _N lines. When clear, enables normal functionality on these lines. This bit can be used to support deployment of the core as one of the masters in a multi-master configuration.
0	NO_TRI_STATE	When set, spi_data_out is not taken tri-state when SPI_CS _N is de-asserted. This bit is normally set for MASTER operation but may be optionally left cleared.

0x16380308 GSBI4_SPI_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

GSBI4_SPI_ERROR_FLAGS

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.

GSBI4_SPI_ERROR_FLAGS (cont.)

Bits	Name	Description
1	SPI_SLV_CLK_OVER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was greater than the programmed value of N. When this happens, only the first N bits are passed to the SPI input FIFO and the output shift value is held at zero.
0	SPI_SLV_CLK_UNDER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was less than the programmed value of N. When this occurs, the bits which were received are passed to the SPI input FIFO and the CURRENT output bit is forced to zero.

0x1638030C GSBI4_SPI_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0003

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of spi_error_irq and the setting of the corresponding error flag in the SPI_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

GSBI4_SPI_ERROR_FLAGS_EN

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.
1	SPI_SLV_CLK_OVER_RUN_ERR_EN	If set, enables clock over run error generation.
0	SPI_SLV_CLK_UNDER_RUN_ERR_EN	If set, enables clock under run error generation.

0x16380310 GSBI4_SPI_DEASSERT_WAIT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the de-assertion wait time of SPI_CS _N between consecutive N-bit transfers in MASTER operation. The wait time is specified in number of cycles of cc_spi_master_clk.

GSBI4_SPI_DEASSERT_WAIT

Bits	Name	Description
31:6	RESERVED	Reserved.

GSBI4_SPI_DEASSERT_WAIT (cont.)

Bits	Name	Description
5:0	DEASSERT_WAIT	Number cc_spi_master_clk ticks associated with the de-asserted time of SPI_CS _N. Only applies to MASTER operation. For SLAVE operation, this field is a "don't care". A value of zero indicates SPI_CS _N remains de-asserted for exactly one clock tick. A value of one, indicates two ticks, etc. All ones indicates 64 ticks.

9.7.4 I2C master mini-core registers

0x16380400 GSBI4_I2C_MASTER_CLK_CTL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_CLK_CTL register is a read/write register that controls clock divider values. This register should only be written to after it is confirmed that the I2C master mini-core is not longer in RESET state (QUP_STATE register).

GSBI4_I2C_MASTER_CLK_CTL

Bits	Name	Description
31:11	RESERVED	Reserved.
10:8	HS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in high-speed (HS) mode. The minimum value should be 3 hex (4 I2C_clk clocks per period) to ensure proper sampling of the bus. For a maximum high speed bit rate of 3.4 Mb/s (high speed mode), this would require a minimum 40.8 MHz I2C_clk clock. The maximum I2C_clk is 81.6 MHz. This register is reset to a maximum value of 7 hex. I2C_HS_CLK = I2C_CLK/(3*(HS_DIVIDER_VALUE+1)
7:0	FS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in fast/standard (FS) mode. The minimum value should be 3 hex to ensure proper sampling of the bus. For a maximum bit rate of 400 kb/s (fast mode), this would require a 4.8 MHz I2C_clk clock. For a maximum bit rate of 100 kb/s (standard mode), this would require a 1.2 MHz I2C_clk clock. Maximum I2C_clk for fast and standard modes are 206.4 MHz and 51.6 MHz respectively. This register is reset to a maximum value of 255 hex. I2C_FS_CLK = I2C_CLK/(2*(FS_DIVIDER_VALUE+3)

0x16380404 GSBI4_I2C_MASTER_STATUS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_STATUS is a status register. Writing a one clears the status bits.

GSBI4_I2C_MASTER_STATUS

Bits	Name	Description
31:26	RESERVED_1	Reserved.
25	INVALID_READ_SEQ	This bit is set (1) when a MI_REC tag does not follow a START tag for an I2C READ. Not applicable for Halcyon.
24	INVALID_READ_ADDR	This bit is set (1) when the I2C controller is trying to receive data from a non-existent I2C slave (address).
23	INVALID_TAG	This bit is set (1) when the I2C controller is trying to process data from the output FIFO that is improperly tagged.
22:20	INPUT_FSM_STATE	This 3-bit field informs the microprocessor of the state of the I2C MASTER INPUT FSM block. Reset, read_last_byte, mi_rec, dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: READ_LAST_BYTE_STATE Value 0x3: MI_REC_STATE Value 0x4: DEC_STATE Value 0x5: STORE_STATE
19:16	OUTPUT_FSM_STATE	This 4-bit field informs the microprocessor of the state of the I2C MASTER OUTPUT FSM block. Reset, decode, send, mi_red, nop, nop_dec, invalid, invalid_dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: DECODE_STATE Value 0x3: SEND_STATE Value 0x4: MI_REC_STATE Value 0x5: NOP_STATE Value 0x6: INVALID_STATE Value 0x7: PEEK_STATE Value 0x8: SEND_R_STATE

GSBI4_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
15:13	CLK_STATE	This 3-bit field informs the microprocessor of the state of the I2C clk_control block. Reset_busidle, not_master, high, low, high_wait, forced_low, hs_addr_low or double_buffer_wait. Value 0x0: RESET_BUSIDLE_STATE Value 0x1: NOT_MASTER_STATE Value 0x2: HIGH_STATE Value 0x3: LOW_STATE Value 0x4: HIGH_WAIT_STATE Value 0x5: FORCED_LOW_STATE Value 0x6: HS_ADDR_LOW_STATE Value 0x7: DOUBLE_BUFFER_WAIT_STATE
12:10	DATA_STATE	This 3-bit field informs the microprocessor of the state of the I2C data_control block. Reset, Tx addr, Tx HS addr, Tx 10-bit addr, Tx 2nd 10-bit addr byte, Tx data and Rx data. Value 0x0: RESET_WAIT_STATE Value 0x1: TX_ADDR_STATE Value 0x2: TX_DATA_STATE Value 0x3: TX_HS_ADDR_STATE Value 0x4: TX_10_BIT_ADDR_STATE Value 0x5: TX_2ND_BYTE_STATE Value 0x6: RX_DATA_STATE
9	BUS_MASTER	This bit is set (1) when the I2C controller is the present bus master.
8	BUS_ACTIVE	This bit is set (1) when the bus is in use by this, or any other controller.
7:6	FAILED	This 2-bit field contains the failure information of the present I2C transfers. If transmitting, failed[1] contains the information regarding the byte that has been transmitted. Failed[0] contains the information of the byte awaiting transmission if there is a byte pipelined. If no byte is pipelined, ignore this bit. If receiving, failed[1] contains the information of the byte received and stored in the buffer, and failed[0] should be ignored. For example: Value 00: Byte n transmitted successfully, byte n+1 to begin transmission Value 01: Byte n transmitted successfully, byte n+1 errored: type of error indicated in other STATUS bits. (queued invalid write, for example) Value 10: Byte n errored: type of error indicated in other STATUS bits, byte n+1 to begin transmission (byte n+1 would have to be a valid address byte for this condition to occur) Value 11: Byte n errored: type of error indicated in other STATUS bits, byte n+1 discarded as well (if the byte was a data byte destined for a NACKed address, data is useless, therefore discarded)
5	INVALID_WRITE	This bit is set (1) when software writes data to the I2C_DATA register that should be flagged as an address but is not.

GSBI4_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
4	ARB_LOST	This bit is set (1) when the controller loses arbitration for the bus. If this bit gets set (1) during the transmission, all data has been lost, and the microprocessor must re-request its transmission.
3	PACKET_NACKED	This bit is set high when a NACK is received from a slave. If a high speed master code is sent and there is an ACK from a slave, then this bit is set (1) to indicate that the high speed mode can not be entered. If the high speed mode is accepted by the slave, then a NACK is performed and this bit is not set (1).
2	BUS_ERROR	This bit is set (1) when an unexpected START or STOP condition is detected. This returns the controller to its reset state.
1:0	RESERVED_2	Reserved.

9.8 GSBI5 Registers (0x1A200000 GSBI5_BASE)

This section contains the GSBI5 registers.

9.8.1 GSBI CTRL Registers

0x1A200000 GSBI5_GSBI_CTRL_REG

Type: Read/write
Clock: HCLK
Reset State: 0x00000000

GSBI5_GSBI_CTRL_REG

Bits	Name	Description
15:12	RESERVED	reserved
11:8	WRAPPER_CTRL	This field has no predefined use. When a wrapper is constructed around one or more GSBIs there may be a need to configure it. E.g., to select which of several GSBIs will be connected to a particular I2S block. All bits of this field emerge from GSBI as output ports which can be used for any such configuration task.
7	RESERVED_7	Reserved. The host can write and read this field, but its state has no effect on anything.
6:4	PROTOCOL_CODE	This field controls which protocol, if any, is applied to the GSBI's four I/O ports. Most codes assign a single protocol, but codes of "001" and "110" assigns I2C to two of the ports and UART (without flow control signals) or SIM to the other two. 0x0: Idle (null values are applied to all four GSBI I/Os) 0x1: I2C on 2 ports, SIM/R-UIM on other 2 0x2: I2C 0x3: SPI 0x4: UART with flow control (or IRDA) 0x5: SIM/R-UIM 0x6: I2C on 2 ports, UART (without HS flow ctrl on other 2) 0x7: Undefined
3:1	RESERVED_3_1	Reserved. The host can write and read this field, but its state has no effect on anything.
0	CRCI_MUX_CTRL	While this bit is low QUP CRCI ports are connected to the GSBI ports nominally for QUP and UART_DM CRCI ports are connected to the GSBI ports nominally for UART_DM. While this bit is high QUP CRCI ports are connected to the GSBI ports nominally for UART_DM and UART_DM CRCI ports are connected to nothing.

0x1A200004 GSBI5_GSBI_DBG0_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI5_GSBI_DBG0_REG

Bits	Name	Description
1:0	GSBI_PLAY0	This field has no function beyond the fact that the ARM can write to it and read from it.

0x1A200008 GSBI5_GSBI_DBG1_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI5_GSBI_DBG1_REG

Bits	Name	Description
1:0	GSBI_PLAY1	This field has no function beyond the fact that the ARM can write to it and read from it.

0x1A20000C GSBI5_GSBI_DBG2_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI5_GSBI_DBG2_REG

Bits	Name	Description
1:0	GSBI_PLAY2	This field has no function beyond the fact that the ARM can write to it and read from it.

0x1A200010 GSBI5_GSBI_DBG3_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI5_GSBI_DBG3_REG

Bits	Name	Description
1:0	GSBI_PLAY3	This field has no function beyond the fact that the ARM can write to it and read from it.

9.9 GSBI5 UART DM Registers (0x1A240000 GSBI5_UART_DM_BASE)

This section contains the GSBI5 UART DM registers.

9.9.1 Write and read/write registers

0x1A240000 GSBI5_UART_DM_MR1

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_MR1 register is the UART mode register 1. It is used, along with UART_DM_MR2, to configure the operational mode of the UART.

GSBI5_UART_DM_MR1

Bits	Name	Description
31:8	AUTO_RFR_LEVEL1	These bits are used, along with bits 5:0 (AUTO_RFR_LEVEL0) to program the level in the receive FIFO at which the RFR_N signal is de-asserted, if programmed to do so (see RX_RDY_CTL field of this register). The level counts the number of words inside the RX FIFO. It doesn't count the character that is being received (shift register) or characters in the packing buffer. This value is programmed from 1 to 2^RAM_ADDR_WIDTH. The RFR_N signal is de-asserted when the RX FIFO level (the number of characters remaining in the RX FIFO) is greater than the level that is programmed into this register. · Only RAM_ADDR_WIDTH +1:8 bits are generated.
7	RX_RDY_CTL	Setting (1) this bit enables the automatic ready-for-receiving (RFR_N) control for the receiver. RFR_N is turned off, or set (1), when a valid start bit is received and the channel FIFO is at the level programmed in bits 4 through 0 of this mode register. When the FIFO level falls back to the programmed level, the RFR_N signal is turned on, or clear (0). When this feature is off, the RFR_N signal can be used by normal signal port bit manipulation (see UART_DM_CR register).
6	CTS_CTL	When this bit is set(1), the transmitter checks the CTS_N input to determine whether to begin transmission of a new character. If CTS_N is low, the character is sent. Otherwise the transmitter continues marking until CTS_N goes low, then the next character is transmitted. A change on CTS_N during the transmission of a character has no effect on that character. When this bit is clear(0), the CTS_N input for the channel has no effect on the transmitter.
5:0	AUTO_RFR_LEVEL0	See the description of bit 8 (AUTO_RFR_LEVEL1).

0x1A240004 GSBI5_UART_DM_MR2

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI5_UART_DM_MR2

Bits	Name	Description
9	RX_ERROR_CHAR_OFF	When this bit is asserted, characters with parity or framing errors don't enter RX FIFO. Otherwise they enter RX FIFO.
8	RX_BREAK_ZERO_CHAR_OFF	When this bit is asserted, the zero character received at rx_break doesn't enter RX FIFO. Otherwise it enters RX FIFO.
7	LOOPBACK	Internal use only
6	ERROR_MODE	This bit controls the operation of the two FIFO status bits for the channel (parity or framing error and received break). · When clear (0), the UART operates in character mode and the status bits apply only to the character at the top of the FIFO. · When set (1), the UART operates in block mode and both bits are the "OR" of the status for all previously received characters arriving after the last `reset error status' command was issued (see CR register).
5:4	BITS_PER_CHAR	These bits determine how many bits are transmitted or received per character, not including the start, stop, and parity bits. 0x0: 5 bits 0x1: 6 bits 0x2: 7 bits 0x3: 8 bits
3:2	STOP_BIT_LEN	This field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 9/16, 1, 1+ 9/16, and 2 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. 0x0: 0.563 (9/16 bit times) 0x1: 1.000 bit time 0x2: 1.563 (1+9/16 bit times) 0x3: 2.000 bit times
1:0	PARITY_MODE	These bits determine which parity mode is used. The user can select between odd, even, space, or no parity. 0x0: no parity 0x1: odd parity 0x2: even parity 0x3: space parity

0x1A240008 GSBI5_UART_DM_CSR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_CSR register is the UART clock selection register. This register is used in conjunction with the UART M/N counter registers to determine the bit rate for the transmitter and receiver. The transmitter and receiver can be clocked at different rates.

The rates below are based on a uart_dm_clk rate of 1.8432 MHz (115.2 * 16).

Table 9-8 lists the hexadecimal values for the clock select field and the corresponding data rates.

Table 9-8 Hexadecimal values and data rates for clock select field

CLK SEL value	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Bit rate (b/sec)	75	150	300	600	1200	2400	3600	4800	7200	9600	14.4k	19.2k	28.8k	38.4k	57.6k	115.2k

GSBI5_UART_DM_CSR

Bits	Name	Description
7:4	UART_RX_CLK_SEL	Use the CLK SEL values to select the appropriate receive and transmit bit rates.
3:0	UART_TX_CLK_SEL	

0x1A240070 GSBI5_UART_DM_TF

Type: Write
Clock: AHB_CLK
Reset State: Undefined

In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM TX FIFO.

GSBI5_UART_DM_TF

Bits	Name	Description
31:0	UART_TF	The UART_TF register is the UART transmit FIFO register. This register is used to access the channel transmit FIFO. If the FIFO is full at the time of writing, the character is lost and an interrupt is generated (see UART_DM_IMR register).

0x1A240074 GSBI5_UART_DM_TF_2

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI5_UART_DM_TF_2

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x1A240078 GSBI5_UART_DM_TF_3

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI5_UART_DM_TF_3

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x1A24007C GSBI5_UART_DM_TF_4

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI5_UART_DM_TF_4

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x1A240010 GSBI5_UART_DM_CR

Type: Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_CR register is the UART command register. This register is used to issue specific commands to the UART subsystem. This register is updated asynchronously.

CAUTION Do not reset the transmitter and disable it at the same time. Do not reset the receiver and disable it at the same time.

Table 9-9 UART DM commands

Value	Description	Result
0	Null command	Does nothing.
1	Reset receiver	Resets the receiver as if a hardware reset were issued. The receiver is disabled and the FIFO, packing buffer and shift registers are flushed.
2	Reset transmitter	Resets the transmitter as if a hardware reset were issued. The transmitter signal goes high (marking) and the FIFO, unpacking register and shift register are flushed.
3	Reset error status	Clears the overrun error and hunt char received status bits in both the character and block error modes. In the block error mode, it clears the error status and received break.
4	Reset break change interrupt	Clears the break change interrupt status bit.
5	Start break	Forces the transmitter signal low. The transmitter must be enabled. If the transmitter is busy, the break is started when all characters in the transmit FIFO and the transmit shift register have been completely sent.
6	Stop break	If executed while channel is breaking, this command causes the transmitter signal to go high. The signal remains high for at least one bit time before sending out a new character.
7	Reset CTS_N	Clears ISR bit 5.
8	Reset stale interrupt	Clears the stale interrupt.
9	Packet mode	Turns on the sample data mode, which causes the receiver to sample the receive data stream at 16 times the programmed baud rate. The data is sampled with the start of the start bit, or the first data bit, and continued until the marking state. To exit this state, write 1100 in the command field.
A	test_parity_on	Internal use only.
B	test_frame_on	Internal use only.
C	Mode reset	Turns off the sample data mode.
D	Set RFR_N	Asserts the ready for receiving signal (active low).
E	Reset RFR_N	De-asserts the ready for receiving signal.
F	uart_reset_int	Internal use only.
10	Reset TX_ERROR	Clears TX_ERROR
11	Clear TX_DONE	Clears the TX_DONE interrupt (ISR bit 9)
12	Reset break start interrupt	Clears the break start interrupt status bit.
13	Reset break end interrupt	Clears the break end interrupt status bit.
14	Reset par_frame_err interrupt	Clears the par_frame_err interrupt status bit.

Table 9-10 UART DM commands

Value	Description	Result
0	Null command	Does nothing.
1	CR Protection Enable	Enables CR HW protection. When two consecutive writes to the CR are detected, the second write is delayed until the command of the first write is finished. The delay is done by de-asserting the AHB ready and this ensures that the first command completes and the second one will be executed right afterward.
2	CR Protection Disable	Disables CR HW protection. SW is responsible for managing delay between writes to the CR register.
3	Reset TX-Ready interrupt	Clears the TX_READY interrupt.
5	Enable Stale Event	Enables the `stale event' mechanism. See Software Procedures.
6	Disable Stale Event	Disables the `stale event' mechanism. See Software Procedures.
4	SW Force Stale	Causes a `stale event' (even if `stale event' is disabled). See Software Procedures.
7	RESERVED	

GSBI5_UART_DM_CR

Bits	Name	Description
11	CHANNEL_COMMAND_MSB	This is the msb of the CHANNEL_COMMAND bitfield.
10:8	GENERAL_COMMAND	Writing the appropriate value to these bits executes the commands that are listed in the table.
7:4	CHANNEL_COMMAND_LSB	Writing the appropriate value to these bits, along with bit 11, executes the commands that are listed in the table.
3	UART_TX_DISABLE	This command terminates the operation of the transmitter after any character in the transmit shift register is sent.
2	UART_TX_EN	This command enables the operation of the transmitter.
1	UART_RX_DISABLE	This command immediately terminates the operation of the channel receiver and any incoming characters are lost. None of the receiver status bits are affected by this command and characters that are already in the receive FIFO remain there.
0	UART_RX_EN	This command enables the channel receiver.

0x1A240014 GSBI5_UART_DM_IMR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IMR register is the UART interrupt mask register. This register is used to enable the corresponding functions in the UART_DM_ISR register. Setting (1) a bit in the UART_DM_IMR register causes an interrupt to be generated, if the corresponding bit in the UART_DM_ISR register is set. Clearing (0) a bit in the UART_DM_IMR register causes the setting of the corresponding bit in the UART_DM_ISR register to have no effect on the interrupt signal.

Bit 6 of the UART_DM_IMR register, CURRENT_CTS, is slightly different. If the current value of the CTS is one (1), no interrupt is generated. However, the user can use bit 6 in this register to mask the CTS value when reading the UART_DM_MISR register or as a general-purpose bit.

GSBI5_UART_DM_IMR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	This bit is asserted in the same condition at which PAR_FRAME_ERR status bit is asserted. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x14.
11	RXBREAK_END	This bit is set (1) if the end of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x13.
10	RXBREAK_START	This bit is set (1) if the start of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x12.
9	TX_DONE	This bit is used only in UIM/SIM_IF mode. Set (1) this bit when the last byte in the transmitter has been sent. · This bit is generated only when SIM_GLUE_GEN generic equals 1.
8	TX_ERROR	Only used in UIM_IF mode. Set (1) this bit to indicate that there has been parity error during transmission. To clear the detection logic associated with this function, write CR[11;7:4]=0x10. · This bit is generated only when SIM_GLUE_GEN generic equals 1.
7	TX_READY	This bit, when set(1), indicates that: 1. TX FIFO is empty. 2. The value written in NO_CHARS_FOR_TX register equals the number of bytes written to the TX FIFO since the register was updated. **NOTE** There may be characters in the unpack buffer or in the shift register. This bit is cleared by issuing `clear TX ready' command (see UART_DM_CR register).

GSBI5_UART_DM_IMR (cont.)

Bits	Name	Description
6	CURRENT_CTS	This bit indicates the current state of the CTS input. It never generates an interrupt.
5	DELTA_CTS	This bit, when set (1), indicates that the CTS input has changed states. To clear the detection logic associated with this function, write CR[7:4]=0x7.
4	RXLEV	This bit is set when a character is loaded into the receive FIFO that brings the total number of characters in the FIFO above the programmed watermark level in the FIFO watermark register (RFWR). This bit is cleared after enough characters have been read to bring the level equal to or below the programmed watermark level.
3	RXSTALE	This bit indicates that a `stale event' occurred. See Software procedures for the exact timing of this interrupt. It is cleared by issuing a reset-stale command (see CR register).
2	RXBREAK_CHANGE	This bit is set (1) if the start or end of a break condition is detected. The logic associated with this condition is cleared (0) by writing CR[7:4]=0x4. A detected break is defined as an all-zeros character with an invalid stop bit AND LOW PARITY. The end of a break is defined as a mark condition (1) at least 1/2 bit width. A detected break occupies one position in the Rx FIFO.
1	RXHUNT	This bit is set (1) when an incoming character matches the value programmed into the UART_DM_HCR register. This condition is cleared (0) by issuing a reset error status command (CR[7:4]=0x3).
0	TXLEV	This bit is set (1) when a character which is transferred from the transmit FIFO to the transmit shift register brings the total number of characters in the FIFO below or equal to the programmed watermark level in the UART_DM_TFWR register. This bit is cleared (0) after enough characters have been written to the FIFO to bring the level above the programmed watermark level.

0x1A240018 GSBI5_UART_DM_IPR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0xffffff9f

The UART_DM_IPR register is the UART interrupt programming register.

GSBI5_UART_DM_IPR

Bits	Name	Description
31:7	STALE_TIMEOUT_MSB	These bits are the STALE_TIMEOUT bitfield. The stale character time-out duration field contains a number from 1 to 2^30 -1. This number determines how many character times must elapse before a `stale event' is generated. This character time is defined as 10 times the bit rate. It is reset whenever a data bit is received. Do not clear (0) this register if the stale character time-out interrupt is enabled. Note the discontinuity in the bit assignments.
6	SAMPLE_DATA	Setting (1) this bit enables the new sample data mode, which means that the start bit is sampled as well as the rest, when in sample data mode. See the CR register, CHANNEL_COMMAND bit for more information.
5	RESERVED	
4:0	STALE_TIMEOUT_LSB	This bitfield is the LSbits of the STALE_TIMEOUT bitfield.

0x1A24001C GSBI5_UART_DM_TFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_TFWR register is the UART transmit FIFO watermark register.

GSBI5_UART_DM_TFWR

Bits	Name	Description
31:0	TFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the transmit FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of TX words in the FIFO) is less than or equal to the value in TFWR. See UART_DM_IMR register. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x1A240020 GSBI5_UART_DM_RFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RFWR register is the UART receive FIFO watermark register.

GSBI5_UART_DM_RFWR

Bits	Name	Description
31:0	RFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the receive FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of words in the RX FIFO) is greater than the value in RFWR. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x1A240024 GSBI5_UART_DM_HCR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI5_UART_DM_HCR

Bits	Name	Description
7:0	DATA	The UART_DM_HCR register is the UART hunt character register, which contains the character for which the receiver looks to assert a hunt character received interrupt.

0x1A240034 GSBI5_UART_DM_DMRX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI5_UART_DM_DMRX

Bits	Name	Description
24:0	RX_DM_CRCI_CHARS	In the DM mode, the number of chars in the Rx FIFO that are used for CRCI handshake with the DM. The written value of RX_DM_CRCI_ CHARS must be a multiple of 16(bits [3:0] are treated as 0x0). After a value is written, the UART will generate CRCI requests as long as RX_DM_CRCI_CHARS is non zero. Read of DMRX register gives the number of characters that were received since the end of the last transfer. It is reset at the end of each Rx transfer Also is used by the software to indicate `transfer initialization'. See Software procedures.

0x1A240038 GSBI5_UART_DM_IRDA

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IRDA register enables the IRDA function, selects a loopback, and allows inversion of RX and TX data. This register also controls the IRDA transceiver that optionally interfaces between the UART and the DP_RX_DATA and DP_TX_DATA pins.

The UART proper is a standard RX/TX configuration that converts the serial pin input and output lines to 8-bit data for the microprocessor. The configuration contains receive and transmit blocks, a control block, a bit rate generator for RX and TX, and FIFO interfaces with the microprocessor data bus. The IRDA register provides the means of switching IRDA circuits into the serial I/O lines and the IRDA function is normally switched out. The IRDA modulator/demodulator may be enabled or disabled under microprocessor control. When enabled, the RX and TX data pathis have individual inversion select bits, so external true or inverted drivers may be used in the signal path.

n The register is generated only when IRDA_IFC_GEN generic equals 1.

GSBI5_UART_DM_IRDA

Bits	Name	Description
4	MEDIUM_RATE_EN	· Set (1) for 1/4 bit-time pulse length (Medium rate) · Clear (0) for 3/16 bit-time pulse length (Low rate)
3	IRDA_LOOPBACK	· This bit loops the IRDA modulated TX line back into the IRDA RX line. The normal UART loopback mode must be off in order to see this effect.
2	INVERT_IRDA_TX	This bit inverts the polarity of the IRDA modulated signal on the DP_TX_DATA pin. · Set (1) this bit for an inverted polarity. · Clear (0) this bit for a non-inverted polarity.
1	INVERT_IRDA_RX	This bit inverts the polarity of the IRDA received signal on the DP_RX_DATA pin. · Set (1) this bit for inverted the polarity. · Clear (0) this bit for non-inverted polarity.
0	IRDA_EN	· Set (1) this bit to enable the IRDA transceiver. · Clear (0) this bit to bypass the IRDA transceiver and ignore the other bits of this register.

0x1A24003C GSBI5_UART_DM_DMEN

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_DMEN register indicates if Data Mover is enabled for TX and RX channels.

GSBI5_UART_DM_DMEN

Bits	Name	Description
1	RX_DM_EN	· Set (1) this bit to enable RX DM interface. · Clear (0) this bit to disable RX DM interface. Clearing this bit requires resetting the receiver (see UART_DM_CR register).
0	TX_DM_EN	Set (1) this bit to enable TX DM interface. Clear (0) this bit to disable TX DM interface.

0x1A240040 GSBI5_UART_DM_NO_CHARS_FOR_TX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI5_UART_DM_NO_CHARS_FOR_TX

Bits	Name	Description
23:0	TX_TOTAL_TRANS_LEN	The total number of characters for transmission. Before writing a new value, the TX FIFO must be empty (as indicated by TX_READY interrupt in IMR register or after a reset). It is used by the transmitter to calculate how many characters to transmit in the last word. In DM mode, it is also used for the CRCI mechanism. Any additional writes to the TX FIFO above TX_TOTAL_TRANS_LEN will be discarded. A TX_READY interrupt is triggered after TX_TOTAL_TRANS_LEN number of characters were moved from the TX FIFO to the unpacking register (not all may have been sent).

0x1A240044 GSBI5_UART_DM_BADR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

GSBI5_UART_DM_BADR

Bits	Name	Description
31:2	RX_BASE_ADDR	RX FIFO base address. Both FIFOs use the same RAM (2^RAM_ADDR_WIDTH, 32-bit entries). This register controls the division of the memory to the RX and TX FIFOs. The division is a multiple of 4 entries, since the DM's burst length is 4. The size of the TX FIFO equals RX_BASE_ADDR. The size of the RX FIFO is 2^RAM_ADDR_WIDTH - RX_BASE_ADDR. ® The default is RX_BASE_ADDR = 2^(RAM_ADDR_WIDTH - 1) ® Only RAM_ADDR_WIDTH -1:2 bits are generated.
1:0	UNUSED	

0x1A240048 GSBI5_UART_DM_TESTSL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI5_UART_DM_TESTSL

Bits	Name	Description
4	TEST_EN	Test bus enable
3:0	TEST_SEL	Test bus selector

0x1A240060 GSBI5_UART_DM_MISR_MODE

Type: Read/Write
Clock: WR_CLK

GSBI5_UART_DM_MISR_MODE

Bits	Name	Description
31:2	RESERVED	unused.
1:0	MODE	0x0: Disabled 0x1: Enabled,TX test 0x2: Enabled, RX test

0x1A240064 GSBI5_UART_DM_MISR_RESET

Type: Write
Clock: WR_CLK
Reset State: Undefined

GSBI5_UART_DM_MISR_RESET

Bits	Name	Description
31:1	RESERVED	unused.
0	RESET	

0x1A240068 GSBI5_UART_DM_MISR_EXPORT

Type: Read/Write
Clock: WR_CLK
Reset State: Undefined

GSBI5_UART_DM_MISR_EXPORT

Bits	Name	Description
31:1	RESERVED	unused.
0	EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., what is the result of the muxing of all the input data streams with <BLOCK>_TEST_MODE) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x1A24006C GSBI5_UART_DM_MISR_VAL

Type: Read
Clock: WR_CLK
Reset State: Undefined

GSBI5_UART_DM_MISR_VAL

Bits	Name	Description
9:0	VAL	Current MISR state

0x1A240080 GSBI5_UART_DM_SIM_CFG

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_SIM_CFG register is used to configure the SIM interface for the UART.

- The register is generated only when SIM_GLUE_GEN generic equals 1.

GSBI5_UART_DM_SIM_CFG

Bits	Name	Description
17	UIM_TX_MODE	When this bit is set (1), the transmission portion of the SIM interface operates in block mode (T=1). When clear (0), the transmission portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.
16	UIM_RX_MODE	When this bit is set (1), the receive portion of the SIM interface operates in block mode (T=1). When clear (0), the receive portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.

GSBI5_UART_DM_SIM_CFG (cont.)

Bits	Name	Description
15:8	SIM_STOP_BIT_LEN	In UIM_IF mode, this field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 1 to 254 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. ..... 11 111110: 254 bit times 0x1: 1 bit times 0x2: 2 bit times
7	SIM_CLK_ON	When this bit is set(1), the UIM_CLK is turned on at either the TD8 or TD4 frequency, as indicated by bit6(UIM_CLK_TD8_SEL). When this bit is cleared, the UIM_CLK is stopped either LOW or HIGH, as indicated by bit 5(UIM_CLK_STOP_HIGH).
6	SIM_CLK_TD8_SEL	This bit selects the UIM_CLK frequency at which the UIM_CLK is turned on. 0x1: TD8 (the UIM_CLK runs at the TD8 frequency) 0x0: TD4 (the UIM_CLK runs at the TD4 frequency)
5	SIM_CLK_STOP_HIGH	This bit indicates at what point - high or low - the UIM_CLK will stop. 0x1: high 0x0: low
4	SIM_CLK_SEL	unused
3	MASK_RX	Setting (1) this bit masks off any 0 on the RX line, which prevents the receiver from seeing the START bit. Set (1) this bit if you do not want to receive the data you transmit.
2	SWAP_D	Setting (1) this bit causes the UIM_IF to swap the 8 data bits (making MSB into LSB, bit 6 into bit1, and so on) before it is read by the microprocessor.
1	INV_D	Set (1) this bit to cause the UIM_IF to invert the 8 data bit before it is read by the microprocessor.
0	SIM_SEL	Set (1) this bit to designate the UIM_IF mode of operation.

0x1A240084 GSBI5_UART_DM_TEST_WR_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI5_UART_DM_TEST_WR_ADDR

Bits	Name	Description
31:0	TEST_WR_ADDR	RAM address at which to write the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x1A240088 GSBI5_UART_DM_TEST_WR_DATA

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI5_UART_DM_TEST_WR_DATA

Bits	Name	Description
31:0	TEST_WR_DATA	The test data to be written to the RAM. Write to this register triggers the write to the RAM, to TEST_WR_ADDR address.

0x1A24008C GSBI5_UART_DM_TEST_RD_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI5_UART_DM_TEST_RD_ADDR

Bits	Name	Description
31:0	TEST_RD_ADDR	RAM address from which to read the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

9.9.2 Read registers

NOTE The addresses of the read-only registers are mapped into the same addresses of the four write-only registers in the section above this one. They are: UART_DM_CSR, UART_DM_TF, UART_DM_CR, and UART_DM_IMR, respectively.

0x1A240008 GSBI5_UART_DM_SR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_SR register is the UART status register. This register is used to obtain the current state of the UART subsystem. This register is updated asynchronously.

GSBI5_UART_DM_SR

Bits	Name	Description
8	RX_BREAK_START_LAST	When break start is detected, this bit is set (1). When break end was detected, this bit is reset (0).

GSBI5_UART_DM_SR (cont.)

Bits	Name	Description
7	HUNT_CHAR	When set (1), this bit indicates that the programmed character in the UART_DM_HCR register was received. If programmed, this condition causes the RXHUNT bit to be set (1) in the UART_DM_ISR register. This bit is cleared by issuing a reset error status command.
6	RX_BREAK	When set (1), this bit indicates that an all-zero character of the programmed length was received without a stop bit. If a break begins in the middle of a character, it is detected if the condition remains until the end of the next character time. Only one all zero character is written into the FIFO upon receiving the break. After the RX input returns high for at least half a bit time, then more characters are accepted by the receiver. Whenever the break condition starts or stops as defined above, the RXBREAK bit is set (1) in the UART_DM_ISR register. This bit is appended to the character in the receive FIFO.
5	PAR_FRAME_ERR	A parity error occurs if parity is programmed to be checked and an incoming character is received with incorrect parity. A framing error occurs when the RX input is low while the stop bit is being sampled. This bit is sampled in the middle of the first stop bit position, regardless of the programmed length of the stop bit. This error bit is appended to the character in the receive FIFO.
4	UART_OVERRUN	An overrun error occurs if one or more incoming characters are lost. This happens when the receive FIFO is full, the packing buffer is full and another character has been received in the shift register. The character in the receive shift register is lost. Upon overrun, this status bit remains high until cleared by a reset error status command.
3	TXEMT	This bit is set (1) when the transmitter under-runs. It is set after the transmission of the stop bit at the end of a character, if there are no characters waiting to be sent. It is reset when a character is written to the transmit FIFO.
2	TXRDY	This bit indicates that the transmit FIFO has space in it. It is reset when the FIFO becomes full and set when space becomes available again. Any characters that are written to the FIFO while this bit is low is lost.
1	RXFULL	This bit is set (1) when the receive FIFO becomes full. It is reset when the CPU reads a word.
0	RXRDY	This bit is set (1) when there is a word in the receive FIFO waiting to be read. It is reset when the last word currently stored in the FIFO is read.

0x1A240070 GSBI5_UART_DM_RF

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RF register is the UART receive FIFO register, which is used to access the channel receive FIFO. In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM RX FIFO.

GSBI5_UART_DM_RF

Bits	Name	Description
31:0	UART_RF	This register returns the next value in the receive FIFO. After the read is completed, the FIFO read pointer is updated to make the next character available.

0x1A240074 GSBI5_UART_DM_RF_2

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI5_UART_DM_RF_2

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x1A240078 GSBI5_UART_DM_RF_3

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI5_UART_DM_RF_3

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x1A24007C GSBI5_UART_DM_RF_4

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI5_UART_DM_RF_4

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x1A240010 GSBI5_UART_DM_MISR

Type: Read
Clock: AHB_CLK
Reset State: 0x0

GSBI5_UART_DM_MISR

Bits	Name	Description
12:0	UART_MISR	The UART_DM_MISR register is the masked interrupt status register. A read from this register returns the "AND" of the UART_DM_ISR and the UART_DM_IMR registers. This register is updated asynchronously. This bit field is misr <= (isr(12 DOWNTO 7) AND imr(12 DOWNTO 7)) & '0' & (isr(5 DOWNTO 0) AND imr(5 DOWNTO 0)).

0x1A240014 GSBI5_UART_DM_ISR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_ISR register is the UART interrupt status register. This register provides the current status of the possible interrupt conditions. If one of these bits is set (1), and the corresponding bit in the UART_DM_IMR register is set (1), an interrupt is generated (with the exception of bit 6, CURRENT_CTS - see the description of the UART_DM_IMR register). If the corresponding bit in the UART_DM_IMR register is clear (0), setting one of these bits has no effect on the UART interrupt request signal. This register is updated asynchronously.

GSBI5_UART_DM_ISR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	· See UART_DM_IMR on page 28-9
11	RXBREAK_END	· See UART_DM_IMR on page 28-9
10	RXBREAK_START	· See UART_DM_IMR on page 28-9
9	TX_DONE	· Bit 9 generated only when SIM_GLUE_GEN generic equals 1
8	TX_ERROR	· Bit 9 generated only when SIM_GLUE_GEN generic equals 1
7	TX_READY	See UART_DM_IMR on page 28-9, for descriptions of the UART_DM_ISR bits.
6	CURRENT_CTS	
5	DELTA_CTS	
4	RXLEV	
3	RXSTALE	

GSBI5_UART_DM_ISR (cont.)

Bits	Name	Description
2	RXBREAK	
1	RXHUNT	
0	TXLEV	

0x1A240038 GSBI5_UART_DM_RX_TOTAL_SNAP

Type: Read
Clock: AHB_CLK
Reset State: 0x0

GSBI5_UART_DM_RX_TOTAL_SNAP

Bits	Name	Description
23:0	RX_TOTAL_BYTES	'RX_TOTAL_SNAP register holds the number of characters received since the end of last Rx transfer. It is updated at the end of an Rx transfer (see Software procedures). Rx transfer ends when one of the conditions is met: · The number of characters which were received since the end of the previous transfer equals the value which was written to DMRX at "Transfer initialization". · A stale event occurred (flush operation already performed if was needed).

0x1A24004C GSBI5_UART_DM_TXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI5_UART_DM_TXFS

Bits	Name	Description
31:14	TX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bitfield. · Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	TX_ASYNC_FIFO_STATE	TX asynchronous fifo status - number of characters in the TX asynchronous FIFO.
9:7	TX_BUFFER_STATE	TX unpacking buffer status - number of bytes in the unpacking buffer
6:0	TX_FIFO_STATE_LSB	TX FIFO status - number of words in the TX FIFO

0x1A240050 GSBI5_UART_DM_RXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI5_UART_DM_RXFS

Bits	Name	Description
31:14	RX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bitfield. Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	RX_ASYNC_FIFO_STATE	RX asynchronous fifo status - number of characters in the RX asynchronous FIFO.
9:7	RX_BUFFER_STATE	RX packing buffer status - number of bytes in the packing buffer
6:0	RX_FIFO_STATE_LSB	The number of entries in the RX FIFO that have at least one valid character. It is incremented each time a word is moved from the packing register to the RX FIFO. It is decremented each time a word is read from the RX FIFO. **NOTE** The Uart does not keep track of non-valid characters in each word. (See Software procedures).

0x1A240090 GSBI5_UART_DM_TEST_RD_DATA

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI5_UART_DM_TEST_RD_DATA

Bits	Name	Description
31:0	TEST_RD_DATA	Read from this register triggers the read from the RAM. The register will hold, after read access, data which is found at TEST_RD_ADDR address in the RAM.

9.10 GSBI5 QUP Registers (0x1A280000 QUP5_BASE)

This section contains the GSBI5 QUP registers.

0x1A280000 GSBI5_QUP_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

a. The contents of this register should only be changed when in the RESET_STATE (see the QUP_STATE register).

b. The value written to the QUP output FIFO, is shifted left toward the MSB before passing it to the mini-core as follows:

- N equals 8 or less - shift 24
- N equals 16 to 9 - shift 16
- N equals 24 to 17 - shift 8
- N equals 32 to 25 - no shift

The MINI_CORE clock selected is as follows:

Null: cc_qup_core_clk

SPI: cc_spi_master_clk

I2C: cc_I2C_clk		

GSBI5_QUP_CONFIG

Bits	Name	Description
31:14	RESERVED_1	reserved
13	CORE_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).
12	APP_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).

GSBI5_QUP_CONFIG (cont.)

Bits	Name	Description
11:8	MINI_CORE	value: 0000 Null core value: 0001 SPI core value: 0010 I2C master controller value: 0011 I2C slave controller value: 0100 Reserved (I2C master & slave for loop back operation) value: 0101 Reserved (map to null core) value: 0110 Reserved (map to null core value: 0111 Reserved (map to null core) See Note 1.
7	NO_INPUT	qup_data_in is not used and the value is a "don't care". The QUP input FIFO is always empty. The input service interrupt and INPUT_SERVICE_FLAG bit are never set. See notes (a) and (b) above.
6	NO_OUTPUT	qup_data_out is not used and is held at the value zero. The QUP output FIFO is always empty. The output service flag and OUTPUT_SERVICE_FLAG bit are never set. qup_data_out is still driven when SPI_CS _N is asserted. The setting for NO_TRI_STATE still applies. See notes (a) and (b) above.
5	RESERVED_2	Reserved.
4:0	N	Number of logical bits N in the mini-core that constitutes a single transfer. The value zero indicates N equals one. The value of all ones indicates N equals 32. The value in this register must be 3 (i.e., N is 4 or higher in order for the STATE field to be set to RUN_STATE). See note (a) above.

0x1A280004 GSBI5_QUP_STATE

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b0000000000000000_00000000000XX100

GSBI5_QUP_STATE

Bits	Name	Description
31:5	RESERVED	reserved.
4	I2C_MAST_GEN	Read only. Reflects the RTL generic setting for GEN_I2C_MASTER_MINI_CORE.
3	SPI_GEN	Read only. Reflects the RTL generic setting for GEN_SPI_MINI_CORE.
2	STATE_VALID	Read only. If and only if set to one, writes to the STATE field is allowed or reads from the STATE field is valid. Writes to this bit is ignored.

GSBI5_QUP_STATE (cont.)

Bits	Name	Description
1:0	STATE	When clear (00), the mini-core and related logic is held in RESET_STATE. When set to "01", the mini-core and related logic is released from reset and enters the RUN_STATE. When set to "11", the mini-core and related logic enters the PAUSE_STATE at the next appropriate point in time. Writing (10) to this field clears these two bits. For PAUSE_STATE to RESET_STATE transition, two writes of (10) are required for the transition to complete. See notes 1 and 2. Note 1: SPI - the "next appropriate point in time" is the next time SPI_CS _N de-asserts. If SPI_CS _N is not asserted when the PAUSE_STATE is entered, the SPI_CS _N is maintained in the not asserted state. The PAUSE_STATE is not available for SLAVE operation. Note 2: I2C -

0x1A280008 GSBI5_QUP_IO_MODES

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b0000000000000000_00000000XXXXXXXX

Unless otherwise stated, register bits written return the value when read.

Notes:

a. "Packing" occurs as follows:

- N equals 8 or less - pack four values into each QUP input FIFO word.
- N equals 16 to 9 - pack two values into each QUP input FIFO word.
- N equals 32 to 17 - no packing. Each mini-core value is moved to an QUP input FIFO word.

b. "Un-Packing" occurs as follows:

- N equals 8 or less - un-pack four values from each QUP output FIFO word.
- N equals 16 to 9 - un-pack two values from each QUP output FIFO word.
- N equals 32 to 17 - no packing. Each QUP output FIFO value is moved to the mini-core.

GSBI5_QUP_IO_MODES

Bits	Name	Description
31:17	RESERVED	reserved
16	OUTPUT_BIT_SHIFT_EN	If set, enables the QUP output FIFO block to do bit shifting on the output data.

GSBI5_QUP_IO_MODES (cont.)

Bits	Name	Description
15	PACK_EN	Indicates data values from the mini-core are to be packed before placement in the QUP input FIFO. See note (a) above.
14	UNPACK_EN	Indicates data values taken from the QUP output FIFO should be unpacked before passing to the mini-core. See note (b) above.
13:12	INPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_INPUT = 0, then only FIFO_Mode is available)
11:10	OUTPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_OUTPUT = 0, then only FIFO_Mode is available)
9:7	INPUT_FIFO_SIZE	Read only, actual value set by RTL generic. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 6x BLOCK_SIZE
6:5	INPUT_BLOCK_SIZE	Read only. Actual value set by RTL generic. Indicates the block size associated with Block_Mode and Data_Mover_Mode for input. Value 00: 4 Bytes (FIFO_Mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved
4:2	OUTPUT_FIFO_SIZE	Read only. Actual value set by RTL GENERIC. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 16 BLOCK_SIZE
1:0	OUTPUT_BLOCK_SIZE	Read only. Actual value set by RTL GENERIC. Value 00: 04 Bytes (FIFO mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved

0x1A28000C GSBI5_QUP_SW_RESET

Type: Write/cmd
Clock: CRIF_CLK
Reset State: 0x0000

A write to this register resets the entire QUP core and all mini-cores. The internal registers are brought back to their reset values. Reading of this register returns zero.

GSBI5_QUP_SW_RESET

Bits	Name	Description
31:0	RESERVED	NA

0x1A280010 GSBI5_QUP_TIME_OUT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies if the QUP_MX_OUTPUT_COUNT register and/or QUP_MX_INPUT_COUNT register are enabled. Additionally, this register only applies to Block_Mode and Data_Mover_Mode. The timer starts "ticking" when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The timer pauses for the PAUSE_STATE. If the timer expires before the QUP_MX_OUTPUT_COUNT and/or QUP_MX_INPUT_COUNT are exhausted, then the TIME_OUT_ERR flag is set in the QUP_ERROR_FLAGS register and the interrupt gsbi_qup_irq may be asserted.

GSBI5_QUP_TIME_OUT

Bits	Name	Description
15:0	TIME_OUT_VALUE	Specifies time out value in units of cc_qup_app clock ticks. A value of zero indicates the timer function is not enabled for use. See QUP_CONFIG register for information on clocks.

0x1A280014 GSBI5_QUP_TIME_OUT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI5_QUP_TIME_OUT_CURRENT

Bits	Name	Description
31:0	TIME_OUT_CURRENT	Current value of time-out counter.

0x1A280018 GSBI5_QUP_OPERATIONAL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0080

GSBI5_QUP_OPERATIONAL

Bits	Name	Description
31:10	RESERVED_1	reserved.
13	IN_BLOCK_READ_REQ	Read only. When set by hardware, indicates QUP input FIFO has BLOCK_SIZE_INPUT amount of data ready for reading. Valid only in Block_Mode.
12	OUT_BLOCK_WRITE_REQ	Read only. When set by hardware, indicates QUP output FIFO needs BLOCK_SIZE_OUTPUT amount of data to be written. Valid only in Block_Mode.
11	MAX_INPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP input FIFO has reached the programmed QUP_MX_INPUT_COUNT value. Valid in FIFO_Mode (only if MX_READ_COUNT is non-zero), Block_Mode and Data_Mover_Mode.
10	MAX_OUTPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP output FIFO has reached the programmed QUP_MX_OUTPUT_COUNT value. Valid in Block_Mode and Data_Mover_Mode.
9	INPUT_SERVICE_FLAG	When set by hardware, indicates QUP input FIFO has an outstanding input service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowleges software has or will read the data. Valid only in all modes.
8	OUTPUT_SERVICE_FLAG	When set by hardware, indicates QUP output FIFO has an outstanding output service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowledges software has or will read the data. Valid only in all modes.
7	INPUT_FIFO_FULL	Read only. When set, indicates the input FIFO is full and can accept no more data from the QUP mini-core.
6	OUTPUT_FIFO_FULL	Read only. When set, indicates the output FIFO is full and can accept no more CRIF writes.
5	INPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the input FIFO has at least one value in it to be read. When clear, indicates the input FIFO is empty.
4	OUTPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the output FIFO has at least one value in it to be shifted out. When clear, indicates the output FIFO is empty.
3:0	RESERVED_2	reserved.

0x1A28001C GSBI5_QUP_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

GSBI5_QUP_ERROR_FLAGS

Bits	Name	Description
31:7	RESERVED_1	reserved.
6	TIME_OUT_ERR	The time out limit for a given transfer has been reached.
5	OUTPUT_OVER_RUN_ERR	Indicates the output FIFO was full when a CRIF write was attempted to the FIFO. The write is discarded.
4	INPUT_UNDER_RUN_ERR	Indicates the input FIFO was empty when a CRIF read was attempted to the FIFO. The read value returns is indeterminate.
3	OUTPUT_UNDER_RUN_ER R	Indicates the output FIFO was empty when an output shift operation required a value.
2	INPUT_OVER_RUN_ERR	Indicates the input FIFO was full when an input shift operation provided a new value. When this happens, the new value is discarded.
1:0	RESERVED_2	reserved

0x1A280020 GSBI5_QUP_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x007C

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of gsbi_qup_irq and the setting of the corresponding error flag in the QUP_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

GSBI5_QUP_ERROR_FLAGS_EN

Bits	Name	Description
31:7	RESERVED_1	reserved
6	TIME_OUT_ERR_EN	If set, enables time out error generation.
5	OUTPUT_OVER_RUN_ERR _EN	If set, enables output over run error generation.

GSBI5_QUP_ERROR_FLAGS_EN (cont.)

Bits	Name	Description
4	INPUT_UNDER_RUN_ERR_EN	If set, enables input under run error generation.
3	OUTPUT_UNDER_RUN_ERR_EN	If set, enables output under run error generation.
2	INPUT_OVER_RUN_ERR_EN	If set, enables input over run error generation.
1:0	RESERVED_2	reserved

0x1A280024 GSBI5_QUP_TEST_CTRL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register enables QUP test bus to be actively driven by QUP core signals.

GSBI5_QUP_TEST_CTRL

Bits	Name	Description
31:1	RESERVED	reserved
0	QUP_TEST_BUS_EN	If set, enables QUP core to actively drive test bus. If zero, the core drives the test bus to all zeros.

9.10.1 QUP output FIFO registers

0x1A280100 GSBI5_QUP_MX_OUTPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each output transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not effect the count.

Notes:

a. Allows the total number of Mini Core transfers to be less than an exact multiple of OUTPUT_BLOCK_SIZE. Any additional outputs are discarded.

GSBI5_QUP_MX_OUTPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_COUNT	Number of writes of size N to the mini-core per RUN_STATE. A value of zero indicates the output count function is not enabled for use. See note (a) above.

0x1A280104 GSBI5_QUP_MX_OUTPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI5_QUP_MX_OUTPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_CNT_CURRENT	Current value of QUP_MX_OUTPUT_COUNT.

0x1A280108 GSBI5_QUP_OUTPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

This register holds the output data hanging out of the QUP output FIFO ready be loaded into the mini-core for the next load operation. This corresponds to signal qup_data_out going into the mini-core block.

GSBI5_QUP_OUTPUT_DEBUG

Bits	Name	Description
31:0	OUTPUT_DEBUG_DATA	Value waiting at the exit of output FIFO.

0x1A28010C GSBI5_QUP_OUTPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the output FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the

value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

GSBI5_QUP_OUTPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	OUTPUT_FIFO_WORD_CNT	Number of words in the output FIFO.

0x1A280110+4*c GSBI5_QUP_OUTPUT_FIFOc, c=[0..15]

Type: Write
Clock: CRIF_CLK
Reset State: 0x0000

Note that consecutive writes to this address keeps filling up the output FIFO. The max address to address the output FIFO is 0x14C.

GSBI5_QUP_OUTPUT_FIFOc

Bits	Name	Description
31:0	OUTPUT	Value to be shifted out.

0x1A280150 GSBI5_QUP_MX_WRITE_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_OUTPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the gsbi_qup_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_OUTPUT_COUNT register case, the SW should not program the QUP_MX_WRITE_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_OUTPUT * FIFO_SIZE_OUTPUT).

GSBI5_QUP_MX_WRITE_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_COUNT	The number of "writes" of size N. This is used only if the core is in FIFO_Mode.

0x1A280154 GSBI5_QUP_MX_WRITE_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI5_QUP_MX_WRITE_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_CNT_CURRENT	Current value of QUP_MX_WRITE_COUNT counter.

9.10.2 QUP input FIFO registers

0x1A280200 GSBI5_QUP_MX_INPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each input transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not affect the count.

Notes:

a. Allows the number of shift register transfers to be less than an exact multiple of INPUT_BLOCK_SIZE. When count reached, remainder of INPUT_BLOCK_SIZE is filled with zeroes.

GSBI5_QUP_MX_INPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_COUNT	Number of reads of size N from the mini-core per RUN_STATE. A value of zero indicates the input count function is not enabled for use. See note (a) above.

0x1A280204 GSBI5_QUP_MX_INPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI5_QUP_MX_INPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_CNT_CURRENT	Current value of QUP_MX_INPUT_COUNT.

0x1A280208 GSBI5_QUP_MX_READ_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_INPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the qup_input_service_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_INPUT_COUNT register case, the SW should not program the QUP_MX_READ_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_INPUT * FIFO_SIZE_INPUT). If the SPI mini-core and slave operation is enabled, then an InputOverRun error will result.

GSBI5_QUP_MX_READ_COUNT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_COUNT	The number of "reads" of size N. This is used only if the core is in FIFO_Mode.

0x1A28020C GSBI5_QUP_MX_READ_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI5_QUP_MX_READ_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_CNT_CURRENT	Current value of QUP_MX_READ_COUNT counter.

0x1A280210 GSBI5_QUP_INPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the value of the last loaded in known-good-data into the QUP input FIFO. May be different from what the actual read of input FIFO will return because of packing enabled at the input side. This corresponds to signal qup_data_in coming from the mini-core block synchronized to the crif_clk.

GSBI5_QUP_INPUT_DEBUG

Bits	Name	Description
31:0	INPUT_DEBUG_DATA	Last known good value shifted into the input FIFO.

0x1A280214 GSBI5_QUP_INPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the input FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

GSBI5_QUP_INPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	INPUT_FIFO_WORD_CNT	Number of words in the input FIFO.

0x1A280218+4*c GSBI5_QUP_INPUT_FIFOc, c=[0..15]

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

Consecutive reads to this address reads the input FIFO contents on a FIFO basis.The max address to read the input FIFO is 0x254.

GSBI5_QUP_INPUT_FIFOc

Bits	Name	Description
31:0	INPUT	Value shifted in.

9.10.3 SPI mini-core registers

0x1A280300 GSBI5_SPI_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register. Both NO_OUTPUT and NO_INPUT set to zero provides default full duplex operation. Setting both these bits to one is not a legal operational state.

GSBI5_SPI_CONFIG

Bits	Name	Description
31:11	RESERVED_1	Reserved.
10	HS_MODE	When set, SPI HS_MODE is enabled. When clear, SPI HS_MODE is disabled.
9	INPUT_FIRST	When set, INPUT FIRST SPI protocol is used. When clear, OUTPUT FIRST SPI protocol is used.
8	LOOP_BACK	Loopback is only valid in non-HS mode. Always clear for normal operation. If set, loop back on SPI_DATA_MO_SI under MASTER operation or SPI_DATA_MI_SO under SLAVE operation.
7:6	RESERVED_2	Reserved.
5	SLAVE_OPERATION	This register is writable only when the hardware signal spi_slave_en is asserted. When set, the SPI is configured for SLAVE operation. Zero indicates MASTER operation.
4:0	RESERVED	Reserved.

0x1A280304 GSBI5_SPI_IO_CONTROL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register.

Unless otherwise stated, register bits written return the value when read.

GSBI5_SPI_IO_CONTROL

Bits	Name	Description
31:11	RESERVED	Reserved.
10	CLK_IDLE_HIGH	Use SPI_CLK_IDLE_HIGH when set.
9	CLK_ALWAYS_ON	When MASTER operation is used, run SPI_CLK during IDLE.
8	MX_CS_MODE	If this bit is set, then for a given RUN state, the associated chip select will be asserted for the first N-bit transfer and will be kept asserted till the last programmed transfer. Applies only in MASTER mode. The number of transfers is determined by SPI_MX_OUTPUT_COUNT and/or SPI_MX_INPUT_COUNT registers.
7:4	CS_N_POLARITY	These four bits control the polarity of four SPI_CS _N respectively. Setting any of this bit to '1', makes the associated SPI_CS _N active HIGH. This field is a "don't care" in SLAVE operation.
3:2	CS_SELECT	When MASTER operation is used, controls the assertion of SPI_CS_ N pins. Selects SPI_CS_N if 00, SPI_CS1_N if 01, SPI_CS2_N if 10, or SPI_CS3_N if 11. The deselected ChipSelects will be driven to inactive state dictated by the field CS_N_POLARITY. This field is a "don't care" in SLAVE operation.
1	TRISTATE_CS	When set, drives Z on all SPI_CS _N lines. When clear, enables normal functionality on these lines. This bit can be used to support deployment of the core as one of the masters in a multi-master configuration.
0	NO_TRI_STATE	When set, spi_data_out is not taken tri-state when SPI_CS _N is de-asserted. This bit is normally set for MASTER operation but may be optionally left cleared.

0x1A280308 GSBI5_SPI_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

GSBI5_SPI_ERROR_FLAGS

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.

GSBI5_SPI_ERROR_FLAGS (cont.)

Bits	Name	Description
1	SPI_SLV_CLK_OVER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was greater than the programmed value of N. When this happens, only the first N bits are passed to the SPI input FIFO and the output shift value is held at zero.
0	SPI_SLV_CLK_UNDER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was less than the programmed value of N. When this occurs, the bits which were received are passed to the SPI input FIFO and the CURRENT output bit is forced to zero.

0x1A28030C GSBI5_SPI_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0003

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of spi_error_irq and the setting of the corresponding error flag in the SPI_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

GSBI5_SPI_ERROR_FLAGS_EN

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.
1	SPI_SLV_CLK_OVER_RUN_ERR_EN	If set, enables clock over run error generation.
0	SPI_SLV_CLK_UNDER_RUN_ERR_EN	If set, enables clock under run error generation.

0x1A280310 GSBI5_SPI_DEASSERT_WAIT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the de-assertion wait time of SPI_CS _N between consecutive N-bit transfers in MASTER operation. The wait time is specified in number of cycles of cc_spi_master_clk.

GSBI5_SPI_DEASSERT_WAIT

Bits	Name	Description
31:6	RESERVED	Reserved.

GSBI5_SPI_DEASSERT_WAIT (cont.)

Bits	Name	Description
5:0	DEASSERT_WAIT	Number cc_spi_master_clk ticks associated with the de-asserted time of SPI_CS _N. Only applies to MASTER operation. For SLAVE operation, this field is a "don't care". A value of zero indicates SPI_CS _N remains de-asserted for exactly one clock tick. A value of one, indicates two ticks, etc. All ones indicates 64 ticks.

9.10.4 I2C master mini-core registers

0x1A280400 GSBI5_I2C_MASTER_CLK_CTL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_CLK_CTL register is a read/write register that controls clock divider values. This register should only be written to after it is confirmed that the I2C master mini-core is not longer in RESET state (QUP_STATE register).

GSBI5_I2C_MASTER_CLK_CTL

Bits	Name	Description
31:11	RESERVED	Reserved.
10:8	HS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in high-speed (HS) mode. The minimum value should be 3 hex (4 I2C_clk clocks per period) to ensure proper sampling of the bus. For a maximum high speed bit rate of 3.4 Mb/s (high speed mode), this would require a minimum 40.8 MHz I2C_clk clock. The maximum I2C_clk is 81.6 MHz. This register is reset to a maximum value of 7 hex. I2C_HS_CLK = I2C_CLK/(3*(HS_DIVIDER_VALUE+1)
7:0	FS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in fast/standard (FS) mode. The minimum value should be 3 hex to ensure proper sampling of the bus. For a maximum bit rate of 400 kb/s (fast mode), this would require a 4.8 MHz I2C_clk clock. For a maximum bit rate of 100 kb/s (standard mode), this would require a 1.2 MHz I2C_clk clock. Maximum I2C_clk for fast and standard modes are 206.4 MHz and 51.6 MHz respectively. This register is reset to a maximum value of 255 hex. I2C_FS_CLK = I2C_CLK/(2*(FS_DIVIDER_VALUE+3)

0x1A280404 GSBI5_I2C_MASTER_STATUS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_STATUS is a status register. Writing a one clears the status bits.

GSBI5_I2C_MASTER_STATUS

Bits	Name	Description
31:26	RESERVED_1	Reserved.
25	INVALID_READ_SEQ	This bit is set (1) when a MI_REC tag does not follow a START tag for an I2C READ. Not applicable for Halcyon.
24	INVALID_READ_ADDR	This bit is set (1) when the I2C controller is trying to receive data from a non-existent I2C slave (address).
23	INVALID_TAG	This bit is set (1) when the I2C controller is trying to process data from the output FIFO that is improperly tagged.
22:20	INPUT_FSM_STATE	This 3-bit field informs the microprocessor of the state of the I2C MASTER INPUT FSM block. Reset, read_last_byte, mi_rec, dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: READ_LAST_BYTE_STATE Value 0x3: MI_REC_STATE Value 0x4: DEC_STATE Value 0x5: STORE_STATE
19:16	OUTPUT_FSM_STATE	This 4-bit field informs the microprocessor of the state of the I2C MASTER OUTPUT FSM block. Reset, decode, send, mi_red, nop, nop_dec, invalid, invalid_dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: DECODE_STATE Value 0x3: SEND_STATE Value 0x4: MI_REC_STATE Value 0x5: NOP_STATE Value 0x6: INVALID_STATE Value 0x7: PEEK_STATE Value 0x8: SEND_R_STATE

GSBI5_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
15:13	CLK_STATE	This 3-bit field informs the microprocessor of the state of the I2C clk_control block. Reset_busidle, not_master, high, low, high_wait, forced_low, hs_addr_low or double_buffer_wait. Value 0x0: RESET_BUSIDLE_STATE Value 0x1: NOT_MASTER_STATE Value 0x2: HIGH_STATE Value 0x3: LOW_STATE Value 0x4: HIGH_WAIT_STATE Value 0x5: FORCED_LOW_STATE Value 0x6: HS_ADDR_LOW_STATE Value 0x7: DOUBLE_BUFFER_WAIT_STATE
12:10	DATA_STATE	This 3-bit field informs the microprocessor of the state of the I2C data_control block. Reset, Tx addr, Tx HS addr, Tx 10-bit addr, Tx 2nd 10-bit addr byte, Tx data and Rx data. Value 0x0: RESET_WAIT_STATE Value 0x1: TX_ADDR_STATE Value 0x2: TX_DATA_STATE Value 0x3: TX_HS_ADDR_STATE Value 0x4: TX_10_BIT_ADDR_STATE Value 0x5: TX_2ND_BYTE_STATE Value 0x6: RX_DATA_STATE
9	BUS_MASTER	This bit is set (1) when the I2C controller is the present bus master.
8	BUS_ACTIVE	This bit is set (1) when the bus is in use by this, or any other controller.
7:6	FAILED	This 2-bit field contains the failure information of the present I2C transfers. If transmitting, failed[1] contains the information regarding the byte that has been transmitted. Failed[0] contains the information of the byte awaiting transmission if there is a byte pipelined. If no byte is pipelined, ignore this bit. If receiving, failed[1] contains the information of the byte received and stored in the buffer, and failed[0] should be ignored. For example: Value 00: Byte n transmitted successfully, byte n+1 to begin transmission Value 01: Byte n transmitted successfully, byte n+1 errored: type of error indicated in other STATUS bits. (queued invalid write, for example) Value 10: Byte n errored: type of error indicated in other STATUS bits, byte n+1 to begin transmission (byte n+1 would have to be a valid address byte for this condition to occur) Value 11: Byte n errored: type of error indicated in other STATUS bits, byte n+1 discarded as well (if the byte was a data byte destined for a NACKed address, data is useless, therefore discarded)
5	INVALID_WRITE	This bit is set (1) when software writes data to the I2C_DATA register that should be flagged as an address but is not.

GSBI5_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
4	ARB_LOST	This bit is set (1) when the controller loses arbitration for the bus. If this bit gets set (1) during the transmission, all data has been lost, and the microprocessor must re-request its transmission.
3	PACKET_NACKED	This bit is set high when a NACK is received from a slave. If a high speed master code is sent and there is an ACK from a slave, then this bit is set (1) to indicate that the high speed mode can not be entered. If the high speed mode is accepted by the slave, then a NACK is performed and this bit is not set (1).
2	BUS_ERROR	This bit is set (1) when an unexpected START or STOP condition is detected. This returns the controller to its reset state.
1:0	RESERVED_2	Reserved.

9.11 GSBI6 Registers (0x16500000 GSBI6_BASE)

This section contains the GSBI6 registers.

9.11.1 GSBI CTRL Registers

0x16500000 GSBI6_GSBI_CTRL_REG

Type: Read/write
Clock: HCLK
Reset State: 0x00000000

GSBI6_GSBI_CTRL_REG

Bits	Name	Description
15:12	RESERVED	reserved
11:8	WRAPPER_CTRL	This field has no predefined use. When a wrapper is constructed around one or more GSBIs there may be a need to configure it. For example, to select which of several GSBIs will be connected to a particular I2S block. All bits of this field emerge from GSBI as output ports which can be used for any such configuration task.
7	RESERVED_7	Reserved. The host can write and read this field, but its state has no effect on anything.
6:4	PROTOCOL_CODE	This field controls which protocol, if any, is applied to the GSBI's four I/O ports. Most codes assign a single protocol, but codes of "001" and "110" assigns I2C to two of the ports and UART (without flow control signals) or SIM to the other two. 0x0: Idle (null values are applied to all four GSBI I/Os) 0x1: I2C on 2 ports, SIM/R-UIM on other 2 0x2: I2C 0x3: SPI 0x4: UART with flow control (or IRDA) 0x5: SIM/R-UIM 0x6: I2C on 2 ports, UART (without HS flow ctrl on other 2) 0x7: Undefined
3:1	RESERVED_3_1	Reserved. The host can write and read this field, but its state has no effect on anything.
0	CRCI_MUX_CTRL	While this bit is low QUP CRCI ports are connected to the GSBI ports nominally for QUP and UART_DM CRCI ports are connected to the GSBI ports nominally for UART_DM. While this bit is high QUP CRCI ports are connected to the GSBI ports nominally for UART_DM and UART_DM CRCI ports are connected to nothing.

0x16500004 GSBI6_GSBI_DBG0_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI6_GSBI_DBG0_REG

Bits	Name	Description
1:0	GSBI_PLAY0	This field has no function beyond the fact that the ARM can write to it and read from it.

0x16500008 GSBI6_GSBI_DBG1_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI6_GSBI_DBG1_REG

Bits	Name	Description
1:0	GSBI_PLAY1	This field has no function beyond the fact that the ARM can write to it and read from it.

0x1650000C GSBI6_GSBI_DBG2_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI6_GSBI_DBG2_REG

Bits	Name	Description
1:0	GSBI_PLAY2	This field has no function beyond the fact that the ARM can write to it and read from it.

0x16500010 GSBI6_GSBI_DBG3_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI6_GSBI_DBG3_REG

Bits	Name	Description
1:0	GSBI_PLAY3	This field has no function beyond the fact that the ARM can write to it and read from it.

9.12 GSBI6 UART DM Registers (0x16540000 GSBI6_UART_DM_BASE)

This section contains the GSBI6 UART DM registers.

9.12.1 Write and read/write registers

0x16540000 GSBI6_UART_DM_MR1

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_MR1 register is the UART mode register 1. It is used, along with UART_DM_MR2, to configure the operational mode of the UART.

GSBI6_UART_DM_MR1

Bits	Name	Description
31:8	AUTO_RFR_LEVEL1	These bits are used, along with bits 5:0 (AUTO_RFR_LEVEL0) to program the level in the receive FIFO at which the RFR_N signal is de-asserted, if programmed to do so (see RX_RDY_CTL field of this register). The level counts the number of words inside the RX FIFO. It doesn't count the character that is being received (shift register) or characters in the packing buffer. This value is programmed from 1 to 2^RAM_ADDR_WIDTH. The RFR_N signal is de-asserted when the RX FIFO level (the number of characters remaining in the RX FIFO) is greater than the level that is programmed into this register. · Only RAM_ADDR_WIDTH +1:8 bits are generated.
7	RX_RDY_CTL	Setting (1) this bit enables the automatic ready-for-receiving (RFR_N) control for the receiver. RFR_N is turned off, or set (1), when a valid start bit is received and the channel FIFO is at the level programmed in bits 4 through 0 of this mode register. When the FIFO level falls back to the programmed level, the RFR_N signal is turned on, or clear (0). When this feature is off, the RFR_N signal can be used by normal signal port bit manipulation (see UART_DM_CR register).
6	CTS_CTL	When this bit is set(1), the transmitter checks the CTS_N input to determine whether to begin transmission of a new character. If CTS_N is low, the character is sent. Otherwise the transmitter continues marking until CTS_N goes low, then the next character is transmitted. A change on CTS_N during the transmission of a character has no effect on that character. When this bit is clear(0), the CTS_N input for the channel has no effect on the transmitter.
5:0	AUTO_RFR_LEVEL0	See the description of bit 8 (AUTO_RFR_LEVEL1).

0x16540004 GSBI6_UART_DM_MR2

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI6_UART_DM_MR2

Bits	Name	Description
9	RX_ERROR_CHAR_OFF	When this bit is asserted, characters with parity or framing errors don't enter RX FIFO. Otherwise they enter RX FIFO.
8	RX_BREAK_ZERO_CHAR_OFF	When this bit is asserted, the zero character received at rx_break doesn't enter RX FIFO. Otherwise it enters RX FIFO.
7	LOOPBACK	Internal use only
6	ERROR_MODE	This bit controls the operation of the two FIFO status bits for the channel (parity or framing error and received break). · When clear (0), the UART operates in character mode and the status bits apply only to the character at the top of the FIFO. · When set (1), the UART operates in block mode and both bits are the "OR" of the status for all previously received characters arriving after the last `reset error status' command was issued (see CR register).
5:4	BITS_PER_CHAR	These bits determine how many bits are transmitted or received per character, not including the start, stop, and parity bits. 0x0: 5 bits 0x1: 6 bits 0x2: 7 bits 0x3: 8 bits
3:2	STOP_BIT_LEN	This field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 9/16, 1, 1+ 9/16, and 2 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. 0x0: 0.563 (9/16 bit times) 0x1: 1.000 bit time 0x2: 1.563 (1+9/16 bit times) 0x3: 2.000 bit times
1:0	PARITY_MODE	These bits determine which parity mode is used. The user can select between odd, even, space, or no parity. 0x0: no parity 0x1: odd parity 0x2: even parity 0x3: space parity

0x16540008 GSBI6_UART_DM_CSR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_CSR register is the UART clock selection register. This register is used in conjunction with the UART M/N counter registers to determine the bit rate for the transmitter and receiver. The transmitter and receiver can be clocked at different rates.

The rates below are based on a uart_dm_clk rate of 1.8432 MHz (115.2 * 16).

Table 9-11 lists the hexadecimal values for the clock select field and the corresponding data rates.

Table 9-11 Hexidecimal values and data rates for the clock select field

CLK SEL value	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Bit rate (b/sec)	75	150	300	600	1200	2400	3600	4800	7200	9600	14.4k	19.2k	28.8k	38.4k	57.6k	115.2k

GSBI6_UART_DM_CSR

Bits	Name	Description
7:4	UART_RX_CLK_SEL	Use the CLK SEL values in Table 28-12 to select the appropriate receive and transmit bit rates.
3:0	UART_TX_CLK_SEL	

0x16540070 GSBI6_UART_DM_TF

Type: Write
Clock: AHB_CLK
Reset State: Undefined

In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM TX FIFO.

GSBI6_UART_DM_TF

Bits	Name	Description
31:0	UART_TF	The UART_TF register is the UART transmit FIFO register. This register is used to access the channel transmit FIFO. If the FIFO is full at the time of writing, the character is lost and an interrupt is generated (see UART_DM_IMR register).

0x16540074 GSBI6_UART_DM_TF_2

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI6_UART_DM_TF_2

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x16540078 GSBI6_UART_DM_TF_3

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI6_UART_DM_TF_3

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x1654007C GSBI6_UART_DM_TF_4

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI6_UART_DM_TF_4

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x16540010 GSBI6_UART_DM_CR

Type: Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_CR register is the UART command register. This register is used to issue specific commands to the UART subsystem. This register is updated asynchronously.

CAUTION Do not reset the transmitter and disable it at the same time. Do not reset the receiver and disable it at the same time.

Table 9-12 UART DM commands

Value	Description	Result
0	Null command	Does nothing.
1	Reset receiver	Resets the receiver as if a hardware reset were issued. The receiver is disabled and the FIFO, packing buffer and shift registers are flushed.
2	Reset transmitter	Resets the transmitter as if a hardware reset were issued. The transmitter signal goes high (marking) and the FIFO, unpacking register and shift register are flushed.
3	Reset error status	Clears the overrun error and hunt char received status bits in both the character and block error modes. In the block error mode, it clears the error status and received break.
4	Reset break change interrupt	Clears the break change interrupt status bit.
5	Start break	Forces the transmitter signal low. The transmitter must be enabled. If the transmitter is busy, the break is started when all characters in the transmit FIFO and the transmit shift register have been completely sent.
6	Stop break	If executed while channel is breaking, this command causes the transmitter signal to go high. The signal remains high for at least one bit time before sending out a new character.
7	Reset CTS_N	Clears ISR bit 5.
8	Reset stale interrupt	Clears the stale interrupt.
9	Packet mode	Turns on the sample data mode, which causes the receiver to sample the receive data stream at 16 times the programmed baud rate. The data is sampled with the start of the start bit, or the first data bit, and continued until the marking state. To exit this state, write 1100 in the command field.
A	test_parity_on	Internal use only.
B	test_frame_on	Internal use only.
C	Mode reset	Turns off the sample data mode.
D	Set RFR_N	Asserts the ready for receiving signal (active low).
E	Reset RFR_N	De-asserts the ready for receiving signal.
F	uart_reset_int	Internal use only.
10	Reset TX_ERROR	Clears TX_ERROR
11	Clear TX_DONE	Clears the TX_DONE interrupt (ISR bit 9)
12	Reset break start interrupt	Clears the break start interrupt status bit.
13	Reset break end interrupt	Clears the break end interrupt status bit.
14	Reset par_frame_err interrupt	Clears the par_frame_err interrupt status bit.

Table 9-13 UART DM commands

Value	Description	Result
0	Null command	Does nothing.
1	CR Protection Enable	Enables CR HW protection. When two consecutive writes to the CR are detected, the second write is delayed until the command of the first write is finished. The delay is done by de-asserting the AHB ready and this ensures that the first command completes and the second one will be executed right afterward.
2	CR Protection Disable	Disables CR HW protection. SW is responsible for managing delay between writes to the CR register.
3	Reset TX-Ready interrupt	Clears the TX_READY interrupt.
5	Enable Stale Event	Enables the `stale event' mechanism. See Software Procedures.
6	Disable Stale Event	Disables the `stale event' mechanism. See Software Procedures.
4	SW Force Stale	Causes a `stale event' (even if `stale event' is disabled). See Software Procedures.
7	RESERVED	

GSBI6_UART_DM_CR

Bits	Name	Description
11	CHANNEL_COMMAND_MSB	This is the msb of the CHANNEL_COMMAND bitfield.
10:8	GENERAL_COMMAND	Writing the appropriate value to these bits executes the commands that are listed in Table .
7:4	CHANNEL_COMMAND_LSB	Writing the appropriate value to these bits along with bit 11,executes the commands that are listed in Table 28-13.
3	UART_TX_DISABLE	This command terminates the operation of the transmitter after any character in the transmit shift register is sent.
2	UART_TX_EN	This command enables the operation of the transmitter.
1	UART_RX_DISABLE	This command immediately terminates the operation of the channel receiver and any incoming characters are lost. None of the receiver status bits are affected by this command and characters that are already in the receive FIFO remain there.
0	UART_RX_EN	This command enables the channel receiver.

0x16540014 GSBI6_UART_DM_IMR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IMR register is the UART interrupt mask register. This register is used to enable the corresponding functions in the UART_DM_ISR register. Setting (1) a bit in the UART_DM_IMR register causes an interrupt to be generated, if the corresponding bit in the UART_DM_ISR register is set. Clearing (0) a bit in the UART_DM_IMR register causes the setting of the corresponding bit in the UART_DM_ISR register to have no effect on the interrupt signal.

Bit 6 of the UART_DM_IMR register, CURRENT_CTS, is slightly different. If the current value of the CTS is one (1), no interrupt is generated. However, the user can use bit 6 in this register to mask the CTS value when reading the UART_DM_MISR register or as a general-purpose bit.

GSBI6_UART_DM_IMR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	This bit is asserted in the same condition at which PAR_FRAME_ERR status bit is asserted. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x14.
11	RXBREAK_END	This bit is set (1) if the end of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x13.
10	RXBREAK_START	This bit is set (1) if the start of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x12.
9	TX_DONE	This bit is used only in UIM/SIM_IF mode. Set (1) this bit when the last byte in the transmitter has been sent. This bit is generated only when SIM_GLUE_GEN generic equals 1.
8	TX_ERROR	Only used in UIM_IF mode. Set (1) this bit to indicate that there has been parity error during transmission. To clear the detection logic associated with this function, write CR[11;7:4]=0x10. This bit is generated only when SIM_GLUE_GEN generic equals 1.
7	TX_READY	This bit, when set(1), indicates that: 1. TX FIFO is empty. 2. The value written in NO_CHARS_FOR_TX register equals the number of bytes written to the TX FIFO since the register was updated. **NOTE** There may be characters in the unpack buffer or in the shift register. This bit is cleared by issuing `clear TX ready' command (see UART_DM_CR register).

GSBI6_UART_DM_IMR (cont.)

Bits	Name	Description
6	CURRENT_CTS	This bit indicates the current state of the CTS input. It never generates an interrupt.
5	DELTA_CTS	This bit, when set (1), indicates that the CTS input has changed states. To clear the detection logic associated with this function, write CR[7:4]=0x7.
4	RXLEV	This bit is set when a character is loaded into the receive FIFO that brings the total number of characters in the FIFO above the programmed watermark level in the FIFO watermark register (RFWR). This bit is cleared after enough characters have been read to bring the level equal to or below the programmed watermark level.
3	RXSTALE	This bit indicates that a `stale event' occurred. See Software procedures for the exact timing of this interrupt. It is cleared by issuing a reset-stale command (see CR register).
2	RXBREAK_CHANGE	This bit is set (1) if the start or end of a break condition is detected. The logic associated with this condition is cleared (0) by writing CR[7:4]=0x4. A detected break is defined as an all-zeros character with an invalid stop bit AND LOW PARITY. The end of a break is defined as a mark condition (1) at least 1/2 bit width. A detected break occupies one position in the Rx FIFO.
1	RXHUNT	This bit is set (1) when an incoming character matches the value programmed into the UART_DM_HCR register. This condition is cleared (0) by issuing a reset error status command (CR[7:4]=0x3).
0	TXLEV	This bit is set (1) when a character which is transferred from the transmit FIFO to the transmit shift register brings the total number of characters in the FIFO below or equal to the programmed watermark level in the UART_DM_TFWR register. This bit is cleared (0) after enough characters have been written to the FIFO to bring the level above the programmed watermark level.

0x16540018 GSBI6_UART_DM_IPR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0xffffff9f

The UART_DM_IPR register is the UART interrupt programming register.

GSBI6_UART_DM_IPR

Bits	Name	Description
31:7	STALE_TIMEOUT_MSB	These bits are the STALE_TIMEOUT bitfield. The stale character time-out duration field contains a number from 1 to 2^30 -1. This number determines how many character times must elapse before a `stale event' is generated. This character time is defined as 10 times the bit rate. It is reset whenever a data bit is received. Do not clear (0) this register if the stale character time-out interrupt is enabled. Note the discontinuity in the bit assignments.
6	SAMPLE_DATA	Setting (1) this bit enables the new sample data mode, which means that the start bit is sampled as well as the rest, when in sample data mode. See the CR register, CHANNEL_COMMAND bit for more information.
5	RESERVED	
4:0	STALE_TIMEOUT_LSB	This bitfield is the LSbits of the STALE_TIMEOUT bitfield.

0x1654001C GSBI6_UART_DM_TFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_TFWR register is the UART transmit FIFO watermark register.

GSBI6_UART_DM_TFWR

Bits	Name	Description
31:0	TFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the transmit FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of TX words in the FIFO) is less than or equal to the value in TFWR. See UART_DM_IMR register. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x16540020 GSBI6_UART_DM_RFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RFWR register is the UART receive FIFO watermark register.

GSBI6_UART_DM_RFWR

Bits	Name	Description
31:0	RFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the receive FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of words in the RX FIFO) is greater than the value in RFWR. nOnly RAM_ADDR_WIDTH -1:0 bits are generated.

0x16540024 GSBI6_UART_DM_HCR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI6_UART_DM_HCR

Bits	Name	Description
7:0	DATA	The UART_DM_HCR register is the UART hunt character register, which contains the character for which the receiver looks to assert a hunt character received interrupt.

0x16540034 GSBI6_UART_DM_DMRX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI6_UART_DM_DMRX

Bits	Name	Description
24:0	RX_DM_CRCI_CHARS	In the DM mode, the number of chars in the Rx FIFO that are used for CRCI handshake with the DM. The written value of RX_DM_CRCI_ CHARS must be a multiple of 16(bits [3:0] are treated as 0x0). After a value is written, the UART will generate CRCI requests as long as RX_DM_CRCI_CHARS is non zero. Read of DMRX register gives the number of characters that were received since the end of the last transfer. It is reset at the end of each Rx transfer Also is used by the software to indicate `transfer initialization'. See Software procedures.

0x16540038 GSBI6_UART_DM_IRDA

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IRDA register enables the IRDA function, selects a loopback, and allows inversion of RX and TX data. This register also controls the IRDA transceiver that optionally interfaces between the UART and the DP_RX_DATA and DP_TX_DATA pins.

The UART proper is a standard RX/TX configuration that converts the serial pin input and output lines to 8-bit data for the microprocessor. The configuration contains receive and transmit blocks, a control block, a bit rate generator for RX and TX, and FIFO interfaces with the microprocessor data bus. The IRDA register provides the means of switching IRDA circuits into the serial I/O lines and the IRDA function is normally switched out. The IRDA modulator/demodulator may be enabled or disabled under microprocessor control. When enabled, the RX and TX data pathis have individual inversion select bits, so external true or inverted drivers may be used in the signal path.

- The register is generated only when IRDA_IFC_GEN generic equals 1.

GSBI6_UART_DM_IRDA

Bits	Name	Description
4	MEDIUM_RATE_EN	· Set (1) for 1/4 bit-time pulse length (Medium rate) · Clear (0) for 3/16 bit-time pulse length (Low rate)
3	IRDA_LOOPBACK	· This bit loops the IRDA modulated TX line back into the IRDA RX line. The normal UART loopback mode must be off in order to see this effect.
2	INVERT_IRDA_TX	This bit inverts the polarity of the IRDA modulated signal on the DP_TX_DATA pin. · Set (1) this bit for an inverted polarity. · Clear (0) this bit for a non-inverted polarity.
1	INVERT_IRDA_RX	This bit inverts the polarity of the IRDA received signal on the DP_RX_DATA pin. · Set (1) this bit for inverted the polarity. · Clear (0) this bit for non-inverted polarity.
0	IRDA_EN	· Set (1) this bit to enable the IRDA transceiver. · Clear (0) this bit to bypass the IRDA transceiver and ignore the other bits of this register.

0x1654003C GSBI6_UART_DM_DMEN

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_DMEN register indicates if Data Mover is enabled for TX and RX channels.

GSBI6_UART_DM_DMEN

Bits	Name	Description
1	RX_DM_EN	· Set (1) this bit to enable RX DM interface. · Clear (0) this bit to disable RX DM interface. Clearing this bit requires resetting the receiver (see UART_DM_CR register).
0	TX_DM_EN	Set (1) this bit to enable TX DM interface. Clear (0) this bit to disable TX DM interface.

0x16540040 GSBI6_UART_DM_NO_CHARS_FOR_TX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI6_UART_DM_NO_CHARS_FOR_TX

Bits	Name	Description
23:0	TX_TOTAL_TRANS_LEN	The total number of characters for transmission. Before writing a new value, the TX FIFO must be empty (as indicated by TX_READY interrupt in IMR register or after a reset). It is used by the transmitter to calculate how many characters to transmit in the last word. In DM mode, it is also used for the CRCI mechanism. Any additional writes to the TX FIFO above TX_TOTAL_TRANS_LEN will be discarded. A TX_READY interrupt is triggered after TX_TOTAL_TRANS_LEN number of characters were moved from the TX FIFO to the unpacking register (not all may have been sent).

0x16540044 GSBI6_UART_DM_BADR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

GSBI6_UART_DM_BADR

Bits	Name	Description
31:2	RX_BASE_ADDR	RX FIFO base address. Both FIFOs use the same RAM (2^RAM_ADDR_WIDTH, 32-bit entries). This register controls the division of the memory to the RX and TX FIFOs. The division is a multiple of 4 entries, since the DM's burst length is 4. The size of the TX FIFO equals RX_BASE_ADDR. The size of the RX FIFO is 2^RAM_ADDR_WIDTH - RX_BASE_ADDR. ® The default is RX_BASE_ADDR = 2^(RAM_ADDR_WIDTH - 1) ® Only RAM_ADDR_WIDTH -1:2 bits are generated.
1:0	UNUSED	

0x16540048 GSBI6_UART_DM_TESTSL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI6_UART_DM_TESTSL

Bits	Name	Description
4	TEST_EN	Test bus enable
3:0	TEST_SEL	Test bus selector

0x16540060 GSBI6_UART_DM_MISR_MODE

Type: Read/Write
Clock: WR_CLK

GSBI6_UART_DM_MISR_MODE

Bits	Name	Description
31:2	RESERVED	unused.
1:0	MODE	0x0: Disabled 0x1: Enabled,TX test 0x2: Enabled, RX test

0x16540064 GSBI6_UART_DM_MISR_RESET

Type: Write
Clock: WR_CLK
Reset State: Undefined

GSBI6_UART_DM_MISR_RESET

Bits	Name	Description
31:1	RESERVED	unused.
0	RESET	

0x16540068 GSBI6_UART_DM_MISR_EXPORT

Type: Read/Write
Clock: WR_CLK
Reset State: Undefined

GSBI6_UART_DM_MISR_EXPORT

Bits	Name	Description
31:1	RESERVED	unused.
0	EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., what is the result of the muxing of all the input data streams with <BLOCK>_TEST_MODE) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x1654006C GSBI6_UART_DM_MISR_VAL

Type: Read
Clock: WR_CLK
Reset State: Undefined

GSBI6_UART_DM_MISR_VAL

Bits	Name	Description
9:0	VAL	Current MISR state

0x16540080 GSBI6_UART_DM_SIM_CFG

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_SIM_CFG register is used to configure the SIM interface for the UART.

- The register is generated only when SIM_GLUE_GEN generic equals 1.

GSBI6_UART_DM_SIM_CFG

Bits	Name	Description
17	UIM_TX_MODE	When this bit is set (1), the transmission portion of the SIM interface operates in block mode (T=1). When clear (0), the transmission portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.
16	UIM_RX_MODE	When this bit is set (1), the receive portion of the SIM interface operates in block mode (T=1). When clear (0), the receive portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.

GSBI6_UART_DM_SIM_CFG (cont.)

Bits	Name	Description
15:8	SIM_STOP_BIT_LEN	In UIM_IF mode, this field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 1 to 254 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. ..... 11 111110: 254 bit times 0x1: 1 bit times 0x2: 2 bit times
7	SIM_CLK_ON	When this bit is set(1), the UIM_CLK is turned on at either the TD8 or TD4 frequency, as indicated by bit6(UIM_CLK_TD8_SEL). When this bit is cleared, the UIM_CLK is stopped either LOW or HIGH, as indicated by bit 5(UIM_CLK_STOP_HIGH).
6	SIM_CLK_TD8_SEL	This bit selects the UIM_CLK frequency at which the UIM_CLK is turned on. 0x1: TD8 (the UIM_CLK runs at the TD8 frequency) 0x0: TD4 (the UIM_CLK runs at the TD4 frequency)
5	SIM_CLK_STOP_HIGH	This bit indicates at what point - high or low - the UIM_CLK will stop. 0x1: high 0x0: low
4	SIM_CLK_SEL	unused
3	MASK_RX	Setting (1) this bit masks off any 0 on the RX line, which prevents the receiver from seeing the START bit. Set (1) this bit if you do not want to receive the data you transmit.
2	SWAP_D	Setting (1) this bit causes the UIM_IF to swap the 8 data bits (making MSB into LSB, bit 6 into bit1, and so on) before it is read by the microprocessor.
1	INV_D	Set (1) this bit to cause the UIM_IF to invert the 8 data bit before it is read by the microprocessor.
0	SIM_SEL	Set (1) this bit to designate the UIM_IF mode of operation.

0x16540084 GSBI6_UART_DM_TEST_WR_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI6_UART_DM_TEST_WR_ADDR

Bits	Name	Description
31:0	TEST_WR_ADDR	RAM address at which to write the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x16540088 GSBI6_UART_DM_TEST_WR_DATA

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI6_UART_DM_TEST_WR_DATA

Bits	Name	Description
31:0	TEST_WR_DATA	The test data to be written to the RAM. Write to this register triggers the write to the RAM, to TEST_WR_ADDR address.

0x1654008C GSBI6_UART_DM_TEST_RD_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI6_UART_DM_TEST_RD_ADDR

Bits	Name	Description
31:0	TEST_RD_ADDR	RAM address from which to read the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

9.12.1.1 Read registers

NOTE The addresses of the read-only registers are mapped into the same addresses of the four write-only registers in the section above this one. They are: UART_DM_CSR, UART_DM_TF, UART_DM_CR, and UART_DM_IMR, respectively.

0x16540008 GSBI6_UART_DM_SR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_SR register is the UART status register. This register is used to obtain the current state of the UART subsystem. This register is updated asynchronously.

GSBI6_UART_DM_SR

Bits	Name	Description
8	RX_BREAK_START_LAST	When break start is detected, this bit is set (1). When break end was detected, this bit is reset (0).

GSBI6_UART_DM_SR (cont.)

Bits	Name	Description
7	HUNT_CHAR	When set (1), this bit indicates that the programmed character in the UART_DM_HCR register was received. If programmed, this condition causes the RXHUNT bit to be set (1) in the UART_DM_ISR register. This bit is cleared by issuing a reset error status command.
6	RX_BREAK	When set (1), this bit indicates that an all-zero character of the programmed length was received without a stop bit. If a break begins in the middle of a character, it is detected if the condition remains until the end of the next character time. Only one all zero character is written into the FIFO upon receiving the break. After the RX input returns high for at least half a bit time, then more characters are accepted by the receiver. Whenever the break condition starts or stops as defined above, the RXBREAK bit is set (1) in the UART_DM_ISR register. This bit is appended to the character in the receive FIFO.
5	PAR_FRAME_ERR	A parity error occurs if parity is programmed to be checked and an incoming character is received with incorrect parity. A framing error occurs when the RX input is low while the stop bit is being sampled. This bit is sampled in the middle of the first stop bit position, regardless of the programmed length of the stop bit. This error bit is appended to the character in the receive FIFO.
4	UART_OVERRUN	An overrun error occurs if one or more incoming characters are lost. This happens when the receive FIFO is full, the packing buffer is full and another character has been received in the shift register. The character in the receive shift register is lost. Upon overrun, this status bit remains high until cleared by a reset error status command.
3	TXEMT	This bit is set (1) when the transmitter under-runs. It is set after the transmission of the stop bit at the end of a character, if there are no characters waiting to be sent. It is reset when a character is written to the transmit FIFO.
2	TXRDY	This bit indicates that the transmit FIFO has space in it. It is reset when the FIFO becomes full and set when space becomes available again. Any characters that are written to the FIFO while this bit is low is lost.
1	RXFULL	This bit is set (1) when the receive FIFO becomes full. It is reset when the CPU reads a word.
0	RXRDY	This bit is set (1) when there is a word in the receive FIFO waiting to be read. It is reset when the last word currently stored in the FIFO is read.

0x16540070 GSBI6_UART_DM_RF

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RF register is the UART receive FIFO register, which is used to access the channel receive FIFO. In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM RX FIFO.

GSBI6_UART_DM_RF

Bits	Name	Description
31:0	UART_RF	This register returns the next value in the receive FIFO. After the read is completed, the FIFO read pointer is updated to make the next character available.

0x16540074 GSBI6_UART_DM_RF_2

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI6_UART_DM_RF_2

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x16540078 GSBI6_UART_DM_RF_3

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI6_UART_DM_RF_3

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x1654007C GSBI6_UART_DM_RF_4

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI6_UART_DM_RF_4

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x16540010 GSBI6_UART_DM_MISR

Type: Read
Clock: AHB_CLK
Reset State: 0x0

GSBI6_UART_DM_MISR

Bits	Name	Description
12:0	UART_MISR	The UART_DM_MISR register is the masked interrupt status register. A read from this register returns the "AND" of the UART_DM_ISR and the UART_DM_IMR registers. This register is updated asynchronously. This bit field is misr <= (isr(12 DOWNTO 7) AND imr(12 DOWNTO 7)) & '0' & (isr(5 DOWNTO 0) AND imr(5 DOWNTO 0)).

0x16540014 GSBI6_UART_DM_ISR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_ISR register is the UART interrupt status register. This register provides the current status of the possible interrupt conditions. If one of these bits is set (1), and the corresponding bit in the UART_DM_IMR register is set (1), an interrupt is generated (with the exception of bit 6, CURRENT_CTS - see the description of the UART_DM_IMR register). If the corresponding bit in the UART_DM_IMR register is clear (0), setting one of these bits has no effect on the UART interrupt request signal. This register is updated asynchronously.

GSBI6_UART_DM_ISR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	· See UART_DM_IMR on page 28-9
11	RXBREAK_END	· See UART_DM_IMR on page 28-9
10	RXBREAK_START	· See UART_DM_IMR on page 28-9
9	TX_DONE	· Bit 9 generated only when SIM_GLUE_GEN generic equals 1
8	TX_ERROR	· Bit 9 generated only when SIM_GLUE_GEN generic equals 1
7	TX_READY	See UART_DM_IMR on page 28-9, for descriptions of the UART_DM_ISR bits.
6	CURRENT_CTS	
5	DELTA_CTS	
4	RXLEV	
3	RXSTALE	

GSBI6_UART_DM_ISR (cont.)

Bits	Name	Description
2	RXBREAK	
1	RXHUNT	
0	TXLEV	

0x16540038 GSBI6_UART_DM_RX_TOTAL_SNAP

Type: Read
Clock: AHB_CLK
Reset State: 0x0

GSBI6_UART_DM_RX_TOTAL_SNAP

Bits	Name	Description
23:0	RX_TOTAL_BYTES	'RX_TOTAL_SNAP register holds the number of characters received since the end of last Rx transfer. It is updated at the end of an Rx transfer (see Software procedures). Rx transfer ends when one of the conditions is met: · The number of characters which were received since the end of the previous transfer equals the value which was written to DMRX at "Transfer initialization". · A stale event occurred (flush operation already performed if was needed).

0x1654004C GSBI6_UART_DM_TXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI6_UART_DM_TXFS

Bits	Name	Description
31:14	TX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bitfield. · Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	TX_ASYNC_FIFO_STATE	TX asynchronous fifo status - number of characters in the TX asynchronous FIFO.
9:7	TX_BUFFER_STATE	TX unpacking buffer status - number of bytes in the unpacking buffer
6:0	TX_FIFO_STATE_LSB	TX FIFO status - number of words in the TX FIFO

0x16540050 GSBI6_UART_DM_RXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI6_UART_DM_RXFS

Bits	Name	Description
31:14	RX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bitfield. Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	RX_ASYNC_FIFO_STATE	RX asynchronous fifo status - number of characters in the RX asynchronous FIFO.
9:7	RX_BUFFER_STATE	RX packing buffer status - number of bytes in the packing buffer
6:0	RX_FIFO_STATE_LSB	The number of entries in the RX FIFO that have at least one valid character. It is incremented each time a word is moved from the packing register to the RX FIFO. It is decremented each time a word is read from the RX FIFO. **NOTE** The Uart does not keep track of non-valid characters in each word. (See Software procedures).

0x16540090 GSBI6_UART_DM_TEST_RD_DATA

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI6_UART_DM_TEST_RD_DATA

Bits	Name	Description
31:0	TEST_RD_DATA	Read from this register triggers the read from the RAM. The register will hold, after read access, data which is found at TEST_RD_ADDR address in the RAM.

9.13 GSBI6 QUP Registers (0x16580000 QUP6_BASE)

This section contains the GSBI6 QUP registers.

0x16580000 GSBI6_QUP_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

a. The contents of this register should only be changed when in the RESET_STATE (see the QUP_STATE register).

b. The value written to the QUP output FIFO, is shifted left toward the MSB before passing it to the mini-core as follows:

- N equals 8 or less - shift 24
- N equals 16 to 9 - shift 16
- N equals 24 to 17 - shift 8
- N equals 32 to 25 - no shift

The MINI_CORE clock selected is as follows:

Null: cc_qup_core_clk

SPI: cc_spi_master_clk

I2C: cc_I2C_clk		

GSBI6_QUP_CONFIG

Bits	Name	Description
31:14	RESERVED_1	reserved
13	CORE_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).
12	APP_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).

GSBI6_QUP_CONFIG (cont.)

Bits	Name	Description
11:8	MINI_CORE	value: 0000 Null core value: 0001 SPI core value: 0010 I2C master controller value: 0011 I2C slave controller value: 0100 Reserved (I2C master & slave for loop back operation) value: 0101 Reserved (map to null core) value: 0110 Reserved (map to null core value: 0111 Reserved (map to null core) See Note 1.
7	NO_INPUT	qup_data_in is not used and the value is a "don't care". The QUP input FIFO is always empty. The input service interrupt and INPUT_SERVICE_FLAG bit are never set. See notes (a) and (b) above.
6	NO_OUTPUT	qup_data_out is not used and is held at the value zero. The QUP output FIFO is always empty. The output service flag and OUTPUT_SERVICE_FLAG bit are never set. qup_data_out is still driven when SPI_CS _N is asserted. The setting for NO_TRI_STATE still applies. See notes (a) and (b) above.
5	RESERVED_2	Reserved.
4:0	N	Number of logical bits N in the mini-core that constitutes a single transfer. The value zero indicates N equals one. The value of all ones indicates N equals 32. The value in this register must be 3 (i.e., N is 4 or higher in order for the STATE field to be set to RUN_STATE). See note (a) above.

0x16580004 GSBI6_QUP_STATE

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b0000000000000000_00000000000XX100

GSBI6_QUP_STATE

Bits	Name	Description
31:5	RESERVED	reserved.
4	I2C_MAST_GEN	Read only. Reflects the RTL generic setting for GEN_I2C_MASTER_MINI_CORE.
3	SPI_GEN	Read only. Reflects the RTL generic setting for GEN_SPI_MINI_CORE.
2	STATE_VALID	Read only. If and only if set to one, writes to the STATE field is allowed or reads from the STATE field is valid. Writes to this bit is ignored.

GSBI6_QUP_STATE (cont.)

Bits	Name	Description
1:0	STATE	When clear (00), the mini-core and related logic is held in RESET_STATE. When set to "01", the mini-core and related logic is released from reset and enters the RUN_STATE. When set to "11", the mini-core and related logic enters the PAUSE_STATE at the next appropriate point in time. Writing (10) to this field clears these two bits. For PAUSE_STATE to RESET_STATE transition, two writes of (10) are required for the transition to complete. See notes 1 and 2. Note 1: SPI - the "next appropriate point in time" is the next time SPI_CS _N de-asserts. If SPI_CS _N is not asserted when the PAUSE_STATE is entered, the SPI_CS _N is maintained in the not asserted state. The PAUSE_STATE is not available for SLAVE operation. Note 2: I2C -

0x16580008 GSBI6_QUP_IO_MODES

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b0000000000000000_00000000XXXXXXXX

Unless otherwise stated, register bits written return the value when read.

Notes:

a. "Packing" occurs as follows:

- N equals 8 or less - pack four values into each QUP input FIFO word.
- N equals 16 to 9 - pack two values into each QUP input FIFO word.
- N equals 32 to 17 - no packing. Each mini-core value is moved to an QUP input FIFO word.

b. "UnPacking" occurs as follows:

- N equals 8 or less - unpack four values from each QUP output FIFO word.
- N equals 16 to 9 - unpack two values from each QUP output FIFO word.
- N equals 32 to 17 - no packing. Each QUP output FIFO value is moved to the mini-core.

GSBI6_QUP_IO_MODES

Bits	Name	Description
31:17	RESERVED	reserved
16	OUTPUT_BIT_SHIFT_EN	If set, enables the QUP output FIFO block to do bit shifting on the output data.

GSBI6_QUP_IO_MODES (cont.)

Bits	Name	Description
15	PACK_EN	Indicates data values from the mini-core are to be packed before placement in the QUP input FIFO. See note (a) above.
14	UNPACK_EN	Indicates data values taken from the QUP output FIFO should be unpacked before passing to the mini-core. See note (b) above.
13:12	INPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_INPUT = 0, then only FIFO_Mode is available)
11:10	OUTPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_OUTPUT = 0, then only FIFO_Mode is available)
9:7	INPUT_FIFO_SIZE	Read only, actual value set by RTL generic. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 6x BLOCK_SIZE
6:5	INPUT_BLOCK_SIZE	Read only. Actual value set by RTL generic. Indicates the block size associated with Block_Mode and Data_Mover_Mode for input. Value 00: 4 Bytes (FIFO_Mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved
4:2	OUTPUT_FIFO_SIZE	Read only. Actual value set by RTL GENERIC. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 16 BLOCK_SIZE
1:0	OUTPUT_BLOCK_SIZE	Read only. Actual value set by RTL GENERIC. Value 00: 04 Bytes (FIFO mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved

0x1658000C GSBI6_QUP_SW_RESET

Type: Write/cmd
Clock: CRIF_CLK
Reset State: 0x0000

A write to this register resets the entire QUP core and all mini-cores. The internal registers are brought back to their reset values. Reading of this register returns zero.

GSBI6_QUP_SW_RESET

Bits	Name	Description
31:0	RESERVED	NA

0x16580010 GSBI6_QUP_TIME_OUT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies if the QUP_MX_OUTPUT_COUNT register and/or QUP_MX_INPUT_COUNT register are enabled. Additionally, this register only applies to Block_Mode and Data_Mover_Mode. The timer starts "ticking" when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The timer pauses for the PAUSE_STATE. If the timer expires before the QUP_MX_OUTPUT_COUNT and/or QUP_MX_INPUT_COUNT are exhausted, then the TIME_OUT_ERR flag is set in the QUP_ERROR_FLAGS register and the interrupt gsbi_qup_irq may be asserted.

GSBI6_QUP_TIME_OUT

Bits	Name	Description
15:0	TIME_OUT_VALUE	Specifies time out value in units of cc_qup_app clock ticks. A value of zero indicates the timer function is not enabled for use. See QUP_CONFIG register for information on clocks.

0x16580014 GSBI6_QUP_TIME_OUT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI6_QUP_TIME_OUT_CURRENT

Bits	Name	Description
31:0	TIME_OUT_CURRENT	Current value of time-out counter.

0x16580018 GSBI6_QUP_OPERATIONAL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0080

GSBI6_QUP_OPERATIONAL

Bits	Name	Description
31:10	RESERVED_1	reserved.
13	IN_BLOCK_READ_REQ	Read only. When set by hardware, indicates QUP input FIFO has BLOCK_SIZE_INPUT amount of data ready for reading. Valid only in Block_Mode.
12	OUT_BLOCK_WRITE_REQ	Read only. When set by hardware, indicates QUP output FIFO needs BLOCK_SIZE_OUTPUT amount of data to be written. Valid only in Block_Mode.
11	MAX_INPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP input FIFO has reached the programmed QUP_MX_INPUT_COUNT value. Valid in FIFO_Mode (only if MX_READ_COUNT is non-zero), Block_Mode and Data_Mover_Mode.
10	MAX_OUTPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP output FIFO has reached the programmed QUP_MX_OUTPUT_COUNT value. Valid in Block_Mode and Data_Mover_Mode.
9	INPUT_SERVICE_FLAG	When set by hardware, indicates QUP input FIFO has an outstanding input service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowleges software has or will read the data. Valid only in all modes.
8	OUTPUT_SERVICE_FLAG	When set by hardware, indicates QUP output FIFO has an outstanding output service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowledges software has or will read the data. Valid only in all modes.
7	INPUT_FIFO_FULL	Read only. When set, indicates the input FIFO is full and can accept no more data from the QUP mini-core.
6	OUTPUT_FIFO_FULL	Read only. When set, indicates the output FIFO is full and can accept no more CRIF writes.
5	INPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the input FIFO has at least one value in it to be read. When clear, indicates the input FIFO is empty.
4	OUTPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the output FIFO has at least one value in it to be shifted out. When clear, indicates the output FIFO is empty.
3:0	RESERVED_2	reserved.

0x1658001C GSBI6_QUP_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

GSBI6_QUP_ERROR_FLAGS

Bits	Name	Description
31:7	RESERVED_1	reserved.
6	TIME_OUT_ERR	The time out limit for a given transfer has been reached.
5	OUTPUT_OVER_RUN_ERR	Indicates the output FIFO was full when a CRIF write was attempted to the FIFO. The write is discarded.
4	INPUT_UNDER_RUN_ERR	Indicates the input FIFO was empty when a CRIF read was attempted to the FIFO. The read value returns is indeterminate.
3	OUTPUT_UNDER_RUN_ER R	Indicates the output FIFO was empty when an output shift operation required a value.
2	INPUT_OVER_RUN_ERR	Indicates the input FIFO was full when an input shift operation provided a new value. When this happens, the new value is discarded.
1:0	RESERVED_2	reserved

0x16580020 GSBI6_QUP_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x007C

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of gsbi_qup_irq and the setting of the corresponding error flag in the QUP_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

GSBI6_QUP_ERROR_FLAGS_EN

Bits	Name	Description
31:7	RESERVED_1	reserved
6	TIME_OUT_ERR_EN	If set, enables time out error generation.
5	OUTPUT_OVER_RUN_ERR _EN	If set, enables output over run error generation.

GSBI6_QUP_ERROR_FLAGS_EN (cont.)

Bits	Name	Description
4	INPUT_UNDER_RUN_ERR_EN	If set, enables input under run error generation.
3	OUTPUT_UNDER_RUN_ERR_EN	If set, enables output under run error generation.
2	INPUT_OVER_RUN_ERR_EN	If set, enables input over run error generation.
1:0	RESERVED_2	reserved

0x16580024 GSBI6_QUP_TEST_CTRL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register enables QUP test bus to be actively driven by QUP core signals.

GSBI6_QUP_TEST_CTRL

Bits	Name	Description
31:1	RESERVED	reserved
0	QUP_TEST_BUS_EN	If set, enables QUP core to actively drive test bus. If zero, the core drives the test bus to all zeros.

9.13.1 QUP output FIFO registers

0x16580100 GSBI6_QUP_MX_OUTPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each output transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not effect the count.

Notes:

a. Allows the total number of Mini Core transfers to be less than an exact multiple of OUTPUT_BLOCK_SIZE. Any additional outputs are discarded.

GSBI6_QUP_MX_OUTPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_COUNT	Number of writes of size N to the mini-core per RUN_STATE. A value of zero indicates the output count function is not enabled for use. See note (a) above.

0x16580104 GSBI6_QUP_MX_OUTPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI6_QUP_MX_OUTPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_CNT_CURRENT	Current value of QUP_MX_OUTPUT_COUNT.

0x16580108 GSBI6_QUP_OUTPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

This register holds the output data hanging out of the QUP output FIFO ready be loaded into the mini-core for the next load operation. This corresponds to signal qup_data_out going into the mini-core block.

GSBI6_QUP_OUTPUT_DEBUG

Bits	Name	Description
31:0	OUTPUT_DEBUG_DATA	Value waiting at the exit of output FIFO.

0x1658010C GSBI6_QUP_OUTPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the output FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the

value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

GSBI6_QUP_OUTPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	OUTPUT_FIFO_WORD_CNT	Number of words in the output FIFO.

0x16580110+4*c GSBI6_QUP_OUTPUT_FIFOc, c=[0..15]

Type: Write
Clock: CRIF_CLK
Reset State: 0x0000

Note that consecutive writes to this address keeps filling up the output FIFO. The max address to address the output FIFO is 0x14C.

GSBI6_QUP_OUTPUT_FIFOc

Bits	Name	Description
31:0	OUTPUT	Value to be shifted out.

0x16580150 GSBI6_QUP_MX_WRITE_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_OUTPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the gsbi_qup_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_OUTPUT_COUNT register case, the SW should not program the QUP_MX_WRITE_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_OUTPUT * FIFO_SIZE_OUTPUT).

GSBI6_QUP_MX_WRITE_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_COUNT	The number of "writes" of size N. This is used only if the core is in FIFO_Mode.

0x16580154 GSBI6_QUP_MX_WRITE_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI6_QUP_MX_WRITE_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_CNT_CURRENT	Current value of QUP_MX_WRITE_COUNT counter.

9.13.2 QUP input FIFO registers

0x16580200 GSBI6_QUP_MX_INPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each input transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not affect the count.

Notes:

a. Allows the number of shift register transfers to be less than an exact multiple of INPUT_BLOCK_SIZE. When count reached, remainder of INPUT_BLOCK_SIZE is filled with zeroes.

GSBI6_QUP_MX_INPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_COUNT	Number of reads of size N from the mini-core per RUN_STATE. A value of zero indicates the input count function is not enabled for use. See note (a) above.

0x16580204 GSBI6_QUP_MX_INPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI6_QUP_MX_INPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_CNT_CURRENT	Current value of QUP_MX_INPUT_COUNT.

0x16580208 GSBI6_QUP_MX_READ_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_INPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the qup_input_service_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_INPUT_COUNT register case, the SW should not program the QUP_MX_READ_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_INPUT * FIFO_SIZE_INPUT). If the SPI mini-core and slave operation is enabled, then an InputOverRun error will result.

GSBI6_QUP_MX_READ_COUNT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_COUNT	The number of "reads" of size N. This is used only if the core is in FIFO_Mode.

0x1658020C GSBI6_QUP_MX_READ_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI6_QUP_MX_READ_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_CNT_CURRENT	Current value of QUP_MX_READ_COUNT counter.

0x16580210 GSBI6_QUP_INPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the value of the last loaded in known-good-data into the QUP input FIFO. May be different from what the actual read of input FIFO will return because of packing enabled at the input side. This corresponds to signal qup_data_in coming from the mini-core block synchronized to the crif_clk.

GSBI6_QUP_INPUT_DEBUG

Bits	Name	Description
31:0	INPUT_DEBUG_DATA	Last known good value shifted into the input FIFO.

0x16580214 GSBI6_QUP_INPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the input FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

GSBI6_QUP_INPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	INPUT_FIFO_WORD_CNT	Number of words in the input FIFO.

0x16580218+4*c GSBI6_QUP_INPUT_FIFOc, c=[0..15]

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

Consecutive reads to this address reads the input FIFO contents on a FIFO basis.The max address to read the input FIFO is 0x254.

GSBI6_QUP_INPUT_FIFOc

Bits	Name	Description
31:0	INPUT	Value shifted in.

9.13.3 SPI mini-core registers

0x16580300 GSBI6_SPI_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register. Both NO_OUTPUT and NO_INPUT set to zero provides default full duplex operation. Setting both these bits to one is not a legal operational state.

GSBI6_SPI_CONFIG

Bits	Name	Description
31:11	RESERVED_1	Reserved.
10	HS_MODE	When set, SPI HS_MODE is enabled. When clear, SPI HS_MODE is disabled.
9	INPUT_FIRST	When set, INPUT FIRST SPI protocol is used. When clear, OUTPUT FIRST SPI protocol is used.
8	LOOP_BACK	Loopback is only valid in non-HS mode. Always clear for normal operation. If set, loop back on SPI_DATA_MO_SI under MASTER operation or SPI_DATA_MI_SO under SLAVE operation.
7:6	RESERVED_2	Reserved.
5	SLAVE_OPERATION	This register is writable only when the hardware signal spi_slave_en is asserted. When set, the SPI is configured for SLAVE operation. Zero indicates MASTER operation.
4:0	RESERVED	Reserved.

0x16580304 GSBI6_SPI_IO_CONTROL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register.

Unless otherwise stated, register bits written return the value when read.

GSBI6_SPI_IO_CONTROL

Bits	Name	Description
31:11	RESERVED	Reserved.
10	CLK_IDLE_HIGH	Use SPI_CLK_IDLE_HIGH when set.
9	CLK_ALWAYS_ON	When MASTER operation is used, run SPI_CLK during IDLE.
8	MX_CS_MODE	If this bit is set, then for a given RUN state, the associated chip select will be asserted for the first N-bit transfer and will be kept asserted till the last programmed transfer. Applies only in MASTER mode. The number of transfers is determined by SPI_MX_OUTPUT_COUNT and/or SPI_MX_INPUT_COUNT registers.
7:4	CS_N_POLARITY	These four bits control the polarity of four SPI_CS _N respectively. Setting any of this bit to '1', makes the associated SPI_CS _N active HIGH. This field is a "don't care" in SLAVE operation.
3:2	CS_SELECT	When MASTER operation is used, controls the assertion of SPI_CS_ N pins. Selects SPI_CS_N if 00, SPI_CS1_N if 01, SPI_CS2_N if 10, or SPI_CS3_N if 11. The deselected ChipSelects will be driven to inactive state dictated by the field CS_N_POLARITY. This field is a "don't care" in SLAVE operation.
1	TRISTATE_CS	When set, drives Z on all SPI_CS _N lines. When clear, enables normal functionality on these lines. This bit can be used to support deployment of the core as one of the masters in a multi-master configuration.
0	NO_TRI_STATE	When set, spi_data_out is not taken tri-state when SPI_CS _N is de-asserted. This bit is normally set for MASTER operation but may be optionally left cleared.

0x16580308 GSBI6_SPI_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

GSBI6_SPI_ERROR_FLAGS

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.

GSBI6_SPI_ERROR_FLAGS (cont.)

Bits	Name	Description
1	SPI_SLV_CLK_OVER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was greater than the programmed value of N. When this happens, only the first N bits are passed to the SPI input FIFO and the output shift value is held at zero.
0	SPI_SLV_CLK_UNDER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was less than the programmed value of N. When this occurs, the bits which were received are passed to the SPI input FIFO and the CURRENT output bit is forced to zero.

0x1658030C GSBI6_SPI_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0003

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of spi_error_irq and the setting of the corresponding error flag in the SPI_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

GSBI6_SPI_ERROR_FLAGS_EN

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.
1	SPI_SLV_CLK_OVER_RUN_ERR_EN	If set, enables clock over run error generation.
0	SPI_SLV_CLK_UNDER_RUN_ERR_EN	If set, enables clock under run error generation.

0x16580310 GSBI6_SPI_DEASSERT_WAIT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the de-assertion wait time of SPI_CS _N between consecutive N-bit transfers in MASTER operation. The wait time is specified in number of cycles of cc_spi_master_clk.

GSBI6_SPI_DEASSERT_WAIT

Bits	Name	Description
31:6	RESERVED	Reserved.

GSBI6_SPI_DEASSERT_WAIT (cont.)

Bits	Name	Description
5:0	DEASSERT_WAIT	Number cc_spi_master_clk ticks associated with the de-asserted time of SPI_CS _N. Only applies to MASTER operation. For SLAVE operation, this field is a "don't care". A value of zero indicates SPI_CS _N remains de-asserted for exactly one clock tick. A value of one, indicates two ticks, etc. All ones indicates 64 ticks.

9.13.4 I2C master mini-core registers

0x16580400 GSBI6_I2C_MASTER_CLK_CTL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_CLK_CTL register is a read/write register that controls clock divider values. This register should only be written to after it is confirmed that the I2C master mini-core is not longer in RESET state (QUP_STATE register).

GSBI6_I2C_MASTER_CLK_CTL

Bits	Name	Description
31:11	RESERVED	Reserved.
10:8	HS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in high-speed (HS) mode. The minimum value should be 3 hex (4 I2C_clk clocks per period) to ensure proper sampling of the bus. For a maximum high speed bit rate of 3.4 Mb/s (high speed mode), this would require a minimum 40.8 MHz I2C_clk clock. The maximum I2C_clk is 81.6 MHz. This register is reset to a maximum value of 7 hex. I2C_HS_CLK = I2C_CLK/(3*(HS_DIVIDER_VALUE+1)
7:0	FS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in fast/standard (FS) mode. The minimum value should be 3 hex to ensure proper sampling of the bus. For a maximum bit rate of 400 kb/s (fast mode), this would require a 4.8 MHz I2C_clk clock. For a maximum bit rate of 100 kb/s (standard mode), this would require a 1.2 MHz I2C_clk clock. Maximum I2C_clk for fast and standard modes are 206.4 MHz and 51.6 MHz respectively. This register is reset to a maximum value of 255 hex. I2C_FS_CLK = I2C_CLK/(2*(FS_DIVIDER_VALUE+3)

0x16580404 GSBI6_I2C_MASTER_STATUS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_STATUS is a status register. Writing a one clears the status bits.

GSBI6_I2C_MASTER_STATUS

Bits	Name	Description
31:26	RESERVED_1	Reserved.
25	INVALID_READ_SEQ	This bit is set (1) when a MI_REC tag does not follow a START tag for an I2C READ. Not applicable for Halcyon.
24	INVALID_READ_ADDR	This bit is set (1) when the I2C controller is trying to receive data from a non-existent I2C slave (address).
23	INVALID_TAG	This bit is set (1) when the I2C controller is trying to process data from the output FIFO that is improperly tagged.
22:20	INPUT_FSM_STATE	This 3-bit field informs the microprocessor of the state of the I2C MASTER INPUT FSM block. Reset, read_last_byte, mi_rec, dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: READ_LAST_BYTE_STATE Value 0x3: MI_REC_STATE Value 0x4: DEC_STATE Value 0x5: STORE_STATE
19:16	OUTPUT_FSM_STATE	This 4-bit field informs the microprocessor of the state of the I2C MASTER OUTPUT FSM block. Reset, decode, send, mi_red, nop, nop_dec, invalid, invalid_dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: DECODE_STATE Value 0x3: SEND_STATE Value 0x4: MI_REC_STATE Value 0x5: NOP_STATE Value 0x6: INVALID_STATE Value 0x7: PEEK_STATE Value 0x8: SEND_R_STATE

GSBI6_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
15:13	CLK_STATE	This 3-bit field informs the microprocessor of the state of the I2C clk_control block. Reset_busidle, not_master, high, low, high_wait, forced_low, hs_addr_low or double_buffer_wait. Value 0x0: RESET_BUSIDLE_STATE Value 0x1: NOT_MASTER_STATE Value 0x2: HIGH_STATE Value 0x3: LOW_STATE Value 0x4: HIGH_WAIT_STATE Value 0x5: FORCED_LOW_STATE Value 0x6: HS_ADDR_LOW_STATE Value 0x7: DOUBLE_BUFFER_WAIT_STATE
12:10	DATA_STATE	This 3-bit field informs the microprocessor of the state of the I2C data_control block. Reset, Tx addr, Tx HS addr, Tx 10-bit addr, Tx 2nd 10-bit addr byte, Tx data and Rx data. Value 0x0: RESET_WAIT_STATE Value 0x1: TX_ADDR_STATE Value 0x2: TX_DATA_STATE Value 0x3: TX_HS_ADDR_STATE Value 0x4: TX_10_BIT_ADDR_STATE Value 0x5: TX_2ND_BYTE_STATE Value 0x6: RX_DATA_STATE
9	BUS_MASTER	This bit is set (1) when the I2C controller is the present bus master.
8	BUS_ACTIVE	This bit is set (1) when the bus is in use by this, or any other controller.
7:6	FAILED	This 2-bit field contains the failure information of the present I2C transfers. If transmitting, failed[1] contains the information regarding the byte that has been transmitted. Failed[0] contains the information of the byte awaiting transmission if there is a byte pipelined. If no byte is pipelined, ignore this bit. If receiving, failed[1] contains the information of the byte received and stored in the buffer, and failed[0] should be ignored. For example: Value 00: Byte n transmitted successfully, byte n+1 to begin transmission Value 01: Byte n transmitted successfully, byte n+1 errored: type of error indicated in other STATUS bits. (queued invalid write, for example) Value 10: Byte n errored: type of error indicated in other STATUS bits, byte n+1 to begin transmission (byte n+1 would have to be a valid address byte for this condition to occur) Value 11: Byte n errored: type of error indicated in other STATUS bits, byte n+1 discarded as well (if the byte was a data byte destined for a NACKed address, data is useless, therefore discarded)
5	INVALID_WRITE	This bit is set (1) when software writes data to the I2C_DATA register that should be flagged as an address but is not.

GSBI6_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
4	ARB_LOST	This bit is set (1) when the controller loses arbitration for the bus. If this bit gets set (1) during the transmission, all data has been lost, and the microprocessor must re-request its transmission.
3	PACKET_NACKED	This bit is set high when a NACK is received from a slave. If a high speed master code is sent and there is an ACK from a slave, then this bit is set (1) to indicate that the high speed mode can not be entered. If the high speed mode is accepted by the slave, then a NACK is performed and this bit is not set (1).
2	BUS_ERROR	This bit is set (1) when an unexpected START or STOP condition is detected. This returns the controller to its reset state.
1:0	RESERVED_2	Reserved.

9.14 GSBI7 Registers (0x16600000 GSBI7_BASE)

This section contains the GSBI7 registers.

9.14.1 GSBI CTRL Registers

0x16600000 GSBI7_GSBI_CTRL_REG

Type: Read/write
Clock: HCLK
Reset State: 0x00000000

GSBI7_GSBI_CTRL_REG

Bits	Name	Description
15:12	RESERVED	reserved
11:8	WRAPPER_CTRL	This field has no predefined use. When a wrapper is constructed around one or more GSBIs there may be a need to configure it. E.g., to select which of several GSBIs will be connected to a particular I2S block. All bits of this field emerge from GSBI as output ports which can be used for any such configuration task.
7	RESERVED_7	Reserved. The host can write and read this field, but its state has no effect on anything.
6:4	PROTOCOL_CODE	This field controls which protocol, if any, is applied to the GSBI's four I/O ports. Most codes assign a single protocol, but codes of "001" and "110" assigns I2C to two of the ports and UART (without flow control signals) or SIM to the other two. 0x0: Idle (null values are applied to all four GSBI I/Os) 0x1: I2C on 2 ports, SIM/R-UIM on other 2 0x2: I2C 0x3: SPI 0x4: UART with flow control (or IRDA) 0x5: SIM/R-UIM 0x6: I2C on 2 ports, UART (without HS flow ctrl on other 2) 0x7: Undefined
3:1	RESERVED_3_1	Reserved. The host can write and read this field, but its state has no effect on anything.
0	CRCI_MUX_CTRL	While this bit is low QUP CRCI ports are connected to the GSBI ports nominally for QUP and UART_DM CRCI ports are connected to the GSBI ports nominally for UART_DM. While this bit is high QUP CRCI ports are connected to the GSBI ports nominally for UART_DM and UART_DM CRCI ports are connected to nothing.

0x16600004 GSBI7_GSBI_DBG0_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI7_GSBI_DBG0_REG

Bits	Name	Description
1:0	GSBI_PLAY0	This field has no function beyond the fact that the ARM can write to it and read from it.

0x16600008 GSBI7_GSBI_DBG1_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI7_GSBI_DBG1_REG

Bits	Name	Description
1:0	GSBI_PLAY1	This field has no function beyond the fact that the ARM can write to it and read from it.

0x1660000C GSBI7_GSBI_DBG2_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI7_GSBI_DBG2_REG

Bits	Name	Description
1:0	GSBI_PLAY2	This field has no function beyond the fact that the ARM can write to it and read from it.

0x16600010 GSBI7_GSBI_DBG3_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

GSBI7_GSBI_DBG3_REG

Bits	Name	Description
1:0	GSBI_PLAY3	This field has no function beyond the fact that the ARM can write to it and read from it.

9.15 GSBI7 UART DM Registers (0x16640000 GSBI7_UART_DM_BASE)

This section contains GSBI7 UART DM registers.

9.15.1 Write and read/write registers

0x16640000 GSBI7_UART_DM_MR1

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_MR1 register is the UART mode register 1. It is used, along with UART_DM_MR2, to configure the operational mode of the UART.

GSBI7_UART_DM_MR1

Bits	Name	Description
31:8	AUTO_RFR_LEVEL1	These bits are used, along with bits 5:0 (AUTO_RFR_LEVEL0) to program the level in the receive FIFO at which the RFR_N signal is de-asserted, if programmed to do so (see RX_RDY_CTL field of this register). The level counts the number of words inside the RX FIFO. It doesn't count the character that is being received (shift register) or characters in the packing buffer. This value is programmed from 1 to 2^RAM_ADDR_WIDTH. The RFR_N signal is de-asserted when the RX FIFO level (the number of characters remaining in the RX FIFO) is greater than the level that is programmed into this register. · Only RAM_ADDR_WIDTH +1:8 bits are generated.
7	RX_RDY_CTL	Setting (1) this bit enables the automatic ready-for-receiving (RFR_N) control for the receiver. RFR_N is turned off, or set (1), when a valid start bit is received and the channel FIFO is at the level programmed in bits 4 through 0 of this mode register. When the FIFO level falls back to the programmed level, the RFR_N signal is turned on, or clear (0). When this feature is off, the RFR_N signal can be used by normal signal port bit manipulation (see UART_DM_CR register).
6	CTS_CTL	When this bit is set(1), the transmitter checks the CTS_N input to determine whether to begin transmission of a new character. If CTS_N is low, the character is sent. Otherwise the transmitter continues marking until CTS_N goes low, then the next character is transmitted. A change on CTS_N during the transmission of a character has no effect on that character. When this bit is clear(0), the CTS_N input for the channel has no effect on the transmitter.
5:0	AUTO_RFR_LEVEL0	See the description of bit 8 (AUTO_RFR_LEVEL1).

0x16640004 GSBI7_UART_DM_MR2

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI7_UART_DM_MR2

Bits	Name	Description
9	RX_ERROR_CHAR_OFF	When this bit is asserted, characters with parity or framing errors don't enter RX FIFO. Otherwise they enter RX FIFO.
8	RX_BREAK_ZERO_CHAR_OFF	When this bit is asserted, the zero character received at rx_break doesn't enter RX FIFO. Otherwise it enters RX FIFO.
7	LOOPBACK	Internal use only
6	ERROR_MODE	This bit controls the operation of the two FIFO status bits for the channel (parity or framing error and received break). · When clear (0), the UART operates in character mode and the status bits apply only to the character at the top of the FIFO. · When set (1), the UART operates in block mode and both bits are the "OR" of the status for all previously received characters arriving after the last `reset error status' command was issued (see CR register).
5:4	BITS_PER_CHAR	These bits determine how many bits are transmitted or received per character, not including the start, stop, and parity bits. 0x0: 5 bits 0x1: 6 bits 0x2: 7 bits 0x3: 8 bits
3:2	STOP_BIT_LEN	This field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 9/16, 1, 1+ 9/16, and 2 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. 0x0: 0.563 (9/16 bit times) 0x1: 1.000 bit time 0x2: 1.563 (1+9/16 bit times) 0x3: 2.000 bit times
1:0	PARITY_MODE	These bits determine which parity mode is used. The user can select between odd, even, space, or no parity. 0x0: no parity 0x1: odd parity 0x2: even parity 0x3: space parity

0x16640008 GSBI7_UART_DM_CSR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_CSR register is the UART clock selection register. This register is used in conjunction with the UART M/N counter registers to determine the bit rate for the transmitter and receiver. The transmitter and receiver can be clocked at different rates.

The rates below are based on a uart_dm_clk rate of 1.8432 MHz (115.2 * 16).

Table 9-14 lists the hexadecimal values for the clock select field and the corresponding data rates.

Table 9-14 Hexadecimal values and data rates for the clock select field

CLK SEL value	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Bit rate (b/sec)	75	150	300	600	1200	2400	3600	4800	7200	9600	14.4k	19.2k	28.8k	38.4k	57.6k	115.2k

GSBI7_UART_DM_CSR

Bits	Name	Description
7:4	UART_RX_CLK_SEL	Use the CLK SEL values in Table 28-12 to select the appropriate receive and transmit bit rates.
3:0	UART_TX_CLK_SEL	

0x16640070 GSBI7_UART_DM_TF

Type: Write
Clock: AHB_CLK
Reset State: Undefined

In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM TX FIFO.

GSBI7_UART_DM_TF

Bits	Name	Description
31:0	UART_TF	The UART_TF register is the UART transmit FIFO register. This register is used to access the channel transmit FIFO. If the FIFO is full at the time of writing, the character is lost and an interrupt is generated (see UART_DM_IMR register).

0x16640074 GSBI7_UART_DM_TF_2

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI7_UART_DM_TF_2

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x16640078 GSBI7_UART_DM_TF_3

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI7_UART_DM_TF_3

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x1664007C GSBI7_UART_DM_TF_4

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI7_UART_DM_TF_4

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x16640010 GSBI7_UART_DM_CR

Type: Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_CR register is the UART command register. This register is used to issue specific commands to the UART subsystem. This register is updated asynchronously.

CAUTION Do not reset the transmitter and disable it at the same time. Do not reset the receiver and disable it at the same time.

Table 9-15 UART DM commands

Value	Description	Result
0	Null command	Does nothing.
1	Reset receiver	Resets the receiver as if a hardware reset were issued. The receiver is disabled and the FIFO, packing buffer and shift registers are flushed.
2	Reset transmitter	Resets the transmitter as if a hardware reset were issued. The transmitter signal goes high (marking) and the FIFO, unpacking register and shift register are flushed.
3	Reset error status	Clears the overrun error and hunt char received status bits in both the character and block error modes. In the block error mode, it clears the error status and received break.
4	Reset break change interrupt	Clears the break change interrupt status bit.
5	Start break	Forces the transmitter signal low. The transmitter must be enabled. If the transmitter is busy, the break is started when all characters in the transmit FIFO and the transmit shift register have been completely sent.
6	Stop break	If executed while channel is breaking, this command causes the transmitter signal to go high. The signal remains high for at least one bit time before sending out a new character.
7	Reset CTS_N	Clears ISR bit 5.
8	Reset stale interrupt	Clears the stale interrupt.
9	Packet mode	Turns on the sample data mode, which causes the receiver to sample the receive data stream at 16 times the programmed baud rate. The data is sampled with the start of the start bit, or the first data bit, and continued until the marking state. To exit this state, write 1100 in the command field.
A	test_parity_on	Internal use only.
B	test_frame_on	Internal use only.
C	Mode reset	Turns off the sample data mode.
D	Set RFR_N	Asserts the ready for receiving signal (active low).
E	Reset RFR_N	De-asserts the ready for receiving signal.
F	uart_reset_int	Internal use only.
10	Reset TX_ERROR	Clears TX_ERROR
11	Clear TX_DONE	Clears the TX_DONE interrupt (ISR bit 9)
12	Reset break start interrupt	Clears the break start interrupt status bit.
13	Reset break end interrupt	Clears the break end interrupt status bit.
14	Reset par_frame_err interrupt	Clears the par_frame_err interrupt status bit.

Table 9-16 UART DM commands

Value	Description	Result
0	Null command	Does nothing.
1	CR Protection Enable	Enables CR HW protection. When two consecutive writes to the CR are detected, the second write is delayed until the command of the first write is finished. The delay is done by de-asserting the AHB ready and this ensures that the first command completes and the second one will be executed right afterward.
2	CR Protection Disable	Disables CR HW protection. SW is responsible for managing delay between writes to the CR register.
3	Reset TX-Ready interrupt	Clears the TX_READY interrupt.
5	Enable Stale Event	Enables the `stale event' mechanism. See Software Procedures.
6	Disable Stale Event	Disables the `stale event' mechanism. See Software Procedures.
4	SW Force Stale	Causes a `stale event' (even if `stale event' is disabled). See Software Procedures.
7	RESERVED	

GSBI7_UART_DM_CR

Bits	Name	Description
11	CHANNEL_COMMAND_MSB	This is the msb of the CHANNEL_COMMAND bitfield.
10:8	GENERAL_COMMAND	Writing the appropriate value to these bits executes the commands that are listed in Table .
7:4	CHANNEL_COMMAND_LSB	Writing the appropriate value to these bits along with bit 11,executes the commands that are listed in Table 28-13.
3	UART_TX_DISABLE	This command terminates the operation of the transmitter after any character in the transmit shift register is sent.
2	UART_TX_EN	This command enables the operation of the transmitter.
1	UART_RX_DISABLE	This command immediately terminates the operation of the channel receiver and any incoming characters are lost. None of the receiver status bits are affected by this command and characters that are already in the receive FIFO remain there.
0	UART_RX_EN	This command enables the channel receiver.

0x16640014 GSBI7_UART_DM_IMR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IMR register is the UART interrupt mask register. This register is used to enable the corresponding functions in the UART_DM_ISR register. Setting (1) a bit in the

UART_DM_IMR register causes an interrupt to be generated, if the corresponding bit in the UART_DM_ISR register is set. Clearing (0) a bit in the UART_DM_IMR register causes the setting of the corresponding bit in the UART_DM_ISR register to have no effect on the interrupt signal.

Bit 6 of the UART_DM_IMR register, CURRENT_CTS, is slightly different. If the current value of the CTS is one (1), no interrupt is generated. However, the user can use bit 6 in this register to mask the CTS value when reading the UART_DM_MISR register or as a general-purpose bit.

GSBI7_UART_DM_IMR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	This bit is asserted in the same condition at which PAR_FRAME_ERR status bit is asserted. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x14.
11	RXBREAK_END	This bit is set (1) if the end of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x13.
10	RXBREAK_START	This bit is set (1) if the start of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x12.
9	TX_DONE	This bit is used only in UIM/SIM_IF mode. Set (1) this bit when the last byte in the transmitter has been sent. This bit is generated only when SIM_GLUE_GEN generic equals 1.
8	TX_ERROR	Only used in UIM_IF mode. Set (1) this bit to indicate that there has been parity error during transmission. To clear the detection logic associated with this function, write CR[11;7:4]=0x10. This bit is generated only when SIM_GLUE_GEN generic equals 1.
7	TX_READY	This bit, when set(1), indicates that: 1. TX FIFO is empty. 2. The value written in NO_CHARS_FOR_TX register equals the number of bytes written to the TX FIFO since the register was updated. **NOTE** There may be characters in the unpack buffer or in the shift register. This bit is cleared by issuing `clear TX ready' command (see UART_DM_CR register).
6	CURRENT_CTS	This bit indicates the current state of the CTS input. It never generates an interrupt.
5	DELTA_CTS	This bit, when set (1), indicates that the CTS input has changed states. To clear the detection logic associated with this function, write CR[7:4]=0x7.

GSBI7_UART_DM_IMR (cont.)

Bits	Name	Description
4	RXLEV	This bit is set when a character is loaded into the receive FIFO that brings the total number of characters in the FIFO above the programmed watermark level in the FIFO watermark register (RFWR). This bit is cleared after enough characters have been read to bring the level equal to or below the programmed watermark level.
3	RXSTALE	This bit indicates that a `stale event' occurred. See Software procedures for the exact timing of this interrupt. It is cleared by issuing a reset-stale command (see CR register).
2	RXBREAK_CHANGE	This bit is set (1) if the start or end of a break condition is detected. The logic associated with this condition is cleared (0) by writing CR[7:4]=0x4. A detected break is defined as an all-zeros character with an invalid stop bit AND LOW PARITY. The end of a break is defined as a mark condition (1) at least 1/2 bit width. A detected break occupies one position in the Rx FIFO.
1	RXHUNT	This bit is set (1) when an incoming character matches the value programmed into the UART_DM_HCR register. This condition is cleared (0) by issuing a reset error status command (CR[7:4]=0x3).
0	TXLEV	This bit is set (1) when a character which is transferred from the transmit FIFO to the transmit shift register brings the total number of characters in the FIFO below or equal to the programmed watermark level in the UART_DM_TFWR register. This bit is cleared (0) after enough characters have been written to the FIFO to bring the level above the programmed watermark level.

0x16640018 GSBI7_UART_DM_IPR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0xffffff9f

The UART_DM_IPR register is the UART interrupt programming register.

GSBI7_UART_DM_IPR

Bits	Name	Description
31:7	STALE_TIMEOUT_MSB	These bits are the STALE_TIMEOUT bitfield. The stale character time-out duration field contains a number from 1 to 2^30 -1. This number determines how many character times must elapse before a `stale event' is generated. This character time is defined as 10 times the bit rate. It is reset whenever a data bit is received. Do not clear (0) this register if the stale character time-out interrupt is enabled. Note the discontinuity in the bit assignments.

GSBI7_UART_DM_IPR (cont.)

Bits	Name	Description
6	SAMPLE_DATA	Setting (1) this bit enables the new sample data mode, which means that the start bit is sampled as well as the rest, when in sample data mode. See the CR register, CHANNEL_COMMAND bit for more information.
5	RESERVED	
4:0	STALE_TIMEOUT_LSB	This bitfield is the LSbits of the STALE_TIMEOUT bitfield.

0x1664001C GSBI7_UART_DM_TFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_TFWR register is the UART transmit FIFO watermark register.

GSBI7_UART_DM_TFWR

Bits	Name	Description
31:0	TFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the transmit FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of TX words in the FIFO) is less than or equal to the value in TFWR. See UART_DM_IMR register. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x16640020 GSBI7_UART_DM_RFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RFWR register is the UART receive FIFO watermark register.

GSBI7_UART_DM_RFWR

Bits	Name	Description
31:0	RFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the receive FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of words in the RX FIFO) is greater than the value in RFWR. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x16640024 GSBI7_UART_DM_HCR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI7_UART_DM_HCR

Bits	Name	Description
7:0	DATA	The UART_DM_HCR register is the UART hunt character register, which contains the character for which the receiver looks to assert a hunt character received interrupt.

0x16640034 GSBI7_UART_DM_DMRX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI7_UART_DM_DMRX

Bits	Name	Description
24:0	RX_DM_CRCI_CHARS	In the DM mode, the number of chars in the Rx FIFO that are used for CRCI handshake with the DM. The written value of RX_DM_CRCI_ CHARS must be a multiple of 16(bits [3:0] are treated as 0x0). After a value is written, the UART will generate CRCI requests as long as RX_DM_CRCI_CHARS is non zero. Read of DMRX register gives the number of characters that were received since the end of the last transfer. It is reset at the end of each Rx transfer Also is used by the software to indicate `transfer initialization'. See Software procedures.

0x16640038 GSBI7_UART_DM_IRDA

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IRDA register enables the IRDA function, selects a loopback, and allows inversion of RX and TX data. This register also controls the IRDA transceiver that optionally interfaces between the UART and the DP_RX_DATA and DP_TX_DATA pins.

The UART proper is a standard RX/TX configuration that converts the serial pin input and output lines to 8-bit data for the microprocessor. The configuration contains receive and transmit blocks, a control block, a bit rate generator for RX and TX, and FIFO interfaces with the microprocessor data bus. The IRDA register provides the means of switching IRDA circuits into the serial I/O lines and the IRDA function is normally switched out. The IRDA modulator/demodulator may be

enabled or disabled under microprocessor control. When enabled, the RX and TX data pathis have individual inversion select bits, so external true or inverted drivers may be used in the signal path.

n The register is generated only when IRDA_IFC_GEN generic equals 1.

GSBI7_UART_DM_IRDA

Bits	Name	Description
4	MEDIUM_RATE_EN	· Set (1) for 1/4 bit-time pulse length (Medium rate) · Clear (0) for 3/16 bit-time pulse length (Low rate)
3	IRDA_LOOPBACK	· This bit loops the IRDA modulated TX line back into the IRDA RX line. The normal UART loopback mode must be off in order to see this effect.
2	INVERT_IRDA_TX	This bit inverts the polarity of the IRDA modulated signal on the DP_TX_DATA pin. · Set (1) this bit for an inverted polarity. · Clear (0) this bit for a non-inverted polarity.
1	INVERT_IRDA_RX	This bit inverts the polarity of the IRDA received signal on the DP_RX_DATA pin. · Set (1) this bit for inverted the polarity. · Clear (0) this bit for non-inverted polarity.
0	IRDA_EN	· Set (1) this bit to enable the IRDA transceiver. · Clear (0) this bit to bypass the IRDA transceiver and ignore the other bits of this register.

0x1664003C GSBI7_UART_DM_DMEN

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_DMEN register indicates if Data Mover is enabled for TX and RX channels.

GSBI7_UART_DM_DMEN

Bits	Name	Description
1	RX_DM_EN	· Set (1) this bit to enable RX DM interface. · Clear (0) this bit to disable RX DM interface. Clearing this bit requires resetting the receiver (see UART_DM_CR register).
0	TX_DM_EN	Set (1) this bit to enable TX DM interface. Clear (0) this bit to disable TX DM interface.

0x16640040 GSBI7_UART_DM_NO_CHARS_FOR_TX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI7_UART_DM_NO_CHARS_FOR_TX

Bits	Name	Description
23:0	TX_TOTAL_TRANS_LEN	The total number of characters for transmission. Before writing a new value, the TX FIFO must be empty (as indicated by TX_READY interrupt in IMR register or after a reset). It is used by the transmitter to calculate how many characters to transmit in the last word. In DM mode, it is also used for the CRCI mechanism. Any additional writes to the TX FIFO above TX_TOTAL_TRANS_LEN will be discarded. A TX_READY interrupt is triggered after TX_TOTAL_TRANS_LEN number of characters were moved from the TX FIFO to the unpacking register (not all may have been sent).

0x16640044 GSBI7_UART_DM_BADR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

GSBI7_UART_DM_BADR

Bits	Name	Description
31:2	RX_BASE_ADDR	RX FIFO base address. Both FIFOs use the same RAM (2^RAM_ADDR_WIDTH, 32-bit entries). This register controls the division of the memory to the RX and TX FIFOs. The division is a multiple of 4 entries, since the DM's burst length is 4. The size of the TX FIFO equals RX_BASE_ADDR. The size of the RX FIFO is 2^RAM_ADDR_WIDTH - RX_BASE_ADDR. ® The default is RX_BASE_ADDR = 2^(RAM_ADDR_WIDTH - 1) ® Only RAM_ADDR_WIDTH -1:2 bits are generated.
1:0	UNUSED	

0x16640048 GSBI7_UART_DM_TESTSL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI7_UART_DM_TESTSL

Bits	Name	Description
4	TEST_EN	Test bus enable
3:0	TEST_SEL	Test bus selector

0x16640060 GSBI7_UART_DM_MISR_MODE

Type: Read/Write
Clock: WR_CLK

GSBI7_UART_DM_MISR_MODE

Bits	Name	Description
31:2	RESERVED	unused.
1:0	MODE	0x0: Disabled 0x1: Enabled,TX test 0x2: Enabled, RX test

0x16640064 GSBI7_UART_DM_MISR_RESET

Type: Write
Clock: WR_CLK
Reset State: Undefined

GSBI7_UART_DM_MISR_RESET

Bits	Name	Description
31:1	RESERVED	unused.
0	RESET	

0x16640068 GSBI7_UART_DM_MISR_EXPORT

Type: Read/Write
Clock: WR_CLK
Reset State: Undefined

GSBI7_UART_DM_MISR_EXPORT

Bits	Name	Description
31:1	RESERVED	unused.

GSBI7_UART_DM_MISR_EXPORT (cont.)

Bits	Name	Description
0	EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., what is the result of the muxing of all the input data streams with <BLOCK>_TEST_MODE) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x1664006C GSBI7_UART_DM_MISR_VAL

Type: Read
Clock: WR_CLK
Reset State: Undefined

GSBI7_UART_DM_MISR_VAL

Bits	Name	Description
9:0	VAL	Current MISR state

0x16640080 GSBI7_UART_DM_SIM_CFG

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_SIM_CFG register is used to configure the SIM interface for the UART.

- The register is generated only when SIM_GLUE_GEN generic equals 1.

GSBI7_UART_DM_SIM_CFG

Bits	Name	Description
17	UIM_TX_MODE	When this bit is set (1), the transmission portion of the SIM interface operates in block mode (T=1). When clear (0), the transmission portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.
16	UIM_RX_MODE	When this bit is set (1), the receive portion of the SIM interface operates in block mode (T=1). When clear (0), the receive portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.

GSBI7_UART_DM_SIM_CFG (cont.)

Bits	Name	Description
15:8	SIM_STOP_BIT_LEN	In UIM_IF mode, this field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 1 to 254 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. ..... 11 111110: 254 bit times 0x1: 1 bit times 0x2: 2 bit times
7	SIM_CLK_ON	When this bit is set(1), the UIM_CLK is turned on at either the TD8 or TD4 frequency, as indicated by bit6(UIM_CLK_TD8_SEL). When this bit is cleared, the UIM_CLK is stopped either LOW or HIGH, as indicated by bit 5(UIM_CLK_STOP_HIGH).
6	SIM_CLK_TD8_SEL	This bit selects the UIM_CLK frequency at which the UIM_CLK is turned on. 0x1: TD8 (the UIM_CLK runs at the TD8 frequency) 0x0: TD4 (the UIM_CLK runs at the TD4 frequency)
5	SIM_CLK_STOP_HIGH	This bit indicates at what point - high or low - the UIM_CLK will stop. 0x1: high 0x0: low
4	SIM_CLK_SEL	unused
3	MASK_RX	Setting (1) this bit masks off any 0 on the RX line, which prevents the receiver from seeing the START bit. Set (1) this bit if you do not want to receive the data you transmit.
2	SWAP_D	Setting (1) this bit causes the UIM_IF to swap the 8 data bits (making MSB into LSB, bit 6 into bit1, and so on) before it is read by the microprocessor.
1	INV_D	Set (1) this bit to cause the UIM_IF to invert the 8 data bit before it is read by the microprocessor.
0	SIM_SEL	Set (1) this bit to designate the UIM_IF mode of operation.

0x16640084 GSBI7_UART_DM_TEST_WR_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI7_UART_DM_TEST_WR_ADDR

Bits	Name	Description
31:0	TEST_WR_ADDR	RAM address at which to write the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x16640088 GSBI7_UART_DM_TEST_WR_DATA

Type: Write
Clock: AHB_CLK
Reset State: Undefined

GSBI7_UART_DM_TEST_WR_DATA

Bits	Name	Description
31:0	TEST_WR_DATA	The test data to be written to the RAM. Write to this register triggers the write to the RAM, to TEST_WR_ADDR address.

0x1664008C GSBI7_UART_DM_TEST_RD_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

GSBI7_UART_DM_TEST_RD_ADDR

Bits	Name	Description
31:0	TEST_RD_ADDR	RAM address from which to read the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

9.15.2 Read registers

NOTE The addresses of the read-only registers are mapped into the same addresses of the four write-only registers in the section above this one. They are: UART_DM_CSR, UART_DM_TF, UART_DM_CR, and UART_DM_IMR, respectively.

0x16640008 GSBI7_UART_DM_SR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_SR register is the UART status register. This register is used to obtain the current state of the UART subsystem. This register is updated asynchronously.

GSBI7_UART_DM_SR

Bits	Name	Description
8	RX_BREAK_START_LAST	When break start is detected, this bit is set (1). When break end was detected, this bit is reset (0).

GSBI7_UART_DM_SR (cont.)

Bits	Name	Description
7	HUNT_CHAR	When set (1), this bit indicates that the programmed character in the UART_DM_HCR register was received. If programmed, this condition causes the RXHUNT bit to be set (1) in the UART_DM_ISR register. This bit is cleared by issuing a reset error status command.
6	RX_BREAK	When set (1), this bit indicates that an all-zero character of the programmed length was received without a stop bit. If a break begins in the middle of a character, it is detected if the condition remains until the end of the next character time. Only one all zero character is written into the FIFO upon receiving the break. After the RX input returns high for at least half a bit time, then more characters are accepted by the receiver. Whenever the break condition starts or stops as defined above, the RXBREAK bit is set (1) in the UART_DM_ISR register. This bit is appended to the character in the receive FIFO.
5	PAR_FRAME_ERR	A parity error occurs if parity is programmed to be checked and an incoming character is received with incorrect parity. A framing error occurs when the RX input is low while the stop bit is being sampled. This bit is sampled in the middle of the first stop bit position, regardless of the programmed length of the stop bit. This error bit is appended to the character in the receive FIFO.
4	UART_OVERRUN	An overrun error occurs if one or more incoming characters are lost. This happens when the receive FIFO is full, the packing buffer is full and another character has been received in the shift register. The character in the receive shift register is lost. Upon overrun, this status bit remains high until cleared by a reset error status command.
3	TXEMT	This bit is set (1) when the transmitter under-runs. It is set after the transmission of the stop bit at the end of a character, if there are no characters waiting to be sent. It is reset when a character is written to the transmit FIFO.
2	TXRDY	This bit indicates that the transmit FIFO has space in it. It is reset when the FIFO becomes full and set when space becomes available again. Any characters that are written to the FIFO while this bit is low is lost.
1	RXFULL	This bit is set (1) when the receive FIFO becomes full. It is reset when the CPU reads a word.
0	RXRDY	This bit is set (1) when there is a word in the receive FIFO waiting to be read. It is reset when the last word currently stored in the FIFO is read.

0x16640070 GSBI7_UART_DM_RF

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RF register is the UART receive FIFO register, which is used to access the channel receive FIFO. In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM RX FIFO.

GSBI7_UART_DM_RF

Bits	Name	Description
31:0	UART_RF	This register returns the next value in the receive FIFO. After the read is completed, the FIFO read pointer is updated to make the next character available.

0x16640074 GSBI7_UART_DM_RF_2

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI7_UART_DM_RF_2

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x16640078 GSBI7_UART_DM_RF_3

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI7_UART_DM_RF_3

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x1664007C GSBI7_UART_DM_RF_4

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI7_UART_DM_RF_4

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x16640010 GSBI7_UART_DM_MISR

Type: Read
Clock: AHB_CLK
Reset State: 0x0

GSBI7_UART_DM_MISR

Bits	Name	Description
12:0	UART_MISR	The UART_DM_MISR register is the masked interrupt status register. A read from this register returns the "AND" of the UART_DM_ISR and the UART_DM_IMR registers. This register is updated asynchronously. This bit field is misr <= (isr(12 DOWNTO 7) AND imr(12 DOWNTO 7)) & '0' & (isr(5 DOWNTO 0) AND imr(5 DOWNTO 0)).

0x16640014 GSBI7_UART_DM_ISR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_ISR register is the UART interrupt status register. This register provides the current status of the possible interrupt conditions. If one of these bits is set (1), and the corresponding bit in the UART_DM_IMR register is set (1), an interrupt is generated (with the exception of bit 6, CURRENT_CTS - see the description of the UART_DM_IMR register). If the corresponding bit in the UART_DM_IMR register is clear (0), setting one of these bits has no effect on the UART interrupt request signal. This register is updated asynchronously.

GSBI7_UART_DM_ISR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	· See UART_DM_IMR on page 28-9
11	RXBREAK_END	· See UART_DM_IMR on page 28-9
10	RXBREAK_START	· See UART_DM_IMR on page 28-9
9	TX_DONE	· Bit 9 generated only when SIM_GLUE_GEN generic equals 1
8	TX_ERROR	· Bit 9 generated only when SIM_GLUE_GEN generic equals 1
7	TX_READY	See UART_DM_IMR on page 28-9, for descriptions of the UART_DM_ISR bits.
6	CURRENT_CTS	
5	DELTA_CTS	
4	RXLEV	
3	RXSTALE	

GSBI7_UART_DM_ISR (cont.)

Bits	Name	Description
2	RXBREAK	
1	RXHUNT	
0	TXLEV	

0x16640038 GSBI7_UART_DM_RX_TOTAL_SNAP

Type: Read
Clock: AHB_CLK
Reset State: 0x0

GSBI7_UART_DM_RX_TOTAL_SNAP

Bits	Name	Description
23:0	RX_TOTAL_BYTES	'RX_TOTAL_SNAP register holds the number of characters received since the end of last Rx transfer. It is updated at the end of an Rx transfer (see Software procedures). Rx transfer ends when one of the conditions is met: · The number of characters which were received since the end of the previous transfer equals the value which was written to DMRX at "Transfer initialization". · A stale event occurred (flush operation already performed if was needed).

0x1664004C GSBI7_UART_DM_TXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI7_UART_DM_TXFS

Bits	Name	Description
31:14	TX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bitfield. · Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	TX_ASYNC_FIFO_STATE	TX asynchronous fifo status - number of characters in the TX asynchronous FIFO.
9:7	TX_BUFFER_STATE	TX unpacking buffer status - number of bytes in the unpacking buffer
6:0	TX_FIFO_STATE_LSB	TX FIFO status - number of words in the TX FIFO

0x16640050 GSBI7_UART_DM_RXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI7_UART_DM_RXFS

Bits	Name	Description
31:14	RX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bitfield. Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	RX_ASYNC_FIFO_STATE	RX asynchronous fifo status - number of characters in the RX asynchronous FIFO.
9:7	RX_BUFFER_STATE	RX packing buffer status - number of bytes in the packing buffer
6:0	RX_FIFO_STATE_LSB	The number of entries in the RX FIFO that have at least one valid character. It is incremented each time a word is moved from the packing register to the RX FIFO. It is decremented each time a word is read from the RX FIFO. **NOTE** The Uart does not keep track of non-valid characters in each word. (See Software procedures).

0x16640090 GSBI7_UART_DM_TEST_RD_DATA

Type: Read
Clock: AHB_CLK
Reset State: Undefined

GSBI7_UART_DM_TEST_RD_DATA

Bits	Name	Description
31:0	TEST_RD_DATA	Read from this register triggers the read from the RAM. The register will hold, after read access, data which is found at TEST_RD_ADDR address in the RAM.

9.16 GSBI7 QUP Registers (0x16680000 QUP7_BASE)

This section contains the GSBI7 QUP registers.

0x16680000 GSBI7_QUP_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

a. The contents of this register should only be changed when in the RESET_STATE (see the QUP_STATE register).

b. The value written to the QUP output FIFO, is shifted left toward the MSB before passing it to the mini-core as follows:

- N equals 8 or less - shift 24
- N equals 16 to 9 - shift 16
- N equals 24 to 17 - shift 8
- N equals 32 to 25 - no shift

The MINI_CORE clock selected is as follows:

Null: cc_qup_core_clk

SPI: cc_spi_master_clk

I2C: cc_I2C_clk		

GSBI7_QUP_CONFIG

Bits	Name	Description
31:14	RESERVED_1	reserved
13	CORE_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).
12	APP_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).

GSBI7_QUP_CONFIG (cont.)

Bits	Name	Description
11:8	MINI_CORE	value: 0000 Null core value: 0001 SPI core value: 0010 I2C master controller value: 0011 I2C slave controller value: 0100 Reserved (I2C master & slave for loop back operation) value: 0101 Reserved (map to null core) value: 0110 Reserved (map to null core value: 0111 Reserved (map to null core) See Note 1.
7	NO_INPUT	qup_data_in is not used and the value is a "don't care". The QUP input FIFO is always empty. The input service interrupt and INPUT_SERVICE_FLAG bit are never set. See notes (a) and (b) above.
6	NO_OUTPUT	qup_data_out is not used and is held at the value zero. The QUP output FIFO is always empty. The output service flag and OUTPUT_SERVICE_FLAG bit are never set. qup_data_out is still driven when SPI_CS _N is asserted. The setting for NO_TRI_STATE still applies. See notes (a) and (b) above.
5	RESERVED_2	Reserved.
4:0	N	Number of logical bits N in the mini-core that constitutes a single transfer. The value zero indicates N equals one. The value of all ones indicates N equals 32. The value in this register must be 3 (i.e., N is 4 or higher in order for the STATE field to be set to RUN_STATE). See note (a) above.

0x16680004 GSBI7_QUP_STATE

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b0000000000000000_00000000000XX100

GSBI7_QUP_STATE

Bits	Name	Description
31:5	RESERVED	reserved.
4	I2C_MAST_GEN	Read only. Reflects the RTL generic setting for GEN_I2C_MASTER_MINI_CORE.
3	SPI_GEN	Read only. Reflects the RTL generic setting for GEN_SPI_MINI_CORE.
2	STATE_VALID	Read only. If and only if set to one, writes to the STATE field is allowed or reads from the STATE field is valid. Writes to this bit is ignored.

GSBI7_QUP_STATE (cont.)

Bits	Name	Description
1:0	STATE	When clear (00), the mini-core and related logic is held in RESET_STATE. When set to "01", the mini-core and related logic is released from reset and enters the RUN_STATE. When set to "11", the mini-core and related logic enters the PAUSE_STATE at the next appropriate point in time. Writing (10) to this field clears these two bits. For PAUSE_STATE to RESET_STATE transition, two writes of (10) are required for the transition to complete. See notes 1 and 2. Note 1: SPI - the "next appropriate point in time" is the next time SPI_CS _N de-asserts. If SPI_CS _N is not asserted when the PAUSE_STATE is entered, the SPI_CS _N is maintained in the not asserted state. The PAUSE_STATE is not available for SLAVE operation. Note 2: I2C -

0x16680008 GSBI7_QUP_IO_MODES

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b000000000000000_00000000XXXXXXXX

Unless otherwise stated, register bits written return the value when read.

Notes:

a. "Packing" occurs as follows:

- N equals 8 or less - pack four values into each QUP input FIFO word.
- N equals 16 to 9 - pack two values into each QUP input FIFO word.
- N equals 32 to 17 - no packing. Each mini-core value is moved to an QUP input FIFO word.

b. "UnPacking" occurs as follows:

- N equals 8 or less - unpack four values from each QUP output FIFO word.
- N equals 16 to 9 - unpack two values from each QUP output FIFO word.
- N equals 32 to 17 - no packing. Each QUP output FIFO value is moved to the mini-core.

GSBI7_QUP_IO_MODES

Bits	Name	Description
31:17	RESERVED	reserved
16	OUTPUT_BIT_SHIFT_EN	If set, enables the QUP output FIFO block to do bit shifting on the output data.

GSBI7_QUP_IO_MODES (cont.)

Bits	Name	Description
15	PACK_EN	Indicates data values from the mini-core are to be packed before placement in the QUP input FIFO. See note (a) above.
14	UNPACK_EN	Indicates data values taken from the QUP output FIFO should be unpacked before passing to the mini-core. See note (b) above.
13:12	INPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_INPUT = 0, then only FIFO_Mode is available)
11:10	OUTPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_OUTPUT = 0, then only FIFO_Mode is available)
9:7	INPUT_FIFO_SIZE	Read only, actual value set by RTL generic. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 6x BLOCK_SIZE
6:5	INPUT_BLOCK_SIZE	Read only. Actual value set by RTL generic. Indicates the block size associated with Block_Mode and Data_Mover_Mode for input. Value 00: 4 Bytes (FIFO_Mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved
4:2	OUTPUT_FIFO_SIZE	Read only. Actual value set by RTL GENERIC. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 16 BLOCK_SIZE
1:0	OUTPUT_BLOCK_SIZE	Read only. Actual value set by RTL GENERIC. Value 00: 04 Bytes (FIFO mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved

0x1668000C GSBI7_QUP_SW_RESET

Type: Write/cmd
Clock: CRIF_CLK
Reset State: 0x0000

A write to this register resets the entire QUP core and all mini-cores. The internal registers are brought back to their reset values. Reading of this register returns zero.

GSBI7_QUP_SW_RESET

Bits	Name	Description
31:0	RESERVED	NA

0x16680010 GSBI7_QUP_TIME_OUT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies if the QUP_MX_OUTPUT_COUNT register and/or QUP_MX_INPUT_COUNT register are enabled. Additionally, this register only applies to Block_Mode and Data_Mover_Mode. The timer starts "ticking" when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The timer pauses for the PAUSE_STATE. If the timer expires before the QUP_MX_OUTPUT_COUNT and/or QUP_MX_INPUT_COUNT are exhausted, then the TIME_OUT_ERR flag is set in the QUP_ERROR_FLAGS register and the interrupt gsbi_qup_irq may be asserted.

GSBI7_QUP_TIME_OUT

Bits	Name	Description
15:0	TIME_OUT_VALUE	Specifies time out value in units of cc_qup_app clock ticks. A value of zero indicates the timer function is not enabled for use. See QUP_CONFIG register for information on clocks.

0x16680014 GSBI7_QUP_TIME_OUT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI7_QUP_TIME_OUT_CURRENT

Bits	Name	Description
31:0	TIME_OUT_CURRENT	Current value of time-out counter.

0x16680018 GSBI7_QUP_OPERATIONAL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0080

GSBI7_QUP_OPERATIONAL

Bits	Name	Description
31:10	RESERVED_1	reserved.
13	IN_BLOCK_READ_REQ	Read only. When set by hardware, indicates QUP input FIFO has BLOCK_SIZE_INPUT amount of data ready for reading. Valid only in Block_Mode.
12	OUT_BLOCK_WRITE_REQ	Read only. When set by hardware, indicates QUP output FIFO needs BLOCK_SIZE_OUTPUT amount of data to be written. Valid only in Block_Mode.
11	MAX_INPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP input FIFO has reached the programmed QUP_MX_INPUT_COUNT value. Valid in FIFO_Mode (only if MX_READ_COUNT is non-zero), Block_Mode and Data_Mover_Mode.
10	MAX_OUTPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP output FIFO has reached the programmed QUP_MX_OUTPUT_COUNT value. Valid in Block_Mode and Data_Mover_Mode.
9	INPUT_SERVICE_FLAG	When set by hardware, indicates QUP input FIFO has an outstanding input service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowleges software has or will read the data. Valid only in all modes.
8	OUTPUT_SERVICE_FLAG	When set by hardware, indicates QUP output FIFO has an outstanding output service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowledges software has or will read the data. Valid only in all modes.
7	INPUT_FIFO_FULL	Read only. When set, indicates the input FIFO is full and can accept no more data from the QUP mini-core.
6	OUTPUT_FIFO_FULL	Read only. When set, indicates the output FIFO is full and can accept no more CRIF writes.
5	INPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the input FIFO has at least one value in it to be read. When clear, indicates the input FIFO is empty.
4	OUTPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the output FIFO has at least one value in it to be shifted out. When clear, indicates the output FIFO is empty.
3:0	RESERVED_2	reserved.

0x1668001C GSBI7_QUP_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

GSBI7_QUP_ERROR_FLAGS

Bits	Name	Description
31:7	RESERVED_1	reserved.
6	TIME_OUT_ERR	The time out limit for a given transfer has been reached.
5	OUTPUT_OVER_RUN_ERR	Indicates the output FIFO was full when a CRIF write was attempted to the FIFO. The write is discarded.
4	INPUT_UNDER_RUN_ERR	Indicates the input FIFO was empty when a CRIF read was attempted to the FIFO. The read value returns is indeterminate.
3	OUTPUT_UNDER_RUN_ER R	Indicates the output FIFO was empty when an output shift operation required a value.
2	INPUT_OVER_RUN_ERR	Indicates the input FIFO was full when an input shift operation provided a new value. When this happens, the new value is discarded.
1:0	RESERVED_2	reserved

0x16680020 GSBI7_QUP_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x007C

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of gsbi_qup_irq and the setting of the corresponding error flag in the QUP_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

GSBI7_QUP_ERROR_FLAGS_EN

Bits	Name	Description
31:7	RESERVED_1	reserved
6	TIME_OUT_ERR_EN	If set, enables time out error generation.
5	OUTPUT_OVER_RUN_ERR _EN	If set, enables output over run error generation.

GSBI7_QUP_ERROR_FLAGS_EN (cont.)

Bits	Name	Description
4	INPUT_UNDER_RUN_ERR_EN	If set, enables input under run error generation.
3	OUTPUT_UNDER_RUN_ERR_EN	If set, enables output under run error generation.
2	INPUT_OVER_RUN_ERR_EN	If set, enables input over run error generation.
1:0	RESERVED_2	reserved

0x16680024 GSBI7_QUP_TEST_CTRL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register enables QUP test bus to be actively driven by QUP core signals.

GSBI7_QUP_TEST_CTRL

Bits	Name	Description
31:1	RESERVED	reserved
0	QUP_TEST_BUS_EN	If set, enables QUP core to actively drive test bus. If zero, the core drives the test bus to all zeros.

9.16.1 QUP output FIFO registers

0x16680100 GSBI7_QUP_MX_OUTPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each output transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not effect the count.

Notes:

a. Allows the total number of Mini Core transfers to be less than an exact multiple of OUTPUT_BLOCK_SIZE. Any additional outputs are discarded.

GSBI7_QUP_MX_OUTPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_COUNT	Number of writes of size N to the mini-core per RUN_STATE. A value of zero indicates the output count function is not enabled for use. See note (a) above.

0x16680104 GSBI7_QUP_MX_OUTPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI7_QUP_MX_OUTPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_CNT_CURRENT	Current value of QUP_MX_OUTPUT_COUNT.

0x16680108 GSBI7_QUP_OUTPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

This register holds the output data hanging out of the QUP output FIFO ready be loaded into the mini-core for the next load operation. This corresponds to signal qup_data_out going into the mini-core block.

GSBI7_QUP_OUTPUT_DEBUG

Bits	Name	Description
31:0	OUTPUT_DEBUG_DATA	Value waiting at the exit of output FIFO.

0x1668010C GSBI7_QUP_OUTPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the output FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the

value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

GSBI7_QUP_OUTPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	OUTPUT_FIFO_WORD_CNT	Number of words in the output FIFO.

0x16680110+4*c GSBI7_QUP_OUTPUT_FIFOc, c=[0..15]

Type: Write
Clock: CRIF_CLK
Reset State: 0x0000

Note that consecutive writes to this address keeps filling up the output FIFO. The max address to address the output FIFO is 0x14C.

GSBI7_QUP_OUTPUT_FIFOc

Bits	Name	Description
31:0	OUTPUT	Value to be shifted out.

0x16680150 GSBI7_QUP_MX_WRITE_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_OUTPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the gsbi_qup_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_OUTPUT_COUNT register case, the SW should not program the QUP_MX_WRITE_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_OUTPUT * FIFO_SIZE_OUTPUT).

GSBI7_QUP_MX_WRITE_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_COUNT	The number of "writes" of size N. This is used only if the core is in FIFO_Mode.

0x16680154 GSBI7_QUP_MX_WRITE_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI7_QUP_MX_WRITE_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_CNT_CURRENT	Current value of QUP_MX_WRITE_COUNT counter.

9.16.2 QUP input FIFO registers

0x16680200 GSBI7_QUP_MX_INPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each input transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not affect the count.

Notes:

a. Allows the number of shift register transfers to be less than an exact multiple of INPUT_BLOCK_SIZE. When count reached, remainder of INPUT_BLOCK_SIZE is filled with zeroes.

GSBI7_QUP_MX_INPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_COUNT	Number of reads of size N from the mini-core per RUN_STATE. A value of zero indicates the input count function is not enabled for use. See note (a) above.

0x16680204 GSBI7_QUP_MX_INPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI7_QUP_MX_INPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_CNT_CURRENT	Current value of QUP_MX_INPUT_COUNT.

0x16680208 GSBI7_QUP_MX_READ_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_INPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the qup_input_service_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_INPUT_COUNT register case, the SW should not program the QUP_MX_READ_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_INPUT * FIFO_SIZE_INPUT). If the SPI mini-core and slave operation is enabled, then an InputOverRun error will result.

GSBI7_QUP_MX_READ_COUNT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_COUNT	The number of "reads" of size N. This is used only if the core is in FIFO_Mode.

0x1668020C GSBI7_QUP_MX_READ_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

GSBI7_QUP_MX_READ_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_CNT_CURRENT	Current value of QUP_MX_READ_COUNT counter.

0x16680210 GSBI7_QUP_INPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the value of the last loaded in known-good-data into the QUP input FIFO. May be different from what the actual read of input FIFO will return because of packing enabled at the input side. This corresponds to signal qup_data_in coming from the mini-core block synchronized to the crif_clk.

GSBI7_QUP_INPUT_DEBUG

Bits	Name	Description
31:0	INPUT_DEBUG_DATA	Last known good value shifted into the input FIFO.

0x16680214 GSBI7_QUP_INPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the input FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

GSBI7_QUP_INPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	INPUT_FIFO_WORD_CNT	Number of words in the input FIFO.

0x16680218+4*c GSBI7_QUP_INPUT_FIFOc, c=[0..15]

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

Consecutive reads to this address reads the input FIFO contents on a FIFO basis.The max address to read the input FIFO is 0x254.

GSBI7_QUP_INPUT_FIFOc

Bits	Name	Description
31:0	INPUT	Value shifted in.

9.16.3 SPI mini-core registers

0x16680300 GSBI7_SPI_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register. Both NO_OUTPUT and NO_INPUT set to zero provides default full duplex operation. Setting both these bits to one is not a legal operational state.

GSBI7_SPI_CONFIG

Bits	Name	Description
31:11	RESERVED_1	Reserved.
10	HS_MODE	When set, SPI HS_MODE is enabled. When clear, SPI HS_MODE is disabled.
9	INPUT_FIRST	When set, INPUT FIRST SPI protocol is used. When clear, OUTPUT FIRST SPI protocol is used.
8	LOOP_BACK	Loopback is only valid in non-HS mode. Always clear for normal operation. If set, loop back on SPI_DATA_MO_SI under MASTER operation or SPI_DATA_MI_SO under SLAVE operation.
7:6	RESERVED_2	Reserved.
5	SLAVE_OPERATION	This register is writable only when the hardware signal spi_slave_en is asserted. When set, the SPI is configured for SLAVE operation. Zero indicates MASTER operation.
4:0	RESERVED	Reserved.

0x16680304 GSBI7_SPI_IO_CONTROL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register.

Unless otherwise stated, register bits written return the value when read.

GSBI7_SPI_IO_CONTROL

Bits	Name	Description
31:11	RESERVED	Reserved.
10	CLK_IDLE_HIGH	Use SPI_CLK_IDLE_HIGH when set.
9	CLK_ALWAYS_ON	When MASTER operation is used, run SPI_CLK during IDLE.
8	MX_CS_MODE	If this bit is set, then for a given RUN state, the associated chip select will be asserted for the first N-bit transfer and will be kept asserted till the last programmed transfer. Applies only in MASTER mode. The number of transfers is determined by SPI_MX_OUTPUT_COUNT and/or SPI_MX_INPUT_COUNT registers.
7:4	CS_N_POLARITY	These four bits control the polarity of four SPI_CS _N respectively. Setting any of this bit to '1', makes the associated SPI_CS _N active HIGH. This field is a "don't care" in SLAVE operation.
3:2	CS_SELECT	When MASTER operation is used, controls the assertion of SPI_CS_ N pins. Selects SPI_CS_N if 00, SPI_CS1_N if 01, SPI_CS2_N if 10, or SPI_CS3_N if 11. The deselected ChipSelects will be driven to inactive state dictated by the field CS_N_POLARITY. This field is a "don't care" in SLAVE operation.
1	TRISTATE_CS	When set, drives Z on all SPI_CS _N lines. When clear, enables normal functionality on these lines. This bit can be used to support deployment of the core as one of the masters in a multi-master configuration.
0	NO_TRI_STATE	When set, spi_data_out is not taken tri-state when SPI_CS _N is de-asserted. This bit is normally set for MASTER operation but may be optionally left cleared.

0x16680308 GSBI7_SPI_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

GSBI7_SPI_ERROR_FLAGS

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.

GSBI7_SPI_ERROR_FLAGS (cont.)

Bits	Name	Description
1	SPI_SLV_CLK_OVER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was greater than the programmed value of N. When this happens, only the first N bits are passed to the SPI input FIFO and the output shift value is held at zero.
0	SPI_SLV_CLK_UNDER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was less than the programmed value of N. When this occurs, the bits which were received are passed to the SPI input FIFO and the CURRENT output bit is forced to zero.

0x1668030C GSBI7_SPI_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0003

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of spi_error_irq and the setting of the corresponding error flag in the SPI_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

GSBI7_SPI_ERROR_FLAGS_EN

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.
1	SPI_SLV_CLK_OVER_RUN_ERR_EN	If set, enables clock over run error generation.
0	SPI_SLV_CLK_UNDER_RUN_ERR_EN	If set, enables clock under run error generation.

0x16680310 GSBI7_SPI_DEASSERT_WAIT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the de-assertion wait time of SPI_CS _N between consecutive N-bit transfers in MASTER operation. The wait time is specified in number of cycles of cc_spi_master_clk.

GSBI7_SPI_DEASSERT_WAIT

Bits	Name	Description
31:6	RESERVED	Reserved.

GSBI7_SPI_DEASSERT_WAIT (cont.)

Bits	Name	Description
5:0	DEASSERT_WAIT	Number cc_spi_master_clk ticks associated with the de-asserted time of SPI_CS _N. Only applies to MASTER operation. For SLAVE operation, this field is a "don't care". A value of zero indicates SPI_CS _N remains de-asserted for exactly one clock tick. A value of one, indicates two ticks, etc. All ones indicates 64 ticks.

9.16.4 I2C master mini-core registers

0x16680400 GSBI7_I2C_MASTER_CLK_CTL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_CLK_CTL register is a read/write register that controls clock divider values. This register should only be written to after it is confirmed that the I2C master mini-core is not longer in RESET state (QUP_STATE register).

GSBI7_I2C_MASTER_CLK_CTL

Bits	Name	Description
31:11	RESERVED	Reserved.
10:8	HS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in high-speed (HS) mode. The minimum value should be 3 hex (4 I2C_clk clocks per period) to ensure proper sampling of the bus. For a maximum high speed bit rate of 3.4 Mb/s (high speed mode), this would require a minimum 40.8 MHz I2C_clk clock. The maximum I2C_clk is 81.6 MHz. This register is reset to a maximum value of 7 hex. I2C_HS_CLK = I2C_CLK/(3*(HS_DIVIDER_VALUE+1)
7:0	FS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in fast/standard (FS) mode. The minimum value should be 3 hex to ensure proper sampling of the bus. For a maximum bit rate of 400 kb/s (fast mode), this would require a 4.8 MHz I2C_clk clock. For a maximum bit rate of 100 kb/s (standard mode), this would require a 1.2 MHz I2C_clk clock. Maximum I2C_clk for fast and standard modes are 206.4 MHz and 51.6 MHz respectively. This register is reset to a maximum value of 255 hex. I2C_FS_CLK = I2C_CLK/(2*(FS_DIVIDER_VALUE+3)

0x16680404 GSBI7_I2C_MASTER_STATUS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_STATUS is a status register. Writing a one clears the status bits.

GSBI7_I2C_MASTER_STATUS

Bits	Name	Description
31:26	RESERVED_1	Reserved.
25	INVALID_READ_SEQ	This bit is set (1) when a MI_REC tag does not follow a START tag for an I2C READ. Not applicable for Halcyon.
24	INVALID_READ_ADDR	This bit is set (1) when the I2C controller is trying to receive data from a non-existent I2C slave (address).
23	INVALID_TAG	This bit is set (1) when the I2C controller is trying to process data from the output FIFO that is improperly tagged.
22:20	INPUT_FSM_STATE	This 3-bit field informs the microprocessor of the state of the I2C MASTER INPUT FSM block. Reset, read_last_byte, mi_rec, dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: READ_LAST_BYTE_STATE Value 0x3: MI_REC_STATE Value 0x4: DEC_STATE Value 0x5: STORE_STATE
19:16	OUTPUT_FSM_STATE	This 4-bit field informs the microprocessor of the state of the I2C MASTER OUTPUT FSM block. Reset, decode, send, mi_red, nop, nop_dec, invalid, invalid_dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: DECODE_STATE Value 0x3: SEND_STATE Value 0x4: MI_REC_STATE Value 0x5: NOP_STATE Value 0x6: INVALID_STATE Value 0x7: PEEK_STATE Value 0x8: SEND_R_STATE

GSBI7_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
15:13	CLK_STATE	This 3-bit field informs the microprocessor of the state of the I2C clk_control block. Reset_busidle, not_master, high, low, high_wait, forced_low, hs_addr_low or double_buffer_wait. Value 0x0: RESET_BUSIDLE_STATE Value 0x1: NOT_MASTER_STATE Value 0x2: HIGH_STATE Value 0x3: LOW_STATE Value 0x4: HIGH_WAIT_STATE Value 0x5: FORCED_LOW_STATE Value 0x6: HS_ADDR_LOW_STATE Value 0x7: DOUBLE_BUFFER_WAIT_STATE
12:10	DATA_STATE	This 3-bit field informs the microprocessor of the state of the I2C data_control block. Reset, Tx addr, Tx HS addr, Tx 10-bit addr, Tx 2nd 10-bit addr byte, Tx data and Rx data. Value 0x0: RESET_WAIT_STATE Value 0x1: TX_ADDR_STATE Value 0x2: TX_DATA_STATE Value 0x3: TX_HS_ADDR_STATE Value 0x4: TX_10_BIT_ADDR_STATE Value 0x5: TX_2ND_BYTE_STATE Value 0x6: RX_DATA_STATE
9	BUS_MASTER	This bit is set (1) when the I2C controller is the present bus master.
8	BUS_ACTIVE	This bit is set (1) when the bus is in use by this, or any other controller.
7:6	FAILED	This 2-bit field contains the failure information of the present I2C transfers. If transmitting, failed[1] contains the information regarding the byte that has been transmitted. Failed[0] contains the information of the byte awaiting transmission if there is a byte pipelined. If no byte is pipelined, ignore this bit. If receiving, failed[1] contains the information of the byte received and stored in the buffer, and failed[0] should be ignored. For example: Value 00: Byte n transmitted successfully, byte n+1 to begin transmission Value 01: Byte n transmitted successfully, byte n+1 errored: type of error indicated in other STATUS bits. (queued invalid write, for example) Value 10: Byte n errored: type of error indicated in other STATUS bits, byte n+1 to begin transmission (byte n+1 would have to be a valid address byte for this condition to occur) Value 11: Byte n errored: type of error indicated in other STATUS bits, byte n+1 discarded as well (if the byte was a data byte destined for a NACKed address, data is useless, therefore discarded)
5	INVALID_WRITE	This bit is set (1) when software writes data to the I2C_DATA register that should be flagged as an address but is not.

GSBI7_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
4	ARB_LOST	This bit is set (1) when the controller loses arbitration for the bus. If this bit gets set (1) during the transmission, all data has been lost, and the microprocessor must re-request its transmission.
3	PACKET_NACKED	This bit is set high when a NACK is received from a slave. If a high speed master code is sent and there is an ACK from a slave, then this bit is set (1) to indicate that the high speed mode can not be entered. If the high speed mode is accepted by the slave, then a NACK is performed and this bit is not set (1).
2	BUS_ERROR	This bit is set (1) when an unexpected START or STOP condition is detected. This returns the controller to its reset state.
1:0	RESERVED_2	Reserved.

10 GSS Registers

10.1 Overview

Table 10-1 GSS Bases

Base Name	Parent	Address
NAV_BASE2	NAV_BASE	0x10100000
GSS_A5_CSR_AHB_CLK_SEL	GSS_A5_CSR_BASE	0x10000000
GSS_A5_SAW2_SECURE	GSS_A5_SPM_BASE	0x10001000
GSS_A5_GICD_CTLR	GSS_A5_QGIC2_BASE	0x10008000
GSS_A5_GICH_HCR	GSS_A5_QGIC2_BASE	0x10008000
GSS_A5_GICC_CTLR	GSS_A5_QGIC2_BASE	0x10008000
GSS_A5_GICV_CTLR	GSS_A5_QGIC2_BASE	0x10008000
GSS_A5_APCS_TMRSECURE	GSS_A5_TIMERS_BASE	0x10002000
SSBI_ENABLE	GSS_A5_SSBI_BASE	0x10003000

10.2 GSS Command Registers

This section defines the Global Navigation Subsystem (GSS) command registers and memories that are accessible from the system bus, the typical bus used by the host processor.

10.2.1 Receiver Control Command Registers

NOTE All command register settings take effect immediately unless otherwise noted.

0x10100000 RC_CONTROL

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

RC_CONTROL

Bits	Name	Description
31:5	RESERVED_BITS	
4	RC_DM_WAIT_ABORT	This bit is used to abort the wait for RTC command that was initiated by the Data Mover. See DM1_RTC_WAIT. Write a logic '1' to this bit to generate the abort, and then write logic '0' to enable the wait function for the next initiation. 0x0: NO 0x1: YES
3	RC_CP_RESET	Reset for Correlation Processor. This command is similar to the RC_SW_RESET, but it only effects the CP module. It allows resetting only the CP while the other modules of the Nav Core are active. 0x0: NO 0x1: YES
2	RC_CCP_RESETN	Reset for CCP. Suggestion is to hold CCP in reset while the microcode program memory is being loaded, and then release reset. Note CCP will be in reset state after main hardware or software reset is applied. 0x0: YES 0x1: NO
1	RC_INIT	Initializes internal registers for millisecond frame count and BP time transfer status registers. The value must be held set until next frame start. The initialization will occur at beginning of next frame. 0x0: NO 0x1: YES
0	RC_SW_RESET	Software controlled reset. When this bit is set, all registers within nav core will be reset (except command registers). All clocks (except wr_clk) will be forced on during the reset phase. When the reset command bit is later cleared, then the command registers will be reset. It is suggested to write a logic 1, then immediately logic 0 to this register. This control has the same effect as the hardware reset in the Modem Clock Block.

0x10100004 RC_CONFIG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

RC_CONFIG

Bits	Name	Description
31:23	RESERVED_BITS	
22	RC_GACC_CLKEN	Clock enable for GACC
21	RC_ARS_CLKEN	Clock enable for ARS command logic
20	RC_SL_IRQ_EN	Enable interrupt from AD Sample Log (includes Spectrum Analyzer).
19:16	RC_DM_IRQ_EN	Enables Data Mover interrupts from each of the 4 security domains. The 4 bits correspond to SD3, SD2, SD1, SD0, with SD0 being the lowest bit. For each bit, 1 = enable interrupt. 0 = disable interrupt.
15:13	RC_DM_CLKEN_SEL	These bits control the Data Mover clock as follows: 0x0: OFF 0x1: DIV1 (main clock rate) 0x2: DIV2 (main clock div 2) 0x3: DIV4 (main clock div 4) 0x4: DIV8 (main clock div 8) 0x5: DIV16 (main clock div 16) 0x6: DIV32 (main clock div 32) 0x7: DIV64 (main clock div 64)
12:11	RC_XFER_SRC	Specifies the time transfer options for the GNSS RTC. The time transfer strobe can occur every 1 ms based on GNSS frame start (rc_frame_start), or by host processor writing to command bit RC_TT, or by external signal (CDMA). The sample phase and counter states for all 4 BPs are saved after time transfer occurs. See RC_BP _COUNT/PHASE. To enable the STB option, also set RC_FRAME_TT_ENABLE. 0x0: OFF 0x1: FRAME (every 1 ms frame based on GNSS RTC) 0x2: STB (re-sync'ed 1ms frame start, strobe from host processor, or CDMA) 0x3: OFF2
10:9	RC_SYNC_MASTER	Defines the BP sub-ms time base that is used as the master time base. Suggestion is to use the BP with lowest sample as the master. 0x0: BP 1 0x1: BP 2 0x2: BP 3 0x3: BP 4
8	RC_MEM_CLKEN	Clock enable for all memories and sample memory interface logic.

RC_CONFIG (cont.)

Bits	Name	Description
7	RC_CCP_CLKEN	Clock enable for Channel Control Processor
6	RC_CP_CLKEN	Clock enable for Correlation Processor
5	RC_BP4_CLKEN	Clock enable for Baseband Processor 4
4	RC_BP3_CLKEN	Clock enable for Baseband Processor 3
3	RC_BP2_CLKEN	Clock enable for Baseband Processor 2
2	RC_BP1_CLKEN	Clock enable for Baseband Processor 1 and ADC Processor
1	RC_TSG_CLKEN	Clock enable for Test Signal Generator
0	RC_RC_CLKEN	Clock enable for Receiver Control. All clock enables are force to 1 during hardware or software reset.

0x10100008 RC_LPM_RTC_CONTROL

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

RC_LPM_RTC_CONTROL

Bits	Name	Description
31:6	RESERVED_BITS_1	
5	RC_CDMA_TT_ENABLE	When RC_CDMA_TT_ENABLE = 1, the current LPM_RTC count will be captured into RC_CDMA_LPM_TT_CNT register when a CDMA time transfer request in received.
4	RC_FRAME_TT_ENABLE	When RC_FRAME_TT_ENABLE = 1, the current LPM_RTC count will be captured into RC_NAV_LPM_TT_CNT register at every 1ms frame start.
3	RESERVED_BITS_2	
2	RC_PPSO_POLARITY	When RC_PPSO_POLARITY = 0, PPS_OUT will be positive pulse, else it will be a negative pulse
1	RC_PPSO_ENABLE	When RC_PPSO_ENABLE = 1, PPS_OUT will be asserted when LPM_RTC count equals to RC_PPSO_ASSERT_RTC, and will be de-asserted when LPM_RTC count equals to RC_PPSO_DEASSERT_RTC
0	RC_PPSI_ENABLE	When RC_PPSI_ENABLE = 1, the LPM_RTC count value will be captured at the synchronized rising edge of the PPS_IN signal.

0x1010000C RC_PPSO_ASSERT

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

RC_PPSO_ASSERT

Bits	Name	Description
31:0	RC_PPSO_ASSERT	When LPM RTC reaches this command value then PPS out will be asserted. RC_PPSO_ENABLE must be set.

0x10100010 RC_PPSO_DEASSERT

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

RC_PPSO_DEASSERT

Bits	Name	Description
31:0	RC_PPSO_DEASSERT	When LPM RTC reaches this command value then PPS out will be de-asserted. RC_PPSO_ENABLE must be set.

0x10100014 RC_GPS_ON

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

RC_GPS_ON

Bits	Name	Description
31:0	RC_GPS_ON	For every write to this register, one interrupt will be generated when the LPM_RTC count value equals RC_LPM_RTC_ON. The comparison begins after the command is written and stops after the interrupt is generated.

0x10100018 RC_TIME_TRANSFER

Type: Read/Write
Clock: WR_CLK
Reset State: 0x0

RC_TIME_TRANSFER

Bits	Name	Description
31:1	RESERVED_BITS	
0	RC_TT	A write to this register will initiate a time transfer. The current LPM RTC count will be captured into RC_NAV_LPM_TT_CNT and strobe signals are generated to capture GNSS_RTC and CDMA_RTC. Reading this register will return all 0. The suggested process is to write this bit and then wait until RC_TT_ACTIVE status is zero. Then it is okay to read the time transfer status registers.

0x1010001C RC_GNSS_RTC_STATUS

Type: Read
Clock: RC_CLK
Reset State: 0x0

RC_GNSS_RTC_STATUS

Bits	Name	Description
31:17	RC_FRAME_COUNT	Current value of GNSS ms frame counter. The RC_SYNC_MASTER command specifies which BP to use for chip count, sample count and frame start. The frame start is used to increment this frame count. The frame counter is modulo 215.
16:7	RC_CHIP_COUNT	Current value of GNSS chip counter. For BP 1, BP 2 and BP 4, the chip counter range is 0 to 1022. For BP 3 (Glonass) the chip counter range is 0 to 510. For BP 3 this status register also includes the upper bit of the sample counter (bp3_chip_count[8:0], bp3_sample_count[7]).
6:0	RC_SAMPLE_COUNT	Current value of GNSS sample counter. For BP 1, BP 2 and BP 4, the sample counter ranges are 0 to 79, 0 to 39, and 0 to 19 for full, half and quarter rates, respectively. See BP _RATE command. For BP 3 (Glonass) this status register contains only the lower 7 bits of the sample counter (bp3_sample_count[6:0]). The sample counter ranges are 0 to 159 and 0 to 79 for full and half rates. See BP3_RATE command.

0x10100020 RC_BP1_COUNT_STATUS

Type: Read
Clock: BP1_CLK
Reset State: 0x0

RC_BP1_COUNT_STATUS

Bits	Name	Description
31:20	RESERVED_BITS	
19:0	RC_BP1_COUNT	BP 1 counter states after time transfer occurred. {bp1_frame_count[1:0], bp1_chip_count[9:0], bp1_sample_count[6:0], bp1_sample_skip}

0x10100024 RC_BP1_PHASE_STATUS

Type: Read
Clock: BP1_CLK
Reset State: 0x0

RC_BP1_PHASE_STATUS

Bits	Name	Description
31:0	RC_BP1_PHASE	BP 1 sample phase state after time transfer occurred.

0x10100028 RC_BP2_COUNT_STATUS

Type: Read
Clock: BP2_CLK
Reset State: 0x0

RC_BP2_COUNT_STATUS

Bits	Name	Description
31:20	RESERVED_BITS	
19:0	RC_BP2_COUNT	BP 2 counter states after time transfer occurred. {bp2_frame_count[1:0], bp2_chip_count[9:0], bp2_sample_count[6:0], bp2_sample_skip}

0x1010002C RC_BP2_PHASE_STATUS

Type: Read
Clock: BP2_CLK
Reset State: 0x0

RC_BP2_PHASE_STATUS

Bits	Name	Description
31:0	RC_BP2_PHASE	BP 2 sample phase state after time transfer occurred.

0x10100030 RC_BP3_COUNT_STATUS

Type: Read
Clock: BP3_CLK
Reset State: 0x0

RC_BP3_COUNT_STATUS

Bits	Name	Description
31:20	RESERVED_BITS	
19:0	RC_BP3_COUNT	BP 3 counter states after time transfer occurred. {bp3_frame_count[1:0], bp3_chip_count[8:0], bp3_sample_count[7:0], bp3_sample_skip}

0x10100034 RC_BP3_PHASE_STATUS

Type: Read
Clock: BP3_CLK
Reset State: 0x0

RC_BP3_PHASE_STATUS

Bits	Name	Description
31:0	RC_BP3_PHASE	BP 3 sample phase state after time transfer occurred.

0x10100038 RC_BP4_COUNT_STATUS

Type: Read
Clock: BP4_CLK
Reset State: 0x0

RC_BP4_COUNT_STATUS

Bits	Name	Description
31:20	RESERVED_BITS	
19:0	RC_BP4_COUNT	BP 4 counter states after time transfer occurred. {bp4_frame_count[1:0], bp4_chip_count[9:0], bp4_sample_count[6:0], bp4_sample_skip}

0x1010003C RC_BP4_PHASE_STATUS

Type: Read
Clock: BP4_CLK
Reset State: 0x0

RC_BP4_PHASE_STATUS

Bits	Name	Description
31:0	RC_BP4_PHASE	BP 4 sample phase state after time transfer occurred.

0x10100040 RC_TT_STATUS

Type: Read
Clock: RC_CLK
Reset State: 0x0

RC_TT_STATUS

Bits	Name	Description
31:1	RESERVED_BITS	
0	RC_TT_ACTIVE	This register indicates the status of the GPS software initiated time transfer command. When the register RC_TT is written, this status register will get set and it will be cleared once the LPM RTC is captured into RC_NAV_TT_RTC

0x10100044 RC_IRQ_STATUS

Type: Read
Clock: RC_CLK
Reset State: 0x04000000

RC_IRQ_STATUS

Bits	Name	Description
31:24	NAV_VERSION	Hardware version number. Set to 0x04 for version 4 of Nav.

RC_IRQ_STATUS (cont.)

Bits	Name	Description
23:4	RESERVED_BITS	
3:0	RC_IRQ	This register keep track of the interrupts asserted. There are 4 sources of interrupts: GPS IDLE to GPS_ON state transition, PPS out assertion, PPS in detection and Sample Log capture done. Anytime an interrupt is asserted it is captured in the status resighter. This register is cleared on read. Bit 3 is for Sample Log done, bit 2 is GPS_IDLE to GPS_ON state transition, bit 1 is PPS out assertion and bit 0 is PPS in detection.

0x10100048 RC_PPSI_RTC

Type: Read
Clock: RC_CLK
Reset State: 0x0

RC_PPSI_RTC

Bits	Name	Description
31:0	RC_PPSI_RTC	This register holds the captured value of the LPM RTC count when the last PPS in event occurred.

0x1010004C RC_NAV_TT_RTC

Type: Read
Clock: RC_CLK
Reset State: 0x0

RC_NAV_TT_RTC

Bits	Name	Description
31:0	RC_NAV_TT_RTC	This register holds the captured value of the LPM RTC count for the last GPS software initiated time transfer or the last frame start initiated time transfer.

0x10100050 RC_CDMA_TT_RTC

Type: Read
Clock: RC_CLK
Reset State: 0x0

RC_CDMA_TT_RTC

Bits	Name	Description
31:0	RC_CDMA_TT_RTC	This register holds the captured value of the LPM RTC count for the last Modem initiated time transfer. The source of this signal can CDMA, WCDMA, GSM or other RTCs.

0x10100054 RC_GNSS_TT_CNT

Type: Read
Clock: RC_CLK
Reset State: 0x0

RC_GNSS_TT_CNT

Bits	Name	Description
31:0	RC_GNSS_TT_RTC	This register holds the captured value of the GNSS RTC count for the last GPS software initiated time transfer or the last frame start initiated time transfer.

0x10100058 RC_NAV_TEST_BUS

Type: Read
Clock: RC_CLK
Reset State: 0x0

RC_NAV_TEST_BUS

Bits	Name	Description
31:0	RC_NAV_TEST_BUS	The Nav Core test bus output is accessible from this register location. Note the data rate may be much higher than the host processor access rate. This mainly serve as a debug feature (e.g., determining if signal pathis are active and capturing samples at unknown or irregular rates for creating histograms).

10.2.2 ADC Processor Command Registers

NOTE All command register settings take effect at the next frame start from the master BP or AD_UPDATE command unless otherwise noted.

0x10100080 AD_MODE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

AD_MODE

Bits	Name	Description
31:18	RESERVED_BITS	
17:16	AD_TESTINSEL	When AD_TESTINSEL[0] = 1, the ADC signals are connected to test bus input instead of normal inputs. {2'b00, adc2_in_i[5:0], 2'b00, adc2_in_q[5:0], 2'b00, adc1_in_i[5:0], 2'b00, adc1_in_q[5:0]} = test_bus_in[31:0]. When AD_TESTINSEL[1] = 1, the blank signals are connected to test bus input instead of normal inputs. blank_signal[3] = test_bus_in[31] blank_signal[2] = test_bus_in[23] blank_signal[1] = test_bus_in[15] blank_signal[0] = test_bus_in[7]
15	AD_TESTSEL	When = 1, these module outputs are connected to ad test bus out: {rc_frame_start, ad1_rate_en, ad2_rate_en, 1'b0, ad2_out_i[6:0], ad2_out_q[6:0], ad1_out_i[6:0], ad1_out_q[6:0]}
14:13	AD_SAMPLELOG_MODE	Sample log mode. Option of continuous circular buffer or single vector capture. The buffer and vector lengthis are specified by AD_SAMPLELOG_DEPTH. Note register takes effect at next frame start. 0x0: OFF 0x1: VECTOR 0x2: CIRCULAR 0x3: FRAME (single vector starting at next frame start.)
12	AD_SAMPLELOG_START	Sample log start control for single vector capture modes (VECTOR or FRAME). Writing a 0 to 1 pattern to this bit will start the vector capture immediately or at next frame start (assuming AD_SAMPLELOG_MODE previously set to VECTOR or FRAME). The capture will continue until the specified vector length is reached (see AD_SAMPLELOG_DEPTH). The status bit AD_SAMPLELOG_DONE and interrupt bit RC_INTR_STATUS[3] indicate when the capture is completed. The interrupt must be enabled with RC_SA_IRQ_EN.

AD_MODE (cont.)

Bits	Name	Description
11:8	AD_SAMPLELOG_SRC	Sample log signal source. For 1010 to 1110 setting the input is fixed to zero. * Not supported if RX1 is async to RX2. ** Due to high bandwidth these modes may not be supported concurrently with BP3 and/or BP4. This limitation also applies if Spectrum Analyzer is set to BYPASS mode. 0x0: RX1IQ1 (1-bit complex samples from receiver 1) 0x1: RX1IQ2 (2-bit complex samples from receiver 1) 0x2: RX1IQ3 (3-bit complex samples from receiver 1) 0x3: RX2IQ1 (1-bit complex samples from receiver 2) 0x4: RX2IQ2 (2-bit complex samples from receiver 2) 0x5: RX2IQ3 (3-bit complex samples from receiver 2) 0x6: RX12IQ1 (1-bit complex samples from rec 1 & 2*) 0x7: RX12IQ2 (2-bit complex samples from receiver 1 & 2*) 0x8: RX1IQ6 (6-bit complex samples from receiver 1 **) 0x9: RX2IQ6 (6-bit complex samples from receiver 2 **) 0xF: SAIQ8 (8-bit complex samples from Spec Analyzer**)
7:5	AD_SAMPLELOG_DEPTH	Number of words (32-bits) to store into sample memory. Each word contains more than one sample. When the range is exceeded in circular buffer mode, then the index starts over (modulo index). 0x0: N512 0x1: N1K 0x2: N2K 0x3: N4K 0x4: N8K 0x5: N16K 0x6: N32K 0x7: NMAX (all of sample memory)
4:3	AD_MEAS_PERIOD	Specifies the measurement period for the preliminary mean and amplitude estimators. 0x0: OFF 0x1: PROG1 (prog by AD_MEAS_ENABLE & RX1 blank) 0x2: PROG2 (prog by AD_MEAS_ENABLE & RX2 blank) 0x3: FRAME (fixed at 1 ms frame period)

AD_MODE (cont.)

Bits	Name	Description
2	AD_MEAS_ENABLE	This command bit controls the immediate start and stop of the measurement interval for the preliminary mean and amplitude estimators. This is only for AD_MEAS_PERIOD = PROG modes. Normally this bit should be at logic 0, the disabled state. When it is set to logic 1, the measurement interval is started, and then when it is cleared the measurement interval is stopped. During the measurement interval the amplitude & mean integrators are active and an interval sample counter (AD_MEAS_LENGTH) is incremented. When blanking occurs then nothing is added to the integrator and the interval sample counter is not incremented. After the measurement interval is completed, the mean/amplitude estimators are saved into the status registers (AD_RX _MEANMONI/Q, AD_RX _AMPLMONI/Q, BP _PREAMPLMONI/Q). The mean and amplitude estimation values can be normalized with the interval length.
1	AD_UPDATE	Normally, command register settings take effect at the frame start. This command bit allows all command registers to take effect immediately. When a logic 0 to 1 transition is written to this bit, then the command registers take effect.
0	AD_INIT	Initializes the internal registers at start of next ms frame. Command registers are not effected. Command registers can only be initialized by the hardware reset signal from the Modem clock block. AD_INIT can still be done when AD1 and AD2 are disabled. 0x0: NO 0x1: YES

0x10100084 AD_RX1_CONFIG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

AD_RX1_CONFIG

Bits	Name	Description
31:19	RESERVED_BITS	
18:17	AD_RX1_QUANTSEL	Quantizer type select. Also see AD_RX1_QUANTMAP 0x0: OFF (power saving) 0x1: SDM (1,2 or 3-bit sigma delta) 0x2: LINEAR (6-bit ADC) 0x3: LIMITER (1-bit hard limiter of 6-bit ADC)

AD_RX1_CONFIG (cont.)

Bits	Name	Description
16	AD_RX1_BLANKSIG	Software blank signal command. This command bit is ORed with the hardware blank signal inputs to the core, and thus allows software to blank the receiver at any time. This is also useful for testing the blanking feature. Note this bit takes effect immediately. It is not depended on state of AD_RX1_BLANKPOL or AD_RX1_BLANKEN . Receiver 1 and 2 have independent software blank controls.
15	AD_RX1_BLANKPOL3	Polarity for blanking signal 3. See AD_RX1_BLANKPOL0
14	AD_RX1_BLANKEN3	Enable for blanking signal 3. See AD_RX1_BLANKEN0
13	AD_RX1_BLANKPOL2	Polarity for blanking signal 2. See AD_RX1_BLANKPOL0
12	AD_RX1_BLANKEN2	Enable for blanking signal 2. See AD_RX1_BLANKEN0
11	AD_RX1_BLANKPOL1	Polarity for blanking signal 1. See AD_RX1_BLANKPOL0
10	AD_RX1_BLANKEN1	Enable for blanking signal 1. See AD_RX1_BLANKEN0
9	AD_RX1_BLANKPOL0	Signal polarity for blanking signal 0. 0x0: POS (Active high) 0x1: NEG (Active low)
8	AD_RX1_BLANKEN0	Enable for blanking signal 0. If blanking enable command is set to ON and blank signal is active (AD_RX1_BLANKSIG OR blank_signal[0] input), then the inverse quantizer outputs are forced to zero (no contribution to mean estimation), and the blank counter is incremented for every sample that is blanked. 0x0: OFF 0x1: ON
7	AD_RX1_NULLQ	Null the Q component input. Only for test. 0x0: NO 0x1: YES
6	AD_RX1_NULLI	Null the I component input. Only for test. 0x0: NO 0x1: YES
5	AD_RX1_SIGNINVQ	Invert polarity of Q component input. Normally not used and should be left at default setting of zero. Only recommended when polarity of Q component is accidently inverted somewhere in the receiver signal path. 0x0: NO 0x1: YES
4	AD_RX1_SIGNINVI	Invert polarity of I component input. Normally not used and should be left at default setting of zero. Only recommended when polarity of I component is accidently inverted somewhere in the receiver signal path. 0x0: NO 0x1: YES

AD_RX1_CONFIG (cont.)

Bits	Name	Description
3	AD_RX1_SWAPIQ	Swap I and Q component inputs. Normally not used and should be left at default setting of zero. Only recommended when I and Q components or local oscillator phases are accidently switched somewhere in the receiver signal path. 0x0: NO 0x1: YES
2	AD_RX1_SRCSEL	Input source selection 0x0: TSG (Test Signal Generator) 0x1: ADC (receiver)
1:0	AD_RX1_RATE	ADC 1 sample rate 0x0: OFF (disable AD 1) 0x1: FULL (main clock rate) 0x2: HALF (half of main clock rate) 0x3: QTR (quarter of main clock rate)

0x10100088 AD_RX2_CONFIG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

AD_RX2_CONFIG

Bits	Name	Description
31:19	RESERVED_BITS	
18:17	AD_RX2_QUANTSEL	See AD_RX1_QUANTSEL
16	AD_RX2_BLANKSIG	See AD_RX1_BLANKSIG
15	AD_RX2_BLANKPOL3	See AD_RX1_BLANKPOL3
14	AD_RX2_BLANKEN3	See AD_RX1_BLANKEN3
13	AD_RX2_BLANKPOL2	See AD_RX1_BLANKPOL2
12	AD_RX2_BLANKEN2	See AD_RX1_BLANKEN2
11	AD_RX2_BLANKPOL1	See AD_RX1_BLANKPOL1
10	AD_RX2_BLANKEN1	See AD_RX1_BLANKEN1
9	AD_RX2_BLANKPOL0	See AD_RX1_BLANKPOL0
8	AD_RX2_BLANKEN0	See AD_RX1_BLANKEN0
7	AD_RX2_NULLQ	See AD_RX1_NULLQ
6	AD_RX2_NULLI	See AD_RX1_NULLI
5	AD_RX2_SIGNINVQ	See AD_RX1_SIGNINVQ

AD_RX2_CONFIG (cont.)

Bits	Name	Description
4	AD_RX2_SIGNINVI	See AD_RX1_SIGNINVI
3	AD_RX2_SWAPIQ	See AD_RX1_SWAPIQ
2	AD_RX2_SRCSEL	See AD_RX1_SRCSEL
1:0	AD_RX2_RATE	See AD_RX1_RATE

0x1010008C AD_RX1_QUANTMAP

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

AD_RX1_QUANTMAP

Bits	Name	Description
31:0	AD_RX1_QUANTMAP	ADC 1 quantization map. Only used for SDM and LIMITER type quantizers (see AD_RX1_QUANTSEL). Converts the eight possible 3-bit binary values into 4-bit signed values. The inverse quantizer output is set to a 4-bit sub-vector of the 32-bit command word, based on the input value (the ADC output). For input values of 0, 1, ...7, the output is set to sub-vector [3:0], [7:4], ... [31:28]. Suggested settings are 0xFDB97531 for GNSS SDM 8-levels 0x000026EA for Astra SDM 4-levels 0x0000004C for Astra SDM 2-levels or hard-limiter

0x10100090 AD_RX2_QUANTMAP

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

AD_RX2_QUANTMAP

Bits	Name	Description
31:0	AD_RX2_QUANTMAP	ADC 2 quantization map. See AD_RX1_QUANTMAP.

0x10100094 AD_MEAS_STATUS

Type: Read
Clock: BP1_CLK
Reset State: 0x0

AD_MEAS_STATUS

Bits	Name	Description
31:18	RESERVED_BITS	
17	AD_RX2_MEAS_BLANK	See AD_RX1_MEAS_BLANK
16	AD_RX1_MEAS_BLANK	This bit indicates if receiver 1 was blanked during the last measurement period. For AD_MEAS_PERIOD = PROG or FRAME mode, this flag is updated after the end of the measurement period.
15:0	AD_MEAS_LENGTH	Status value that indicates the number of valid (non-blanked RX) ADC samples included in the last measurement period of the preliminary mean and amplitude estimators. This is only for AD_MEAS_PERIOD = PROG modes. The measurement period is controlled by the AD_MEAS_ENABLE command and when there is no blanking active on selected RX . This is implemented with a 16-bit counter operating at 4.092 MHz rate, which provides up to a 16 ms range. If the count range is exceeded, the counter will wrap around.

0x10100098 AD_RX1_MEAN_MON

Type: Read
Clock: BP1_CLK
Reset State: 0x0

AD_RX1_MEAN_MON

Bits	Name	Description
31:16	AD_RX1_MEANMONQ	Mean estimator for Q component of receiver 1. See AD_RX1_MEANMONI
15:0	AD_RX1_MEANMONI	Mean estimator for I component of receiver 1. Measures the mean (DC offset) of the signal over a 1 ms or programmable interval. The result is read by software and use to determine DC correction values for the RF device. The measurement period is specified by the AD_MEAS_PERIOD and AD_MEAS_ENABLE commands. If the measurement period is programmable, then the mean estimation values can be normalized with the interval length (see AD_MEAS_LENGTH). If the measurement period is 1 ms, then the estimation value is normalized by 1/4096. If blanking occurs during the 1 ms fixed interval mode, then the preliminary mean estimators are not updated. See AD_RX1_MEAS_BLANK. The mean estimator is implemented with a 23-bit integrator. The 7-bit samples are added to the integrator over the measurement period. At the period end, the result is scaled by 7-bits to fit into a 16-bit status register. The integrator must not be allowed to overflow, which can occur after 16 ms with a full scale input.

0x1010009C AD_RX2_MEAN_MON

Type: Read
Clock: BP1_CLK
Reset State: 0x0

AD_RX2_MEAN_MON

Bits	Name	Description
31:16	AD_RX2_MEANMONQ	Mean estimator for Q component of receiver 2. See AD_RX1_MEANMONI
15:0	AD_RX2_MEANMONI	Mean estimator for I component of receiver 2. See AD_RX1_MEANMONI

0x101000A0 AD_RX1_BLANK_MONITOR

Type: Read
Clock: BP1_CLK
Reset State: 0x0

AD_RX1_BLANK_MONITOR

Bits	Name	Description
31:18	RESERVED_BITS	
17:0	AD_RX1_BLANKMON	Status value that indicates the number of ADC samples that were blanked. The blank signal state is checked at a rate of 4.092 MHz. An internal 18-bit counter is advanced for every blank case (thus a range of 64 ms of continuous blanking). The counter wraps around after 218-1. On every 1 ms frame start, the counter value is saved in this status register. Software can read this status and the GNSS RTC at any time, and then compare to the values to the previous read. This information can be used to determine the duration of time and the number of blanked samples in the last interval. When AD_RX1_BLANKEN are disabled, this register is unchanged. Register is cleared to zero after AD_INIT or RC_SW_RESET or hardware reset

0x101000A4 AD_RX2_BLANK_MONITOR

Type: Read
Clock: BP1_CLK
Reset State: 0x0

AD_RX2_BLANK_MONITOR

Bits	Name	Description
31:18	RESERVED_BITS	

AD_RX2_BLANK_MONITOR (cont.)

Bits	Name	Description
17:0	AD_RX2_BLANKMON	Blank monitor for receiver 2. See AD_RX1_BLANKMON

0x101000A8 AD_SL_INDEX

Type: Read
Clock: BP1_CLK
Reset State: 0x0

AD_SL_INDEX

Bits	Name	Description
31:17	RESERVED_BITS	
16	AD_SAMPLELOG_DONE	Indicates when sample log capture is completed. need to define.
15:0	AD_SL_INDEX	Status value that indicates the sample log row index at the last frame start. The range of the row index is specified by AD_SAMPLELOG_DEPTH. On every 1 ms frame start, the index value is saved in this status register.

0x101000AC AD_RX1_AMPL_MON

Type: Read
Clock: BP1_CLK
Reset State: 0x0

AD_RX1_AMPL_MON

Bits	Name	Description
31:16	AD_RX1_AMPLMONQ	Amplitude estimator for Q component of receiver 1. See AD_RX1_AMPLMONI
15:0	AD_RX1_AMPLMONI	Amplitude estimator for Q component of receiver 1. Same operation as AD_RX1_MEANMONI, but estimates the mean-magnitude of the signal. More details needed.

0x101000B0 AD_RX2_AMPL_MON

Type: Read
Clock: BP1_CLK
Reset State: 0x0

AD_RX2_AMPL_MON

Bits	Name	Description
31:16	AD_RX2_AMPLMONQ	Amplitude estimator for Q component of receiver 2. See AD_RX1_AMPLMONI
15:0	AD_RX2_AMPLMONI	Amplitude estimator for I component of receiver 2. See AD_RX1_AMPLMONI

0x101000B4 AD_SPEC_ANALYZER_CMD

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

AD_SPEC_ANALYZER_CMD

Bits	Name	Description
31:25	RESERVED_BITS	
24:21	AD_SA_GAINSTEP	Spectrum analyzer gain adjustment. Fixed 3 dB gain steps. 0x0: G0 (gain = 1, default) 0x1: G3 (gain = 3/4) 0x2: G6 (gain = 1/2) 0x3: G9 (gain = 3/8) 0x4: G12 (gain = 1/4) 0x5: G15 (gain = 3/16) 0x6: G18 (gain = 1/8) 0x7: G21 (gain = 3/32) 0x8: G24 (gain = 1/16) 0x9: G27 (gain = 3/64) 0xA: default value_1 0xB: default value_2 0xC: default value_3 0xD: default value_4 0xE: default value_5 0xF: default value_6
20:19	AD_SA_SRC_SEL	Spectrum analyzer BP signal source selection. See BP _SA_PROBE for probe selection within each BP. 0x0: BP1 0x1: BP2 0x2: BP3 0x3: BP4

AD_SPEC_ANALYZER_CMD (cont.)

Bits	Name	Description
18:16	AD_SA_MODE	Spectrum analyzer mode. 0x0: OFF (Disable SA to save power) 0x1: BYPASS (bypass SA and go directly from BP to SL) 0x2: DEC32 (decimate by 32) 0x3: DEC64 (decimate by 64) 0x4: DEC128 (decimate by 128) 0x5: DEC256 (decimate by 256) 0x6: OFF2 0x7: OFF3
15:0	AD_SA_FREQ	Spectrum analyzer frequency converter. Represented as signed fractional value (i.e., negative values are for down-conversion). AD_SA_FREQ = fc / fs * 216 where fc is the conversion frequency, and fs is the sample rate. The sample rates are 4.092 MHz for BP1 and BP2, 10.22 MHz for BP3 and 20.46 or 24.552 MHz for BP4.

0x101000B8 AD_SPEC_ANALYZER_STATUS

Type: Read
Clock: WR_CLK
Reset State: 0x0

AD_SPEC_ANALYZER_STATUS

Bits	Name	Description
31:14	RESERVED_BITS	
13:0	AD_SA_BLANKMON	Spectrum analyzer blanking counter. Indicates the number of logged samples that were captured while blanking was active.

10.2.3 Baseband Processor 1 Command Registers

NOTE All command register settings take effect at the next frame start from the master BP or BP1_UPDATE command unless otherwise noted.

0x10100200 BP1_CONFIG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_CONFIG

Bits	Name	Description
31:30	RESERVED_BITS	
29:28	BP1_SA_PROBE	BP1 probe points for the spectrum analyzer or bypass SA to go directly to sample log. All probes select the 8 MSBs from each I and Q component. Unbiased rounding is performed. 0x0: P1 (pre-notch filter input) 0x1: P2 (pre-notch filter output) 0x2: P3 (first notch filter input or test bus input) 0x3: P4 (last notch filter output)
27	BP1_TESTINSEL	When BP1_TESTINSEL[0] = 1, the notch filter is connected to test bus input instead of normal inputs. Can also be routed to the spectrum analyzer. {nf_i[8:0], nf_q[8:0]} = test_bus_in[17:0]
26:24	BP1_TESTSEL	Specifies the probe point to send to the BP1 test bus output 0x0: OFF (zero out) 0x1: P1 (linear interpolator input) 0x2: P2 (linear interpolator output) 0x3: P3 (decimate by 5 output) 0x4: P4 (baseband frequency converter output) 0x5: P5 (unused, zero out) 0x6: P6 (sub-ch 2 final quantizer input) 0x7: P7 (sub-ch 3 final quantizer input)
23	BP1_PREAMPLMON_EN	Enable for preliminary amplitude estimator (see BP1_PREAMPLMONI/Q) 0x0: OFF 0x1: ON
22:19	BP1_GAINSTEP	Fixed 3 dB gain steps. The setting is predetermined based on receiver configuration or testing with typical RF receivers. Ideally for optimum performance the output RMS level of the gain step should be within the range of 16 to 64 over the possible range of RF & ADC gain variation. The signal width after gain step is limited to only 9-bits, so setting an optimal level is important. See BP1_PREAMPLMONI for description of RMS estimation at the gain step input. 0x0: G0 (gain = 1, default) 0x1: G3 (gain = 3/4) 0x2: G6 (gain = 1/2) 0x3: G9 (gain = 3/8) 0x4: G12 (gain = 1/4) 0x5: G15 (gain = 3/16) 0x6: G18 (gain = 1/8) 0x7: G21 (gain = 3/32) 0x8: G24 (gain = 1/16) 0x9: G27 (gain = 3/64)

BP1_CONFIG (cont.)

Bits	Name	Description
18:16	BP1_DCNOTCHPOLE	DC notch filter pole magnitude. Controls the notch bandwidth. Range of 0 to 7. See BP1_NOTCHPOLE1 for frequency response for each pole magnitude.
15	BP1_GAINALIGN	Automatic-alignment mode for final quantizer threshold. When enabled, the gain control is done in hardware. When disabled, the software must control the threshold settings (see BP1_SCH _THRESHI/Q). 0x0: OFF 0x1: ON
14:13	BP1_MEANMONMODE	Control the type of mean estimation. The estimate result is accessible from status register BP1_MEANMONI/Q and is used when in automatic alignment mode BP1_DCALIGN. 0x0: OFF (power savings) 0x1: INT (integrate-hold estimator for 1 ms) 0x2: IIR (IIR LPF estimator) 0x3: OFF2 (power savings)
12	BP1_DCALIGN	Automatic-alignment mode for DC offset. When enabled, the DC offset control is done in hardware. When disabled, the software must control DC offset (see BP1_OFFSETI/Q). 0x0: OFF (manual alignment) 0x1: ON (automatic)
11	BP1_AAF_EN	Option to bypass the anti-alias filter (for low resampling frequency ratio) 0x0: OFF 0x1: ON
10	BP1_RS_EN	Enable resampler operation, or bypass linear interpolator and disable resampler phase accumulator. 0x0: OFF 0x1: ON
9	BP1_RS_LOAD	Option to load the resampler phase accumulator with BP1_RSPHASE at next ms interval. This will also reset the sample, chip and 4 ms frame counters. 0x0: NO 0x1: YES
8	BP1_IF_TYPE	Receiver IF Type 0x0: ZIF (bypass digital IF down converter) 0x1: LIF (use digital IF down converter)
7	BP1_AUXSEL	BP 1 auxiliary source selection 0x0: NO 0x1: YES

BP1_CONFIG (cont.)

Bits	Name	Description
6	BP1_ADCSEL	BP 1 input source selection This also selects the blank input source and the measurement control for the preliminary amplitude estimator. 0x0: AD1 (receiver 1) 0x1: AD2 (receiver 2)
5	BP1_SCH3_EN	Enable sub-channel 3 output. The BOC(1,1) at 4 spc. 0x0: OFF 0x1: ON
4	BP1_SCH2_EN	Enable sub-channel 2 output. The BPSK at 2 spc. Note, if both sub-channel enables are set to off, then all processing in BP1 will be disabled. However, it is still possible to keep the time base running with the BP1_RATE command. 0x0: OFF 0x1: ON
3:2	BP1_RATE	BP 1 sample rate. Note this command takes effect at next frame start or BP1_UPDATE. It should match the rate specified for the ADC processor that is the source for this BP. See AD _RATE. 0x0: OFF (disable BP 1 time base) 0x1: FULL (main clock rate) 0x2: HALF (half of main clock rate) 0x3: QTR (quarter of main clock rate)
1	BP1_UPDATE	Normally, command register settings take effect at the frame start. This command bit allows all command registers to take effect immediately. When a logic 0 to 1 transition is written to this bit, then the command registers take effect. Note that this may cause problems with some command that depend on exact frame interval, such as anything related to resampler, mean and amplitude estimators. If the update command is issued, then all amplitude and mean estimators are not updated at the next frame start because they are potentially invalid.
0	BP1_INIT	Initializes the internal registers at start of next ms frame. Command registers are not effected. Command registers can only be initialized by the hardware reset signal from the Modem clock block. BP1_INIT can still be done when BP1 is off. 0x0: NO 0x1: YES

0x10100204 BP1_IF_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_IF_FREQ

Bits	Name	Description
31:25	RESERVED_BITS	
24:22	BP1_INTDELAY	Group delay compensation, integer part. Number of unit sample delays added to the signal path. The range is 0 to 6 sample delays at 20.46 MHz sample rate, which is equivalent to range of 0 to 293 ns with steps of 48.9 ns.
21:16	BP1_FRACDELAY	Group delay compensation, fraction part. Fraction of unit sample delay added to the signal path. The command range of 0 to 63 is assigned to sample delays from 0 to 63/64 in steps of 1/64 sample period, which is equivalent to 0.76 ns steps.
15:0	BP1_IFFREQ	Digital IF down converter frequency. Represented as signed fractional value (i.e., negative values are for down-conversion). BP1_IFFREQ = fc / fs *216 where fc is the down converter frequency, and fs is the ADC sample rate, which could be higher than 81.84, 40.92 or 20.46 MHz when the resampler is used.

0x10100208 BP1_RS_RATE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_RS_RATE

Bits	Name	Description
31:0	BP1_RSRATE	Resampler rate command. An unsigned 32-bit fraction (U0.32) that is added to the sample phase accumulator on ever valid RS output sample. The command is based on the ratio of output sample rate to input sample rate. BP1_RSRATE = (fs / fo -1) * 232 where fs is the ADC sample rate, and fo is the resampler output rate of 81.84, 40.92 or 20.46 MHz based on BP1_RATE. The ratio of fs / fo must be greater than 1 but less than 1.5.

0x1010020C BP1_OFFSET

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_OFFSET

Bits	Name	Description
31:16	BP1_OFFSETQ	DC offset setting for Q component. Performs the same function as the I component.
15:0	BP1_OFFSETI	DC offset setting for I component. In manual-alignment mode (BP1_DCALIGN), this register is directly subtracted from the received signal. In automatic-alignment mode, this register is ignored and the mean estimate (BP1_MEANNONI) calculated in the previous millisecond frame is directly subtracted from the signal. The result is the output signal has a zero mean. When the DC error is over the recommended range, than coarse DC adjustments must be made in the RF down converter.

0x10100210 BP1_NOTCH1

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_NOTCH1

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP1_NOTCHMODE1	Notch filter on/off control. When in OFF state, the notch filter is bypassed but the sample delay is still the same. 0x0: OFF 0x1: ON
22:20	BP1_NOTCHPOLE1	Notch filter pole magnitude. Controls the notch bandwidth. Range of 0 to 7. List the 6 dB bandwidthis (in Hz) for the 8 settings, based on fs in MHz, then list fs in each BP
19:0	BP1_NOTCHFREQ1	Notch filter center frequency, represented as signed fractional value (S1.19). BP1_NOTCHFREQ1 = fc / 4.092 MHz * 220

0x10100214 BP1_NOTCH2

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_NOTCH2

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP1_NOTCHMODE2	See BP1_NOTCHMODE1
22:20	BP1_NOTCHPOLE2	See BP1_NOTCHPOLE1
19:0	BP1_NOTCHFREQ2	See BP1_NOTCHFREQ1

0x10100218 BP1_NOTCH3

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_NOTCH3

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP1_NOTCHMODE3	See BP1_NOTCHMODE1
22:20	BP1_NOTCHPOLE3	See BP1_NOTCHPOLE1
19:0	BP1_NOTCHFREQ3	See BP1_NOTCHFREQ1

0x1010021C BP1_NOTCH4

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_NOTCH4

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP1_NOTCHMODE4	See BP1_NOTCHMODE1
22:20	BP1_NOTCHPOLE4	See BP1_NOTCHPOLE1
19:0	BP1_NOTCHFREQ4	See BP1_NOTCHFREQ1

0x10100220 BP1_NOTCH5

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_NOTCH5

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP1_NOTCHMODE5	See BP1_NOTCHMODE1
22:20	BP1_NOTCHPOLE5	See BP1_NOTCHPOLE1
19:0	BP1_NOTCHFREQ5	See BP1_NOTCHFREQ1

0x10100224 BP1_NOTCH6

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_NOTCH6

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP1_NOTCHMODE6	See BP1_NOTCHMODE1
22:20	BP1_NOTCHPOLE6	See BP1_NOTCHPOLE1
19:0	BP1_NOTCHFREQ6	See BP1_NOTCHFREQ1

0x10100228 BP1_EQ_COEF_REAL

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_EQ_COEF_REAL

Bits	Name	Description
31:24	RESERVED_BITS	
23:16	BP1_EQCOEF3I	
15:8	BP1_EQCOEF2I	
7:0	BP1_EQCOEF1I	Complex FIR equalizer with programmable coefficients. Real coefficients = [c3i c2i c1i 512 c1i c2i c3i].

0x1010022C BP1_EQ_COEF_IMAG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_EQ_COEF_IMAG

Bits	Name	Description
31:24	RESERVED_BITS	
23:16	BP1_EQCOEF3Q	
15:8	BP1_EQCOEF2Q	
7:0	BP1_EQCOEF1Q	Complex FIR equalizer with programmable coefficients. Imaginary coefficients = [-c3q -c2q -c1q 0 c1q c2q c3q]

0x10100230 BP1_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_FREQ

Bits	Name	Description
31:0	BP1_FREQ	Fine frequency adjustment. Represented as signed fractional value. Used to compensate for residual frequency offset. BP1_FREQ = fc / 4.092 MHz * 232

0x10100234 BP1_THRESH

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_THRESH

Bits	Name	Description
31:24	BP1_SCH3_THRESHQ	See BP1_SCH2_THRESHI
23:16	BP1_SCH3_THRESHI	See BP1_SCH2_THRESHI
15:8	BP1_SCH2_THRESHQ	Final quantizer threshold for the Q component of sub-channel 2. Performs the same function as the I component.

BP1_THRESH (cont.)

Bits	Name	Description
7:0	BP1_SCH2_THRESHI	Final quantizer threshold for the I component of sub-ch 2. In manual-alignment mode (BP1_GAINALIGN=OFF), this register specifies the first threshold of the 16-level quantizer. The higher thresholds are linearly scaled from this value (that is, the quantizer is linear and symmetrical). For a 16-level quantizer, the optimum threshold equals 0.3352 times the signal RMS value. The RMS value is sqrt(p/2) times the mean-magnitude estimate (BP1_SCH2_AMPLMONI). Thus the threshold should be set to 0.427 times the mean-magnitude estimate. In automatic-alignment mode, this register is ignored, and the amplitude estimate measured in the previous millisecond frame is used to determine the optimum threshold setting. The optimum threshold is approximated by 7/16 * BP1_SCH2_AMPLMONI.

0x10100238 BP1_PRE_NOTCH

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_PRE_NOTCH

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP1_PRENOTCHMODE	See BP1_NOTCHMODE1
22:20	BP1_PRENOTCHPOLE	See BP1_NOTCHPOLE1
19:0	BP1_PRENOTCHFREQ	See BP1_NOTCHFREQ1

0x1010023C BP1_RS_PHASE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP1_RS_PHASE

Bits	Name	Description
31:0	BP1_RSPHASE	Resampler initial phase command. An unsigned 32-bit fraction (U0.32) that is applied to the sample phase accumulator at the beginning of a frame when BP1_RS_LOAD is set. Suggested value is 0x80000000.

0x10100240 BP1_PRE_AMPL_MON

Type: Read
Clock: BP1_CLK
Reset State: 0x0

BP1_PRE_AMPL_MON

Bits	Name	Description
31:16	BP1_PREAMPLMONQ	Preliminary amplitude estimator for the Q component. See BP1_PREAMPLMONI
15:0	BP1_PREAMPLMONI	Preliminary amplitude estimator for the I component. Measures the mean-magnitude of the signal over a 1 ms or programmable interval. The result is read by software and use to determine optimum gain settings for the RF device. The measurement period is specified by the AD_MEAS_PERIOD and AD_MEAS_ENABLE commands. If the measurement period is programmable, then the mean estimation values can be normalized with the interval length (see AD_MEAS_LENGTH). In 1 ms frame interval mode, if blanking occurs or the BP1_UPDATE command occurs during the measurement period, the estimate is consider invalid and this register is not updated. See AD_RX _MEAS_BLANK. The amplitude estimate is done on the 11-bit signal at the input to the gain step after mean is subtracted. It is performed by integrating the signal magnitude over the measurement period. The 26-bit accumulator result is normalized by 10-bits to fit into the 16-bit range of this status register. The estimate is done with 4092 samples/ms. Thus the actual mean-magnitude of the signal is 210 / 4092 = 0.25 times the estimate result per ms interval. The RMS value is sqrt(p/2) times the mean-magnitude value.

0x10100244 BP1_MEAN_MON

Type: Read
Clock: BP1_CLK
Reset State: 0x0

BP1_MEAN_MON

Bits	Name	Description
31:16	BP1_MEANMONQ	Signal mean estimate for the Q component. The estimate is performed by the same method as for the I component.

BP1_MEAN_MON (cont.)

Bits	Name	Description
15:0	BP1_MEANMONI	Signal mean estimate for the I component. The mean estimate is done on the 16-bit signal at the input to the offset subtractor (see BP1_OFFSETI). It is performed by either a IIR LPF or an integrator. The integration is done over a 1 ms period, which contains 4092 samples. The result is approximately normalized by dividing by 4096 and rounding. If the blank signal or the BP1_UPDATE command occurs during the measurement period, the estimate is consider invalid and this register is not updated. When the DC error is over the recommended range, than coarse DC adjustments must be made in the RF down converter.

0x10100248 BP1_SCH2_AMPL_MON

Type: Read
Clock: BP1_CLK
Reset State: 0x0

BP1_SCH2_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP1_SCH2_AMPLMONQ	Signal amplitude estimate for the Q component of sub-channel 2.
10:0	BP1_SCH2_AMPLMONI	Signal amplitude estimate for the I component of sub-channel 2. The amplitude estimate is done on the 12-bit signal at the input to the final quantizer. It is performed by integrating the signal magnitude over a 1 ms period, which contains 2046 samples. The result is approximately normalized by dividing by 2048 (that is, the result is shifted right by 11 positions). This provides a mean-magnitude estimate of the signal, which can be converted to RMS by multiplying by sqrt(p/2). If the blank signal or the BP1_UPDATE command occurs during the measurement period, the estimate is consider invalid and this register is not updated.

0x1010024C BP1_SCH3_AMPL_MON

Type: Read
Clock: BP1_CLK
Reset State: 0x0

BP1_SCH3_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP1_SCH3_AMPLMONQ	Signal amplitude estimate for the Q component of sub-channel 3.

BP1_SCH3_AMPL_MON (cont.)

Bits	Name	Description
10:0	BP1_SCH3_AMPLMONI	Signal amplitude estimate for the I component of sub-channel 3. The estimate is performed by the same method as sub-channel 2, except the estimation interval contains 4092 samples and is approximately normalized by dividing by 4096.

10.2.4 Baseband Processor 2 Command Registers

NOTE All command register settings take effect at the next frame start from the master BP or BP2_UPDATE command unless otherwise noted.

0x10100300 BP2_CONFIG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_CONFIG

Bits	Name	Description
31:30	RESERVED_BITS	
29:28	BP2_SA_PROBE	See BP1_SA_PROBE
27	BP2_TESTINSEL	See BP1_TESTINSEL
26:24	BP2_TESTSEL	See BP1_TESTSEL
23	BP2_PREAMPLMON_EN	See BP1_PREAMPLMON_EN
22:19	BP2_GAINSTEP	See BP1_GAINSTEP
18:16	BP2_DCNOTCHPOLE	See BP1_DCNOTCHPOLE
15	BP2_GAINALIGN	See BP1_GAINALIGN
14:13	BP2_MEANMONMODE	See BP1_MEANMONMODE
12	BP2_DCALIGN	See BP1_DCALIGN
11	BP2_AAF_EN	See BP1_AAF_EN
10	BP2_RS_EN	See BP1_RS_EN
9	BP2_RS_LOAD	See BP1_RS_LOAD
8	BP2_IF_TYPE	See BP1_IF_TYPE
7	BP2_AUXSEL	See BP1_AUXSEL
6	BP2_ADCSEL	See BP1_ADCSEL
5	BP2_SCH3_EN	See BP1_SCH3_EN
4	BP2_SCH2_EN	See BP1_SCH2_EN

BP2_CONFIG (cont.)

Bits	Name	Description
3:2	BP2_RATE	See BP1_RATE
1	BP2_UPDATE	See BP1_UPDATE
0	BP2_INIT	See BP1_INIT

0x10100304 BP2_IF_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_IF_FREQ

Bits	Name	Description
31:25	RESERVED_BITS	
24:22	BP2_INTDELAY	See BP1_INTDELAY
21:16	BP2_FRACDELAY	See BP1_FRACDELAY
15:0	BP2_IFFREQ	See BP1_IFFREQ

0x10100308 BP2_RS_RATE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_RS_RATE

Bits	Name	Description
31:0	BP2_RSRATE	See BP1_RSRATE

0x1010030C BP2_OFFSET

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_OFFSET

Bits	Name	Description
31:16	BP2_OFFSETQ	See BP1_OFFSETQ

BP2_OFFSET (cont.)

Bits	Name	Description
15:0	BP2_OFFSETI	See BP1_OFFSETI

0x10100310 BP2_NOTCH1

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_NOTCH1

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP2_NOTCHMODE1	See BP1_NOTCHMODE1
22:20	BP2_NOTCHPOLE1	See BP1_NOTCHPOLE1
19:0	BP2_NOTCHFREQ1	See BP1_NOTCHFREQ1

0x10100314 BP2_NOTCH2

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_NOTCH2

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP2_NOTCHMODE2	See BP1_NOTCHMODE1
22:20	BP2_NOTCHPOLE2	See BP1_NOTCHPOLE1
19:0	BP2_NOTCHFREQ2	See BP1_NOTCHFREQ1

0x10100318 BP2_NOTCH3

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_NOTCH3

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP2_NOTCHMODE3	See BP1_NOTCHMODE1
22:20	BP2_NOTCHPOLE3	See BP1_NOTCHPOLE1
19:0	BP2_NOTCHFREQ3	See BP1_NOTCHFREQ1

0x1010031C BP2_NOTCH4

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_NOTCH4

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP2_NOTCHMODE4	See BP1_NOTCHMODE1
22:20	BP2_NOTCHPOLE4	See BP1_NOTCHPOLE1
19:0	BP2_NOTCHFREQ4	See BP1_NOTCHFREQ1

0x10100320 BP2_NOTCH5

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_NOTCH5

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP2_NOTCHMODE5	See BP1_NOTCHMODE1
22:20	BP2_NOTCHPOLE5	See BP1_NOTCHPOLE1
19:0	BP2_NOTCHFREQ5	See BP1_NOTCHFREQ1

0x10100324 BP2_NOTCH6

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_NOTCH6

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP2_NOTCHMODE6	See BP1_NOTCHMODE1
22:20	BP2_NOTCHPOLE6	See BP1_NOTCHPOLE1
19:0	BP2_NOTCHFREQ6	See BP1_NOTCHFREQ1

0x10100328 BP2_EQ_COEF_REAL

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_EQ_COEF_REAL

Bits	Name	Description
31:24	RESERVED_BITS	
23:16	BP2_EQCOEF3I	See BP1_EQCOEF3I
15:8	BP2_EQCOEF2I	See BP1_EQCOEF2I
7:0	BP2_EQCOEF1I	See BP1_EQCOEF1I

0x1010032C BP2_EQ_COEF_IMAG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_EQ_COEF_IMAG

Bits	Name	Description
31:24	RESERVED_BITS	
23:16	BP2_EQCOEF3Q	See BP1_EQCOEF3Q
15:8	BP2_EQCOEF2Q	See BP1_EQCOEF2Q
7:0	BP2_EQCOEF1Q	See BP1_EQCOEF1Q

0x10100330 BP2_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_FREQ

Bits	Name	Description
31:0	BP2_FREQ	See BP1_FREQ

0x10100334 BP2_THRESH

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_THRESH

Bits	Name	Description
31:24	BP2_SCH3_THRESHQ	See BP1_SCH2_THRESHI
23:16	BP2_SCH3_THRESHI	See BP1_SCH2_THRESHI
15:8	BP2_SCH2_THRESHQ	See BP1_SCH2_THRESHI
7:0	BP2_SCH2_THRESHI	See BP1_SCH2_THRESHI

0x10100338 BP2_PRE_NOTCH

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_PRE_NOTCH

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP2_PRENOTCHMODE	See BP1_NOTCHMODE1
22:20	BP2_PRENOTCHPOLE	See BP1_NOTCHPOLE1
19:0	BP2_PRENOTCHFREQ	See BP1_NOTCHFREQ1

0x1010033C BP2_RS_PHASE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP2_RS_PHASE

Bits	Name	Description
31:0	BP2_RSPHASE	See BP1_RSPHASE

0x10100340 BP2_PRE_AMPL_MON

Type: Read
Clock: BP2_CLK
Reset State: 0x0

BP2_PRE_AMPL_MON

Bits	Name	Description
31:16	BP2_PREAMPLMONQ	See BP1_PREAMPLMONI
15:0	BP2_PREAMPLMONI	See BP1_PREAMPLMONI

0x10100344 BP2_MEAN_MON

Type: Read
Clock: BP2_CLK
Reset State: 0x0

BP2_MEAN_MON

Bits	Name	Description
31:16	BP2_MEANMONQ	See BP1_MEANMONI
15:0	BP2_MEANMONI	See BP1_MEANMONI

0x10100348 BP2_SCH2_AMPL_MON

Type: Read
Clock: BP2_CLK
Reset State: 0x0

BP2_SCH2_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP2_SCH2_AMPLMONQ	See BP1_SCH2_AMPLMONQ
10:0	BP2_SCH2_AMPLMONI	See BP1_SCH2_AMPLMONI

0x1010034C BP2_SCH3_AMPL_MON

Type: Read
Clock: BP2_CLK
Reset State: 0x0

BP2_SCH3_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP2_SCH3_AMPLMONQ	See BP1_SCH3_AMPLMONQ
10:0	BP2_SCH3_AMPLMONI	See BP1_SCH3_AMPLMONI

10.2.5 Baseband Processor 3 Command Registers

NOTE All command register settings take effect at the next frame start from the master BP or BP3_UPDATE command unless otherwise noted.

0x10100400 BP3_CONFIG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_CONFIG

Bits	Name	Description
31:30	RESERVED_BITS	
29:28	BP3_SA_PROBE	See BP1_SA_PROBE
27	BP3_TESTINSEL	See BP1_TESTINSEL

BP3_CONFIG (cont.)

Bits	Name	Description
26:23	BP3_TESTSEL	Specifies the probe point to send to the BP3 test bus output 0x0: OFF (zero out) 0x1: P1 (sub-ch 1 final quantizer input) 0x2: P2 (sub-ch 2 final quantizer input) 0x3: P3 (sub-ch 3 final quantizer input) 0x4: P4 (sub-ch 4 final quantizer input) 0x1: P5 (sub-ch 5 final quantizer input) 0x2: P6 (sub-ch 6 final quantizer input) 0x3: P7 (sub-ch 7 final quantizer input) 0x4: P8 (sub-ch 8 final quantizer input) 0x1: P9 (sub-ch 9 final quantizer input) 0x2: P10 (sub-ch 10 final quantizer input) 0x3: P11 (sub-ch 11 final quantizer input) 0x4: P12 (sub-ch 12 final quantizer input) 0xD: P13 (linear interpolator input) 0xE: P14 (linear interpolator output) 0xF: P15 (equalizer output)
22	BP3_PREAMPLMON_EN	See BP1_PREAMPLMON_EN
21:18	BP3_GAINSTEP	See BP1_GAINSTEP
17:15	BP3_DCNOTCHPOLE	See BP1_DCNOTCHPOLE
14	BP3_GAINALIGN	See BP1_GAINALIGN
13:12	BP3_MEANMONMODE	See BP1_MEANMONMODE
11	BP3_DCALIGN	See BP1_DCALIGN
10	BP3_AAF_EN	See BP1_AAF_EN
9	BP3_RS_EN	See BP1_RS_EN
8	BP3_RS_LOAD	See BP1_RS_LOAD
7	BP3_IF_TYPE	See BP1_IF_TYPE
6	BP3_AUXSEL	See BP1_AUXSEL
5	BP3_ADCSEL	See BP1_ADCSEL
4	BP3_MODE	Enable BP3 control and front-end processing independent of sub-channel states. See BP3_SCH _MODE 0x0: OFF 0x1: ON

BP3_CONFIG (cont.)

Bits	Name	Description
3:2	BP3_RATE	BP 3 sample rate Note this command takes effect immediately. It should match the rate specified for the ADC processor that is the source for this BP. See AD _RATE. 0x0: OFF (disable BP 3 time base) 0x1: FULL (main clock rate) 0x2: HALF (half of main clock rate) 0x3: OFF2 (disable BP 3 time base)
1	BP3_UPDATE	See BP1_UPDATE
0	BP3_INIT	See BP1_INIT

0x10100404 BP3_IF_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_IF_FREQ

Bits	Name	Description
31:25	RESERVED_BITS	
24:22	BP3_INTDELAY	Group delay compensation, integer part. Number of unit sample delays added to the signal path. The range is 0 to 6 sample delays at 10.22 MHz sample rate, which is equivalent to range of 0 to 587 ns with steps of 97.8 ns.
21:16	BP3_FRACDELAY	Group delay compensation, fraction part. Fraction of unit sample delay added to the signal path. The command range of 0 to 63 is assigned to sample delays from 0 to 63/64 in steps of 1/64 sample period, which is equivalent to 1.53 ns steps.
15:0	BP3_IFFREQ	Digital IF down converter frequency. Represented as signed fractional value (i.e., negative values are for down-conversion). BP3_IFFREQ = fc / fs *216 where fc is the down converter frequency, and fs is the ADC sample rate, which are equal or higher than 81.84 or 40.92 when the resampler is used (default case when processing GPS simultaneously).

0x10100408 BP3_RS_RATE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_RS_RATE

Bits	Name	Description
31:0	BP3_RSRATE	Resampler rate command. An unsigned 32-bit fraction (U0.32) that is added to the sample phase accumulator on ever valid RS output sample. The command is based on the ratio of output sample rate to input sample rate. BP3_RSRATE = (fs / fo -1) * 232 where fs is the ADC sample rate, and fo is the resampler output rate of 81.76 or 40.88 MHz based on BP3_RATE. The ratio of fs / fo must be greater than 1 but less than 1.5.

0x1010040C BP3_OFFSET

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_OFFSET

Bits	Name	Description
31:16	BP3_OFFSETQ	See BP1_OFFSETQ
15:0	BP3_OFFSETI	See BP1_OFFSETI

0x10100410 BP3_NOTCH1

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_NOTCH1

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP3_NOTCHMODE1	See BP1_NOTCHMODE1
22:20	BP3_NOTCHPOLE1	See BP1_NOTCHPOLE1
19:0	BP3_NOTCHFREQ1	Notch filter center frequency, represented as signed fractional value (S1.19). BP3_NOTCHFREQ1 = fc / 10.22 MHz * 220

0x10100414 BP3_NOTCH2

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_NOTCH2

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP3_NOTCHMODE2	See BP1_NOTCHMODE1
22:20	BP3_NOTCHPOLE2	See BP1_NOTCHPOLE1
19:0	BP3_NOTCHFREQ2	See BP3_NOTCHFREQ1

0x10100418 BP3_NOTCH3

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_NOTCH3

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP3_NOTCHMODE3	See BP1_NOTCHMODE1
22:20	BP3_NOTCHPOLE3	See BP1_NOTCHPOLE1
19:0	BP3_NOTCHFREQ3	See BP3_NOTCHFREQ1

0x1010041C BP3_NOTCH4

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_NOTCH4

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP3_NOTCHMODE4	See BP1_NOTCHMODE1
22:20	BP3_NOTCHPOLE4	See BP1_NOTCHPOLE1
19:0	BP3_NOTCHFREQ4	See BP3_NOTCHFREQ1

0x10100420 BP3_NOTCH5

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_NOTCH5

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP3_NOTCHMODE5	See BP1_NOTCHMODE1
22:20	BP3_NOTCHPOLE5	See BP1_NOTCHPOLE1
19:0	BP3_NOTCHFREQ5	See BP3_NOTCHFREQ1

0x10100424 BP3_NOTCH6

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_NOTCH6

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP3_NOTCHMODE6	See BP1_NOTCHMODE1
22:20	BP3_NOTCHPOLE6	See BP1_NOTCHPOLE1
19:0	BP3_NOTCHFREQ6	See BP3_NOTCHFREQ1

0x10100428 BP3_EQ_COEF_REAL

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_EQ_COEF_REAL

Bits	Name	Description
31:24	RESERVED_BITS	
23:16	BP3_EQCOEF3I	See BP1_EQCOEF3I
15:8	BP3_EQCOEF2I	See BP1_EQCOEF2I
7:0	BP3_EQCOEF1I	See BP1_EQCOEF1I

0x1010042C BP3_EQ_COEF_IMAG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_EQ_COEF_IMAG

Bits	Name	Description
31:24	RESERVED_BITS	
23:16	BP3_EQCOEF3Q	See BP1_EQCOEF3Q
15:8	BP3_EQCOEF2Q	See BP1_EQCOEF2Q
7:0	BP3_EQCOEF1Q	See BP1_EQCOEF1Q

0x10100430 BP3_RS_PHASE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_RS_PHASE

Bits	Name	Description
31:0	BP3_RSPHASE	See BP1_RSPHASE

0x10100434 BP3_SCH1_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH1_FREQ

Bits	Name	Description
31:0	BP3_SCH1_FREQ	Sub-channel frequency converter. Set to one of 14 possible Glonass channel frequencies plus fine adjustment to compensate for residual frequency offset. Represented as signed fractional value (i.e., negative values are for down-conversion). BP3_SCH1_FREQ = fc / 10.22 MHz * 232

0x10100438 BP3_SCH2_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH2_FREQ

Bits	Name	Description
31:0	BP3_SCH2_FREQ	See BP3_SCH1_FREQ

0x1010043C BP3_SCH3_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH3_FREQ

Bits	Name	Description
31:0	BP3_SCH3_FREQ	See BP3_SCH1_FREQ

0x10100440 BP3_SCH4_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH4_FREQ

Bits	Name	Description
31:0	BP3_SCH4_FREQ	See BP3_SCH1_FREQ

0x10100444 BP3_SCH5_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH5_FREQ

Bits	Name	Description
31:0	BP3_SCH5_FREQ	See BP3_SCH1_FREQ

0x10100448 BP3_SCH6_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH6_FREQ

Bits	Name	Description
31:0	BP3_SCH6_FREQ	See BP3_SCH1_FREQ

0x1010044C BP3_SCH7_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH7_FREQ

Bits	Name	Description
31:0	BP3_SCH7_FREQ	See BP3_SCH1_FREQ

0x10100450 BP3_SCH8_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH8_FREQ

Bits	Name	Description
31:0	BP3_SCH8_FREQ	See BP3_SCH1_FREQ

0x10100454 BP3_SCH9_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH9_FREQ

Bits	Name	Description
31:0	BP3_SCH9_FREQ	See BP3_SCH1_FREQ

0x10100458 BP3_SCH10_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH10_FREQ

Bits	Name	Description
31:0	BP3_SCH10_FREQ	See BP3_SCH1_FREQ

0x1010045C BP3_SCH11_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH11_FREQ

Bits	Name	Description
31:0	BP3_SCH11_FREQ	See BP3_SCH1_FREQ

0x10100460 BP3_SCH12_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH12_FREQ

Bits	Name	Description
31:0	BP3_SCH12_FREQ	See BP3_SCH1_FREQ

0x10100464 BP3_THRESH_A

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_THRESH_A

Bits	Name	Description
31:24	BP3_SCH2_THRESHQ	See BP1_SCH1_THRESHI
23:16	BP3_SCH2_THRESHI	See BP1_SCH1_THRESHI

BP3_THRESH_A (cont.)

Bits	Name	Description
15:8	BP3_SCH1_THRESHQ	See BP1_SCH1_THRESHI
7:0	BP3_SCH1_THRESHI	See BP1_SCH1_THRESHI

0x10100468 BP3_THRESH_B

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_THRESH_B

Bits	Name	Description
31:24	BP3_SCH4_THRESHQ	See BP1_SCH1_THRESHI
23:16	BP3_SCH4_THRESHI	See BP1_SCH1_THRESHI
15:8	BP3_SCH3_THRESHQ	See BP1_SCH1_THRESHI
7:0	BP3_SCH3_THRESHI	See BP1_SCH1_THRESHI

0x1010046C BP3_THRESH_C

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_THRESH_C

Bits	Name	Description
31:24	BP3_SCH6_THRESHQ	See BP1_SCH1_THRESHI
23:16	BP3_SCH6_THRESHI	See BP1_SCH1_THRESHI
15:8	BP3_SCH5_THRESHQ	See BP1_SCH1_THRESHI
7:0	BP3_SCH5_THRESHI	See BP1_SCH1_THRESHI

0x10100470 BP3_THRESH_D

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_THRESH_D

Bits	Name	Description
31:24	BP3_SCH8_THRESHQ	See BP1_SCH1_THRESHI
23:16	BP3_SCH8_THRESHI	See BP1_SCH1_THRESHI
15:8	BP3_SCH7_THRESHQ	See BP1_SCH1_THRESHI
7:0	BP3_SCH7_THRESHI	See BP1_SCH1_THRESHI

0x10100474 BP3_THRESH_E

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_THRESH_E

Bits	Name	Description
31:24	BP3_SCH10_THRESHQ	See BP1_SCH1_THRESHI
23:16	BP3_SCH10_THRESHI	See BP1_SCH1_THRESHI
15:8	BP3_SCH9_THRESHQ	See BP1_SCH1_THRESHI
7:0	BP3_SCH9_THRESHI	See BP1_SCH1_THRESHI

0x10100478 BP3_THRESH_F

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_THRESH_F

Bits	Name	Description
31:24	BP3_SCH12_THRESHQ	See BP1_SCH1_THRESHI
23:16	BP3_SCH12_THRESHI	See BP1_SCH1_THRESHI
15:8	BP3_SCH11_THRESHQ	See BP1_SCH1_THRESHI
7:0	BP3_SCH11_THRESHI	See BP1_SCH1_THRESHI

0x1010047C BP3_PRE_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_PRE_AMPL_MON

Bits	Name	Description
31:16	BP3_PREAMPLMONQ	Preliminary amplitude estimator for the Q component. See BP3_PREAMPLMONI
15:0	BP3_PREAMPLMONI	Similar to BP1_PREAMPLMONI, except the accumulator is 32-bits and it is normalized by 16-bits to fit into the 16-bit range of this status register. The amplitude estimate is done on the 16-bit signal at the input to the gain step after mean is subtracted. It is performed by integrating the signal magnitude over the measurement period. The estimate is done with 10220 samples/ms. Thus the actual mean-magnitude of the signal is either 216 / 10220 = 6.413 times the estimate result per ms interval. The RMS value is 4/p times the mean-magnitude value.

0x10100480 BP3_MEAN_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_MEAN_MON

Bits	Name	Description
31:16	BP3_MEANMONQ	Signal mean estimate for the Q component. The estimate is performed by the same method as for the I component.
15:0	BP3_MEANMONI	Signal mean estimate for the I component. The mean estimate is done on the 16-bit signal at the input to the offset subtractor (see BP3_OFFSETI). It is performed by integrating the signal over a 1 ms period, which contains 10220 samples. The result is approximately normalized by dividing by 2048 and 5 (divide by 5 is approximated as 205/1024). If the blank signal or the BP3_UPDATE command occurs during the measurement period, the estimate is consider invalid and this register is not updated. When the DC error is over the recommended range, than coarse DC adjustments must be made in the RF down converter.

0x10100484 BP3_SCH1_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_SCH1_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP3_SCH1_AMPLMONQ	Signal amplitude estimate for the Q component of sub-channel 1. The estimate is performed by the same method as for the I component.
10:0	BP3_SCH1_AMPLMONI	Signal amplitude estimate for the I component of sub-channel 1. The amplitude estimate is done on the 12-bit signal at the input to the final quantizer. It is performed by integrating the signal magnitude over a 1 ms period, which contains 1022 samples. The result is approximately normalized by dividing by 1024 (that is, the result is shifted right by 10 positions). This provides a mean-magnitude estimate of the signal, which can be converted to RMS by multiplying by 4/p. If the blank signal or the BP3_UPDATE command occurs during the measurement period, the estimate is consider invalid and this register is not updated.

0x10100488 BP3_SCH2_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_SCH2_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP3_SCH2_AMPLMONQ	See BP3_SCH1_AMPLMONI
10:0	BP3_SCH2_AMPLMONI	See BP3_SCH1_AMPLMONI

0x1010048C BP3_SCH3_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_SCH3_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP3_SCH3_AMPLMONQ	See BP3_SCH1_AMPLMONI
10:0	BP3_SCH3_AMPLMONI	See BP3_SCH1_AMPLMONI

0x10100490 BP3_SCH4_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_SCH4_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP3_SCH4_AMPLMONQ	See BP3_SCH1_AMPLMONI
10:0	BP3_SCH4_AMPLMONI	See BP3_SCH1_AMPLMONI

0x10100494 BP3_SCH5_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_SCH5_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP3_SCH5_AMPLMONQ	See BP3_SCH1_AMPLMONI
10:0	BP3_SCH5_AMPLMONI	See BP3_SCH1_AMPLMONI

0x10100498 BP3_SCH6_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_SCH6_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP3_SCH6_AMPLMONQ	See BP3_SCH1_AMPLMONI
10:0	BP3_SCH6_AMPLMONI	See BP3_SCH1_AMPLMONI

0x1010049C BP3_SCH7_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_SCH7_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP3_SCH7_AMPLMONQ	See BP3_SCH1_AMPLMONI
10:0	BP3_SCH7_AMPLMONI	See BP3_SCH1_AMPLMONI

0x101004A0 BP3_SCH8_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_SCH8_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP3_SCH8_AMPLMONQ	See BP3_SCH1_AMPLMONI
10:0	BP3_SCH8_AMPLMONI	See BP3_SCH1_AMPLMONI

0x101004A4 BP3_SCH9_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_SCH9_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP3_SCH9_AMPLMONQ	See BP3_SCH1_AMPLMONI
10:0	BP3_SCH9_AMPLMONI	See BP3_SCH1_AMPLMONI

0x101004A8 BP3_SCH10_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_SCH10_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP3_SCH10_AMPLMONQ	See BP3_SCH1_AMPLMONI
10:0	BP3_SCH10_AMPLMONI	See BP3_SCH1_AMPLMONI

0x101004AC BP3_SCH11_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_SCH11_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP3_SCH11_AMPLMONQ	See BP3_SCH1_AMPLMONI
10:0	BP3_SCH11_AMPLMONI	See BP3_SCH1_AMPLMONI

0x101004B0 BP3_SCH12_AMPL_MON

Type: Read
Clock: BP3_CLK
Reset State: 0x0

BP3_SCH12_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	BP3_SCH12_AMPLMONQ	See BP3_SCH1_AMPLMONI
10:0	BP3_SCH12_AMPLMONI	See BP3_SCH1_AMPLMONI

0x101004B4 BP3_SCH_MODE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_SCH_MODE

Bits	Name	Description
31:12	RESERVED_BITS	
11	BP3_SCH12_MODE	Subchannel enable
10	BP3_SCH11_MODE	Subchannel enable
9	BP3_SCH10_MODE	Subchannel enable
8	BP3_SCH9_MODE	Subchannel enable
7	BP3_SCH8_MODE	Subchannel enable
6	BP3_SCH7_MODE	Subchannel enable
5	BP3_SCH6_MODE	Subchannel enable
4	BP3_SCH5_MODE	Subchannel enable
3	BP3_SCH4_MODE	Subchannel enable
2	BP3_SCH3_MODE	Subchannel enable
1	BP3_SCH2_MODE	Subchannel enable
0	BP3_SCH1_MODE	Enable subchannel 1 processing 0x0: OFF 0x1: ON

0x101004B8 BP3_PRE_NOTCH

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP3_PRE_NOTCH

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP3_PRENOTCHMODE	See BP1_NOTCHMODE1
22:20	BP3_PRENOTCHPOLE	See BP1_NOTCHPOLE1
19:0	BP3_PRENOTCHFREQ	See BP1_NOTCHFREQ1

10.2.6 Baseband Processor 4 Command Registers

NOTE All command register settings take effect at the next frame start from the master BP or BP4_UPDATE command unless otherwise noted.

0x10100500 BP4_CONFIG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_CONFIG

Bits	Name	Description
31	RESERVED_BITS	
30:29	BP4_SA_PROBE	See BP1_SA_PROBE
28	BP4_TESTINSEL	See BP1_TESTINSEL
27:25	BP4_TESTSEL	Specifies the probe point to send to the BP4 test bus output 0x0: OFF (zero out) 0x1: P1 (IF down converter output) 0x2: P2 (linear interpolator input) 0x3: P3 (linear interpolator output) 0x4: P4 (decimate by 4 or 3 output) 0x5: P5 (notch filter output) 0x6: P6 (baseband frequency converter output) 0x7: P7 (final quantizer input)
24	BP4_PREAMPLMON_EN	See BP1_PREAMPLMON_EN
23:20	BP4_GAINSTEP	See BP1_GAINSTEP
19:17	BP4_DCNOTCHPOLE	See BP1_DCNOTCHPOLE
16	BP4_GAINALIGN	See BP1_GAINALIGN
15:14	BP4_MEANMONMODE	See BP1_MEANMONMODE
13	BP4_DCALIGN	See BP1_DCALIGN
12	BP4_AAF_EN	See BP1_AAF_EN
11	BP4_RS_EN	See BP1_RS_EN
10	BP4_RS_LOAD	See BP1_RS_LOAD
9	BP4_IF_TYPE	See BP1_IF_TYPE
8	BP4_AUXSEL	See BP1_AUXSEL
7	BP4_ADCSEL	See BP1_ADCSEL

BP4_CONFIG (cont.)

Bits	Name	Description
6:5	BP4_FORMAT	Specifies the chip matched filter type and output rate 0x0: NOCMF (no CMF, 20 spc) 0x1: L1_20 (BPSK1 CMF, 20 spc) 0x2: L1_24 (BOC6,1 CMF, 24 spc, BP4_RATE=R72) 0x3: L5_2 (BPSK10 CMF, 2 spc)
4	BP4_MODE	Enable BP 4 processing It is still possible to keep the time base running with the BP4_RATE command. 0x0: OFF 0x1: ON
3:2	BP4_RATE	BP 4 sample rate, after resampler Note this command takes effect immediately. It should match the rate specified for the ADC processor that is the source for this BP. See AD _RATE. 0x0: OFF (disable BP 4 time base) 0x1: R80 (80 spc) 0x2: R72 (72 spc, only for BOC6,1) 0x3: OFF2
1	BP4_UPDATE	See BP1_UPDATE
0	BP4_INIT	See BP1_INIT

0x10100504 BP4_IF_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_IF_FREQ

Bits	Name	Description
31:25	RESERVED_BITS	
24:22	BP4_INTDELAY	See BP1_INTDELAY
21:16	BP4_FRACDELAY	See BP1_FRACDELAY
15:0	BP4_IFFREQ	See BP1_IFFREQ. Supported sample rate, fs, is only 81.84 MHz or higher when the resampler is used.

0x10100508 BP4_RS_RATE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_RS_RATE

Bits	Name	Description
31:0	BP4_RSRATE	Resampler rate command. An unsigned 32-bit fraction (U0.32) that is added to the sample phase accumulator on ever valid RS output sample. The command is based on the ratio of output sample rate to input sample rate. BP4_RSRATE = (fs / fo -1) * 232 where fs is the ADC sample rate which is greater or equal to 81.84 MHz, and fo is the resampler output rate of 81.84 or 73.656 MHz based on BP4_RATE. The ratio of fs / fo must be greater than 1 but less than 1.5.

0x1010050C BP4_OFFSET

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_OFFSET

Bits	Name	Description
31:16	BP4_OFFSETQ	See BP1_OFFSETQ
15:0	BP4_OFFSETI	See BP1_OFFSETI

0x10100510 BP4_NOTCH1

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_NOTCH1

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP4_NOTCHMODE1	See BP1_NOTCHMODE1
22:20	BP4_NOTCHPOLE1	See BP1_NOTCHPOLE1
19:0	BP4_NOTCHFREQ1	Notch filter center frequency, represented as signed fractional value (S1.19). BP4_NOTCHFREQ1 = fc / fs * 220 where fs is 20.46 or 24.552 MHz based on BP4_RATE command.

0x10100514 BP4_NOTCH2

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_NOTCH2

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP4_NOTCHMODE2	See BP1_NOTCHMODE1
22:20	BP4_NOTCHPOLE2	See BP1_NOTCHPOLE1
19:0	BP4_NOTCHFREQ2	See BP4_NOTCHFREQ1

0x10100518 BP4_NOTCH3

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_NOTCH3

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP4_NOTCHMODE3	See BP1_NOTCHMODE1
22:20	BP4_NOTCHPOLE3	See BP1_NOTCHPOLE1
19:0	BP4_NOTCHFREQ3	See BP4_NOTCHFREQ1

0x1010051C BP4_NOTCH4

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_NOTCH4

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP4_NOTCHMODE4	See BP1_NOTCHMODE1
22:20	BP4_NOTCHPOLE4	See BP1_NOTCHPOLE1
19:0	BP4_NOTCHFREQ4	See BP4_NOTCHFREQ1

0x10100520 BP4_NOTCH5

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_NOTCH5

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP4_NOTCHMODE5	See BP1_NOTCHMODE1
22:20	BP4_NOTCHPOLE5	See BP1_NOTCHPOLE1
19:0	BP4_NOTCHFREQ5	See BP4_NOTCHFREQ1

0x10100524 BP4_NOTCH6

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_NOTCH6

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP4_NOTCHMODE6	See BP1_NOTCHMODE1
22:20	BP4_NOTCHPOLE6	See BP1_NOTCHPOLE1
19:0	BP4_NOTCHFREQ6	See BP4_NOTCHFREQ1

0x10100528 BP4_EQ_COEF_REAL

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_EQ_COEF_REAL

Bits	Name	Description
31:24	RESERVED_BITS	
23:16	BP4_EQCOEF3I	See BP1_EQCOEF3I
15:8	BP4_EQCOEF2I	See BP1_EQCOEF2I
7:0	BP4_EQCOEF1I	See BP1_EQCOEF1I

0x1010052C BP4_EQ_COEF_IMAG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_EQ_COEF_IMAG

Bits	Name	Description
31:24	RESERVED_BITS	
23:16	BP4_EQCOEF3Q	See BP1_EQCOEF3Q
15:8	BP4_EQCOEF2Q	See BP1_EQCOEF2Q
7:0	BP4_EQCOEF1Q	See BP1_EQCOEF1Q

0x10100530 BP4_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_FREQ

Bits	Name	Description
31:0	BP4_FREQ	Fine frequency adjustment. Represented as signed fractional value. Used to compensate for residual frequency offset. BP4_FREQ = fc / fs * 232 where fs is 20.46 or 24.552 MHz based on BP4_RATE command of R80 or R72.

0x10100534 BP4_THRESH

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_THRESH

Bits	Name	Description
31:16	RESERVED_BITS	
15:8	BP4_THRESHQ	Final quantizer threshold for the Q component of sub-channel. Performs the same function as the I component.

BP4_THRESH (cont.)

Bits	Name	Description
7:0	BP4_THRESHI	Final quantizer threshold for the I component of sub-channel. In manual-alignment mode (BP4_GAINALIGN = OFF), this register specifies the first threshold of the 16-level quantizer. The higher thresholds are linearly scaled from this value (that is, the quantizer is linear and symmetrical). For a 16-level quantizer, the optimum threshold equals 0.3352 times the signal RMS value. The RMS value is sqrt(p/2) times the mean-magnitude estimate. The threshold should be set to 0.342 or 0.285 times the mean-magnitude estimate (BP4_AMPLMONI) based on the BP4_RATE command of R80 or R72, respectively (See description in BP4_AMPLMONI). In automatic-alignment mode this register is ignored, and the amplitude estimate measured in the previous millisecond frame is used to determine the optimum threshold setting. The optimum threshold is approximated by 11/32 or 9/32 times the BP4_AMPLMONI.

0x10100538 BP4_RS_PHASE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_RS_PHASE

Bits	Name	Description
31:0	BP4_RSPHASE	See BP1_RSPHASE

0x1010053C BP4_PRE_AMPL_MON

Type: Read
Clock: BP4_CLK
Reset State: 0x0

BP4_PRE_AMPL_MON

Bits	Name	Description
31:16	BP4_PREAMPLMONQ	See BP4_PREAMPLMONI

BP4_PRE_AMPL_MON (cont.)

Bits	Name	Description
15:0	BP4_PREAMPLMONI	Similar to BP1_PREAMPLMONI, except the accumulator is 33-bits and it is normalized by 17-bits to fit into the 16-bit range of this status register. The amplitude estimate is done on the 16-bit signal at the input to the gain step after mean is subtracted. It is performed by integrating the signal magnitude over the measurement period. The estimate is done with either 20460 or 24552 samples/ms based on the BP4_RATE command. Thus the actual mean-magnitude of the signal is either 217 / 20460 = 6.406 or 217 / 24552 = 5.339 times the estimate result per ms interval. The RMS value is 4/p times the mean-magnitude value. Update for prog mode!!!

0x10100540 BP4_MEAN_MON

Type: Read
Clock: BP4_CLK
Reset State: 0x0

BP4_MEAN_MON

Bits	Name	Description
31:16	BP4_MEANMONQ	Signal mean estimate for the Q component. The estimate is performed by the same method as for the I component.
15:0	BP4_MEANMONI	Signal mean estimate for the I component. The mean estimate is done on the 16-bit signal at the input to the offset subtractor (see BP4_OFFSETI). It is performed by integrating the signal over a 1 ms period, which contains either 20460 or 24552 samples (see BP4_RATE). The result is approximately normalized by dividing by 4096 and 5 or 6 based on sample rate. The divide by 5 and 6 are approximated as 205/1024 and 171/1024, respectively. If the blank signal or the BP4_UPDATE command occurs during the measurement period, the estimate is consider invalid and this register is not updated. When the DC error is over the recommended range, than coarse DC adjustments must be made in the RF down converter.

0x10100544 BP4_AMPL_MON

Type: Read
Clock: BP4_CLK
Reset State: 0x0

BP4_AMPL_MON

Bits	Name	Description
31:22	RESERVED_BITS	

BP4_AMPL_MON (cont.)

Bits	Name	Description
21:11	BP4_AMPLMONQ	Signal amplitude estimate for the Q component of sub-channel. The estimate is performed by the same method as for the I component.
10:0	BP4_AMPLMONI	Signal amplitude estimate for the I component of sub-channel. The amplitude estimate is done on the 12-bit signal at the input to the final quantizer. It is performed by integrating the signal magnitude over a 1 ms period, which contains either 20460 or 24552 samples (see BP4_RATE). The result is scaled by dividing by 16384 (the result is shifted right by 14 positions). There is still a residual scale factor of

0x10100548 BP4_PRE_NOTCH

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

BP4_PRE_NOTCH

Bits	Name	Description
31:24	RESERVED_BITS	
23	BP4_PRENOTCHMODE	See BP1_NOTCHMODE1
22:20	BP4_PRENOTCHPOLE	See BP1_NOTCHPOLE1
19:0	BP4_PRENOTCHFREQ	See BP1_NOTCHFREQ1

10.2.7 Test Signal Generator Command Registers

NOTE All command register settings take effect at the next frame start from the master BP unless otherwise noted.

0x10100100 TSG_CMD0

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CMD0

Bits	Name	Description
31:4	RESERVED_BITS	

TSG_CMD0 (cont.)

Bits	Name	Description
3:1	TSG_TESTSEL	Specifies the probe point to send to the TSG test bus output 0x0: OFF (zero out) 0x1: P1 (RX1 signal + noise sum) 0x2: P2 (RX2 signal + noise sum) 0x3: P3 (RX1 SDM output) 0x4: P4 (RX2 SDM output) 0x5: P5 (unused) 0x6: P6 (unused) 0x7: P7 (unused)
0	TSG_INIT	Initializes the TSG and synchronizes it to the receiver time base. After the frame start pulse from the receiver control module, the TSG frame, chip and cycle counters are set to command values, the carrier phase accumulator is set to command, the up-sample phase is set to zero, the seed values for the code and noise generators are loaded, and the data sequence generator is restarted. Command registers are not effected. Command registers can only be initialized by the hardware reset signal from the Modem clock block. 0x0: NO 0x1: YES

0x10100104 TSG_CH1_CONFIG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CH1_CONFIG

Bits	Name	Description
31:19	RESERVED_BITS	
18:16	TSG_CH1_SNR	Ratio of infinite BW signal to noise in 1MHz BW. For var = 0 to 6, SNR (dB) = -46.25 + 6.02 * var If var = 7, then the signal is set to the maximum level (24 dB above case for var = 6) which may be too strong for SDM (TBD). The SNR values will be scaled based on sample rate (TBD)
15:13	TSG_CH1_MODLEV	Amplitude of I and Q modulated signals before frequency conversion. Range is 1 to 7. Note that the code generator output is modulo-2 added with data generator output to produce a composite output (with convention 1=positive value, 0=negative value), and then the result is scaled by mod level command.
12	TSG_CH1_PILOTBIT	Channel 1 pilot sub-channel data bit. Takes effect at start of 20 ms period.
11	TSG_CH1_DATABIT	Channel 1 data sub-channel data bit. Takes effect based on TSG_CH1_DATATYPE.

TSG_CH1_CONFIG (cont.)

Bits	Name	Description
10	TSG_CH1_MEANDER	Option to enable meander (Manchester) encoding of the data sequence before modulation. For the first 10 ms of 20 ms period the data bit is not effected. For the second 10 ms the data bit is inverted.
9:8	TSG_CH1_DATATYPE	Channel 1 data bit type The data bit sequence is restarted after TSG_INIT command. The random sequence is 63 bits (list it here) 0x0: PROG1 (update data bit every 1 ms) 0x1: PROG20 (update data bit every 20 ms) 0x2: TOGGLE (toggle data bit every 20 ms) 0x3: RANDOM (random data bit every 20 ms)
7:6	TSG_CH1_CONSTCODE	Channel 1 code source select. 0x0: NO (non-constant from code generator) 0x1: ONE (constant logic one for CW) 0x2: ZERO (constant logic zero for CW) 0x3: NO2 (non-constant from code generator)
5	TSG_CH1_RS_EN	Channel 1 up-sampler enable (see TSG_CH1_RSRATE) 0x0: OFF 0x1: ON
4:3	TSG_CH1_RATE	Channel 1 sample rate 0x0: OFF (disable CH 1 time base) 0x1: FULL (main clock rate) 0x2: HALF (half of main clock rate) 0x3: QTR (quarter of main clock rate)
2:0	TSG_CH1_MODE	Channel 1 signal mode Note, L1C, L2C, L5 and E5A modes may not be fully functional. E1 mode is not implemented on version 1. 0x0: OFF (disable CH 1) 0x1: L1 (GPS L1-C/A) 0x2: R1 (Glonass R1) 0x3: L1C (GPS L1C) 0x4: L2C (GPS L2C) 0x5: L5 (GPS L5) 0x6: E1 (Galileo E1) 0x7: E5A (Galileo E5A)

0x10100108 TSG_CH1_RS_RATE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CH1_RS_RATE

Bits	Name	Description
31:0	TSG_CH1_RSRATE	Up-sampling rate for code generator. Ratio of code generator sample rate (fs,gen) to TSG output sample rate (fs,out), represented as 32-bit unsigned fractional value. TSG_CH1_RSRATE = fs,gen / fs,out * 232

0x1010010C TSG_CH1_INIT_COUNT

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CH1_INIT_COUNT

Bits	Name	Description
31:22	RESERVED_BITS	
21:17	TSG_CH1_INITFRAME	Initial value of 20 ms frame counter in channel 1 time base. This takes effect at the next RC frame start when the TSG_INIT command is set during the previous millisecond. Setting the frame/chip/sample counters to values other than zero allows the TSG to have a constant time offset with respect to the BPs or other TSG channel.
16:7	TSG_CH1_INITCHIP	Initial value of chip counter in channel 1 time base. Takes effect at same time as TSG_CH1_INITFRAME. For R1 mode the valid range is 0 to 510, and for all other modes the valid range is 0 to 1022.
6:0	TSG_CH1_INITSAMPLE	Initial value of sample counter in channel 1 time base. Takes effect at same time as TSG_CH1_INITFRAME. For R1 mode, the valid range is 0 to 159 or 79 or 39 for full, half or quarter rates. For all other modes, the valid range is 0 to 79 or 39 or 19 for full, half or quarter rates.

0x10100110 TSG_CH1_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CH1_FREQ

Bits	Name	Description
31:24	TSG_CH1_PHASE	Carrier phase. Represented as a fraction of a cycle. Only takes effect after TSG_INIT.

TSG_CH1_FREQ (cont.)

Bits	Name	Description
23:0	TSG_CH1_FREQ	Carrier frequency. Represented as signed fractional value. TSG_CH1_FREQ = fc / fs * 224 where fc is the carrier frequency and fs is the ADC sample rate, which could be higher than 81.84, 40.92 or 20.46 MHz when the up-sampler is used.

0x10100114 TSG_CH1_DATA_SEED

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CH1_DATA_SEED

Bits	Name	Description
31:27	RESERVED_BITS	
26:0	TSG_CH1_DATA_SEED	Data channel seed value for code generator. Loaded every frame and after the TSG_INIT command. Show how it's used for diff modes.

0x10100118 TSG_CH1_PILOT_SEED

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CH1_PILOT_SEED

Bits	Name	Description
31:27	RESERVED_BITS	
26:0	TSG_CH1_PILOT_SEED	Pilot channel seed value for code generator. Loaded every frame and after the TSG_INIT command.

0x1010011C TSG_CH2_CONFIG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CH2_CONFIG

Bits	Name	Description
31:19	RESERVED_BITS	
18:16	TSG_CH2_SNR	See TSG_CH1_SNR
15:13	TSG_CH2_MODLEV	See TSG_CH1_MODLEV
12	TSG_CH2_PILOTBIT	See TSG_CH1_PILOTBIT
11	TSG_CH2_DATABIT	See TSG_CH1_DATABIT
10	TSG_CH2_MEANDER	See TSG_CH1_MEANDER
9:8	TSG_CH2_DATATYPE	See TSG_CH1_DATATYPE
7:6	TSG_CH2_CONSTCODE	See TSG_CH1_CONSTCODE
5	TSG_CH2_RS_EN	See TSG_CH1_RS_EN
4:3	TSG_CH2_RATE	See TSG_CH1_RATE
2:0	TSG_CH2_MODE	See TSG_CH1_MODE

0x10100120 TSG_CH2_RS_RATE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CH2_RS_RATE

Bits	Name	Description
31:0	TSG_CH2_RSRATE	See TSG_CH1_RSRATE

0x10100124 TSG_CH2_INIT_COUNT

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CH2_INIT_COUNT

Bits	Name	Description
31:22	RESERVED_BITS	
21:17	TSG_CH2_INITFRAME	See TSG_CH1_INITFRAME
16:7	TSG_CH2_INITCHIP	See TSG_CH1_INITCHIP
6:0	TSG_CH2_INITSAMPLE	See TSG_CH1_INITSAMPLE

0x10100128 TSG_CH2_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CH2_FREQ

Bits	Name	Description
31:24	TSG_CH2_PHASE	See TSG_CH1_PHASE
23:0	TSG_CH2_FREQ	See TSG_CH1_FREQ

0x1010012C TSG_CH2_DATA_SEED

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CH2_DATA_SEED

Bits	Name	Description
31:27	RESERVED_BITS	
26:0	TSG_CH2_DATA_SEED	See TSG_CH1_DATA_SEED

0x10100130 TSG_CH2_PILOT_SEED

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_CH2_PILOT_SEED

Bits	Name	Description
31:27	RESERVED_BITS	
26:0	TSG_CH2_PILOT_SEED	See TSG_CH1_PILOT_SEED

0x10100134 TSG_RX1_CONFIG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_RX1_CONFIG

Bits	Name	Description
31:14	RESERVED_BITS	
13	TSG_RX1_QUANTSEL	Quantizer type for receiver 1. Linear 6-bit ADC or 2-bit sigma-delta. 0x0: LINEAR 0x1: SDM
12:11	TSG_RX1_SDMQUANT	Quantizer levels for sigma-delta modulator of receiver 1. 0x0: OFF 0x1: Q2 (Two levels) 0x2: Q3 (Three levels) 0x3: Q4 (Four levels)
10:9	TSG_RX1_DACREF	Sigma-delta modulator quantizer reference voltage for receiver 1. 0x0: 100 mV 0x1: 200 mV 0x2: 400 mV 0x3: 800 mV
8:6	TSG_RX1_SDMAMP	Sigma-delta modulator or linear ADC input amplitude for receiver 1. Register value is defined as N, where N is 0 to 7. For SDM, amplitude =
5	TSG_RX1_LPFSW	Option to lowpass filter the composite signal (noise+ch1+ch2) before receiver 1 SDM. 0x0: OFF (Bypass filter with unity gain) 0x1: ON (Enable filter)
4	TSG_RX1_FINEAMP	Fine amplitude control. 0x0: ATTEN (Reduce signal plus noise by 0.75 = -2.5 dB) 0x1: PASS (Pass signal without attenuation)
3	TSG_RX1_SIGNALSW2	Option to add channel 2 signal to receiver 1 composite signal. 0x0: NO 0x1: YES
2	TSG_RX1_SIGNALSW1	Option to add channel 1 signal to receiver 1 composite signal. 0x0: NO 0x1: YES
1	TSG_RX1_NOISESW	Option to add noise generator signal to receiver 1 composite signal. 0x0: NO 0x1: YES
0	TSG_RX1_RATE	Select the source of the time base for receiver 1. Ideally, if both channels are applied to receiver 1, then they should be set to the same rate. See TSG_CH _RATE 0x0: CH1 (channel 1) 0x1: CH2 (channel 2)

0x10100138 TSG_RX1_OFFSET

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_RX1_OFFSET

Bits	Name	Description
31:16	RESERVED_BITS	
15:8	TSG_RX1_NOISESEED	Receiver 1 noise generator seed. Upper 8-bits of seed value for length 32 noise generator. Must be set to non-zero value. Lower 24-bits are set to logic 0. Only loaded after the TSG_INIT command is issued, then free runs.
7:0	TSG_RX1_DCOFFSET	DC offset for receiver 1. This 8-bit signed value has range of +/- 125 mV and resolution of 1 mV (TBD).

0x1010013C TSG_RX2_CONFIG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_RX2_CONFIG

Bits	Name	Description
31:14	RESERVED_BITS	
13	TSG_RX2_QUANTSEL	See TSG_RX1_QUANTSEL
12:11	TSG_RX2_SDMQUANT	See TSG_RX1_SDMQUANT
10:9	TSG_RX2_DACREF	See TSG_RX1_DACREF
8:6	TSG_RX2_SDMAMP	See TSG_RX1_SDMAMP
5	TSG_RX2_LPFSW	See TSG_RX1_LPFSW
4	TSG_RX2_FINEAMP	See TSG_RX1_FINEAMP
3	TSG_RX2_SIGNALSW2	See TSG_RX1_SIGNALSW2
2	TSG_RX2_SIGNALSW1	See TSG_RX1_SIGNALSW1
1	TSG_RX2_NOISESW	See TSG_RX1_NOISESW
0	TSG_RX2_RATE	See TSG_RX1_RATE

0x10100140 TSG_RX2_OFFSET

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_RX2_OFFSET

Bits	Name	Description
31:16	RESERVED_BITS	
15:8	TSG_RX2_NOISESEED	TSG_RX1_NOISESEED
7:0	TSG_RX2_DCOFFSET	TSG_RX1_DCOFFSET

0x10100144 TSG_FIRST_CODE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

TSG_FIRST_CODE

Bits	Name	Description
31:14	RESERVED_BITS	
13:0	TSG_FIRST_CODE	Index of first code bit. Only used for L1C and E1.

0x10100148 TSG_CH1_COUNT_STATUS

Type: Read
Clock: TSG_CLK
Reset State: 0x0

TSG_CH1_COUNT_STATUS

Bits	Name	Description
31:22	RESERVED_BITS	
21:0	TSG_CH1_COUNT	Channel 1 time base counters. For Glonass R1 mode, count_status = {frame_count[4:0], chip_count[8:0], sample_count[7:0]}. For all other modes, count_status = {frame_count[4:0], chip_count[9:0], sample_count[6:0]}.

0x1010014C TSG_CH2_COUNT_STATUS

Type: Read
Clock: TSG_CLK
Reset State: 0x0

TSG_CH2_COUNT_STATUS

Bits	Name	Description
31:22	RESERVED_BITS	
21:0	TSG_CH2_COUNT	See TSG_CH1_COUNT.

10.2.8 Sample Memory Interface Command Registers

NOTE All command register settings take effect at the next frame start from the master BP or SMI_UPDATE command unless otherwise noted.

0x10100600 SMI_MODE

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

SMI_MODE

Bits	Name	Description
31:2	RESERVED_BITS	
1	SMI_UPDATE	See BP1_UPDATE
0	SMI_INIT	See BP1_INIT

0x10100604 SMI_BASEADDR1

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

SMI_BASEADDR1

Bits	Name	Description
31:16	RESERVED_BITS	
15:8	SMI_BASEADDR1_3	Sample memory base address for BP 1 sub-channel 3
7:0	SMI_BASEADDR1_2	Sample memory base address for BP 1 sub-channel 2

0x10100608 SMI_BASEADDR2

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

SMI_BASEADDR2

Bits	Name	Description
31:16	RESERVED_BITS	
15:8	SMI_BASEADDR2_3	Sample memory base address for BP 2 sub-channel 3
7:0	SMI_BASEADDR2_2	Sample memory base address for BP 2 sub-channel 2

0x1010060C SMI_BASEADDR3A

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

SMI_BASEADDR3A

Bits	Name	Description
31:24	SMI_BASEADDR3_4	Sample memory base address for BP 3 sub-channel 4
23:16	SMI_BASEADDR3_3	Sample memory base address for BP 3 sub-channel 3
15:8	SMI_BASEADDR3_2	Sample memory base address for BP 3 sub-channel 2
7:0	SMI_BASEADDR3_1	Sample memory base address for BP 3 sub-channel 1

0x10100610 SMI_BASEADDR3B

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

SMI_BASEADDR3B

Bits	Name	Description
31:24	SMI_BASEADDR3_8	Sample memory base address for BP 3 sub-channel 8
23:16	SMI_BASEADDR3_7	Sample memory base address for BP 3 sub-channel 7
15:8	SMI_BASEADDR3_6	Sample memory base address for BP 3 sub-channel 6
7:0	SMI_BASEADDR3_5	Sample memory base address for BP 3 sub-channel 5

0x10100614 SMI_BASEADDR3C

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

SMI_BASEADDR3C

Bits	Name	Description
31:24	SMI_BASEADDR3_12	Sample memory base address for BP 3 sub-channel 12
23:16	SMI_BASEADDR3_11	Sample memory base address for BP 3 sub-channel 11
15:8	SMI_BASEADDR3_10	Sample memory base address for BP 3 sub-channel 10
7:0	SMI_BASEADDR3_9	Sample memory base address for BP 3 sub-channel 9

0x10100618 SMI_BASEADDR4

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

SMI_BASEADDR4

Bits	Name	Description
31:16	RESERVED_BITS	
15:8	SMI_BASEADDR_SL	Sample memory base address for Sample Log vectors
7:0	SMI_BASEADDR4_1	Sample memory base address for BP 4

10.2.9 Correlation Processor Command Registers

All registers become active after the start control flag.

0x10100700 CP_START

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_START

Bits	Name	Description
31:5	RESERVED_BITS	

CP_START (cont.)

Bits	Name	Description
4	CP_MEM_B_LOCK	Selects the destination memory to be locked for the correlation results. When this bit is logic 1, DM is not allowed access to Memory block B. Upon reset both of the memories are unlocked
3	CP_MEM_A_LOCK	Selects the destination memory to be locked for the correlation results. When this bit is logic 1, DM is not allowed access to Memory block A. Upon reset both of the memories are unlocked.
2	CP_BLANK	When this bit is logic 1, the correlation results are forced to zero before they are entered into result memory. This feature is typically used when an error condition is detected and the next tasks may have corrupted sample set, thus the results are blanked. The CP will operate as specified by the other command registers, but only the results are blanked.
1	CP_DISABLE	When this bit is set to logic 1, the Data Mover is not prohibited from freely accessing CP result memories A/B and all results are forced to zeros. This feature is used when the CCP has detected an error condition and the DM must quickly flush the results to catch up.
0	CP_START	Start control flag. When this bit transitions from logic 0 to logic 1, the CP task is started. It is suggested to write a pattern of logic 1 then logic 0 to this bit.

0x10100704 CP_CONFIG1

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_CONFIG1

Bits	Name	Description
31:27	RESERVED_BITS	
26:21	CP_NR_CORRS	Specifies the number of correlations, K, to perform during the current task. K = 4 * (CP_NR_CORRS+1). Thus, the range is 4 to 256 with resolution of 4.
20	CP_DATA_BIT	Data channel bit. This bit is modulo-2 added with the data channel code generator.
19	CP_PILOT_BIT	Pilot channel bit. This bit is modulo-2 added with the pilot channel code generator.
18	CP_RESULT_MEM	Selects the destination memory for the correlation results. When block A is selected it is locked by the CP and block B is unlocked, and vice versa. One block is always locked while the other is unlocked. This register setting must match CP_MEM_A_LOCK and CP_MEM_B_LOCK registers. 0x0: A (Memory block A) 0x1: B (Memory block B)

CP_CONFIG1 (cont.)

Bits	Name	Description
17	CP_RESULT_BITS	Specifies the number of bits to store the correlation result (per I and Q component). 0x0: FOUR 0x1: EIGHT
16	CP_SAT_BITS	Specifies the signal range of the correlation result (per I and Q component) Note the correlation result may be saturated to a 4-bit range and still stored as a 8-bit value. 0x0: FOUR (saturate to +/- 7) 0x1: EIGHT (saturate to +/- 127)
15:12	CP_SCALE	The scale factor for scaling the 20-bit correlation accumulator into an 8 or 4-bit result. The final correlation result is produced by an arithmetic shift right of the accumulator. The CP_SCALE command specifies a right shift range of 4 to 15 bit positions. If values 0 to 3 are specified then default scaling is 16 positions. Each step is 6 dB.
11	CP_FINE_SCALE	When logic 1, the correlation accumulator is scaled by 3 or + 9.5 dB, otherwise no scaling is performed. This could be followed with an addition shift of 2 positions for CP_SCALE such that the total scale amount is 0.75 or -2.5 dB.
10:7	CP_SUBCH	Specifies the sub-channel number. Other values are not valid and will produce incorrect results. For BP 1 and BP 2 only N1, N2 and N3 are available For BP 3 N1 to N12 are available For BP 4 only N1 is available 0x1: N1 0x2: N2 0x3: N3 0x4: N4 0x5: N5 0x6: N6 0x7: N7 0x8: N8 0x9: N9 0xA: N10 0xB: N11 0xC: N12
6:5	CP_CH	Specifies the channel number 0x0: N1 (Baseband Processor 1) 0x1: N2 (Baseband Processor 2) 0x2: N3 (Baseband Processor 3) 0x3: N4 (Baseband Processor 4)

CP_CONFIG1 (cont.)

Bits	Name	Description
4:0	CP_MODE	Correlation mode. Other values are reserved. 0x0: OFF (need to change to binary vector) 0x1: L1_1 0x2: L1_2 0x3: L1_20 0x4: L1_NU4_20 0x5: L1_NU8_20 0x6: R1_1 0x7: R1_2 0x0: L1C_D_4 0x0: L1C_P_4 0x0: L1C_DP_4 0x0: L1C_P_24 0x0: E1_B_4 0x0: E1_C_4 0x0: E1_BC_4 0x0: E1_B_24 0xA: E1_C_24 0xB: L2C_M_2 0xC: L2C_L_2 0xD: L2C_ML_2 0xE: L5_I_2 0xF: L5_Q_2 0x10: E5A_I_2 0x11: E5A_Q_2

0x10100708 CP_CONFIG2

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_CONFIG2

Bits	Name	Description
31:19	RESERVED_BITS	
18	CP_SI_CONSTCOEF	Allows a fixed coefficient set for the CP sample interpolator instead of programmable set specified in CP_H0 to CP_H23. This feature is for power savings. 0x0: NO (programmable coef) 0x1: YES (fixed coef)

CP_CONFIG2 (cont.)

Bits	Name	Description
17:16	CP_TESTSEL	Specifies the probe point to send to the test bus output 0x0: OFF (zero out) 0x1: P1 (sample interpolator I outputs) 0x2: P2 (sample interpolator Q outputs) 0x3: P3 (TBD)
15	CP_SI_BYPASS	Bypass option for CP sample interpolator. 0x0: NO 0x1: YES (sample delay is zero)
14	CP_FC_BYPASS	Bypass option for CP frequency converter 0x0: NO 0x1: YES
13:12	CP_CONSTCODE	Control to override the code generator output and force the code sequence to a constant value for the duration of correlation interval. 0x0: NO (normal operation) 0x1: ONE (constant logic 1 for the code sequence) 0x2: ZERO (constant logic 0 for the code sequence) 0x3: NO2 (normal operation)
11:10	CP_ALPHA	Specifies the required phase shift of the pilot channel to phase align it with the data channel before coherent sum. This feature is only supported for the correlation modes of L1C_DP_4 and E1_BC_4. 0x0: POS1 (a = +1) 0x1: NEG1 (a = -1) 0x2: POSJ (a = +j) 0x3: NEGJ (a = -j)
9	CP_L2EVEN	Specifies an even/odd frame segment for the L2 correlation modes. The correlation length for even segments is 512 chips and for odd segments it is 511 chips. 0x0: EVEN 0x1: ODD
8	CP_CD_ENABLE	Enable for the optional data channel correlator that will operate concurrently with pilot channel correlators. This feature is only supported for correlation modes L2C_M_2, L1C_P_4, E1_C_4, L5_Q_2 and E5A_Q_2 0x0: NO 0x1: YES
7:2	CP_CD_TIME_OFFSET	Time offset of the optional data channel correlator. The valid command values are 0 to 63.
1:0	CP_CD_SAMP_PHS	Sample phase for the optional data channel correlator. The valid command values are 0 to 3.

0x1010070C CP_SAMPLE_INDEX

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_SAMPLE_INDEX

Bits	Name	Description
31:19	RESERVED_BITS	
18:2	CP_FIRST_INDEX	First sample index within sample memory. The 2 lower bits are the column index and the upper bits are the row index. The number of rows is based on the mode.
1:0	CP_DELAY	Interpolator delay of 2, 2.25, 2.5 and 2.75 samples from CP_FIRST_INDEX for CP_DELAY command settings of 0, 1, 2 and 3, respectively.

0x10100710 CP_PHASE

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_PHASE

Bits	Name	Description
31:24	RESERVED_BITS	
23:0	CP_PHASE	Initial phase of the frequency converter - represented as signed fractional value. phase = p * CP_PHASE * 2-23 radians CP_PHASE = round(phase/p * 223) CP_PHASE = round(phase/2p * 224)

0x10100714 CP_FREQ

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_FREQ

Bits	Name	Description
31:24	RESERVED_BITS	

CP_FREQ (cont.)

Bits	Name	Description
23:0	CP_FREQ	frequency converter - represented as signed fractional value frequency = sample rate/2 * CP_FREQ * 2-23 CP_FREQ = round(frequency/sample_rate * 224)

0x10100718 CP_DATA_SEED

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_DATA_SEED

Bits	Name	Description
31:27	RESERVED_BITS	
26:0	CP_DATA_SEED	Data channel, code generator seed value. For L1-C/A the seed value is CP_DATA_SEED[9:0] For L2C the seed value is CP_DATA_SEED[26:0] For L5 the seed value is CP_DATA_SEED[12:0] For E5A the seed value is CP_DATA_SEED[13:0] For L1C the insertion index is CP_DATA_SEED[13:0] and the Weil index is CP_DATA_SEED[26:14]

0x1010071C CP_PILOT_SEED

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_PILOT_SEED

Bits	Name	Description
31:27	RESERVED_BITS	
26:0	CP_PILOT_SEED	Pilot channel, code generator seed value. For L2C the seed value is CP_PILOT_SEED[26:0] For L5 the seed value is CP_PILOT_SEED[12:0] For E5A the seed value is CP_PILOT_SEED[13:0] For L1C the insertion index is CP_PILOT_SEED[13:0] and the Weil index is CP_PILOT_SEED[26:14]

0x10100720 CP_CODE_INDEX

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_CODE_INDEX

Bits	Name	Description
31:16	RESERVED_BITS	
15:0	CP_FIRST_CODE	Index of first code bit. Only used for L1C and E1. For L1C the first code bit index is CP_FIRST_CODE[13:0] For E1 the code sequence number (SV) is CP_FIRST_CODE[15:12], and code bit number (0 to 4091) is CP_FIRST_CODE[11:0]. The code bit number has typically values of 0, 1023, 2046 and 3069. In version 4, the E1 code memory was reduced to support only 1 SV (only used for evaluation). The CP_FIRST_CODE[15:12] bits are ignored.

0x10100724 CP_COEF1

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_COEF1

Bits	Name	Description
31:24	CP_H3	Interpolation coefficients.
23:16	CP_H2	
15:8	CP_H1	
7:0	CP_H0	

0x10100728 CP_COEF2

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_COEF2

Bits	Name	Description
31:24	CP_H7	Interpolation coefficients.
23:16	CP_H6	

CP_COEF2 (cont.)

Bits	Name	Description
15:8	CP_H5	
7:0	CP_H4	

0x1010072C CP_COEF3

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_COEF3

Bits	Name	Description
31:24	CP_H11	Interpolation coefficients.
23:16	CP_H10	
15:8	CP_H9	
7:0	CP_H8	

0x10100730 CP_COEF4

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_COEF4

Bits	Name	Description
31:24	CP_H15	Interpolation coefficients.
23:16	CP_H14	
15:8	CP_H13	
7:0	CP_H12	

0x10100734 CP_COEF5

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_COEF5

Bits	Name	Description
31:24	CP_H19	Interpolation coefficients.
23:16	CP_H18	
15:8	CP_H17	
7:0	CP_H16	

0x10100738 CP_COEF6

Type: Write/Read
Clock: CP_CLK
Reset State: 0x0

CP_COEF6

Bits	Name	Description
31:24	CP_H23	Interpolation coefficients.
23:16	CP_H22	
15:8	CP_H21	
7:0	CP_H20	

0x1010073C CP_STATUS

Type: Read
Clock: CP_CLK
Reset State: 0x1A

CP_STATUS

Bits	Name	Description
31:30	RESERVED_BITS	
29:6	CP_STALL_CNT	Current value of the stall counter.
5	CP_STALL	Stall state status bit.
4	CP_MEMB_EMPTY	Indicates that correlation result memory B is empty. The CP monitors the number of values written to memory and sets this flag when all values have been fully read by Data Mover.
3	CP_MEMA_EMPTY	Indicates that correlation result memory A is empty.
2	CP_ACTIVE	When logic 1, the CP is actively processing a task.
1	CP_READY	Indicates CP is ready for next start command.

CP_STATUS (cont.)

Bits	Name	Description
0	CP_ERROR	Current value of the error flag. The error flag is set when Data Mover tries to read more correlation results then were stored by CP.

10.2.10 Channel Control Processor Registers

0x10100800 CCP_BREAKPOINT

Type: Read/Write
Clock: CCP_CLK

CCP_BREAKPOINT

Bits	Name	Description
31:21	RESERVED_BITS	
20	CCP_BRKPNT_SET	Writing logic 1 to this register bit will start the next break point check. Writing logic 0 to this register bit will disable break points (CCP will free-run).
19:16	CCP_BRKPNT_SELECT	Select the register to check for target value. 0x0: PC (program counter, 10 bits) 0x1: PS (program status flags, 4-bits or 8-bits) 0x2: G0 0x3: G1 0x4: G2 0x5: G3 0x6: G4 0x7: G5 0x8: G6 0x9: G7 0xA: P0 0xB: P1 0xC: P2 0xD: unused1 0xE: unused2 0xF: unused3
15:0	CCP_BRKPNT_VALUE	Target value for selected register

0x10100804 CCP_BREAK_STATE

Type: Read
Clock: CCP_CLK

CCP_BREAK_STATE

Bits	Name	Description
31:1	RESERVED_BITS	
0	CCP_BREAK_STATE	This register is set when a new break point is set (see CCP_BRKPNT_SET) and cleared after the break point is reached.

0x10100808 CCP_PROG_STATUS

Type: Read
Clock: CCP_CLK

CCP_PROG_STATUS

Bits	Name	Description
31:20	RESERVED_BITS	
19	CCP_FLAG_V	CCP overflow flag
18	CCP_FLAG_N	CCP negative flag
17	CCP_FLAG_C	CCP carry flag
16	CCP_FLAG_Z	CCP zero flag
15:10	RESERVED_BITS2	read all zeros
9:0	CCP_PC	CCP program counter register contents

0x1010080C CCP_G10_STATUS

Type: Read
Clock: CCP_CLK

CCP_G10_STATUS

Bits	Name	Description
31:16	CCP_G1	CCP G1 register contents
15:0	CCP_G0	CCP G0 register contents

0x10100810 CCP_G32_STATUS

Type: Read
Clock: CCP_CLK

CCP_G32_STATUS

Bits	Name	Description
31:16	CCP_G3	CCP G3 register contents

CCP_G32_STATUS (cont.)

Bits	Name	Description
15:0	CCP_G2	CCP G2 register contents

0x10100814 CCP_G54_STATUS

Type: Read
Clock: CCP_CLK

CCP_G54_STATUS

Bits	Name	Description
31:16	CCP_G5	CCP G5 register contents
15:0	CCP_G4	CCP G4 register contents

0x10100818 CCP_G76_STATUS

Type: Read
Clock: CCP_CLK

CCP_G76_STATUS

Bits	Name	Description
31:16	CCP_G7	CCP G7 register contents
15:0	CCP_G6	CCP G6 register contents

0x1010081C CCP_P10_STATUS

Type: Read
Clock: CCP_CLK

CCP_P10_STATUS

Bits	Name	Description
31:16	CCP_P1	CCP P1register contents
15:0	CCP_P0	CCP P0 register contents

0x10100820 CCP_P2_STATUS

Type: Read
Clock: CCP_CLK

CCP_P2_STATUS

Bits	Name	Description
31:16	RESERVED_BITS	
15:0	CCP_P2	CCP P2 register contents

10.2.11 Sample Memory

0x10140000 SM_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

SM_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	Sample memory begin address

0x10164FFC SM_ADDR_END

Type: Read/Write
Clock: MEM_CLK

SM_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	Sample memory end address

10.2.12 Correlation Processor Memories

0x10104000 GPM_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

GPM_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	Galileo pilot code memory

0x101041FC GPM_ADDR_END

Type: Read/Write
Clock: MEM_CLK

GPM_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	Only 1 SV supported in version 4.

0x10108000 GDM_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

GDM_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	Galileo data code memory

0x101081FC GDM_ADDR_END

Type: Read/Write
Clock: MEM_CLK

GDM_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	Only 1 SV supported in version 4.

0x1010C000 CMA_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

CMA_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	Correlation results memory - A block

0x1010EDFC CMA_ADDR_END

Type: Read/Write
Clock: MEM_CLK

CMA_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	

0x10110000 CMB_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

CMB_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	Correlation results memory - B block

0x10112DFC CMB_ADDR_END

Type: Read/Write
Clock: MEM_CLK

CMB_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	

10.2.13 Channel Control Processor Memories and Command Words

0x10114000 CCM_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

CCM_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	Channel command memory

0x101147FC CCM_ADDR_END

Type: Read/Write
Clock: MEM_CLK

CCM_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	

0x10118000 VM_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

VM_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	CCP variable memory

0x10118FFC VM_ADDR_END

Type: Read/Write
Clock: MEM_CLK

VM_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	

0x1011C000 PM_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

PM_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	CCP program memory

0x1011CFFC PM_ADDR_END

Type: Read/Write
Clock: MEM_CLK

PM_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	

Channel Control Processor Command Words

The structure of command words is as follow:

- The first word in memory must be the start command (CCM_START_CMD). General information that is common to all channels is specified here.
- Next are 5 command words per channel (CCM_WORD1_CMD to CCM_WORD5_CMD). The command words are placed into consecutive addresses in memory. There is sufficient memory for up to 100 channels. Note that command words 6 and 7 are currently not implemented in the microcode. They are reserved for the future.

- The last entry in memory is indicated by the end command (CCM_END_CMD). The CCP will parse all the channel commands and store into variable memory until the end command is reached.

0x10115000 CCM_START_CMD

Type: Write/Read
Clock: MEM_CLK

CCM_START_CMD

Bits	Name	Description
31	RESERVED_BITS	
30	CCM_FIRST_MEMORY	This bit sets which memory gets the results of the first channel commands. 0 = memory A, 1 = memory B. The memory set here will stay in effect until CCP gets a channel command with the toggle bit set.
29:10	CCM_WAIT_RTC	This command is compared to the GNSS RTC. The CCP will start processing the channel command set after the count value is reached. Allocate 15-bits for ms count and 5-bits for sub-ms count (upper 5-bits of chip counter).
9:5	CCM_NR_MS	Number of milliseconds for the channel command set. The CCP will continue processing the command set for specified number of ms. It will expect a new command set before the number of ms is reached.
4:0	CCM_MODE	Must be set to 30 for the start command. This command word indicates the start of the channel command set. It is assumed to always be at the first memory address.

0x10115004 CCM_WORD1_CMD

Type: Write/Read
Clock: MEM_CLK

CCM_WORD1_CMD

Bits	Name	Description
31	CCM_SEGMENT_TYPE	Specifies if the processing interval is the full duration of the channel command set (equal to CCM_NR_MS) or only partial duration (less than CCM_NR_MS). 0x0: FULL 0x1: PART
30	CCM_SEGMENT_TERM	Specifies if the segment number (CCM_SEGMENT_NR) is the beginning or ending of processing interval. This command is only valid when CCM_SEGMENT_TYPE = PART. 0x0: BEGIN 0x1: END

CCM_WORD1_CMD (cont.)

Bits	Name	Description
29:21	CCM_NR_CORRS	See CP_NR_CORRS. The command is expanded to handle up to 2048 correlations per channel. If more than 256 correlations are specified, the CCP will allocate additional CP tasks.
20	CCM_BIT1	See CP_PILOT_BIT and CP_DATA_BIT. This command bit may specify the first data (or pilot) channel bit. It is active while current ms is less than CCM_SEGMENT_NR. This is interpreted as a data or pilot channel based on CCM_MODE command.
19	CCM_BIT2	This command bit specifies the second data (or pilot) channel bit. It is active while current ms is greater than (or equal to) CCM_SEGMENT_NR, until the last millisecond (see CCM_NR_MS).
18	CCM_TOGGLE_MEMORY	This bit tells CCP to toggle the current memory from A to B or from B to A. The current memory is where all CP results will be stored. The current memory will stay in effect for all CP tasks until CCP gets a command with the toggle bit set.
17	CCM_RESULT_BITS	See CP_RESULT_BITS
16	CCM_SAT_BITS	See CP_SAT_BITS
15:12	CCM_SCALE	See CP_SCALE
11	CCM_FINE_SCALE	See CP_FINE_SCALE
10:7	CCM_SUBCH	See CP_SUBCH
6:5	CCM_CH	See CP_CH
4:0	CCM_MODE	See CP_MODE

0x10115008 CCM_WORD2_CMD

Type: Write/Read
Clock: MEM_CLK
Reset State: 0x0

CCM_WORD2_CMD

Bits	Name	Description
31:24	CCM_PHASE	This is the upper 8-bits of the CP_PHASE command. The CCP calculates the CP_PHASE value on every ms.
23:0	CCM_FREQ	See CP_FREQ

0x1011500C CCM_WORD3_CMD

Type: Write/Read
Clock: MEM_CLK
Reset State: 0x0

CCM_WORD3_CMD

Bits	Name	Description
31:24	RESERVED_BITS	
23:0	CCM_TIME_INDEX	The time index, modulo 4 ms, for the sample memory index. The upper bits are the integer sample index, which are directly assigned to the CP_FIRST_INDEX command on the first 1 ms interval. The lower bits are fractional sample delay. The 2 most significant fraction bits are directly assigned to the CP_DELAY command. The remaining fraction bits define the fraction of a quarter sample delay. The number of integer and fraction bits is mode dependent. The number format ranges from U17.7 for wideband modes down to U11.13 for Glonass R1_1 mode. For MBOC and wideband L1/L5 the time resolutions are 0.38 ns and 0.32 ns. In all other modes the resolution is 0.24 ns.

0x10115010 CCM_WORD4_CMD

Type: Write/Read
Clock: MEM_CLK

CCM_WORD4_CMD

Bits	Name	Description
31:27	CCM_SEGMENT_NR	Specifies the millisecond segment relative to data/pilot bit transition or the overlay code sequence. The range is typically 0 to 19. Note, the CP_L2EVEN command is derived from the segment number. Note, for L1C and E1 modes the CCP multiples the CCM_SEGMENT_NR by 1023 to determine the CP_FIRST_CODE value.
26:0	CCM_CODE_SEED	See CP_DATA_SEED and CP_PILOT_SEED. This is interpreted as a data or pilot channel seed based on CCM_MODE command. For Glonass R1 modes, CCM_CODE_SEED [19:0] specifies a 20-bit overlay code, 1 bit per ms for 20 ms, with bit 0 as the first bit. For E1 the code sequence number (SV) is CCM_CODE_SEED[3:0]. This specifies one of 16 possible memory codes. The CP_ALPHA command is CCM_CODE_SEED[9:8]

0x10115014 CCM_WORD5_CMD

Type: Write/Read
Clock: MEM_CLK

CCM_WORD5_CMD

Bits	Name	Description
31:24	RESERVED_BITS	
23:22	CCM_CONSTCODE	See CP_CONSTCODE
21:12	CCM_TIME_RESIDUAL	Accumulated time offset in fractions of one-quarter sample index. The sample index resolution is CP mode dependent. This value is used to maintain the sample phase dithering process over multiple command sets.
11:0	CCM_TIME_DOP	Time Doppler offset. This command is an additional time offset that is added (or subtracted) to the time index on every 1 ms interval. This is a signed number. The resolution is 1/32 of the CCM_TIME_INDEX.

0x10115018 CCM_WORD6_CMD

Type: Write/Read
Clock: MEM_CLK

CCM_WORD6_CMD

Bits	Name	Description
31:9	RESERVED_BITS	Note, word 6 is optional. It is only required for modes that have 1 data channel correlator operating concurrently with pilot channel correlators. This option is available on L2C, L1C, L5, E1, E5A pilot channel correlation modes.
8	CCM_CD_ENABLE	See CP_CD_ENABLE
7:2	CCM_CD_TIME_OFFSET	See CP_CD_TIME_OFFSET
1:0	CCM_CD_SAMP_PHS	See CP_CD_SAMP_PHS

0x1011501C CCM_WORD7_CMD

Type: Write/Read
Clock: MEM_CLK

CCM_WORD7_CMD

Bits	Name	Description
31:29	RESERVED_BITS	This command word is only used for L1C, L2C and E5A modes that have concurrent/coherent processing of pilot and data channels. For other modes the data channel seed is added to Word 4. Note word 7 may be used together with word 6 in some modes and separate in other modes (TBD). Thus in some cases word 7 may be the 6th command word.
30:29	CCM_ALPHA	See CP_ALPHA command. This command is specified here for the L1C_DP_4 mode (for E1 it's located in word 4)
28	CCM_DATA_BIT1	This command bit may specify the first data channel bit. It is active until the segment number is reached (see CCM_SEGMENT_NR).
27	CCM_DATA_BIT2	This command bit may specify the second data channel bit. It is active after the segment number is reached and until the last millisecond (see CCM_NR_MS).
26:0	CCM_DATA_SEED	Code generator seed for concurrent data channel. See CCM_SEED and CP_DATA_SEED.

0x10115020 CCM_END_CMD

Type: Write/Read
Clock: MEM_CLK

CCM_END_CMD

Bits	Name	Description
31:5	RESERVED_BITS	
4:0	CCM_MODE	Must be set to 31 for the end command. This command word indicates the end of the channel command set. It should be located in the word following the last channel command.

0x101157DC CCM_STOP_CMD

Type: Write/Read
Clock: MEM_CLK

CCM_STOP_CMD

Bits	Name	Description
31:1	RESERVED_BITS	
0	CCM_STOP	Terminates CCP execution until next load command.

0x101157E0 CCM_LOAD_CMD

Type: Write/Read
Clock: MEM_CLK

CCM_LOAD_CMD

Bits	Name	Description
31:1	RESERVED_BITS	
0	CCM_LOAD	Indicates that a new set of commands has been written to CCM memory. When CCP see this bit set to logic 1, it begins processing the latest command set. After CCP finishes consuming all commands, then it clears this bit and increments the command sequence number. After the specified number of milliseconds is completed, the CCP will again wait for the load command.

0x101157E4 CCM_ERROR_CLEAR_CMD

Type: Write/Read
Clock: MEM_CLK

CCM_ERROR_CLEAR_CMD

Bits	Name	Description
31:1	RESERVED_BITS	
0	CCM_ERROR_CLEAR	After the CCP detects an error, it will go into a wait loop. It will stay in this state until the error clear command is sent (or the CCP is reset). When CCP see this bit set to logic 1, it will immediately clear this bit, error status bits and CP_DISABLE. Then CCP will wait for the next CCM_LOAD command.

0x101157E8 CCM_TIME_MARGIN_CMD

Type: Write/Read
Clock: MEM_CLK

CCM_TIME_MARGIN_CMD

Bits	Name	Description
31:7	RESERVED_BITS	
6:0	CCM_TIME_MARGIN	Specifies the amount of time that a CP task start can be delay before an error condition occurs. See CCM_LATE_TASK_ERROR for usage. This variable is defined as a U2.5 type with unit of millisecond. The typical value is slightly greater than 1. The value could be adjusted based on expected CP utilization for the next command set.

0x101157EC CCM_LATE_TASK_ERROR_STATUS

Type: Read
Clock: MEM_CLK

CCM_LATE_TASK_ERROR_STATUS

Bits	Name	Description
31:1	RESERVED_BITS	
0	CCM_LATE_TASK_ERROR	An error condition occurs when a CP task is started later then the specified time margin. A CP task can be delayed due to commands arriving too late (CCM_LOAD) or Data Mover transfers occurring too late (causing significant stalling). This error bit is set when current RTC is greater than sum of CCM_WAIT_RTC + CCM_TIME_MARGIN + ms_count, where ms_count is from 0 to CCM_NR_MS-1. All variables have unit of millisecond with 5-bit fraction. When the error condition occurs, the CCP will go into a wait loop (see CCM_ERROR_CLEAR) and the CP_DISABLE command will be set.

0x101157F0 CCM_OVERRUN_ERROR_STATUS

Type: Read
Clock: MEM_CLK

CCM_OVERRUN_ERROR_STATUS

Bits	Name	Description
31:1	RESERVED_BITS	
0	CCM_OVERRUN_ERROR	An error condition is set when the Data Mover reads more correlation results than the CP stored. This is considered a catastrophic software error. The error flag is generated by the CP, and can only be cleared by a software reset (RC_SW_RESET) or hardware reset. Before the beginning of each CP task, the CCP transfers the error flag to this memory location. When the error condition occurs, the CCP will go into a wait loop and the CP_DISABLE command will be set.

0x101157F4 CCM_SEQ_NUMBER_STATUS

Type: Read
Clock: MEM_CLK

CCM_SEQ_NUMBER_STATUS

Bits	Name	Description
31:0	CCM_SEQ_NUMBER	Indicates the command set sequence number. After CCP detects the CCM_LOAD command and consumes the command set, it increments the sequence number. This is a modulo 32-bit counter.

0x101157F8 CCM_DONE_RTC_STATUS

Type: Read
Clock: MEM_CLK

CCM_DONE_RTC_STATUS

Bits	Name	Description
31:0	CCM_DONE_RTC	Records the GNSS real time counter state after the last CP task of the millisecond is completed. This is mainly meant for diagnostic purpose. The 32-bit GNSS RTC is composed of {frame_count[15], chip_count[10], sample_count[7]}. Since this value is updated every 1 ms, one should schedule a Data Mover transfer after the correlation results are transferred.

0x101157FC CCM_STALL_COUNT_STATUS

Type: Read
Clock: MEM_CLK

CCM_STALL_COUNT_STATUS

Bits	Name	Description
31:0	CCM_STALL_COUNT	Indicates the approximate number of clock cycles that the CP was stalled due to Data Mover late transfer of correlation result memory. This is mainly meant for diagnostic purpose. Some amount of stalling is tolerable as long as the tasks are not delayed too much. This is a modulo 32-bit counter.

10.2.14 Test Signal Generator Memories

0x10120000 TPM_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

TPM_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	TSG pilot code memory

0x101201FC TPM_ADDR_END

Type: Read/Write
Clock: MEM_CLK

TPM_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	

0x10124000 TDM_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

TDM_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	TSG data code memory

0x101241FC TDM_ADDR_END

Type: Read/Write
Clock: MEM_CLK

TDM_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	

10.2.15 GNSS Tracking Memory

0x10180000 GTM_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

GTM_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	GTM begin address

0x1019FFFC GTM_ADDR_END

Type: Read/Write
Clock: MEM_CLK

GTM_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	GTM end address

10.2.16 Async Resample Command Registers

NOTE all registers in ARS group take effect immediately.

0x10100900 ARS_CONFIG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

ARS_CONFIG

Bits	Name	Description
31:23	RESERVED_BITS	
22:21	ARS_TESTINSEL	When ARS_TESTINSEL[0] = 1, the ADC signals are connected to test bus input instead of normal inputs. adc_in_i = test_bus_in[5:4] adc_in_q = test_bus_in[1:0] When ARS_TESTINSEL[1] = 1, the input to the async resampler block is driven from the test bus input instead of normal inputs. ars_test_i = test_bus_in[9:0] ars_test_q = test_bus_in[19:10]
20:19	ARS_TESTSEL	Specifies the probe point to send to the ARS test bus output 0x0: OFF (zero out) 0x1: P1 (resampler input from AAF) 0x2: P2 (resampler output) 0x3: P3 (ARS_SOFTWARE_DEBUG register)
19:16	ARS_FLOOR_CNT_VAL	Set this register = floor(ref_clk_freq/adc_clk_freq)-1. The hardware compares the latched end count value with this register to determine which phase mapping to select.
15:14	ARS_SAMPLELOG_MODE	See AD_SAMPLELOG_MODE
13	ARS_SAMPLELOG_START	See AD_SAMPLELOG_START
12:10	ARS_SAMPLELOG_DEPTH	See AD_SAMPLELOG_DEPTH
9	ARS_RATE	Resampler output sampling rate with respect to main clock. Used for output clock generation. 0x0: HALF (main clock divided by 2) 0x1: QTR (main clock divided by 4)
8	ARS_AAF_EN	See BP1_AAF_EN

ARS_CONFIG (cont.)

Bits	Name	Description
7	ARS_IF_TYPE	See BP1_IF_TYPE
6	ARS_NULLQ	See AD_RX1_NULLQ
5	ARS_NULLI	See AD_RX1_NULLI
4	ARS_SIGNINVQ	See AD_RX1_SIGNINVQ
3	ARS_SIGNINVI	See AD_RX1_SIGNINVI
2	ARS_SWAPIQ	See AD_RX1_SWAPIQ
1	ARS_SRCSEL	See AD_RX1_SRCSEL
0	ARS_EN	Set to logic 1 to enable the ARS module

0x10100904 ARS_QUANT_MAP

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

ARS_QUANT_MAP

Bits	Name	Description
31:16	RESERVED_BITS	
15:0	ARS_DRX_QUANTMAP	See AD_RX1_QUANTMAP, but only lower 4 values are specified.

0x10100908 ARS_IF_FREQ

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

NOTE ARS_PHASE_MAP_L registers hold the mapping values when the hardware phase counter end value is equal to floor(ref_clk_freq/adc_clk_freq) - 1.
ARS_PHASE_MAP_H registers hold the mapping values when the hardware phase counter end value is greater than floor(ref_clk_freq/adc_clk_freq) - 1.

ARS_IF_FREQ

Bits	Name	Description
31:16	RESERVED_BITS	
15:0	ARS_IFFREQ	See BP1_IFFREQ. fs = ADC sample rate

0x1010090C ARS_PHASE_MAP_L0

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

ARS_PHASE_MAP_L0

Bits	Name	Description
31:28	ARS_PHASE_MAP_L7	The mapped phase when HW generated phase = “0111”
27:24	ARS_PHASE_MAP_L6	The mapped phase when HW generated phase = “0110”
23:20	ARS_PHASE_MAP_L5	The mapped phase when HW generated phase = “0101”
19:16	ARS_PHASE_MAP_L4	The mapped phase when HW generated phase = “0100”
15:12	ARS_PHASE_MAP_L3	The mapped phase when HW generated phase = “0011”
11:8	ARS_PHASE_MAP_L2	The mapped phase when HW generated phase = “0010”
7:4	ARS_PHASE_MAP_L1	The mapped phase when HW generated phase = “0001”
3:0	ARS_PHASE_MAP_L0	The mapped phase when HW generated phase = “0000”

0x10100910 ARS_PHASE_MAP_L8

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

ARS_PHASE_MAP_L8

Bits	Name	Description
31:28	ARS_PHASE_MAP_L15	The mapped phase when HW generated phase = “1111”
27:24	ARS_PHASE_MAP_L14	The mapped phase when HW generated phase = “1110”
23:20	ARS_PHASE_MAP_L13	The mapped phase when HW generated phase = “1101”
19:16	ARS_PHASE_MAP_L12	The mapped phase when HW generated phase = “1100”
15:12	ARS_PHASE_MAP_L11	The mapped phase when HW generated phase = “1011”
11:8	ARS_PHASE_MAP_L10	The mapped phase when HW generated phase = “1010”
7:4	ARS_PHASE_MAP_L9	The mapped phase when HW generated phase = “1001”
3:0	ARS_PHASE_MAP_L8	The mapped phase when HW generated phase = “1000”

0x10100914 ARS_PHASE_MAP_H0

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

ARS_PHASE_MAP_H0

Bits	Name	Description
31:28	ARS_PHASE_MAP_H7	The mapped phase when HW generated phase = “0111”
27:24	ARS_PHASE_MAP_H6	The mapped phase when HW generated phase = “0110”
23:20	ARS_PHASE_MAP_H5	The mapped phase when HW generated phase = “0101”
19:16	ARS_PHASE_MAP_H4	The mapped phase when HW generated phase = “0100”
15:12	ARS_PHASE_MAP_H3	The mapped phase when HW generated phase = “0011”
11:8	ARS_PHASE_MAP_H2	The mapped phase when HW generated phase = “0010”
7:4	ARS_PHASE_MAP_H1	The mapped phase when HW generated phase = “0001”
3:0	ARS_PHASE_MAP_H0	The mapped phase when HW generated phase = “0000”

0x10100918 ARS_PHASE_MAP_H8

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

ARS_PHASE_MAP_H8

Bits	Name	Description
31:28	ARS_PHASE_MAP_H15	The mapped phase when HW generated phase = “1111”
27:24	ARS_PHASE_MAP_H14	The mapped phase when HW generated phase = “1110”
23:20	ARS_PHASE_MAP_H13	The mapped phase when HW generated phase = “1101”
19:16	ARS_PHASE_MAP_H12	The mapped phase when HW generated phase = “1100”
15:12	ARS_PHASE_MAP_H11	The mapped phase when HW generated phase = “1011”
11:8	ARS_PHASE_MAP_H10	The mapped phase when HW generated phase = “1010”
7:4	ARS_PHASE_MAP_H9	The mapped phase when HW generated phase = “1001”
3:0	ARS_PHASE_MAP_H8	The mapped phase when HW generated phase = “1000”

0x1010091C ARS_SW_DEBUG

Type: Write/Read
Clock: WR_CLK
Reset State: 0x0

ARS_SW_DEBUG

Bits	Name	Description
31:0	ARS_SOFTWARE_DEBUG	Software debug & report status register. Values written to this register will appear on the test bus out. See ARS_TESTSEL to configure. Note, test bus out may not be routed off-chip so this feature may not useful.

0x10100920 ARS_MEAN_MON

Type: Read
Clock: MAIN_CLK
Reset State: 0x0

ARS_MEAN_MON

Bits	Name	Description
31:16	ARS_MEANMONQ	
15:0	ARS_MEANMONI	See AD_RX1_PREMEANMONI. fs = ADC sample rate

0x10100924 ARS_AMPL_MON

Type: Read
Clock: MAIN_CLK
Reset State: 0x0

ARS_AMPL_MON

Bits	Name	Description
31:16	ARS_AMPLMONQ	
15:0	ARS_AMPLMONI	See AD_RX1_AMPLMONI. fs = ADC sample rate

0x10100928 ARS_SAMPLE_LOG

Type: Read
Clock: MAIN_CLK
Reset State: 0x0

ARS_SAMPLE_LOG

Bits	Name	Description
31:17	RESERVED_BITS	
16	ARS_SAMPLELOG_DONE	See AD_SAMPLELOG_DONE
15:0	ARS_SAMPLELOG_INDEX	See AD_SL_INDEX. fs = ADC sample rate

10.2.17 GPS Accelerator Command Registers

The writable registers occupy sequential addresses so that the host processor or Data Mover can program all of them with one block transfer. If the GPS accelerator is active, any write to these registers will not be acknowledged until it is inactive. Also, the read-only registers occupy sequential addresses so they can be moved with one block transfer.

0x10100A00 GACC_CLK_CTL

Type: Write/Read
Clock: GACC_WR_CLK
Reset State: 0x0

GACC_CLK_CTL

Bits	Name	Description
31:4	RESERVED_BITS	
3	GACC_TEST_BUS_EN	Enable for test bus output. Set to logic 1 to enable. When logic 0 the bus will be forced to zero.
2	GACC_HW_LCG_EN	Enables dynamic HW clock gating scheme. When logic 1, the GACC can control the clock depending on the FSM state. This allows power savings. When logic 0, the software can control the state of the clock with the GACC_MICRO_CLK_EN register.
1	GACC_SW_CLK_EN	Controls the on/off of the logic clocks associated with core interfaces.
0	GACC_CLK_EN	When GACC_HW_LCG_EN = 0, this bit takes over the clock gating. This controls clocks related to core functions.

0x10100A04 GACC_RTC_WAIT

Type: Write/Read
Clock: GACC_WR_CLK
Reset State: 0

GACC_RTC_WAIT

Bits	Name	Description
31:26	RESERVED_BITS	
25:24	GACC_RTC_SELECT	Determines which RTC input to use for the GACC_PAUSE, GACC_DONE, and GACC_RTC commands. 0x0: GPS 0x1: CDMA 0x2: HDR 0x3: Reserved
23:0	GACC_RTC_WAIT	GACC operation is paused until the subtraction of START_RTC from selected RTC[23:0] results in 0 for bit number 23. After the condition is met, the GACC will send an acknowledge for the write to this register. This effectively holds any bus transfer until a specified time.

0x10100A08 GACC_START_ADDR

Type: Write/Read
Clock: GACC_WR_CLK
Reset State: 0

GACC_START_ADDR

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	GACC_ENERGY_ADDR	Starting address for values within energy memory.
10:0	GACC_SAMPLE_ADDR	Starting address for values within sample memory.

0x10100A0C GACC_COUNT

Type: Write/Read
Clock: GACC_WR_CLK
Reset State: 0

GACC_COUNT

Bits	Name	Description
31:25	GACC_ENERGY_ITER	Specifies the number of coherent integrations for each energy.
24:15	GACC_HYP_ITER	Specifies the number of time hypotheses.
14:8	GACC_SAMP_ITER	Specifies the number of accumulation for each set of samples.
7:0	GACC_FREQ_ITER	Specifies the iterations of frequency loop.

0x10100A10 GACC_INCR

Type: Write/Read
Clock: GACC_WR_CLK
Reset State: 0

GACC_INCR

Bits	Name	Description
31:22	GACC_SAMP_INCR_SAMP	Unsigned increment of the starting sample address after all frequency integrations of a sample offset of a hypothesis. An advance sample pointer to the next sample offset.
21:11	GACC_SAMP_INCR_TIME	Signed increment of the starting sample address after all sample offset integrations of a hypothesis. An advance sample pointer to the next hypothesis.
10:0	GACC_SAMP_INCR_ENERGY	Unsigned increment of the starting sample address after all hypotheses. An advance sample pointer to the samples for the next set of coherent integrations.

0x10100A14 GACC_FREQ

Type: Write/Read
Clock: GACC_WR_CLK
Reset State: 0

GACC_FREQ

Bits	Name	Description
31:16	GACC_FIRST_FREQ	Signed phase step for the first frequency.
15:0	GACC_FREQ_INCR	Signed phase step increment between frequencies.

0x10100A18 GACC_CONFIG

Type: Write/Read
Clock: GACC_WR_CLK
Reset State: 0

GACC_CONFIG

Bits	Name	Description
31:24	RESERVED_BITS	

GACC_CONFIG (cont.)

Bits	Name	Description
23	GACC_ENERGY_MEM_BANK	Specifies the memory bank connections. 0x0: bank 0 is connected to GPS accelerator, bank 1 is connected to Data Mover. 0x1: bank1 is connected to GPS accelerator, bank 0 is connected Data Mover.
22	GACC_SAMPLE_MEM_BANK	Specifies the memory bank connections. 0x0: bank 0 is connected to GPS accelerator, bank 1 is connected to Data Mover. 0x1: bank1 is connected to GPS accelerator, bank 0 is connected Data Mover.
21	GACC_START	Set this bit to 1 to start the GPS accelerator.
20	GACC_COHERENT_OUT	Specifies the format result: 0x0: update energy grid 0x1: output coherent sums
19	GACC_FIRST_ENERGY	Set this bit to 1 to erase the energy sum before adding the first energy.
18:16	GACC_LAST_NFREQ	Specifies the frequency bins in the last iteration of the frequency iteration.
15:5	GACC_COHERENT_LEN	Specifies the coherent integration length.
4:2	GACC_SUM_TRUNC	Specifies the I/Q sum truncation; the maximum is 5.
1:0	GACC_ENERGY_TRUNC	Specifies the energy sum truncation before adding to sum; the maximum is 3.

0x10100A1C GACC_PEAK

Type: Read
Clock: GACC_WR_CLK
Reset State: 0

GACC_PEAK

Bits	Name	Description
31:27	RESERVED_BITS	
26:16	GACC_MAX_INDEX	Specifies the index to the maximum energy grid value.
15:0	GACC_MAX_ENERGY	Specifies the maximum energy grid value.

0x10100A20 GACC_DONE

Type: Read
Clock: GACC_WR_CLK
Reset State: 0

GACC_DONE

Bits	Name	Description
31:24	RESERVED_BITS	
23:0	GACC_DONE_RTC	RTC value when the previous computation completed. When the state machine is in the all_done state, the current RTC is saved in this register. The RTC type is specified in the most recent GACC_PAUSE command.

0x10100A24 GACC_RTC

Type: Read
Clock: GACC_WR_CLK
Reset State: 0

GACC_RTC

Bits	Name	Description
31:24	RESERVED_BITS	
23:0	GACC_CURRENT_RTC	Current RTC value. The RTC type is specified in the most recent GACC_PAUSE command.

0x10100A28 GACC_TEST_BUS_OUT

Type: Read
Reset State: 0xA0

GACC_TEST_BUS_OUT

Bits	Name	Description
31:8	RESERVED_BITS	
7	GACC_AHB2HB_IDLE	Set to 1 when the AHB2AHB bridge is in the idle state.
6	GACC_WAIT_FOR_RTC	Set to 1 when the interface is waiting for the RTC to hit the target value
5	GACC_INTF_IDLE_STATE	Set to 1 when in INTF_IDLE_STATE of interface state machine
4	GACC_READ_PEAK_WAIT_STATE	Set to 1 when in READ_PEAK_WAIT_STATE of interface state machine

GACC_TEST_BUS_OUT (cont.)

Bits	Name	Description
3:1	GACC_SP_CURRENT_STATE	The current state of the signal processing state machine
0	GACC_CLK_IS_ON	Indicates clock activity. Logic 1 means this clock is on.

10.2.18 GACC Memories

0x10128000 GACC_SAMPLE_MEM_START_ADDR

Type: Write/Read
Clock: MEM_CLK

GACC_SAMPLE_MEM_START_ADDR

Bits	Name	Description
31:0	GACC_SAMPLE_MEM	First address of sample memory. The memory is physically partitioned into 2 banks, called bank 0 and 1, each of size 1280 by 16-bits. From the software perspective, this memory appears as 640 by 32-bits with 2 consecutive locations accessed for each 32-bit transfer. The memory bank is selected by SAMPLE_MEM_BANK of the GACC_CONFIG register.

0x101289FC GACC_SAMPLE_MEM_END_ADDR

Type: Write/Read
Clock: MEM_CLK

GACC_SAMPLE_MEM_END_ADDR

Bits	Name	Description
31:0	GACC_SAMPLE_MEM	Last address of sample memory. The memory is physically partitioned into 2 banks, called bank 0 and 1, each of size 1280 by 16-bits. From the software perspective, this memory appears as 640 by 32-bits with 2 consecutive locations accessed for each 32-bit transfer. The memory bank is selected by SAMPLE_MEM_BANK of the GACC_CONFIG register.

0x1012C000 GACC_ENERGY_MEM_START_ADDR

Type: Write/Read
Clock: MEM_CLK

GACC_ENERGY_MEM_START_ADDR

Bits	Name	Description
31:0	GACC_ENERGY_MEM	First address of energy memory.The memory is physically partitioned into 2 banks, called bank 0 and 1, each of size 1280 by 16-bits. From the software perspective, this memory appears as 640 by 32-bits with 2 consecutive locations accessed for each 32-bit transfer. The memory bank is selected by ENERGY_MEM_BANK of the GACC_CONFIG register.

0x1012C9FC GACC_ENERGY_MEM_END_ADDR

Type: Write/Read
Clock: MEM_CLK

GACC_ENERGY_MEM_END_ADDR

Bits	Name	Description
31:0	GACC_ENERGY_MEM	Last address of energy memory.The memory is physically partitioned into 2 banks, called bank 0 and 1, each of size 1280 by 16-bits. From the software perspective, this memory appears as 640 by 32-bits with 2 consecutive locations accessed for each 32-bit transfer. The memory bank is selected by ENERGY_MEM_BANK of the GACC_CONFIG register.

10.2.19 Data Mover Host Command Registers

10.2.19.0.1 Channel programming registers

NOTE Suggestion to use only security domain 0. Thus s = 0 in all register sets.

0x10100B00+4*n HI0_CHn_CMD_PTR_SDs, n=[0..7], s=[0..3]

Type: Read/Write
Clock: DM2_CORE
Reset State: 0xXXXXXXXX

The HI0_CHn_CMD_PTR_SDs register is used to supply the top-level programming structure pointer to the N'th DM2 channel. This register is implemented as a FIFO that can accept two top-level pointers in addition to a third that is executing.

HI0_CHn_CMD_PTR_SDs

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:0	ADDR	Address (in double words) of the command structure

0x10100B40+ 4*n HI0_CHn_RSLT_SDs, n=[0..7], s=[0..3]

Type: Read
Clock: DM2_CORE
Reset State: V(alid) bit=0, all other bits X

The HI0_CHn_RSLT_SDs register is used to read the results produced by N'th DM2 channel.

NOTE Reading this register pops one item from the 3-deep result FIFO. The combined depth of the result FIFO and the top-level pointer FIFO is only allowed to be two deep unless there isn't already a top-level pointer executing in which case the combined depth can be three.

There almost always is a one-to-one correspondence between the top-level pointers and the results. The only exception is when an error occurs (as indicated by ERR). In this case, all queued top-level pointers will be discarded, but only one result will be created.

HI0_CHn_RSLT_SDs

Bits	Name	Description
31	V	Valid - the result is valid If this bit is cleared (0), it indicates that the host has emptied the result FIFO.
3	ERR	Error - The result was generated because of an error
2	F	Flush - The result was generated because of a flush operation
1	TPD	Top pointer done - The result was generated because of the completion of the last command in the top-level programming structure
0	RESERVED_BIT0	

0x10100B80+ 4*n HI0_CHn_FLUSH_STATE0_SDs, n=[0..7], s=[0..3]

Type: Read/Write
Clock: DM2_CORE
Reset State: V(alid) bit = 1, all other bits X

Writing to the HI0_CHn_FLUSH_STATE0_SDs register clears (0) the V bit, which then causes the channel to begin a flush operation. When writing to this register, bit 31 should be set to the desired flush type (discard or graceful). Upon completion of the flush state assembly (as indicated by a set V flag), this and the other five FLUSH_STATE registers will contain the state of the channel at the time of the flush. The DM2 may also initiate a channel flush operation internally when the channel encounters an error.

NOTE If a flush is already underway for a given channel and a result from this flush has not yet been generated, then a subsequent flush to the same channel will have no impact and will not generate a second result. This can be determined by the CH_STATE after

a flush request. If set to FLUSH_WAIT then this indicates that a flush is already in progress and the subsequent flush was ignored.

Also, if the NO_DATA_XFER field is set, then the flush occurred prior any data transfers occurring for the top-level pointer, and thus all other flush state registers will not contain valid data.

If the LAST_CPLE_MPU field is set then the last command list entry processed was an MPU command. As such, all other flush state registers will not contain valid data, except for the PTR_NUM field in the FLUSH_STATE5 register. In this case, PTR_NUM will point to the next CLE entry AFTER the MPU command.

If the NO_INB_INSTR field is set, then the flush occurred at a point where no INB instruction was loaded or being processed. In this case the DPH_CMD_TYPE field of FLUSH_STATE0, the SRC_REM_LEN field of FLUSH_STATE3, and the SRC_DSCR_NUM field of the FLUSH_STATE4 register provide information on the last INB operation to fully complete. This can happen between commands, between scatter/gather indices, or between scatter/gather descriptors.

If the NO_OTB_INSTR field is set, then the flush occurred at a point where no OTB instruction was loaded or being processed. In this case the DST_REM_LEN field of FLUSH_STATE3 and the DST_DSCR_NUM field of the FLUSH_STATE4 register provide information on the last OTB operation to fully complete. This can happen between commands, between scatter/gather indices, or between scatter/gather descriptors.

Also, if both the NO_INB_INSTR and NO_OTB_INSTR fields are set then the flush occurred at a time when no instructions (INB or OTB) were loaded for the channel. This can happen between commands, between scatter/gather indices, or between scatter/gather descriptors. In this case all flush state registers provide information on what just completed rather than what was next to be processed.

When following the requirement that only the FLUSH_STATE1 register, and the PTR_NUM and DSCR_INDX_NUM fields of the FLUSH_STATE5 register are used in conjunction with NO_DATA_XFER, CH_STATE, and LAST_CPLE_MPU to resubmit flushed commands, the NO_INB_INSTR and NO_OTB_INSTR fields can be ignored and are provided for debug purposes only.

Host initiated flush operations only terminate the top-level pointer that is currently being executed. If a second top-level pointer is valid, it will not be affected by the flush.. On the other hand, a flush due to an error condition will flush all top-level pointers.

HI0_CHn_FLUSH_STATE0_SDs

Bits	Name	Description
31	FLUSH_TYPE	Notes: 1. FLUSH_TYPE=1 is only supported for single and box mode commands. It currently is not supported for commands that are zero length, and should not be attempted on commands of zero length or unpredictable results may occur. 2. On reads, this bit indicates the type of flush that occurred based on the command type being processed at the time that the flush was requested. 3. If a graceful flush is requested just as one command is completing and another is about to start, the FLUSH_TYPE may not agree with the DPH_CMD_TYPE. This is because the FLUSH_TYPE is based on the command that is completing, while the DPH_CMD_TYPE will be based on the command that is about to start (assuming another command is loaded). This only occurs under the condition that the flush had no impact on the command completing. For example FLUSH_TYPE = 1 and DPH_CMD_TYPE = SG indicates that a single or box mode command was finishing at the time that a graceful flush was requested, but the next command is of type SG and thus only the SG command was affected by the flush. In this case graceful flush and discard flush are equivalent, since no data is buffered. 0x0: Flush should discard any data already read into data buffer 0x1: Flush should write all INB data received or requested prior to terminating the top-level command
30:21	RESERVED_BITS30_21	
20	CMD_ERR	Indicates that an error occurred when parsing a command. For example if ADDR_MODE=2 (reserved) in the first word of the command. This type of error is imprecise in that the DPH_CMD_TYPE field as well as the FLUSH_STATE1-5 registers provide details of the command that is currently in the data phase (or the last command to complete data phase processing if no commands are in the data phase) at the time that the error occurs. This is because the discard flush is applied as soon as the error is detected. The command that is in the data phase may or may not be the command to cause this type of error since up to two commands are processed at a time (one in data phase and one in command phase).
19	LAST_CPLE_MPU	The last command pointer list entry to be processed was an MPU command. As such, the DPH_CMD_TYPE field, as well as all of the other flush state registers will not contain valid data. The one exception is the PTR_NUM field in FLUSH_STATE5 which is valid.
18	NO_OTB_INSTR	Flush occurred at a time when no OTB instructions were loaded. See above for details.
17	NO_INB_INSTR	Flush occurred at a time when no INB instructions were loaded. See above for details.

HI0_CHn_FLUSH_STATE0_SDs (cont.)

Bits	Name	Description
16	NO_DATA_XFER	The channel had begun to process the top-level pointer for this channel, but no data transfers for the top-level pointer had yet begun. As such, all other flush state registers will not be valid. A result will be generated for this top-level pointer.
15:14	DPH_CMD_TYPE	Specifies the type of command that has been flushed (only valid if CH_STATE is not idle, NO_DATA_XFER is not set (1), and LAST_CPLE_MPU is not set (1)): 0x0: Single 0x1: Scatter/gather 0x2: Reserved_programming 0x3: Box
13	PTR_NUM_OVRFLW	Indicates that the PTR_NUM field in FLUSH_STATE5 has overflowed and is not valid (this is only a status indication, it is not a cause for a flush)
12	DSCR_INDX_OVRFLW	Indicates that the DSCR_INDX_NUM field in FLUSH_STATE5 has overflowed and is not valid (this is only a status indication, it is not a cause for a flush)
11	LEN_ERROR	A flush was triggered internally because a box mode or scatter/gather command encountered a length error.
10	MPU_ERROR	A flush was triggered internally because a command encountered an internal MPU error.
9	DPH_BUS_ERROR	A flush was triggered internally because a command encountered a bus error from one of the data transfer requests.
8	CPH_BUS_ERROR	A flush was triggered internally because a command encountered a bus error from one of the command fetch requests. This type of error is imprecise in that the DPH_CMD_TYPE field as well as the FLUSH_STATE1-5 registers provide details of the command that is currently in the data phase (or the last command to complete data phase processing if no commands are in the data phase) at the time that the error occurs. This is because the discard flush is applied as soon as the error is detected. The command that is in the data phase may or may not be the command to cause this type of error since up to two commands are processed at a time (one in data phase and one in command phase).
7:3	RESERVED_BITS7_3	

HI0_CHn_FLUSH_STATE0_SDs (cont.)

Bits	Name	Description
2:1	CH_STATE	Specifies the processing state of the channel at the time that the flush was requested The channel was completely idle at the time of a flush and thus the flush has been ignored and has no impact. In this case a result will not be generated for this flush request. In this case all of the other flush state registers will not update. They will continue to provide the state of the last flush (if any). The channel was processing a command at the time of the flush. A result will be generated if the flush is due to an error condition, or if flush results are enabled. The channel was already processing a flush (either host initiated or due to an error) at the time that the latest flush was requested. As such, the latest flush request will be ignored. Other flush state registers do not update and continue to correspond to the initial flush. No result will be generated for the latest flush. 0x0: IDLE 0x1: PROCESS 0x3: FLUSH_WAIT
0	V	Indicates that the flush state is now valid. If an error occurs on a top-pointer after the previous top-pointer was flushed, this bit will go low while the DM2 core gathers the flush state for the error. In this case the flush state from the previous top-pointer will be lost if it has not already been read by the host.

0x10100BC0+4*n HI0_CHn_FLUSH_STATE1_SDs, n=[0..7], s=[0..3]

Type: Read
Clock: DM2_CORE
Reset State: 0xXXXXXXXX

The HI0_CHn_FLUSH_STATE1_SDs register is only meaningful if CH_STATE is not idle (00), NO_DATA_XFER is not set (1), and LAST_CPLE_MPU is not set (1).

HI0_CHn_FLUSH_STATE1_SDs

Bits	Name	Description
31:0	CMD_ADDR	Address of the command being processed by the data phase at the time of flush operation.

0x10100C00+4*n HI0_CHn_FLUSH_STATE2_SDs, n=[0..7], s=[0..3]

Type: Read
Clock: DM2_CORE
Reset State: 0xXXXXXXXX

The HI0_CHn_FLUSH_STATE2_SDs register is reserved.

HI0_CHn_FLUSH_STATE2_SDs

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x10100C40+ 4*n HI0_CHn_FLUSH_STATE3_SDs, n=[0..7], s=[0..3]

Type: Read
Clock: DM2_CORE
Reset State: 0xXXXXXXXX

The HI0_CHn_FLUSH_STATE3_SDs register is only meaningful if CH_STATE is not idle (00), NO_DATA_XFER is not set (1), and LAST_CPLE_MPU is not set (1). This register is intended for debug purposes and should not be relied upon by software.

HI0_CHn_FLUSH_STATE3_SDs

Bits	Name	Description
31:16	DST_REM_LEN	Specifies the number of bytes yet to be written to the command's current destination buffer (assuming all outstanding bus requests have completed). In the case of box mode commands, this is the number of bytes remaining for the current line.
15:0	SRC_REM_LEN	Specifies the number of bytes yet to be read from the command's current source buffer (assuming all outstanding bus requests have completed). In the case of box mode commands, this is the number of bytes remaining for the current line.

0x10100C80+ 4*n HI0_CHn_FLUSH_STATE4_SDs, n=[0..7], s=[0..3]

Type: Read
Clock: DM2_CORE
Reset State: 0xXXXXXXXX

The HI0_CHn_FLUSH_STATE4_SDs register is only meaningful if CH_STATE is not idle (00), NO_DATA_XFER is not set (1), and LAST_CPLE_MPU is not set (1). This register is intended only for debug purposes and should not be relied upon for software.

HI0_CHn_FLUSH_STATE4_SDs

Bits	Name	Description
31:16	DST_DSCR_NUM	Box mode commands: Specifies the number of remaining destination lines for the command, including the current line (assuming all outstanding requests completed) Scatter/gather commands: Specifies the scatter/gather command's current destination descriptor position in the descriptor list (assuming all outstanding requests completed)
15:0	SRC_DSCR_NUM	Box mode commands: Specifies the number of remaining source lines for the command, including the current line (assuming all outstanding requests completed) Scatter/gather commands: Specifies the scatter/gather command's current source descriptor position in the descriptor list (assuming all outstanding requests completed)

0x10100CC0+4*n HI0_CHn_FLUSH_STATE5_SDs, n=[0..7], s=[0..3]

Type: Read
Clock: DM2_CORE
Reset State: 0xXXXXXXXX

The HI0_CHn_FLUSH_STATE5_SDs register is only meaningful if CH_STATE is not idle (00), and NO_DATA_XFER is not set (1). If LAST_CPLE_MPU is set (1), then only the PTR_NUM field in this register is valid. In this case PTR_NUM points to the command list entry AFTER the MPU command.

HI0_CHn_FLUSH_STATE5_SDs

Bits	Name	Description
31:24	PTR_NUM	Specifies the current command's list pointer position in the pointer list (assuming all outstanding requests completed).
23:16	DSCR_INDX_NUM	Specifies the indirect scatter/gather command's current descriptor index position in the descriptor index list (assuming all outstanding requests completed).
15:8	BUFFERED_LEN	Specifies the number of data bytes read from the source but not written to the destination (assuming all outstanding requests complete). This field is intended for debug purposes only and should not be relied upon by software.
2:0	RESERVED_BITS2_0	

Interrupt status registers

0x10100E80 HI0_SEC_DOMAIN_IRQ_STATUS_SDS, s=[0..3]

Type: Read
Clock: DM2_CORE
Reset State: 0x00000000

The HI0_SEC_DOMAIN_IRQ_STATUS_SDs register is the N'th security domain's interrupt status register, which reflects the state of only those channels that belong to the N'th security domain. The other IRQ bits are always cleared (0). Reading the N'th security domain's interrupt status register clears (0) all of the interrupt requests from the channels belonging to the N'th security domain. The other channel interrupt requests are not affected.

HI0_SEC_DOMAIN_IRQ_STATUS_SDS

Bits	Name	Description
15	CH_15_IRQ	Indicates a pending interrupt request from channel 15
14	CH_14_IRQ	Indicates a pending interrupt request from channel 14
13	CH_13_IRQ	Indicates a pending interrupt request from channel 13
12	CH_12_IRQ	Indicates a pending interrupt request from channel 12
11	CH_11_IRQ	Indicates a pending interrupt request from channel 11
10	CH_10_IRQ	Indicates a pending interrupt request from channel 10
9	CH_9_IRQ	Indicates a pending interrupt request from channel 9
8	CH_8_IRQ	Indicates a pending interrupt request from channel 8
7	CH_7_IRQ	Indicates a pending interrupt request from channel 7
6	CH_6_IRQ	Indicates a pending interrupt request from channel 6
5	CH_5_IRQ	Indicates a pending interrupt request from channel 5
4	CH_4_IRQ	Indicates a pending interrupt request from channel 4
3	CH_3_IRQ	Indicates a pending interrupt request from channel 3
2	CH_2_IRQ	Indicates a pending interrupt request from channel 2
1	CH_1_IRQ	Indicates a pending interrupt request from channel 1
0	CH_0_IRQ	Indicates a pending interrupt request from channel 0

10.2.19.0.2 Channel status and configuration registers accessible to all security domains

0x10100E00+4*n HI0_CHn_RSLT_CONF_SDs, n=[0..7], s=[0..3]

Type: Read/Write
Clock: DM2_CORE
Reset State: 0x00000002

The HI0_CHn_RSLT_CONF_SDs register provides the interrupt configuration status of the indicated channel.

HI0_CHn_RSLT_CONF_SDs

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	FLUSH_RSLT_EN	When set (1), a result will be generated for each top-level pointer that is flushed due to a host initiated flush. Note that all top-level pointers that either fully complete or that generate an error always produce a result. This bit should be set for normal operation, since it results in a one-to-one correspondence between top-pointers and results (with the only exception being that if a top-pointer causes an error, any top pointers that are queued are discarded without a result)
0	IRQ_EN	Indicates that an interrupt should be generated when the result FIFO becomes not empty, i.e., transition from 0 valid entry to 1 valid entry.

0x10100D00+4*n HI0_CHn_STATUS_SDs, n=[0..7], s=[0..3]

Type: Read
Clock: DM2_CORE
Reset State: 0x00000001

The HI0_CHn_STATUS_SDs register provides the channel status of the indicated channel.

HI0_CHn_STATUS_SDs

Bits	Name	Description
31:29	RSLT_FIFO_CNTR	Number of valid entries in the result FIFO. 0-3 are supported.
28:27	CMD_PTR_FIFO_CNTR	Number of valid entries in the command pointer FIFO. Note that there may also be a command pointer already being processed.
26	CMD_IN_PROGRESS	Indicates that a top-level pointer is currently being processed.
1	RSLT_VLD	At least one valid result may be dequeued from the result FIFO
0	CMD_PTR_RDY	At least one command pointer may be enqueued to the command pointer FIFO. This will only assert if all of the following are true: 1. CMD_PTR_FIFO_CNTR < 2 2. (CMD_PTR_FIFO_CNTR + RSLT_FIFO_CNTR < 2) OR ((CMD_PTR_FIFO_CNTR + RSLT_FIFO_CNTR < 3) AND CMD_IN_PROGRESS = 0)

10.2.19.0.3 Security domain 0 channel configuration and debug registers

0x10100D40+4*n HI0_CHn_CONF, n=[0..7]

Type: Read/Write
Clock: DM2_CORE
Reset State: 0x00000081

The HI0_CHn_CONF register provides the configuration status of the indicated channel and accessible through the security domain 0 only.

HI0_CHn_CONF

Bits	Name	Description
31:16	OTHER_CH_BLK_MASK	Each set (1) bit specifies that the corresponding channel is controlled by this channel via the OCU and OCB control field.
12	RSLT_CONF_SHADOW_EN	If set (1), the CH_CONF field IRQ_EN and FLUSH_RSLT_EN fields are set through register CHn_RSLT_CONF_SDs. During subsequent writes to CHn_CONF, writes to those fields are ignored. If clear, access to CHn_RSLT_CONF_SDs is ignored.
11	MPU_DISABLE	Disables MPU error detection
10	RESERVED_BIT10	
9	PERM_MPU_CONF	Indicates that the MPU configuration structure pointed to by the top-level pointer will be executed. If this bit is cleared (0), all MPU structures will be silently ignored.
8	RESERVED_BIT8	
7	FLUSH_RSLT_EN	When set (1), a result will be generated for each top-level pointer that is flushed due to a host initiated flush. Note that all top-level pointers that either fully complete or that generate an error always produce a result. This bit should be set for normal operation, since it results in a one-to-one correspondence between top-pointers and results (with the only exception being that if a top-pointer causes an error, any top pointers that are queued are discarded without a result)
6	IRQ_EN	Indicates that an interrupt should be generated when the result FIFO becomes not empty, i.e., transition from 0 valid entry to 1 valid entry. if RSLT_CONF_SHADOW_EN is set (1), writes to this field will be ignored.
5:4	SEC_DOMAIN	Specifies the channel security domain (controls channel programming and status register aliasing, and selects which of the four interrupts should be used by the channel)

HI0_CHn_CONF (cont.)

Bits	Name	Description
3:0	PRIORITY	Specifies channel priority, in which 0 is the highest priority. This is the weight to the arbitration scheme. Note that assigning a channel's priority value to 0 causes the channel to stay at the highest priority, i.e., the channel will always be granted whenever there's a command to be executed, as the accumulator value is never incremented (incremented with 0). The priority can be viewed as the period between service intervals, such that a weight of 1 will be serviced twice as often as a weight of 2. Though arbitration occurs for each client interface separately, a channel's priority is common to all client interfaces. If multiple channels are configured for the same priority and are ready for access to the same client interface, round-robin servicing will be provided between these channels. The only exception to this is if more than one channel is configured as priority 0. In this case the zero-priority channel with the lowest number is always given preference.

0x10100D80+4*n HI0_CHn_DBG_0, n=[0..7]

Type: Read/Write
Clock: DM2_CORE
Reset State: 0x00000000

The HI0_CHn_DBG_0 register is used for debugging purposes for the indicated channel and accessible through the security domain 0 only.

HI0_CHn_DBG_0

Bits	Name	Description
3	REQ_ENG_HALT	When set (1), prevents the channel from being chosen by the arbiter for data transfers. The current operation on the channel (if already selected) will complete.
2	CMD_ENG_HALT	When set (1), prevents the channel from being chosen by the arbiter for command transfers. The current operation on the channel (if already selected) will complete.
1	CMD_PTR_FIFO_HALT	When set (1), prevents the command pointer FIFO from accepting any new command pointers from hosts. The writes to the command pointer register will be ignored.
0	ERROR	When set (1), indicates that the channel has encountered an error and is now in the stalled state. Specific error information may be obtained by reading the channel flush state registers (see Error handling section). The software must clear (0) this bit before the channel may be used again. This bit can only be cleared by S/W; it cannot be set to 1 by S/W.

0x10100DC0+4*n HI0_CHn_DBG_1, n=[0..7]

Type: Read
Clock: DM2_CORE
Reset State: 0xXXXXXXXX

The HI0_CHn_DBG_1 register is used for additional debugging purposes for the indicated channel and accessible through the security domain 0 only.

HI0_CHn_DBG_1

Bits	Name	Description
31:0	DBG_STATE	TBD

10.2.19.0.4 Global configuration, and debug registers

0x10100E90+4*n HI0_CIn_CONF, n=[0..7]

Type: Read/Write
Clock: DM2_CORE
Reset State: 0x00010001

The HI0_CIn_CONF register is the CI configuration register for the indicated client interface.

It is possible to configure two or more client interfaces to have overlapping address regions. In this case accesses to the overlapping region will be sent to the highest numbered client interface. CI0 is the default client interface, and receives accesses to addresses that have not been assigned to any client interface. Setting RANGE_END < RANGE_START will disable the client interface, with the exception of CI0. On reset only CI0 is enabled. While the CI0 RANGE_START and RANGE_END parameters can be written and read, they do not have an impact on the address decode.

HI0_CIn_CONF

Bits	Name	Description
31:24	RANGE_END	Specifies the end of the N'th CI address range in 16-MB blocks. Note that this is the last block within the client interface region. For example setting RANGE_START=0x00 and RANGE_END=0x00 specifies that the client interface supports the address range 0x00000000-0x00FFFFFF. APQ 7200/7500: For CI 1 (SMI), the upper bit of this field must not be set. Any addresses in the range 0x80000000-0xFFFFFFFF must go to CI 0 if unused.
23:16	RANGE_START	Specifies the start of the N'th CI address range in 16-MB blocks

HI0_CIn_CONF (cont.)

Bits	Name	Description
5:4	CI_WEIGHT	Specifies the relative weight that the client interface receives when arbitrating for access to the channel buffer memory. Normally this can be left at 0 for all client interfaces, which means that each CI gets 25% of the channel buffer memory BW when all client interfaces are requesting (more BW is available if not all of the client interfaces are busy). At 133MHz the channel buffer memory has a half-duplex capacity of 500MB/sec. Assuming that each client interface is performing 32-byte bursts, a weight of 0 guarantees at least 125MB/sec of half duplex channel buffer memory BW to each CI. If the CI is doing 16 byte bursts while all other client interfaces are doing 32-byte bursts, then that CI is guaranteed at least 83.3 MB/sec of half duplex BW. If more than this amount of half-duplex BW is required on a single client interface, the CI weight parameter allows for a redistribution of the channel buffer memory BW. The minimum BW that the channel buffer memory will supply to a given CIn is determined by multiplying the following ratio by the BW capacity of the channel buffer memory (500MB/sec at 133MHz) (CI_WEIGHT(CIn)+1)*MAX_BURST_LEN(CIn) --- Sum for i=0 to 3 of ((CI_WEIGHT(CIi)+1)*MAX_BURST_LEN(CIi) Assuming that all bursts are 32-bytes long, then CI_WEIGHT does not need to be set to more than 1. Setting CI_WEIGHT to 1 for a high BW CI and to 0 for the remaining three CIs will result in the channel buffer memory supporting a minimum of 200MB/sec of half-duplex BW to the high BW CI, and 100 MB/sec to each of the remaining 3 low-BW CIs. With a maximum requirement of 100MB/sec full-duplex (200MB/sec half-duplex) across all 4 CIs, this is more than sufficient. Note that this parameter only distributes the BW of the channel buffer memory. It does not ensure that the client interfaces or the command processing can keep up with these rates.
3:0	MAX_BURST_LEN	Specifies the maximum burst length in 32-bit words. Only values of 1, 4, and 8 are currently supported, which specify 1, 4, or 8 word bursts. The following are the limitations of each client interface: AHB client interfaces (CI2, CI3): 1, 4, 8 AXI client interfaces (CI0, CI1): 4, 8 The AXI client interfaces will also work with a setting of 1, but not all bursts are limited to 1 word. It is recommended that AXI client interfaces be set to 8 word bursts and AHB client interfaces be set to at least 4 word bursts for optimal system performance.

0x10100EB0+4*n HI0_CIn_DBG_ERR, n=[0..7]

Type: Read
Clock: DM2_CORE
Reset State: 0x00000000

The HI0_CIn_DBG_ERR register is the CI debug register for the indicated client interface.

HI0_CIn_DBG_ERR

Bits	Name	Description
31:16	DATA_BUS_ERR	The N'th bit in the mask becomes set (1) when the N'th channel data transfer traffic causes a bus error on this interface. By clearing the ERROR bit in the HI0_CHn_DBG_0 register, the bit corresponding to the channel will be cleared in this register.
15:0	CMD_BUS_ERR	The N'th bit in the mask becomes set (1) when the N'th channel command fetch traffic causes a bus error on this interface. By clearing the ERROR bit in the HI0_CHn_DBG_0 register, the bit corresponding to the channel will be cleared in this register.

0x10100ED0 HI0_CRCI_DBG

Type: Read/Write
Clock: DM2_CORE
Reset State: 0x0000FFFF

The HI0_CRCI_DBG register is the CRCI debug register for the indicated CRCI.

HI0_CRCI_DBG

Bits	Name	Description
15:0	CRCI_RST	When set (1), this bit resets the corresponding CRCI and keeps it in the reset state. When cleared (0), this bit re-enables the CRCI. This field becomes all '1' after reset.

0x10100ED4 HI0_CRCI_STATUS

Type: Read
Clock: DM2_CORE
Reset State: 0x00000001

The HI0_CRCI_STATUS register provides the CRCI status.

HI0_CRCI_STATUS

Bits	Name	Description
15:0	CRCI_RDY	Each bit set (1) in this register indicates that the corresponding CRCI has at least one token for sending data or a command

0x10100ED8 HI0_GP_CTL

Type: Read/Write
Clock: DM2_CORE
Reset State: 0x00000000

The HI0_GP_CTL register is a general purpose control register intended for DM2 instance specific control functions.

HI0_GP_CTL

Bits	Name	Description
31:0	GP_CTL	These bits are defined as necessary for DM2 instance specific functions.

0x10100EDC HI0_GP_STATUS

Type: Read
Clock: DM2_CORE
Reset State: 0xXXXXXXXX

The HI0_GP_STATUS register is a general purpose status register intended for DM2 instance specific status information.

HI0_GP_STATUS

Bits	Name	Description
31:0	GP_STATUS	These bits are defined as necessary for DM2 instance specific functions.

0x10100EE0 HI0_GLBL_DBG_CMD_ENG

Type: Read/Write
Clock: DM2_CORE
Reset State: 0xXXXXXXXX

HI0_GLBL_DBG_CMD_ENG

Bits	Name	Description
31:0	DBG_STATE	TBD

0x10100EE4 HI0_GLBL_DBG_REQ_ENG

Type: Read/Write
Clock: DM2_CORE
Reset State: 0xXXXXXXXX

HI0_GLBL_DBG_REQ_ENG

Bits	Name	Description
31:0	DBG_STATE	TBD

0x10100EE8 HI0_GLBL_DBG_XFR_ENG

Type: Read/Write
Clock: DM2_CORE
Reset State: 0xXXXXXXXX

HI0_GLBL_DBG_XFR_ENG

Bits	Name	Description
31:0	DBG_STATE	TBD

0x10100EEC HI0_GLBL_DBG_CHAN_BLK

Type: Read
Clock: DM2_CORE
Reset State: 0x00000000

HI0_GLBL_DBG_CHAN_BLK

Bits	Name	Description
15:0	CHAN_BLK_MASK	Indicates which channel(s) are currently blocked (see other channel block or this channel block command arguments)

0x10100EF0 HI0_GLBL_DBG_CHAN_BLK_CLR

Type: Read/Write
Clock: DM2_CORE
Reset State: 0x00000000

HI0_GLBL_DBG_CHAN_BLK_CLR

Bits	Name	Description
3:0	CHAN_BLK_CLR_CHAN_NNUM	Writing to this register causes the bit, corresponding to the channel number written, in GLBL_DBG_CHAN_BLK register to clear. This allows hosts to selectively clear channel block bits without relying on read-modify-write of GLBL_DBG_CHAN_BLK which would cause race-condition.

0x10100EF4 HI0_GLBL_DBG_TEST_SEL

Type: Read/Write
Clock: DM2_CORE
Reset State: 0x00000000

HI0_GLBL_DBG_TEST_SEL

Bits	Name	Description
5:0	TEST_BUS_SEL	This signal selects the signals to show on the DM2 testbus. The encoding for each set of test signal is as follows: 11xxxx Reserved_programming 0x0: None (output is all zeros) 0x1: Reserved_programming_1 0x2: Reserved_programming_2 0x3: Reserved_programming_3 0x4: Command engine 0x8: Request engine 0xC: Transfer engine 0x10: Reserved_programming_4 0x20: CI0 0x24: CI1 0x28: CI2 0x2C: CI3

10.2.20 Nav Clock Command Registers

0x101F8000 NAV_CLK_ENABLE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

NAV_CLK_ENABLE

Bits	Name	Description
31:5	RESERVED_BITS	
4	NC_RSREF_CLK_ENABLE	Resample reference clock enable
3	NC_ADC2_CLK_ENABLE	Diversity ADC clock enable
2	NC_ADC1_CLK_ENABLE	Primary ADC clock enable
1	NC_MAIN_CLK_ENABLE	Main clock enable
0	NC_XO_CLK_ENABLE	Crystal oscillator clock enable. These enables control the CXCs. During power-up reset, the XO clock source is routed to the other clocks, which allows initialization of all internal registers. After power-up reset, all clocks are disabled. Software must configure dividers and mux's and then enable clocks as needed.

0x101F8004 NAV_CLK_RESET

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

NAV_CLK_RESET

Bits	Name	Description
31:5	RESERVED_BITS	
4	NC_RSREF_CLK_RESET	Resample reference clock domain reset
3	NC_ADC2_CLK_RESET	Diversity ADC clock domain reset
2	NC_ADC1_CLK_RESET	Primary ADC clock domain reset
1	NC_MAIN_CLK_RESET	Main clock domain reset
0	NC_XO_CLK_RESET	Crystal oscillator clock domain reset Software resets for each clock domain. It is required to write a logic 1 to a register bit to engage reset followed by a logic 0 to disengage reset. When a reset is activated, the clock will be activated to initialize all internal registers (even if the clock enable command bit is disabled).

0x101F8008 NAV_CLK_CTL

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register selects which strobe is used to update the Nav M/N:D divider settings.

0 : HOST (Host processor write to NC_FRAC _UPDATE register)

NAV_CLK_CTL

Bits	Name	Description
31:22	RESERVED_BITS	
21	NC_MEMORY_RETAIN	When this bit is set, the contents of all memories will be retained during power down. Note there is a power penalty.
20	NC_HS_DBG_CLK_SEL	Higher speed clock select for test out 0x0: OFF 0x1: RSREF
19:18	NC_LS_DBG_CLK_SEL	Lower speed clock select for test out 0x0: OFF 0x1: MAIN 0x2: ADC1 0x3: ADC2
17:16	NC_SRC_CLK_DIV	Clock divider on selected PLL source (NC_CLK_SRC_SEL), before M/N:D dividers. Potential power savings in down stream dividers if selected PLL clock is very high (e.g. > 600 MHz). 0x0: BYPASS 0x1: DIV2 0x2: DIV3 0x3: DIV4
15	NC_FRAC_UPDATE_SEL	
14	NC_FRAC8_RESET	
13	NC_FRAC8_DUAL_MODE	
12	NC_FRAC8_ENABLE	
11	NC_FRAC31_RESET	
10	NC_FRAC31_DUAL_MODE	
9	NC_FRAC31_ENABLE	
8:7	NC_RSREF_CLK_DIV	00: BYPASS 01: DIV2 10: DIV3 11: DIV4

NAV_CLK_CTL (cont.)

Bits	Name	Description
6:5	NC_ADC1_CLK_DIV	00: BYPASS 01: DIV2 10: DIV3 (not functional, do not use) 11: DIV4
4:3	NC_MAIN_CLK_DIV	00: BYPASS 01: FRAC8 10: FRAC31 11: BYPASS2
2:0	NC_CLK_SRC_SEL	000: XO 001: PLL0 010: PLL1 011: PLL2 100: EXTCLK 101: GND1 110: GND2 111: GND3

0x101F800C NAV_CLK_FRAC31_M

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

NAV_CLK_FRAC31_M

Bits	Name	Description
31	RESERVED_BITS	
30:0	NC_FRAC31_M	

0x101F8010 NAV_CLK_FRAC31_NOT_2D

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

NAV_CLK_FRAC31_NOT_2D

Bits	Name	Description
31	RESERVED_BITS	
30:0	NC_FRAC31_NOT_2D	

0x101F8014 NAV_CLK_FRAC31_NOT_N_MINUS_M

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

NAV_CLK_FRAC31_NOT_N_MINUS_M

Bits	Name	Description
31	RESERVED_BITS	
30:0	NC_FRAC31_NOT_N_MINUS_M	

0x101F8018 NAV_CLK_FRAC31_UPDATE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

NAV_CLK_FRAC31_UPDATE

Bits	Name	Description
31:1	RESERVED_BITS	
0	NC_FRAC31_UPDATE	When NC_FRAC_UPDATE_SEL = HOST, then writing a 1 then 0 pattern to this register will cause an immediate update to FRAC31 divider settings.

0x101F801C NAV_CLK_FRAC8

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

NAV_CLK_FRAC8

Bits	Name	Description
31:27	RESERVED_BITS	
26:18	NC_FRAC8_M	
17:9	NC_FRAC8_NOT_2D	
8:0	NC_FRAC8_NOT_N_MINUS_M	

0x101F8020 NAV_CLK_FRAC8_UPDATE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

NAV_CLK_FRAC8_UPDATE

Bits	Name	Description
31:1	RESERVED_BITS	
0	NC_FRAC8_UPDATE	When NC_FRAC_UPDATE_SEL = HOST, then writing a 1 then 0 pattern to this register will cause an immediate update to FRAC8 divider settings.

10.2.21 ADC Command Registers

0x101F0000 GNSS_ADC_CMD0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

GNSS_ADC_CMD0

Bits	Name	Description
31:24	ADC_REG4	
23:16	ADC_REG3	
15:8	ADC_REG2	
7:0	ADC_REG1	See GNSS ADC SWI document

0x101F0004 GNSS_ADC_CMD1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

GNSS_ADC_CMD1

Bits	Name	Description
31:24	ADC_REG8	
23:16	ADC_REG7	
15:8	ADC_REG6	
7:0	ADC_REG5	

0x101F0008 GNSS_ADC_CMD2

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

GNSS_ADC_CMD2

Bits	Name	Description
31:24	ADC_REG12	
23:16	ADC_REG11	
15:8	ADC_REG10	
7:0	ADC_REG9	

0x101F000C GNSS_ADC_CMD3

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

GNSS_ADC_CMD3

Bits	Name	Description
31:24	ADC_REG16	
23:16	ADC_REG15	
15:8	ADC_REG14	
7:0	ADC_REG13	

0x101F0010 GNSS_ADC_IDDQ

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

GNSS_ADC_IDDQ

Bits	Name	Description
31:30	RESERVED_BITS	
0	ADC_IDDQ	Quiescent current test enable. Active low control. This register bit directly drive the gnss_adc_iddq_n signal. After reset the test mode is enabled. SW must set to logic 1 to enable the ADC for normal operation.

10.2.22 Data Mover Client One

10.2.22.1 Command Registers

0x10100000 DM1_RTC_WAIT

Type: Read/Write
Clock: MEM_CLK

DM1_RTC_WAIT

Bits	Name	Description
31:0	RESERVED_BITS	RTC wait.

10.2.22.2 Nav Core Memories

0x1010C000 DM1_CMA_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

DM1_CMA_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	Correlation results memory - A block

0x1010EDFC DM1_CMA_ADDR_END

Type: Read/Write
Clock: MEM_CLK

DM1_CMA_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	

0x10110000 DM1_CMB_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

DM1_CMB_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	Correlation results memory - B block

0x101120FC DM1_CMB_ADDR_END

Type: Read/Write
Clock: MEM_CLK

DM1_CMB_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	

0x10114000 DM1_CCM_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

DM1_CCM_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	Channel command memory

0x101147FC DM1_CCM_ADDR_END

Type: Read/Write
Clock: MEM_CLK

DM1_CCM_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	

0x10140000 DM1_SM_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

DM1_SM_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	Sample memory begin address

0x10164FFC DM1_SM_ADDR_END

Type: Read/Write
Clock: MEM_CLK

DM1_SM_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	Sample memory end address

10.2.23 Data Mover Client Two

10.2.23.1 Command Registers

0x10100000 DM2_RTC_WAIT

Type: Read/Write
Clock: MEM_CLK

DM2_RTC_WAIT

Bits	Name	Description
31:0	RESERVED_BITS	RTC wait.

10.2.23.2 GNSS Tracking Memory

0x10180000 DM2_GTM_ADDR_BEGIN

Type: Read/Write
Clock: MEM_CLK

DM2_GTM_ADDR_BEGIN

Bits	Name	Description
31:0	RESERVED_BITS	GTM begin address

0x1019FFFC DM2_GTM_ADDR_END

Type: Read/Write
Clock: MEM_CLK

DM2_GTM_ADDR_END

Bits	Name	Description
31:0	RESERVED_BITS	GTM end address

10.2.24 Data Mover Client Three

Data Mover client interface 3 is a dedicated connection to the GPS Accelerator (GACC). Because the Data Mover and the host processor have access to the same registers in the GACC, the registers below are a duplicate of the GACC registers described in the System Bus section of this document. The register names and fields are repeated here.

10.2.24.1 GPS Accelerator Command Registers

0x10100A00 DM3_GACC_CLK_CTL

Type: Write/Read
Clock: GACC_CLK_
Reset State: 0x0

The writable registers occupy sequential addresses so that the Data Mover can program all of them with one block transfer. If the GPS accelerator is active, any write to these registers will not be acknowledged until it is inactive. Also, the read-only registers occupy sequential addresses so they can be moved with one block transfer.

DM3_GACC_CLK_CTL

Bits	Name	Description
31:4	RESERVED_BITS	
3	GACC_TEST_BUS_EN	Enable for test bus output. Set to logic 1 to enable. When logic 0 the bus will be forced to zero.
2	GACC_HW_LCG_EN	Enables dynamic HW clock gating scheme. When logic 1, the GACC can control the clock depending on the FSM state. This allows power savings. When logic 0, the software can control the state of the clock with the GACC_MICRO_CLK_EN register.
1	GACC_SW_CLK_EN	Controls the on/off of the logic clocks associated with core interfaces.
0	GACC_CLK_EN	When GACC_HW_LCG_EN = 0, this bit takes over the clock gating. This controls clocks related to core functions.

0x10100A04 DM3_GACC_RTC_WAIT

Type: Write/Read
Clock: GACC_CLK
Reset State: 0

DM3_GACC_RTC_WAIT

Bits	Name	Description
31:26	RESERVED_BITS	

DM3_GACC_RTC_WAIT (cont.)

Bits	Name	Description
25:24	GACC_RTC_SELECT	Determines which RTC input to use for the GACC_PAUSE, GACC_DONE, and GACC_RTC commands. 0x0: GPS 0x1: CDMA 0x2: HDR 0x3: Reserved
23:0	GACC_RTC_WAIT	GACC operation is paused until the subtraction of START_RTC from selected RTC[23:0] results in 0 for bit number 23. After the condition is met, the GACC will send an acknowledge for the write to this register. This effectively holds any bus transfer until a specified time.

0x10100A08 DM3_GACC_START_ADDR

Type: Write/Read
Clock: GACC_CLK
Reset State: 0

DM3_GACC_START_ADDR

Bits	Name	Description
31:22	RESERVED_BITS	
21:11	GACC_ENERGY_ADDR	Starting address for values within sample memory.
10:0	GACC_SAMPLE_ADDR	Starting address for values within sample memory.

0x10100A0C DM3_GACC_COUNT

Type: Write/Read
Clock: GACC_CLK
Reset State: 0

DM3_GACC_COUNT

Bits	Name	Description
31:25	GACC_ENERGY_ITER	Specifies the number of coherent integrations for each energy.
24:15	GACC_HYP_ITER	Specifies the number of time hypotheses.
14:8	GACC_SAMP_ITER	Specifies the number of accumulation for each set of samples.
7:0	GACC_FREQ_ITER	Specifies the iterations of frequency loop.

0x10100A10 DM3_GACC_INCR

Type: Write/Read
Clock: GACC_CLK
Reset State: 0

DM3_GACC_INCR

Bits	Name	Description
31:22	GACC_SAMP_INCR_SAMP	Unsigned increment of the starting sample address after all frequency integrations of a sample offset of a hypothesis. An advance sample pointer to the next sample offset.
21:11	GACC_SAMP_INCR_TIME	Signed increment of the starting sample address after all sample offset integrations of a hypothesis. An advance sample pointer to the next hypothesis.
10:0	GACC_SAMP_INCR_ENERGY	Unsigned increment of the starting sample address after all hypotheses. An advance sample pointer to the samples for the next set of coherent integrations.

0x10100A14 DM3_GACC_FREQ

Type: Write/Read
Clock: GACC_CLK
Reset State: 0

DM3_GACC_FREQ

Bits	Name	Description
31:16	GACC_FIRST_FREQ	Signed phase step for the first frequency.
15:0	GACC_FREQ_INCR	Signed phase step increment between frequencies.

0x10100A18 DM3_GACC_CONFIG

Type: Write/Read
Clock: GACC_CLK
Reset State: 0

DM3_GACC_CONFIG

Bits	Name	Description
31:24	RESERVED_BITS	
23	GACC_ENERGY_MEM_BANK	Specifies the memory bank connections. 0x0: bank 0 is connected to GPS accelerator, bank 1 is connected to Data Mover. 0x1: bank1 is connected to GPS accelerator, bank 0 is connected Data Mover.

DM3_GACC_CONFIG (cont.)

Bits	Name	Description
22	GACC_SAMPLE_MEM_BANK	Specifies the memory bank connections. 0x0: bank 0 is connected to GPS accelerator, bank 1 is connected to Data Mover. 0x1: bank1 is connected to GPS accelerator, bank 0 is connected Data Mover.
21	GACC_START	Set this bit to 1 to start the GPS accelerator.
20	GACC_COHERENT_OUT	Specifies the format result: 0x0: update energy grid 0x1: output coherent sums
19	GACC_FIRST_ENERGY	Set this bit to 1 to erase the energy sum before adding the first energy.
18:16	GACC_LAST_NFREQ	Specifies the frequency bins in the last iteration of the frequency iteration.
15:5	GACC_COHERENT_LEN	Specifies the coherent integration length.
4:2	GACC_SUM_TRUNC	Specifies the I/Q sum truncation; the maximum is 5.
1:0	GACC_ENERGY_TRUNC	Specifies the energy sum truncation before adding to sum; the maximum is 3.

0x10100A1C DM3_GACC_PEAK

Type: Read
Clock: GACC_CLK
Reset State: 0

DM3_GACC_PEAK

Bits	Name	Description
31:27	RESERVED_BITS	
26:16	GACC_MAX_INDEX	Specifies the index to the maximum energy grid value.
15:0	GACC_MAX_ENERGY	Specifies the maximum energy grid value.

0x10100A20 DM3_GACC_DONE

Type: Read
Clock: GACC_CLK
Reset State: 0

DM3_GACC_DONE

Bits	Name	Description
31:24	RESERVED_BITS	

DM3_GACC_DONE (cont.)

Bits	Name	Description
23:0	GACC_DONE_RTC	RTC value when the previous computation completed. When the state machine is in the all_done state, the current RTC is saved in this register. The RTC type is specified in the most recent GACC_PAUSE command.

0x10100A24 DM3_GACC_RTC

Type: Read
Clock: GACC_CLK
Reset State: 0

DM3_GACC_RTC

Bits	Name	Description
31:24	RESERVED_BITS	
23:0	GACC_CURRENT_RTC	

0x10100A28 DM3_GACC_TEST_BUS_OUT

Type: Read
Clock: GACC_CLK
Reset State: 0xA0

DM3_GACC_TEST_BUS_OUT

Bits	Name	Description
31:8	RESERVED_BITS	
7	GACC_AHB2HB_IDLE	Current RTC value. The RTC type is specified in the most recent GACC_PAUSE command.
6	GACC_WAIT_FOR_RTC	Set to 1 when the interface is waiting for the RTC to hit the target value
5	GACC_INTF_IDLE_STATE	Set to 1 when in INTF_IDLE_STATE of interface state machine
4	GACC_READ_PEAK_WAIT_STATE	Set to 1 when in READ_PEAK_WAIT_STATE of interface state machine
3:1	GACC_SP_CURRENT_STATE	The current state of the signal processing state machine
0	GACC_CLK_IS_ON	Indicates clock activity. Logic 1 means this clock is on.

10.2.24.2 GACC Memories

0x10128000 DM3_GACC_SAMPLE_MEM_START_ADDR

Type: Write/Read
Clock: GACC_CLK

DM3_GACC_SAMPLE_MEM_START_ADDR

Bits	Name	Description
31:0	GACC_SAMPLE_MEM	First address of sample memory. The memory is physically partitioned into 2 banks, called bank 0 and 1, each of size 1280 by 16-bits. From the software perspective, this memory appears as 640 by 32-bits with 2 consecutive locations accessed for each 32-bit transfer. The memory bank is selected by SAMPLE_MEM_BANK of the GACC_CONFIG register.

0x101289FC DM3_GACC_SAMPLE_MEM_END_ADDR

Type: Write/Read
Clock: GACC_CLK

DM3_GACC_SAMPLE_MEM_END_ADDR

Bits	Name	Description
31:0	GACC_SAMPLE_MEM	Last address of sample memory. The memory is physically partitioned into 2 banks, called bank 0 and 1, each of size 1280 by 16-bits. From the software perspective, this memory appears as 640 by 32-bits with 2 consecutive locations accessed for each 32-bit transfer. The memory bank is selected by SAMPLE_MEM_BANK of the GACC_CONFIG register.

0x1012C000 DM3_GACC_ENERGY_MEM_START_ADDR

Type: Write/Read
Clock: GACC_CLK

DM3_GACC_ENERGY_MEM_START_ADDR

Bits	Name	Description
31:0	GACC_ENERGY_MEM	First address of energy memory.The memory is physically partitioned into 2 banks, called bank 0 and 1, each of size 1280 by 16-bits. From the software perspective, this memory appears as 640 by 32-bits with 2 consecutive locations accessed for each 32-bit transfer. The memory bank is selected by ENERGY_MEM_BANK of the GACC_CONFIG register.

0x1012C9FC DM3_GACC_ENERGY_MEM_END_ADDR

Type: Write/Read
Clock: GACC_CLK

DM3_GACC_ENERGY_MEM_END_ADDR

Bits	Name	Description
31:0	GACC_ENERGY_MEM	Last address of energy memory.The memory is physically partitioned into 2 banks, called bank 0 and 1, each of size 1280 by 16-bits. From the software perspective, this memory appears as 640 by 32-bits with 2 consecutive locations accessed for each 32-bit transfer. The memory bank is selected by ENERGY_MEM_BANK of the GACC_CONFIG register.

10.3 GSS A5 Wrapper Registers (0x10000000 GSS_A5_CSR_BASE)

This section contains the Global Navigation Subsystem (GSS) A5 Wrapper registers.

10.3.1 A5 Wrapper Config/Status Registers (CSR)

NOTE All command register settings take effect immediately unless otherwise noted

All registers are initialized with power_on_reset excepted CSR_AHB_CLK_SEL and CSR_RESET registers with power_on_reset or warm_reset

0x10000000 GSS_A5_CSR_AHB_CLK_SEL

Type: Write/Read
Clock: GSS_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_AHB_CLK_SEL

Bits	Name	Description
31:1	RESERVED_BITS	
0	CSR_GSS_AHB_CLK_SEL	Select the source clock for the Fabric AHB Async Slave Port 0x0: XO clock 0x1: AHB clock

0x10000004 GSS_A5_CSR_RESET

Type: Write/Read
Clock: GSS_AHB_HCLK
Reset State: 0x1

GSS_A5_CSR_RESET

Bits	Name	Description
31:7	RESERVED_BITS	
6	CSR_SPM_RESET	Reset of SPM module
5	CSR_TIMERS_SLEEP_RESET	Reset of 2 GP timers and 1 watch dog timer at sleep clock
4	CSR_TIMERS_XO_RESET	Reset of 1 debug timer at XO clock
3	CSR_QGIC2_RESET	Reset of GIC2 module
2	CSR_AHB_RESET	Reset of AHB bus
1	CSR_AXI_RESET	Reset of AXI bus

GSS_A5_CSR_RESET (cont.)

Bits	Name	Description
0	CSR_A5_RESET	Reset of A5 CPU

0x10000008 GSS_A5_CSR_CLK_BLK_CONFIG

Type: Write/Read
Clock: GSS_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_CLK_BLK_CONFIG

Bits	Name	Description
31:18	RESERVED_BITS	
17:16	AHB_CLK_DIV_OVERRIDE	Real integer divider of source clock for AHB bus (Integer - 1). Reading only.
15:14	AXI_CLK_DIV_OVERRIDE	Real integer divider of source clock for AXI bus (Integer - 1). Reading only.
13:12	CSR_DEBUG_LS_CLK_SEL	Select the debug clock 0x0: OFF 0x1: GSS_AHB_CLK 0x2: XO_CLK 0x3: SLEEP_CLK
11:10	CSR_DEBUG_HS_CLK_SEL	Select the debug clock 0x0: OFF 0x1: A5_CLK 0x2: AXI_CLK 0x3: LOC_AHB_CLK
9:8	CSR_AHB_DIV	Integer divider of source clock for AHB bus (Integer - 1). The source clock rate divided by (CSR_A5_DIV+1) then divided by (CSR_AHB_DIV+1) has to be less than 72MHz.
7:6	CSR_AXI_DIV	Integer divider of source clock for AXI bus (Integer - 1). The source clock rate divided by (CSR_A5_DIV+1) then divided by (CSR_AXI_DIV+1) has to be less than 144MHz.
5:2	CSR_A5_DIV	Integer divider (by 1, 2, ..., 16) of source clock for A5 CPU (Integer - 1)
1:0	CSR_CLK_SRC_SEL	Select the PLL source clock between the source and test input 0x0: OFF 0x1: PLL_SCR_CLK 0x2: PLL_TEST_CLK 0x3: XO_SRC_CLK

0x1000000C GSS_A5_CSR_CLK_ENABLE

Type: Write/Read
Clock: GSS_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_CLK_ENABLE

Bits	Name	Description
31:7	RESERVED_BITS	
6	CSR_SPM_SYSTEM_CLK_EN	When set to 1, then SPM has control of the system/PLL clock on request signal. Otherwise SPM has no control. The AP should set this bit during boot up. For testing there is an option to disable SPM control.
5	CSR_SPM_FORCE_CLK_EN	When set to 1, then SPM has control of the A5, AXI, AHB clock enables. Otherwise SPM has no control. The AP should set this bit during boot up. For testing there is an option to disable SPM control.
4	CSR_SLEEP_CLK_ENABLE	Clock enable for Sleep clock
3	CSR_XO_CLK_ENABLE	Clock enable for XO clock
2	CSR_AHB_CLK_ENABLE	Clock enable for AHB bus
1	CSR_AXI_CLK_ENABLE	Clock enable for AXI bus
0	CSR_A5_CLK_ENABLE	Clock enable for A5 CPU

0x10000010 GSS_A5_CSR_A5_CONTROL

Type: Write/Read
Clock: LOC_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_A5_CONTROL

Bits	Name	Description
31:5	RESERVED_BITS	
5	CSR_A5_EVENTO	Reading only
4	CSR_A5_EVENTI	
3	CSR_L1RSTDISABLE	Disable invalidate entire data cache, instruction cache and TLB at reset
2	CSR_CP15SDISABLE	Disables write access to some system control processor registers.
1	CSR_TEINIT	Default exception handling state (0 = ARM)
0	CSR_VINITHI	Comes up in High-Vecs model

0x10000014 GSS_A5_CSR_BOOT_REMAP

Type: Write/Read
Clock: LOC_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_BOOT_REMAP

Bits	Name	Description
31:17	RESERVED_BITS	
16	CSR_BOOT_REMAP_EN	Enable of boot remapper.
15:0	CSR_BOOT_REMAP_ADDRESS	Bit [31: 16] for the boot remapper address

0x10000018 GSS_A5_CSR_POWER_UP_DOWN

Type: Write/Read
Clock: LOC_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_POWER_UP_DOWN

Bits	Name	Description
31:6	RESERVED_BITS	
5	CSR_NAV_PWRON	Power on status. Reading only
4	CSR_A5_PWRON	Power on status. Reading only
3	CSR_SPM_A5_PWRUP_EN	When set to 1, then SPM has control of the A5 power sequencer. Otherwise SPM has no control. The AP should set this bit during boot up. For testing there is an option to disable SPM control.
2	CSR_MEMORY_RETAIN	Memory retention 0x0: NO 0x1: YES
1	CSR_NAV_PWRUP	Power up the Nav Core 0x0: NO 0x1: YES
0	CSR_A5_PWRUP	Power up the A5 0x0: NO 0x1: YES

0x1000001C GSS_A5_CSR_PRIORITY_ARBITER

Type: Write/Read
Clock: LOC_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_PRIORITY_ARBITER

Bits	Name	Description
31:4	RESERVED_BITS	
3:2	CSR_DM_AXI_PRIORITY	Priority level of DM for 2 masters AXI to AXI arbitration bridge
1:0	CSR_A5_AXI_PRIORITY	Priority level of A5 CPU for 2 masters AXI to AXI arbitration bridge

0x10000020 GSS_A5_CSR_A5_IRQ

Type: Write/Read
Clock: LOC_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_A5_IRQ

Bits	Name	Description
31:22	RESERVED_BITS	
21:0	CSR_A5_IRQ	22 interrupts

0x10000024 GSS_A5_CSR_DBGROM

Type: Write/Read
Clock: LOC_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_DBGROM

Bits	Name	Description
31:21	RESERVED_BITS	
20	CSR_DBGROMADDRV	Debug ROM address valid
19:0	CSR_DBGROMADDR	Debug ROM address

0x10000028 GSS_A5_CSR_DBGSELF

Type: Write/Read
Clock: LOC_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_DBGSELF

Bits	Name	Description
31:21	RESERVED_BITS	
20	CSR_DBGSELFADDRV	Debug SELF address valid
19:0	CSR_DBGSELFADDR	Debug SELF address

0x1000002C GSS_A5_CSR_CFG_HID

Type: Write/Read
Clock: LOC_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_CFG_HID

Bits	Name	Description
31:8	RESERVED_BITS	
7:3	CSR_CFG_HPID	Bus Port ID’
2:0	CSR_CFG_HBID	Bus ID’

0x10000030 GSS_A5_CSR_QGIC_CFG

Type: Write/Read
Clock: LOC_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_QGIC_CFG

Bits	Name	Description
31:3	RESERVED_BITS	
2:0	CSR_QGIC_CFG_LM_MID	

0x10000034 GSS_A5_CSR_TEST_BUS_OUT

Type: Write/Read
Clock: LOC_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_TEST_BUS_OUT

Bits	Name	Description
31:13	RESERVED_BITS	
12	CSR_SO_DISABLE	To disable Strongly Order hardware support in axi_spliter
11:9	CSR_GSS_A5_TESTBUS_SEL	Debug test bus output selection in GSS_A5_WRAPPER 0x0: 0FF; 0x1: axi2ahb_testbus_out 0x2: timers_testbus_out 0x3: saw2_testbus_out 0x4: data_packer_tb 0x5: data_unpacker_tb 0x6: axi_spliter_tb 0x7: OFF
8:6	CSR_MAXI2AXI_TESTBUS_SEL	Debug test bus output selection for Data Mover Master AXI and A5 AXI into GSS AXI for Fabric bridge
5:3	CSR_AHB2AXI_TESTBUS_SEL	Debug test bus output selection for Data Mover Master AHB to AXI bridge
2:0	CSR_AXI2AHB_TESTBUS_SEL	Debug test bus output selection for AXI to AHB bridge for A5 access to peripheral

0x10000038 GSS_A5_CSR_SPM_STATUS

Type: Read
Clock: LOC_AHB_HCLK
Reset State: 0x0

GSS_A5_CSR_SPM_STATUS

Bits	Name	Description
31:9	RESERVED_BITS	
8	SPM_CPU_WAIT_ACK	SPM executing programmed power management sequence
7	SPM_SYS_SLEEP_STATE	Indicate CPU is in programmed sleep state
6:0	SPM_SYS_START_ADDR	Start address of SPM command array

10.4 GSS A5 SAW2 Registers (0x10001000 GSS_A5_SPM_BASE)

This section contains the Global Navigation Subsystem (GSS) A5 SAW2 registers.

The SAW2 (SPM and AVS. Wrapper2) design is an AHB slave that contains both SPM and AVS. CSRs.

0x10001000 GSS_A5_SAW2_SECURE

Type: Read/write
Clock: SYS_REF_CLK
Reset State: {3{CFGNSINIT}}

Security Treatment: Restricted

The SAW2_SECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by ahb_saw_hprotns pin. When ahb_saw_hprotns is set to ‘0’, the state of the SAW2_SECURE register is not considered; a secure transaction is always allowed. When ahb_saw_hprotns is set to ‘1’, the SAW2_SECURE register security treatment bit of that register must be ‘1’ for access to be granted. If the security treatment bit of the register is set to ’0’, the non-secure (ahb_saw_hprotns = ‘1’) transactions are denied. When access is denied, a write is ignored, and a read will return ‘0’. No error is signaled.

When reading the SAW2_SECURE register, non secure agents will always read ‘0’. Secure agents will see the actual value of the register. The reset value is controlled by CFGNSINIT input pin.

GSS_A5_SAW2_SECURE

Bits	Name	Description
31:3	RESERVED	
2	SAW_CTL	Controls security treatment for SAW2 registers: SAW2_ID, SAW2_CFG, SAW2_STS_0, SAW2_STS_1, SAW2_RST 0x1: NSEC 0x0: SEC
1	PWR_CTL	Controls security treatment for SPM registers: SAW2_SPM_CTL, SAW2_SPM_PMIC_DLY, SAW2_SPM_PMIC_DATA_0, SAW2_SPM_PMIC_DATA_1, SAW2_SPM_SLP_SEQ_ENTRY_n, SAW2_SPM_DLY 0x1: NSEC 0x0: SEC
0	VLT_CTL	Controls security treatment for the AVS. registers: SAW2_AVS_CTL, SAW2_VLVL, SAW2_AVS_HYSTERESIS 0x1: NSEC 0x0: SEC

0x10001004 GSS_A5_SAW2_ID

Type: Read
Clock: SYS_REF_CLK
Reset State: Undefined

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register reports the revision and parameter information for the SAW2 core.

GSS_A5_SAW2_ID

Bits	Name	Description
31	RESERVED_BITS31	
30:25	NUM_SPM_ENTRY	SAW2 parameter: Indicates number of SAW2_SPM_SLP_SEQ_ENTRY register implemented. Value can range from 1 - 32
24:20	NUM_PWR_CTL	SAW2 parameter: Indicates number of power control implemented. Value can range from 2 - 16
19	RESERVED_BITS19	
18	PMIC_ARB_INTF	SAW2 parameter: Indicates PMIC Arbiter Interface function is implemented
17	AVS_PRESENT	SAW2 parameter: Indicates AVS. function is implemented
16	SPM_PRESENT	SAW2 parameter: Indicates SPM function is implemented
15:12	MAJOR	Major variant
11:0	MINOR	Minor variant

0x10001008 GSS_A5_SAW2_CFG

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_CFG register is used to configure the common control between AVS. and SPM.system.

GSS_A5_SAW2_CFG

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12	FRC_REF_CLK_ON	Chicken bit to force saw_sys_ref_clk_on_req ON.
11:8	ADR_IDX	PMIC Arbiter Address Index. Drive the saw_pmic_addr_idx output port.

GSS_A5_SAW2_CFG (cont.)

Bits	Name	Description
7:6	RESERVED_BITS7_6	
5	PMIC_MODE	PMIC Handshake 0x0: 8K_PMIC (only DONE signal) 0x1: 7K_PMIC (both ACK and DONE signals)
4:0	CLK_DIV	Divider ratio for clock. This is used to generate timer tick for the timer. Timer tick is asserted every (CLK_DIV + 1) sys_ref_clk period. ..... For sys_ref_clk = 20 MHz (53ns) The timer tick range 53 ns to 1.6us. 0x0: Timer Tick every sys_ref_clk 0x1F: Timer Tick every 128 sys_ref_clk.

0x1000100C GSS_A5_SAW2_STS_0

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

GSS_A5_SAW2_STS_0

Bits	Name	Description
15	SHTDWN_REQ	This bit reflects the shutdown request from the SPM(spm_rpm_shutdown_req) to RPM.
14	SHTDWN_ACK	This bit reflects the shutdown acknowledgement from the RPM(rpm_spm_shutdown_ack) to SPM.
13	BRNGUP_REQ	This bit reflects the bringup request from the SPM(spm_rpm_bringup_req) to RPM.
12	BRNGUP_ACK	This bit reflects the bringup acknowledgement from the RPM(rpm_spm_bringup_ack) to SPM.
11:10	PMIC_STATE	State of the PMIC FSM: transitions back to IDLE) transitions back to IDLE) 0x0: IDLE (waiting for PMIC transaction from AVS. or SPM) 0x1: ACK (waiting for ACK from PMIC Arb) 0x2: DONE (waiting for DONE form PMIC Arb before) 0x3: DELAY (waiting for delay count termination before)

GSS_A5_SAW2_STS_0 (cont.)

Bits	Name	Description
9:8	RPM_STATE	State of the RPM FSM: 0x0: RUN (waiting for SPM request) 0x1: STDNACK (waiting for shutdown ACK from RPM) 0x2: WAKEUP (waiting for wakeup interrupt) 0x3: BGUPACK (waiting for bringup ACK from RPM)
7	AVS_STATE	State of the AVS. FSM: indication) 0x0: IDLE (waiting to be enabled or for next UP/DOWN) 0x1: REQ (waiting for PMIC FSM to transition to IDLE)
6:0	SPM_CMD_ADDR	Last SPM command executed.

0x10001010 GSS_A5_SAW2_STS_1

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

GSS_A5_SAW2_STS_1

Bits	Name	Description
31	RESERVED1	
30	SW_WR_PEND	This bit reflects the VLVL state of the request from the SAW2_VCTL write is pending.
29	CPU_UP	This bit reflects the VLVL state of the request from the CPU (avs_saw_up) to raise the VLVL.
28	CPU_DN	This bit reflects the VLVL state of the request from the CPU (avs_saw_down) to lower the VLVL.
27	MAX_INT	IRQ status bit, AVS. controller detected that raising the VLVL by AVS_CTL[VLVL_STEP] would result in a value greater than AVS_CTL[MAX_VLVL]. If AVS_CTL[IRQ_MAX_EN] is set, an interrupt is issued. NOTE that SW can set MAX_VLVL lower than current VLVL creating a condition where VLVL is higher than MAX_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MAX.

GSS_A5_SAW2_STS_1 (cont.)

Bits	Name	Description
26	MIN_INT	IRQ status bit, AVS. controller detected that lowering the VLVL by SAW2_AVS_CTL[VLVL_STEP] would result in a value less than SAW2_AVS_CTL[MIN_VLVL]. If SAW2_AVS_CTL[IRQ_MIN_EN] is set, an interrupt is issued. NOTE that SW can set MIN_VLVL higher than current VLVL creating a condition where VLVL is lower than MIN_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MIN.
25:16	CURR_DLY	VLVL value of the counter used to calculate the time until the next AVS. controller request for a new VLVL.

0x10001014 GSS_A5_SAW2_VCTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

Though this register is read/writable, it also causes a command pulse to the PMIC FSM. Writing this register results in a transaction to the PMIC with SAW2_VCTL being sent to the PMIC. SAW2 support both 8901 and 8058 regulator.

GSS_A5_SAW2_VCTL

Bits	Name	Description
31:16	RESERVED_BITS31_16	

0x10001018 GSS_A5_SAW2_AVS_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_CTL register is used to control the Adaptive Voltage Scaling (AVS) system.

GSS_A5_SAW2_AVS_CTL

Bits	Name	Description
31	RESERVED	

GSS_A5_SAW2_AVS_CTL (cont.)

Bits	Name	Description
30	VLVL_WIDTH	Defines the VLVL field of PMIC data. SAW2 at minimum supports 8901 and 8058 regulator. See PMIC document for details. 0x0: 5 bits VLVL (8058 regulator) 0x1: 6 bits VLVL (8901 regulator)
29:28	VLVL_STEP	Controls the step size of each request to PMIC Arbiter. SW may use values from 0 to 3. Note that the value 0 will result in no change - that is if the CPU requests UP or DOWN, the CURR_PVLVL will be sent to the PMIC Arbiter. This may be useful for debug. If an increment or decrement operation would cause the current VLVL to transition above or below the MAX_VLVL or MIN_VLVL, the current VLVL will not be changed. An interrupt will be signaled if IRQ_MAX/MIN_EN is 1
27	EN	AVS. Enable. **NOTE** Setting to 0 does not disable any pending interrupts. **NOTE** AVS. FSM and SPM FSM are mutually exclusive. Only one FSM is active at a time. SW does not have to disable AVS. before going to sleep. 0x0: Disable AVS 0x1: Enable AVS
26	SW_DONE_INT_EN	Set to 1 to turn on AVS. interrupt for when a SW initiated voltage change has completed. Set to 0 to mask it (turn it off). ASSERTION: This interrupt is asserted only after a SW write to SAW2_AVS_VLVL. Specifically, after the AVS. FSM traverses through all its states and transitions back to IDLE, the interrupt line is pulsed. The interrupt controller should be set to edge capture to receive this interrupt. CLEARING: None. This interrupt is a pulse, SW does not need to clear it (aside from requirements of the interrupt controller).
25	MAX_INT_EN	Set to 1 to turn on AVS. interrupt for MAX_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be greater than MAX_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit.
24	MIN_INT_EN	Set to 1 to turn on AVS. interrupt for MIN_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be smaller than MIN_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit
23	RESERVED_23	

GSS_A5_SAW2_AVS_CTL (cont.)

Bits	Name	Description
22:17	MAX_VLVL	Control maximum value of AVS. controller's VLVL. When current VLVL reaches this value it may not grow any larger. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level higher, an interrupt is issued. This value may be updated at anytime. Setting to a value lower than MIN_VLVL is not supported, and unpredictable results may occur.
16	RESERVED_16	
15:10	MIN_VLVL	Control the minimum value of AVS. controller's VLVL. When the current VLVL reaches this level it may not shrink any smaller. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level lower, an interrupt is issued. This value may be updated at anytime. Setting to a value higher than MAX_VLVL is not supported, and unpredictable results may occur.
9:0	AVS_DELAY	Control the time between AVS. controller's requests to change the VLVL

0x1000101C GSS_A5_SAW2_AVS_HYSTERESIS

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_HYSTERESIS register is used to delay the AVS. UP/DN signal to AVS. FSM. This is used to prevent the false PMIC step due to PDN noise.

GSS_A5_SAW2_AVS_HYSTERESIS

Bits	Name	Description
31:24	RESERVED31_24	
23:16	DN_COUNT	HYSTERESIS DN COUNT. Delays of PMIC DN step operation.
15:8	RESERVED15_8	
7:0	UP_COUNT	HYSTERESIS UP COUNT. Delays of PMIC UP step operation.

0x10001020 GSS_A5_SAW2_SPM_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_CTL register is used to control the subsystem power management system. This are parameters that controls the operation of SPM FSM.

GSS_A5_SAW2_SPM_CTL

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	SPM_START_ADR	Start address for the SPM sequence.
3	ISAR	Inhibit Start Address Reset 0x0: End of program reset the SPM_START_ADR to zero. 0x1: Inhibit End of program to reset SPM_START_ADR
2:1	WAKEUP_CONFIG	Wakeup Configuration 0x0: sys_spm_wakeup 0x1: sys_spm_wakeup or !cpu_spm_wait_req 0x2: sys_spm_wakeup or rising edge of sys_spm_dbg_nopwrdwn 0x3: sys_spm_wakeup or !cpu_spm_wait_req or rising edge of sys_spm_dbg_nopwrdwn
0	SPM_EN	SPM En.

0x10001024 GSS_A5_SAW2_SPM_PMIC_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC delay values after SPM FSM PMIC transaction. SPM wait for the programmed delay before executing the next SPM command.

GSS_A5_SAW2_SPM_PMIC_DLY

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:24	DATA_1_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
23:19	RESERVED_BITS23_19	
18:16	DATA_1_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
15:11	RESERVED_BITS15_11	

GSS_A5_SAW2_SPM_PMIC_DLY (cont.)

Bits	Name	Description
10:8	DATA_0_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
7:3	RESERVED_BITS7_3	
2:0	DATA_0_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms

0x10001028 GSS_A5_SAW2_SPM_PMIC_DATA_0

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

GSS_A5_SAW2_SPM_PMIC_DATA_0

Bits	Name	Description

0x1000102C GSS_A5_SAW2_SPM_PMIC_DATA_1

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

GSS_A5_SAW2_SPM_PMIC_DATA_1

Bits	Name	Description

0x10001030 GSS_A5_SAW2_RST

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_RST register is used to reset the SAW logic. This register clear itself. It does not reset any SAW2 CSR's. It reset AVS. and SPM FSM and control registers. This is use to clear any hang condition.

GSS_A5_SAW2_RST

Bits	Name	Description
31:1	RESERVED31_1	
0	RST	Reset AVS. and SPM FSM and control registers.

0x10001034 GSS_A5_SAW2_SPM_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the delay values for SPM Delay command. SPM wait for the programmed delay before executing the next SPM command.

GSS_A5_SAW2_SPM_DLY

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:20	DLY3	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
19:10	DLY2	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
9:0	DLY1	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms

0x10001080+4*n GSS_A5_SAW2_SPM_SLP_SEQ_ENTRY_n

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_SLP_SEQ_ENTRY_n is an array used to sequence through the steps during various power mode. The register width is defined by CLOG_PWR_CTL parameter.

GSS_A5_SAW2_SPM_SLP_SEQ_ENTRY_n

Bits	Name	Description

10.5 GSS A5 GIC2 Registers (0x10008000 GSS_A5_QGIC2_BASE)

This section contains the Global Navigation Subsystem (GSS) A5 GIC GICD registers.

The Generic Interrupt Controller 2 (GIC2) is a reusable configurable soft core. This GIC2 specification conforms to ARM's Generic Interrupt Controller architecture specification. Where differences exist, either additional features have been added or this document must change to conform to ARM's specified architecture. Where additional features were added, they will be clearly marked. The GIC2 design supports ARM's TrustZone architecture with two security zones: secure and non-secure.

The GIC2 is made of two parts: the Distributor and CPU Interfaces (up to eight). Each of these interfaces contains a CRIF slave interface. There must be at least one CPU Interface in the design.

In this manual, addresses are offsets from zero. When constants are exported, they are re-assigned to the appropriate base address.

Half-word and Byte access is supported by a subset of the registers.

Security treatment of registers in the GIC2 is divided into four types of registers. These are:

- "Common" indicates that both secure and non-secure software have full access to the register.
- "NS-int Dependent" indicates that state belonging to both secure and non-secure interrupts may be present in the register, depending on the value set in the Interrupt Security Register. Secure accesses to such a register are able to access all of the register's state, regardless of the Interrupt Security Register setting. Non-secure accesses may only access state belonging to non-secure interrupts. For non-secure accesses to state belonging to secure interrupts, writes are ignored and reads return zero.
- "Banked" indicates that the register exhibits different functionality according to whether it is accessed with a secure or non-secure request.
- "Restricted" indicates that only secure requests may access this register. If non-secure accesses are attempted, writes are ignored and reads return zero.

The type of register is specified for each register individual. Table 10-2 explains security treatment for register bits.

Table 10-2 Register security treatment

bus NS bit	SECURITY BIT	ALLOW Access
0	0	1
0	1	1
1	0	0
1	1	1

Glossary:

CPU Interface: That part of the GIC2 responsible for receiving the next interrupt from the Distributor and, if the interrupt has sufficient priority, asserting an interrupt indication to the CPU.

CPU MID: The Master ID of a CPU interface (as in AXI's AMID). The CPU MID reaching the Distributor must match the CPU Interface connected to that master.

Distributor: That part of the GIC2 responsible for detecting, disabling, prioritizing, and directing interrupts to CPU(s). The Distributor also accepts requests from and signals software interrupts to the CPU(s).

FABRIC: Flexible Advanced Buses & Reusable Interconnect Cores

NS-int: Security status of a particular interrupt ID. The value 0x0 is "secure", 0x1 is "non-secure".

NS-prot: Security status of the a bus transaction (read or write) according to the NS bit.

PPI: Private Peripheral Interrupt, interrupt from a peripheral whose interrupt line is destined to a particular CPU and can't be physically connected/directed to any other.

SGI: Software Generated Interrupt, interrupt from one CPU (or thread) to another.

SPI: Shared Peripheral Interrupt, interrupt from a peripheral whose interrupt line's CPU target is programmable to one or more CPU interface by the Distributor.

10.5.1 GIC2 Distributor

Table 10-3 GIC2 Distributor Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x0000	GICD_CTLR	RW	0x0	Banked	distributor control
0x0004	GICD_TYPER	R	Unknown	Common	distributor type
0x0008	GICD_IIDR	R	0x0000_1070	Common	distributor ID
0x0020	GICD_ANSACR	RW	0x0	Restricted	access control register
0x0024	GICD_CGCR	RW	0x0	Restricted	clock gate control register
0x0080 + 4n	GICD_ISR	RW	0x0	Restricted	distributor interrupt security
0x0100 + 4n	GICD_ISENABLER	RW	0x0	NS-int dependent	distributor interrupt set-enable
0x0180 + 4n	GICD_ICENABLER	RW	0x0	NS-int dependent	distributor interrupt clear-enable
0x0200 + 4n	GICD_ISPENDR	RW	0x0	NS-int dependent	distributor interrupt set-pending
0x0280 + 4n	GICD_ICPENDR	RW	0x0	NS-int dependent	distributor interrupt clear-pending

Table 10-3 GIC2 Distributor Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x0300 + 4n	GICD_ISACTIVER	R	0x0	NS-int dependent	distributor interrupt set-active
0x0380 + 4n	GICD_ICACTIVER	R	0x0	NS-int dependent	distributor interrupt clear-active
0x0400 + 4n	GICD_IPRIORITYR	RW	0x0	NS-int dependent	distributor interrupt priority
0x0800 + 4n	GICD_ITARGETSR	RW	0x0	NS-int dependent	distributor interrupt targets
0x0C00 + 4n	GICD_ICFGR	RW	0x5555_5555	NS-int dependent	distributor interrupt configuration
0x0D00-0x0EFF	Reserved				
0x0F00	GICD_SGIR	W	N/A	Banked	distributor software-generated interrupt
0x0F10-0xF1C	GICD_CPENDSGIR	W	N/A	Banked	SGI pend set
0x0F20-0xF2C	GICD_SPENDSGIR	W	N/A	Banked	SGI pend set
0x0FD0	GICD_PIDR0	R	0x0000_0090	Common	distributor peripheral ID
0x0FD4	GICD_PIDR1	R	0x0000_0003	Common	
0x0FD8	GICD_PIDR2	R	0x0000_002F	Common	
0x0FDC	GICD_PIDR3	R	0x0000_0000	Common	
0x0FE0	GICD_PIDR4	R	0x0000_0000	Common	
0x0FE4	GICD_PIDR5	R	0x0000_0000	Common	
0x0FE8	GICD_PIDR6	R	0x0000_0000	Common	
0x0FEC	GICD_PIDR7	R	0x0000_0000	Common	
0xFF0	GICD_CIDR0	R	0x0000_000D	Common	distributor component ID
0xFF4	GICD_CIDR1	R	0x0000_00F0	Common	
0xFF8	GICD_CIDR2	R	0x0000_0005	Common	
0xFFC	GICD_CIDR3	R	0x0000_00B1	Common	

10.5.2 GIC2 distributor registers

0x10008000 GSS_A5_GICD_CTLR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICD_CTLR register controls if the Distributor responds to external interrupt stimulus changes.

Non-secure access: Distributor provides access to the enable_ns register in bit 0.

Secure access: Distributor provides access to the enable_s register in bit 0, and the enable_ns register in bit 1.

GSS_A5_GICD_CTLR

Bits	Name	Description
31:2	RESERVED	
1	ENABLE_NS	This bit is an alias of the enable_ns bit. This bit is only usable by Secure software. 0x0: CLR 0x1: SET
0	ENABLE	This bit is the enable bit for both Secure and Non-secure software. Secure software accesses enable_s at this location. Non-secure software accesses enable_ns. 0x0: CLR 0x1: SET

0x10008004 GSS_A5_GICD_TYPER

Type: Read
Clock: CLK
Reset State: Unknown

Security Treatment: Common

The GICD_TYPER register provides information about the configuration of the GIC2.

GSS_A5_GICD_TYPER

Bits	Name	Description
31:16	RESERVED	
15:11	LSPI	Returns the number of Lockable Shared Peripheral Interrupts (LSPIs) that the GIC2 contains. GIC2 does not support lockable SPIs, always reads back 0x0.
10	TZ	TrustZone support. GIC2 supports TrustZone, always reads back 0x1.
9:8	RESERVED_BITS9_TO_8	

GSS_A5_GICD_TYPER (cont.)

Bits	Name	Description
7:5	CPU_NUM	Returns the number of CPU interfaces that the GIC provides. The GIC provides either: 0b 000 = one CPU interface 0b 001 = two CPU interfaces 0b 010 = three CPU interfaces 0b 011 = four CPU interfaces 0b 100 = five CPU interfaces 0b 101 = six CPU interfaces 0b 110 = seven CPU interfaces 0b 111 = eight CPU interfaces.
4:0	IT_LINES	Returns the number of INTIDs, to the nearest 32, that the Distributor provides. Read as: 0b 00000 = the Distributor is configured for up to 32 INTIDs 0b 00001 = the Distributor is configured for up to 64 INTIDs 0b 00010 = the Distributor is configured for up to 96 INTIDs 0b 00011 = the Distributor is configured for up to 128 INTIDs . . . 0b 11110 = the Distributor is configured for up to 992 INTIDs 0b 11111 = the Distributor is configured for up to 1020 INTIDs.

0x10008008 GSS_A5_GICD_IIDR

Type: Read
Clock: CLK
Reset State: 0x00001070

Security Treatment: Common

The GICD_IIDR register provides the implementor of the Distributor and the revision of the Distributor.

GSS_A5_GICD_IIDR

Bits	Name	Description
31:24	RESERVED	
15:12	REVISION	Returns the revision number of the Distributor, 0x1
11:0	IMPLEMENTOR	Returns JEP106 ID number, 0b 01110000

0x10008020 GSS_A5_GICD_ANSACR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Restricted

The auxiliary non-secure access control register (GICD_ANSACR) is used to control non-secure access to GICD_CGCR.

GSS_A5_GICD_ANSACR

Bits	Name	Description
31:1	RESERVED	
0	GICD_CGCR	0x0: SEC (Dis-allows non-secure access.) 0x1: NS (Allows non-secure access.)

0x10008024 GSS_A5_GICD_CGCR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Restricted

The clock gate control register (GICD_CGCR) is used to control localized clock gating over-ride logic. Setting bits in GICD_CGCR disables the corresponding local clock gating logic. The local clock gating logic normally turns off a local (small subset) clock tree automatically if there is no need for the clock. If any error is found in the gating logic, these bits can be used to over-ride it.

GSS_A5_GICD_CGCR

Bits	Name	Description
31:17	RESERVED_31_TO_17	
16	TOP	Controls the top level clock gate (which gates entire GIC2). 0x1: DISABLE 0x0: ENABLE
15:4	RESERVED_15_TO_4	
3	DI_SGI_STATE	Controls the clock gate for Distributor interrupt state data base registers for SGI interrupts. 0x1: DISABLE 0x0: ENABLE
2	DI_PPI_SPI_STATE	Controls the clock gate for Distributor interrupt state data base registers for PPI and SPI interrupts. 0x1: DISABLE 0x0: ENABLE

GSS_A5_GICD_CGCR (cont.)

Bits	Name	Description
1	DI_DEMET	Controls the clock gate for Distributor interrupt input demet registers. 0x1: DISABLE 0x0: ENABLE
0	DI_RD	Controls the clock gate for Distributor CRIF Read Data. 0x1: DISABLE 0x0: ENABLE

0x10008080+4*n GSS_A5_GICD_ISRn, n=[0..8]

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Restricted

Each bit in an GICD_ISR register controls the security state of an interrupt, to be either secure or non-secure. You can only access these registers with secure read or secure write accesses.

NOTE The GICD_ISR register at address offset 0x0080 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

GSS_A5_GICD_ISRn

Bits	Name	Description
31:0	INT_NS	0x0: SEC (Assigns INTID N to the Secure state.) 0x1: NS (Assigns INTID N to the Non-secure state.)

0x10008100+4*n GSS_A5_GICD_ISENABLERn, n=[0..8]

Type: Write (command - readable)
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in an GICD_ISENABLER register controls the enabling of an interrupt.

Reading this register returns the currently enabled interrupts subject to NS-int dependent access rules.

NOTE The GICD_ISENABLER register at address offset 0x0100 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

GSS_A5_GICD_ISENABLERn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ICENABLER register.) 0x1: SET (Enables INTID N.)

0x10008180+ 4*n GSS_A5_GICD_ICENABLERn, n=[0..8]

Type: Write (command - readable)
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in an GICD_ICENABLER register controls the disabling of an interrupt.

Reading this register returns the currently enabled interrupts subject to NS-int dependent access rules.

NOTE The GICD_ICENABLER register at address offset 0x0180 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

GSS_A5_GICD_ICENABLERn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ISENABLER register.) 0x1: CLR (Enables INTID N.)

0x10008200+ 4*n GSS_A5_GICD_ISPENDRn, n=[0..8]

Type: Write (command - readable)
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in an GICD_ISPENDR register controls the enabling of an interrupt.

Reading this register returns the currently pending interrupts subject to NS-int dependent access rules.

NOTE The GICD_ISPENDR register at address offset 0x0200 is repeated once per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI interrupts. SGI interrupt bits are read-only, however the distributor updates these using the GICD_SGIR register. The remaining registers control the SPI interrupts.

GSS_A5_GICD_ISPENDRn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ICPENDR register.) 0x1: SET (Sets INTID N to the Pending state.)

0x10008280+ 4*n GSS_A5_GICD_ICPENDRn, n=[0..8]

Type: Write (command - readable)
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in an GICD_ICPENDR register controls the disabling of an interrupt.

Reading this register returns the currently pending interrupts subject to NS-int dependent access rules.

NOTE The GICD_ICPENDR register at address offset 0x0280 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI interrupts. SGI interrupt bits are read-only, however the distributor updates these using the GICD_SGIR register. The remaining registers control the SPI interrupts.

GSS_A5_GICD_ICPENDRn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ISPENDR register.) 0x1: CLR (Clears INTID N. from the pending state.)

0x10008300+ 4*n GSS_A5_GICD_ISACTIVERn, n=[0..8]

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in the GICD_ISACTIVER register provides the active status of an interrupt. Writing a 1 to any of these bits will transition the corresponding interrupt to the Active (or Active and Pending) state

NOTE The GICD_ISACTIVER register at address offset 0x0300 is repeated once per CPU Interface. It is only accessible from the designated CPU and provides information for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

GSS_A5_GICD_ISACTIVERn

Bits	Name	Description
31:0	INT	0x0: DO NOTHING 0x1: SET

0x10008380+4*n GSS_A5_GICD_ICACTIVERn, n=[0..8]

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in the GICD_ICACTIVER register provides the active status of an interrupt. Writing a 1 to any of these bits will transition the corresponding interrupt out of the Active (or Active and Pending) state

NOTE The GICD_ICACTIVER register at address offset 0x0300 is repeated once per CPU Interface. It is only accessible from the designated CPU and provides information for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

GSS_A5_GICD_ICACTIVERn

Bits	Name	Description
31:0	INT	0x1: CLR 0x0: DO NOTHING

0x10008400+4*n GSS_A5_GICD_IPRIORITYRn, n=[0..71]

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each field in the GICD_IPRIORITYR registers controls the priority level of an interrupt.

NOTE The GICD_IPRIORITYR registers at address offsets 0x0400 to 0x41C are repeated once per CPU Interface. These are only accessible from the designated CPU and control the priority levels for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupt priority levels.

NOTE This register is byte addressable.

The GICD_IPRIORITYR register behaves differently depending on the security setting of interrupt associated with the address written (NS-int) and the security of the bus transaction (NS-prot).

GSS_A5_GICD_IPRIORITYRn

Bits	Name	Description
31:27	INT3	
26:24	RESERVED_1	
23:19	INT2	
18:16	RESERVED_2	
15:11	INT1	
10:8	RESERVED_3	
7:3	INT0	All bits cleared (0x0) is the highest priority. All bits set (5'b11111) is the lowest priority. For non-secure write access, the MSB is always set (1). For non-secure read access, the MSB is always clear (0). Non-secure entities can't use the highest priorities without secure software setting such a priority. The highest priorities are typically reserved for secure software. On the other hand, secure software can, if needed, write and read the MSB. Secure entities have access to all priorities. Secure interrupts can use priority numbers 5'b10000-5'b11111 (the lower half of the priority spectrum) if needed. Due to strict "less than" comparisons used in the CPU interface, setting an interrupt's priority to 5'b11111 effectively disables that interrupt. The number of priorities actually supported is 32. Software can determine this number by writing 0xFF and reading back the result.
2:0	RESERVED_4	

0x10008800+4*n GSS_A5_GICD_ITARGETSRn, n=[0..71]

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each field in the GICD_ITARGETSR registers controls the destination CPU(s) of an interrupt.

NOTE The GICD_ITARGETSR registers at address offsets 0x0800 to 0x81C are not actually implemented. These are place holders PPI and SGI interrupts. PPI interrupts, being private, only have one destination CPU. SGI interrupts are generated by the

GIC2_DI_SOFT_INT register only. The remaining registers control the SPI interrupt destinations.

NOTE This register is byte addressable.

GSS_A5_GICD_ITARGETSRn

Bits	Name	Description
31:24	INT3	
23:16	INT2	
15:8	INT1	
7:0	INT0	Each bit represents one of 8 CPUs. Bit 0 represents the zeroth CPU, bit 7 represents the seventh CPU. Setting this field to 0 will disable the interrupt as no CPU will see it set. For INTIDs < 32 (the SGI and PPI), reads return the bit corresponding to the CPU performing the read (i.e., CPU 0 reads back 0x01010101). Writes are ignored. The number of CPUs actually supported is determined by NUM_CPU generic. Software can determine this number by writing 0xFF and reading back the result.

0x10008C00+4*n GSS_A5_GICD_ICFGRn, n=[0..17]

Type: Read/write
Clock: CLK
Reset State: 0x55555555

Security Treatment: NS-int dependent

Each field in the GICD_ICFGR registers allows:

- control of type of an SPI:
- level-sensitive
- edge-sensitive
- reading the type of PPIs and SGIs

NOTE The GICD_ICFGR registers at address offsets 0x0C00 to 0xC04 are repeated once per CPU Interface. These are only accessible from the designated CPU and allow read access for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

NOTE PPI(0) is the maintenance interrupt and must be configured as level type.

NOTE This register is not byte addressable, interrupts should be disabled before configuring their type.

NOTE Reset state for GICD_ICFGR0 is 0xaaaaaaaa.

GSS_A5_GICD_ICFGRn

Bits	Name	Description
31:30	INT15	
29:28	INT14	
27:26	INT13	
25:24	INT12	
23:22	INT11	
21:20	INT10	
19:18	INT9	
17:16	INT8	
15:14	INT7	
13:12	INT6	
11:10	INT5	
9:8	INT4	
7:6	INT3	
5:4	INT2	
3:2	INT1	
1:0	INT0	These bits behave differently for each of the three interrupt types as follows: ' For SGI, read back as 0b10 - SGI interrupts are edge-sensitive and use the N-N model. ' For PPI/SPI, read/writable as 0b01 or 0b11 - PPI/SPI interrupts can be edge or level sensitive and use the 1-N model. 0x0: LVL N to N 0x1: LVL 1 to N 0x2: EDGE N to N 0x3: EDGE 1 to N

0x10008F00 GSS_A5_GICD_SGIR

Type: Write (command)
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICD_SGIR register provides the method by which software may cause interrupts to become pending for designated target CPU(s). The GIC2 maintains an internal database of all outstanding software interrupt requests pended to each CPU Interface and rotates through them in Round Robin fashion. Signaling the same interrupt a second time before it is serviced will result in only one interrupt from the source CPU to the target CPU(s).

Table 10-4 Security status

Security status of the write event to the GICD_SGIR register (the state of the NS bit)	SATT Value	Interrupt's security status as set by GICD_ISR	Requested Interrupt set as pending on the target CPU
Secure	0	Secure	YES
Secure	0	Non-secure	NO
Secure	1	Secure	NO
Secure	1	Non-secure	YES
Non-secure	X	Secure	NO
Non-secure	X	Non-secure	YES

GSS_A5_GICD_SGIR

Bits	Name	Description
31:26	RESERVED_BITS31_TO_26	
25:24	T_FILTER	Target Filter 0x0: LIST (Use the T_LIST as is) 0x1: OTHERS (Send to all CPUs accept the CPU MID making the request, ignoring T_LIST) 0x2: MID (Send to only the CPU MID making the request, ignoring T_LIST) 0x3: NA (Reserved)
23:16	T_LIST	Target List. Each bit set represents a CPU target for the INT_ID, subject to the T_FILTER field. 0x1: CPU0 0x2: CPU1 0x4: CPU2 0x8: CPU3 0x10: CPU4 0x20: CPU5 0x40: CPU6 0x80: CPU7
15	SATT	Security ATTribute. This bit is only programmable by secure Software. See 0x0: SECURE (Secure interrupt is issued) 0x1: NONSECURE (Non-secure interrupt is issued.)
14:4	RESERVED_BITS14_TO_4	

GSS_A5_GICD_SGIR (cont.)

Bits	Name	Description
3:0	INT_ID	The INT ID number (0-15) of the SGI to be set as pending. See the SGI pending truth table for security status Table 10-4 (SATT vs. NS-prot) for information on the conditions that allow an SGI to be set pending.

0x10008F10+4*n GSS_A5_GICD_CPENDSGIRn, n=[0..3]

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

Each field in the GICD_CPENDSGIR register, when written as 1, clears the corresponding pending bit of the source CPU for the corresponding SGI.

NOTE If the SGI is marked secure, only a secure access can access that SGI's pending bits.

NOTE This register is byte addressable.

GSS_A5_GICD_CPENDSGIRn

Bits	Name	Description
31:24	SGI3	
23:16	SGI2	
15:8	SGI1	
7:0	SGI0	Each bit represents one of 8 CPUs. Bit 0 represents the zeroth CPU, bit 7 represents the seventh CPU. Writing a 1 to any bit clears the pending status bit from the CPU to the SGI.

0x10008F20+4*n GSS_A5_GICD_SPENDSGIRn, n=[0..3]

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

Each field in the GICD_SPENDSGIR register, when written as 1, sets the corresponding pending bit of the source CPU for the corresponding SGI.

NOTE If the SGI is marked secure, only a secure access can access that SGI's pending bits.

NOTE This register is byte addressable.

GSS_A5_GICD_SPENDSGIRn

Bits	Name	Description
31:24	SGI3	
23:16	SGI2	
15:8	SGI1	
7:0	SGI0	Each bit represents one of 8 CPUs. Bit 0 represents the zeroth CPU, bit 7 represents the seventh CPU. Writing a 1 to any bit sets the pending status bit from the CPU to the SGI.

0x10008FD0 GSS_A5_GICD_PIDR0

Type: Read
Clock: CLK
Reset State: 0x00000090

Security Treatment: Common

The GICD_PIDR0 provides access to GIC2 peripheral identification.

GSS_A5_GICD_PIDR0

Bits	Name	Description
31:8	RESERVED	
7:0	PART_NUM	Returns lower byte of the GIC2 part number 0xB390, 0x90

0x10008FD4 GSS_A5_GICD_PIDR1

Type: Read
Clock: CLK
Reset State: 0x00000003

Security Treatment: Common

The GICD_PIDR1 provides access to GIC2 peripheral identification.

GSS_A5_GICD_PIDR1

Bits	Name	Description
31:8	RESERVED	
7:4	DESIGNER	Returns EDEC JEP code bits 3:0, 0x0.
3:0	PART_NUM	Returns upper nibble of the GIC2 part number 0x390, 0x3

0x10008FD8 GSS_A5_GICD_PIDR2

Type: Read
Clock: CLK
Reset State: 0x0000002F

Security Treatment: Common

The GICD_PIDR2 provides access to GIC2 peripheral identification.

GSS_A5_GICD_PIDR2

Bits	Name	Description
31:8	RESERVED	
7:4	ARCH_VERSION	Returns the GIC2's architecture revision number, 0x2
3	USES_JEP_CODE	Reads 0x1.
2:0	DESIGNER	Returns JEDEC JEP code bits 6:4, 0x7.

0x10008FDC GSS_A5_GICD_PIDR3

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR3 provides access to GIC2 peripheral identification.

GSS_A5_GICD_PIDR3

Bits	Name	Description
31:0	RESERVED_1	
7:4	REVISION	Returns 0x0.
3:0	RESERVED_2	ARM defined field.

0x10008FE0 GSS_A5_GICD_PIDR4

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR4 provides access to GIC2 peripheral identification.

GSS_A5_GICD_PIDR4

Bits	Name	Description
31:8	RESERVED_1	
7:4	RESERVED_2	ARM defined field.
3:0	DESIGNER	JEDEC JEP code bits 10:7, 0x0

0x10008FE4 GSS_A5_GICD_PIDR5

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR5 provides access to GIC2 peripheral identification.

GSS_A5_GICD_PIDR5

Bits	Name	Description
31:0	RESERVED	

0x10008FE8 GSS_A5_GICD_PIDR6

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR6 provides access to GIC2 peripheral identification.

GSS_A5_GICD_PIDR6

Bits	Name	Description
31:0	RESERVED	

0x10008FEC GSS_A5_GICD_PIDR7

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR7 provides access to GIC2 peripheral identification.

GSS_A5_GICD_PIDR7

Bits	Name	Description
31:0	RESERVED	

0x10008FF0 GSS_A5_GICD_CIDR0

Type: Read
Clock: CLK
Reset State: 0x0000000D

Security Treatment: Common

The GICD_CIDR0 provides access to GIC2 component identification.

GSS_A5_GICD_CIDR0

Bits	Name	Description
31:8	RESERVED	
7:0	COMP_ID_0	Reads back as 0x0D.

0x10008FF4 GSS_A5_GICD_CIDR1

Type: Read
Clock: CLK
Reset State: 0x000000F0

Security Treatment: Common

The GICD_CIDR1 provides access to GIC2 component identification.

GSS_A5_GICD_CIDR1

Bits	Name	Description
31:8	RESERVED	
7:0	COMP_ID_1	Reads back as 0xF0.

0x10008FF8 GSS_A5_GICD_CIDR2

Type: Read
Clock: CLK
Reset State: 0x00000005

Security Treatment: Common

The GICD_CIDR2 provides access to GIC2 component identification.

GSS_A5_GICD_CIDR2

Bits	Name	Description
31:8	RESERVED	
7:0	COMP_ID_2	Reads back as 0x05.

0x10008FFC GSS_A5_GICD_CIDR3

Type: Read
Clock: CLK
Reset State: 0x000000B1

Security Treatment: Common

The GICD_CIDR3 provides access to GIC2 component identification.

GSS_A5_GICD_CIDR3

Bits	Name	Description
31:8	RESERVED	
7:0	COMP_ID_3	Reads back as 0xB1.

10.6 GSS A5 GIC2 GICH Registers (0x10008000 GSS_A5_QGIC2_BASE)

This section contains the Global Navigation Subsystem (GSS) A5 GIC2 GICH registers.

The Generic Interrupt Controller 2 (GIC2) is a reusable configurable soft core. This GIC2 specification conforms to ARM's Generic Interrupt Controller architecture specification. Where differences exist, either additional features have been added or this document must change to conform to ARM's specified architecture. Where additional features were added, they will be clearly marked. The GIC2 design supports ARM's TrustZone architecture with two security zones: secure and non-secure.

The GIC2 is made of two parts: the Distributor and CPU Interfaces (up to eight). Each of these interfaces contains a CRIF slave interface . There must be at least one CPU Interface in the design.

In this manual, addresses are offsets from zero. When constants are exported, they are re-assigned to the appropriate base address.

Half-word and Byte access is supported by a subset of the registers.

Security treatment of registers in the GIC2 is divided into four types of registers. These are:

- "Common" indicates that both secure and non-secure software have full access to the register.
- "NS-int Dependent" indicates that state belonging to both secure and non-secure interrupts may be present in the register, depending on the value set in the Interrupt Security Register. Secure accesses to such a register are able to access all of the register's state, regardless of the Interrupt Security Register setting. Non-secure accesses may only access state belonging to non-secure interrupts. For non-secure accesses to state belonging to secure interrupts, writes are ignored and reads return zero.
- "Banked" indicates that the register exhibits different functionality according to whether it is accessed with a secure or non-secure request.
- "Restricted" indicates that only secure requests may access this register. If non-secure accesses are attempted, writes are ignored and reads return zero.

The type of register is specified for each register individual. Table 10-5 explains security treatment for register bits.

Table 10-5 Register security treatment

bus NS bit	SECURITY BIT	ALLOW Access
0	0	1
0	1	1
1	0	0
1	1	1

Glossary:

CPU Interface: That part of the GIC2 responsible for receiving the next interrupt from the Distributor and, if the interrupt has sufficient priority, asserting an interrupt indication to the CPU.

CPU MID: The Master ID of a CPU interface (as in AXI's AMID). The CPU MID reaching the Distributor must match the CPU Interface connected to that master.

Distributor: That part of the GIC2 responsible for detecting, disabling, prioritizing, and directing interrupts to CPU(s). The Distributor also accepts requests from and signals software interrupts to the CPU(s).

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NS-int: Security status of a particular interrupt ID. The value 0x0 is "secure", 0x1 is "non-secure".

NS-prot: Security status of the a bus transaction (read or write) according to the NS bit.

PPI: Private Peripheral Interrupt, interrupt from a peripheral whose interrupt line is destined to a particular CPU and can't be physically connected/directed to any other.

SGI: Software Generated Interrupt, interrupt from one CPU (or thread) to another.

SPI: Shared Peripheral Interrupt, interrupt from a peripheral whose interrupt line's CPU target is programmable to one or more CPU interface by the Distributor.

10.6.1 GIC2 Hypervisor Interface

Table 10-6 GIC2 Hypervisor Interface Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x1000	GICH_HCR	RW	0x0000_0000	Common	general Hypervisor control
0x1004	GICH_VTR	R	0x9000_0003	Common	hypervisor implementation - type register
0x1008	GICH_VMCR	R/W	0x004C_0000	Common	virtual machine control register
0x1010	GICH_MISR	R	0x0000_0000	Common	Maintenance interrupt syndrome
0x1020	GICH_EISR	R	0x0000_0000	Common	List registers' EOI status
0x1030	GICH_ELRSR	R	0x0000_000F	Common	List registers' empty status
0x10F0	GICH_APR	R/W	0x0000_0000	Common	Active Priority in hypervisor
0x1100 + 4n	GICH_LRn	R/W	0x0000_0000	Common	List registers

10.6.1.1 GIC2 Hypervisor interface registers

0x10009000 GSS_A5_GICH_HCR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICH_HCR configures the GIC2 Hypervisor interface.

GSS_A5_GICH_HCR

Bits	Name	Description
31:27	EOICOUNT	Counts the number of EOIs which have been received without a corresponding entry being found among the list registers. Incremented automatically by the CPU Interface when such an EOI is received. EOIs which do not clear a bit in the Active Priorities register do not cause an increment. The maintenance interrupt is asserted whenever this field is non-zero and the SKIDIE bit is set (see below).
26:8	RESERVED	
7	VDG1IE	If this bit is set, the maintenance interrupt will be asserted whenever the GICV_CTLR[EnableG1] is cleared. 0x0: CLR 0x1: SET
6	VEG1IE	If this bit is set, the maintenance interrupt will be asserted whenever the GICV_CTLR[EnableG1] is set. 0x0: CLR 0x1: SET
5	VDG0IE	If this bit is set, the maintenance interrupt will be asserted whenever the GICV_CTLR[EnalbeG0] is cleared. 0x0: CLR 0x1: SET
4	VEG0IE	If this bit is set, the maintenance interrupt will be asserted whenever the GICV_CTLR[EnableG0] is set. 0x0: CLR 0x1: SET
3	NPIE	No Pending Interrupt Maintenance Interrupt Enable. If this bit is set, the maintenance interrupt will be asserted whenever no list registers contain an interrupt in PENDING state. 0x0: CLR 0x1: SET

GSS_A5_GICH_HCR (cont.)

Bits	Name	Description
2	SKIDIE	SKID Maintenance Interrupt Enable. If this bit is set, the maintenance interrupt will be asserted whenever GICH_HCR[EOICount] is non-zero. 0x0: CLR 0x1: SET
1	UIE	Underflow Maintenance Interrupt Enable. If this bit is set, the maintenance interrupt will be asserted whenever zero or one of the list entries are marked as valid. 0x0: CLR 0x1: SET
0	EN	Enable or Disable maintenance and by proxy Virtual CPU interface Interrupts 0x0: CLR 0x1: SET

0x10009004 GSS_A5_GICH_VTR

Type: Read
Clock: CLK
Reset State: 0x90000003

Security Treatment: Common

The GICH_VTR provides information about the configuration of the Hypervisor Interface (virtual generic interrupt controller type register).

GSS_A5_GICH_VTR

Bits	Name	Description
31:29	PRIBITS	Indicates the number of priority bits implemented, minus one. For this version of the specification the only acceptable value is 100, indicating 5 bits of priority (32 levels)
28:26	PREBITS	Indicates the number of preemption bits implemented, minus one. For this version of the specification the only acceptable value is 100, indicating 5 bits of preemption (32 levels)
25:6	RESERVED	
5:0	LISTREGS	Indicates the number of implemented List Registers, minus one. GIC2 has 4 list registers. This is set to 0x3

0x10009008 GSS_A5_GICH_VMCR

Type: Read/write
Clock: CLK
Reset State: 0x004C0000

Security Treatment: Common

The GICH_VMCR contains read/write aliases of all the Virtual Machine accessible state (aliases from the GICV_* registers). This alias allows the Hypervisor to easily save and restore this state with a single read or write, and without needing to map in the Virtual Machine registers.

NOTE Various bits of this register include the terms group 0 or group 1in their names. This is purely for compatibility with the physical generic interrupt controller interface and does not pertain to actual TrustZone security.

GSS_A5_GICH_VMCR

Bits	Name	Description
31:27	VMPMR	Alias of the GICV_PMR bits 7:3 in GICV
26:24	RESERVED_1	
23:21	VMG0BP	Alias of the group0 GICV_BPR bit in GICV
20:18	VMG1BP	Alias of the group1 GICV_ABPR bit in GICV
17:10	RESERVED_2	
9	VEM	Alias of the GICV_CTLR[EOIMode] bit in GICV
8:5	RESERVED	
4	VMGBPR	Alias of the GICV_CTLR[GBPR] bit in GICV
3	VMFIQEN	Alias of the GICV_CTLR[FIQen] bit in GICV.
2	VMACKCTL	Alias of the GICV_CTLR[ActCtl] bit in GICV.
1	VMENABLE_G1	Alias of the GICV_CTLR[ENABLE_G1] bit in GICV.
0	VMENABLE_G0	Alias of the GICV_CTLR[ENABLE_G0] bit in GICV.

0x10009010 GSS_A5_GICH_MISR

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICH_MISR is the Maintenance interrupt syndrome register in the Hypervisor Interface. This register indicates which Maintenance Interrupts are currently asserted. This takes into account the individual Maintenance Interrupt Enable bits in GICH_HCR. However, the global enable in

GICH_HCR (EN) is not factored in to these bits. Therefore the maintenance interrupt is asserted if and only if at least one bit is set in this register and the EN bit in GICH_HCR is set.

GSS_A5_GICH_MISR

Bits	Name	Description
31:8	RESERVED	
7	VDNSI	
6	VENSI	
5	VDSI	
4	VESI	
3	NPI	
2	SKIDI	
1	UI	
0	EI	

0x10009020 GSS_A5_GICH_EISR

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICH_EISR provides EOI interrupt status in the Hypervisor Interface - which Software interrupts in the LRn registers that have EI set and are currently in the Invalid state.

GSS_A5_GICH_EISR

Bits	Name	Description
25:5	RESERVED	
3:0	LR	0x0: NOT_EOI 0x1: EOI

0x10009030 GSS_A5_GICH_ELRSR

Type: Read
Clock: CLK
Reset State: 0x0000000F

Security Treatment: Common

The GICH_ELRSR provides Empty List Register Status in the Hypervisor Interface.

GSS_A5_GICH_ELRSR

Bits	Name	Description
31:5	RESERVED	
3:0	LR	0x0: NOT EMPTY 0x1: EMPTY

0x100090F0 GSS_A5_GICH_APR

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICH_APR provides information about the priorities currently active in the Hypervisor Interface.

GSS_A5_GICH_APR

Bits	Name	Description
31:0	PRI	0x0: INACTIVE 0x1: ACTIVE

0x10009100+4*n GSS_A5_GICH_LRn, n=[0..3]

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICH_LRn provides access to each of the list registers in the Hypervisor Interface.

GSS_A5_GICH_LRn

Bits	Name	Description
31	HW	Indicates that this is a Hardware interrupt. When this bit is set, bits 19:10 contain the Physical interrupt number, and when this interrupt is subject to an EOI request, a Deactivate Interrupt request will be sent to the Interrupt Distributor.

GSS_A5_GICH_LRn (cont.)

Bits	Name	Description
30	GRP	Indicates that this interrupt should be treated as Group1. This means that the interrupt will present as an IRQ if GICV_CTLR[EnableG1] bit is set. If the GRP bit is clear, the interrupt is put into Group0 and will present as either IRQ or FIQ depending on the setting of the GICV_CTLR[FIQen] but only if GICV_CTLR[EnableG0] bit is also set. This bit is also used with GICV_CTLR[CBPR] to determine which Binary Point register is used in GICV for preemption calculations.
29:28	STATE	**NOTE** For hardware interrupts, the PENDING+ACTIVE state is held in the physical Distributor rather than the VCPUIF. The PENDING+ACTIVE state (11) should only be used for software originated interrupts (Virtual Devices) or SGIs. 0x0: IDL (INVALID) 0x1: PNA (PENDING, NOT ACTIVE) 0x2: A (ACTIVE) 0x3: PA (PENDING and ACTIVE)
27:23	PRI	Indicates the priority of this interrupt. This is converted to a traditional 8-bit generic interrupt controller priority value by appending three zero bits.
22:20	RESERVED	
19:10	PHY_ID	The physical ID of the interrupt (which SGI/PPI/SPI it is). When the HW bit is set this field indicates the physical interrupt ID, which is forwarded to the Distributor when this interrupt is subject to an EOI request. See below for details when the HW bit is clear. If the Physical ID is between 16 and 31 inclusive (PPI space), the Deactivation will apply to the PPI associated with the same physical CPU as the VCPUIF making the request. If the Physical ID is between 0 and 15 inclusive (SGI space), the Deactivation will still apply to SGI associated with the same physical CPU as the VCPUIF making the request but it is expected that the HW bit and Physical ID will NOT be used for SGIs.
9:0	VIRTL_ID	Indicates the Virtual ID. This ID is returned to the Guest OS when this interrupt is acknowledged via the GICV_IAR (Interrupt Acknowledge register).

0x10009120 GSS_A5_GICH_SW_LR

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

This register is not a real physical register or address in the design. It is placed here in the Software Manual to describe the alternate meanings for bits 19:10 in the LRn registers. Adding it here allows SW to pick up defines for these alternate meanings and use them in LRn accesses.

The HW uses these alternate definitions when bit 31 (HW) is set to 0, indicating a (a pure virtual interrupt) written directly to this Hypervisor interface or an interrupt generated due to an SGI that originated in the Distributor. Bits 31:20 and 9:0 retain the normal GICH_LRn meanings.

GSS_A5_GICH_SW_LR

Bits	Name	Description
19	EI	Indicates that this interrupt should trigger an EOI Interrupt. When this bit is set, a maintenance interrupt will be asserted whenever this interrupt becomes INVALID.
18:13	RESERVED	
12:10	CPUID	If this interrupt is an SGI, indicates the requesting CPU ID. This will appear in the relevant field of the VM Interrupt Acknowledge register. If the interrupt is not an SGI, software must set this field to 0.

10.7 GSS A5 GIC2 GICC Registers (0x10008000 GSS_A5_QGIC2_BASE)

This section contains the Global Navigation Subsystem (GSS) A5 GIC2 GICC registers.

The Generic Interrupt Controller 2 (GIC2) is a reusable configurable soft core. This GIC2 specification conforms to ARM's Generic Interrupt Controller architecture specification. Where differences exist, either additional features have been added or this document must change to conform to ARM's specified architecture. Where additional features were added, they will be clearly marked. The GIC2 design supports ARM's TrustZone architecture with two security zones: secure and non-secure.

The GIC2 is made of two parts: the Distributor and CPU Interfaces (up to eight). Each of these interfaces contains a CRIF slave interface. There must be at least one CPU Interface in the design.

In this manual, addresses are offsets from zero. When constants are exported, they are re-assigned to the appropriate base address.

Half-word and Byte access is supported by a subset of the registers.

Security treatment of registers in the GIC2 is divided into four types of registers. These are:

- "Common" indicates that both secure and non-secure software have full access to the register.
- "NS-int Dependent" indicates that state belonging to both secure and non-secure interrupts may be present in the register, depending on the value set in the Interrupt Security Register. Secure accesses to such a register are able to access all of the register's state, regardless of the Interrupt Security Register setting. Non-secure accesses may only access state belonging to non-secure interrupts. For non-secure accesses to state belonging to secure interrupts, writes are ignored and reads return zero.
- "Banked" indicates that the register exhibits different functionality according to whether it is accessed with a secure or non-secure request.
- "Restricted" indicates that only secure requests may access this register. If non-secure accesses are attempted, writes are ignored and reads return zero.

The type of register is specified for each register individual. Table 10-7 explains security treatment for register bits.

Table 10-7 Register security treatment

bus NS bit	SECURITY BIT	ALLOW Access
0	0	1
0	1	1
1	0	0
1	1	1

Glossary:

CPU Interface: That part of the GIC2 responsible for receiving the next interrupt from the Distributor and, if the interrupt has sufficient priority, asserting an interrupt indication to the CPU.

CPU MID: The Master ID of a CPU interface (as in AXI's AMID). The CPU MID reaching the Distributor must match the CPU Interface connected to that master.

Distributor: That part of the GIC2 responsible for detecting, disabling, prioritizing, and directing interrupts to CPU(s). The Distributor also accepts requests from and signals software interrupts to the CPU(s).

FABRIC: Flexible Advanced Buses & Reusable Interconnect Cores

NS-int: Security status of a particular interrupt ID. The value 0x0 is "secure", 0x1 is "non-secure".

NS-prot: Security status of the a bus transaction (read or write) according to the NS bit.

PPI: Private Peripheral Interrupt, interrupt from a peripheral whose interrupt line is destined to a particular CPU and can't be physically connected/directed to any other.

SGI: Software Generated Interrupt, interrupt from one CPU (or thread) to another.

SPI: Shared Peripheral Interrupt, interrupt from a peripheral whose interrupt line's CPU target is programmable to one or more CPU interface by the Distributor.

10.7.1 GIC2 CPU Interface

Table 10-8 GIC2 CPU Interface Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x2000	GICC_CTLR	RW	0x0000_0000	Banked	control register
0x2004	GICC_PMR	RW	0x0000_0000	Banked	priority mask
0x2008	GICC_BPR	RW	0x0000_0002	Banked	binary point
0x200C	GICC_IAR	R (CMD)	0x0000_03ff	Banked	interrupt acknowledge
0x2010	GICC_EOIR	W (CMD)		Banked	end-of-interrupt
0x2014	GICC_RPR	R	0x0000_00F8	Banked	running priority
0x2018	GICC_HPPIR	R	0x0000_03FF	Banked	highest priority pending
0x201C	GICC_ABPR	RW	0x0000_0003	Restricted	aliased binary point
0x2020	GICC_AIAR	R (CMD)	0x0000_03FF	Restricted	aliased interrupt acknowledge
0x2024	GICC_AEOIR	W(CMD)		Restricted	aliased end of interrupt
0x2028	GICC_AHPPIR	R	0x0000_03FF	Restricted	aliased highest priority pending

Table 10-8 GIC2 CPU Interface Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x202C-0x20CC	Reserved				
0x20D0-0x20DC	GICC_APR	RW	0x0000_0000	Banked	Active Priorities
0x20E0-0x20EC	GICC_NSAPR	RW	0x0000_0000	Secure	aliased non-secure Active Priorities
0x20F0-0x2F8	Reserved				
0x20FC	GICC_IIDR	R	0x0002_0070	Common	ID
0x2100-0x2FFC	Reserved				
0x3000	GICC_DIR	W		Banked	Deactivate Interrupt

10.7.1.1 GIC2 CPU interface registers

0x1000A000 GSS_A5_GICC_CTLR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_CTLR configures the GIC2 CPU interface.

Non-secure access: Access is granted only to bits 0, 5,6 and 9.

Secure access: Access is granted to all register bits. Non-secure bits 0,5,6, and 9 are aliased into bits 1, 7, 8, and 10 for access by secure software.Modifying these aliased bits will modify the non-secure settings. Bits 0, 5, 6, 9 are physically banked into Secure and Non-secure space.

GSS_A5_GICC_CTLR

Bits	Name	Description
31:11	RESERVED	
10	EOIMODENS	For secure software, a read/writable alias of Non-Secure EOImode.
9	EOIMODE	For secure software, controls the behavior of secure access to GICC_EOI and GICC_DIR. For non-secure software, controls the behavior of non-secure access to GICC_EOI and GICC_DIR. 0x0: PD_AND_DI (Both Priority Drop and Deactivate Interrupt, GICC_DIR does not function) 0x1: PD (GICC_EOI performs Priority Drop, GICC_DIR performs deactivate interrupt function)

GSS_A5_GICC_CTLR (cont.)

Bits	Name	Description
8	IRQBYPDISABLENS	For secure software, a read/writable alias of Non-secure version of IRQBypDisable.
7	FIQBYPDISABLENS	For secure software, a read/writable alias of Non-secure version of FIQBypDisable
6	IRQBYPDISABLE	For Non-secure software, when CPU Interface is disabled, prevents the legacy bypass IRQ signal from being forwarded to the CPU (if IRQ is under Non-secure control). For secure software, prevents bypass if FIQ is under secure control. 0x0: CLR 0x1: SET
5	FIQBYPDISABLE	For Non-secure software, when CPU Interface is disabled, prevents the legacy bypass FIQ signal from being forwarded to the CPU (if FIQ is under Non-secure control). For secure software, prevents bypass if FIQ is under secure control. 0x0: CLR 0x1: SET
4	SBPR	Controls which binary point register is used to calculate preemption. 0x0: BANKED (secure interrupts use the secure Binary Point Register, non-secure interrupts use the non-secure Binary Point Register) 0x1: RESTRICTED (all interrupts use the secure Binary Point Register)
3	S_DEST	Controls destination of secure interrupts. 0x0: IRQ 0x1: FIQ
2	ACKCTL	Controls the side effect behavior of a secure read request to the Interrupt Acknowledge Register in the case where the highest priority pending interrupt is non-secure. If AckCtl is set to 0, a secure read request to the Interrupt Acknowledge Register returns an Interrupt ID value of 1022, and the read request does not cause the interrupt to be acknowledged (that is the Pending status of the interrupt remains unchanged). If AckCtl is set to 1, a secure read request to the Interrupt Acknowledge Register returns the Interrupt ID value of the non-secure interrupt, and causes the interrupt to be acknowledged (that is the interrupt becomes Active, or Active and Pending). 0x0: DISABLE ACK OF NS PENDING 0x1: ENABLE ACK OF NS PENDING

GSS_A5_GICC_CTLR (cont.)

Bits	Name	Description
1	ENABLE_NS	For secure software, a read/writable alias of non secure software's enable bit (bit 0 of this same register in non secure space). 0x0: CLR 0x1: SET
0	ENABLE	For non-secure software, this bit enables/disables non secure interrupts. For secure software, this bit enables/disables secure interrupts. 0x0: CLR 0x1: SET

0x1000A004 GSS_A5_GICC_PMR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_PMR register configures the GIC2 CPU interface Priority Mask. The Priority Mask can be used to limit the interrupts that can cause an interrupt request to the CPU based on priority levels.

Non-secure access: Write access is granted only if bit 7 is 0x1, writes are ignored otherwise. Reads are always granted, however, bit 7 is always set in the data returned. Bit 0 is always zero.

Secure access: Access is granted to all register bits.

GSS_A5_GICC_PMR

Bits	Name	Description
31:8	RESERVED_1	
7:3	LEVEL	Set the Priority Mask Level. The CPU interface asserts an interrupt request to CPU if the priority of the highest Pending interrupt sent by the interrupt Distributor is strictly higher than at least the mask set in Priority Mask Register.
2:0	RESERVED_2	

0x1000A008 GSS_A5_GICC_BPR

Type: Read/write
Clock: CLK
Reset State: 0x00000002

Security Treatment: Banked

The GICC_BPR register configures the GIC2 CPU interface Binary Point. The Binary Point is used to limit interrupts that can cause an interrupt request to the CPU based on the interrupt's priority and the interrupt priority that currently being serviced by the CPU (if there is one). If the CPU is not servicing an interrupt, the Binary Point register is not used.

Non-secure: access Provides access to the non-secure Binary Point register.

Secure access: Provides access to the secure Binary Point register. Secure software may access the non-secure Binary Point register at offset 0x001C.

Table 10-9 Interpretation of Binary Point Register value

Register value	Priority bits used to determine preemption for secure interrupts	Priority bits used to determine preemption for non-secure interrupts (Bit 7 is always 0x1)
0	7:1	7:0
1	7:2	7:1
2	7:3	7:2
3	7:4	7:3
4	7:5	7:4
5	7:6	7:5
6	7	7:6
7	No preemption	No preemption

GSS_A5_GICC_BPR

Bits	Name	Description
31:3	RESERVED	
2:0	VAL	The VAL setting is used to determine the priority bits used for preemption according to Table 10-9, Interpretation of Binary Point Register value.

0x1000A00C GSS_A5_GICC_IAR

Type: Read (Command)
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Banked

The GICC_IAR register is used by the CPU to obtain the ID of the interrupt which caused the assertion if IRQn or FIQn.

Performing this read has the side effect of causing the Distributor to change the interrupt from the Pending state to the Active or Active and Pending state according the description below:

Using three bits defined by AHB bus security state (1=non-secure), security of the HPPI (1=non-secure) and the value of GICC_CTLR[AckCtl]:

- 00x ’ respond with the true interrupt number, transitioning to active (secure request to secure interrupt, ACKCTL is don't care)
- 010 ’ respond with 1022 (secure request to non-secure interrupt but ACKCTL=0 disabling secure handling of non-secure interrupts)
- 011 ’ respond with the true interrupt number, transitioning to active (secure request to non-secure interrupt with ACKCTL=1)
- 10x ’ respond with 1023 (non-secure request to secure interrupt)
- 11x ’ respond with the true interrupt number, transitioning to active (non-secure request to non-secure interrupt)

GSS_A5_GICC_IAR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier. The value returned in this field is dependent on the security state of the access to the register, the security state of any outstanding interrupts, the value of GICC_CTLR[AckCtl] as defined in the description above.

0x1000A010 GSS_A5_GICC_EOIR

Type: Write (Command)
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

Unlike GIC1, GICC_EOIR (End Of Interrupt) register has two possible behaviors. By default it acts as it did in GIC1, that is, it can be written to indicate when software has finished handling an interrupt.

In GIC2, if GICC_CTLR[EOImode] is set (1), writing this register has the "priority drop" (PD) effect. The PD effect is when the active priority bit for the highest priority active interrupt is cleared. The key difference, when EOImode is one, is that the Distributor is not notified that this happened - that is, the interrupt itself does not become inactive.

When EOImode is zero, writing to this register will, in addition to the PD effect described above, set the interrupt to Inactive or Pending (if prior to writing to this register, the interrupt was both Active and Pending it becomes just pending) in the Distributor.

In either case, the value written must be the interrupt ID, and the CPU Source ID for SGIs, of the interrupt that is being completed.

The security status of the write to this register (NS-prot) must match the security status (NS-int) of the interrupt ID, according to Table 10-10 for the interrupt to be successfully cleared.

Non-secure access: See Table 10-10.

Secure access: See Table 10-10.

Table 10-10 GICC_EOIR Priority Drop Effect Definition

[AckCtl]	Security status of the write request	Highest Priority Active interrupt security value	Effect
x	Non-secure	Non-secure	Clear the highest active Non-secure priority level
x	Non-secure	Secure	Clear the highest active Non-secure priority level
0	Secure	X	Clear the highest active Secure priority level
1	Secure	X	Clears the highest active priority level.

GSS_A5_GICC_EOIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it must match the ID of the CPU which requested the Interrupt. As described in Table 17-9 (GICC_EIOR security (and source CPU) match definition), the CPU Source ID must match an active interrupt in order for the GICC_EOIR to take effect. The CPU_ID is written must match that delivered to software when GICC_IAR is read. For PPIs and SPIs the CPU source ID field is ignored.
9:0	INT_ID	Interrupt Identifier. The value must match the interrupt ID that software received when reading the GICC_IAR register. If the security settings match (see Table 17-9) a write will cause the priority drop effect and if EOImode=0, the Active state in the Distributor for the corresponding interrupt will also be cleared.

0x1000A014 GSS_A5_GICC_RPR

Type: Read
Clock: CLK
Reset State: 0x000000F8

Security Treatment: Banked

The GICC_RPR (Running Priority) register provides access to the highest priority of all the Active interrupts on this CPU. The priority value returned is sensitive to the security status (NS-int) of the interrupt currently running and the NS-prot

Non-secure access: If the currently interrupt is secure (NS-int = 0), and a non-secure read of the Running Priority register is attempted (NS-prot = 1), then the value 0 (maximum priority) is returned.

Secure access: Returns the true value in the register.

GSS_A5_GICC_RPR

Bits	Name	Description
31:8	RESERVED_1	
7:3	VAL	Running Priority
2:0	RESERVED_2	

0x1000A018 GSS_A5_GICC_HPPIR

Type: Read
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Banked

The GICC_HPPIR register provides access to the highest priority pending interrupt to the CPU Interface.

NOTE Interrupts that are Active and Pending in the Distributor are not considered candidates to become the highest priority pending interrupt.

Using three bits defined by AHB bus security state (1=non-secure), security of the HPPI(1=non-secure) and the value of GICC_CTLR[AckCtl]:

00x ’ respond with the true interrupt number (secure request to secure interrupt, ACKCTL is don't care)

010 ’ respond with 1022 (secure request to non-secure interrupt but ACKCTL=0 disabling secure handling of non-secure interrupts)

011 ’ respond with the true interrupt number (secure request to non-secure interrupt with ACKCTL=1)

10x ’ respond with 1023 (non-secure request to secure interrupt)

11x ’ respond with the true interrupt number (non-secure request to non-secure interrupt)

GSS_A5_GICC_HPPIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier. The value returned in this field is dependent on the security state of the access to the register, and the security state of any outstanding interrupts, as described above.

0x1000A01C GSS_A5_GICC_ABPR

Type: Read/write
Clock: CLK
Reset State: 0x00000003

Security Treatment: Restricted

The GICC_ABPR register provides a copy of the non-secure binary point register for use by secure software. See the definition of the GICC_BPR register for details on the use of this register.

Non-secure access: No access.

Secure access: Access granted, updates are reflected to non-secure software at the GICC_BPR register at address offset 0x08.

GSS_A5_GICC_ABPR

Bits	Name	Description
31:3	RESERVED	
2:0	VAL	Same as the GICC_BPR register - affects only non-secure interrupts.

0x1000A020 GSS_A5_GICC_AIAR

Type: Read (Command)
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Restricted

The GICC_AIAR register is used by the CPU to obtain the ID of the interrupt which caused the assertion if IRQn or FIQn. This is a secure only register used to read non-secure interrupts by Secure Software.

Performing this read has the side effect of causing the Distributor to change the interrupt from the Pending state to the Active or Active and Pending state.

Non-secure access: No access. Read as zero.

Secure access: See description below.

Based on the 2 bits defined by the AHB Security of the request (1=non-secure) and the security of the interrupt (1=non-secure):

00 ’ respond with 1023 (secure request that behaves as if it is a non-secure request, to secure interrupt)

01 ’ respond with the true interrupt number, transitioning to active (secure request that behaves as if it is a non-secure request, to non-secure interrupt)

1x ’ RAZ/WI (non-secure request cannot access this register)

GSS_A5_GICC_AIAR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier..

0x1000A024 GSS_A5_GICC_AEOIR

Type: Write (Command)
Clock: CLK
Reset State: 0x00000000

Security Treatment: Restricted

A secure write to this register has an identical effect to a non-secure write to GICC_EOIR, with the exception of the EOImode bit; the value of the secure EOImode bit (bit 9) in GICC_CTLR is used to determine whether the interrupt is deactivated or just priority dropped rather than the non-secure EOImode bit (bit 10).

This register must be used by secure software to signal completion of non-secure interrupts when GICC_CTLR AckCtl bit is set to 0; GICC_EOIR cannot be used for this purpose since it would affect GICC_APRn rather than GICC_NSAPRn.

Non-secure access: ignored

Secure access: signal completion of non-secure interrupt

GSS_A5_GICC_AEOIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it must match the ID of the CPU which requested the Interrupt. The CPU Source ID must match an active interrupt in order for the GICC_AEOIR to take effect. The CPU_ID is written must match that delivered to software when GICC_IAR is read. For PPIs and SPIs the CPU source ID field is ignored.
9:0	INT_ID	Interrupt Identifier. The value must match the interrupt ID that software received when reading the GICC_IAR register. Interrupt Identifier. A write will cause the priority drop effect and if EOImode=0, the Active state in the Distributor for the corresponding interrupt will also be cleared.

0x1000A028 GSS_A5_GICC_AHPPIR

Type: Read
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Restricted

This is a Secure-Only register.

A read from this register has an identical effect to a Non-Secure read from GICC_HPPIR. It can therefore be used to check for a pending Non-Secure interrupt without the possibility of returning a Secure Interrupt ID value.

Interrupts that are Active and Pending in the Distributor are not considered candidates to become the highest priority pending interrupt.

Non-secure access: No access. Read as zero.

Secure access: See description below.

NOTE

Using three bits defined by AHB bus security state (1=non-secure), security of the HPPI(1=non-secure)and the value of GICC_CTLR[AckCtl]:

00x ’ respond with 1023 (hppi is a secure interrupt)

01x ’ respond with the true interrupt number (hppi is a non-secure interrupt)

1xx ’ RAZ/WI (non-secure request cannot access this register)

.GSS_A5_GICC_APR

GSS_A5_GICC_AHPPIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier. The value returned in this field is dependent on the security state of the access to the register, and the security state of any outstanding interrupts, as described above.

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

Each bit in the GICC_APR register provides the active status of priorities in the CPU Interface.

Non-secure access: Bits 15-0 represent priorities 31 to 16 of the non-secure active priorities.

Secure access: Bits 31-0 represent priorities 31 to 0 of the active secure priorities.

GSS_A5_GICC_APR

Bits	Name	Description
31:0	PRI	0x1: A (ACTIVE) 0x0: NA (NOT ACTIVE)

0x1000A0E0 GSS_A5_GICC_NSAPR

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Restricted

Each bit in the GICC_NSAPR register provides the active status of non-secure priorities in the CPU Interface.

Non-secure access: None - write ignore, read-as-zero.

Secure access: Bits 31-0 represent priorities 31 to 0 of teh active non-secure priorities.

GSS_A5_GICC_NSAPR

Bits	Name	Description
31:0	PRI	0x1: A (ACTIVE) 0x0: NA (NOT ACTIVE)

0x1000A0FC GSS_A5_GICC_IIDR

Type: Read
Clock: CLK
Reset State: 0x00020070

Security Treatment: Common

The GICC_IIDR register provides information about the GIC2 CPU Interface version and device implementor information.

GSS_A5_GICC_IIDR

Bits	Name	Description
31:20	PART_NUM	Part Number: 0x0
19:16	ARCH_VERSION	Architecture Version : 0x2
15:12	REVISION	Revision number: 0x0
11:0	IMPLEMENTOR	Bits[11:8] contain the implementor's JEP106 continuation code, 0x0 Bit[7] is always 0 Bits[6:0] contain bits [6:0] of the implementor's JEP106 code,

0x1000B000 GSS_A5_GICC_DIR

Type: Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_DIR register provides the mechanism by which Software can Deactivate a specific interrupt.

Secure writes can deactivate secure and non-secure interrupts.

Non-secure writes can only deactivate non-secure interrupts..

Note that unlike GICC_EOIR and GICC_IAR, there is no restriction of the Deactivation of Non-Secure interrupts with Secure accesses. The AckCtl bit does not affect the behaviour of GICC_DIR. This is because unlike GICC_IAR there is no chance of the access affecting an

interrupt from an unexpected security state, and unlike GICC_EOIR there is no effect on GICC_APRn or GICC_NSAPRn, so there is no need to indicate which register should be affected.

GSS_A5_GICC_DIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier. INT_ID written should match value returned from GICC_IAR read.

10.8 GSS A5 GIC2 GICV Registers (0x10008000 GSS_A5_QGIC2_BASE)

This section contains the Global Navigation Subsystem (GSS) A5 GIC2 GICV registers.

The Generic Interrupt Controller 2 (GIC2) is a reusable configurable soft core. This GIC2 specification conforms to ARM's Generic Interrupt Controller architecture specification. Where differences exist, either additional features have been added or this document must change to conform to ARM's specified architecture. Where additional features were added, they will be clearly marked. The GIC2 design supports ARM's TrustZone architecture, with two security zones: secure and non-secure.

The GIC2 is made of two parts: the Distributor and up to eight CPU Interfaces. Each of these interfaces contains a CRIF slave interface. There must be at least one CPU Interface in the design.

In this manual, addresses are offsets from zero. When constants are exported, they are re-assigned to the appropriate base address.

Half-word and Byte access is supported by a subset of the registers.

Security treatment of registers in the GIC2 is divided into four types of registers. These are:

- "Common" indicates that both secure and non-secure software have full access to the register.
- "NS-int Dependent" indicates that state belonging to both secure and non-secure interrupts may be present in the register, depending on the value set in the Interrupt Security Register. Secure accesses to such a register are able to access all of the register's state, regardless of the Interrupt Security Register setting. Non-secure accesses may only access state belonging to non-secure interrupts. For non-secure accesses to state belonging to secure interrupts, writes are ignored and reads return zero.
- "Banked" indicates that the register exhibits different functionality according to whether it is accessed with a secure or non-secure request.
- "Restricted" indicates that only secure requests may access this register. If non-secure accesses are attempted, writes are ignored and reads return zero.

The type of register is specified for each register individual. Table 10-11 explains security treatment for register bits.

Table 10-11 Register security treatment

bus NS bit	SECURITY BIT	ALLOW Access
0	0	1
0	1	1
1	0	0
1	1	1

Glossary:

CPU Interface: That part of the GIC2 responsible for receiving the next interrupt from the Distributor and, if the interrupt has sufficient priority, asserting an interrupt indication to the CPU.

CPU MID: The Master ID of a CPU interface (as in AXI's AMID). The CPU MID reaching the Distributor must match the CPU Interface connected to that master.

Distributor: That part of the GIC2 responsible for detecting, disabling, prioritizing, and directing interrupts to CPU(s). The Distributor also accepts requests from and signals software interrupts to the CPU(s).

FABRIC: Flexible Advanced Buses & Reusable Interconnect Cores

NS-int: Security status of a particular interrupt ID. The value 0x0 is "secure", 0x1 is "non-secure".

NS-prot: Security status of the a bus transaction (read or write) according to the NS bit.

PPI: Private Peripheral Interrupt, interrupt from a peripheral whose interrupt line is destined to a particular CPU and can't be physically connected/directed to any other.

SGI: Software Generated Interrupt, interrupt from one CPU (or thread) to another.

SPI: Shared Peripheral Interrupt, interrupt from a peripheral whose interrupt line's CPU target is programmable to one or more CPU interface by the Distributor.

10.8.1 QGIC2 Virtual CPU Interface

Table 10-12 QGIC2 Virtual CPU Interface Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x4000	GICV_CTLR	RW	0x0000_0000	Common	control register
0x4004	GICV_PMR	RW	0x0000_0000	Common	priority mask
0x4008	GICV_BPR	RW	0x0000_0002	Common	binary point
0x400C	GICV_IAR	R (CMD)	0x0000_0000	Common	interrupt acknowledge
0x4010	GICV_EOIR	W (CMD)		Common	end-of-interrupt
0x4014	GICV_RPR	R	0x0000_00F8	Common	running priority
0x4018	GICV_HPPIR	R	0x0000_03FF	Common	highest priority pending
0x401C	GICV_ABPR	RW	0x0000_0003	Common	aliased binary point
0x4020	GICV_AIAR	R (CMD)	0x0000_03FF	Common	aliased interrupt acknowledge
0x4024	GICV_AEOIR	W (CMD)		Common	aliased end-of-interrupt
0x4028	GICV_AHPPIR	R	0x0000_03FF	Common	aliased highest priority pending

Table 10-12 QGIC2 Virtual CPU Interface Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x402C-0x40CC	Reserved				
0x40D0	GICV_APR	RW	0x0000_0000	Common	Active Priorities
0x40D4-0x40F8	Reserved				
0x40FC	GICV_IIDR	R	0x0002_0070	Common	ID
0x4100-0x4FFC	Reserved				
0x5000	GICV_DIR	W		Common	Deactivate Interrupt

10.8.1.1 QGIC2 Virtual CPU interface registers

NOTE All transactions to the Virtual CPU Interface are treated as secure. All bits are accessible to every transaction. There the secure and non-secure views do not apply to this block of registers. All access to GICV registers operate upon the hypervisor portion of GIC2 in a similar fashion as GICC registers operate on the distributor.

0x1000C000 GSS_A5_GICV_CTLR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICV_CTLR configures the GIC2 Virtual CPU interface.

GSS_A5_GICV_CTLR

Bits	Name	Description
31:10	RESERVED_1	
9	EOIMODE	Controls the behavior of Non-secure access to GICV_EOI and GICV_DIR 0x0: PD_AND_DI (Both Priority Drop and Deactivate Interrupt, GICV_DIR does not function) 0x1: PD (GICV_EOI performs Priority Drop, GICV_DIR performs deactivate interrupt function)
8:5	RESERVED_2	

GSS_A5_GICV_CTLR (cont.)

Bits	Name	Description
4	GBPR	Controls which binary point register is used to calculate preemption, GICV_BPR or the GICV_ABPR. 0x0: BANKED (Group 0 interrupts use the Group 0 Binary Point Register, Group 1 interrupts use the Group 1 Binary Point Register) 0x1: G0 (all interrupts use the Group 0 Binary Point Register)
3	FIQEN	Controls destination of secure interrupts. 0x0: IRQ 0x1: FIQ
2	ACKCTL	Controls whether reads of the VM Interrupt Acknowledge Register can acknowledge interrupts where the NS bit is set in the List Register. acknowledged only if the NS bit is clear in the corresponding List Register. If the NS bit in that List Register is set, the read will return 1022 and the interrupt can only be acknowledge by a read to the VM Aliased Interrupt Acknowledge Register.) always acknowledged regardless of the NS bit setting in the corresponding List Register.) 0x0: NO_IAR_4G0 (On a read of GICV_IAR, the highest priority unmasked PENDING interrupt is) 0x1: IAR_4G0 (On a read of GICV_IAR, the highest priority unmasked PENDING interrupt is)
1	ENABLE_G1	This bit enables Group 1 interrupts. 0x0: CLR 0x1: SET
0	ENABLE_G0	This bit enables Group 0 interrupts. 0x0: CLR 0x1: SET

0x1000C004 GSS_A5_GICV_PMR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICV_PMR register configures the GIC2 Virtual CPU interface Priority Mask. The Priority Mask can be used to limit the interrupts that can cause an interrupt request to the CPU based on priority levels.

GSS_A5_GICV_PMR

Bits	Name	Description
31:8	RESERVED_1	
7:3	LEVEL	Set the Priority Mask Level. The CPU interface asserts an interrupt request to CPU if the priority of the highest Pending interrupt sent by the interrupt Distributor is strictly higher than at least the mask set in Priority Mask Register.
2:0	RESERVED_2	

0x1000C008 GSS_A5_GICV_BPR

Type: Read/write
Clock: CLK
Reset State: 0x00000002

Security Treatment: Common

The GICV_BPR register configures the GIC2 Virtual CPU interface Binary Point. The Binary Point is used to limit interrupts that can cause an interrupt request to the CPU based on the interrupt's priority and the interrupt priority that currently being serviced by the CPU (if there is one). If the CPU is not servicing an interrupt, the Binary Point register is not used.

GSS_A5_GICV_BPR

Bits	Name	Description
31:3	RESERVED	
2:0	VAL	The VAL setting is used to determine the priority bits used for preemption according to Table 10-9 Interpretation of Binary Point Register value.

0x1000C00C GSS_A5_GICV_IAR

Type: Read (Command)
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Common

The GICV_IAR register is used by the CPU to obtain the ID of the interrupt which caused the assertion if IRQn or FIQn.

Performing this read has the side effect of causing the GICH to change the interrupt from the Pending state to the Active or Active and Pending state according to the rules below:

Using the 2 bits defined by Security of the HPPI(1=non-secure) and the value of GICV_CTLR[AckCtl]:

0x ’ respond with the true interrupt number, transitioning to active (ignore APROTNS and consider as a secure request to secure interrupt, ACKCTL is don't care)

10 ’ respond with 1022 (ignore APROTNS and consider as secure request to non-secure interrupt but ACKCTL=0 disabling secure handling of non-secure interrupts)

11 ’ respond with the true interrupt number, transitioning to active (ignore APROTNS and consider as secure request to non-secure interrupt with ACKCTL=1)

GSS_A5_GICV_IAR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier - a virtual interrupt number determined by the Hypervisor SW.

0x1000C010 GSS_A5_GICV_EOIR

Type: Write (Command)
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

GICV_EOIR (End Of Interrupt) register has two possible behaviors. By default it can be written to to indicate when software has finished handling an interrupt.

If GICV_CTLR[EOImode] is set (1), writing this register has the "priority drop" (PD) effect. The PD effect is when the active priority bit for the highest priority active interrupt is cleared. The key difference, when EOImode is (1), is the interrupt itself does not become inactive.

When EOImode is (0), writing to this register will, in addition to the PD effect described above, set the interrupt to Inactive or Pending (if prior to writing to this register, the interrupt was both Active and Pending it becomes just pending). However, if GICV_CTLR[EOImode] is (0), then the CPU_ID and INT_ID must match an active interrupt for a state change to occur.

In either case, the value written must be the interrupt ID, and the CPU Source ID for SGIs, of the interrupt that is being completed.

GSS_A5_GICV_EOIR

Bits	Name	Description
31:13	RESERVED	

GSS_A5_GICV_EOIR (cont.)

Bits	Name	Description
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it must match the ID of the CPU which requested the Interrupt. The CPU_ID is written must match that delivered to software when GICV_IAR is read. For PPIs and SPIs the CPU source ID field is ignored.
9:0	INT_ID	Interrupt Identifier. The value must match the interrupt ID that software received when reading the GICV_IAR register.

0x1000C014 GSS_A5_GICV_RPR

Type: Read
Clock: CLK
Reset State: 0x000000F8

Security Treatment: Common

The GICV_RPR (Running Priority) register provides access to the highest priority of all the Active interrupts on this Virtual CPU.

GSS_A5_GICV_RPR

Bits	Name	Description
31:8	RESERVED_1	
7:3	VAL	Running Priority
2:0	RESERVED_2	

0x1000C018 GSS_A5_GICV_HPPIR

Type: Read
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Common

The GICV_HPPIR register provides access to the highest priority pending interrupt to the Virtual CPU Interface. If no interrupt is pending, responds with 0x3FF.

NOTE Interrupts that are Active and Pending in the GICH (hypervisor) are not considered candidates to be come the highest priority pending interrupt.

Using 2 bits defined by the value of GICV_CTLR[AckCtl]and the NS bit of the HPPI(1=non-secure):

1x ’ respond with the virtual interrupt number

00 ’ respond with the virtual interrupt number

01 ’ respond with 1022

GSS_A5_GICV_HPPIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier.

0x1000C01C GSS_A5_GICV_ABPR

Type: Read/write
Clock: CLK
Reset State: 0x00000003

Security Treatment: Common

The GICV_ABPR register provides access to the non-secure binary point register used by non-secure interrupts when GICV_CTRL[GBPR]=0. See the definition of the GICV_BPR register for details on the use of this register.

GSS_A5_GICV_ABPR

Bits	Name	Description
31:3	RESERVED	
2:0	VAL	Same as the GICV_BPR register - affects only non-secure interrupts.

0x1000C020 GSS_A5_GICV_AIAR

Type: Read (Command)
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Common

The GICV_AIAR register is used by the CPU to obtain the ID of the interrupt which caused the assertion if IRQn or FIQn.

Performing this read has the side effect of causing the GICH to change the interrupt from the Pending state to the Active or Active and Pending state according to the rules below:

Using the security state of the pending interrupt:

- 0 ’ respond with 1023
- 1 ’ respond with the true interrupt number, transitioning to active

GSS_A5_GICV_AIAR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier - a virtual interrupt number determined by the Hypervisor SW.

0x1000C024 GSS_A5_GICV_AEOIR

Type: Write (Command)
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

This register presents the same programmers model as GICC_AEOIR.

The effect of writing to this register is identical to the effect of writing the same value to the GICV_EOIR register. This alias is provided for compatibility with the Physical CPU Interface, where the two registers have a different effect due to the provision of separate Secure and Non-Secure Active Priority Registers.

GSS_A5_GICV_AEOIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it must match the ID of the CPU which requested the Interrupt. The CPU_ID is written must match that delivered to software when GICV_IAR is read. For PPIs and SPIs the CPU source ID field is ignored.
9:0	INT_ID	Interrupt Identifier. The value must match the interrupt ID that software received when reading the GICV_IAR register.

0x1000C028 GSS_A5_GICV_AHPPIR

Type: Read
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Common

This register presents the same programmers model as GICC_AHPPIR.

This register returns the interrupt ID of the highest priority PENDING interrupt if it has an NS value of 1. Reading this interrupt has no side effects and simply returns the highest priority PENDING interrupt among the list registers or a status code according to the following table:

Using the NS bit of the HPPI(1=non-secure):

0 ’ 1023

1 ’ respond with the virtual interrupt number

Note that in some cases the returned value may not be strictly accurate if interrupts are currently paged out in software.

GSS_A5_GICV_AHPPIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier.

0x1000C0D0 GSS_A5_GICV_APR

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

Each bit in the GICV_APR is an alias of GICH_APR. The data and access control are one and the same.

GSS_A5_GICV_APR

Bits	Name	Description
31:0	PRI	0x1: A (ACTIVE) 0x0: NA (NOT ACTIVE)

0x1000C0FC GSS_A5_GICV_IIDR

Type: Read
Clock: CLK
Reset State: 0x00020070

Security Treatment: Common

The GICV_IIDR register provides information about the GIC2 Virtual CPU Interface version and device implementor information.

GSS_A5_GICV_IIDR

Bits	Name	Description
31:20	PART_NUM	Part Number: 0x390
19:16	ARCH_VERSION	Architecture Version : 0x2
15:12	REVISION	Revision number: 0x0
11:0	IMPLEMENTOR	Bits[11:8] contain the implementor's JEP106 continuation code, 0x0 Bit[7] is always 0 Bits[6:0] contain bits [6:0] of the implementor's JEP106 code,

0x1000D000 GSS_A5_GICV_DIR

Type: Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICV_DIR register provides the mechanism by which Software can Deactivate a specific interrupt.

GSS_A5_GICV_DIR

Bits	Name	Description
31:13	RESERVED	

GSS_A5_GICV_DIR (cont.)

Bits	Name	Description
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt.
9:0	INT_ID	Interrupt Identifier. The value should match the INT_ID returned from the read of GICV_IAR.

10.9 GSS A5 Timer Registers (0x10002000 GSS_A5_TIMERS_BASE)

This section contains the Global Navigation Subsystem (GSS) A5 Timer registers.

10.9.1 a5ss Registers

0x10002000 GSS_A5_APCS_TMRSECURE

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Restricted

The APCS_TMRSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Scorpion's APROTNS pin. When APROTNS is set to '0' the state of the APCS_TMRSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_TMRSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_TMRSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_TMRSECURE register correspond to.

GSS_A5_APCS_TMRSECURE

Bits	Name	Description
4	WDT0	Controls security treatment for the Watch Dog Timer registers: APCS_WDT0_FRZ, APCS_WDT0_INT_EN, APCS_WDT0_STS, APCS_WDT0_INT_WIDTH, APCS_WDT0_BARK_TIME, APCS_WDT0_TST_LD_STS, APCS_WDT0_TST_LD. 0x1: NSEC 0x0: SEC
3	WDT1	Controls security treatment for the Watch Dog Timer registers: APCS_WDT1_FRZ, APCS_WDT1_INT_EN, APCS_WDT1_STS, APCS_WDT1_INT_WIDTH, APCS_WDT1_BARK_TIME, APCS_WDT1_TST_LD_STS, APCS_WDT1_TST_LD. 0x1: NSEC 0x0: SEC
2	GPT0	Controls security treatment for the General Purpose Timer registers: APCS_GPT1_MTCH, APCS_GPT1__CNT, APCS_GPT1_EN, APCS_GPT1_CLR and bits 11-8 of APCS_TMR_STS. 0x1: NSEC 0x0: SEC

GSS_A5_APCS_TMRSECURE (cont.)

Bits	Name	Description
1	GPT1	Controls security treatment for the General Purpose Timer registers: APCS_GPT0_MTCH, APCS_GPT0__CNT, APCS_GPT0_EN, APCS_GPT0_CLR and bits 11-8 of APCS_TMR_STS. 0x1: NSEC 0x0: SEC
0	DGT	Controls security treatment for the Debug Timer registers; APCS_DGT_MTCH, APCS_DGT_CNT, APCS_DGT_EN, APCS_DGT_CLR, APCS_DGT_CLK_CTL, and bits 3-0 of APCS_TMR_STS 0x1: NSEC 0x0: SEC

0x10002004 GSS_A5_APCS_GPT0_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: APCS_TMRSECURE [GPT0].

The general purpose timer will signal interrupt when its counter value has reached the value stored in the APCS_GPT0_MTCH register.

GSS_A5_APCS_GPT0_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_GPT0_CNT at which an interrupt will be generated.

0x10002008 GSS_A5_APCS_GPT0_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_CNT register contains the current value of the GPT0 timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_GPT0_MTCH register at the same time due to HW re-use. The procedure for writing the APCS_GPT0_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_GPT0_EN.

- Write APCS_GPT0_CNT.
- Write (to set/restore) APCS_GPT0_MTCH if required.
- Enable the timer by setting the EN bit in APCS_GPT0_EN.

GSS_A5_APCS_GPT0_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer.

0x1000200C GSS_A5_APCS_GPT0_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_EN register is used to enable the GPT0 timer.

GSS_A5_APCS_GPT0_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	CLR_ON_MTCH_EN	When set (1), the timer will clear when it reaches the match value.
0	EN	When set (1), the timer is enabled and counts with frequency ACC_SLP_CLK.

0x10002010 GSS_A5_APCS_GPT0_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_CLR register is a one-shot command register that, when written with any value, resets the timer to a value of 0. This occurs regardless of the state of the APCS_GPT0_EN register.

GSS_A5_APCS_GPT0_CLR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Data written is not used.

0x10002014 GSS_A5_APCS_GPT1_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The GPT timer will signal interrupt when its counter value has reached the value stored in the APCS_GPT1_MTCH register.

GSS_A5_APCS_GPT1_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_GPT1_CNT at which an interrupt will be generated.

0x10002018 GSS_A5_APCS_GPT1_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_CNT register contains the current value of the GPT1 timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_GPT1_MTCH register at the same time. The procedure for writing the APCS_GPT1_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_GPT1_EN.
- Write APCS_GPT1_CNT.
- Write (to set/restore) APCS_GPT1_MTCH if required.
- Enable the timer by setting the EN bit in APCS_GPT1_EN.

GSS_A5_APCS_GPT1_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer

0x1000201C GSS_A5_APCS_GPT1_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_EN register is used to enable the GPT1 timer.

GSS_A5_APCS_GPT1_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	CLR_ON_MTCH_EN	When set (1), timer will clear when it reaches the match value.
0	EN	When set (1), timer is enabled and counts with frequency sleep clock.

0x10002020 GSS_A5_APCS_GPT1_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_CLR register is a one-shot command register that, when written with any value, resets the GPT1 timer to a value of 0. This occurs regardless of the state of the APCS_GPT1_EN register.

GSS_A5_APCS_GPT1_CLR

Bits	Name	Description
31:0	RESERVED_BITS_31_0	Data written is not used.

0x10002024 GSS_A5_APCS_DGT_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The DBG timer will signal interrupt when its counter value has reached the value stored in the APCS_DGT_MTCH register.

GSS_A5_APCS_DGT_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_DGT_CNT at which an interrupt will be generated.

0x10002028 GSS_A5_APCS_DGT_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CNT register contains the current value of the DGT timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_DGT_MTCH register at the same time due to HW re-use. The procedure for writing the APCS_DGT_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_DGT_EN.
- Write APCS_DGT_CNT.
- Write (to set/restore) APCS_DGT_MTCH if required.
- Enable the timer by setting the EN bit in APCS_DGT_EN.

GSS_A5_APCS_DGT_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer count

0x1000202C GSS_A5_APCS_DGT_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_EN register is used to enable the DGT timer.

GSS_A5_APCS_DGT_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	

GSS_A5_APCS_DGT_EN (cont.)

Bits	Name	Description
1	CLR_ON_MTCH_EN	When set (1), the timer will clear when it reaches the match value.
0	EN	When set (1), the timer is enabled and counts with frequency TCXO clock.

0x10002030 GSS_A5_APCS_DGT_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CLR register is a one-shot command register that, when written with any value, resets the DGT timer to a value of 0. This occurs regardless of the state of the APCS_DGT_EN register.

GSS_A5_APCS_DGT_CLR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Data written is not used.

0x10002034 GSS_A5_APCS_DGT_CLK_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0003

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CLK_CTL controls the clock divider inside the Debug Timer.

NOTE It is possible for the AHB clock to run at as slow as 5 MHz using settings of the Global Clock Controller. The debug timer's counter can also run at 5 MHz (TCXO divided by 4). However, due to the synchronization circuit using the edge detect, the timer should always run at least 4x slower than the AHB clock. Thus, if the timer's use is required by the system, the divider should be set to divide by 4 and the slowest usable AHB frequency is 20MHz. The timer would run at 5MHz in this case.

GSS_A5_APCS_DGT_CLK_CTL

Bits	Name	Description
31:2	RESERVED_BITS_31_2	

GSS_A5_APCS_DGT_CLK_CTL (cont.)

Bits	Name	Description
1:0	DIV	0x3: 4 0x2: 3 0x1: 2 0x0: 1

0x10002038 GSS_A5_APCS_WDT0_RST

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_RST register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset the watch dog counter. This command register also disables the watchdog freeze

GSS_A5_APCS_WDT0_RST

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	STB	This bit generates the WDT0_STB during the non-sleep mode. A pulse is generated on WDT0_STB when this bit is written with a ’1

0x1000203C GSS_A5_APCS_WDT0_FRZ

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_FRZ register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the APCS_WDT0_RST register.

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

GSS_A5_APCS_WDT0_FRZ

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved

GSS_A5_APCS_WDT0_FRZ (cont.)

Bits	Name	Description
0	FRZ	This bit is used to freeze the watchdog timer at time 0. To enable the watchdog timer auto-kicker, write a '1'.

0x10002040 GSS_A5_APCS_WDT0_EN

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_EN register controls when the watch dog timer is enabled.

GSS_A5_APCS_WDT0_EN

Bits	Name	Description
31:2	RESERVED_BITS_31_2	Reserved
1	INT_EN	Any write to this register: 0x1: yes (any unmasked IRQ or FIQ will enable the WDT0 timer.) 0x0: no
0	EN	Any write to this register: 0x1: yes (the watch dog timer is enabled) 0x0: no

0x10002044 GSS_A5_APCS_WDT0_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_STS register is the watchdog status register.

GSS_A5_APCS_WDT0_STS

Bits	Name	Description
31:3	WDT_CNT	Counter value [28:0] of the watch dog counter. **NOTE** The sleep counter value is sampled using the AHB clk. Multiple reads are required to determine the value (assuming AHB clk is much faster than sleep clock).
2	WDT_RST_STS	Show the status of watchdog0 counter reset.

GSS_A5_APCS_WDT0_STS (cont.)

Bits	Name	Description
1	AUTOKICK	This bit indicates whether the auto-kicker is on. 0x1: On 0x0: Off
0	RST_STS	0x1: wdt (the last system reset was due to WDT0) 0x0: reset (the last system reset was not due to WDT0.)

0x10002048 GSS_A5_APCS_WDT0_INT_WIDTH

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_INT_WIDTH register defines the width of the WDT0 biteExpired pulse in the number of sleep_clk pulses. The default value is 0x0C7C, but this reset value is not readable through the AHB interface.

GSS_A5_APCS_WDT0_INT_WIDTH

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter value on which to de-assert the WDI bite pulse.

0x1000204C GSS_A5_APCS_WDT0_BARK_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (‘bark’) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, but this reset value is not readable through the AHB interface. Note that this value is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (‘bark’) interrupt.

GSS_A5_APCS_WDT0_BARK_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter value on which to trigger the bark interrupt.

0x10002050 GSS_A5_APCS_WDT0_TST_LD_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TST_LD_STS register indicates when the watchdog test load is synchronizing to the SLP_CLK.

GSS_A5_APCS_WDT0_TST_LD_STS

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SYNC_STS	When set (1) wdog test load is synchronizing to SLP_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x10002054 GSS_A5_APCS_WDT0_TST_LD

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TEST_LD register loads the WDT0_TST register value into the watchdog counter.

GSS_A5_APCS_WDT0_TST_LD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	LD	Set on this bit to load the value into the WDT0_TST register into the WDT0 counter.

0x10002058 GSS_A5_APCS_WDT0_TST

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TST register indicates that the watchdog test is synchronizing to the SLP_CLK and contains the watch dog counter test load value.

GSS_A5_APCS_WDT0_TST

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter test load value [28:0].

0x1000205C GSS_A5_APCS_WDT0_BITE_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_31F3

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_BITE_TIME register determines the counter value at which WDT0 asserts the biteExpired signal.

GSS_A5_APCS_WDT0_BITE_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog bite time is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 bite expiration time [28:0].

0x10002060 GSS_A5_APCS_WDT1_RST

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_RST register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset the watch dog counter. This command register also disables the watchdog freeze

GSS_A5_APCS_WDT1_RST

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	STB	This bit generates the WDT1_STB during the non-sleep mode. A pulse is generated on WDT1_STB when this bit is written with a '1'

0x10002064 GSS_A5_APCS_WDT1_FRZ

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_FRZ register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the APCS_WDT1_RST register.

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

GSS_A5_APCS_WDT1_FRZ

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	FRZ	This bit is used to freeze the watchdog timer at time 0. To enable the watchdog timer auto-kicker, write a '1'.

0x10002068 GSS_A5_APCS_WDT1_EN

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_EN register controls when the watchdog timer is enabled.

GSS_A5_APCS_WDT1_EN

Bits	Name	Description
31:2	RESERVED_BITS_31_2	Reserved
1	INT_EN	Any write to this register: 0x1: yes (any unmasked IRQ or FIQ will enable the WDT0 timer.) 0x0: no
0	EN	Any write to this register: 0x1: yes (the watch dog timer is enabled) 0x0: no

0x1000206C GSS_A5_APCS_WDT1_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_STS register is the watchdog status register.

GSS_A5_APCS_WDT1_STS

Bits	Name	Description
31:3	WDT_CNT	Counter value [28:0] of the watch dog counter. **NOTE** The counter value is sampled using the ahb clk. Multiple reads are required to determine the value (assuming ahb clk is much faster than sleep clock).
2	WDT_RST_STS	Show the status of watchdog counter reset.
1	AUTOKICK	This bit indicates whether the auto-kicker is on. 0x1: On 0x0: Off
0	RST_STS	0x1: wdt (the last system reset was due to WDT1) 0x0: reset (the last system reset was not due to WDT1.)

0x10002070 GSS_A5_APCS_WDT1_INT_WIDTH

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_INT_WIDTH register defines the width of the WDT1_expired pulse in the number of sleep_clk pulses.The default value is 0x0C7C, but this reset value is not readable through the AHB interface.

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GSS_A5_APCS_WDT1_INT_WIDTH

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter value on which to de-assert the WDI expired pulse.

0x10002074 GSS_A5_APCS_WDT1_BARK_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (‘bark’) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, but this reset value is not readable through the AHB interface. Note that this value is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (‘bark’) interrupt.

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GSS_A5_APCS_WDT1_BARK_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter value on which to trigger the bark interrupt.

0x10002078 GSS_A5_APCS_WDT1_TST_LD_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TST_LD_STS register indicates when the watchdog test load is synchronizing to the SLP_CLK.

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GSS_A5_APCS_WDT1_TST_LD_STS

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SYNC_STS	When set (1) wdog test load is synchronizing to SLP_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x1000207C GSS_A5_APCS_WDT1_TST_LD

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TEST_LD register loads the WDT1_TST register value into the watchdog counter.

GSS_A5_APCS_WDT1_TST_LD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	LD	Set on this bit to load the value into the WDT1_TST register into the WDT counter

0x10002080 GSS_A5_APCS_WDT1_TST

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TST register indicates that the watchdog test is synchronizing to the SLP_CLK and contains the watch dog counter test load value.

GSS_A5_APCS_WDT1_TST

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter test load value [28:0]

0x10002084 GSS_A5_APCS_WDT1_BITE_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_31F3

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_BITE_TIME register determines the counter value at which WDT1 asserts the biteExpired signal.

GSS_A5_APCS_WDT1_BITE_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog bite time is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 bite expiration time [28:0].

0x10002088 GSS_A5_APCS_TMR_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [WDT0, WDT1, GPT0, GPT1, DGT].

The APCS_TMR_STS can be used to determine the status of each of the SCSS timers in the timer's resident clock domain. Since the timer clock domain may be much slower than the AHB clock, AHB transactions may be delayed in taking effect. This information can be used to qualify other actions or used simply for debug purposes. For example, software can determine when a write to APCS_DGT_CLR has taken effect by examining the DGT_CLR_PEND bit.

Each timer's bits are receive security treatment as specified by the APCS_TMRSECURE register.

GSS_A5_APCS_TMR_STS

Bits	Name	Description
31	RESERVED_BIT31	
30	WDT1_AUTOKICK	Auto-kicker is on (1) or off (0)
29	WDT1_INT_EN	An unmasked interrupt will enable the timer (1) or not (0)
28	WDT1_EN	Timer is enabled (1) or not (0)
27	RESERVED_BIT27	
26	WDT0_AUTOKICK	Auto-kicker is on (1) or off (0)
25	WDT0_INT_EN	An unmasked interrupt will enable the timer (1) or not (0)
24	WDT0_EN	Timer is enabled (1) or not (0)
23:20	RESERVED_BIT20_23	
19	GPT1_WR_PEND	Timer has a write pending (1) or not (0)
18	GPT1_CLR_PEND	Timer has a clear pending (1) or not (0)
17	GPT1_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
16	GPT1_EN	Timer is enabled (1) or not (0)
15:12	RESERVED_BITS15_12	
11	GPT0_WR_PEND	Timer has a write pending (1) or not (0)
10	GPT0_CLR_PEND	Timer has a clear pending (1) or not (0)
9	GPT0_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
8	GPT0_EN	Timer is enabled (1) or not (0)
7:4	RESERVED_BITS7_4	
3	DGT_WR_PEND	Timer has a write pending (1) or not (0)
2	DGT_CLR_PEND	Timer has a clear pending (1) or not (0)
1	DGT_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
0	DGT_EN	Timer is enabled (1) or not (0)

10.10 GSS A5 Wrapper SSBI Registers (0x10003000 GSS_A5_SSBI_BASE)

This section contains the Global Navigation Subsystem (GSS) A5 Wrapper SSBI registers.

10.10.1 Singlewire Serial Bus Interface (SSBI)

This section defines registers and tasks to configure and access SSBI Engine. All registers are AHB accessible.

NOTE All command register settings take effect immediately unless otherwise noted.

0x10003000 SSBI_ENABLE

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

This register provides clock enable for each SSBI master.

SSBI_ENABLE

Bits	Name	Description
31:1	RESERVED_BITS	
0	CLK_EN	Setting (1) enables clock for SSBI master

0x10003004 SSBI_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0F8001

SSBI control register. It specifies various generic control information.

SSBI_CTL

Bits	Name	Description
31:21	RESERVED_BITS_1	
20:17	WAKEUP_FINAL_CNT	This field specifies the number of idle clock cycles between wakeup pulse and actual read/write access to SSBI slave.
16	SSBI_DATA_PDEN	Pull down enable for SSBI_DATA pad.
15	RESERVED_BITS_2	
14	DISABLE_TERM_SYM	In FTM mode, set this bit to disable the termination symbol.

SSBI_CTL (cont.)

Bits	Name	Description
13:8	SLAVE_ID	In FTM mode, specifies the Slave ID.
7	FTM_MODE	Set this bit to force all the transfers to be in FTM mode.
6:5	SEL_RD_DATA	Safety feature to address routing delay Increase SEL_RD_DATA increase waiting cycles before getting the rd_data
4	ENABLE_SSBI_INT	When asserted, SSBI IRQ is generated when SSBI R/W through AHB is done
3:2	SSBI_DATA_DEL	Specifies the number of 1/2 clock periods, SSBI_DATA will be delayed before sampling.
1:0	IDLE_SYMS	The master ensures there are at least this number of idle symbol periods in between the accesses. For successive writes, this value can be 0x0. However if the following access is a read operation, then this value has to be greater then 0x0.

0x10003008 SSBI_RESET

Type: Command
Clock: AHB_CLK
Reset State: 0x0

SSBI_RESET

Bits	Name	Description
31:1	RESERVED_BITS	
0	RESET_REQ	Setting (1) this bit resets the SSBI master

0x1000300C SSBI_CMD

Type: Command
Clock: AHB_CLK
Reset State: 0x0

This register specifies the information to use for the transfer. For both reads and writes, SW must write to this register to initiate the transfer. The REG_DATA field is ignored for reads. For a read, once it has completed, read the data through SSBI_RD. Note that, if software initiates a read, it is expected that no subsequent access will be done until that data has been read from SSBI_RD. When this register is read, 0 is returned.

SSBI_CMD

Bits	Name	Description
31:28	RESERVED_BITS_1	

SSBI_CMD (cont.)

Bits	Name	Description
27	SEND_TERM_SYM	In FTM mode, writing 0x1 to this bit generates just the termination symbol without requesting for an access.
26	WAKEUP_SLAVE	When set(1), any following read or write transactions will first cause the ssbi_master_if block to send a single wakeup pulse to the slave. After WAKEUP_FINAL_CNT number of idle clocks, the read or write transaction begins. Setting this bit allows the SSBI slave to shut off its clock between transactions.
25	RESERVED_BIT	
24	RDWRN	Denotes whether the command to perform is a register write (0) or read (1).
23:16	REG_ADDR	Slave register address.
15:8	RESERVED_BITS_2	
7:0	REG_DATA	Write data for a slave register.

0x10003010 SSBI_BYPASS

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

This register allows software to override SSBI_DATA value. This provides a safety option to drive SSBI_DATA with different values in idle mode.

SSBI_BYPASS

Bits	Name	Description
31:2	RESERVED_BITS	
1	OVR_VALUE	When OVR_MODE is 1, this bit is driven onto SSBI_DATA. This is NOT intended to enable SW to bit-bang SSBI commands. Rather, this is a safety option in case a need arises to program this bit differently in idle mode.
0	OVR_MODE	Override mode bit. When set(1), the value driven onto SSBI_DATA is given by OVR_VALUE.

0x10003018 SSBI_RD

Type: Read
Clock: AHB_CLK
Reset State: 0x0

When reading a slave register, write to SSBI_CMD (REG_DATA is ignored). Once data is ready, read this register and it returns the read data from the slave and the other fields filled in correctly to match. Reading from this register may clear some bits in SSBI_STATUS. Note if software send the second read command to SSBI_CMD before reading the contents of this register after the 1st read command. All fields except REG_DATA may be invalid, and depending on the second access, REG_DATA may reflect the first read data or second read data.

SSBI_RD

Bits	Name	Description
31:26	RESERVED_BITS_1	
25	USE_ENABLE	Reflects how SSBI_CMD was written to initiate this read.
24	RDWRN	Reflects how SSBI_CMD was written to initiate this read.
23:16	REG_ADD	Reflects how SSBI_CMD was written to initiate this read.
15:8	RESERVED_BITS_2	
7:0	REG_DATA	Returned read register data.

0x1000301C SSBI_STATUS

Type: Read
Clock: AHB_CLK
Reset State: 0x0

Returns information about the internal status of the SSBI master. If software wants to perform an access, it should first ensure READY is 1. If software wants to wait until the transfer has completed, it can poll MCHN_BUSY. If software wants to know when read data has returned, it can poll RD_READY.

SSBI_STATUS

Bits	Name	Description
31:5	RESERVED_BITS	
4	SSBI_DATA_IN	Returns the instantaneous value of SSBI_DATA input. This is not affected by SSBI_CTL: SSBI_DATA_DEL. This is intended as a test feature.
3	RD_CLOBBERED	This bit gets set(1) if SW initiates another access (read or write) while a SSBI read is being performed. The result of this action is that all the fields except REG_DATA in SSBI_RD will be invalid. Reads from SSBI_RD clear this bit.
2	RD_READY	Normally clear(0). If a SSBI read is performed, this bit will be set upon read completion (DONE assertion). Reads from SSBI_RD clear this bit.

SSBI_STATUS (cont.)

Bits	Name	Description
1	READY	Indicates that the master can accept a new transfer request. When clear(0), further writes to SSBI_CMD should not be done since the previous access may be lost. This signal will be clear for the duration from REQ assertion until ACK assertion. It also remains clear following reset, until the time SW writes to SSBI_CTL register and resets SSBI_DATA_PDEN bit.
0	MCHN_BUSY	When set(1), indicates the SSBI master is actively performing a transfer. This signal will be set for the duration from REQ assertion until DONE assertion.

11 Krait MP Subsystem Registers

11.1 Overview

Table 11-1 KraitMP_Sub_System Bases

Base Name	Parent	Address
APCS_GICD_CTLR	APCS_QGIC2_BASE	0x02000000
APCS_GICH_HCR	APCS_QGIC2_BASE	0x02000000
APCS_GICC_CTLR	APCS_QGIC2_BASE	0x02000000
APCS_GICV_CTLR	APCS_QGIC2_BASE	0x02000000
APCS_ACCSECURE	APCS_ACC_BASE	0x02008000
APCS_SAW2_SECURE	APCS_SAW2_BASE	0x02009000
APCS_TMRSECURE	APCS_TMR_BASE	0x0200A000
APCS_GLBSECURE	APCS_GLB_BASE	0x02010000
APCS_GCCSECURE	APCS_GCC_BASE	0x02011000
APCS_L2_SAW2_SECURE	APCS_L2_GDHS_BASE	0x02012000
APCS_MPU_PRTn_RACR	APCS_L2_MPU_BASE	0x02013000
APCS_QGIC	APCS_HSEL_BASE	0x02100000
CPU0_APCS_ACCSECURE	CPU0_APCS_ACC_BASE	0x02088000
CPU0_APCS_SAW2_SECURE	CPU0_APCS_SAW2_BASE	0x02089000
CPU0_APCS_TMRSECURE	CPU0_APCS_TMR_BASE	0x0208A000
CPU1_APCS_ACCSECURE	CPU1_APCS_ACC_BASE	0x02098000
CPU1_APCS_SAW2_SECURE	CPU1_APCS_SAW2_BASE	0x02099000
CPU1_APCS_TMRSECURE	CPU1_APCS_TMR_BASE	0x0209A000
CPU2_APCS_ACCSECURE	CPU2_APCS_ACC_BASE	0x020A8000
CPU2_APCS_SAW2_SECURE	CPU2_APCS_SAW2_BASE	0x020A9000
CPU2_APCS_TMRSECURE	CPU2_APCS_TMR_BASE	0x020AA000
CPU3_APCS_ACCSECURE	CPU3_APCS_ACC_BASE	0x020B8000
CPU3_APCS_SAW2_SECURE	CPU3_APCS_SAW2_BASE	0x020B9000
CPU3_APCS_TMRSECURE	CPU3_APCS_TMR_BASE	0x020BA000
EXT_APCS_GLBSECURE	EXT_APCS_GLB_BASE	0x02090000
EXT_APCS_GCCSECURE	EXT_APCS_GCC_BASE	0x02091000

Table 11-1 KraitMP_Sub_System Bases (cont.)

Base Name	Parent	Address
EXT_APCS_L2_SAW2_SECURE	EXT_APCS_L2_GDHS_BASE	0x02092000
EXT_APCS_MPU_PRTn_RACR	EXT_APCS_L2_MPU_BASE	0x02093000

11.2 KPSS GIC2 GICD Registers (0x02000000 APCS_QGIC2_BASE)

This section contains the Krait Processor Subsystem (KPSS) GIC2 GICD registers.

The Generic Interrupt Controller 2 (GIC2) is a reusable configurable soft core. This GIC2 specification conforms to ARM's Generic Interrupt Controller architecture specification. Where differences exist, either additional features have been added or this document must change to conform to ARM's specified architecture. Where additional features were added, they will be clearly marked. The GIC2 design supports ARM's TrustZone architecture with two security zones: secure and non-secure.

The GIC2 is made of two parts: the Distributor and CPU Interfaces (up to eight). Each of these interfaces contains a CRIF slave interface. There must be at least one CPU Interface in the design.

In this manual, addresses are offsets from zero. When constants are exported, they are re-assigned to the appropriate base address.

Half-word and Byte access is supported by a subset of the registers.

Security treatment of registers in the GIC2 is divided into four types of registers. These are:

- "Common" indicates that both secure and non-secure software have full access to the register.
- "NS-int Dependent" indicates that state belonging to both secure and non-secure interrupts may be present in the register, depending on the value set in the Interrupt Security Register. Secure accesses to such a register are able to access all of the register's state, regardless of the Interrupt Security Register setting. Non-secure accesses may only access state belonging to non-secure interrupts. For non-secure accesses to state belonging to secure interrupts, writes are ignored and reads return zero.
- "Banked" indicates that the register exhibits different functionality according to whether it is accessed with a secure or non-secure request.
- "Restricted" indicates that only secure requests may access this register. If non-secure accesses are attempted, writes are ignored and reads return zero.

The type of register is specified for each register individual. Table 11-2 explains security treatment for register bits.

Table 11-2 Register security treatment

bus NS bit	SECURITY BIT	ALLOW Access
0	0	1
0	1	1
1	0	0
1	1	1

Glossary:

CPU Interface: That part of the GIC2 responsible for receiving the next interrupt from the Distributor and, if the interrupt has sufficient priority, asserting an interrupt indication to the CPU.

CPU MID: The Master ID of a CPU interface (as in AXI's AMID). The CPU MID reaching the Distributor must match the CPU Interface connected to that master.

Distributor: That part of the GIC2 responsible for detecting, disabling, prioritizing, and directing interrupts to CPU(s). The Distributor also accepts requests from and signals software interrupts to the CPU(s).

FABRIC: Flexible Advanced Buses & Reusable Interconnect Cores

NS-int: Security status of a particular interrupt ID. The value 0x0 is "secure", 0x1 is "non-secure".

NS-prot: Security status of the a bus transaction (read or write) according to the NS bit.

PPI: Private Peripheral Interrupt, interrupt from a peripheral whose interrupt line is destined to a particular CPU and can't be physically connected/directed to any other.

SGI: Software Generated Interrupt, interrupt from one CPU (or thread) to another.

SPI: Shared Peripheral Interrupt, interrupt from a peripheral whose interrupt line's CPU target is programmable to one or more CPU interface by the Distributor.

11.2.1 GIC2 Distributor

Table 11-3 GIC2 Distributor Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x0000	GICD_CTLR	RW	0x0	Banked	distributor control
0x0004	GICD_TYPER	R	Unknown	Common	distributor type
0x0008	GICD_IIDR	R	0x0000_1070	Common	distributor ID
0x0020	GICD_ANSACR	RW	0x0	Restricted	access control register
0x0024	GICD_CGCR	RW	0x0	Restricted	clock gate control register
0x0080 + 4n	GICD_ISR	RW	0x0	Restricted	distributor interrupt security
0x0100 + 4n	GICD_ISENABLER	RW	0x0	NS-int dependent	distributor interrupt set-enable
0x0180 + 4n	GICD_ICENABLER	RW	0x0	NS-int dependent	distributor interrupt clear-enable
0x0200 + 4n	GICD_ISPENDR	RW	0x0	NS-int dependent	distributor interrupt set-pending

Table 11-3 GIC2 Distributor Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x0280 + 4n	GICD_ICPENDR	RW	0x0	NS-int dependent	distributor interrupt clear-pending
0x0300 + 4n	GICD_ISACTIVER	R	0x0	NS-int dependent	distributor interrupt set-active
0x0380 + 4n	GICD_ICACTIVER	R	0x0	NS-int dependent	distributor interrupt clear-active
0x0400 + 4n	GICD_IPRIORITYR	RW	0x0	NS-int dependent	distributor interrupt priority
0x0800 + 4n	GICD_ITARGETSR	RW	0x0	NS-int dependent	distributor interrupt targets
0x0C00 + 4n	GICD_ICFGR	RW	0x5555_5555	NS-int dependent	distributor interrupt configuration
0x0D00-0x0EFF	Reserved				
0x0F00	GICD_SGIR	W	N/A	Banked	distributor software-generated interrupt
0x0F10-0xF1C	GICD_CPENDSGIR	W	N/A	Banked	SGI pend set
0x0F20-0xF2C	GICD_SPENDSGIR	W	N/A	Banked	SGI pend set
0x0FD0	GICD_PIDR0	R	0x0000_0090	Common	distributor peripheral ID
0x0FD4	GICD_PIDR1	R	0x0000_0003	Common	
0x0FD8	GICD_PIDR2	R	0x0000_002F	Common	
0x0FDC	GICD_PIDR3	R	0x0000_0000	Common	
0x0FE0	GICD_PIDR4	R	0x0000_0000	Common	
0x0FE4	GICD_PIDR5	R	0x0000_0000	Common	
0x0FE8	GICD_PIDR6	R	0x0000_0000	Common	
0x0FEC	GICD_PIDR7	R	0x0000_0000	Common	
0xFF0	GICD_CIDR0	R	0x0000_000D	Common	distributor component ID
0xFF4	GICD_CIDR1	R	0x0000_00F0	Common	
0xFF8	GICD_CIDR2	R	0x0000_0005	Common	
0xFFC	GICD_CIDR3	R	0x0000_00B1	Common	

11.2.1.1 GIC2 distributor registers

0x02000000 APCS_GICD_CTLR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICD_CTLR register controls if the Distributor responds to external interrupt stimulus changes.

Non-secure access: Distributor provides access to the enable_ns register in bit 0.

Secure access: Distributor provides access to the enable_s register in bit 0, and the enable_ns register in bit 1.

APCS_GICD_CTLR

Bits	Name	Description
31:2	RESERVED	
1	ENABLE_NS	This bit is an alias of the enable_ns bit. This bit is only usable by Secure software. 0x0: CLR 0x1: SET
0	ENABLE	This bit is the enable bit for both Secure and Non-secure software. Secure software accesses enable_s at this location. Non-secure software accesses enable_ns. 0x0: CLR 0x1: SET

0x02000004 APCS_GICD_TYPER

Type: Read
Clock: CLK
Reset State: Unknown

Security Treatment: Common

The GICD_TYPER register provides information about the configuration of the GIC2.

APCS_GICD_TYPER

Bits	Name	Description
31:16	RESERVED	

APCS_GICD_TYPER (cont.)

Bits	Name	Description
15:11	LSPI	Returns the number of Lockable Shared Peripheral Interrupts (LSPIs) that the GIC2 contains. GIC2 does not support lockable SPIs, always reads back 0x0.
10	TZ	TrustZone support. GIC2 supports TrustZone, always reads back 0x1.
9:8	RESERVED_BITS9_TO_8	
7:5	CPU_NUM	Returns the number of CPU interfaces that the generic interrupt controller provides. The generic interrupt controller provides either: 0b 000 = one CPU interface 0b 001 = two CPU interfaces 0b 010 = three CPU interfaces 0b 011 = four CPU interfaces 0b 100 = five CPU interfaces 0b 101 = six CPU interfaces 0b 110 = seven CPU interfaces 0b 111 = eight CPU interfaces.
4:0	IT_LINES	Returns the number of INTIDs, to the nearest 32, that the Distributor provides. Read as: 0b 00000 = the Distributor is configured for up to 32 INTIDs 0b 00001 = the Distributor is configured for up to 64 INTIDs 0b 00010 = the Distributor is configured for up to 96 INTIDs 0b 00011 = the Distributor is configured for up to 128 INTIDs . . . 0b 11110 = the Distributor is configured for up to 992 INTIDs 0b 11111 = the Distributor is configured for up to 1020 INTIDs.

0x02000008 APCS_GICD_IIDR

Type: Read
Clock: CLK
Reset State: 0x00001070

Security Treatment: Common

The GICD_IIDR register provides the implementor of the Distributor and the revision of the Distributor.

APCS_GICD_IIDR

Bits	Name	Description
31:24	RESERVED	

APCS_GICD_IIDR (cont.)

Bits	Name	Description
15:12	REVISION	Returns the revision number of the Distributor, 0x1
11:0	IMPLEMENTOR	Returns JEP106 ID number, 0b 01110000

0x02000020 APCS_GICD_ANSACR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Restricted

The auxiliary non-secure access control register (GICD_ANSACR) is used to control non-secure access to GICD_CGCR.

APCS_GICD_ANSACR

Bits	Name	Description
31:1	RESERVED	
0	GICD_CGCR	0x0: SEC (Dis-allows non-secure access.) 0x1: NS (Allows non-secure access.)

0x02000024 APCS_GICD_CGCR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Restricted

The clock gate control register (GICD_CGCR) is used to control localized clock gating over-ride logic. Setting bits in GICD_CGCR disables the corresponding local clock gating logic. The local clock gating logic normally turns off a local (small subset) clock tree automatically if there is no need for the clock. If any error is found in the gating logic, these bits can be used to over-ride it.

APCS_GICD_CGCR

Bits	Name	Description
31:17	RESERVED_31_TO_17	
16	TOP	Controls the top level clock gate (which gates entire GIC2). 0x1: DISABLE 0x0: ENABLE
15:4	RESERVED_15_TO_4	

APCS_GICD_CGCR (cont.)

Bits	Name	Description
3	DI_SGI_STATE	Controls the clock gate for Distributor interrupt state data base registers for SGI interrupts. 0x1: DISABLE 0x0: ENABLE
2	DI_PPI_SPI_STATE	Controls the clock gate for Distributor interrupt state data base registers for PPI and SPI interrupts. 0x1: DISABLE 0x0: ENABLE
1	DI_DEMET	Controls the clock gate for Distributor interrupt input demet registers. 0x1: DISABLE 0x0: ENABLE
0	DI_RD	Controls the clock gate for Distributor CRIF Read Data. 0x1: DISABLE 0x0: ENABLE

0x02000080+4*n APCS_GICD_ISRn, n=[0..8]

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Restricted

Each bit in an GICD_ISR register controls the security state of an interrupt, to be either secure or non-secure. You can only access these registers with secure read or secure write accesses.

NOTE The GICD_ISR register at address offset 0x0080 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

APCS_GICD_ISRn

Bits	Name	Description
31:0	INT_NS	0x0: SEC (Assigns INTID N to the Secure state.) 0x1: NS (Assigns INTID N to the Non-secure state.)

0x02000100+4*n APCS_GICD_ISENABLERn, n=[0..8]

Type: Write (command - readable)
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in an GICD_ISENABLER register controls the enabling of an interrupt.

Reading this register returns the currently enabled interrupts subject to NS-int dependent access rules.

NOTE The GICD_ISENABLER register at address offset 0x0100 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

APCS_GICD_ISENABLERn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ICENABLER register.) 0x1: SET (Enables INTID N.)

0x02000180+4*n APCS_GICD_ICENABLERn, n=[0..8]

Type: Write (command - readable)
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in an GICD_ICENABLER register controls the disabling of an interrupt.

Reading this register returns the currently enabled interrupts subject to NS-int dependent access rules.

NOTE The GICD_ICENABLER register at address offset 0x0180 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

APCS_GICD_ICENABLERn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ISENABLER register.) 0x1: CLR (Enables INTID N.)

0x02000200+4*n APCS_GICD_ISPENDRn, n=[0..8]

Type: Write (command - readable)
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in an GICD_ISPENDR register controls the enabling of an interrupt.

Reading this register returns the currently pending interrupts subject to NS-int dependent access rules.

NOTE The GICD_ISPENDR register at address offset 0x0200 is repeated once per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI interrupts. SGI interrupt bits are read-only, however the distributor updates these using the GICD_SGIR register. The remaining registers control the SPI interrupts.

APCS_GICD_ISPENDRn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ICPENDR register.) 0x1: SET (Sets INTID N to the Pending state.)

0x02000280+4*n APCS_GICD_ICPENDRn, n=[0..8]

Type: Write (command - readable)
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in an GICD_ICPENDR register controls the disabling of an interrupt.

Reading this register returns the currently pending interrupts subject to NS-int dependent access rules.

NOTE The GICD_ICPENDR register at address offset 0x0280 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI interrupts. SGI interrupt bits are read-only, however the distributor updates these using the GICD_SGIR register. The remaining registers control the SPI interrupts.

APCS_GICD_ICPENDRn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ISPENDR register.) 0x1: CLR (Clears INTID N. from the pending state.)

0x02000300+4*n APCS_GICD_ISACTIVERn, n=[0..8]

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in the GICD_ISACTIVER register provides the active status of an interrupt. Writing a 1 to any of these bits will transition the corresponding interrupt to the Active (or Active and Pending) state

NOTE The GICD_ISACTIVER register at address offset 0x0300 is repeated once per CPU Interface. It is only accessible from the designated CPU and provides information for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

APCS_GICD_ISACTIVERn

Bits	Name	Description
31:0	INT	0x0: DO NOTHING 0x1: SET

0x02000380+4*n APCS_GICD_ICACTIVERn, n=[0..8]

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in the GICD_ICACTIVER register provides the active status of an interrupt. Writing a 1 to any of these bits will transition the corresponding interrupt out of the Active (or Active and Pending) state

NOTE The GICD_ICACTIVER register at address offset 0x0300 is repeated once per CPU Interface. It is only accessible from the designated CPU and provides information for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

APCS_GICD_ICACTIVERn

Bits	Name	Description
31:0	INT	0x1: CLR 0x0: DO NOTHING

0x02000400+4*n APCS_GICD_IPRIORITYRn, n=[0..71]

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each field in the GICD_IPRIORITYR registers controls the priority level of an interrupt.

NOTE The GICD_IPRIORITYR registers at address offsets 0x0400 to 0x41C are repeated once per CPU Interface. These are only accessible from the designated CPU and control the priority levels for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupt priority levels.

NOTE This register is byte addressable.

The GICD_IPRIORITYR register behaves differently depending on the security setting of interrupt associated with the address written (NS-int) and the security of the bus transaction (NS-prot).

APCS_GICD_IPRIORITYRn

Bits	Name	Description
31:27	INT3	
26:24	RESERVED_1	
23:19	INT2	
18:16	RESERVED_2	
15:11	INT1	
10:8	RESERVED_3	
7:3	INT0	All bits cleared (0x0) is the highest priority. All bits set (5'b11111) is the lowest priority. For non-secure write access, the MSB is always set (1). For non-secure read access, the MSB is always clear (0). Non-secure entities can't use the highest priorities without secure software setting such a priority. The highest priorities are typically reserved for secure software. On the other hand, secure software can, if needed, write and read the MSB. Secure entities have access to all priorities. Secure interrupts can use priority numbers 5'b10000-5'b11111 (the lower half of the priority spectrum) if needed. Due to strict "less than" comparisons used in the CPU interface, setting an interrupt's priority to 5'b11111 effectively disables that interrupt. The number of priorities actually supported is 32. Software can determine this number by writing 0xFF and reading back the result.
2:0	RESERVED_4	

0x02000800+ 4*n APCS_GICD_ITARGETSRn, n=[0..71]

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each field in the GICD_ITARGETSR registers controls the destination CPU(s) of an interrupt.

NOTE The GICD_ITARGETSR registers at address offsets 0x0800 to 0x81C are not actually implemented. These are place holders PPI and SGI interrupts. PPI interrupts, being private, only have one destination CPU. SGI interrupts are generated by the GIC2_DI_SOFT_INT register only. The remaining registers control the SPI interrupt destinations.

NOTE This register is byte addressable.

APCS_GICD_ITARGETSRn

Bits	Name	Description
31:24	INT3	
23:16	INT2	
15:8	INT1	
7:0	INT0	Each bit represents one of 8 CPUs. Bit 0 represents the zeroth CPU, bit 7 represents the seventh CPU. Setting this field to 0 will disable the interrupt as no CPU will see it set. For INTIDs < 32 (the SGI and PPI), reads return the bit corresponding to the CPU performing the read (ie CPU 0 reads back 0x01010101). Writes are ignored. The number of CPUs actually supported is determined by NUM_CPU generic. Software can determine this number by writing 0xFF and reading back the result.

0x02000C00+ 4*n APCS_GICD_ICFGRn, n=[0..17]

Type: Read/write
Clock: CLK
Reset State: 0x55555555

Security Treatment: NS-int dependent

Each field in the GICD_ICFGR registers allows:

- control of type of an SPI:
- level-sensitive

- edge-sensitive
- reading the type of PPIs and SGIs

NOTE The GICD_ICFGR registers at address offsets 0x0C00 to 0xC04 are repeated once per CPU Interface. These are only accessible from the designated CPU and allow read access for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

NOTE PPI(0) is the maintenance interrupt and must be configured as level type.

NOTE This register is not byte addressable, interrupts should be disabled before configuring their type.

NOTE Reset state for GICD_ICFGR0 is 0xaaaaaaaa.

APCS_GICD_ICFGRn

Bits	Name	Description
31:30	INT15	
29:28	INT14	
27:26	INT13	
25:24	INT12	
23:22	INT11	
21:20	INT10	
19:18	INT9	
17:16	INT8	
15:14	INT7	
13:12	INT6	
11:10	INT5	
9:8	INT4	
7:6	INT3	
5:4	INT2	
3:2	INT1	

APCS_GICD_ICFGRn (cont.)

Bits	Name	Description
1:0	INT0	These bits behave differently for each of the three interrupt types as follows: ' For SGI, read back as 0b10 - SGI interrupts are edge-sensitive and use the N-N model. ' For PPI/SPI, read/writable as 0b01 or 0b11 - PPI/SPI interrupts can be edge or level sensitive and use the 1-N model. 0x0: LVL N to N 0x1: LVL 1 to N 0x2: EDGE N to N 0x3: EDGE 1 to N

0x02000F00 APCS_GICD_SGIR

Type: Write (command)
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICD_SGIR register provides the method by which software may cause interrupts to become pending for designated target CPU(s). The GIC2 maintains an internal database of all outstanding software interrupt requests pended to each CPU Interface and rotates through them in Round Robin fashion. Signaling the same interrupt a second time before it is serviced will result in only one interrupt from the source CPU to the target CPU(s).

Table 11-4 Security status

Security status of the write event to the GICD_SGIR register (the state of the NS bit)	SATT Value	Interrupt's security status as set by GICD_ISR	Requested Interrupt set as pending on the target CPU
Secure	0	Secure	YES
Secure	0	Non-secure	NO
Secure	1	Secure	NO
Secure	1	Non-secure	YES
Non-secure	X	Secure	NO
Non-secure	X	Non-secure	YES

APCS_GICD_SGIR

Bits	Name	Description
31:26	RESERVED_BITS31_TO_26	

APCS_GICD_SGIR (cont.)

Bits	Name	Description
25:24	T_FILTER	Target Filter 0x0: LIST (Use the T_LIST as is) 0x1: OTHERS (Send to all CPUs except the CPU MID making the request, ignoring T_LIST) 0x2: MID (Send to only the CPU MID making the request, ignoring T_LIST) 0x3: NA (Reserved)
23:16	T_LIST	Target List. Each bit set represents a CPU target for the INT_ID, subject to the T_FILTER field. 0x1: CPU0 0x2: CPU1 0x4: CPU2 0x8: CPU3 0x10: CPU4 0x20: CPU5 0x40: CPU6 0x80: CPU7
15	SATT	Security ATTribute. This bit is only programmable by secure Software. See 0x0: SECURE (Secure interrupt is issued) 0x1: NONSECURE (Non-secure interrupt is issued.)
14:4	RESERVED_BITS14_TO_4	
3:0	INT_ID	The INT ID number (0-15) of the SGI to be set as pending. See the SGI pending truth table for security status Table 11-4 (SATT vs. NS-prot) for information on the conditions that allow an SGI to be set pending.

0x02000F10+4*n APCS_GICD_CPENDSGIRn, n=[0..3]

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

Each field in the GICD_CPENDSGIR register, when written as 1, clears the corresponding pending bit of the source CPU for the corresponding SGI.

NOTE If the SGI is marked secure, only a secure access can access that SGI's pending bits.

NOTE This register is byte addressable.

APCS_GICD_CPENDSGIRn

Bits	Name	Description
31:24	SGI3	
23:16	SGI2	
15:8	SGI1	
7:0	SGI0	Each bit represents one of 8 CPUs. Bit 0 represents the zeroth CPU, bit 7 represents the seventh CPU. Writing a 1 to any bit clears the pending status bit from the CPU to the SGI.

0x02000F20+4*n APCS_GICD_SPENDSGIRn, n=[0..3]

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

Each field in the GICD_SPENDSGIR register, when written as 1, sets the corresponding pending bit of the source CPU for the corresponding SGI.

NOTE If the SGI is marked secure, only a secure access can access that SGI's pending bits.

NOTE This register is byte addressable.

APCS_GICD_SPENDSGIRn

Bits	Name	Description
31:24	SGI3	
23:16	SGI2	
15:8	SGI1	
7:0	SGI0	Each bit represents one of 8 CPUs. Bit 0 represents the zeroth CPU, bit 7 represents the seventh CPU. Writing a 1 to any bit sets the pending status bit from the CPU to the SGI.

0x02000FD0 APCS_GICD_PIDR0

Type: Read
Clock: CLK
Reset State: 0x00000090

Security Treatment: Common

The GICD_PIDR0 provides access to GIC2 peripheral identification.

APCS_GICD_PIDR0

Bits	Name	Description
31:8	RESERVED	
7:0	PART_NUM	Returns lower byte of the GIC2 part number 0xB390, 0x90

0x02000FD4 APCS_GICD_PIDR1

Type: Read
Clock: CLK
Reset State: 0x00000003

Security Treatment: Common

The GICD_PIDR1 provides access to GIC2 peripheral identification.

APCS_GICD_PIDR1

Bits	Name	Description
31:8	RESERVED	
7:4	DESIGNER	Returns JEDEC JEP code bits 3:0, 0x0.
3:0	PART_NUM	Returns upper nibble of the GIC2 part number 0x390, 0x3

0x02000FD8 APCS_GICD_PIDR2

Type: Read
Clock: CLK
Reset State: 0x0000002F

Security Treatment: Common

The GICD_PIDR2 provides access to GIC2 peripheral identification.

APCS_GICD_PIDR2

Bits	Name	Description
31:8	RESERVED	
7:4	ARCH_VERSION	Returns the GIC2's architecture revision number, 0x2
3	USES_JEP_CODE	Reads 0x1.
2:0	DESIGNER	Returns JEDEC JEP code bits 6:4, 0x7.

0x02000FDC APCS_GICD_PIDR3

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR3 provides access to GIC2 peripheral identification.

APCS_GICD_PIDR3

Bits	Name	Description
31:0	RESERVED_1	
7:4	REVISION	Returns 0x0.
3:0	RESERVED_2	ARM defined field.

0x02000FE0 APCS_GICD_PIDR4

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR4 provides access to GIC2 peripheral identification.

APCS_GICD_PIDR4

Bits	Name	Description
31:8	RESERVED_1	
7:4	RESERVED_2	ARM defined field.
3:0	DESIGNER	JEDEC JEP code bits 10:7, 0x0

0x02000FE4 APCS_GICD_PIDR5

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR5 provides access to GIC2 peripheral identification.

APCS_GICD_PIDR5

Bits	Name	Description
31:0	RESERVED	

0x02000FE8 APCS_GICD_PIDR6

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR6 provides access to GIC2 peripheral identification.

APCS_GICD_PIDR6

Bits	Name	Description
31:0	RESERVED	

0x02000FEC APCS_GICD_PIDR7

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR7 provides access to GIC2 peripheral identification.

APCS_GICD_PIDR7

Bits	Name	Description
31:0	RESERVED	

0x02000FF0 APCS_GICD_CIDR0

Type: Read
Clock: CLK
Reset State: 0x0000000D

Security Treatment: Common

The GICD_CIDR0 provides access to GIC2 component identification.

APCS_GICD_CIDR0

Bits	Name	Description
31:8	RESERVED	
7:0	COMP_ID_0	Reads back as 0x0D.

0x02000FF4 APCS_GICD_CIDR1

Type: Read
Clock: CLK
Reset State: 0x000000F0

Security Treatment: Common

The GICD_CIDR1 provides access to GIC2 component identification.

APCS_GICD_CIDR1

Bits	Name	Description
31:8	RESERVED	
7:0	COMP_ID_1	Reads back as 0xF0.

0x02000FF8 APCS_GICD_CIDR2

Type: Read
Clock: CLK
Reset State: 0x00000005

Security Treatment: Common

The GICD_CIDR2 provides access to GIC2 component identification.

APCS_GICD_CIDR2

Bits	Name	Description
31:8	RESERVED	
7:0	COMP_ID_2	Reads back as 0x05.

0x02000FFC APCS_GICD_CIDR3

Type: Read
Clock: CLK
Reset State: 0x000000B1

Security Treatment: Common

The GICD_CIDR3 provides access to GIC2 component identification.

APCS_GICD_CIDR3

Bits	Name	Description
31:8	RESERVED	
7:0	COMP_ID_3	Reads back as 0xB1.

11.3 KPSS GIC2 GICH Registers (0x02000000 APCS_QGIC2_BASE)

This section contains the Krait Processor Subsystem (KPSS) GIC2 GICH registers.

The Generic Interrupt Controller 2 (GIC2) is a reusable configurable soft core. This GIC2 specification conforms to ARM's Generic Interrupt Controller architecture specification. Where differences exist, either additional features have been added or this document must change to conform to ARM's specified architecture. Where additional features were added, they will be clearly. The GIC2 design supports ARM's TrustZone architecture, with two security zones: secure and non-secure.

The GIC2 is made of two parts: the Distributor and up to eight CPU Interfaces. Each of these interfaces contains a CRIF slave interface. There must be at least one CPU Interface in the design.

In this manual, addresses are offsets from zero. When constants are exported, they are re-assigned to the appropriate base address.

Half-word and Byte access is supported by a subset of the registers.

Security treatment of registers in the GIC2 is divided into four types of registers. These are:

- "Common" indicates that both secure and non-secure software have full access to the register.
- "NS-int Dependent" indicates that state belonging to both secure and non-secure interrupts may be present in the register, depending on the value set in the Interrupt Security Register. Secure accesses to such a register are able to access all of the register's state, regardless of the Interrupt Security Register setting. Non-secure accesses may only access state belonging to non-secure interrupts. For non-secure accesses to state belonging to secure interrupts, writes are ignored and reads return zero.
- "Banked" indicates that the register exhibits different functionality according to whether it is accessed with a secure or non-secure request.
- "Restricted" indicates that only secure requests may access this register. If non-secure accesses are attempted, writes are ignored and reads return zero.

The type of register is specified for each register individual. Table 11-5 explains security treatment for register bits.

Table 11-5 Register security treatment

bus NS bit	SECURITY BIT	ALLOW Access
0	0	1
0	1	1
1	0	0
1	1	1

Glossary:

CPU Interface: That part of the GIC2 responsible for receiving the next interrupt from the Distributor and, if the interrupt has sufficient priority, asserting an interrupt indication to the CPU.

CPU MID: The Master ID of a CPU interface (as in AXI's AMID). The CPU MID reaching the Distributor must match the CPU Interface connected to that master.

Distributor: That part of the GIC2 responsible for detecting, disabling, prioritizing, and directing interrupts to CPU(s). The Distributor also accepts requests from and signals software interrupts to the CPU(s).

FABRIC: Flexible Advanced Buses & Reusable Interconnect Cores

NS-int: Security status of a particular interrupt ID. The value 0x0 is "secure", 0x1 is "non-secure".

NS-prot: Security status of the a bus transaction (read or write) according to the NS bit.

PPI: Private Peripheral Interrupt, interrupt from a peripheral whose interrupt line is destined to a particular CPU and can't be physically connected/directed to any other.

SGI: Software Generated Interrupt, interrupt from one CPU (or thread) to another.

SPI: Shared Peripheral Interrupt, interrupt from a peripheral whose interrupt line's CPU target is programmable to one or more CPU interface by the Distributor.

11.3.1 QGIC2 Hypervisor Interface

Table 11-6 QGIC2 Hypervisor Interface Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x1000	GICH_HCR	RW	0x0000_0000	Common	general Hypervisor control
0x1004	GICH_VTR	R	0x9000_0003	Common	Hypervisor implementation - type register
0x1008	GICH_VMCR	R/W	0x004C_0000	Common	virtual machine control register
0x1010	GICH_MISR	R	0x0000_0000	Common	Maintenance interrupt syndrome
0x1020	GICH_EISR	R	0x0000_0000	Common	List registers' EOI status
0x1030	GICH_ELRSR	R	0x0000_000F	Common	List registers' empty status
0x10F0	GICH_APR	R/W	0x0000_0000	Common	Active Priority in Hypervisor
0x1100 + 4n	GICH_LRn	R/W	0x0000_0000	Common	List registers

11.3.2 QGIC2 Hypervisor interface registers

0x02001000 APCS_GICH_HCR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICH_HCR configures the GIC2 Hypervisor interface.

APCS_GICH_HCR

Bits	Name	Description
31:27	EOICOUNT	Counts the number of EOIs which have been received without a corresponding entry being found among the list registers. Incremented automatically by the CPU Interface when such an EOI is received. EOIs which do not clear a bit in the Active Priorities register do not cause an increment. The maintenance interrupt is asserted whenever this field is non-zero and the SKIDIE bit is set (see below).
26:8	RESERVED	
7	VDG1IE	If this bit is set, the maintenance interrupt will be asserted whenever the GICV_CTLR[EnableG1] is cleared. 0x0: CLR 0x1: SET
6	VEG1IE	If this bit is set, the maintenance interrupt will be asserted whenever the GICV_CTLR[EnableG1] is set. 0x0: CLR 0x1: SET
5	VDG0IE	If this bit is set, the maintenance interrupt will be asserted whenever the GICV_CTLR[EnalbeG0] is cleared. 0x0: CLR 0x1: SET
4	VEG0IE	If this bit is set, the maintenance interrupt will be asserted whenever the GICV_CTLR[EnableG0] is set. 0x0: CLR 0x1: SET
3	NPIE	No Pending Interrupt Maintenance Interrupt Enable. If this bit is set, the maintenance interrupt will be asserted whenever no list registers contain an interrupt in PENDING state. 0x0: CLR 0x1: SET

APCS_GICH_HCR (cont.)

Bits	Name	Description
2	SKIDIE	SKID Maintenance Interrupt Enable. If this bit is set, the maintenance interrupt will be asserted whenever GICH_HCR[EOICount] is non-zero. 0x0: CLR 0x1: SET
1	UIE	Underflow Maintenance Interrupt Enable. If this bit is set, the maintenance interrupt will be asserted whenever zero or one of the list entries are marked as valid. 0x0: CLR 0x1: SET
0	EN	Enable or Disable maintenance and by proxy Virtual CPU interface Interrupts 0x0: CLR 0x1: SET

0x02001004 APCS_GICH_VTR

Type: Read
Clock: CLK
Reset State: 0x90000003

Security Treatment: Common

The GICH_VTR provides information about the configuration of the Hypervisor Interface (virtual generic interrupt controller type register).

APCS_GICH_VTR

Bits	Name	Description
31:29	PRIBITS	Indicates the number of priority bits implemented, minus one. For this version of the specification the only acceptable value is 100, indicating 5 bits of priority (32 levels)
28:26	PREBITS	Indicates the number of preemption bits implemented, minus one. For this version of the specification the only acceptable value is 100, indicating 5 bits of preemption (32 levels)
25:6	RESERVED	
5:0	LISTREGS	Indicates the number of implemented List Registers, minus one. GIC2 has 4 list registers. This is set to 0x3

0x02001008 APCS_GICH_VMCR

Type: Read/write
Clock: CLK
Reset State: 0x004C0000

Security Treatment: Common

The GICH_VMCR contains read/write aliases of all the Virtual Machine accessible state (aliases from the GICV_* registers). This alias allows the Hypervisor to easily save and restore this state with a single read or write, and without needing to map in the Virtual Machine registers.

NOTE Various bits of this register include the terms group 0 or group 1in their names. This is purely for compatibility with the physical generic interrupt controller interface and does not pertain to actual TrustZone security.

APCS_GICH_VMCR

Bits	Name	Description
31:27	VMPMR	Alias of the GICV_PMR bits 7:3 in GICV
26:24	RESERVED_1	
23:21	VMG0BP	Alias of the group0 GICV_BPR bit in GICV
20:18	VMG1BP	Alias of the group1 GICV_ABPR bit in GICV
17:10	RESERVED_2	
9	VEM	Alias of the GICV_CTLR[EOIMode] bit in GICV
8:5	RESERVED	
4	VMGBPR	Alias of the GICV_CTLR[GBPR] bit in GICV
3	VMFIQEN	Alias of the GICV_CTLR[FIQen] bit in GICV.
2	VMACKCTL	Alias of the GICV_CTLR[ActCtl] bit in GICV.
1	VMENABLE_G1	Alias of the GICV_CTLR[ENABLE_G1] bit in GICV.
0	VMENABLE_G0	Alias of the GICV_CTLR[ENABLE_G0] bit in GICV.

0x02001010 APCS_GICH_MISR

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICH_MISR is the Maintenance interrupt syndrome register in the Hypervisor Interface. This register indicates which Maintenance Interrupts are currently asserted. This takes into account the individual Maintenance Interrupt Enable bits in GICH_HCR. However, the global enable in

GICH_HCR (EN) is not factored in to these bits. Therefore the maintenance interrupt is asserted if and only if at least one bit is set in this register and the EN bit in GICH_HCR is set.

APCS_GICH_MISR

Bits	Name	Description
31:8	RESERVED	
7	VDNSI	
6	VENSI	
5	VDSI	
4	VESI	
3	NPI	
2	SKIDI	
1	UI	
0	EI	

0x02001020 APCS_GICH_EISR

Type: Read
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICH_EISR provides EOI interrupt status in the Hypervisor Interface - which Software interrupts in the LRn registers that have EI set and are currently in the Invalid state.

APCS_GICH_EISR

Bits	Name	Description
25:5	RESERVED	
3:0	LR	0x0: NOT_EOI 0x1: EOI

0x02001030 APCS_GICH_ELRSR

Type: Read
Clock: CLK
Reset State: 0x0000000F

Security Treatment: Common

The GICH_ELRSR provides Empty List Register Status in the Hypervisor Interface.

APCS_GICH_ELRSR

Bits	Name	Description
31:5	RESERVED	
3:0	LR	0x0: NOT EMPTY 0x1: EMPTY

0x020010F0 APCS_GICH_APR

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICH_APR provides information about the priorities currently active in the Hypervisor Interface.

APCS_GICH_APR

Bits	Name	Description
31:0	PRI	0x0: INACTIVE 0x1: ACTIVE

0x02001100+4*n APCS_GICH_LRn, n=[0..3]

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICH_LRn provides access to each of the list registers in the Hypervisor Interface.

APCS_GICH_LRn

Bits	Name	Description
31	HW	Indicates that this is a Hardware interrupt. When this bit is set, bits 19:10 contain the Physical interrupt number, and when this interrupt is subject to an EOI request, a Deactivate Interrupt request will be sent to the Interrupt Distributor.

APCS_GICH_LRn (cont.)

Bits	Name	Description
30	GRP	Indicates that this interrupt should be treated as Group1. This means that the interrupt will present as an IRQ if GICV_CTLR[EnableG1] bit is set. If the GRP bit is clear, the interrupt is put into Group0 and will present as either IRQ or FIQ depending on the setting of the GICV_CTLR[FIQen] but only if GICV_CTLR[EnableG0] bit is also set. This bit is also used with GICV_CTLR[CBPR] to determine which Binary Point register is used in GICV for preemption calculations.
29:28	STATE	**NOTE** For hardware interrupts, the PENDING+ACTIVE state is held in the physical Distributor rather than the VCPUIF. The PENDING+ACTIVE state (11) should only be used for software originated interrupts (Virtual Devices) or SGIs. 0x0: IDL (INVALID) 0x1: PNA (PENDING, NOT ACTIVE) 0x2: A (ACTIVE) 0x3: PA (PENDING and ACTIVE)
27:23	PRI	Indicates the priority of this interrupt. This is converted to a traditional 8-bit generic interrupt controller priority value by appending three zero bits.
22:20	RESERVED	
19:10	PHY_ID	The physical ID of the interrupt (which SGI/PPI/SPI is it'). When the HW bit is set this field indicates the physical interrupt ID, which is forwarded to the Distributor when this interrupt is subject to an EOI request. See below for details when the HW bit is clear. If the Physical ID is between 16 and 31 inclusive (PPI space), the Deactivation will apply to the PPI associated with the same physical CPU as the VCPUIF making the request. If the Physical ID is between 0 and 15 inclusive (SGI space), the Deactivation will still apply to SGI associated with the same physical CPU as the VCPUIF making the request but it is expected that the HW bit and Physical ID will NOT be used for SGIs.
9:0	VIRTL_ID	Indicates the Virtual ID. This ID is returned to the Guest OS when this interrupt is acknowledged via the GICV_IAR (Interrupt Acknowledge register).

0x02001120 APCS_GICH_SW_LR

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

This register is not a real physical register or address in the design. It is placed here in the Software Manual to describe the alternate meanings for bits 19:10 in the LRn registers. Adding it here allows SW to pick up defines for these alternate meanings and use them in LRn accesses.

The HW uses these alternate definitions when bit 31 (HW) is set to 0 - indicating a (a pure virtual interrupt) written directly to this Hypervisor interface or an interrupt generated due to an SGI that originated in the Distributor. Bits 31:20 and 9:0 retain the normal GICH_LRn meanings.

APCS_GICH_SW_LR

Bits	Name	Description
19	EI	Indicates that this interrupt should trigger an EOI Interrupt. When this bit is set, a maintenance interrupt will be asserted whenever this interrupt becomes INVALID.
18:13	RESERVED	
12:10	CPUID	If this interrupt is an SGI, indicates the requesting CPU ID. This will appear in the relevant field of the VM Interrupt Acknowledge register. If the interrupt is not an SGI, software must set this field to 0.

11.4 KPSS GIC2 GICC Registers (0x02000000 APCS_QGIC2_BASE)

This section contains the Krait Processor Subsystem (KPSS) GIC2 GICC registers.

The Generic Interrupt Controller 2 (QGIC2) is a re-usable configurable soft core. This GIC2 specification conforms to ARM's Generic Interrupt Controller architecture specification. Where differences exist, either additional features were added or this document must change to conform to ARM's specified architecture. Where additional features were added, they will be clearly marked. The GIC2 design supports ARM's TrustZone architecture, with two security zones: secure and non-secure.

The GIC2 is made of two parts: the Distributor and CPU Interfaces (up to eight). Each of these interfaces contains a CRIF slave interface. There must be at least one CPU Interface in the design.

In this manual, addresses are offsets from zero. When constants are exported, they are re-assigned to the appropriate base address.

Half-word and Byte access is supported by a subset of the registers.

Security treatment of registers in the GIC2 is divided into four types of registers. These are:

- "Common" indicates that both secure and non-secure software have full access to the register.
- "NS-int Dependent" indicates that state belonging to both secure and non-secure interrupts may be present in the register, depending on the value set in the Interrupt Security Register. Secure accesses to such a register are able to access all of the register's state, regardless of the Interrupt Security Register setting. Non-secure accesses may only access state belonging to non-secure interrupts. For non-secure accesses to state belonging to secure interrupts, writes are ignored and reads return zero.
- "Banked" indicates that the register exhibits different functionality according to whether it is accessed with a secure or non-secure request.
- "Restricted" indicates that only secure requests may access this register. If non-secure accesses are attempted, writes are ignored and reads return zero.

The type of register is specified for each register individual. Table 11-7 explains security treatment for register bits.

Table 11-7 Register security treatment

bus NS bit	SECURITY BIT	ALLOW Access
0	0	1
0	1	1
1	0	0
1	1	1

Glossary:

CPU Interface: That part of the GIC2 responsible for receiving the next interrupt from the Distributor and, if the interrupt has sufficient priority, asserting an interrupt indication to the CPU.

CPU MID: The Master ID of a CPU interface (as in AXI's AMID). The CPU MID reaching the Distributor must match the CPU Interface connected to that master.

Distributor: That part of the GIC2 responsible for detecting, disabling, prioritizing, and directing interrupts to CPU(s). The Distributor also accepts requests from and signals software interrupts to the CPU(s).

FABRIC: Flexible Advanced Buses & Reusable Interconnect Cores

NS-int: Security status of a particular interrupt ID. The value 0x0 is "secure", 0x1 is "non-secure".

NS-prot: Security status of the a bus transaction (read or write) according to the NS bit.

PPI: Private Peripheral Interrupt, interrupt from a peripheral whose interrupt line is destined to a particular CPU and can't be physically connected/directed to any other.

SGI: Software Generated Interrupt, interrupt from one CPU (or thread) to another.

SPI: Shared Peripheral Interrupt, interrupt from a peripheral whose interrupt line's CPU target is programmable to one or more CPU interface by the Distributor.

11.4.1 QGIC2 CPU Interface

Table 11-8 QGIC2 CPU Interface Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x2000	GICC_CTLR	RW	0x0000_0000	Banked	control register
0x2004	GICC_PMR	RW	0x0000_0000	Banked	priority mask
0x2008	GICC_BPR	RW	0x0000_0002	Banked	binary point
0x200C	GICC_IAR	R (CMD)	0x0000_03ff	Banked	interrupt acknowledge
0x2010	GICC_EOIR	W (CMD)		Banked	end-of-interrupt
0x2014	GICC_RPR	R	0x0000_00F8	Banked	running priority
0x2018	GICC_HPPIR	R	0x0000_03FF	Banked	highest priority pending
0x201C	GICC_ABPR	RW	0x0000_0003	Restricted	aliased binary point
0x2020	GICC_AIAR	R (CMD)	0x0000_03FF	Restricted	aliased interrupt acknowledge
0x2024	GICC_AEOIR	W(CMD)		Restricted	aliased end of interrupt
0x2028	GICC_AHPPIR	R	0x0000_03FF	Restricted	aliased highest priority pending

Table 11-8 QGIC2 CPU Interface Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x202C-0x20CC	Reserved				
0x20D0-0x20DC	GICC_APR	RW	0x0000_0000	Banked	Active Priorities
0x20E0-0x20EC	GICC_NSAPR	RW	0x0000_0000	Secure	aliased non-secure Active Priorities
0x20F0-0x2F8	Reserved				
0x20FC	GICC_IIDR	R	0x0002_0070	Common	ID
0x2100-0x2FFC	Reserved				
0x3000	GICC_DIR	W		Banked	Deactivate Interrupt

11.4.2 QGIC2 CPU interface registers

0x02002000 APCS_GICC_CTLR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_CTLR configures the GIC2 CPU interface.

Non-secure access: Access is granted only to bits 0, 5,6 and 9.

Secure access: Access is granted to all register bits. Non-secure bits 0,5,6, and 9 are aliased into bits 1, 7, 8, and 10 for access by secure software.Modifying these aliased bits will modify the non-secure settings. Bits 0, 5, 6, 9 are physically banked into Secure and Non-secure space.

APCS_GICC_CTLR

Bits	Name	Description
31:11	RESERVED	
10	EOIMODENS	For secure software, a read/writable alias of Non-Secure EOImode.

APCS_GICC_CTLR (cont.)

Bits	Name	Description
9	EOIMODE	For secure software, controls the behavior of secure access to GICC_EOI and GICC_DIR. For non-secure software, controls the behavior of non-secure access to GICC_EOI and GICC_DIR. 0x0: PD_AND_DI (Both Priority Drop and Deactivate Interrupt, GICC_DIR does not function) 0x1: PD (GICC_EOI performs Priority Drop, GICC_DIR performs deactivate interrupt function)
8	IRQBYPDISABLENS	For secure software, a read/writable alias of Non-secure version of IRQBypDisable.
7	FIQBYPDISABLENS	For secure software, a read/writable alias of Non-secure version of FIQBypDisable
6	IRQBYPDISABLE	For Non-secure software, when CPU Interface is disabled, prevents the legacy bypass IRQ signal from being forwarded to the CPU (if IRQ is under Non-secure control). For secure software, prevents bypass if FIQ is under secure control. 0x0: CLR 0x1: SET
5	FIQBYPDISABLE	For Non-secure software, when CPU Interface is disabled, prevents the legacy bypass FIQ signal from being forwarded to the CPU (if FIQ is under Non-secure control). For secure software, prevents bypass if FIQ is under secure control. 0x0: CLR 0x1: SET
4	SBPR	Controls which binary point register is used to calculate preemption. 0x0: BANKED (secure interrupts use the secure Binary Point Register, non-secure interrupts use the non-secure Binary Point Register) 0x1: RESTRICTED (all interrupts use the secure Binary Point Register)
3	S_DEST	Controls destination of secure interrupts. 0x0: IRQ 0x1: FIQ

APCS_GICC_CTLR (cont.)

Bits	Name	Description
2	ACKCTL	Controls the side effect behavior of a secure read request to the Interrupt Acknowledge Register in the case where the highest priority pending interrupt is non-secure. If AckCtl is set to 0, a secure read request to the Interrupt Acknowledge Register returns an Interrupt ID value of 1022, and the read request does not cause the interrupt to be acknowledged (that is the Pending status of the interrupt remains unchanged). If AckCtl is set to 1, a secure read request to the Interrupt Acknowledge Register returns the Interrupt ID value of the non-secure interrupt, and causes the interrupt to be acknowledged (that is the interrupt becomes Active, or Active and Pending). 0x0: DISABLE ACK OF NS PENDING 0x1: ENABLE ACK OF NS PENDING
1	ENABLE_NS	For secure software, a read/writable alias of non secure software's enable bit (bit 0 of this same register in non secure space). 0x0: CLR 0x1: SET
0	ENABLE	For non-secure software, this bit enables/disables non secure interrupts. For secure software, this bit enables/disables secure interrupts. 0x0: CLR 0x1: SET

0x02002004 APCS_GICC_PMR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_PMR register configures the GIC2 CPU interface Priority Mask. The Priority Mask can be used to limit the interrupts that can cause an interrupt request to the CPU based on priority levels.

Non-secure access: Write access is granted only if bit 7 is 0x1, writes are ignored otherwise. Reads are always granted, however, bit 7 is always set in the data returned. Bit 0 is always zero.

Secure access: Access is granted to all register bits.

APCS_GICC_PMR

Bits	Name	Description
31:8	RESERVED_1	
7:3	LEVEL	Set the Priority Mask Level. The CPU interface asserts an interrupt request to CPU if the priority of the highest Pending interrupt sent by the interrupt Distributor is strictly higher than at least the mask set in Priority Mask Register.
2:0	RESERVED_2	

0x02002008 APCS_GICC_BPR

Type: Read/write
Clock: CLK
Reset State: 0x00000002

Security Treatment: Banked

The GICC_BPR register configures the GIC2 CPU interface Binary Point. The Binary Point is used to limit interrupts that can cause an interrupt request to the CPU based on the interrupt's priority and the interrupt priority that is currently being serviced by the CPU (if there is one). If the CPU is not servicing an interrupt, the Binary Point register is not used.

Non-secure access: Provides access to the non-secure Binary Point register.

Secure access: Provides access to the secure Binary Point register.
Secure software may access the non-secure Binary Point register at offset 0x001C.

Table 11-9 Interpretation of Binary Point Register value

register value	Priority bits used to determine preemption for secure interrupts.	Priority bits used to determine preemption for non-secure interrupts. (Bit 7 is always 0x1)
0	7:1	7:0
1	7:2	7:1
2	7:3	7:2
3	7:4	7:3
4	7:5	7:4
5	7:6	7:5
6	7	7:6
7	No preemption	No preemption

APCS_GICC_BPR

Bits	Name	Description
31:3	RESERVED	
2:0	VAL	The VAL setting is used to determine the priority bits used for preemption according to Table 11-9.

0x0200200C APCS_GICC_IAR

Type: Read (Command)
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Banked

The GICC_IAR register is used by the CPU to obtain the ID of the interrupt which caused the assertion if IRQn or FIQn.

Performing this read has the side effect of causing the Distributor to change the interrupt from the Pending state to the Active or Active and Pending state according the description below:

Using three bits defined by AHB bus security state (1=non-secure), security of the HPPI(1=non-secure)and the value of GICC_CTLR[AckCtl]:

00x ’ respond with the true interrupt number, transitioning to active (secure request to secure interrupt, ACKCTL is don't care)

010 ’ respond with 1022 (secure request to non-secure interrupt but ACKCTL=0 disabling secure handling of non-secure interrupts)

011 ’ respond with the true interrupt number, transitioning to active (secure request to non-secure interrupt with ACKCTL=1)

10x ’ respond with 1023 (non-secure request to secure interrupt)

11x ’ respond with the true interrupt number, transitioning to active (non-secure request to non-secure interrupt)

APCS_GICC_IAR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.

APCS_GICC_IAR (cont.)

Bits	Name	Description
9:0	INT_ID	Interrupt Identifier. The value returned in this field is dependent on the security state of the access to the register, the security state of any outstanding interrupts, the value of GICC_CTLR[AckCtl] as defined in the description above.

0x02002010 APCS_GICC_EOIR

Type: Write (Command)
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

Unlike GIC1, GICC_EOIR (End Of Interrupt) register has two possible behaviors. By default it acts as it did in GIC1, that is, it can be written to indicate when software has finished handling an interrupt.

In GIC2, if GICC_CTLR[EOImode] is set (1), writing this register has the "priority drop" (PD) effect. The PD effect is when the active priority bit for the highest priority active interrupt is cleared. The key difference, when EOImode is one, is that the Distributor is not notified that this happened - that is, the interrupt itself does not become inactive.

When EOImode is zero, writing to this register will, in addition to the PD effect described above, set the interrupt to Inactive or Pending (if prior to writing to this register, the interrupt was both Active and Pending it becomes just pending) in the Distributor.

In either case, the value written must be the interrupt ID, and the CPU Source ID for SGIs, of the interrupt that is being completed.

The security status of the write to this register (NS-prot) must match the security status (NS-int) of the interrupt ID, according to Table 11-10 for the interrupt to be successfully cleared.

Non-secure access: See Table 11-10.

Secure access: See Table 11-10.

Table 11-10 GICC_EOIR Priority Drop Effect Definition

[AckCtl]	Security status of the write request	Highest Priority Active interrupt security value	Effect
x	Non-secure	Non-secure	Clear the highest active Non-secure priority level
x	Non-secure	Secure	Clear the highest active Non-secure priority level

Table 11-10 GICC_EOIR Priority Drop Effect Definition

[AckCtl]	Security status of the write request	Highest Priority Active interrupt security value	Effect
0	Secure	X	Clear the highest active Secure priority level
1	Secure	X	Clears the highest active priority level.

APCS_GICC_EOIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it must match the ID of the CPU which requested the Interrupt. As described in Table 17-9 (GICC_EIOR security (and source CPU) match definition), the CPU Source ID must match an active interrupt in order for the GICC_EOIR to take effect. The CPU_ID is written must match that delivered to software when GICC_IAR is read. For PPIs and SPIs the CPU source ID field is ignored.
9:0	INT_ID	Interrupt Identifier. The value must match the interrupt ID that software received when reading the GICC_IAR register. If the security settings match (see Table 11-10) a write will cause the priority drop effect and if EOImode=0, the Active state in the Distributor for the corresponding interrupt will also be cleared.

0x02002014 APCS_GICC_RPR

Type: Read
Clock: CLK
Reset State: 0x000000F8

Security Treatment: Banked

The GICC_RPR (Running Priority) register provides access to the highest priority of all the Active interrupts on this CPU. The priority value returned is sensitive to the security status (NS-int) of the interrupt currently running and the NS-prot

Non-secure access: If the currently interrupt is secure (NS-int = 0), and a non-secure read of the Running Priority register is attempted (NS-prot = 1), then the value 0 (maximum priority) is returned.

Secure access: Returns the true value in the register.

APCS_GICC_RPR

Bits	Name	Description
31:8	RESERVED_1	
7:3	VAL	Running Priority
2:0	RESERVED_2	

0x02002018 APCS_GICC_HPPIR

Type: Read
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Banked

The GICC_HPPIR register provides access to the highest priority pending interrupt to the CPU Interface.

NOTE Interrupts that are Active and Pending in the Distributor are not considered candidates to become the highest priority pending interrupt.

Using three bits defined by AHB bus security state (1=non-secure), security of the HPPI(1=non-secure)and the value of GICC_CTLR[AckCtl]:

00x ’ respond with the true interrupt number (secure request to secure interrupt, ACKCTL is don't care)

010 ’ respond with 1022 (secure request to non-secure interrupt but ACKCTL=0 disabling secure handling of non-secure interrupts)

011 ’ respond with the true interrupt number (secure request to non-secure interrupt with ACKCTL=1)

10x ’ respond with 1023 (non-secure request to secure interrupt)

11x ’ respond with the true interrupt number (non-secure request to non-secure interrupt).

APCS_GICC_HPPIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.

APCS_GICC_HPPIR (cont.)

Bits	Name	Description
9:0	INT_ID	Interrupt Identifier. The value returned in this field is dependent on the security state of the access to the register, and the security state of any outstanding interrupts, as described above.

0x0200201C APCS_GICC_ABPR

Type: Read/write
Clock: CLK
Reset State: 0x00000003

Security Treatment: Restricted

The GICC_ABPR register provides a copy of the non-secure binary point register for use by secure software. See the definition of the GICC_BPR register for details on the use of this register.

Non-secure access: No access.

Secure access: Access granted, updates are reflected to non-secure software at the GICC_BPR register at address offset 0x08.

APCS_GICC_ABPR

Bits	Name	Description
31:3	RESERVED	
2:0	VAL	Same as the GICC_BPR register - affects only non-secure interrupts.

0x02002020 APCS_GICC_AIAR

Type: Read (Command)
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Restricted

The GICC_AIAR register is used by the CPU to obtain the ID of the interrupt which caused the assertion if IRQn or FIQn. This is a secure only register used to read non-secure interrupts by Secure Software.

Performing this read has the side effect of causing the Distributor to change the interrupt from the Pending state to the Active or Active and Pending state.

Non-secure access: No access. Read as zero.

Secure access: See description below.

Based on the 2 bits defined by the AHB Security of the request (1=non-secure) and the security of the interrupt (1=non-secure):

00 ’ respond with 1023 (secure request that behaves as if it is a non-secure request, to secure interrupt)

01 ’ respond with the true interrupt number, transitioning to active (secure request that behaves as if it is a non-secure request, to non-secure interrupt)

1x ’ RAZ/WI (non-secure request cannot access this register)

APCS_GICC_AIAR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier..

0x02002024 APCS_GICC_AEOIR

Type: Write (Command)
Clock: CLK
Reset State: 0x00000000

Security Treatment: Restricted

A secure write to this register has an identical effect to a non-secure write to GICC_EOIR, with the exception of the EOImode bit; the value of the secure EOImode bit (bit 9) in GICC_CTLR is used to determine whether the interrupt is deactivated or just priority dropped rather than the non-secure EOImode bit (bit 10).

This register must be used by secure software to signal completion of non-secure interrupts when GICC_CTLR AckCtl bit is set to 0; GICC_EOIR cannot be used for this purpose since it would affect GICC_APRn rather than GICC_NSAPRn.

Non-secure access: ignored

Secure access: signal completion of non-secure interrupt

APCS_GICC_AEOIR

Bits	Name	Description
31:13	RESERVED	

APCS_GICC_AEOIR (cont.)

Bits	Name	Description
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it must match the ID of the CPU which requested the Interrupt. The CPU Source ID must match an active interrupt in order for the GICC_AEOIR to take effect. The CPU_ID is written must match that delivered to software when GICC_IAR is read. For PPIs and SPIs the CPU source ID field is ignored.
9:0	INT_ID	Interrupt Identifier. The value must match the interrupt ID that software received when reading the GICC_IAR register. Interrupt Identifier. A write will cause the priority drop effect and if EOImode=0, the Active state in the Distributor for the corresponding interrupt will also be cleared.

0x02002028 APCS_GICC_AHPPIR

Type: Read
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Restricted

This is a Secure-Only register.

A read from this register has an identical effect to a Non-Secure read from GICC_HPPIR. It can therefore be used to check for a pending Non-Secure interrupt without the possibility of returning a Secure Interrupt ID value.

Interrupts that are Active and Pending in the Distributor are not considered candidates to become the highest priority pending interrupt.

Non-secure access: No access. Read as zero.

Secure access: See description below.

NOTE

Using three bits defined by AHB bus security state (1=non-secure), security of the HPPI(1=non-secure)and the value of GICC_CTLR[AckCtl]:

00x ’ respond with 1023 (hppi is a secure interrupt)

01x ’ respond with the true interrupt number (hppi is a non-secure interrupt)

1xx ’ RAZ/WI (non-secure request cannot access this register)

.

APCS_GICC_AHPPIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier. The value returned in this field is dependent on the security state of the access to the register, and the security state of any outstanding interrupts, as described above.

0x020020D0 APCS_GICC_APR

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

Each bit in the GICC_APR register provides the active status of priorities in the CPU Interface.

Non-secure access: Bits 15-0 represent priorities 31 to 16 of the non-secure active priorities.

Secure access: Bits 31-0 represent priorities 31 to 0 of the active secure priorities.

APCS_GICC_APR

Bits	Name	Description
31:0	PRI	0x1: A (ACTIVE) 0x0: NA (NOT ACTIVE)

0x020020E0 APCS_GICC_NSAPR

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Restricted

Each bit in the GICC_NSAPR register provides the active status of non-secure priorities in the CPU Interface.

Non-secure access: None - write ignore, read-as-zero.

Secure access: Bits 31-0 represent priorities 31 to 0 of teh active non-secure priorities.

APCS_GICC_NSAPR

Bits	Name	Description
31:0	PRI	0x1: A (ACTIVE) 0x0: NA (NOT ACTIVE)

0x020020FC APCS_GICC_IIDR

Type: Read
Clock: CLK
Reset State: 0x00020070

Security Treatment: Common

The GICC_IIDR register provides information about the GIC2 CPU Interface version and device implementor information.

APCS_GICC_IIDR

Bits	Name	Description
31:20	PART_NUM	Part Number: 0x0
19:16	ARCH_VERSION	Architecture Version : 0x2
15:12	REVISION	Revision number: 0x0
11:0	IMPLEMENTOR	Bits[11:8] contain the implementor's JEP106 continuation code, 0x0 Bit[7] is always 0 Bits[6:0] contain bits [6:0] of the implementor's JEP106 code,

0x02003000 APCS_GICC_DIR

Type: Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_DIR register provides the mechanism by which Software can Deactivate a specific interrupt.

Secure writes can deactivate secure and non-secure interrupts.

Non-secure writes can only deactivate non-secure interrupts.

Note that unlike GICC_EOIR and GICC_IAR, there is no restriction of the Deactivation of Non-Secure interrupts with Secure accesses. The AckCtl bit does not affect the behavior of GICC_DIR. This is because unlike GICC_IAR there is no chance of the access affecting an interrupt from an

unexpected security state, and unlike GICC_EOIR there is no effect on GICC_APRn or GICC_NSAPRn, so there is no need to indicate which register should be affected.

APCS_GICC_DIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier. INT_ID written should match value returned from GICC_IAR read.

11.5 KPSS GIC2 GICV Registers (0x02000000 APCS_QGIC2_BASE)

This section contains the Krait Processor Subsystem (KPSS) GIC2 GICV registers.

The Generic Interrupt Controller 2 (GIC2) is a reusable configurable soft core. This GIC2 specification conforms to ARM's Generic Interrupt Controller architecture specification. Where differences exist, either additional features were added or this document must change to conform to ARM's specified architecture. Where additional features were added, they will be clearly marked. The GIC2 design supports ARM's TrustZone architecture with two security zones: secure and non-secure.

The GIC2 is made of two parts: the Distributor and CPU Interfaces (up to eight). Each of these interfaces contains a CRIF slave interface. There must be at least one CPU Interface in the design.

In this manual, addresses are offsets from zero. When constants are exported, they are re-assigned to the appropriate base address.

Half-word and Byte access is supported by a subset of the registers.

Security treatment of registers in the GIC2 is divided into four types of registers. These are:

- "Common" indicates that both secure and non-secure software have full access to the register.
- "NS-int Dependent" indicates that state belonging to both secure and non-secure interrupts may be present in the register, depending on the value set in the Interrupt Security Register. Secure accesses to such a register are able to access all of the register's state, regardless of the Interrupt Security Register setting. Non-secure accesses may only access state belonging to non-secure interrupts. For non-secure accesses to state belonging to secure interrupts, writes are ignored and reads return zero.
- "Banked" indicates that the register exhibits different functionality according to whether it is accessed with a secure or non-secure request.
- "Restricted" indicates that only secure requests may access this register. If non-secure accesses are attempted, writes are ignored and reads return zero.

The type of register is specified for each register individual. Table 11-11 explains security treatment for register bits.

Table 11-11 Register security treatment

bus NS bit	SECURITY BIT	ALLOW Access
0	0	1
0	1	1
1	0	0
1	1	1

Glossary:

CPU Interface: That part of the GIC2 responsible for receiving the next interrupt from the Distributor and, if the interrupt has sufficient priority, asserting an interrupt indication to the CPU.

CPU MID: The Master ID of a CPU interface (as in AXI's AMID). The CPU MID reaching the Distributor must match the CPU Interface connected to that master.

Distributor: That part of the GIC2 responsible for detecting, disabling, prioritizing, and directing interrupts to CPU(s). The Distributor also accepts requests from and signals software interrupts to the CPU(s).

FABRIC: Flexible Advanced Buses & Reusable Interconnect Cores

NS-int: Security status of a particular interrupt ID. The value 0x0 is "secure", 0x1 is "non-secure".

NS-prot: Security status of the a bus transaction (read or write) according to the NS bit.

PPI: Private Peripheral Interrupt, interrupt from a peripheral whose interrupt line is destined to a particular CPU and can't be physically connected/directed to any other.

SGI: Software Generated Interrupt, interrupt from one CPU (or thread) to another.

SPI: Shared Peripheral Interrupt, interrupt from a peripheral whose interrupt line's CPU target is programmable to one or more CPU interface by the Distributor.

11.5.1 QGIC2 Virtual CPU Interface

Table 11-12 QGIC2 Virtual CPU Interface Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x4000	GICV_CTLR	RW	0x0000_0000	Common	control register
0x4004	GICV_PMR	RW	0x0000_0000	Common	priority mask
0x4008	GICV_BPR	RW	0x0000_0002	Common	binary point
0x400C	GICV_IAR	R (CMD)	0x0000_0000	Common	interrupt acknowledge
0x4010	GICV_EOIR	W (CMD)		Common	end-of-interrupt
0x4014	GICV_RPR	R	0x0000_00F8	Common	running priority
0x4018	GICV_HPPIR	R	0x0000_03FF	Common	highest priority pending
0x401C	GICV_ABPR	RW	0x0000_0003	Common	aliased binary point
0x4020	GICV_AIAR	R (CMD)	0x0000_03FF	Common	aliased interrupt acknowledge
0x4024	GICV_AEOIR	W (CMD)		Common	aliased end-of-interrupt
0x4028	GICV_AHPPIR	R	0x0000_03FF	Common	aliased highest priority pending

Table 11-12 QGIC2 Virtual CPU Interface Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x402C-0x40CC	Reserved				
0x40D0	GICV_APR	RW	0x0000_0000	Common	Active Priorities
0x40D4-0x40F8	Reserved				
0x40FC	GICV_IIDR	R	0x0002_0070	Common	ID
0x4100-0x4FFC	Reserved				
0x5000	GICV_DIR	W		Common	Deactivate Interrupt

11.5.2 QGIC2 Virtual CPU interface registers

NOTE All transactions to the Virtual CPU Interface are treated as secure. All bits are accessible to every transaction. There the secure and non-secure views do not apply to this block of registers. All access to GICV registers operate upon the Hypervisor portion of GIC2 in a similar fashion as GICC registers operate on the distributor.

0x02004000 APCS_GICV_CTLR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICV_CTLR configures the GIC2 Virtual CPU interface.

APCS_GICV_CTLR

Bits	Name	Description
31:10	RESERVED_1	
9	EOIMODE	Controls the behavior of Non-secure access to GICV_EOI and GICV_DIR 0x0: PD_AND_DI (Both Priority Drop and Deactivate Interrupt, GICV_DIR does not function) 0x1: PD (GICV_EOI performs Priority Drop, GICV_DIR performs deactivate interrupt function)
8:5	RESERVED_2	

APCS_GICV_CTLR (cont.)

Bits	Name	Description
4	GBPR	Controls which binary point register is used to calculate preemption, GICV_BPR or the GICV_ABPR. 0x0: BANKED (Group 0 interrupts use the Group 0 Binary Point Register, Group 1 interrupts use the Group 1 Binary Point Register) 0x1: G0 (all interrupts use the Group 0 Binary Point Register)
3	FIQEN	Controls destination of secure interrupts. 0x0: IRQ 0x1: FIQ
2	ACKCTL	Controls whether reads of the VM Interrupt Acknowledge Register can acknowledge interrupts where the NS bit is set in the List Register. acknowledged only if the NS bit is clear in the corresponding List Register. If the NS bit in that List Register is set, the read will return 1022 and the interrupt can only be acknowledge by a read to the VM Aliased Interrupt Acknowledge Register.) always acknowledged regardless of the NS bit setting in the corresponding List Register.) 0x0: NO_IAR_4G0 (On a read of GICV_IAR, the highest priority unmasked PENDING interrupt is) 0x1: IAR_4G0 (On a read of GICV_IAR, the highest priority unmasked PENDING interrupt is)
1	ENABLE_G1	This bit enables Group 1 interrupts. 0x0: CLR 0x1: SET
0	ENABLE_G0	This bit enables Group 0 interrupts. 0x0: CLR 0x1: SET

0x02004004 APCS_GICV_PMR

Type: Read/write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

The GICV_PMR register configures the GIC2 Virtual CPU interface Priority Mask. The Priority Mask can be used to limit the interrupts that can cause an interrupt request to the CPU based on priority levels.

APCS_GICV_PMR

Bits	Name	Description
31:8	RESERVED_1	
7:3	LEVEL	Set the Priority Mask Level. The CPU interface asserts an interrupt request to CPU if the priority of the highest Pending interrupt sent by the interrupt Distributor is strictly higher than at least the mask set in Priority Mask Register.
2:0	RESERVED_2	

0x02004008 APCS_GICV_BPR

Type: Read/write
Clock: CLK
Reset State: 0x00000002

Security Treatment: Common

The GICV_BPR register configures the GIC2 Virtual CPU interface Binary Point. The Binary Point is used to limit interrupts that can cause an interrupt request to the CPU based on the interrupt's priority and the interrupt priority that currently being serviced by the CPU (if there is one). If the CPU is not servicing an interrupt, the Binary Point register is not used.

APCS_GICV_BPR

Bits	Name	Description
31:3	RESERVED	
2:0	VAL	The VAL setting is used to determine the priority bits used for preemption according to Table 11-9 Interpretation of Binary Point Register value.

0x0200400C APCS_GICV_IAR

Type: Read (Command)
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Common

The GICV_IAR register is used by the CPU to obtain the ID of the interrupt which caused the assertion if IRQn or FIQn.

Performing this read has the side effect of causing the GICH to change the interrupt from the Pending state to the Active or Active and Pending state according to the rules below:

Using the 2 bits defined by Security of the HPPI(1=non-secure) and the value of GICV_CTLR[AckCtl]:

0x ’ respond with the true interrupt number, transitioning to active (ignore APROTNS and consider as a secure request to secure interrupt, ACKCTL is don't care)

10 ’ respond with 1022 (ignore APROTNS and consider as secure request to non-secure interrupt but ACKCTL=0 disabling secure handling of non-secure interrupts)

11 ’ respond with the true interrupt number, transitioning to active (ignore APROTNS and consider as secure request to non-secure interrupt with ACKCTL=1)

APCS_GICV_IAR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier - a virtual interrupt number determined by the Hypervisor SW.

0x02004010 APCS_GICV_EOIR

Type: Write (Command)
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

GICV_EOIR (End Of Interrupt) register has two possible behaviors. By default it can be written to to indicate when software has finished handling an interrupt.

If GICV_CTLR[EOImode] is set (1), writing this register has the "priority drop" (PD) effect. The PD effect is when the active priority bit for the highest priority active interrupt is cleared. The key difference, when EOImode is (1), is the interrupt itself does not become inactive.

When EOImode is (0), writing to this register will, in addition to the PD effect described above, set the interrupt to Inactive or Pending (if prior to writing to this register, the interrupt was both Active and Pending it becomes just pending). However, if GICV_CTLR[EOImode] is (0), then the CPU_ID and INT_ID must match an active interrupt for a state change to occur.

In either case, the value written must be the interrupt ID, and the CPU Source ID for SGIs, of the interrupt that is being completed.

APCS_GICV_EOIR

Bits	Name	Description
31:13	RESERVED	

APCS_GICV_EOIR (cont.)

Bits	Name	Description
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it must match the ID of the CPU which requested the Interrupt. The CPU_ID is written must match that delivered to software when GICV_IAR is read. For PPIs and SPIs the CPU source ID field is ignored.
9:0	INT_ID	Interrupt Identifier. The value must match the interrupt ID that software received when reading the GICV_IAR register.

0x02004014 APCS_GICV_RPR

Type: Read
Clock: CLK
Reset State: 0x000000F8

Security Treatment: Common

The GICV_RPR (Running Priority) register provides access to the highest priority of all the Active interrupts on this Virtual CPU.

APCS_GICV_RPR

Bits	Name	Description
31:8	RESERVED_1	
7:3	VAL	Running Priority
2:0	RESERVED_2	

0x02004018 APCS_GICV_HPPIR

Type: Read
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Common

The GICV_HPPIR register provides access to the highest priority pending interrupt to the Virtual CPU Interface. If no interrupt is pending, responds with 0x3FF.

NOTE Interrupts that are Active and Pending in the GICH (hypervisor) are not considered candidates to be come the highest priority pending interrupt.

Using 2 bits defined by the value of GICV_CTLR[AckCtl]and the NS bit of the HPPI(1=non-secure):

1x ’ respond with the virtual interrupt number

00 ’ respond with the virtual interrupt number

01 ’ respond with 1022

APCS_GICV_HPPIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier.

0x0200401C APCS_GICV_ABPR

Type: Read/write
Clock: CLK
Reset State: 0x00000003

Security Treatment: Common

The GICV_ABPR register provides access to the non-secure binary point register used by non-secure interrupts when GICV_CTRL[GBPR]=0. See the definition of the GICV_BPR register for details on the use of this register.

APCS_GICV_ABPR

Bits	Name	Description
31:3	RESERVED	
2:0	VAL	Same as the GICV_BPR register - affects only non-secure interrupts.

0x02004020 APCS_GICV_AIAR

Type: Read (Command)
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Common

The GICV_AIAR register is used by the CPU to obtain the ID of the interrupt which caused the assertion if IRQn or FIQn.

Performing this read has the side effect of causing the GICH to change the interrupt from the Pending state to the Active or Active and Pending state according to the rules below:

Using the security state of the pending interrupt:

- 0 ’ respond with 1023
- 1 ’ respond with the true interrupt number, transitioning to active

APCS_GICV_AIAR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier - a virtual interrupt number determined by the Hypervisor SW.

0x02004024 APCS_GICV_AEOIR

Type: Write (Command)
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

This register presents the same programmers model as GICC_AEOIR.

The effect of writing to this register is identical to the effect of writing the same value to the GICV_EOIR register. This alias is provided for compatibility with the Physical CPU Interface, where the two registers have a different effect due to the provision of separate Secure and Non-Secure Active Priority Registers.

APCS_GICV_AEOIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it must match the ID of the CPU which requested the Interrupt. The CPU_ID is written must match that delivered to software when GICV_IAR is read. For PPIs and SPIs the CPU source ID field is ignored.
9:0	INT_ID	Interrupt Identifier. The value must match the interrupt ID that software received when reading the GICV_IAR register.

0x02004028 APCS_GICV_AHPPIR

Type: Read
Clock: CLK
Reset State: 0x000003FF

Security Treatment: Common

This register presents the same programmers model as GICC_AHPPIR.

This register returns the interrupt ID of the highest priority PENDING interrupt if it has an NS value of 1. Reading this interrupt has no side effects and simply returns the highest priority PENDING interrupt among the list registers or a status code according to the following table:

Using the NS bit of the HPPI(1=non-secure):

0 ’ 1023

1 ’ respond with the virtual interrupt number

Note that in some cases the returned value may not be strictly accurate if interrupts are currently paged out in software.

APCS_GICV_AHPPIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier.

0x020040D0 APCS_GICV_APR

Type: Read/Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Common

Each bit in the GICV_APR is an alias of GICH_APR. The data and access control are one and the same.

APCS_GICV_APR

Bits	Name	Description
31:0	PRI	0x1: A (ACTIVE) 0x0: NA (NOT ACTIVE)

0x020040FC APCS_GICV_IIDR

Type: Read
Clock: CLK
Reset State: 0x00020070

Security Treatment: Common

The GICV_IIDR register provides information about the GIC2 Virtual CPU Interface version and device implementor information.

APCS_GICV_IIDR

Bits	Name	Description
31:20	PART_NUM	Part Number: 0x390
19:16	ARCH_VERSION	Architecture Version : 0x2
15:12	REVISION	Revision number: 0x0
11:0	IMPLEMENTOR	Bits[11:8] contain the implementor's JEP106 continuation code, 0x0 Bit[7] is always 0 Bits[6:0] contain bits [6:0] of the implementor's JEP106 code,

0x02005000 APCS_GICV_DIR

Type: Write
Clock: CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICV_DIR register provides the mechanism by which Software can Deactivate a specific interrupt.

APCS_GICV_DIR

Bits	Name	Description
31:13	RESERVED	

APCS_GICV_DIR (cont.)

Bits	Name	Description
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt.
9:0	INT_ID	Interrupt Identifier. The value should match the INT_ID returned from the read of GICV_IAR.

11.6 KPSS ACC Registers (0x02008000 APCS_ACC_BASE)

This section contains the Krait Processor Subsystem (KPSS) ACC Secure registers.

0x02008000 APCS_ACCSECURE

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0007

Security Treatment: Restricted

The APCS_ACCSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Krait's APROTNS pin. When APROTNS is set to '0' the state of the APCS_ACCSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_ACCSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_ACCSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_ACCSECURE register correspond to.

APCS_ACCSECURE

Bits	Name	Description
31:4	RESERVED	
31:3	RESERVED_BITS31_3	
2	TST	Controls security treatment for test control registers: APCS_ATSTBUS_SEL 0x1: NSEC 0x0: SEC
1	CLK_CTL	Controls security treatment for the clock control registers: APCS_ACC_STS, APCS_CPU_AUX_CLK_SEL. 0x1: NSEC 0x0: SEC
0	SLP_CTL	Controls security treatment for the sleep control registers: APCS_CPU_PWR_CTL, APCS_CPU_TRGTD_DBG_RST. 0x1: NSEC 0x0: SEC

0x02008004 APCS_CPU_PWR_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0109

Security Treatment: Controlled by APCS_ACCSECURE [SLP_CTL].

The APCS_CPU_PWR_CTL register is used to control the clamps, reset and array head switches.

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APCS_CPU_PWR_CTL

Bits	Name	Description
31:21	RESERVED_BITS31_21	
20:16	CLK_EN	Clock enables for CORE clock. This is only to workaround hardware dynamic clock gating problems. [20:18]= SYS_apcNAux_Clk[3:1] [17] = SYS_apcsRef_Clk [16] = SYS_apcNPll_Clk 0x1: Always enabled 0x0: dynamically enabled by hardware
15:10	RESERVED_BITS15_10	
9	RET_SLP_REQ	When set, this bit request the L2SCU to in-flight snoop operation and block new snoops request from entering FIFO. This control is intended to permit external masters such as the RPM to put CPU to retention sleep modes, when power control is being done by an external master instead of the SPM. The output of this register bit is ORed with a retention sleep request control output from the SPM, so that if either the SPM asserts the control, or the RPM sets this bit, the CPU's snoop FIFO is quiesce.
8	PLL_CLAMP	When set, this bit clamp the output of TDC logic in PLL. This signal that must be asserted prior to collapsing CPU voltage, vdd_apc0. This bit is ORed with SAW output before passing to the APC PLL.
7	CORE_PWRD_UP	Report that the CPU is powered up.
6	GATE_CLK	When set, this bit forces the CPU clock to be gated off. This control is intended to permit external masters such as the RPM to gate off the CPU clock during sleep modes, when power control is being done by an external master instead of the SPM. The output of this register bit is ORed with a clock gating control output from the SPM, so that if either the SPM asserts the control, or the RPM sets this bit, the CPU clock will be gated off. When set, this bit gate the CPU clock that must be asserted during sleep state. This bit is ORed with a SAW output before passing to the CPU core.
5	COREPOR_RST	When set, this bit asserts corepor areset to the CPU core.
4	CORE_RST	When set, this bit asserts core areset to the COPU core.

APCS_CPU_PWR_CTL (cont.)

Bits	Name	Description
3	L2DT_SLP	When set, this bit opens a head switch to put the L2 duplicate tag array into a low-leakage, non-data-retaining state. This bit is ORed with a SAW output before passing to the CPU core. The controlled memory array contains a duplicate of the tags contained in the L1 data cache, and is used by the L2 to snoop and see if a shared memory access from one processor necessitates invalidating a line in another processor's L1 data cache. Thus, this memory array generally can be offline when the associated CPU is power-collapsed and its L1 data cache is also off-line.
2	RESERVED_BIT2	Previously ETB HS
1	RESERVED_BIT1	Previously L1 HS
0	CLAMP	When set, this bit asserts the clamp signal that must be asserted prior to collapsing CPU voltage, vdd_apc0. This bit is ORed with SAW output before passing to the CPU core.

0x02008008 APCS_ACC_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: N/A

Security Treatment: Controlled by APCS_ACCSECURE [CLK_CTL].

The APCS_ACC_STS register is used to monitor the output of the clock gating cells.

APCS_ACC_STS

Bits	Name	Description
31:18	RESERVED_BITS31_18	
17	RET_SLP_ACK	This bit reflect the status of APCN_sysRetSlpAck bit. L2 assert the signal when it see the APCN_sysRetSlpReq and CPU snoop FIFO is quieced. L2 de-assert this signal after APCN_sysRetSlpReq is de-asserted and all snoop invalidation is completed.
16	SLP_CLK	This bit reflect the status of APCN_sleepClkOnReq bit
15	AHB_CLK	This bit reflect the status of APCN_ahbClkOnReq bit
14	REF_CLK	This bit reflect the status of APCN_refClkOnReq bit
13	SPM_SLP_STATE	This bit reflect the status of SPM Sleep State
12	FRC_CLK_OFF	This bit reflect the status of APCN_apccForceClocksOff bit
11	RET_SLP_REQ	This bit reflect the status of APCN_apccRetSlpReq bit
10	TRGTD_DBG_RST	This bit reflect the status of APCN_apcTargetedDbg_Areset_N bit
9	CORE_RST	This bit reflect the status of APCN_apccCore_Areset_N bit
8	COREPOR_RST	This bit reflect the status of APCN_apccCorePor_Areset_N bit

APCS_ACC_STS (cont.)

Bits	Name	Description
7	L2DT_HS	This bit reflect the status of the SYS_apcNSwCtlDupTagArrayCollapse bit
6	CLAMP	This bit reflect the status of the SYS_apcNClampApcNvd bit.
5:3	CORE_AUX_CLK	This bits reflect the status of the APCS_sysApcNAuxClkOnReq bits.
2	CORE_PLL_CLK	This bit reflect the status of the APCS_sysApcNPllClkOnReq bit.
1	CORE_NO_PWR_DWN	This bit reflect the status of the APCN_dbgCoreNoPwrDwn bits.
0	CORE_PWRUP_REQ	This bit reflect the status of the APCN_dbgCorePwrUpReq bits.

0x0200800C APCS_ATSTBUS_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [TST].

APCS_ATSTBUS_SEL selects different modules' test bus outputs.

APCS_ATSTBUS_SEL

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	EN	Set to 1 to cause APCS to drive the test bus outputs. 0x1: enabled 0x0: disabled
1:0	SEL	0x3: CONSTANT 0x2: SAW 0x1: TMR 0x0: CLK

0x02008010 APCS_CPU_TRGTD_DBG_RST

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [SLP_CTL].

APCS_CPU_TRGTD_DBG_RST is used to reset the CPU core debug logic. The hardware clear the register after the CPU debug logic is reset. Software need to poll this register to check if the reset is complete.

APCS_CPU_TRGTD_DBG_RST

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	RST	When set this bit de-assert SYS_apcNTargetedDbg_Areset_N to the CPU core for 32 REF clock cycle to the CPU core. At the end of the reset hardware clear this bit.

0x02008014 APCS_CPU_AUX_CLK_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [CLK_CTL]

The APCS_CPU_AUX_CLK_SEL register controls the gfmux, which selects the AUX clock source for the Krait CPU clock. An additional selection set is provided to determine the clock source for the Krait core (4-1 GFMUX) in the Krait Hard Macro. The QSB clock is the raw source clk at reset.

APCS_CPU_AUX_CLK_SEL

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	AUX_SRC	Krait CPU AUX clock select: 0x3: SYS_apcNAux_Clk_1 0x2: SYS_apcNAux_Clk_2 0x1: SYS_apcNAux_Clk_3 0x0: SYS_apcsRef_Clk

11.7 KPSS SAW2 Registers (0x02009000 APCS_SAW2_BASE)

This section contains the Krait Processor Subsystem (KPSS) SAW2 registers.

The SAW2 (SPM and AVS. Wrapper2) design is an AHB slave that contains both SPM and AVS. CSRs.

0x02009000 APCS_SAW2_SECURE

Type: Read/write
Clock: SYS_REF_CLK
Reset State: {3{CFGNSINIT}}

Security Treatment: Restricted

The SAW2_SECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by ahb_saw_hprotns pin. When ahb_saw_hprotns is set to ‘0’ the state of the SAW2_SECURE register is not considered; a secure transaction is always allowed. When ahb_saw_hprotns is set to ‘1’, the SAW2_SECURE register security treatment bit of that register must be ‘1’ for access to be granted. If the security treatment bit of the register is set to ‘0’, the non-secure (ahb_saw_hprotns = ‘1’) transactions are denied. When access is denied, a write is ignored, and a read will return ‘0’. No error is signaled.

When reading the SAW2_SECURE register, non-secure agents will always read ‘0’. Secure agents will see the actual value of the register. The reset value is controlled by CFGNSINIT input pin.

APCS_SAW2_SECURE

Bits	Name	Description
31:3	RESERVED	
2	SAW_CTL	Controls security treatment for SAW2 registers: SAW2_ID, SAW2_CFG, SAW2_STS_0, SAW2_STS_1, SAW2_RST 0x1: NSEC 0x0: SEC
1	PWR_CTL	Controls security treatment for SPM registers: SAW2_SPM_CTL, SAW2_SPM_PMIC_DLY, SAW2_SPM_PMIC_DATA_0, SAW2_SPM_PMIC_DATA_1, SAW2_SPM_SLP_SEQ_ENTRY_n, SAW2_SPM_DLY 0x1: NSEC 0x0: SEC
0	VLT_CTL	Controls security treatment for the AVS. registers: SAW2_AVS_CTL, SAW2_VLVL, SAW2_AVS_HYSTERESIS 0x1: NSEC 0x0: SEC

0x02009004 APCS_SAW2_ID

Type: Read
Clock: SYS_REF_CLK
Reset State: Undefined

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register reports the revision and parameter information for the SAW2 core.

APCS_SAW2_ID

Bits	Name	Description
31	RESERVED_BITS31	
30:25	NUM_SPM_ENTRY	SAW2 parameter: Indicates number of SAW2_SPM_SLP_SEQ_ENTRY register implemented. Value can range from 1 - 32
24:20	NUM_PWR_CTL	SAW2 parameter: Indicates number of power control implemented. Value can range from 2 - 16
19	RESERVED_BITS19	
18	PMIC_ARB_INTF	SAW2 parameter: Indicates PMIC Arbiter Interface function is implemented
17	AVS_PRESENT	SAW2 parameter: Indicates AVS. function is implemented
16	SPM_PRESENT	SAW2 parameter: Indicates SPM function is implemented
15:12	MAJOR	Major variant
11:0	MINOR	Minor variant

0x02009008 APCS_SAW2_CFG

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_CFG register is used to configure the common control between AVS. and SPM.system.

APCS_SAW2_CFG

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12	FRC_REF_CLK_ON	Chicken bit to force saw_sys_ref_clk_on_req ON.
11:8	ADR_IDX	PMIC Arbiter Address Index. Drive the saw_pmic_addr_idx output port.

APCS_SAW2_CFG (cont.)

Bits	Name	Description
7:6	RESERVED_BITS7_6	
5	PMIC_MODE	PMIC Handshake 0x0: 8K_PMIC (only DONE signal) 0x1: 7K_PMIC (both ACK and DONE signals)
4:0	CLK_DIV	Divider ratio for clock. This is used to generate timer tick for the timer. Timer tick is asserted every (CLK_DIV + 1) sys_ref_clk period. ..... For sys_ref_clk = 20 MHz (53ns) The timer tick range 53 ns to 1.6us. 0x0: Timer Tick every sys_ref_clk 0x1F: Timer Tick every 128 sys_ref_clk.

0x0200900C APCS_SAW2_STS_0

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

APCS_SAW2_STS_0

Bits	Name	Description
15	SHTDWN_REQ	This bit reflects the shutdown request from the SPM(spm_rpm_shutdown_req) to RPM.
14	SHTDWN_ACK	This bit reflects the shutdown acknowledgement from the RPM(rpm_spm_shutdown_ack) to SPM.
13	BRNGUP_REQ	This bit reflects the bringup request from the SPM(spm_rpm_bringup_req) to RPM.
12	BRNGUP_ACK	This bit reflects the bringup acknowledgement from the RPM(rpm_spm_bringup_ack) to SPM.
11:10	PMIC_STATE	State of the PMIC FSM: transitions back to IDLE) transitions back to IDLE) 0x0: IDLE (waiting for PMIC transaction from AVS. or SPM) 0x1: ACK (waiting for ACK from PMIC Arb) 0x2: DONE (waiting for DONE form PMIC Arb before) 0x3: DELAY (waiting for delay count termination before)

APCS_SAW2_STS_0 (cont.)

Bits	Name	Description
9:8	RPM_STATE	State of the RPM FSM: 0x0: RUN (waiting for SPM request) 0x1: STDNACK (waiting for shutdown ACK from RPM) 0x2: WAKEUP (waiting for wakeup interrupt) 0x3: BGUPACK (waiting for bringup ACK from RPM)
7	AVS_STATE	State of the AVS. FSM: indication) 0x0: IDLE (waiting to be enabled or for next UP/DOWN) 0x1: REQ (waiting for PMIC FSM to transition to IDLE)
6:0	SPM_CMD_ADDR	Last SPM command executed.

0x02009010 APCS_SAW2_STS_1

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

APCS_SAW2_STS_1

Bits	Name	Description
31	RESERVED1	
30	SW_WR_PEND	This bit reflects the VLVL state of the request from the SAW2_VCTL write is pending.
29	CPU_UP	This bit reflects the VLVL state of the request from the CPU (avs_saw_up) to raise the VLVL.
28	CPU_DN	This bit reflects the VLVL state of the request from the CPU (avs_saw_down) to lower the VLVL.
27	MAX_INT	IRQ status bit, AVS. controller detected that raising the VLVL by AVS_CTL[VLVL_STEP] would result in a value greater than AVS_CTL[MAX_VLVL]. If AVS_CTL[IRQ_MAX_EN] is set, an interrupt is issued. NOTE that SW can set MAX_VLVL lower than current VLVL creating a condition where VLVL is higher than MAX_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MAX.

APCS_SAW2_STS_1 (cont.)

Bits	Name	Description
26	MIN_INT	IRQ status bit, AVS. controller detected that lowering the VLVL by SAW2_AVS_CTL[VLVL_STEP] would result in a value less than SAW2_AVS_CTL[MIN_VLVL]. If SAW2_AVS_CTL[IRQ_MIN_EN] is set, an interrupt is issued. NOTE that SW can set MIN_VLVL higher than current VLVL creating a condition where VLVL is lower than MIN_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MIN.
25:16	CURR_DLY	VLVL value of the counter used to calculate the time until the next AVS. controller request for a new VLVL.

0x02009014 APCS_SAW2_VCTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

Though this register is read/writable, it also causes a command pulse to the PMIC FSM. Writing this register results in a transaction to the PMIC with SAW2_VCTL being sent to the PMIC. SAW2 support both 8901 and 8058 regulator.

APCS_SAW2_VCTL

Bits	Name	Description
31:16	RESERVED_BITS31_16	

0x02009018 APCS_SAW2_AVS_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_CTL register is used to control the Adaptive Voltage Scaling (AVS) system.

APCS_SAW2_AVS_CTL

Bits	Name	Description
31	RESERVED	

APCS_SAW2_AVS_CTL (cont.)

Bits	Name	Description
30	VLVL_WIDTH	Defines the VLVL field of PMIC data. SAW2 at minimum supports 8901 and 8058 regulator. See PMIC document for details. 0x0: 5 bits VLVL (8058 regulator) 0x1: 6 bits VLVL (8901 regulator)
29:28	VLVL_STEP	Controls the step size of each request to PMIC Arbiter. SW may use values from 0 to 3. Note that the value 0 will result in no change - that is if the CPU requests UP or DOWN, the CURR_PVLVL will be sent to the PMIC Arbiter. This may be useful for debug. If an increment or decrement operation would cause the current VLVL to transition above or below the MAX_VLVL or MIN_VLVL, the current VLVL will not be changed. An interrupt will be signaled if IRQ_MAX/MIN_EN is 1
27	EN	AVS. Enable. **NOTE** Setting to 0 does not disable any pending interrupts. **NOTE** AVS. FSM and SPM FSM are mutually exclusive. Only one FSM is active at a time. SW does not have to disable AVS. before going to sleep. 0x0: Disable AVS 0x1: Enable AVS
26	SW_DONE_INT_EN	Set to 1 to turn on AVS. interrupt for when a SW initiated voltage change has completed. Set to 0 to mask it (turn it off). ASSERTION: This interrupt is asserted only after a SW write to SAW2_AVS_VLVL. Specifically, after the AVS. FSM traverses through all its states and transitions back to IDLE, the interrupt line is pulsed. The interrupt controller should be set to edge capture to receive this interrupt. CLEARING: None. This interrupt is a pulse, SW does not need to clear it (aside from requirements of the interrupt controller).
25	MAX_INT_EN	Set to 1 to turn on AVS. interrupt for MAX_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be greater than MAX_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit.
24	MIN_INT_EN	Set to 1 to turn on AVS. interrupt for MIN_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be smaller than MIN_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit
23	RESERVED_23	

APCS_SAW2_AVS_CTL (cont.)

Bits	Name	Description
22:17	MAX_VLVL	Control maximum value of AVS. controller's VLVL. When current VLVL reaches this value it may not grow any larger. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level higher, an interrupt is issued. This value may be updated at anytime. Setting to a value lower than MIN_VLVL is not supported, and unpredictable results may occur.
16	RESERVED_16	
15:10	MIN_VLVL	Control the minimum value of AVS. controller's VLVL. When the current VLVL reaches this level it may not shrink any smaller. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level lower, an interrupt is issued. This value may be updated at anytime. Setting to a value higher than MAX_VLVL is not supported, and unpredictable results may occur.
9:0	AVS_DELAY	Control the time between AVS. controller's requests to change the VLVL

0x0200901C APCS_SAW2_AVS_HYSTERESIS

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_HYSTERESIS register is used to delay the AVS. UP/DN signal to AVS. FSM. This is used to prevent the false PMIC step due to PDN noise.

APCS_SAW2_AVS_HYSTERESIS

Bits	Name	Description
31:24	RESERVED31_24	
23:16	DN_COUNT	HYSTERESIS DN COUNT. Delays of PMIC DN step operation.
15:8	RESERVED15_8	
7:0	UP_COUNT	HYSTERESIS UP COUNT. Delays of PMIC UP step operation.

0x02009020 APCS_SAW2_SPM_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_CTL register is used to control the subsystem power management system. This are parameters that controls the operation of SPM FSM.

APCS_SAW2_SPM_CTL

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	SPM_START_ADR	Start address for the SPM sequence.
3	ISAR	Inhibit Start Address Reset 0x0: End of program reset the SPM_START_ADR to zero. 0x1: Inhibit End of program to reset SPM_START_ADR
2:1	WAKEUP_CONFIG	Wakeup Configuration 0x0: sys_spm_wakeup 0x1: sys_spm_wakeup or !cpu_spm_wait_req 0x2: sys_spm_wakeup or rising edge of sys_spm_dbg_nopwrdwn 0x3: sys_spm_wakeup or !cpu_spm_wait_req or rising edge of sys_spm_dbg_nopwrdwn
0	SPM_EN	SPM En.

0x02009024 APCS_SAW2_SPM_PMIC_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC delay values after SPM FSM PMIC transaction. SPM wait for the programmed delay before executing the next SPM command.

APCS_SAW2_SPM_PMIC_DLY

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:24	DATA_1_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
23:19	RESERVED_BITS23_19	
18:16	DATA_1_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
15:11	RESERVED_BITS15_11	

APCS_SAW2_SPM_PMIC_DLY (cont.)

Bits	Name	Description
10:8	DATA_0_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
7:3	RESERVED_BITS7_3	
2:0	DATA_0_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms

0x02009028 APCS_SAW2_SPM_PMIC_DATA_0

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

APCS_SAW2_SPM_PMIC_DATA_0

Bits	Name	Description

0x0200902C APCS_SAW2_SPM_PMIC_DATA_1

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

APCS_SAW2_SPM_PMIC_DATA_1

Bits	Name	Description

0x02009030 APCS_SAW2_RST

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_RST register is used to reset the SAW logic. This register clear itself. It does not reset any SAW2 CSR's. It reset AVS. and SPM FSM and control registers. This is use to clear any hang condition.

APCS_SAW2_RST

Bits	Name	Description
31:1	RESERVED31_1	
0	RST	Reset AVS. and SPM FSM and control registers.

0x02009034 APCS_SAW2_SPM_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the delay values for SPM Delay command. SPM wait for the programmed delay before executing the next SPM command.

APCS_SAW2_SPM_DLY

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:20	DLY3	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
19:10	DLY2	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
9:0	DLY1	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms

0x02009080+4*n APCS_SAW2_SPM_SLP_SEQ_ENTRY_n

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_SLP_SEQ_ENTRY_n is an array used to sequence through the steps during various power mode. The register width is defined by CLOG_PWR_CTL parameter.

APCS_SAW2_SPM_SLP_SEQ_ENTRY_n

Bits	Name	Description

11.8 KPSS Timer Registers (0x0200A000 APCS_TMR_BASE)

This section contains the Krait Processor Subsystem (KPSS) Timer registers.

0x0200A000 APCS_TMRSECURE

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Restricted

The APCS_TMRSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Scorpion's APROTNS pin. When APROTNS is set to '0' the state of the APCS_TMRSECURE register is not considered; a secure transaction is always allowed. When APROTNS is set to '1', the APCS_TMRSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_TMRSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_TMRSECURE register correspond to.

APCS_TMRSECURE

Bits	Name	Description
31:5	RESERVED	
4	WDT0	Controls security treatment for the Watch Dog Timer registers: APCS_WDT0_FRZ, APCS_WDT0_INT_EN, APCS_WDT0_STS, APCS_WDT0_INT_WIDTH, APCS_WDT0_BARK_TIME, APCS_WDT0_TST_LD_STS, APCS_WDT0_TST_LD. 0x1: NSEC 0x0: SEC
3	WDT1	Controls security treatment for the Watch Dog Timer registers: APCS_WDT1_FRZ, APCS_WDT1_INT_EN, APCS_WDT1_STS, APCS_WDT1_INT_WIDTH, APCS_WDT1_BARK_TIME, APCS_WDT1_TST_LD_STS, APCS_WDT1_TST_LD. 0x1: NSEC 0x0: SEC
2	GPT0	Controls security treatment for the General Purpose Timer registers: APCS_GPT1_MTCH, APCS_GPT1__CNT, APCS_GPT1_EN, APCS_GPT1_CLR and bits 11-8 of APCS_TMR_STS. 0x1: NSEC 0x0: SEC

APCS_TMRSECURE (cont.)

Bits	Name	Description
1	GPT1	Controls security treatment for the General Purpose Timer registers: APCS_GPT0_MTCH, APCS_GPT0__CNT, APCS_GPT0_EN, APCS_GPT0_CLR and bits 11-8 of APCS_TMR_STS. 0x1: NSEC 0x0: SEC
0	DGT	Controls security treatment for the Debug Timer registers; APCS_DGT_MTCH, APCS_DGT_CNT, APCS_DGT_EN, APCS_DGT_CLR, APCS_DGT_CLK_CTL, and bits 3-0 of APCS_TMR_STS 0x1: NSEC 0x0: SEC

0x0200A004 APCS_GPT0_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: APCS_TMRSECURE [GPT0].

The general purpose timer will signal interrupt when its counter value has reached the value stored in the APCS_GPT0_MTCH register.

APCS_GPT0_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_GPT0_CNT at which an interrupt will be generated.

0x0200A008 APCS_GPT0_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_CNT register contains the current value of the GPT0 timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_GPT0_MTCH register at the same time due to HW re-use. The procedure for writing the APCS_GPT0_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_GPT0_EN.

- Write APCS_GPT0_CNT.
- Write (to set/restore) APCS_GPT0_MTCH if required.
- Enable the timer by setting the EN bit in APCS_GPT0_EN.

APCS_GPT0_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer.

0x0200A00C APCS_GPT0_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_EN register is used to enable the GPT0 timer.

APCS_GPT0_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	CLR_ON_MTCH_EN	When set (1), the timer will clear when it reaches the match value.
0	EN	When set (1), the timer is enabled and counts with frequency ACC_SLP_CLK.

0x0200A010 APCS_GPT0_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_CLR register is a one-shot command register that, when written with any value, resets the timer to a value of 0. This occurs regardless of the state of the APCS_GPT0_EN register.

APCS_GPT0_CLR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Data written is not used.

0x0200A014 APCS_GPT1_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The GPT timer will signal interrupt when its counter value has reached the value stored in the APCS_GPT1_MTCH register.

APCS_GPT1_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_GPT1_CNT at which an interrupt will be generated.

0x0200A018 APCS_GPT1_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_CNT register contains the current value of the GPT1 timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_GPT1_MTCH register at the same time. The procedure for writing the APCS_GPT1_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_GPT1_EN.
- Write APCS_GPT1_CNT.
- Write (to set/restore) APCS_GPT1_MTCH if required.
- Enable the timer by setting the EN bit in APCS_GPT1_EN.

APCS_GPT1_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer

0x0200A01C APCS_GPT1_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_EN register is used to enable the GPT1 timer.

APCS_GPT1_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	CLR_ON_MTCH_EN	When set (1), timer will clear when it reaches the match value.
0	EN	When set (1), timer is enabled and counts with frequency sleep clock.

0x0200A020 APCS_GPT1_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_CLR register is a one-shot command register that, when written with any value, resets the GPT1 timer to a value of 0. This occurs regardless of the state of the APCS_GPT1_EN register.

APCS_GPT1_CLR

Bits	Name	Description
31:0	RESERVED_BITS_31_0	Data written is not used.

0x0200A024 APCS_DGT_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The DBG timer will signal interrupt when its counter value has reached the value stored in the APCS_DGT_MTCH register.

APCS_DGT_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_DGT_CNT at which an interrupt will be generated.

0x0200A028 APCS_DGT_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CNT register contains the current value of the DGT timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_DGT_MTCH register at the same time due to HW re-use. The procedure for writing the APCS_DGT_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_DGT_EN.
- Write APCS_DGT_CNT.
- Write (to set/restore) APCS_DGT_MTCH if required.
- Enable the timer by setting the EN bit in APCS_DGT_EN.

APCS_DGT_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer count

0x0200A02C APCS_DGT_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_EN register is used to enable the DGT timer.

APCS_DGT_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	

APCS_DGT_EN (cont.)

Bits	Name	Description
1	CLR_ON_MTCH_EN	When set (1), the timer will clear when it reaches the match value.
0	EN	When set (1), the timer is enabled and counts with frequency TCXO clock.

0x0200A030 APCS_DGT_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CLR register is a one-shot command register that, when written with any value, resets the DGT timer to a value of 0. This occurs regardless of the state of the APCS_DGT_EN register.

APCS_DGT_CLR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Data written is not used.

0x0200A034 APCS_DGT_CLK_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0003

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CLK_CTL controls the clock divider inside the Debug Timer.

NOTE It is possible for the AHB clock to run at as slow as 5 MHz using settings of the Global Clock Controller. The debug timer's counter can also run at 5 MHz (TCXO divided by 4). However, due to the synchronization circuit using the edge detect, the timer should always run at least 4x slower than the AHB clock. Thus, if the timer's use is required by the system, the divider should be set to divide by 4 and the slowest usable AHB frequency is 20MHz. The timer would run at 5MHz in this case.

APCS_DGT_CLK_CTL

Bits	Name	Description
31:2	RESERVED_BITS_31_2	

APCS_DGT_CLK_CTL (cont.)

Bits	Name	Description
1:0	DIV	0x3: 4 0x2: 3 0x1: 2 0x0: 1

0x0200A038 APCS_WDT0_RST

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_RST register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset the watch dog counter. This command register also disables the watchdog freeze

APCS_WDT0_RST

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	STB	This bit generates the WDT0_STB during the non-sleep mode. A pulse is generated on WDT0_STB when this bit is written with a ’1

0x0200A03C APCS_WDT0_FRZ

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_FRZ register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the APCS_WDT0_RST register.

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

APCS_WDT0_FRZ

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved

APCS_WDT0_FRZ (cont.)

Bits	Name	Description
0	FRZ	This bit is used to freeze the watchdog timer at time 0. To enable the watchdog timer auto-kicker, write a '1'.

0x0200A040 APCS_WDT0_EN

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_EN register controls when the watch dog timer is enabled.

APCS_WDT0_EN

Bits	Name	Description
31:2	RESERVED_BITS_31_2	Reserved
1	INT_EN	Any write to this register: 0x1: yes (any unmasked IRQ or FIQ will enable the WDT0 timer.) 0x0: no
0	EN	Any write to this register: 0x1: yes (the watch dog timer is enabled) 0x0: no

0x0200A044 APCS_WDT0_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_STS register is the watchdog status register.

APCS_WDT0_STS

Bits	Name	Description
31:3	WDT_CNT	Counter value [28:0] of the watch dog counter. **NOTE** The sleep counter value is sampled using the AHB clk. Multiple reads are required to determine the value (assuming AHB clk is much faster than sleep clock).
2	WDT_RST_STS	Show the status of watchdog0 counter reset.

APCS_WDT0_STS (cont.)

Bits	Name	Description
1	AUTOKICK	This bit indicates whether the auto-kicker is on. 0x1: On 0x0: Off
0	RST_STS	0x1: wdt (the last system reset was due to WDT0) 0x0: reset (the last system reset was not due to WDT0.)

0x0200A048 APCS_WDT0_INT_WIDTH

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_INT_WIDTH register defines the width of the WDT0 biteExpired pulse in the number of sleep_clk pulses. The default value is 0x0C7C, but this reset value is not readable through the AHB interface.

APCS_WDT0_INT_WIDTH

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter value on which to de-assert the WDI bite pulse.

0x0200A04C APCS_WDT0_BARK_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (’bark’) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, but this reset value is not readable through the AHB interface. Note that this value is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (’bark’) interrupt.

APCS_WDT0_BARK_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter value on which to trigger the bark interrupt.

0x0200A050 APCS_WDT0_TST_LD_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TST_LD_STS register indicates when the watchdog test load is synchronizing to the SLP_CLK.

APCS_WDT0_TST_LD_STS

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SYNC_STS	When set (1) wdog test load is synchronizing to SLP_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x0200A054 APCS_WDT0_TST_LD

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TEST_LD register loads the WDT0_TST register value into the watchdog counter.

APCS_WDT0_TST_LD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	LD	Set on this bit to load the value into the WDT0_TST register into the WDT0 counter.

0x0200A058 APCS_WDT0_TST

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TST register indicates that the watchdog test is synchronizing to the SLP_CLK and contains the watch dog counter test load value.

APCS_WDT0_TST

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter test load value [28:0].

0x0200A05C APCS_WDT0_BITE_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_31F3

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_BITE_TIME register determines the counter value at which WDT0 asserts the biteExpired signal.

APCS_WDT0_BITE_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog bite time is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 bite expiration time [28:0].

0x0200A060 APCS_WDT1_RST

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_RST register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset the watch dog counter. This command register also disables the watchdog freeze

APCS_WDT1_RST

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	STB	This bit generates the WDT1_STB during the non-sleep mode. A pulse is generated on WDT1_STB when this bit is written with a '1'.

0x0200A064 APCS_WDT1_FRZ

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_FRZ register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the APCS_WDT1_RST register.

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

APCS_WDT1_FRZ

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	FRZ	This bit is used to freeze the watchdog timer at time 0. To enable the watchdog timer auto-kicker, write a '1'.

0x0200A068 APCS_WDT1_EN

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_EN register controls when the watchdog timer is enabled.

APCS_WDT1_EN

Bits	Name	Description
31:2	RESERVED_BITS_31_2	Reserved
1	INT_EN	Any write to this register: 0x1: yes (any unmasked IRQ or FIQ will enable the WDT0 timer.) 0x0: no
0	EN	Any write to this register: 0x1: yes (the watch dog timer is enabled) 0x0: no

0x0200A06C APCS_WDT1_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_STS register is the watchdog status register.

APCS_WDT1_STS

Bits	Name	Description
31:3	WDT_CNT	Counter value [28:0] of the watch dog counter. **NOTE** The counter value is sampled using the ahb clk. Multiple reads are required to determine the value (assuming ahb clk is much faster than sleep clock).
2	WDT_RST_STS	Show the status of watchdog counter reset.
1	AUTOKICK	This bit indicates whether the auto-kicker is on. 0x1: On 0x0: Off
0	RST_STS	0x1: wdt (the last system reset was due to WDT1) 0x0: reset (the last system reset was not due to WDT1.)

0x0200A070 APCS_WDT1_INT_WIDTH

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_INT_WIDTH register defines the width of the WDT1_expired pulse in the number of sleep_clk pulses.The default value is 0x0C7C, but this reset value is not readable through the AHB interface.

APCS_WDT1_INT_WIDTH

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter value on which to de-assert the WDI expired pulse.

0x0200A074 APCS_WDT1_BARK_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (’bark’) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, but this reset value is not readable through the AHB interface. Note that this value is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (’bark’) interrupt.

APCS_WDT1_BARK_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter value on which to trigger the bark interrupt.

0x0200A078 APCS_WDT1_TST_LD_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TST_LD_STS register indicates when the watchdog test load is synchronizing to the SLP_CLK.

APCS_WDT1_TST_LD_STS

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SYNC_STS	When set (1) wdog test load is synchronizing to SLP_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x0200A07C APCS_WDT1_TST_LD

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TEST_LD register loads the WDT1_TST register value into the watchdog counter.

APCS_WDT1_TST_LD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	LD	Set on this bit to load the value into the WDT1_TST register into the WDT counter

0x0200A080 APCS_WDT1_TST

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TST register indicates that the watchdog test is synchronizing to the SLP_CLK and contains the watch dog counter test load value.

APCS_WDT1_TST

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter test load value [28:0]

0x0200A084 APCS_WDT1_BITE_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_31F3

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_BITE_TIME register determines the counter value at which WDT1 asserts the biteExpired signal.

APCS_WDT1_BITE_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog bite time is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 bite expiration time [28:0].

0x0200A088 APCS_TMR_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [WDT0, WDT1, GPT0, GPT1, DGT].

The APCS_TMR_STS can be used to determine the status of each of the SCSS timers in the timer's resident clock domain. Since the timer clock domain may be much slower than the AHB clock, AHB transactions may be delayed in taking effect. This information can be used to qualify other actions or used simply for debug purposes. For example, software can determine when a write to APCS_DGT_CLR has taken effect by examining the DGT_CLR_PEND bit.

Each timer's bits are receive security treatment as specified by the APCS_TMRSECURE register.

APCS_TMR_STS

Bits	Name	Description
31	RESERVED_BIT31	
30	WDT1_AUTOKICK	Auto-kicker is on (1) or off (0)
29	WDT1_INT_EN	An unmasked interrupt will enable the timer (1) or not (0)
28	WDT1_EN	Timer is enabled (1) or not (0)
27	RESERVED_BIT27	
26	WDT0_AUTOKICK	Auto-kicker is on (1) or off (0)

APCS_TMR_STS (cont.)

Bits	Name	Description
25	WDT0_INT_EN	An unmasked interrupt will enable the timer (1) or not (0)
24	WDT0_EN	Timer is enabled (1) or not (0)
23:20	RESERVED_BIT20_23	
19	GPT1_WR_PEND	Timer has a write pending (1) or not (0)
18	GPT1_CLR_PEND	Timer has a clear pending (1) or not (0)
17	GPT1_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
16	GPT1_EN	Timer is enabled (1) or not (0)
15:12	RESERVED_BITS15_12	
11	GPT0_WR_PEND	Timer has a write pending (1) or not (0)
10	GPT0_CLR_PEND	Timer has a clear pending (1) or not (0)
9	GPT0_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
8	GPT0_EN	Timer is enabled (1) or not (0)
7:4	RESERVED_BITS7_4	
3	DGT_WR_PEND	Timer has a write pending (1) or not (0)
2	DGT_CLR_PEND	Timer has a clear pending (1) or not (0)
1	DGT_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
0	DGT_EN	Timer is enabled (1) or not (0)

11.9 KPSS GLB Registers (0x02010000 APCS_GLB_BASE)

This section contains the Krait Processor Subsystem (KPSS) GLB Secure registers.

0x02010000 APCS_GLBSECURE

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0001

Security Treatment: Restricted

The APCS_GLBSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Krait's APROTNS pin. When APROTNS is set to '0' the state of the APCS_GLBSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_GLBSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_GLBSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_GCCSECURE register correspond to.

APCS_GLBSECURE

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	GLB_CTL	Controls security treatment for the global control registers: APCS_START_ADDR. 0x1: NSEC 0x0: SEC

0x02010004 APCS_START_ADDR

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: {START_ADDR, 0x0000}

Security Treatment: Controlled by APCS_GLBSECURE[GLB_CTL].

The APCS_START_ADDR register is used to determine the address to boot from. It resets to the value on START_ADDR PARAMETER.Reset by SYS_apcsSYSPor_Ares|SYS_apcsSys_Ares

APCS_START_ADDR

Bits	Name	Description
31:16	ADDR	Start address for the Krait

APCS_START_ADDR (cont.)

Bits	Name	Description
15:0	RESERVED_BITS15_0	

11.10 KPSS L2 SAW2 Registers (0x02012000 APCS_L2_GDHS_BASE)

This section contains the Krait Processor Subsystem (KPSS) L2 SAW2 registers.

The SAW2 (SPM and AVS. Wrapper2) design is an AHB slave that contains both SPM and AVS. CSRs.

0x02012000 APCS_L2_SAW2_SECURE

Type: Read/write
Clock: SYS_REF_CLK
Reset State: {3{CFGNSINIT}}

Security Treatment: Restricted

The SAW2_SECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by ahb_saw_hprotns pin. When ahb_saw_hprotns is set to ’0’ the state of the SAW2_SECURE register is not considered - a secure transaction is always allowed. When ahb_saw_hprotns is set to ’1’, the SAW2_SECURE register security treatment bit of that register must be ’1’ for access to be granted. If the security treatment bit of the register is set to ’0’, the non-secure (ahb_saw_hprotns = ’1’) transactions are denied. When access is denied, a write is ignored, and a read will return ’0’. No error is signaled.

When reading the SAW2_SECURE register, non secure agents will always read ’0’. Secure agents will see the actual value of the register. The reset value is controlled by CFGNSINIT input pin.

APCS_L2_SAW2_SECURE

Bits	Name	Description
31:3	RESERVED	
2	SAW_CTL	Controls security treatment for SAW2 registers: SAW2_ID, SAW2_CFG, SAW2_STS_0, SAW2_STS_1, SAW2_RST 0x1: NSEC 0x0: SEC
1	PWR_CTL	Controls security treatment for SPM registers: SAW2_SPM_CTL, SAW2_SPM_PMIC_DLY, SAW2_SPM_PMIC_DATA_0, SAW2_SPM_PMIC_DATA_1, SAW2_SPM_SLP_SEQ_ENTRY_n, SAW2_SPM_DLY 0x1: NSEC 0x0: SEC
0	VLT_CTL	Controls security treatment for the AVS. registers: SAW2_AVS_CTL, SAW2_VLVL, SAW2_AVS_HYSTERESIS 0x1: NSEC 0x0: SEC

0x02012004 APCS_L2_SAW2_ID

Type: Read
Clock: SYS_REF_CLK
Reset State: Undefined

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register reports the revision and parameter information for the SAW2 core.

APCS_L2_SAW2_ID

Bits	Name	Description
31	RESERVED_BITS31	
30:25	NUM_SPM_ENTRY	SAW2 parameter: Indicates number of SAW2_SPM_SLP_SEQ_ENTRY register implemented. Value can range from 1 - 32
24:20	NUM_PWR_CTL	SAW2 parameter: Indicates number of power control implemented. Value can range from 2 - 16
19	RESERVED_BITS19	
18	PMIC_ARB_INTF	SAW2 parameter: Indicates PMIC Arbiter Interface function is implemented
17	AVS_PRESENT	SAW2 parameter: Indicates AVS. function is implemented
16	SPM_PRESENT	SAW2 parameter: Indicates SPM function is implemented
15:12	MAJOR	Major variant
11:0	MINOR	Minor variant

0x02012008 APCS_L2_SAW2_CFG

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_CFG register is used to configure the common control between AVS. and SPM.system.

APCS_L2_SAW2_CFG

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12	FRC_REF_CLK_ON	Chicken bit to force saw_sys_ref_clk_on_req ON.
11:8	ADR_IDX	PMIC Arbiter Address Index. Drive the saw_pmic_addr_idx output port.

APCS_L2_SAW2_CFG (cont.)

Bits	Name	Description
7:6	RESERVED_BITS7_6	
5	PMIC_MODE	PMIC Handshake 0x0: 8K_PMIC (only DONE signal) 0x1: 7K_PMIC (both ACK and DONE signals)
4:0	CLK_DIV	Divider ratio for clock. This is used to generate timer tick for the timer. Timer tick is asserted every (CLK_DIV + 1) sys_ref_clk period. ..... For sys_ref_clk = 20 MHz (53ns) The timer tick range 53 ns to 1.6us. 0x0: Timer Tick every sys_ref_clk 0x1F: Timer Tick every 128 sys_ref_clk.

0x0201200C APCS_L2_SAW2_STS_0

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

APCS_L2_SAW2_STS_0

Bits	Name	Description
15	SHTDWN_REQ	This bit reflects the shutdown request from the SPM(spm_rpm_shutdown_req) to RPM.
14	SHTDWN_ACK	This bit reflects the shutdown acknowledgement from the RPM(rpm_spm_shutdown_ack) to SPM.
13	BRNGUP_REQ	This bit reflects the bringup request from the SPM(spm_rpm_bringup_req) to RPM.
12	BRNGUP_ACK	This bit reflects the bringup acknowledgement from the RPM(rpm_spm_bringup_ack) to SPM.
11:10	PMIC_STATE	State of the PMIC FSM: transitions back to IDLE) transitions back to IDLE) 0x0: IDLE (waiting for PMIC transaction from AVS. or SPM) 0x1: ACK (waiting for ACK from PMIC Arb) 0x2: DONE (waiting for DONE form PMIC Arb before) 0x3: DELAY (waiting for delay count termination before)

APCS_L2_SAW2_STS_0 (cont.)

Bits	Name	Description
9:8	RPM_STATE	State of the RPM FSM: 0x0: RUN (waiting for SPM request) 0x1: STDNACK (waiting for shutdown ACK from RPM) 0x2: WAKEUP (waiting for wakeup interrupt) 0x3: BGUPACK (waiting for bringup ACK from RPM)
7	AVS_STATE	State of the AVS. FSM: indication) 0x0: IDLE (waiting to be enabled or for next UP/DOWN) 0x1: REQ (waiting for PMIC FSM to transition to IDLE)
6:0	SPM_CMD_ADDR	Last SPM command executed.

0x02012010 APCS_L2_SAW2_STS_1

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

APCS_L2_SAW2_STS_1

Bits	Name	Description
31	RESERVED1	
30	SW_WR_PEND	This bit reflects the VLVL state of the request from the SAW2_VCTL write is pending.
29	CPU_UP	This bit reflects the VLVL state of the request from the CPU (avs_saw_up) to raise the VLVL.
28	CPU_DN	This bit reflects the VLVL state of the request from the CPU (avs_saw_down) to lower the VLVL.
27	MAX_INT	IRQ status bit, AVS. controller detected that raising the VLVL by AVS_CTL[VLVL_STEP] would result in a value greater than AVS_CTL[MAX_VLVL]. If AVS_CTL[IRQ_MAX_EN] is set, an interrupt is issued. NOTE that SW can set MAX_VLVL lower than current VLVL creating a condition where VLVL is higher than MAX_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MAX.

APCS_L2_SAW2_STS_1 (cont.)

Bits	Name	Description
26	MIN_INT	IRQ status bit, AVS. controller detected that lowering the VLVL by SAW2_AVS_CTL[VLVL_STEP] would result in a value less than SAW2_AVS_CTL[MIN_VLVL]. If SAW2_AVS_CTL[IRQ_MIN_EN] is set, an interrupt is issued. NOTE that SW can set MIN_VLVL higher than current VLVL creating a condition where VLVL is lower than MIN_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MIN.
25:16	CURR_DLY	VLVL value of the counter used to calculate the time until the next AVS. controller request for a new VLVL.

0x02012014 APCS_L2_SAW2_VCTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

Though this register is read/writable, it also causes a command pulse to the PMIC FSM. Writing this register results in a transaction to the PMIC with SAW2_VCTL being sent to the PMIC. SAW2 support both 8901 and 8058 regulator.

APCS_L2_SAW2_VCTL

Bits	Name	Description
31:16	RESERVED_BITS31_16	

0x02012018 APCS_L2_SAW2_AVS_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_CTL register is used to control the Adaptive Voltage Scaling (AVS) system.

APCS_L2_SAW2_AVS_CTL

Bits	Name	Description
31	RESERVED	

APCS_L2_SAW2_AVS_CTL (cont.)

Bits	Name	Description
30	VLVL_WIDTH	Defines the VLVL field of PMIC data. SAW2 at minimum supports 8901 and 8058 regulator. See PMIC document for details. 0x0: 5 bits VLVL (8058 regulator) 0x1: 6 bits VLVL (8901 regulator)
29:28	VLVL_STEP	Controls the step size of each request to PMIC Arbiter. SW may use values from 0 to 3. Note that the value 0 will result in no change - that is if the CPU requests UP or DOWN, the CURR_PVLVL will be sent to the PMIC Arbiter. This may be useful for debug. If an increment or decrement operation would cause the current VLVL to transition above or below the MAX_VLVL or MIN_VLVL, the current VLVL will not be changed. An interrupt will be signaled if IRQ_MAX/MIN_EN is 1
27	EN	AVS. Enable. **NOTE** Setting to 0 does not disable any pending interrupts. **NOTE** AVS. FSM and SPM FSM are mutually exclusive. Only one FSM is active at a time. SW does not have to disable AVS. before going to sleep. 0x0: Disable AVS 0x1: Enable AVS
26	SW_DONE_INT_EN	Set to 1 to turn on AVS. interrupt for when a SW initiated voltage change has completed. Set to 0 to mask it (turn it off). ASSERTION: This interrupt is asserted only after a SW write to SAW2_AVS_VLVL. Specifically, after the AVS. FSM traverses through all its states and transitions back to IDLE, the interrupt line is pulsed. The interrupt controller should be set to edge capture to receive this interrupt. CLEARING: None. This interrupt is a pulse, SW does not need to clear it (aside from requirements of the interrupt controller).
25	MAX_INT_EN	Set to 1 to turn on AVS. interrupt for MAX_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be greater than MAX_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit.
24	MIN_INT_EN	Set to 1 to turn on AVS. interrupt for MIN_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be smaller than MIN_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit
23	RESERVED_23	

APCS_L2_SAW2_AVS_CTL (cont.)

Bits	Name	Description
22:17	MAX_VLVL	Control maximum value of AVS. controller's VLVL. When current VLVL reaches this value it may not grow any larger. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level higher, an interrupt is issued. This value may be updated at anytime. Setting to a value lower than MIN_VLVL is not supported, and unpredictable results may occur.
16	RESERVED_16	
15:10	MIN_VLVL	Control the minimum value of AVS. controller's VLVL. When the current VLVL reaches this level it may not shrink any smaller. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level lower, an interrupt is issued. This value may be updated at anytime. Setting to a value higher than MAX_VLVL is not supported, and unpredictable results may occur.
9:0	AVS_DELAY	Control the time between AVS. controller's requests to change the VLVL

0x0201201C APCS_L2_SAW2_AVS_HYSTERESIS

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_HYSTERESIS register is used to delay the AVS. UP/DN signal to AVS. FSM. This is used to prevent the false PMIC step due to PDN noise.

APCS_L2_SAW2_AVS_HYSTERESIS

Bits	Name	Description
31:24	RESERVED31_24	
23:16	DN_COUNT	HYSTERESIS DN COUNT. Delays of PMIC DN step operation.
15:8	RESERVED15_8	
7:0	UP_COUNT	HYSTERESIS UP COUNT. Delays of PMIC UP step operation.

0x02012020 APCS_L2_SAW2_SPM_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_CTL register is used to control the subsystem power management system. This are parameters that controls the operation of SPM FSM.

APCS_L2_SAW2_SPM_CTL

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	SPM_START_ADR	Start address for the SPM sequence.
3	ISAR	Inhibit Start Address Reset 0x0: End of program reset the SPM_START_ADR to zero. 0x1: Inhibit End of program to reset SPM_START_ADR
2:1	WAKEUP_CONFIG	Wakeup Configuration 0x0: sys_spm_wakeup 0x1: sys_spm_wakeup or !cpu_spm_wait_req 0x2: sys_spm_wakeup or rising edge of sys_spm_dbg_nopwrdwn 0x3: sys_spm_wakeup or !cpu_spm_wait_req or rising edge of sys_spm_dbg_nopwrdwn
0	SPM_EN	SPM En.

0x02012024 APCS_L2_SAW2_SPM_PMIC_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC delay values after SPM FSM PMIC transaction. SPM wait for the programmed delay before executing the next SPM command.

APCS_L2_SAW2_SPM_PMIC_DLY

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:24	DATA_1_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
23:19	RESERVED_BITS23_19	
18:16	DATA_1_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
15:11	RESERVED_BITS15_11	

APCS_L2_SAW2_SPM_PMIC_DLY (cont.)

Bits	Name	Description
10:8	DATA_0_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
7:3	RESERVED_BITS7_3	
2:0	DATA_0_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms

0x02012028 APCS_L2_SAW2_SPM_PMIC_DATA_0

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

APCS_L2_SAW2_SPM_PMIC_DATA_0

Bits	Name	Description

0x0201202C APCS_L2_SAW2_SPM_PMIC_DATA_1

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

APCS_L2_SAW2_SPM_PMIC_DATA_1

Bits	Name	Description

0x02012030 APCS_L2_SAW2_RST

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_RST register is used to reset the SAW logic. This register clear itself. It does not reset any SAW2 CSR's. It reset AVS. and SPM FSM and control registers. This is use to clear any hang condition.

APCS_L2_SAW2_RST

Bits	Name	Description
31:1	RESERVED31_1	
0	RST	Reset AVS. and SPM FSM and control registers.

0x02012034 APCS_L2_SAW2_SPM_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the delay values for SPM Delay command. SPM wait for the programmed delay before executing the next SPM command.

APCS_L2_SAW2_SPM_DLY

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:20	DLY3	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
19:10	DLY2	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
9:0	DLY1	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms

0x02012080+4*n APCS_L2_SAW2_SPM_SLP_SEQ_ENTRY_n

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_SLP_SEQ_ENTRY_n is an array used to sequence through the steps during various power mode. The register width is defined by CLOG_PWR_CTL parameter.

APCS_L2_SAW2_SPM_SLP_SEQ_ENTRY_n

Bits	Name	Description

11.11 KPSS XPU Registers (0x02013000 APCS_L2_MPU_BASE)

This section contains the Krait Processor Subsystem (KPSS) XPU registers.

0x02013000+4*n APCS_MPU_PRTn_RACR, n=[0..31]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU. These registers include a single bit per VMID granting read access

APCS_MPU_PRTn_RACR

Bits	Name	Description
31:0	RE	Read enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read access to the registers in the associated resource group.

0x02013400+4*n APCS_MPU_PRTn_WACR, n=[0..31]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

These registers exist only for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU.

APCS_MPU_PRTn_WACR

Bits	Name	Description
31:0	WE	Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID write access to the registers in the associated resource group.

0x02013800+4*n APCS_MPU_PRTn_START, n=[0..31]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition Start Address Register. This register contains the start address of the partition. Only the bit numbers indicated by MPU_IDR[MSb] through MPU_IDR[LSb] are valid and physically exist.

APCS_MPU_PRTn_START

Bits	Name	Description
31:12	ADDR	MPU Partition Start Address
11:0	RESERVED_11_0	Reserved

0x02013C00+4*n APCS_MPU_PRTn_END, n=[0..31]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition End Address Register. This register contains the start address of the partition.Only the bit numbers indicated by MPU_IDR[MSB] through MPU_IDR[LSB] are valid and physically exist.

APCS_MPU_PRTn_END

Bits	Name	Description
31:12	ADDR	MPU Partition End Address
11:0	RESERVED_11_0	Reserved

0x02013F80 APCS_MPU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Configuration Register: This register includes fields governing various MPU behaviors.

APCS_MPU_CR

Bits	Name	Description
31:2	RESERVED31_2	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set MPU_ESR. MPU_EAR and MPU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set MPU_ESR. MPU_EAR and MPU_ESYNR0 updated with address and syndrome of error.

APCS_MPU_CR (cont.)

Bits	Name	Description
2	MPUEIE	MPU Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the MPU. Interrupt output is asserted if MPU_CR[MPUEIE] = 1 and any bit is set in MPU_ESR.
1	MPUERE	MPU Error Report Enable. MPUERE = 0 causes the MPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master. MPUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective MPU port. Errors from either port are terminated by the MPU as RAZ/WI Both client and configuration port errors are recorded in MPU_ESR, independent of the value of MPU_CR[MPUERE]
0	MPUE	MPU Enable. Governs whether MPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures MPU and the MID to VMID mapping tables.

0x02013F84 APCS_MPU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the MPU, for both the client port and the configuration port. Client port addresses are 32 bits width and configuration port addresses are 12 bits wide (the width of the configuration address port).

APCS_MPU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x02013F88 APCS_MPU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the MPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and

leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the MPU's interrupt output (when enabled by MPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the MPU_ESYNRn registers, which are merely the "syndrome" of an error indicated by MPU_ESR.

APCS_MPU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x02013F8C APCS_MPU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Restore Register. This register is an aliased address for the MPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

APCS_MPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x02013F90 APCS_MPU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

APCS_MPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x02013F94 APCS_MPU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

APCS_MPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved

APCS_MPU_ESYNR1 (cont.)

Bits	Name	Description
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x02013FF4 APCS_MPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

MPU Revision Register: This register provides major/minor revision codes for the implementation.

APCS_MPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x02013FF8 APCS_MPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x1F0C2C1F

MPU ID Register: Read-only register that defines various configuration attributes of the MPU instance.

APCS_MPU_IDR

Bits	Name	Description
31:29	RESERVED31_29	Reserved
28:24	MSB	Indicates most significant address bit number used in START/END address comparisons.
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used in START/END address comparisons.
15:14	RESERVED15_12	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only MPU_PRTn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate MPU_PRTn_RACR and MPU_PRTn_WACR registers govern read vs. write access. For single VMID, MPU_PRTn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. MPU_PRTn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMD type access control. MPU_PRTn_xACR registers include separate bit per VMID (32 bits) for governing access.
9	RESERVED9	Reserved
8:0	NPRT	Number of partitions. Indicates the number of partitions (minus 1) supported by the MPU. Values range from 0-223 (1-224 partitions)

0x02013FFC APCS_MPU_MPU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

MPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the MPU (including the MPU_MPU_ACR itself).

APCS_MPU_MPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the MPU's 4KB address region (including the MPU_MPU_ACR itself). For single VMID type MPUs (MPU_IDR[MV] = 0) the MPU_MPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

11.12 KPSS Base Offset Registers (0x02100000 APCS_HSEL_BASE)

This section contains the Krait Processor Subsystem (KPSS) Base Offset registers.

0x02100000 APCS_QGIC

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: NA.

APCS_QGIC

Bits	Name	Description
14:2	ADDR	These are the bits needed to address the generic interrupt controller registers.

0x02108000 APCS_ACC

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: NA

APCS_ACC

Bits	Name	Description
5:2	ADDR	These are the bits needed to address the ACC registers

0x02109000 APCS_SAW2

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: NA

APCS_SAW2

Bits	Name	Description
7:2	ADDR	These are the bits needed to address the SAW registers

0x0210A000 APCS_TMR

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: NA

APCS_TMR

Bits	Name	Description
7:2	ADDR	These are the bits needed to address the TMR registers

0x02110000 APCS_GLB

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: NA

APCS_GLB

Bits	Name	Description
6:2	ADDR	These are the bits needed to address the GLB registers

0x02111000 APCS_GCC

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: NA

x1_2000

APCS_L2_GDHS

7:2	ADDR	These are the bits needed to address the SAW2 registers for L2 GDHS

APCS_GCC

Bits	Name	Description
6:2	ADDR	These are the bits needed to address the GCC registers

0x02113000 APCS_L2_MPU

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: NA

This is the base address of the AHB slave in the MPU.

APCS_L2_MPU

Bits	Name	Description

0x02180000 APCS_EXT_MSTR_ALIAS0

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: NA

This is the aliased address to access CPU0's private peripherals from an external master.

APCS_EXT_MSTR_ALIAS0

Bits	Name	Description

0x02190000 APCS_EXT_MSTR_ALIAS1

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: NA

This is the aliased address to access CPU1's private peripherals from an external master.

APCS_EXT_MSTR_ALIAS1

Bits	Name	Description

0x021A0000 APCS_EXT_MSTR_ALIAS2

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: NA

This is the aliased address to access CPU2's private peripherals from an external master.

APCS_EXT_MSTR_ALIAS2

Bits	Name	Description

0x021B0000 APCS_EXT_MSTR_ALIAS3

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: NA

This is the aliased address to access CPU3's private peripherals from an external master.

APCS_EXT_MSTR_ALIAS3

Bits	Name	Description

11.13 KPSS ACC Registers (0x02088000 CPU0_APCS_ACC_BASE)

This section contains the Krait Processor Subsystem (KPSS) CPU0 ACC registers.

0x02088000 CPU0_APCS_ACCSECURE

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0007

Security Treatment: Restricted

The APCS_ACCSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Krait's APROTNS pin. When APROTNS is set to '0' the state of the APCS_ACCSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_ACCSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_ACCSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_ACCSECURE register correspond to.

CPU0_APCS_ACCSECURE

Bits	Name	Description
31:4	RESERVED	
31:3	RESERVED_BITS31_3	
2	TST	Controls security treatment for test control registers: APCS_ATSTBUS_SEL 0x1: NSEC 0x0: SEC
1	CLK_CTL	Controls security treatment for the clock control registers: APCS_ACC_STS, APCS_CPU_AUX_CLK_SEL. 0x1: NSEC 0x0: SEC
0	SLP_CTL	Controls security treatment for the sleep control registers: APCS_CPU_PWR_CTL, APCS_CPU_TRGTD_DBG_RST. 0x1: NSEC 0x0: SEC

0x02088004 CPU0_APCS_CPU_PWR_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0109

Security Treatment: Controlled by APCS_ACCSECURE [SLP_CTL].

The APCS_CPU_PWR_CTL register is used to control the clamps, reset and array head switches.

CPU0_APCS_CPU_PWR_CTL

Bits	Name	Description
31:21	RESERVED_BITS31_21	
20:16	CLK_EN	Clock enables for CORE clock. This is only to workaround hardware dynamic clock gating problems. [20:18]= SYS_apcNAux_Clk[3:1] [17] = SYS_apcsRef_Clk [16] = SYS_apcNPll_Clk 0x1: Always enabled 0x0: dynamically enabled by hardware
15:10	RESERVED_BITS15_10	
9	RET_SLP_REQ	When set, this bit request the L2SCU to in-flight snoop operation and block new snoops request from entering FIFO. This control is intended to permit external masters such as the RPM to put CPU to retention sleep modes, when power control is being done by an external master instead of the SPM. The output of this register bit is ORed with a retention sleep request control output from the SPM, so that if either the SPM asserts the control, or the RPM sets this bit, the CPU's snoop FIFO is quiesce.
8	PLL_CLAMP	When set, this bit clamp the output of TDC logic in PLL. This signal that must be asserted prior to collapsing CPU voltage, vdd_apc0. This bit is ORed with SAW output before passing to the APC PLL.
7	CORE_PWRD_UP	Report that the CPU is powered up.
6	GATE_CLK	When set, this bit forces the CPU clock to be gated off. This control is intended to permit external masters such as the RPM to gate off the CPU clock during sleep modes, when power control is being done by an external master instead of the SPM. The output of this register bit is ORed with a clock gating control output from the SPM, so that if either the SPM asserts the control, or the RPM sets this bit, the CPU clock will be gated off. When set, this bit gate the CPU clock that must be asserted during sleep state. This bit is ORed with a SAW output before passing to the CPU core.
5	COREPOR_RST	When set, this bit asserts corepor areset to the CPU core.
4	CORE_RST	When set, this bit asserts core areset to the COPU core.

CPU0_APCS_CPU_PWR_CTL (cont.)

Bits	Name	Description
3	L2DT_SLP	When set, this bit opens a head switch to put the L2 duplicate tag array into a low-leakage, non-data-retaining state. This bit is ORed with a SAW output before passing to the CPU core. The controlled memory array contains a duplicate of the tags contained in the L1 data cache, and is used by the L2 to snoop and see if a shared memory access from one processor necessitates invalidating a line in another processor's L1 data cache. Thus, this memory array generally can be offline when the associated CPU is power-collapsed and its L1 data cache is also off-line.
2	RESERVED_BIT2	Previously ETB HS
1	RESERVED_BIT1	Previously L1 HS
0	CLAMP	When set, this bit asserts the clamp signal that must be asserted prior to collapsing CPU voltage, vdd_apc0. This bit is ORed with SAW output before passing to the CPU core.

0x02088008 CPU0_APCS_ACC_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: N/A

Security Treatment: Controlled by APCS_ACCSECURE [CLK_CTL].

The APCS_ACC_STS register is used to monitor the output of the clock gating cells.

CPU0_APCS_ACC_STS

Bits	Name	Description
31:18	RESERVED_BITS31_18	
17	RET_SLP_ACK	This bit reflect the status of APCN_sysRetSlpAck bit. L2 assert the signal when it see the APCN_sysRetSlpReq and CPU snoop FIFO is quiesced. L2 de-assert this signal after APCN_sysRetSlpReq is de-asserted and all snoop invalidation is completed.
16	SLP_CLK	This bit reflect the status of APCN_sleepClkOnReq bit
15	AHB_CLK	This bit reflect the status of APCN_ahbClkOnReq bit
14	REF_CLK	This bit reflect the status of APCN_refClkOnReq bit
13	SPM_SLP_STATE	This bit reflect the status of SPM Sleep State
12	FRC_CLK_OFF	This bit reflect the status of APCN_apccForceClocksOff bit
11	RET_SLP_REQ	This bit reflect the status of APCN_apccRetSlpReq bit
10	TRGTD_DBG_RST	This bit reflect the status of APCN_apcTargetedDbg_Areset_N bit
9	CORE_RST	This bit reflect the status of APCN_apccCore_Areset_N bit
8	COREPOR_RST	This bit reflect the status of APCN_apccCorePor_Areset_N bit

CPU0_APCS_ACC_STS (cont.)

Bits	Name	Description
7	L2DT_HS	This bit reflect the status of the SYS_apcNSwCtlDupTagArrayCollapse bit
6	CLAMP	This bit reflect the status of the SYS_apcNClampApcNvd bit.
5:3	CORE_AUX_CLK	This bits reflect the status of the APCS_sysApcNAuxClkOnReq bits.
2	CORE_PLL_CLK	This bit reflect the status of the APCS_sysApcNPllClkOnReq bit.
1	CORE_NO_PWR_DWN	This bit reflect the status of the APCN_dbgCoreNoPwrDwn bits.
0	CORE_PWRUP_REQ	This bit reflect the status of the APCN_dbgCorePwrUpReq bits.

0x0208800C CPU0_APCS_ATSTBUS_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [TST].

APCS_ATSTBUS_SEL selects different modules' test bus outputs.

CPU0_APCS_ATSTBUS_SEL

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	EN	Set to 1 to cause APCS to drive the test bus outputs. 0x1: enabled 0x0: disabled
1:0	SEL	0x3: CONSTANT 0x2: SAW 0x1: TMR 0x0: CLK

0x02088010 CPU0_APCS_CPU_TRGTD_DBG_RST

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [SLP_CTL].

APCS_CPU_TRGTD_DBG_RST is used to reset the CPU core debug logic. The hardware clear the register after the CPU debug logic is reset. Software need to poll this register to check if the reset is complete.

CPU0_APCS_CPU_TRGTD_DBG_RST

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	RST	When set this bit de-assert SYS_apcNTargetedDbg_Areset_N to the CPU core for 32 REF clock cycle to the CPU core. At the end of the reset hardware clear this bit.

0x02088014 CPU0_APCS_CPU_AUX_CLK_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [CLK_CTL]

The APCS_CPU_AUX_CLK_SEL register controls the gfmux which selects the AUX clock source for the Krait CPU clock. An additional selection set is provided to determine the clock source for the Krait core (4-1 GFMUX) in the Krait Hard Macro. The QSB clock is the raw source clk at reset.

CPU0_APCS_CPU_AUX_CLK_SEL

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	AUX_SRC	Krait CPU AUX clock select: 0x3: SYS_apcNAux_Clk_1 0x2: SYS_apcNAux_Clk_2 0x1: SYS_apcNAux_Clk_3 0x0: SYS_apcsRef_Clk

11.14 KPSS CPU0 SAW2 Registers (0x02089000 CPU0_APCS_SAW2_BASE)

This section contains the Krait Processor Subsystem (KPSS) CPU0 SAW2 registers.

The SAW2 (SPM and AVS. Wrapper2) design is an AHB slave that contains both SPM and AVS. CSRs.

0x02089000 CPU0_APCS_SAW2_SECURE

Type: Read/write
Clock: SYS_REF_CLK
Reset State: {3{CFGNSINIT}}

Security Treatment: Restricted

The SAW2_SECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by ahb_saw_hprotns pin. When ahb_saw_hprotns is set to ‘0’ the state of the SAW2_SECURE register is not considered - a secure transaction is always allowed. When ahb_saw_hprotns is set to ‘1’, the SAW2_SECURE register security treatment bit of that register must be ‘1’ for access to be granted. If the security treatment bit of the register is set to ‘0’, the non-secure (ahb_saw_hprotns = ‘1’) transactions are denied. When access is denied, a write is ignored, and a read will return ‘0’. No error is signaled.

When reading the SAW2_SECURE register, non-secure agents will always read ‘0’. Secure agents will see the actual value of the register. The reset value is controlled by CFGNSINIT input pin.

CPU0_APCS_SAW2_SECURE

Bits	Name	Description
31:3	RESERVED	
2	SAW_CTL	Controls security treatment for SAW2 registers: SAW2_ID, SAW2_CFG, SAW2_STS_0, SAW2_STS_1, SAW2_RST 0x1: NSEC 0x0: SEC
1	PWR_CTL	Controls security treatment for SPM registers: SAW2_SPM_CTL, SAW2_SPM_PMIC_DLY, SAW2_SPM_PMIC_DATA_0, SAW2_SPM_PMIC_DATA_1, SAW2_SPM_SLP_SEQ_ENTRY_n, SAW2_SPM_DLY 0x1: NSEC 0x0: SEC
0	VLT_CTL	Controls security treatment for the AVS. registers: SAW2_AVS_CTL, SAW2_VLVL, SAW2_AVS_HYSTERESIS 0x1: NSEC 0x0: SEC

0x02089004 CPU0_APCS_SAW2_ID

Type: Read
Clock: SYS_REF_CLK
Reset State: Undefined

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register reports the revision and parameter information for the SAW2 core.

CPU0_APCS_SAW2_ID

Bits	Name	Description
31	RESERVED_BITS31	
30:25	NUM_SPM_ENTRY	SAW2 parameter: Indicates number of SAW2_SPM_SLP_SEQ_ENTRY register implemented. Value can range from 1 - 32
24:20	NUM_PWR_CTL	SAW2 parameter: Indicates number of power control implemented. Value can range from 2 - 16
19	RESERVED_BITS19	
18	PMIC_ARB_INTF	SAW2 parameter: Indicates PMIC Arbiter Interface function is implemented
17	AVS_PRESENT	SAW2 parameter: Indicates AVS. function is implemented
16	SPM_PRESENT	SAW2 parameter: Indicates SPM function is implemented
15:12	MAJOR	Major variant
11:0	MINOR	Minor variant

0x02089008 CPU0_APCS_SAW2_CFG

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_CFG register is used to configure the common control between AVS. and SPM.system.

CPU0_APCS_SAW2_CFG

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12	FRC_REF_CLK_ON	Chicken bit to force saw_sys_ref_clk_on_req ON.
11:8	ADR_IDX	PMIC Arbiter Address Index. Drive the saw_pmic_addr_idx output port.

CPU0_APCS_SAW2_CFG (cont.)

Bits	Name	Description
7:6	RESERVED_BITS7_6	
5	PMIC_MODE	PMIC Handshake 0x0: 8K_PMIC (only DONE signal) 0x1: 7K_PMIC (both ACK and DONE signals)
4:0	CLK_DIV	Divider ratio for clock. This is used to generate timer tick for the timer. Timer tick is asserted every (CLK_DIV + 1) sys_ref_clk period. ..... For sys_ref_clk = 20 MHz (53ns) The timer tick range 53 ns to 1.6us. 0x0: Timer Tick every sys_ref_clk 0x1F: Timer Tick every 128 sys_ref_clk.

0x0208900C CPU0_APCS_SAW2_STS_0

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

CPU0_APCS_SAW2_STS_0

Bits	Name	Description
15	SHTDWN_REQ	This bit reflects the shutdown request from the SPM(spm_rpm_shutdown_req) to RPM.
14	SHTDWN_ACK	This bit reflects the shutdown acknowledgement from the RPM(rpm_spm_shutdown_ack) to SPM.
13	BRNGUP_REQ	This bit reflects the bringup request from the SPM(spm_rpm_bringup_req) to RPM.
12	BRNGUP_ACK	This bit reflects the bringup acknowledgement from the RPM(rpm_spm_bringup_ack) to SPM.
11:10	PMIC_STATE	State of the PMIC FSM: transitions back to IDLE) transitions back to IDLE) 0x0: IDLE (waiting for PMIC transaction from AVS. or SPM) 0x1: ACK (waiting for ACK from PMIC Arb) 0x2: DONE (waiting for DONE form PMIC Arb before) 0x3: DELAY (waiting for delay count termination before)

CPU0_APCS_SAW2_STS_0 (cont.)

Bits	Name	Description
9:8	RPM_STATE	State of the RPM FSM: 0x0: RUN (waiting for SPM request) 0x1: STDNACK (waiting for shutdown ACK from RPM) 0x2: WAKEUP (waiting for wakeup interrupt) 0x3: BGUPACK (waiting for bringup ACK from RPM)
7	AVS_STATE	State of the AVS. FSM: indication) 0x0: IDLE (waiting to be enabled or for next UP/DOWN) 0x1: REQ (waiting for PMIC FSM to transition to IDLE)
6:0	SPM_CMD_ADDR	Last SPM command executed.

0x02089010 CPU0_APCS_SAW2_STS_1

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

CPU0_APCS_SAW2_STS_1

Bits	Name	Description
31	RESERVED1	
30	SW_WR_PEND	This bit reflects the VLVL state of the request from the SAW2_VCTL write is pending.
29	CPU_UP	This bit reflects the VLVL state of the request from the CPU (avs_saw_up) to raise the VLVL.
28	CPU_DN	This bit reflects the VLVL state of the request from the CPU (avs_saw_down) to lower the VLVL.
27	MAX_INT	IRQ status bit, AVS. controller detected that raising the VLVL by AVS_CTL[VLVL_STEP] would result in a value greater than AVS_CTL[MAX_VLVL]. If AVS_CTL[IRQ_MAX_EN] is set, an interrupt is issued. NOTE that SW can set MAX_VLVL lower than current VLVL creating a condition where VLVL is higher than MAX_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MAX.

CPU0_APCS_SAW2_STS_1 (cont.)

Bits	Name	Description
26	MIN_INT	IRQ status bit, AVS. controller detected that lowering the VLVL by SAW2_AVS_CTL[VLVL_STEP] would result in a value less than SAW2_AVS_CTL[MIN_VLVL]. If SAW2_AVS_CTL[IRQ_MIN_EN] is set, an interrupt is issued. NOTE that SW can set MIN_VLVL higher than current VLVL creating a condition where VLVL is lower than MIN_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MIN.
25:16	CURR_DLY	VLVL value of the counter used to calculate the time until the next AVS. controller request for a new VLVL.

0x02089014 CPU0_APCS_SAW2_VCTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

Though this register is read/writable, it also causes a command pulse to the PMIC FSM. Writing this register results in a transaction to the PMIC with SAW2_VCTL being sent to the PMIC. SAW2 support both 8901 and 8058 regulator.

CPU0_APCS_SAW2_VCTL

Bits	Name	Description
31:16	RESERVED_BITS31_16	

0x02089018 CPU0_APCS_SAW2_AVS_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_CTL register is used to control the Adaptive Voltage Scaling (AVS) system.

CPU0_APCS_SAW2_AVS_CTL

Bits	Name	Description
31	RESERVED	

CPU0_APCS_SAW2_AVS_CTL (cont.)

Bits	Name	Description
30	VLVL_WIDTH	Defines the VLVL field of PMIC data. SAW2 at minimum supports 8901 and 8058 regulator. See PMIC document for details. 0x0: 5 bits VLVL (8058 regulator) 0x1: 6 bits VLVL (8901 regulator)
29:28	VLVL_STEP	Controls the step size of each request to PMIC Arbiter. SW may use values from 0 to 3. Note that the value 0 will result in no change - that is if the CPU requests UP or DOWN, the CURR_PVLVL will be sent to the PMIC Arbiter. This may be useful for debug. If an increment or decrement operation would cause the current VLVL to transition above or below the MAX_VLVL or MIN_VLVL, the current VLVL will not be changed. An interrupt will be signaled if IRQ_MAX/MIN_EN is 1
27	EN	AVS. Enable. **NOTE** Setting to 0 does not disable any pending interrupts. **NOTE** AVS. FSM and SPM FSM are mutually exclusive. Only one FSM is active at a time. SW does not have to disable AVS. before going to sleep. 0x0: Disable AVS 0x1: Enable AVS
26	SW_DONE_INT_EN	Set to 1 to turn on AVS. interrupt for when a SW initiated voltage change has completed. Set to 0 to mask it (turn it off). ASSERTION: This interrupt is asserted only after a SW write to SAW2_AVS_VLVL. Specifically, after the AVS. FSM traverses through all its states and transitions back to IDLE, the interrupt line is pulsed. The interrupt controller should be set to edge capture to receive this interrupt. CLEARING: None. This interrupt is a pulse, SW does not need to clear it (aside from requirements of the interrupt controller).
25	MAX_INT_EN	Set to 1 to turn on AVS. interrupt for MAX_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be greater than MAX_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit.
24	MIN_INT_EN	Set to 1 to turn on AVS. interrupt for MIN_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be smaller than MIN_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit
23	RESERVED_23	

CPU0_APCS_SAW2_AVS_CTL (cont.)

Bits	Name	Description
22:17	MAX_VLVL	Control maximum value of AVS. controller's VLVL. When current VLVL reaches this value it may not grow any larger. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level higher, an interrupt is issued. This value may be updated at anytime. Setting to a value lower than MIN_VLVL is not supported, and unpredictable results may occur.
16	RESERVED_16	
15:10	MIN_VLVL	Control the minimum value of AVS. controller's VLVL. When the current VLVL reaches this level it may not shrink any smaller. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level lower, an interrupt is issued. This value may be updated at anytime. Setting to a value higher than MAX_VLVL is not supported, and unpredictable results may occur.
9:0	AVS_DELAY	Control the time between AVS. controller's requests to change the VLVL

0x0208901C CPU0_APCS_SAW2_AVS_HYSTERESIS

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_HYSTERESIS register is used to delay the AVS. UP/DN signal to AVS. FSM. This is used to prevent the false PMIC step due to PDN noise.

CPU0_APCS_SAW2_AVS_HYSTERESIS

Bits	Name	Description
31:24	RESERVED31_24	
23:16	DN_COUNT	HYSTERESIS DN COUNT. Delays of PMIC DN step operation.
15:8	RESERVED15_8	
7:0	UP_COUNT	HYSTERESIS UP COUNT. Delays of PMIC UP step operation.

0x02089020 CPU0_APCS_SAW2_SPM_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_CTL register is used to control the subsystem power management system. This are parameters that controls the operation of SPM FSM.

CPU0_APCS_SAW2_SPM_CTL

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	SPM_START_ADR	Start address for the SPM sequence.
3	ISAR	Inhibit Start Address Reset 0x0: End of program reset the SPM_START_ADR to zero. 0x1: Inhibit End of program to reset SPM_START_ADR
2:1	WAKEUP_CONFIG	Wakeup Configuration 0x0: sys_spm_wakeup 0x1: sys_spm_wakeup or !cpu_spm_wait_req 0x2: sys_spm_wakeup or rising edge of sys_spm_dbg_nopwrdwn 0x3: sys_spm_wakeup or !cpu_spm_wait_req or rising edge of sys_spm_dbg_nopwrdwn
0	SPM_EN	SPM En.

0x02089024 CPU0_APCS_SAW2_SPM_PMIC_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC delay values after SPM FSM PMIC transaction. SPM wait for the programmed delay before executing the next SPM command.

CPU0_APCS_SAW2_SPM_PMIC_DLY

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:24	DATA_1_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
23:19	RESERVED_BITS23_19	
18:16	DATA_1_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
15:11	RESERVED_BITS15_11	

CPU0_APCS_SAW2_SPM_PMIC_DLY (cont.)

Bits	Name	Description
10:8	DATA_0_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
7:3	RESERVED_BITS7_3	
2:0	DATA_0_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms

0x02089028 CPU0_APCS_SAW2_SPM_PMIC_DATA_0

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

CPU0_APCS_SAW2_SPM_PMIC_DATA_0

Bits	Name	Description

0x0208902C CPU0_APCS_SAW2_SPM_PMIC_DATA_1

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

CPU0_APCS_SAW2_SPM_PMIC_DATA_1

Bits	Name	Description

0x02089030 CPU0_APCS_SAW2_RST

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_RST register is used to reset the SAW logic. This register clear itself. It does not reset any SAW2 CSR's. It reset AVS. and SPM FSM and control registers. This is use to clear any hang condition.

CPU0_APCS_SAW2_RST

Bits	Name	Description
31:1	RESERVED31_1	
0	RST	Reset AVS. and SPM FSM and control registers.

0x02089034 CPU0_APCS_SAW2_SPM_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the delay values for SPM Delay command. SPM wait for the programmed delay before executing the next SPM command.

CPU0_APCS_SAW2_SPM_DLY

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:20	DLY3	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
19:10	DLY2	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
9:0	DLY1	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms

0x02089080+4*n CPU0_APCS_SAW2_SPM_SLP_SEQ_ENTRY_n

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_SLP_SEQ_ENTRY_n is an array used to sequence through the steps during various power mode. The register width is defined by CLOG_PWR_CTL parameter.

CPU0_APCS_SAW2_SPM_SLP_SEQ_ENTRY_n

Bits	Name	Description

11.15 KPSS CPU0 Timer Registers (0x0208A000 CPU0_APCS_TMR_BASE)

This section contains the Krait Processor Subsystem (KPSS) CPU0 Timer registers.

0x0208A000 CPU0_APCS_TMRSECURE

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Restricted

The APCS_TMRSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Scorpion's APROTNS pin. When APROTNS is set to '0' the state of the APCS_TMRSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_TMRSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_TMRSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_TMRSECURE register correspond to.

CPU0_APCS_TMRSECURE

Bits	Name	Description
31:5	RESERVED	
4	WDT0	Controls security treatment for the Watch Dog Timer registers: APCS_WDT0_FRZ, APCS_WDT0_INT_EN, APCS_WDT0_STS, APCS_WDT0_INT_WIDTH, APCS_WDT0_BARK_TIME, APCS_WDT0_TST_LD_STS, APCS_WDT0_TST_LD. 0x1: NSEC 0x0: SEC
3	WDT1	Controls security treatment for the Watch Dog Timer registers: APCS_WDT1_FRZ, APCS_WDT1_INT_EN, APCS_WDT1_STS, APCS_WDT1_INT_WIDTH, APCS_WDT1_BARK_TIME, APCS_WDT1_TST_LD_STS, APCS_WDT1_TST_LD. 0x1: NSEC 0x0: SEC
2	GPT0	Controls security treatment for the General Purpose Timer registers: APCS_GPT1_MTCH, APCS_GPT1__CNT, APCS_GPT1_EN, APCS_GPT1_CLR and bits 11-8 of APCS_TMR_STS. 0x1: NSEC 0x0: SEC

CPU0_APCS_TMRSECURE (cont.)

Bits	Name	Description
1	GPT1	Controls security treatment for the General Purpose Timer registers: APCS_GPT0_MTCH, APCS_GPT0__CNT, APCS_GPT0_EN, APCS_GPT0_CLR and bits 11-8 of APCS_TMR_STS. 0x1: NSEC 0x0: SEC
0	DGT	Controls security treatment for the Debug Timer registers; APCS_DGT_MTCH, APCS_DGT_CNT, APCS_DGT_EN, APCS_DGT_CLR, APCS_DGT_CLK_CTL, and bits 3-0 of APCS_TMR_STS 0x1: NSEC 0x0: SEC

0x0208A004 CPU0_APCS_GPT0_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: APCS_TMRSECURE [GPT0].

The general purpose timer will signal interrupt when its counter value has reached the value stored in the APCS_GPT0_MTCH register.

CPU0_APCS_GPT0_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_GPT0_CNT at which an interrupt will be generated.

0x0208A008 CPU0_APCS_GPT0_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_CNT register contains the current value of the GPT0 timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_GPT0_MTCH register at the same time due to HW re-use. The procedure for writing the APCS_GPT0_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_GPT0_EN.

- Write APCS_GPT0_CNT.
- Write (to set/restore) APCS_GPT0_MTCH if required.
- Enable the timer by setting the EN bit in APCS_GPT0_EN.

CPU0_APCS_GPT0_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer.

0x0208A00C CPU0_APCS_GPT0_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_EN register is used to enable the GPT0 timer.

CPU0_APCS_GPT0_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	CLR_ON_MTCH_EN	When set (1), the timer will clear when it reaches the match value.
0	EN	When set (1), the timer is enabled and counts with frequency ACC_SLP_CLK.

0x0208A010 CPU0_APCS_GPT0_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_CLR register is a one-shot command register that, when written with any value, resets the timer to a value of 0. This occurs regardless of the state of the APCS_GPT0_EN register.

CPU0_APCS_GPT0_CLR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Data written is not used.

0x0208A014 CPU0_APCS_GPT1_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The GPT timer will signal interrupt when its counter value has reached the value stored in the APCS_GPT1_MTCH register.

CPU0_APCS_GPT1_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_GPT1_CNT at which an interrupt will be generated.

0x0208A018 CPU0_APCS_GPT1_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_CNT register contains the current value of the GPT1 timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_GPT1_MTCH register at the same time. The procedure for writing the APCS_GPT1_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_GPT1_EN.
- Write APCS_GPT1_CNT.
- Write (to set/restore) APCS_GPT1_MTCH if required.
- Enable the timer by setting the EN bit in APCS_GPT1_EN.

CPU0_APCS_GPT1_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer

0x0208A01C CPU0_APCS_GPT1_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_EN register is used to enable the GPT1 timer.

CPU0_APCS_GPT1_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	CLR_ON_MTCH_EN	When set (1), timer will clear when it reaches the match value.
0	EN	When set (1), timer is enabled and counts with frequency sleep clock.

0x0208A020 CPU0_APCS_GPT1_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_CLR register is a one-shot command register that, when written with any value, resets the GPT1 timer to a value of 0. This occurs regardless of the state of the APCS_GPT1_EN register.

CPU0_APCS_GPT1_CLR

Bits	Name	Description
31:0	RESERVED_BITS_31_0	Data written is not used.

0x0208A024 CPU0_APCS_DGT_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The DBG timer will signal interrupt when its counter value has reached the value stored in the APCS_DGT_MTCH register.

CPU0_APCS_DGT_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_DGT_CNT at which an interrupt will be generated.

0x0208A028 CPU0_APCS_DGT_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CNT register contains the current value of the DGT timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_DGT_MTCH register at the same time due to HW re-use. The procedure for writing the APCS_DGT_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_DGT_EN.
- Write APCS_DGT_CNT.
- Write (to set/restore) APCS_DGT_MTCH if required.
- Enable the timer by setting the EN bit in APCS_DGT_EN.

CPU0_APCS_DGT_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer count

0x0208A02C CPU0_APCS_DGT_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_EN register is used to enable the DGT timer.

CPU0_APCS_DGT_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	

CPU0_APCS_DGT_EN (cont.)

Bits	Name	Description
1	CLR_ON_MTCH_EN	When set (1), the timer will clear when it reaches the match value.
0	EN	When set (1), the timer is enabled and counts with frequency TCXO clock.

0x0208A030 CPU0_APCS_DGT_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CLR register is a one-shot command register that, when written with any value, resets the DGT timer to a value of 0. This occurs regardless of the state of the APCS_DGT_EN register.

CPU0_APCS_DGT_CLR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Data written is not used.

0x0208A034 CPU0_APCS_DGT_CLK_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0003

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CLK_CTL controls the clock divider inside the Debug Timer.

NOTE It is possible for the AHB clock to run at as slow as 5 MHz using settings of the Global Clock Controller. The debug timer's counter can also run at 5 MHz (TCXO divided by 4). However, due to the synchronization circuit using the edge detect, the timer should always run at least 4x slower than the AHB clock. Thus, if the timer's use is required by the system, the divider should be set to divide by 4 and the slowest usable AHB frequency is 20MHz. The timer would run at 5MHz in this case.

CPU0_APCS_DGT_CLK_CTL

Bits	Name	Description
31:2	RESERVED_BITS_31_2	

CPU0_APCS_DGT_CLK_CTL (cont.)

Bits	Name	Description
1:0	DIV	0x3: 4 0x2: 3 0x1: 2 0x0: 1

0x0208A038 CPU0_APCS_WDT0_RST

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_RST register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset the watch dog counter. This command register also disables the watchdog freeze

CPU0_APCS_WDT0_RST

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	STB	This bit generates the WDT0_STB during the non-sleep mode. A pulse is generated on WDT0_STB when this bit is written with a ’1

0x0208A03C CPU0_APCS_WDT0_FRZ

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_FRZ register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the APCS_WDT0_RST register.

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

CPU0_APCS_WDT0_FRZ

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved

CPU0_APCS_WDT0_FRZ (cont.)

Bits	Name	Description
0	FRZ	This bit is used to freeze the watchdog timer at time 0. To enable the watchdog timer auto-kicker, write a '1'.

0x0208A040 CPU0_APCS_WDT0_EN

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_EN register controls when the watch dog timer is enabled.

CPU0_APCS_WDT0_EN

Bits	Name	Description
31:2	RESERVED_BITS_31_2	Reserved
1	INT_EN	Any write to this register: 0x1: yes (any unmasked IRQ or FIQ will enable the WDT0 timer.) 0x0: no
0	EN	Any write to this register: 0x1: yes (the watch dog timer is enabled) 0x0: no

0x0208A044 CPU0_APCS_WDT0_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_STS register is the watchdog status register.

CPU0_APCS_WDT0_STS

Bits	Name	Description
31:3	WDT_CNT	Counter value [28:0] of the watch dog counter. **NOTE** The sleep counter value is sampled using the AHB clk. Multiple reads are required to determine the value (assuming AHB clk is much faster than sleep clock).
2	WDT_RST_STS	Show the status of watchdog0 counter reset.

CPU0_APCS_WDT0_STS (cont.)

Bits	Name	Description
1	AUTOKICK	This bit indicates whether the auto-kicker is on. 0x1: On 0x0: Off
0	RST_STS	0x1: wdt (the last system reset was due to WDT0) 0x0: reset (the last system reset was not due to WDT0.)

0x0208A048 CPU0_APCS_WDT0_INT_WIDTH

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_INT_WIDTH register defines the width of the WDT0 biteExpired pulse in the number of sleep_clk pulses. The default value is 0x0C7C, but this reset value is not readable through the AHB interface.

CPU0_APCS_WDT0_INT_WIDTH

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter value on which to de-assert the WDI bite pulse.

0x0208A04C CPU0_APCS_WDT0_BARK_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (’bark’) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, but this reset value is not readable through the AHB interface. Note that this value is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (’bark’) interrupt.

CPU0_APCS_WDT0_BARK_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter value on which to trigger the bark interrupt.

0x0208A050 CPU0_APCS_WDT0_TST_LD_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TST_LD_STS register indicates when the watchdog test load is synchronizing to the SLP_CLK.

CPU0_APCS_WDT0_TST_LD_STS

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SYNC_STS	When set (1) wdog test load is synchronizing to SLP_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x0208A054 CPU0_APCS_WDT0_TST_LD

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TEST_LD register loads the WDT0_TST register value into the watchdog counter.

CPU0_APCS_WDT0_TST_LD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	LD	Set on this bit to load the value into the WDT0_TST register into the WDT0 counter.

0x0208A058 CPU0_APCS_WDT0_TST

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TST register indicates that the watchdog test is synchronizing to the SLP_CLK and contains the watch dog counter test load value.

CPU0_APCS_WDT0_TST

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter test load value [28:0].

0x0208A05C CPU0_APCS_WDT0_BITE_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_31F3

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_BITE_TIME register determines the counter value at which WDT0 asserts the biteExpired signal.

CPU0_APCS_WDT0_BITE_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog bite time is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 bite expiration time [28:0].

0x0208A060 CPU0_APCS_WDT1_RST

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_RST register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset the watch dog counter. This command register also disables the watchdog freeze

CPU0_APCS_WDT1_RST

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	STB	This bit generates the WDT1_STB during the non-sleep mode. A pulse is generated on WDT1_STB when this bit is written with a ’1

0x0208A064 CPU0_APCS_WDT1_FRZ

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_FRZ register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the APCS_WDT1_RST register.

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

CPU0_APCS_WDT1_FRZ

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	FRZ	This bit is used to freeze the watchdog timer at time 0. To enable the watchdog timer auto-kicker, write a ’1’.

0x0208A068 CPU0_APCS_WDT1_EN

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_EN register controls when the watchdog timer is enabled.

CPU0_APCS_WDT1_EN

Bits	Name	Description
31:2	RESERVED_BITS_31_2	Reserved
1	INT_EN	Any write to this register: 0x1: yes (any unmasked IRQ or FIQ will enable the WDT0 timer.) 0x0: no
0	EN	Any write to this register: 0x1: yes (the watch dog timer is enabled) 0x0: no

0x0208A06C CPU0_APCS_WDT1_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_STS register is the watchdog status register.

CPU0_APCS_WDT1_STS

Bits	Name	Description
31:3	WDT_CNT	Counter value [28:0] of the watch dog counter. **NOTE** The counter value is sampled using the ahb clk. Multiple reads are required to determine the value (assuming ahb clk is much faster than sleep clock).
2	WDT_RST_STS	Show the status of watchdog counter reset.
1	AUTOKICK	This bit indicates whether the auto-kicker is on. 0x1: On 0x0: Off
0	RST_STS	0x1: wdt (the last system reset was due to WDT1) 0x0: reset (the last system reset was not due to WDT1.)

0x0208A070 CPU0_APCS_WDT1_INT_WIDTH

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_INT_WIDTH register defines the width of the WDT1_expired pulse in the number of sleep_clk pulses.The default value is 0x0C7C, but this reset value is not readable through the AHB interface.

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CPU0_APCS_WDT1_INT_WIDTH

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter value on which to de-assert the WDI expired pulse.

0x0208A074 CPU0_APCS_WDT1_BARK_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (’bark’) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, but this reset value is not readable through the AHB interface. Note that this value is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (’bark’) interrupt.

CPU0_APCS_WDT1_BARK_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter value on which to trigger the bark interrupt.

0x0208A078 CPU0_APCS_WDT1_TST_LD_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TST_LD_STS register indicates when the watchdog test load is synchronizing to the SLP_CLK.

CPU0_APCS_WDT1_TST_LD_STS

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SYNC_STS	When set (1) wdog test load is synchronizing to SLP_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x0208A07C CPU0_APCS_WDT1_TST_LD

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TEST_LD register loads the WDT1_TST register value into the watchdog counter.

CPU0_APCS_WDT1_TST_LD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	LD	Set on this bit to load the value into the WDT1_TST register into the WDT counter

0x0208A080 CPU0_APCS_WDT1_TST

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TST register indicates that the watchdog test is synchronizing to the SLP_CLK and contains the watch dog counter test load value.

CPU0_APCS_WDT1_TST

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.

CPU0_APCS_WDT1_TST (cont.)

Bits	Name	Description
28:0	DATA	The WDT1 counter test load value [28:0]

0x0208A084 CPU0_APCS_WDT1_BITE_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_31F3

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_BITE_TIME register determines the counter value at which WDT1 asserts the biteExpired signal.

CPU0_APCS_WDT1_BITE_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog bite time is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 bite expiration time [28:0].

0x0208A088 CPU0_APCS_TMR_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [WDT0, WDT1, GPT0, GPT1, DGT].

The APCS_TMR_STS can be used to determine the status of each of the SCSS timers in the timer's resident clock domain. Since the timer clock domain may be much slower than the AHB clock, AHB transactions may be delayed in taking effect. This information can be used to qualify other actions or used simply for debug purposes. For example, software can determine when a write to APCS_DGT_CLR has taken effect by examining the DGT_CLR_PEND bit.

Each timer's bits are receive security treatment as specified by the APCS_TMRSECURE register.

CPU0_APCS_TMR_STS

Bits	Name	Description
31	RESERVED_BIT31	
30	WDT1_AUTOKICK	Auto-kicker is on (1) or off (0)

CPU0_APCS_TMR_STS (cont.)

Bits	Name	Description
29	WDT1_INT_EN	An unmasked interrupt will enable the timer (1) or not (0)
28	WDT1_EN	Timer is enabled (1) or not (0)
27	RESERVED_BIT27	
26	WDT0_AUTOKICK	Auto-kicker is on (1) or off (0)
25	WDT0_INT_EN	An unmasked interrupt will enable the timer (1) or not (0)
24	WDT0_EN	Timer is enabled (1) or not (0)
23:20	RESERVED_BIT20_23	
19	GPT1_WR_PEND	Timer has a write pending (1) or not (0)
18	GPT1_CLR_PEND	Timer has a clear pending (1) or not (0)
17	GPT1_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
16	GPT1_EN	Timer is enabled (1) or not (0)
15:12	RESERVED_BITS15_12	
11	GPT0_WR_PEND	Timer has a write pending (1) or not (0)
10	GPT0_CLR_PEND	Timer has a clear pending (1) or not (0)
9	GPT0_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
8	GPT0_EN	Timer is enabled (1) or not (0)
7:4	RESERVED_BITS7_4	
3	DGT_WR_PEND	Timer has a write pending (1) or not (0)
2	DGT_CLR_PEND	Timer has a clear pending (1) or not (0)
1	DGT_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
0	DGT_EN	Timer is enabled (1) or not (0)

11.16 KPSS CPU1 ACC Registers (0x02098000 CPU1_APCS_ACC_BASE)

This section contains the Krait Processor Subsystem (KPSS) CPU1 ACC registers.

0x02098000 CPU1_APCS_ACCSECURE

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0007

Security Treatment: Restricted

The APCS_ACCSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Krait's APROTNS pin. When APROTNS is set to '0' the state of the APCS_ACCSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_ACCSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_ACCSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_ACCSECURE register correspond to.

CPU1_APCS_ACCSECURE

Bits	Name	Description
31:4	RESERVED	
31:3	RESERVED_BITS31_3	
2	TST	Controls security treatment for test control registers: APCS_ATSTBUS_SEL 0x1: NSEC 0x0: SEC
1	CLK_CTL	Controls security treatment for the clock control registers: APCS_ACC_STS, APCS_CPU_AUX_CLK_SEL. 0x1: NSEC 0x0: SEC
0	SLP_CTL	Controls security treatment for the sleep control registers: APCS_CPU_PWR_CTL, APCS_CPU_TRGTD_DBG_RST. 0x1: NSEC 0x0: SEC

0x02098004 CPU1_APCS_CPU_PWR_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0109

Security Treatment: Controlled by APCS_ACCSECURE [SLP_CTL].

The APCS_CPU_PWR_CTL register is used to control the clamps, reset and array head switches.

CPU1_APCS_CPU_PWR_CTL

Bits	Name	Description
31:21	RESERVED_BITS31_21	
20:16	CLK_EN	Clock enables for CORE clock. This is only to workaround hardware dynamic clock gating problems. [20:18]= SYS_apcNAux_Clk[3:1] [17] = SYS_apcsRef_Clk [16] = SYS_apcNPll_Clk 0x1: Always enabled 0x0: dynamically enabled by hardware
15:10	RESERVED_BITS15_10	
9	RET_SLP_REQ	When set, this bit request the L2SCU to in-flight snoop operation and block new snoops request from entering FIFO. This control is intended to permit external masters such as the RPM to put CPU to retention sleep modes, when power control is being done by an external master instead of the SPM. The output of this register bit is ORed with a retention sleep request control output from the SPM, so that if either the SPM asserts the control, or the RPM sets this bit, the CPU's snoop FIFO is quiesce.
8	PLL_CLAMP	When set, this bit clamp the output of TDC logic in PLL. This signal that must be asserted prior to collapsing CPU voltage, vdd_apc0. This bit is ORed with SAW output before passing to the APC PLL.
7	CORE_PWRD_UP	Report that the CPU is powered up.
6	GATE_CLK	When set, this bit forces the CPU clock to be gated off. This control is intended to permit external masters such as the RPM to gate off the CPU clock during sleep modes, when power control is being done by an external master instead of the SPM. The output of this register bit is ORed with a clock gating control output from the SPM, so that if either the SPM asserts the control, or the RPM sets this bit, the CPU clock will be gated off. When set, this bit gate the CPU clock that must be asserted during sleep state. This bit is ORed with a SAW output before passing to the CPU core.
5	COREPOR_RST	When set, this bit asserts corepor areset to the CPU core.
4	CORE_RST	When set, this bit asserts core areset to the COPU core.

CPU1_APCS_CPU_PWR_CTL (cont.)

Bits	Name	Description
3	L2DT_SLP	When set, this bit opens a head switch to put the L2 duplicate tag array into a low-leakage, non-data-retaining state. This bit is ORed with a SAW output before passing to the CPU core. The controlled memory array contains a duplicate of the tags contained in the L1 data cache, and is used by the L2 to snoop and see if a shared memory access from one processor necessitates invalidating a line in another processor's L1 data cache. Thus, this memory array generally can be offline when the associated CPU is power-collapsed and its L1 data cache is also off-line.
2	RESERVED_BIT2	Previously ETB HS
1	RESERVED_BIT1	Previously L1 HS
0	CLAMP	When set, this bit asserts the clamp signal that must be asserted prior to collapsing CPU voltage, vdd_apc0. This bit is ORed with SAW output before passing to the CPU core.

0x02098008 CPU1_APCS_ACC_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: N/A

Security Treatment: Controlled by APCS_ACCSECURE [CLK_CTL].

The APCS_ACC_STS register is used to monitor the output of the clock gating cells.

CPU1_APCS_ACC_STS

Bits	Name	Description
31:18	RESERVED_BITS31_18	
17	RET_SLP_ACK	This bit reflect the status of APCN_sysRetSlpAck bit. L2 assert the signal when it see the APCN_sysRetSlpReq and CPU snoop FIFO is quiesced. L2 de-assert this signal after APCN_sysRetSlpReq is de-asserted and all snoop invalidation is completed.
16	SLP_CLK	This bit reflect the status of APCN_sleepClkOnReq bit
15	AHB_CLK	This bit reflect the status of APCN_ahbClkOnReq bit
14	REF_CLK	This bit reflect the status of APCN_refClkOnReq bit
13	SPM_SLP_STATE	This bit reflect the status of SPM Sleep State
12	FRC_CLK_OFF	This bit reflect the status of APCN_apccForceClocksOff bit
11	RET_SLP_REQ	This bit reflect the status of APCN_apccRetSlpReq bit
10	TRGTD_DBG_RST	This bit reflect the status of APCN_apcTargetedDbg_Areset_N bit
9	CORE_RST	This bit reflect the status of APCN_apccCore_Areset_N bit
8	COREPOR_RST	This bit reflect the status of APCN_apccCorePor_Areset_N bit

CPU1_APCS_ACC_STS (cont.)

Bits	Name	Description
7	L2DT_HS	This bit reflect the status of the SYS_apcNSwCtlDupTagArrayCollapse bit
6	CLAMP	This bit reflect the status of the SYS_apcNClampApcNvd bit.
5:3	CORE_AUX_CLK	This bits reflect the status of the APCS_sysApcNAuxClkOnReq bits.
2	CORE_PLL_CLK	This bit reflect the status of the APCS_sysApcNPllClkOnReq bit.
1	CORE_NO_PWR_DWN	This bit reflect the status of the APCN_dbgCoreNoPwrDwn bits.
0	CORE_PWRUP_REQ	This bit reflect the status of the APCN_dbgCorePwrUpReq bits.

0x0209800C CPU1_APCS_ATSTBUS_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [TST].

APCS_ATSTBUS_SEL selects different modules' test bus outputs.

CPU1_APCS_ATSTBUS_SEL

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	EN	Set to 1 to cause APCS to drive the test bus outputs. 0x1: enabled 0x0: disabled
1:0	SEL	0x3: CONSTANT 0x2: SAW 0x1: TMR 0x0: CLK

0x02098010 CPU1_APCS_CPU_TRGTD_DBG_RST

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [SLP_CTL].

APCS_CPU_TRGTD_DBG_RST is used to reset the CPU core debug logic. The hardware clear the register after the CPU debug logic is reset. Software need to poll this register to check if the reset is complete.

CPU1_APCS_CPU_TRGTD_DBG_RST

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	RST	When set this bit de-assert SYS_apcNTargetedDbg_Areset_N to the CPU core for 32 REF clock cycle to the CPU core. At the end of the reset hardware clear this bit.

0x02098014 CPU1_APCS_CPU_AUX_CLK_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [CLK_CTL]

The APCS_CPU_AUX_CLK_SEL register controls the gfmux which selects the AUX clock source for the Krait CPU clock. An additional selection set is provided to determine the clock source for the Krait core (4-1 GFMUX) in the Krait Hard Macro. The QSB clock is the raw source clk at reset.

CPU1_APCS_CPU_AUX_CLK_SEL

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	AUX_SRC	Krait CPU AUX clock select: 0x3: SYS_apcNAux_Clk_1 0x2: SYS_apcNAux_Clk_2 0x1: SYS_apcNAux_Clk_3 0x0: SYS_apcsRef_Clk

11.17 KPSS CPU1 SAW2 Registers (0x02099000 CPU1_APCS_SAW2_BASE)

This section contains the Krait Processor Subsystem (KPSS) CPU1 SAW2 registers.

The SAW2 (SPM and AVS. Wrapper2) design is an AHB slave that contains both SPM and AVS. CSRs.

0x02099000 CPU1_APCS_SAW2_SECURE

Type: Read/write
Clock: SYS_REF_CLK
Reset State: {3{CFGNSINIT}}

Security Treatment: Restricted

The SAW2_SECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by ahb_saw_hprotns pin. When ahb_saw_hprotns is set to ’0’ the state of the SAW2_SECURE register is not considered - a secure transaction is always allowed. When ahb_saw_hprotns is set to ’1’, the SAW2_SECURE register security treatment bit of that register must be ’1’ for access to be granted. If the security treatment bit of the register is set to ’0’, the non-secure (ahb_saw_hprotns = ’1’) transactions are denied. When access is denied, a write is ignored, and a read will return ’0’. No error is signaled.

When reading the SAW2_SECURE register, non-secure agents will always read ’0’. Secure agents will see the actual value of the register. The reset value is controlled by CFGNSINIT input pin.

CPU1_APCS_SAW2_SECURE

Bits	Name	Description
31:3	RESERVED	
2	SAW_CTL	Controls security treatment for SAW2 registers: SAW2_ID, SAW2_CFG, SAW2_STS_0, SAW2_STS_1, SAW2_RST 0x1: NSEC 0x0: SEC
1	PWR_CTL	Controls security treatment for SPM registers: SAW2_SPM_CTL, SAW2_SPM_PMIC_DLY, SAW2_SPM_PMIC_DATA_0, SAW2_SPM_PMIC_DATA_1, SAW2_SPM_SLP_SEQ_ENTRY_n, SAW2_SPM_DLY 0x1: NSEC 0x0: SEC
0	VLT_CTL	Controls security treatment for the AVS. registers: SAW2_AVS_CTL, SAW2_VLVL, SAW2_AVS_HYSTERESIS 0x1: NSEC 0x0: SEC

0x02099004 CPU1_APCS_SAW2_ID

Type: Read
Clock: SYS_REF_CLK
Reset State: Undefined

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register reports the revision and parameter information for the SAW2 core.

CPU1_APCS_SAW2_ID

Bits	Name	Description
31	RESERVED_BITS31	
30:25	NUM_SPM_ENTRY	SAW2 parameter: Indicates number of SAW2_SPM_SLP_SEQ_ENTRY register implemented. Value can range from 1 - 32
24:20	NUM_PWR_CTL	SAW2 parameter: Indicates number of power control implemented. Value can range from 2 - 16
19	RESERVED_BITS19	
18	PMIC_ARB_INTF	SAW2 parameter: Indicates PMIC Arbiter Interface function is implemented
17	AVS_PRESENT	SAW2 parameter: Indicates AVS. function is implemented
16	SPM_PRESENT	SAW2 parameter: Indicates SPM function is implemented
15:12	MAJOR	Major variant
11:0	MINOR	Minor variant

0x02099008 CPU1_APCS_SAW2_CFG

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_CFG register is used to configure the common control between AVS. and SPM.system.

CPU1_APCS_SAW2_CFG

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12	FRC_REF_CLK_ON	Chicken bit to force saw_sys_ref_clk_on_req ON.
11:8	ADR_IDX	PMIC Arbiter Address Index. Drive the saw_pmic_addr_idx output port.

CPU1_APCS_SAW2_CFG (cont.)

Bits	Name	Description
7:6	RESERVED_BITS7_6	
5	PMIC_MODE	PMIC Handshake 0x0: 8K_PMIC (only DONE signal) 0x1: 7K_PMIC (both ACK and DONE signals)
4:0	CLK_DIV	Divider ratio for clock. This is used to generate timer tick for the timer. Timer tick is asserted every (CLK_DIV + 1) sys_ref_clk period. ..... For sys_ref_clk = 20 MHz (53ns) The timer tick range 53 ns to 1.6us. 0x0: Timer Tick every sys_ref_clk 0x1F: Timer Tick every 128 sys_ref_clk.

0x0209900C CPU1_APCS_SAW2_STS_0

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

CPU1_APCS_SAW2_STS_0

Bits	Name	Description
15	SHTDWN_REQ	This bit reflects the shutdown request from the SPM(spm_rpm_shutdown_req) to RPM.
14	SHTDWN_ACK	This bit reflects the shutdown acknowledgement from the RPM(rpm_spm_shutdown_ack) to SPM.
13	BRNGUP_REQ	This bit reflects the bringup request from the SPM(spm_rpm_bringup_req) to RPM.
12	BRNGUP_ACK	This bit reflects the bringup acknowledgement from the RPM(rpm_spm_bringup_ack) to SPM.
11:10	PMIC_STATE	State of the PMIC FSM: transitions back to IDLE) transitions back to IDLE) 0x0: IDLE (waiting for PMIC transaction from AVS. or SPM) 0x1: ACK (waiting for ACK from PMIC Arb) 0x2: DONE (waiting for DONE form PMIC Arb before) 0x3: DELAY (waiting for delay count termination before)

CPU1_APCS_SAW2_STS_0 (cont.)

Bits	Name	Description
9:8	RPM_STATE	State of the RPM FSM: 0x0: RUN (waiting for SPM request) 0x1: STDNACK (waiting for shutdown ACK from RPM) 0x2: WAKEUP (waiting for wakeup interrupt) 0x3: BGUPACK (waiting for bringup ACK from RPM)
7	AVS_STATE	State of the AVS. FSM: indication) 0x0: IDLE (waiting to be enabled or for next UP/DOWN) 0x1: REQ (waiting for PMIC FSM to transition to IDLE)
6:0	SPM_CMD_ADDR	Last SPM command executed.

0x02099010 CPU1_APCS_SAW2_STS_1

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

CPU1_APCS_SAW2_STS_1

Bits	Name	Description
31	RESERVED1	
30	SW_WR_PEND	This bit reflects the VLVL state of the request from the SAW2_VCTL write is pending.
29	CPU_UP	This bit reflects the VLVL state of the request from the CPU (avs_saw_up) to raise the VLVL.
28	CPU_DN	This bit reflects the VLVL state of the request from the CPU (avs_saw_down) to lower the VLVL.
27	MAX_INT	IRQ status bit, AVS. controller detected that raising the VLVL by AVS_CTL[VLVL_STEP] would result in a value greater than AVS_CTL[MAX_VLVL]. If AVS_CTL[IRQ_MAX_EN] is set, an interrupt is issued. NOTE that SW can set MAX_VLVL lower than current VLVL creating a condition where VLVL is higher than MAX_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MAX.

CPU1_APCS_SAW2_STS_1 (cont.)

Bits	Name	Description
26	MIN_INT	IRQ status bit, AVS. controller detected that lowering the VLVL by SAW2_AVS_CTL[VLVL_STEP] would result in a value less than SAW2_AVS_CTL[MIN_VLVL]. If SAW2_AVS_CTL[IRQ_MIN_EN] is set, an interrupt is issued. NOTE that SW can set MIN_VLVL higher than current VLVL creating a condition where VLVL is lower than MIN_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MIN.
25:16	CURR_DLY	VLVL value of the counter used to calculate the time until the next AVS. controller request for a new VLVL.

0x02099014 CPU1_APCS_SAW2_VCTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

Though this register is read/writable, it also causes a command pulse to the PMIC FSM. Writing this register results in a transaction to the PMIC with SAW2_VCTL being sent to the PMIC. SAW2 support both 8901 and 8058 regulator.

CPU1_APCS_SAW2_VCTL

Bits	Name	Description
31:16	RESERVED_BITS31_16	

0x02099018 CPU1_APCS_SAW2_AVS_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_CTL register is used to control the Adaptive Voltage Scaling (AVS) system.

CPU1_APCS_SAW2_AVS_CTL

Bits	Name	Description
31	RESERVED	

CPU1_APCS_SAW2_AVS_CTL (cont.)

Bits	Name	Description
30	VLVL_WIDTH	Defines the VLVL field of PMIC data. SAW2 at minimum supports 8901 and 8058 regulator. See PMIC document for details. 0x0: 5 bits VLVL (8058 regulator) 0x1: 6 bits VLVL (8901 regulator)
29:28	VLVL_STEP	Controls the step size of each request to PMIC Arbiter. SW may use values from 0 to 3. Note that the value 0 will result in no change - that is if the CPU requests UP or DOWN, the CURR_PVLVL will be sent to the PMIC Arbiter. This may be useful for debug. If an increment or decrement operation would cause the current VLVL to transition above or below the MAX_VLVL or MIN_VLVL, the current VLVL will not be changed. An interrupt will be signaled if IRQ_MAX/MIN_EN is 1
27	EN	AVS. Enable. **NOTE** Setting to 0 does not disable any pending interrupts. **NOTE** AVS. FSM and SPM FSM are mutually exclusive. Only one FSM is active at a time. SW does not have to disable AVS. before going to sleep. 0x0: Disable AVS 0x1: Enable AVS
26	SW_DONE_INT_EN	Set to 1 to turn on AVS. interrupt for when a SW initiated voltage change has completed. Set to 0 to mask it (turn it off). ASSERTION: This interrupt is asserted only after a SW write to SAW2_AVS_VLVL. Specifically, after the AVS. FSM traverses through all its states and transitions back to IDLE, the interrupt line is pulsed. The interrupt controller should be set to edge capture to receive this interrupt. CLEARING: None. This interrupt is a pulse, SW does not need to clear it (aside from requirements of the interrupt controller).
25	MAX_INT_EN	Set to 1 to turn on AVS. interrupt for MAX_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be greater than MAX_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit.
24	MIN_INT_EN	Set to 1 to turn on AVS. interrupt for MIN_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be smaller than MIN_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit
23	RESERVED_23	

CPU1_APCS_SAW2_AVS_CTL (cont.)

Bits	Name	Description
22:17	MAX_VLVL	Control maximum value of AVS. controller's VLVL. When current VLVL reaches this value it may not grow any larger. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level higher, an interrupt is issued. This value may be updated at anytime. Setting to a value lower than MIN_VLVL is not supported, and unpredictable results may occur.
16	RESERVED_16	
15:10	MIN_VLVL	Control the minimum value of AVS. controller's VLVL. When the current VLVL reaches this level it may not shrink any smaller. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level lower, an interrupt is issued. This value may be updated at anytime. Setting to a value higher than MAX_VLVL is not supported, and unpredictable results may occur.
9:0	AVS_DELAY	Control the time between AVS. controller's requests to change the VLVL

0x0209901C CPU1_APCS_SAW2_AVS_HYSTERESIS

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_HYSTERESIS register is used to delay the AVS. UP/DN signal to AVS. FSM. This is used to prevent the false PMIC step due to PDN noise.

CPU1_APCS_SAW2_AVS_HYSTERESIS

Bits	Name	Description
31:24	RESERVED31_24	
23:16	DN_COUNT	HYSTERESIS DN COUNT. Delays of PMIC DN step operation.
15:8	RESERVED15_8	
7:0	UP_COUNT	HYSTERESIS UP COUNT. Delays of PMIC UP step operation.

0x02099020 CPU1_APCS_SAW2_SPM_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_CTL register is used to control the subsystem power management system. This are parameters that controls the operation of SPM FSM.

CPU1_APCS_SAW2_SPM_CTL

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	SPM_START_ADR	Start address for the SPM sequence.
3	ISAR	Inhibit Start Address Reset 0x0: End of program reset the SPM_START_ADR to zero. 0x1: Inhibit End of program to reset SPM_START_ADR
2:1	WAKEUP_CONFIG	Wakeup Configuration 0x0: sys_spm_wakeup 0x1: sys_spm_wakeup or !cpu_spm_wait_req 0x2: sys_spm_wakeup or rising edge of sys_spm_dbg_nopwrdwn 0x3: sys_spm_wakeup or !cpu_spm_wait_req or rising edge of sys_spm_dbg_nopwrdwn
0	SPM_EN	SPM En.

0x02099024 CPU1_APCS_SAW2_SPM_PMIC_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC delay values after SPM FSM PMIC transaction. SPM wait for the programmed delay before executing the next SPM command.

CPU1_APCS_SAW2_SPM_PMIC_DLY

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:24	DATA_1_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
23:19	RESERVED_BITS23_19	
18:16	DATA_1_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
15:11	RESERVED_BITS15_11	

CPU1_APCS_SAW2_SPM_PMIC_DLY (cont.)

Bits	Name	Description
10:8	DATA_0_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
7:3	RESERVED_BITS7_3	
2:0	DATA_0_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms

0x02099028 CPU1_APCS_SAW2_SPM_PMIC_DATA_0

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

CPU1_APCS_SAW2_SPM_PMIC_DATA_0

Bits	Name	Description

0x0209902C CPU1_APCS_SAW2_SPM_PMIC_DATA_1

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

CPU1_APCS_SAW2_SPM_PMIC_DATA_1

Bits	Name	Description

0x02099030 CPU1_APCS_SAW2_RST

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_RST register is used to reset the SAW logic. This register clear itself. It does not reset any SAW2 CSR's. It reset AVS. and SPM FSM and control registers. This is use to clear any hang condition.

CPU1_APCS_SAW2_RST

Bits	Name	Description
31:1	RESERVED31_1	
0	RST	Reset AVS. and SPM FSM and control registers.

0x02099034 CPU1_APCS_SAW2_SPM_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the delay values for SPM Delay command. SPM wait for the programmed delay before executing the next SPM command.

CPU1_APCS_SAW2_SPM_DLY

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:20	DLY3	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
19:10	DLY2	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
9:0	DLY1	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms

0x02099080+4*n CPU1_APCS_SAW2_SPM_SLP_SEQ_ENTRY_n

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_SLP_SEQ_ENTRY_n is an array used to sequence through the steps during various power mode. The register width is defined by CLOG_PWR_CTL parameter.

CPU1_APCS_SAW2_SPM_SLP_SEQ_ENTRY_n

Bits	Name	Description

11.18 KPSS CPU1 Timer Registers (0x0209A000 CPU1_APCS_TMR_BASE)

This section contains the Krait Processor Subsystem (KPSS) CPU1 Timer registers.

0x0209A000 CPU1_APCS_TMRSECURE

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Restricted

The APCS_TMRSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Scorpion's APROTNS pin. When APROTNS is set to '0' the state of the APCS_TMRSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_TMRSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_TMRSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_TMRSECURE register correspond to.

CPU1_APCS_TMRSECURE

Bits	Name	Description
31:5	RESERVED	
4	WDT0	Controls security treatment for the Watch Dog Timer registers: APCS_WDT0_FRZ, APCS_WDT0_INT_EN, APCS_WDT0_STS, APCS_WDT0_INT_WIDTH, APCS_WDT0_BARK_TIME, APCS_WDT0_TST_LD_STS, APCS_WDT0_TST_LD. 0x1: NSEC 0x0: SEC
3	WDT1	Controls security treatment for the Watch Dog Timer registers: APCS_WDT1_FRZ, APCS_WDT1_INT_EN, APCS_WDT1_STS, APCS_WDT1_INT_WIDTH, APCS_WDT1_BARK_TIME, APCS_WDT1_TST_LD_STS, APCS_WDT1_TST_LD. 0x1: NSEC 0x0: SEC
2	GPT0	Controls security treatment for the General Purpose Timer registers: APCS_GPT1_MTCH, APCS_GPT1__CNT, APCS_GPT1_EN, APCS_GPT1_CLR and bits 11-8 of APCS_TMR_STS. 0x1: NSEC 0x0: SEC

CPU1_APCS_TMRSECURE (cont.)

Bits	Name	Description
1	GPT1	Controls security treatment for the General Purpose Timer registers: APCS_GPT0_MTCH, APCS_GPT0__CNT, APCS_GPT0_EN, APCS_GPT0_CLR and bits 11-8 of APCS_TMR_STS. 0x1: NSEC 0x0: SEC
0	DGT	Controls security treatment for the Debug Timer registers; APCS_DGT_MTCH, APCS_DGT_CNT, APCS_DGT_EN, APCS_DGT_CLR, APCS_DGT_CLK_CTL, and bits 3-0 of APCS_TMR_STS 0x1: NSEC 0x0: SEC

0x0209A004 CPU1_APCS_GPT0_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: APCS_TMRSECURE [GPT0].

The general purpose timer will signal interrupt when its counter value has reached the value stored in the APCS_GPT0_MTCH register.

CPU1_APCS_GPT0_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_GPT0_CNT at which an interrupt will be generated.

0x0209A008 CPU1_APCS_GPT0_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_CNT register contains the current value of the GPT0 timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_GPT0_MTCH register at the same time due to HW re-use. The procedure for writing the APCS_GPT0_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_GPT0_EN.

- Write APCS_GPT0_CNT.
- Write (to set/restore) APCS_GPT0_MTCH if required.
- Enable the timer by setting the EN bit in APCS_GPT0_EN.

CPU1_APCS_GPT0_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer.

0x0209A00C CPU1_APCS_GPT0_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_EN register is used to enable the GPT0 timer.

CPU1_APCS_GPT0_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	CLR_ON_MTCH_EN	When set (1), the timer will clear when it reaches the match value.
0	EN	When set (1), the timer is enabled and counts with frequency ACC_SLP_CLK.

0x0209A010 CPU1_APCS_GPT0_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_CLR register is a one-shot command register that, when written with any value, resets the timer to a value of 0. This occurs regardless of the state of the APCS_GPT0_EN register.

CPU1_APCS_GPT0_CLR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Data written is not used.

0x0209A014 CPU1_APCS_GPT1_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The GPT timer will signal interrupt when its counter value has reached the value stored in the APCS_GPT1_MTCH register.

CPU1_APCS_GPT1_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_GPT1_CNT at which an interrupt will be generated.

0x0209A018 CPU1_APCS_GPT1_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_CNT register contains the current value of the GPT1 timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_GPT1_MTCH register at the same time. The procedure for writing the APCS_GPT1_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_GPT1_EN.
- Write APCS_GPT1_CNT.
- Write (to set/restore) APCS_GPT1_MTCH if required.
- Enable the timer by setting the EN bit in APCS_GPT1_EN.

CPU1_APCS_GPT1_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer

0x0209A01C CPU1_APCS_GPT1_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_EN register is used to enable the GPT1 timer.

CPU1_APCS_GPT1_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	CLR_ON_MTCH_EN	When set (1), timer will clear when it reaches the match value.
0	EN	When set (1), timer is enabled and counts with frequency sleep clock.

0x0209A020 CPU1_APCS_GPT1_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_CLR register is a one-shot command register that, when written with any value, resets the GPT1 timer to a value of 0. This occurs regardless of the state of the APCS_GPT1_EN register.

CPU1_APCS_GPT1_CLR

Bits	Name	Description
31:0	RESERVED_BITS_31_0	Data written is not used.

0x0209A024 CPU1_APCS_DGT_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The DBG timer will signal interrupt when its counter value has reached the value stored in the APCS_DGT_MTCH register.

CPU1_APCS_DGT_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_DGT_CNT at which an interrupt will be generated.

0x0209A028 CPU1_APCS_DGT_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CNT register contains the current value of the DGT timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_DGT_MTCH register at the same time due to HW re-use. The procedure for writing the APCS_DGT_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_DGT_EN.
- Write APCS_DGT_CNT.
- Write (to set/restore) APCS_DGT_MTCH if required.
- Enable the timer by setting the EN bit in APCS_DGT_EN.

CPU1_APCS_DGT_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer count

0x0209A02C CPU1_APCS_DGT_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_EN register is used to enable the DGT timer.

CPU1_APCS_DGT_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	

CPU1_APCS_DGT_EN (cont.)

Bits	Name	Description
1	CLR_ON_MTCH_EN	When set (1), the timer will clear when it reaches the match value.
0	EN	When set (1), the timer is enabled and counts with frequency TCXO clock.

0x0209A030 CPU1_APCS_DGT_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CLR register is a one-shot command register that, when written with any value, resets the DGT timer to a value of 0. This occurs regardless of the state of the APCS_DGT_EN register.

CPU1_APCS_DGT_CLR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Data written is not used.

0x0209A034 CPU1_APCS_DGT_CLK_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0003

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CLK_CTL controls the clock divider inside the Debug Timer.

NOTE It is possible for the AHB clock to run at as slow as 5 MHz using settings of the Global Clock Controller. The debug timer's counter can also run at 5 MHz (TCXO divided by 4). However, due to the synchronization circuit using the edge detect, the timer should always run at least 4x slower than the AHB clock. Thus, if the timer's use is required by the system, the divider should be set to divide by 4 and the slowest usable AHB frequency is 20MHz. The timer would run at 5MHz in this case.

CPU1_APCS_DGT_CLK_CTL

Bits	Name	Description
31:2	RESERVED_BITS_31_2	

CPU1_APCS_DGT_CLK_CTL (cont.)

Bits	Name	Description
1:0	DIV	0x3: 4 0x2: 3 0x1: 2 0x0: 1

0x0209A038 CPU1_APCS_WDT0_RST

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_RST register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset the watch dog counter. This command register also disables the watchdog freeze

CPU1_APCS_WDT0_RST

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	STB	This bit generates the WDT0_STB during the non-sleep mode. A pulse is generated on WDT0_STB when this bit is written with a ’1

0x0209A03C CPU1_APCS_WDT0_FRZ

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_FRZ register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the APCS_WDT0_RST register.

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

CPU1_APCS_WDT0_FRZ

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved

CPU1_APCS_WDT0_FRZ (cont.)

Bits	Name	Description
0	FRZ	This bit is used to freeze the watchdog timer at time 0. To enable the watchdog timer auto-kicker, write a '1'.

0x0209A040 CPU1_APCS_WDT0_EN

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_EN register controls when the watch dog timer is enabled.

CPU1_APCS_WDT0_EN

Bits	Name	Description
31:2	RESERVED_BITS_31_2	Reserved
1	INT_EN	Any write to this register: 0x1: yes (any unmasked IRQ or FIQ will enable the WDT0 timer.) 0x0: no
0	EN	Any write to this register: 0x1: yes (the watch dog timer is enabled) 0x0: no

0x0209A044 CPU1_APCS_WDT0_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_STS register is the watchdog status register.

CPU1_APCS_WDT0_STS

Bits	Name	Description
31:3	WDT_CNT	Counter value [28:0] of the watch dog counter. **NOTE** The sleep counter value is sampled using the AHB clk. Multiple reads are required to determine the value (assuming AHB clk is much faster than sleep clock).
2	WDT_RST_STS	Show the status of watchdog0 counter reset.

CPU1_APCS_WDT0_STS (cont.)

Bits	Name	Description
1	AUTOKICK	This bit indicates whether the auto-kicker is on. 0x1: On 0x0: Off
0	RST_STS	0x1: wdt (the last system reset was due to WDT0) 0x0: reset (the last system reset was not due to WDT0.)

0x0209A048 CPU1_APCS_WDT0_INT_WIDTH

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_INT_WIDTH register defines the width of the WDT0 biteExpired pulse in the number of sleep_clk pulses. The default value is 0x0C7C, but this reset value is not readable through the AHB interface.

CPU1_APCS_WDT0_INT_WIDTH

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter value on which to de-assert the WDI bite pulse.

0x0209A04C CPU1_APCS_WDT0_BARK_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (’bark’) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, but this reset value is not readable through the AHB interface. Note that this value is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (’bark’) interrupt.

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CPU1_APCS_WDT0_BARK_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter value on which to trigger the bark interrupt.

0x0209A050 CPU1_APCS_WDT0_TST_LD_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TST_LD_STS register indicates when the watchdog test load is synchronizing to the SLP_CLK.

CPU1_APCS_WDT0_TST_LD_STS

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SYNC_STS	When set (1) wdog test load is synchronizing to SLP_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x0209A054 CPU1_APCS_WDT0_TST_LD

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TEST_LD register loads the WDT0_TST register value into the watchdog counter.

CPU1_APCS_WDT0_TST_LD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	LD	Set on this bit to load the value into the WDT0_TST register into the WDT0 counter.

0x0209A058 CPU1_APCS_WDT0_TST

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TST register indicates that the watchdog test is synchronizing to the SLP_CLK and contains the watch dog counter test load value.

CPU1_APCS_WDT0_TST

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter test load value [28:0].

0x0209A05C CPU1_APCS_WDT0_BITE_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_31F3

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_BITE_TIME register determines the counter value at which WDT0 asserts the biteExpired signal.

CPU1_APCS_WDT0_BITE_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog bite time is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 bite expiration time [28:0].

0x0209A060 CPU1_APCS_WDT1_RST

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_RST register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset the watch dog counter. This command register also disables the watchdog freeze

CPU1_APCS_WDT1_RST

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	STB	This bit generates the WDT1_STB during the non-sleep mode. A pulse is generated on WDT1_STB when this bit is written with a ’1

0x0209A064 CPU1_APCS_WDT1_FRZ

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_FRZ register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the APCS_WDT1_RST register.

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

CPU1_APCS_WDT1_FRZ

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	FRZ	This bit is used to freeze the watchdog timer at time 0. To enable the watchdog timer auto-kicker, write a ’1’.

0x0209A068 CPU1_APCS_WDT1_EN

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_EN register controls when the watchdog timer is enabled.

CPU1_APCS_WDT1_EN

Bits	Name	Description
31:2	RESERVED_BITS_31_2	Reserved
1	INT_EN	Any write to this register: 0x1: yes (any unmasked IRQ or FIQ will enable the WDT0 timer.) 0x0: no
0	EN	Any write to this register: 0x1: yes (the watch dog timer is enabled) 0x0: no

0x0209A06C CPU1_APCS_WDT1_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_STS register is the watchdog status register.

CPU1_APCS_WDT1_STS

Bits	Name	Description
31:3	WDT_CNT	Counter value [28:0] of the watch dog counter. **NOTE** The counter value is sampled using the ahb clk. Multiple reads are required to determine the value (assuming ahb clk is much faster than sleep clock).
2	WDT_RST_STS	Show the status of watchdog counter reset.
1	AUTOKICK	This bit indicates whether the auto-kicker is on. 0x1: On 0x0: Off
0	RST_STS	0x1: wdt (the last system reset was due to WDT1) 0x0: reset (the last system reset was not due to WDT1.)

0x0209A070 CPU1_APCS_WDT1_INT_WIDTH

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_INT_WIDTH register defines the width of the WDT1_expired pulse in the number of sleep_clk pulses.The default value is 0x0C7C, but this reset value is not readable through the AHB interface.

CPU1_APCS_WDT1_INT_WIDTH

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter value on which to de-assert the WDI expired pulse.

0x0209A074 CPU1_APCS_WDT1_BARK_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (’bark’) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, but this reset value is not readable through the AHB interface. Note that this value is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (’bark’) interrupt.

CPU1_APCS_WDT1_BARK_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter value on which to trigger the bark interrupt.

0x0209A078 CPU1_APCS_WDT1_TST_LD_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TST_LD_STS register indicates when the watchdog test load is synchronizing to the SLP_CLK.

CPU1_APCS_WDT1_TST_LD_STS

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SYNC_STS	When set (1) wdog test load is synchronizing to SLP_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x0209A07C CPU1_APCS_WDT1_TST_LD

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TEST_LD register loads the WDT1_TST register value into the watchdog counter.

CPU1_APCS_WDT1_TST_LD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	LD	Set on this bit to load the value into the WDT1_TST register into the WDT counter

0x0209A080 CPU1_APCS_WDT1_TST

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TST register indicates that the watchdog test is synchronizing to the SLP_CLK and contains the watch dog counter test load value.

CPU1_APCS_WDT1_TST

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter test load value [28:0]

0x0209A084 CPU1_APCS_WDT1_BITE_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_31F3

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_BITE_TIME register determines the counter value at which WDT1 asserts the biteExpired signal.

CPU1_APCS_WDT1_BITE_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog bite time is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 bite expiration time [28:0].

0x0209A088 CPU1_APCS_TMR_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [WDT0, WDT1, GPT0, GPT1, DGT].

The APCS_TMR_STS can be used to determine the status of each of the SCSS timers in the timer's resident clock domain. Since the timer clock domain may be much slower than the AHB clock, AHB transactions may be delayed in taking effect. This information can be used to qualify other actions or used simply for debug purposes. For example, software can determine when a write to APCS_DGT_CLR has taken effect by examining the DGT_CLR_PEND bit.

Each timer's bits are receive security treatment as specified by the APCS_TMRSECURE register.

CPU1_APCS_TMR_STS

Bits	Name	Description
31	RESERVED_BIT31	
30	WDT1_AUTOKICK	Auto-kicker is on (1) or off (0)
29	WDT1_INT_EN	An unmasked interrupt will enable the timer (1) or not (0)
28	WDT1_EN	Timer is enabled (1) or not (0)
27	RESERVED_BIT27	
26	WDT0_AUTOKICK	Auto-kicker is on (1) or off (0)

CPU1_APCS_TMR_STS (cont.)

Bits	Name	Description
25	WDT0_INT_EN	An unmasked interrupt will enable the timer (1) or not (0)
24	WDT0_EN	Timer is enabled (1) or not (0)
23:20	RESERVED_BIT20_23	
19	GPT1_WR_PEND	Timer has a write pending (1) or not (0)
18	GPT1_CLR_PEND	Timer has a clear pending (1) or not (0)
17	GPT1_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
16	GPT1_EN	Timer is enabled (1) or not (0)
15:12	RESERVED_BITS15_12	
11	GPT0_WR_PEND	Timer has a write pending (1) or not (0)
10	GPT0_CLR_PEND	Timer has a clear pending (1) or not (0)
9	GPT0_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
8	GPT0_EN	Timer is enabled (1) or not (0)
7:4	RESERVED_BITS7_4	
3	DGT_WR_PEND	Timer has a write pending (1) or not (0)
2	DGT_CLR_PEND	Timer has a clear pending (1) or not (0)
1	DGT_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
0	DGT_EN	Timer is enabled (1) or not (0)

11.19 KPSS CPU2 ACC Registers (0x020A8000 CPU2_APCS_ACC_BASE)

This section contains the Krait Processor Subsystem (KPSS) CPU2 ACC registers.

0x020A8000 CPU2_APCS_ACCSECURE

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0007

Security Treatment: Restricted

The APCS_ACCSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Krait's APROTNS pin. When APROTNS is set to '0' the state of the APCS_ACCSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_ACCSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_ACCSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_ACCSECURE register correspond to.

CPU2_APCS_ACCSECURE

Bits	Name	Description
31:4	RESERVED	
31:3	RESERVED_BITS31_3	
2	TST	Controls security treatment for test control registers: APCS_ATSTBUS_SEL 0x1: NSEC 0x0: SEC
1	CLK_CTL	Controls security treatment for the clock control registers: APCS_ACC_STS, APCS_CPU_AUX_CLK_SEL. 0x1: NSEC 0x0: SEC
0	SLP_CTL	Controls security treatment for the sleep control registers: APCS_CPU_PWR_CTL, APCS_CPU_TRGTD_DBG_RST. 0x1: NSEC 0x0: SEC

0x020A8004 CPU2_APCS_CPU_PWR_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0109

Security Treatment: Controlled by APCS_ACCSECURE [SLP_CTL].

The APCS_CPU_PWR_CTL register is used to control the clamps, reset and array head switches.

CPU2_APCS_CPU_PWR_CTL

Bits	Name	Description
31:21	RESERVED_BITS31_21	
20:16	CLK_EN	Clock enables for CORE clock. This is only to workaround hardware dynamic clock gating problems. [20:18]= SYS_apcNAux_Clk[3:1] [17] = SYS_apcsRef_Clk [16] = SYS_apcNPll_Clk 0x1: Always enabled 0x0: dynamically enabled by hardware
15:10	RESERVED_BITS15_10	
9	RET_SLP_REQ	When set, this bit request the L2SCU to in-flight snoop operation and block new snoops request from entering FIFO. This control is intended to permit external masters such as the RPM to put CPU to retention sleep modes, when power control is being done by an external master instead of the SPM. The output of this register bit is ORed with a retention sleep request control output from the SPM, so that if either the SPM asserts the control, or the RPM sets this bit, the CPU's snoop FIFO is quiesced.
8	PLL_CLAMP	When set, this bit clamp the output of TDC logic in PLL. This signal that must be asserted prior to collapsing CPU voltage, vdd_apc0. This bit is ORed with SAW output before passing to the APC PLL.
7	CORE_PWRD_UP	Report that the CPU is powered up.
6	GATE_CLK	When set, this bit forces the CPU clock to be gated off. This control is intended to permit external masters such as the RPM to gate off the CPU clock during sleep modes, when power control is being done by an external master instead of the SPM. The output of this register bit is ORed with a clock gating control output from the SPM, so that if either the SPM asserts the control, or the RPM sets this bit, the CPU clock will be gated off. When set, this bit gate the CPU clock that must be asserted during sleep state. This bit is ORed with a SAW output before passing to the CPU core.
5	COREPOR_RST	When set, this bit asserts corepor areset to the CPU core.
4	CORE_RST	When set, this bit asserts core areset to the COPU core.

CPU2_APCS_CPU_PWR_CTL (cont.)

Bits	Name	Description
3	L2DT_SLP	When set, this bit opens a head switch to put the L2 duplicate tag array into a low-leakage, non-data-retaining state. This bit is ORed with a SAW output before passing to the CPU core. The controlled memory array contains a duplicate of the tags contained in the L1 data cache, and is used by the L2 to snoop and see if a shared memory access from one processor necessitates invalidating a line in another processor's L1 data cache. Thus, this memory array generally can be offline when the associated CPU is power-collapsed and its L1 data cache is also off-line.
2	RESERVED_BIT2	Previously ETB HS
1	RESERVED_BIT1	Previously L1 HS
0	CLAMP	When set, this bit asserts the clamp signal that must be asserted prior to collapsing CPU voltage, vdd_apc0. This bit is ORed with SAW output before passing to the CPU core.

0x020A8008 CPU2_APCS_ACC_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: N/A

Security Treatment: Controlled by APCS_ACCSECURE [CLK_CTL].

The APCS_ACC_STS register is used to monitor the output of the clock gating cells.

CPU2_APCS_ACC_STS

Bits	Name	Description
31:18	RESERVED_BITS31_18	
17	RET_SLP_ACK	This bit reflect the status of APCN_sysRetSlpAck bit. L2 assert the signal when it see the APCN_sysRetSlpReq and CPU snoop FIFO is quiesced. L2 de-assert this signal after APCN_sysRetSlpReq is de-asserted and all snoop invalidation is completed.
16	SLP_CLK	This bit reflect the status of APCN_sleepClkOnReq bit
15	AHB_CLK	This bit reflect the status of APCN_ahbClkOnReq bit
14	REF_CLK	This bit reflect the status of APCN_refClkOnReq bit
13	SPM_SLP_STATE	This bit reflect the status of SPM Sleep State
12	FRC_CLK_OFF	This bit reflect the status of APCN_apccForceClocksOff bit
11	RET_SLP_REQ	This bit reflect the status of APCN_apccRetSlpReq bit
10	TRGTD_DBG_RST	This bit reflect the status of APCN_apcTargetedDbg_Areset_N bit
9	CORE_RST	This bit reflect the status of APCN_apccCore_Areset_N bit
8	COREPOR_RST	This bit reflect the status of APCN_apccCorePor_Areset_N bit

CPU2_APCS_ACC_STS (cont.)

Bits	Name	Description
7	L2DT_HS	This bit reflect the status of the SYS_apcNSwCtlDupTagArrayCollapse bit
6	CLAMP	This bit reflect the status of the SYS_apcNClampApcNvd bit.
5:3	CORE_AUX_CLK	This bits reflect the status of the APCS_sysApcNAuxClkOnReq bits.
2	CORE_PLL_CLK	This bit reflect the status of the APCS_sysApcNPllClkOnReq bit.
1	CORE_NO_PWR_DWN	This bit reflect the status of the APCN_dbgCoreNoPwrDwn bits.
0	CORE_PWRUP_REQ	This bit reflect the status of the APCN_dbgCorePwrUpReq bits.

0x020A800C CPU2_APCS_ATSTBUS_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [TST].

APCS_ATSTBUS_SEL selects different modules' test bus outputs.

CPU2_APCS_ATSTBUS_SEL

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	EN	Set to 1 to cause APCS to drive the test bus outputs. 0x1: enabled 0x0: disabled
1:0	SEL	0x3: CONSTANT 0x2: SAW 0x1: TMR 0x0: CLK

0x020A8010 CPU2_APCS_CPU_TRGTD_DBG_RST

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [SLP_CTL].

APCS_CPU_TRGTD_DBG_RST is used to reset the CPU core debug logic. The hardware clear the register after the CPU debug logic is reset. Software need to poll this register to check if the reset is complete.

CPU2_APCS_CPU_TRGTD_DBG_RST

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	RST	When set this bit de-assert SYS_apcNTargetedDbg_Areset_N to the CPU core for 32 REF clock cycle to the CPU core. At the end of the reset hardware clear this bit.

0x020A8014 CPU2_APCS_CPU_AUX_CLK_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [CLK_CTL]

The APCS_CPU_AUX_CLK_SEL register controls the gfmux which selects the AUX clock source for the Krait CPU clock. An additional selection set is provided to determine the clock source for the Krait core (4-1 GFMUX) in the Krait Hard Macro. The QSB clock is the raw source clk at reset.

CPU2_APCS_CPU_AUX_CLK_SEL

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	AUX_SRC	Krait CPU AUX clock select: 0x3: SYS_apcNAux_Clk_1 0x2: SYS_apcNAux_Clk_2 0x1: SYS_apcNAux_Clk_3 0x0: SYS_apcsRef_Clk

11.20 KPSS CPU2 SAW2 Registers (0x020A9000 CPU2_APCS_SAW2_BASE)

This section contains the Krait Processor Subsystem (KPSS) CPU2 SAW2 registers.

The SAW2 (SPM and AVS. Wrapper2) design is an AHB slave that contains both SPM and AVS. CSRs.

0x020A9000 CPU2_APCS_SAW2_SECURE

Type: Read/write
Clock: SYS_REF_CLK
Reset State: {3{CFGNSINIT}}

Security Treatment: Restricted

The SAW2_SECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by ahb_saw_hprotns pin. When ahb_saw_hprotns is set to ’0’ the state of the SAW2_SECURE register is not considered - a secure transaction is always allowed. When ahb_saw_hprotns is set to ’1’, the SAW2_SECURE register security treatment bit of that register must be ’1’ for access to be granted. If the security treatment bit of the register is set to ’0’, the non-secure (ahb_saw_hprotns = ’1’) transactions are denied. When access is denied, a write is ignored, and a read will return ’0’. No error is signaled.

When reading the SAW2_SECURE register, non-secure agents will always read ’0’. Secure agents will see the actual value of the register. The reset value is controlled by CFGNSINIT input pin.

CPU2_APCS_SAW2_SECURE

Bits	Name	Description
31:3	RESERVED	
2	SAW_CTL	Controls security treatment for SAW2 registers: SAW2_ID, SAW2_CFG, SAW2_STS_0, SAW2_STS_1, SAW2_RST 0x1: NSEC 0x0: SEC
1	PWR_CTL	Controls security treatment for SPM registers: SAW2_SPM_CTL, SAW2_SPM_PMIC_DLY, SAW2_SPM_PMIC_DATA_0, SAW2_SPM_PMIC_DATA_1, SAW2_SPM_SLP_SEQ_ENTRY_n, SAW2_SPM_DLY 0x1: NSEC 0x0: SEC
0	VLT_CTL	Controls security treatment for the AVS. registers: SAW2_AVS_CTL, SAW2_VLVL, SAW2_AVS_HYSTERESIS 0x1: NSEC 0x0: SEC

0x020A9004 CPU2_APCS_SAW2_ID

Type: Read
Clock: SYS_REF_CLK
Reset State: Undefined

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register reports the revision and parameter information for the SAW2 core.

CPU2_APCS_SAW2_ID

Bits	Name	Description
31	RESERVED_BITS31	
30:25	NUM_SPM_ENTRY	SAW2 parameter: Indicates number of SAW2_SPM_SLP_SEQ_ENTRY register implemented. Value can range from 1 - 32
24:20	NUM_PWR_CTL	SAW2 parameter: Indicates number of power control implemented. Value can range from 2 - 16
19	RESERVED_BITS19	
18	PMIC_ARB_INTF	SAW2 parameter: Indicates PMIC Arbiter Interface function is implemented
17	AVS_PRESENT	SAW2 parameter: Indicates AVS. function is implemented
16	SPM_PRESENT	SAW2 parameter: Indicates SPM function is implemented
15:12	MAJOR	Major variant
11:0	MINOR	Minor variant

0x020A9008 CPU2_APCS_SAW2_CFG

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_CFG register is used to configure the common control between AVS. and SPM.system.

CPU2_APCS_SAW2_CFG

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12	FRC_REF_CLK_ON	Chicken bit to force saw_sys_ref_clk_on_req ON.
11:8	ADR_IDX	PMIC Arbiter Address Index. Drive the saw_pmic_addr_idx output port.

CPU2_APCS_SAW2_CFG (cont.)

Bits	Name	Description
7:6	RESERVED_BITS7_6	
5	PMIC_MODE	PMIC Handshake 0x0: 8K_PMIC (only DONE signal) 0x1: 7K_PMIC (both ACK and DONE signals)
4:0	CLK_DIV	Divider ratio for clock. This is used to generate timer tick for the timer. Timer tick is asserted every (CLK_DIV + 1) sys_ref_clk period. ..... For sys_ref_clk = 20 MHz (53ns) The timer tick range 53 ns to 1.6us. 0x0: Timer Tick every sys_ref_clk 0x1F: Timer Tick every 128 sys_ref_clk.

0x020A900C CPU2_APCS_SAW2_STS_0

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

CPU2_APCS_SAW2_STS_0

Bits	Name	Description
15	SHTDWN_REQ	This bit reflects the shutdown request from the SPM(spm_rpm_shutdown_req) to RPM.
14	SHTDWN_ACK	This bit reflects the shutdown acknowledgement from the RPM(rpm_spm_shutdown_ack) to SPM.
13	BRNGUP_REQ	This bit reflects the bringup request from the SPM(spm_rpm_bringup_req) to RPM.
12	BRNGUP_ACK	This bit reflects the bringup acknowledgement from the RPM(rpm_spm_bringup_ack) to SPM.
11:10	PMIC_STATE	State of the PMIC FSM: transitions back to IDLE) transitions back to IDLE) 0x0: IDLE (waiting for PMIC transaction from AVS. or SPM) 0x1: ACK (waiting for ACK from PMIC Arb) 0x2: DONE (waiting for DONE form PMIC Arb before) 0x3: DELAY (waiting for delay count termination before)

CPU2_APCS_SAW2_STS_0 (cont.)

Bits	Name	Description
9:8	RPM_STATE	State of the RPM FSM: 0x0: RUN (waiting for SPM request) 0x1: STDNACK (waiting for shutdown ACK from RPM) 0x2: WAKEUP (waiting for wakeup interrupt) 0x3: BGUPACK (waiting for bringup ACK from RPM)
7	AVS_STATE	State of the AVS. FSM: indication) 0x0: IDLE (waiting to be enabled or for next UP/DOWN) 0x1: REQ (waiting for PMIC FSM to transition to IDLE)
6:0	SPM_CMD_ADDR	Last SPM command executed.

0x020A9010 CPU2_APCS_SAW2_STS_1

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

CPU2_APCS_SAW2_STS_1

Bits	Name	Description
31	RESERVED1	
30	SW_WR_PEND	This bit reflects the VLVL state of the request from the SAW2_VCTL write is pending.
29	CPU_UP	This bit reflects the VLVL state of the request from the CPU (avs_saw_up) to raise the VLVL.
28	CPU_DN	This bit reflects the VLVL state of the request from the CPU (avs_saw_down) to lower the VLVL.
27	MAX_INT	IRQ status bit, AVS. controller detected that raising the VLVL by AVS_CTL[VLVL_STEP] would result in a value greater than AVS_CTL[MAX_VLVL]. If AVS_CTL[IRQ_MAX_EN] is set, an interrupt is issued. NOTE that SW can set MAX_VLVL lower than current VLVL creating a condition where VLVL is higher than MAX_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MAX.

CPU2_APCS_SAW2_STS_1 (cont.)

Bits	Name	Description
26	MIN_INT	IRQ status bit, AVS. controller detected that lowering the VLVL by SAW2_AVS_CTL[VLVL_STEP] would result in a value less than SAW2_AVS_CTL[MIN_VLVL]. If SAW2_AVS_CTL[IRQ_MIN_EN] is set, an interrupt is issued. NOTE that SW can set MIN_VLVL higher than current VLVL creating a condition where VLVL is lower than MIN_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MIN.
25:16	CURR_DLY	VLVL value of the counter used to calculate the time until the next AVS. controller request for a new VLVL.

0x020A9014 CPU2_APCS_SAW2_VCTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

Though this register is read/writable, it also causes a command pulse to the PMIC FSM. Writing this register results in a transaction to the PMIC with SAW2_VCTL being sent to the PMIC. SAW2 support both 8901 and 8058 regulator.

CPU2_APCS_SAW2_VCTL

Bits	Name	Description
31:16	RESERVED_BITS31_16	

0x020A9018 CPU2_APCS_SAW2_AVS_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_CTL register is used to control the Adaptive Voltage Scaling (AVS) system.

CPU2_APCS_SAW2_AVS_CTL

Bits	Name	Description
31	RESERVED	

CPU2_APCS_SAW2_AVS_CTL (cont.)

Bits	Name	Description
30	VLVL_WIDTH	Defines the VLVL field of PMIC data. SAW2 at minimum supports 8901 and 8058 regulator. See PMIC document for details. 0x0: 5 bits VLVL (8058 regulator) 0x1: 6 bits VLVL (8901 regulator)
29:28	VLVL_STEP	Controls the step size of each request to PMIC Arbiter. SW may use values from 0 to 3. Note that the value 0 will result in no change - that is if the CPU requests UP or DOWN, the CURR_PVLVL will be sent to the PMIC Arbiter. This may be useful for debug. If an increment or decrement operation would cause the current VLVL to transition above or below the MAX_VLVL or MIN_VLVL, the current VLVL will not be changed. An interrupt will be signaled if IRQ_MAX/MIN_EN is 1
27	EN	AVS. Enable. **NOTE** Setting to 0 does not disable any pending interrupts. **NOTE** AVS. FSM and SPM FSM are mutually exclusive. Only one FSM is active at a time. SW does not have to disable AVS. before going to sleep. 0x0: Disable AVS 0x1: Enable AVS
26	SW_DONE_INT_EN	Set to 1 to turn on AVS. interrupt for when a SW initiated voltage change has completed. Set to 0 to mask it (turn it off). ASSERTION: This interrupt is asserted only after a SW write to SAW2_AVS_VLVL. Specifically, after the AVS. FSM traverses through all its states and transitions back to IDLE, the interrupt line is pulsed. The interrupt controller should be set to edge capture to receive this interrupt. CLEARING: None. This interrupt is a pulse, SW does not need to clear it (aside from requirements of the interrupt controller).
25	MAX_INT_EN	Set to 1 to turn on AVS. interrupt for MAX_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be greater than MAX_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit.
24	MIN_INT_EN	Set to 1 to turn on AVS. interrupt for MIN_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be smaller than MIN_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit
23	RESERVED_23	

CPU2_APCS_SAW2_AVS_CTL (cont.)

Bits	Name	Description
22:17	MAX_VLVL	Control maximum value of AVS. controller's VLVL. When current VLVL reaches this value it may not grow any larger. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level higher, an interrupt is issued. This value may be updated at anytime. Setting to a value lower than MIN_VLVL is not supported, and unpredictable results may occur.
16	RESERVED_16	
15:10	MIN_VLVL	Control the minimum value of AVS. controller's VLVL. When the current VLVL reaches this level it may not shrink any smaller. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level lower, an interrupt is issued. This value may be updated at anytime. Setting to a value higher than MAX_VLVL is not supported, and unpredictable results may occur.
9:0	AVS_DELAY	Control the time between AVS. controller's requests to change the VLVL

0x020A901C CPU2_APCS_SAW2_AVS_HYSTERESIS

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_HYSTERESIS register is used to delay the AVS. UP/DN signal to AVS. FSM. This is used to prevent the false PMIC step due to PDN noise.

CPU2_APCS_SAW2_AVS_HYSTERESIS

Bits	Name	Description
31:24	RESERVED31_24	
23:16	DN_COUNT	HYSTERESIS DN COUNT. Delays of PMIC DN step operation.
15:8	RESERVED15_8	
7:0	UP_COUNT	HYSTERESIS UP COUNT. Delays of PMIC UP step operation.

0x020A9020 CPU2_APCS_SAW2_SPM_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_CTL register is used to control the subsystem power management system. This are parameters that controls the operation of SPM FSM.

CPU2_APCS_SAW2_SPM_CTL

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	SPM_START_ADR	Start address for the SPM sequence.
3	ISAR	Inhibit Start Address Reset 0x0: End of program reset the SPM_START_ADR to zero. 0x1: Inhibit End of program to reset SPM_START_ADR
2:1	WAKEUP_CONFIG	Wakeup Configuration 0x0: sys_spm_wakeup 0x1: sys_spm_wakeup or !cpu_spm_wait_req 0x2: sys_spm_wakeup or rising edge of sys_spm_dbg_nopwrdwn 0x3: sys_spm_wakeup or !cpu_spm_wait_req or rising edge of sys_spm_dbg_nopwrdwn
0	SPM_EN	SPM En.

0x020A9024 CPU2_APCS_SAW2_SPM_PMIC_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC delay values after SPM FSM PMIC transaction. SPM wait for the programmed delay before executing the next SPM command.

CPU2_APCS_SAW2_SPM_PMIC_DLY

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:24	DATA_1_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
23:19	RESERVED_BITS23_19	
18:16	DATA_1_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
15:11	RESERVED_BITS15_11	

CPU2_APCS_SAW2_SPM_PMIC_DLY (cont.)

Bits	Name	Description
10:8	DATA_0_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
7:3	RESERVED_BITS7_3	
2:0	DATA_0_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms

0x020A9028 CPU2_APCS_SAW2_SPM_PMIC_DATA_0

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

CPU2_APCS_SAW2_SPM_PMIC_DATA_0

Bits	Name	Description

0x020A902C CPU2_APCS_SAW2_SPM_PMIC_DATA_1

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

CPU2_APCS_SAW2_SPM_PMIC_DATA_1

Bits	Name	Description

0x020A9030 CPU2_APCS_SAW2_RST

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_RST register is used to reset the SAW logic. This register clear itself. It does not reset any SAW2 CSRs. It reset AVS. and SPM FSM and control registers. This is use to clear any hang condition.

CPU2_APCS_SAW2_RST

Bits	Name	Description
31:1	RESERVED31_1	
0	RST	Reset AVS. and SPM FSM and control registers.

0x020A9034 CPU2_APCS_SAW2_SPM_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the delay values for SPM Delay command. SPM wait for the programmed delay before executing the next SPM command.

CPU2_APCS_SAW2_SPM_DLY

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:20	DLY3	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
19:10	DLY2	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
9:0	DLY1	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms

0x020A9080+4*n CPU2_APCS_SAW2_SPM_SLP_SEQ_ENTRY_n

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_SLP_SEQ_ENTRY_n is an array used to sequence through the steps during various power mode. The register width is defined by CLOG_PWR_CTL parameter.

CPU2_APCS_SAW2_SPM_SLP_SEQ_ENTRY_n

Bits	Name	Description

11.21 KPSS CPU2 Timer Registers (0x020AA000 CPU2_APCS_TMR_BASE)

This section contains the Krait Processor Subsystem (KPSS) CPU2 Timer registers.

0x020AA000 CPU2_APCS_TMRSECURE

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Restricted

The APCS_TMRSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Scorpion's APROTNS pin. When APROTNS is set to '0' the state of the APCS_TMRSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_TMRSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_TMRSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_TMRSECURE register correspond to.

CPU2_APCS_TMRSECURE

Bits	Name	Description
31:5	RESERVED	
4	WDT0	Controls security treatment for the Watch Dog Timer registers: APCS_WDT0_FRZ, APCS_WDT0_INT_EN, APCS_WDT0_STS, APCS_WDT0_INT_WIDTH, APCS_WDT0_BARK_TIME, APCS_WDT0_TST_LD_STS, APCS_WDT0_TST_LD. 0x1: NSEC 0x0: SEC
3	WDT1	Controls security treatment for the Watch Dog Timer registers: APCS_WDT1_FRZ, APCS_WDT1_INT_EN, APCS_WDT1_STS, APCS_WDT1_INT_WIDTH, APCS_WDT1_BARK_TIME, APCS_WDT1_TST_LD_STS, APCS_WDT1_TST_LD. 0x1: NSEC 0x0: SEC
2	GPT0	Controls security treatment for the General Purpose Timer registers: APCS_GPT1_MTCH, APCS_GPT1__CNT, APCS_GPT1_EN, APCS_GPT1_CLR and bits 11-8 of APCS_TMR_STS. 0x1: NSEC 0x0: SEC

CPU2_APCS_TMRSECURE (cont.)

Bits	Name	Description
1	GPT1	Controls security treatment for the General Purpose Timer registers: APCS_GPT0_MTCH, APCS_GPT0__CNT, APCS_GPT0_EN, APCS_GPT0_CLR and bits 11-8 of APCS_TMR_STS. 0x1: NSEC 0x0: SEC
0	DGT	Controls security treatment for the Debug Timer registers; APCS_DGT_MTCH, APCS_DGT_CNT, APCS_DGT_EN, APCS_DGT_CLR, APCS_DGT_CLK_CTL, and bits 3-0 of APCS_TMR_STS 0x1: NSEC 0x0: SEC

0x020AA004 CPU2_APCS_GPT0_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: APCS_TMRSECURE [GPT0].

The general purpose timer will signal interrupt when its counter value has reached the value stored in the APCS_GPT0_MTCH register.

CPU2_APCS_GPT0_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_GPT0_CNT at which an interrupt will be generated.

0x020AA008 CPU2_APCS_GPT0_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_CNT register contains the current value of the GPT0 timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_GPT0_MTCH register at the same time due to HW re-use. The procedure for writing the APCS_GPT0_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_GPT0_EN.

- Write APCS_GPT0_CNT.
- Write (to set/restore) APCS_GPT0_MTCH if required.
- Enable the timer by setting the EN bit in APCS_GPT0_EN.

CPU2_APCS_GPT0_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer.

0x020AA00C CPU2_APCS_GPT0_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_EN register is used to enable the GPT0 timer.

CPU2_APCS_GPT0_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	CLR_ON_MTCH_EN	When set (1), the timer will clear when it reaches the match value.
0	EN	When set (1), the timer is enabled and counts with frequency ACC_SLP_CLK.

0x020AA010 CPU2_APCS_GPT0_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_CLR register is a one-shot command register that, when written with any value, resets the timer to a value of 0. This occurs regardless of the state of the APCS_GPT0_EN register.

CPU2_APCS_GPT0_CLR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Data written is not used.

0x020AA014 CPU2_APCS_GPT1_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The GPT timer will signal interrupt when its counter value has reached the value stored in the APCS_GPT1_MTCH register.

CPU2_APCS_GPT1_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_GPT1_CNT at which an interrupt will be generated.

0x020AA018 CPU2_APCS_GPT1_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_CNT register contains the current value of the GPT1 timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_GPT1_MTCH register at the same time. The procedure for writing the APCS_GPT1_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_GPT1_EN.
- Write APCS_GPT1_CNT.
- Write (to set/restore) APCS_GPT1_MTCH if required.
- Enable the timer by setting the EN bit in APCS_GPT1_EN.

CPU2_APCS_GPT1_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer

0x020AA01C CPU2_APCS_GPT1_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_EN register is used to enable the GPT1 timer.

CPU2_APCS_GPT1_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	CLR_ON_MTCH_EN	When set (1), timer will clear when it reaches the match value.
0	EN	When set (1), timer is enabled and counts with frequency sleep clock.

0x020AA020 CPU2_APCS_GPT1_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_CLR register is a one-shot command register that, when written with any value, resets the GPT1 timer to a value of 0. This occurs regardless of the state of the APCS_GPT1_EN register.

CPU2_APCS_GPT1_CLR

Bits	Name	Description
31:0	RESERVED_BITS_31_0	Data written is not used.

0x020AA024 CPU2_APCS_DGT_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The DBG timer will signal interrupt when its counter value has reached the value stored in the APCS_DGT_MTCH register.

CPU2_APCS_DGT_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_DGT_CNT at which an interrupt will be generated.

0x020AA028 CPU2_APCS_DGT_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CNT register contains the current value of the DGT timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_DGT_MTCH register at the same time due to HW re-use. The procedure for writing the APCS_DGT_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_DGT_EN.
- Write APCS_DGT_CNT.
- Write (to set/restore) APCS_DGT_MTCH if required.
- Enable the timer by setting the EN bit in APCS_DGT_EN.

CPU2_APCS_DGT_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer count

0x020AA02C CPU2_APCS_DGT_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_EN register is used to enable the DGT timer.

CPU2_APCS_DGT_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	

CPU2_APCS_DGT_EN (cont.)

Bits	Name	Description
1	CLR_ON_MTCH_EN	When set (1), the timer will clear when it reaches the match value.
0	EN	When set (1), the timer is enabled and counts with frequency TCXO clock.

0x020AA030 CPU2_APCS_DGT_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CLR register is a one-shot command register that, when written with any value, resets the DGT timer to a value of 0. This occurs regardless of the state of the APCS_DGT_EN register.

CPU2_APCS_DGT_CLR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Data written is not used.

0x020AA034 CPU2_APCS_DGT_CLK_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0003

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CLK_CTL controls the clock divider inside the Debug Timer.

NOTE It is possible for the AHB clock to run at as slow as 5 MHz using settings of the Global Clock Controller. The debug timer's counter can also run at 5 MHz (TCXO divided by 4). However, due to the synchronization circuit using the edge detect, the timer should always run at least 4x slower than the AHB clock. Thus, if the timer's use is required by the system, the divider should be set to divide by 4 and the slowest usable AHB frequency is 20MHz. The timer would run at 5MHz in this case.

CPU2_APCS_DGT_CLK_CTL

Bits	Name	Description
31:2	RESERVED_BITS_31_2	

CPU2_APCS_DGT_CLK_CTL (cont.)

Bits	Name	Description
1:0	DIV	0x3: 4 0x2: 3 0x1: 2 0x0: 1

0x020AA038 CPU2_APCS_WDT0_RST

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_RST register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset the watch dog counter. This command register also disables the watchdog freeze

CPU2_APCS_WDT0_RST

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	STB	This bit generates the WDT0_STB during the non-sleep mode. A pulse is generated on WDT0_STB when this bit is written with a '1'.

0x020AA03C CPU2_APCS_WDT0_FRZ

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_FRZ register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the APCS_WDT0_RST register.

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

CPU2_APCS_WDT0_FRZ

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved

CPU2_APCS_WDT0_FRZ (cont.)

Bits	Name	Description
0	FRZ	This bit is used to freeze the watchdog timer at time 0. To enable the watchdog timer auto-kicker, write a '1'.

0x020AA040 CPU2_APCS_WDT0_EN

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_EN register controls when the watch dog timer is enabled.

CPU2_APCS_WDT0_EN

Bits	Name	Description
31:2	RESERVED_BITS_31_2	Reserved
1	INT_EN	Any write to this register: 0x1: yes (any unmasked IRQ or FIQ will enable the WDT0 timer.) 0x0: no
0	EN	Any write to this register: 0x1: yes (the watch dog timer is enabled) 0x0: no

0x020AA044 CPU2_APCS_WDT0_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_STS register is the watchdog status register.

CPU2_APCS_WDT0_STS

Bits	Name	Description
31:3	WDT_CNT	Counter value [28:0] of the watch dog counter. **NOTE** The sleep counter value is sampled using the AHB clk. Multiple reads are required to determine the value (assuming AHB clk is much faster than sleep clock).
2	WDT_RST_STS	Show the status of watchdog0 counter reset.

CPU2_APCS_WDT0_STS (cont.)

Bits	Name	Description
1	AUTOKICK	This bit indicates whether the auto-kicker is on. 0x1: On 0x0: Off
0	RST_STS	0x1: wdt (the last system reset was due to WDT0) 0x0: reset (the last system reset was not due to WDT0.)

0x020AA048 CPU2_APCS_WDT0_INT_WIDTH

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_INT_WIDTH register defines the width of the WDT0 biteExpired pulse in the number of sleep_clk pulses. The default value is 0x0C7C, but this reset value is not readable through the AHB interface.

CPU2_APCS_WDT0_INT_WIDTH

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter value on which to de-assert the WDI bite pulse.

0x020AA04C CPU2_APCS_WDT0_BARK_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (’bark’) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, but this reset value is not readable through the AHB interface. Note that this value is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (’bark’) interrupt.

CPU2_APCS_WDT0_BARK_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter value on which to trigger the bark interrupt.

0x020AA050 CPU2_APCS_WDT0_TST_LD_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TST_LD_STS register indicates when the watchdog test load is synchronizing to the SLP_CLK.

CPU2_APCS_WDT0_TST_LD_STS

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SYNC_STS	When set (1) wdog test load is synchronizing to SLP_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x020AA054 CPU2_APCS_WDT0_TST_LD

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TEST_LD register loads the WDT0_TST register value into the watchdog counter.

CPU2_APCS_WDT0_TST_LD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	LD	Set on this bit to load the value into the WDT0_TST register into the WDT0 counter.

0x020AA058 CPU2_APCS_WDT0_TST

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TST register indicates that the watchdog test is synchronizing to the SLP_CLK and contains the watch dog counter test load value.

CPU2_APCS_WDT0_TST

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter test load value [28:0].

0x020AA05C CPU2_APCS_WDT0_BITE_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_31F3

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_BITE_TIME register determines the counter value at which WDT0 asserts the biteExpired signal.

CPU2_APCS_WDT0_BITE_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog bite time is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 bite expiration time [28:0].

0x020AA060 CPU2_APCS_WDT1_RST

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_RST register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset the watch dog counter. This command register also disables the watchdog freeze

CPU2_APCS_WDT1_RST

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	STB	This bit generates the WDT1_STB during the non-sleep mode. A pulse is generated on WDT1_STB when this bit is written with a ’1

0x020AA064 CPU2_APCS_WDT1_FRZ

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_FRZ register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the APCS_WDT1_RST register.

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

CPU2_APCS_WDT1_FRZ

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	FRZ	This bit is used to freeze the watchdog timer at time 0. To enable the watchdog timer auto-kicker, write a ’1’.

0x020AA068 CPU2_APCS_WDT1_EN

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_EN register controls when the watchdog timer is enabled.

CPU2_APCS_WDT1_EN

Bits	Name	Description
31:2	RESERVED_BITS_31_2	Reserved
1	INT_EN	Any write to this register: 0x1: yes (any unmasked IRQ or FIQ will enable the WDT0 timer.) 0x0: no
0	EN	Any write to this register: 0x1: yes (the watch dog timer is enabled) 0x0: no

0x020AA06C CPU2_APCS_WDT1_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_STS register is the watchdog status register.

CPU2_APCS_WDT1_STS

Bits	Name	Description
31:3	WDT_CNT	Counter value [28:0] of the watch dog counter. **NOTE** The counter value is sampled using the ahb clk. Multiple reads are required to determine the value (assuming ahb clk is much faster than sleep clock).
2	WDT_RST_STS	Show the status of watchdog counter reset.
1	AUTOKICK	This bit indicates whether the auto-kicker is on. 0x1: On 0x0: Off
0	RST_STS	0x1: wdt (the last system reset was due to WDT1) 0x0: reset (the last system reset was not due to WDT1.)

0x020AA070 CPU2_APCS_WDT1_INT_WIDTH

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_INT_WIDTH register defines the width of the WDT1_expired pulse in the number of sleep_clk pulses.The default value is 0x0C7C, but this reset value is not readable through the AHB interface.

CPU2_APCS_WDT1_INT_WIDTH

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter value on which to de-assert the WDI expired pulse.

0x020AA074 CPU2_APCS_WDT1_BARK_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (’bark’) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, but this reset value is not readable through the AHB interface. Note that this value is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (’bark’) interrupt.

CPU2_APCS_WDT1_BARK_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter value on which to trigger the bark interrupt.

0x020AA078 CPU2_APCS_WDT1_TST_LD_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TST_LD_STS register indicates when the watchdog test load is synchronizing to the SLP_CLK.

CPU2_APCS_WDT1_TST_LD_STS

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SYNC_STS	When set (1) wdog test load is synchronizing to SLP_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x020AA07C CPU2_APCS_WDT1_TST_LD

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TEST_LD register loads the WDT1_TST register value into the watchdog counter.

CPU2_APCS_WDT1_TST_LD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	LD	Set on this bit to load the value into the WDT1_TST register into the WDT counter

0x020AA080 CPU2_APCS_WDT1_TST

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TST register indicates that the watchdog test is synchronizing to the SLP_CLK and contains the watch dog counter test load value.

CPU2_APCS_WDT1_TST

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter test load value [28:0]

0x020AA084 CPU2_APCS_WDT1_BITE_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_31F3

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_BITE_TIME register determines the counter value at which WDT1 asserts the biteExpired signal.

CPU2_APCS_WDT1_BITE_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog bite time is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 bite expiration time [28:0].

0x020AA088 CPU2_APCS_TMR_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [WDT0, WDT1, GPT0, GPT1, DGT].

The APCS_TMR_STS can be used to determine the status of each of the SCSS timers in the timer's resident clock domain. Since the timer clock domain may be much slower than the AHB clock, AHB transactions may be delayed in taking effect. This information can be used to qualify other actions or used simply for debug purposes. For example, software can determine when a write to APCS_DGT_CLR has taken effect by examining the DGT_CLR_PEND bit.

Each timer's bits are receive security treatment as specified by the APCS_TMRSECURE register.

CPU2_APCS_TMR_STS

Bits	Name	Description
31	RESERVED_BIT31	
30	WDT1_AUTOKICK	Auto-kicker is on (1) or off (0)
29	WDT1_INT_EN	An unmasked interrupt will enable the timer (1) or not (0)
28	WDT1_EN	Timer is enabled (1) or not (0)
27	RESERVED_BIT27	
26	WDT0_AUTOKICK	Auto-kicker is on (1) or off (0)

CPU2_APCS_TMR_STS (cont.)

Bits	Name	Description
25	WDT0_INT_EN	An unmasked interrupt will enable the timer (1) or not (0)
24	WDT0_EN	Timer is enabled (1) or not (0)
23:20	RESERVED_BIT20_23	
19	GPT1_WR_PEND	Timer has a write pending (1) or not (0)
18	GPT1_CLR_PEND	Timer has a clear pending (1) or not (0)
17	GPT1_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
16	GPT1_EN	Timer is enabled (1) or not (0)
15:12	RESERVED_BITS15_12	
11	GPT0_WR_PEND	Timer has a write pending (1) or not (0)
10	GPT0_CLR_PEND	Timer has a clear pending (1) or not (0)
9	GPT0_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
8	GPT0_EN	Timer is enabled (1) or not (0)
7:4	RESERVED_BITS7_4	
3	DGT_WR_PEND	Timer has a write pending (1) or not (0)
2	DGT_CLR_PEND	Timer has a clear pending (1) or not (0)
1	DGT_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
0	DGT_EN	Timer is enabled (1) or not (0)

11.22 KPSS CPU3 ACC Registers (0x020B8000 CPU3_APCS_ACC_BASE)

This section contains the Krait Processor Subsystem (KPSS) CPU3 ACC registers.

0x020B8000 CPU3_APCS_ACCSECURE

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0007

Security Treatment: Restricted

The APCS_ACCSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Krait's APROTNS pin. When APROTNS is set to '0' the state of the APCS_ACCSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_ACCSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_ACCSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_ACCSECURE register correspond to.

CPU3_APCS_ACCSECURE

Bits	Name	Description
31:4	RESERVED	
31:3	RESERVED_BITS31_3	
2	TST	Controls security treatment for test control registers: APCS_ATSTBUS_SEL 0x1: NSEC 0x0: SEC
1	CLK_CTL	Controls security treatment for the clock control registers: APCS_ACC_STS, APCS_CPU_AUX_CLK_SEL. 0x1: NSEC 0x0: SEC
0	SLP_CTL	Controls security treatment for the sleep control registers: APCS_CPU_PWR_CTL, APCS_CPU_TRGTD_DBG_RST. 0x1: NSEC 0x0: SEC

0x020B8004 CPU3_APCS_CPU_PWR_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0109

Security Treatment: Controlled by APCS_ACCSECURE [SLP_CTL].

The APCS_CPU_PWR_CTL register is used to control the clamps, reset and array head switches.

CPU3_APCS_CPU_PWR_CTL

Bits	Name	Description
31:21	RESERVED_BITS31_21	
20:16	CLK_EN	Clock enables for CORE clock. This is only to workaround hardware dynamic clock gating problems. [20:18]= SYS_apcNAux_Clk[3:1] [17] = SYS_apcsRef_Clk [16] = SYS_apcNPll_Clk 0x1: Always enabled 0x0: dynamically enabled by hardware
15:10	RESERVED_BITS15_10	
9	RET_SLP_REQ	When set, this bit request the L2SCU to in-flight snoop operation and block new snoops request from entering FIFO. This control is intended to permit external masters such as the RPM to put CPU to retention sleep modes, when power control is being done by an external master instead of the SPM. The output of this register bit is ORed with a retention sleep request control output from the SPM, so that if either the SPM asserts the control, or the RPM sets this bit, the CPU's snoop FIFO is quiesce.
8	PLL_CLAMP	When set, this bit clamp the output of TDC logic in PLL. This signal that must be asserted prior to collapsing CPU voltage, vdd_apc0. This bit is ORed with SAW output before passing to the APC PLL.
7	CORE_PWRD_UP	Report that the CPU is powered up.
6	GATE_CLK	When set, this bit forces the CPU clock to be gated off. This control is intended to permit external masters such as the RPM to gate off the CPU clock during sleep modes, when power control is being done by an external master instead of the SPM. The output of this register bit is ORed with a clock gating control output from the SPM, so that if either the SPM asserts the control, or the RPM sets this bit, the CPU clock will be gated off. When set, this bit gate the CPU clock that must be asserted during sleep state. This bit is ORed with a SAW output before passing to the CPU core.
5	COREPOR_RST	When set, this bit asserts corepor areset to the CPU core.
4	CORE_RST	When set, this bit asserts core areset to the COPU core.

CPU3_APCS_CPU_PWR_CTL (cont.)

Bits	Name	Description
3	L2DT_SLP	When set, this bit opens a head switch to put the L2 duplicate tag array into a low-leakage, non-data-retaining state. This bit is ORed with a SAW output before passing to the CPU core. The controlled memory array contains a duplicate of the tags contained in the L1 data cache, and is used by the L2 to snoop and see if a shared memory access from one processor necessitates invalidating a line in another processor's L1 data cache. Thus, this memory array generally can be offline when the associated CPU is power-collapsed and its L1 data cache is also off-line.
2	RESERVED_BIT2	Previously ETB HS
1	RESERVED_BIT1	Previously L1 HS
0	CLAMP	When set, this bit asserts the clamp signal that must be asserted prior to collapsing CPU voltage, vdd_apc0. This bit is ORed with SAW output before passing to the CPU core.

0x020B8008 CPU3_APCS_ACC_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: N/A

Security Treatment: Controlled by APCS_ACCSECURE [CLK_CTL].

The APCS_ACC_STS register is used to monitor the output of the clock gating cells.

CPU3_APCS_ACC_STS

Bits	Name	Description
31:18	RESERVED_BITS31_18	
17	RET_SLP_ACK	This bit reflect the status of APCN_sysRetSlpAck bit. L2 assert the signal when it see the APCN_sysRetSlpReq and CPU snoop FIFO is quiesced. L2 de-assert this signal after APCN_sysRetSlpReq is de-asserted and all snoop invalidation is completed.
16	SLP_CLK	This bit reflect the status of APCN_sleepClkOnReq bit
15	AHB_CLK	This bit reflect the status of APCN_ahbClkOnReq bit
14	REF_CLK	This bit reflect the status of APCN_refClkOnReq bit
13	SPM_SLP_STATE	This bit reflect the status of SPM Sleep State
12	FRC_CLK_OFF	This bit reflect the status of APCN_apccForceClocksOff bit
11	RET_SLP_REQ	This bit reflect the status of APCN_apccRetSlpReq bit
10	TRGTD_DBG_RST	This bit reflect the status of APCN_apcTargetedDbg_Areset_N bit
9	CORE_RST	This bit reflect the status of APCN_apccCore_Areset_N bit
8	COREPOR_RST	This bit reflect the status of APCN_apccCorePor_Areset_N bit

CPU3_APCS_ACC_STS (cont.)

Bits	Name	Description
7	L2DT_HS	This bit reflect the status of the SYS_apcNSwCtlDupTagArrayCollapse bit
6	CLAMP	This bit reflect the status of the SYS_apcNClampApcNvd bit.
5:3	CORE_AUX_CLK	This bits reflect the status of the APCS_sysApcNAuxClkOnReq bits.
2	CORE_PLL_CLK	This bit reflect the status of the APCS_sysApcNPllClkOnReq bit.
1	CORE_NO_PWR_DWN	This bit reflect the status of the APCN_dbgCoreNoPwrDwn bits.
0	CORE_PWRUP_REQ	This bit reflect the status of the APCN_dbgCorePwrUpReq bits.

0x020B800C CPU3_APCS_ATSTBUS_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [TST].

APCS_ATSTBUS_SEL selects different modules' test bus outputs.

CPU3_APCS_ATSTBUS_SEL

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	EN	Set to 1 to cause APCS to drive the test bus outputs. 0x1: enabled 0x0: disabled
1:0	SEL	0x3: CONSTANT 0x2: SAW 0x1: TMR 0x0: CLK

0x020B8010 CPU3_APCS_CPU_TRGTD_DBG_RST

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [SLP_CTL].

APCS_CPU_TRGTD_DBG_RST is used to reset the CPU core debug logic. The hardware clear the register after the CPU debug logic is reset. Software need to poll this register to check if the reset is complete.

CPU3_APCS_CPU_TRGTD_DBG_RST

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	RST	When set this bit de-assert SYS_apcNTargetedDbg_Areset_N to the CPU core for 32 REF clock cycle to the CPU core. At the end of the reset hardware clear this bit.

0x020B8014 CPU3_APCS_CPU_AUX_CLK_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_ACCSECURE [CLK_CTL]

The APCS_CPU_AUX_CLK_SEL register controls the gfmux which selects the AUX clock source for the Krait CPU clock. An additional selection set is provided to determine the clock source for the Krait core (4-1 GFMUX) in the Krait Hard Macro. The QSB clock is the raw source clk at reset.

CPU3_APCS_CPU_AUX_CLK_SEL

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	AUX_SRC	Krait CPU AUX clock select: 0x3: SYS_apcNAux_Clk_1 0x2: SYS_apcNAux_Clk_2 0x1: SYS_apcNAux_Clk_3 0x0: SYS_apcsRef_Clk

11.23 KPSS GCC Registers (0x02011000 APCS_GCC_BASE)

This section contains the Krait Processor Subsystem (KPSS) GCC Secure registers.

0x02011000 APCS_GCCSECURE

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0007

Security Treatment: Restricted

The APCS_GCCSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Krait's APROTNS pin. When APROTNS is set to '0' the state of the APCS_GCCSECURE register is not considered; a secure transaction is always allowed. When APROTNS is set to '1', the APCS_GCCSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_GCCSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_GCCSECURE register correspond to.

APCS_GCCSECURE

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	TST	Controls security treatment for the global test control registers: APCS_ALL_TSTBUS_SEL, APCS_CLK_DIAG, APCS_SPARE, APCS_SPARE_STS 0x1: NSEC 0x0: SEC
1	SLP_CTL	Controls security treatment for the global sleep control registers: APCS_L2_PWR_CTL, APCS_PWR_STS, APCS_DBG_PWR_CTL 0x1: NSEC 0x0: SEC
0	CLK_CTL	Controls security treatment for the global clock control registers: APCS_PWR_CTL_OVERRIDE, APCS_GCLK_STS, APCS_L2_AUX_CLK_SEL 0x1: NSEC 0x0: SEC

0x02011004 APCS_IPC_SECURITY

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Restricted

The APCS_IPC_SECURITY register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Krait's APROTNS pin. When APROTNS is set to '0' the state of the APCS_IPC_SECURITY register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_IPC_SECURITY register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_IPC_SECURITY register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_IPC_SECURITY register correspond to.

APCS_IPC_SECURITY

Bits	Name	Description
31:0	IPC_SEC	User-defined. (Each bit in this register controls access to the corresponding bit in the APCS_IPC).

0x02011008 APCS_IPC

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_IPC_SECURITY on a bit-wise basis.

Inter-process communication signals from Krait to other masters.

APCS_IPC

Bits	Name	Description
31:0	IPC_INT	User-defined. (Each bit can be written and it will cause an IPC interrupt).

0x0201100C APCS_PWR_CTL_OVERRIDE

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [CLK_CTL].

The APCS_PWR_CTL_OVERRIDE register is used to enable the global APCS clocks. This is used to workaround hardware dynamic clock gating problems.

APCS_PWR_CTL_OVERRIDE

Bits	Name	Description
31:17	RESERVED_BITS31_17	
16	L2_RET_SLP_DIS	When set, this bit will take L2 array out of retention mode. This bit needs to be set before the vdd_mem voltage is lowered. The L2 data will be lost if vdd_mem is lowered to a voltage level such that the internal array voltage is below the retention voltage.
15:10	RESERVED_BITS15_10	
9:0	CLK_EN	Clock enables for global APCS clocks. This is only to work-around hardware dynamic clock gating problems. [9:7]= SYS_apcsL2Aux_Clk[3:1] [6] = SYS_apccL2Pll_Clk [5] = ATB_apcc_Clk [4] = APB_apccDbg_Clk [3] = SYS_apcsPiSleep_Clk [2] = SYS_apcsRef_Clk [1] = SYS_apcsAhb_Clk [0] = SYS_apcsQsb_Clk 0x1: Always enabled 0x0: dynamically enabled by hardware

0x02011010 APCS_GCLK_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: N/A

Security Treatment: Controlled by APCS_GCCSECURE [CLK_CTL].

The APCS_GCLK_STS register is used to monitor the output of the clock gating cells.

APCS_GCLK_STS

Bits	Name	Description
31:10	RESERVED_BITS31_10	

APCS_GCLK_STS (cont.)

Bits	Name	Description
9:0	STS	Status for global APCS clocks [9:7]= APCS_sysL2AuxClkOnReq [6] = APCS_sysL2PllClkOnReq [5] = APCS_sysAtbClkOnReq [4] = APCS_sysApbDbgClkOnReq [3] = APCS_sysSleepClkOnReq [2] = APCS_sysRefClkOnReq [1] = APCS_sysAhbClkOnReq [0] = APCS_sysQsbClkOnReq 0x1: toggling, 0x0: halted

0x02011014 APCS_L2_PWR_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_8100

Security Treatment: Controlled by APCS_GCCSECURE [SLP_CTL].

The APCS_L2_PWR_CTL register controls the L2 Global Distrubuted Head Switch and L2 array head switches.

APCS_L2_PWR_CTL

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	L2_HS_CNT	Count value for headswitched L2 logic
15	PLL_CLAMP	When set, this bit clamp the output of TDC logic in PLL. This signal must be asserted prior to opening the l2swvd head switch.This bit is ORed with SAW output before passing to the L2 PLL .
14	LVE	When set, this bit select the ACC value for low voltage mode for all Krait L2 RAMs.
13	L2_RET_SLP	When set, this bit will put the L2 array in retention mode resulting in lower cache array leakage.The data in the L2 array is retained.. This is ORed with SAW output before passing to the CPU.
12	SYS_RESET	Setting this bit asserts the SYS_apccSys_Areset_N input to the Krait CPU, causing a warm system reset (all powered non-debug logic will be reset) to the CPU core without resetting subsystem functions such as timers, clock control, etc.
11	RESERVED_BIT11	Previous drive SYS_scQdmapHaltReq (resets to 1)
10	L2_HS_RST	When set, this bit asserts reset to the headswitched L2 logic

APCS_L2_PWR_CTL (cont.)

Bits	Name	Description
9	L2_HS_EN	When set, this bit closes the switches for the headswitched L2 logic, putting it into an operational state
8	L2_HS_CLAMP	When set, this bit clamps the outputs from the headswitched L2 logic into the unswitched domain This bit is ORed with SAW outputs before passing to the CPU(resets to 1).
7:4	RESERVED_BITS7_4	
3:2	L2_ARRAY_HS3_2	(Reserved if NUM_CPU < 4). Only for QUAD Krait variant (2 MB L2). When set, these bits open the array head switches for 512 KB sections of the L2 cache array, resulting a lower cache array leakage when data does not need to be retained in the array. These bits are ORed with SAW outputs before passing to the CPU
1:0	L2_ARRAY_HS1_0	When set, these bits open the array head switches for 512 KB sections of the L2 cache array, resulting a lower cache array leakage when data does not need to be retained in the array. These bits are ORed with SAW outputs before passing to the CPU

0x02011018 APCS_PWR_STS

Type: Read Only
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_GCCSECURE [SLP_CTL].

The APCS_PWR_STS register contains the status bits necessary to support an MP with foot switched L2.

APCS_PWR_STS

Bits	Name	Description
31:15	RESERVED_BITS31_15	
14:13	L2_HS_STS3_2	(Reserved if NUM_CPU < 4). Only for QUAD Krait variant (2MB L2). This bit reflects the status of APCS_apccSwCtlL2ArrayCollapse[3:2] signal
12	SPM_SLP_STATE	This bit reflects the status of L2 SPM Sleep state.
11	SAW_SLP_ACK	This bit reflects the status of APCS_apccL2SleepAck signal
10	DBG_RST_STS	This bit reflects the status of APCS_apccDbg_Areset_N signal
9	L2_HS_RST_STS	This bit reflects the status of APCS_apccL2swvd_Areset_N signal
8	L2_CLMP_STS	This bit reflects the status of APCS_apccClampL2swvd signal

APCS_PWR_STS (cont.)

Bits	Name	Description
7	L2_RET_SLP_STS	This bit reflects the status of APCS_apccSwCtlL2RetentionSleep signal
6:5	L2_HS_STS1_0	This bit reflects the status of APCS_apccSwCtlL2ArrayCollapse[1:0] signal
4	DBG_PWRUP_REQ	This bit reflects the status of SYS_apcsDbgPwrUpReq
3	L2_FS_STS	Status for foot-switched L2 logic
2	RESERVED_BITS2	Legacy SC_sysQdmapHaltAck signal
1	L2_CLK_IDLE	This bit reflects the status of the APCC_sysL2ClkIdle signal
0	L2_SLV_IDLE	This bit reflects the status of the APCC_qsbSlvIdle signal

0x0201101C APCS_CLK_DIAG

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [TST].

The APCS_CLK_DIAG register selects the test clock to be output from the APCS to the chip's clock controller. It also controls the functional inputs to the Boundary Scan block.

NOTE The Krait core Leaf clock is always sent to the chip's clock controller as the first test clock. Under proper configuration of the chip's clock controller and the GPIO, this clock can be observed at either the EXT_CLK or through the clock debug test bus.

APCS_CLK_DIAG

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	FAST_CLK_EN	Enable the Krait Diagnostic clock from the leaf of the clock tree.
6	FAST_CLK_INV	Invert the Krait Diagnostic clock output.
5:3	FAST_CLK_SEL	Selects the Krait HS Leaf clock to output for test mode. 0x0: APC0_sysLeaf_Clk 0x1: APC1_sysLeaf_Clk 0x2: APCC_sysL2Leaf_Clk 0x3: SYS_apcsQsb_Clk 0x4: APC2_sysLeaf_Clk (Quad Krait Variant only) 0x5: APC3_sysLeaf_Clk (Quad Krait Variant only) 0x6: Reserved_1 0x7: Reserved_2

APCS_CLK_DIAG (cont.)

Bits	Name	Description
2:0	SLOW_CLK_SEL	Selects the APCS slow clock to output for test mode. 0x0: None (No clock selected, tied low.) 0x1: SYS_apcsAhb_Clk 0x2: SYS_apcsRef_Clk 0x3: SYS_apcsPiSleep_Clk 0x4: APB_apccDbg_Clk 0x5: ATB_apcc_Clk 0x6: Reserved_1 0x7: Reserved_2

0x02011020 APCS_ALL_TSTBUS_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [TST].

The APCS_ALL_TSTBUS_SEL register selects which module's test bus output will be sent out of the subsystem.

APCS_ALL_TSTBUS_SEL

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	EN	Set to 1 to cause APCS to drive the test bus outputs. 0x1: enabled 0x0: disabled
3:0	SEL	For each category, see appropriate selections for control of the output. 0x6: CONSTANT 0x5: L2 GDHS (SAW2.) 0x4: GLB (global testbus) 0x3: APC3 (Reserved if NUM_CPU < 4.) 0x2: APC2 (Reserved if NUM_CPU < 3.) 0x1: APC1 (Reserved if NUM_CPU < 2) 0x0: APC0

0x02011024 APCS_DBG_PWR_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [SLP_CTL].

The APCS_DBG_PWR_CTL register is used for debugger communication. The REQ bit is used to enable a signal to the RPM to assert a power up sequence when the APCS's interrupt controller receives any enabled interrupt. The clocks need not be running for this signal to propagate.

APCS_DBG_PWR_CTL

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	REQ	Setting this bit asserts APCS_dbgPwrUpInt. Note that this signal can also be set by hardware.

0x02011028 APCS_L2_AUX_CLK_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [CLK_CTL]

The APCS_L2_AUX_CLK_SEL register controls the gfmux which selects the AUX clock source for the Krait MP's L2 clock. An additional selection set is provided to determine the clock source for the Krait core (4-1 GFMUX) in the Krait Hard Macor. The QSB clock is the raw source clk at reset.

APCS_L2_AUX_CLK_SEL

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	AUX_SRC	Krait AUX clock select: 0x3: SYS_apcsL2Aux_Clk_1 0x2: SYS_apcsL2Aux_Clk_2 0x1: SYS_apcsL2Aux_Clk_3 0x0: SYS_apcsRef_Clk

0x0201102C APCS_SPARE

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [TST].

The APCS_SPARE register is used for ECO. The output of this register is controlled by BSL.

APCS_SPARE

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BITS	SPARE BITS for ECO

0x02011030 APCS_SPARE_STS

Type: Read Only
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [TST].

The output of the APCS_SPARE BSL register.

APCS_SPARE_STS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BITS	SPARE BITS for ECO

0x02011FD0 APCS_VERSION

Type: Read Only
Clock: SYS_AHB_CLK
Reset State: 0x1001_0000
Security Treatment: Controlled by APCS_GCCSECURE [CLK_CTL].

This read only register reports the hardware version information for the KPSS core.

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APCS_VERSION

Bits	Name	Description
31:28	MAJOR	Indicate different interface version. Major version changes are not backward compatible
15:0	MINOR	Indicates expanded functionality. Minor versions add functionality while being backward compatible
15:0	STEP	Indicates a change in the hardware which is not intended to impact software

11.24 KPSS CPU3 SAW2 Registers (0x020B9000 CPU3_APCS_SAW2_BASE)

This section contains the Krait Processor Subsystem (KPSS) CPU3 SAW2 registers.

11.24.1 SAW2 Registers

The SAW2 (SPM and AVS. Wrapper2) design is an AHB slave that contains both SPM and AVS. CSRs.

0x020B9000 CPU3_APCS_SAW2_SECURE

Type: Read/write
Clock: SYS_REF_CLK
Reset State: {3{CFGNSINIT}}

Security Treatment: Restricted

The SAW2_SECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by ahb_saw_hprotns pin. When ahb_saw_hprotns is set to ’0’ the state of the SAW2_SECURE register is not considered - a secure transaction is always allowed. When ahb_saw_hprotns is set to ’1’, the SAW2_SECURE register security treatment bit of that register must be ’1’ for access to be granted. If the security treatment bit of the register is set to ’0’, the non-secure (ahb_saw_hprotns = ’1’) transactions are denied. When access is denied, a write is ignored, and a read will return ’0’. No error is signaled.

When reading the SAW2_SECURE register, non-secure agents will always read ’0’. Secure agents will see the actual value of the register. The reset value is controlled by CFGNSINIT input pin.

CPU3_APCS_SAW2_SECURE

Bits	Name	Description
31:3	RESERVED	
2	SAW_CTL	Controls security treatment for SAW2 registers: SAW2_ID, SAW2_CFG, SAW2_STS_0, SAW2_STS_1, SAW2_RST 0x1: NSEC 0x0: SEC
1	PWR_CTL	Controls security treatment for SPM registers: SAW2_SPM_CTL, SAW2_SPM_PMIC_DLY, SAW2_SPM_PMIC_DATA_0, SAW2_SPM_PMIC_DATA_1, SAW2_SPM_SLP_SEQ_ENTRY_n, SAW2_SPM_DLY 0x1: NSEC 0x0: SEC
0	VLT_CTL	Controls security treatment for the AVS. registers: SAW2_AVS_CTL, SAW2_VLVL, SAW2_AVS_HYSTERESIS 0x1: NSEC 0x0: SEC

0x020B9004 CPU3_APCS_SAW2_ID

Type: Read
Clock: SYS_REF_CLK
Reset State: Undefined

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register reports the revision and parameter information for the SAW2 core.

CPU3_APCS_SAW2_ID

Bits	Name	Description
31	RESERVED_BITS31	
30:25	NUM_SPM_ENTRY	SAW2 parameter: Indicates number of SAW2_SPM_SLP_SEQ_ENTRY register implemented. Value can range from 1 - 32
24:20	NUM_PWR_CTL	SAW2 parameter: Indicates number of power control implemented. Value can range from 2 - 16
19	RESERVED_BITS19	
18	PMIC_ARB_INTF	SAW2 parameter: Indicates PMIC Arbiter Interface function is implemented
17	AVS_PRESENT	SAW2 parameter: Indicates AVS. function is implemented
16	SPM_PRESENT	SAW2 parameter: Indicates SPM function is implemented
15:12	MAJOR	Major variant
11:0	MINOR	Minor variant

0x020B9008 CPU3_APCS_SAW2_CFG

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_CFG register is used to configure the common control between AVS. and SPM.system.

CPU3_APCS_SAW2_CFG

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12	FRC_REF_CLK_ON	Chicken bit to force saw_sys_ref_clk_on_req ON.
11:8	ADR_IDX	PMIC Arbiter Address Index. Drive the saw_pmic_addr_idx output port.

CPU3_APCS_SAW2_CFG (cont.)

Bits	Name	Description
7:6	RESERVED_BITS7_6	
5	PMIC_MODE	PMIC Handshake 0x0: 8K_PMIC (only DONE signal) 0x1: 7K_PMIC (both ACK and DONE signals)
4:0	CLK_DIV	Divider ratio for clock. This is used to generate timer tick for the timer. Timer tick is asserted every (CLK_DIV + 1) sys_ref_clk period. ..... For sys_ref_clk = 20 MHz (53ns) The timer tick range 53 ns to 1.6us. 0x0: Timer Tick every sys_ref_clk 0x1F: Timer Tick every 128 sys_ref_clk.

0x020B900C CPU3_APCS_SAW2_STS_0

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

CPU3_APCS_SAW2_STS_0

Bits	Name	Description
15	SHTDWN_REQ	This bit reflects the shutdown request from the SPM(spm_rpm_shutdown_req) to RPM.
14	SHTDWN_ACK	This bit reflects the shutdown acknowledgement from the RPM(rpm_spm_shutdown_ack) to SPM.
13	BRNGUP_REQ	This bit reflects the bringup request from the SPM(spm_rpm_bringup_req) to RPM.
12	BRNGUP_ACK	This bit reflects the bringup acknowledgement from the RPM(rpm_spm_bringup_ack) to SPM.
11:10	PMIC_STATE	State of the PMIC FSM: transitions back to IDLE) transitions back to IDLE) 0x0: IDLE (waiting for PMIC transaction from AVS. or SPM) 0x1: ACK (waiting for ACK from PMIC Arb) 0x2: DONE (waiting for DONE form PMIC Arb before) 0x3: DELAY (waiting for delay count termination before)

CPU3_APCS_SAW2_STS_0 (cont.)

Bits	Name	Description
9:8	RPM_STATE	State of the RPM FSM: 0x0: RUN (waiting for SPM request) 0x1: STDNACK (waiting for shutdown ACK from RPM) 0x2: WAKEUP (waiting for wakeup interrupt) 0x3: BGUPACK (waiting for bringup ACK from RPM)
7	AVS_STATE	State of the AVS. FSM: indication) 0x0: IDLE (waiting to be enabled or for next UP/DOWN) 0x1: REQ (waiting for PMIC FSM to transition to IDLE)
6:0	SPM_CMD_ADDR	Last SPM command executed.

0x020B9010 CPU3_APCS_SAW2_STS_1

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

CPU3_APCS_SAW2_STS_1

Bits	Name	Description
31	RESERVED1	
30	SW_WR_PEND	This bit reflects the VLVL state of the request from the SAW2_VCTL write is pending.
29	CPU_UP	This bit reflects the VLVL state of the request from the CPU (avs_saw_up) to raise the VLVL.
28	CPU_DN	This bit reflects the VLVL state of the request from the CPU (avs_saw_down) to lower the VLVL.
27	MAX_INT	IRQ status bit, AVS. controller detected that raising the VLVL by AVS_CTL[VLVL_STEP] would result in a value greater than AVS_CTL[MAX_VLVL]. If AVS_CTL[IRQ_MAX_EN] is set, an interrupt is issued. NOTE that SW can set MAX_VLVL lower than current VLVL creating a condition where VLVL is higher than MAX_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MAX.

CPU3_APCS_SAW2_STS_1 (cont.)

Bits	Name	Description
26	MIN_INT	IRQ status bit, AVS. controller detected that lowering the VLVL by SAW2_AVS_CTL[VLVL_STEP] would result in a value less than SAW2_AVS_CTL[MIN_VLVL]. If SAW2_AVS_CTL[IRQ_MIN_EN] is set, an interrupt is issued. NOTE that SW can set MIN_VLVL higher than current VLVL creating a condition where VLVL is lower than MIN_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MIN.
25:16	CURR_DLY	VLVL value of the counter used to calculate the time until the next AVS. controller request for a new VLVL.

0x020B9014 CPU3_APCS_SAW2_VCTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

Though this register is read/writable, it also causes a command pulse to the PMIC FSM. Writing this register results in a transaction to the PMIC with SAW2_VCTL being sent to the PMIC. SAW2 support both 8901 and 8058 regulator.

CPU3_APCS_SAW2_VCTL

Bits	Name	Description
31:16	RESERVED_BITS31_16	

0x020B9018 CPU3_APCS_SAW2_AVS_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_CTL register is used to control the Adaptive Voltage Scaling (AVS) system.

CPU3_APCS_SAW2_AVS_CTL

Bits	Name	Description
31	RESERVED	

CPU3_APCS_SAW2_AVS_CTL (cont.)

Bits	Name	Description
30	VLVL_WIDTH	Defines the VLVL field of PMIC data. SAW2 at minimum supports 8901 and 8058 regulator. See PMIC document for details. 0x0: 5 bits VLVL (8058 regulator) 0x1: 6 bits VLVL (8901 regulator)
29:28	VLVL_STEP	Controls the step size of each request to PMIC Arbiter. SW may use values from 0 to 3. Note that the value 0 will result in no change - that is if the CPU requests UP or DOWN, the CURR_PVLVL will be sent to the PMIC Arbiter. This may be useful for debug. If an increment or decrement operation would cause the current VLVL to transition above or below the MAX_VLVL or MIN_VLVL, the current VLVL will not be changed. An interrupt will be signaled if IRQ_MAX/MIN_EN is 1
27	EN	AVS. Enable. **NOTE** Setting to 0 does not disable any pending interrupts. **NOTE** AVS. FSM and SPM FSM are mutually exclusive. Only one FSM is active at a time. SW does not have to disable AVS. before going to sleep. 0x0: Disable AVS 0x1: Enable AVS
26	SW_DONE_INT_EN	Set to 1 to turn on AVS. interrupt for when a SW initiated voltage change has completed. Set to 0 to mask it (turn it off). ASSERTION: This interrupt is asserted only after a SW write to SAW2_AVS_VLVL. Specifically, after the AVS. FSM traverses through all its states and transitions back to IDLE, the interrupt line is pulsed. The interrupt controller should be set to edge capture to receive this interrupt. CLEARING: None. This interrupt is a pulse, SW does not need to clear it (aside from requirements of the interrupt controller).
25	MAX_INT_EN	Set to 1 to turn on AVS. interrupt for MAX_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be greater than MAX_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit.
24	MIN_INT_EN	Set to 1 to turn on AVS. interrupt for MIN_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be smaller than MIN_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit
23	RESERVED_23	

CPU3_APCS_SAW2_AVS_CTL (cont.)

Bits	Name	Description
22:17	MAX_VLVL	Control maximum value of AVS. controller's VLVL. When current VLVL reaches this value it may not grow any larger. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level higher, an interrupt is issued. This value may be updated at anytime. Setting to a value lower than MIN_VLVL is not supported, and unpredictable results may occur.
16	RESERVED_16	
15:10	MIN_VLVL	Control the minimum value of AVS. controller's VLVL. When the current VLVL reaches this level it may not shrink any smaller. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level lower, an interrupt is issued. This value may be updated at anytime. Setting to a value higher than MAX_VLVL is not supported, and unpredictable results may occur.
9:0	AVS_DELAY	Control the time between AVS. controller's requests to change the VLVL

0x020B901C CPU3_APCS_SAW2_AVS_HYSTERESIS

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_HYSTERESIS register is used to delay the AVS. UP/DN signal to AVS. FSM. This is used to prevent the false PMIC step due to PDN noise.

CPU3_APCS_SAW2_AVS_HYSTERESIS

Bits	Name	Description
31:24	RESERVED31_24	
23:16	DN_COUNT	HYSTERESIS DN COUNT. Delays of PMIC DN step operation.
15:8	RESERVED15_8	
7:0	UP_COUNT	HYSTERESIS UP COUNT. Delays of PMIC UP step operation.

0x020B9020 CPU3_APCS_SAW2_SPM_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_CTL register is used to control the subsystem power management system. This are parameters that controls the operation of SPM FSM.

CPU3_APCS_SAW2_SPM_CTL

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	SPM_START_ADR	Start address for the SPM sequence.
3	ISAR	Inhibit Start Address Reset 0x0: End of program reset the SPM_START_ADR to zero. 0x1: Inhibit End of program to reset SPM_START_ADR
2:1	WAKEUP_CONFIG	Wakeup Configuration 0x0: sys_spm_wakeup 0x1: sys_spm_wakeup or !cpu_spm_wait_req 0x2: sys_spm_wakeup or rising edge of sys_spm_dbg_nopwrdwn 0x3: sys_spm_wakeup or !cpu_spm_wait_req or rising edge of sys_spm_dbg_nopwrdwn
0	SPM_EN	SPM En.

0x020B9024 CPU3_APCS_SAW2_SPM_PMIC_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC delay values after SPM FSM PMIC transaction. SPM wait for the programmed delay before executing the next SPM command.

CPU3_APCS_SAW2_SPM_PMIC_DLY

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:24	DATA_1_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
23:19	RESERVED_BITS23_19	
18:16	DATA_1_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
15:11	RESERVED_BITS15_11	

CPU3_APCS_SAW2_SPM_PMIC_DLY (cont.)

Bits	Name	Description
10:8	DATA_0_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
7:3	RESERVED_BITS7_3	
2:0	DATA_0_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms

0x020B9028 CPU3_APCS_SAW2_SPM_PMIC_DATA_0

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

CPU3_APCS_SAW2_SPM_PMIC_DATA_0

Bits	Name	Description

0x020B902C CPU3_APCS_SAW2_SPM_PMIC_DATA_1

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

CPU3_APCS_SAW2_SPM_PMIC_DATA_1

Bits	Name	Description

0x020B9030 CPU3_APCS_SAW2_RST

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_RST register is used to reset the SAW logic. This register clear itself. It does not reset any SAW2 CSRs. It reset AVS. and SPM FSM and control registers. This is use to clear any hang condition.

CPU3_APCS_SAW2_RST

Bits	Name	Description
31:1	RESERVED31_1	
0	RST	Reset AVS. and SPM FSM and control registers.

0x020B9034 CPU3_APCS_SAW2_SPM_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the delay values for SPM Delay command. SPM wait for the programmed delay before executing the next SPM command.

CPU3_APCS_SAW2_SPM_DLY

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:20	DLY3	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
19:10	DLY2	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
9:0	DLY1	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms

0x020B9080+4*n CPU3_APCS_SAW2_SPM_SLP_SEQ_ENTRY_n

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_SLP_SEQ_ENTRY_n is an array used to sequence through the steps during various power mode. The register width is defined by CLOG_PWR_CTL parameter.

CPU3_APCS_SAW2_SPM_SLP_SEQ_ENTRY_n

Bits	Name	Description

11.25 KPSS CPU3Timer Registers (0x020BA000 CPU3_APCS_TMR_BASE)

This section contains the Krait Processor Subsystem (KPSS) CPU3 Timer registers.

0x020BA000 CPU3_APCS_TMRSECURE

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Restricted

The APCS_TMRSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Scorpion's APROTNS pin. When APROTNS is set to '0' the state of the APCS_TMRSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_TMRSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_TMRSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_TMRSECURE register correspond to.

CPU3_APCS_TMRSECURE

Bits	Name	Description
31:5	RESERVED	
4	WDT0	Controls security treatment for the Watch Dog Timer registers: APCS_WDT0_FRZ, APCS_WDT0_INT_EN, APCS_WDT0_STS, APCS_WDT0_INT_WIDTH, APCS_WDT0_BARK_TIME, APCS_WDT0_TST_LD_STS, APCS_WDT0_TST_LD. 0x1: NSEC 0x0: SEC
3	WDT1	Controls security treatment for the Watch Dog Timer registers: APCS_WDT1_FRZ, APCS_WDT1_INT_EN, APCS_WDT1_STS, APCS_WDT1_INT_WIDTH, APCS_WDT1_BARK_TIME, APCS_WDT1_TST_LD_STS, APCS_WDT1_TST_LD. 0x1: NSEC 0x0: SEC
2	GPT0	Controls security treatment for the General Purpose Timer registers: APCS_GPT1_MTCH, APCS_GPT1__CNT, APCS_GPT1_EN, APCS_GPT1_CLR and bits 11-8 of APCS_TMR_STS. 0x1: NSEC 0x0: SEC

CPU3_APCS_TMRSECURE (cont.)

Bits	Name	Description
1	GPT1	Controls security treatment for the General Purpose Timer registers: APCS_GPT0_MTCH, APCS_GPT0__CNT, APCS_GPT0_EN, APCS_GPT0_CLR and bits 11-8 of APCS_TMR_STS. 0x1: NSEC 0x0: SEC
0	DGT	Controls security treatment for the Debug Timer registers; APCS_DGT_MTCH, APCS_DGT_CNT, APCS_DGT_EN, APCS_DGT_CLR, APCS_DGT_CLK_CTL, and bits 3-0 of APCS_TMR_STS 0x1: NSEC 0x0: SEC

0x020BA004 CPU3_APCS_GPT0_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: APCS_TMRSECURE [GPT0].

The general purpose timer will signal interrupt when its counter value has reached the value stored in the APCS_GPT0_MTCH register.

CPU3_APCS_GPT0_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_GPT0_CNT at which an interrupt will be generated.

0x020BA008 CPU3_APCS_GPT0_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_CNT register contains the current value of the GPT0 timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_GPT0_MTCH register at the same time due to HW re-use. The procedure for writing the APCS_GPT0_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_GPT0_EN.

- Write APCS_GPT0_CNT.
- Write (to set/restore) APCS_GPT0_MTCH if required.
- Enable the timer by setting the EN bit in APCS_GPT0_EN.

CPU3_APCS_GPT0_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer.

0x020BA00C CPU3_APCS_GPT0_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_EN register is used to enable the GPT0 timer.

CPU3_APCS_GPT0_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	CLR_ON_MTCH_EN	When set (1), the timer will clear when it reaches the match value.
0	EN	When set (1), the timer is enabled and counts with frequency ACC_SLP_CLK.

0x020BA010 CPU3_APCS_GPT0_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [GPT0].

The APCS_GPT0_CLR register is a one-shot command register that, when written with any value, resets the timer to a value of 0. This occurs regardless of the state of the APCS_GPT0_EN register.

CPU3_APCS_GPT0_CLR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Data written is not used.

0x020BA014 CPU3_APCS_GPT1_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The GPT timer will signal interrupt when its counter value has reached the value stored in the APCS_GPT1_MTCH register.

CPU3_APCS_GPT1_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_GPT1_CNT at which an interrupt will be generated.

0x020BA018 CPU3_APCS_GPT1_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_CNT register contains the current value of the GPT1 timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_GPT1_MTCH register at the same time. The procedure for writing the APCS_GPT1_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_GPT1_EN.
- Write APCS_GPT1_CNT.
- Write (to set/restore) APCS_GPT1_MTCH if required.
- Enable the timer by setting the EN bit in APCS_GPT1_EN.

CPU3_APCS_GPT1_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer

0x020BA01C CPU3_APCS_GPT1_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_EN register is used to enable the GPT1 timer.

CPU3_APCS_GPT1_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	CLR_ON_MTCH_EN	When set (1), timer will clear when it reaches the match value.
0	EN	When set (1), timer is enabled and counts with frequency sleep clock.

0x020BA020 CPU3_APCS_GPT1_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [GPT1].

The APCS_GPT1_CLR register is a one-shot command register that, when written with any value, resets the GPT1 timer to a value of 0. This occurs regardless of the state of the APCS_GPT1_EN register.

CPU3_APCS_GPT1_CLR

Bits	Name	Description
31:0	RESERVED_BITS_31_0	Data written is not used.

0x020BA024 CPU3_APCS_DGT_MTCH

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The DBG timer will signal interrupt when its counter value has reached the value stored in the APCS_DGT_MTCH register.

CPU3_APCS_DGT_MTCH

Bits	Name	Description
31:0	MTCH	The value of APCS_DGT_CNT at which an interrupt will be generated.

0x020BA028 CPU3_APCS_DGT_CNT

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CNT register contains the current value of the DGT timer. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the APCS_DGT_MTCH register at the same time due to HW re-use. The procedure for writing the APCS_DGT_CNT is as follows:

- Disable the timer by clearing the EN bit in APCS_DGT_EN.
- Write APCS_DGT_CNT.
- Write (to set/restore) APCS_DGT_MTCH if required.
- Enable the timer by setting the EN bit in APCS_DGT_EN.

CPU3_APCS_DGT_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer count

0x020BA02C CPU3_APCS_DGT_EN

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_EN register is used to enable the DGT timer.

CPU3_APCS_DGT_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	

CPU3_APCS_DGT_EN (cont.)

Bits	Name	Description
1	CLR_ON_MTCH_EN	When set (1), the timer will clear when it reaches the match value.
0	EN	When set (1), the timer is enabled and counts with frequency TCXO clock.

0x020BA030 CPU3_APCS_DGT_CLR

Type: Write (Command)
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CLR register is a one-shot command register that, when written with any value, resets the DGT timer to a value of 0. This occurs regardless of the state of the APCS_DGT_EN register.

CPU3_APCS_DGT_CLR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Data written is not used.

0x020BA034 CPU3_APCS_DGT_CLK_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0003

Security Treatment: Controlled by APCS_TMRSECURE [DGT].

The APCS_DGT_CLK_CTL controls the clock divider inside the Debug Timer.

NOTE It is possible for the AHB clock to run at as slow as 5 MHz using settings of the Global Clock Controller. The debug timer's counter can also run at 5 MHz (TCXO divided by 4). However, due to the synchronization circuit using the edge detect, the timer should always run at least 4x slower than the AHB clock. Thus, if the timer's use is required by the system, the divider should be set to divide by 4 and the slowest usable AHB frequency is 20MHz. The timer would run at 5MHz in this case.

CPU3_APCS_DGT_CLK_CTL

Bits	Name	Description
31:2	RESERVED_BITS_31_2	

CPU3_APCS_DGT_CLK_CTL (cont.)

Bits	Name	Description
1:0	DIV	0x3: 4 0x2: 3 0x1: 2 0x0: 1

0x020BA038 CPU3_APCS_WDT0_RST

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_RST register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset the watch dog counter. This command register also disables the watchdog freeze

CPU3_APCS_WDT0_RST

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	STB	This bit generates the WDT0_STB during the non-sleep mode. A pulse is generated on WDT0_STB when this bit is written with a ’1

0x020BA03C CPU3_APCS_WDT0_FRZ

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_FRZ register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the APCS_WDT0_RST register.

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

CPU3_APCS_WDT0_FRZ

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved

CPU3_APCS_WDT0_FRZ (cont.)

Bits	Name	Description
0	FRZ	This bit is used to freeze the watchdog timer at time 0. To enable the watchdog timer auto-kicker, write a '1'.

0x020BA040 CPU3_APCS_WDT0_EN

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_EN register controls when the watch dog timer is enabled.

CPU3_APCS_WDT0_EN

Bits	Name	Description
31:2	RESERVED_BITS_31_2	Reserved
1	INT_EN	Any write to this register: 0x1: yes (any unmasked IRQ or FIQ will enable the WDT0 timer.) 0x0: no
0	EN	Any write to this register: 0x1: yes (the watch dog timer is enabled) 0x0: no

0x020BA044 CPU3_APCS_WDT0_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_STS register is the watchdog status register.

CPU3_APCS_WDT0_STS

Bits	Name	Description
31:3	WDT_CNT	Counter value [28:0] of the watch dog counter. **NOTE** The sleep counter value is sampled using the AHB clk. Multiple reads are required to determine the value (assuming AHB clk is much faster than sleep clock).
2	WDT_RST_STS	Show the status of watchdog0 counter reset.

CPU3_APCS_WDT0_STS (cont.)

Bits	Name	Description
1	AUTOKICK	This bit indicates whether the auto-kicker is on. 0x1: On 0x0: Off
0	RST_STS	0x1: wdt (the last system reset was due to WDT0) 0x0: reset (the last system reset was not due to WDT0.)

0x020BA048 CPU3_APCS_WDT0_INT_WIDTH

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_INT_WIDTH register defines the width of the WDT0 biteExpired pulse in the number of sleep_clk pulses. The default value is 0x0C7C, but this reset value is not readable through the AHB interface.

CPU3_APCS_WDT0_INT_WIDTH

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter value on which to de-assert the WDI bite pulse.

0x020BA04C CPU3_APCS_WDT0_BARK_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (’bark’) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, but this reset value is not readable through the AHB interface. Note that this value is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (’bark’) interrupt.

CPU3_APCS_WDT0_BARK_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter value on which to trigger the bark interrupt.

0x020BA050 CPU3_APCS_WDT0_TST_LD_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TST_LD_STS register indicates when the watchdog test load is synchronizing to the SLP_CLK.

CPU3_APCS_WDT0_TST_LD_STS

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SYNC_STS	When set (1) wdog test load is synchronizing to SLP_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x020BA054 CPU3_APCS_WDT0_TST_LD

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TEST_LD register loads the WDT0_TST register value into the watchdog counter.

CPU3_APCS_WDT0_TST_LD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	LD	Set on this bit to load the value into the WDT0_TST register into the WDT0 counter.

0x020BA058 CPU3_APCS_WDT0_TST

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_TST register indicates that the watchdog test is synchronizing to the SLP_CLK and contains the watch dog counter test load value.

CPU3_APCS_WDT0_TST

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 counter test load value [28:0].

0x020BA05C CPU3_APCS_WDT0_BITE_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_31F3

Security Treatment: .Controlled by APCS_TMRSECURE [WDT0].

The APCS_WDT0_BITE_TIME register determines the counter value at which WDT0 asserts the biteExpired signal.

CPU3_APCS_WDT0_BITE_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog bite time is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT0 bite expiration time [28:0].

0x020BA060 CPU3_APCS_WDT1_RST

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_RST register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset the watch dog counter. This command register also disables the watchdog freeze

CPU3_APCS_WDT1_RST

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	STB	This bit generates the WDT1_STB during the non-sleep mode. A pulse is generated on WDT1_STB when this bit is written with a ’1

0x020BA064 CPU3_APCS_WDT1_FRZ

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_FRZ register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the APCS_WDT1_RST register.

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

CPU3_APCS_WDT1_FRZ

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	FRZ	This bit is used to freeze the watchdog timer at time 0. To enable the watchdog timer auto-kicker, write a ’1’.

0x020BA068 CPU3_APCS_WDT1_EN

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_EN register controls when the watchdog timer is enabled.

CPU3_APCS_WDT1_EN

Bits	Name	Description
31:2	RESERVED_BITS_31_2	Reserved
1	INT_EN	Any write to this register: 0x1: yes (any unmasked IRQ or FIQ will enable the WDT0 timer.) 0x0: no
0	EN	Any write to this register: 0x1: yes (the watch dog timer is enabled) 0x0: no

0x020BA06C CPU3_APCS_WDT1_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_STS register is the watchdog status register.

CPU3_APCS_WDT1_STS

Bits	Name	Description
31:3	WDT_CNT	Counter value [28:0] of the watch dog counter. **NOTE** The counter value is sampled using the ahb clk. Multiple reads are required to determine the value (assuming ahb clk is much faster than sleep clock).
2	WDT_RST_STS	Show the status of watchdog counter reset.
1	AUTOKICK	This bit indicates whether the auto-kicker is on. 0x1: On 0x0: Off
0	RST_STS	0x1: wdt (the last system reset was due to WDT1) 0x0: reset (the last system reset was not due to WDT1.)

0x020BA070 CPU3_APCS_WDT1_INT_WIDTH

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_INT_WIDTH register defines the width of the WDT1_expired pulse in the number of sleep_clk pulses.The default value is 0x0C7C, but this reset value is not readable through the AHB interface.

CPU3_APCS_WDT1_INT_WIDTH

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter value on which to de-assert the WDI expired pulse.

0x020BA074 CPU3_APCS_WDT1_BARK_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (’bark’) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, but this reset value is not readable through the AHB interface. Note that this value is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (’bark’) interrupt.

CPU3_APCS_WDT1_BARK_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the wdog bark time is synchronizing to the SLP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter value on which to trigger the bark interrupt.

0x020BA078 CPU3_APCS_WDT1_TST_LD_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TST_LD_STS register indicates when the watchdog test load is synchronizing to the SLP_CLK.

CPU3_APCS_WDT1_TST_LD_STS

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SYNC_STS	When set (1) wdog test load is synchronizing to SLP_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x020BA07C CPU3_APCS_WDT1_TST_LD

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TEST_LD register loads the WDT1_TST register value into the watchdog counter.

CPU3_APCS_WDT1_TST_LD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	LD	Set on this bit to load the value into the WDT1_TST register into the WDT counter

0x020BA080 CPU3_APCS_WDT1_TST

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: Undefined

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_TST register indicates that the watchdog test is synchronizing to the SLP_CLK and contains the watch dog counter test load value.

CPU3_APCS_WDT1_TST

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 counter test load value [28:0]

0x020BA084 CPU3_APCS_WDT1_BITE_TIME

Type: Read/write
Clock: SYS_AHB_CLK
Reset State: 0x0000_31F3

Security Treatment: .Controlled by APCS_TMRSECURE [WDT1].

The APCS_WDT1_BITE_TIME register determines the counter value at which WDT1 asserts the biteExpired signal.

CPU3_APCS_WDT1_BITE_TIME

Bits	Name	Description
31:30	RESERVED_BITS_31_30	Reserved
29	SYNC_STS	When set (1), the watchdog bite time is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STS bit is clear (0). This bit is read only.
28:0	DATA	The WDT1 bite expiration time [28:0].

0x020BA088 CPU3_APCS_TMR_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_TMRSECURE [WDT0, WDT1, GPT0, GPT1, DGT].

The APCS_TMR_STS can be used to determine the status of each of the SCSS timers in the timer's resident clock domain. Since the timer clock domain may be much slower than the AHB clock, AHB transactions may be delayed in taking effect. This information can be used to qualify other actions or used simply for debug purposes. For example, software can determine when a write to APCS_DGT_CLR has taken effect by examining the DGT_CLR_PEND bit.

Each timer's bits are receive security treatment as specified by the APCS_TMRSECURE register.

CPU3_APCS_TMR_STS

Bits	Name	Description
31	RESERVED_BIT31	
30	WDT1_AUTOKICK	Auto-kicker is on (1) or off (0)
29	WDT1_INT_EN	An unmasked interrupt will enable the timer (1) or not (0)
28	WDT1_EN	Timer is enabled (1) or not (0)
27	RESERVED_BIT27	
26	WDT0_AUTOKICK	Auto-kicker is on (1) or off (0)

CPU3_APCS_TMR_STS (cont.)

Bits	Name	Description
25	WDT0_INT_EN	An unmasked interrupt will enable the timer (1) or not (0)
24	WDT0_EN	Timer is enabled (1) or not (0)
23:20	RESERVED_BIT20_23	
19	GPT1_WR_PEND	Timer has a write pending (1) or not (0)
18	GPT1_CLR_PEND	Timer has a clear pending (1) or not (0)
17	GPT1_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
16	GPT1_EN	Timer is enabled (1) or not (0)
15:12	RESERVED_BITS15_12	
11	GPT0_WR_PEND	Timer has a write pending (1) or not (0)
10	GPT0_CLR_PEND	Timer has a clear pending (1) or not (0)
9	GPT0_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
8	GPT0_EN	Timer is enabled (1) or not (0)
7:4	RESERVED_BITS7_4	
3	DGT_WR_PEND	Timer has a write pending (1) or not (0)
2	DGT_CLR_PEND	Timer has a clear pending (1) or not (0)
1	DGT_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
0	DGT_EN	Timer is enabled (1) or not (0)

11.26 KPSS GLB Registers (0x02090000 EXT_APCS_GLB_BASE)

This section contains the Krait Processor Subsystem (KPSS) GLB registers.

0x02090000 EXT_APCS_GLBSECURE

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0001

Security Treatment: Restricted

The APCS_GLBSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Krait's APROTNS pin. When APROTNS is set to '0' the state of the APCS_GLBSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_GLBSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_GLBSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_GCCSECURE register correspond to.

EXT_APCS_GLBSECURE

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	GLB_CTL	Controls security treatment for the global control registers: APCS_START_ADDR. 0x1: NSEC 0x0: SEC

0x02090004 EXT_APCS_START_ADDR

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: {START_ADDR, 0x0000}

Security Treatment: Controlled by APCS_GLBSECURE[GLB_CTL].

The APCS_START_ADDR register is used to determine the address to boot from. It resets to the value on START_ADDR PARAMETER.Reset by SYS_apcsSYSPor_Ares|SYS_apcsSys_Ares

EXT_APCS_START_ADDR

Bits	Name	Description
31:16	ADDR	Start address for the Krait

EXT_APCS_START_ADDR (cont.)

Bits	Name	Description
15:0	RESERVED_BITS15_0	

11.27 KPSS GCC Registers (0x02091000 EXT_APCS_GCC_BASE)

This section contains the Krait Processor Subsystem (KPSS) GCC registers.

0x02091000 EXT_APCS_GCCSECURE

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0007

Security Treatment: Restricted

The APCS_GCCSECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Krait's APROTNS pin. When APROTNS is set to '0' the state of the APCS_GCCSECURE register is not considered - a secure transaction is always allowed. When APROTNS is set to '1', the APCS_GCCSECURE register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_GCCSECURE register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_GCCSECURE register correspond to.

EXT_APCS_GCCSECURE

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	TST	Controls security treatment for the global test control registers: APCS_ALL_TSTBUS_SEL, APCS_CLK_DIAG, APCS_SPARE, APCS_SPARE_STS 0x1: NSEC 0x0: SEC
1	SLP_CTL	Controls security treatment for the global sleep control registers: APCS_L2_PWR_CTL, APCS_PWR_STS, APCS_DBG_PWR_CTL 0x1: NSEC 0x0: SEC
0	CLK_CTL	Controls security treatment for the global clock control registers: APCS_PWR_CTL_OVERRIDE, APCS_GCLK_STS, APCS_L2_AUX_CLK_SEL 0x1: NSEC 0x0: SEC

0x02091004 EXT_APCS_IPC_SECURITY

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Restricted

The APCS_IPC_SECURITY register is used to enable or disable non-secure bus transactions. The bus security status is signaled by Krait's APROTNS pin. When APROTNS is set to '0' the state of the APCS_IPC_SECURITY register is not considered; a secure transaction is always allowed. When APROTNS is set to '1', the APCS_IPC_SECURITY register's SECURE bit must be '1' for access to be granted. If the SECURE bit is set to '0', the non-secure (APROTNS = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled.

When reading the APCS_IPC_SECURITY register, non-secure agents will always read '0'. Secure agents will see the actual value of the register. The same is true for the registers or bits each bit in the APCS_IPC_SECURITY register correspond to.

EXT_APCS_IPC_SECURITY

Bits	Name	Description
31:0	IPC_SEC	User-defined. (Each bit in this register controls access to the corresponding bit in the APCS_IPC).

0x02091008 EXT_APCS_IPC

Type: Write (command)
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_IPC_SECURITY on a bit-wise basis.

Inter-process communication signals from Krait to other masters.

EXT_APCS_IPC

Bits	Name	Description
31:0	IPC_INT	User-defined. (Each bit can be written and it will cause an IPC interrupt).

0x0209100C EXT_APCS_PWR_CTL_OVERRIDE

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [CLK_CTL].

The APCS_PWR_CTL_OVERRIDE register is used to enable the global APCS clocks. This is used to workaround hardware dynamic clock gating problems.

EXT_APCS_PWR_CTL_OVERRIDE

Bits	Name	Description
31:17	RESERVED_BITS31_17	
16	L2_RET_SLP_DIS	When set, this bit will take L2 array out of retention mode. This bit needs to be set before the vdd_mem voltage is lowered. The L2 data will be lost if vdd_mem is lowered to a voltage level such that the internal array voltage is below the retention voltage.
15:10	RESERVED_BITS15_10	
9:0	CLK_EN	Clock enables for global APCS clocks. This is only to workaround hardware dynamic clock gating problems. [9:7]= SYS_apcsL2Aux_Clk[3:1] [6] = SYS_apccL2Pll_Clk [5] = ATB_apcc_Clk [4] = APB_apccDbg_Clk [3] = SYS_apcsPiSleep_Clk [2] = SYS_apcsRef_Clk [1] = SYS_apcsAhb_Clk [0] = SYS_apcsQsb_Clk 0x1: Always enabled 0x0: dynamically enabled by hardware

0x02091010 EXT_APCS_GCLK_STS

Type: Read
Clock: SYS_AHB_CLK
Reset State: N/A

Security Treatment: Controlled by APCS_GCCSECURE [CLK_CTL].

The APCS_GCLK_STS register is used to monitor the output of the clock gating cells.

EXT_APCS_GCLK_STS

Bits	Name	Description
31:10	RESERVED_BITS31_10	

EXT_APCS_GCLK_STS (cont.)

Bits	Name	Description
9:0	STS	Status for global APCS clocks [9:7]= APCS_sysL2AuxClkOnReq [6] = APCS_sysL2PllClkOnReq [5] = APCS_sysAtbClkOnReq [4] = APCS_sysApbDbgClkOnReq [3] = APCS_sysSleepClkOnReq [2] = APCS_sysRefClkOnReq [1] = APCS_sysAhbClkOnReq [0] = APCS_sysQsbClkOnReq 0x1: toggling, 0x0: halted

0x02091014 EXT_APCS_L2_PWR_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_8100

Security Treatment: Controlled by APCS_GCCSECURE [SLP_CTL].

The APCS_L2_PWR_CTL register controls the L2 Global Distrubuted Head Switch and L2 array head switches.

EXT_APCS_L2_PWR_CTL

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	L2_HS_CNT	Count value for headswitched L2 logic
15	PLL_CLAMP	When set, this bit clamp the output of TDC logic in PLL. This signal must be asserted prior to opening the l2swvd head switch.This bit is ORed with SAW output before passing to the L2 PLL .
14	LVE	When set, this bit select the ACC value for low voltage mode for all Krait L2 RAMs.
13	L2_RET_SLP	When set, this bit will put the L2 array in retention mode resulting in lower cache array leakage.The data in the L2 array is retained.. This is ORed with SAW output before passing to the CPU.
12	SYS_RESET	Setting this bit asserts the SYS_apccSys_Areset_N input to the Krait CPU, causing a warm system reset (all powered non-debug logic will be reset) to the CPU core without resetting subsystem functions such as timers, clock control, etc.
11	RESERVED_BIT11	Previous drive SYS_scQdmapHaltReq (resets to 1)
10	L2_HS_RST	When set, this bit asserts reset to the headswitched L2 logic

EXT_APCS_L2_PWR_CTL (cont.)

Bits	Name	Description
9	L2_HS_EN	When set, this bit closes the switches for the headswitched L2 logic, putting it into an operational state
8	L2_HS_CLAMP	When set, this bit clamps the outputs from the headswitched L2 logic into the unswitched domain This bit is ORed with SAW outputs before passing to the CPU(resets to 1).
7:4	RESERVED_BITS7_4	
3:2	L2_ARRAY_HS3_2	(Reserved if NUM_CPU < 4). Only for QUAD Krait variant (2 MB L2). When set, these bits open the array head switches for 512 KB sections of the L2 cache array, resulting a lower cache array leakage when data does not need to be retained in the array. These bits are ORed with SAW outputs before passing to the CPU
1:0	L2_ARRAY_HS1_0	When set, these bits open the array head switches for 512 KB sections of the L2 cache array, resulting a lower cache array leakage when data does not need to be retained in the array. These bits are ORed with SAW outputs before passing to the CPU

0x02091018 EXT_APCS_PWR_STS

Type: Read Only
Clock: SYS_AHB_CLK
Reset State: NA

Security Treatment: Controlled by APCS_GCCSECURE [SLP_CTL].

The APCS_PWR_STS register contains the status bits necessary to support an MP with foot switched L2.

EXT_APCS_PWR_STS

Bits	Name	Description
31:15	RESERVED_BITS31_15	
14:13	L2_HS_STS3_2	(Reserved if NUM_CPU < 4). Only for QUAD Krait variant (2MB L2). This bit reflects the status of APCS_apccSwCtlL2ArrayCollapse[3:2] signal
12	SPM_SLP_STATE	This bit reflects the status of L2 SPM Sleep state.
11	SAW_SLP_ACK	This bit reflects the status of APCS_apccL2SleepAck signal
10	DBG_RST_STS	This bit reflects the status of APCS_apccDbg_Areset_N signal
9	L2_HS_RST_STS	This bit reflects the status of APCS_apccL2swvd_Areset_N signal
8	L2_CLMP_STS	This bit reflects the status of APCS_apccClampL2swvd signal

EXT_APCS_PWR_STS (cont.)

Bits	Name	Description
7	L2_RET_SLP_STS	This bit reflects the status of APCS_apccSwCtlL2RetentionSleep signal
6:5	L2_HS_STS1_0	This bit reflects the status of APCS_apccSwCtlL2ArrayCollapse[1:0] signal
4	DBG_PWRUP_REQ	This bit reflects the status of SYS_apcsDbgPwrUpReq
3	L2_FS_STS	Status for foot-switched L2 logic
2	RESERVED_BITS2	Legacy SC_sysQdmapHaltAck signal
1	L2_CLK_IDLE	This bit reflects the status of the APCC_sysL2ClkIdle signal
0	L2_SLV_IDLE	This bit reflects the status of the APCC_qsbSlvIdle signal

0x0209101C EXT_APCS_CLK_DIAG

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [TST].

The APCS_CLK_DIAG register selects the test clock to be output from the APCS to the chip's clock controller. It also controls the functional inputs to the Boundary Scan block.

NOTE The Krait core Leaf clock is always sent to the chip's clock controller as the first test clock. Under proper configuration of the chip's clock controller and the GPIO, this clock can be observed at either the EXT_CLK or through the clock debug test bus.

EXT_APCS_CLK_DIAG

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	FAST_CLK_EN	Enable the Krait Diagnostic clock from the leaf of the clock tree.
6	FAST_CLK_INV	Invert the Krait Diagnostic clock output.
5:3	FAST_CLK_SEL	Selects the Krait HS Leaf clock to output for test mode. 0x0: APC0_sysLeaf_Clk 0x1: APC1_sysLeaf_Clk 0x2: APCC_sysL2Leaf_Clk 0x3: SYS_apcsQsb_Clk 0x4: APC2_sysLeaf_Clk (Quad Krait Variant only) 0x5: APC3_sysLeaf_Clk (Quad Krait Variant only) 0x6: Reserved_1 0x7: Reserved_2

EXT_APCS_CLK_DIAG (cont.)

Bits	Name	Description
2:0	SLOW_CLK_SEL	Selects the APCS slow clock to output for test mode. 0x0: None (No clock selected, tied low.) 0x1: SYS_apcsAhb_Clk 0x2: SYS_apcsRef_Clk 0x3: SYS_apcsPiSleep_Clk 0x4: APB_apccDbg_Clk 0x5: ATB_apcc_Clk 0x6: Reserved_1 0x7: Reserved_2

0x02091020 EXT_APCS_ALL_TSTBUS_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [TST].

The APCS_ALL_TSTBUS_SEL register selects which module's test bus output will be sent out of the subsystem.

EXT_APCS_ALL_TSTBUS_SEL

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	EN	Set to 1 to cause APCS to drive the test bus outputs. 0x1: enabled 0x0: disabled
3:0	SEL	For each category, see appropriate selections for control of the output. 0x6: CONSTANT 0x5: L2 GDHS (SAW2.) 0x4: GLB (global testbus) 0x3: APC3 (Reserved if NUM_CPU < 4.) 0x2: APC2 (Reserved if NUM_CPU < 3.) 0x1: APC1 (Reserved if NUM_CPU < 2) 0x0: APC0

0x02091024 EXT_APCS_DBG_PWR_CTL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [SLP_CTL].

The APCS_DBG_PWR_CTL register is used for debugger communication. The REQ bit is used to enable a signal to the RPM to assert a power up sequence when the APCS's interrupt controller receives any enabled interrupt. The clocks need not be running for this signal to propagate.

EXT_APCS_DBG_PWR_CTL

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	REQ	Setting this bit asserts APCS_dbgPwrUpInt. Note that this signal can also be set by hardware.

0x02091028 EXT_APCS_L2_AUX_CLK_SEL

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [CLK_CTL]

The APCS_L2_AUX_CLK_SEL register controls the gfmux which selects the AUX clock source for the Krait MP's L2 clock. An additional selection set is provided to determine the clock source for the Krait core (4-1 GFMUX) in the Krait Hard Macro. The QSB clock is the raw source clk at reset.

EXT_APCS_L2_AUX_CLK_SEL

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	AUX_SRC	Krait AUX clock select: 0x3: SYS_apcsL2Aux_Clk_1 0x2: SYS_apcsL2Aux_Clk_2 0x1: SYS_apcsL2Aux_Clk_3 0x0: SYS_apcsRef_Clk

0x0209102C EXT_APCS_SPARE

Type: Read/Write
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [TST].

The APCS_SPARE register is used for ECO. The output of this register is controlled by BSL.

EXT_APCS_SPARE

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BITS	SPARE BITS for ECO

0x02091030 EXT_APCS_SPARE_STS

Type: Read Only
Clock: SYS_AHB_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by APCS_GCCSECURE [TST].

The output of the APCS_SPARE BSL register.

EXT_APCS_SPARE_STS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BITS	SPARE BITS for ECO

0x02091FD0 EXT_APCS_VERSION

Type: Read Only
Clock: SYS_AHB_CLK
Reset State: 0x1001_0000
Security Treatment: Controlled by APCS_GCCSECURE [CLK_CTL].

This read only register reports the hardware version information for the KPSS core.

EXT_APCS_VERSION

Bits	Name	Description
31:28	MAJOR	Indicate different interface version. Major version changes are not backward compatible
15:0	MINOR	Indicates expanded functionality. Minor versions add functionality while being backward compatible
15:0	STEP	Indicates a change in the hardware which is not intended to impact software

11.28 KPSS L2 SAW2 Registers (0x02092000 EXT_APCS_L2_GDHS_BASE)

This section contains the Krait Processor Subsystem (KPSS) L2 SAW2 registers.

The SAW2 (SPM and AVS. Wrapper2) design is an AHB slave that contains both SPM and AVS. CSRs.

0x02092000 EXT_APCS_L2_SAW2_SECURE

Type: Read/write
Clock: SYS_REF_CLK
Reset State: {3{CFGNSINIT}}

Security Treatment: Restricted

The SAW2_SECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by ahb_saw_hprotns pin. When ahb_saw_hprotns is set to ’0’ the state of the SAW2_SECURE register is not considered - a secure transaction is always allowed. When ahb_saw_hprotns is set to ’1’, the SAW2_SECURE register security treatment bit of that register must be ’1’ for access to be granted. If the security treatment bit of the register is set to ’0’, the non-secure (ahb_saw_hprotns = ’1’) transactions are denied. When access is denied, a write is ignored, and a read will return ’0’. No error is signaled.

When reading the SAW2_SECURE register, non-secure agents will always read ’0’. Secure agents will see the actual value of the register. The reset value is controlled by CFGNSINIT input pin.

EXT_APCS_L2_SAW2_SECURE

Bits	Name	Description
31:3	RESERVED	
2	SAW_CTL	Controls security treatment for SAW2 registers: SAW2_ID, SAW2_CFG, SAW2_STS_0, SAW2_STS_1, SAW2_RST 0x1: NSEC 0x0: SEC
1	PWR_CTL	Controls security treatment for SPM registers: SAW2_SPM_CTL, SAW2_SPM_PMIC_DLY, SAW2_SPM_PMIC_DATA_0, SAW2_SPM_PMIC_DATA_1, SAW2_SPM_SLP_SEQ_ENTRY_n, SAW2_SPM_DLY 0x1: NSEC 0x0: SEC
0	VLT_CTL	Controls security treatment for the AVS. registers: SAW2_AVS_CTL, SAW2_VLVL, SAW2_AVS_HYSTERESIS 0x1: NSEC 0x0: SEC

0x02092004 EXT_APCS_L2_SAW2_ID

Type: Read
Clock: SYS_REF_CLK
Reset State: Undefined

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register reports the revision and parameter information for the SAW2 core.

EXT_APCS_L2_SAW2_ID

Bits	Name	Description
31	RESERVED_BITS31	
30:25	NUM_SPM_ENTRY	SAW2 parameter: Indicates number of SAW2_SPM_SLP_SEQ_ENTRY register implemented. Value can range from 1 - 32
24:20	NUM_PWR_CTL	SAW2 parameter: Indicates number of power control implemented. Value can range from 2 - 16
19	RESERVED_BITS19	
18	PMIC_ARB_INTF	SAW2 parameter: Indicates PMIC Arbiter Interface function is implemented
17	AVS_PRESENT	SAW2 parameter: Indicates AVS. function is implemented
16	SPM_PRESENT	SAW2 parameter: Indicates SPM function is implemented
15:12	MAJOR	Major variant
11:0	MINOR	Minor variant

0x02092008 EXT_APCS_L2_SAW2_CFG

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_CFG register is used to configure the common control between AVS. and SPM.system.

EXT_APCS_L2_SAW2_CFG

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12	FRC_REF_CLK_ON	Chicken bit to force saw_sys_ref_clk_on_req ON.
11:8	ADR_IDX	PMIC Arbiter Address Index. Drive the saw_pmic_addr_idx output port.

EXT_APCS_L2_SAW2_CFG (cont.)

Bits	Name	Description
7:6	RESERVED_BITS7_6	
5	PMIC_MODE	PMIC Handshake 0x0: 8K_PMIC (only DONE signal) 0x1: 7K_PMIC (both ACK and DONE signals)
4:0	CLK_DIV	Divider ratio for clock. This is used to generate timer tick for the timer. Timer tick is asserted every (CLK_DIV + 1) sys_ref_clk period. ..... For sys_ref_clk = 20 MHz (53ns) The timer tick range 53 ns to 1.6us. 0x0: Timer Tick every sys_ref_clk 0x1F: Timer Tick every 128 sys_ref_clk.

0x0209200C EXT_APCS_L2_SAW2_STS_0

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

EXT_APCS_L2_SAW2_STS_0

Bits	Name	Description
15	SHTDWN_REQ	This bit reflects the shutdown request from the SPM(spm_rpm_shutdown_req) to RPM.
14	SHTDWN_ACK	This bit reflects the shutdown acknowledgement from the RPM(rpm_spm_shutdown_ack) to SPM.
13	BRNGUP_REQ	This bit reflects the bringup request from the SPM(spm_rpm_bringup_req) to RPM.
12	BRNGUP_ACK	This bit reflects the bringup acknowledgement from the RPM(rpm_spm_bringup_ack) to SPM.
11:10	PMIC_STATE	State of the PMIC FSM: transitions back to IDLE) transitions back to IDLE) 0x0: IDLE (waiting for PMIC transaction from AVS. or SPM) 0x1: ACK (waiting for ACK from PMIC Arb) 0x2: DONE (waiting for DONE form PMIC Arb before) 0x3: DELAY (waiting for delay count termination before)

EXT_APCS_L2_SAW2_STS_0 (cont.)

Bits	Name	Description
9:8	RPM_STATE	State of the RPM FSM: 0x0: RUN (waiting for SPM request) 0x1: STDNACK (waiting for shutdown ACK from RPM) 0x2: WAKEUP (waiting for wakeup interrupt) 0x3: BGUPACK (waiting for bringup ACK from RPM)
7	AVS_STATE	State of the AVS. FSM: indication) 0x0: IDLE (waiting to be enabled or for next UP/DOWN) 0x1: REQ (waiting for PMIC FSM to transition to IDLE)
6:0	SPM_CMD_ADDR	Last SPM command executed.

0x02092010 EXT_APCS_L2_SAW2_STS_1

Type: Read
Clock: SYS_REF_CLK
Reset State: Unknown

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

This read only register provides SW with SAW2 status.

EXT_APCS_L2_SAW2_STS_1

Bits	Name	Description
31	RESERVED1	
30	SW_WR_PEND	This bit reflects the VLVL state of the request from the SAW2_VCTL write is pending.
29	CPU_UP	This bit reflects the VLVL state of the request from the CPU (avs_saw_up) to raise the VLVL.
28	CPU_DN	This bit reflects the VLVL state of the request from the CPU (avs_saw_down) to lower the VLVL.
27	MAX_INT	IRQ status bit, AVS. controller detected that raising the VLVL by AVS_CTL[VLVL_STEP] would result in a value greater than AVS_CTL[MAX_VLVL]. If AVS_CTL[IRQ_MAX_EN] is set, an interrupt is issued. NOTE that SW can set MAX_VLVL lower than current VLVL creating a condition where VLVL is higher than MAX_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MAX.

EXT_APCS_L2_SAW2_STS_1 (cont.)

Bits	Name	Description
26	MIN_INT	IRQ status bit, AVS. controller detected that lowering the VLVL by SAW2_AVS_CTL[VLVL_STEP] would result in a value less than SAW2_AVS_CTL[MIN_VLVL]. If SAW2_AVS_CTL[IRQ_MIN_EN] is set, an interrupt is issued. NOTE that SW can set MIN_VLVL higher than current VLVL creating a condition where VLVL is lower than MIN_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MIN.
25:16	CURR_DLY	VLVL value of the counter used to calculate the time until the next AVS. controller request for a new VLVL.

0x02092014 EXT_APCS_L2_SAW2_VCTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

Though this register is read/writable, it also causes a command pulse to the PMIC FSM. Writing this register results in a transaction to the PMIC with SAW2_VCTL being sent to the PMIC. SAW2 support both 8901 and 8058 regulator.

EXT_APCS_L2_SAW2_VCTL

Bits	Name	Description
31:16	RESERVED_BITS31_16	

0x02092018 EXT_APCS_L2_SAW2_AVS_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_CTL register is used to control the Adaptive Voltage Scaling (AVS) system.

EXT_APCS_L2_SAW2_AVS_CTL

Bits	Name	Description
31	RESERVED	

EXT_APCS_L2_SAW2_AVS_CTL (cont.)

Bits	Name	Description
30	VLVL_WIDTH	Defines the VLVL field of PMIC data. SAW2 at minimum supports 8901 and 8058 regulator. See PMIC document for details. 0x0: 5 bits VLVL (8058 regulator) 0x1: 6 bits VLVL (8901 regulator)
29:28	VLVL_STEP	Controls the step size of each request to PMIC Arbiter. SW may use values from 0 to 3. Note that the value 0 will result in no change - that is if the CPU requests UP or DOWN, the CURR_PVLVL will be sent to the PMIC Arbiter. This may be useful for debug. If an increment or decrement operation would cause the current VLVL to transition above or below the MAX_VLVL or MIN_VLVL, the current VLVL will not be changed. An interrupt will be signaled if IRQ_MAX/MIN_EN is 1
27	EN	AVS. Enable. **NOTE** Setting to 0 does not disable any pending interrupts. **NOTE** AVS. FSM and SPM FSM are mutually exclusive. Only one FSM is active at a time. SW does not have to disable AVS. before going to sleep. 0x0: Disable AVS 0x1: Enable AVS
26	SW_DONE_INT_EN	Set to 1 to turn on AVS. interrupt for when a SW initiated voltage change has completed. Set to 0 to mask it (turn it off). ASSERTION: This interrupt is asserted only after a SW write to SAW2_AVS_VLVL. Specifically, after the AVS. FSM traverses through all its states and transitions back to IDLE, the interrupt line is pulsed. The interrupt controller should be set to edge capture to receive this interrupt. CLEARING: None. This interrupt is a pulse, SW does not need to clear it (aside from requirements of the interrupt controller).
25	MAX_INT_EN	Set to 1 to turn on AVS. interrupt for MAX_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be greater than MAX_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit.
24	MIN_INT_EN	Set to 1 to turn on AVS. interrupt for MIN_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be smaller than MIN_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit
23	RESERVED_23	

EXT_APCS_L2_SAW2_AVS_CTL (cont.)

Bits	Name	Description
22:17	MAX_VLVL	Control maximum value of AVS. controller's VLVL. When current VLVL reaches this value it may not grow any larger. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level higher, an interrupt is issued. This value may be updated at anytime. Setting to a value lower than MIN_VLVL is not supported, and unpredictable results may occur.
16	RESERVED_16	
15:10	MIN_VLVL	Control the minimum value of AVS. controller's VLVL. When the current VLVL reaches this level it may not shrink any smaller. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level lower, an interrupt is issued. This value may be updated at anytime. Setting to a value higher than MAX_VLVL is not supported, and unpredictable results may occur.
9:0	AVS_DELAY	Control the time between AVS. controller's requests to change the VLVL

0x0209201C EXT_APCS_L2_SAW2_AVS_HYSTERESIS

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [VLT_CTL].

The SAW2_AVS_HYSTERESIS register is used to delay the AVS. UP/DN signal to AVS. FSM. This is used to prevent the false PMIC step due to PDN noise.

EXT_APCS_L2_SAW2_AVS_HYSTERESIS

Bits	Name	Description
31:24	RESERVED31_24	
23:16	DN_COUNT	HYSTERESIS DN COUNT. Delays of PMIC DN step operation.
15:8	RESERVED15_8	
7:0	UP_COUNT	HYSTERESIS UP COUNT. Delays of PMIC UP step operation.

0x02092020 EXT_APCS_L2_SAW2_SPM_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_CTL register is used to control the subsystem power management system. This are parameters that controls the operation of SPM FSM.

EXT_APCS_L2_SAW2_SPM_CTL

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	SPM_START_ADR	Start address for the SPM sequence.
3	ISAR	Inhibit Start Address Reset 0x0: End of program reset the SPM_START_ADR to zero. 0x1: Inhibit End of program to reset SPM_START_ADR
2:1	WAKEUP_CONFIG	Wakeup Configuration 0x0: sys_spm_wakeup 0x1: sys_spm_wakeup or !cpu_spm_wait_req 0x2: sys_spm_wakeup or rising edge of sys_spm_dbg_nopwrdwn 0x3: sys_spm_wakeup or !cpu_spm_wait_req or rising edge of sys_spm_dbg_nopwrdwn
0	SPM_EN	SPM En.

0x02092024 EXT_APCS_L2_SAW2_SPM_PMIC_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC delay values after SPM FSM PMIC transaction. SPM wait for the programmed delay before executing the next SPM command.

EXT_APCS_L2_SAW2_SPM_PMIC_DLY

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:24	DATA_1_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
23:19	RESERVED_BITS23_19	
18:16	DATA_1_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
15:11	RESERVED_BITS15_11	

EXT_APCS_L2_SAW2_SPM_PMIC_DLY (cont.)

Bits	Name	Description
10:8	DATA_0_VLVL1_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms
7:3	RESERVED_BITS7_3	
2:0	DATA_0_VLVL0_DLY	PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms

0x02092028 EXT_APCS_L2_SAW2_SPM_PMIC_DATA_0

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

EXT_APCS_L2_SAW2_SPM_PMIC_DATA_0

Bits	Name	Description

0x0209202C EXT_APCS_L2_SAW2_SPM_PMIC_DATA_1

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

EXT_APCS_L2_SAW2_SPM_PMIC_DATA_1

Bits	Name	Description

0x02092030 EXT_APCS_L2_SAW2_RST

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW2_SECURE [SAW_CTL].

The SAW2_RST register is used to reset the SAW logic. This register clear itself. It does not reset any SAW2 CSR's. It reset AVS. and SPM FSM and control registers. This is use to clear any hang condition.

EXT_APCS_L2_SAW2_RST

Bits	Name	Description
31:1	RESERVED31_1	
0	RST	Reset AVS. and SPM FSM and control registers.

0x02092034 EXT_APCS_L2_SAW2_SPM_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

This register provide the delay values for SPM Delay command. SPM wait for the programmed delay before executing the next SPM command.

EXT_APCS_L2_SAW2_SPM_DLY

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:20	DLY3	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
19:10	DLY2	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms
9:0	DLY1	SPM Delay. Controls the time between SPM_SLP_SEQ SPM Delay and the next SPM_SLP_SEQ command. Time range: 52ns to 1.7ms

0x02092080+4*n EXT_APCS_L2_SAW2_SPM_SLP_SEQ_ENTRY_n

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0xXXXX_XXXX

Security Treatment: Controlled by SAW2_SECURE [PWR_CTL].

The SAW2_SPM_SLP_SEQ_ENTRY_n is an array used to sequence through the steps during various power mode. The register width is defined by CLOG_PWR_CTL parameter.

EXT_APCS_L2_SAW2_SPM_SLP_SEQ_ENTRY_n

Bits	Name	Description

11.29 KPSS XPU Registers (0x02093000 EXT_APCS_L2_MPU_BASE)

This section contains the Krait Processor Subsystem (KPSS) XPU registers.

0x02093000+4*n EXT_APCS_MPU_PRTn_RACR, n=[0..31]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU. These registers include a single bit per VMID granting read access

EXT_APCS_MPU_PRTn_RACR

Bits	Name	Description
31:0	RE	Read enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read access to the registers in the associated resource group.

0x02093400+4*n EXT_APCS_MPU_PRTn_WACR, n=[0..31]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

These registers exist only for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU.

EXT_APCS_MPU_PRTn_WACR

Bits	Name	Description
31:0	WE	Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID write access to the registers in the associated resource group.

0x02093800+4*n EXT_APCS_MPU_PRTn_START, n=[0..31]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition Start Address Register. This register contains the start address of the partition. Only the bit numbers indicated by MPU_IDR[MSb] through MPU_IDR[LSb] are valid and physically exist.

EXT_APCS_MPU_PRTn_START

Bits	Name	Description
31:12	ADDR	MPU Partition Start Address
11:0	RESERVED_11_0	Reserved

0x02093C00+4*n EXT_APCS_MPU_PRTn_END, n=[0..31]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition End Address Register. This register contains the start address of the partition.Only the bit numbers indicated by MPU_IDR[MSB] through MPU_IDR[LSB] are valid and physically exist.

EXT_APCS_MPU_PRTn_END

Bits	Name	Description
31:12	ADDR	MPU Partition End Address
11:0	RESERVED_11_0	Reserved

0x02093F80 EXT_APCS_MPU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Configuration Register: This register includes fields governing various MPU behaviors.

EXT_APCS_MPU_CR

Bits	Name	Description
31:2	RESERVED31_2	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set MPU_ESR. MPU_EAR and MPU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set MPU_ESR. MPU_EAR and MPU_ESYNR0 updated with address and syndrome of error.

EXT_APCS_MPU_CR (cont.)

Bits	Name	Description
2	MPUEIE	MPU Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the MPU. Interrupt output is asserted if MPU_CR[MPUEIE] = 1 and any bit is set in MPU_ESR.
1	MPUERE	MPU Error Report Enable. MPUERE = 0 causes the MPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master. MPUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective MPU port. Errors from either port are terminated by the MPU as RAZ/WI Both client and configuration port errors are recorded in MPU_ESR, independent of the value of MPU_CR[MPUERE]
0	MPUE	MPU Enable. Governs whether MPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures MPU and the MID to VMID mapping tables.

0x02093F84 EXT_APCS_MPU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the MPU, for both the client port and the configuration port. Client port addresses are 32 bits width and configuration port addresses are 12 bits wide (the width of the configuration address port).

EXT_APCS_MPU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x02093F88 EXT_APCS_MPU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the MPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and

leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the MPU's interrupt output (when enabled by MPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the MPU_ESYNRn registers, which are merely the "syndrome" of an error indicated by MPU_ESR.

EXT_APCS_MPU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x02093F8C EXT_APCS_MPU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Restore Register. This register is an aliased address for the MPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

EXT_APCS_MPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x02093F90 EXT_APCS_MPU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

EXT_APCS_MPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x02093F94 EXT_APCS_MPU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

EXT_APCS_MPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved

EXT_APCS_MPU_ESYNR1 (cont.)

Bits	Name	Description
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x02093FF4 EXT_APCS_MPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

MPU Revision Register: This register provides major/minor revision codes for the implementation.

EXT_APCS_MPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x02093FF8 EXT_APCS_MPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x1F0C2C1F

MPU ID Register: Read-only register that defines various configuration attributes of the MPU instance.

EXT_APCS_MPU_IDR

Bits	Name	Description
31:29	RESERVED31_29	Reserved
28:24	MSB	Indicates most significant address bit number used in START/END address comparisons.
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used in START/END address comparisons.
15:14	RESERVED15_12	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only MPU_PRTn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate MPU_PRTn_RACR and MPU_PRTn_WACR registers govern read vs. write access. For single VMID, MPU_PRTn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. MPU_PRTn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMD type access control. MPU_PRTn_xACR registers include separate bit per VMID (32 bits) for governing access.
9	RESERVED9	Reserved
8:0	NPRT	Number of partitions. Indicates the number of partitions (minus 1) supported by the MPU. Values range from 0-223 (1-224 partitions)

0x02093FFC EXT_APCS_MPU_MPU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

MPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the MPU (including the MPU_MPU_ACR itself).

EXT_APCS_MPU_MPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the MPU's 4KB address region (including the MPU_MPU_ACR itself). For single VMID type MPUs (MPU_IDR[MV] = 0) the MPU_MPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

12 LP Audio Subsystem Registers

12.1 Overview

Table 12-1 LP_Audio_Sub_System Bases

Base Name	Parent	Address
LCC_PLL0_MODE	LPASS_CSR_BASE	0x28000000
LPASS_M2VMT_M2VMRn	LPASS_M2VMT_BASE	0x28002000
Q6SS_M2VMT_M2VMRn	LPASS_M2VMT_Q6SS_BASE	0x28003000
LPASS_AHBTM_CFG	LPASS_AHBTM_BASE	0x2800A000
LPASS_SB_COMP_CFG	LPASS_SLIMBUS_BASE	0x28080000
LPASS_BAM_CTRL	LPASS_BAM_LITE_BASE	0x28084000
LPAIF_PCM_CTL	LPA_IF_BASE	0x28100000
MIDI_CORE_CONTROL	MIDI_BASE	0x28200000
LPASS_QDSP6SS_RST_EVB	LPASS_QDSP6SS_PUB_BASE	0x28800000
LPASS_QDSP6SS_RGPT_MATCH_VAL	LPASS_QDSP6SS_CSR_BASE	0x28880000
LPASS_QDSP6SS_L2VIC_INT_ENABLEn	LPASS_QDSP6SS_L2VIC_BASE	0x28890000
LPASS_SAW_SECURE	LPASS_QDSP6SS_SAW_BASE	0x288B0000

12.2 LPA SS Registers (0x28000000 LPASS_CSR_BASE)

This section contains the Low Power Audio Subsystem (LPASS) Clocks registers.

12.2.1 Clocks

0x28000000 LCC_PLL0_MODE

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to configure the LPASS PLL.

LCC_PLL0_MODE

Bits	Name	Description
31:22	RESERVED_31_22	RESERVED
21	PLL_VOTE_FSM_RESET	Resets PLL voting FSM: 0x0: De-asserts Reset to PLL voting FSM 0x1: Resets PLL voting FSM
20	PLL_VOTE_FSM_ENA	Enables PLL voting FSM: 0x0: Disabled 0x1: Enabled
19:14	PLL_BIAS_COUNT	Sets PLL bias count of PLL voting FSM.
13:8	PLL_LOCK_COUNT	Sets PLL lock time of PLL voting FSM.
7:6	RESERVED_7_6	RESERVED
5:4	REF_XO_SEL	Specify the reference XO to be used 0x0: PXO (24.576MHz) 0x1: MXO (27MHz) 0x2: CXO (19.2MHz)
3	PLLTEST	Put the PLL in normal mode. Put the PLL in test mode. 0x0: NORMAL_MODE 0x1: TEST_MODE
2	RESET_N	Reset the digital logic of the PLL including the MN counters and integer divider. Normal mode. 0x0: RESET 0x1: NORMAL_MODE

LCC_PLL0_MODE (cont.)

Bits	Name	Description
1	BYPASSNL	Bypass the PLL. This causes the input reference clock to be routed directly to the PLL clock output, PLLOUT_*. Normal mode. MN counters and integer divider used. 0x0: BYPASS 0x1: NORMAL_MODE
0	OUTCTRL	Disable the PLL output clock, PLLOUT_*. This saves power in the raw clock tree. Enable the PLL output clock, PLLOUT_*. 0x0: DISABLE_OUTPUT_CLOCKS 0x1: ENABLE_OUTPUT_CLOCKS

0x28000004 LCC_PLL0_L_VAL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000001

The PLL clock output frequency is determined as follows:

- Fractional mode: PLLOUT_*: LPXO * [L + M/N] / (PRE_DIV * POST_DIV)
- Integer mode: PLLOUT_*: LPXO * L / (PRE_DIV * POST_DIV)

This register specifics the L value.

LCC_PLL0_L_VAL

Bits	Name	Description
31:10	RESERVED_31_10	Reserved.
9:0	L_VAL	Specifies the L value used in the PLL's multiplication factor. Used in integer and fractional modes.

0x28000008 LCC_PLL0_M_VAL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

See the register description for LCC_PLL0_L_VAL for more information.

LCC_PLL0_M_VAL

Bits	Name	Description
31:19	RESERVED_31_19	Reserved.
18:0	M_VAL	Specifies the M value used in the PLL's multiplication factor. Used only when the PLL is in fractional mode.

0x2800000C LCC_PLL0_N_VAL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000001

See the register description for LCC_PLL0_L_VAL for more information.

LCC_PLL0_N_VAL

Bits	Name	Description
31:19	RESERVED_31_19	Reserved.
18:0	N_VAL	Specifies the N value used in the PLL's reference multiplication factor. Used only when the PLL is in fractional mode. This value cannot be 0x0 (division by 0).

0x28000010 LCC_PLL0_TEST_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

First section of the field descriptions shows the mapping from 45nm NT wrapper PLL0_TEST register to SR PLL input, PLL_TEST_CTL. Second section describes corresponding PLL_TEST_CTL bit assignment. Some bits of PLL_TEST_CTL come from PLL0_CONFIG, MMCC_PLL2_N_VAL andMMCC_PLL2_M_VAL (CR154463).

LCC_PLL0_TEST_CTL

Bits	Name	Description
31:19	SPARE_31_19	LCC_PLL0_TEST_CTL(31:19): Not Used
18:17	TESTOUT_SEL	LCC_PLL0_TEST_CTL(18:17): Not Used

LCC_PLL0_TEST_CTL (cont.)

Bits	Name	Description
16	INVERT_EN	LCC_PLL0_TEST_CTL(16): PLL_CONFIG_CTL(5) Output clock polarity Use the normal PLL output. Invert the PLL output. 0x0: DISABLE 0x1: ENABLE
15	PLLOUT_LV_TEST_EN	LCC_PLL0_TEST_CTL(15): PLL_CONFIG_CTL(4) PLLOUT_LV_TEST enable 0x0: DISABLE 0x1: ENABLE
14	SPARE_14	LCC_PLL0_TEST_CTL(14): Not used. See MMCC_PLL2_M_VAL CSR PLLOUT_LV_TEST field which maps to PLL_TEST_CTL(14).
13	PLLOUT_LV_BIST_EN	LCC_PLL0_TEST_CTL(13): PLL_CONFIG_CTL(2) PLLOUT_LV_BIST enable 0x0: DISABLE 0x1: ENABLE
12	PLLOUT_LV_AUX_EN	LCC_PLL0_TEST_CTL(12): PLL_CONFIG_CTL(1) PLLOUT_LV_AUX enable 0x0: DISABLE 0x1: ENABLE
11	NT_TEST0_SWITCH_EN	LCC_PLL0_TEST_CTL(11): Not Used
10	NT_TEST1_SWITCH_EN	LCC_PLL0_TEST_CTL(10): PLL_TEST_CTL(8) Charge pump external bias control 0x0: DISABLE 0x1: ENABLE
9	PFD_UP_GATE_EN	LCC_PLL0_TEST_CTL(9:8): PLL_CONFIG_CTL(29:28) PFD force bits PLL0_TEST_CTL(9) = Force PFD up See MMCC_PLL2_N_VAL CSR ICP_TST_EN field for PLL_TEST_CTL(9) control. 0x0: Normal operation 0x1: Force PFD UP -> 1
8	PFD_DN_GATE_EN	LCC_PLL0_TEST_CTL(9:8): PLL_CONFIG_CTL(29:28) PFD force bits PLL0_TEST_CTL(8) = Force PFD down See LCC_PLL0_TEST_CTL CSR NT_TEST1_SWITCH_EN field for PLL_TEST_CTL(8) control. 0x0: Normal operation 0x1: Force PFD DN -> 1

LCC_PLL0_TEST_CTL (cont.)

Bits	Name	Description
7	SPARE_7	This is a reserved field for LPASS CSR. See MMCC_PLL2_M_VAL CSR DTEST_SEL field for PLL_TEST_CTL(7) control.
6	SPARE_6	This is a reserved field for LPASS CSR. See MMCC_PLL2_M_VAL CSR BYP_TESTAMP field for PLL_TEST_CTL(6) control.
5	TEST_OP_AMP_IMODE	LCC_PLL0_TEST_CTL(5:4): PLL_TEST_CTL(5:4) ATEST1 signal select
4	FILTER_OP_AMP_EN	LCC_PLL0_TEST_CTL(5:4): PLL_TEST_CTL(5:4) ATEST1 signal select
3	EXT_VOLTAGE_EN	LCC_PLL0_TEST_CTL(3:2): PLL_TEST_CTL(3:2) ATEST0 signal select
2	VCTRL_CONN_EN	LCC_PLL0_TEST_CTL(3:2): PLL_TEST_CTL(3:2) ATEST0 signal select
1	VFS1_CONN_EN	LCC_PLL0_TEST_CTL(1): PLL_TEST_CTL(1) ATEST1 Control 0x0: Disable ATEST1 0x1: Enable ATEST1
0	VFS0_CONN_EN	LCC_PLL0_TEST_CTL(0): PLL_TEST_CTL(0) ATEST0 Control 0x0: Disable ATEST0 0x1: Enable ATEST0

0x28000014 LCC_PLL0_CONFIG

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to configure the LPASS PLL:

- Enable the main output
- Setup integer or fractional mode
- Setup the Post divider ratio
- Setup the Pre-divider ratio
- Select the appropriate VCO depending on the generated frequency

First section of the field descriptions shows the mapping from 45nm NT wrapper PLL0_CONFIG register to SR PLL input, PLL_CONFIG_CTL. Second section describes corresponding PLL_CONFIG_CTL bit assignment. Some bits of PLL_CONFIG_CTL come from PLL0_TEST_CTL, MMCC_PLL2_N_VAL andMMCC_PLL2_M_VAL (CR154463).

LCC_PLL0_CONFIG

Bits	Name	Description
31:24	SPARE_31_24	This is a reserved field for LPASS CSR. See LCC_PLL0_TEST_CTL CSR PFD_UP_GATE_EN field for PLL_CONFIG_CTL(29) control. See LCC_PLL0_TEST_CTL CSR PFD_DN_GATE_EN field for PLL_CONFIG_CTL(28) control. See MMCC_PLL2_M_VAL CSR NMOSC_FREQ_CTL field for PLL_CONFIG_CTL(27:26) control. See MMCC_PLL2_N_VAL CSR PFD_DZSEL field for PLL_CONFIG_CTL(25:24) control.
23	PLLOUT_LV_MAIN_EN	PLL0_CONFIG(23): PLL_CONFIG_CTL(0) PLLOUT_LV_MAIN enable See MMCC_PLL2_M_VAL CSR NMOSC_EN field for PLL_CONFIG_CTL(23) control. 0x0: DISABLE 0x1: ENABLE
22	FRAC_MODE_EN	PLL0_CONFIG(22): PLL_CONFIG_CTL(14) PLL fractional mode control 0x0: DISABLE 0x1: ENABLE
21:20	POST_DIV	PLL0_CONFIG(21:20): PLL_CONFIG_CTL(8:7) PLL Post-divider control See MMCC_PLL2_N_VAL CSR ICP_DIV field for PLL_CONFIG_CTL(21:20) control. 0x0: DIV 1 0x1: DIV 2 0x2: DIV 4 0x3: RESERVED
19	PRE_DIV	PLL0_CONFIG(19): PLL_CONFIG_CTL(6) PLL pre-divider control Disable a DIV 2 pre-division of the input reference clock (PFD frequency: reference frequency). Enable a DIV 2 pre-division of the input reference clock (PFD frequency: reference frequency / 2). See MMCC_PLL2_N_VAL CSR IREG_DIV field for PLL_CONFIG_CTL(19) control. 0x0: DIV1 0x1: DIV2

LCC_PLL0_CONFIG (cont.)

Bits	Name	Description
18	NO_CLK_GATE_EN	Not Used. See MMCC_PLL2_N_VAL CSR IREG_DIV field for PLL_CONFIG_CTL(18) control.
17:16	VCO_SEL	PLL0_CONFIG(17): PLL_CONFIG_CTL(9). VCO select. Ensure the proper VCO is selected based on the frequency output. Low frequency (100 - 500 MHz) High frequency (400 - 1400 MHz) PLL0_CONFIG(16): Not Used. See MMCC_PLL2_N_VAL CSR CUSEL field for PLL_CONFIG_CTL(17:16) control. 0x0: LO_FREQ 0x1: HI_FREQ
15	ADZ_SIZE_SEL	Not Used See MMCC_PLL2_M_VAL CSR REF_MODE field for PLL_CONFIG_CTL(15) control.
14:11	ADZ_LEN_SEL	Not Used See LCC_PLL0_CONFIG CSR FRAC_MODE_EN field for PLL_CONFIG_CTL(14) control. See MMCC_PLL2_N_VAL CSR CFG_LOCKDET field for PLL_CONFIG_CTL(13:12) control. See MMCC_PLL2_N_VAL CSR FORCE_ISEED field for PLL_CONFIG_CTL(11) control.
10:9	ISTARTUP_CTL	Not Used See LCC_PLL0_CONFIG CSR VCO_SEL field for PLL_CONFIG_CTL(9) control.
8:4	ISEED_CTL	Not Used See LCC_PLL0_CONFIG CSR POST_DIV (1:0) field for PLL_CONFIG_CTL(8:7) control. See LCC_PLL0_CONFIG CSR PRE_DIV field for PLL_CONFIG_CTL(6) control. See LCC_PLL0_TEST_CTL CSR INVERT_EN field for PLL_CONFIG_CTL(5) control. See LCC_PLL0_TEST_CTL CSR PLLOUT_LV_TEST_EN field for PLL_CONFIG_CTL(4) control.

LCC_PLL0_CONFIG (cont.)

Bits	Name	Description
3:2	IMIRROR_DIV	Not Used See MMCC_PLL2_M_VAL CSR LVEARLY_EN field for PLL_CONFIG_CTL(3) control. See LCC_PLL0_TEST_CTL CSR PLLOUT_LV_BIST_EN field for PLL_CONFIG_CTL(2) control.
1:0	REF_PATH_DELAY	Not Used See LCC_PLL0_TEST_CTL CSR PLLOUT_LV_AUX_EN field for PLL_CONFIG_CTL(1) control. See LCC_PLL0_CONFIG CSR PLLOUT_LV_MAIN_EN field for PLL_CONFIG_CTL(0) control.

0x28000018 LCC_PLL0_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

Read-only register used to query the status of the PLL.

LCC_PLL0_STATUS

Bits	Name	Description
31:17	RESERVED_31_17	Reserved.
16	PLL_ACTIVE_FLAG	pll_active_flag from PLL voting FSM. It indicates when FSM has enabled the PLL and PLL should be locked.
15:1	DUMMY	Unused, driven to VSS.
0	NO_CLOCK_N	Negated version of the no_clock signal.

0x2800001C LCC_Q6_FUNC

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00002D50

This register is used to configure the Q6 functional clocks and resets.

LCC_Q6_FUNC

Bits	Name	Description
31:14	RESERVED_31_14	Reserved.
13	Q6_JTAG_CRC_EN	This field enables or disables the CRC for the Q6 JTAG clock. 0x0: DISABLE 0x1: ENABLE
12	Q6_JTAG_INV_EN	This field enables or disables inversion of the Q6 JTAG clock at the CXC. Uninverted clock Inverted clock 0x0: DISABLE 0x1: ENABLE
11	Q6_JTAG_CXC_EN	This field enables or disables the Q6 JTAG clock at the CXC. 0x0: DISABLE 0x1: ENABLE
10	Q6_PXO_CRC_EN	This field enables or disables the CRC for the Q6 PXO clock. 0x0: DISABLE 0x1: ENABLE
9	Q6_PXO_INV_EN	This field enables or disables inversion of the Q6 PXO clock at the CXC. Uninverted clock Inverted clock 0x0: DISABLE 0x1: ENABLE
8	Q6_PXO_CXC_EN	This field enables or disables the Q6 PXO clock at the CXC. 0x0: DISABLE 0x1: ENABLE
7	Q6_PXO_SLEEP_EN	This field enables Q6 PXO HW clock halt 0x0: DISABLE 0x1: ENABLE
6	Q6_SLP_CRC_EN	This field enables or disables the CRC for the Q6 sleep clock. 0x0: DISABLE 0x1: ENABLE

LCC_Q6_FUNC (cont.)

Bits	Name	Description
5	Q6_SLP_INV_EN	This field enables or disables inversion of the Q6 sleep clock at the CXC. Uninverted clock Inverted clock 0x0: DISABLE 0x1: ENABLE
4	Q6_SLP_CXC_EN	This field enables or disables the Q6 sleep clock at the CXC. 0x0: DISABLE 0x1: ENABLE
3:2	CORE_FUNC_DIV_SEL	Integer divide for Q6 Core clock which is fed via glit-free mux (GFM4) C port. 0x0: BYPASS (DIV1) 0x1: DIV2 0x2: DIV3 0x3: DIV4
1	CORE_FUNC_SRC_SEL	Select PLL source for Q6 Core integer clock which is fed via glit-free mux (GFM4) C port. 0x0: Primary LPASS PLL 0x1: Secondary PLL (MMPLL1 or GPLL0)
0	Q6_SYS_ARES	Soft reset for Q6 Subsystem and Q6 core. 0x0: NORMAL_MODE 0x1: RESET

0x28000020 LCC_Q6_CORE_FRACDIV_CLK

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000600

This register is used to configure the Q6 functional clocks and resets.

LCC_Q6_CORE_FRACDIV_CLK

Bits	Name	Description
31:20	RESERVED_31_20	Reserved.
19:12	N_VAL	MN Circuit to derive fractional divide clock for Q6 Core feeding D port of GFM4 mux. Specifies the N value for the MN counter. Used only when the MN counter is enabled. Must use software register format NOT(N-M).

LCC_Q6_CORE_FRACDIV_CLK (cont.)

Bits	Name	Description
11	INV_EN	This field enables or disables inversion of the fractional divide Q6 core clock at the CXC. Uninverted clock Inverted clock 0x0: DISABLE 0x1: ENABLE
10	CXC_EN	This field enables or disables the fractional divide Q6 core clock at the CXC. 0x0: DISABLE 0x1: ENABLE
9	MNCNTR_CLK_EN	MN Circuit to derive fractional divide clock for Q6 Core feeding D port of GFM4 mux. Halts the output clock of the MN counter. 0x0: DISABLE 0x1: ENABLE
8	MNCNTR_EN	MN Circuit to derive fractional divide clock for Q6 Core feeding D port of GFM4 mux. This field is used to enable or disable the MN counter. 0x0: DISABLE 0x1: ENABLE
7	MNCNTR_RST	MN Circuit to derive fractional divide clock for Q6 Core feeding D port of GFM4 mux. This field activates the MN counter reset. 0x0: NORMAL_MODE 0x1: RESET
6:5	MNCNTR_MODE	MN Circuit to derive fractional divide clock for Q6 Core feeding D port of GFM4 mux. This field sets the mode of the MN counter. No division. Remove clock cycles to reduce the average frequency. Requires timing closure at the undivided frequency. Uses both edges of the input clock to perform division. Provides better output duty cycles than single edge and swallow. Uses only the rising edge of the input clock to perform division. Better than clock swallowing. 0x0: BYPASS 0x1: SWALLOW 0x2: DUAL_EDGE 0x3: SINGLE_EDGE

LCC_Q6_CORE_FRACDIV_CLK (cont.)

Bits	Name	Description
4:3	PRE_DIV_SEL	MN Circuit to derive fractional divide clock for Q6 Core feeding D port of GFM4 mux. This field sets the pre-division of the input clock to the MN counter. 0x0: BYPASS 0x1: DIV2 0x2: DIV3 0x3: DIV4
2:0	MN_SRC_SEL	MN Circuit to derive fractional divide clock for Q6 Core feeding D port of GFM4 mux. This field sets the clock select of the MN counter. OTHERS: RESERVED 0x0: PXO 0x1: CXO 0x2: LPA_PLL 0x3: SEC_PLL 0x6: CLK_TEST_SE 0x7: PLL_TEST_SE

0x28000024 LCC_Q6_CORE_FRACDIV_CLK_MD

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to configure the Q6 Core fractional divide clock.

LCC_Q6_CORE_FRACDIV_CLK_MD

Bits	Name	Description
31:16	RESERVED_31_16	Reserved.
15:8	M_VAL	Specifies the M value for the MN counter. Used only when the MN counter is enabled.
7:0	NOT_2D_VAL	Specifies the NOT(2*D) value for the MN counter.

0x28000028 LCC_Q6_CORE_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register provides status feedback on the Q6 clocks.

LCC_Q6_CORE_STATUS

Bits	Name	Description
31:3	RESERVED_31_4	Reserved.
3	Q6_SLEEP_CLK_ON	Set if the Q6 sleep clock is on.
2	Q6_JTAG_CLK_ON	Set if the Q6 sub-system JTAG clock is on.
1	Q6_PXO_CLK_ON	Set if the Q6 PXO clock is on.
0	Q6_FRACDIV_CLK_ON	Set if the Q6 Core Fractional divide clock is on.

0x2800002C LCC_MIDI_NS

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x0001aa00

This register is used to configure the MIDI clock.

LCC_MIDI_NS

Bits	Name	Description
31:24	N_VAL	Specifies the N value for the MN counter. Used only when the MN counter is enabled. Must use software register format NOT(N-M).
23:18	RESERVED_23_18	Reserved.
17	ARES	MIDI core asynchronous reset. This resets both the core and its bus interface. 0x0: NORMAL_MODE 0x1: RESET
16	MEM_CORE_EN	Power collapses the MIDI memory core. All data will be lost. 0x0: COLLAPSE 0x1: NORMAL_MODE
15:14	MEM_PERIPH_EN	Power collapse the MIDI memory periphery. Data is retained but is inaccessible until the periphery is powered up. 0x0: COLLAPSE_GRACEFULLY 0x1: COLLAPSE_IMMEDIATELY 0x2: NORMAL_MODE 0x3: RESERVED
13	CRC_EN	This field enables or disables the CRC (right after the GFM) feeding all downstream CXCs. 0x0: DISABLE 0x1: ENABLE

LCC_MIDI_NS (cont.)

Bits	Name	Description
12	INV_EN	This field enables or disables inversion of the MIDI clock at the CXC. Uninverted clock Inverted clock 0x0: DISABLE 0x1: ENABLE
11	CXC_EN	This field enables or disables the MIDI clock at the CXC. 0x0: DISABLE 0x1: ENABLE
10	GFM_SRC_SEL	This field sets the clock select of the downstream glitch free clock mux. This mux is used to switch to LPXO when software wishes to change the MN counter values (which results in glitches in the MN counter output clock). 0x0: MN_COUNTER 0x1: PXO
9	MNCNTR_CLK_EN	Halts the output clock of the MN counter. 0x0: DISABLE 0x1: ENABLE
8	MNCNTR_EN	This field is used to enable or disable the MN counter. 0x0: DISABLE 0x1: ENABLE
7	MNCNTR_RST	This field activates the MN counter reset. 0x0: NORMAL_MODE 0x1: RESET
6:5	MNCNTR_MODE	This field sets the mode of the MN counter. No division. Remove clock cycles to reduce the average frequency. Requires timing closure at the undivided frequency. Uses both edges of the input clock to perform division. Provides better output duty cycles than single edge and swallow. Uses only the rising edge of the input clock to perform division. Better than clock swallowing. 0x0: BYPASS 0x1: SWALLOW 0x2: DUAL_EDGE 0x3: SINGLE_EDGE

LCC_MIDI_NS (cont.)

Bits	Name	Description
4:3	PRE_DIV_SEL	This field sets the pre-division of the input clock to the MN counter. 0x0: BYPASS 0x1: DIV2 0x2: DIV3 0x3: DIV4
2:0	MN_SRC_SEL	This field sets the clock select of the MN counter. OTHERS: RESERVED 0x0: PXO 0x1: CXO 0x2: LPA_PLL 0x3: SEC_PLL 0x6: CLK_TEST_SE 0x7: PLL_TEST_SE

0x28000030 LCC_MIDI_MD

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to configure the MIDI clock.

LCC_MIDI_MD

Bits	Name	Description
31:16	RESERVED_31_16	Reserved.
15:8	M_VAL	Specifies the M value for the MN counter. Used only when the MN counter is enabled.
7:0	NOT_2D_VAL	Specifies the NOT(2*D) value for the MN counter.

0x28000034 LCC_MIDI_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000007

This register provides status feedback on the MIDI core clock.

LCC_MIDI_STATUS

Bits	Name	Description
31:3	RESERVED_31_3	Reserved.
2	MEM_CORE_ON	Set if the MIDI memory core is on.
1	MEM_PERIPH_ON	Set if the MIDI memory periphery is on.
0	CLK_ON	Set if the final MIDI core clock is on.

0x28000038 LCC_AHBIX_NS

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000a00

This register is used to configure the common LPASS clocks.

LCC_AHBIX_NS

Bits	Name	Description
31:24	N_VAL	Specifies the N value for the MN counter. Used only when the MN counter is enabled. Must use software register format NOT(N-M).
23:12	RESERVED_23_12	Reserved.
11	CRC_EN	This field enables or disables the CRC (right after the GFM) feeding all downstream CXCs. 0x0: DISABLE 0x1: ENABLE
10	GFM_SRC_SEL	This field sets the clock select of the downstream glitch free clock mux. This mux is used to switch to LPXO when software wishes to change the MN counter values (which results in glitches in the MN counter output clock). 0x0: PXO 0x1: MN_COUNTER
9	MNCNTR_CLK_EN	Halts the output clock of the MN counter. 0x0: DISABLE 0x1: ENABLE
8	MNCNTR_EN	This field is used to enable or disable the MN counter. 0x0: DISABLE 0x1: ENABLE
7	MNCNTR_RST	This field activates the MN counter reset. 0x0: NORMAL_MODE 0x1: RESET

LCC_AHBIX_NS (cont.)

Bits	Name	Description
6:5	MNCNTR_MODE	This field sets the mode of the MN counter. No division. Remove clock cycles to reduce the average frequency. Requires timing closure at the undivided frequency. Uses both edges of the input clock to perform division. Provides better output duty cycles than single edge and swallow. Uses only the rising edge of the input clock to perform division. Better than clock swallowing. 0x0: BYPASS 0x1: SWALLOW 0x2: DUAL_EDGE 0x3: SINGLE_EDGE
4:3	PRE_DIV_SEL	This field sets the pre-division of the input clock to the MN counter. 0x0: BYPASS 0x1: DIV2 0x2: DIV3 0x3: DIV4
2:0	MN_SRC_SEL	This field sets the clock select of the MN counter. OTHERS: RESERVED 0x0: PXO 0x1: CXO 0x2: LPA_PLL 0x3: SEC_PLL 0x6: CLK_TEST_SE 0x7: PLL_TEST_SE

0x2800003C LCC_AHBIX_MD

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to configure the common LPASS clocks.

LCC_AHBIX_MD

Bits	Name	Description
31:16	RESERVED_31_16	Reserved.

LCC_AHBIX_MD (cont.)

Bits	Name	Description
15:8	M_VAL	Specifies the M value for the MN counter. Used only when the MN counter is enabled.
7:0	NOT_2D_VAL	Specifies the NOT(2*D) value for the MN counter.

0x28000040 LCC_AHBIX_BRANCH_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x53524B2A

This register is used to configure the AHBIX LPASS clock branches.

LCC_AHBIX_BRANCH_CTL

Bits	Name	Description
31	AVT_HCLK_INV_EN	This field enables or disables inversion of the AV timer AHB clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
30	AVT_HCLK_CXC_EN	This field enables or disables the AVTimer clock at the CXC. 0x0: DISABLE 0x1: ENABLE
29	AHB_HCLK_INV_EN	This field enables or disables inversion of the LPASS AHB clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
28	AHB_HCLK_CXC_EN	This field enables or disables the AHB clock at the CXC. 0x0: DISABLE 0x1: ENABLE
27	AIF_ARES	LPA_IF core asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET

LCC_AHBIX_BRANCH_CTL (cont.)

Bits	Name	Description
26	AIF_HCLK_INV_EN	This field enables or disables inversion of the LPA_IF clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
25	AIF_HCLK_CXC_EN	This field enables or disables the LPA_IF clock at the CXC. 0x0: DISABLE 0x1: ENABLE
24	HW_DYNAMIC_CLK_EN	This field enables or disables hardware dynamic clocking for all AHB Clock branches. 0x0: DISABLE 0x1: ENABLE.
23	SECURITY_HCLK_INV_EN	This field enables or disables inversion of the security clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
22	SECURITY_HCLK_CXC_EN	This field enables or disables the security clock at the CXC. 0x0: DISABLE 0x1: ENABLE
21	LPB_SF_FORCE_CLKON	This field forces lpb_sf_clkon signal to one. lpb_sf_clkon controlled by internal logic lpb_sf_clkon is forced to one. 0x0: DISABLE 0x1: ENABLE
20	SF_LPB_CLKON	This field sets the value of sf_lpb_clkon signal. sf_lpb_clkon is zero sf_lpb_clkon is one 0x0: ZERO 0x1: ONE
19	DML_ARES	DMLite core asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET

LCC_AHBIX_BRANCH_CTL (cont.)

Bits	Name	Description
18	DML_HCLK_INV_EN	This field enables or disables inversion of the DML clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
17	DML_HCLK_CXC_EN	This field enables or disables the DML clock at the CXC. 0x0: DISABLE 0x1: ENABLE
16	FAB_LPB_ARES	Asynchronous reset for the FABRIC to LPASS bus interface. 0x0: NORMAL_MODE 0x1: RESET
15	FAB_LPB_HCLK_INV_EN	This field enables or disables inversion of the FABRIC to LPASS bus clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
14	FAB_LPB_HCLK_CXC_EN	This field enables or disables the FABRIC to LPASS bus clock at the CXC. 0x0: DISABLE 0x1: ENABLE
13	LPB_FAB_ARES	Asynchronous reset for the LPASS bus to FABRIC interface. 0x0: NORMAL_MODE 0x1: RESET
12	LPB_FAB_HCLK_INV_EN	This field enables or disables inversion of the LPASS bus to FABRIC clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
11	LPB_FAB_HCLK_CXC_EN	This field enables or disables the LPASS bus to FABRIC clock at the CXC. 0x0: DISABLE 0x1: ENABLE

LCC_AHBIX_BRANCH_CTL (cont.)

Bits	Name	Description
10	LPM_ARES	LPM asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET
9	LPM_MEM_CORE_EN	Power collapses the LPM memory core. All data will be lost. 0x0: COLLAPSE 0x1: NORMAL_MODE
8:7	LPM_MEM_PERIPH_EN	Power collapse the LPM memory periphery. Data is retained but is inaccessible until the periphery is powered up. 0x0: COLLAPSE_GRACEFULLY 0x1: COLLAPSE_IMMEDIATELY 0x2: NORMAL_MODE 0x3: RESERVED
6	LPM_HCLK_INV_EN	This field enables or disables inversion of the LPM clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
5	LPM_HCLK_CXC_EN	This field enables or disables the LPM clock at the CXC. 0x0: DISABLE 0x1: ENABLE
4	MIDI_HCLK_INV_EN	This field enables or disables inversion of the MIDI AHB clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
3	MIDI_HCLK_CXC_EN	This field enables or disables the AHB clock at the CXC. 0x0: DISABLE 0x1: ENABLE
2	Q6SS_HCLK_INV_EN	This field enables or disables inversion of the Q6SS AHB clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE

LCC_AHBIX_BRANCH_CTL (cont.)

Bits	Name	Description
1	Q6SS_HCLK_CXC_EN	This field enables or disables the Q6SS AHB clock at the CXC. 0x0: DISABLE 0x1: ENABLE
0	Q6SS_HCLK_SLEEP_EN	This field enables QDSP6SS HW clock halt. 0x0: DISABLE 0x1: ENABLE

0x28000044 LCC_AHBIX_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000fff

This register provides status feedback on the AHBIX clocks.

LCC_AHBIX_STATUS

Bits	Name	Description
31:12	RESERVED_31_12	Reserved.
11	AVT_HCLK_ON	Set if the final AV timer AHB clock is on.
10	AHB_HCLK_ON	Set if the final LPASS bus AHB clock is on.
9	AIF_HCLK_ON	Set if the final LPA_IF AHB clock is on.
8	SECURITY_HCLK_ON	Set if the final Crypto3 AHB clock is on.
7	DML_HCLK_ON	Set if the final DMLite AHB clock is on.
6	FAB_LPB_HCLK_ON	Set if the final FABRIC to LPASS bus AHB clock is on.
5	LPB_FAB_HCLK_ON	Set if the final LPASS bus to FABRIC AHB clock is on.
4	LPM_MEM_CORE_ON	Set if the LPM memory core is on.
3	LPM_MEM_PERIPH_ON	Set if the LPM memory periphery is on.
2	LPM_HCLK_ON	Set if the final LPM AHB clock is on.
1	MIDI_HCLK_ON	Set if the final MIDI AHB clock is on.
0	Q6SS_HCLK_ON	Set if the final Q6SS AHB clock is on.

0x28000048 LCC_MI2S_NS

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00028200

This register is used to configure the MI2S clocks.

LCC_MI2S_NS

Bits	Name	Description
31:24	N_VAL	Specifies the N value for the MN counter. Used only when the MN counter is enabled. Must use software register format NOT(N-M).
23:20	RESERVED_23_20	Reserved.
19	ARES	MI2S asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET
18	OSR_INV_EN	This field enables or disables inversion of the OSR clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
17	OSR_CXC_EN	This field enables or disables the OSR clock at the CXC. 0x0: DISABLE 0x1: ENABLE
16	BIT_INV_EN	This field enables or disables inversion of the bit-clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
15	BIT_CXC_EN	This field enables or disables the bit-clock at the CXC. 0x0: DISABLE 0x1: ENABLE

LCC_MI2S_NS (cont.)

Bits	Name	Description
14	BIT_SRC_SEL	This field is used to select the bit-clock source between the internally generated clock of the MN counter and an external GPIO clock provided by the codec. In normal mode, the bit-clock is provided by the internal MN counter. In bit-clock slave mode, the bit-clock is provided by the external codec via a GPIO. The external codec uses its own OSR clock and not the one generated by the LCC. Normal mode Bit-clock slave mode 0x0: MASTER 0x1: SLAVE
13:10	BIT_DIV	This field is used to configure further division of the bit-clock relative to the OSR clock. 0x0: BYPASS 0x1: DIV2 0x2: DIV3 0x3: DIV4 0x4: DIV5 0x5: DIV6 0x6: DIV7 0x7: DIV8 0x8: DIV9 0x9: DIV10 0xA: DIV11 0xB: DIV12 0xC: DIV13 0xD: DIV14 0xE: DIV15 0xF: DIV16
9	MNCNTR_CLK_EN	Halts the output clock of the MN counter which is also the CRC. 0x0: DISABLE 0x1: ENABLE
8	MNCNTR_EN	This field is used to enable or disable the MN counter. 0x0: DISABLE 0x1: ENABLE
7	MNCNTR_RST	This field activates the MN counter reset. 0x0: NORMAL_MODE 0x1: RESET

LCC_MI2S_NS (cont.)

Bits	Name	Description
6:5	MNCNTR_MODE	This field sets the mode of the MN counter. No division. Remove clock cycles to reduce the average frequency. Requires timing closure at the undivided frequency. Uses both edges of the input clock to perform division. Provides better output duty cycles than single edge and swallow. Uses only the rising edge of the input clock to perform division. Better than clock swallowing. 0x0: BYPASS 0x1: SWALLOW 0x2: DUAL_EDGE 0x3: SINGLE_EDGE
4:3	PRE_DIV_SEL	This field sets the pre-division of the input clock to the MN counter. 0x0: BYPASS 0x1: DIV2 0x2: DIV3 0x3: DIV4
2:0	MN_SRC_SEL	This field sets the clock select of the MN counter. OTHERS: RESERVED 0x0: PXO 0x1: CXO 0x2: LPA_PLL 0x3: SEC_PLL 0x6: CLK_TEST_SE 0x7: PLL_TEST_SE

0x2800004C LCC_MI2S_MD

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to configure the MI2S clocks.

LCC_MI2S_MD

Bits	Name	Description
31:16	RESERVED_31_16	Reserved.

LCC_MI2S_MD (cont.)

Bits	Name	Description
15:8	M_VAL	Specifies the M value for the MN counter. Used only when the MN counter is enabled.
7:0	NOT_2D_VAL	Specifies the NOT(2*D) value for the MN counter.

0x28000050 LCC_MI2S_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000003

This register provides status feedback on the MI2S clocks.

LCC_MI2S_STATUS

Bits	Name	Description
31:2	RESERVED_31_2	Reserved.
1	OSR_CLK_ON	Set if the final MI2S OSR clock is on.
0	BIT_CLK_ON	Set if the final MI2S bit clock is on.

0x28000054 LCC_PCM_NS

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000a00

This register is used to configure the PCM clock.

LCC_PCM_NS

Bits	Name	Description
31:16	N_VAL	Specifies the N value for the MN counter. Used only when the MN counter is enabled. Must use software register format NOT(N-M).
15:14	RESERVED_15_14	Reserved.
13	ARES	PCM asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET

LCC_PCM_NS (cont.)

Bits	Name	Description
12	INV_EN	This field enables or disables inversion of the PCM clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
11	CXC_EN	This field enables or disables the PCM clock at the CXC. 0x0: DISABLE 0x1: ENABLE
10	SRC_SEL	This field is used to select the PCM clock source between the internally generated clock of the MN counter and an external GPIO clock provided by the codec. In normal mode, the PCM clock is provided by the internal MN counter. In slave mode, the PCM clock is provided by the external codec via a GPIO. Normal mode Slave mode 0x0: MASTER 0x1: SLAVE
9	MNCNTR_CLK_EN	Halts the output clock of the MN counter which is also the CRC. 0x0: DISABLE 0x1: ENABLE
8	MNCNTR_EN	This field is used to enable or disable the MN counter. 0x0: DISABLE 0x1: ENABLE
7	MNCNTR_RST	This field activates the MN counter reset. 0x0: NORMAL_MODE 0x1: RESET

LCC_PCM_NS (cont.)

Bits	Name	Description
6:5	MNCNTR_MODE	This field sets the mode of the MN counter. No division. Remove clock cycles to reduce the average frequency. Requires timing closure at the undivided frequency. Uses both edges of the input clock to perform division. Provides better output duty cycles than single edge and swallow. Uses only the rising edge of the input clock to perform division. Better than clock swallowing. 0x0: BYPASS 0x1: SWALLOW 0x2: DUAL_EDGE 0x3: SINGLE_EDGE
4:3	PRE_DIV_SEL	This field sets the pre-division of the input clock to the MN counter. 0x0: BYPASS 0x1: DIV2 0x2: DIV3 0x3: DIV4
2:0	MN_SRC_SEL	This field sets the clock select of the MN counter. OTHERS: RESERVED 0x0: PXO 0x1: CXO 0x2: LPA_PLL 0x3: SEC_PLL 0x6: CLK_TEST_SE 0x7: PLL_TEST_SE

0x28000058 LCC_PCM_MD

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to configure the PCM clock.

LCC_PCM_MD

Bits	Name	Description
31:16	M_VAL	Specifies the M value for the MN counter. Used only when the MN counter is enabled.

LCC_PCM_MD (cont.)

Bits	Name	Description
15:0	NOT_2D_VAL	Specifies the NOT(2*D) value for the MN counter.

0x2800005C LCC_PCM_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000001

This register provides status feedback on the PCM clock.

LCC_PCM_STATUS

Bits	Name	Description
31:1	RESERVED_31_1	Reserved.
0	CLK_ON	Set if the final PCM clock is on.

0x28000060 LCC_CODEC_I2S_MIC_NS

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x002C0200

This register is used to configure the codec I2S microphone clocks.

LCC_CODEC_I2S_MIC_NS

Bits	Name	Description
31:24	N_VAL	Specifies the N value for the MN counter. Used only when the MN counter is enabled. Must use software register format NOT(N-M).
23	ARES	Codec I2S microphone asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET
22	OSR_INV_EN	This field enables or disables inversion of the OSR clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE

LCC_CODEC_I2S_MIC_NS (cont.)

Bits	Name	Description
21	OSR_CXC_EN	This field enables or disables the OSR clock at the CXC. 0x0: DISABLE 0x1: ENABLE
20	BIT_INV_EN	This field enables or disables inversion of the bit-clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
19	BIT_CXC_EN	This field enables or disables the bit-clock at the CXC. 0x0: DISABLE 0x1: ENABLE
18	BIT_SRC_SEL	This field is used to select the bit-clock source between the internally generated clock of the MN counter and an external GPIO clock provided by the codec. In normal mode, the bit-clock is provided by the internal MN counter. In bit-clock slave mode, the bit-clock is provided by the external codec via a GPIO. The external codec uses its own OSR clock and not the one generated by the LCC. **NOTE** After reset codec MIC clock is defaulted to slave mode. Normal mode Bit-clock slave mode 0x0: MASTER 0x1: SLAVE
17:10	BIT_DIV	This field is used to configure further division of the bit-clock relative to the OSR clock. 0x0: DIV1 0xFF: DIV256
9	MNCNTR_CLK_EN	Halts the output clock of the MN counter which is also the CRC. 0x0: DISABLE 0x1: ENABLE
8	MNCNTR_EN	This field is used to enable or disable the MN counter. 0x0: DISABLE 0x1: ENABLE
7	MNCNTR_RST	This field activates the MN counter reset. 0x0: NORMAL_MODE 0x1: RESET

LCC_CODEC_I2S_MIC_NS (cont.)

Bits	Name	Description
6:5	MNCNTR_MODE	This field sets the mode of the MN counter. No division. Remove clock cycles to reduce the average frequency. Requires timing closure at the undivided frequency. Uses both edges of the input clock to perform division. Provides better output duty cycles than single edge and swallow. Uses only the rising edge of the input clock to perform division. Better than clock swallowing. 0x0: BYPASS 0x1: SWALLOW 0x2: DUAL_EDGE 0x3: SINGLE_EDGE
4:3	PRE_DIV_SEL	This field sets the pre-division of the input clock to the MN counter. 0x0: DIV1 0x1: DIV2 0x2: DIV3 0x3: DIV4
2:0	MN_SRC_SEL	This field sets the clock select of the MN counter. OTHERS: RESERVED 0x0: PXO 0x1: CXO 0x2: LPA_PLL 0x3: SEC_PLL 0x6: CLK_TEST_SE 0x7: PLL_TEST_SE

0x28000064 LCC_CODEC_I2S_MIC_MD

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to configure the codec I2S microphone clocks.

LCC_CODEC_I2S_MIC_MD

Bits	Name	Description
31:16	RESERVED_31_16	Reserved.

LCC_CODEC_I2S_MIC_MD (cont.)

Bits	Name	Description
15:8	M_VAL	Specifies the M value for the MN counter. Used only when the MN counter is enabled.
7:0	NOT_2D_VAL	Specifies the NOT(2*D) value for the MN counter.

0x28000068 LCC_CODEC_I2S_MIC_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000003

This register provides status feedback on the codec I2S microphone clocks.

LCC_CODEC_I2S_MIC_STATUS

Bits	Name	Description
31:2	RESERVED_31_2	Reserved.
1	OSR_CLK_ON	Set if the final codec I2S microphone OSR clock is on.
0	BIT_CLK_ON	Set if the final codec I2S microphone bit clock is on.

0x2800006C LCC_CODEC_I2S_SPKR_NS

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x002C0200

This register is used to configure the codec I2S speaker clocks.

LCC_CODEC_I2S_SPKR_NS

Bits	Name	Description
31:24	N_VAL	Specifies the N value for the MN counter. Used only when the MN counter is enabled. Must use software register format NOT(N-M).
23	ARES	Codec I2S speaker asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET

LCC_CODEC_I2S_SPKR_NS (cont.)

Bits	Name	Description
22	OSR_INV_EN	This field enables or disables inversion of the OSR clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
21	OSR_CXC_EN	This field enables or disables the OSR clock at the CXC. 0x0: DISABLE 0x1: ENABLE
20	BIT_INV_EN	This field enables or disables inversion of the bit-clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
19	BIT_CXC_EN	This field enables or disables the bit-clock at the CXC. 0x0: DISABLE 0x1: ENABLE
18	BIT_SRC_SEL	This field is used to select the bit-clock source between the internally generated clock of the MN counter and an external GPIO clock provided by the codec. In normal mode, the bit-clock is provided by the internal MN counter. In bit-clock slave mode, the bit-clock is provided by the external codec via a GPIO. The external codec uses its own OSR clock and not the one generated by the LCC. **NOTE** After reset codec SPKR clock is defaulted to slave mode. Normal mode Bit-clock slave mode 0x0: MASTER 0x1: SLAVE
17:10	BIT_DIV	This field is used to configure further division of the bit-clock relative to the OSR clock. 0x0: DIV1 0xFF: DIV256
9	MNCNTR_CLK_EN	Halts the output clock of the MN counter which is also the CRC. 0x0: DISABLE 0x1: ENABLE

LCC_CODEC_I2S_SPKR_NS (cont.)

Bits	Name	Description
8	MNCNTR_EN	This field is used to enable or disable the MN counter. 0x0: DISABLE 0x1: ENABLE
7	MNCNTR_RST	This field activates the MN counter reset. 0x0: NORMAL_MODE 0x1: RESET
6:5	MNCNTR_MODE	This field sets the mode of the MN counter. No division. Remove clock cycles to reduce the average frequency. Requires timing closure at the undivided frequency. Uses both edges of the input clock to perform division. Provides better output duty cycles than single edge and swallow. Uses only the rising edge of the input clock to perform division. Better than clock swallowing. 0x0: BYPASS 0x1: SWALLOW 0x2: DUAL_EDGE 0x3: SINGLE_EDGE
4:3	PRE_DIV_SEL	This field sets the pre-division of the input clock to the MN counter. 0x0: DIV1 0x1: DIV2 0x2: DIV3 0x3: DIV4
2:0	MN_SRC_SEL	This field sets the clock select of the MN counter. OTHERS: RESERVED 0x0: PXO 0x1: CXO 0x2: LPA_PLL 0x3: SEC_PLL 0x6: CLK_TEST_SE 0x7: PLL_TEST_SE

0x28000070 LCC_CODEC_I2S_SPKR_MD

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to configure the codec I2S speaker clocks.

LCC_CODEC_I2S_SPKR_MD

Bits	Name	Description
31:16	RESERVED_31_16	Reserved.
15:8	M_VAL	Specifies the M value for the MN counter. Used only when the MN counter is enabled.
7:0	NOT_2D_VAL	Specifies the NOT(2*D) value for the MN counter.

0x28000074 LCC_CODEC_I2S_SPKR_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000003

This register provides status feedback on the codec I2S speaker clocks.

LCC_CODEC_I2S_SPKR_STATUS

Bits	Name	Description
31:2	RESERVED_31_2	Reserved.
1	OSR_CLK_ON	Set if the final codec I2S speaker OSR clock is on.
0	BIT_CLK_ON	Set if the final codec I2S speaker bit clock is on.

0x28000078 LCC_SPARE_I2S_MIC_NS

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00280200

This register is used to configure the spare I2S microphone clocks.

LCC_SPARE_I2S_MIC_NS

Bits	Name	Description
31:24	N_VAL	Specifies the N value for the MN counter. Used only when the MN counter is enabled. Must use software register format NOT(N-M).
23	ARES	Spare I2S microphone asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET

LCC_SPARE_I2S_MIC_NS (cont.)

Bits	Name	Description
22	OSR_INV_EN	This field enables or disables inversion of the OSR clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
21	OSR_CXC_EN	This field enables or disables the OSR clock at the CXC. 0x0: DISABLE 0x1: ENABLE
20	BIT_INV_EN	This field enables or disables inversion of the bit-clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
19	BIT_CXC_EN	This field enables or disables the bit-clock at the CXC. 0x0: DISABLE 0x1: ENABLE
18	BIT_SRC_SEL	This field is used to select the bit-clock source between the internally generated clock of the MN counter and an external GPIO clock provided by the codec. In normal mode, the bit-clock is provided by the internal MN counter. In bit-clock slave mode, the bit-clock is provided by the external codec via a GPIO. The external codec uses its own OSR clock and not the one generated by the LCC. Normal mode Bit-clock slave mode 0x0: MASTER 0x1: SLAVE
17:10	BIT_DIV	This field is used to configure further division of the bit-clock relative to the OSR clock. 0x0: DIV1 0xFF: DIV256
9	MNCNTR_CLK_EN	Halts the output clock of the MN counter which is also the CRC. 0x0: DISABLE 0x1: ENABLE

LCC_SPARE_I2S_MIC_NS (cont.)

Bits	Name	Description
8	MNCNTR_EN	This field is used to enable or disable the MN counter. 0x0: DISABLE 0x1: ENABLE
7	MNCNTR_RST	This field activates the MN counter reset. 0x0: NORMAL_MODE 0x1: RESET
6:5	MNCNTR_MODE	This field sets the mode of the MN counter. No division. Remove clock cycles to reduce the average frequency. Requires timing closure at the undivided frequency. Uses both edges of the input clock to perform division. Provides better output duty cycles than single edge and swallow. Uses only the rising edge of the input clock to perform division. Better than clock swallowing. 0x0: BYPASS 0x1: SWALLOW 0x2: DUAL_EDGE 0x3: SINGLE_EDGE
4:3	PRE_DIV_SEL	This field sets the pre-division of the input clock to the MN counter. 0x0: DIV1 0x1: DIV2 0x2: DIV3 0x3: DIV4
2:0	MN_SRC_SEL	This field sets the clock select of the MN counter. OTHERS: RESERVED 0x0: PXO 0x1: CXO 0x2: LPA_PLL 0x3: SEC_PLL 0x6: CLK_TEST_SE 0x7: PLL_TEST_SE

0x2800007C LCC_SPARE_I2S_MIC_MD

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to configure the spare I2S microphone clocks.

LCC_SPARE_I2S_MIC_MD

Bits	Name	Description
31:16	RESERVED_31_16	Reserved.
15:8	M_VAL	Specifies the M value for the MN counter. Used only when the MN counter is enabled.
7:0	NOT_2D_VAL	Specifies the NOT(2*D) value for the MN counter.

0x28000080 LCC_SPARE_I2S_MIC_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000003

This register provides status feedback on the spare I2S microphone clocks.

LCC_SPARE_I2S_MIC_STATUS

Bits	Name	Description
31:2	RESERVED_31_2	Reserved.
1	OSR_CLK_ON	Set if the final spare I2S microphone OSR clock is on.
0	BIT_CLK_ON	Set if the final spare I2S microphone bit clock is on.

0x28000084 LCC_SPARE_I2S_SPKR_NS

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00280200

This register is used to configure the spare I2S speaker clocks.

LCC_SPARE_I2S_SPKR_NS

Bits	Name	Description
31:24	N_VAL	Specifies the N value for the MN counter. Used only when the MN counter is enabled. Must use software register format NOT(N-M).
23	ARES	Spare I2S speaker asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET

LCC_SPARE_I2S_SPKR_NS (cont.)

Bits	Name	Description
22	OSR_INV_EN	This field enables or disables inversion of the OSR clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
21	OSR_CXC_EN	This field enables or disables the OSR clock at the CXC. 0x0: DISABLE 0x1: ENABLE
20	BIT_INV_EN	This field enables or disables inversion of the bit-clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
19	BIT_CXC_EN	This field enables or disables the bit-clock at the CXC. 0x0: DISABLE 0x1: ENABLE
18	BIT_SRC_SEL	This field is used to select the bit-clock source between the internally generated clock of the MN counter and an external GPIO clock provided by the codec. In normal mode, the bit-clock is provided by the internal MN counter. In bit-clock slave mode, the bit-clock is provided by the external codec via a GPIO. The external codec uses its own OSR clock and not the one generated by the LCC. Normal mode Bit-clock slave mode 0x0: MASTER 0x1: SLAVE
17:10	BIT_DIV	This field is used to configure further division of the bit-clock relative to the OSR clock. 0x0: DIV1 0xFF: DIV256
9	MNCNTR_CLK_EN	Halts the output clock of the MN counter which is also the CRC. 0x0: DISABLE 0x1: ENABLE

LCC_SPARE_I2S_SPKR_NS (cont.)

Bits	Name	Description
8	MNCNTR_EN	This field is used to enable or disable the MN counter. 0x0: DISABLE 0x1: ENABLE
7	MNCNTR_RST	This field activates the MN counter reset. 0x0: NORMAL_MODE 0x1: RESET
6:5	MNCNTR_MODE	This field sets the mode of the MN counter. No division. Remove clock cycles to reduce the average frequency. Requires timing closure at the undivided frequency. Uses both edges of the input clock to perform division. Provides better output duty cycles than single edge and swallow. Uses only the rising edge of the input clock to perform division. Better than clock swallowing. 0x0: BYPASS 0x1: SWALLOW 0x2: DUAL_EDGE 0x3: SINGLE_EDGE
4:3	PRE_DIV_SEL	This field sets the pre-division of the input clock to the MN counter. 0x0: DIV1 0x1: DIV2 0x2: DIV3 0x3: DIV4
2:0	MN_SRC_SEL	This field sets the clock select of the MN counter. OTHERS: RESERVED 0x0: PXO 0x1: CXO 0x2: LPA_PLL 0x3: SEC_PLL 0x6: CLK_TEST_SE 0x7: PLL_TEST_SE

0x28000088 LCC_SPARE_I2S_SPKR_MD

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to configure the spare I2S speaker clocks.

LCC_SPARE_I2S_SPKR_MD

Bits	Name	Description
31:16	RESERVED_31_16	Reserved.
15:8	M_VAL	Specifies the M value for the MN counter. Used only when the MN counter is enabled.
7:0	NOT_2D_VAL	Specifies the NOT(2*D) value for the MN counter.

0x2800008C LCC_SPARE_I2S_SPKR_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000003

This register provides status feedback on the spare I2S speaker clocks.

LCC_SPARE_I2S_SPKR_STATUS

Bits	Name	Description
31:2	RESERVED_31_2	Reserved.
1	OSR_CLK_ON	Set if the final spare I2S speaker OSR clock is on.
0	BIT_CLK_ON	Set if the final spare I2S speaker bit clock is on.

0x28000090 LCC_AVT_NS

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x000318D8

This register is used to configure the AV timer clocks.

LCC_AVT_NS

Bits	Name	Description
31:19	RESERVED_31_19	Reserved.
18	RIVA_BT_XO_INV_EN	This field enables or disables inversion of the AV timer RIVA interface BT XO clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE

LCC_AVT_NS (cont.)

Bits	Name	Description
17	RIVA_BT_XO_CXC_EN	This field enables or disables the AV timer RIVA interface BT XO clock at the CXC. 0x0: DISABLE 0x1: ENABLE
16	RIVA_BT_XO_CRC_EN	This field enables or disables the AV timer RIVA interface BT XO clock at the CRC. 0x0: DISABLE 0x1: ENABLE
15:14	RIVA_BT_XO_SRC_SEL	AV Timer RIVA interface BT XO Clock mux select. This mux is used to select BT XO clock to be MXO, CXO or PXO. 0x0: PXO 0x1: MXO 0x2: CXO 0x3: Unused
13	RIVA_FM_XO_INV_EN	This field enables or disables inversion of the AV timer RIVA interface FM XO clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
12	RIVA_FM_XO_CXC_EN	This field enables or disables the AV timer RIVA interface FM XO clock at the CXC. 0x0: DISABLE 0x1: ENABLE
11	RIVA_FM_XO_CRC_EN	This field enables or disables the AV timer RIVAinterface FM XO clock at the CRC. 0x0: DISABLE 0x1: ENABLE
10:9	RIVA_FM_XO_SRC_SEL	AV Timer RIVA interface FM XO Clock mux select. This mux is used to select FM XO clock to be MXO, CXO or PXO. 0x0: PXO 0x1: MXO 0x2: CXO 0x3: Unused
8	AVT_PXO_INV_EN	This field enables or disables inversion of the AV timer PXO clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE

LCC_AVT_NS (cont.)

Bits	Name	Description
7	AVT_PXO_CXC_EN	This field enables or disables the AV timer PXO clock at the CXC. 0x0: DISABLE 0x1: ENABLE
6	AVT_PXO_CRC_EN	This field enables or disables the AV timer PXO clock at the CRC. 0x0: DISABLE 0x1: ENABLE
5	AVT_MXO_INV_EN	This field enables or disables inversion of the AV timer MXO clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
4	AVT_MXO_CXC_EN	This field enables or disables the AV timer MXO clock at the CXC. 0x0: DISABLE 0x1: ENABLE
3	AVT_MXO_CRC_EN	This field enables or disables the AV timer MXO clock at the CRC. 0x0: DISABLE 0x1: ENABLE
2:1	AVT_GFM_SRC_SEL	XO Clock Select. This mux is used to switch to MXO, CXO or PXO. 0x0: PXO 0x1: MXO 0x2: CXO 0x3: Unused
0	ARES	AV timer asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET

0x28000094 LCC_AVT_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register provides status feedback on the AV Timer clocks.

LCC_AVT_STATUS

Bits	Name	Description
31:4	RESERVED_31_4	Reserved.

LCC_AVT_STATUS (cont.)

Bits	Name	Description
3	AVT_RIVA_BT_XO_CLK_ON	Set if the AVT timer RIVA BT Interface XO clock is on.
2	AVT_RIVA_FM_XO_CLK_ON	Set if the AVT timer RIVA FM Interface XO clock is on.
1	AVT_PCLK_ON	Set if the AVT timer PXO clock is on.
0	AVT_MCLK_ON	Set if the AVT timer MXO clock is on.

0x28000098 LCC_GLOBAL_SLP_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x000000ff

This register is used to configure global memory sleep settings.

LCC_GLOBAL_SLP_CTL

Bits	Name	Description
31:9	RESERVED_31_9	Reserved.
7:4	S	Specifies the number of cycles to wait before power collapsing the memory core/periphery after gating the clock.
3:0	W	Specifies the number of clock cycles to wait before ungating the clock after the memory core/periphery has been powered up.

0x2800009C LCC_DEBUG_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

Register for controlling LPASS Clock Control debug bus.

LCC_DEBUG_CTL

Bits	Name	Description
31:5	RESERVED_31_5	Reserved.
4:1	LCC_DEBUG_SEL	Select LPASS core debug signals.
0	LCC_DEBUG_EN	Enable debug for LCC. 0x0: Disable driving LCC debug bus on to MUX. 0x1: Drive debug bus.

0x280000A4 LCC_CLK_HS_DEBUG_CFG

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register controls mux for high speed clock debugging.

LCC_CLK_HS_DEBUG_CFG

Bits	Name	Description
31:3	RESERVED_31_3	Reserved.
2:1	HS_DEBUG_SEL	Select high speed clk to be driven to IO. 0x0: CLK_VEC_HS_lcc_q6_func_clk 0x1: CLK_VEC_HS_lcc_q6_fracdiv_clk
0	HS_DEBUG_EN	Enable debug clock.

0x280000A8 LCC_CLK_LS_DEBUG_CFG

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register controls mux for low speed clock debugging.

LCC_CLK_LS_DEBUG_CFG

Bits	Name	Description
31:7	RESERVED_31_7	Reserved.

LCC_CLK_LS_DEBUG_CFG (cont.)

Bits	Name	Description
6:1	LS_DEBUG_SEL	Select clk to be driven to IO. 0x0: CLK_VEC_LS_lcc_ahb_hclk 0x1: CLK_VEC_LS_lcc_aif_hclk 0x2: CLK_VEC_LS_lcc_security_hclk 0x3: CLK_VEC_LS_lcc_dml_hclk 0x4: CLK_VEC_LS_lcc_fab_lpb_hclk 0x5: CLK_VEC_LS_lcc_lpb_fab_hclk 0x6: CLK_VEC_LS_lcc_lpm_hclk 0x7: CLK_VEC_LS_lcc_midi_hclk 0x8: CLK_VEC_LS_lcc_q6ss_hclk 0x9: CLK_VEC_LS_lcc_avt_hclk 0xA: CLK_VEC_LS_lcc_ebus_hclk 0xB: CLK_VEC_LS_lcc_ibus_hclk 0xC: CLK_VEC_LS_lcc_core_csr_hclk 0xD: CLK_VEC_LS_lcc_lpaif_csr_hclk 0xE: CLK_VEC_LS_lcc_slimbus_hclk 0xF: CLK_VEC_LS_lcc_mi2s_bit_clk 0x10: CLK_VEC_LS_lcc_codec_i2s_mic_bit_clk 0x11: CLK_VEC_LS_lcc_codec_i2s_spkr_bit_clk 0x12: CLK_VEC_LS_lcc_spare_i2s_mic_bit_clk 0x13: CLK_VEC_LS_lcc_spare_i2s_spkr_bit_clk 0x14: CLK_VEC_LS_lcc_pcm_clk 0x15: CLK_VEC_LS_lcc_midi_clk 0x16: CLK_VEC_LS_lcc_q6_tcxo_clk 0x17: CLK_VEC_LS_lcc_q6_jtag_clk 0x18: CLK_VEC_LS_lcc_q6_slp_clk 0x19: CLK_VEC_LS_lcc_avt_mclk 0x1A: CLK_VEC_LS_lcc_avt_pclk 0x1B: CLK_VEC_LS_lcc_avt_riva_bt_clk 0x1C: CLK_VEC_LS_lcc_avt_riva_fm_clk 0x1D: CLK_VEC_LS_lcc_slimbus_core_clk
0	LS_DEBUG_EN	Enable debug clock.

0x280000AC LCC_CLK_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register provides the current status of the LPASS clocks.

LCC_CLK_STATUS

Bits	Name	Description
31:0	RESERVED_31_0	Reserved.

0x280000B0 LCC_LPM_MEM_FSCGC_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0xffffffff

LPM memory foot-switch control and clock gating cell control register.

LCC_LPM_MEM_FSCGC_CTL

Bits	Name	Description
31:24	CGC_EN	This will enable or disable the CGC clocks connected to each of the LPM memories. When enabled, the CGC block will take into account the SLP_MODE settings for the particular power collapse mode requested.
23:20	SLEEP_TIME	Programmable delay in the HM_FSCGC to turn off the clock. Min delay from HM_FSCGC is 3 cycles. Setting these bits to 0000 will result in no extra cycle delay. Setting to 1111 will result in 16 extra cycles delay.
19:16	WAKE_TIME	Programmable delay in the HM_FSCGC to turn on the clock. Min delay from HM_FSCGC is 2 cycles. Setting these bits to 0000 will result in no extra cycle delay. Setting to 1111 will result in 16 extra cycles delay.
15:0	SLP_MODE	Power collapse mode. Each successive pair of bits control the GDFS to one 16KB memory bank. Bits [1:0] correspond to the lowest 16KB, bits [3:2] correspond to the next 16KB, etc. Available modes are: ['b00] - Full Memory Collapse (immediate collapse of both periphery and core power subject to SLEEP_TIME and WAKE_TIME settings; data not retained) ['b01] - Partial Memory Collapse (collapse of periphery power subject to SLEEP_TIME and WAKE_TIME settings; collapse of core power; data retained) ['b11] - No Memory Collapse (both periphery and core power not collapsed; memory remains active and data retained)

0x280000B4 LCC_PXO_SRC_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

PXO clock source mux control register.

LCC_PXO_SRC_CTL

Bits	Name	Description
31:3	RESERVED_31_3	Reserved.
2	PXO_SRC_SEL	This mux is used to switch PXO source clock from PXO to MXO sources. This field sets the clock select of the clock mux to select. 0x0: PXO 0x1: MXO
1	GFM_CXO_SRC_ARES	CXO GFM asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET
0	GFM_CXO_SRC_SEL	There are three possible XO sources: CXO (external from PMIC), PXO (from internal oscillator) and MXO (from internal oscillator). This anti-glitch mux is used to switch PXO source clock from CXO to other possible XO sources. This field sets the clock select of the glitch free clock mux to select. 0x0: CXO 0x1: MXO/PXO

0x280000B8 LCC_SPDM_CYCNTR_CLK_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x0000000B

This register is used to configure the SPDM cycle counter clock.

LCC_SPDM_CYCNTR_CLK_CTL

Bits	Name	Description
31:5	RESERVED_31_5	Reserved.
4:3	FUNC_DIV_SEL	Controls the division ratio of the integer divider feeding the SPDM cycle counter clock. 0x0: BYPASS (DIV1) 0x1: DIV2 0x2: DIV3 0x3: DIV4

LCC_SPDM_CYCNTR_CLK_CTL (cont.)

Bits	Name	Description
2	INV_EN	This field enables or disables inversion of the SPDM cycle counter clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
1	CXC_EN	This field enables or disables the SPDM cycle counter clock at the CXC. 0x0: DISABLE 0x1: ENABLE
0	CRC_EN	This field enables or disables the SPDM cycle counter clock at the CRC. 0x0: DISABLE 0x1: ENABLE

0x280000BC LCC_SPDM_CYCNTR_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register provides status feedback on the SPDM cycle counter clock.

LCC_SPDM_CYCNTR_STATUS

Bits	Name	Description
31:1	RESERVED_31_1	Reserved.
0	CLK_ON	Set if the SPDM cycle counter clock is on.

0x280000C0 LCC_AHBIX_CSR_ARES

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

Soft Reset register for LPASS Clock Control CSR.

LCC_AHBIX_CSR_ARES

Bits	Name	Description
31:1	RESERVED_31_1	RESERVED
0	ARES	Soft Reset for CSR on AHBE Bus which consists of LCC and AHBE CSs. CSR asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET

0x280000C4 LCC_PRI_PLL_CLK_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

PXO clock source mux control register.

LCC_PRI_PLL_CLK_CTL

Bits	Name	Description
31:2	RESERVED_31_2	Reserved.
1	GFM_PRI_PLL_ARES	Primary PLL GFM asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET
0	GFM_PRI_PLL_SRC_SEL	This field sets the clock select of the glitch free clock mux to select. 0x0: PXO 0x1: PRI_PLL_CLK

0x280000C8 LCC_SEC_PLL_CLK_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

Secondary PLL clock source mux control register.

LCC_SEC_PLL_CLK_CTL

Bits	Name	Description
31:5	RESERVED_31_5	Reserved.
4	GFM_SEC_PLL_ARES	Secondary PLL GFM asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET

LCC_SEC_PLL_CLK_CTL (cont.)

Bits	Name	Description
3:2	SEC_PLL_CLK_DIV_SEL	Controls the division ratio of the integer divider feeding the muxed secondary PLL clock. 0x0: BYPASS (DIV1) 0x1: DIV2 0x2: DIV3 0x3: DIV4
1	GFM_SEC_PLL_XO_SEL	This field sets the clock select of the glitch free clock mux to select. 0x0: PXO 0x1: SEC_PLL_CLK
0	SEC_PLL_MUX_SEL	This field sets the clock select of clock mux to select: 0x0: MMPLL1 clock source (800 MHz.) 0x1: GPLL0 clock source (552 MHz.)

0x280000CC LCC_SLIMBUS_NS

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00001600

This register is used to configure the SLIMBus Core clock.

LCC_SLIMBUS_NS

Bits	Name	Description
31:24	N_VAL	Specifies the N value for the MN counter. Used only when the MN counter is enabled. Must use software register format NOT(N-M).
23:14	RESERVED_23_14	Reserved.
13	SPS_SLIMBUS_INV_EN	LPASS shares SLIMBus in SPS. This field enables or disables the inversion of the SLIMBus clock to SPS at the CXC. Uninverted clock Inverted clock 0x0: DISABLE 0x1: ENABLE
12	SPS_SLIMBUS_CXC_EN	LPASS shares SLIMBus in SPS. This field enables or disables the SLIMBus clock to SPS at the CXC. 0x0: DISABLE 0x1: ENABLE

LCC_SLIMBUS_NS (cont.)

Bits	Name	Description
11	AUDIO_SLIMBUS_INV_EN	This field enables or disables inversion of the Audio SLIMBus clock at the CXC. Uninverted clock Inverted clock 0x0: DISABLE 0x1: ENABLE
10	AUDIO_SLIMBUS_CXC_EN	This field enables or disables the Audio SLIMBus clock at the CXC. 0x0: DISABLE 0x1: ENABLE
9	MNCNTR_CLK_EN	Halts the output clock of the MN counter. 0x0: DISABLE 0x1: ENABLE
8	MNCNTR_EN	This field is used to enable or disable the MN counter. 0x0: DISABLE 0x1: ENABLE
7	MNCNTR_RST	This field activates the MN counter reset. 0x0: NORMAL_MODE 0x1: RESET
6:5	MNCNTR_MODE	This field sets the mode of the MN counter. No division. Remove clock cycles to reduce the average frequency. Requires timing closure at the undivided frequency. Uses both edges of the input clock to perform division. Provides better output duty cycles than single edge and swallow. Uses only the rising edge of the input clock to perform division. Better than clock swallowing. 0x0: BYPASS 0x1: SWALLOW 0x2: DUAL_EDGE 0x3: SINGLE_EDGE
4:3	PRE_DIV_SEL	This field sets the pre-division of the input clock to the MN counter. 0x0: BYPASS 0x1: DIV2 0x2: DIV3 0x3: DIV4

LCC_SLIMBUS_NS (cont.)

Bits	Name	Description
2:0	MN_SRC_SEL	This field sets the clock select of the MN counter. OTHERS: RESERVED 0x0: PXO 0x1: CXO 0x2: LPA_PLL 0x3: SEC_PLL 0x6: CLK_TEST_SE 0x7: PLL_TEST_SE

0x280000D0 LCC_SLIMBUS_MD

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to configure the SLIMBus clock.

LCC_SLIMBUS_MD

Bits	Name	Description
31:16	RESERVED_31_16	Reserved.
15:8	M_VAL	Specifies the M value for the MN counter. Used only when the MN counter is enabled.
7:0	NOT_2D_VAL	Specifies the NOT(2*D) value for the MN counter.

0x280000D4 LCC_SLIMBUS_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register provides status feedback on the SLIMBus core clock.

LCC_SLIMBUS_STATUS

Bits	Name	Description
31:2	RESERVED_31_2	Reserved.
1	SPS_SLIMBUS_CLK_ON	Set if the SPS SLIMBus core clock is on.
0	AUDIO_SLIMBUS_CLK_ON	Set if the LPASS Audio SLIMBus core clock is on.

0x280000D8 LCC_GFS_CNTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000300

Control for Global Footer Switch Controller.

LCC_GFS_CNTL

Bits	Name	Description
31:10	RESERVED_31_10	Reserved.
9	GFS_RET	Foot-switch Retention bit. GFS_RET = 0 and GFS_EN = 0 will collapse the power to the core. GFS_RET = 1 and GFS_EN = 0 put core into VDD_MIN stage (aka sleep mode).
8	GFS_EN	Foot-switch enable bit. GFS_EN = 1 for core operational mode. When GFS_EN = 1, GFS_RET is a don't care.
7:6	RESERVED_7_6	Reserved
5	CLAMP	Clamp I/O bit for the core. 0x1: clamp 0x0: unclamp
4:0	GFS_CNT	This is the number of AHB_CLK cycles to delay the assertion of gfs_en_all after the assertion of gfs_en1 when enabling the global distributed footswitch. Should set to all 1s for safe mode operation. Decreasing the CNT value can reduce latency.

0x280000DC LCC_GFS_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

Control for Global Footer Switch Controller Status.

LCC_GFS_STATUS

Bits	Name	Description
31:1	RESERVED_31_1	Reserved.
0	GFS_STATUS	Power status for GFS 0x0: OFF 0x1: ON.

0x280000E0 LCC_MEM_ACC_NS

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

.Controls LPASS Memory ACC value settings.

LCC_MEM_ACC_NS

Bits	Name	Description
31:24	RESERVED_31_24	Reserved.
23:20	SPLRF240	Compiler regfile.
19:16	STDSP155	Compiler single port RAM.
15:12	LLRF240	Compiler regfile.
11:8	STDVROM	Compiler ROM.
7:4	LLPDP155	Compiler pseudo dual port RAM.
3:0	LLSP155	Compiler single port RAM.

0x280000E4 LCC_AHBEX_BRANCH_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x000A1259

This register is used to configure the AHB LPASS clock branches.

LCC_AHBEX_BRANCH_CTL

Bits	Name	Description
31:21	RESERVED_31_21	Reserved
20	CORE_IBUS_SPDMTM_HCLK_INV_EN	This field enables or disables inversion of the LPASSCore AHB-IX Fabric SPDM Traffic Monitor CSR clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
19	CORE_IBUS_SPDMTM_HCLK_CXC_EN	This field enables or disables the LPASS Core AHB-IX Fabric SPDM Traffic Monitor CSR clock at the CXC. 0x0: DISABLE 0x1: ENABLE

LCC_AHBEX_BRANCH_CTL (cont.)

Bits	Name	Description
18	LPASS_EBUS_HCLK_INV_EN	This field enables or disables inversion of the LPASS AHB-E Bus clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
17	LPASS_EBUS_HCLK_CXC_EN	This field enables or disables the LPASS AHB-E Bus clock at the CXC. 0x0: DISABLE 0x1: ENABLE
16	CORE_SPDM_XBUS_CGC_EN	LPASS Core AHB-X Bus SPDM Traffic monitor clock enable.
15	CORE_SPDM_IBUS_CGC_EN	LPASS Core AHB-I Bus SPDM Traffic monitor clock enable.
14	CORE_IBUS_ARES	LPASS Core AHB-IX Bus Fabric soft reset. 0x0: NORMAL_MODE 0x1: RESET
13	CORE_IBUS_HCLK_INV_EN	This field enables or disables inversion of the LPASS Core AHB-IX Bus clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
12	CORE_IBUS_HCLK_CXC_EN	This field enables or disables the LPASS Core AHB-IX Bus clock at the CXC. 0x0: DISABLE 0x1: ENABLE
11	CORE_CSR_ARES	LPASS Core CSR core soft reset. 0x0: NORMAL_MODE 0x1: RESET
10	CORE_CSR_HCLK_INV_EN	This field enables or disables inversion of the LPASS Core CSR clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE

LCC_AHBEX_BRANCH_CTL (cont.)

Bits	Name	Description
9	CORE_CSR_HCLK_CXC_EN	This field enables or disables the LPASS Core CSR clock at the CXC. 0x0: DISABLE 0x1: ENABLE
8	LPAIF_CSR_ARES	Asynchronous reset for the LPA Interface CSR interface. 0x0: NORMAL_MODE 0x1: RESET
7	LPAIF_CSR_HCLK_INV_EN	This field enables or disables inversion of the LPA Interface CSR clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
6	LPAIF_CSR_HCLK_CXC_EN	This field enables or disables the LPA Interface CSR clock at the CXC. 0x0: DISABLE 0x1: ENABLE
5	SLIMBUS_ARES	SLIMBus asynchronous reset. 0x0: NORMAL_MODE 0x1: RESET
4	SLIMBUS_MEM_CORE_EN	Power collapses the SLIMBus memory core. All data will be lost. 0x0: COLLAPSE 0x1: NORMAL_MODE
3:2	SLIMBUS_MEM_PERIPH_EN	Power collapse the SLIMBus memory periphery. Data is retained but is inaccessible until the periphery is powered up. 0x0: COLLAPSE_GRACEFULLY 0x1: COLLAPSE_IMMEDIATELY 0x2: NORMAL_MODE 0x3: RESERVED
1	SLIMBUS_HCLK_INV_EN	This field enables or disables inversion of the SLIMBus clock at the CXC. Uninverted clock. Inverted clock. 0x0: DISABLE 0x1: ENABLE
0	SLIMBUS_HCLK_CXC_EN	This field enables or disables the SLIMBus clock at the CXC. 0x0: DISABLE 0x1: ENABLE

0x280000E8 LCC_AHBEX_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x000000ff

This register provides status feedback on the AHB LPASS clocks.

LCC_AHBEX_STATUS

Bits	Name	Description
31:8	RESERVED_31_8	Reserved.
7	LPASS_IBUS_SPDMTM_HCLK_ON	Set if the final LPASS Core Fabric AHB-IX SPADM Traffic Monitor Clock AHB clock is on.
6	LPASS_EBUS_HCLK_ON	Set if the final LPASS AHB-E AHB clock is on.
5	CORE_IBUS_HCLK_ON	Set if the final LPASS Core AHB-I Bus AHB clock is on.
4	CORE_CSR_HCLK_ON	Set if the final LPASS Core CSR AHB clock is on.
3	LPAIF_CSR_HCLK_ON	Set if the final LPA Interface CSR AHB clock is on.
2	SLIMBUS_MEM_CORE_ON	Set if the SLIMBus memory core is on.
1	SLIMBUS_MEM_PERIPH_ON	Set if the SLIMBus memory periphery is on.
0	SLIMBUS_HCLK_ON	Set if the final SLIMBus AHB clock is on.

0x280000EC LCC_AHBM_CLK_HYSTERISIS_CTL

Type: Read/Write
Clock: LCC_AHB_HCLK
Reset State: 0x00000001

This register controls LPASS AHB Master Interface to System fabric clock hysterisis counters.

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LCC_AHBM_CLK_HYSTERISIS_CTL

Bits	Name	Description
31:11	RESERVED_31_11	Reserved.

LCC_AHBM_CLK_HYSTERISIS_CTL (cont.)

Bits	Name	Description
10:8	SEL_STARTUP_HYSTERISIS	This fields specifies the number of cycles the clock has to be active before the AHB Master can begin any transaction. 0x0: 0 clocks. 0x1: 3 clocks. 0x2: 5 clocks. 0x3: 7 clocks. 0x4: 9 clocks. 0x5: 11clocks. 0x6: 13 clocks. 0x7: 15 clocks.
7	RESERVED_7	Reserved.
6:4	SELECT_HALT_HYSTERISIS	This counter is meant to cover any gaps resulting from early de-assertion of CLK ON. Number of clock cycles to wait before halting LPASS Master AHBIX Clock after clock active is de-asserted. Keep Clock running for: 0x0: 15 clocks. 0x1: 13 clocks. 0x2: 11 clocks. 0x3: 9 clocks. 0x4: 7 clocks. 0x5: 5 clocks. 0x6: 3 clocks. 0x7: 0 clocks.
3:1	SEL_ACTIVE_HYSTERISIS	This counter start counting with after CLK ON is deasseterd. Number of clock cycles to wait before de-asserting clock active status. Number of clock to wait before de-asserting Clock Active: 0x0: 255 Clock 0x1: 128 Clock 0x2: 64 Clock 0x3: 32 Clock 0x4: 16 Clock 0x5: 8 Clock 0x6: 4 Clock 0x7: 2 Clock
0	DISABLE	Enable Hysteris Counter for LPASS Master AHBIX Clock.

12.2.2 AHBE

0x28001000 AHBE_CFG

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000100

In programmable priority mode a higher value on master priority indicates higher priority. Priority values programmed must lie in the range [0,1].

AHBE_CFG

Bits	Name	Description
31:9	RESERVED_31_9	Reserved.
8	Q6SS_PRIORITY	Q6SS priority in programmable priority mode
7:5	RESERVED_7_5	Reserved.
4	FABRIC_PRIORITY	FABRIC priority in programmable priority mode
3:1	RESERVED_3_1	Reserved.
0	ROUND_ROBIN_EN	Set(1) to enable round robin arbitration on AHB Clear(0) to enable priority based arbitration on AHB

0x28001004 AHBE_LOCK_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to enable or disable locking of the AHBE bus by its masters.

AHBE_LOCK_CTL

Bits	Name	Description
31:2	RESERVED_31_2	Reserved.
1	Q6SS_LOCK_EN	Set(1) to enable locking of AHBE by Q6SS Clear(0) to disable locking of AHBE by Q6SS
0	FABRIC_LOCK_EN	Set(1) to enable locking of AHBE by FABRIC Clear(0) to disable locking of AHBE by FABRIC

0x28001008 LPASS_AHBE_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register provides the status of lpass_ahbe errors.

LPASS_AHBE_STATUS

Bits	Name	Description
31:8	RESERVED_31_3	Reserved.
2	AHBE_DECODE_BOUNDARY_ERROR	This bit is set when beats of a burst on AHBE are decoded to different slaves.
1	AHBE_DECODE_ERROR	This bit is set when an access is made to a reserved region.on AHBE.
0	AHBE_MISALIGNED	This bit is set if there is a word or half-word access on AHBE with address not aligned to word or half-word boundary respectively. e.g., hsize=1, haddr(0)=1

0x2800100C LPASS_AHBE_ACK

Type: Write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This write-only register is used to clear the status bits set in LPASS_AHBE_STATUS.

LPASS_AHBE_ACK

Bits	Name	Description
31:8	RESERVED_31_3	Reserved.
2	AHBE_DECODE_BOUNDARY_ERROR	Set (1) to clear corresponding bit in LPASS_AHBE_STATUS.
1	AHBE_DECODE_ERROR	Set (1) to clear corresponding bit in LPASS_AHBE_STATUS.
0	AHBE_MISALIGNED	Set (1) to clear corresponding bit in LPASS_AHBE_STATUS.

0x28001010 LPASS_AHBE_SPARE

Type: Read/Write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This is spare register for using future.

LPASS_AHBE_SPARE

Bits	Name	Description
31:0	AHBE_SPARE	Spare register.

12.2.3 LPASS Wrapper General Registers

0x28004004 LPASS_VFR_IRQ_MUX_CTL

Type: Read/Write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This is spare register for using future.

LPASS_VFR_IRQ_MUX_CTL

Bits	Name	Description
31:3	RESERVED_31_3	Reserved
2:0	SEL	(source from internal modem) 0x0: VFR. Vocoder frame rate interrupt from modem for voice rate matching. 0x1: EXT_VFR. External VFR from gpio. 20 ms reference time tick for tracking audio rates vs. the air interface. 0x2: LPASS IRQ0_1 0x3: LPASS IRQ0_2 0x4: LPASS IRQ0_3 0x5: LPASS IRQ0_4 0x6: LPASS IRQ0_5 0x7: Undefined

12.2.4 Non-Clock

12.2.4.1 General subsystem

0x28008000 LPASS_CSR_GP_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000001

General purpose ECO over-ride bits.

LPASS_CSR_GP_CTL

Bits	Name	Description
31:7	SPARE_LPASS	Spare register for using future
6	BUS_BUG_RRBUG_DIS	Disable of bug fix logic related to CR-0000146349.
5	BUS_BUG_BUSY_DIS	Disable of fixed hready de-assert timing when busy cycle.

LPASS_CSR_GP_CTL (cont.)

Bits	Name	Description
4	BUS_BUG_SEL_DIS	Disable of fixed hsel signal active time.
3	BUS_BUG_ARITER_DIS	Disable of hgrant extending logic.
2	DML_HPROT_NB_EN	Enable DMLITE non-buffer-able transfers
1	MIDI_HPROT_NB_EN	Enable non-bufferable AHB transfer for MIDI.
0	AHB2AXI_HPROT_RETAIN	Disable AHB to AXI HPROT retaining.

12.2.4.2 AHB

0x28008004 AHBI_CFG

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00512340

In programmable priority mode a higher value on master priority indicates higher priority. Priority values programmed must lie in the range [0,4].

AHBI_CFG

Bits	Name	Description
31:27	RESERVED_31_23	Reserved.
26:24	SLIMBUS_PRIORITY	SLIMBUS priority in programmable priority mode.
23	RESERVED_23	Reserved.
22:20	MIDI_PRIORITY	MIDI priority in programmable priority mode.
19	RESERVED_19	Reserved.
18:16	FABRIC_PRIORITY	FABRIC priority in programmable priority mode.
15	RESERVED_15	Reserved.
14:12	DM_PRIORITY	DM priority in programmable priority mode
11	RESERVED_11	Reserved.
10:8	Q6SS_PRIORITY	Q6SS priority in programmable priority mode
7	RESERVED_7	Reserved
6:4	AUDIO_IF_PRIORITY	Audio_If priority in programmable priority mode
3:1	RESERVED_3_1	Reserved.
0	ROUND_ROBIN_EN	Set(1) to enable round robin arbitration on AHB Clear(0) to enable priority based arbitration on AHB

0x28008008 AHBX_CFG

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00301020

In programmable priority mode a higher value on master priority indicates higher priority. Priority values programmed must lie in the range [0,3].

AHBX_CFG

Bits	Name	Description
31:26	RESERVED_31_26	Reserved.
25:24	SLIMBUS_PRIORITY	SLIMBUS priority in programmable priority mode.
23:22	RESERVED_23_22	Reserved.
21:20	MIDI_PRIORITY	MIDI priority in programmable priority mode.
19:14	RESERVED_19_14	Reserved.
13:12	DM_PRIORITY	DM priority in programmable priority mode
11:6	RESERVED_11_6	Reserved.
5:4	AUDIO_IF_PRIORITY	Audio_If priority in programmable priority mode
3:1	RESERVED_3_1	Reserved.
0	ROUND_ROBIN_EN	Set(1) to enable round robin arbitration on AHB Clear(0) to enable priority based arbitration on AHB

0x2800800C AHB_CLK_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is un-used.

AHB_CLK_CTL

Bits	Name	Description
31:16	RESERVED_31_16	Reserved.
15:8	FORCE_CLK_ON_AHBI	Force AHB (I) slave clock on.
7:0	FORCE_CLK_ON_AHBX	Force AHB (X) slave clock on.

0x28008010 AHBI_LOCK_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to enable or disable locking of the AHBI bus by its masters.

AHBI_LOCK_CTL

Bits	Name	Description
31:6	RESERVED_31_6	Reserved.
5	SLIMBUS_LOCK_EN	Set(1) to enable locking of AHBI by SLIMBUS Clear(0) to disable locking of AHBI by SLIMBUS
4	MIDI_LOCK_EN	Set(1) to enable locking of AHBI by MIDI Clear(0) to disable locking of AHBI by MIDI
3	FABRIC_LOCK_EN	Set(1) to enable locking of AHBI by FABRIC Clear(0) to disable locking of AHBI by FABRIC
2	DM_LOCK_EN	Set(1) to enable locking of AHBI by DM Clear(0) to disable locking of AHBI by DM
1	Q6SS_LOCK_EN	Set(1) to enable locking of AHBI by Q6SS Clear(0) to disable locking of AHBI by Q6SS
0	AUDIO_IF_LOCK_EN	Set(1) to enable locking of AHBI by AUDIO_IF Clear(0) to disable locking of AHBI by AUDIO_IF

0x28008014 AHBX_LOCK_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to enable or disable locking of the AHBI bus by its masters

AHBX_LOCK_CTL

Bits	Name	Description
31:6	RESERVED_31_6	Reserved.
5	SLIMBUS_LOCK_EN	Set(1) to enable locking of AHBX by SLIMBUS Clear(0) to disable locking of AHBX by SLIMBUS
4	MIDI_LOCK_EN	Set(1) to enable locking of AHBX by MIDI Clear(0) to disable locking of AHBX by MIDI
3	RESERVED_3	Reserved.

AHBX_LOCK_CTL (cont.)

Bits	Name	Description
2	DM_LOCK_EN	Set(1) to enable locking of AHBX by DM Clear(0) to disable locking of AHBX by DM
1	RESERVED_1	Reserved.
0	AUDIO_IF_LOCK_EN	Set(1) to enable locking of AHBX by AUDIO_IF Clear(0) to disable locking of AHBX by AUDIO_IF

0x2800802C LPASS_BUS_STATUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register provides the status of lpass_bus errors.

LPASS_BUS_STATUS

Bits	Name	Description
31:8	RESERVED_31_8	Reserved.
7	Q6TCM_WRITE_ERROR	This bit is set when the Q6 AXI slave returns a write response error.
6	Q6TCM_READ_ERROR	This bit is set when the Q6 AXI slave returns a read response error.
5	AHBX_DECODE_BOUNDARY_ERROR	This bit is set when beats of a burst on AHBX are decoded to different slaves.
4	AHBX_DECODE_ERROR	This bit is set when an access is made to a reserved region.on AHBX.
3	AHBX_MISALIGNED	This bit is set if there is a word or half-word access on AHBX with address not aligned to word or half-word boundary respectively. e.g., hsize=1, haddr(0)=1
2	AHBI_DECODE_BOUNDARY_ERROR	This bit is set when beats of a burst on AHBI are decoded to different slaves.
1	AHBI_DECODE_ERROR	This bit is set when an access is made to a reserved region.on AHBI.
0	AHBI_MISALIGNED	This bit is set if there is a word or half-word access on AHBI with address not aligned to word or half-word boundary respectively. e.g., hsize=1, haddr(0)=1

0x28008030 LPASS_BUS_ACK

Type: Write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This write-only register is used to clear the status bits set in LPASS_BUS_STATUS.

LPASS_BUS_ACK

Bits	Name	Description
31:8	RESERVED_31_8	Reserved.
7	Q6TCM_WRITE_ERROR	Set (1) to clear corresponding bit in LPASS_BUS_STATUS.
6	Q6TCM_READ_ERROR	Set (1) to clear corresponding bit in LPASS_BUS_STATUS.
5	AHBX_DECODE_BOUNDARY_ERROR	Set (1) to clear corresponding bit in LPASS_BUS_STATUS.
4	AHBX_DECODE_ERROR	Set (1) to clear corresponding bit in LPASS_BUS_STATUS.
3	AHBX_MISALIGNED	Set (1) to clear corresponding bit in LPASS_BUS_STATUS.
2	AHBI_DECODE_BOUNDARY_ERROR	Set (1) to clear corresponding bit in LPASS_BUS_STATUS.
1	AHBI_DECODE_ERROR	Set (1) to clear corresponding bit in LPASS_BUS_STATUS.
0	AHBI_MISALIGNED	Set (1) to clear corresponding bit in LPASS_BUS_STATUS.

12.2.4.3 DM lite

DM is a single channel data mover that has been designed to offload DSP from long/large size transfers, while not incurring the area or power penalty of a fully-functional data mover such as ADM2 etc. The intended mode of operation is DM operating as a slave accelerator of the LPASS QDSP6. However protection from other processors is not guaranteed. Other processors (or even user mode QDSP6 processes) can reprogram DMLite in the midst of an active transfer, and cause undefined states in the system. Only QDSP6 has the outgoing interrupt from DMLite, and hence is fully capable of controlling it.

0x28008040 DML_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register controls the operation for the DM-Lite block. The Crypto block is not featured in this version of LPASS, therefore the Crypto enable register (bit 4) is not functional.

DML_CTL

Bits	Name	Description
31:5	RESERVED_31_5	Reserved.
4	CRYPTO_EN	When set (1), pipe through internal crypto engine
3:2	SWAP	No modification {a,b,c,d} -> {c,d,a,b} {a,b,c,d} -> {d,c,b,a} {a,b,c,d} -> {b,a,d,c} 0x0: NULL 0x1: Half word 0x2: Half word and byte 0x3: Byte
1:0	CMD	Commands to the DML can be Flush will force DM to terminate an initiate or a zero command if it is in progress. If DM is active, flush has no effect. Initiate is used to start a single transfer from the given source to destination. Zero is a special mode to initiate a transfer where the source data value is constant and equal to zero. This command can be used to zero fill a memory 0x0: Flush 0x1: Initiate 0x2: Zero

0x28008044 DML_SRC

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register will provide the DML block with the source address from which to request data from.

DML_SRC

Bits	Name	Description
31:2	ADDR	Source address.
1:0	RESERVED_1_0	Reserved due to 32-bit alignment of address.

0x28008048 DML_DST

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register will provide the DML block with the destination address from which to write data to.

DML_DST

Bits	Name	Description
31:2	ADDR	Destination address.
1:0	RESERVED_1_0	Reserved due to 32-bit alignment of address.

0x2800804C DML_TRAN

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to identify the number of bytes the DML should transfer from the source address to the destination address. The maximum amount of data that can be transferred is 128KB. The value programmed into this register should be (number of dwords) - 1.

DML_TRAN

Bits	Name	Description
31:20	RESERVED_31_20	Reserved.
19:2	LEN	Maximum length of transfer is 128 KB.
1:0	RESERVED_1_0	Reserved due to 32-bit alignment of address.

0x28008050 DML_STATUS

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to convey the status of some DML internal signals.

DML_STATUS

Bits	Name	Description
23:6	WORDS	READ ONLY: DWords remaining.
5:2	RESERVED_5_2	Reserved.
1	ERROR	Error during transfer. Set (1) to clear error bit.
0	DONE	Transfer complete. Set (1) to clear done bit.

0x2800805C LPASS_DEBUG_CTL

Type: Read/write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

This register is used to select which module or sub-core drives the lpass test bus.

LPASS_DEBUG_CTL

Bits	Name	Description
31:23	RESERVED_31_23	Reserved.
22:11	LPASS_DEBUG_SEL	Select LPASS core debug signals.
10:7	LPASS_DEBUG_SEL_4	Select AVTimer debug signals.
6	LPASS_DEBUG_EN	Enable debug for LPASS core. 0x0: Disable driving LPASS bus on to MUX 0x1: Drive debug bus
5:3	IP_DEBUG_SEL	Selects connection of LPASS_TEST_BUS to: 0x0: All 0's 0x1: All 5's 0x2: All A's 0x3: LPA_IF debug bus 0x4: MIDI debug bus 0x5: LCC debug bus 0x6: Q6SS debug bus 0x7: LPASS_CORE debug bus
2:0	SEL	Selects connection of LPASS_CORE debug bus to: 0x0: LPM0 signals 0x1: LPM1 signals 0x2: DML debug bus 0x3: AHB debug bus 0x4: CSR debug bus 0x5: AVTIMER debug bus 0x6: SLIMBus debug bus

0x28008060 LPASS_DEBUG_BUS

Type: Read
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

Debug signals sourced by lpass modules or subcores.

LPASS_DEBUG_BUS

Bits	Name	Description
31:0	READ	Read back for debug bus.

0x28008070 LPASS_CORE_GEN_CTL

Type: Read/Write
Clock: LCC_AHB_HCLK
Reset State: 0x00000000

LPASS Core General Control.

LPASS_CORE_GEN_CTL

Bits	Name	Description
31:1	RESERVED_31_1	Reserved.
0	VFR_IRQ_SRC_SEL	VFR IRQ source select 0x0: AVTIMER output 0x1: On-chip modem output

12.2.5 AVtimer/AVsync

0x28009000 AVTIMER_CTL

Type: Read/write
Clock: LCC_AVT_HCLK
Reset State: 0x00000000

AVtimer control/status register

AVTIMER_CTL

Bits	Name	Description
31:12	RESERVED_31_12	Reserved.
11	VCAP_TIMER_OUT_EN	VCAP Timer output enable. 0x1: Enable
10	DRE_BUSY	READ ONLY: High when DRE counter is running.
9	TIMEOUT_EN	Enables time out function if ahb to mxo transfers takes longer than timeout value register 0x1: Enable ahb timeout

AVTIMER_CTL (cont.)

Bits	Name	Description
8	TIMER_RST	Sets timer counter to zero. This is not a soft reset for AVTIMER. 0x1: Reset timer value to zero
7	TIMER_EN	0x1: Enable timer
6	INTD_MSK	0x1: Mask DRE interrupt 0x0: Unmask DRE interrupt
5	INT1_MSK	0x1: Mask INT1 0x0: Unmask INT1
4	INT0_MSK	0x1: Mask INT0 0x0: Unmask INT0
3	INTD_CLR	0x1: Clear DRE INT
2	INT1_CLR	0x1: Clear INT1
1	INT0_CLR	0x1: Clear INT0
0	DRE_GO	0x1: Start DRE operation

0x28009004 AVTIMER_RESMOD

Type: Read/write
Clock: LCC_AVT_HCLK
Reset State: 0x0000000

Residue_modulus register.

AVTIMER_RESMOD

Bits	Name	Description
31:0	RESMOD	Resmod value (12.20 fixed format).

0x28009008 AVTIMER_TIMER_LSB

Type: Read/write
Clock: LCC_AVT_HCLK
Reset State: 0x00000000

Timer LSB bits.

AVTIMER_TIMER_LSB

Bits	Name	Description
31:0	TIMER_LSB	Value of timer lsb[31:0] bits.

0x2800900C AVTIMER_TIMER_MSB

Type: Read/write
Clock: LCC_AVT_HCLK
Reset State: 0x00000000

Timer MSB bits.

AVTIMER_TIMER_MSB

Bits	Name	Description
31:16	RESERVED	Reserved.
15:0	TIMER_MSB	Value of timer lsb[47:32] bits.

0x28009010 AVTIMER_INT0_LSB

Type: Read/write
Clock: LCC_AVT_HCLK
Reset State: 0x00000000

INT0 LSB bits.

AVTIMER_INT0_LSB

Bits	Name	Description
31:0	INT0_LSB	Value at which timer issues int0. LSB bits.

0x28009014 AVTIMER_INT0_MSB

Type: Read/write
Clock: LCC_AVT_HCLK
Reset State: 0x00000000

INT0 MSB bits

AVTIMER_INT0_MSB

Bits	Name	Description
31:16	RESERVED	Reserved.
15:0	INT0_MSB	Value at which timer issues int0. MSB bits.

0x28009018 AVTIMER_INT1_LSB

Type: Read/write
Clock: LCC_AVT_HCLK
Reset State: 0x00000000

INT1 LSB bits.

AVTIMER_INT1_LSB

Bits	Name	Description
31:0	INT1_LSB	Value at which timer issues int1. LSB bits.

0x2800901C AVTIMER_INT1_MSB

Type: Read/write
Clock: LCC_AVT_HCLK
Reset State: 0x00000000

INT1 MSB bits

AVTIMER_INT1_MSB

Bits	Name	Description
31:16	RESERVED	Reserved.
15:0	INT1_MSB	Value at which timer issues int1. MSB bits.

0x28009020 AVTIMER_DRE_TARGET_VALUE

Type: Read/write
Clock: LCC_AVT_HCLK
Reset State: 0x00000000

DRE target value (max count) in mxo domain.

AVTIMER_DRE_TARGET_VALUE

Bits	Name	Description
31:0	DRE_TARGET_VALUE	DRE target value.

0x28009024 AVTIMER_TIMEOUT_VAL

Type: Read/write
Clock: LCC_AVT_HCLK
Reset State: 0x00000000

AHB interface timeout.

AVTIMER_TIMEOUT_VAL

Bits	Name	Description
31:12	RESERVED	Reserved.
11:0	TIMEOUT_VAL	AHB to MXO interface will abort if it does not receive an ack from mxo after this number of ahb clocks. Returns ERROR on AHB.

0x28009028 AVTIMER_DRE_CNT_PXO

Type: Read
Clock: LCC_AVT_HCLK
Reset State: 0x00000000

DRE (slave) counter in pxo domain.

AVTIMER_DRE_CNT_PXO

Bits	Name	Description
31:0	DRE_CNT_PXO	Value of dre slave counter in PXO clock domain

0x28009400 AUD_SYNC_CTL

Type: Read/write
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

Control register

AUD_SYNC_CTL

Bits	Name	Description
31:17	RESERVED_1	RESERVED
16	VFR_INT_SEL	Selects either the external modem interrupt or the internal modem interrupt. 0x0: internal 0x1: external

AUD_SYNC_CTL (cont.)

Bits	Name	Description
15:14	RESERVED_2	RESERVED
13	FM_PH_ADJ_NEG_WE	In SW tracking method, writing 1 to this bit decrements sample counter by 1
12	FM_PH_ADJ_POS_WE	In SW tracking method, writing 1 to this bit increments sample counter by 1
11	FM_XO_DIV_EN	Enables XO divider 0x1: ENABLE
10	FM_PH_TRK_EN	FM Phase Tracker Enable 0x1: ENABLE
9	FM_XO_DIV_RESET	FM XO divider Reset 0x1: RESET
8	FM_PH_TRK_RESET	Resets FM Phase Tracker. 0x1: RESET
7	BT_PH_ADJ_NEG_WE2	In SW tracking method, writing 1 to this bit decrements sample counter by 1 for DPLL 2
6	BT_PH_ADJ_POS_WE2	In SW tracking method, writing 1 to this bit increments sample counter by 1 for DPLL 2.
5	BT_PH_ADJ_NEG_WE1	In SW tracking method, writing 1 to this bit decrements sample counter by 1 for DPLL 1
4	BT_PH_ADJ_POS_WE1	In SW tracking method, writing 1 to this bit increments sample counter by 1 for DPLL 1
3	BT_XO_DIV_EN	Enables XO divider 0x1: ENABLE
2	BT_PH_TRK_EN	Enables BT SCO TX Phase Tracker. 0x1: ENABLE
1	BT_XO_DIV_RESET	Resets BT SCO TX divider 0x1: RESET
0	BT_PH_TRK_RESET	BT SCO TX Phase Tracker Reset 0x1: RESET

0x28009404 AUD_SYNC_STATUS

Type: Read/write
Clock: LCC_RES_XCLK
Reset State: 0x00000000

Status of AUD_SYNC module. This is a write-one-to-clear register.

AUD_SYNC_STATUS

Bits	Name	Description
31:6	RESEREVED	RESERVED
5	FM_COUNT_OVF_REF	FM overflow status for reference counter
4	FM_COUNT_OVF_XO	FM overflow status for sample counter
3	BT_COUNT_OVF_REF2	BT SCO TX overflow status for reference counter 2
2	BT_COUNT_OVF_XO2	BT SCO TX overflow status for sample counter 2
1	BT_COUNT_OVF_REF1	BT SCO TX overflow status for reference counter 1
0	BT_COUNT_OVF_XO1	BT SCO TX overflow status for sample counter 1

0x28009408 AUD_SYNC_BT_REF_INC

Type: Read/write
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

AUD_SYNC_BT_REF_INC

Bits	Name	Description
31:16	REF_INC2	Number of samples strobe counter is incremented each time for BT SCO TX for second DPLL.
15:0	REF_INC1	Number of samples strobe counter is incremented each time for BT SCO TX for first DPLL.

0x2800940C AUD_SYNC_BT_XO_DIV_MOD

Type: Read/write
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

BT SCO TX L and M Register

AUD_SYNC_BT_XO_DIV_MOD

Bits	Name	Description
27:16	L	This is the integer portion.
11:0	M	This is the fractional portion.

0x28009410 AUD_SYNC_BT_PHASE_CHK_XO1

Type: Read
Clock: LCC_RES_XCLK
Reset State: 0x00000000

Bluetooth SCO TX XO Phase Check

AUD_SYNC_BT_PHASE_CHK_XO1

Bits	Name	Description
31:0	COUNTER	Snapshot of sample counter

0x28009414 AUD_SYNC_BT_PHASE_CHK_REF1

Type: Read
Clock: LCC_RES_XCLK
Reset State: 0x00000000

Bluetooth SCO TX Reference Phase Check

AUD_SYNC_BT_PHASE_CHK_REF1

Bits	Name	Description
31:0	COUNTER	Snapshot of strobe counter

0x28009418 AUD_SYNC_BT_VFR_TIMESTAMP

Type: Read
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

Bluetooth SCO TX VFR Timestamp

AUD_SYNC_BT_VFR_TIMESTAMP

Bits	Name	Description
31:0	TIMESTAMP	Adjusted value of sample counter

0x2800941C AUD_SYNC_BT_COUNT_LOAD_XO1

Type: Read/write
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

pBT TX SCO sample counter load

AUD_SYNC_BT_COUNT_LOAD_XO1

Bits	Name	Description
31:0	COUNT	Writing to this register causes the content of this register to be loaded into the BT SCO TX sample counter number 1.

0x28009420 AUD_SYNC_BT_COUNT_LOAD_REF1

Type: Read/write
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

BT SCO TX strobe counter load.p

AUD_SYNC_BT_COUNT_LOAD_REF1

Bits	Name	Description
31:0	COUNT	Writing to this register causes the contents of this register to be loaded into the BT SCO TX strobe counter.number 1.

0x28009424 AUD_SYNC_BT_PHASE_CHK_XO2

Type: Read
Clock: LCC_RES_XCLK
Reset State: 0x00000000

Bluetooth SCO TX XO Phase Check number 2

AUD_SYNC_BT_PHASE_CHK_XO2

Bits	Name	Description
31:0	COUNTER	Snapshot of sample counter

0x28009428 AUD_SYNC_BT_PHASE_CHK_REF2

Type: Read
Clock: LCC_RES_XCLK
Reset State: 0x00000000

Bluetooth SCO TX Reference Phase Check number 2

AUD_SYNC_BT_PHASE_CHK_REF2

Bits	Name	Description
31:0	COUNTER	Snapshot of strobe counter

0x2800942C AUD_SYNC_BT_COUNT_LOAD_XO2

Type: Read/write
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

pBT TX SCO sample counter load

AUD_SYNC_BT_COUNT_LOAD_XO2

Bits	Name	Description
31:0	COUNT	Writing to this register causes the contents of this register to be loaded into the BT SCO TX sample counter number 1.

0x28009430 AUD_SYNC_BT_COUNT_LOAD_REF2

Type: Read/write
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

BT SCO TX strobe counter load.p

AUD_SYNC_BT_COUNT_LOAD_REF2

Bits	Name	Description
31:0	COUNT	Writing to this register causes the contents of this register to be loaded into the BT SCO TX strobe counter.number 1.

0x28009434 AUD_SYNC_FM_REF_INC

Type: Read/write
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

AUD_SYNC_FM_REF_INC

Bits	Name	Description
31:16	RESERVED	RESERVED
15:0	REF_INC1	Number of samples strobe counter is incremented each timef for FM

0x28009438 AUD_SYNC_FM_XO_DIV_MOD

Type: Read/write
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

FM L and M Register

AUD_SYNC_FM_XO_DIV_MOD

Bits	Name	Description
27:16	L	This is the integer portion.
11:0	M	This is the fractional portion.

0x2800943C AUD_SYNC_FM_PHASE_CHK_XO

Type: Read
Clock: LCC_RES_XCLK
Reset State: 0x00000000

FM XO Phase Check

AUD_SYNC_FM_PHASE_CHK_XO

Bits	Name	Description
31:0	COUNTER	Snapshot of sample counter

0x28009440 AUD_SYNC_FM_PHASE_CHK_REF

Type: Read
Clock: LCC_RES_XCLK
Reset State: 0x00000000

FM Reference Phase Check

AUD_SYNC_FM_PHASE_CHK_REF

Bits	Name	Description
31:0	COUNTER	Snapshot of strobe counter

0x28009444 AUD_SYNC_FM_VFR_TIMESTAMP

Type: Read
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

FM VFR Timestamp.

AUD_SYNC_FM_VFR_TIMESTAMP

Bits	Name	Description
31:0	TIMESTAMP	Adjusted value of sample counter

0x28009448 AUD_SYNC_FM_COUNT_LOAD_XO

Type: Read/write
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

FM sample counter load.

AUD_SYNC_FM_COUNT_LOAD_XO

Bits	Name	Description
31:0	COUNT	Writing to this register loads the FM sample counter.

0x2800944C AUD_SYNC_FM_COUNT_LOAD_REF

Type: Read/write
Clock: LCC_AVS_XCLK
Reset State: 0x00000000

FM strobe counter load.

AUD_SYNC_FM_COUNT_LOAD_REF

Bits	Name	Description
31:0	COUNT	Writing to this register loads the FM strobe counter.

12.3 LPA SS M2VMT Registers (0x28002000 LPASS_M2VMT_BASE)

This section contains the Low Power Audio Subsystem (LPASS) M2MVT registers.

12.3.1 M2VMT VMID mapping registers

0x28002000+ 0x4*n LPASS_M2VMT_M2VMRn

Type: Read/Write
Clock: CRIF_BUS_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where n = NUM_M2VMT_ENTRIES from the design generics

LPASS_M2VMT_M2VMRn

Bits	Name	Description
31:5	RESERVED	n = NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRn address associations. For the tables of the size of non power of 2, there will be undefined/unmapped entries and such entities will be set to 'zero' value. In other word, when such entities are accessed, vmid will always be set to zero.

12.3.2 M2VMT configuration registers

0x28002F80 LPASS_M2VMT_CR

Type: Read/Write
Clock: CRIF_BUS_CLOCK
Reset State: xxx0

Global configuration register.

NOTE When REMOVE_M2VMT_RPU = '1', this register is not available. Also, bit [2], is not valid or has no effect when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT ='1'.

LPASS_M2VMT_CR

Bits	Name	Description
31:4	RESERVED	
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., in valid addresses) are recorded as such. Decode error is asserted when config access to un-implemented and/or unmapped register/address are done. Also, note that decode error is never asserted for client port accesses. When value is set to '0' i.e., 'do not record', decode errors do not set the M2VMT_ESR[CFG], and M2VMT_EAR & M2VMT_SYNRn is not updated. When value is set to '1', i.e., 'record', decode errors set M2VMT_ESR[CFG] and M2VMT_EAR & M2VMT_SYNRn is updated with the address and the syndrome of the error. Reset State: x
2	RPUEIE	RPU error interrupt Enable: When set, configuration port errors are reported directly to the interrupt controller via the M2VMT_intr, interrupt output signal. Interrupt output is asserted if M2VMT_CR[RPUIE_EN] is '1' and ANY bit is set in the M2VMT_ESR register. **NOTE** Not valid or has no effect on the interrupt when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT='1' Reset State: x
1	RPUERE	RPU error report enable: When set, M2VMT reports configuration port errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via CRIF port will use a decode error, rather than a slave error. Regardless of the value of this field, both configuration port errors are terminated by the M2VMT as RAZ/WI, and are recorded in M2VMT_ESR register. **NOTE** Current design does not support the configurable slave error responses, therefore, effect of this bit is similar to RPUE. Reset State: X
0	RPUE	RPU Enable: Governs whether M2VMT_RPU_ACR is enabled to check the VMID of the configuration request. When set, all configuration port accesses are checked against M2VMT_RPU_ACR register for access permissions. It's cleared by reset. Set once SROT configures MID->VMID mapping tables Reset State: 0

12.3.3 M2VMT error report registers

0x28002F84 LPASS_M2VMT_EAR

Type: Read/Write
Clock: CRIF_BUS_CLOCK
Reset State: unknown

When there is an error, this register holds the physical address of the errant transaction.

LPASS_M2VMT_EAR

Bits	Name	Description
31:0	PA	M2VMT Error Address Register: Physical address[31:0]. Contains the physical address of the errant request. Based on implementation, it may not contain the full 32 bits of the address. Captures the address on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT = '1', this register is not available and therefore access to this register are treated as RAZ/WI.

0x28002F88 LPASS_M2VMT_ESR

Type: Read/Write to clear
Clock: CRIF_BUS_CLOCK
Reset State: Undefined

M2VMT Error Status Register:

Captures the status upon M2VMT configuration errors, as determined by the M2VMT_RPU_ACR.

This register has read/write-clear access, meaning that reads simply provide a value in the register, while writes are performed by clearing those bits corresponding to '1's in the value written data, and leaving unchanged those bits corresponding to 0s n the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old error. A write with a '1' set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

The presence of an asserted value on any bit in this register is what prompts the assertion when enabled by M2VMT_CR[RPUEIE] of the M2MVT's interrupt output. Therefore these bits must be cleared by the interrupt handler. This is contrasted with the fields in the M2VMT_ESYNRn register, which are merely the 'syndrome' of an error indicated by the M2VMT_ESR.

For M2VMT, there is only one defined error status bit in the M2VMT_SER (actually two counting multi-error).

LPASS_M2VMT_ESR

Bits	Name	Description
31	MULTI	Multi-Error: When set to '1', indicates that an additional error occurred while M2VMT_ESR is non-zero. The M2VMT_EAR,M2VMT_ESYNRn and M2VMT_ESR registers (with the exception of this bit) lock on the first error, and must be cleared to unlock. Therefore, the status and the syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., syndrome register and status register stores details of only the first error. **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this register is treated as RAZ/WI.
30:1	RESERVED	
0	CFG	Configuration Port Error: When set to '1', indicates an error associated with a configuration port request.

0x28002F8C LPASS_M2VMT_ESRRESTORE

Type: Write Only/reads ignored
Clock: CRIF_BUS_CLOCK
Reset State: unknown

LPASS_M2VMT_ESRRESTORE

Bits	Name	Description
31:0	M2VMT_ESRRTORE	M2VMT Error Status Register Restore This is just an aliased address for M2VMT_ESR, which provides direct write access (rather than write-clear) for restoration purpose **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this register is treated as RAZ/WI.

0x28002F90 LPASS_M2VMT_ESYNR0

Type: Read/Write
Clock: CRIF_BUS_CLOCK
Reset State: undefined

Error Syndrome Register 0:

Captures the syndrome on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) 'lock' upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., the syndrome register and the status register stores details of only the first error.

LPASS_M2VMT_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request. **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT="1", this register is not available and therefore access to this register is treated as RAZ/WI.
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request.
15:0	AMID	AMID[15:0] field of errant request.

0x28002F94 LPASS_M2VMT_ESYNR1

Type: Read/Write
Clock: CRIF_BUS_CLOCK
Reset State: Undefined

Error Syndrome Register 1:

Captures syndrome upon M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) 'lock' upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., the syndrome register and the status register stores details of only the first error.

LPASS_M2VMT_ESYNR1

Bits	Name	Description
31	DCD	Decode: Indicates configuration port error due to invalid/ unrecognized/ unmapped/ un-implemented address (e.g., a reserved register address). Includes decode errors within the global address space. Also, note that decode error is never asserted for client port accesses. **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this registers is treated as RAZ/WI.

LPASS_M2VMT_ESYNR1 (cont.)

Bits	Name	Description
30	AC	Access control: Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	AOOOWR	AOOOWR field of the errant request
22	AOOORD	AOOORD field of the errant request.
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request).
19	RESERVED_2	
18:16	ASIZE	ASIZE[2:0] field of the errant request).
15:12	ALEN	ALEN[3:0] field of the errant request.
11:10	ABURST	ABURST[1:0] field of the errant request.
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request.
7	AINST	AINST field of the errant request.
6	APROTNS	APROTNS field of the errant request.
5	APRIV	APRIV field of the errant request.
4	AINNERSHARED	AINNERSHARED field of the errant request.
3	ASHARED	ASHARED field of the errant request.
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

12.3.4 M2VMT revision register

0x28002FF4 LPASS_M2VMT_REV

Type: Read
Clock: CRIF_BUS_CLOCK
Reset State: 0x00000010

Reports the revision information for the M2VMT core and wrapper.

LPASS_M2VMT_REV

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	Major variant field

LPASS_M2VMT_REV (cont.)

Bits	Name	Description
3:0	MINOR	Minor variant field.

12.3.5 M2VMT implementation parameter register

0x28002FF8 LPASS_M2VMT_IDR

Type: Read
Clock: CRIF_BUS_CLOCK
Reset State: 0x00000001

Reports the size of the M2VMT table. It is a read-only register.

LPASS_M2VMT_IDR

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.
8:0	M2VMTSIZE	.M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x28002FFC LPASS_M2VMT_RPU_ACR

Type: Read/Write
Clock: CRIF_BUS_CLOCK
Reset State: Undefined

Using the incoming VMID, this register controls access to the global register space.

LPASS_M2VMT_RPU_ACR

Bits	Name	Description
31:0	RWE	M2VMT local RPU Access control Register. Each bit position corresponds to a VMID. When set to ’1’, that VMID is granted VMID read/write access to the entire block of registers within the M2VMT’s 4KB global address space, including this register itself. In practice, this register designates the VMID(s) that can act as SROT (e.g., scorpion-secure) or pseudo SROT (e.g., RPM ARM11). **NOTE** When REMOVE_M2VMT_RPU=’1’, this register is not available and therefore access to this register is treated as RAZ/WI.

12.4 LPA SS Q6 SS M2VMT Registers (0x28003000 LPASS_M2VMT_Q6SS_BASE)

This section contains the Low Power Audio Subsystem (LPASS) Q6SS M2MVT registers.

12.4.1 M2VMT VMID mapping register

0x28003000+ 0x4*n Q6SS_M2VMT_M2VMRn

Type: Read/Write
Clock: CRIF_BUS_CLOCK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where n = NUM_M2VMT_ENTRIES from the design generics

Q6SS_M2VMT_M2VMRn

Bits	Name	Description
31:5	RESERVED	n = NUM_M2VMT_ENTRIES from the design generic/parameter.
4:0	VMID	Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRn address associations. For the tables of the size of non power of 2, there will be undefined/unmapped entries and such entities will be set to 'zero' value. In other word, when such entities are accessed, vmid will always be set to zero.

12.4.2 M2VMT configuration registers

0x28003F80 Q6SS_M2VMT_CR

Type: Read/Write
Clock: CRIF_BUS_CLOCK
Reset State: xxx0

Global configuration register.

NOTE When REMOVE_M2VMT_RPU = '1', this register is not available. Also, bit [2], is not valid or has no effect when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT ='1'.

Q6SS_M2VMT_CR

Bits	Name	Description
31:4	RESERVED	
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., in valid addresses) are recorded as such. Decode error is asserted when config access to un-implemented and/or unmapped register/address are done. Also, note that decode error is never asserted for client port accesses. When value is set to ’0’ i.e., ’do not record’, decode errors do not set the M2VMT_ESR[CFG], and M2VMT_EAR & M2VMT_SYNRn is not updated. When value is set to ’1’, i.e., ’record’, decode errors set M2VMT_ESR[CFG] and M2VMT_EAR & M2VMT_SYNRn is updated with the address and the syndrome of the error. Reset State: x
2	RPUEIE	RPU error interrupt Enable: When set, configuration port errors are reported directly to the interrupt controller via the M2VMT_intr, interrupt output signal. Interrupt output is asserted if M2VMT_CR[RPUIE_EN] is ’1’ and ANY bit is set in the M2VMT_ESR register. **Note**: Not valid or has no effect on the interrupt when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT=’1’. Reset State: x
1	RPUERE	RPU error report enable: When set, M2VMT reports configuration port errors to the requesting bus master, according to the respective port’s bus protocol. All error types reported via CRIF port will use a decode error, rather than a slave error. Regardless of the value of this field, both configuration port errors are terminated by the M2VMT as RAZ/WI, and are recorded in M2VMT_ESR register. **NOTE** Current design does not support the configurable slave error responses, therefore, effect of this bit is similar to RPUE. Reset State: X
0	RPUE	RPU Enable: Governs whether M2VMT_RPU_ACR is enabled to check the VMID of the configuration request. When set, all configuration port accesses are checked against M2VMT_RPU_ACR register for access permissions. It’s cleared by reset. Set once SROT configures MID->VMID mapping tables Reset State: 0

12.4.3 M2VMT error report registers

0x28003F84 Q6SS_M2VMT_EAR

Type: Read/Write
Clock: CRIF_BUS_CLOCK
Reset State: unknown

When there is an error, this register holds the physical address of the errant transaction.

Q6SS_M2VMT_EAR

Bits	Name	Description
31:0	PA	M2VMT Error Address Register: Physical address[31:0]. Contains the physical address of the errant request. Based on implementation, it may not contain the full 32 bits of the address. Captures the address on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT = '1', this register is not available and therefore access to this register are treated as RAZ/WI.

0x28003F88 Q6SS_M2VMT_ESR

Type: Read/Write to clear
Clock: CRIF_BUS_CLOCK
Reset State: Undefined

M2VMT Error Status Register:

Captures the status upon M2VMT configuration errors, as determined by the M2VMT_RPU_ACR.

This register has read/write-clear access, meaning that reads simply provide a value in the register, while writes are performed by clearing those bits corresponding to '1's in the value written data, and leaving unchanged those bits corresponding to 0s n the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old error. A write with a '1' set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

The presence of an asserted value on any bit in this register is what prompts the assertion when enabled by M2VMT_CR[RPUEIE] of the M2MVT's interrupt output. Therefore these bits must be cleared by the interrupt handler. This is contrasted with the fields in the M2VMT_ESYNRn register, which are merely the 'syndrome' of an error indicated by the M2VMT_ESR.

For M2VMT, there is only one defined error status bit in the M2VMT_SER (actually two, if you count multi-error).

Q6SS_M2VMT_ESR

Bits	Name	Description
31	MULTI	Multi-Error: When set to ’1’, indicates that an additional error occurred while M2VMT_ESR is non-zero. The M2VMT_EAR,M2VMT_ESYNRn and M2VMT_ESR registers (with the exception of this bit) lock on the first error, and must be cleared to unlock. Therefore, the status and the syndrome of errors that occurred while M2VMT_ESR[CFG] is ’1’ are lost., ie., syndrome register and status register stores details of only the first error. **NOTE** When REMOVE_M2VMT_RPU=’1’ OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT=’1’, this register is not available and therefore access to this register is treated as RAZ/WI.
30:1	RESERVED	
0	CFG	Configuration Port Error: When set to ’1’, indicates an error associated with a configuration port request.

0x28003F8C Q6SS_M2VMT_ESRRESTORE

Type: Write Only/reads ignored
Clock: CRIF_BUS_CLOCK
Reset State: unknown

Q6SS_M2VMT_ESRRESTORE

Bits	Name	Description
31:0	M2VMT_ESRRTORE	M2VMT Error Status Register Restore This is just an aliased address for M2VMT_ESR, which provides direct write access (rather than write-clear) for restoration purpose **NOTE** When REMOVE_M2VMT_RPU=’1’ OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT=’1’, this register is not available and therefore access to this register is treated as RAZ/WI.

0x28003F90 Q6SS_M2VMT_ESYNR0

Type: Read/Write
Clock: CRIF_BUS_CLOCK
Reset State: undefined

Error Syndrome Register 0:

Captures the syndrome on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) 'lock' upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., the syndrome register and the status register stores details of only the first error.

Q6SS_M2VMT_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request. **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT="1", this register is not available and therefore access to this register is treated as RAZ/WI.
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request.
15:0	AMID	AMID[15:0] field of errant request.

0x28003F94 Q6SS_M2VMT_ESYNR1

Type: Read/Write
Clock: CRIF_BUS_CLOCK
Reset State: Undefined

Error Syndrome Register 1:

Captures syndrome upon M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) 'lock' upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., the syndrome register and the status register stores details of only the first error.

Q6SS_M2VMT_ESYNR1

Bits	Name	Description
31	DCD	Decode: Indicates configuration port error due to invalid/ unrecognized/ unmapped/ un-implemented address (e.g., a reserved register address). Includes decode errors within the global address space. Also, note that decode error is never asserted for client port accesses. **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this registers is treated as RAZ/WI.

Q6SS_M2VMT_ESYNR1 (cont.)

Bits	Name	Description
30	AC	Access control: Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	AOOOWR	AOOOWR field of the errant request
22	AOOORD	AOOORD field of the errant request.
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request).
19	RESERVED_2	
18:16	ASIZE	ASIZE[2:0] field of the errant request).
15:12	ALEN	ALEN[3:0] field of the errant request.
11:10	ABURST	ABURST[1:0] field of the errant request.
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request.
7	AINST	AINST field of the errant request.
6	APROTNS	APROTNS field of the errant request.
5	APRIV	APRIV field of the errant request.
4	AINNERSHARED	AINNERSHARED field of the errant request.
3	ASHARED	ASHARED field of the errant request.
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

12.4.4 M2VMT revision register

0x28003FF4 Q6SS_M2VMT_REV

Type: Read
Clock: CRIF_BUS_CLOCK
Reset State: 0x00000010

Reports the revision information for the M2VMT core and wrapper.

Q6SS_M2VMT_REV

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	Major variant field

Q6SS_M2VMT_REV (cont.)

Bits	Name	Description
3:0	MINOR	Minor variant field.

12.4.5 M2VMT implementation parameter register

0x28003FF8 Q6SS_M2VMT_IDR

Type: Read
Clock: CRIF_BUS_CLOCK
Reset State: 0x00000001

Reports the size of the M2VMT table. It is a read-only register.

Q6SS_M2VMT_IDR

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.
8:0	M2VMTSIZE	.M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x28003FFC Q6SS_M2VMT_RPU_ACR

Type: Read/Write
Clock: CRIF_BUS_CLOCK
Reset State: Undefined

Using the incoming VMID, this register controls access to the global register space.

Q6SS_M2VMT_RPU_ACR

Bits	Name	Description
31:0	RWE	M2VMT local RPU Access control Register. Each bit position corresponds to a VMID. When set to ’1’, that VMID is granted VMID read/write access to the entire block of registers within the M2VMT’s 4KB global address space, including this register itself. In practice, this register designates the VMID(s) that can act as SROT (e.g., scorpion-secure) or pseudo SROT (e.g., RPM ARM11). **NOTE** When REMOVE_M2VMT_RPU=’1’, this register is not available and therefore access to this register is treated as RAZ/WI.

12.5 LPA SS AHBTM Registers (0x2800A000 LPASS_AHBTM_BASE)

This section contains the Low Power Audio Subsystem (LPASS) AHBTM registers.

12.5.1 LPASS AHMTM Configuration registers

0x2800A000 LPASS_AHBTM_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The AHBTM_CFG register configures the following:

LPASS_AHBTM_CFG

Bits	Name	Description
29:31	UNUSED_1	
28	RESERVED_BIT28	
27:1	UNUSED_2	
0	CGC_CLK_ENA	0x0: No clock running 0x1: Clock enabled

0x2800A020+ 0x20*n LPASS_AHBTM_Cn_CFG0, n=[0..7]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The AHBTM_Cn_CFG0 register configures the following:

LPASS_AHBTM_Cn_CFG0

Bits	Name	Description
31:28	PORT_SELECT	Identifies which AHB port the monitor should be observing

0x2800A024+ 0x20*n LPASS_AHBTM_Cn_CFG1, n=[0..7]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The AHBTM_Cn_CFG1 register configures the following:

LPASS_AHBTM_Cn_CFG1

Bits	Name	Description
20	SEQ_ADDR_ENA	Setting (1) this bit enables the Sequential Address state checking in the enable logic of the counter. On reset this bit is initialized to 0.
18	HMASTLOCK_ENA	Setting (1) this bit enables the HMASTLOCK state checking in the enable logic of the counter. On reset this bit is initialized to 0.
17	HWRITE_ENA	Setting (1) this bit enables the HWRITE state checking in the enable logic of the counter. On reset this bit is initialized to 0.
16	HREADY_ENA	Setting (1) this bit enables the HREADY state checking in the enable logic of the counter. On reset this bit is initialized to 0.
15	HBURST_ENA	Setting (1) this bit enables the HBURST state checking in the enable logic of the counter. On reset this bit is initialized to 0.
14	HTRANS_ENA	Setting (1) this bit enables the HTRANS state checking in the enable logic of the counter. On reset this bit is initialized to 0.
13	HSIZE_ENA	Setting (1) this bit enables the HSIZE state checking in the enable logic of the counter. On reset this bit is initialized to 0.
12	HRESP_ENA	Setting (1) this bit enables the HRESP state checking in the enable logic of the counter. On reset this bit is initialized to 0.
9	HPROT_ENA	Setting (1) this bit enables the HPROT state checking in the enable logic of the counter. On reset this bit is initialized to 0.
8	HSEL_ENA	Setting (1) this bit enables the HSEL state checking in the enable logic of the counter. On reset this bit is initialized to 0.
4	HADDR_ENA	Setting (1) this bit enables the HADDR state checking in the enable logic of the counter. On reset this bit is initialized to 0.
1	MSTR_GNT_ENA	Setting (1) this bit enables the MSTR_GNTstate checking in the enable logic of the counter. On reset this bit is initialized to 0.
0	ARB_LAT_ENA	Setting (1) this bit enables the ARB_LAT state checking in the enable logic of the counter. On reset this bit is initialized to 0.

0x2800A028+0x20*n LPASS_AHBTM_Cn_CFG2, n=[0..7]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The AHBTM_Cn_CFG2 register configures the following:

LPASS_AHBTM_Cn_CFG2

Bits	Name	Description
8	HMASTLOCK_VAL	Value used in the match circuit.
4	HWRITE_VAL	Value used in the match circuit.
0	HREADY_VAL	Value used in the match circuit.

0x2800A02C+0x20*n LPASS_AHBTM_Cn_CFG3, n=[0..7]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The AHBTM_Cn_CFG3 register configures the following:

LPASS_AHBTM_Cn_CFG3

Bits	Name	Description
30:28	HBURST_MASK	Setting (1) these bits masks off the corresponding bit in the VAL register prior to being used in the match circuit.
27	HBURST_INV	Setting (1) this bit inverts the match circuit output to provide the ability to disable the counter when a match occurs.
26:24	HBURST_VAL	Value used in the match circuit.
22:20	HTRANS_MASK	Setting (1) these bits masks off the corresponding bit in the VAL register prior to being used in the match circuit.
19	HTRANS_INV	Setting (1) this bit inverts the match circuit output to provide the ability to disable the counter when a match occurs.
18:16	HTRANS_VAL	Value used in the match circuit.
14:12	HSIZE_MASK	Setting (1) these bits masks off the corresponding bit in the VAL register prior to being used in the match circuit.
11	HSIZE_INV	Setting (1) this bit inverts the match circuit output to provide the ability to disable the counter when a match occurs.
10:8	HSIZE_VAL	Value used in the match circuit.
6:4	HRESP_MASK	Setting (1) these bits masks off the corresponding bit in the VAL register prior to being used in the match circuit.

LPASS_AHBTM_Cn_CFG3 (cont.)

Bits	Name	Description
3	HRESP_INV	Setting (1) this bit inverts the match circuit output to provide the ability to disable the counter when a match occurs.
2:0	HRESP_VAL	Value used in the match circuit.

0x2800A030+ 0x20*n LPASS_AHBTM_Cn_CFG4, n=[0..7]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The AHBTM_Cn_CFG4 register configures the following:

LPASS_AHBTM_Cn_CFG4

Bits	Name	Description
27:24	HPROT_MASK	Setting (1) this bit masks off the corresponding bit in the VAL register prior to being used in the match circuit.
20	HPROT_INV	Setting (1) this bit inverts the match circuit output to provide the ability to disable the counter when a match occurs.
19:16	HPROT_VAL	Value used in the match circuit.
11:4	HSEL_MASK	Setting (1) this bit masks off the corresponding bit in the VAL register prior to being used in the match circuit.
0	HSEL_VAL	Value used in the match circuit.

0x2800A034+ 0x20*n LPASS_AHBTM_Cn_CFG5, n=[0..7]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The AHBTM_Cn_CFG5 register configures the following:

LPASS_AHBTM_Cn_CFG5

Bits	Name	Description
28	HADDR_INV	Setting (1) this bit inverts the match circuit output to provide the ability to disable the counter when a match occurs.
27:8	HADDR_VAL	Value used in the match circuit.
7:0	HADDR_MASK	Setting (1) this bit masks off the corresponding bit (7->15...0->8) in the VAL register prior to being used in the match circuit.

0x2800A038+ 0x20*n LPASS_AHBTM_Cn_CFG6, n=[0..7]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The AHBTM_Cn_CFG6 register configures the following:

LPASS_AHBTM_Cn_CFG6

Bits	Name	Description
27:20	MSTR_GNT_MASK	Setting (1) these bits masks off the corresponding bits being used in the match circuit. When set = 0xFF this disables the MSTR_GNT state checking from the enable logic of the counter
16	MSTR_GNT_VAL	Value used in the match circuit.
11:4	ARB_LAT_MASK	Setting (1) these bits masks off the corresponding bits being used in the match circuit. When set = 0xFF this disables the ARB_LAT state checking from the enable logic of the counter
0	ARB_LAT_VAL	Value used in the match circuit.

12.6 LPA SS SLIM Bus Registers (0x28080000 LPASS_SLIMBUS_BASE)

This section contains the Low Power Audio Subsystem (LPASS) SLIMBus registers.

12.6.1 Component registers

0x28080000 LPASS_SB_COMP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

1. Enable for the entire component

LPASS_SB_COMP_CFG

Bits	Name	Description
31:1	RESERVED	
0	ENABLE	If set, enables the entire component

0x28080004 LPASS_SB_SW_RESET

Type: Write
Clock: HCLK
Reset State: 0x00000000

A Write to this register resets the whole SLIMBus component. The write data accompanying the write is ignored.

LPASS_SB_SW_RESET

Bits	Name	Description
31:0	RESERVED31_0	Reserved.

0x28080008 LPASS_SB_COMP_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_COMP_STATUS

Bits	Name	Description
31:0	RESERVED	reserved

0x2808000C LPASS_SB_COMP_TEST

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

Setting a INT_EE* bit of this register asserts interrupt for that EE. Clearing that bit again clears that interrupt. This is mainly for testing interrupt connectivity of a component at chip top without a functional test.

LPASS_SB_COMP_TEST

Bits	Name	Description
6:4	SB_TESTBUS_SEL	0x0: select intf def testbus 0x1: select frm def testbus 0x2: select mgr def testbus 0x3: select pgd def testbus 0x4: select ngd1 def testbus 0x5: select ngd2 def testbus 0x6: select mp testbus 0x7: select frame layer testbus
3	SB_TESTBUS_EN	If set, the debug bus is driven actively by the SLIMbus component.
2	INT_EE2	
1	INT_EE1	
0	INT_EE0	Assert interrupt for EE (EE0) if set, de-assert the interrupt if cleared.

0x28080010 LPASS_SB_COMP_DEBUG

Type: Read
Clock: HCLK
Reset State: 0x00000000

Mainly for testing/debug.

LPASS_SB_COMP_DEBUG

Bits	Name	Description
0	TBD	Tbd

0x28080014 LPASS_SB_COMP_TRUST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

NOTE Note the very consistent device interrupts found in: SB_MGR_INT_*, SB_FRM_INT_*, SB_INTF_INT_*, SB_NGD1_INT_*, SB_NGD2_INT_*, SB_NGD3_INT_*, and SB_PGD_DEV_INT_*. This register provides a means of routing same to one of the available EE's.

LPASS_SB_COMP_TRUST_CFG

Bits	Name	Description
11:10	EE_FOR_MGR_RSRC_GRP	EE value (i.e., 0,1,2,3) for the Manager resource group containing Manager, Framer and Interface and PGD* Devices. Used to route device interrupts from this group to the programmed EE.
9:8	EE_FOR_NGD1	EE value for NGD1 - to route NGD1 interrupts
7:6	EE_FOR_NGD2	EE value for NGD2 - to route NGD1 interrupts
5	HALD_MGR_MSG_TX	Prevents MGR from sending out any SLIMbus message to the trusted device
4	HALT_NGD2_MSG_TX	Prevents NGD2 from sending out any SLIMbus message to the trusted device
3	HALT_NGD1_MSG_TX	Prevents NGD1 from sending out any SLIMbus message to the trusted device
2	HALT_EN_CHANGE	Blocks changes to EN bit of all devices in the component.
1	HALT_SW_RESET	
0	HALT_RECONFIG	Blocks Reconfig messages from being sent or executed if received.

0x28080018 LPASS_SB_COMP_TRUST_DEV1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_COMP_TRUST_DEV1

Bits	Name	Description
31:16	TRUSTED_EA_MSB	MSB Bits 47:32 of the EA of the trusted device whose LA should be assigned as above
15:8	TRUSTED_LA	LA of the Trusted Device. Used by NGDs as well if HALT_NGD*_MSG_TX bit is set.

LPASS_SB_COMP_TRUST_DEV1 (cont.)

Bits	Name	Description
7:1	RESERVED	
0	TRUST_DEV_EN	Enables the Manager to monitor for said Trusted device access

0x2808001C LPASS_SB_COMP_TRUST_DEV2

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_COMP_TRUST_DEV2

Bits	Name	Description
31:0	TRUSTED_EA_LSB	LSB Bits 31:0 of the EA of the trusted device whose LA should be assigned as above

12.6.2 Manager Device Registers

0x28080200 LPASS_SB_MGR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_MGR_CFG

Bits	Name	Description
3	TX_MSGQ_EN_LOW	
2	TX_MSGQ_EN_HIGH	
1	RX_MSGQ_EN	
0	ENABLE	

0x28080204 LPASS_SB_MGR_STATUS

Type: Read
Clock: HCLK
Reset State: 0x0000000U

LPASS_SB_MGR_STATUS

Bits	Name	Description
23:17	NACKED_TX_MSG_MC	Read Only. The MC of the TX msg that was nacked by the destination twice or the MC of the invalid message depending on which intr bit is set.
16:10	ACKED_TX_MSG_MC	Read Only. The MC of the latest TX msg from the msg queues that was positively acked by the destination.
9:8	ERROR	Read only. Two bits holding any error conditions that the device may want to report. Valid only if DEV_ERR intr bit is set
7:2	PIPE_NUM_OFFSET	This field is the pipe to which the RxQ of the Manager is connected to. The TxL and TxH are connected to pipe with numbers PIPE_NUM_OFFSET+1, PIPE_NUM_OFFSET+2 respectively
1	ENUMERATED	If set, the device has been enumerated.
0	TX_MSG_BUFFER_BUSY	If set, then the Tx Msg Buffer has a message waiting to be sent out. Hence the direct access should not be used until this bit is a 0 again. Its recommended to wait for the enumerated bit to get set before polling this bit. Should not be used as a check for txmsg sent.

0x28080208 LPASS_SB_MGR_RX_MSGQ_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The fields that control the RX message queue (i.e., producer queue).

LPASS_SB_MGR_RX_MSGQ_CFG

Bits	Name	Description
31:16	TIME_OUT_VAL	TIme out counter enabled if this field is non zero and when the first message is received. Time out cntr reset after every Rx msg received, If next Rx message not received before it expires, a trans_end is automatically generated even if BLOCK_SIZE/TRANS_SIZE is not got. Specified in terms of AHB Bus clock cycles given to the core by the ClockCtrl of SoC.
15:8	TRANS_SIZE	Specified in units of messages. After receiving that many a trans_end is asserted.
7:0	BLOCK_SIZE	Specified in units of messages. After receiving this many, a block_end is asserted. SW can leave this 0 in system producer mode to prevent block_end assertion.

0x28080210 LPASS_SB_MGR_INT_EN

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_MGR_INT_EN

Bits	Name	Description
31	TX_MSG_SENT	If queue is not enabled, this bit is set When a message written to TX_MSG reg is sent out. If queue is enabled, this bit is set when last TX msg of the current transaction is sent out.
30	RX_MSG_RCVD	When a message has been received in the RX_MSG registers.Honoured only if RX Q is disabled.
29	DEV_ERR	Device reported error. See status register for details.
28	IE_VE_CHANGE	An IE or VE has changed its value.
27	INVALID_TX_MSG	An invalid TX message not allowed for this device is written into the Tx buffer.
26	TX_MSG_BUF_CONTENTIO N	If enabled, this generates an interrupt whenever SW (through direct AHB access) tries to write to an tx buffer that is not available for SW.
25	TX_MSG_NACKED_TWICE	A TX msg was nacked twice by destination.
24	RECONFIG_DONE	After successfully sending a RECONFIG_NOW command

0x28080214 LPASS_SB_MGR_INT_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

Status of interrupt elements mentioned in the MSG_INT_EN register.

LPASS_SB_MGR_INT_STATUS

Bits	Name	Description
31	TX_MSG_SENT	
30	RX_MSG_RCVD	
29	DEV_ERR	
28	IE_VE_CHANGE	
27	INVALID_TX_MSG	
26	TX_MSG_BUF_CONTENTIO N	

LPASS_SB_MGR_INT_STATUS (cont.)

Bits	Name	Description
25	TX_MSG_NACKED_TWICE	.
24	RECONFIG_DONE	

0x28080218 LPASS_SB_MGR_INT_CLR

Type: Write
Clock: HCLK
Reset State: 0x00000000

Interrupt clear for the listed interrupt events.

LPASS_SB_MGR_INT_CLR

Bits	Name	Description
31	TX_MSG_SENT	
30	RX_MSG_RCVD	
29	DEV_ERR	
28	IE_VE_CHANGE	
27	INVALID_TX_MSG	
26	TX_MSG_BUF_CONTENTION	
25	TX_MSG_NACKED_TWICE	
24	RECONFIG_DONE	

0x28080230+4*n LPASS_SB_MGR_TX_MSGn, n=[0..9]

Type: Write
Clock: HCLK
Reset State: 0x00000000

SW uses these registers for Direct Access Tx Message sending over SLIMbus. These hold the TX message to be sent (40bytes max).

CAUTION This Direct access Messaging registers SHOULD NOT be used if any of the Tx queues are enabled. The resulting behavior is not defined.

LPASS_SB_MGR_TX_MSGn

Bits	Name	Description
31:0	MSGVAL	message contents

0x28080270+4*n LPASS_SB_MGR_RX_MSGn, n=[0..9]

Type: Read
Clock: HCLK
Reset State: 0x00000000

SW uses these registers for Direct Access Rx Message receiving over SLIMbus. These hold the RX message received and waiting for SW to consume(40bytes max).

CAUTION This Direct access Messaging registers SHOULD NOT be used if the Rx queue is enabled. The resulting behavior is not defined.

LPASS_SB_MGR_RX_MSGn

Bits	Name	Description
31:0	MSGVAL	message contents

0x280802F0 LPASS_SB_MGR_IE_STATUS

Type: Read
Clock: HCLK
Reset State: 0xFF010000

Holds status of IE elements listed out in spec.

LPASS_SB_MGR_IE_STATUS

Bits	Name	Description
31:24	DEV_CLASS_CODE	
23:16	DEV_CLASS_VER	
15:4	RESERVED_15_4	reserved
3	EX_ERROR	
2	RECONFIG_OBJ	
1	RESERVED	reserved
0	UNSPRTD_MSG	unsupported msg

0x28080300 LPASS_SB_MGR_VE_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

Place Holder.

LPASS_SB_MGR_VE_STATUS

Bits	Name	Description
31:0	VE_VAL	presently reads all 0's

Framer Device Registers

0x28080400 LPASS_SB_FRM_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_FRM_CFG

Bits	Name	Description
25	SEL_INTFB_CAPTURE_CLK	When 1, the intfb clk is chosen as capture clock When 0, the ext clk is chosen as capture clock
24:22	CDL_TIMEOUT	Number of superframes that Active framer stays in checking DataLine state before timing out and returning to Undefined state. When timeout value of 0 is provided, timeout functionality is disabled. If Framer times out before exiting CheckingDataLine state, a timeout interrupt is triggered. Refer section 10.1.1.2 of SLIMbus spec v 1.01.01 for more details on CheckingDataLine state. See http://www.mipi.org/specifications/serial-low-power-inter-chip-media-bus-slimbussm-specification
21:20	CLK_QUALITY	Encoded as specified in Table 76 of SLIMbus spec v 1.01.01
19	INTERNAL_WAKEUP_EN	When set, allows devices within component to wakeup framer when in idle mode.
18:15	REFERENCE_CLK_CG	The equivalent CG of the SLIMbus Reference CLK
14:11	BOOT_ROOT_FREQ	The Boot value of RF used by Framer if defined as the active one
10:7	BOOT_CLOCK_GEAR	The Boot value of CG used by Framer if defined as the active one
6:2	BOOT_SUBFRAME_MODE	The Boot value of SM used by Framer if defined as the active one

LPASS_SB_FRM_CFG (cont.)

Bits	Name	Description
1	BOOT_AS_ACTIVE_FRAMER	If set, this Framer Device is made the active one in the bus. This setting takes effect only when bus is booting up. Any subsequent changes to this bit has no effect until bus re-boots again.
0	ENABLE	If enabled it will be the active Framer and will start booting the bus, when component is also enabled.

0x28080404 LPASS_SB_FRM_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_FRM_STATUS

Bits	Name	Description
31:27	RESERVED	
26:19	DEV_LA	Assigned logical address of device. Only valid when enumerated.
18	ENUMERATED	When set, device is enumerated and has been assigned a logical address
17	IDLE_MODE	When set, framer is in idle mode and must be woken up by one of the defined wake-up methods.
16	ACTIVE_FRAMER	Read only. When set, component is active framer.
15:12	CUR_ROOT_FREQUENCY	
11:8	CUR_CLOCK_GEAR	
7:6	ERROR	Read only. Two bits holding any error conditions that the device may want to report. Valid only if FRM DEV_ERR bit is set.
5:1	CUR_SUBFRAME_MODE	
0	FRAMER_BOOTED	Asserted after framer has finished booting up

0x28080410 LPASS_SB_FRM_INT_EN

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_FRM_INT_EN

Bits	Name	Description
4	CDL_TIMEDOUT	Active Framer could not exit CheckingDataLine state before timer expired. This interrupt is triggered only if programmable timer value set in register SB_FRM_CFG register is non-zero.
3	IDLE_MODE_EXITED	Slimbus has exited idle mode
2	FRAMER_BOOT_COMPLETE	Framer has booted successfully
1	IE_VE_CHANGE	An IE or VE has changed its value.
0	DEV_ERR	Device reported error. See status register for details.

0x28080414 LPASS_SB_FRM_INT_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

Status of interrupt elements.

LPASS_SB_FRM_INT_STATUS

Bits	Name	Description
4	CDL_TIMEDOUT	Active Framer could not exit CheckingDataLine state before timer expired. This interrupt is triggered only if programmable timer value set in register SB_FRM_CFG register is non-zero.
3	IDLE_MODE_EXITED	Slimbus has exited idle mode
2	FRAMER_BOOT_COMPLETE	Framer has booted successfully
1	IE_VE_CHANGE	An IE or VE has changed its value.
0	DEV_ERR	Device reported error. See status register for details.

0x28080418 LPASS_SB_FRM_INT_CLR

Type: Write
Clock: HCLK
Reset State: 0x00000000

Interrupt clear.

LPASS_SB_FRM_INT_CLR

Bits	Name	Description
4	CDL_TIMEDOUT	Active Framer could not exit CheckingDataLine state before timer expired. This interrupt is triggered only if programmable timer value set in register SB_FRM_CFG register is non-zero.
3	IDLE_MODE_EXITED	Slimbus has exited idle mode
2	FRAMER_BOOT_COMPLETE	Framer has booted successfully
1	IE_VE_CHANGE	An IE or VE has changed its value.
0	DEV_ERR	Device reported error. See status register for details.

0x2808041C LPASS_SB_FRM_WAKEUP

Type: Write
Clock: HCLK
Reset State: 0x00000000

Wakeup register.

LPASS_SB_FRM_WAKEUP

Bits	Name	Description
0	WAKEUP_NOW	Wakes up framer if in idle mode.

0x28080420 LPASS_SB_FRM_CLKCTL_DONE

Type: Write
Clock: HCLK
Reset State: 0x00000000

This command-type register is used to indicate to hardware that clk_ctl block has completed reconfiguring the clock.

LPASS_SB_FRM_CLKCTL_DONE

Bits	Name	Description
0	CLKCTL_DONE	Indicates to H/W that clkctl block is done re-configuring the ref clk.

0x28080430 LPASS_SB_FRM_IE_STATUS

Type: Read
Clock: HCLK
Reset State: 0xFE010000

Holds status of IE elements listed out in spec.

LPASS_SB_FRM_IE_STATUS

Bits	Name	Description
31:24	DEV_CLASS_CODE	
23:16	DEV_CLASS_VER	
15:10	RESERVED_15	reserved
9:8	QUAL	Framer Clk Quality
7	GC_TX_COL	
6	FI_TX_COL	
5	FS_TX_COL	
4	ACTIVE_FRAMER	
3	EX_ERROR	
2	RECONFIG_OBJ	
1	RESERVED	reserved
0	UNSPRTD_MSG	unsupported msg

0x28080440 LPASS_SB_FRM_VE_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

place holder.

LPASS_SB_FRM_VE_STATUS

Bits	Name	Description
31:0	VE_VAL	currently reads all zeroes

12.6.3 Interface Device Registers

0x28080600 LPASS_SB_INTF_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_INTF_CFG

Bits	Name	Description
0	ENABLE	

0x28080604 LPASS_SB_INTF_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_INTF_STATUS

Bits	Name	Description
13	MESSAGE_SYNC_ACQUIRED	
12	SUPERFRAME_SYNC_ACQUIRED	
11	FRAME_SYNC_ACQUIRED	
10:3	DEV_LA	Logical address assigned to device. Valued only if ENUMERATED is asserted.
2	ENUMERATED	Indicates if Interface device has been assigned a logical address.
1:0	ERROR	Read only. Two bits holding any error conditions that the device may want to report. Valid only if INTF DEV_ERR bit is set.

0x28080610 LPASS_SB_INTF_INT_EN

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_INTF_INT_EN

Bits	Name	Description
1	IE_VE_CHANGE	An IE or VE has changed its value.
0	DEV_ERR	Device reported error. See status register for details.

0x28080614 LPASS_SB_INTF_INT_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

Status of interrupt elements.

LPASS_SB_INTF_INT_STATUS

Bits	Name	Description
1	IE_VE_CHANGE	An IE or VE has changed its value.
0	DEV_ERR	Device reported error. See status register for details.

0x28080618 LPASS_SB_INTF_INT_CLR

Type: Write
Clock: HCLK
Reset State: 0x00000000

Interrupt clear.

LPASS_SB_INTF_INT_CLR

Bits	Name	Description
1	IE_VE_CHANGE	An IE or VE has changed its value.
0	DEV_ERR	Device reported error. See status register for details.

0x28080630 LPASS_SB_INTF_IE_STATUS

Type: Read
Clock: HCLK
Reset State: 0xFD010000

Holds status of IE elements listed out in spec.

LPASS_SB_INTF_IE_STATUS

Bits	Name	Description
31:24	DEV_CLASS_CODE	
23:16	DEV_CLASS_VER	
15:9	RESERVED_15	reserved
8	DS_OVERLAP	

LPASS_SB_INTF_IE_STATUS (cont.)

Bits	Name	Description
7	LOST_MS	
6	LOST_SFS	
5	LOST_FS	
4	MC_TX_COL	
3	EX_ERROR	
2	RECONFIG_OBJ	
1	DATA_TX_COL	reserved
0	UNSPRTD_MSG	unsupported msg

0x28080640 LPASS_SB_INTF_VE_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

place holder.

LPASS_SB_INTF_VE_STATUS

Bits	Name	Description
31:0	VE_VAL	currently reads all zeroes

12.6.4 Non-Ported Generic Device(s) (NGD) Registers

There are two NGDs in a given slimbus component. NGDs do not have ports hence no data channel support. They are intended to help the various EE send messages to devices across SLIMbus and to each other through SLIMbus. NGDs may or may not have message queue support as per what their register bits states.

0x28080800 LPASS_SB_NGD1_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_NGD1_CFG

Bits	Name	Description
2	TX_MSGQ_EN	Enable the Tx Msg Queue if supported. If not supported, this bit is a don’t care and will read back 0.

LPASS_SB_NGD1_CFG (cont.)

Bits	Name	Description
1	RX_MSGQ_EN	Enable the Rx Msg Queue if supported. If not supported, this bit is a don't care and will read back a 0.
0	ENABLE	

0x28080804 LPASS_SB_NGD1_STATUS

Type: Read
Clock: HCLK
Reset State: 0x0000040C

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LPASS_SB_NGD1_STATUS

Bits	Name	Description
26:20	NACKED_TX_MSG_MC	Read Only. The MC of the TX msg that was nacked by the destination twice or the MC of the invalid tx msg depending on which intr bit is set
19:13	ACKED_TX_MSG_MC	Read Only. The MC of the latest TX msg from the msg queues that was positively acked by the destination.
12:11	ERROR	Read only. Two bits holding any error conditions that the device may want to report. Valid only if Gen DEV_ERR bit is set.
10	MSGQ_SUPPORT	If set, this Generic device supports two message queues - Tx and Rx - at pipe numbers OFFSET and OFFSET+1
9:2	PIPE_NUM_OFFSET	The offset value for pipe number set for this generic devices. If MSGQ_SUPPORT=1, then this offset indicates the pipe number for Rx and Tx Msg Queues at pipe numbers OFFSET and OFFSET+1 respectively. This field is don't care if MSQ_SUPPORT = 0.
1	ENUMERATED	If set, the device has been enumerated.
0	TX_MSG_BUFFER_BUSY	If set, then the Tx Msg Buffer has a message waiting to be sent out. Hence the direct access should not be used until this bit is a 0 again. Its recommended to wait for the enumerated bit to get set before polling this bit. Should not be used as a check for txmsg sent.

0x28080808 LPASS_SB_NGD1_RX_MSGQ_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The fields that control the RX message queue (i.e., producer queue) if present.

LPASS_SB_NGD1_RX_MSGQ_CFG

Bits	Name	Description
31:16	TIME_OUT_VAL	TIme out counter enabled if this field is non zero and when the first message is received. Time out cntr reset after every Rx msg received, If next Rx message not received before it expires, a trans_end is automatically generated even if BLOCK_SIZE/TRANS_SIZE is not got. Specified in terms of AHB Bus clock cycles given to the core by the ClockCtrl of SoC.
15:8	TRANS_SIZE	Specified in units of messages. After receiving that many a trans_end is asserted.Honored only if MSGQ_SUPPORT bit reads a 1
7:0	BLOCK_SIZE	Specified in units of messages. AFter receiving this many, a block_end is asserted.SW can leave this 0 in system producer mode to prevent block_end assertion. Honored only if MSGQ_SUPPORT bit reads a 1.

0x28080810 LPASS_SB_NGD1_INT_EN

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register has interrupt enables for regular device events (bits 31:28)

LPASS_SB_NGD1_INT_EN

Bits	Name	Description
31	TX_MSG_SENT	If queue is not enabled, this bit is set When a message written to TX_MSG reg is sent out. If queue is enabled, this bit is set when last TX msg of the current transaction is sent out.
30	RX_MSG_RCVD	When a message has been received in the RX_MSG registers.
29	DEV_ERR	Device reported error. See status register for details.
28	IE_VE_CHANGE	An IE or VE has changed its value.
27	INVALID_TX_MSG	An invalid TX message not allowed for this device is written into the Tx buffer.
26	TX_MSG_BUF_CONTENTIO N	If enabled, this generates an interrupt whenever SW (through direct AHB access) tries to write to an tx buffer that is not available for SW.
25	TX_MSG_NACKED_TWICE	A Tx msg nacked twice
24	RECONFIG_DONE	After successfully sending a RECONFIG_NOW command

0x28080814 LPASS_SB_NGD1_INT_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

Status of interrupt elements.

LPASS_SB_NGD1_INT_STATUS

Bits	Name	Description
31	TX_MSG_SENT	
30	RX_MSG_RCVD	
29	DEV_ERR	
28	IE_VE_CHANGE	
27	INVALID_TX_MSG	
26	TX_MSG_BUF_CONTENTION	
25	TX_MSG_NACKED_TWICE	
24	RECONFIG_DONE	

0x28080818 LPASS_SB_NGD1_INT_CLR

Type: Write
Clock: HCLK
Reset State: 0x00000000

Interrupt clear.

LPASS_SB_NGD1_INT_CLR

Bits	Name	Description
31	TX_MSG_SENT	
30	RX_MSG_RCVD	
29	DEV_ERR	
28	IE_VE_CHANGE	
27	INVALID_TX_MSG	
26	TX_MSG_BUF_CONTENTION	
25	TX_MSG_NACKED_TWICE	
24	RECONFIG_DONE	

0x28080830+4*n LPASS_SB_NGD1_TX_MSGn, n=[0..9]

Type: Write
Clock: HCLK
Reset State: 0x00000000

SW uses these registers for Direct Access Tx Message receiving over SLIMbus. These hold the Tx message to be sent (40bytes max).

CAUTION This Direct access Messaging registers SHOULD NOT be used if the Tx queue is enabled. The resulting behavior is not defined.

LPASS_SB_NGD1_TX_MSGn

Bits	Name	Description
31:0	MSGVAL	message contents

0x28080870+4*n LPASS_SB_NGD1_RX_MSGn, n=[0..9]

Type: Read
Clock: HCLK
Reset State: 0x00000000

SW uses these registers for Direct Access Rx Message receiving over SLIMbus. These hold the RX message received and waiting for SW to consume(40bytes max).

CAUTION This Direct access Messaging registers SHOULD NOT be used if the Rx queue is enabled. The resulting behavior is not defined.

LPASS_SB_NGD1_RX_MSGn

Bits	Name	Description
31:0	MSGVAL	message contents

0x280808F0 LPASS_SB_NGD1_IE_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00010000

Holds status of IE elements listed out in spec

LPASS_SB_NGD1_IE_STATUS

Bits	Name	Description
31:24	DEV_CLASS_CODE	
23:16	DEV_CLASS_VER	
15:4	RESERVED_15_4	reserved
3	EX_ERROR	
2	RECONFIG_OBJ	
1	DATA_TX_COL	reserved
0	UNSPRTD_MSG	unsupported msg

0x28080900 LPASS_SB_NGD1_VE_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

place holder

Registers for Second NGD device.

LPASS_SB_NGD1_VE_STATUS

Bits	Name	Description
31:0	VE_VAL	reads zeroes

0x28080A00 LPASS_SB_NGD2_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_NGD2_CFG

Bits	Name	Description
2	TX_MSGQ_EN	Enable the Tx Msg Queue if supported. If not supported, this bit is a don’t care and will read back 0.
1	RX_MSGQ_EN	Enable the Rx Msg Queue if supported. If not supported, this bit is a don’t care and will read back a 0.
0	ENABLE	

0x28080A04 LPASS_SB_NGD2_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000414

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LPASS_SB_NGD2_STATUS

Bits	Name	Description
26:20	NACKED_TX_MSG_MC	Read Only. The MC of the TX msg that was nacked by the destination twice or the MC of the invalid tx msg depending on which intr bit is set
19:13	ACKED_TX_MSG_MC	Read Only. The MC of the latest TX msg from the msg queues that was positively acked by the destination.
12:11	ERROR	Read only. Two bits holding any error conditions that the device may want to report. Valid only if Gen DEV_ERR bit is set.
10	MSGQ_SUPPORT	If set, this Generic device supports two message queues - Tx and Rx - at pipe numbers OFFSET and OFFSET+1
9:2	PIPE_NUM_OFFSET	The offset value for pipe number set for this generic devices. If MSGQ_SUPPORT=1, then this offset indicates the pipe number for Rx and Tx Msg Queues at pipe numbers OFFSET and OFFSET+1 respectively. This field is don't care if MSQ_SUPPORT = 0.
1	ENUMERATED	If set, the device has been enumerated.
0	TX_MSG_BUFFER_BUSY	If set, then the Tx Msg Buffer has a message waiting to be sent out. Hence the direct access should not be used until this bit is a 0 again. Its recommended to wait for the enumerated bit to get set before polling this bit.Should not be used as a check for txmsg sent.

0x28080A08 LPASS_SB_NGD2_RX_MSGQ_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The fields that control the RX message queue (i.e., producer queue) if present.

LPASS_SB_NGD2_RX_MSGQ_CFG

Bits	Name	Description
31:16	TIME_OUT_VAL	TIme out counter enabled if this field is non zero and when the first message is received. Time out cntr reset after every Rx msg received, If next Rx message not received before it expires, a trans_end is automatically generated even if BLOCK_SIZE/TRANS_SIZE is not got. Specified in terms of AHB Bus clock cycles given to the core by the ClockCtrl of SoC.
15:8	TRANS_SIZE	Specified in units of messages. After receiving that many a trans_end is asserted.Honored only if MSGQ_SUPPORT bit reads a 1
7:0	BLOCK_SIZE	Specified in units of messages. AFter receiving this many, a block_end is asserted.SW can leave this 0 in system producer mode to prevent block_end assertion. Honored only if MSGQ_SUPPORT bit reads a 1.

0x28080A10 LPASS_SB_NGD2_INT_EN

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register has interrupt enables for regular device events (bits 31:28)

LPASS_SB_NGD2_INT_EN

Bits	Name	Description
31	TX_MSG_SENT	If queue is not enabled, this bit is set When a message written to TX_MSG reg is sent out. If queue is enabled, this bit is set when last TX msg of the current transaction is sent out.
30	RX_MSG_RCVD	When a message has been received in the RX_MSG registers.
29	DEV_ERR	Device reported error. See status register for details.
28	IE_VE_CHANGE	An IE or VE has changed its value.
27	INVALID_TX_MSG	An invalid TX message not allowed for this device is written into the Tx buffer.
26	TX_MSG_BUF_CONTENTIO N	If enabled, this generates an interrupt whenever SW (through direct AHB access) tries to write to an tx buffer that is not available for SW.
25	TX_MSG_NACKED_TWICE	An TX msg nacked twice
24	RECONFIG_DONE	After successfully sending a RECONFIG_NOW command

0x28080A14 LPASS_SB_NGD2_INT_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

Status of interrupt elements.

LPASS_SB_NGD2_INT_STATUS

Bits	Name	Description
31	TX_MSG_SENT	
30	RX_MSG_RCVD	
29	DEV_ERR	
28	IE_VE_CHANGE	
27	INVALID_TX_MSG	
26	TX_MSG_BUF_CONTENTIO N	
25	TX_MSG_NACKED_TWICE	
24	RECONFIG_DONE	

0x28080A18 LPASS_SB_NGD2_INT_CLR

Type: Write
Clock: HCLK
Reset State: 0x00000000

Interrupt clear.

LPASS_SB_NGD2_INT_CLR

Bits	Name	Description
31	TX_MSG_SENT	
30	RX_MSG_RCVD	
29	DEV_ERR	
28	IE_VE_CHANGE	
27	INVALID_TX_MSG	
26	TX_MSG_BUF_CONTENTIO N	
25	TX_MSG_NACKED_TWICE	.
24	RECONFIG_DONE	

0x28080A30+ 4*n LPASS_SB_NGD2_TX_MSGn, n=[0..9]

Type: Write
Clock: HCLK
Reset State: 0x00000000

SW uses these registers for Direct Access Tx Message receiving over SLIMbus. These hold the Tx message to be sent out(40bytes max).

CAUTION This Direct access Messaging registers SHOULD NOT be used if the Tx queue is enabled. The resulting behavior is not defined.

LPASS_SB_NGD2_TX_MSGn

Bits	Name	Description
31:0	MSGVAL	message contents

0x28080A70+ 4*n LPASS_SB_NGD2_RX_MSGn, n=[0..9]

Type: Read
Clock: HCLK
Reset State: 0x00000000

SW uses these registers for Direct Access Rx Message receiving over SLIMbus. These hold the RX message received and waiting for SW to consume(40bytes max).

CAUTION This Direct access Messaging registers SHOULD NOT be used if the Rx queue is enabled. The resulting behavior is not defined.

LPASS_SB_NGD2_RX_MSGn

Bits	Name	Description
31:0	MSGVAL	message contents

0x28080AF0 LPASS_SB_NGD2_IE_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00010000

Holds status of IE elements listed out in spec

LPASS_SB_NGD2_IE_STATUS

Bits	Name	Description
31:24	DEV_CLASS_CODE	
23:16	DEV_CLASS_VER	
15:4	RESERVED_15_4	reserved
3	EX_ERROR	
2	RECONFIG_OBJ	
1	DATA_TX_COL	reserved
0	UNSPRTD_MSG	unsupported msg

0x28080B00 LPASS_SB_NGD2_VE_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

place holder

LPASS_SB_NGD2_VE_STATUS

Bits	Name	Description
31:0	VE_VAL	reads zeroes

12.6.5 Ported Generic Device (PGD) Registers

0x28081000 LPASS_SB_PGD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_PGD_CFG

Bits	Name	Description
0	ENABLE	

0x28081004 LPASS_SB_PGD_STATUS

Type: Read
Clock: HCLK
Reset State: 0x000U07UU

LPASS_SB_PGD_STATUS

Bits	Name	Description
20:19	ERROR	Read only. Two bits holding any error conditions that the device may want to report. Valid only if Gen DEV_ERR bit is set. 0x0: a TX message from this device was nacked twice by the destination.
18:16	NUM_PC_VFR_BLKS	The RTL Generic set for inferring the number of 'Progress counter and VFR Timestamp logic'
15:8	PIPE_NUM_OFFSET	The offset value for pipe number set for this generic devices. This is the pipe number from which ports of this generic device are connected. Pipe number is also reflected in the individual port registers.
7:0	NUM_PORTS	No. of Ports that is inferred on this Generic Device

0x28081010 LPASS_SB_PGD_DEV_INT_EN

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register has interrupt enables for regular device events (bits 31:28)

LPASS_SB_PGD_DEV_INT_EN

Bits	Name	Description
1	IE_VE_CHANGE	An IE or VE has changed its value.
0	DEV_ERR	Device reported error. See status register for details.

0x28081014 LPASS_SB_PGD_DEV_INT_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

Status of interrupt elements.

LPASS_SB_PGD_DEV_INT_STATUS

Bits	Name	Description
1	IE_VE_CHANGE	An IE or VE has changed its value.
0	DEV_ERR	Device reported error. See status register for details.

0x28081018 LPASS_SB_PGD_DEV_INT_CLR

Type: Write
Clock: HCLK
Reset State: 0x00000000

Interrupt clear.

LPASS_SB_PGD_DEV_INT_CLR

Bits	Name	Description
1	IE_VE_CHANGE	An IE or VE has changed its value.
0	DEV_ERR	Device reported error. See status register for details.

0x28081020 LPASS_SB_PGD_TRUST_OWN_EE0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

.Decides the port int ownership of a given EE. This register is programmed by the Trusted EE.

LPASS_SB_PGD_TRUST_OWN_EE0

Bits	Name	Description
31:0	PORT_OWN	If bit n of this register is set, then EE0 owns that port. EE0 may choose to enable an interrupt from this port based on its setting in SB_PGD_PORT_INT_EN_EE0 register. This owner is allocated by the trusted EE to prevent an EE from receiving intr from a port that it does NOT own.

0x28081024 LPASS_SB_PGD_TRUST_OWN_EE1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

.Decides the port int ownership of a given EE. This register is programmed by the Trusted EE.

LPASS_SB_PGD_TRUST_OWN_EE1

Bits	Name	Description
31:0	PORT_OWN	If bit n of this register is set, then EE1 owns that port. EE1 may choose to enable an interrupt from this port based on its setting in SB_PGD_PORT_INT_EN_EE1 register. This owner is allocated by the trusted EE to prevent an EE from receiving intr from a port that it does NOT own.

0x28081028 LPASS_SB_PGD_TRUST_OWN_EE2

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

.Decides the port int ownership of a given EE. This register is programmed by the Trusted EE.

LPASS_SB_PGD_TRUST_OWN_EE2

Bits	Name	Description
31:0	PORT_OWN	If bit n of this register is set, then EE2 owns that port. EE2 may choose to enable an interrupt from this port based on its setting in SB_PGD_PORT_INT_EN_EE2 register. This owner is allocated by the trusted EE to prevent an EE from receiving intr from a port that it does NOT own.

0x28081030+16*n LPASS_SB_PGD_PORT_INT_EN_EEn, n=[0..2]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register has an enable per port. Port events are recorded in the corresponding port status/param registers and this enable bit merely makes sure that an interrupt to the said EE is fired if the port has an event to report per port status bits. Only bits up to the number dictated by NUM_PORTS field of the Generics register is valid.

The sources of interrupt for a port could be -

i. Over flow condition of FIFOs (reflected in PGD_PORT_STATUSn register)

ii. Underflow condition of FIFOs (reported in PGD_PORT_STATUSn register)

iii. A port Disconnect event (reported in PGD_PORT_STATUSn register)

LPASS_SB_PGD_PORT_INT_EN_EEn

Bits	Name	Description
31:0	PORT_INT	Interrupt event from Ports. The actual number of bits here depends on the number of ports inferred for the generic device.

0x28081034+16*n LPASS_SB_PGD_PORT_INT_STATUS_EEn, n=[0..2]

Type: Read
Clock: HCLK
Reset State: 0x00000000

Status of interrupt elements.

LPASS_SB_PGD_PORT_INT_STATUS_EEn

Bits	Name	Description
31:0	PORT_INT	Interrupt event from Ports. The actual number of bits here depends on the number of ports inferred for the generic device.

0x28081038+16*n LPASS_SB_PGD_PORT_INT_CLR_EEn, n=[0..2]

Type: Write
Clock: HCLK
Reset State: 0x00000000

Interrupt clear.

LPASS_SB_PGD_PORT_INT_CLR_EEn

Bits	Name	Description
31:0	PORT_INT	Interrupt event from Ports. The actual number of bits here depends on the number of ports inferred for the generic device.

0x28081080+32*n LPASS_SB_PGD_PORT_CFGn, n=[0..23]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

Only EVEN numbered ports (0,2,4, ...) should be configured by the Manager to support a Half duplex or extended half duplex data channel. If so, the data stream and hence the FIFOs etc corresponding to that port should be configured appropriately for outbound traffic (consumer). And hence its own Block and Trans size registers should NOT be used.

If Half duplex data channel, then use an even numbered port. Its immediately next odd numbered port should not be used for another channel as long as that half duplex channel is active. Even port's data stream (pipe) should be outbound (i.e., consumer or TX). Its immediate next odd port's data stream (pipe) is inbound (producer or Rx) and hence blk/trans size for this odd port should be configured as needed. The BAM pipe should be configured appropriately.

LPASS_SB_PGD_PORT_CFGn

Bits	Name	Description
7	ALIGN_MSB	If set, data is MSB aligned. If 0, data is LSB aligned. (applies to pieces data segments that are not integer multiple of words or packed to word boundary).
6	PACK	If set by SW, implies the incoming data to this port is to be packed by HW (or if port is outbound, then the HW is getting a packed data to send out and hence should unpack before sending).
5:1	WATERMARK	Water mark for the FIFO in bytes. Legal values are 1 to max fifo size.
0	ENABLE	Enables the port

0x28081084+ 32*n LPASS_SB_PGD_PORT_STATUSn, n=[0..23]

Type: Read
Clock: HCLK
Reset State: 0x00000UUU

LPASS_SB_PGD_PORT_STATUSn

Bits	Name	Description
19	PRT_DISCONN	If set, a port Disconnect Event has happened.Read only
18	FIFO_FILL_LEVEL	If set, implies that the FIFO is having 'watermark' worth of data when acting as a source to a data channel.
17:12	FIFO_WORD_CNT	Dynamically Reflects the number of words in the FIFO
11:4	PIPE_NUM	The pipe number (aka data stream number this port is connected to). Takes into account the offset and presence of other generic devices if any.
3	UNDERFLOW	IF set, this port has faced a FIFO underflow. Read only
2	OVERFLOW	If set, this port has faced a FIFO overflow. Read only
1:0	FIFO_SIZE	Encoded size of the data stream FIFO. 0x0: 8 bytes (2x 32bits) 0x1: 16 bytes (4x32bits) 0x2: 32 bytes (8x32bits) 0x3: reserved

0x28081088+ 32*n LPASS_SB_PGD_PORT_PARAMn, n=[0..23]

Type: Read
Clock: HCLK
Reset State: 0x00000000

Reflects if the port is active, if so, what is the SD, SL, CN, TP etc.

LPASS_SB_PGD_PORT_PARAMn

Bits	Name	Description
29:25	SEG_LENGTH	
24:21	TRANSPORT_PROTOCOL	
20:9	SEG_DISTN	
8:1	CHANNEL_NUMBER	
0	CHANNEL_ACTIVE	

0x2808108C+ 32*n LPASS_SB_PGD_PORT_BLK_SIZEn, n=[0..23]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_PGD_PORT_BLK_SIZEn

Bits	Name	Description
31:0	BLK_SIZE	In units of bytes. SW can leave this 0 in system producer mode to prevent block_end assertion.

0x28081090+ 32*n LPASS_SB_PGD_PORT_TRANS_SIZEn, n=[0..23]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_PGD_PORT_TRANS_SIZEn

Bits	Name	Description
31:0	TRANS_SIZE	In units of bytes

0x28081094+ 32*n LPASS_SB_PGD_PORT_MULTI_CHNLn, n=[0..23]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

Each bit m of this register represents a port. If that bit m is set, then it means port m is involved in a multichannel audio stream with this port n. The number of bits set in this register hence represents the number of streams in the multichnl stream. Note, even the participating port's bit (i.e., bit n) should be set as well. For example, if ports 0 to 5 participate in a 5:1 audio stream, then the SB_PGD_MULTI_CHNLn register for n=0..5 should be set to 0x3F (i.e., bits 0 to 5 of each being set). These register for every port are used to generate silence tone if any of the participating streams run dry.

CAUTION To ensure proper functionality, for a given port number p, at least one bit of this register MUST be set, i.e., bit p should be set in SB_PGD_PORT_MULTI_CHNLp when port number p is used. If the said port p was involved in a multichannel stream, then one or more other bits in this register can be set to 1.

LPASS_SB_PGD_PORT_MULTI_CHNLn

Bits	Name	Description
31:0	PORTS	see description of register

0x28081098+ 32*n LPASS_SB_PGD_PORT_PUSHPULLn, n=[0..23]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

Contains the repeat_period and num_samples parameters used the push/pull TP hardware to calculate the P-bit, SRQ-bit and the STRbit.

LPASS_SB_PGD_PORT_PUSHPULLn

Bits	Name	Description
31:16	NUM_SAMPLES	Num_samples value.
15:0	RPT_PERIOD	repeat period value

0x28081600+ 32*n LPASS_SB_PGD_PC_CFGn, n=[0..5]

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

Progress Counter Configuration

LPASS_SB_PGD_PC_CFGn

Bits	Name	Description
31	INIT	write-only. Reads a 0 always. When written a 1, its rise edge detected to load the PC with INIT_VAL field value.
29:30	RESERVED	reserved
28:24	PORT_SEL	The Port number that this nth instance of PC/VFR Logic is associated to.
23:0	INIT_VAL	The PC init val to be loaded into the PC. Value Loaded only when INIT bit is set. INIT bit is rise-edge detected inside for loading PC.

0x28081604+ 32*n LPASS_SB_PGD_PC_VALn, n=[0..5]

Type: Read
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_PGD_PC_VALn

Bits	Name	Description
31:24	PC_FIFO_SAMPLES	The number of samples in the FIFO (taking into account segment length and pack bit settings) plus any sample in the phy/FL stages. **NOTE** When acting as SRC, there will be duplication between the DMA and the SAMPLE fields, as samples already counted in DMA may still be awaiting processing in FIFO
23:0	PC_DMA	Value of the 24bit counter counting the ‘number of words’ DMA-ed to (if src) or from (if snk) from the associated port. The Firmware needs to convert it into number of samples based on sample size and if pack bit is set or not.

0x28081608+ 32*n LPASS_SB_PGD_PC_VFR_TSn, n=[0..5]

Type: Read
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_PGD_PC_VFR_TSn

Bits	Name	Description
31:0	VAL	The value of the 32bit PC_VAL register when the VFR TS Interrupt occurred.

0x2808160C+32*n LPASS_SB_PGD_PC_VFR_TS_STATUSn, n=[0..5]

Type: Read
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_PGD_PC_VFR_TS_STATUSn

Bits	Name	Description
31:30	RESERVED	reserved
0	VFR_INT	Set when VFR interrupt pulse gets asserted, cleared when clear register is written to.

0x28081610+32*n LPASS_SB_PGD_PC_VFR_TS_CLRn, n=[0..5]

Type: Write
Clock: HCLK
Reset State: 0x00000000

LPASS_SB_PGD_PC_VFR_TS_CLRn

Bits	Name	Description
31:30	RESERVED	reserved
0	VFR_INT	When written with 1, clears the TS_STATUS bit if that is set.

0x28081700 LPASS_SB_PGD_IE_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00010000

Holds status of IE elements listed out in spec

LPASS_SB_PGD_IE_STATUS

Bits	Name	Description
31:24	DEV_CLASS_CODE	
23:16	DEV_CLASS_VER	
15:4	RESERVED_15_4	reserved
3	EX_ERROR	
2	RECONFIG_OBJ	
1	DATA_TX_COL	reserved
0	UNSPRTD_MSG	unsupported msg

0x28081710 LPASS_SB_PGD_VE_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

place holder

LPASS_SB_PGD_VE_STATUS

Bits	Name	Description
31:0	VE_VAL	reads zeroes

12.7 LPASS BAM Registers (0x28084000 LPASS_BAM_LITE_BASE)

This section contains the Low Power Audio Subsystem (LPASS) BAM registers.

BAM supports only Word (4 byte) aligned writes and reads on the Configuration Bus interface.

BAM has MAX_PIPES hardware generic parameter defining the number of pipes it supports. Each BAM can have up to 31 pipes supported.

BAM has BAM_CONF_AHBS_ADDR_WIDTH hardware generic parameter defining the Bit Number for selecting BAM access or Peripheral access. Legal Ranges are 14 to 20. Count starts from 1, meaning a value of 17 will set BAM Base address as 0x0001_0000.

12.7.1 BAM control registers

BAM Control registers configure the BAM operational state, SW reset, interrupts and others.

0x28084F80 LPASS_BAM_CTRL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

BAM Control register allows global controls for the BAM.

LPASS_BAM_CTRL

Bits	Name	Description
31:17	RESERVED_BITS31_17	Set to Zero (0)
16	IBC_DISABLE	This Bit enables power saving by disabling the inactivity clock timer/counter. This is useful when: 1) The BAM is Enabled but idling for long periods. 2) The BAM is Enabled and running but the inactivity timers/counters are not required by the SW for operating the BAM. When the BAM is Disabled, it automatically shuts down those timers to save power. 1’b1 - Enable Power Saving Mode 1’b0 - Disable Power Saving Mode

LPASS_BAM_CTRL (cont.)

Bits	Name	Description
15	BAM_CACHED_DESC_STORE	This Bit enables storage of a cached Descriptor into RAM when doing Context Switch and loading it back when returning to this pipe. This is relevant for System Modes Only. BAM to BAM Consumer mode doesn't have this option. Enabling this makes the Context Switch process slightly longer but reduces AHB Descriptor Fetch time later on. It also reduces the number of descriptor fetches done by the BAM if BAM is treating more than 2 pipes. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
14:13	BAM_DESC_CACHE_SEL	This Selector chooses which Descriptor Caching mode will be used. This is relevant for System Producer or Consumer modes only. 2’b00 - Cache when current descriptor has less than 64 bytes left. 2’b01 - Cache when current descriptor has less than 128 bytes left. 2’b10 - Immediate Auto cache - cache will happen whenever there are no descriptors cached. This might cause unnecessary descriptors reads when switching between more than 2 pipes. It is the most effective when each pipe processes more bytes than there are in an average descriptor (small descriptors, big block size), or when working with 2 or less pipes. 2’b11 - Cache when descriptor is needed only. This results in 1 descriptor present in cache at most. Available in BAM only
12	RESERVED_BITS12	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_SIC_SEL
11:5	BAM_TESTBUS_SEL	Set to Zero (0) Obsolete field: BAM_TESTBUS_SEL Test Bus selector. Supported until (including) bam_p3q3r29 (BlackBird). Moved to a dedicated register - BAM_TEST_BUS_SEL in the following releases.
4	BAM_EN_ACCUM	When Enabled, BAM will accumulate data written by the peripheral in Direct Mode into INCR8 Bursts. This is an optimization feature for Producer Direct Mode cases. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
3	RESERVED_BITS3	Set to Zero (0)
2	RESERVED_BITS2	Set to Zero (0)

LPASS_BAM_CTRL (cont.)

Bits	Name	Description
1	BAM_EN	After reset the BAM wakes up in Disabled Mode. While Disabled, BAM operates in Legacy mode (all the transfers from the peripheral go around the BAM as if it doesn't exist) Software Enables this bit to allow BAM operation. This bit doesn't affect the PIPE enable bit in BAM_P_CTRL register. The only possibility to Disable the BAM after it has been enabled is by Hardware or Software reset. 1'b1 - Enabled 1'b0 - Disabled
0	BAM_SW_RST	This will reset the BAM & all Pipes. Software may use this to reset the BAM. As long as the bit remains high the BAM remains in reset state. Software should clear this bit 1'b1 - Reset state 1'b0 - Normal state

0x28084F84 LPASS_BAM_REVISION

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a hard coded revision number of the BAM RTL. This corresponds to the BAM target number in the IMS. Also additional BAM settings are reflected here.

LPASS_BAM_REVISION

Bits	Name	Description
31:24	INACTIV_TMR_BASE	This indicates the width of the inactivity timers base counter
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	NUM_INACTIV_TMRS	This bit is checked only if INACTIV_TMRS_EXST = 1. This bit indicates how many inactivity timers are implemented according to value of INACTIVITY_TIMERS_SUPPORTED generic: 1'b1 - One timer for global BAM activity (INACTIVITY_TIMERS_SUPPORTED = 1) 1'b0 - MAX_PIPES timers for each pipe activity (INACTIVITY_TIMERS_SUPPORTED = 2)
19	INACTIV_TMRS_EXST	This indicates BAM has inactivity timers. 1'b1 - Timers available (INACTIVITY_TIMERS_SUPPORTED = 1 or 2) 1'b0 - No timers available (INACTIVITY_TIMERS_SUPPORTED = 0)

LPASS_BAM_REVISION (cont.)

Bits	Name	Description
18	HIGH_FREQUENCY_BAM	This indicates BAM has Double Sampling on the Ack On Success interface. 1'b1 - Ack On Success double sampled 1'b0 - No double sampling of Ack On Success
17	BAM_HAS_NO_BYPASS	This field indicates BAM has no bypass on the AHB Data bus, from the Peripheral AHB Master to the fabric. When Bypass is available, it is the default routing when BAM is disabled. 1'b1 - No Bypass 1'b0 - Bypass Exists
16	SECURED	This field indicates BAM/BAM-Lite has security support (APU inside) 1'b1 - Secured 1'b0 - Not Secured
15:12	RESERVED_BITS15_12	Set to Zero (0)
11:8	NUM_EES	This indicates the Number of Interrupt Lines (Execution Environments) supported by the BAM. When 1 EE is supported, only the BAM_IRQ_SRCS*_EE0 registers exist. When 4 EEs are supported, all BAM_IRQ_SRCS*_EEn registers exist for n=[0..3].
7:0	REVISION	This field contains the revision number of the core, Hard Coded. 8'h01 - Voyager (bam_p3q3r22 +) 8'h02 - BlackBird (bam_p3q3r27 +) 8'h03 - Waverider BAM (bam_p3q3r30 +) 8'h04 - Aurora BAM (bam_p3q2r43 +) 8'h05 - Shelby BAM (bam_p2q2r45 +) 8'h10 - Waverider BAM Lite (bam_lite_p1q1r0 +) 8'h11 - Aurora BAM Lite (bam_lite_p3q2r16 +) 8'h12 - Shelby BAM Lite (bam_lite_p2q2r18 +)

0x28084FBC LPASS_BAM_NUM_PIPES

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a the hard coded number of pipes in the BAM. Since each BAM may have a different number of pipes instantiated in HW, this register allows the SW to know this parameter. The reset state value doesn't have any meaning in this register since it is a constant.

LPASS_BAM_NUM_PIPES

Bits	Name	Description
31:24	BAM_NON_PIPE_GRP	This field contains the number of BAM Non Pipe security groups (APU Entries). Zeros when Non-Secured BAM
23:16	PERIPH_NON_PIPE_GRP	This field contains the number of Peripheral's Non Pipe security groups (APU Entries). Zeros when Non-Secured BAM
15:8	RESERVED_BITS15_8	Set to Zero (0)
7:0	BAM_NUM_PIPES	This field contains the number of pipes available in this BAM

0x28084FC0 LPASS_BAM_TIMER

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the BAM (all the pipes are in idle state).

LPASS_BAM_TIMER

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x28084FC4 LPASS_BAM_TIMER_CTRL

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The register can be written and read only when INACTIVITY_TIMERS_SUPPORTED generic equals to 1.

The resolution of the BAM inactivity timer are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define

the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * TIMER_TRSHLD.

LPASS_BAM_TIMER_CTRL

Bits	Name	Description
31	TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1 to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	TIMER_RUN	Will be used along with TIMER_MODE Not implemented at this time. Set to zero(0)
29	TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x28084F88 LPASS_BAM_DESC_CNT_TRSHLD

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds a threshold value for the counter summing the Size of the Descriptors Provided. This value is Global for all pipes but it is relevant for System Producer BAM mode and Both Consumer modes, where Descriptors summing takes place in order to provide the information to the peripheral via pipe bytes free (producer) or pipe bytes available interfaces.

LPASS_BAM_DESC_CNT_TRSHLD

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0).
15:0	CNT_TRSHLD	Threshold value. The maximum allowed value is 32kByte. Available in BAM only

0x28084F8C LPASS_BAM_IRQ_SRCS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking out this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register points to the physical BAM_IRQ_SRCS_EE0 register.

LPASS_BAM_IRQ_SRCS

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x28084F90 LPASS_BAM_IRQ_SRCS_MSK

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register points to the physical BAM_IRQ_SRCS_MSK_EE0 register.

LPASS_BAM_IRQ_SRCS_MSK

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x28084FB0 LPASS_BAM_IRQ_SRCS_UNMASKED

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register points to the physical BAM_IRQ_SRCS_UNMASKED_EE0 register.

LPASS_BAM_IRQ_SRCS_UNMASKED

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

0x28084F94 LPASS_BAM_IRQ_STTS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only.

Clearing the interrupt bits is done by writing to BAM_IRQ_CLR register.

LPASS_BAM_IRQ_STTS

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
3	BAM_EMPTY_IRQ	This interrupt is for DEBUG purpose only. It should not be used in normal SW flows. The interrupt indicates the BAMs buffer is empty. This bit can become high only when BAM_DATA_ERASE or BAM_DATA_FLUSH is high in BAM_TEST_BUS_SEL register.
2	BAM_ERROR_IRQ	This Indicates a Fatal Error has happened in the BAM. Currently this might happen due to an UnSuccessful Pipe Reset operation.

LPASS_BAM_IRQ_STTS (cont.)

Bits	Name	Description
1	BAM_HRESP_ERR_IRQ	This interrupt Indicates that an Erroneous HResponse has been received by the AHB Master. Additional Information about the error may be read at BAM_AHB_MASTER_ERR_* Registers. Clearing this interrupt also clears the BAM_AHB_MASTER_ERR_* Registers. Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x28084F98 LPASS_BAM_IRQ_CLR

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

LPASS_BAM_IRQ_CLR

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
3	BAM_EMPTY_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM-Lite only
2	BAM_ERROR_CLR	1'b1 - Clear 1'b0 - Unchanged
1	BAM_HRESP_ERR_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x28084F9C LPASS_BAM_IRQ_EN

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the BAM Interrupt Status register.

LPASS_BAM_IRQ_EN

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_EN	Enables Inactivity timer interrupt by writing this bit 1'b1 - Enable 1'b0 - Disable
3	BAM_EMPTY_EN	1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
2	BAM_ERROR_EN	1'b1 - Enable 1'b0 - Disable
1	BAM_HRESP_ERR_EN	1'b1 - Enable 1'b0 - Disable Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x28084FA0 LPASS_BAM_RESERVED_1

Type: Read
Clock: BAM_CLK
Reset State: 0x00000000

LPASS_BAM_RESERVED_1

Bits	Name	Description
31	RESERVED_BITS31	Set to Zero (0) Obsolete field: BAM_IRQ_SIC_SEL
30:0	RESERVED_BITS30_0	Set to Zero (0) Obsolete field: P_IRQ_SIC_SEL

0x28084FA4 LPASS_BAM_AHB_MASTER_ERR_CTRLS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

LPASS_BAM_AHB_MASTER_ERR_CTRLS

Bits	Name	Description
31:23	RESERVED_BITS31_16	Set to Zero (0)
22:18	BAM_ERR_HVMID	HVMID
17	BAM_ERR_DIRECT_MODE	DIRECT MODE
16:12	BAM_ERR_HCID	HCID
11:8	BAM_ERR_HPROT	HPROT
7:5	BAM_ERR_HBURST	HBURST
4:3	BAM_ERR_HSIZE	HSIZE
2	BAM_ERR_HWRITE	HWRITE
1:0	BAM_ERR_HTRANS	HTRANS

0x28084FA8 LPASS_BAM_AHB_MASTER_ERR_ADDR

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

LPASS_BAM_AHB_MASTER_ERR_ADDR

Bits	Name	Description
31:0	BAM_ERR_ADDR	HADDR

0x28084FAC LPASS_BAM_AHB_MASTER_ERR_DATA

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

LPASS_BAM_AHB_MASTER_ERR_DATA

Bits	Name	Description
31:0	BAM_ERR_DATA	HDATA

0x28084FB4 LPASS_BAM_RESERVED_2

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

LPASS_BAM_RESERVED_2

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_IRQ_DEST_ADDR

0x28084FB8 LPASS_BAM_RESERVED_3

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

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LPASS_BAM_RESERVED_3

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_DEST_ADDR

0x28084FF0 LPASS_BAM_TRUST_REG

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside - SECURED field in the BAM_REVISION register) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

LPASS_BAM_TRUST_REG

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_VMID	Those bits indicate the VMID value to be used when performing BAM type accesses to the bus. BAM Type accesses include BAM MTI (or Direct Mode accesses, not applicable for BAM Lite)
7	BAM_RST_BLOCK	When enabled, the BAM Global SW reset will not be available for usage. This is in order to deny Global SW reset requests by the Global security group. 1'b1 - Enable 1'b0 - Disable
6:2	RESERVED_BITS6_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_EE	This Field Indicates the EE (0,1,2,3) to which the BAM Interrupt belongs to. The pipe interrupts will fire on the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x28084FF4 LPASS_BAM_TEST_BUS_SEL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This is the testbus selector register.

Supported in releases after bam_p3q3r29 (BlackBird).

LPASS_BAM_TEST_BUS_SEL

Bits	Name	Description
31:19	RESERVED_BITS31_19	Set to Zero (0)
18	BAM_DATA_ERASE	When enabled, BAM will be instructed to erase all the data it currently has inside. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Erase 1'b0 - Disabled
17	BAM_DATA_FLUSH	When enabled, BAM will be instructed to flush all the data it currently has inside. BAM will only flush the data once it has enough data and a valid destination for it. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Flush 1'b0 - Disabled
16	BAM_CLK_ALWAYS_ON	This bit controls the BAM to issue 'always on' clock request. 1'b1 - Enable Always On clock request. 1'b0 - Disabled
15:7	RESERVED_BITS15_7	Set to Zero (0)
6:0	BAM_TESTBUS_SEL	Test Bus selector. Values with bit[11] set high are reserved for the BAM Lite integrator to provide testbus from outside of the BAM Lite. For example, eDML testbus may reside at X'100_0000' to X'111_1111' selector values. eDML has no registers thus has no test bus selector, so its test bus is combined with the BAM lite's. BAM provides zeroes on its testbus when external values selected. X'000_0000' - Zeros X'000_0001' - Slave test bus X'000_0010' - Pipe state machine test bus X'000_0011' - Buffer test bus X'000_0100' - Sideband test bus X'000_1101' - Bus Manager test bus X'001_0000' - Reg file test bus X'1''_''''' - BAM Lite sets zeroes on the test bus, leaving it for external use

0x28084FF8 LPASS_BAM_TEST_BUS_REG

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the value being output to the testbus of the chip. It is not intended for SW usage but for lab debugging of the BAM. Values here can change every cycle.

LPASS_BAM_TEST_BUS_REG

Bits	Name	Description
31:0	BAM_TESTBUS_REG	32 bit Testbus value. To select the Block in BAM to show here, use the BAM_TESTBUS_SEL field in BAM_CTRL register.

0x28084FFC LPASS_BAM_CNFG_BITS

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM configuration bits for bug fixes. It is highly recommended to follow the directions for each bit and set it accordingly.

LPASS_BAM_CNFG_BITS

Bits	Name	Description
31:27	RESERVED_BITS31_27	Set to Zero (0)
26	BAM_AU_ACCUMED	Recommended value: 1 This bit fixes a bug in the Ack Update state machine, where an overflow happened while counting descriptors and reaching more than 64kB of calculated sizes. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only
25	BAM_PSM_P_HD_DATA	Recommended value: 1 This bit allows pipe state machine to ignore retransmission requests if a pipe has just been initialized and process those as a regular fetch request. (consumer modes only). When this bit disabled, BAM could fetch descriptors for a pipe which was reset and no descriptors were added yet, if a retransmission request followed after the reset. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only

LPASS_BAM_CNFG_BITS (cont.)

Bits	Name	Description
24	BAM_REG_P_EN	Recommended value: 1 This bit fixes the pipe configuration signals mux for the current active pipe in 2 pipes BAM. When disabled, internal state machines might get into enabled states while the pipe is disabled. This would typically happen after pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
23	BAM_WB_DSC_AVL_P_RST	Recommended value: 1 This bit allows the Writeback state machine to reset the vector indicating there are available descriptors when a pipe reset occurs. If disabled, BAM might fetch descriptors after resetting and reconfiguring a pipe, even though no Event (descriptors) was provided. 1'b1 - Enable 1'b0 - Disable Available in BAM only
22	BAM_WB_RETR_SVPNT	Recommended value: 1 This bit fixes a bug where a pipe which was reset, still stored its retransmission savepoint, but into the illegal's pipe address space, thus hurting the last pipe of the BAM if the BAM had a total 4, 8 or 16 pipes. This is relevant for Producer to System modes only. (CR-0000151585) 1'b1 - Enabled 1'b0 - Disable Available in BAM only
21	BAM_WB_CSW_ACK_IDL	Recommended value: 1 This bit allows the Writeback state machine to switch into idle state prior to visiting disabled state. This is needed when context switching from mode X to another pipe of mode X is well. This is required to fix a bug in the 2 pipes BAM. 1'b1 - Enable 1'b0 - Disable Available in BAM only
20	BAM_WB_BLK_CSW	Recommended value: 1 When Enabled, this bit does not allow context switch to happen in the Writeback state machine until it has created a descriptor. This is relevant when the descriptor fifo is becoming full and there's no space to create a descriptor, while another pipe is context switching. This might result in the descriptor not to be created ever, if it was the last one for that pipe. Relevant for Producer BAM-to-BAM mode only. 1'b1 - Enable 1'b0 - Disable Available in BAM only

LPASS_BAM_CNFG_BITS (cont.)

Bits	Name	Description
19	BAM_WB_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Writeback state machine when performing pipe reset. 1'b1 - 1'b0 - Disable Available in BAM only
18	BAM_SI_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Sideband Inform state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
17	BAM_AU_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Ack Update state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
16	BAM_PSM_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Pipe state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
15	BAM_PSM_CSW_REQ	Recommended value: 1 This bit forces the context switch request from pipe state machine to RAM controller not to last longer than the slave requested. (2 Pipes BAM bug fix) 1'b1 - Enable 1'b0 - Disable Available in BAM only
14	BAM_SB_CLK_REQ	Recommended value: 1 This bit allows the clock request from the sideband block to propagate into the BAM's common clock request. 1'b1 - Propagate Sideband Clock Request 1'b0 - Disable Available in BAM only
13	BAM_IBC_DISABLE	Recommended value: 1 This bit helps to save power by allowing the BAM to keep the inactivity base counter in reset when BAM is disabled or when SW configures IBC_DISABLE bit high. 1'b1 - Enable Power Saving 1'b0 - Disable Power Saving

LPASS_BAM_CNFG_BITS (cont.)

Bits	Name	Description
12	BAM_NO_EXT_P_RST	Recommended value: 1 This bit allows the BAM / BAM Lite to ignore the externally connected blocks (eDML) when doing pipe reset. The BAM, once instructed to pipe reset, first thing lets the externally connected block know a reset is needed. Then it waits for the externally connected block to Acknowledge it is ready for the pipe reset (meaning it doesn't push any data for the reset pipe) and then the BAM Lite completes the pipe reset operation internally. When disabled, the BAM doesn't require any Acknowledge from the external block to perform pipe reset. 1'b1 - Enable external block pipe reset 1'b0 - Disable - ignore external block pipe reset
11	BAM_FULL_PIPE	Recommended value: 0 This enables the BAM support for a BAM to BAM Producer which insists to write to a full pipe. When 0, BAM might issue data overflow if producers write to a full pipe. When 1 BAM will not allow this and lower HReady when peripheral tries to do so. Once space is freed in the pipe, Hready will rise and the flow will continue. This functionality has been found to be buggy and was removed from APQ8064. Bit is currently unused. 1'b1 - Enable 1'b0 - Disable Available in BAM only
10:3	RESERVED_BITS10_3	Set to Zero (0)
2	BAM_PIPE_CNFG	Recommended value: 1 Pipe SM upgrade for writing EOT bit to the previous descriptor. It's invoked only when EOB arrives in the end of a descriptor. It is highly recommended to set this bit high. Leaving it low might cause incorrect Pipe Bytes Free value reported to peripheral in rare cases. 1'b1 - Enable 1'b0 - Disable Available in BAM only
1:0	RESERVED_BITS1_0	Set to Zero (0)

0x28085800+ 128*n LPASS_BAM_IRQ_SRCS_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking this register, SW reads

the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register has an alias - BAM_IRQ_SRCS register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

LPASS_BAM_IRQ_SRCS_EEn

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x28085804+ 128*n LPASS_BAM_IRQ_SRCS_MSK_EEn, n=[0..3]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register has an alias - BAM_IRQ_SRCS_MSK register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

LPASS_BAM_IRQ_SRCS_MSK_EEn

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x28085808+ 128*n LPASS_BAM_IRQ_SRCS_UNMASKED_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register has an alias - BAM_IRQ_SRCS_UNMASKED register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

LPASS_BAM_IRQ_SRCS_UNMASKED_EEn

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

12.7.2 BAM PIPE management registers

BAM Pipe management registers control each pipe's parameters. Those reside in physical registers.

0x28084000+ 128*n LPASS_BAM_P_CTRLn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Control register provides various controls for the pipe.

LPASS_BAM_P_CTRLn

Bits	Name	Description
31:11	RESERVED_BITS31_11	Set to Zero (0)
10:9	P_PREFETCH_LIMIT	Bam Lite feature Selects the number of bytes to be prefetched by the Bam Lite, once a peripheral requests to read data from a pipe. This feature is relevant for Consumer modes only. 2'b00 - 32 bytes at most (INCR8) 2'b01 - 16 bytes at most (INCR4) 2'b10 - 4 bytes at most (SINGLE) Available in BAM-Lite only

LPASS_BAM_P_CTRLn (cont.)

Bits	Name	Description
8:7	P_AUTO_EOB_SEL	Bam Lite feature. Selects the number of bytes to be processed before creating End Of Block indication internally by the BAM. See P_AUTO_EOB. Descriptors generated by this feature (bam to bam producer mode) will always be of the chosen size, unless an End Of Transfer, causes a smaller descriptor to be created. 2'b00 - 512 Bytes 2'b01 - 256 Bytes 2'b10 - 128 Bytes 2'b11 - 64 Bytes Available in BAM-Lite only
6	P_AUTO_EOB	BAM Lite feature. When Enabled, the BAM Lite will ignore any incoming End Of Block indications from the peripheral (if any). Instead, the BAM Lite will generate it's own End Of Block indications internally, every P_AUTO_EOB_SEL bytes. This feature is relevant for Producer Bam 2 Bam modes only. It is a must for peripherals which are not able to produce End Of Block indications. 1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
5	P_SYS_MODE	This bit sets the pipe to work in System Mode, where the Software is the second side of the pipe. 1'b1 - System mode. 1'b0 - BAM to BAM mode.
4	P_SYS_STRM	Streaming Enable. Relevant to System Producer BAM mode only.When enabled, BAM will not close descriptors with End Of Transfer notifications received from peripheral, but continue writing the data to the same descriptor. 1'b1 - Enable Streaming Mode 1'b0 - None-Streaming Mode
3	P_DIRECTION	This bit denotes pipe direction. 1'b1 - The pipe can be written (producer mode) 1'b0 - The pipe can be read (consumer mode)
2	RESERVED_BITS2	Set to Zero (0)
1	P_EN	1'b1 - Enable Pipe 1'b0 - Disable Pipe
0	RESERVED_BITS0	Set to Zero (0)

0x28084004+ 128*n LPASS_BAM_P_RSTn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Reset register provides Pipe Reset ability. Software needs to write 1 to this register to make the Pipe Reset. Writing 0 to this register will finish the Pipe Reset. Writing zero is needed prior to Peripheral reconfiguration for the same pipe.

LPASS_BAM_P_RSTn

Bits	Name	Description
31:1	RESERVED_BITS31_1	Set to Zero (0)
0	P_SW_RST	This resets the pipe and its' registers, (Both Flip-Flops and RAM). 1'b1 - Reset 1'b0 - Do Nothing

0x28084008+ 128*n LPASS_BAM_P_HALTn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Halt register Enables/Disables the Halt Sequence.

This is a self-modifying register.

LPASS_BAM_P_HALTn

Bits	Name	Description
31:2	RESERVED_BITS31_2	Set to Zero (0)
1	P_PROD_HALTED	This bit is used to inform the Consumer about the Producer being in Halt mode now. This is a part of the Halt procedure. 1'b1 - Sets this bit to 1 1'b0 - Does Nothing This bit will be cleared by the HW.
0	P_HALT	When Enabled, the Pipe will enter Halt Mode. 1'b1 - Enable Halt 1'b0 - Disable Halt For B2B Producer pipes, this bit is self modifying. It doesn't need the SW to clear it.

0x28084030+ 128*n LPASS_BAM_P_TRUST_REGn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

LPASS_BAM_P_TRUST_REGn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_P_VMID	Those bits indicate the VMID value to be used when performing Pipe type accesses to the bus. BAM Type accesses include Pipe MTI, Data and Descriptors.
7:2	RESERVED_BITS7_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_P_EE	This Field Indicates the EE (0,1,2,3) to which the Pipe Interrupt belongs to. The BAM interrupt will fire to the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x28084010+ 128*n LPASS_BAM_P_IRQ_STTSn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only. It also has informative bits which are not interrupts.

Clearing the interrupt bits is done by writing to P_IRQ_CLR register.

LPASS_BAM_P_IRQ_STTSn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_IRQ	For producer this interrupt happens whenever the last AHB burst of a transfer happens For Consumer when ack_on_success closes a transfer
4	P_ERR_IRQ	Pipe Error interrupt indicates that an error has happened. TBD: Error reason is not yet defined. Interrupt not in use.
3	P_OUT_OF_DESC_IRQ	Out of descriptors interrupt has several meanings depending on the operation mode: Producer - no free space in the descriptors fifo for adding a descriptor Consumer - no descriptors in the descriptors fifo for processing IO Vectors Producer - No descriptors to read (and therefore no space for data to write to the pipe) IO Vectors Consumer - No descriptors to read (and therefore no data to read from pipe)
2	P_WAKE_IRQ	Wake peripheral interrupt signals the driver to wake up the peripheral (USB for example) for transmission via the current pipe. This interrupt is issued whenever an Event comes to the specific pipe.
1	P_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
0	P_PRCSD_DESC_IRQ	This Interrupt rises when BAM finishes processing an IO Vector which has INT bit selected

0x28084014+128*n LPASS_BAM_P_IRQ_CLRn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

LPASS_BAM_P_IRQ_CLRn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_CLR	1’b1 - Clear 1’b0 - Unchanged
4	P_ERR_CLR	1’b1 - Clear 1’b0 - Unchanged
3	P_OUT_OF_DESC_CLR	1’b1 - Clear 1’b0 - Unchanged

LPASS_BAM_P_IRQ_CLRn (cont.)

Bits	Name	Description
2	P_WAKE_CLR	Clear Wake peripheral interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
1	P_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
0	P_PRCSD_DESC_CLR	Clear Descriptor Processed interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged

0x28084018+128*n LPASS_BAM_P_IRQ_ENn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the Pipe Interrupt Status register.

LPASS_BAM_P_IRQ_ENn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_EN	1'b1 - Enable 1'b0 - Disable
4	P_ERR_EN	1'b1 - Enable 1'b0 - Disable
3	P_OUT_OF_DESC_EN	1'b1 - Enable 1'b0 - Disable
2	P_WAKE_EN	Enable Wake peripheral interrupt 1'b1 - Enable 1'b0 - Disable
1	P_TIMER_EN	Enable Inactivity timer Interrupt 1'b1 - Enable 1'b0 - Disable
0	P_PRCSD_DESC_EN	Enable Descriptor Processed Interrupt 1'b1 - Enable 1'b0 - Disable

0x2808401C+ 128*n LPASS_BAM_P_TIMERn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the pipe.

LPASS_BAM_P_TIMERn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x28084020+ 128*n LPASS_BAM_P_TIMER_CTRLn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The resolution of the pipe inactivity timers are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the P_TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * P_TIMER_TRSHLD.

LPASS_BAM_P_TIMER_CTRLn

Bits	Name	Description
31	P_TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the P_TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	P_TIMER_RUN	Will be used along with P_TIMER_MODE Not implemented at this time. Set to zero(0)
29	P_TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	P_TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x28084024+ 128*n LPASS_BAM_P_PRDCR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Producer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

LPASS_BAM_P_PRDCR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_producer
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	BAM_P_TOGGLE	Pipe Bytes Free Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Free Ctrl value
15:0	BAM_P_BYTES_FREE	Pipe Bytes Free value

0x28084028+ 128*n LPASS_BAM_P_CNSMR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Consumer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

LPASS_BAM_P_CNSMR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_consumer
23	BAM_P_WAIT_4_ACK	waiting_for_ack_bytes_avail_r
22	BAM_P_ACK_TOGGLE	ack_bytes_avail_toggle
21	BAM_P_ACK_TOGGLE_R	ack_bytes_avail_toggle_r
20	BAM_P_TOGGLE	Pipe Bytes Avail Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Avail Ctrl value
15:0	BAM_P_BYTES_AVAIL	Pipe Bytes AVAIL value

12.7.3 BAM PIPE configuration registers (RAM)

BAM Pipe management registers configure each pipes' parameters.

Pipe Address span: currently defining each pipe to have 32 addresses, therefore inter pipe offset is 32*4=128=0x80 bytes.

0x2808502C+ 64*n LPASS_BAM_P_EVNT_DEST_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Event Destination Address which is the address of BAM_P_EVNT_REG in the BAM on the other side of the Pipe.

Producer BAM will send Write Events to this address.

Consumer BAM will send Read Events to this address.

This is relevant only for BAM to BAM modes. In System modes, BAM doesn't issue Write/Read events.

LPASS_BAM_P_EVNT_DEST_ADDRn

Bits	Name	Description
31:0	P_EVNT_DEST_ADDR	Address of the Event Register in the peer BAM (second end of the pipe). Driver will configure this when initializing the pipe.

0x28085018+ 64*n LPASS_BAM_P_EVNT_REGn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register is where Read/Write events are sent to. If current BAM works as Producer, it will receive Read events into this register from the Consumer. If the Consumer is another BAM, it will write read events to this register. If the Consumer is the Software, it will prepare descriptors in the descriptor FIFO and update the DESC_FIFO_PEER_OFST value in this register.

If current BAM works as Consumer, opposite behavior is assumed.

LPASS_BAM_P_EVNT_REGn

Bits	Name	Description
31:16	P_BYTES_CONSUMED	This field is used only in the B2B mode. It indicates the number of bits consumed by the Consumer. Consumer sends this value to the Producer as a part of a read event, for the Producer to know how many bytes were consumed. When working in System mode, this value should be set to zero. BAM to BAM Producer writes zero in this value.
15:0	P_DESC_FIFO_PEER_OFST	This field indicates the Descriptor Fifo Offset Pointer of the Peer BAM (The BAM or the Software which creates descriptors). For example when current BAM works as consumer for the current pipe, Producer BAM (or the software) updates this value to let the current pipe know about the new descriptors added in the Descriptor Fifo.

0x28085000+ 64*n LPASS_BAM_P_SW_OFSTSn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register denotes the pointer Offset of the first Not Acknowledged Descriptor. Meaning all Descriptors prior to this one have been processed by the BAM. This register is only used by the Software. After receiving an interrupt, software reads this register in order to know what descriptors has been processed.

When the BAM works as Producer, Software will usually read this value after Descriptor Processed Interrupt or after the End of Transfer Interrupt.

When the BAM works as Consumer, Software will usually read this value after Descriptor Processed Interrupt.

NOTE This is non relevant in BAM to BAM modes.

NOTE Although being Writable, Software should never write to this register.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

LPASS_BAM_P_SW_OFSTSn

Bits	Name	Description
31:16	SW_OFST_IN_DESC	Offset inside the Descriptor. This value is used by the Software only when a BAM is working as System Producer. Then the SW can read this value to know how many Bytes were written to the current descriptor if it was not closed down. This is useful for Streaming mode.
15:0	SW_DESC_OFST	Descriptor FIFO offset.

0x28085024+ 64*n LPASS_BAM_P_DATA_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Beginning of the Data Address space.

This register is non relevant in System Modes.

LPASS_BAM_P_DATA_FIFO_ADDRn

Bits	Name	Description
31:0	P_DATA_FIFO_ADDR	Data Address Space beginning.

0x2808501C+ 64*n LPASS_BAM_P_DESC_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Address of the Descriptor Fifo beginning.

NOTE This register is used by all modes.

LPASS_BAM_P_DESC_FIFO_ADDRn

Bits	Name	Description
31:0	P_DESC_FIFO_ADDR	Address of the Descriptors Fifo. This address must be 8 bytes aligned.

0x28085028+64*n LPASS_BAM_P_EVNT_GEN_TRSHLDn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register configures the threshold value for Read/Write event generation by the BAM towards another BAM. When a BAM pushes/pops this number of bytes to/from the pipe an event to the other BAM will be generated. A counter summing up the bytes pushed/popped is reset when event is issued, thus restarting count for the threshold.

Events are also issued after End Of Transfer received from the peripheral (Producer case), non regarding whether the pushed bytes count has reached the threshold or not.

This register is non relevant in System Modes.

LPASS_BAM_P_EVNT_GEN_TRSHLDn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TRSHLD	Threshold value. The maximum allowed value is 32kByte.

0x28085020+64*n LPASS_BAM_P_FIFO_SIZESn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

The least significant field is the Descriptor Fifo Size.

The most significant field is the Data Fifo Size.

NOTE This Descriptor Fifo Size is used by all modes. The Data Fifo Size is non relevant in System Modes.

LPASS_BAM_P_FIFO_SIZESn

Bits	Name	Description
31:16	P_DATA_FIFO_SIZE	Size of the Data Address Space.
15:0	P_DESC_FIFO_SIZE	Size of the Descriptors Fifo. Must be 8 byte aligned. Each descriptor is 8 bytes. Size of the descriptor fifo must contain an integer number of Descriptors.

12.7.4 BAM PIPE internal state registers (RAM)

BAM Pipe debug registers allow a software look inside on the internal parameters of the BAM State Machines stored in RAM.

Those shouldn't be normally used or altered by the software.

0x28085034+64*n LPASS_BAM_P_RETR_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context stored for retransmission.

This is being stored by Ack Update state machine in consumer mode or by the Writeback state machine in producer mode.

This is being loaded by the Writeback state machine when retransmission happens.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

LPASS_BAM_P_RETR_CNTXT_n

Bits	Name	Description
31:16	RETR_DESC_OFST	Descriptor Fifo Offset for retransmission.
15:0	RETR_OFST_IN_DESC	The Offset inside the Descriptor for retransmission.

0x28085038+64*n LPASS_BAM_P_SI_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Sideband Inform state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

LPASS_BAM_P_SI_CNTXT_n

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	SI_DESC_OFST	The Descriptor Fifo Offset pointer stored by the Sideband Inform state machine.

0x28085004+ 64*n LPASS_BAM_P_AU_PSM_CNTXT_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Ack Update state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

LPASS_BAM_P_AU_PSM_CNTXT_1_n

Bits	Name	Description
31:16	AU_PSM_ACCUMED	PSM: The acknowledged (EOB/T) number of bytes since last Write Event. AU: The accumulation of the descriptor sizes for the present ack_on_success event. This is never bigger than the ACKED field. Once the ACCUMED values are bigger than Event Threshold, an Event will be issued, the ACKED value will decrease by the ACCUMED size and this value will be zeroed. This also serves as the Bytes Consumed value in the Event.
15:0	AU_ACKED	AU: The left over of the number of bytes that were received via the ack_on_success, that did not cause a descriptor closure. This value is down counting upon issuing Read Event. PSM:

0x28085008+ 64*n LPASS_BAM_P_PSM_CNTXT_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

LPASS_BAM_P_PSM_CNTXT_2_n

Bits	Name	Description
31	PSM_DESC_VALID	The Descriptor Valid bit provided by the Writeback state machine to Pipe state machine.
30	PSM_DESC_IRQ	The Descriptor Interrupt bit provided by the Writeback state machine to pipe state machine.
29	PSM_DESC_IRQ_DONE	The Descriptor Interrupt needed selection bit.
28:25	PSM_GENERAL_BITS	General Context Switch Bits
24:22	PSM_CONS_STATE	State of the Pipe Consumer state machine.
21:19	PSM_PROD_SYS_STATE	State of the Pipe Producer System state machine.
18:16	PSM_PROD_B2B_STATE	State of the Pipe Producer BAM to BAM state machine.
15:0	PSM_DESC_SIZE	The Descriptor Size provided by the Writeback state machine to pipe state machine.

0x2808500C+ 64*n LPASS_BAM_P_PSM_CNTXT_3_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

LPASS_BAM_P_PSM_CNTXT_3_n

Bits	Name	Description
31:0	PSM_DESC_ADDR	The Data Address provided in the current descriptor from the Writeback state machine.

0x28085010+ 64*n LPASS_BAM_P_PSM_CNTXT_4_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

LPASS_BAM_P_PSM_CNTXT_4_n

Bits	Name	Description
31:16	PSM_DESC_OFST	The running Descriptor Fifo Offset of the Writeback state machine
15:0	PSM_SAVED_ACCUMED_SIZE	The Saved Accumulated Size from the Pipe state machine.

0x28085014+64*n LPASS_BAM_P_PSM_CNTXT_5_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

LPASS_BAM_P_PSM_CNTXT_5_n

Bits	Name	Description
31:16	PSM_BLOCK_BYTE_CNT	The Byte count inside the current Block.
15:0	PSM_OFST_IN_DESC	The Offset inside a register. This is used by pipe state machine to compute offset inside a register after retransmission

0x28085030+64*n LPASS_BAM_P_RESERVED_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

LPASS_BAM_P_RESERVED_1_n

Bits	Name	Description
31:0	BAM_P_RES_1	Set to zero (0) Reserved

0x2808503C+64*n LPASS_BAM_P_RESERVED_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

LPASS_BAM_P_RESERVED_2_n

Bits	Name	Description
31:0	BAM_P_RES_2	Set to zero (0) Obsolete Register: BAM_P_IRQ_DEST_ADDRn, n=[0..30]

12.8 MIDI CORE Registers (0x28200000 MIDI_BASE)

This section contains MIDI core registers.

12.8.1 Config Registers

0x28200000 MIDI_CORE_CONTROL

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

This register is used to control core operations and to enable/disable clocks for the sub-blocks.

MIDI_CORE_CONTROL

Bits	Name	Description
31:16	SUM_BUF_LOCK	Each bit corresponds to locking a section of the summing buffer. and so on... NOTE Each sum buffer line is read as 2 32-bit words, and hence locking granularity here is 64 32-bit words. 0x1F: sum_buffer to sum_buff_1 0x1E: sum_buffer to sum_buff_2 0x11: sum_buffer to sum_buff_3 0x10: sum_buffer to sum_buff_4
15:14	RESERVED_15_14	
13	WFU_SKIP_PHASE_ENABLE	Set (1) to stop the WFU from sending the fractional phase back to the PE.
12	SVRLINK_LOAD_ENABLE	Set (1) to enable link list and SVR loading.
11	SUM_ENABLE	Set (1) to enable sum buffer operation
10	WFU_ENABLE	Set (1) to enable WFU operation
9	LFO_ENABLE	Set (1) to enable LFO operation
8	WFU_INVALIDATE_ENABLE	Set (1) to enable the WFU cache invalidate at the beginning of the SVR list processing.
7	RESERVED_7	
6	PE_ENABLE_2	Set (1) to enable the processing element 2. This bit needs to be set to program the program RAM for processing element 2.
5	PE_ENABLE_1	Set (1) to enable the processing element 1. This bit needs to be set to program the program RAM for processing element 1.
4	PE_ENABLE_0	Set (1) to enable the processing element 0. This bit needs to be set to program the program RAM for processing element 0.

MIDI_CORE_CONTROL (cont.)

Bits	Name	Description
3	SUM_CLEAR_ENABLE	Set (1) to enable/disable the summing buffer clear at the beginning of the SVR list.
2	PREEMPT	Set (1) to preempt core functionality and return with ADSP interrupt as soon as all current SVRs are synthesized.
1	OFSM_ENABLE	Set (1) to enable overall state machine operation. If 0, then registers can be programmed, but there won't be core activity. For programming program RAMs, this bit must be 0.
0	TEST_MODE	Set (1) to initiate a built-in self-test.

0x28200004 MIDI_LINK_BASE

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_LINK_BASE

Bits	Name	Description
31:2	VALUE	This bit field is a 32-bit word-aligned base of the link list. Entries of the link list give the SVR number, which is multiplied by SVR offset to get the actual address of the SVR.
1:0	RESERVED_1_0	

0x28200008 MIDI_SVR_BASE

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_SVR_BASE

Bits	Name	Description
31:2	VALUE	This bit field is a 32-bit word-aligned AHB word address of the SVR record. This field is used in addition to the MIDI_SVR_OFFSET thus base of SVR(n) = MIDI_SVR_OFFSET * MIDI_LINK_BASE(n) MIDI_SVR_BASE.
1:0	RESERVED_1_0	

0x2820000C MIDI_SVR_TOTAL_LENGTH

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_SVR_TOTAL_LENGTH

Bits	Name	Description
31:10	RESERVED_31_10	
9:2	VALUE	Size in words (32 bits) of a single SVR record type. For N words, program N in this register.
1:0	RESERVED_1_0	

0x28200010 MIDI_NUM_OF_SVRS

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_NUM_OF_SVRS

Bits	Name	Description
31:8	RESERVED_31_8	
7:0	VALUE	Number of SVRs to be processed. If N SVRs need to be processed, program N-1 in this register.

0x28200014 MIDI_SVR_HW_LENGTH

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_SVR_HW_LENGTH

Bits	Name	Description
31:9	RESERVED_31_9	
8:2	VALUE	Length of the SVR section that is fetched by hardware, specified in number of 32-bit words. If N words are to be fetched, program N-1.
1:0	RESERVED_1_0	

0x28200018 MIDI_SVR_RW_OFFSET

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_SVR_RW_OFFSET

Bits	Name	Description
31:9	RESERVED_31_9	
8:2	VALUE	Offset of the read/write section in the hardware fetched portion, specified in number of 32-bit words. This is the first word that is written back. If N words are fetched, program N-1.
1:0	RESERVED_1_0	

0x2820001C MIDI_SVR_RW_LENGTH

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_SVR_RW_LENGTH

Bits	Name	Description
31:9	RESERVED_31_9	
8:2	VALUE	Length of the read/write section in the hardware fetched portion, specified in number of 32 bit words. If N words are fetched, program N-1.
1:0	RESERVED_1_0	

0x28200020 MIDI_SAMPLES_PER_FRAME

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_SAMPLES_PER_FRAME

Bits	Name	Description
31:9	RESERVED_31_9	
8:0	VALUE	Number of samples per frame. If there are N samples, program N-1.

0x28200024 MIDI_INTR_ENABLE

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_INTR_ENABLE

Bits	Name	Description
31:17	RESERVED_31_17	
16	ARM_INTR	Enable the interrupt to ARM
15:6	RESERVED_15_6	
5	AXI_ERROR	Enable the AXI master error interrupt. valid only if MIDI has AXI master
4	AHB_ERROR	Enable the AHB error interrupt
3	TEST_ERROR	Enable the TM error interrupt
2	WFU_ERROR	Enable the WFU error interrupt
1	PE_DEC_ERROR	Enable the PE decoder error
0	SYNTH_DONE	Enable synthesis done interrupt

0x28200028 MIDI_INTR_STATUS

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_INTR_STATUS

Bits	Name	Description
31:16	RESERVED_31_16	
15:8	SVR_COUNT	Current number of SVR(s) processed. This field is read-only, and is equal to N where N is the number of SVRs processed.
7:6	RESERVED_7_6	
5	AXI_ERROR	Indicates an AXI error when set. This is only a status indicator.
4	AHB_ERROR	Indicates an AHB error when set. This is only a status indicator.
3	TEST_ERROR	Indicates a TM error when set. This is only a status indicator.
2	WFU_ERROR	Indicates WFU error when set. This is only a status indicator.
1	PE_DEC_ERROR	Indicates decoder error when set. This is only a status indicator.
0	SYNTH_DONE	Indicates synthesis done when set. To clear interrupt, write 1 to this bit.

0x2820002C MIDI_RESETS

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_RESETS

Bits	Name	Description
31:2	RESERVED_31_1	
1	AXI_BRIDGE_RESET	Resets the AXI bridge, not self clearing
0	OVERALL_RESET	Resets internal core including Xmemc registers, self clearing.

0x28200030 MIDI_PE_MISR

Type: Read
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

This register is used to read back the MISR values corresponding to each PE in test mode.

MIDI_PE_MISR

Bits	Name	Description
31:0	VALUE	Value of the PE MISR.

0x28200034 MIDI_PE_LFSR

Type: Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x12345678

This register is used to seed each PE separately, if needed, before putting the core in the test mode.

MIDI_PE_LFSR

Bits	Name	Description
31:0	SEED	Seed for the PE LFSR.

0x28200038 MIDI_BUS_STATS

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_BUS_STATS

Bits	Name	Description
31:0	COUNT	Total number of bus accesses since last clear.

0x2820003C MIDI_DEBUG_REG_01

Type: Read
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_DEBUG_REG_01

Bits	Name	Description
31:16	WFU_CACHE_TAG_0	The WFU cache tag for PE 0.
15:0	WFU_CACHE_TAG_1	The WFU cache tag for PE 1.

0x28200040 MIDI_DEBUG_REG_02

Type: Read
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_DEBUG_REG_02

Bits	Name	Description
31:16	WFU_CACHE_TAG_2	The WFU cache tag for PE 2.
15	WFU_TAG_0_VALID	The valid bit for PE 0's WFU cache.
14	WFU_TAG_1_VALID	The valid bit for PE 1's WFU cache.
13	WFU_TAG_2_VALID	The valid bit for PE 2's WFU cache.
12:10	WFU_OUTFSM_0_STATE	The WFU OUTFSM state for PE 0.
9:7	WFU_OUTFSM_1_STATE	The WFU OUTFSM state for PE 1.
6:4	WFU_OUTFSM_2_STATE	The WFU OUTFSM state for PE 2.
3:1	WFU_SRFSM_STATE	The WFU SRFSM state.
0	SB_CLRFSM_STATE	The SB CLRFSM state.

0x28200044 MIDI_DEBUG_REG_03

Type: Read
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_DEBUG_REG_03

Bits	Name	Description
31:29	WFU_ACRFSM_STATE	The WFU ACRFSM state.
28:27	WFU_OWFSM_STATE	The WFU OWFSM state.
26:24	TEST_STATE	The TM state.
23:22	SB_SBFSM_STATE	The SB SBFSM state.
21:6	SB_THERMOMETER	The SB internal SB RAM lock.
5:3	BUSIF_AHB_MASTER_STATE	The BUSIF AHB master state.
2:0	LFO_STATE	The LFO state.

0x28200048 MIDI_DEBUG_REG_04

Type: Read
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_DEBUG_REG_04

Bits	Name	Description
31:28	OFSM_STATE	The OFSM state.
27:20	OFSM_SVR_ID_0	The SVR ID being processed by PE 0.
19:12	OFSM_SVR_ID_1	The SVR ID being processed by PE 1.
11:4	OFSM_SVR_ID_2	The SVR ID being processed by PE 2.
3	OFSM_SVR_ID_0_VALID	Set if OFSM_SVR_ID_0 is valid.
2	OFSM_SVR_ID_1_VALID	Set if OFSM_SVR_ID_1 is valid.
1	OFSM_SVR_ID_2_VALID	Set if OFSM_SVR_ID_2 is valid.
0	BUSIF_AHB_CRIF2INT_STATE	The BUSIF AHB CRIF2INT state.

0x2820004C MIDI_DEBUG_REG_05

Type: Read
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_DEBUG_REG_05

Bits	Name	Description
31	BUSIF_XMEMC_CRIF2INT_STATE	The BUSIF XMEMC CRIF2INT state.
30	PE0_SVR_R_BUSY	Set if PE 0's SVR RAM read port is busy.
29:24	PE0_PC	The program counter for PE 0.
23:15	PE0_SUM_CNT	The sum counter value for PE 0.
14:9	PE1_PC	The program counter for PE 1.
8:0	PE1_SUM_CNT	The sum counter value for PE 1.

0x28200050 MIDI_DEBUG_REG_06

Type: Read
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_DEBUG_REG_06

Bits	Name	Description
31	PE1_SVR_R_BUSY	Set if PE 1's SVR RAM read port is busy.
30	PE2_SVR_R_BUSY	Set if PE 2's SVR RAM read port is busy.
29:24	PE2_PC	The program counter for PE 2.
23:15	PE2_SUM_CNT	The sum counter value for PE 2.
14:13	PE0_DEC_STATE	The PE 0 decoder state.
12:11	PE1_DEC_STATE	The PE 1 decoder state.
10:9	PE2_DEC_STATE	The PE 2 decoder state.
8	PE0_SVR_W_BUSY	Set if PE 0's SVR RAM write port is busy.
7	PE1_SVR_W_BUSY	Set if PE 1's SVR RAM write port is busy.
6	PE2_SVR_W_BUSY	Set if PE 2's SVR RAM write port is busy.
5	PE0_SB_R_BUSY	Set if PE 0's SB RAM read port is busy.
4	PE1_SB_R_BUSY	Set if PE 1's SB RAM read port is busy.
3	PE2_SB_R_BUSY	Set if PE 2's SB RAM read port is busy.

MIDI_DEBUG_REG_06 (cont.)

Bits	Name	Description
2	PE0_SB_W_BUSY	Set if PE 0's SB RAM write port is busy.
1	PE1_SB_W_BUSY	Set if PE 1's SB RAM write port is busy.
0	PE2_SB_W_BUSY	Set if PE 2's SB RAM write port is busy.

0x28200054 MIDI_DEBUG_REG_07

Type: Read
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_DEBUG_REG_07

Bits	Name	Description
31:9	RESERVED_31_9	
8	PE0_LFO_BUSY	Set if PE 0 interface to the LFO is busy.
7	PE1_LFO_BUSY	Set if PE 1 interface to the LFO is busy.
6	PE2_LFO_BUSY	Set if PE 2 interface to the LFO is busy.
5	PE0_WFU_R_BUSY	Set if PE 0 WFU RAM read port is busy.
4	PE1_WFU_R_BUSY	Set if PE 1 WFU RAM read port is busy.
3	PE2_WFU_R_BUSY	Set if PE 2 WFU RAM read port is busy.
2	PE0_WFU_W_BUSY	Set if PE 0 WFU RAM write port is busy.
1	PE1_WFU_W_BUSY	Set if PE 1 WFU RAM write port is busy.
0	PE2_WFU_W_BUSY	Set if PE 2 WFU RAM write port is busy.

0x28200058 MIDI_DEBUG_BUS_CTL

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

This register is used to switch/enable the test bus muxes and enable the BPM triggers.

MIDI_DEBUG_BUS_CTL

Bits	Name	Description
31:6	RESERVED_31_6	
5	ENA	Set (1) to enable the test bus.

MIDI_DEBUG_BUS_CTL (cont.)

Bits	Name	Description
4	BPM_MODE	Set (1) to switch to level mode trigger. Clear (0) for edge mode trigger.
3:0	SEL	Test mode is as specified in the Debug table/spreadsheet.

0x28200060 MIDI_CONFIG_SPARE_0

Type: Read/Write
Clock: ADSP_AHB_AS_APPLICABLE
Reset State: 0x00000000

MIDI_CONFIG_SPARE_0

Bits	Name	Description
31:8	RESERVED_31_8	Reserved
7:0	SPARE	This address range is reserved as a spare for ECOs.

12.8.2 Data Registers

0x28203700 MIDI_DATA_SPARE_0

Type: Read/Write
Clock: AHB
Reset State: 0x00000000

MIDI_DATA_SPARE_0

Bits	Name	Description
31:8	RESERVED_31_8	Reserved.
7:0	SPARE	This address range is reserved as a Spare for ECOs.

12.9 LPA SS QDSP6 SS Public Registers (0x28800000 LPASS_QDSP6SS_PUB_BASE)

This section contains the Low Power Audio Subsystem (LPASS) QDSPSS Public registers.

These registers configure some of the settings for QDSP6 and QDSP6SS. The base address for these registers is configurable. They belong to uncacheable address space of QDSP6.

0x28800000 LPASS_QDSP6SS_RST_EVB

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

This register contains the QDSP6 event vector table base address. These 20 bits define the boot address for QDSP6.

LPASS_QDSP6SS_RST_EVB

Bits	Name	Description
31:24	RESERVED_BITS_31_24	Reserved
23:0	EVB	Event vector table base address. This corresponds to bits 31:8 of the address bits.

0x28800004 LPASS_QDSP6SS_RESET

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x32

This register is used to control reset.

LPASS_QDSP6SS_RESET

Bits	Name	Description
31:6	RESERVED_BITS_31_6	Reserved
5	PRIV	Software reset for the QDSP6SS private peripheral. 0x1: Active
4	STOP_CORE	Software stop core out of reset and only TCM is out of reset when CORE reset is de-asserted 0x1: Active
3	ETM	Software reset for the QDSP6 ETM. 0x1: Active

LPASS_QDSP6SS_RESET (cont.)

Bits	Name	Description
2	ISDB	Software reset for the QDSP6 ISDB. 0x1: Active
1	CORE	Software reset for the QDSP6 core. 0x1: Active
0	SS	Software reset for the QDSP6SS. 1 Active, resets the QDSP6SS. Since it will assert qdsp6_clamp_io, resetting the subsystem should always be accompanied by resetting QDSP6. To program any other registers in the subsystem, this bit needs to be set to 0.

0x28800008 LPASS_QDSP6SS_STRAP_ACC

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x0

This register contains the ACC values of all the memories inside the QDSP6 hardmacro.

LPASS_QDSP6SS_STRAP_ACC

Bits	Name	Description
31:24	UNUSED_31_24	Reserved, writeable
23:22	L2_DATA_WACC	Write ACC for L2 data
21:16	L2_DATA_RACC	Read ACC for L2 data
15:14	RESERVED_BITS_15_14	Reserved
13:12	OTHER_WACC	Shared write ACC for ITCM, ETB and L2 Tag
11	RSERVED_BITS_11	Reserved
10:7	OTHER_RACC	Shared read ACC for ITCM, ETB and L2 Tag
6:5	DU_DATA_WACC	Write ACC for DU data Array
4	RESERVED_BITS_4	Reserved
3:0	DU_DATA_RACC	Read ACC for DU data array

0x2880000C LPASS_QDSP6SS_DCC_CTRL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

This register contains control value for the duty cycle corrector inside QDSP6 hardmacro.

LPASS_QDSP6SS_DCC_CTRL

Bits	Name	Description
31:0	CTRL	Control value for the Duty cycle corrector

0x28800010 LPASS_QDSP6SS_NMI

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

This register controls QDSP6 non-maskable interrupt (NMI) signal.

LPASS_QDSP6SS_NMI

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	SET	0x0: Disabled 0x1: ENABLED (assert the QDSP NMI IRQ signal)

0x28800018 LPASS_QDSP6SS_CGC_OVERRIDE

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000010

This register controls various CGC overrides in QDSP6 subsystem and core.

LPASS_QDSP6SS_CGC_OVERRIDE

Bits	Name	Description
31:11	RESERVED_BITS_31_11	Reserved
10	AHBM_HCLK_EN	When reset (0), it enables the QDSP6 AHBM_HCLK to be gated off. When set (1), the AHBM_HCLK runs whenever there is cc_ahb_clk. Leave the bit clear for normal operations.
9	AXIS_ACLK_EN	When reset (0), it enables the QDSP6 AXIS_ACLK to be gated off if this bus is not used. When set (1), AXIS_ACLK is always running. Leave the bit clear for normal operations.
8	TEST_HCLK_EN	When reset (0), it enables the crpc_test_ahb_gclk to be gated off if testbus and TCXO counter are disabled. When set (1), the crpc_test_ahb_gclk runs whenever there is cc_ahb_clk. Leave the bit clear for normal operations.

LPASS_QDSP6SS_CGC_OVERRIDE (cont.)

Bits	Name	Description
7	L2VIC_HCLK_EN	When reset (0), it enables the crpc_l2vic_ahb_gclk to be gated. It will add 2 additional AHB clocks for interrupt latency. When set (1), the crpc_l2vic_ahb_gclk runs whenever there is cc_ahb_clk. Leave the bit clear for power savings. Set the bit to 1 if minimal interrupt latency is required.
6	TCXO_CLK_EN	When reset (0), it enables TCXO clock to be gated. When set (1), the TCXO clock is always running.
5	TIMER_HCLK_EN	When reset (0), it enables the crpc_timer_ahb_gclk to be gated off if all timers are disabled. When set (1), the crpc_timer_ahb_gclk runs whenever there is cc_ahb_clk. Leave the bit clear for normal operations.
4	PUB_HCLK_EN	crpc_pub_ahb_gclk is used for doing the AHB transactions to public CSR registers. When this bit is reset(0), it enables the crpc_pub_ahb_gclk to be gated off when there are no AHB transactions. When set(1), the crpc_pub_ahb_gclk runs whenever there is cc_ahb_clk. The reset value for this bit is 0x1
3	CSR_HCLK_EN	crpc_csr_ahb_gclk is used for doing the AHB transactions to AHB router and private CSR. The qdsp6 core, crpc, ugpt, rgpt, AVS. controller and tcxo_counter operate on the ungated cc_ahb_clk. When this EN bit is reset (0), this enables the crpc_ahb_gclk to be gated off. When set (1), the crpc_ahb_gclk runs whenever there is cc_ahb_clk.
2	CORE_BUS_EN	0x0: hardware clock gating enabled 0x1: force on QDSP6 bus clk
1	CORE_RCLK_EN	0x0: hardware clock gating enabled 0x1: force on QDSP6 core rclk
0	CORE_CLK_EN	0x0: hardware clock gating enabled 0x1: force on QDSP6 core clk

0x2880001C LPASS_QDSP6SS_STRAP_TCM

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x02000000

These bits define the upper bits of the TCM base and the config table. If the core accesses any address within the TCM config/TCM region, it goes to TCM config/TCM. Otherwise, it goes to either AHB or AXI access. The TCM address space must be at 4 MB boundary.

The default value of this register does not match with SoC address map necessarily. It must be programmed before QDSP6 is out of reset.

LPASS_QDSP6SS_STRAP_TCM

Bits	Name	Description
31:27	RESERVED_BITS_31_27	Reserved
26:16	BASE_ADDR	QDSP TCM Base Address
15:0	RESERVED_BITS_15_0	Reserved

0x28800020 LPASS_QDSP6SS_STRAP_AHB

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00A10A00

These bits define the upper and lower bits for the AHB boundary. If the address is between the upper AHB address (exclusive) and lower AHB address (inclusive) and not for the TCM configuration space, it is decoded and sent to the AHB interface. The AHB address space must be at 16 MB boundary.

The default value of this register does not match with SoC address map necessarily. It must be programmed before QDSP6 is out of reset.

LPASS_QDSP6SS_STRAP_AHB

Bits	Name	Description
31:24	RESERVED_BITS_31_24	Reserved
23:16	UPPER_ADDRESS	QDSP6 AHB Upper Address
15:12	RESERVED_BITS_15_12	Reserved
11:4	LOWER_ADDRESS	QDSP6 AHB Lower Address
3:0	RESERVED_BITS_3_0	Reserved

0x28800024 LPASS_QDSP6SS_EXT_WAKEUP

Type: Write (Command)
Clock: AHB_CLOCK
Reset State: 0x0

This register is used by external processor to start the wakeup process. To enable this feature, QDSP6 must program 1 to CSR register QDSP6SS_SLPC_CFG bit EXT_WAKEUP_ENA.

LPASS_QDSP6SS_EXT_WAKEUP

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	CMD	Write 1 starts wakeup process.

0x28800028 LPASS_QDSP6SS_EXT_PD

Type: Write (Command)
Clock: AHB_CLOCK
Reset State: 0x0

This register is used by external processor to continue the power down process. To enable this feature, QDSP6 must program 1 to CSR register QDSP6SS_SLPC_CFG bit PD_SRC_SEL. The external processor must respond to QDSP6 core idle interrupt and write 1 to QDSP6SS_EXT_PD when it is ready for QDSP6SS to proceed with actual power down.

LPASS_QDSP6SS_EXT_PD

Bits	Name	Description
31:1	RESERVED_BITS_31_1	Reserved
0	CMD	Write 1 starts power down process.

0x2880002C LPASS_QDSP6SS_ZMEAS_CONFIG

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x0

This register is used to control impedance measurement circuit.

LPASS_QDSP6SS_ZMEAS_CONFIG

Bits	Name	Description
31:24	RESERVED_BITS_31_24	Reserved
23:5	ZMEAS_COUNT	19-bit count value for setting the clock divides value. This directly determines the resonance cycle time period.
4	MUX_SEL	0 normal functional mode. The output from the circuit in not used 1 The output from the circuit is connected to GFMUX input d for impedance measurement
3	ZMEAS_CLK_R_ENA	Gates the output clock of the circuit regardless of how bypass is set. CGC_EN bit must be set in order for this enable to take effect.

LPASS_QDSP6SS_ZMEAS_CONFIG (cont.)

Bits	Name	Description
2	ZMEAS_CGC_EN	It activates the internal clock "CGC" so that activity is present only when the circuit is in use. When cleared, the internal FSM clock is not active to save power.
1	ZMEAS_BYPASS	When set, it enables which passes the input clock to the unit's output pin "clk_divn" so as to appear continuous and undivided
0	ZMEAS_SW_RESET	When set, it resets the circuit

0x28800030 LPASS_QDSP6SS_GFMUX_CTL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x102

This register is used for QDSP6 core clock GFMUX control

LPASS_QDSP6SS_GFMUX_CTL

Bits	Name	Description
31:10	RESERVED_BITS_31_10	Reserved
9	IDLE_CORE_CLK_EN	When reset (0), it enables core clock gating if QDSP6 core is idle. When set (1), the core clock keeps running even if QDSP6 core is idle.
8	SRC_SWITCH_CLK_OVR	0x1: force clock on during source switch 0x0: Not force clock on during source switch
7:4	RESERVED_BITS_7_4	Reserved
3:2	CLK_SRC_SEL	GFMUX clock source select
1	CLK_ENA	SW enable for QDSP6 core clock from GFMUX 0x0: QDSP6 core clock is off 0x1: QDSP6 core clock in on, if dynamic clock gating is enabled, the clock is under hardware control
0	CLK_ARES	Reset GFMUX

0x28800034 LPASS_QDSP6SS_GFMUX_STATUS

Type: Read
Clock: AHB_CLOCK
Reset State: NA

This register reads GFMUX status during clock source switching.

LPASS_QDSP6SS_GFMUX_STATUS

Bits	Name	Description
31:5	RESERVED_BITS31_5	Reserved
4:1	SEL_STATUS	Reflect the sel value (sel_d, sel_c, sel_b, sel_a) **NOTE** The bits are all 0 if clock is halted
0	SWITCH_STATUS	0x1: GFMUX has yet to switch to new clock source 0x0: GFMUX matches the clock source selection

0x28800038 LPASS_QDSP6SS_PWR_CTL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x7D

This register is used for QDSP6 CORE power control sequence directly by SW during initial PON boot up or when SPM is not used.

LPASS_QDSP6SS_PWR_CTL

Bits	Name	Description
31:7	RESERVED_BITS_31_7	Reserved
6	CLAMP_IO	Assert QDSP6 core clamp when set to 1. Must be programmed to 0 before boot up QDSP6
5	ARR_STBY_N	De-assert active low memory arr_stby_n when set to 0. Must be programmed to 1 before boot up QDSP6
4	ETB_SLP_NRET_N	De-assert active low ETB memory non-retention sleep signal when set to 0. Must be programmed to 0 before boot up QDSP6
3	L2TAG_SLP_NRET_N	De-assert active low L2TAG memory non-retention sleep signal when set to 0. Must be programmed to 0 before boot up QDSP6
2	L1TCM_SLP_NRET_N	De-assert active low L1TCM memory non-retention sleep signal when set to 0. Must be programmed to 0 before boot up QDSP6
1	SLP_RET_N	De-assert active low QDSP6 memory retention sleep signal when set to 0. Must be programmed to 0 before boot up QDSP6
0	L2DATA_SLP_NRET_N	De-assert active low L2DATA memory non-retention sleep signal when set to 0. Must be programmed to 0 before boot up QDSP6

0x2880003C LPASS_QDSP6SS_FLL_CTL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x0

This register is used for QDSP6 frequency locked loop (FLL) control. FLL is a low power alternative to PLL for QDSP6 core clock.

LPASS_QDSP6SS_FLL_CTL

Bits	Name	Description
31:28	RESERVED_BITS_31_28	Reserved
27:16	M	FLL M value
15:11	N	FLL N value
10:3	DCO_INIT	Initial value of FLL DCO
2	CLK_SEL	0x0: select normal clk source 0x1: select FLL clock
1	RESET	0x0: Do nothing 0x1: Assert FLL reset
0	ENA	0x0: disable FLL 0x1: enable FLL

0x28800040 LPASS_QDSP6SS_FLL_STATUS

Type: Read
Clock: AHB_CLOCK
Reset State: NA

This register is used for QDSP6 FLL status. The register needs to be read multiple times for accurate value, due to the implementation of clock gating.

LPASS_QDSP6SS_FLL_STATUS

Bits	Name	Description
31:9	RESERVED_BITS_31_9	Reserved
8:1	DCO_CURRENT	Current FLL DCO value. It needs multiple reads for a correct value due to possible delay variation between multiple bits
0	LOCKED	0x0: FLL not locked 0x1: FLL locked

0x28800048 LPASS_QDSP6SS_TEST_BUS_CTL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0000_0000

QDSP6SS_TEST_BUS_CTL controls the test bus muxes in the QDSP6SS. The TESTBUS_EN field is used to enable testbus and the clock to synchronize testbus value to register QDSP6SS_TEST_BUS_VALUE. When not enabled, the test bus sources hold the test bus at 0 to save power. The Q6_SEL field is used to choose between QDSP6 core or QDSP6 subsystem. The field SEL only lists selections for subsystem test bus. For QDSP6 testbus selection, refer to the QDSP6 document.

LPASS_QDSP6SS_TEST_BUS_CTL

Bits	Name	Description
31:24	SPARE_CFG	Spare r/w bits available for ECOs.
23:18	RESERVED_BITS23_18	Reserved
17	TESTBUS_EN	0x1: enable testbus 0x0: disable testbus
16	Q6_SEL	Select the test bus from QDSP6 or QDSP6SS 0x0: SUBSYSTEM_EN 0x1: Q6_EN

LPASS_QDSP6SS_TEST_BUS_CTL (cont.)

Bits	Name	Description
15:0	SEL	When bit[16]=0, select the test bus from QDSP6SS. 0x0: NONE 0x1: POWER_CNTL 0x2: UGPT_COUNT 0x3: RGPT_COUNT 0x4: IDLT_COUNT 0x5: CRPC 0x6: TCXOC_COUNT 0x7: JTAG 0x8: SAW_WRAPPER 0x9: WDOG_WRAPPER 0xA: SLPC 0xB: L2VIC 0xC: TESTBUS_WDATA 0x20: INT_SRC_31_0 0x21: INT_SRC_63_32 0x22: INT_SRC_95_64 0x23: INT_SRC_127_96 0x24: INT_SRC_159_128 0x25: INT_SRC_191_160 0x26: INT_SRC_223_192 0x27: INT_SRC_255_224 0x28: INT_SRC_287_256 0x29: INT_SRC_319_288 0x2A: INT_SRC_351_320 0x2B: INT_SRC_383_352 0x2C: INT_SRC_415_384 0x2D: INT_SRC_447_416 0x2E: INT_SRC_479_448 0x2F: INT_SRC_511_480 0x30: INT_SRC_543_512 0x31: INT_SRC_575_544 0x32: INT_SRC_607_576 0x33: INT_SRC_639_608 0x34: INT_SRC_671_640 0x35: INT_SRC_703_672 0x36: INT_SRC_735_704 0x37: INT_SRC_767_736 0x38: INT_SRC_799_768 0x39: INT_SRC_831_800 0x3A: INT_SRC_863_832 0x3B: INT_SRC_895_864 0x3C: INT_SRC_927_896 0x3D: INT_SRC_959_928 0x3E: INT_SRC_991_960 0x3F: INT_SRC_1023_992

0x2880004C LPASS_QDSP6SS_TEST_BUS_VALUE

Type: Read
Clock: AHB_CLOCK
Reset State: NA

This register is used for accessing testbus values during debug.

LPASS_QDSP6SS_TEST_BUS_VALUE

Bits	Name	Description
31:0	VALUE	The data may have incorrect value due to timing difference between signals

0x28800050 LPASS_QDSP6SS_TEST_BUS_WDATA

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x0

This register is used for driving testbus values during debug.

LPASS_QDSP6SS_TEST_BUS_WDATA

Bits	Name	Description
31:0	VALUE	

0x28800054 LPASS_QDSP6SS_TEST_CLK_CTL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0000_0000

The QDSP6SS_TEST_CLK_CTL register selects the high speed and low speed test clocks to be output from the QDSP6SS to the chip's clock controller.

LPASS_QDSP6SS_TEST_CLK_CTL

Bits	Name	Description
31:5	RESERVED_BITS31_5	Reserved
4	Q6_DBG_CLK_EN	Selects the high speed clock to output for test mode 0x0: No clock selected, tied low. 0x1: QDSP6 core clock (non-inverted or inverted - determined by Q6_DBG_CLK_INV)

LPASS_QDSP6SS_TEST_CLK_CTL (cont.)

Bits	Name	Description
3	Q6_DBG_CLK_INV	When set (1), selects inverted QDSP6 core clock
2:0	DBG_LS_CLK_SEL	Selects the local clock to output for test mode 0x0: No clock selected, tie_1 0x1: AXI master clock 0x2: AXI slave clock 0x3: QDSP6SS ahb clock 0x4: No clock selected, tie_2 0x5: XO clock 0x6: Sleep (RGPT timer clock) 0x7: JTAG TCK

12.10 LPA SS QDSP6 SS Slave Registers (0x28880000 LPASS_QDSP6SS_CSR_BASE)

This section contains the Low Power Audio Subsystem (LPASS) QDSP6SS CSR AHB Slave registers.

These registers belong to the CSR AHB slave in the QDSP6SS. The base address for these registers is configurable. They belong to uncacheable address space of QDSP6.

12.10.1 RTOS general purpose timer registers

0x28880000 LPASS_QDSP6SS_RGPT_MATCH_VAL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x00000000

The QDSP6SS_RGPT_MATCH_VAL register contains the RGPT timer match value. The RTOS general purpose timer generates an interrupt to QDSP6 when its counter value reaches this match value. Due to the synchronization to the slow 32 kHz timer clock, we should not program the match value to be less than 3 ticks from the timer's current value as obtained from reading RGPT_COUNT_VAL register.

LPASS_QDSP6SS_RGPT_MATCH_VAL

Bits	Name	Description
31:0	MATCH	During the reset, the count gets initialized to zero. If the timer is enabled, it starts counting up in SLP_CLK domain. An interrupt is generated if the count reaches this programmed match value.

0x28880004 LPASS_QDSP6SS_RGPT_COUNT_VAL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_RGPT_COUNT_VAL register returns the current value of the RGPT timer. It should be considered read-only for software. The count value is writable ONLY as a test/debug feature.

Writing this register ALSO changes the QDSP6SS_RGPT_MATCH_VAL register at the same time due to HW reuse. The procedure for writing the QDSP6SS_RGPT_COUNT_VAL is as follows:

1. Disable the timer by clearing the EN bit in QDSP6SS_RGPT_ENABLE.
2. Write QDSP6SS_RGPT_COUNT_VAL.
3. Make sure that the COUNT_VAL is written by reading the QDSP6SS_RGPT_COUNT_VAL

4. Write (to set/restore) QDSP6SS_RGPT_MATCH_VAL, if required.
5. Enable the timer by setting the EN bit in QDSP6SS_RGPT_ENABLE.

LPASS_QDSP6SS_RGPT_COUNT_VAL

Bits	Name	Description
31:0	COUNT	When read, it specifies the current value of the COUNTER. If written the timer starts to count from the written value. Follow the procedure mentioned above for writing the timer.

0x28880008 LPASS_QDSP6SS_RGPT_ENABLE

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x00000000

The QDSP6SS_RGPT_ENABLE register is used to enable the RGPT timer.

LPASS_QDSP6SS_RGPT_ENABLE

Bits	Name	Description
31:9	RESERVED_BITS31_9	Reserved
8:2	STATUS	Due to the synchronization between the ahb_clk (which programs the timer) and the SLP_CLK (the clock at which the timer runs), it might take up to one SLP_CLK cycle to transfer the AHB_CLK programmed values to SLP_CLK registers. These status bits read back the internal status. bit 8: rtos timer is still under reset after the subsystem reset. bit 7: write transaction to QDSP6SS_RGPT_MATCH_VAL is pending. bit 6: write transaction to QDSP6SS_RGPT_ENABLE is pending. bit 5: write transaction to QDSP6SS_RGPT_COUNT_VAL is pending. bit 4: write transaction to QDSP6SS_RGPT_CLEAR is pending. bit 3: CLR_ON_MATCH_EN in SLP_CLK domain bit 2: EN in SLP_CLK domain
1	CLR_ON_MATCH_EN	When set (1), the TIMER clears when it reaches the match value.
0	EN	When set (1), the TIMER is enabled and counts with frequency SLP_CLK

0x2888000C LPASS_QDSP6SS_RGPT_CLEAR

Type: Write (Command)
Clock: AHB_CLK
Reset State: NA

The QDSP6SS_RGPT_CLEAR register is a one-shot command register that, when written with any value, resets the TIMER to a value of 0. This occurs regardless of the state of the QDSP6SS_RGPT_ENABLE register.

Upon clearing the counter with RGPT_CLEAR command, the immediate following RGPT_COUNT_VAL read returns zero even if the command has not synchronized and takes effect in the timer hardware. Software may read RGPT_ENABLE(4) to determine whether the command has taken full effect.

LPASS_QDSP6SS_RGPT_CLEAR

Bits	Name	Description
31:0	RESERVED_BITS31_0	Reserved

12.10.2 Idle timer registers

0x28881000 LPASS_QDSP6SS_IDLT_MATCH_VAL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x00000010

The QDSP6SS_IDLT_MATCH_VAL register contains the idle timer match value. The idle timer starts counting if the QDSP6 core is in all-wait (i.e., QDSP6_core_state is 1). It generates an interrupt to QDSP6 when its counter value reaches this match value. If the QDSP6 is active, the counter will be reset and held at 0. Due to the synchronization to the slow 32 kHz timer clock, we should not program the match value to be less than 3.

LPASS_QDSP6SS_IDLT_MATCH_VAL

Bits	Name	Description
31:0	MATCH	During the reset, the count gets initialized to zero. If the timer is enabled, it starts counting up in SLP_CLK domain. An interrupt is generated if the count reaches this programmed match value.

0x28881004 LPASS_QDSP6SS_IDLT_COUNT_VAL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_IDLT_COUNT_VAL register returns the current value of the idle timer. It should be considered debug-only feature.

NOTE It will be automatically held to 0 when QDSP6 is active.

LPASS_QDSP6SS_IDLT_COUNT_VAL

Bits	Name	Description
31:0	COUNT	When read, it specifies the current value of the COUNTER. If written, the timer starts to count from the written value. Follow the procedure mentioned above for writing the timer.

0x28881008 LPASS_QDSP6SS_IDLT_ENABLE

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x00000000

The QDSP6SS_IDLT_ENABLE register is used to enable the idle timer.

LPASS_QDSP6SS_IDLT_ENABLE

Bits	Name	Description
31:9	RESERVED_BITS31_9	Reserved
8:2	STATUS	Due to the synchronization between the ahb_clk (which programs the timer) and the SLP_CLK (the clock at which the timer runs), it might take up to one SLP_CLK cycle to transfer the AHB_CLK programmed values to SLP_CLK registers. These status bits read back the internal status. bit 8: rtos timer is still under reset after the subsystem reset. bit 7: write transaction to QDSP6SS_IDLT_MATCH_VAL is pending. bit 6: write transaction to QDSP6SS_IDLT_ENABLE is pending. bit 5: write transaction to QDSP6SS_IDLT_COUNT_VAL is pending. bit 4: Reserved, always 0. bit 3: CLR_ON_MATCH_EN in SLP_CLK domain bit 2: EN in SLP_CLK domain
1	CLR_ON_MATCH_EN	When set (1), the TIMER clears when it reaches the match value.

LPASS_QDSP6SS_IDLT_ENABLE (cont.)

Bits	Name	Description
0	EN	When set (1), the TIMER is enabled and counts with frequency SLP_CLK

12.10.3 Watchdog timer registers

The watchdog registers exists in ahb_clock domain and they are reset by SS reset or private peripheral reset. The watchdog timer runs at a separate sleep_clock.

NOTE When QDSP6 is in debug mode (ISDB break), the watchdog timer is halted to keep its current value until QDSP6 is resumed in normal mode. The debugger must program ISDBCFG1[5:0] to all ones to enable this feature.

0x28882000 LPASS_QDSP6SS_WDOG_RESET

Type: Write (Command)
Clock: AHB_CLK
Reset State: NA

The QDSP6SS_WDOG_RESET register resets the watchdog counter. In normal operation, QDSP6 should periodically write this command register to reset watchdog. This command register also resets (clears) watchdog freeze, re-enabling the watchdog counter.

LPASS_QDSP6SS_WDOG_RESET

Bits	Name	Description
0	QDSP6SS_WDOG_RESET	This bit generates the wdog_reset_stb during the non-sleep mode. A pulse is generated on wdog_reset_stb when this bit is written with a 0x1.

0x28882004 LPASS_QDSP6SS_WDOG_FREEZE

Type: Write (Command)
Clock: AHB_CLK
Reset State: NA

The QDSP6SS_WDOG_FREEZE register freezes the watchdog timer at count 0. QDSP6 should write this register before it goes to power-down mode to avoid a watchdog timeout during power-down. It may be wakened (unfreeze) by interrupts enabled in the interrupt monitor when QDSP6SS_WDOG_UNMASKED_INT_EN is set to 1. This register is also reset by writing to the QDSP6SS_WDOG_RESET register.

It is expected that QDSP6 power-up sequence as triggered by the same interrupt event that wakes up WDOG should be completed before WDOG expires in approximated 390 ms.

LPASS_QDSP6SS_WDOG_FREEZE

Bits	Name	Description
0	QDSP6SS_WDOG_FREEZE	Set 1 to this bit to freeze the watchdog timer at time 0.

0x28882008 LPASS_QDSP6SS_WDOG_UNMASKED_INT_EN

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_WDOG_UNMASKED_INT_EN register enables the unfreeze of WDOG on the interrupt as detected in the interrupt monitor or SIRC during QDSP6 power-down. The interrupt monitor and SIRC must be programmed ahead of the power-down process to enable all or a sub-set of interrupts to power up the QDSP6 and unfreeze the WDOG.

If this register bit is cleared, QDSP6 should program WDOG_RESET to unfreeze the WDOG after it is powered up.

This register must be programmed before WDOG freezes.

LPASS_QDSP6SS_WDOG_UNMASKED_INT_EN

Bits	Name	Description
0	WDOG_UNMASKED_INT_EN	Set 1 to this bit to enable interrupt wakeup.

0x2888200C LPASS_QDSP6SS_WDOG_STATUS

Type: Read
Clock: AHB_CLK
Reset State: NA

The QDSP6SS_WDOG_STATUS register provides watchdog status.

WDOG_RESET_STATUS bit is intended to inform QDSP6 processor cold boot routine whether the cold boot is caused by a watchdog expire event. To support this feature, the system software handling QDSP6 reset on WDOG expiration must apply only to the QDSP6SS private reset and QDSP6 core reset.

The WDOG_RESET_STATUS bit is cleared on full subsystem reset. QDSP6 firmware can write to WDOG_RESET to clear it.

WDOG_READY bit should be checked when:

- Programming watchdog for the first time after reset
- Before writing WDOG_FREEZE. Otherwise the freeze command might never be taken.

LPASS_QDSP6SS_WDOG_STATUS

Bits	Name	Description
17	WDOG_READY	The bit indicates whether it is safe to write to watchdog registers. Watchdog in reset from the assertion of QDSP6SS full reset or private reset Watchdog has not taken the previously issued WDOG_RESET command due to synchronization 0x1: Watchdog is ready. 0x0: Watchdog is not ready. Writing to watchdog register may cause handshaking error. Watchdog not-ready status can be caused by any of these events:
16:3	WDOG_COUNT	Counter value [13:0] of watch dog counter. **NOTE** The sleep counter value is sampled using the AHB_CLK. Multiple reads are required to determine the value (assuming AHB_CLK is much faster than sleep clock)
2	WDOG_CNT_RESET_STATUS	Show the value of watchdog internal counter reset signal wdog_res signal (for test).
1	WDOG_IS_FROZEN	This bit indicates whether the watchdog timer is frozen (disabled). 0x1: Watchdog Frozen (disabled) 0x0: Watchdog not Frozen (enabled)
0	WDOG_RESET_STATUS	Reading 1 indicates a watchdog expired event occurs after a full subsystem reset is asserted.After watchdog expires, it is 1 until software writes 1 to register QDSP6SS_WDOG_RESET

0x28882010 LPASS_QDSP6SS_WDOG_EXPIRED_WIDTH

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0C7C

The WDOG_EXPIRED_WIDTH register defines the width of the wdog_expired pulse in the number of sleep_clk. The default value is 0x0C7C = 3196.

WDOG_EXPIRED_WIDTH should not be programmed with a value greater than 0x31F3 = 12787.

LPASS_QDSP6SS_WDOG_EXPIRED_WIDTH

Bits	Name	Description
14	SYNC_STATUS	When set (1), the wdog expired width data is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STATUS bit is clear (0).
13:0	DATA	Wdog counter terminal value to de-assert the wdog_expired pulse. The wdog counter is14-bits.

0x28882014 LPASS_QDSP6SS_WDOG_BARK_TIME

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x3FFF

The WDOG_BARK_TIME register defines the time in sleep_clk when to assert the watchdog (bark) interrupts. The value can be between 0 and 12787 (the time when the watchdog times out). The default value is 0x3FFF, which is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog (bark) interrupt.

LPASS_QDSP6SS_WDOG_BARK_TIME

Bits	Name	Description
14	SYNC_STATUS	When set (1), the wdog bark time is synchronizing to the SLEEP_CLK. The data value is not guaranteed until the SYNC_STATUS bit is clear (0).
13:0	DATA	The wdog counter value on which to trigger the bark interrupt

0x28882020 LPASS_QDSP6SS_WDOG_TEST

Type: Read/Write
Clock: AHB_CLK
Reset State: NA

The WDOG_TEST register is used to load a test value into the watchdog timer counter. After the value is loaded, the watchdog counts from this value.

LPASS_QDSP6SS_WDOG_TEST

Bits	Name	Description
14	SYNC_STATUS	When set (1), the watchdog test is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STATUS bit is clear (0).
13:0	WDOG_TEST_CNT	The watchdog counter test load value [13:0]. The watchdog counter is 14-bits.

0x28882024 LPASS_QDSP6SS_WDOG_ENABLE

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

If the QDSP6SS_WDOG_ENABLE register is 0, the watchdog timer is held in reset.

LPASS_QDSP6SS_WDOG_ENABLE

Bits	Name	Description
0	WDOG_ENABLE	Set 1 to this bit to enable watchdog.

12.10.4 User general purpose timer registers

0x28884000 LPASS_QDSP6SS_UGPT_MATCH_VAL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x00000000

The QDSP6SS_UGPT_MATCH_VAL register contains the UGPT match value. The user general purpose timer generates an interrupt to QDSP6 when its counter value reaches this match value.

LPASS_QDSP6SS_UGPT_MATCH_VAL

Bits	Name	Description
31:0	MATCH	During the reset, the count gets initialized to zero. If the timer is enabled, it starts counting up. An interrupt is generated if the count reaches this programmed match value.

0x28884004 LPASS_QDSP6SS_UGPT_COUNT_VAL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_UGPT_COUNT_VAL register contains the current value of the UGPT TIMER. The current value can be set by software.

The count value is writable as a test/debug only feature. The procedure for writing the QDSP6SS_UGPT_COUNT_VAL is as follows:

1. Disable the timer by clearing the EN bit in QDSP6SS_UGPT_ENABLE.
2. Write QDSP6SS_UGPT_COUNT_VAL (Do not write to the QDSP6SS_UGPT_COUNT_VAL for a second time. It might result in different bits capturing the first or second write value.)
3. Enable the timer by setting the EN bit in QDSP6SS_UGPT_ENABLE.
4. The count value can be read back to see that the timer starts to count from the programmed value (it may take up to 32 tcxo clock cycles to get the value reflected).

LPASS_QDSP6SS_UGPT_COUNT_VAL

Bits	Name	Description
31:0	COUNT	When read, it returns the current value of the COUNTER. If written, the timer starts to count from the written value. Follow the procedure mentioned above for writing the timer.

0x28884008 LPASS_QDSP6SS_UGPT_ENABLE

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x00000000

The UGPT_ENABLE register is used to enable the UGPT timer.

LPASS_QDSP6SS_UGPT_ENABLE

Bits	Name	Description
31:2	RESERVED_BITS31_2	Reserved
1	CLR_ON_MATCH_EN	When set (1), the TIMER clears when it reaches the match value.
0	EN	When set (1), the TIMER is enabled and counts with frequency TCXO_CLK.

0x2888400C LPASS_QDSP6SS_UGPT_CLEAR

Type: Write (Command)
Clock: AHB_CLK
Reset State: NA

The UGPT_CLEAR register is a one-shot command register that, when written with any value, resets the UGPT TIMER to a value of 0. This occurs regardless of the state of the UGPT_ENABLE register.

LPASS_QDSP6SS_UGPT_CLEAR

Bits	Name	Description
31:0	RESERVED_BITS_31_0	Reserved

12.10.5 QDSP6SS interrupt registers

0x28885000+ 4*n LPASS_QDSP6SS_INTn, n=[0..31]

Type: Write (Command)
Clock: AHB_CLK
Reset State: 0x0

Writing any value to the QDSP6SS_INTn register generates an interrupt pulse from the QDSP6SS to other processors.

LPASS_QDSP6SS_INTn

Bits	Name	Description
31:0	RESERVED_BITS31_0	Reserved

12.10.6 Reset/Clock/Power control registers

0x28887004 LPASS_QDSP6SS_CORE_IDLE_GATEOFF

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0000_000F

This register is introduced to enable other processors (another QDSP6, Scorpion, ARM9, MPM) to control QDSP6 power collapse or Vdd-minimization. In a SoC with RPM, this feature might not be used since QDSP6SS SPM may communicate with RPM on the processor power state.

If the QDSP6 wants itself to enter into Vdd-Min or a power collapsed state, it needs to communicate itself to another master in the system via a core idle interrupt. It should write to QDSP6SS_PD_HS_START first before going into idle. The idle interrupt needs to be sent only to the master that is performing the task. To gate off the interrupts to other masters, this register is used. Software should program the register to enable only one of the masters. How the 4-bit idle interrupts are mapped is chip-specific. One recommended way is as follows:

1. IDLE_0 is sent to the MPM
2. IDLE_1 is sent to the ARM9
3. IDLE_2 is sent to the other QDSP6
4. IDLE_3 is sent to the Scorpion

LPASS_QDSP6SS_CORE_IDLE_GATEOFF

Bits	Name	Description
31:4	RESERVED_BITS31_4	reserved space.

LPASS_QDSP6SS_CORE_IDLE_GATEOFF (cont.)

Bits	Name	Description
3:0	GATEOFF	0xF: IDLE_NONE 0xE: IDLE_0 0xD: IDLE_1 0xB: IDLE_2 0x7: IDLE_3

0x2888700C LPASS_QDSP6SS_PD_HS_START

Type: Write/Command
Clock: AHB_CLK
Reset State: NA

This is the command register for starting the power down preparation process.

It should be written (the written value is ignored) when the core decides to power down after QDSP6 core interrupt is disabled globally by QDSP6 CR register SYSCFG bit. Firmware must poll QDSP6_PD_HS_DONE to indicate hardware has completed the preparation before proceed further.

Writing this register triggers a hardware state machine in the sleep controller to isolate interrupt inputs to QDSP6 core, and de-isolate interrupt inputs to the interrupt monitor. It also clears all status registers in the interrupt monitor. As a result, the interrupt monitor is now responding to external interrupt event and QDSP6 core is isolated from external interrupt during the power down process.

Writing this register also clears idle interrupts to other processors, which is asserted from previous core idle event.

LPASS_QDSP6SS_PD_HS_START

Bits	Name	Description
31:0	RESERVED_BITS31_0	reserved space

0x28887010 LPASS_QDSP6SS_PD_HS_DONE

Type: Read
Clock: AHB_CLK
Reset State: 0x0

This is the handshake response register for the power down preparation process. The value 1 indicates hardware has completed the preparation

After polling the register, QDSP6 firmware should check the level one interrupt controller pending status CR register IPEND, copy pending interrupts to interrupt monitor, and then re-enable interrupt globally by QDSP6 CR register SYSCFG bit before putting the last thread to wait.

LPASS_QDSP6SS_PD_HS_DONE

Bits	Name	Description
31:1	RESERVED_BITS31_1	reserved space.
0	DONE	Status bit showing 1 if power down steps are complete.

0x28887014 LPASS_QDSP6SS_PU_HS_START

Type: Write/Command
Clock: AHB_CLK
Reset State: NA

This is used to request the hardware to complete power up process after the QDSP6 core has booted up from the power down state.

Writing this register triggers a hardware state machine in the sleep controller to de-isolate interrupt inputs to QDSP6 core, replay edge trigger interrupts recorded by the interrupt monitor since last time the interrupts to QDSP6 core is isolated, and then isolate the interrupt inputs to the interrupt monitor.

LPASS_QDSP6SS_PU_HS_START

Bits	Name	Description
31:0	RESERVED_BITS31_0	reserved space.

0x28887018 LPASS_QDSP6SS_PU_HS_DONE

Type: Read
Clock: AHB_CLK
Reset State: 0x1

This register is asserted after hardware has completed the power up sequence as triggered by QDSP6SS_PU_HS_START. It is optional for the SW to check this register after writing to PU_HS_START.

LPASS_QDSP6SS_PU_HS_DONE

Bits	Name	Description
31:1	RESERVED_BITS31_1	reserved space.
0	DONE	Status bit showing 1 if power up steps are complete.

0x2888701C LPASS_QDSP6SS_SLPC_CFG

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

Sleep controller configuration register. It should be configured before power down sequence starts.

LPASS_QDSP6SS_SLPC_CFG

Bits	Name	Description
31:5	RESERVED_BITS31_5	reserved space.
4	EXT_AVS_SRC_EN	0x0: use QDSP6 AVS. macro up/down request to trigger AVS 0x1: use both QDSP6 AVS. macro and external AVS. macro up/down request to trigger AVS
3	SAW_DBG	Set to 1 to allow SPM to go through states without actually turning off clock, hsfs, and clamp. This bit is expected to be set by ISDB via stuffed instruction to enable ISDB during the power down sequence
2:1	PD_SRC_SEL	Failure to provide the proper power down trigger after hardware has completed the power down preparation leaves the QDSP6 core in an unusable state because the core interrupt controller is isolated and no interrupt reaches the core. 0x0: use qdsp6_core_idle to trigger power down. 0x1: use public CSR register QDSP6SS_EXT_PD to trigger power down. 0x2: use external signal input to trigger power down 0x3: Un-used
0	EXT_WAKEUP_ENA	Set to 1 to enable wakeup by external processor writing to public CSR register QDSP6SS_EXT_WAKEUP. Set to 0 to disable. It needs to be set to 1 before power down if external processor is expected to initiate the wakeup.

0x28887020 LPASS_QDSP6SS_SLPC_STATUS

Type: Read
Clock: AHB_CLK
Reset State: 0x0

Sleep controller status register. This register is intended for debugging purposes.

LPASS_QDSP6SS_SLPC_STATUS

Bits	Name	Description
31:2	RESERVED_BITS31_2	reserved space.
1:0	FSM_STATE	This is the SLPC FSM current state

12.10.7 Test/Debug registers

0x28888008 LPASS_QDSP6SS_INSTANCE_ID

Type: Read
Clock: AHB_CLK
Reset State: N/A

In a chip, it is possible to have multiple instances of QDSP6SS to be present. This register returns the instance ID of the QDSP6SS.

LPASS_QDSP6SS_INSTANCE_ID

Bits	Name	Description
31:3	RESERVED_BITS31_3	reserved space.
2:0	ID	returns the instance ID value of the QDSP6SS

12.10.8 Free Running TCXO counter

0x2888C000 LPASS_QDSP6SS_TCXO_COUNT_VAL

Type: Read
Clock: AHB_CLK
Reset State: 0x0000_0000

The TCXO counter is reset when the QDSP6SS subsystem is reset and starts counting up on every pulse of the TCXO clock (the nominal operating frequency of TXCO clock is 19.2 MHz). The counter can be read through the CSR.

LPASS_QDSP6SS_TCXO_COUNT_VAL

Bits	Name	Description
31:0	COUNT	Returns the count value of the free running TCXO counter. This counter is reset when the QDSP6SS is reset. Due to the frequency relations between the TCXO clock and the AHB clock, the count can differ by an ahb_clk period or a TCXO clock period, whichever is higher.

0x2888C004 LPASS_QDSP6SS_TCXO_COUNTER_ENABLE

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_TCXO_COUNTER_ENABLE register is used to enable the TCXO counter. The counter is enabled after the reset. The counter keeps running until it is disabled by programming above register to 0x0.

LPASS_QDSP6SS_TCXO_COUNTER_ENABLE

Bits	Name	Description
31:1	RESERVED_BITS31_1	Reserved
0	EN	When set (1), the TIMER is enabled and incremented on TCXO clk

12.11 LPA SS QDSP6 SS L2VIC Slave Registers (0x28890000 LPASS_QDSP6SS_L2VIC_BASE)

This section contains the Low Power Audio Subsystem (LPASS) QDSP6SS L2VIC registers.

QDSP6SS L2VIC register starts at the base from QDSP6SS_CSR_BASE + 0x1_0000.

0x28890100+ 4*n LPASS_QDSP6SS_L2VIC_INT_ENABLEn, n=[0..31]

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_L2VIC_INT_ENABLE register enables interrupts sources to generate both an IRQ and a wakeup (both are generated for any detected interrupt).

LPASS_QDSP6SS_L2VIC_INT_ENABLEn

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x28890180+ 4*n LPASS_QDSP6SS_L2VIC_INT_ENABLE_CLEARn, n=[0..31]

Type: Write (Command)
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_L2VIC_INT_ENABLE_CLEARn register is used to clear to 0x0 the bits of the QDSP6SS_L2VIC_INT_ENABLEn register. Any bit that is written 0x1 causes the corresponding enable bit to be cleared..

LPASS_QDSP6SS_L2VIC_INT_ENABLE_CLEARn

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x28890200+ 4*n LPASS_QDSP6SS_L2VIC_INT_ENABLE_SETn, n=[0..31]

Type: Write (Command)
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_L2VIC_INT_ENABLE_SETn register is used to set to 0x1 the bits of the QDSP6SS_L2VIC_INT_ENABLEn register. Any bit that is written 0x1 causes the corresponding enable bit to be set. Because interrupts are automatically cleared and disabled when it is taken by QDSP6 core, the interrupt service should re-enable this interrupt after the interrupt source is cleared.

LPASS_QDSP6SS_L2VIC_INT_ENABLE_SETn

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Set

0x28890280+4*n LPASS_QDSP6SS_L2VIC_INT_TYPEn, n=[0..31]

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_L2VIC_INT_TYPEn register determines the edge/level type of interrupt..

LPASS_QDSP6SS_L2VIC_INT_TYPEn

Bits	Name	Description
31:0	SRC_TYPE	0x0: Level 0x1: Edge

0x28890300+4*n LPASS_QDSP6SS_L2VIC_INT_POLARITYn, n=[0..31]

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_L2VIC_INT_POLARITYn register determines the polarity of interrupt..

LPASS_QDSP6SS_L2VIC_INT_POLARITYn

Bits	Name	Description
31:0	POL	0x0: Active high 0x1: Active low

0x28890380+4*n LPASS_QDSP6SS_L2VIC_INT_STATUSn, n=[0..31]

Type: Read
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_L2VIC_INT_STATUSn register indicates which enabled interrupt is active..

LPASS_QDSP6SS_L2VIC_INT_STATUSn

Bits	Name	Description
31:0	STATUS	0x0: Inactive 0x1: Active

0x28890400+4*n LPASS_QDSP6SS_L2VIC_INT_CLEARn, n=[0..31]

Type: Write (Command)
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_L2VIC_INT_CLEARn register is used to clear the status of an active edge interrupt. Because an interrupt is automatically cleared and disabled after the interrupt is taken by QDSP6 core, this register is not used in normal interrupt service.

LPASS_QDSP6SS_L2VIC_INT_CLEARn

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x28890480+4*n LPASS_QDSP6SS_L2VIC_SOFT_INTn, n=[0..31]

Type: Write (Command)
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_L2VIC_SOFT_INTn register is used to set the status of an edge interrupt..

LPASS_QDSP6SS_L2VIC_SOFT_INTn

Bits	Name	Description
31:0	SW_INT	0x0: Do nothing 0x1: Set

0x28890500+4*n LPASS_QDSP6SS_L2VIC_INT_PENDINGn, n=[0..31]

Type: Read
Clock: AHB_CLK
Reset State: 0x0

The QDSP6SS_L2VIC_INT_PENDINGn register is used to indicate the status of an interrupt regardless of the enable. It is mainly for debug purpose.

LPASS_QDSP6SS_L2VIC_INT_PENDINGn

Bits	Name	Description
31:0	STATUS	0x0: Inactive 0x1: Active

12.12 LPA SS SAW Slave Registers (0x288B0000 LPASS_QDSP6SS_SAW_BASE)

This section contains the Low Power Audio Subsystem (LPASS) QDSP6SS SAW registers.

0x288B0000 LPASS_SAW_SECURE

Type: Read/write
Clock: SYS_REF_CLK
Reset State: 0x0000_0007

Security Treatment: Restricted

The SAW_SECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by ahb_saw_hprotns pin. When ahb_saw_hprotns is set to 0x0 the state of the SAW_SECURE register is not considered - a secure transaction is always allowed. When ahb_saw_hprotns is set to 0x1, the SAW_SECURE register security treatment bit of that register must be 0x1 for access to be granted. If the security treatment bit of the register is set to 0x0, the non-secure (ahb_saw_hprotns = 0x1) transactions are denied. When access is denied, a write is ignored and a read returns 0x0. No error is signaled.

When reading the SAW_SECURE register, non-secure agents always read 0x0. Secure agents see the actual value of the register. The reset value is controlled by CFGNSINIT input pin.

NOTE In QDSP6SS, the signal ahb_saw_hprotns is driven by input port q6ss_hs_hprotns. The CFGNSINIT is pulled to 1. It is recommended to leave the register unchanged from its default setting to disable the security feature, not needed for the QDSP6SS.

LPASS_SAW_SECURE

Bits	Name	Description
31:3	RESERVED	Reserved
2	SAW_CTL	Controls security treatment for SAW registers: SAW_TMR_CFG, SAW_STS 0x1: NSEC 0x0: SEC
1	PWR_CTL	Controls security treatment for SPM registers: SAW_SPM_CTL, SAW_SPM_SLP_TMR_DLY, SAW_SPM_WAKE_TMR_DLY, SAW_SPM_PMIC_CTL, SAW_SLP_CLK_EN, SAW_SLP_HSFS_PRECLMP_EN, SAW_SLP_HSFS_POSTCLMP_EN, SAW_SLP_CLMP_EN, SAW_SLP_RST_EN, SAW_SPM_MPM_CFG 0x1: NSEC 0x0: SEC
0	VLT_CTL	Controls security treatment for the AVS. registers: SAW_AVS_CTL, SAW_VCTL 0x1: NSEC 0x0: SEC

0x288B0004 LPASS_SAW_AVS_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW_SECURE [VLT_CTL].

The SAW_AVS_CTL register is used to control the Adaptive Voltage Scaling (AVS) system.

LPASS_SAW_AVS_CTL

Bits	Name	Description
31	RESERVED_1	Reserved
30	VLVL_WIDTH	Defines the VLVL field of PMIC data. SAW at minimum supports 8901 and 8058 regulator. See PMIC document for details. 0x0: 5 bits VLVL (8058 regulator) 0x1: 6 bits VLVL (8901 regulator)
29:28	VLVL_STEP	Controls the step size of each request to PMIC Arbiter. SW may use values from 0 to 3. Note that the value 0 results in no change - that is if the CPU requests UP or DOWN, the CURR_PVLVL is sent to the PMIC Arbiter. This may be useful for debug. If an increment or decrement operation would cause the current VLVL to transition above or below the MAX_VLVL or MIN_VLVL, the current VLVL is not changed. An interrupt is signaled if IRQ_MAX/MIN_EN is 1
27	EN	AVS. Enable. **NOTE** Setting to 0 does not disable any pending interrupts. **NOTE** AVS. FSM and SPM FSM are mutually exclusive. Only one FSM is active at a time. SW does not have to disable AVS. before going to sleep. 0x0: Disable AVS 0x1: Enable AVS
26	SW_DONE_INT_EN	Set to 1 to turn on AVS. interrupt for when a SW initiated voltage change has completed. Set to 0 to mask it (turn it off). ASSERTION: This interrupt is asserted only after a SW write to SAW_AVS_VLVL. Specifically, after the AVS. FSM traverses through all its states and transitions back to IDLE, the interrupt line is pulsed. The interrupt controller should be set to edge capture to receive this interrupt. CLEARING: None. This interrupt is a pulse, SW does not need to clear it (aside from requirements of the interrupt controller).

LPASS_SAW_AVS_CTL (cont.)

Bits	Name	Description
25	MAX_INT_EN	Set to 1 to turn on AVS. interrupt for MAX_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be greater than MAX_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit.
24	MIN_INT_EN	Set to 1 to turn on AVS. interrupt for MIN_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be smaller than MIN_VLVL. CLEARING: SW may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit
23	RESERVED_2	Reserved
22:17	MAX_VLVL	Control maximum value of AVS. controller's VLVL. When current VLVL reaches this value it may not grow any larger. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level higher, an interrupt is issued. This value may be updated at anytime. Setting to a value lower than MIN_VLVL is not supported, and unpredictable results may occur.
16	RESERVED	Reserved
15:10	MIN_VLVL	Control the minimum value of AVS. controller's VLVL. When the current VLVL reaches this level it may not shrink any smaller. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level lower, an interrupt is issued. This value may be updated at anytime. Setting to a value higher than MAX_VLVL is not supported, and unpredictable results may occur.
9:0	AVS_DELAY	Control the time between AVS. controller's requests to change the VLVL

0x288B0008 LPASS_SAW_VCTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: NA

Security Treatment: Controlled by SAW_SECURE [SAW_CTL].

Though this register is read/writable, it also causes a command pulse to the PMIC FSM. Writing this register results in a transaction to the PMIC with SAW_VCTL being sent to the PMIC. SAW support both 8901 and 8058 regulator.

LPASS_SAW_VCTL

Bits	Name	Description
31:8	RESERVED	Reserved
7:0	PMIC_DATA	PMIC DATA sent to the PMIC Arbiter

0x288B000C LPASS_SAW_STS

Type: Read
Clock: SYS_REF_CLK
Reset State: NA

Security Treatment: Controlled by SAW_SECURE [SAW_CTL].

This read only register provides SW with SAW status.

LPASS_SAW_STS

Bits	Name	Description
31:27	SPM_STATE	State of the SPM FSM.
26	SW_WR_PEND	This bit reflects the VLVL state of the request from the SAW_VCTL write is pending.
25	CPU_UP	This bit reflects the VLVL state of the request from the CPU (avs_saw_up) to raise the VLVL.
24	CPU_DN	This bit reflects the VLVL state of the request from the CPU (avs_saw_down) to lower the VLVL.
23	MAX_INT	IRQ status bit, AVS. controller detected that raising the VLVL by AVS_CTL[VLVL_STEP] would result in a value greater than AVS_CTL[MAX_VLVL]. If AVS_CTL[IRQ_MAX_EN] is set, an interrupt is issued. NOTE that SW can set MAX_VLVL lower than current VLVL creating a condition where VLVL is higher than MAX_VLVL. The AVS. controller can not correct VLVL. However, this condition sets IRQ_MAX.
22	MIN_INT	IRQ status bit, AVS. controller detected that lowering the VLVL by SAW_AVS_CTL[VLVL_STEP] would result in a value less than SAW_AVS_CTL[MIN_VLVL]. If SAW_AVS_CTL[IRQ_MIN_EN] is set, an interrupt is issued. NOTE that SW can set MIN_VLVL higher than current VLVL creating a condition where VLVL is lower than MIN_VLVL. The AVS. controller can not correct VLVL. However, this condition sets IRQ_MIN.

LPASS_SAW_STS (cont.)

Bits	Name	Description
21:20	PMIC_STATE	State of the PMIC FSM: transitions back to IDLE) 0x0: IDLE (waiting for PMIC transaction from AVS. or SPM) 0x1: ACK (waiting for ACK from PMIC Arb) 0x2: DONE (waiting for DONE form PMIC Arb before)
19:18	AVS_STATE	State of the AVS. FSM: indication) transitions back to IDLE) 0x0: IDLE (waiting to be enabled or for next UP/DOWN) 0x1: REQ (waiting for DONE from PMIC Arb) 0x3: DELAY (waiting for delay count termination before)
17:10	CURR_PMIC_DATA	Last PMIC DATA sent to the PMIC Arbiter (and the PMIC).
9:0	CURR_DLY	VLVL value of the counter used to calculate the time until the next AVS. controller request for a new VLVL.

0x288B0010 LPASS_SAW_CFG

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW_SECURE [SAW_CTL].

The SAW_CFG register is used to configure the common control between AVS. and SPM.system.

LPASS_SAW_CFG

Bits	Name	Description
31:13	RESERVED_BITS31_13	Reserved
12	FRC_REF_CLK_ON	Chicken bit to force saw_sys_ref_clk_on_req ON.
11:8	ADR_IDX	PMIC Arbiter Address Index. Drive the saw_pmic_addr_idx output port.
7:6	RESERVED_BITS7_6	Reserved
5	PMIC_MODE	PMIC Handshake 0x0: 8K_PMIC (only DONE signal) 0x1: 7K_PMIC (both ACK and DONE signals)

LPASS_SAW_CFG (cont.)

Bits	Name	Description
4:0	CLK_DIV	Divider ratio for clock. This is used to generate timer tick for the timer. Timer tick is asserted every (CLK_DIV + 1) sys_ref_clk period. ..... For sys_ref_clk = 20 MHz (53ns) The timer tick range 53 ns to 1.6us. 0x0: Timer Tick every sys_ref_clk 0x1F: Timer Tick every 128 sys_ref_clk.

0x288B0014 LPASS_SAW_SPM_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW_SECURE [PWR_CTL].

The SAW_SPM_CTL register is used to control the subsystem power management system. This are parameters that controls the operation of SPM FSM.

LPASS_SAW_SPM_CTL

Bits	Name	Description
31:8	RESERVED_BITS31_8	Reserved
7	NO_CLKEN2GATE	Disable SPM FSM ENBL_CLK to GATE_CLK state transition. This is set to 1 for ARM11 subsystem. 0x0: Allow SPM FSM ENBL_CLK to GATE_CLK state transition (SCSS and Q6SS) 0x1: Disable SPM FSM ENBL_CLK to GATE_CLK state transition (MSS)
6	PWR_RESTORE	Steps to restore VDD during bring up. 0x0: ONE_STEP (SAW_SPM_PMIC, one PMIC operation) 0x1: TWO_STEPS (SAW_SPM_PMIC then SAW_SPM_PMIC, two PMIC operation)
5	PWR_COLLAPSE	Steps to lower VDD during shutdown. 0x0: ONE_STEP (SAW_SPM_PMIC, one PMIC operation) 0x1: TWO_STEPS (SAW_SPM_PMIC then SAW_SPM_PMIC, two PMIC operation)
4	MEM_RET	Turn ON CLOCK and RESET immediately after power restore and before head/foot switch are CLOSE/ON. (Used by Q6 L2 array)
3	RPM_BYP	Bypass RPM Handshake 0x0: PERFORM RPM handshake 0x1: BYPASS RPM handshake (Also set for Halcyon for MPM handshake)

LPASS_SAW_SPM_CTL (cont.)

Bits	Name	Description
2:0	MODE	SPM Power Mode. The various low power sleep state are, 0x0: CLK GATE (clk gate only) 0x1: GDFS (clk gate, head/foot switch) 0x2: PWR DN (clk gate, head/foot switch, vdd min/collapse.) 0x3: RPM S/W DRIVEN (clk gate, RPM controls hsfs, vdd) 0x4: RESERVED_1 0x5: RESERVED_2 0x6: PWR DN 2 (Same as PWR DN for QDSP6 retention mode) 0x7: RESERVED_3

0x288B0018 LPASS_SAW_SPM_SLP_TMR_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW_SECURE [PWR_CTL].

LPASS_SAW_SPM_SLP_TMR_DLY

Bits	Name	Description
31:24	PMIC_SLP	PMIC Sleep Delay. Controls the time between PMIC SLP operation and RPM shutdown request. The delay count is shifted left by 2. 8'h00: 0 timer tick 8'h01: 4 timer tick Time range: 53ns to 1.638ms
23:16	PMIC_MID	PMIC MID Delay. Controls the time between PMIC MID operation and preclamp head/foot switches are OPEN/OFF (low current state). The delay count is shifted left by 2. 8'h00: 0 8'h01: 4 Time range: 53ns to 1.638ms
15:12	HSFS_POST	Header Foot Switch Post Clamp Delay. Controls the time between postclamp head/foot switches are OPEN/OFF (low current state) and PMIC operation begins. Time range: 53ns to 25.6us
11:8	HSFS_PRE	Header Foot Switch Pre Clamp Delay. Controls the time between preclamp head/foot switches are OPEN/OFF (low current state) and clamp is asserted. Time range: 53ns to 25.6us
7:4	CLAMP	Clamp Delay. Controls the time between assertion of clamp and postclamp head/foot switches are OPEN/OFF (low current state). Time range: 53ns to 25.6us

LPASS_SAW_SPM_SLP_TMR_DLY (cont.)

Bits	Name	Description
3:0	CLK_GATE	Clock Gate Delay. Controls the time between clock gating and preclamp head/foot switches are OPEN/OFF (low current state). Time range: 53ns to 25.6us

0x288B001C LPASS_SAW_SPM_WAKE_TMR_DLY

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW_SECURE [PWR_CTL].

This register provide the timer delay values for SPM FSM power up states. The formula for calculate the time delay is:

(SAW_CFG[CLK_DIV]+1) * delay field * sys_ref_clk_period

The sys_ref_clk is commonly connect to TCXO.

LPASS_SAW_SPM_WAKE_TMR_DLY

Bits	Name	Description
31:24	PMIC_WAKE	PMIC Wake Delay. Controls the time between PMIC WAKE operation and next bring up sequence. The delay count is shifted left by 2. 8'h00: 0 timer tick 8'h01: 4 timer tick Time range: 53ns to 1.638ms
23:16	PMIC_MID	PMIC MID Delay. Controls the time between PMIC MID operation and head/foot switches are CLOSE/ON. The delay count is shifted left by 2. 8'h00: 0 timer tick 8'h01: 4 timer tick Time range: 53ns to 1.638ms
15:12	CLAMP_HSFS	Clamp Head/Foot switch Delay. Control the time between clamp_hsfs is de-asserted and clocks are enabled. Time range: 53ns to 25.6us
11:8	HSFS	Header Foot Switch Delay. Controls the time between head/foot switches are CLOSE/ON (functional state) and clocks are enabled. Time range: 53ns to 25.6us
7:4	CLAMP	Clamp Delay. Controls the time between clamp is de-asserted and reset is de-asserted. Time range: 53ns to 25.6us

LPASS_SAW_SPM_WAKE_TMR_DLY (cont.)

Bits	Name	Description
3:0	CLK_EN	Clock Enable Delay. Controls the time between clock is enabled and clamp is de-asserted. Time range: 53ns to 25.6us

0x288B0020 LPASS_SAW_SPM_PMIC_CTL

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: NA

Security Treatment: Controlled by SAW_SECURE [PWR_CTL].

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

LPASS_SAW_SPM_PMIC_CTL

Bits	Name	Description
31:24	RESERVED_BITS31_24	Reserved
23:16	MID	VDD MID Value. This value is only used if SAW_SPM_CTL[PWR_RESTORE] or SAW_SPM_CTL[PWR_COLLAPSE] is set to 0x1. The VLVL should be in average of WAKE VLVL and SLP VLVL.
15:8	WAKE	Wake Up Value. The VLVL during wake (normal operation).
7:0	SLP	Sleep VDD Value. The VLVL during sleep

0x288B0024 LPASS_SAW_SLP_CLK_EN

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW_SECURE [PWR_CTL].

The SAW_SLP_CLK_EN register is used to enable the clocks during sleep. The register width is defined by NUM_CLKEN parameter. The parameter values for subsystems are SCSS = 5, Q6SS = 1, MSS = 4.

LPASS_SAW_SLP_CLK_EN

Bits	Name	Description
31:1	RESERVED_BITS31_1	Reserved

LPASS_SAW_SLP_CLK_EN (cont.)

Bits	Name	Description
0	SLP_CLK_EN	Core clock gating enable during sleep. 0x0: clock ON during sleep 0x1: clock halted during sleep.

0x288B0028 LPASS_SAW_SLP_HSFS_PRECLMP_EN

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: NA

Security Treatment: Controlled by SAW_SECURE [PWR_CTL].

The SAW_SLP_HSFS_PRECLMP_EN register is used to enable the head/foot switch which needs to be assert before clamp during sleep. The register width is defined by NUM_HSFSPREC parameter.The parameter values for subsystems are SCSS = 3, Q6SS = 1, MSS = 1.

LPASS_SAW_SLP_HSFS_PRECLMP_EN

Bits	Name	Description
31:1	RESERVED_BITS31_1	Reserved
0	HSFS_PRE_EN	Header Footer Switch Pre Clamp Enable (unused). 0x0: ON/CLOSE during sleep 0x1: OFF/OPEN during sleep (low current state)

0x288B002C LPASS_SAW_SLP_HSFS_POSTCLMP_EN

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: NA

Security Treatment: Controlled by SAW_SECURE [PWR_CTL].

.The SAW_SLP_HSFS_POSTCLMP_EN register is used to enable the head/foot switch which needs to be assert after clamp during sleep. The register width is defined by NUM_HSFSPOSTC parameter. The parameter values for subsystems are SCSS = 1, Q6SS = 6, MSS = 1.

LPASS_SAW_SLP_HSFS_POSTCLMP_EN

Bits	Name	Description
31:6	RESERVED_BITS31_6	Reserved

LPASS_SAW_SLP_HSFS_POSTCLMP_EN (cont.)

Bits	Name	Description
5:0	HSFS_POST_EN	Header Footer Switch Post Clamp Enable. Used for memory sleep control bit 5 to qdsp6_arr_stby_n bit 4 to qdsp6_etb_slp_nret_n bit 3 to qdsp6_l2tag_slp_nret_n bit 2 to qdsp6_l1tcm_slp_nret_n bit 1 to qdsp6_slp_ret_n bit 0 to qdsp6_l2data_slp_nret_n 0x0: ON/CLOSE during sleep 0x1: OFF/OPEN during sleep (low current state)

0x288B0030 LPASS_SAW_SLP_CLMP_EN

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: NA

Security Treatment: Controlled by SAW_SECURE [PWR_CTL].

The SAW_SLP_CLMP_EN register is used to enable the clamps which needs to be assert during sleep. The register width is defined by NUM_CLMPEN parameter. The parameter values for subsystems are SCSS = 1, Q6SS = 1, MSS = 1.

LPASS_SAW_SLP_CLMP_EN

Bits	Name	Description
31:1	RESERVED_BITS31_1	Reserved
0	CLMP_EN	QDSP6 Core clamp Enable. 0x0: OFF during sleep 0x1: ON during sleep.

0x288B0034 LPASS_SAW_SLP_RST_EN

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: NA

Security Treatment: Controlled by SAW_SECURE [PWR_CTL].

The SAW_SLP_RST_EN register is used to enable the reset during sleep. The register width is defined by NUM_RSTEN parameter. The parameter values for subsystems are SCSS = 1, Q6SS = 1, MSS = 1.

LPASS_SAW_SLP_RST_EN

Bits	Name	Description
31:1	RESERVED_BITS31_1	Reserved
0	SLP_RST_EN	QDSP6 Core Reset Enable during sleep. When enabled, SPM resets QDSP6 core, isdb and etm during power up. In the special case of bit SAW_DBG of QDSP6SS_SLPC_CFG register is asserted, the reset from SPM propagates to QDSP6 core reset only. 0x0: OFF after power restore 0x1: ON after power restore.

0x288B0038 LPASS_SAW_SPM_MPM_CFG

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: 0x0000_0000

Security Treatment: Controlled by SAW_SECURE [PWR_CTL].

The SAW_SPM_MPM_CFG register is used to interface with 7K MPM for TCXO shutdown or power down vetoes.

LPASS_SAW_SPM_MPM_CFG

Bits	Name	Description
31:4	RESERVED_BITS31_4	Reserved
3	TCXO_SD_VOTE	TCXO shutdown vote enable 0x0: No 0x1: Yes.
2	VDD_DIG_MIN_VOTE	VDD_DIG power retention vote enable 0x0: No 0x1: Yes.
1	VDD_DIG_PD_VOTE	VDD_DIG power down vote enable. 0x0: No 0x1: Yes
0	EN	SPM - MPM interface Enable. **NOTE** Setting to 0 votes Yes for the 3 votes, assert SWFI and de-assert wakeup_req to MPM. 0x0: Disable 0x1: Enable

0x288B003C LPASS_SAW_SLP_CLMP_HSFS_EN

Type: Read/Write
Clock: SYS_REF_CLK
Reset State: NA

Security Treatment: Controlled by SAW_SECURE [PWR_CTL].

The SAW_SLP_CLMP_HSFS_EN register is used to enable the clamps which clamps the head/foot switch of the memory during sleep. The register width is defined by NUM_CLMPHSFSEN parameter. The parameter values for subsystems are SCSS = 1, Q6SS = 1, MSS = 1.

LPASS_SAW_SLP_CLMP_HSFS_EN

Bits	Name	Description
31:1	RESERVED_BITS31_1	Reserved
0:0	CLMP_HSFS_EN	Clamp Head/Foot switch Enable (Unused). 0x0: OFF during sleep 0x1: ON during sleep.

13 LPDDR Registers

13.1 Overview

Table 13-1 LPDDR Bases

Base Name	Parent	Address
EBI1_CH0_TOP_MISC_CNTL	EBI1_CH0_BASE	0x00A00000
EBI1_CH1_TOP_MISC_CNTL	EBI1_CH1_BASE	0x00D00000
DIM_D00_DIM_DQ_TOP_CFG	DIM_D00_REG_BASE	0x1A700000
DIM_D01_DIM_DQ_TOP_CFG	DIM_D01_REG_BASE	0x1A800000
DIM_D02_DIM_DQ_TOP_CFG	DIM_D02_REG_BASE	0x1A900000
DIM_D03_DIM_DQ_TOP_CFG	DIM_D03_REG_BASE	0x1AA00000
DIM_C00_DIM_CA_TOP_CFG	DIM_C00_REG_BASE	0x1AB00000
DIM_D10_DIM_DQ_TOP_CFG	DIM_D10_REG_BASE	0x1AC00000
DIM_D11_DIM_DQ_TOP_CFG	DIM_D11_REG_BASE	0x1AD00000
DIM_D12_DIM_DQ_TOP_CFG	DIM_D12_REG_BASE	0x1AE00000
DIM_D13_DIM_DQ_TOP_CFG	DIM_D13_REG_BASE	0x1AF00000
DIM_C10_DIM_CA_TOP_CFG	DIM_C10_REG_BASE	0x1B000000

13.2 EBI1 CH0 Registers (0x00A00000 EBI1_CH0_BASE)

This section contains the EBI1 CH0 registers.

The HSDDRx generation 5 memory controller core is an AXI r0p0+ slave that provides a high-performance, low-latency, 32-bit wide interface to LPDDR, LPDDR2, PCDDR2 or PCDDR3 memory.

This section describes the Configuration Status Registers which are available to software for configuring the HSDDRx memory controller core. The configuration registers in the core are organized into the following sub groups based on register functionality.

The access to configuration registers is performed via the AHB bus.

Table 13-2 HSDDRx Register Categories Grouped by Functionality

Function	Prefix	Address Bit (19:16)
Wrapper Configuration Registers	TOP	000x
AXI Performance Monitors	PMON_AXI	0010
DDR Performance Monitors	PMON_DDR	0011
AXI Configuration Registers	SLV	010x
MPU Configuration Registers	HSDDR_MPU	011x
DDRx Configuration Registers	DDR	10xx
LBST Configuration Registers	LBST	11xx

13.2.1 EBI1 Ch0 HSDDRx Registers

13.2.1.1 Top-Level Wrapper Registers

0x00A00004 EBI1_CH0_TOP_MISC_CNTL

Type: Read/Write
Clock: CLK_XO
Reset State: 0x0004A0A8

Top level Miscellaneous Control register.

EBI1_CH0_TOP_MISC_CNTL

Bits	Name	Description
31:21	RESERVED_31_21	

EBI1_CH0_TOP_MISC_CNTL (cont.)

Bits	Name	Description
20	IOCAL_UPDATE_METHOD	SW : RW Specify a way to update command/address IO pads' PCNT/NCNT values. 0x0: Update when the bus is idle but CK could be running 0x1: Update when the memory is in self-refresh state and CK is not running
19:16	IOCAL_UPDATE_PULSE_WIDTH	SW : RW Number of DDR1X clock cycles for the pulse for IOCal updates. 0x0: reserved 0x1: 1 DDR 1x cycle 0x2: 2 DDR 1x cycles 0x3: 3 DDR 1x cycles 0x4: 4 DDR 1x cycles 0x5: 5 DDR 1x cycles 0x6: 6 DDR 1x cycles 0x7: 7 DDR 1x cycles 0x8: 8 DDR 1x cycles 0x9: 9 DDR 1x cycles 0xA: 10 DDR 1x cycles 0xB: 11 DDR 1x cycles 0xC: 12 DDR 1x cycles 0xD: 13 DDR 1x cycles 0xE: 14 DDR 1x cycles 0xF: 15 DDR 1x cycles
15	CLKON_DDR_PIPE_MANUAL	SW : RW Control pipeline DDR 1x on/off in clkon manual mode 0x0: Off 0x1: On
14	MODE_CLKON_DDR_PIPE	SW : RW Mode to control clkon for pipeline DDR 1X 0x0: controlled by CLKON_DDR_PIPE_MANUAL 0x1: controlled by internal logic
13	CLKON_DDR_2X_MANUAL	SW : RW Control clk_ddr_2x on/off in clkon manual mode 0x0: Off 0x1: On
12	MODE_CLKON_DDR_2X	SW : RW Mode to control clkon for clk_ddr_2x 0x0: controlled by CLKON_DDR_2X_MANUAL 0x1: controlled by internal logic
11	MODE_MEM_HALT	SW : RW Momory mode used when SW requests clock switching. 0x0: self-refresh mode 0x1: clock-stop/power-down mode

EBI1_CH0_TOP_MISC_CNTL (cont.)

Bits	Name	Description
10:8	TEST_CLK_SEL	SW : RW Test clock select: 0x0: no clock output_1 0x1: ddr_1x 0x2: clk_axi 0x3: clk_ahb 0x4: clk_xo 0x5: no clock output_2 0x6: dqs positive edge 0x7: dqs negative edge
7	CLKON_AHB_MANUAL	SW : RW Control clk_ddr on/off in clkon manual mode 0x0: Off 0x1: On
6	MODE_CLKON_AHB	SW : RW Mode to control clkon for clk_ahb 0x0: controlled by CLKON_AHB_MANUAL 0x1: controlled by internal logic
5	CLKON_DDR_1X_MANUAL	SW : RW Control clk_ddr on/off in clkon manual mode 0x0: Off 0x1: On
4	MODE_CLKON_DDR_1X	SW : RW Mode to control clkon for clk_ddr_1x 0x0: controlled by CLKON_DDR_1X_MANUAL 0x1: controlled by internal logic
3	CLKON_AXI_MANUAL	SW : RW Control clk_axi on/off in clkon manual mode 0x0: Off 0x1: On
2	MODE_CLKON_AXI	SW : RW Mode to control clkon for clk_axi 0x0: controlled by CLKON_AXI_MANUAL 0x1: controlled by internal logic
1:0	RESERVED_1_0	

13.2.1.2 Performance Monitor Registers

0x00A20000 EBI1_CH0_PMON_AXI_CNTL

Type: Read/Write
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Control register.

EBI1_CH0_PMON_AXI_CNTL

Bits	Name	Description
31:17	RESERVED_31_17	
16	INTERRUPT	SW : R 0x0: No interrupt 0x1: Interrupt occurred
15:3	RESERVED_15_3	
2	RESET_COUNTER	SW : W write to '1' resets all the counters
1	STOP_COUNTER	SW : W write to '1' causes all the counters stop counting
0	START_COUNTER	SW : W write to '1' causes all the counters start counting

0x00A20004 EBI1_CH0_PMON_AXI_INTERRUPT

Type: Read/Write
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Interrupt Event Counter register.

EBI1_CH0_PMON_AXI_INTERRUPT

Bits	Name	Description
31:0	INT_EVENT_CNT	SW : RW Number of counter 0 events that will trigger interrupt

0x00A20008 EBI1_CH0_PMON_AXI_SOURCE_0

Type: Read/Write
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Source Control register 0.

EBI1_CH0_PMON_AXI_SOURCE_0

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00A2000C EBI1_CH0_PMON_AXI_COUNT_0

Type: Read
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Count register 0.

EBI1_CH0_PMON_AXI_COUNT_0

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00A20010 EBI1_CH0_PMON_AXI_SOURCE_1

Type: Read/Write
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Source Control register 1.

EBI1_CH0_PMON_AXI_SOURCE_1

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00A20014 EBI1_CH0_PMON_AXI_COUNT_1

Type: Read
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Count register 1.

EBI1_CH0_PMON_AXI_COUNT_1

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00A20018 EBI1_CH0_PMON_AXI_SOURCE_2

Type: Read/Write
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Source Control register 2.

EBI1_CH0_PMON_AXI_SOURCE_2

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00A2001C EBI1_CH0_PMON_AXI_COUNT_2

Type: Read
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Count register 2.

EBI1_CH0_PMON_AXI_COUNT_2

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00A20020 EBI1_CH0_PMON_AXI_SOURCE_3

Type: Read/Write
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Source Control register 3.

EBI1_CH0_PMON_AXI_SOURCE_3

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00A20024 EBI1_CH0_PMON_AXI_COUNT_3

Type: Read
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Count register 3.

EBI1_CH0_PMON_AXI_COUNT_3

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00A30000 EBI1_CH0_PMON_DDR_CNTL

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Control register.

EBI1_CH0_PMON_DDR_CNTL

Bits	Name	Description
31:17	RESERVED_31_17	
16	INTERRUPT	SW : R 0x0: No interrupt 0x1: Interrupt occurred

EBI1_CH0_PMON_DDR_CNTL (cont.)

Bits	Name	Description
15:3	RESERVED_15_3	
2	RESET_COUNTER	SW : W write to '1' resets all the counters
1:0	RESERVED_1_0	

0x00A30004 EBI1_CH0_PMON_DDR_INTERRUPT

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Interrupt Event Counter register.

EBI1_CH0_PMON_DDR_INTERRUPT

Bits	Name	Description
31:0	INT_EVENT_CNT	SW : RW Number of counter 0 events that will trigger interrupt

0x00A30008 EBI1_CH0_PMON_DDR_SOURCE_0

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Source Control register 0.

EBI1_CH0_PMON_DDR_SOURCE_0

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00A3000C EBI1_CH0_PMON_DDR_COUNT_0

Type: Read
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Count register 0.

EBI1_CH0_PMON_DDR_COUNT_0

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00A30010 EBI1_CH0_PMON_DDR_SOURCE_1

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Source Control register 1.

EBI1_CH0_PMON_DDR_SOURCE_1

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00A30014 EBI1_CH0_PMON_DDR_COUNT_1

Type: Read
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Count register 1.

EBI1_CH0_PMON_DDR_COUNT_1

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00A30018 EBI1_CH0_PMON_DDR_SOURCE_2

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Source Control register 2.

EBI1_CH0_PMON_DDR_SOURCE_2

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00A3001C EBI1_CH0_PMON_DDR_COUNT_2

Type: Read
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Count register 2.

EBI1_CH0_PMON_DDR_COUNT_2

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00A30020 EBI1_CH0_PMON_DDR_SOURCE_3

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Source Control register 3.

EBI1_CH0_PMON_DDR_SOURCE_3

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00A30024 EBI1_CH0_PMON_DDR_COUNT_3

Type: Read
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Count register 3.

EBI1_CH0_PMON_DDR_COUNT_3

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

13.2.1.3 AXI Slave Registers

0x00A40000 EBI1_CH0_SLV_CONFIG

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x80400003

AXI Slave Configuration Register.

This register defines the core interface configuration and memory controller clocking modes.

EBI1_CH0_SLV_CONFIG

Bits	Name	Description
31	CLKON_DISABLE	The slave logic's AXI CLKON signal will be de-asserted when the slave is idle and no data remains in the write data or command buffer. Additionally, AXI_AREADY and AXI_WREADY will be de-asserted when AXI CLKON is de-asserted. The AXI CLKON signal from the slave logic will be constantly driven to 1 and AXI_AREADY and AXI_WREADY will never be de-asserted due to de-asserting the AXI CLKON. 0x0: Disable 0x1: Enable
30:26	RESERVED_30_26	Reserved
25:16	CLKON_IDLE_TIMER	The number of AXI clock cycles that AXI CLKON will remain high after the slave is idle and the write data and command buffers are empty. 0x0: Reserved
15:14	RESERVED_15_14	Reserved
13:12	INTERLEAVE	Defines the way that bus system slave reconstructs the system address for MPU, error capture. 0x0: Disabled 0x1: Done at 1K Granularity 0x2: Done at 2K Granularity 0x3: Done at 4K Granularity
11:10	RESERVED_11_10	Reserved

EBI1_CH0_SLV_CONFIG (cont.)

Bits	Name	Description
9:8	CMD_ORDERING	Defines command reordering strategy (Based on the OOORD signal. OOOWT is not used since all buffered responses are returned immediately. Potentially lower power, higher average latency.) (All transactions from a particular master will be executed in time order. Reordering can occur between masters. Potentially more power, lower average latency.) (All transactions will be executed in time order, independent of the master association.) 0x0: reordering (default) 0x1: in-order per master 0x2: in-order globally 0x3: Reserved
7:3	RESERVED_7_3	RFU
2:0	CMD_Q_DEPTH	Defines number of outstanding requests that may be queued up for processing 0x0: 1 0x1: 2 0x2: 3 0x3: 4 0x4: 5 0x5: 6 0x6: 7 0x7: 8

0x00A40004 EBI1_CH0_SLV_RD_CONFIG

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x000B000F

Read Buffer Configuration Register

EBI1_CH0_SLV_RD_CONFIG

Bits	Name	Description
31:22	RESERVED_31_22	RFU
21:16	RD_CMD_FIFO_DEPTH	Sets the maximum number of read command FIFO entries that may be used at any time. The AXI slave will use at most RD_CMD_FIFO_DEPTH + 1 entires. For example setting this field to 0x0F allows all 16 entires of the buffer to be used.
15:6	RESERVED_15_6	RFU

EBI1_CH0_SLV_RD_CONFIG (cont.)

Bits	Name	Description
5:0	RD_DATA_FIFO_DEPTH	Sets the maximum number of 64 bit Read Buffer entries that may be used at any time. The Read Buffer will use at most RD_FIFO_DEPTH + 1 entires. For example setting this field to 0x3F allows all 64 entires of the buffer to be used. Must not be less than 0xF.

0x00A40008 EBI1_CH0_SLV_RD_STATUS

Type: Read
Clock: AXI_CLK
Reset State: 0x0000FF00

EBI1_CH0_SLV_RD_STATUS

Bits	Name	Description
31:28	RESERVED_31_28	RFU
27:24	RDQUAL_FIFO_ENTRIES_IN_USE	The number of read qualifier FIFO entries that have been reserved for use by reads commands sent to the DDR controller.
23:16	RDDATA_FIFO_ENTRIES_IN_USE	The number of read data FIFO entries that have been reserved for use by reads commands sent to the DDR controller.
15:8	RDDATA_FIFO_EMPTY	The empty status of each of the read data FIFOs. Bit 8 corresponds to the positive-edge dq[0] FIFO. Bit 9corresponds to the positive-edge dq[1] FIFO. Bit 10corresponds to the positive-edge dq[2] FIFO. Bit 11corresponds to the positive-edge dq[3] FIFO. Bit 12corresponds to the negative-edge dq[0] FIFO. Bit 13corresponds to the negative-edge dq[1] FIFO. Bit 14corresponds to the negative-edge dq[2] FIFO. Bit 15corresponds to the negative-edge dq[3] FIFO
7:1	RESERVED_7_1	RFU
0	DQS_ERROR	Set by the hardware if the read data FIFOs have been non-empty while no read commands where outstanding since reset. This bit being set is a strong indication of a spurious DQS edge.

0x00A4000C EBI1_CH0_SLV_WR_CONFIG

Type: Read/Write
Clock: AXI_CLK
Reset State: 0xD70F040F

Write Buffer Configuration Register

The write coalescing buffer is part of the write data path and cannot be completely disabled. However, all read merging and all write coalescing across bursts can be disabled via the SLV_WR_CONFIG register. Beats within narrow (each beat transfers less than the bus width) bursts may be coalesced in any configuration.

EBI1_CH0_SLV_WR_CONFIG

Bits	Name	Description
31	COALESCE_EN	Enable write coalescing. When enabled, data from separate AXI bursts will coalesced. Packing of narrow beats from a single burst is always allowed. 0x0: Disable 0x1: Enable
30	READ_MERGE_EN	Enable read merging with Write Coalescing buffer data. When disabled reads are not executed while the required data is in the write buffer. Also, the Write Buffer is flushed after each burst. 0x0: Disable 0x1: Enable
29	FLUSH	When set to 1, the hardware will flush the Write Coalescing Buffer. Hardware will clear this bit when the requested flush is complete.
28	EMPTY	1 when any valid data exists in the Write Coalescing Buffer. Read-only to software.
27	WRITE_BLOCK_READ	When set, no read command is allowed to execute while there is any write data in the buffer or there are any write commands in the write command buffer. When the Read Command Buffer is limited to one command, read merging is disabled and write coalescing is disabled and this bit is set, the DDR controller will execute commands in the order in which they were received on the AXI bus.
26:24	CMD_BUF_DEPTH	
23:21	RESERVED_23_21	RFU
20:16	FLUSH_UPPER_LIMIT	The flush high water mark. Flushing will begin when the number of valid lines in the Write Coalescing Buffer is greater than FLUSH_UPPER_LIMIT. FLUSH_UPPER_LIMIT must be less than or equal to the number of lines specified in WR_BUFFER_DEPTH. Also, FLUSH_UPPER_LIMIT must be greater than FLUSH_LOWER_LIMIT.
15:13	RESERVED_15_13	RFU
12:8	FLUSH_LOWER_LIMIT	The flush low water mark. Once flushing has begun, lines will be flushed until the number of valid lines is less than or equal to FLUSH_LOWER_LIMIT.
7:5	RESERVED_7_5	RFU
4:0	WR_BUFFER_DEPTH	Sets the maximum number of Write Coalescing Buffer lines that may be used at any time. The Write Coalescing Buffer will use at most WR_BUFFER_DEPTH + 1 entires. For example setting this field to 0xF allows 16 entires of the buffer to be used. Must not be less than 0x5.

0x00A40010 EBI1_CH0_SLV_FLUSH_CONFIG

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x8000800F

Write Buffer Flush Configuration Register

EBI1_CH0_SLV_FLUSH_CONFIG

Bits	Name	Description
31:30	FLUSH_PRIORITY	When the high water mark (see SLV_WR_CONFIG) has been reached, flush the lines with a priority of FLUSH_PRIORITY.
29	RESERVED_29	RFU
28	FLUSH_IN_ORDER	Write Coalescing Buffer lines are flushed in the order in which they were created
27:18	RESERVED_27_18	RFU
17:8	FLUSH_IDLE_DELAY	After the controller is idle for FLUSH_IDLE_DELAY AXI cycles, the Write Buffer will be flushed.
7:0	PAGE_HIT_WINDOW	If the last line was flushed less than PAGE_HIT_WINDOW AXI cycles ago, lines within the same page as the last victim are preferred. Otherwise, lines are flushed oldest to youngest.

0x00A40014 EBI1_CH0_SLV_ID_REVISION

Type: Read
Clock: AXI_CLK
Reset State: 0x00005310

Revision ID Register

This register contains the revision numbers of DDR controller core.

EBI1_CH0_SLV_ID_REVISION

Bits	Name	Description
31:16	RESERVED_31_16	
15:12	REV_MAJOR	Major Revision
11:8	REV_MINOR	Minor Revision
7:4	SITE_ID	Site ID 0x1: RTP
3:0	RESERVED_3_0	

0x00A40020+4*n EBI1_CH0_SLV_ADDR_BASE_CSn, n=[0..1]

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000000

System Base Address Register for n

This register defines the base address for the memory that associates to chip select n.

When using ADDR_MAP_MODE == 2'b10 (see SLV_ADDR_MAP_CSn), the base address must be the base address of the entire space allocated to the controller.

EBI1_CH0_SLV_ADDR_BASE_CSn

Bits	Name	Description
31:16	RESERVED_31_16	
15:8	BASE_ADDR	Defines the Base Address decode, in conjunction with the SLV_ADDR_MAP_CSn, to determine the address space of the targeted chip select. The Base Address is compared to the AXI address bus bits [31:24]. If the portions of the two addresses match, then the particular CS is accessed.
7:0	RESERVED_7_0	RFU

0x00A40030+4*n EBI1_CH0_SLV_ADDR_MAP_CSn, n=[0..1]

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000100

System Address Mapping Register for Rank n.

This register defines the way to map AXI system address into rank/bank/row/column address to memory devices. Once the number of bank, row size and column size are defined, the memory size of the associated rank is defined.

NOTE When ADDR_MAP_MODE is set to 2'b10 and the controller both ranks must be programmed identically with respect to the SLV_ADDR_BASE_CSn, SLV_ADDR_MAP_CSn and SLV_ADDR_SIZE_MASK_CSn registers.

EBI1_CH0_SLV_ADDR_MAP_CSn

Bits	Name	Description
31:16	RESERVED_31_16	

EBI1_CH0_SLV_ADDR_MAP_CSn (cont.)

Bits	Name	Description
15	RANK_EN	Rank has memory devices attached 0x0: Rank not present (default) 0x1: Rank is present
14	RESERVED_14	RFU
13:12	ADDR_MAP_MODE	Addressing Mode Configuration. Selects the Addressing Mode of the Rank and determines the mapping of the System Address to the Memory Address. Configuring the AddrMode for "Rank,Bank, Row, Column" mode will map the system address in manner that is compatible with the Partial Array Self-Refresh Mechanism. The Partial Array Self-Refresh Mechanism is not supported unless AddrMode is configured for "Rank,Bank,Row,Column" mode. Mapping mode 10 (Row, Bank, Rank, Column) requires that the memory device on each rank has the same row, bank and column width and that SLV_ADDR_BASE_CSn, SLV_ADDR_SIZE_MASK_CSn and SLV_ADDR_MAP_CSn are programmed identically for each rank. Those registers are programmed as normal, according to the device parameters. 0x0: Rank, Row, Bank, Column (default) 0x1: Rank, Bank, Row, Column 0x2: Row, Bank, Rank, Column 0x3: Reserved
11:9	RESERVED_11_9	RFU
8	NUM_BANK	Specifies the number of banks in the memory device. 0x0: 4 banks 0x1: 8 banks (default)
7:6	RESERVED_7_6	RFU
5:4	WIDTH_ROW	Specifies the number of bits used for the row address of the external memory 0x0: 12 bits (default) 0x1: 13 bits 0x2: 14 bits 0x3: 15 bits
3:2	RESERVED_3_2	RFU
1:0	WIDTH_COL	Specifies the number of bits used for the column address of the external memory 0x0: 8 bits (default) 0x1: 9 bits 0x2: 10 bits 0x3: 11 bits

0x00A40040+4*n EBI1_CH0_SLV_ADDR_SIZE_MASK_CSn, n=[0..1]

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000000

System Address Size Mask Register for Rank n

This register defines the memory capacity of memory that associates to chip select n.

EBI1_CH0_SLV_ADDR_SIZE_MASK_CSn

Bits	Name	Description
31:16	RESERVED_31_16	
15:8	ADDR_MASK	Define the address size mask bits: 0x0: reserved 0x80: 2GB 0xC0: 1GB 0xE0: 512MB 0xF0: 256MB 0xF8: 128MB 0xFC: 64MB 0xFE: 32MB 0xFF: 16MB
7:0	RESERVED_7_0	RFU

0x00A40050 EBI1_CH0_SLV_STALL

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000004

SMI/EBI1 Stall Request and Status Register.

This register provides a mechanism to stall the AXI traffic and drain the internal request queues for the memory controller.

EBI1_CH0_SLV_STALL

Bits	Name	Description
31:3	RESERVED_31_3	
2	AXI_IDLE	The value of the o_axi_idle pin. This is only an indication that all read, write and QoS responses have been sent. It does, by itself, guarantee that the controller has completed all transactions.

EBI1_CH0_SLV_STALL (cont.)

Bits	Name	Description
1	STALL_ACK	SMI/EBI1 Stall Request Status: (After a valid STALL_REQ is asserted, this bit will be set to 1'b1 when AXI interface is stalled and all internal memory commands are executed. No further read/write commands will be sent to memory.) 0x0: normal operation (default) 0x1: AXI stalled and cmd q empty
0	STALL_REQ	SMI/EBI1 Stall Request: (Setting this bit to 1'b1 will stall all AXI traffic. axi_aready and axi_wready will be de-asserted and all AXI requests will NOT be accepted. Previously accepted DDR memory requests will continued be serviced. Setting this bit to 1'b0 will make the controller accept the new AXI requests. This mechanism can be used whenever software needs to switch the voltage or clock frequency of the controller.) 0x0: normal operation (default) 0x1: stall AXI traffic

0x00A40100 EBI1_CH0_SLV_ERR_ADDR

Type: Read
Clock: AXI_CLK
Reset State: 0x00000000

Slave Error Address Register.

This register contains the address of the request that caused the decode or MPU error. The error address is locked with the first error address.

EBI1_CH0_SLV_ERR_ADDR

Bits	Name	Description
31:0	ERR_ADDR	The address of the request that caused the bus error

0x00A40108 EBI1_CH0_SLV_ERR_APACKET_0

Type: Read
Clock: AXI_CLK
Reset State: 0x0000

Slave Error Address Attributes Register 0.

This register provides various information about the request that caused the AXI bus error.

EBI1_CH0_SLV_ERR_APACKET_0

Bits	Name	Description
31:16	RESERVED_31_16	RFU
15:0	ERR_AMID	The master ID of the request that caused the bus error.

0x00A4010C EBI1_CH0_SLV_ERR_APACKET_1

Type: Read
Clock: AXI_CLK
Reset State: 0x00000000

Slave Error Address Attributes Register 1.

This register provides various information about the request that caused the AXI bus error.

EBI1_CH0_SLV_ERR_APACKET_1

Bits	Name	Description
31:28	RESERVED_31_28	RFU
27:24	ERR_ALEN	The burst length of the request that caused bus error
23:16	ERR_ATID	The transfer ID of the request that caused the bus error.
15:13	ERR_ASIZE	The ASIZE of the request that caused the bus error 0x0: byte 0x1: half_word 0x2: word 0x3: double_word 0x4: Reserved_4 0x5: Reserved_5 0x6: Reserved_6 0x7: Reserved_7
12	ERR_ABURST	The ABURST of the request that caused the bus error 0x0: wrap 0x1: increment

EBI1_CH0_SLV_ERR_APACKET_1 (cont.)

Bits	Name	Description
11:8	ERR_ATYPE	The ATYPE of the request that caused the bus error Strongly-ordered and weakly-ordered concatenated with the integer. 0x0: strongly_ordered_0 0x1: strongly_ordered_1 0x2: weakly_ordered_2 0x3: weakly_ordered_3 0x4: weakly_ordered_4 0x5: weakly_ordered_5 0x6: weakly_ordered_6 0x7: weakly_ordered_7 0x8: strongly_ordered_8 0x9: strongly_ordered_9 0xA: weakly_ordered_A 0xB: weakly_ordered_B 0xC: weakly_ordered_C 0xD: weakly_ordered_D 0xE: weakly_ordered_E 0xF: weakly_ordered_F
7:6	ERR_ALOCK	The ALOCK of the request that caused the bus error 0x0: normal 0x1: exclusive 0x2: locked 0x3: barrier
5:4	RESERVED_5_4	Reserved
3	ERR_APROTNS	The APROTNS of the request that caused the bus error. 0x0: secure 0x1: non secure
2	ERR_AOOORD	The AOOORD of the request that caused the bus error 0x0: in order 0x1: out of order
1	ERR_AOOOWR	The AOOOWR of the request that caused the bus error 0x0: in order 0x1: out of order
0	ERR_AWRITE	The awrite of the request that caused bus error 0x0: read 0x1: write

0x00A40114 EBI1_CH0_SLV_ERR_CNTL

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00001000

Slave Error Code Register.

This register provides additional data about the bus error. Additionally, each slave which is capable of detecting an error is also required to have a single programmable register that can be used to optionally interrupt the processor core. This interrupt mechanism is required since write transfers may be posted on the bus and the AXI transfer may complete prior to the occurrence of the error in the AXI interconnect or slave device. The interrupt from the AXI interconnect and the AXI slave devices will be directed to the interrupt controller.

EBI1_CH0_SLV_ERR_CNTL

Bits	Name	Description
31:16	RESERVED_31_16	
15:13	RESERVED_15_13	
12	IRQ_EN	Mask off the bus error interrupt to processor 0x0: disables IRQ 0x1: enables IRQ (default)
11:9	RESERVED_11_9	
8	CLEAR_ERR	Clear error status bit Writing a '1' to this bit will clear the ERR_OCCURRED bit in this register. It will NOT clear other error registers. 0x0: no clear (default) 0x1: clear
7:5	RESERVED_7_5	
4	ERR_OCCURRED	Error Status bit to indicate that an error has occurred. This bit can be set by software. To clear this bit a '1' must be written to the CLEAR_ERR field. Writing a '0' to this field has no effect. 0x0: no error occurred 0x1: error occurred
3:2	RESERVED_3_2	
1:0	ERR_CODE	MPU error and address decode error: Writes to this field are ignored. 0x0: no error (default) 0x1: address decode error 0x2: mpu error 0x3: both

0x00A40200 EBI1_CH0_SLV_PMON_CFG_ACHAN

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000000

AXI Slave Performance Monitors

Table 13-3 AXI Performance Monitor event index

Index	Description
0	AXI cycles
1	AXI address channel commands accepted
2	AXI address channel commands matching the attribute in SLV_PMON_CFG_ACHAN
3	High priority AXI address channel commands accepted
4	Number of AXI cycles in which the number of reserved global monitors is greater than or equal to SLV_PMON_CFG_0[N_MONITORS]
5	Number of AXI cycles in which the number of read commands in the read command buffer is greater than or equal to SLV_PMON_CFG_0[N_RD_CMDS]
6	Number of AXI cycles in which the number of write commands in the write command buffer is greater than or equal to SLV_PMON_CFG_0[N_WR_CMDS]
7	Number of AXI cycles in which the number of reserved read data FIFO entires is greater than or equal to SLV_PMON_CFG_0[N_RD_DATA_ENTRIES]
8	Number of AXI cycles in which the number of reserved read qualifier FIFO entires is greater than or equal to SLV_PMON_CFG_0[N_RD_QUAL_ENTRIES]
9	Number of AXI cycles in which the number of valid write data buffer lines is greater than or equal to SLV_PMON_CFG_0[N_WR_DATA]
10	The number of read commands that fully or partially hit in the write buffer
11	The number of write commands that fully or partially hit in the write buffer
12	TBD - Hazards

AXI Performance Monitor event index 2 records the number of address channel requests that match the following fields. The fields can be independently enabled/disabled with the MATCH_* fields in SLV_PMON_CFG_0. When an address channel request is accepted from the bus its attributes are compared to the fields of this register. If all enabled fields in SLV_PMON_CFG_ACHAN (see SLV_PMON_CFG_0) match the address channel request, the performance monitor is incremented. Any disabled fields match all transactions.

EBI1_CH0_SLV_PMON_CFG_ACHAN

Bits	Name	Description
31:16	AMID	AMID field of transactions to be counted with performance monitor index 2.
15:13	RESERVED_15_13	RFU
12:8	ATID	ATID field of transactions to be counted with performance monitor index 2.

EBI1_CH0_SLV_PMON_CFG_ACHAN (cont.)

Bits	Name	Description
7	RESERVED_7	RFU
6:4	ASIZE	ASIZE field of transactions to be counted with performance monitor index 2.
3:0	ALEN	ALEN field of transactions to be counted with performance monitor index 2.

0x00A40204 EBI1_CH0_SLV_PMON_CFG_0

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000000

EBI1_CH0_SLV_PMON_CFG_0

Bits	Name	Description
31	MATCH_AMID	Enable AMID matching for event index 2. When disabled, all AMIDs are considered a match.
30	MATCH_ATID	Enable ATID matching for event index 2. When disabled, all ATIDs are considered a match.
29	MATCH_ASIZE	Enable ASIZE matching for event index 2. When disabled, all ASIZEs are considered a match.
28	MATCH_ALEN	Enable ALEN matching for event index 2. When disabled, all ALENs are considered a match.
27:23	N_WR_DATA	See Table 1-3.
22:19	N_WR_CMDS	See Table 1-3.
18:14	N_RD_QUAL_ENTRIES	See Table 1-3.
13:7	N_RD_DATA_ENTRIES	See Table 1-3.
6:3	N_RD_CMDS	See Table 1-3.
2:0	N_MONITORS	See Table 1-3.

0x00A40208 EBI1_CH0_SLV_TEST_CONFIG

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000000

EBI1_CH0_SLV_TEST_CONFIG

Bits	Name	Description
31:8	RESERVED_31_8	RFU
7:4	SELECT	Selects the AXI slave internal signal to drive out on the AXI test bus. All other values will result in undefined behavior. 0x0: test_bus_0 0x1: test_bus_1 0x2: test_bus_2 0x3: test_bus_3 0x4: test_bus_4 0x5: test_bus_5 0x6: test_bus_6
3:1	RESERVED_3_1	RFU
0	ENABLE	Enable the slave's test bus.

13.2.1.4 MPU Configuration Registers

0x00A60000+ 4*n EBI1_CH0_MPU_PRTn_RACR, n=[0..15]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU. These registers include a single bit per VMID granting read access

EBI1_CH0_MPU_PRTn_RACR

Bits	Name	Description
31:0	RE	Read enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read access to the registers in the associated resource group.

0x00A60400+ 4*n EBI1_CH0_MPU_PRTn_WACR, n=[0..15]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

These registers exist only for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU.

EBI1_CH0_MPU_PRTn_WACR

Bits	Name	Description
31:0	WE	Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID write access to the registers in the associated resource group.

0x00A60800+4*n EBI1_CH0_MPU_PRTn_START, n=[0..15]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition Start Address Register. This register contains the start address of the partition. Only the bit numbers indicated by MPU_IDR[MSb] through MPU_IDR[LSb] are valid and physically exist.

EBI1_CH0_MPU_PRTn_START

Bits	Name	Description
31:12	ADDR	MPU Partition Start Address
11:0	RESERVED_11_0	Reserved

0x00A60C00+4*n EBI1_CH0_MPU_PRTn_END, n=[0..15]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition End Address Register. This register contains the start address of the partition.Only the bit numbers indicated by MPU_IDR[MSB] through MPU_IDR[LSB] are valid and physically exist.

EBI1_CH0_MPU_PRTn_END

Bits	Name	Description
31:12	ADDR	MPU Partition End Address
11:0	RESERVED_11_0	Reserved

0x00A60F80 EBI1_CH0_MPU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Configuration Register: This register includes fields governing various MPU behaviors.

EBI1_CH0_MPU_CR

Bits	Name	Description
31:2	RESERVED31_2	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set MPU_ESR. MPU_EAR and MPU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set MPU_ESR. MPU_EAR and MPU_ESYNR0 updated with address and syndrome of error.
2	MPUEIE	MPU Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the MPU. Interrupt output is asserted if MPU_CR[MPUEIE] = 1 and any bit is set in MPU_ESR.
1	MPUERE	MPU Error Report Enable. MPUERE = 0 causes the MPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master. MPUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective MPU port. Errors from either port are terminated by the MPU as RAZ/WI Both client and configuration port errors are recorded in MPU_ESR, independent of the value of MPU_CR[MPUERE]
0	MPUE	MPU Enable. Governs whether MPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures MPU and the MID to VMID mapping tables.

0x00A60F84 EBI1_CH0_MPU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the MPU, for both the client port and the configuration port.

EBI1_CH0_MPU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x00A60F88 EBI1_CH0_MPU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the MPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the MPU's interrupt output (when enabled by MPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the MPU_ESYNRn registers, which are merely the "syndrome" of an error indicated by MPU_ESR.

EBI1_CH0_MPU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x00A60F8C EBI1_CH0_MPU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Restore Register. This register is an aliased address for the MPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

EBI1_CH0_MPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x00A60F90 EBI1_CH0_MPU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

EBI1_CH0_MPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x00A60F94 EBI1_CH0_MPU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

EBI1_CH0_MPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x00A60FF4 EBI1_CH0_MPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

MPU Revision Register: This register provides major/minor revision codes for the implementation.

EBI1_CH0_MPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x00A60FF8 EBI1_CH0_MPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x1F0C2C0F

MPU ID Register: Read-only register that defines various configuration attributes of the MPU instance.

EBI1_CH0_MPU_IDR

Bits	Name	Description
31:29	RESERVED31_29	Reserved
28:24	MSB	Indicates most significant address bit number used in START/END address comparisons.
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used in START/END address comparisons.
15:14	RESERVED15_12	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only MPU_PRTn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate MPU_PRTn_RACR and MPU_PRTn_WACR registers govern read vs. write access. For single VMID, MPU_PRTn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields

EBI1_CH0_MPU_IDR (cont.)

Bits	Name	Description
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. MPU_PRTn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMD type access control. MPU_PRTn_xACR registers include separate bit per VMID (32 bits) for governing access.
9:8	RESERVED9_8	Reserved
7:0	NPRT	Number of partitions. Indicates the number of partitions (minus 1) supported by the MPU. Values range from 0-223 (1-224 partitions)

0x00A60FFC EBI1_CH0_MPU_MPU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

MPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the MPU (including the MPU_MPU_ACR itself).

EBI1_CH0_MPU_MPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the MPU's 4KB address region (including the MPU_MPU_ACR itself). For single VMID type MPUs (MPU_IDR[MV] = 0) the MPU_MPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

13.2.1.5 DDR Configuration Registers

0x00A80000 EBI1_CH0_DDR_DEVICE_CONFIG

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Memory Configuration Register.

The register is used to set up DRAM configuration in the DDR controller.

EBI1_CH0_DDR_DEVICE_CONFIG

Bits	Name	Description
31:28	RESERVED_31_28	
27:26	DEVICE_CONFIG_RANK1	SW: RW, HW: R Device Configuration for Rank 1. This is required for SRR in order to update the refresh rate correctly if multiple devices are involved. 0x0: reserved (default) 0x1: x8,x8,x8,x8 0x2: x16, x16 0x3: x32
25:24	DEVICE_CONFIG_RANK0	SW: RW, HW: R Device Configuration for Rank 0. This is required for SRR in order to update the refresh rate correctly if multiple devices are involved. 0x0: reserved (default) 0x1: x8,x8,x8,x8 0x2: x16, x16 0x3: x32
23:18	RESERVED_23_18	
17	INIT_DONE_RANK1	SW: RW, HW: R DDR Software initialization Complete SW writes this bit after initialization is complete for rank 1. 0x0: init incomplete (default) 0x1: init complete
16	INIT_DONE_RANK0	SW: RW, HW: R DDR Software initialization Complete SW writes this bit after initialization is complete for rank 0. 0x0: init incomplete (default) 0x1: init complete
15:14	NUM_BANKS	SW: RW, HW: R Indicates number of banks of the SDRAM device. Typically, LPDDR1 devices are 4 bank only, LPDDR2 & PCDDR2 devices can be 4 or 8 bank while PCDDR3 devices are 8 bank only. 0x0: 4 (default) 0x1: 8 0x2: Reserved_1 0x3: Reserved_2
13:12	RESERVED_13_12	

EBI1_CH0_DDR_DEVICE_CONFIG (cont.)

Bits	Name	Description
11:10	CLK_SYNC_MODE	SW: R, HW: RW DDR clocked programmed by SW. Read Only. 0x0: Asynchronous (default) 0x1: Synchronous 0x2: Iso Synchronous 0x3: Reserved
9:7	DEVICE_TYPE	SW: RW, HW: None Specify DRAM Device Type. 0x0: LPDDR (default) 0x1: LPDDR2-S2 0x2: LPDDR2-S4 0x3: PCDDR2 0x4: PCDDR3 0x5: Reserved_1 0x6: Reserved_2 0x7: Reserved_3
6	RESERVED_6	
5	MEM_CLK_CONFIG	SW: RW, HW: R Rank Clock Configuration: Note that the initialization of the individual memory ranks is otherwise unchanged when using this feature. 0x0: CK0 drives both Rank 0 and 1 (default) 0x1: CK0 for Rank0 and CK1 for Rank1
4	DDR_COMMAND_BUS	SW: RW, HW: R Specify if DDR needs to be used on the command bus (in addition to the data bus). This needs to be enabled LPDDR2 SDRAM devices & disabled for others. 0x0: Disable (default) 0x1: Enable
3:2	RESERVED_3_2	
1	RANK1_EN	SW: RW, HW: R Rank 1 is present 0x0: Rank not present (default) 0x1: Rank is present
0	RANK0_EN	SW: RW, HW: R Rank 0 is present. 0x0: Rank not present (default) 0x1: Rank is present

0x00A80004 EBI1_CH0_DDR_DEVICE_STATUS

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Device Status Register

This register enables software to read memory device status.

EBI1_CH0_DDR_DEVICE_STATUS

Bits	Name	Description
31:18	RESERVED_31_18	
17	INTERRUPT_EN	SW: RW, HW: R Interrupt will be generated if temperature out-of-range is detected i.e RANK0/1_TEMP_OO_RANGE is set. The interrupt will be set (sticky behavior) until SW can clear it by clearing the RANK0/1_TEMP_OO_RANGE field. The temperature out of range is due to SRR which is a feature only available in LPDDR1/LPDDR2 devices. 0x0: Disable (default) 0x1: Enable
16	CURR_SEL_REG_FREQ_SWITCH	SW: R, HW: W Indicates which DDR timing register set is being currently used. If DDR_CMD_EXEC_OPT_2[UPDATE_MEM_LATENCY_ON_FREQ_SWITCH] is set, then certain CSR fields in DDR_DRAM_TIMING_6 and DDR_CMD_EXEC_OPT_3 are also shadowed. 0x0: DDR_DRAM_TIMING CSRs (default) 0x1: DDR_DRAM_TIMING_ALT CSRs
15:14	RESERVED_15_14	
13	IN_DEEP_POWER_DOWN_RANK1	SW: R, HW: W Indicates the rank 1 is currently in deep power down mode. Deep power down feature is only available in LPDDR1/LPDDR2 devices. 0x0: Not in deep power down (default) 0x1: in deep power down
12	IN_DEEP_POWER_DOWN_RANK0	SW: R, HW: W Indicates the rank 0 is currently in deep power down mode. Deep power down feature is only available in LPDDR1/LPDDR2 devices. 0x0: Not in deep power down (default) 0x1: in deep power down
11:10	RESERVED_11_10	
9	IN_SELF_RFSH_RANK1	SW: R, HW: W Indicates the rank 1 is currently in self-refresh mode 0x0: Not in self-refresh (default) 0x1: in self-refresh

EBI1_CH0_DDR_DEVICE_STATUS (cont.)

Bits	Name	Description
8	IN_SELF_RFSH_RANK0	SW: R, HW: W Indicates the rank 0 is currently in self-refresh mode 0x0: Not in self-refresh (default) 0x1: in self-refresh
7:6	RESERVED_7_6	
5	RANK1_TEMP_OO_RANGE	SW: RW, HW: W Indicates any out-of-range operating temperature for Rank1 This bit is set to '1' if the SRR read returns a temperature reading that is out of range on the high side. This bit is sticky and can only be cleared by software write. The temperature out of range is due to SRR which is a feature only available in LPDDR1/LPDDR2 devices. 0x0: Within range (default) 0x1: Out of range
4	RANK0_TEMP_OO_RANGE	SW: RW, HW: W Indicates any out-of-range operating temperature for Rank0 This bit is set to '1' if the SRR read returns a temperature reading that is out of range on the high side. This bit is sticky and can only be cleared by software write. The temperature out of range is due to SRR which is a feature only available in LPDDR1/LPDDR2 devices. 0x0: Within range (default) 0x1: Out of range
3:2	RESERVED_3_2	
1	RANK1_IDLE	SW: R, HW: W Rank1 Idle Status. If set, it indicates that there are no transactions to that rank and also indicates that the timing parameters have been satisfied such that if the pages are open, they could be closed. 0x0: Rank Busy (default) 0x1: Rank Idle
0	RANK0_IDLE	SW: R, HW: W Rank0 Idle Status. If set, it indicates that there are no transactions to that rank and also indicates that the timing parametes have been satisfied such that if the pages are open, they could be closed. 0x0: Rank Busy (default) 0x1: Rank Idle

0x00A80010 EBI1_CH0_DDR_MANUAL_CMD

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Manual Command Register

This register enables the software to manually issue commands to DDR SDRAM interface. A value of '1' should be written in the bit field of the command that the software wants to force the controller to perform. (This includes the MRR and MRW bits of the DDR_MR_CNTL_WDATA CSR) Only one bit should be active at any given time, except for the "external clock on", the "reset_n" bit and the "CKE" bit. When the controller has finished executing the command, it will clear the bit (including the MRR, MRW and the RD_DQCAL bits of the DDR_MR_CNTL_WDATA CSR), except for the external clock on bit, the "CKE" bit and the "reset_n" bits. It is the software's responsibility to ensure all timing parameters are satisfied before executing the next manual command before the rank is initialized. Once the rank is initialized, it is HW's responsibility to execute the command when possible. The AUTO_REFRESH and PRECHARGE_ALL commands are not to be used after the rank has been initialized.

Once these bits are set, HW can potentially delay executing the command in order to ensure that the memory timings have been satisfied. (This statement is only applicable after the rank is initialized)

The initialization sequence of the SDRAM device is executed by SW via this register and the DDR_MR_CNTL_WDATA CSR.

EBI1_CH0_DDR_MANUAL_CMD

Bits	Name	Description
31:18	RESERVED_31_18	
17:16	RANK_SEL	SW: RW, HW: R Select which chip select should be targeted for the chosen manual command to be executed. 0x0: Invalid (default) 0x1: CS0 only 0x2: CS1 only 0x3: both CS0 CS1
15	RESERVED_15	
14	CK_ON	SW: RW, HW: R Turns on/off external clock CK, CKN. This bit does not reset automatically. Software must turn it on when the clock to the device needs to be enabled and keep it on.Unitl the rank is initialized, HW would control the clocks based on this setting. 0x0: Off (default) 0x1: On
13	CKE	SW: RW, HW: R Turns on/off clock enable CKE. This bit does not reset automatically. Software must turn it on when the clock to the device needs to be enabled and keep it on.Unitl the rank is initialized, HW would control the CKE based on this setting. 0x0: Off (default) 0x1: On

EBI1_CH0_DDR_MANUAL_CMD (cont.)

Bits	Name	Description
12	RESET_N	SW: RW, HW: R Turns on/off reset pin to PCDDR3 device only. This bit does not reset automatically. Software must turn it on, then turn it off 0x0: Active (default) 0x1: Inactive
11:7	RESERVED_11_7	
6	ENTER_DEEP_PD	SW: RW, HW: R Issue Deep Power Down. This bit is self-cleared once the command is executed. Deep Power down feature is only available on LPDDR1 and LPDDR2 SDRAM devices. HW will check to ensure all commands outstanding to the rank have completed before issuing the DPD command. 0x0: no-op (default) 0x1: Issue DPD
5	EXIT_DEEP_PD	SW: RW, HW: R Issue Exit Deep Power Down. This bit is self-cleared once the command is executed. Deep Power down feature is only available on LPDDR1 and LPDDR2 SDRAM devices. When exiting Deep Power Down for a given Rank, it is required to re-initialize the LPDDR1 SDRAM devices by repeating the initialization sequence for the associated Rank before that memory can be utilized or accessed. As such, it is necessary to clear the initialization complete state of the associated Rank by setting DDR_DEVICE_CONFIG[15/14] to 1'b0 before exiting Deep Power Down. It is SW's responsibility to ensure that the minimum duration of DPD is met. Additionally SW needs to ensure that the clocks are stable before exiting DPD. 0x0: no-op (default) 0x1: Issue DPD exit
4	ZQ_CAL_SHORT	SW: RW, HW: RW Issue Short ZQ-Cal Command. This bit is self-cleared once the command is executed. This only applies to PCDDR3 devices. For LPDDR2, use the DDR_MR_CNTL_WDATA CSR. 0x0: no-op (default) 0x1: Issue ZQ-Cal
3	ZQ_CAL_LONG	SW: RW, HW: RW Issue Long ZQ-Cal Command. This bit is self-cleared once the command is executed. This only applies to PCDDR3 devices. For LPDDR2, use the DDR_MR_CNTL_WDATA CSR. 0x0: no-op (default) 0x1: Issue ZQ-Cal

EBI1_CH0_DDR_MANUAL_CMD (cont.)

Bits	Name	Description
2	AUTO_REFRESH	SW: RW, HW: RW Auto-Refresh Command. This can only be set when the rank has not been initialized. This bit is self-cleared once the command is executed. 0x0: no-op (default) 0x1: execute
1	PRECHARGE_ALL	SW: RW, HW: RW Precharge All Command. This can only be set when the rank has not been initialized. This bit is self-cleared once the command is executed. 0x0: no-op (default) 0x1: execute
0	SR_READ	SW: RW, HW: RW Status Register Read Command for LPDDR1. SRR feature is only supported by LPDDR1 and LPDDR2 SDRAM devices. This bit is self-cleared once the command is executed and SR data is captured. The SR data for LPDDR1 is captured in DDR_MR_RDDATA_RANK0/1. A manual SRR command to LPDDR2 devices can be initiated by using the DDR_MR_CNTL_WDATA CSR. 0x0: no-op (default) 0x1: execute

0x00A80014 EBI1_CH0_DDR_MR_CNTL_WDATA

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Access Control Register

This register is used whenever SW needs to access the DRAM Mode Register. It is used in device initialization for programming the memory device's mode registers. Once the SDRAM device is initialized, it is used for issuing MRW commands to LPDDR1/LPDDR2/PCDDR2/PCDDR3. and MRR commands (manual SRR, manual ZQ commands) for LPDDR2.

EBI1_CH0_DDR_MR_CNTL_WDATA

Bits	Name	Description
31:24	MR_ADDR	SW: RW, HW: R Specify which mode register to access. Note that LPDDR2 supports up to 256 Mode registers. Hence the programmed MR_ADDR needs to be valid based on the specific SDRAM device. 0000_0000 : MR (Mode Register or SR for LPDDR1) 0000_0001 : EMR1 (Extended Mode Register 1) 0000_0010 : EMR2 (Extended Mode Register 2) 0000_0011 : EMR2 (Extended Mode Register 3) .....
23	RESERVED_23	
22	RD_DQCAL	SW: W, HW: RW DQ Calibration command. This is only supported for LPDDR2 & PCDDR3 devices. This is used for read training and/or rank auto detect. A pre-defined read pattern is sent out by the DRAM and captured by the controller. In case of LPDDR2, this is an MRR command with MR_ADDR specified above (valid MR_ADDR is 0x32 & 0x40). In case of PCDDR3 devices, this is an MPR Read command and hence MR_ADDR field is a don't care. The status of the DQ Calibration command is recorded in DDR_DQCAL_STATUS_RANK0/1 and in DDR_DQCAL_RDATA_RANK0/1. This bit is cleared by HW once the command is executed. 0x0: do not execute (default) 0x1: execute
21:20	RD_DQCAL_EXP_PATTERN	SW: RW, HW: R This is the read data pattern from the memory device. The values "00" and "01" are applicable only for LPDDR2 devices (memory burst length of 4), whereas the value "10" is applicable only for PCDDR3 devices (memory burst length of 8). 0x0: Pattern_1010 0x1: Pattern_0011 0x2: Pattern_01010101
19:18	MR_RANK_SEL	SW: RW, HW: R Specify DRAM rank to which the command goes. After the SDRAM device has been initialized, a value of "11" is considered illegal. 0x0: Invalid (default) 0x1: Rank 0 only 0x2: Rank 1 only 0x3: Both ranks 0 and 1

EBI1_CH0_DDR_MR_CNTL_WDATA (cont.)

Bits	Name	Description
17	MRR	SW: W, HW: RW Read Mode Register from LPDDR2 SDRAM. This bit is cleared by HW once the command is executed. MRR commands are only supported by LPDDR2 SDRAM devices and the read data is available in DDR_MR_RDATA_RANK0/1 after the command completes. 0x0: do not execute (default) 0x1: execute
16	MRW	SW: W, HW: RW Writes the Mode Register to the SDRAM. This bit is cleared by HW once the command is executed. 0x0: do not execute (default) 0x1: execute
15:0	MR_WDATA	SW: RW, HW: R Data for Mode Register Writes. SW needs to program the mode register based on the specific SDRAM device as the mapping of the 16-bits is different for different SDRAM device types.

0x00A80020 EBI1_CH0_DDR_MR_RDATA_RANK0

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Access Data Register for Rank0

This register contains the DRAM mode register contents. This is used to capture the read data from the SDRAM device's mode register. This register has bit-to-bit direct mapping to the DRAM mode register and it's software's responsibility to interpret results for reads. The bit definition will be different depending on mode registers and/or types of memory devices.

EBI1_CH0_DDR_MR_RDATA_RANK0

Bits	Name	Description
31:0	MR_RDATA	SW: R, HW: W Data for Mode Register Reads for Rank0

0x00A80024 EBI1_CH0_DDR_MR_RDATA_RANK1

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Access Data Register for Rank1

This register contains the DRAM mode register contents. This is used to capture the read data from the SDRAM device's mode register. This register has bit-to-bit direct mapping to the DRAM mode register and it's software's responsibility to interpret results for reads. The bit definition will be different depending on mode registers and/or types of memory devices.

EBI1_CH0_DDR_MR_RDATA_RANK1

Bits	Name	Description
31:0	MR_RDATA	SW: R, HW: W Data for Mode Register Reads for Rank1

0x00A80028 EBI1_CH0_DDR_MRR_REPEAT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Read Recurrence Register

This register is used to control recurrence of MR read. The most common use of these set of registers would be for the purpose of supporting SRR (Status Register Read) feature.

EBI1_CH0_DDR_MRR_REPEAT

Bits	Name	Description
31:24	MRR_ADDR	SW: RW, HW: R Specify which mode register to access. Note that LPDDR2 has up to 256 mode registers. The MRR_ADDR needs to be set such that it is valid for the specific SDRAM device. 0000_0000: MR (Mode Register or SR for LPDDR1) 0000_0001: (EMR1) Extended Mode Register 1 0000_0010: (EMR 2) Extended Mode Register 2 0000_0011: (EMR 3) Extended Mode Register 3 ....
23:19	RESERVED_23_19	
18:16	MRR_INTERVAL	SW: RW, HW: R Number of 128*1024 tcxo clock edges between SRR samples. 0x0: Disabled (default) 0x1: 128 0x2: 256 0x3: 512 0x4: 1024 0x5: 2048 0x6: 4096 0x7: 8192

EBI1_CH0_DDR_MRR_REPEAT (cont.)

Bits	Name	Description
15:14	MRR_RANK_SEL	SW: RW, HW: R Specifiy DRAM rank to which the command goes. 0x0: Not valid (default) 0x1: Rank 0 only 0x2: Rank 1 only 0x3: Both ranks 0 and 1
13:12	RESERVED_13_12	
11:8	MRR_INTERVAL_OVERRIDE	SW: RW, HW: R This is a debug switch which is only to be enabled for simulation purposes. As the MRR interval is huge, setting this reduces the size of the interval down counter. E.g., setting this to "1000" results in MRR interval of "001" to be mapped to an 8-bit down-counter (instead of 26 bit down-counter), MRR interval of "010" to be mapped to a 9-bit down counter and so on. This basically sets the down counter size of the first MRR interval mode (of "001") & the remaining MRR interval modes which are mapped to down-counter widthis are incremented by 1. 0x0: Disabled (default) 0x1: RESERVED_1 0x2: RESERVED_2 0x3: RESERVED_3 0x4: Size_of_4 0x5: Size_of_5 0x6: Size_of_6 0x7: Size_of_7 0x8: Size_of_8 0x9: Size_of_9 0xA: RESERVED_4 0xB: RESERVED_5 0xC: RESERVED_6 0xD: RESERVED_7 0xE: RESERVED_8 0xF: RESERVED_9
7:0	RESERVED_7_0	

0x00A80034 EBI1_CH0_DDR_MRR_REPEAT_DATA_RANK0

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Access Data Register for Rank0

This register contains the DRAM mode register contents the 32 bits of data for repetitive MR reads perfomed via DDR_MRR_REPEAT CSR. A common use of this register would be to hold the data for the SRR reads.

EBI1_CH0_DDR_MRR_REPEAT_DATA_RANK0

Bits	Name	Description
31:0	MRR_DATA	SW: R HW: W Mode register data for repetitive reads for Rank0

0x00A80038 EBI1_CH0_DDR_MRR_REPEAT_DATA_RANK1

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Access Data Register for Rank1

This register contains the DRAM mode register contents the 32 bits of data for repetitive MR reads performed via DDR_MRR_REPEAT CSR. A common use of this register would be to hold the data for the SRR reads.

EBI1_CH0_DDR_MRR_REPEAT_DATA_RANK1

Bits	Name	Description
31:0	MRR_DATA	SW: R HW: W Mode register data for repetitive reads for Rank1

0x00A8003C EBI1_CH0_DDR_CMD_EXEC_OPT_0

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00030000

DDR Command Execution Optimization Register 0.

This register is used to define the page management mode, command starvation of the DDR module. Additionally it also controls the enabling of the clockstop/powerdown features of the SDRAM device.

EBI1_CH0_DDR_CMD_EXEC_OPT_0

Bits	Name	Description
31:28	RESERVED_31_28	

EBI1_CH0_DDR_CMD_EXEC_OPT_0 (cont.)

Bits	Name	Description
27:16	PAGE_OPEN_TIMER	SW: RW, HW: R This field is only applicable if the page management policy/mode field is set to "timer-based". In this mode, a down counter based on DDR1x clock is started when the page is opened and the counter enabled only when the page is idle and has no pending runnable HITS. The value indicated by this field determines how long to wait for a potential runnable HIT to come along. When a runnable HIT appears while it is counting down, the counter gets reloaded to the initial value. 12'h000: Reserved 12'h001: Reserved 12'h002: Reserved 12'h003: MIN_CC (3 cycles) (default)
15	PAGE_MGMT_POLICY	SW: RW, HW: R Control how HW manages DRAM pages. 0x0: Keep Page Open (Keep Page Open unless forced to close it. e.g. forced to close because of a refresh, different page to open in the same bank if command causing a conflict has a priority greater than the highest priority of a pending HIT*, tRASmax timer expiry) 0x1: Timer Based (An additional reason to close the page would be if the "page_open_timer" expires)
14:7	RDCMD_STARVATION_TIMER	SW: RW, HW: R This specifies the number of ddr1x cycles since a read command became runnable. Once the down timer expires and the read command hasn't been executed, it gets elevated to a higher priority within the command's original priority level. 0000_0000: Disable (default) 0000_0001: RESERVED 0000_0010: MIN_CC (2 cycles)
6	WR_RD_PREF	SW: RW, HW: R Indicates the Column Command Selection Preference. For example, if set to '0', the column logic will give preference to selecting Read hits Vs. Write hits given they are of equal priority. 0x0: Prefer Reads (default) 0x1: Prefer Writes
5	DDR_CK_ALWAYS_ON_DBG_MODE	SW: RW, HW: R Debug mode wherein the clock to the memory device is always on. This is a debug mode as most of the chip configurations run in shared clock mode. If this debug mode is enabled, then SW needs to ensure that there are no IOCAL requests sent to the DDR controller for calibrating the clock pad. 0x0: Disabled (default) 0x1: Enable

EBI1_CH0_DDR_CMD_EXEC_OPT_0 (cont.)

Bits	Name	Description
4	CONCURRENT_SELF_REFRESH_EN	SW: RW, HW: R This only applies to multi-rank configurations. When set, this causes self refresh to be always entered/exited together for both ranks. This is specifically required to be set for ODT say for example, when DDR_CMD_EXEC_OPT_3[RANK0_ODT_ON_RD_RANK1] or DDR_CMD_EXEC_OPT_3[RANK1_ODT_ON_RD_RANK0] are set or in write scenarios wherein DDR_CMD_EXEC_OPT_3[EN_ODT_SWITCH_RANK_UNAVAIL] isn't used. It is to be noted that in this mode, SW will not have independent rank control for self refresh using DDR_CMD_EXEC_OPT_1[SELF_REFRESH_RANK1/0]. SW can set both bits and both the ranks will enter self refresh together when they can. 0x0: Disabled (default) 0x1: Enabled
3	SEL_REG_FREQ_SWITCH	SW: RW, HW: RW Not Supported. Switch the currently used timing register set to the other set (current set is determined via ddr_device_status[curr_sel_reg_freq_switch]). SW needs to guarantee that this bit is written only when HW is in self refresh mode. Additionally, SW should not write this bit if SW initiated HW sequence for clock switching is in progress. This bit is self-cleared once the command is executed. 0x0: no-op (default) 0x1: execute switch
2	PWR_DOWN_EN	SW: RW, HW: R Enable Power Down mode for the memory device. Power down is supported by LPDDR1/2 and PCDDR2/3 devices. **NOTE** HW will enter clockstop and powerdown irrespective of the enable setting if HW frequency switch using clockstop and powerdown request is received. 0x0: Disabled (default) 0x1: Enabled
1	CLK_STOP_EN	SW: RW, HW: R Enable Clock Stop mode for the memory device. This needs to be set depending on the SDRAM device present. For LPDDR1, this can be enabled, but for PCDDR2/3 & LPDDR2 devices, this must be disabled. **NOTE** HW will enter clockstop and powerdown irrespective of the enable setting if HW frequency switch using clockstop and powerdown request is received. 0x0: Disabled (default) 0x1: Enabled

EBI1_CH0_DDR_CMD_EXEC_OPT_0 (cont.)

Bits	Name	Description
0	CLK_STOP_DURING_PWR_DOWN_EN	SW: RW, HW: R Clock can be stopped to the memory device ONLY during Power Down. This can be enabled for LPDDR2, but must be disabled for PCDDR devices. Note that only CLK_STOP_EN field or this field can be set. LPDDR1 devices should utilize the CLK_STOP_EN setting rather than this setting. **NOTE** HW will enter clockstop and powerdown irrespective of the enable setting if HW frequency switch using clockstop and powerdown request is received. 0x0: Disabled (default) 0x1: Enabled

0x00A80040 EBI1_CH0_DDR_CMD_EXEC_OPT_1

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x0000FF0

DDR Command Execution Optimization Register 1.

EBI1_CH0_DDR_CMD_EXEC_OPT_1

Bits	Name	Description
31:28	RESERVED_31_28	
27	SELF_REFRESH_RANK1	SW: RW, HW: R Enter/Exit Self-Refresh. This bit does not reset automatically. Software must turn it on, then turn it off 0x0: exit (default) 0x1: enter
26	SELF_REFRESH_RANK0	SW: RW, HW: R Enter/Exit Self-Refresh. This bit does not reset automatically. Software must turn it on, then turn it off 0x0: exit (default) 0x1: enter
25:22	RESERVED_25_22	

EBI1_CH0_DDR_CMD_EXEC_OPT_1 (cont.)

Bits	Name	Description
21:12	RANK_IDLE_TIMER	SW: RW, HW: R Counts the number of XO clock cycles wherein the rank(s) is idle. Once expired, this will cause the rank to be in precharge state. This is an useful feature to enable especially if DDR_CMD_EXEC_OPT_0[PAGE_MGMT_POLICY] is set to "Keep Pages Open". 00_0000_0000: Disabled (default) 00_0000_0001: Reserved 00_0000_0010: Reserved
11:8	RUN_AT LEAST_ONE_TRANS_RD_CONFLICT	SW: RW, HW: R This is a vector sized to the number of priority levels (4). It the bit position corresponding to a priority level is set, then it indicates that a read conflict of that priority level can cause a page to close (if the conflict priority level is greater than the priority level of a pending HIT to the open page) only if at least one transaction has been run to an open page. 0xF: run_at least_one (default)
7:4	RUN_AT LEAST_ONE_TRANS_WR_CONFLICT	SW: RW, HW: R This is a vector sized to the number of priority levels (4). It the bit position corresponding to a priority level is set, then it indicates that a write conflict of that priority level can cause a page to close (if the conflict priority level is greater than the priority level of a pending HIT to the open page) only if at least one transaction has been run to an open page. 0xF: run_at least_one (default)
3	ENABLE_DDR2X_CLKON_DURING_CSPD	SW: RW, HW: R By default, the 2X clock will only be turned off only when both ranks are in self refresh and memory clock is no longer needed. This switch enables also turning off the 2X clock during clockstop and powerdown (this from memory perspective only applies to LPDDR1/LPDDR2 devices). 0x0: Disabled (default) 0x1: Enabled
2	ENABLE_POWER_OPT_AUTO_SRR_ZQ	SW: RW, HW: R When enabled, the design will not wakeup the memory device from self refresh (if in self refresh) just because of an auto SRR or an auto ZQCAL is needed. Instead it will promote the auto ZQCAL required to be a long zqcal if a normal auto ZQ was missed. 0x0: Disabled (default) 0x1: Enabled

EBI1_CH0_DDR_CMD_EXEC_OPT_1 (cont.)

Bits	Name	Description
1	ENABLE_CMD_ADDR_OE_CNTL	SW: RW, HW: R This is typically used for PCDDR3 devices. When enabled, the design will indicate to the PHY to tri-state the command address bus when all ranks are in self refresh and the memory clocks are off, as an additional power savings mode. This is required as a shunt resistance is typically used in the command address path for PCDDR3 memory boards and hence will always burn power as the command address is always driven. 0x0: Disabled (default) 0x1: Enabled
0	LOAD_TRP_CNTL	SW: RW, HW: R This bit controls as to when the TRP timer gets started. There seems to be a difference in the memory specifications which requires this control bit. When set to '0' (required for LPDDR1), the TRP timer gets loaded with the first precharge command that closes a rank/bank. Any subsequent precharges (e.g., precharge all) to that rank/bank are ignored as the state of the page is closed. When set to '1' (required for LPDDR2/PCDDR2/PCDDR3), the latest precharge command, e.g., precharge all will cause TRP timer to get reloaded even if the page was closed. 0x0: Valid Precharge (default) 0x1: Latest Precharge

0x00A80044 EBI1_CH0_DDR_CMD_EXEC_OPT_2

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000390

DDR Command Execution Optimization Register 2.

EBI1_CH0_DDR_CMD_EXEC_OPT_2

Bits	Name	Description
31	RESERVED_31	

EBI1_CH0_DDR_CMD_EXEC_OPT_2 (cont.)

Bits	Name	Description
30:28	ZQCAL_INTERVAL	SW: RW, HW: R Number of 256 timer clock edges between short ZQCalibrations. This feature is only available for LPDDR2 and PCDDR3 devices. When enabled, zqcalibration is scheduled for rank0 if enabled. Once it completes, zqcalibration is scheduled for rank1 if enabled. This assumes that the ranks zqcalibration commands cannot be overlapped. The timer clock usually runs at 32KHz, providing interval range of 40-2560ms. 0x0: Disabled (default) 0x1: 4 0x2: 8 0x3: 16 0x4: 32 0x5: 64 0x6: 128 0x7: 256
27:20	CLKON_IDLE_TIMER	SW: RW, HW: R Counts the number of DDR1x clock cycles wherein the DDR controller is idle and it's clock can be shut off. Once expired, this will cause the clkon request to get de-asserted. If TOP_MISC_CNTL[MODE_CLKON_DDR_2X] is set, then the value of this field needs to be at least the value of DDR_CMD_EXEC_OPT_2[CLKON2X_ASSERT_WAIT_TIMER]. 0000_0000: Disabled (default)
19:14	CLKON2X_ASSERT_WAIT_TIMER	SW: RW, HW: R Counts the number of DDR1x clock cycles to wait before waking up from self refresh or clockstop-powerdown (if DDR_CMD_EXEC_OPT_1[ENABLE_DDR2X_CLKON_DURING_CSPD] is enabled) after clkon2x asserts. This is to avoid any clock glitches propagating to the memory device. This delay (clock controller -> hsddrx) is not expected to be more than 15-20 ddr1x clock cycles and needs to be set if TOP_MISC_CNTL[MODE_CLKON_DDR_2X] is set. 00_0000: Disabled (default)
13:10	RESERVED_13_10	
9:8	RDCMD_HP_REMAP_LEVEL3	SW: RW, HW: R This is used to remap the high priority level 3 of the AXI Read command to a different priority level. 0x0: Map to Priority Level 0 0x1: Map to Priority Level 1 0x2: Map to Priority Level 2 0x3: Map to Priority Level 3 (default)

EBI1_CH0_DDR_CMD_EXEC_OPT_2 (cont.)

Bits	Name	Description
7:6	RDCMD_HP_REMAP_LEVEL2	SW: RW, HW: R This is used to remap the high priority level 2of the AXI Read command to a different priority level. 0x0: Map to Priority Level 0 0x1: Map to Priority Level 1 0x2: Map to Priority Level 2 (default) 0x3: Map to Priority Level 3
5:4	RDCMD_HP_REMAP_LEVEL1	SW: RW, HW: R This is used to remap the high priority level 1of the AXI Read command to a different priority level. 0x0: Map to Priority Level 0 0x1: Map to Priority Level 1 (default) 0x2: Map to Priority Level 2 0x3: Map to Priority Level 3
3:2	RDCMD_HP_REMAP_LEVEL0	SW: RW, HW: R This is used to remap the high priority level 0 of the AXI Read command to a different priority level. 0x0: Map to Priority Level 0 (default) 0x1: Map to Priority Level 1 0x2: Map to Priority Level 2 0x3: Map to Priority Level 3
1	RESERVED_1	
0	UPDATE_MEM_LATENCY_ON_FREQ_SWITCH	SW: RW, HW: R This is a valid bit which controls whether the memory latencies are required to be changed as part of frequency switch. The setting of this bit is dependent on the device type, the frequency of operation and the current memory latencies. If this bit is set, then the alternate values specified in DDR_UPDATE_FREQ_CHANGE_ALT CSR will be taken into account upon receiving a HW based frequency change request. Additionally, when this bit is set, then the mode register writes programmed in DDR_MRW0/1_HW_FREQ_SWITCH will be executed as part of the HW based frequency switch. 0x0: Disabled (default) 0x1: Enabled

0x00A80048 EBI1_CH0_DDR_CMD_EXEC_OPT_3

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000150

DDR Command Execution Optimization Register 3.

This register has controls for ODT for PCDDR2 and PCDDR3.

If DDR_CMD_EXEC_OPT_2[UPDATE_MEM_LATENCY_ON_FREQ_SWITCH] is set, then ODT_START_DELAY_RD/WR, ODT_OFF_DELAY and tANPD are frequency dependent fields.The alternate CSR field for ODT_START_DELAY_RD/WR below is DDR_UPDATE_FREQ_CHANGE_ALT[ODT_START_DELAY_RD/WR].

The alternate CSR field for ODT_OFF_DELAY below is DDR_UPDATE_FREQ_CHANGE_ALT[ODT_OFF_DELAY].

The alternate CSR field for tANPD below is DDR_UPDATE_FREQ_CHANGE_ALT[tANPD].

EBI1_CH0_DDR_CMD_EXEC_OPT_3

Bits	Name	Description
31	CODT_ON_WR	SW: RW, HW: R Enable the Controller ODT to be driven when write occurs on any rank. 0x0: Disable (default) 0x1: Enable
30	CODT_ON_RD	SW: RW, HW: R Enable the Controller ODT to be driven when read occurs on any rank. 0x0: Disable (default) 0x1: Enable
29	RANK1_ODT_ON_WR_RANK1	SW: RW, HW: R Enable Rank1 ODT to be driven when write occurs on Rank1. 0x0: Disable (default) 0x1: Enable
28	RANK1_ODT_ON_WR_RANK0	SW: RW, HW: R Enable Rank1 ODT to be driven when write occurs on Rank0. 0x0: Disable (default) 0x1: Enable
27	RANK1_ODT_ON_RD_RANK1	SW: RW, HW: R Enable Rank1 ODT to be driven when read occurs on Rank1. 0x0: Disable (default) 0x1: Enable
26	RANK1_ODT_ON_RD_RANK0	SW: RW, HW: R Enable Rank1 ODT to be driven when read occurs on Rank0. 0x0: Disable (default) 0x1: Enable
25	RANK0_ODT_ON_WR_RANK1	SW: RW, HW: R Enable Rank0 ODT to be driven when write occurs on Rank1. 0x0: Disable (default) 0x1: Enable

EBI1_CH0_DDR_CMD_EXEC_OPT_3 (cont.)

Bits	Name	Description
24	RANK0_ODT_ON_WR_RANK0	SW: RW, HW: R Enable Rank0 ODT to be driven when write occurs on Rank0. 0x0: Disable (default) 0x1: Enable
23	RANK0_ODT_ON_RD_RANK1	SW: RW, HW: R Enable Rank0 ODT to be driven when read occurs on Rank1. 0x0: Disable (default) 0x1: Enable
22	RANK0_ODT_ON_RD_RANK0	SW: RW, HW: R Enable Rank0 ODT to be driven when read occurs on Rank0. 0x0: Disable (default) 0x1: Enable
21:19	ODT_START_DELAY_WR	SW: RW, HW: R This delay only applies to the Rank ODT and not the controller ODT. Specifies the delay in ddr1x clock cycles between the DDR Write command and the ODT being driven high. Typically for PCDDR2 devices for writes, this should be set to (Write latency - tAOND) and for PCDDR3 devices for writes, this must be set to "1" for optimal settings. The above indicates the maximum value allowed for the ODT signal to be turned on/driven high w.r.t the write CAS command. Note that a value of "0" indicates that the ODT signal is turned on 1 cycle before the write CAS command. A value of "1" indicates that the ODT signal is turned on in the same cycle as the write CAS command and so on. The difference between the maximum value and the value programmed is required to be added as additional incremental delays to DDR_DRAM_TIMING_2[tOST], DDR_DRAM_TIMING_2[tRTW_SAME_RANK] and DDR_DRAM_TIMING_2[tRTW_DIFF_RANK] to avoid cases where in there is overlap among the different ODT signals. The values verified are MAX and MAX-1.

EBI1_CH0_DDR_CMD_EXEC_OPT_3 (cont.)

Bits	Name	Description
18:16	ODT_START_DELAY_RD	SW: RW, HW: R This delay only applies to the Rank ODT and not the controller ODT. Specifies the delay in ddr1x clock cycles between the DDR Read command and the ODT being driven high. Typically for PCDDR2 devices for reads, this should be set to (Read latency - tAOND) and for PCDDR3 devices for reads, this must be set to (Read Latency - (Write Latency - 2)) for optimal settings. The above indicates the maximum value allowed for the ODT signal to be turned on/driven high w.r.t the read CAS command. Note that a value of "0" indicates that the ODT signal is turned on 1 cycle before the read CAS command. A value of "1" indicates that the ODT signal is turned on in the same cycle as the read CAS command and so on. The difference between the maximum value and the value programmed might need to be added as additional incremental delays to DDR_SM_TIMING_0[DLY_RD_DIFF_RANK], DDR_DRAM_TIMING_2[WR_TO_RD_DLY_DIFF_RANK] to avoid cases where in there is overlap among the different ODT signals. The values verified are MAX and MAX-1.
15:13	ODT_OFF_DELAY	SW: RW, HW: R This delay specifies the ODT off memory timing parameter for rank ODT. For PCDDR2, if DDR_CMD_EXEC_OPT_0[PWR_DOWN_EN] is 1'b0 then program this to the timing parameter, tAOFD. For PCDDR2, if DDR_CMD_EXEC_OPT_0[PWR_DOWN_EN] is 1'b1 then program this to MAX(tAOFD, tANPD). For PCDDR3, this is to be programmed to "Write Latency -2", which is ODTLoff.
12:10	ODTH8	SW: RW, HW: R Specifies the timing parameter ODTH8 (for PCDDR3) in ddr1x clock cycles. If using PCDDR2, leave this as POR.
9	EN_ODT_SWITCH_RANK_UNAVAIL	SW: RW, HW: R This only applies in multi-rank systems. When enabled, the design will automatically turn ON the same rank's odt on a write (if not already configured) if the other rank's odt should have been turned on, but it can't as the other rank is in self refresh or power down (If EN_ODT_POWER_DOWN is 1'b1, then the only scenario where the dynamic switch is enabled is when the other rank is in self refresh). 0x0: Disable (default) 0x1: Enable
8	EN_ODT_POWER_DOWN	SW: RW, HW: R If set, then ODT will be driven to a rank (if required - based on ODT configuration) in powerdown mode. The optimal setting is for this bit to be enabled. 0x0: Disable 0x1: Enable (default)

EBI1_CH0_DDR_CMD_EXEC_OPT_3 (cont.)

Bits	Name	Description
7:6	ODT_EXTEND_DELAY_WR	SW: RW, HW: R Specifies the number of ddr1x clock cycles after the write completes should the rank's Rtt ODT resistance be turned off. The optimal case is "01". Additional delays might require the write to read same/diff rank timer delays to be increased. The difference between the value programmed and the optimal settings might need to be added as additional incremental delays to DDR_DRAM_TIMING_2[tOST], DDR_DRAM_TIMING_2[WR_TO_RD_DLY_DIFF_RANK] to avoid cases where in there is overlap among the different ODT signals. The values verified are "01" and "10". 0x0: Reserved 0x1: 1 clock cycle later (default) 0x2: 2 clock cycles later 0x3: 3 clock cycles later
5:4	ODT_EXTEND_DELAY_RD	SW: RW, HW: R Specifies the number of ddr1x clock cycles after the read completes should the rank's Rtt ODT resistance be turned off. The optimal case is "01". Additional delays might require the write to read same/diff rank timer delays to be increased. The difference between the value programmed and the optimal settings might need to be added as additional incremental delays to DDR_SM_TIMING_0[DLY_RD_DIFF_RANK], DDR_DRAM_TIMING_2[tRTW_SAME_RANK] and DDR_DRAM_TIMING_2[tRTW_DIFF_RANK] to avoid cases where in there is overlap among the different ODT signals. The values verified are "01" and "10". 0x0: Reserved 0x1: 1 clock cycle later (default) 0x2: 2 clock cycles later 0x3: 3 clock cycles later
3:1	TANPD	SW: RW, HW: R This specifies the memory timing parameter tANPD in ddr1x clock cycles. For PCDDR2 devices, program this to the timing parameter tANPD, for PCDDR3 devices, this needs to be programmed to WL - 1 (as per PCDDR3 spec).
0	DLL_CNTL_PCHG_PD	SW: RW, HW: R This field only applies to PCDDR3 devices. It indicates the mode register setting for MR0 bit 12. A value "0" represents that the DLL is frozen when precharge powerdown is entered, while a value "1" represents that the DLL is enabled during precharge powerdown. This is used to determine the ODT to be used (synchronous/asynchronous)

0x00A8004C EBI1_CH0_DDR_CMD_EXEC_OPT_4

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Command Execution Optimization Register 4.

This register has the programmable idle timer for entering powerdown.

EBI1_CH0_DDR_CMD_EXEC_OPT_4

Bits	Name	Description
31:24	PWR_DOWN_IDLE_TIMER	SW: RW, HW: R Count idle ddr1x cycles before entering powerdown/clockstop/clostop-powerdown. This is only valid if powerdown/clockstop/clockstop-powerdown is enabled via the DDR_CMD_EXEC_OPT_0 CSR. A value of 0 indicates that the powerdown/clockstop/clockstop-powerdown will be entered immediately when idle. 0x0: Disable (default)
23:0	RESERVED_23_0	

0x00A80050 EBI1_CH0_DDR_SM_TIMING_0

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00001000

DDR State Machine Timing Register 0

The fields in this register control the behavior of the Column State Machine.

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EBI1_CH0_DDR_SM_TIMING_0

Bits	Name	Description
31:15	RESERVED_31_15	

EBI1_CH0_DDR_SM_TIMING_0 (cont.)

Bits	Name	Description
14:12	DLY_RD_DIFF_RANK	SW: RW, HW: R Delays read to read when going to different ranks. For LPDDR1/2 devices (or PCDDR2/3 with ODT disabled), this can be set to MAX(1, RU((tHZ(DQ)max - tLZ(DQ)min)/tck) for optimal setting as these devices do not have ODT. tck here represents the time period for the fastest DDR1x clock frequency which will be used. The optimal value of this CSR is 4 cycles for PCDDR2/3, if Read Rank ODT (i.e DDR_CMD_EXEC_OPT_3[RANK0/1_ODT_ON_RD_RANK0/1]) is enabled. This accounts for the difference in the ODT off max and min timing, the requirement that Rtt needs to be off half cycle before read preamble, etc. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles
11	RD_INT_BY_RD	SW: RW, HW: R Indicates whether Read Interrupt by Read is allowed. This field needs to be set depending on the specific SDRAM device present. Use "Allowed" for LPDDR1/2 and PCDDR2. Use "Not Allowed" for PCDDR3. 0x1: Allowed 0x0: Not Allowed (default)
10	WR_INT_BY_WR	SW: RW, HW: R Indicates whether Write Interrupt by Write is allowed. This field needs to be set depending on the specific SDRAM device present. Use "Allowed" for LPDDR1/2 and PCDDR2. Use "Not Allowed" for PCDDR3. 0x1: Allowed 0x0: Not Allowed (default)
9	RD_INT_BY_BST	SW: RW, HW: R Indicates whether Read Interrupt by Burst Terminate is allowed. This field needs to be set depending on the specific SDRAM device present. Use "Allowed" for LPDDR1/2. Use "Not Allowed" for PCDDR2/3. 0x1: Allowed 0x0: Not Allowed (default)
8	WR_INT_BY_BST	SW: RW, HW: R Indicates whether Write Interrupt by Burst Terminate is allowed. This field needs to be set depending on the specific SDRAM device present. Use "Allowed" for LPDDR2. Use "Not Allowed" for LPDDR1 and PCDDR2/3. 0x1: Allowed 0x0: Not Allowed (default)

EBI1_CH0_DDR_SM_TIMING_0 (cont.)

Bits	Name	Description
7:6	WR_INT_RD_OR_PRECHG_MODE	SW: RW, HW: R Indicates the interruption mode to be allowed for write transactions when followed by Precharge or Reads.This field needs to be set depending on the specific SDRAM device present. Use "Interrupt with no delay" for LPDDR1 devices. Use "Non Interrupting" for PCDDR2/3 and LPDDR2-S2/S4. This basically sets the starting point for twr and twtr timers. 0x0: Int with no dly (default) 0x1: Int with single cc dly (Not Supported) 0x2: Non Interrupting 0x3: Reserved
5:4	RESERVED_5_4	
3:2	INT_BOUNDARY	SW: RW, HW: R Determines when the interrupting/concatenating command can be issued. This field needs to be set depending on the specific SDRAM device present. Use "Every Cycle" for LPDDR1 and LPDDR2-S2 devices. Use "Every 2 cycles" for LPDDR2-S4 and PCDDR2 devices. For PCDDR3 devices, the above fields would indicate that interruption is not allowed. Hence the value used here is not relevant. 0x0: Every Cycle (default) 0x1: Every 2 cycles 0x2: RESERVED_1 0x3: RESERVED_2
1:0	RESERVED_1_0	

0x00A80054 EBI1_CH0_DDR_SM_TIMING_1

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000004

DDR State Machine Timing Register 1

This register is used to control the behavior of the Column state machine.

EBI1_CH0_DDR_SM_TIMING_1

Bits	Name	Description
31:24	RESERVED_31_24	

EBI1_CH0_DDR_SM_TIMING_1 (cont.)

Bits	Name	Description
23:20	MEM_START_BURST_RD	SW: RW, HW: R Specifies the starting column address restrictions. This field needs to be set depending on the specific SDRAM device. Note that "interleaved" mode of addressing at the SDRAM device is not being supported. For LPDDR1/2 (all burst lengthis) and PCDDR2 (memory BL of 4) use "0000". For PCDDR3 (memory BL of 8) & PCDDR2 (memory BL of 8) use "0011". For PCDDR3 OTF burst mode, this field is a don't care. Others: Reserved 0x0: Address_0_2_4_6_etc (default) 0x3: Address_0_4_etc 0xF: Address_0_only
19:16	MEM_START_BURST_WR	SW: RW, HW: R Specifies the starting column address restrictions. This field needs to be set depending on the specific SDRAM device. Note that "interleaved" mode of addressing at the SDRAM device is not being supported. For LPDDR1/2 (all burst lengthis) and PCDDR2 (memory BL of 4) use "0000". For PCDDR2 (memory BL of 8) use "0011" and for PCDDR3 (memory BL of 8) use "1111". For PCDDR3 OTF burst mode, this field is a don't care. Others: Reserved 0x0: Address_0_2_4_6_etc (default) 0x3: Address_0_4_etc 0xF: Address_0_only
15:14	SYS_TIMING_MODE	SW: RW, HW: R Specifies the command interface timing relative to the chip select. This is necessary to provide an option to guarantee an additional cycle for the more heavily command interface signals to propagate to the RAMs and settle (to meet input setup requirements) before being clocked in. This is not applicable for LPDDR2. 0x0: 1T (default: Address and command can be driven in the same cycle as the chip select.) 0x1: 2T (Address and command must be driven at least 1 cycle before chip select is asserted) 0x2: RESERVED_1 0x3: RESERVED_2
13:8	RESERVED_13_8	
7	USE_ORIG_BL	SW: RW, HW: R Indicates if original or effective burst length should be used when computing timing between column commands. This field needs to be set depending on the specific SDRAM device. For LPDDR1/2, use "effective" and for PCDDR2/3, use "original". 0x1: Original 0x0: Effective (default)
6	RESERVED_6	

EBI1_CH0_DDR_SM_TIMING_1 (cont.)

Bits	Name	Description
5	ON_THE_FLY_MODE	SW: RW, HW: R Indicates that the memory burst mode selected is OTF (on-the-fly) mode. This field is only applicable for PCDDR3 SDRAM devices. 0x1: Allowed 0x0: Not Allowed (default)
4	DRIVE_WR_DQS_EARLY	SW: RW, HW: R Indicates if DQS needs to be toggled a cycle before the write data gets driven. This means that the first piece of write data will be driven on the 2nd rising edge of the Data strobe. This field needs to be set depending on the specific SDRAM device present. This is only "enabled" for PCDDR3 devices. 0x1: Enabled 0x0: Disabled (default)
3:0	BURST_LENGTH	SW: RW, HW: R Specified as Memory Burst Length. This must be in sync with the value programmed in SDRAM's mode register. For PCDDR3, memory BL of 8 ("0100" setting) and On-the-fly (OTF) mode are supported. For PCDDR3 OTF mode program CSR - DDR_SM_TIMING_1[ON_THE_FLY_MODE]. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: BL of 4 0x3: RESERVED_3 0x4: BL of 8 (default) 0x5: RESERVED_4 0x6: RESERVED_5 0x7: RESERVED_6 0x8: BL of 16 0x9: RESERVED_7 0xA: RESERVED_8 0xB: RESERVED_9 0xC: RESERVED_10 0xD: RESERVED_11 0xE: RESERVED_12 0xF: RESERVED_13

0x00A80058 EBI1_CH0_DDR_DRAM_TIMING_0

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x44301003

DDR DRAM Timing Register 0

This register contains parameters which are specified by the memory vendor in ns. The alternate register is DDR_DRAM_TIMING_0_ALT

This register holds the SDRAM timing parameters. The value of the settings is in clock cycles and may vary from one SDRAM vendor to another. The value that should be selected for each field is:

the number_of_clock_cycles of the vendor's specified value.

An example:

When the vendor's specification states tRCD = 44nS and the SDRAM clock rate = 166 MHz, the calculations are:

1. 1/166 MHz = 6nS.
2. 44nS/6nS = 7.33 clocks.
3. 7.33 clocks rounds up to 8 clocks.

Therefore, the value of RASmin_timer should be written as 4'b1000.

EBI1_CH0_DDR_DRAM_TIMING_0

Bits	Name	Description
31:29	TRTP	SW: RW, HW: R This is not the same as the memory timing parameter tRTP. Number of Additional clock cycles between a Read and a Precharge command to the same page with actual BL/2 as the initial base delay. This needs to be set depending on the memory device present. For LPDDR, this needs to be set to at least 2 cycles. For LPDDR2-S2, use MAX(2, "tRTP (memory timing parameter in ddr1x clock cycles) -1") For LPDDR2-S4, use MAX(2, "tRTP (memory timing parameter in clock cycles) -2") For PCDDR2, use MAX(2, "tRTP (memory timing parameter in clock cycles) -2") For PCDDR3, use MAX(2, "tRTP (memory timing parameter in clock cycles) -4") 0x0: RESERVED_1 0x1: RESERVED_2 0x2: Additional 2 clock cycles (default) 0x3: Additional 3 clock cycles 0x4: Additional 4 clock cycles 0x5: Additional 5 clock cycles 0x6: Additional 6 clock cycles 0x7: Additional 7 clock cycles

EBI1_CH0_DDR_DRAM_TIMING_0 (cont.)

Bits	Name	Description
28:24	TFAW	SW: RW, HW: R Programmable rolling window during which the number of activations should not exceed the CSR field - max_num_activations_tFAW. This needs to be set based on the specific SDRAM device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: RESERVED_4 0x4: MIN_CC (4 cycles default)
23:20	TRCD	SW: RW, HW: R Number of clock cycles from activate to column command (same bank). This needs to be set based on the specific SDRAM device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)
19:16	RESERVED_19_16	
15:12	TRRD	SW: RW, HW: R Number of clock cycles between Activate to Activate (different banks on same chip select). This needs to be set based on the specific SDRAM device. 0x0: RESERVED 0x1: MIN_CC (1 cycle default)
11:9	PWR_DOWN_ODT_OFF_MAX_MIN_DIFF	SW: RW, HW: R Number of clock cycles specifying the difference in the power down ODT off max/min timing parameter. For PCDDR2 & PCDDR3, this is rounded up version in ddr1x clock cycles of (tAOFPDmax - tAOFPDmin).
8:7	RESERVED_8_7	
6:5	TZQCL_MSB	SW: RW, HW: R The complete value of tZQCL timer is {tZQCL_MSB, tZQCL}. tZQCL is from DDR_DRAM_TIMING_7 CSR. Number of ddr1x clock cycles required for the long calibration sequence to execute. ZQ Calibration commands are only supported by LPDDR2 and PCDDR3 devices. For LPDDR2, this is the timing parametet - tZQCL and for PCDDR3, this is the timing parameter tZQoper.
4:0	TRAS_MIN	SW: W, HW: R Number of clocks cycles between Active and Precharge (same bank). This needs to be set based on the specific SDRAM device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)

0x00A8005C EBI1_CH0_DDR_DRAM_TIMING_1

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x000FF000

DDR Timing Parameters Register 1.

EBI1_CH0_DDR_DRAM_TIMING_1

Bits	Name	Description
31:30	RESERVED_31_30	
29	INCL_DARF_MAX_NUM_ACT_RANK1	SW: RW, HW: R NOT SUPPORTED. If set, then a DARF command is included in the maximum number of activations for tFAW window. This needs to be set based on the specific SDRAM device. For LPDDR2 devices with 8-banks, this field needs to be set to 1. For other devices, this field is set to 0. 0x0: Do not include (default) 0x1: Include
28	INCL_DARF_MAX_NUM_ACT_RANK0	SW: RW, HW: R NOT SUPPORTED. If set, then a DARF command is included in the maximum number of activations for tFAW window. This needs to be set based on the specific SDRAM device. For LPDDR2 devices with 8-banks, this field needs to be set to 1. For other devices, this field is set to 0. 0x0: Do not include (default) 0x1: Include
27:20	RESERVED_27_20	
19:16	MAX_NUM_ACT_RANK1	SW: RW, HW: R This indicates the maximum number of activations allowed in the TFAW rolling window. This needs to be set based on the specific SDRAM device. For LPDDR1 devices, LPDDR2 devices (with 4 banks) & PCDDR2 devices (with 4 banks), leave this as POR. For others (PCDDR3, LPDDR2 (8 bank devices) & PCDDR2 (8 bank devices)), the optimal value is "0100". 0xF: 15 (default)
15:12	MAX_NUM_ACT_RANK0	SW: RW, HW: R This indicates the maximum number of activations allowed in the TFAW rolling window. This needs to be set based on the specific SDRAM device. For LPDDR1 devices, LPDDR2 devices (with 4 banks) & PCDDR2 devices (with 4 banks), leave this as POR. For others (PCDDR3, LPDDR2 (8 bank devices) & PCDDR2 (8 bank devices)), the optimal value is "0100". 0xF: 15 (default)

EBI1_CH0_DDR_DRAM_TIMING_1 (cont.)

Bits	Name	Description
11:8	MAX_NUM_REFRESHES_TREFBW	SW: RW, HW: R This indicates the maximum number of refreshes allowed in the TREFBW rolling window. This applies to LPDDR2 as a means to limit the maximum current consumption. Typically, for LPDDR2, upto 8 all-bank refreshes are permitted in the tREFBW rolling window. For non-LPDDR2 devices, this field should be disabled. 0x0: Disabled (default) 0x1: RESERVED_1 0x2: RESERVED_2 0x3: 3 refreshes 0x4: 4 refreshes 0x5: 5 refreshes 0x6: 6 refreshes 0x7: 7 refreshes 0x8: 8 refreshes 0x9: RESERVED_3 0xA: RESERVED_4 0xB: RESERVED_5 0xC: RESERVED_6 0xD: RESERVED_7 0xE: RESERVED_8 0xF: RESERVED_9
7	RESERVED_7	
6:4	TMRD_READS	SW: RW, HW: R Number of clocks from Mode register set (read) to next valid command. This needs to be set based on the specific SDRAM device. Please note that the acutal tmrd_read observed will be several cycles beyond the programmed value (implementation detail)
3	RESERVED_3	
2:0	TMRD_WRITES	SW: RW, HW: R Number of clocks from Mode register set (write) to next valid command. This needs to be set based on the specific SDRAM device. Please note that the acutal tmrd_write observed will be several cycles beyond the programmed value (implementation detail)

0x00A80060 EBI1_CH0_DDR_DRAM_TIMING_2

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0xD2080220

DDR Timing Parameters Register 2.

EBI1_CH0_DDR_DRAM_TIMING_2

Bits	Name	Description
31:21	TRAS_MAX	SW: RW, HW: R tRASmax timer. The number of XO clock cycles before the page is closed. This needs to be loaded with the Trasmax value specified by the vendor minus 70 ddr1x clock cycles minus 6 tcxo clock cycles minus DDR_DRAM_TIMING_7[tZQCL] (if ZQCAL is used) ddr1x clock cycles.. The ddr1x clock period used for computing the offset needs to be based on the minimum ddr1x clock frequency used, especially in cases wherein the ddr1x clock frequency is changed. Note that this value is specified as number of tcxo clock cycles & hence the above needs to be computed in absolute time and then divided by the XO clock period.
20:18	TCKE	SW: RW, HW: R Minimum CKE pulse (low or high) width. This needs to be set based on the specific SDRAM device present. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
17:15	RESERVED_17_15	Reserved
14:12	WR_TO_RD_DLY_DIFF_RANK	SW: RW, HW: R Additional sync time when crossing ranks. For PCDDR2/3, if the other rank write ODT is enabled (i.e DDR_CMD_EXEC_OPT_3[RANK0_ODT_ON_WR_RANK1] or DDR_CMD_EXEC_OPT_3[RANK1_ODT_ON_WR_RANK0]) then, the value programmed must be at least 3 cycles. This is to account for the difference in the ODT off max and min timing, the requirement that Rtt needs to be off half cycle before read preamable, etc. 0x0: 0 Cycles (default) 0x1: 1 Cycle 0x2: 2 Cycles 0x3: 3 Cycles 0x4: 4 Cycles 0x5: 5 Cycles 0x6: 6 Cycles 0x7: 7 Cycles
11	RESERVED_11	Reserved\
10:8	TRTW_SAME_RANK	SW: RW, HW: R 0x0: 0 Cycles 0x1: 1 Cycle 0x2: 2 Cycles (default) 0x3: 3 Cycles 0x4: 4 Cycles 0x5: 5 Cycles 0x6: 6 Cycles 0x7: 7 Cycles

EBI1_CH0_DDR_DRAM_TIMING_2 (cont.)

Bits	Name	Description
7	RESERVED_7	Reserved\
6:4	TRTW_DIFF_RANK	SW: RW, HW: R 0x0: RESERVED_1 0x1: RESERVED_2 0x2: 2 Cycles (default) 0x3: 3 Cycles 0x4: 4 Cycles 0x5: 5 Cycles 0x6: 6 Cycles 0x7: 7 Cycles
3	RESERVED_3	Reserved
2:0	TOST	SW: RW, HW: R ODT Switching time when crossing ranks for write column commands. For LPDDR1/2 devices, (or PCDDR2/3 with ODT disabled) this can be set to "000" for optimal settings as these devices do not have ODT. The optimal value of this CSR is 2 cycles for PCDDR2/3, if write rank ODT (DDR_CMD_EXEC_OPT_3[RANK0/1_ODT_ON_WR_RANK0/1]) is enabled. 0x0: 0 Cycles (default) 0x1: 1 Cycle 0x2: 2 Cycles 0x3: 3 Cycles 0x4: 4 Cycles 0x5: 5 Cycles 0x6: 6 Cycles 0x7: 7 Cycles

0x00A80064 EBI1_CH0_DDR_DRAM_TIMING_3

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x01000603

DDR Timing Parameters Register 3

This register contains parameters which are specified by the memory vendor in ns. The alternalte/shadow register is DDR_DRAM_TIMING_3_ALT and is used during HW frequency switching.

EBI1_CH0_DDR_DRAM_TIMING_3

Bits	Name	Description
31:28	PD_EXIT_DURATION_ODT	SW: RW, HW: R This specifies the amount of time after a powerdown exit (which qualifies as asynchronous ODT for PCDDR2/3 devices) for which the column commands will be blocked to avoid large ODT on/off timing ranges. For PCDDR3 devices, this needs to be programmed to the timing parameter tXPDLL delay in ddr1x clock cycles. For PCDDR2 devices, this needs to be programmed to the timing parameter tAXPD delay in ddr1x clock cycles. For LPDDR1/2 devices, leave this field as POR value. The MSB value of this timer is PD_EXIT_DURATION_ODT_MSB.
27:24	TWTR	SW: RW, HW: R tWTR delay in clock cycles. 0x1: 1Cycle (default)
23	PD_EXIT_DURATION_ODT_MSB	SW: RW, HW: R The MSB bit for PD_EXIT_DURATION_ODT. This is required for PCDDR3 at higher frequencies.
22:19	TWR	SW: RW, HW: R Number of clocks from last data word to precharge
18:9	TXSRD	SW: RW, HW: R Number of clock cycles between self refresh exit and next valid Read command. The value is based on the specific SDRAM device present. For PCDDR3, this needs to be programmed with tXSDLL timing parameter. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)
8	RESERVED_8	Reserved
7:0	TXSNR	SW: RW, HW: R Number of clock cycles between self refresh exit and next valid Non-Read command. The value is based on the specific SDRAM device present. For LPDDR1/2 devices, the value programmed in TXSNR should be the same as in TXSRD. The different parameters are required for SDRAM devices with DLL's - PCDDR2/3. For PCDDR3, this needs to be programmed with tXS timing parameter. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)

0x00A80068 EBI1_CH0_DDR_DRAM_TIMING_4

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x02022220

DDR Timing Parameters Register 4

This register contains parameters which are specified by the memory vendor in ns. The alternalte/shadow register is DDR_DRAM_TIMING_4_ALT and is used during HW frequency switch.

EBI1_CH0_DDR_DRAM_TIMING_4

Bits	Name	Description
31:24	TRFC	SW: RW, HW: R Number of clock cycles between auto-refresh command and the next activate command. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
23:20	TMOD	SW: RW, HW: R Specifies the timing parameter TMOD in ddr1x clock cycles for PCDDR2/3 devices.
19:16	TXPNR_ACT_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next valid non-read command. This value gets used only if the Power down state was active power down. This distinction is required for PCDDR devices where in a slow/fast exit option in the Mode Register could potentially mean different timers for read commands (which require a DLL) Vs. a non-read command. For PCDDR2, program this to "tXPNR" if available, else set to "tXP". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. For LPDDR1/2 program this to "tXPNR" if available, else set to "tXP". For PCDDR3, set this to "tXP". 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)

EBI1_CH0_DDR_DRAM_TIMING_4 (cont.)

Bits	Name	Description
15:12	TXPR_ACT_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next read command. This value gets used only if the Power down state was active power down. For PCDDR2, if Mode register for "Active Power Down Exit Time" is programmed to "fast exit", set this to memory timing parameter "tXARD", else program this to "tXARDS". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. For LPDDR1/2, program this to "tXPR" if available, else set to "tXP". For PCDDR3, set this to "tXP". 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
11:8	TXPNR_PCHG_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next non-read command. This value gets used only if the Power down state was precharge power down. For PCDDR3, if ODT is enabled and the Mode register for "DLL control for Precharge PD" is programmed to "fast exit", set this to memory timing parameter "tXPDLL", else program this to "tXP". For LPDDR1/2 & PCDDR2, program this to "tXPNR" if available, else set to "tXP". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. The MSB bit for this is from TXPNR_PCHG_PWR_DOWN_MSB. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
7:4	TXPR_PCHG_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next read command. This value gets used only if the Power down state was precharge power down. For PCDDR3, if Mode register for "DLL control for Precharge PD" is programmed to "fast exit", set this to memory timing parameter "tXP", else program this to "tXPDLL". For LPDDR1/2 & PCDDR2, program this to "tXPNR" if available, else set to "tXP". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. The MSB bit for this is from TXPR_PCHG_PWR_DOWN_MSB. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
3:2	RESERVED_3_2	Reserved
1	TXPNR_PCHG_PWR_DOWN_MSB	SW: RW, HW: R The MSB bit for TXPNR_PCHG_PWR_DOWN. This is required for PCDDR3 at higher frequencies.
0	TXPR_PCHG_PWR_DOWN_MSB	SW: RW, HW: R The MSB bit for TXPR_PCHG_PWR_DOWN. This is required for PCDDR3 at higher frequencies.

0x00A8006C EBI1_CH0_DDR_DRAM_TIMING_5

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00003033

DDR Timing Parameters Register 5

This register contains parameters which are specified by the memory vendor in ns. The alternalte/shadow register is DDR_DRAM_TIMING_5_ALT and is used during HW frequency switch.

EBI1_CH0_DDR_DRAM_TIMING_5

Bits	Name	Description
31:24	SELF_RFSH_MIN_DURATION	SW: RW, HW: R This specifies the minimum number of ddr1x clock cycles the SDRAM device is required to remain in self refresh mode once a self refresh command is registered. For LPDDR1, this is specified as tRFC, for LPDDR2, this is specified as tCKESR, for PCDDR2/3, this is specified as tCKE. Based on current implementation, the design waits this CSR field plus DDR_DRAM_TIMING_5[CLK_RESTART_BEFORE_SELF_RFSH_EXIT] plus 2 ddr1x cycles at least before coming out of self refresh.
23	RESERVED_23	Reserved
22:20	CLK_STOP_AFTER_SELF_RFSH_ENTRY	SW: RW, HW: R This specifies the minimum number of ddr1x clock cycles after the Self Refresh command is registered that the external clock to the memory device needs to run before it can be turned off. For LPDDR1/2 and PCDDR2 SDRAM devices, this should be set to "1", for PCDDR3 SDRAM devices, this should be set to "tCKSRE"
19:16	CLK_RESTART_BEFORE_SELF_RFSH_EXIT	SW: RW, HW: R This specifies the minimum number of ddr1x clock cycles the memory clock is required to be stable/re-started before CKE can go high to indicate a self refresh exit. Based on the memory device alone, for LPDDR1, this is at least "1", for LPDDR2, this needs to be set to at least 2 clock cycles. For PCDDR2 SDRAM devices, this should be set to "1", for PCDDR3 SDRAM devices, this should be set to "tCKSRX". This CSR field represents the lower 4 bits. The upper 4 bits are in CLK_RESTART_BEFORE_SR_EXIT_UPPER CSR field below. If the cur_mode in the pads is enabled and the system is configured to dynamically turn off the cur_mode during self refresh, then the 8-bit timer needs to be programmed such that it provides at least 100ns of pad settling time.

EBI1_CH0_DDR_DRAM_TIMING_5 (cont.)

Bits	Name	Description
15:12	TRP_AB	SW: RW, HW: R Number of clocks from all bank precharge to Activate (same bank). This needs to be set based on the specific SDRAM device. For LPDDR1, PCDDR3 & 4-bank PCDDR2 devices, set this to timing parameter tRP. For 8-bank PCDDR2 devices, set this to tRP + 1*tck (in clock cycles). For LPDDR2 devices, set this to timing parameter tRPab. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)
11:8	CLK_RESTART_BEFORE_SR_EXIT_UPPER	SW: RW, HW: R These bits are the upper 4 bits for the CLK_RESTART_BEFORE_SELF_RFSH_EXIT CSR field above. The timer is 8 bits wide. If the cur_mode in the pads is enabled and the system is configured to dynamically turn off the cur_mode during self refresh, then the 8-bit timer needs to be programmed such that it provides at least 100ns of pad settling time.
7:4	TRP_PB	SW: RW, HW: R Number of clocks from per bank precharge to Activate (same bank). This needs to be set based on the specific SDRAM device. For LPDDR1, PCDDR3 & PCDDR2 devices, set this to timing parameter tRP. For LPDDR2 devices, set this to timing parameter tRPpb. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)

EBI1_CH0_DDR_DRAM_TIMING_5 (cont.)

Bits	Name	Description
3:0	RD_LATENCY	SW: RW, HW: R Actual Rd Latency (from Chip select assertion to the clock edge where read data is expected - This will not be exactly equal to CAS latency from memory specs) For LPDDR1, use Read latency of 3(fixed), for LPDDR2, use Read latency of memory device + RU(tdqsckmax/tck) (RU - round up) where tck is the time period of the current ddr1x clock frequency of operation. For PCDDR2/3 devices, use the read latency of the device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: 2 cycles 0x3: 3 cycles (default) 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

0x00A80070 EBI1_CH0_DDR_DRAM_TIMING_6

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x10102000

DDR Timing Parameters Register 6.

If DDR_CMD_EXEC_OPT_2[UPDATE_MEM_LATENCY_ON_FREQ_SWITCH] is set, then WR_LATENCY is a frequency dependent field.The alternate CSR field for WR_LATENCY below is DDR_UPDATE_FREQ_CHANGE_ALT[WR_LATENCY].

EBI1_CH0_DDR_DRAM_TIMING_6

Bits	Name	Description
31:28	WR_LATENCY	SW: RW, HW: R Actual Write Latency (from Chip select assertion to the clock edge where write data is driven - This will not be exactly equal to tWL latency from memory specs). For LPDDR1, use Write latency of 1 (fixed), for LPDDR2, use Write latency of device parameter tWL + 1. For PCDDR2/3 devices, use the write latency of the device. 0x0: RESERVED 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
27:24	RESERVED_27_24	Reserved
23:20	RESTART_CLK_PWR_DOWN_EXIT	SW: RW, HW: R Number of clock cycles required for the clock to be stable before the SDRAM device exits power-down mode. This only applies if the clock was stopped during power down. For LPDDR1/2, this needs to be set to at least 2 cycles. 0x0: RESERVED 0x1: MIN_CC (1 cycle default)
19	RESERVED_19	Reserved
18:16	STOP_CLK_PWR_DOWN_ENTRY	SW: RW, HW: R Number of clock cycles required for the clock to be stable after the SDRAM device enters power-down mode. For minimum memory timings, for LPDDR1, this can be set to "000" or higher; for LPDDR2-S2/S4, this can be set to "001" or higher. 0x7: RESERVED
15:14	RESERVED_15_14	Reserved

EBI1_CH0_DDR_DRAM_TIMING_6 (cont.)

Bits	Name	Description
13:12	TSRR	SW: RW, HW: R Number of clock cycles between MRS for SRR and Read command. SRR is an LPDDR1 feature only. 0x0: 0 Cycles 0x1: 1 Cycle 0x2: 2 Cycles (default) 0x3: 3 Cycles
11:0	RESERVED_11_0	Reserved

0x00A80074 EBI1_CH0_DDR_DRAM_TIMING_7

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00011212

DDR Timing Parameters Register 7

This register contains parameters which are specified by the memory vendor in ns. The alternalte/shadow register is DDR_DRAM_TIMING_7_ALT and gets used during HW frequency switch.

EBI1_CH0_DDR_DRAM_TIMING_7

Bits	Name	Description
31:24	TZQCL	SW: RW, HW: R The complete value of tZQCL timer is {tZQCL_MSB, tZQCL}. tZQCL_MSB is from DDR_DRAM_TIMING_0 CSR. Number of ddr1x clock cycles required for the long calibration sequence to execute. ZQ Calibration commands are only supported by LPDDR2 and PCDDR3 devices. For LPDDR2, this is the timing parametet - tZQCL and for PCDDR3, this is the timing parameter tZQoper.
23:17	TZQCS	SW: RW, HW: R Number of ddr1x clock cycles required for the short calibration sequence to execute. ZQ Calibration commands are only supported by LPDDR2 and PCDDR3 devices. For LPDDR2, this is the timing parametet - tZQCS and for PCDDR3, this is the timing parameter tZQCS.
16	PAD_LOW_POWER_MODE	SW: RW, HW: R SW needs to indicate the power mode based on the frequency of operation. 0x0: Low Power Mode 0x1: High Power Mode (default)

EBI1_CH0_DDR_DRAM_TIMING_7 (cont.)

Bits	Name	Description
15:12	DLY_RD_CAPTURE	SW: RW, HW: R Enables the read capture window n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
11:8	EXT_RD_CAPTURE	SW: RW, HW: R Extends the read capture window to account for board delays for getting read data from memory. For simulation, this needs to be set to at least 2 + DDR_IO_STAGE (design parameter) pipleline delay. 0x0: 0 cycles 0x1: 1 cycle 0x2: 2 cycles (default) 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

EBI1_CH0_DDR_DRAM_TIMING_7 (cont.)

Bits	Name	Description
7:4	DLY_IE_START	SW: RW, HW: R Enables the DQ/DQS pad input enable window n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
3:0	EXT_IE_WINDOW	SW: RW, HW: R Extends the DQS/DQ pad input enable window to account for board delays for getting read data from memory. For simulation, this needs to be set to at least 1 cycle. 0x0: 0 cycles 0x1: 1 cycle 0x2: 2 cycles (default) 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

0x00A80078 EBI1_CH0_DDR_DRAM_TIMING_8

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x01010101

DDR Timing Parameters Register 8

The alternalte/shadow register is DDR_DRAM_TIMING_8_ALT and gets used during HW frequency switch. This CSR has the start delay and the config delay controls for the external RCW (Read Capture Window) used for DQS qualification window generation in the PHY.

EBI1_CH0_DDR_DRAM_TIMING_8

Bits	Name	Description
31:30	RESERVED_31_30	Reserved
29:28	RCW_CFG_COARSE_DLY_DATA_BYTE3	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle
27:24	RCW_START_DLY_BYTE3	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
23:22	RESERVED_23_22	Reserved
21:20	RCW_CFG_COARSE_DLY_DATA_BYTE2	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH0_DDR_DRAM_TIMING_8 (cont.)

Bits	Name	Description
19:16	RCW_START_DLY_BYTE2	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
15:14	RESERVED_15_14	Reserved
13:12	RCW_CFG_COARSE_DLY_DATA_BYTE1	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH0_DDR_DRAM_TIMING_8 (cont.)

Bits	Name	Description
11:8	RCW_START_DLY_BYTE1	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
7:6	RESERVED_7_6	Reserved
5:4	RCW_CFG_COARSE_DLY_DATA_BYTE0	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH0_DDR_DRAM_TIMING_8 (cont.)

Bits	Name	Description
3:0	RCW_START_DLY_BYTE0	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

0x00A8007C EBI1_CH0_DDR_DRAM_TIMING_9

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Timing Parameters Register 9

The alternalte/shadow register is DDR_DRAM_TIMING_9_ALT and gets used during HW frequency switch. This CSR has the start delay and the config delay controls for the external RCW (Read Capture Window) used for DQS qualification window generation in the PHY.

EBI1_CH0_DDR_DRAM_TIMING_9

Bits	Name	Description
31:24	RCW_CFG_FINE_DLY_DATA_BYTE3	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.
23:16	RCW_CFG_FINE_DLY_DATA_BYTE2	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.

EBI1_CH0_DDR_DRAM_TIMING_9 (cont.)

Bits	Name	Description
15:8	RCW_CFG_FINE_DLY_DATA_BYTE1	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.
7:0	RCW_CFG_FINE_DLY_DATA_BYTE0	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.

0x00A80080 EBI1_CH0_DDR_DRAM_TIMING_0_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x44301003

DDR DRAM Timing Register 0_ALT

This register contains parameters which are specified by the memory vendor in ns. The alternalte/shadow register is DDR_DRAM_TIMING_0 and gets used during HW frequency switch.

This register holds the SDRAM timing parameters. The value of the settings is in clock cycles and may vary from one SDRAM vendor to another. The value that should be selected for each field is:

the number_of_clock_cycles of the vendor's specified value.

An example:

When the vendor's specification states tRCD = 44nS and the SDRAM clock rate = 166 MHz, the calculations are:

1. 1/166 MHz = 6nS.
2. 44nS/6nS = 7.33 clocks.
3. 7.33 clocks rounds up to 8 clocks.

Therefore, the value of RASmin_timer should be written as 4'b1000.

EBI1_CH0_DDR_DRAM_TIMING_0_ALT

Bits	Name	Description
31:29	TRTP	SW: RW, HW: R This is not the same as the memory timing parameter tRTP. Number of Additional clock cycles between a Read and a Precharge command to the same page with actual BL/2 as the intial base delay. This needs to be set depending on the memory device present. For LPDDR, this needs to be set to at least 2 cycles. For LPDDR2-S2, use MAX(2, "tRTP (memory timing parameter in ddr1x clock cycles) -1") For LPDDR2-S4, use MAX(2, "tRTP (memory timing parameter in clock cycles) -2") For PCDDR2, use MAX(2, "tRTP (memory timing parameter in clock cycles) -2") For PCDDR3, use MAX(2, "tRTP (memory timing parameter in clock cycles) -4") 0x0: RESERVED_1 0x1: RESERVED_2 0x2: Additional 2 clock cycles (default) 0x3: Additional 3 clock cycles 0x4: Additional 4 clock cycles 0x5: Additional 5 clock cycles 0x6: Additional 6 clock cycles 0x7: Additional 7 clock cycles
28:24	TFAW	SW: RW, HW: R Programmable rolling window during which the number of activations should not exceed the CSR field - max_num_activations_tFAW. This needs to be set based on the specific SDRAM device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: RESERVED_4 0x4: MIN_CC (4 cycles default)
23:20	TRCD	SW: RW, HW: R Number of clock cycles from activate to column command (same bank). This needs to be set based on the specific SDRAM device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)
19:16	RESERVED_19_16	

EBI1_CH0_DDR_DRAM_TIMING_0_ALT (cont.)

Bits	Name	Description
15:12	TRRD	SW: RW, HW: R Number of clock cycles between Activate to Activate (different banks on same chip select). This needs to be set based on the specific SDRAM device. 0x0: RESERVED 0x1: MIN_CC (1 cycle default)
11:9	PWR_DOWN_ODT_OFF_MAX_MIN_DIFF	SW: RW, HW: R Number of clock cycles specifying the difference in the power down ODT off max/min timing parameter. For PCDDR2 & PCDDR3, this is rounded up version in ddr1x clock cycles of (tAOFPDmax - tAOFPDmin).
8:7	RESERVED_8_7	
6:5	TZQCL_MSB	SW: RW, HW: R The complete value of tZQCL timer is {tZQCL_MSB, tZQCL}. tZQCL is from DDR_DRAM_TIMING_7 CSR. Number of ddr1x clock cycles required for the long calibration sequence to execute. ZQ Calibration commands are only supported by LPDDR2 and PCDDR3 devices. For LPDDR2, this is the timing parametet - tZQCL and for PCDDR3, this is the timing parameter tZQoper.
4:0	TRAS_MIN	SW: W, HW: R Number of clocks cycles between Active and Precharge (same bank). This needs to be set based on the specific SDRAM device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)

0x00A80084 EBI1_CH0_DDR_DRAM_TIMING_3_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x01000603

DDR Timing Parameters Register 3_ALT

This register contains parameters which are specified by the memory vendor in ns. The alternalte/shadow register is DDR_DRAM_TIMING_3 and gets used during HW frequency switch.

EBI1_CH0_DDR_DRAM_TIMING_3_ALT

Bits	Name	Description
31:28	PD_EXIT_DURATION_ODT	SW: RW, HW: R This specifies the amount of time after a powerdown exit (which qualifies as asynchronous ODT for PCDDR2/3 devices) for which the column commands will be blocked to avoid large ODT on/off timing ranges. For PCDDR3 devices, this needs to be programmed to the timing parameter tXPDLL delay in ddr1x clock cycles. For PCDDR2 devices, this needs to be programmed to the timing parameter tAXPD delay in ddr1x clock cycles. For LPDDR1/2 devices, leave this field as POR value. The MSB value of this timer is PD_EXIT_DURATION_ODT_MSB.
27:24	TWTR	SW: RW, HW: R tWTR delay in clock cycles. 0x1: 1Cycle (default)
23	PD_EXIT_DURATION_ODT_MSB	SW: RW, HW: R The MSB bit for PD_EXIT_DURATION_ODT. This is required for PCDDR3 at higher frequencies.
22:19	TWR	SW: RW, HW: R Number of clocks from last data word to precharge
18:9	TXSRD	SW: RW, HW: R Number of clock cycles between self refresh exit and next valid Read command. The value is based on the specific SDRAM device present. For PCDDR3, this needs to be programmed with tXSDLL timing parameter. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)
8	RESERVED_8	Reserved
7:0	TXSNR	SW: RW, HW: R Number of clock cycles between self refresh exit and next valid Non-Read command. The value is based on the specific SDRAM device present. For LPDDR1/2 devices, the value programmed in TXSNR should be the same as in TXSRD. The different parameters are required for SDRAM devices with DLL's - PCDDR2/3. For PCDDR3, this needs to be programmed with tXS timing parameter. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)

0x00A80088 EBI1_CH0_DDR_DRAM_TIMING_4_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x02022220

DDR Timing Parameters Register 4_ALT

This register contains parameters which are specified by the memory vendor in ns. The alternalte/shadow register is DDR_DRAM_TIMING_4 and gets used during HW frequency switch.

EBI1_CH0_DDR_DRAM_TIMING_4_ALT

Bits	Name	Description
31:24	TRFC	SW: RW, HW: R Number of clock cycles between auto-refresh command and the next activate command. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
23:20	TMOD	SW: RW, HW: R Specifies the timing parameter TMOD in ddr1x clock cycles for PCDDR2/3 devices.
19:16	TXPNR_ACT_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next valid non-read command. This value gets used only if the Power down state was active power down. This distinction is required for PCDDR devices where in a slow/fast exit option in the Mode Register could potentially mean different timers for read commands (which require a DLL) Vs. a non-read command. For PCDDR2, program this to "tXPNR" if available, else set to "tXP". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. For LPDDR1/2 program this to "tXPNR" if available, else set to "tXP". For PCDDR3, set this to "tXP". 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)

EBI1_CH0_DDR_DRAM_TIMING_4_ALT (cont.)

Bits	Name	Description
15:12	TXPR_ACT_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next read command. This value gets used only if the Power down state was active power down. For PCDDR2, if Mode register for "Active Power Down Exit Time" is programmed to "fast exit", set this to memory timing parameter "tXARD", else program this to "tXARDS". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. For LPDDR1/2, program this to "tXPR" if available, else set to "tXP". For PCDDR3, set this to "tXP". 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
11:8	TXPNR_PCHG_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next non-read command. This value gets used only if the Power down state was precharge power down. For PCDDR3, if ODT is enabled and the Mode register for "DLL control for Precharge PD" is programmed to "fast exit", set this to memory timing parameter "tXPDLL", else program this to "tXP". For LPDDR1/2 & PCDDR2, program this to "tXPNR" if available, else set to "tXP". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. The MSB bit for this is from TXPNR_PCHG_PWR_DOWN_MSB. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
7:4	TXPR_PCHG_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next read command. This value gets used only if the Power down state was precharge power down. For PCDDR3, if Mode register for "DLL control for Precharge PD" is programmed to "fast exit", set this to memory timing parameter "tXP", else program this to "tXPDLL". For LPDDR1/2 & PCDDR2, program this to "tXPNR" if available, else set to "tXP". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. The MSB bit for this is from TXPR_PCHG_PWR_DOWN_MSB. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
3:2	RESERVED_3_2	Reserved
1	TXPNR_PCHG_PWR_DOWN_MSB	SW: RW, HW: R The MSB bit for TXPNR_PCHG_PWR_DOWN. This is required for PCDDR3 at higher frequencies.
0	TXPR_PCHG_PWR_DOWN_MSB	SW: RW, HW: R The MSB bit for TXPR_PCHG_PWR_DOWN. This is required for PCDDR3 at higher frequencies.

0x00A8008C EBI1_CH0_DDR_DRAM_TIMING_5_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00003033

DDR Timing Parameters Register 5_ALT

This register contains parameters which are specified by the memory vendor in ns. The alternalte/shadow register is DDR_DRAM_TIMING_5 and gets used during HW frequency switch.

EBI1_CH0_DDR_DRAM_TIMING_5_ALT

Bits	Name	Description
31:24	SELF_RFSH_MIN_DURATION	SW: RW, HW: R This specifies the minimum number of ddr1x clock cycles the SDRAM device is required to remain in self refresh mode once a self refresh command is registered. For LPDDR1, this is specified as tRFC, for LPDDR2, this is specified as tCKESR, for PCDDR2/3, this is specified as tCKE. Based on current implementation, the design waits this CSR field plus DDR_DRAM_TIMING_5[CLK_RESTART_BEFORE_SELF_RFSH_EXIT] plus 2 ddr1x cycles at least before coming out of self refresh.
23	RESERVED_23	Reserved
22:20	CLK_STOP_AFTER_SELF_RFSH_ENTRY	SW: RW, HW: R This specifies the minimum number of ddr1x clock cycles after the Self Refresh command is registered that the external clock to the memory device needs to run before it can be turned off. For LPDDR1/2 and PCDDR2 SDRAM devices, this should be set to "1", for PCDDR3 SDRAM devices, this should be set to "tCKSRE"
19:16	CLK_RESTART_BEFORE_SELF_RFSH_EXIT	SW: RW, HW: R This specifies the minimum number of ddr1x clock cycles the memory clock is required to be stable/re-started before CKE can go high to indicate a self refresh exit. Based on the memory device alone, for LPDDR1, this is at least "1", for LPDDR2, this needs to be set to at least 2 clock cycles. For PCDDR2 SDRAM devices, this should be set to "1", for PCDDR3 SDRAM devices, this should be set to "tCKSRX". This CSR field represents the lower 4 bits. The upper 4 bits are in CLK_RESTART_BEFORE_SR_EXIT_UPPER CSR field below. If the cur_mode in the pads is enabled and the system is configured to dynamically turn off the cur_mode during self refresh, then the 8-bit timer needs to be programmed such that it provides at least 100ns of pad settling time.

EBI1_CH0_DDR_DRAM_TIMING_5_ALT (cont.)

Bits	Name	Description
15:12	TRP_AB	SW: RW, HW: R Number of clocks from all bank precharge to Activate (same bank). This needs to be set based on the specific SDRAM device. For LPDDR1, PCDDR3 & 4-bank PCDDR2 devices, set this to timing parameter tRP. For 8-bank PCDDR2 devices, set this to tRP + 1*tck (in clock cycles). For LPDDR2 devices, set this to timing parameter tRPab. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)
11:8	CLK_RESTART_BEFORE_SR_EXIT_UPPER	SW: RW, HW: R These bits are the upper 4 bits for the CLK_RESTART_BEFORE_SELF_RFSH_EXIT CSR field above. The timer is 8 bits wide. If the cur_mode in the pads is enabled and the system is configured to dynamically turn off the cur_mode during self refresh, then the 8-bit timer needs to be programmed such that it provides at least 100ns of pad settling time.
7:4	TRP_PB	SW: RW, HW: R Number of clocks from per bank precharge to Activate (same bank). This needs to be set based on the specific SDRAM device. For LPDDR1, PCDDR3 & PCDDR2 devices, set this to timing parameter tRP. For LPDDR2 devices, set this to timing parameter tRPpb. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)

EBI1_CH0_DDR_DRAM_TIMING_5_ALT (cont.)

Bits	Name	Description
3:0	RD_LATENCY	SW: RW, HW: R Actual Rd Latency (from Chip select assertion to the clock edge where read data is expected - This will not be exactly equal to CAS latency from memory specs) For LPDDR1, use Read latency of 3(fixed), for LPDDR2, use Read latency of memory device + RU(tdqsckmax/tck) (RU - round up) where tck is the time period of the current ddr1x clock frequency of operation. For PCDDR2/3 devices, use the read latency of the device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: 2 cycles 0x3: 3 cycles (default) 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

0x00A80090 EBI1_CH0_DDR_DRAM_TIMING_7_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00011212

DDR Timing Parameters Register 7_ALT

This register contains parameters which are specified by the memory vendor in ns. The alternalte/shadow register is DDR_DRAM_TIMING_7 and gets used during HW frequency switch.

EBI1_CH0_DDR_DRAM_TIMING_7_ALT

Bits	Name	Description
31:24	TZQCL	SW: RW, HW: R The complete value of tZQCL timer is {tZQCL_MSB, tZQCL}. tZQCL_MSB is from DDR_DRAM_TIMING_0_ALT CSR. Number of ddr1x clock cycles required for the long calibration sequence to execute. ZQ Calibration commands are only supported by LPDDR2 and PCDDR3 devices. For LPDDR2, this is the timing parametet - tZQCL and for PCDDR3, this is the timing parameter tZQoper.
23:17	TZQCS	SW: RW, HW: R Number of ddr1x clock cycles required for the short calibration sequence to execute. ZQ Calibration commands are only supported by LPDDR2 and PCDDR3 devices. For LPDDR2, this is the timing parametet - tZQCS and for PCDDR3, this is the timing parameter tZQCS.
16	PAD_LOW_POWER_MODE	SW: RW, HW: R SW needs to indicate the power mode based on the frequency of operation. 0x0: Low Power Mode 0x1: High Power Mode (default)
15:12	DLY_RD_CAPTURE	SW: RW, HW: R Enables the read capture window n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

EBI1_CH0_DDR_DRAM_TIMING_7_ALT (cont.)

Bits	Name	Description
11:8	EXT_RD_CAPTURE	SW: RW, HW: R Extends the read capture window to account for board delays for getting read data from memory. For simulation, this needs to be set to at least 2 + DDR_IO_STAGE (design parameter) pipleline delay. 0x0: 0 cycles 0x1: 1 cycle 0x2: 2 cycles (default) 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
7:4	DLY_IE_START	SW: RW, HW: R Enables the DQ/DQS pad input enable window n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

EBI1_CH0_DDR_DRAM_TIMING_7_ALT (cont.)

Bits	Name	Description
3:0	EXT_IE_WINDOW	SW: RW, HW: R Extends the DQS/DQ pad input enable window to account for board delays for getting read data from memory. For simulation, this needs to be set to at least 1 cycle. 0x0: 0 cycles 0x1: 1 cycle 0x2: 2 cycles (default) 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

0x00A80094 EBI1_CH0_DDR_DRAM_TIMING_8_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x01010101

DDR Timing Parameters Register 8_ALT

The alternate/shadow register is DDR_DRAM_TIMING_8 and gets used during HW frequency switch. This CSR has the start delay and the config delay controls for the external RCW (Read Capture Window) used for DQS qualification window generation in the PHY.

EBI1_CH0_DDR_DRAM_TIMING_8_ALT

Bits	Name	Description
31:30	RESERVED_31_30	Reserved
29:28	RCW_CFG_COARSE_DLY_DATA_BYTE3	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH0_DDR_DRAM_TIMING_8_ALT (cont.)

Bits	Name	Description
27:24	RCW_START_DLY_BYTE3	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
23:22	RESERVED_23_22	Reserved
21:20	RCW_CFG_COARSE_DLY_DATA_BYTE2	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH0_DDR_DRAM_TIMING_8_ALT (cont.)

Bits	Name	Description
19:16	RCW_START_DLY_BYTE2	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
15:14	RESERVED_15_14	Reserved
13:12	RCW_CFG_COARSE_DLY_DATA_BYTE1	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH0_DDR_DRAM_TIMING_8_ALT (cont.)

Bits	Name	Description
11:8	RCW_START_DLY_BYTE1	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
7:6	RESERVED_7_6	Reserved
5:4	RCW_CFG_COARSE_DLY_DATA_BYTE0	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH0_DDR_DRAM_TIMING_8_ALT (cont.)

Bits	Name	Description
3:0	RCW_START_DLY_BYTE0	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

0x00A80098 EBI1_CH0_DDR_DRAM_TIMING_9_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Timing Parameters Register 9_ALT

The alternate/shadow register is DDR_DRAM_TIMING_9 and gets used during HW frequency switch. This CSR has the start delay and the config delay controls for the external RCW (Read Capture Window) used for DQS qualification window generation in the PHY.

EBI1_CH0_DDR_DRAM_TIMING_9_ALT

Bits	Name	Description
31:24	RCW_CFG_FINE_DLY_DATA_BYTE3	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.
23:16	RCW_CFG_FINE_DLY_DATA_BYTE2	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.

EBI1_CH0_DDR_DRAM_TIMING_9_ALT (cont.)

Bits	Name	Description
15:8	RCW_CFG_FINE_DLY_DATA_BYTE1	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.
7:0	RCW_CFG_FINE_DLY_DATA_BYTE0	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.

0x00A8009C EBI1_CH0_DDR_UPDATE_FREQ_CHANGE_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x10000000

DDR Update Frequency Change ALT register.

This register contains parameters which are dependent on the frequency of operation. The fields in this register are valid only if DDR_CMD_EXEC_OPT_2[UPDATE_MEM_LATENCY_ON_FREQ_SWITCH] is set.

The original CSR field for WR_LATENCY below is DDR_DRAM_TIMING_6[WR_LATENCY].

The original CSR field for ODT_START_DELAY_RD/WR below is DDR_CMD_EXEC_OPT_3[ODT_START_DELAY_RD/WR].

The original CSR field for ODT_OFF_DELAY below is DDR_CMD_EXEC_OPT_3[ODT_OFF_DELAY].

The original CSR field for tANPD below is DDR_CMD_EXEC_OPT_3[tANPD].

EBI1_CH0_DDR_UPDATE_FREQ_CHANGE_ALT

Bits	Name	Description
31:28	WR_LATENCY	SW: RW, HW: R Actual Write Latency (from Chip select assertion to the clock edge where write data is driven - This will not be exactly equal to tWL latency from memory specs). For LPDDR1, use Write latency of 1 (fixed), for LPDDR2, use Write latency of device parameter tWL + 1. For PCDDR2/3 devices, use the write latency of the device. 0x0: RESERVED 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
27:22	RESERVED_27_22	Reserved
21:19	ODT_START_DELAY_WR	SW: RW, HW: R This delay only applies to the Rank ODT and not the controller ODT. Specifies the delay in ddr1x clock cycles between the DDR Write command and the ODT being driven high. Typically for PCDDR2 devices for writes, this should be set to (Write latency - tAOND) and for PCDDR3 devices for writes, this must be set to "1" for optimal settings. The above indicates the maximum value allowed for the ODT signal to be turned on/driven high w.r.t the write CAS command. Note that a value of "0" indicates that the ODT signal is turned on 1 cycle before the write CAS command. A value of "1" indicates that the ODT signal is turned on in the same cycle as the write CAS command and so on. The difference between the maximum value and the value programmed is required to be added as additional incremental delays to DDR_DRAM_TIMING_2[tOST], DDR_DRAM_TIMING_2[tRTW_SAME_RANK] and DDR_DRAM_TIMING_2[tRTW_DIFF_RANK] to avoid cases where in there is overlap among the different ODT signals. The values verified are MAX and MAX-1.

EBI1_CH0_DDR_UPDATE_FREQ_CHANGE_ALT (cont.)

Bits	Name	Description
18:16	ODT_START_DELAY_RD	SW: RW, HW: R This delay only applies to the Rank ODT and not the controller ODT. Specifies the delay in ddr1x clock cycles between the DDR Read command and the ODT being driven high. Typically for PCDDR2 devices for reads, this should be set to (Read latency - tAOND) and for PCDDR3 devices for reads, this must be set to (Read Latency - (Write Latency - 2)) for optimal settings. The above indicates the maximum value allowed for the ODT signal to be turned on/driven high w.r.t the read CAS command. Note that a value of "0" indicates that the ODT signal is turned on 1 cycle before the read CAS command. A value of "1" indicates that the ODT signal is turned on in the same cycle as the read CAS command and so on. The difference between the maximum value and the value programmed might need to be added as additional incremental delays to DDR_SM_TIMING_0[DLY_RD_DIFF_RANK], DDR_DRAM_TIMING_2[WR_TO_RD_DLY_DIFF_RANK] to avoid cases where in there is overlap among the different ODT signals. The values verified are MAX and MAX-1.
15:13	ODT_OFF_DELAY	SW: RW, HW: R This delay specifies the ODT off memory timing parameter for rank ODT. For PCDDR2, if DDR_CMD_EXEC_OPT_0[PWR_DOWN_EN] is 1'b0 then program this to the timing parameter, tAOFD. For PCDDR2, if DDR_CMD_EXEC_OPT_0[PWR_DOWN_EN] is 1'b1 then program this to MAX(tAOFD, tANPD). For PCDDR3, this is to be programmed to "Write Latency -2", which is ODTLoff.
12:4	RESERVED_12_4	Reserved
3:1	TANPD	SW: RW, HW: R This specifies the memory timing parameter tANPD in ddr1x clock cycles. For PCDDR2 devices, program this to the timing parameter tANPD, for PCDDR3 devices, this needs to be programmed to WL - 1 (as per PCDDR3 spec).
0	RESERVED_0	Reserved

0x00A800A0 EBI1_CH0_DDR_AUTO_RFSH_CNTL

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00001007

DDR Refresh Control Register.

This register configures the refresh operating mode of the DDR SDRAM controller.

EBI1_CH0_DDR_AUTO_RFSH_CNTL

Bits	Name	Description
31:28	RESERVED_31_28	
27:24	COUNT_RFSH_AHEAD	SW: RW, HW: R Number of refresh cycles ahead allowed. A value of '0' disables the refresh ahead mechanism. For all SDRAM devices, the max value allowed for Auto Refresh mode is 7. 0000: (default) 0x1: Ahead of 1 0x2: Ahead of 2 0x3: Ahead of 3 0x4: Ahead of 4 0x5: Ahead of 5 0x6: Ahead of 6 0x7: Ahead of 7 0x8: RESERVED_1 0x9: RESERVED_2 0xA: RESERVED_3 0xB: RESERVED_4 0xC: RESERVED_5 0xD: RESERVED_6 0xE: RESERVED_7 0xF: RESERVED_8
23	TEMP_ADJUST_RFSH	SW: RW, HW: R When used, sdTemp pin inputs automatically adjust the refresh rate. 0x0: ignore (default) 0x1: use
22:14	TREFI	SW: RW, HW: R Number of clock cycle delay (in tcxo clock cycles) between auto-refresh commands (when MODE_AUTO_RFSH is set to autoRef) or directed auto-refresh commands (when MODE_AUTO_RFSH is set to directedAutoRef). This is required to be set to the "desired tREFI" -1 tcxo cycles.
13:12	MODE_AUTO_RFSH	SW: RW, HW: R Specifies the refresh mode. For normal operation, this needs to be set to "01". 0x0: no refreshing 0x1: autoRef (default) 0x2: RESERVED_1 0x3: RESERVED_2
11:3	RESERVED_11_3	

EBI1_CH0_DDR_AUTO_RFSH_CNTL (cont.)

Bits	Name	Description
2:0	REFRESH_IDLE_ACROSS_RANKS	SW: RW, HW: R Number of clock cycles between auto-refresh commands across ranks. This is to avoid cases wherein the auto refreshes to 2 ranks occur concurrently/too close which might cause a current spike. 0x0: RESERVED 0x1: 1 cycle 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles (default)

0x00A800A8 EBI1_CH0_DDR_SELF_RFSH_CNTL

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000200

DDR SDRAM Self-Refresh Control Register

EBI1_CH0_DDR_SELF_RFSH_CNTL

Bits	Name	Description
31:28	RESERVED_31_28	Reserved
27	HW_SELF_RFSH_EN_RANK1	SW: RW, HW: R Enables HW to look for no activity for rank1 and trigger an idle timer specified based on the value of HW_SELF_RFSH_TIMER. If there is no activity still and the timer expires, the HW will initiate entry to self refresh mode. 0x0: Disabled (default) 0x1: Enabled
26	HW_SELF_RFSH_EN_RANK0	SW: RW, HW: R Enables HW to look for no activity for rank0 and trigger an idle timer specified based on the value of HW_SELF_RFSH_TIMER. If there is no activity still and the timer expires, the HW will initiate entry to self refresh mode. 0x0: Disabled (default) 0x1: Enabled
25:20	RESERVED_25_20	

EBI1_CH0_DDR_SELF_RFSH_CNTL (cont.)

Bits	Name	Description
19:8	HW_SELF_RFSH_TIMER	SW: RW, HW: R Count idle tcxo cycles before entering self refresh. The timer is based on XO clock frequency. Valid only when HW_SELF_RFSH_EN is set. 'h000: RESERVED 'h001: RESERVED 'h002: 2 cycles (default)
7:0	RESERVED_7_0	

0x00A800B0 EBI1_CH0_DDR_PMON_EVENT_CNTL0

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x3EF87BFF

DDR SDRAM Performance Monitor Event Control Register

EBI1_CH0_DDR_PMON_EVENT_CNTL0

Bits	Name	Description
31	RESERVED_31	
30	EVENTS_ENABLE	SW: RW, HW: R Global Event Enable bit
29:28	EVENT0_TRANS_MATCH	SW: RW, HW: R Counts the number of AXI Read or Write transactions or both. 0x0: Reserved 0x1: Read 0x2: Write 0x3: Read_or_Write (default)
27:25	EVENT0_PRIORITY_MATCH	SW: RW, HW: R Additional Match on priority value/range for Event0 0x0: Reserved 0x1: PVAL0 0x2: PVAL1 0x3: PVAL0_or_PVAL1 0x4: PVAL2 0x5: PVAL0_or_PVAL2 0x6: PVAL1_or_PVAL2 0x7: PVAL0_or_PVAL1_or_PVAL2 (default)

EBI1_CH0_DDR_PMON_EVENT_CNTL0 (cont.)

Bits	Name	Description
24	EVENT0_CMD_STARVED_MATCH	SW: RW, HW: R Additional Match on command starved for Event0. Note that command starvation is only applicable to read transactions 0x1: Match_Enable 0x0: Ignore (default)
23:21	EVENT0_PAGE_ATTR_MATCH	SW: RW, HW: R Additional Match on whether the transaction is a page hit or miss or conflict for Event0 0x0: Reserved 0x1: HIT 0x2: MISS 0x3: HIT_or_MISS 0x4: CONFLICT 0x5: HIT_or_CONFLICT 0x6: MISS_or_CONFLICT 0x7: HIT_or_MISS_or_CONFLICT (default)
20:19	EVENT0_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event0 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
18:11	EVENT0_BANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to which bank(s) for Event0 Others: Similar decode for all 8 banks 0x0: Reserved 0x1: Bank0 0x2: Bank1 0x3: Bank0_or_Bank1 0x4: Bank2 0x5: Bank0_or_Bank2 0x6: Bank1_or_Bank2 0x7: Bank0_or_Bank1_or_Bank2 0x8: Bank3 0x9: Bank0_or_Bank3 0xA: Bank1_or_Bank3 0xB: Bank0_or_Bank1_or_Bank3 0xC: Bank2_or_Bank3 0xD: Bank0_or_Bank2_or_Bank3 0xE: Bank1_or_Bank2_or_Bank3 0xF: Any_Banks0_3 (default)
10	RESERVED_10	

EBI1_CH0_DDR_PMON_EVENT_CNTL0 (cont.)

Bits	Name	Description
9:2	EVENT12_TRANS_MATCH	SW: RW, HW: R Counts the number of DDR1x clock cycles where in the rank is refreshed ahead and matches one or more of the following. Bit 0 indicates if Rfsh Ahead val of 0 is matched Bit 1 indicates if Rfsh Ahead val of 1 is matched Bit 2 indicates if Rfsh Ahead val of 2 is matched Bit 3 indicates if Rfsh Ahead val of 3 is matched Bit 4 indicates if Rfsh Ahead val of 4 is matched Bit 5 indicates if Rfsh Ahead val of 5 is matched Bit 6 indicates if Rfsh Ahead val of 6 is matched Bit 7 indicates if Rfsh Ahead val of 7 is matched **NOTE** A combination of 1's in the vector indicates an OR condition. e.g., 0000_1110 indicates a required refresh ahead range of 1-3 0xFF: Any Rfsh Ahead (default)
1:0	EVENT12_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event12 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)

0x00A800B4 EBI1_CH0_DDR_PMON_EVENT0_MID_MATCH

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR SDRAM Performance Monitor Event0 MID Match Register

EBI1_CH0_DDR_PMON_EVENT0_MID_MATCH

Bits	Name	Description
31:16	EVENT0_MID_VAL_MATCH	SW: RW, HW: R Match the MID value for Event0. This is only applicable/useful if the transaction type match is a read. For writes this field will be ignored.
15:0	EVENT0_MID_MATCH_EN_MASK	SW: RW, HW: R Match enable mask for MID for Event0

0x00A800B8 EBI1_CH0_DDR_PMON_EVENT_CNTL1

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x3EF87800

DDR SDRAM Performance Monitor Event Control Register

EBI1_CH0_DDR_PMON_EVENT_CNTL1

Bits	Name	Description
31:30	RESERVED_31_30	
29:28	EVENT1_TRANS_MATCH	SW: RW, HW: R Counts the number of AXI Read or Write transactions or both. 0x0: Reserved 0x1: Read 0x2: Write 0x3: Read_or_Write (default)
27:25	EVENT1_PRIORITY_MATCH	SW: RW, HW: R Additional Match on priority value/range for Event1 0x0: Reserved 0x1: PVAL0 0x2: PVAL1 0x3: PVAL0_or_PVAL1 0x4: PVAL2 0x5: PVAL0_or_PVAL2 0x6: PVAL1_or_PVAL2 0x7: PVAL0_or_PVAL1_or_PVAL2 (default)
24	EVENT1_CMD_STARVED_MATCH	SW: RW, HW: R Additional Match on command starved for Event1. Note that command starvation is only applicable to read transactions 0x1: Match_Enable 0x0: Ignore (default)
23:21	EVENT1_PAGE_ATTR_MATCH	SW: RW, HW: R Additional Match on whether the transaction is a page hit or miss or conflict for Event1 0x0: Reserved 0x1: HIT 0x2: MISS 0x3: HIT_or_MISS 0x4: CONFLICT 0x5: HIT_or_CONFLICT 0x6: MISS_or_CONFLICT 0x7: HIT_or_MISS_or_CONFLICT (default)

EBI1_CH0_DDR_PMON_EVENT_CNTL1 (cont.)

Bits	Name	Description
20:19	EVENT1_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event1 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
18:11	EVENT1_BANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to which bank(s) for Event1 Others : Similar decode for all 8 banks 0x0: Reserved 0x1: Bank0 0x2: Bank1 0x3: Bank0_or_Bank1 0x4: Bank2 0x5: Bank0_or_Bank2 0x6: Bank1_or_Bank2 0x7: Bank0_or_Bank1_or_Bank2 0x8: Bank3 0x9: Bank0_or_Bank3 0xA: Bank1_or_Bank3 0xB: Bank0_or_Bank1_or_Bank3 0xC: Bank2_or_Bank3 0xD: Bank0_or_Bank2_or_Bank3 0xE: Bank1_or_Bank2_or_Bank3 0xF: Any_Banks0_3 (default)
10:0	RESERVED_10_0	

0x00A800BC EBI1_CH0_DDR_PMON_EVENT1_MID_MATCH

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR SDRAM Performance Monitor Event1 MID Match Register

EBI1_CH0_DDR_PMON_EVENT1_MID_MATCH

Bits	Name	Description
31:16	EVENT1_MID_VAL_MATCH	SW: RW, HW: R Match the MID value for Event1. This is only applicable/useful if the transaction type match is a read. For writes this field will be ignored.

EBI1_CH0_DDR_PMON_EVENT1_MID_MATCH (cont.)

Bits	Name	Description
15:0	EVENT1_MID_MATCH_EN_MASK	SW: RW, HW: R Match enable mask for MID for Event1

0x00A800C0 EBI1_CH0_DDR_PMON_EVENT_CNTL2

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x3EF87FFE

DDR SDRAM Performance Monitor Event Control Register

EBI1_CH0_DDR_PMON_EVENT_CNTL2

Bits	Name	Description
31:30	RESERVED_31_30	
29:28	EVENT2_TRANS_MATCH	SW: RW, HW: R Counts the number of AXI Read or Write transactions or both. 0x0: Reserved 0x1: Read 0x2: Write 0x3: Read_or_Write (default)
27:25	EVENT2_PRIORITY_MATCH	SW: RW, HW: R Additional Match on priority value/range for Event2 0x0: Reserved 0x1: PVAL0 0x2: PVAL1 0x3: PVAL0_or_PVAL1 0x4: PVAL2 0x5: PVAL0_or_PVAL2 0x6: PVAL1_or_PVAL2 0x7: PVAL0_or_PVAL1_or_PVAL2 (default)
24	EVENT2_CMD_STARVED_MATCH	SW: RW, HW: R Additional Match on command starved for Event2. Note that command starvation is only applicable to read transactions 0x1: Match_Enable 0x0: Ignore (default)

EBI1_CH0_DDR_PMON_EVENT_CNTL2 (cont.)

Bits	Name	Description
23:21	EVENT2_PAGE_ATTR_MATCH	SW: RW, HW: R Additional Match on whether the transaction is a page hit or miss or conflict for Event2 0x0: Reserved 0x1: HIT 0x2: MISS 0x3: HIT_or_MISS 0x4: CONFLICT 0x5: HIT_or_CONFLICT 0x6: MISS_or_CONFLICT 0x7: HIT_or_MISS_or_CONFLICT (default)
20:19	EVENT2_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event2 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
18:11	EVENT2_BANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to which bank(s) for Event2 Others : Similar decode for all 8 banks 0x0: Reserved 0x1: Bank0 0x2: Bank1 0x3: Bank0_or_Bank1 0x4: Bank2 0x5: Bank0_or_Bank2 0x6: Bank1_or_Bank2 0x7: Bank0_or_Bank1_or_Bank2 0x8: Bank3 0x9: Bank0_or_Bank3 0xA: Bank1_or_Bank3 0xB: Bank0_or_Bank1_or_Bank3 0xC: Bank2_or_Bank3 0xD: Bank0_or_Bank2_or_Bank3 0xE: Bank1_or_Bank2_or_Bank3 0xF: Any_Banks0_3 (default)

EBI1_CH0_DDR_PMON_EVENT_CNTL2 (cont.)

Bits	Name	Description
10:8	EVENT13_TRANS_MATCH	SW: RW, HW: R Counts the number of DDR1x clock cycles where in the rank(s) is in one or more of the following states - clock stop, power down, self refresh, idle, etc. 0x0: Reserved 0x1: Clock_Stop 0x2: Pwr_Down 0x3: Clock_Stop_or_Pwr_Down 0x4: Clock_Stop_and_Pwr_Down 0x5: Hardware Self_Refresh 0x6: Software Self_Refresh 0x7: Idle (default)
7:6	EVENT13_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event13 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
5:3	EVENT14_TRANS_MATCH	SW: RW, HW: R Counts the number of DDR1x clock cycles where in the rank(s) is in one or more of the following states - clock stop, power down, self refresh, idle, etc. 0x0: Reserved 0x1: Clock_Stop 0x2: Pwr_Down 0x3: Clock_Stop_or_Pwr_Down 0x4: Clock_Stop_and_Pwr_Down 0x5: Hardware Self_Refresh 0x6: Software Self_Refresh 0x7: Idle (default)
2:1	EVENT14_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event14 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
0	RESERVED_0	

0x00A800C4 EBI1_CH0_DDR_PMON_EVENT2_MID_MATCH

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR SDRAM Performance Monitor Event2 MID Match Register

EBI1_CH0_DDR_PMON_EVENT2_MID_MATCH

Bits	Name	Description
31:16	EVENT2_MID_VAL_MATCH	SW: RW, HW: R Match the MID value for Event2. This is only applicable/useful if the transaction type match is a read. For writes this field will be ignored.
15:0	EVENT2_MID_MATCH_EN_MASK	SW: RW, HW: R Match enable mask for MID for Event2

0x00A800C8 EBI1_CH0_DDR_PMON_EVENT_CNTL3

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x3EF87F30

DDR SDRAM Performance Monitor Event Control Register

EBI1_CH0_DDR_PMON_EVENT_CNTL3

Bits	Name	Description
31:30	RESERVED_31_30	
29:28	EVENT3_TRANS_MATCH	SW: RW, HW: R Counts the number of AXI Read or Write transactions or both. 0x0: Reserved 0x1: Read 0x2: Write 0x3: Read_or_Write (default)
27:25	EVENT3_PRIORITY_MATCH	SW: RW, HW: R Additional Match on priority value/range for Event3 0x0: Reserved 0x1: PVAL0 0x2: PVAL1 0x3: PVAL0_or_PVAL1 0x4: PVAL2 0x5: PVAL0_or_PVAL2 0x6: PVAL1_or_PVAL2 0x7: PVAL0_or_PVAL1_or_PVAL2 (default)

EBI1_CH0_DDR_PMON_EVENT_CNTL3 (cont.)

Bits	Name	Description
24	EVENT3_CMD_STARVED_MATCH	SW: RW, HW: R Additional Match on command starved for Event3. Note that command starvation is only applicable to read transactions 0x1: Match_Enable 0x0: Ignore (default)
23:21	EVENT3_PAGE_ATTR_MATCH	SW: RW, HW: R Additional Match on whether the transaction is a page hit or miss or conflict for Event3 0x0: Reserved 0x1: HIT 0x2: MISS 0x3: HIT_or_MISS 0x4: CONFLICT 0x5: HIT_or_CONFLICT 0x6: MISS_or_CONFLICT 0x7: HIT_or_MISS_or_CONFLICT (default)
20:19	EVENT3_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event3 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
18:11	EVENT3_BANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to which bank(s) for Event3 Others : Similar decode for all 8 banks 0x0: Reserved 0x1: Bank0 0x2: Bank1 0x3: Bank0_or_Bank1 0x4: Bank2 0x5: Bank0_or_Bank2 0x6: Bank1_or_Bank2 0x7: Bank0_or_Bank1_or_Bank2 0x8: Bank3 0x9: Bank0_or_Bank3 0xA: Bank1_or_Bank3 0xB: Bank0_or_Bank1_or_Bank3 0xC: Bank2_or_Bank3 0xD: Bank0_or_Bank2_or_Bank3 0xE: Bank1_or_Bank2_or_Bank3 0xF: Any_Banks0_3 (default)

EBI1_CH0_DDR_PMON_EVENT_CNTL3 (cont.)

Bits	Name	Description
10:8	EVENT15_TRANS_MATCH	SW: RW, HW: R Counts the number of DDR1x clock cycles where in the rank(s) is in one or more of the following states - clock stop, power down, self refresh, idle, etc. 0x0: Reserved 0x1: Clock_Stop 0x2: Pwr_Down 0x3: Clock_Stop_or_Pwr_Down 0x4: Clock_Stop_and_Pwr_Down 0x5: Hardware Self_Refresh 0x6: Software Self_Refresh 0x7: Idle (default)
7:6	RESERVED_7_6	
5:4	EVENT15_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event15 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
3:0	RESERVED_3_0	

0x00A800CC EBI1_CH0_DDR_PMON_EVENT3_MID_MATCH

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR SDRAM Performance Monitor Event3 MID Match Register

EBI1_CH0_DDR_PMON_EVENT3_MID_MATCH

Bits	Name	Description
31:16	EVENT3_MID_VAL_MATCH	SW: RW, HW: R Match the MID value for Event3. This is only applicable/useful if the transaction type match is a read. For writes this field will be ignored.
15:0	EVENT3_MID_MATCH_EN_MASK	SW: RW, HW: R Match enable mask for MID for Event3

0x00A800D0 EBI1_CH0_DDR_PMON_EVENT_CNTL4

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x7F30F000

DDR SDRAM Performance Monitor Event Control Register

EBI1_CH0_DDR_PMON_EVENT_CNTL4

Bits	Name	Description
31	RESERVED_31	
30:24	EVENT10_TRANS_MATCH	SW: RW, HW: R Counts the number of memory transactions which match the following. Use Bit 0 to indicate if Activates are to be included. Use Bit 1 to indicate if Reads are to be included. Use Bit 2 to indicate if Writes are to be included. Use Bit 3 to indicate if Bst's are to be included. Use Bit 4 to indicate if Auto Refreshes are included Use Bit 5 to indicate if Precharge All is included. Use Bit 6 to indicate if Per-Bank Precharge is included. **NOTE** A combination of 1's in the vector indicates an OR condition. e.g., 0000_011 indicates match condition would trigger on an Activate or Read command. 0000_000 : Reserved 1111_1111 : All of the above memory commands (default)
23:22	RESERVED_23_22	
21:20	EVENT10_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event10 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)

EBI1_CH0_DDR_PMON_EVENT_CNTL4 (cont.)

Bits	Name	Description
19:12	EVENT10_BANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to which bank(s) for Event10 Others : Similar decode for all 8 banks 0x0: Reserved 0x1: Bank0 0x2: Bank1 0x3: Bank0_or_Bank1 0x4: Bank2 0x5: Bank0_or_Bank2 0x6: Bank1_or_Bank2 0x7: Bank0_or_Bank1_or_Bank2 0x8: Bank3 0x9: Bank0_or_Bank3 0xA: Bank1_or_Bank3 0xB: Bank0_or_Bank1_or_Bank3 0xC: Bank2_or_Bank3 0xD: Bank0_or_Bank2_or_Bank3 0xE: Bank1_or_Bank2_or_Bank3 0xF: Any_Banks0_3 (default)
11:0	RESERVED_11_0	

0x00A800D4 EBI1_CH0_DDR_PMON_EVENT_CNTL5

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x7F30F000

DDR SDRAM Performance Monitor Event Control Register

EBI1_CH0_DDR_PMON_EVENT_CNTL5

Bits	Name	Description
31	RESERVED_31	

EBI1_CH0_DDR_PMON_EVENT_CNTL5 (cont.)

Bits	Name	Description
30:24	EVENT11_TRANS_MATCH	SW: RW, HW: R Counts the number of memory transactions which match the following. Use Bit 0 to indicate if Activates are to be included. Use Bit 1 to indicate if Reads are to be included. Use Bit 2 to indicate if Writes are to be included. Use Bit 3 to indicate if Bst's are to be included. Use Bit 4 to indicate if Auto Refreshes are included Use Bit 5 to indicate if Precharge All is included. Use Bit 6 to indicate if Per-Bank Precharge is included. **NOTE** A combination of 1's in the vector indicates an OR condition. e.g., 0000_011 indicates match condition would trigger on an Activate or Read command. 0000_000 : Reserved 1111_111 : All of the above memory commands (default)
23:22	RESERVED_23_22	
21:20	EVENT11_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event11 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
19:12	EVENT11_BANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to which bank(s) for Event11 Others : Similar decode for all 8 banks 0x0: Reserved 0x1: Bank0 0x2: Bank1 0x3: Bank0_or_Bank1 0x4: Bank2 0x5: Bank0_or_Bank2 0x6: Bank1_or_Bank2 0x7: Bank0_or_Bank1_or_Bank2 0x8: Bank3 0x9: Bank0_or_Bank3 0xA: Bank1_or_Bank3 0xB: Bank0_or_Bank1_or_Bank3 0xC: Bank2_or_Bank3 0xD: Bank0_or_Bank2_or_Bank3 0xE: Bank1_or_Bank2_or_Bank3 0xF: Any_Banks0_3 (default)
11:0	RESERVED_11_0	

0x00A800D8 EBI1_CH0_DDR_TEST_MUX

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR SDRAM Test Bus Mux Register

The following are the contents of the 32-bit test bus for each test bus select value. This only applies if the test bus is enabled.

- test_bus_sel == rd_vld_cmdptr0 (Hierarchy: hsddrx_ddrValidGen.sv)

assign o_testbus_rd_vld_cmdptr0 = {rank_ready_cs, i_rdcmdptrfifo_cmdptr, i_rdcmdptrfifo_empty, i_rdcmdptrfifo_rd_en, rdvalid_ddr_noptr, rdvalid_ddr_early, i_rdvalid_ddr_clear, 1'b0};

- test_bus_sel == rd_vld_cmdptr1 (Hierarchy: hsddrx_ddrValidGen.sv)

assign o_testbus_rd_vld_cmdptr1 = {rank_ready_cs, i_rdcmdptrfifo_cmdptr, i_rdcmdptrfifo_empty, i_rdcmdptrfifo_rd_en, rdvalid_ddr_noptr, i_rdvalid_ddr_set_toggle, copy_valid_ddr_clear_toggle, 1'b0};

- test_bus_sel == wr_vld_cmdptr (Hierarchy: hsddrx_ddrValidGen.sv)

assign o_testbus_wr_vld_cmdptr = {i_wrcmdptrfifo_cmdptr, i_wrcmdptrfifo_empty, i_wrcmdptrfifo_rd_en, i_wrvalid_ddr_clear, wrcmdptr_received_D, {11{1'b0}}};

- test_bus_sel == rd_runnable (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_rd_runnable = {rank_ready_csn, i_rdcmdptrfifo_cmdptr, i_rdcmdptrfifo_empty, rdcmdptrfifo_rd_en, rdvalid_ddr, rd_no_mem_runnable_axi_vec, rd_runnable_axi_vec, 1'b0};

- test_bus_sel == wr_runnable (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_wr_runnable = {rank_ready_csn, i_wrcmdptrfifo_cmdptr, i_wrcmdptrfifo_empty, wrcmdptrfifo_rd_en, wrvalid_ddr, wr_runnable_axi_vec, mod_runnable_exist_csn, interrupt, 6'b000000};

- test_bus_sel == ahb_csr (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_ahb_csr = {i_csr_addr[19:0], i_csr_req, i_csr_sync_mode, i_csr_wr, csr_ack, rank_ready_csn, 6'b000000};

- test_bus_sel == cmd_arbiter (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_cmd_arbiter = {reset_ddr_1x, rank_ready_csn, i_rdcmdptrfifo_empty, rdcmdptrfifo_rd_en, i_wrcmdptrfifo_empty, wrcmdptrfifo_rd_en, req_act_cmd, req_col_cmd_fsm, col_sel_wr_rd_cmdbuf, req_col_cmd, req_manual_cmd, req_precharge_cmd, loc_req_refresh_cmd, loc_self_refresh_req, grant_act_cmd, grant_col_cmd, grant_manual_cmd, grant_precharge_cmd, loc_grant_refresh_cmd, loc_self_refresh_grant, loc_in_self_refresh, loc_ddr_cke, loc_ddr_drive_ck, 2'b00};

- test_bus_sel == act_pchg_rfsh_addr (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_act_pchg_rfsh_addr = {rank_ready_csn, loc_rank_idle_exclude_rfsh, page_open_valid, page_close_valid, refresh_cmd_valid, loc_cmd_bank_addr, loc_cmd_rank_addr, cmd_row_addr};

- test_bus_sel == col_addr (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_col_addr = {rank_ready_csn, loc_rank_idle_exclude_rfsh, ddr_ca_even, loc_ddr_ba, loc_ddr_cs_n, req_col_cmd_fsm, col_sel_wr_rd_cmdbuf, req_col_cmd, drive_col_bst, drive_col_cmd, issue_srr_req, loc_in_dpd};

- test_bus_sel == act_algorithm0 (Hierarchy: hsddrx_actReqGen.sv)

assign o_testbus_act_algorithm0 = {i_rank_ready_cs, valid_act_runnable_rd_vec, valid_act_runnable_wr_vec, i_block_ddr_act_col_cmds_urg_rfsh_srr, i_block_ddr_cmds_urg_rfsh_srr, i_ddr_cmd_bus_idle_req, o_req_act_cmd, i_loc_cmd_bank_addr, i_loc_cmd_rank_addr};

- test_bus_sel == act_algorithm1 (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_act_algorithm1 = {rank_ready_csn, req_act_cmd, act_sel_wr_rd_cmdbuf, act_rdcmdbuf_ptr, act_wrcmdbuf_ptr, loc_cmd_bank_addr, loc_cmd_rank_addr, block_ddr_cmds_urg_rfsh_srr, block_ddr_act_col_cmds_urg_rfsh_srr, ddr_cmd_bus_idle_req, {9{1'b0}}};

- test_bus_sel == pchg_algorithm (Hierarchy: hsddrx_prechargeReqGen.sv)

assign o_testbus_pchg_algorithm = {i_rank_ready_cs, loc_precharge_bank_addr, precharge_rank_addr, req_precharge_all, o_req_precharge_cmd, i_block_ddr_cmds_urg_rfsh_srr, i_ddr_cmd_bus_idle_req, avail_valid_precharge_req_urg_refresh, avail_valid_precharge_req_trasmax_timer, avail_valid_precharge_req_page_mgmt_timer, avail_valid_precharge_req_srr, avail_valid_precharge_req_rank_idle, avail_valid_precharge_req_resource_unavail, loc_rank_available_cmd_exec, prefer_writes, selected_rd_cmdptr_precharge_res_unavail, selected_wr_cmdptr_precharge_res_unavail, loc_rank_idle_timer_expired, {5{1'b0}}};

- test_bus_sel == rfsh_algorithm0 (Hierarchy: hsddrx_refreshReqGen.sv)

assign o_testbus_rfsh_algorithm0 = {refresh_all_bank_mode, loc_grant_refresh_cmd, loc_sync_refresh_req_pend, loc_refresh_ahead_counter, loc_urgent_refresh_req_valid, 1'b0};

- test_bus_sel == rfsh_algorithm1 (Hierarchy: hsddrx_refreshReqGen.sv)

assign o_testbus_rfsh_algorithm1 = {loc_refresh_bank_addr, loc_req_refresh_cmd, loc_update_refresh_rate, loc_refresh_interval_timer};

- test_bus_sel == axi_col_algorithm (Hierarchy: hsddrx_colReqGen.sv)

assign o_testbus_axi_col_algorithm = {i_rank_ready_cs, col_rd_cmdptr, col_wr_cmdptr, no_col_req, col_sel_wr_rd_cmdbuf[0], req_col_cmd_fsm, i_col_cmd_en, i_ddr_cmd_bus_idle_req, i_rd_idle_req, i_wr_idle_req, valid_runnable_col_rd_vec, valid_runnable_col_wr_vec, wait_hp_req};

- test_bus_sel == manual_cmd_algorithm (Hierarchy: hsddrx_manualReqGen.sv)

assign o_testbus_manual_cmd_algorithm = {i_rank_ready_cs, 1'b0,o_manual_cmd_enc, loc_manual_cmd_rank_en, o_req_manual_cmd, i_grant_manual_cmd, loc_rank_idle, loc_in_dpd, loc_dpd_valid_cs, valid_dpd_entry, 16'h0000};

- test_bus_sel == self_rfsh_algorithm0 (Hierarchy: hsddrx_selfRefresh.sv)

assign o_testbus_self_rfsh_algorithm0 = {2'b00,current_state,2'b00,next_state, 1'b0,sw_self_rfsh_valid_req, 1'b0,self_refresh_req, 1'b0,i_self_refresh_grant, 1'b0,rank_available_cmd_exec, 1'b0,wakeup_sr, 1'b0,in_self_refresh, 1'b0,sr_exit_non_rd_expired, 1'b0,sr_exit_rd_expired, 1'b0,pend_self_refresh_req, 1'b0,i_ddr_cke, 1'b0,i_ddr_drive_ck, 1'b0,valid_sw_self_refresh_exit};

- test_bus_sel == self_rfsh_algorithm1 (Hierarchy: hsddrx_selfRefresh.sv)

assign o_testbus_self_rfsh_algorithm1 = {2'b00,current_state,2'b00,next_state, 1'b0,hw_self_rfsh_valid_req, 1'b0,self_refresh_req, 1'b0,i_self_refresh_grant, 1'b0,rank_available_cmd_exec, 1'b0,wakeup_sr, 1'b0,in_self_refresh, 1'b0,sr_exit_non_rd_expired, 1'b0,sr_exit_rd_expired, 1'b0,pend_self_refresh_req, 1'b0,i_ddr_cke, 1'b0,i_ddr_drive_ck, 1'b0,hw_self_refresh_idle_timer_expired};

- test_bus_sel == clock_stop_pwr_dwn (Hierarchy: hsddrx_clockStopPowerDown.sv)

assign o_testbus_cspd = {2'b00,current_state,2'b00,next_state, 1'b0,enter_clock_stop, 1'b0,enter_power_down, 1'b0,ddr_cke_cspd, 1'b0,ddr_drive_ck_cspd, 1'b0,i_ddr_cke, 1'b0,i_ddr_drive_ck, {12{1'b0}}};

- test_bus_sel == rank_timers (Hierarchy: hsddrx_ddrRankTimers.sv)

assign o_testbus_rank_timers = {4'b0000,i_cmd_bank_addr, 1'b0,i_cmd_rank_addr, i_page_open_valid, i_refresh_cmd_valid, 1'b0,loc_perbank_rfsh_satisfied_vec, 1'b0,loc_tRRD_satisfied_vec, {8{1'b0}},4'b0000,tRFC_satisfied_vec};

- test_bus_sel == open_pages_table0 (Hierarchy: hsddrx_openPagesTable.sv)

assign o_testbus_open_pages_table0 = {{8{1'b0}}, 4'b0000, opt_col_cmd_in_progress_Q[0],{8{1'b0}}, 4'b0000, opt_valid_Q[0]};

- test_bus_sel == open_pages_table1 (Hierarchy: hsddrx_openPagesTable.sv)

assign o_testbus_open_pages_table1 = {{8{1'b0}}, 4'b0000, opt_one_trans_exec_Q[0],

{8{1'b0}}, 4'b0000, opt_valid_Q[0]};

- test_bus_sel == cdc_iocal_req_ack (Hierarchy: hsddrx_iocalcdcIntf.sv)

  assign o_testbus_cdc_iocal_cdc_req = {i_rank_ready_cs, sync_cdc_update_req_ca, sync_cdc_update_req_rd, sync_cdc_update_req_wr, sync_iocal_update_req_ctrl, sync_iocal_update_req_data, loc_cdc_update_ack_ca, loc_cdc_update_ack_rd, loc_cdc_update_ack_wr, loc_iocal_update_ack_ctrl, loc_iocal_update_ack_data, ddr_cmd_bus_idle_req, rd_idle_req, wr_idle_req, i_act_cmd_rdy_calib, i_col_cmd_rdy_calib, i_manual_cmd_rdy_calib, 1'b0, i_rddata_rdy_calib, 1'b0, i_wrdata_rdy_calib, i_col_req_idle, i_req_col_cmd_fsm, i_col_sel_wr_rd_cmdbuf, i_grant_act_cmd, i_grant_col_cmd, i_grant_precharge_cmd, 1'b0,i_grant_refresh_cmd, 1'b0,i_grant_self_refresh_cmd};

- test_bus_sel == mem_cmd_gen0 (Hierarchy: hsddrx_memCmdGen.sv)

assign o_testbus_mem_cmd_gen0 = {i_rank_ready_cs, i_req_col_cmd_fsm, alen_counter_Q, axi_col_trans_aburst_req_Q, axi_col_trans_addr_byte_Q, axi_col_trans_alen_Q, axi_col_trans_asize_Q, axi_col_trans_readmerge_Q, axi_col_trans_wr_Q, mem_bl_count_Q, loc_col_cmd_en, loc_mem_cmd_valid, i_mem_cmd_accept, loc_mem_bl_dw_valid_serial, mem_cmd_cas_in_prog, mod_mem_cmd_last_cas, mem_col_last_beat_cmd_early};

- test_bus_sel == mem_cmd_gen1 (Hierarchy: hsddrx_memCmdGen.sv)

assign o_testbus_mem_cmd_gen1 = {i_rank_ready_cs, i_req_col_cmd_fsm, axi_col_trans_aburst_req_Q, 1'b0,axi_col_trans_addr_bank_Q, axi_col_trans_addr_col_Q, axi_col_trans_addr_rank_Q, axi_col_trans_addr_row_Q};

- test_bus_sel == col_fsm0 (Hierarchy: hsddrx_colFsm.sv)

assign o_testbus_col_fsm0 = {i_rank_ready_cs, current_state, next_state, i_req_col_cmd_fsm, i_mem_cmd_cas_in_prog, i_mem_cmd_valid, mem_cmd_accept, i_mem_col_last_beat_cmd_reg, i_mem_col_write, i_timing_satisfied, i_use_bst_cmd_to_int_rd, i_use_bst_cmd_to_int_wr, i_use_next_rd_cmd_to_int, i_use_next_wr_cmd_to_int, drive_col_bst, drive_col_rd, drive_col_wr, req_col_cmd, 1'b0};

- test_bus_sel == col_fsm1 (Hierarchy: hsddrx_colFsm.sv)

assign o_testbus_col_fsm1 = {current_state, next_state, i_req_col_cmd_fsm, i_mem_cmd_cas_in_prog, mem_cmd_accept, load_multiT_timer, i_multiT_timer_expired, mem_cmd_valid_rd, mem_cmd_valid_wr, i_use_bst_cmd_to_int_rd, i_use_bst_cmd_to_int_wr, i_use_next_rd_cmd_to_int, i_use_next_wr_cmd_to_int, drive_col_bst_cs, drive_col_bst_except_cs, drive_col_rd_cs, drive_col_rd_except_cs, drive_col_wr_cs, drive_col_wr_except_cs, req_col_cmd};

- test_bus_sel == col_cmd_int_cntl (Hierarchy: hsddrx_colCmdInterruptCtrl.sv)

assign o_testbus_col_cmd_int_cntl = {qual_almost_expired_bl_dw, cmd_int_qual, curr_cmd_can_be_int, expired_bl_dw, i_mem_cmd_valid, i_mem_col_rank, i_mem_col_write, i_mem_col_valid_curr_cmd, i_mem_col_rank_curr_cmd, i_mem_col_write_curr_cmd, int_boundary_met, int_every_cycle, int_every_fourth_cycle, int_every_second_cycle, loc_use_bst_cmd_to_int_rd, loc_use_bst_cmd_to_int_wr, rd_cmd_int_by_rd, wr_cmd_int_by_wr, 14{1'b0}}};

- test_bus_sel == wr_data (Hierarchy: hsddrx_wrDataCtrl.sv)

assign o_testbus_wrdata = {i_rank_ready_cs, i_req_col_cmd_fsm, i_drive_col_wr, tburst_expired_wr, i_drive_col_wr_cs, start_bl_cnt, stop_bl_cnt, stop_bl_cnt_reg, drive_col_wr, ddr_drive_wr_dqs, ddr_wr_2dm, loc_load_tWR_valid, wrdatabuf_request, loc_wrdatabuf_firstword, loc_wrdatabuf_cmdptr, loc_wrdatabuf_lineptr, loc_wrdatabuf_wordptr, 2'b00};

- test_bus_sel == rd_data (Hierarchy: hsddrx_rdData.v & hsddrx_rdDataCtrl.sv)

assign o_testbus_rddata1 = {tburst_expired_rd, capture_rd_fifo_wen, loc_pad_ie_dq, loc_pad_ie_dqs, loc_rd_data_keep_throw_fifo_wdata, loc_rd_data_keep_throw_fifo_wen, ie_capture_cntr_expired, ie_start_dly_cntr_expired, rd_data_capture_cntr_expired, rd_data_dly_cntr_expired, bst_col_cmd_reg, rd_col_cmd_reg, srr_rd_cmd_reg};

assign o_testbus_rddata0 = {capture_rd_fifo_empty, i_capture_rd_fifo_wen, 1'b0, 1'b0, {8{1'b0}}};

assign testbus_rddata = {testbus_rddata1,testbus_rddata0};

- test_bus_sel == ddr_bus0 (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_ddr_bus0 = {rank_ready_csn, ddr_ca_even, loc_ddr_ba, ddr_cas_n, ddr_cke, loc_ddr_cs_n, ddr_drive_ck, ddr_drive_wr_dqs, ddr_ras_n, ddr_we_n, pad_ie_dq, pad_oe_dq, pad_ie_dqs, pad_oe_dqs, 1'b0};

- test_bus_sel == ddr_bus1 (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_ddr_bus1 = {rank_ready_csn, loc_ddr_ba, ddr_cas_n, ddr_cke, loc_ddr_cs_n, ddr_drive_ck, ddr_drive_wr_dqs, ddr_ras_n, ddr_we_n, pad_ie_dq, pad_oe_dq, pad_ie_dqs, pad_oe_dqs, loc_ddr_odt, loc_pad_odt_dq, loc_pad_odt_dqs, loc_ddr_reset_n, loc_ddr_wr_2dm, 1'b0};

- test_bus_sel == ddr_bus2 (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_ddr_bus2 = {ddr_ca_even, ddr_ca_odd, pad_ie_dq, pad_oe_dq};

EBI1_CH0_DDR_TEST_MUX

Bits	Name	Description
31	ENABLE	SW: RW, HW: R Test Bus Enable. 0x0: Disable (ddr_test_bus drives 32'b0 default) 0x1: Enable (ddr_test_bus drives selected signals)
30:6	RESERVED_30_6	

EBI1_CH0_DDR_TEST_MUX (cont.)

Bits	Name	Description
5:0	TEST_BUS_SEL	SW: RW, HW: R Selects internally generated signals for observation on the ddr_test_bus. 0x0: rd_vld_cmdptr0 0x1: rd_vld_cmdptr1 0x2: wr_vld_cmdptr 0x3: rd_runnable 0x4: wr_runnable 0x5: ahb_csr 0x6: cmd_arbiter 0x7: act_pchg_rfsh_addr 0x8: col_addr 0x9: act_algorithm0 0xA: act_algorithm1 0xB: pchg_algorithm 0xC: rfsh_algorithm0 0xD: rfsh_algorithm1 0xE: axi_col_algorithm 0xF: manual_cmd_algorithm 0x10: self_rfsh_algorithm0 0x11: self_rfsh_algorithm1 0x12: clock_stop_pwr_dwn 0x13: rank_timers 0x14: open_pages_table0 0x15: open_pages_table1 0x16: cdc_iocal_req_ack 0x17: mem_cmd_gen0 0x18: mem_cmd_gen1 0x19: col_fsm0 0x1A: col_fsm1 0x1B: col_cmd_int_cntl 0x1C: wr_data 0x1D: rd_data 0x1E: ddr_bus0 0x1F: ddr_bus1 0x20: ddr_bus2

0x00A80100 EBI1_CH0_DDR_MRW0_HW_FREQ_SWITCH

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Write Control for HW Frequency Switch Register

This register is used/valid as part of HW based frequency switch if DDR_CMD_EXEC_OPT_2[UPDATE_MEM_LATENCY_ON_FREQ_SWITCH] is set.There is no rank select field as the mode register write command goes to all initialized ranks. If the memory latencies are required to be changed as part of frequency switching, SW would be required to program the correct Read/Write latency in the corresponding _ALT registers and also program this register to have HW perform an MRW with the updated latency values when a frequency switch request is being processed.

EBI1_CH0_DDR_MRW0_HW_FREQ_SWITCH

Bits	Name	Description
31:24	MRW_ADDR	SW: RW, HW: R Specify which mode register to access. Note that LPDDR2 supports up to 256 Mode registers. Hence the programmed MR_ADDR needs to be valid based on the specific SDRAM device. 0000_0000 : MR (Mode Register or SR for LPDDR1) 0000_0001 : EMR1 (Extended Mode Register 1) 0000_0010 : EMR2 (Extended Mode Register 2) 0000_0011 : EMR2 (Extended Mode Register 3) .....
23:21	RESERVED_23_21	
20	MRW_VALID	SW: RW, HW: R Indicates if the contents of this register are valid.
19:16	RESERVED_19_16	
15:0	MRW_DATA	SW: RW, HW: R Data for Mode Register Writes. SW needs to program the mode register based on the specific SDRAM device as the mapping of the 16-bits is different for different SDRAM device types.

0x00A80104 EBI1_CH0_DDR_MRW1_HW_FREQ_SWITCH

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Write Control for HW Frequency Switch Register

This register is used/valid as part of HW based frequency switch if DDR_CMD_EXEC_OPT_2[UPDATE_MEM_LATENCY_ON_FREQ_SWITCH] is set.There is no rank select field as the mode register write command goes to all initialized ranks. If the memory latencies are required to be changed as part of frequency switching, SW would be required to program the correct Read/Write latency in the corresponding _ALT registers and also program this register to have HW perform an MRW with the updated latency values when a frequency switch request is being processed.

EBI1_CH0_DDR_MRW1_HW_FREQ_SWITCH

Bits	Name	Description
31:24	MRW_ADDR	SW: RW, HW: R Specify which mode register to access. Note that LPDDR2 supports up to 256 Mode registers. Hence the programmed MR_ADDR needs to be valid based on the specific SDRAM device. 0000_0000 : MR (Mode Register or SR for LPDDR1) 0000_0001 : EMR1 (Extended Mode Register 1) 0000_0010 : EMR2 (Extended Mode Register 2) 0000_0011 : EMR2 (Extended Mode Register 3) .....
23:21	RESERVED_23_21	
20	MRW_VALID	SW: RW, HW: R Indicates if the contents of this register are valid.
19:16	RESERVED_19_16	
15:0	MRW_DATA	SW: RW, HW: R Data for Mode Register Writes. SW needs to program the mode register based on the specific SDRAM device as the mapping of the 16-bits is different for different SDRAM device types.

0x00A80120 EBI1_CH0_DDR_DQCAL_RDATA_RANK1

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR DQ Calibration Read Data Register for Rank1

This register contains the DRAM mode register contents for a DQ calibration command triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] to Rank1. This is used to capture the read data from the SDRAM device's mode register for a read DQ calibration command for LPDDR2 or an MPR read command for PCDDR3. The DQS data bits 0, 8, 16 and 24 are only captured on each DQS edge. Hence for a memory burst length of 4 (LPDDR2 DQ calibration), only 16:0 bits of the field below have valid data. In case of PCDDR3 MPR read command (memory burst length of 8), all 32 bits of the field below are valid.

EBI1_CH0_DDR_DQCAL_RDATA_RANK1

Bits	Name	Description
31:0	DQCAL_RDATA	SW: R, HW: W Data for DQ Calibration Read for Rank1. The data captures the lowest bit for each byte across the memory burst. For example, each cycle of memory burst is 8 bytes of data - 1 bit for each byte is captured which is 8 bits for every cycle of DQS.

0x00A80124 EBI1_CH0_DDR_DQCAL_RDATA_RANK0

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR DQ Calibration Read Data Register for Rank0

This register contains the DRAM mode register contents for a DQ calibration command triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] to Rank0. This is used to capture the read data from the SDRAM device's mode register for a read DQ calibration command for LPDDR2 or an MPR read command for PCDDR3. The DQS data bits 0, 8, 16 and 24 are only captured on each DQS edge. Hence for a memory burst length of 4 (LPDDR2 DQ calibration), only 16:0 bits of the field below have valid data. In case of PCDDR3 MPR read command (memory burst length of 8), all 32 bits of the field below are valid.

EBI1_CH0_DDR_DQCAL_RDATA_RANK0

Bits	Name	Description
31:0	DQCAL_RDATA	SW: R, HW: W Data for DQ Calibration Read for Rank1. The data captures the lowest bit for each byte across the memory burst. For example, each cycle of memory burst is 8 bytes of data - 1 bit for each byte is captured which is 8 bits for every cycle of DQS.

0x00A80130 EBI1_CH0_DDR_DQCAL_STATUS_RANK1

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR DQ Calibration Status Register for Rank1

EBI1_CH0_DDR_DQCAL_STATUS_RANK1

Bits	Name	Description
31	DQCAL_COMPARE_BYTE3	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE3) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS
30	DQCAL_COMPARE_BYTE2	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE2) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS
29	DQCAL_COMPARE_BYTE1	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE1) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS
28	DQCAL_COMPARE_BYTE0	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE0) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS

EBI1_CH0_DDR_DQCAL_STATUS_RANK1 (cont.)

Bits	Name	Description
27	RESERVED_27	
26:24	NUM_DQS_PE_EDGES_RECD_BYTE3	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
23	RESERVED_23	
22:20	NUM_DQS_PE_EDGES_RECD_BYTE2	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
19	RESERVED_19	

EBI1_CH0_DDR_DQCAL_STATUS_RANK1 (cont.)

Bits	Name	Description
18:16	NUM_DQS_PE_EDGES_RECD_BYTE1	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
15	RESERVED_15	
14:12	NUM_DQS_PE_EDGES_RECD_BYTE0	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
11:9	NUM_DQS_NE_EDGES_RECD_BYTE3	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges

EBI1_CH0_DDR_DQCAL_STATUS_RANK1 (cont.)

Bits	Name	Description
8:6	NUM_DQS_NE_EDGES_RECD_BYTE2	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
5:3	NUM_DQS_NE_EDGES_RECD_BYTE1	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
2:0	NUM_DQS_NE_EDGES_RECD_BYTE0	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges

0x00A80134 EBI1_CH0_DDR_DQCAL_STATUS_RANK0

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR DQ Calibration Status Register for Rank0

EBI1_CH0_DDR_DQCAL_STATUS_RANK0

Bits	Name	Description
31	DQCAL_COMPARE_BYTE3	Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE3) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS
30	DQCAL_COMPARE_BYTE2	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE2) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS
29	DQCAL_COMPARE_BYTE1	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE1) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS

EBI1_CH0_DDR_DQCAL_STATUS_RANK0 (cont.)

Bits	Name	Description
28	DQCAL_COMPARE_BYTE0	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE0) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS
27	RESERVED_27	
26:24	NUM_DQS_PE_EDGES_RECD_BYTE3	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
23	RESERVED_23	
22:20	NUM_DQS_PE_EDGES_RECD_BYTE2	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
19	RESERVED_19	

EBI1_CH0_DDR_DQCAL_STATUS_RANK0 (cont.)

Bits	Name	Description
18:16	NUM_DQS_PE_EDGES_RECD_BYTE1	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
15	RESERVED_15	
14:12	NUM_DQS_PE_EDGES_RECD_BYTE0	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
11:9	NUM_DQS_NE_EDGES_RECD_BYTE3	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges

EBI1_CH0_DDR_DQCAL_STATUS_RANK0 (cont.)

Bits	Name	Description
8:6	NUM_DQS_NE_EDGES_RECD_BYTE2	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
5:3	NUM_DQS_NE_EDGES_RECD_BYTE1	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
2:0	NUM_DQS_NE_EDGES_RECD_BYTE0	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges

0x00A80140 EBI1_CH0_DDR_RCW_RESET_AND_CNTL

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR RCW Async Reset & Control Register

This register controls the async reset for the generated RCW (Read capture window for DQS)

signal for DQS qualification in the PHY. It also includes a global disable control which results in the external RCW signal being driven always to 1'b1.

EBI1_CH0_DDR_RCW_RESET_AND_CNTL

Bits	Name	Description
31:28	RESERVED_31_28	
27	RCW_ASYNC_RESET_BYTE3	SW: RW, HW: R SW control for the async reset for the flops in the RCW generation circuit for PHY data byte3. SW writes this field to 1'b1 if the flops in the PHY are required to be reset. HW will assert reset for a few cycles and then de-assert. Sw need not write this to 1'b0. The read value will always be 1'b0. 0x0: RESET OFF (default) 0x1: RESET ON
26	RCW_ASYNC_RESET_BYTE2	SW: RW, HW: R SW control for the async reset for the flops in the RCW generation circuit for PHY data byte3. SW writes this field to 1'b1 if the flops in the PHY are required to be reset. HW will assert reset for a few cycles and then de-assert. Sw need not write this to 1'b0. The read value will always be 1'b0. 0x0: RESET OFF (default) 0x1: RESET ON
25	RCW_ASYNC_RESET_BYTE1	SW: RW, HW: R SW control for the async reset for the flops in the RCW generation circuit for PHY data byte3. SW writes this field to 1'b1 if the flops in the PHY are required to be reset. HW will assert reset for a few cycles and then de-assert. Sw need not write this to 1'b0. The read value will always be 1'b0. 0x0: RESET OFF (default) 0x1: RESET ON
24	RCW_ASYNC_RESET_BYTE0	SW: RW, HW: R SW control for the async reset for the flops in the RCW generation circuit for PHY data byte3. SW writes this field to 1'b1 if the flops in the PHY are required to be reset. HW will assert reset for a few cycles and then de-assert. Sw need not write this to 1'b0. The read value will always be 1'b0. 0x0: RESET OFF (default) 0x1: RESET ON

EBI1_CH0_DDR_RCW_RESET_AND_CNTL (cont.)

Bits	Name	Description
23:17	RESERVED_23_17	
16	RCW_ENABLE	SW: RW, HW: R When set to 1'b0, the external RCW (Read capture window) for precise DQS qualification is always driven to 1'b1 for all data bytes. When enabled (required only for PCDDR3), the design will send out an RCW pulse equal to the memory BL/2 -1 cycles to the PHY data bytes. 0x0: Disable (default) 0x1: Enable
15:1	RESERVED_15_1	
0	RD_FIFO_CNTL_DBG_EN	SW: RW, HW: R When set to 1'b1, this will match the previous design behavior wherein the read data keep/throw is written for MRR commands. If this field is set, then RCW_ENABLE must be disabled. 0x0: Disable (default) 0x1: Enable

0x00A80200 EBI1_CH0_DDR_ENHPRI_EN

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Enable Register.

This register is used to enable and configure enable enhanced prioritization of read and write commands within the DDR controller.

EBI1_CH0_DDR_ENHPRI_EN

Bits	Name	Description
31	ENHANCED_PRI_EN	SW: RW, HW: R Enables enhanced transaction prioritization mode. When enabled the priority of read and write transactions within the DDR controller can be modified to more quickly resolve blocking conditions and minimize worse case latencies. When this feature is enabled is it required that read command starvation be disabled by programming DDR_CMD_EXEC_OPT_0[RDCMD_STARVATION_TIMER] = 0. 0x0: Disable (default) 0x1: Enable

EBI1_CH0_DDR_ENHPRI_EN (cont.)

Bits	Name	Description
30	RD_PRI_AGING_EN	When enabled the DDR priority of read commands increases the longer they remaining unserviced. The priority adjustment is set through the DDR_ENHPRI_RDn registers. 0x0: Disable (default) 0x1: Enable
29	WR_PRI_AGING_EN	When enabled the DDR priority of write commands increases the longer they remaining unserviced. The priority adjustment is set through the DDR_ENHPRI_WRn registers. 0x0: Disable (default) 0x1: Enable
28	RESERVED_28	
27	ADJ_PRI_RDBLOCKING	SW: RW, HW: R When enabled the AXI priority of a read command blocking acceptance of write data is replaced with the value in the PRI_RDBLOCKING field. 0x0: Disable (default) 0x1: Enable
26	ADJ_PRI_RDMERGE	SW: RW, HW: R When enabled a read merge is considered to be blocking write data and its priority is replaced with the value in the PRI_RDBLOCKING field. 0x0: Disable (default) 0x1: Enable
25:24	PRI_RDBLOCKING	AXI priority for blocking read commands 0x0: AXI priority Level 0 (default) 0x1: AXI priority Level 1 0x2: AXI priority Level 2 0x3: AXI priority Level 3
23	ADJ_PRI_WRBLOCKING	SW: RW, HW: R When enabled the AXI priority of a write command blocking acceptance of write data or execution of a subsequent read is replaced with the value in the PRI_RDBLOCKING field. 0x0: Disable (default) 0x1: Enable
22	RESERVED_22	
21:20	PRI_WRBLOCKING	AXI priority for blocking write commands 0x0: AXI priority Level 0 (default) 0x1: AXI priority Level 1 0x2: AXI priority Level 2 0x3: AXI priority Level 3
19:16	RESERVED_19_16	

EBI1_CH0_DDR_ENHPRI_EN (cont.)

Bits	Name	Description
15:8	CONFLICT_BLOCK_HIT	SW: RW, HW: R When not disabled a page conflict of the given priority level(s) blocks any new command presented to the DDR controller from being a page hit to the same rank/bank as the conflict. Others: All combinations of priorities are legal. 0x0: Disabled 0x1: Priority 0 0x2: Priority 1 0x3: Priorities 0 and 1 0x4: Priority 2 0x8: Priority 3 0x10: Priority 4 0x20: Priority 5 0x40: Priority 6 0x80: Priority 7
7:0	RESERVED_7_0	

0x00A80224 EBI1_CH0_DDR_ENHPRI_RD1

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 1.

Number of cycles for a read command to attain DDR priority level 1.

EBI1_CH0_DDR_ENHPRI_RD1

Bits	Name	Description
31:7	RESERVED_31_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 0 becomes DDR priority 1.

0x00A80228 EBI1_CH0_DDR_ENHPRI_RD2

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 2.

Number of cycles for a read command to attain DDR priority level 2.

EBI1_CH0_DDR_ENHPRI_RD2

Bits	Name	Description
31:7	RESERVED_31_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 0 becomes DDR priority 2.

0x00A8022C EBI1_CH0_DDR_ENHPRI_RD3

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 3.

Number of cycles for a read command to attain DDR priority level 3.

EBI1_CH0_DDR_ENHPRI_RD3

Bits	Name	Description
31:15	RESERVED_31_15	
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 1 becomes DDR priority 3.
7	RESERVED_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 0 becomes DDR priority 3.

0x00A80230 EBI1_CH0_DDR_ENHPRI_RD4

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 4.

Number of cycles for a read command to attain DDR priority level 4.

EBI1_CH0_DDR_ENHPRI_RD4

Bits	Name	Description
31:15	RESERVED_31_15	

EBI1_CH0_DDR_ENHPRI_RD4 (cont.)

Bits	Name	Description
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 1 becomes DDR priority 4.
7	RESERVED_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 0 becomes DDR priority 4.

0x00A80234 EBI1_CH0_DDR_ENHPRI_RD5

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 5.

Number of cycles for a read command to attain DDR priority level 5.

EBI1_CH0_DDR_ENHPRI_RD5

Bits	Name	Description
31:23	RESERVED_31_23	
22:16	CYCLES_AXIPRI2	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 2 becomes DDR priority 5.
15	RESERVED_15	
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 1 becomes DDR priority 5.
7	RESERVED_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 0 becomes DDR priority 5.

0x00A80238 EBI1_CH0_DDR_ENHPRI_RD6

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 6.

Number of cycles for a read command to attain DDR priority level 6.

EBI1_CH0_DDR_ENHPRI_RD6

Bits	Name	Description
31:23	RESERVED_31_23	
22:16	CYCLES_AXIPRI2	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 2 becomes DDR priority 6.
15	RESERVED_15	
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 1 becomes DDR priority 6.
7	RESERVED_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 0 becomes DDR priority 6.

0x00A8023C EBI1_CH0_DDR_ENHPRI_RD7

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 7.

Number of cycles for a read command to attain DDR priority level 7.

EBI1_CH0_DDR_ENHPRI_RD7

Bits	Name	Description
31	RESERVED_31	
30:24	CYCLES_AXIPRI3	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 3 becomes DDR priority 7.
23	RESERVED_23	
22:16	CYCLES_AXIPRI2	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 2 becomes DDR priority 7.
15	RESERVED_15	
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which7a read with AXI priority 1 becomes DDR priority 7.

EBI1_CH0_DDR_ENHPRI_RD7 (cont.)

Bits	Name	Description
7	RESERVED_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with priority 0 becomes DDR priority 7.

0x00A80248 EBI1_CH0_DDR_ENHPRI_WR2

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Write Latency 2.

Number of cycles for a write command to attain DDR priority level 2.

EBI1_CH0_DDR_ENHPRI_WR2

Bits	Name	Description
31:7	RESERVED_31_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a write with AXI priority 0 becomes DDR priority 2.

0x00A80250 EBI1_CH0_DDR_ENHPRI_WR4

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Write Latency 4.

Number of cycles for a write command to attain DDR priority level 4.

EBI1_CH0_DDR_ENHPRI_WR4

Bits	Name	Description
31:15	RESERVED_31_15	
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which a write with AXI priority 1 becomes DDR priority 4.
7	RESERVED_7	

EBI1_CH0_DDR_ENHPRI_WR4 (cont.)

Bits	Name	Description
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a write with AXI priority 0 becomes DDR priority 4.

0x00A80258 EBI1_CH0_DDR_ENHPRI_WR6

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Write Latency 6.

Number of cycles for a write command to attain DDR priority level 6.

EBI1_CH0_DDR_ENHPRI_WR6

Bits	Name	Description
31:23	RESERVED_31_23	
22:16	CYCLES_AXIPRI2	SW: RW, HW: R DDR cycles divided by 8 after which a write with AXI priority 2 becomes DDR priority 6.
15	RESERVED_15	
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which a write with AXI priority 1 becomes DDR priority 6.
7	RESERVED_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a write with AXI priority 0 becomes DDR priority 6.

13.2.1.6 Loop-back Self-test Registers

This section contains the registers that are related to loop-back self-test logic. They control the loop-back path and logic behaviors. They also provide a mechanism to read out the MISR signature registers for software to compare the results.

0x00AD0000 EBI1_CH0_LBST_CNTL

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

LBST logic control register.

EBI1_CH0_LBST_CNTL

Bits	Name	Description
31	FORCE_DRIVE_DQS	SW : RW Force DIM to drive memory dqs 0x0: stop forcing to drive DQS 0x1: start driving always
30	FORCE_DRIVE_CK	SW : RW Force DIM to drive memory clock 0x0: stop forcing to drive CK 0x1: start driving always
29	CLR_CNTR_DQ_ALL	SW : W Writing '1' to this bit will clear all the counters for DQ 0x0: no action 0x1: clear the counter
28	CLR_CNTR_CA_ALL	SW : W Writing '1' to this bit will clear all the counters for CA 0x0: no action 0x1: clear the counter
27	RESET_FIFO	SW : W Write '1' to this bit clear the DQ and CA FIFO 0x0: no action 0x1: reset FIFO
26	SHIFT_PRPG_DQ	SW : RW Control if DQ PRPG should be shifting 0x0: no shifting PRPG 0x1: start shifting PRPG
25	SHIFT_PRPG_CA	SW : RW Control if CA PRPG should be shifting 0x0: no shifting PRPG 0x1: start shifting PRPG
24	DATA_SRC_CA	SW : RW Data source for command and address: 0x0: from DDR controller 0x1: from LBST CA PRPG
23:22	DATA_SRC_DQ	SW : RW Data source for read data: 0x0: from DDR controller 0x1: from LBST DQ PRPGs 0x2: Dynamicall switching in read/write.

EBI1_CH0_LBST_CNTL (cont.)

Bits	Name	Description
21:20	FIFO_WE_DQ	SW : RW WE for CA FIFOs and DQ FIFOs 0x0: Write is disabled on all FIFOs 0x1: Write disabled on DQ FIFOs, enabled on CA FIFOs. 0x2: Write enabled all FIFOs 0x3: Dynamic all switching in read/write on DQ FIFOs. Always enabled on CA FIFOs
19	FORCE_OE_DQ	SW : RW Control DQ's OE if FORCE_MODE_DQ == 1 0x0: Force DQ IE to be 0 0x1: Force DQ IE to be 1
18	FORCE_IE_DQ	SW : RW Control DQ's IE if FORCE_MODE_DQ == 1 0x0: Force DQ IE to be 0 0x1: Force DQ IE to be 1
17	FORCE_MODE_DQ	SW : RW DQ's IE/OE is either controlled by DDR controller or by the FORCE_IE_DQ, FORCE_OE_DQ 0x0: Controlled by DDR controller 0x1: Manually controlled by LBST logic
16	FORCE_IE_CA	SW : RW Force IE to turn on all the command/address pads 0x0: Stop forcing IE 0x1: Force to turn on
15:14	READ_BURST	SW : RW Controls numbers of data burst per matching read command: 0x0: 4 burst of data 0x1: 8 burst of data 0x2: 16 burst of data 0x3: unused
13	IGNORE_IDLE_CMD	SW : RW Controls whether IDLE command will be ignored in MISR operation 0x0: Don't ignore zero data 0x1: Ignore zero data
12	IGNORE_ZERO_DQ	SW : RW Controls whether zero data will be ignored or not in MISR operation 0x0: Don't ignore zero data 0x1: Ignore zero data

EBI1_CH0_LBST_CNTL (cont.)

Bits	Name	Description
11:10	MISR_TRIG_DQ	SW : RW Specify condition that triggers shifting of DQ MISR: 0x0: When DQ FIFO is not empty 0x1: by matching command 0x2: by external shift enable bit 0x3: CSR controlled enable. Turned on by writing to START_SHIFT_PRPG. Turned off by writing to STOP_SHIFT_PRPG.
9:8	MISR_TRIG_CA	SW : RW Specify condition that triggers shifting of CA MISR: 0x0: when CMD FIFO is not empty and command matches 0x1: unused 0x2: by external shift enable bit 0x3: CSR controlled enable. Turned on by writing to START_SHIFT_PRPG. Turned off by writing to STOP_SHIFT_PRPG.
7:6	MISR_MODE_DQ	SW : RW Operating mode for DQ MISRs 0x0: Hold 0x1: Parallel-in parallel-out FF buffer 0x2: LFSR 0x3: Shift register only
5:4	MISR_MODE_CA	SW : RW Operating mode for CA MISR 0x0: Hold 0x1: Parallel-in parallel-out FF buffer 0x2: LFSR 0x3: Shift register only
3:2	LB_MODE_DQ	SW : RW Controls loop-back path within DIMs for write data 0x0: Normal functional mode 0x1: External loop-back mode 0x2: Do not use. 0x3: Internal loop-back mode
1	LB_CK_SEL_CA	SW : RW Controls which of the 2 memory clocks is used in command/address loop back 0x0: use rank 0's clock 0x1: use rank 1's clock
0	LB_MODE_CA	SW : RW Controls loop-back path within DIMs for command/address 0x0: path is disabled 0x1: path is enabled

0x00AD0004 EBI1_CH0_LBST_MISR_CA

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

LBST MISR register for command & address. Software can either read out this register to get the signature results, or write to this register to set up the seed for PRPG.

EBI1_CH0_LBST_MISR_CA

Bits	Name	Description
31:0	MISR_VAL	SW : RW MISR value

0x00AD0008 EBI1_CH0_LBST_MISR_DQ_EVEN

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

LBST MISR register for even data burst. Software can either read out this register to get the signature results, or write to this register to set up the seed for PRPG.

EBI1_CH0_LBST_MISR_DQ_EVEN

Bits	Name	Description
31:0	MISR_VAL	SW : RW MISR value

0x00AD000C EBI1_CH0_LBST_MISR_DQ_ODD

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

LBST MISR register for odd data burst. Software can either read out this register to get the signature results, or write to this register to set up the seed for PRPG.

EBI1_CH0_LBST_MISR_DQ_ODD

Bits	Name	Description
31:0	MISR_VAL	SW : RW MISR value

0x00AD0010 EBI1_CH0_LBST_COUNT_CA_ALL

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

This register displays the CA counter value. The counter counts number of all the looped-back commands burst. In SDR command mode, a burst equals to one DRAM command shots. In DDR mode, a burst equals to two DRAM command shots. The counter freezes at 0xFFFF.

EBI1_CH0_LBST_COUNT_CA_ALL

Bits	Name	Description
31:0	COUNT	SW : RW Counter value

0x00AD0014 EBI1_CH0_LBST_COUNT_CA_CMPR

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

This register displays the CA counter value. The counter counts number of all the looped-back commands burst that match the compare value and enable conditions. In SDR command mode, a burst equals to one DRAM command shots. In DDR mode, a burst equals to two DRAM command shots. The counter freezes at 0xFFFF.

EBI1_CH0_LBST_COUNT_CA_CMPR

Bits	Name	Description
31:0	COUNT	SW : R/W Counter value

0x00AD0018 EBI1_CH0_LBST_COUNT_DQ_ALL

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

This register displays the DQ counter value. The counter counts number of all the looped-back DQ data. One DQ data cycle equals to two DQ bursts. The counter freezes at 0xFFFF.

EBI1_CH0_LBST_COUNT_DQ_ALL

Bits	Name	Description
31:0	COUNT	SW : R/W Counter value

0x00AD001C EBI1_CH0_LBST_COUNT_DQ_CMPR

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

This register displays the DQ counter value. The counter counts number of all the looped-back DQ data cycle that are non-zero if the IGNORE_ZERO_DATA in LBST_CNTL is turned on. One DQ data cycle equals to two DQ bursts. The counter freezes at 0xFFFF.

EBI1_CH0_LBST_COUNT_DQ_CMPR

Bits	Name	Description
31:0	COUNT	SW : R/W Counter value

0x00AD0030 EBI1_CH0_LBST_CMPR_VAL_CA_EVEN

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

The command/address compare value for even address burst. If the looped-back CA match the compare value after the LBST_CMPR_EN_CA_EVEN is applied, the matching condition can be used to trigger read data generation. It will also increment the CA compare counter.

EBI1_CH0_LBST_CMPR_VAL_CA_EVEN

Bits	Name	Description
31:29	RESERVED_31_29	
28:8	CMPR_CA	SW : RW Compare value for command/address. Bit definition varies depending on the DRAM technologies.
7:6	CMPR_RESET_N	SW : RW Compare value for RESET_N of both ranks.
5:4	CMPR_CS_N	SW : RW Compare value for CS_N of both ranks.

EBI1_CH0_LBST_CMPR_VAL_CA_EVEN (cont.)

Bits	Name	Description
3:2	CMPR_CKE	SW : RW Compare value for CKE of both ranks.
1:0	CMPR_ODT	SW : RW Compare value for ODT of both ranks.

0x00AD0034 EBI1_CH0_LBST_CMPR_VAL_CA_ODD

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

The command/address compare value for odd address burst. If the looped-back CA match the compare value after the LBST_CMPR_EN_CA_ODD is applied, the matching condition can be used to trigger read data generation. It will also increment the CA compare counter.

EBI1_CH0_LBST_CMPR_VAL_CA_ODD

Bits	Name	Description
31:18	RESERVED_31_18	
17:8	CMPR_CA	SW : RW Compare value for odd command/address in LPDDR2 mode.
7:0	RESERVED_7_0	

0x00AD0038 EBI1_CH0_LBST_CMPR_EN_CA_EVEN

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

The command/address compare Enable for even address burst. The Enable bits of corresponding DRAM command/address bits match the definitions in LBST_CMPR_VAL_CA_EVEN.

EBI1_CH0_LBST_CMPR_EN_CA_EVEN

Bits	Name	Description
31	CMPR_NOT	SW : RW Inverse the compare condition so a match means NOT equal to the compare value and enable conditions.
30:29	RESERVED_30_29	

EBI1_CH0_LBST_CMPR_EN_CA_EVEN (cont.)

Bits	Name	Description
28:8	CMPR_EN_CA	SW : RW Enable bit for command/address compare. 0x0: don't care. 0x1: compare enabled.
7:0	CMPR_EN_CMD	SW : RW Enable bit for command compare. 0x0: don't care. 0x1: compare enabled.

0x00AD003C EBI1_CH0_LBST_CMPR_EN_CA_ODD

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

The command/address compare Enable for odd address burst. The Enable bits of corresponding DRAM command/address bits match the definitions in LBST_CMPR_VAL_CA_ODD.

EBI1_CH0_LBST_CMPR_EN_CA_ODD

Bits	Name	Description
31:18	RESERVED_31_18	
17:8	CMPR_EN_CA	SW : RW Enable bit for command/address compare. 0x0: don't care. 0x1: compare enabled.
7:0	RESERVED_7_0	

0x00AD0040 EBI1_CH0_LBST_CNTL2

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

LBST logic control register 2.

EBI1_CH0_LBST_CNTL2

Bits	Name	Description
31:2	RESERVED_31_2	

EBI1_CH0_LBST_CNTL2 (cont.)

Bits	Name	Description
1	IGNORE_DM	SW : RW When the loop-back data is written into MISR, This bit controls whether the DM bits are used to mask off the data (to force it to zero) or not. 0x0: consider DM bits. Zero the data only when DM is asserted 0x1: Ignore DM bits. Always take the data bit directly
0	MODE_SYNC_DRIVE_PRPG	SW : RW Controls the flop delay along the i_drive_prpg input path. 0x0: i_drive_prpg is feed into a DDR_1x demet directly 0x1: i_drive_prpg is going through 5-stage XO flops then goes to DDR_1x demet

13.3 EBI1 CH1 Registers (0x00D00000 EBI1_CH1_BASE)

This section contains the EBI1 CH1 registers.

The HSDDRx generation 5 memory controller core is an AXI r0p0+ slave that provides a high-performance, low-latency, 32-bit wide interface to LPDDR, LPDDR2, PCDDR2 or PCDDR3 memory.

This section describes the Configuration Status Registers which are available to software for configuring the HSDDRx memory controller core. The configuration registers in the core are organized into the following sub groups based on register functionality.

The access to configuration registers is performed via the AHB bus.

Table 13-4 HSDDRx Register Categories Grouped by Functionality

Function	Prefix	Address Bit (19:16)
Wrapper Configuration Registers	TOP	000x
AXI Performance Monitors	PMON_AXI	0010
DDR Performance Monitors	PMON_DDR	0011
AXI Configuration Registers	SLV	010x
MPU Configuration Registers	HSDDR_MPU	011x
DDRx Configuration Registers	DDR	10xx
LBST Configuration Registers	LBST	11xx

13.3.1 EBI1 CH1 HSDDRx Registers

13.3.1.1 Top-Level Wrapper Registers

0x00D00004 EBI1_CH1_TOP_MISC_CNTL

Type: Read/Write
Clock: CLK_XO
Reset State: 0x0004A0A8

Top level Miscellaneous Control register.

EBI1_CH1_TOP_MISC_CNTL

Bits	Name	Description
31:21	RESERVED_31_21	

EBI1_CH1_TOP_MISC_CNTL (cont.)

Bits	Name	Description
20	IOCAL_UPDATE_METHOD	SW : RW Specify a way to update command/address IO pads' PCNT/NCNT values. 0x0: Update when the bus is idle but CK could be running 0x1: Update when the memory is in self-refresh state and CK is not running
19:16	IOCAL_UPDATE_PULSE_WIDTH	SW : RW Number of DDR1X clock cycles for the pulse for IOCal updates. 0x0: reserved 0x1: 1 DDR 1x cycle 0x2: 2 DDR 1x cycles 0x3: 3 DDR 1x cycles 0x4: 4 DDR 1x cycles 0x5: 5 DDR 1x cycles 0x6: 6 DDR 1x cycles 0x7: 7 DDR 1x cycles 0x8: 8 DDR 1x cycles 0x9: 9 DDR 1x cycles 0xA: 10 DDR 1x cycles 0xB: 11 DDR 1x cycles 0xC: 12 DDR 1x cycles 0xD: 13 DDR 1x cycles 0xE: 14 DDR 1x cycles 0xF: 15 DDR 1x cycles
15	CLKON_DDR_PIPE_MANUAL	SW : RW Control pipeline DDR 1x on/off in clkon manual mode 0x0: Off 0x1: On
14	MODE_CLKON_DDR_PIPE	SW : RW Mode to control clkon for pipeline DDR 1X 0x0: controlled by CLKON_DDR_PIPE_MANUAL 0x1: controlled by internal logic
13	CLKON_DDR_2X_MANUAL	SW : RW Control clk_ddr_2x on/off in clkon manual mode 0x0: Off 0x1: On
12	MODE_CLKON_DDR_2X	SW : RW Mode to control clkon for clk_ddr_2x 0x0: controlled by CLKON_DDR_2X_MANUAL 0x1: controlled by internal logic
11	MODE_MEM_HALT	SW : RW Memory mode used when SW requests clock switching. 0x0: self-refresh mode 0x1: clock-stop/power-down mode

EBI1_CH1_TOP_MISC_CNTL (cont.)

Bits	Name	Description
10:8	TEST_CLK_SEL	SW : RW Test clock select: 0x0: no clock output_1 0x1: ddr_1x 0x2: clk_axi 0x3: clk_ahb 0x4: clk_xo 0x5: no clock output_2 0x6: dqs positive edge 0x7: dqs negative edge
7	CLKON_AHB_MANUAL	SW : RW Control clk_ddr on/off in clkon manual mode 0x0: Off 0x1: On
6	MODE_CLKON_AHB	SW : RW Mode to control clkon for clk_ahb 0x0: controlled by CLKON_AHB_MANUAL 0x1: controlled by internal logic
5	CLKON_DDR_1X_MANUAL	SW : RW Control clk_ddr on/off in clkon manual mode 0x0: Off 0x1: On
4	MODE_CLKON_DDR_1X	SW : RW Mode to control clkon for clk_ddr_1x 0x0: controlled by CLKON_DDR_1X_MANUAL 0x1: controlled by internal logic
3	CLKON_AXI_MANUAL	SW : RW Control clk_axi on/off in clkon manual mode 0x0: Off 0x1: On
2	MODE_CLKON_AXI	SW : RW Mode to control clkon for clk_axi 0x0: controlled by CLKON_AXI_MANUAL 0x1: controlled by internal logic
1:0	RESERVED_1_0	

13.3.1.2 Performance Monitor Registers

0x00D20000 EBI1_CH1_PMON_AXI_CNTL

Type: Read/Write
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Control register.

EBI1_CH1_PMON_AXI_CNTL

Bits	Name	Description
31:17	RESERVED_31_17	
16	INTERRUPT	SW : R 0x0: No interrupt 0x1: Interrupt occurred
15:3	RESERVED_15_3	
2	RESET_COUNTER	SW : W write to '1' resets all the counters
1	STOP_COUNTER	SW : W write to '1' causes all the counters stop counting
0	START_COUNTER	SW : W write to '1' causes all the counters start counting

0x00D20004 EBI1_CH1_PMON_AXI_INTERRUPT

Type: Read/Write
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Interrupt Event Counter register.

EBI1_CH1_PMON_AXI_INTERRUPT

Bits	Name	Description
31:0	INT_EVENT_CNT	SW : RW Number of counter 0 events that will trigger interrupt

0x00D20008 EBI1_CH1_PMON_AXI_SOURCE_0

Type: Read/Write
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Source Control register 0.

EBI1_CH1_PMON_AXI_SOURCE_0

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00D2000C EBI1_CH1_PMON_AXI_COUNT_0

Type: Read
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Count register 0.

EBI1_CH1_PMON_AXI_COUNT_0

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00D20010 EBI1_CH1_PMON_AXI_SOURCE_1

Type: Read/Write
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Source Control register 1.

EBI1_CH1_PMON_AXI_SOURCE_1

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00D20014 EBI1_CH1_PMON_AXI_COUNT_1

Type: Read
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Count register 1.

EBI1_CH1_PMON_AXI_COUNT_1

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00D20018 EBI1_CH1_PMON_AXI_SOURCE_2

Type: Read/Write
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Source Control register 2.

EBI1_CH1_PMON_AXI_SOURCE_2

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00D2001C EBI1_CH1_PMON_AXI_COUNT_2

Type: Read
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Count register 2.

EBI1_CH1_PMON_AXI_COUNT_2

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00D20020 EBI1_CH1_PMON_AXI_SOURCE_3

Type: Read/Write
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Source Control register 3.

EBI1_CH1_PMON_AXI_SOURCE_3

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00D20024 EBI1_CH1_PMON_AXI_COUNT_3

Type: Read
Clock: CLK_AXI
Reset State: 0x00000000

Performance Monitor Count register 3.

EBI1_CH1_PMON_AXI_COUNT_3

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00D30000 EBI1_CH1_PMON_DDR_CNTL

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Control register.

EBI1_CH1_PMON_DDR_CNTL

Bits	Name	Description
31:17	RESERVED_31_17	
16	INTERRUPT	SW : R 0x0: No interrupt 0x1: Interrupt occurred

EBI1_CH1_PMON_DDR_CNTL (cont.)

Bits	Name	Description
15:3	RESERVED_15_3	
2	RESET_COUNTER	SW : W write to '1' resets all the counters
1:0	RESERVED_1_0	

0x00D30004 EBI1_CH1_PMON_DDR_INTERRUPT

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Interrupt Event Counter register.

EBI1_CH1_PMON_DDR_INTERRUPT

Bits	Name	Description
31:0	INT_EVENT_CNT	SW : RW Number of counter 0 events that will trigger interrupt

0x00D30008 EBI1_CH1_PMON_DDR_SOURCE_0

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Source Control register 0.

EBI1_CH1_PMON_DDR_SOURCE_0

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00D3000C EBI1_CH1_PMON_DDR_COUNT_0

Type: Read
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Count register 0.

EBI1_CH1_PMON_DDR_COUNT_0

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00D30010 EBI1_CH1_PMON_DDR_SOURCE_1

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Source Control register 1.

EBI1_CH1_PMON_DDR_SOURCE_1

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00D30014 EBI1_CH1_PMON_DDR_COUNT_1

Type: Read
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Count register 1.

EBI1_CH1_PMON_DDR_COUNT_1

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00D30018 EBI1_CH1_PMON_DDR_SOURCE_2

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Source Control register 2.

EBI1_CH1_PMON_DDR_SOURCE_2

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00D3001C EBI1_CH1_PMON_DDR_COUNT_2

Type: Read
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Count register 2.

EBI1_CH1_PMON_DDR_COUNT_2

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

0x00D30020 EBI1_CH1_PMON_DDR_SOURCE_3

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Source Control register 3.

EBI1_CH1_PMON_DDR_SOURCE_3

Bits	Name	Description
31:4	RESERVED_31_4	
3:0	PMON_SOURCE	SW : RW Specify the source of the performance monitor counter

0x00D30024 EBI1_CH1_PMON_DDR_COUNT_3

Type: Read
Clock: CLK_DDR_1X
Reset State: 0x00000000

Performance Monitor Count register 3.

EBI1_CH1_PMON_DDR_COUNT_3

Bits	Name	Description
31:0	PMON_COUNT	SW : R Contains the current counter value

13.3.1.3 AXI Slave Registers

0x00D40000 EBI1_CH1_SLV_CONFIG

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x80400003

AXI Slave Configuration Register.

This register defines the core interface configuration and memory controller clocking modes.

EBI1_CH1_SLV_CONFIG

Bits	Name	Description
31	CLKON_DISABLE	The slave logic's AXI CLKON signal will be de-asserted when the slave is idle and no data remains in the write data or command buffer. Additionally, AXI_AREADY and AXI_WREADY will be de-asserted when AXI CLKON is de-asserted. The AXI CLKON signal from the slave logic will be constantly driven to 1 and AXI_AREADY and AXI_WREADY will never be de-asserted due to de-asserting the AXI CLKON. 0x0: Disable 0x1: Enable
30:26	RESERVED_30_26	Reserved
25:16	CLKON_IDLE_TIMER	The number of AXI clock cycles that AXI CLKON will remain high after the slave is idle and the write data and command buffers are empty. 0x0: Reserved
15:14	RESERVED_15_14	Reserved
13:12	INTERLEAVE	Defines the way that bus system slave reconstructs the system address for MPU, error capture. 0x0: Disabled 0x1: Done at 1K Granularity 0x2: Done at 2K Granularity 0x3: Done at 4K Granularity
11:10	RESERVED_11_10	Reserved

EBI1_CH1_SLV_CONFIG (cont.)

Bits	Name	Description
9:8	CMD_ORDERING	Defines command reordering strategy (Based on the OOORD signal. OOOWT is not used since all buffered responses are returned immediately. Potentially lower power, higher average latency.) (All transactions from a particular master will be executed in time order. Reordering can occur between masters. Potentially more power, lower average latency.) (All transactions will be executed in time order, independent of the master association.) 0x0: reordering (default) 0x1: in-order per master 0x2: in-order globally 0x3: Reserved
7:3	RESERVED_7_3	RFU
2:0	CMD_Q_DEPTH	Defines number of outstanding requests that may be queued up for processing 0x0: 1 0x1: 2 0x2: 3 0x3: 4 0x4: 5 0x5: 6 0x6: 7 0x7: 8

0x00D40004 EBI1_CH1_SLV_RD_CONFIG

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x000B000F

Read Buffer Configuration Register

EBI1_CH1_SLV_RD_CONFIG

Bits	Name	Description
31:22	RESERVED_31_22	RFU
21:16	RD_CMD_FIFO_DEPTH	Sets the maximum number of read command FIFO entries that may be used at any time. The AXI slave will use at most RD_CMD_FIFO_DEPTH + 1 entires. For example setting this field to 0x0F allows all 16 entires of the buffer to be used.
15:6	RESERVED_15_6	RFU

EBI1_CH1_SLV_RD_CONFIG (cont.)

Bits	Name	Description
5:0	RD_DATA_FIFO_DEPTH	Sets the maximum number of 64 bit Read Buffer entries that may be used at any time. The Read Buffer will use at most RD_FIFO_DEPTH + 1 entires. For example setting this field to 0x3F allows all 64 entires of the buffer to be used. Must not be less than 0xF.

0x00D40008 EBI1_CH1_SLV_RD_STATUS

Type: Read
Clock: AXI_CLK
Reset State: 0x0000FF00

EBI1_CH1_SLV_RD_STATUS

Bits	Name	Description
31:28	RESERVED_31_28	RFU
27:24	RDQUAL_FIFO_ENTRIES_IN_USE	The number of read qualifier FIFO entries that have been reserved for use by reads commands sent to the DDR controller.
23:16	RDDATA_FIFO_ENTRIES_IN_USE	The number of read data FIFO entries that have been reserved for use by reads commands sent to the DDR controller.
15:8	RDDATA_FIFO_EMPTY	The empty status of each of the read data FIFOs. Bit 8 corresponds to the positive-edge dq[0] FIFO. Bit 9corresponds to the positive-edge dq[1] FIFO. Bit 10corresponds to the positive-edge dq[2] FIFO. Bit 11corresponds to the positive-edge dq[3] FIFO. Bit 12corresponds to the negative-edge dq[0] FIFO. Bit 13corresponds to the negative-edge dq[1] FIFO. Bit 14corresponds to the negative-edge dq[2] FIFO. Bit 15corresponds to the negative-edge dq[3] FIFO
7:1	RESERVED_7_1	RFU
0	DQS_ERROR	Set by the hardware if the read data FIFOs have been non-empty while no read commands where outstanding since reset. This bit being set is a strong indication of a spurious DQS edge.

0x00D4000C EBI1_CH1_SLV_WR_CONFIG

Type: Read/Write
Clock: AXI_CLK
Reset State: 0xD70F040F

Write Buffer Configuration Register

The write coalescing buffer is part of the write data path and cannot be completely disabled. However, all read merging and all write coalescing across bursts can be disabled via the SLV_WR_CONFIG register. Beats within narrow (each beat transfers less than the bus width) bursts may be coalesced in any configuration.

EBI1_CH1_SLV_WR_CONFIG

Bits	Name	Description
31	COALESCE_EN	Enable write coalescing. When enabled, data from separate AXI bursts will coalesced. Packing of narrow beats from a single burst is always allowed. 0x0: Disable 0x1: Enable
30	READ_MERGE_EN	Enable read merging with Write Coalescing buffer data. When disabled reads are not executed while the required data is in the write buffer. Also, the Write Buffer is flushed after each burst. 0x0: Disable 0x1: Enable
29	FLUSH	When set to 1, the hardware will flush the Write Coalescing Buffer. Hardware will clear this bit when the requested flush is complete.
28	EMPTY	1 when any valid data exists in the Write Coalescing Buffer. Read-only to software.
27	WRITE_BLOCK_READ	When set, no read command is allowed to execute while there is any write data in the buffer or there are any write commands in the write command buffer. When the Read Command Buffer is limited to one command, read merging is disabled and write coalescing is disabled and this bit is set, the DDR controller will execute commands in the order in which they were received on the AXI bus.
26:24	CMD_BUF_DEPTH	
23:21	RESERVED_23_21	RFU
20:16	FLUSH_UPPER_LIMIT	The flush high water mark. Flushing will begin when the number of valid lines in the Write Coalescing Buffer is greater than FLUSH_UPPER_LIMIT. FLUSH_UPPER_LIMIT must be less than or equal to the number of lines specified in WR_BUFFER_DEPTH. Also, FLUSH_UPPER_LIMIT must be greater than FLUSH_LOWER_LIMIT.
15:13	RESERVED_15_13	RFU
12:8	FLUSH_LOWER_LIMIT	The flush low water mark. Once flushing has begun, lines will be flushed until the number of valid lines is less than or equal to FLUSH_LOWER_LIMIT.
7:5	RESERVED_7_5	RFU
4:0	WR_BUFFER_DEPTH	Sets the maximum number of Write Coalescing Buffer lines that may be used at any time. The Write Coalesing Buffer will use at most WR_BUFFER_DEPTH + 1 entires. For example setting this field to 0xF allows 16 entires of the buffer to be used. Must not be less than 0x5.

0x00D40010 EBI1_CH1_SLV_FLUSH_CONFIG

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x8000800F

Write Buffer Flush Configuration Register

EBI1_CH1_SLV_FLUSH_CONFIG

Bits	Name	Description
31:30	FLUSH_PRIORITY	When the high water mark (see SLV_WR_CONFIG) has been reached, flush the lines with a priority of FLUSH_PRIORITY.
29	RESERVED_29	RFU
28	FLUSH_IN_ORDER	Write Coalescing Buffer lines are flushed in the order in which they were created
27:18	RESERVED_27_18	RFU
17:8	FLUSH_IDLE_DELAY	After the controller is idle for FLUSH_IDLE_DELAY AXI cycles, the Write Buffer will be flushed.
7:0	PAGE_HIT_WINDOW	If the last line was flushed less than PAGE_HIT_WINDOW AXI cycles ago, lines within the same page as the last victim are preferred. Otherwise, lines are flushed oldest to youngest.

0x00D40014 EBI1_CH1_SLV_ID_REVISION

Type: Read
Clock: AXI_CLK
Reset State: 0x00005310

Revision ID Register

This register contains the revision numbers of DDR controller core.

EBI1_CH1_SLV_ID_REVISION

Bits	Name	Description
31:16	RESERVED_31_16	
15:12	REV_MAJOR	Major Revision
11:8	REV_MINOR	Minor Revision
7:4	SITE_ID	Site ID 0x1: RTP
3:0	RESERVED_3_0	

0x00D40020+4*n EBI1_CH1_SLV_ADDR_BASE_CSn, n=[0..1]

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000000

System Base Address Register for n

This register defines the base address for the memory that associates to chip select n.

When using ADDR_MAP_MODE == 2'b10 (see SLV_ADDR_MAP_CSn), the base address must be the base address of the entire space allocated to the controller.

EBI1_CH1_SLV_ADDR_BASE_CSn

Bits	Name	Description
31:16	RESERVED_31_16	
15:8	BASE_ADDR	Defines the Base Address decode, in conjunction with the SLV_ADDR_MAP_CSn, to determine the address space of the targeted chip select. The Base Address is compared to the AXI address bus bits [31:24]. If the portions of the two addresses match, then the particular CS is accessed.
7:0	RESERVED_7_0	RFU

0x00D40030+4*n EBI1_CH1_SLV_ADDR_MAP_CSn, n=[0..1]

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000100

System Address Mapping Register for Rank n.

This register defines the way to map AXI system address into rank/bank/row/column address to memory devices. Once the number of bank, row size and column size are defined, the memory size of the associated rank is defined.

NOTE When ADDR_MAP_MODE is set to 2'b10 and the controller both ranks must be programmed identically with respect to the SLV_ADDR_BASE_CSn, SLV_ADDR_MAP_CSn and SLV_ADDR_SIZE_MASK_CSn registers.

EBI1_CH1_SLV_ADDR_MAP_CSn

Bits	Name	Description
31:16	RESERVED_31_16	

EBI1_CH1_SLV_ADDR_MAP_CSn (cont.)

Bits	Name	Description
15	RANK_EN	Rank has memory devices attached 0x0: Rank not present (default) 0x1: Rank is present
14	RESERVED_14	RFU
13:12	ADDR_MAP_MODE	Addressing Mode Configuration. Selects the Addressing Mode of the Rank and determines the mapping of the System Address to the Memory Address. Configuring the AddrMode for "Rank,Bank, Row, Column" mode will map the system address in manner that is compatible with the Partial Array Self-Refresh Mechanism. The Partial Array Self-Refresh Mechanism is not supported unless AddrMode is configured for "Rank,Bank,Row,Column" mode. Mapping mode 10 (Row, Bank, Rank, Column) requires that the memory device on each rank has the same row, bank and column width and that SLV_ADDR_BASE_CSn, SLV_ADDR_SIZE_MASK_CSn and SLV_ADDR_MAP_CSn are programmed identically for each rank. Those registers are programmed as normal, according to the device parameters. 0x0: Rank, Row, Bank, Column (default) 0x1: Rank, Bank, Row, Column 0x2: Row, Bank, Rank, Column 0x3: Reserved
11:9	RESERVED_11_9	RFU
8	NUM_BANK	Specifies the number of banks in the memory device. 0x0: 4 banks 0x1: 8 banks (default)
7:6	RESERVED_7_6	RFU
5:4	WIDTH_ROW	Specifies the number of bits used for the row address of the external memory 0x0: 12 bits (default) 0x1: 13 bits 0x2: 14 bits 0x3: 15 bits
3:2	RESERVED_3_2	RFU
1:0	WIDTH_COL	Specifies the number of bits used for the column address of the external memory 0x0: 8 bits (default) 0x1: 9 bits 0x2: 10 bits 0x3: 11 bits

0x00D40040+4*n EBI1_CH1_SLV_ADDR_SIZE_MASK_CSn, n=[0..1]

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000000

System Address Size Mask Register for Rank n

This register defines the memory capacity of memory that associates to chip select n.

EBI1_CH1_SLV_ADDR_SIZE_MASK_CSn

Bits	Name	Description
31:16	RESERVED_31_16	
15:8	ADDR_MASK	Define the address size mask bits: 0x0: reserved 0x80: 2GB 0xC0: 1GB 0xE0: 512MB 0xF0: 256MB 0xF8: 128MB 0xFC: 64MB 0xFE: 32MB 0xFF: 16MB
7:0	RESERVED_7_0	RFU

0x00D40050 EBI1_CH1_SLV_STALL

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000004

SMI/EBI1 Stall Request and Status Register.

This register provides a mechanism to stall the AXI traffic and drain the internal request queues for the memory controller.

EBI1_CH1_SLV_STALL

Bits	Name	Description
31:3	RESERVED_31_3	
2	AXI_IDLE	The value of the o_axi_idle pin. This is only an indication that all read, write and QoS responses have been sent. It does, by itself, guarantee that the controller has completed all transactions.

EBI1_CH1_SLV_STALL (cont.)

Bits	Name	Description
1	STALL_ACK	SMI/EBI1 Stall Request Status: (After a valid STALL_REQ is asserted, this bit will be set to 1'b1 when AXI interface is stalled and all internal memory commands are executed. No further read/write commands will be sent to memory.) 0x0: normal operation (default) 0x1: AXI stalled and cmd q empty
0	STALL_REQ	SMI/EBI1 Stall Request: (Setting this bit to 1'b1 will stall all AXI traffic. axi_aready and axi_wready will be de-asserted and all AXI requests will NOT be accepted. Previously accepted DDR memory requests will continued be serviced. Setting this bit to 1'b0 will make the controller accept the new AXI requests. This mechanism can be used whenever software needs to switch the voltage or clock frequency of the controller.) 0x0: normal operation (default) 0x1: stall AXI traffic

0x00D40100 EBI1_CH1_SLV_ERR_ADDR

Type: Read
Clock: AXI_CLK
Reset State: 0x00000000

Slave Error Address Register.

This register contains the address of the request that caused the decode or MPU error. The error address is locked with the first error address.

EBI1_CH1_SLV_ERR_ADDR

Bits	Name	Description
31:0	ERR_ADDR	The address of the request that caused the bus error

0x00D40108 EBI1_CH1_SLV_ERR_APACKET_0

Type: Read
Clock: AXI_CLK
Reset State: 0x0000

Slave Error Address Attributes Register 0.

This register provides various information about the request that caused the AXI bus error.

EBI1_CH1_SLV_ERR_APACKET_0

Bits	Name	Description
31:16	RESERVED_31_16	RFU
15:0	ERR_AMID	The master ID of the request that caused the bus error.

0x00D4010C EBI1_CH1_SLV_ERR_APACKET_1

Type: Read
Clock: AXI_CLK
Reset State: 0x00000000

Slave Error Address Attributes Register 1.

This register provides various information about the request that caused the AXI bus error.

EBI1_CH1_SLV_ERR_APACKET_1

Bits	Name	Description
31:28	RESERVED_31_28	RFU
27:24	ERR_ALEN	The burst length of the request that caused bus error
23:16	ERR_ATID	The transfer ID of the request that caused the bus error.
15:13	ERR_ASIZE	The ASIZE of the request that caused the bus error 0x0: byte 0x1: half_word 0x2: word 0x3: double_word 0x4: Reserved_4 0x5: Reserved_5 0x6: Reserved_6 0x7: Reserved_7
12	ERR_ABURST	The ABURST of the request that caused the bus error 0x0: wrap 0x1: increment

EBI1_CH1_SLV_ERR_APACKET_1 (cont.)

Bits	Name	Description
11:8	ERR_ATYPE	The ATYPE of the request that caused the bus error Strongly-ordered and weakly-ordered concatenated with the integer. 0x0: strongly_ordered_0 0x1: strongly_ordered_1 0x2: weakly_ordered_2 0x3: weakly_ordered_3 0x4: weakly_ordered_4 0x5: weakly_ordered_5 0x6: weakly_ordered_6 0x7: weakly_ordered_7 0x8: strongly_ordered_8 0x9: strongly_ordered_9 0xA: weakly_ordered_A 0xB: weakly_ordered_B 0xC: weakly_ordered_C 0xD: weakly_ordered_D 0xE: weakly_ordered_E 0xF: weakly_ordered_F
7:6	ERR_ALOCK	The ALOCK of the request that caused the bus error 0x0: normal 0x1: exclusive 0x2: locked 0x3: barrier
5:4	RESERVED_5_4	Reserved
3	ERR_APROTNS	The APROTNS of the request that caused the bus error. 0x0: secure 0x1: non secure
2	ERR_AOOORD	The AOOORD of the request that caused the bus error 0x0: in order 0x1: out of order
1	ERR_AOOOWR	The AOOOWR of the request that caused the bus error 0x0: in order 0x1: out of order
0	ERR_AWRITE	The awrite of the request that caused bus error 0x0: read 0x1: write

0x00D40114 EBI1_CH1_SLV_ERR_CNTL

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00001000

Slave Error Code Register.

This register provides additional data about the bus error. Additionally, each slave which is capable of detecting an error is also required to have a single programmable register that can be used to optionally interrupt the processor core. This interrupt mechanism is required since write transfers may be posted on the bus and the AXI transfer may complete prior to the occurrence of the error in the AXI interconnect or slave device. The interrupt from the AXI interconnect and the AXI slave devices will be directed to the interrupt controller.

EBI1_CH1_SLV_ERR_CNTL

Bits	Name	Description
31:16	RESERVED_31_16	
15:13	RESERVED_15_13	
12	IRQ_EN	Mask off the bus error interrupt to processor 0x0: disables IRQ 0x1: enables IRQ (default)
11:9	RESERVED_11_9	
8	CLEAR_ERR	Clear error status bit Writing a '1' to this bit will clear the ERR_OCCURRED bit in this register. It will NOT clear other error registers. 0x0: no clear (default) 0x1: clear
7:5	RESERVED_7_5	
4	ERR_OCCURRED	Error Status bit to indicate that an error has occurred. This bit can be set by software. To clear this bit a '1' must be written to the CLEAR_ERR field. Writing a '0' to this field has no effect. 0x0: no error occurred 0x1: error occurred
3:2	RESERVED_3_2	
1:0	ERR_CODE	MPU error and address decode error: Writes to this field are ignored. 0x0: no error (default) 0x1: address decode error 0x2: mpu error 0x3: both

0x00D40200 EBI1_CH1_SLV_PMON_CFG_ACHAN

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000000

AXI Slave Performance Monitors

Table 13-5 AXI Slave Performance Monitor event index

Index	Description
0	AXI cycles
1	AXI address channel commands accepted
2	AXI address channel commands matching the attribute in SLV_PMON_CFG_ACHAN
3	High priority AXI address channel commands accepted
4	Number of AXI cycles in which the number of reserved global monitors is greater than or equal to SLV_PMON_CFG_0[N_MONITORS]
5	Number of AXI cycles in which the number of read commands in the read command buffer is greater than or equal to SLV_PMON_CFG_0[N_RD_CMDS]
6	Number of AXI cycles in which the number of write commands in the write command buffer is greater than or equal to SLV_PMON_CFG_0[N_WR_CMDS]
7	Number of AXI cycles in which the number of reserved read data FIFO entires is greater than or equal to SLV_PMON_CFG_0[N_RD_DATA_ENTRIES]
8	Number of AXI cycles in which the number of reserved read qualifier FIFO entires is greater than or equal to SLV_PMON_CFG_0[N_RD_QUAL_ENTRIES]
9	Number of AXI cycles in which the number of valid write data buffer lines is greater than or equal to SLV_PMON_CFG_0[N_WR_DATA]
10	The number of read commands that fully or partially hit in the write buffer
11	The number of write commands that fully or partially hit in the write buffer
12	TBD - Hazards

AXI Performance Monitor event index 2 records the number of address channel requests that match the following fields. The fields can be independently enabled/disabled with the MATCH_* fields in SLV_PMON_CFG_0. When an address channel request is accepted from the bus its attributes are compared to the fields of this register. If all enabled fields in SLV_PMON_CFG_ACHAN (see SLV_PMON_CFG_0) match the address channel request, the performance monitor is incremented. Any disabled fields match all transactions.

EBI1_CH1_SLV_PMON_CFG_ACHAN

Bits	Name	Description
31:16	AMID	AMID field of transactions to be counted with performance monitor index 2.
15:13	RESERVED_15_13	RFU
12:8	ATID	ATID field of transactions to be counted with performance monitor index 2.

EBI1_CH1_SLV_PMON_CFG_ACHAN (cont.)

Bits	Name	Description
7	RESERVED_7	RFU
6:4	ASIZE	ASIZE field of transactions to be counted with performance monitor index 2.
3:0	ALEN	ALEN field of transactions to be counted with performance monitor index 2.

0x00D40204 EBI1_CH1_SLV_PMON_CFG_0

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000000

EBI1_CH1_SLV_PMON_CFG_0

Bits	Name	Description
31	MATCH_AMID	Enable AMID matching for event index 2. When disabled, all AMIDs are considered a match.
30	MATCH_ATID	Enable ATID matching for event index 2. When disabled, all ATIDs are considered a match.
29	MATCH_ASIZE	Enable ASIZE matching for event index 2. When disabled, all ASIZEs are considered a match.
28	MATCH_ALEN	Enable ALEN matching for event index 2. When disabled, all ALENs are considered a match.
27:23	N_WR_DATA	See Table 1-3.
22:19	N_WR_CMDS	See Table 1-3.
18:14	N_RD_QUAL_ENTRIES	See Table 1-3.
13:7	N_RD_DATA_ENTRIES	See Table 1-3.
6:3	N_RD_CMDS	See Table 1-3.
2:0	N_MONITORS	See Table 1-3.

0x00D40208 EBI1_CH1_SLV_TEST_CONFIG

Type: Read/Write
Clock: AXI_CLK
Reset State: 0x00000000

EBI1_CH1_SLV_TEST_CONFIG

Bits	Name	Description
31:8	RESERVED_31_8	RFU
7:4	SELECT	Selects the AXI slave internal signal to drive out on the AXI test bus. All other values will result in undefined behavior. 0x0: test_bus_0 0x1: test_bus_1 0x2: test_bus_2 0x3: test_bus_3 0x4: test_bus_4 0x5: test_bus_5 0x6: test_bus_6
3:1	RESERVED_3_1	RFU
0	ENABLE	Enable the slave's test bus.

13.3.1.4 MPU Configuration Registers

0x00D60000+ 4*n EBI1_CH1_MPU_PRTn_RACR, n=[0..15]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU. These registers include a single bit per VMID granting read access

EBI1_CH1_MPU_PRTn_RACR

Bits	Name	Description
31:0	RE	Read enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read access to the registers in the associated resource group.

0x00D60400+ 4*n EBI1_CH1_MPU_PRTn_WACR, n=[0..15]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

These registers exist only for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU.

EBI1_CH1_MPU_PRTn_WACR

Bits	Name	Description
31:0	WE	Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID write access to the registers in the associated resource group.

0x00D60800+4*n EBI1_CH1_MPU_PRTn_START, n=[0..15]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition Start Address Register. This register contains the start address of the partition. Only the bit numbers indicated by MPU_IDR[MSb] through MPU_IDR[LSb] are valid and physically exist.

EBI1_CH1_MPU_PRTn_START

Bits	Name	Description
31:12	ADDR	MPU Partition Start Address
11:0	RESERVED_11_0	Reserved

0x00D60C00+4*n EBI1_CH1_MPU_PRTn_END, n=[0..15]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition End Address Register. This register contains the start address of the partition.Only the bit numbers indicated by MPU_IDR[MSB] through MPU_IDR[LSB] are valid and physically exist.

EBI1_CH1_MPU_PRTn_END

Bits	Name	Description
31:12	ADDR	MPU Partition End Address
11:0	RESERVED_11_0	Reserved

0x00D60F80 EBI1_CH1_MPU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Configuration Register: This register includes fields governing various MPU behaviors.

EBI1_CH1_MPU_CR

Bits	Name	Description
31:2	RESERVED31_2	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set MPU_ESR. MPU_EAR and MPU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set MPU_ESR. MPU_EAR and MPU_ESYNR0 updated with address and syndrome of error.
2	MPUEIE	MPU Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the MPU. Interrupt output is asserted if MPU_CR[MPUEIE] = 1 and any bit is set in MPU_ESR.
1	MPUERE	MPU Error Report Enable. MPUERE = 0 causes the MPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master. MPUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective MPU port. Errors from either port are terminated by the MPU as RAZ/WI Both client and configuration port errors are recorded in MPU_ESR, independent of the value of MPU_CR[MPUERE]
0	MPUE	MPU Enable. Governs whether MPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures MPU and the MID to VMID mapping tables.

0x00D60F84 EBI1_CH1_MPU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the MPU, for both the client port and the configuration port.

EBI1_CH1_MPU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x00D60F88 EBI1_CH1_MPU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the MPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the MPU's interrupt output (when enabled by MPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the MPU_ESYNRn registers, which are merely the "syndrome" of an error indicated by MPU_ESR.

EBI1_CH1_MPU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x00D60F8C EBI1_CH1_MPU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Restore Register. This register is an aliased address for the MPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

EBI1_CH1_MPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x00D60F90 EBI1_CH1_MPU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

EBI1_CH1_MPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x00D60F94 EBI1_CH1_MPU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

EBI1_CH1_MPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x00D60FF4 EBI1_CH1_MPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

MPU Revision Register: This register provides major/minor revision codes for the implementation.

EBI1_CH1_MPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x00D60FF8 EBI1_CH1_MPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x1F0C2C0F

MPU ID Register: Read-only register that defines various configuration attributes of the MPU instance.

EBI1_CH1_MPU_IDR

Bits	Name	Description
31:29	RESERVED31_29	Reserved
28:24	MSB	Indicates most significant address bit number used in START/END address comparisons.
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used in START/END address comparisons.
15:14	RESERVED15_12	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only MPU_PRTn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate MPU_PRTn_RACR and MPU_PRTn_WACR registers govern read vs. write access. For single VMID, MPU_PRTn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields

EBI1_CH1_MPU_IDR (cont.)

Bits	Name	Description
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. MPU_PRTn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMD type access control. MPU_PRTn_xACR registers include separate bit per VMID (32 bits) for governing access.
9:8	RESERVED9_8	Reserved
7:0	NPRT	Number of partitions. Indicates the number of partitions (minus 1) supported by the MPU. Values range from 0-223 (1-224 partitions)

0x00D60FFC EBI1_CH1_MPU_MPU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

MPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the MPU (including the MPU_MPU_ACR itself).

EBI1_CH1_MPU_MPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the MPU's 4KB address region (including the MPU_MPU_ACR itself). For single VMID type MPUs (MPU_IDR[MV] = 0) the MPU_MPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

13.3.1.5 DDR Configuration Registers

0x00D80000 EBI1_CH1_DDR_DEVICE_CONFIG

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Memory Configuration Register.

The register is used to set up DRAM configuration in the DDR controller

EBI1_CH1_DDR_DEVICE_CONFIG

Bits	Name	Description
31:28	RESERVED_31_28	
27:26	DEVICE_CONFIG_RANK1	SW: RW, HW: R Device Configuration for Rank 1. This is required for SRR in order to update the refresh rate correctly if multiple devices are involved. 0x0: reserved (default) 0x1: x8,x8,x8,x8 0x2: x16, x16 0x3: x32
25:24	DEVICE_CONFIG_RANK0	SW: RW, HW: R Device Configuration for Rank 0. This is required for SRR in order to update the refresh rate correctly if multiple devices are involved. 0x0: reserved (default) 0x1: x8,x8,x8,x8 0x2: x16, x16 0x3: x32
23:18	RESERVED_23_18	
17	INIT_DONE_RANK1	SW: RW, HW: R DDR Software initialization Complete SW writes this bit after initialization is complete for rank 1. 0x0: init incomplete (default) 0x1: init complete
16	INIT_DONE_RANK0	SW: RW, HW: R DDR Software initialization Complete SW writes this bit after initialization is complete for rank 0. 0x0: init incomplete (default) 0x1: init complete
15:14	NUM_BANKS	SW: RW, HW: R Indicates number of banks of the SDRAM device. Typically, LPDDR1 devices are 4 bank only, LPDDR2 & PCDDR2 devices can be 4 or 8 bank while PCDDR3 devices are 8 bank only. 0x0: 4 (default) 0x1: 8 0x2: Reserved_1 0x3: Reserved_2
13:12	RESERVED_13_12	

EBI1_CH1_DDR_DEVICE_CONFIG (cont.)

Bits	Name	Description
11:10	CLK_SYNC_MODE	SW: R, HW: RW DDR clocked programmed by SW. Read Only. 0x0: Asynchronous (default) 0x1: Synchronous 0x2: Iso Synchronous 0x3: Reserved
9:7	DEVICE_TYPE	SW: RW, HW: None Specify DRAM Device Type. 0x0: LPDDR (default) 0x1: LPDDR2-S2 0x2: LPDDR2-S4 0x3: PCDDR2 0x4: PCDDR3 0x5: Reserved_1 0x6: Reserved_2 0x7: Reserved_3
6	RESERVED_6	
5	MEM_CLK_CONFIG	SW: RW, HW: R Rank Clock Configuration: Note that the initialization of the individual memory ranks is otherwise unchanged when using this feature. 0x0: CK0 drives both Rank 0 and 1 (default) 0x1: CK0 for Rank0 and CK1 for Rank1
4	DDR_COMMAND_BUS	SW: RW, HW: R Specify if DDR needs to be used on the command bus (in addition to the data bus). This needs to be enabled LPDDR2 SDRAM devices & disabled for others. 0x0: Disable (default) 0x1: Enable
3:2	RESERVED_3_2	
1	RANK1_EN	SW: RW, HW: R Rank 1 is present 0x0: Rank not present (default) 0x1: Rank is present
0	RANK0_EN	SW: RW, HW: R Rank 0 is present. 0x0: Rank not present (default) 0x1: Rank is present

0x00D80004 EBI1_CH1_DDR_DEVICE_STATUS

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Device Status Register

This register enables software to read memory device status.

EBI1_CH1_DDR_DEVICE_STATUS

Bits	Name	Description
31:18	RESERVED_31_18	
17	INTERRUPT_EN	SW: RW, HW: R Interrupt will be generated if temperature out-of-range is detected i.e RANK0/1_TEMP_OO_RANGE is set. The interrupt will be set (sticky behavior) until SW can clear it by clearing the RANK0/1_TEMP_OO_RANGE field. The temperature out of range is due to SRR which is a feature only available in LPDDR1/LPDDR2 devices. 0x0: Disable (default) 0x1: Enable
16	CURR_SEL_REG_FREQ_SWITCH	SW: R, HW: W Indicates which DDR timing register set is being currently used. If DDR_CMD_EXEC_OPT_2[UPDATE_MEM_LATENCY_ON_FREQ_SWITCH] is set, then certain CSR fields in DDR_DRAM_TIMING_6 and DDR_CMD_EXEC_OPT_3 are also shadowed. 0x0: DDR_DRAM_TIMING CSRs (default) 0x1: DDR_DRAM_TIMING_ALT CSRs
15:14	RESERVED_15_14	
13	IN_DEEP_POWER_DOWN_RANK1	SW: R, HW: W Indicates the rank 1 is currently in deep power down mode. Deep power down feature is only available in LPDDR1/LPDDR2 devices. 0x0: Not in deep power down (default) 0x1: in deep power down
12	IN_DEEP_POWER_DOWN_RANK0	SW: R, HW: W Indicates the rank 0 is currently in deep power down mode. Deep power down feature is only available in LPDDR1/LPDDR2 devices. 0x0: Not in deep power down (default) 0x1: in deep power down
11:10	RESERVED_11_10	
9	IN_SELF_RFSH_RANK1	SW: R, HW: W Indicates the rank 1 is currently in self-refresh mode 0x0: Not in self-refresh (default) 0x1: in self-refresh

EBI1_CH1_DDR_DEVICE_STATUS (cont.)

Bits	Name	Description
8	IN_SELF_RFSH_RANK0	SW: R, HW: W Indicates the rank 0 is currently in self-refresh mode 0x0: Not in self-refresh (default) 0x1: in self-refresh
7:6	RESERVED_7_6	
5	RANK1_TEMP_OO_RANGE	SW: RW, HW: W Indicates any out-of-range operating temperature for Rank1 This bit is set to '1' if the SRR read returns a temperature reading that is out of range on the high side. This bit is sticky and can only be cleared by software write. The temperature out of range is due to SRR which is a feature only available in LPDDR1/LPDDR2 devices. 0x0: Within range (default) 0x1: Out of range
4	RANK0_TEMP_OO_RANGE	SW: RW, HW: W Indicates any out-of-range operating temperature for Rank0 This bit is set to '1' if the SRR read returns a temperature reading that is out of range on the high side. This bit is sticky and can only be cleared by software write. The temperature out of range is due to SRR which is a feature only available in LPDDR1/LPDDR2 devices. 0x0: Within range (default) 0x1: Out of range
3:2	RESERVED_3_2	
1	RANK1_IDLE	SW: R, HW: W Rank1 Idle Status. If set, it indicates that there are no transactions to that rank and also indicates that the timing parametes have been satisfied such that if the pages are open, they could be closed. 0x0: Rank Busy (default) 0x1: Rank Idle
0	RANK0_IDLE	SW: R, HW: W Rank0 Idle Status. If set, it indicates that there are no transactions to that rank and also indicates that the timing parameter have been satisfied such that if the pages are open, they could be closed. 0x0: Rank Busy (default) 0x1: Rank Idle

0x00D80010 EBI1_CH1_DDR_MANUAL_CMD

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Manual Command Register

This register enables the software to manually issue commands to DDR SDRAM interface. A value of '1' should be written in the bit field of the command that the software wants to force the controller to perform. (This includes the MRR and MRW bits of the DDR_MR_CNTL_WDATA CSR) Only one bit should be active at any given time, except for the "external clock on", the "reset_n" bit and the "CKE" bit. When the controller has finished executing the command, it will clear the bit (including the MRR, MRW and the RD_DQCAL bits of the DDR_MR_CNTL_WDATA CSR), except for the external clock on bit, the "CKE" bit and the "reset_n" bits. It is the software's responsibility to ensure all timing parameters are satisfied before executing the next manual command before the rank is initialized. Once the rank is initialized, it is HW's responsibility to execute the command when possible. The AUTO_REFRESH and PRECHARGE_ALL commands are not to be used after the rank has been initialized.

Once these bits are set, HW can potentially delay executing the command in order to ensure that the memory timings have been satisfied. (This statement is only applicable after the rank is initialized)

The initialization sequence of the SDRAM device is executed by SW via this register and the DDR_MR_CNTL_WDATA CSR.

EBI1_CH1_DDR_MANUAL_CMD

Bits	Name	Description
31:18	RESERVED_31_18	
17:16	RANK_SEL	SW: RW, HW: R Select which chip select should be targeted for the chosen manual command to be executed. 0x0: Invalid (default) 0x1: CS0 only 0x2: CS1 only 0x3: both CS0 CS1
15	RESERVED_15	
14	CK_ON	SW: RW, HW: R Turns on/off external clock CK, CKN. This bit does not reset automatically. Software must turn it on when the clock to the device needs to be enabled and keep it on.Unitl the rank is initialized, HW would control the clocks based on this setting. 0x0: Off (default) 0x1: On
13	CKE	SW: RW, HW: R Turns on/off clock enable CKE. This bit does not reset automatically. Software must turn it on when the clock to the device needs to be enabled and keep it on.Unitl the rank is initialized, HW would control the CKE based on this setting. 0x0: Off (default) 0x1: On

EBI1_CH1_DDR_MANUAL_CMD (cont.)

Bits	Name	Description
12	RESET_N	SW: RW, HW: R Turns on/off reset pin to PCDDR3 device only. This bit does not reset automatically. Software must turn it on, then turn it off 0x0: Active (default) 0x1: Inactive
11:7	RESERVED_11_7	
6	ENTER_DEEP_PD	SW: RW, HW: R Issue Deep Power Down. This bit is self-cleared once the command is executed. Deep Power down feature is only available on LPDDR1 and LPDDR2 SDRAM devices. HW will check to ensure all commands outstanding to the rank have completed before issuing the DPD command. 0x0: no-op (default) 0x1: Issue DPD
5	EXIT_DEEP_PD	SW: RW, HW: R Issue Exit Deep Power Down. This bit is self-cleared once the command is executed. Deep Power down feature is only available on LPDDR1 and LPDDR2 SDRAM devices. When exiting Deep Power Down for a given Rank, it is required to re-initialize the LPDDR1 SDRAM devices by repeating the initialization sequence for the associated Rank before that memory can be utilized or accessed. As such, it is necessary to clear the initialization complete state of the associated Rank by setting DDR_DEVICE_CONFIG[15/14] to 1'b0 before exiting Deep Power Down. It is SW's responsibility to ensure that the minimum duration of DPD is met. Additionally SW needs to ensure that the clocks are stable before exiting DPD. 0x0: no-op (default) 0x1: Issue DPD exit
4	ZQ_CAL_SHORT	SW: RW, HW: RW Issue Short ZQ-Cal Command. This bit is self-cleared once the command is executed. This only applies to PCDDR3 devices. For LPDDR2, use the DDR_MR_CNTL_WDATA CSR. 0x0: no-op (default) 0x1: Issue ZQ-Cal
3	ZQ_CAL_LONG	SW: RW, HW: RW Issue Long ZQ-Cal Command. This bit is self-cleared once the command is executed. This only applies to PCDDR3 devices. For LPDDR2, use the DDR_MR_CNTL_WDATA CSR. 0x0: no-op (default) 0x1: Issue ZQ-Cal
2	AUTO_REFRESH	SW: RW, HW: RW Auto-Refresh Command. This can only be set when the rank has not been initialized. This bit is self-cleared once the command is executed. 0x0: no-op (default) 0x1: execute

EBI1_CH1_DDR_MANUAL_CMD (cont.)

Bits	Name	Description
1	PRECHARGE_ALL	SW: RW, HW: RW Precharge All Command. This can only be set when the rank has not been initialized. This bit is self-cleared once the command is executed. 0x0: no-op (default) 0x1: execute
0	SR_READ	SW: RW, HW: RW Status Register Read Command for LPDDR1. SRR feature is only supported by LPDDR1 and LPDDR2 SDRAM devices. This bit is self-cleared once the command is executed and SR data is captured. The SR data for LPDDR1 is captured in DDR_MR_RDDATA_RANK0/1. A manual SRR command to LPDDR2 devices can be initiated by using the DDR_MR_CNTL_WDATA CSR. 0x0: no-op (default) 0x1: execute

0x00D80014 EBI1_CH1_DDR_MR_CNTL_WDATA

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Access Control Register

This register is used whenever SW needs to access the DRAM Mode Register. It is used in device initialization for programming the memory device's mode registers. Once the SDRAM device is initialized, it is used for issuing MRW commands to LPDDR1/LPDDR2/PCDDR2/PCDDR3. and MRR commands (manual SRR, manual ZQ commands) for LPDDR2.

EBI1_CH1_DDR_MR_CNTL_WDATA

Bits	Name	Description
31:24	MR_ADDR	SW: RW, HW: R Specify which mode register to access. Note that LPDDR2 supports up to 256 Mode registers. Hence the programmed MR_ADDR needs to be valid based on the specific SDRAM device. 0000_0000: MR (Mode Register or SR for LPDDR1) 0000_0001: EMR1 (Extended Mode Register 1) 0000_0010: EMR2 (Extended Mode Register 2) 0000_0011: EMR2 (Extended Mode Register 3) .....
23	RESERVED_23	

EBI1_CH1_DDR_MR_CNTL_WDATA (cont.)

Bits	Name	Description
22	RD_DQCAL	SW: W, HW: RW DQ Calibration command. This is only supported for LPDDR2 & PCDDR3 devices. This is used for read training and/or rank auto detect. A pre-defined read pattern is sent out by the DRAM and captured by the controller. In case of LPDDR2, this is an MRR command with MR_ADDR specified above (valid MR_ADDR is 0x32 & 0x40). In case of PCDDR3 devices, this is an MPR Read command and hence MR_ADDR field is a don't care. The status of the DQ Calibration command is recorded in DDR_DQCAL_STATUS_RANK0/1 and in DDR_DQCAL_RDATA_RANK0/1. This bit is cleared by HW once the command is executed. 0x0: do not execute (default) 0x1: execute
21:20	RD_DQCAL_EXP_PATTERN	SW: RW, HW: R This is the read data pattern from the memory device. The values "00" and "01" are applicable only for LPDDR2 devices (memory burst length of 4), whereas the value "10" is applicable only for PCDDR3 devices (memory burst length of 8). 0x0: Pattern_1010 0x1: Pattern_0011 0x2: Pattern_01010101
19:18	MR_RANK_SEL	SW: RW, HW: R Specify DRAM rank to which the command goes. After the SDRAM device has been initialized, a value of "11" is considered illegal. 0x0: Invalid (default) 0x1: Rank 0 only 0x2: Rank 1 only 0x3: Both ranks 0 and 1
17	MRR	SW: W, HW: RW Read Mode Register from LPDDR2 SDRAM. This bit is cleared by HW once the command is executed. MRR commands are only supported by LPDDR2 SDRAM devices and the read data is available in DDR_MR_RDATA_RANK0/1 after the command completes. 0x0: do not execute (default) 0x1: execute
16	MRW	SW: W, HW: RW Writes the Mode Register to the SDRAM. This bit is cleared by HW once the command is executed. 0x0: do not execute (default) 0x1: execute
15:0	MR_WDATA	SW: RW, HW: R Data for Mode Register Writes. SW needs to program the mode register based on the specific SDRAM device as the mapping of the 16-bits is different for different SDRAM device types.

0x00D80020 EBI1_CH1_DDR_MR_RDATA_RANK0

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Access Data Register for Rank0

This register contains the DRAM mode register contents. This is used to capture the read data from the SDRAM device's mode register. This register has bit-to-bit direct mapping to the DRAM mode register and it's software's responsibility to interpret results for reads. The bit definition will be different depending on mode registers and/or types of memory devices.

EBI1_CH1_DDR_MR_RDATA_RANK0

Bits	Name	Description
31:0	MR_RDATA	SW: R, HW: W Data for Mode Register Reads for Rank0

0x00D80024 EBI1_CH1_DDR_MR_RDATA_RANK1

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Access Data Register for Rank1

This register contains the DRAM mode register contents. This is used to capture the read data from the SDRAM device's mode register. This register has bit-to-bit direct mapping to the DRAM mode register and it's software's responsibility to interpret results for reads. The bit definition will be different depending on mode registers and/or types of memory devices.

EBI1_CH1_DDR_MR_RDATA_RANK1

Bits	Name	Description
31:0	MR_RDATA	SW: R, HW: W Data for Mode Register Reads for Rank1

0x00D80028 EBI1_CH1_DDR_MRR_REPEAT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Read Recurrence Register

This register is used to control recurrence of MR read. The most common use of these set of registers would be for the purpose of supporting SRR (Status Register Read) feature.

EBI1_CH1_DDR_MRR_REPEAT

Bits	Name	Description
31:24	MRR_ADDR	SW: RW, HW: R Specify which mode register to access. Note that LPDDR2 has up to 256 mode registers. The MRR_ADDR needs to be set such that it is valid for the specific SDRAM device. 0000_0000: MR (Mode Register or SR for LPDDR1) 0000_0001: (EMR1) Extended Mode Register 1 0000_0010: (EMR 2) Extended Mode Register 2 0000_0011: (EMR 3) Extended Mode Register 3 ....
23:19	RESERVED_23_19	
18:16	MRR_INTERVAL	SW: RW, HW: R Number of 128*1024 tcxo clock edges between SRR samples. 0x0: Disabled (default) 0x1: 128 0x2: 256 0x3: 512 0x4: 1024 0x5: 2048 0x6: 4096 0x7: 8192
15:14	MRR_RANK_SEL	SW: RW, HW: R Specify DRAM rank to which the command goes. 0x0: Not valid (default) 0x1: Rank 0 only 0x2: Rank 1 only 0x3: Both ranks 0 and 1
13:12	RESERVED_13_12	

EBI1_CH1_DDR_MRR_REPEAT (cont.)

Bits	Name	Description
11:8	MRR_INTERVAL_OVERRIDE	SW: RW, HW: R This is a debug switch which is only to be enabled for simulation purposes. As the MRR interval is huge, setting this reduces the size of the interval down counter. e.g., Setting this to "1000" results in MRR interval of "001" to be mapped to an 8-bit down-counter (instead of 26 bit down counter), MRR interval of "010" to be mapped to a 9-bit down counter and so on. This basically sets the down counter size of the first MRR interval mode (of "001") & the remaining MRR interval modes which are mapped to down counter widthis are incremented by 1. 0x0: Disabled (default) 0x1: RESERVED_1 0x2: RESERVED_2 0x3: RESERVED_3 0x4: Size_of_4 0x5: Size_of_5 0x6: Size_of_6 0x7: Size_of_7 0x8: Size_of_8 0x9: Size_of_9 0xA: RESERVED_4 0xB: RESERVED_5 0xC: RESERVED_6 0xD: RESERVED_7 0xE: RESERVED_8 0xF: RESERVED_9
7:0	RESERVED_7_0	

0x00D80034 EBI1_CH1_DDR_MRR_REPEAT_DATA_RANK0

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Access Data Register for Rank0

This register contains the DRAM mode register contents the 32 bits of data for repetitive MR reads perfomed via DDR_MRR_REPEAT CSR. A common use of this register would be to hold the data for the SRR reads.

EBI1_CH1_DDR_MRR_REPEAT_DATA_RANK0

Bits	Name	Description
31:0	MRR_DATA	SW: R HW: W Mode register data for repetitive reads for Rank0

0x00D80038 EBI1_CH1_DDR_MRR_REPEAT_DATA_RANK1

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Access Data Register for Rank1

This register contains the DRAM mode register contents the 32 bits of data for repetitive MR reads performed via DDR_MRR_REPEAT CSR. A common use of this register would be to hold the data for the SRR reads.

EBI1_CH1_DDR_MRR_REPEAT_DATA_RANK1

Bits	Name	Description
31:0	MRR_DATA	SW: R HW: W Mode register data for repetitive reads for Rank1

0x00D8003C EBI1_CH1_DDR_CMD_EXEC_OPT_0

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00030000

DDR Command Execution Optimization Register 0.

This register is used to define the page management mode, command starvation of the DDR module. Additionally it also controls the enabling of the clockstop/powerdown features of the SDRAM device.

EBI1_CH1_DDR_CMD_EXEC_OPT_0

Bits	Name	Description
31:28	RESERVED_31_28	
27:16	PAGE_OPEN_TIMER	SW: RW, HW: R This field is only applicable if the page management policy/mode field is set to "timer-based". In this mode, a down counter based on DDR1x clock is started when the page is opened and the counter enabled only when the page is idle and has no pending runnable HITS. The value indicated by this field determines how long to wait for a potential runnable HIT to come along. When a runnable HIT appears while it is counting down, the counter gets reloaded to the initial value. 12'h000: Reserved 12'h00 : Reserved 12'h002: Reserved 12'h003: MIN_CC (3 cycles) (default)

EBI1_CH1_DDR_CMD_EXEC_OPT_0 (cont.)

Bits	Name	Description
15	PAGE_MGMT_POLICY	SW: RW, HW: R Control how HW manages DRAM pages. 0x0: Keep Page Open (Keep Page Open unless forced to close it. e.g. forced to close because of a refresh, different page to open in the same bank if command causing a conflict has a priority greater than the highest priority of a pending HIT*, tRASmax timer expiry) 0x1: Timer Based (An additional reason to close the page would be if the "page_open_timer" expires)
14:7	RDCMD_STARVATION_TIMER	SW: RW, HW: R This specifies the number of ddr1x cycles since a read command became runnable. Once the down timer expires and the read command hasn't been executed, it gets elevated to a higher priority within the command's original priority level. 0000_0000: Disable (default) 0000_0001: RESERVED 0000_0010: MIN_CC (2 cycles)
6	WR_RD_PREF	SW: RW, HW: R Indicates the Column Command Selection Preference. For example, if set to '0', the column logic will give preference to selecting Read hits Vs. Write hits given they are of equal priority. 0x0: Prefer Reads (default) 0x1: Prefer Writes
5	DDR_CK_ALWAYS_ON_DBG_MODE	SW: RW, HW: R Debug mode wherein the clock to the memory device is always on. This is a debug mode as most of the chip configurations run in shared clock mode. If this debug mode is enabled, then SW needs to ensure that there are no IOCAL requests sent to the DDR controller for calibrating the clock pad. 0x0: Disabled (default) 0x1: Enable
4	CONCURRENT_SELF_REFRESH_EN	SW: RW, HW: R This only applies to multi-rank configurations. When set, this causes self refresh to be always entered/exited together for both ranks. This is specifically required to be set for ODT say for example, when DDR_CMD_EXEC_OPT_3[RANK0_ODT_ON_RD_RANK1] or DDR_CMD_EXEC_OPT_3[RANK1_ODT_ON_RD_RANK0] are set or in write scenarios wherein DDR_CMD_EXEC_OPT_3[EN_ODT_SWITCH_RANK_UNAVAIL] isn't used. It is to be noted that in this mode, SW will not have independent rank control for self refresh using DDR_CMD_EXEC_OPT_1[SELF_REFRESH_RANK1/0]. SW can set both bits and both the ranks will enter self refresh together when they can. 0x0: Disabled (default) 0x1: Enabled

EBI1_CH1_DDR_CMD_EXEC_OPT_0 (cont.)

Bits	Name	Description
3	SEL_REG_FREQ_SWITCH	SW: RW, HW: RW Not Supported. Switch the currently used timing register set to the other set (current set is determined via ddr_device_status[curr_sel_reg_freq_switch]). SW needs to guarantee that this bit is written only when HW is in self refresh mode. Additionally, SW should not write this bit if SW initiated HW sequence for clock switching is in progress. This bit is self-cleared once the command is executed. 0x0: no-op (default) 0x1: execute switch
2	PWR_DOWN_EN	SW: RW, HW: R Enable Power Down mode for the memory device. Power down is supported by LPDDR1/2 and PCDDR2/3 devices. **NOTE** HW will enter clockstop and powerdown irrespective of the enable setting if HW frequency switch using clockstop and powerdown request is received. 0x0: Disabled (default) 0x1: Enabled
1	CLK_STOP_EN	SW: RW, HW: R Enable Clock Stop mode for the memory device. This needs to be set depending on the SDRAM device present. For LPDDR1, this can be enabled, but for PCDDR2/3 & LPDDR2 devices, this must be disabled. **NOTE** HW will enter clockstop and powerdown irrespective of the enable setting if HW frequency switch using clockstop and powerdown request is received. 0x0: Disabled (default) 0x1: Enabled
0	CLK_STOP_DURING_PWR_DOWN_EN	SW: RW, HW: R Clock can be stopped to the memory device ONLY during Power Down. This can be enabled for LPDDR2, but must be disabled for PCDDR devices. Note that only CLK_STOP_EN field or this field can be set. LPDDR1 devices should utilize the CLK_STOP_EN setting rather than this setting. **NOTE** HW will enter clockstop and powerdown irrespective of the enable setting if HW frequency switch using clockstop and powerdown request is received. 0x0: Disabled (default) 0x1: Enabled

0x00D80040 EBI1_CH1_DDR_CMD_EXEC_OPT_1

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x0000FF0

DDR Command Execution Optimization Register 1.

EBI1_CH1_DDR_CMD_EXEC_OPT_1

Bits	Name	Description
31:28	RESERVED_31_28	
27	SELF_REFRESH_RANK1	SW: RW, HW: R Enter/Exit Self-Refresh. This bit does not reset automatically. Software must turn it on, then turn it off 0x0: exit (default) 0x1: enter
26	SELF_REFRESH_RANK0	SW: RW, HW: R Enter/Exit Self-Refresh. This bit does not reset automatically. Software must turn it on, then turn it off 0x0: exit (default) 0x1: enter
25:22	RESERVED_25_22	
21:12	RANK_IDLE_TIMER	SW: RW, HW: R Counts the number of XO clock cycles wherein the rank(s) is idle. Once expired, this will cause the rank to be in precharge state. This is an useful feature to enable especially if DDR_CMD_EXEC_OPT_0[PAGE_MGMT_POLICY] is set to "Keep Pages Open". 00_0000_0000: Disabled (default) 00_0000_0001: Reserved 00_0000_0010: Reserved
11:8	RUN_ATLEAST_ONE_TRANS_RD_CONFLICT	SW: RW, HW: R This is a vector sized to the number of priority levels (4). It the bit position corresponding to a priority level is set, then it indicates that a read conflict of that priority level can cause a page to close (if the conflict priority level is greater than the priority level of a pending HIT to the open page) only if at least one transaction has been run to an open page. 0xF: run_at least_one (default)
7:4	RUN_ATLEAST_ONE_TRANS_WR_CONFLICT	SW: RW, HW: R This is a vector sized to the number of priority levels (4). It the bit position corresponding to a priority level is set, then it indicates that a write conflict of that priority level can cause a page to close (if the conflict priority level is greater than the priority level of a pending HIT to the open page) only if at least one transaction has been run to an open page. 0xF: run_at least_one (default)

EBI1_CH1_DDR_CMD_EXEC_OPT_1 (cont.)

Bits	Name	Description
3	ENABLE_DDR2X_CLKON_DURING_CSPD	SW: RW, HW: R By default, the 2X clock will only be turned off only when both ranks are in self refresh and memory clock is no longer needed. This switch enables also turning off the 2X clock during clockstop and powerdown (this from memory perspective only applies to LPDDR1/LPDDR2 devices). 0x0: Disabled (default) 0x1: Enabled
2	ENABLE_POWER_OPT_AUTO_SRR_ZQ	SW: RW, HW: R When enabled, the design will not wakeup the memory device from self refresh (if in self refresh) just because of an auto SRR or an auto ZQCAL is needed. Instead it will promote the auto ZQCAL required to be a long zqcal if a normal auto ZQ was missed. 0x0: Disabled (default) 0x1: Enabled
1	ENABLE_CMD_ADDR_OE_CNTL	SW: RW, HW: R This is typically used for PCDDR3 devices. When enabled, the design will indicate to the PHY to tri-state the command address bus when all ranks are in self refresh and the memory clocks are off, as an additional power savings mode. This is required as a shunt resistance is typically used in the command address path for PCDDR3 memory boards and hence will always burn power as the command address is always driven. 0x0: Disabled (default) 0x1: Enabled
0	LOAD_TRP_CNTL	SW: RW, HW: R This bit controls as to when the TRP timer gets started. There seems to be a difference in the memory specifications which requires this control bit. When set to '0' (required for LPDDR1), the TRP timer gets loaded with the first precharge command that closes a rank/bank. Any subsequent precharges (e.g., precharge all) to that rank/bank are ignored as the state of the page is closed. When set to '1' (required for LPDDR2/PCDDR2/PCDDR3), the latest precharge command, e.g., precharge all will cause TRP timer to get reloaded even if the page was closed. 0x0: Valid Precharge (default) 0x1: Latest Precharge

0x00D80044 EBI1_CH1_DDR_CMD_EXEC_OPT_2

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000390

DDR Command Execution Optimization Register 2.

EBI1_CH1_DDR_CMD_EXEC_OPT_2

Bits	Name	Description
31	RESERVED_31	
30:28	ZQCAL_INTERVAL	SW: RW, HW: R Number of 256 timer clock edges between short ZQCalibrations. This feature is only available for LPDDR2 and PCDDR3 devices. When enabled, zqcalibration is scheduled for rank0 if enabled. Once it completes, zqcalibration is scheduled for rank1 if enabled. This assumes that the ranks zqcalibration commands cannot be overlapped. The timer clock usually runs at 32KHz, providing interval range of 40-2560ms. 0x0: Disabled (default) 0x1: 4 0x2: 8 0x3: 16 0x4: 32 0x5: 64 0x6: 128 0x7: 256
27:20	CLKON_IDLE_TIMER	SW: RW, HW: R Counts the number of DDR1x clock cycles wherein the DDR controller is idle and it's clock can be shut off. Once expired, this will cause the clkon request to get de-asserted. If TOP_MISC_CNTL[MODE_CLKON_DDR_2X] is set, then the value of this field needs to be at least the value of DDR_CMD_EXEC_OPT_2[CLKON2X_ASSERT_WAIT_TIMER]. 0000_0000 : Disabled (default)
19:14	CLKON2X_ASSERT_WAIT_TIMER	SW: RW, HW: R Counts the number of DDR1x clock cycles to wait before waking up from self refresh or clockstop-powerdown (if DDR_CMD_EXEC_OPT_1[ENABLE_DDR2X_CLKON_DURING_CSPD] is enabled) after clkon2x asserts. This is to avoid any clock glitches propagating to the memory device. This delay (clock controller -> hsddrx) is not expected to be more than 15-20 ddr1x clock cycles and needs to be set if TOP_MISC_CNTL[MODE_CLKON_DDR_2X] is set. 00_0000 : Disabled (default)
13:10	RESERVED_13_10	
9:8	RDCMD_HP_REMAP_LEVEL3	SW: RW, HW: R This is used to remap the high priority level 3 of the AXI Read command to a different priority level. 0x0: Map to Priority Level 0 0x1: Map to Priority Level 1 0x2: Map to Priority Level 2 0x3: Map to Priority Level 3 (default)

EBI1_CH1_DDR_CMD_EXEC_OPT_2 (cont.)

Bits	Name	Description
7:6	RDCMD_HP_REMAP_LEVEL2	SW: RW, HW: R This is used to remap the high priority level 2of the AXI Read command to a different priority level. 0x0: Map to Priority Level 0 0x1: Map to Priority Level 1 0x2: Map to Priority Level 2 (default) 0x3: Map to Priority Level 3
5:4	RDCMD_HP_REMAP_LEVEL1	SW: RW, HW: R This is used to remap the high priority level 1of the AXI Read command to a different priority level. 0x0: Map to Priority Level 0 0x1: Map to Priority Level 1 (default) 0x2: Map to Priority Level 2 0x3: Map to Priority Level 3
3:2	RDCMD_HP_REMAP_LEVEL0	SW: RW, HW: R This is used to remap the high priority level 0 of the AXI Read command to a different priority level. 0x0: Map to Priority Level 0 (default) 0x1: Map to Priority Level 1 0x2: Map to Priority Level 2 0x3: Map to Priority Level 3
1	RESERVED_1	
0	UPDATE_MEM_LATENCY_ON_FREQ_SWITCH	SW: RW, HW: R This is a valid bit which controls whether the memory latencies are required to be changed as part of frequency switch. The setting of this bit is dependent on the device type, the frequency of operation and the current memory latencies. If this bit is set, then the alternate values specified in DDR_UPDATE_FREQ_CHANGE_ALT CSR will be taken into account upon receiving a HW based frequency change request. Additionally, when this bit is set, then the mode register writes programmed in DDR_MRW0/1_HW_FREQ_SWITCH will be executed as part of the HW based frequency switch. 0x0: Disabled (default) 0x1: Enabled

0x00D80048 EBI1_CH1_DDR_CMD_EXEC_OPT_3

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000150

DDR Command Execution Optimization Register 3.

This register has controls for ODT for PCDDR2 and PCDDR3.

If DDR_CMD_EXEC_OPT_2[UPDATE_MEM_LATENCY_ON_FREQ_SWITCH] is set, then ODT_START_DELAY_RD/WR, ODT_OFF_DELAY and tANPD are frequency dependent fields.The alternate CSR field for ODT_START_DELAY_RD/WR below is DDR_UPDATE_FREQ_CHANGE_ALT[ODT_START_DELAY_RD/WR].

The alternate CSR field for ODT_OFF_DELAY below is DDR_UPDATE_FREQ_CHANGE_ALT[ODT_OFF_DELAY].

The alternate CSR field for tANPD below is DDR_UPDATE_FREQ_CHANGE_ALT[tANPD].

EBI1_CH1_DDR_CMD_EXEC_OPT_3

Bits	Name	Description
31	CODT_ON_WR	SW: RW, HW: R Enable the Controller ODT to be driven when write occurs on any rank. 0x0: Disable (default) 0x1: Enable
30	CODT_ON_RD	SW: RW, HW: R Enable the Controller ODT to be driven when read occurs on any rank. 0x0: Disable (default) 0x1: Enable
29	RANK1_ODT_ON_WR_RANK1	SW: RW, HW: R Enable Rank1 ODT to be driven when write occurs on Rank1. 0x0: Disable (default) 0x1: Enable
28	RANK1_ODT_ON_WR_RANK0	SW: RW, HW: R Enable Rank1 ODT to be driven when write occurs on Rank0. 0x0: Disable (default) 0x1: Enable
27	RANK1_ODT_ON_RD_RANK1	SW: RW, HW: R Enable Rank1 ODT to be driven when read occurs on Rank1. 0x0: Disable (default) 0x1: Enable
26	RANK1_ODT_ON_RD_RANK0	SW: RW, HW: R Enable Rank1 ODT to be driven when read occurs on Rank0. 0x0: Disable (default) 0x1: Enable
25	RANK0_ODT_ON_WR_RANK1	SW: RW, HW: R Enable Rank0 ODT to be driven when write occurs on Rank1. 0x0: Disable (default) 0x1: Enable

EBI1_CH1_DDR_CMD_EXEC_OPT_3 (cont.)

Bits	Name	Description
24	RANK0_ODT_ON_WR_RANK0	SW: RW, HW: R Enable Rank0 ODT to be driven when write occurs on Rank0. 0x0: Disable (default) 0x1: Enable
23	RANK0_ODT_ON_RD_RANK1	SW: RW, HW: R Enable Rank0 ODT to be driven when read occurs on Rank1. 0x0: Disable (default) 0x1: Enable
22	RANK0_ODT_ON_RD_RANK0	SW: RW, HW: R Enable Rank0 ODT to be driven when read occurs on Rank0. 0x0: Disable (default) 0x1: Enable
21:19	ODT_START_DELAY_WR	SW: RW, HW: R This delay only applies to the Rank ODT and not the controller ODT. Specifies the delay in ddr1x clock cycles between the DDR Write command and the ODT being driven high. Typically for PCDDR2 devices for writes, this should be set to (Write latency - tAOND) and for PCDDR3 devices for writes, this must be set to "1" for optimal settings. The above indicates the maximum value allowed for the ODT signal to be turned on/driven high w.r.t the write CAS command. Note that a value of "0" indicates that the ODT signal is turned on 1 cycle before the write CAS command. A value of "1" indicates that the ODT signal is turned on in the same cycle as the write CAS command and so on. The difference between the maximum value and the value programmed is required to be added as additional incremental delays to DDR_DRAM_TIMING_2[tOST], DDR_DRAM_TIMING_2[tRTW_SAME_RANK] and DDR_DRAM_TIMING_2[tRTW_DIFF_RANK] to avoid cases where in there is overlap among the different ODT signals. The values verified are MAX and MAX-1.

EBI1_CH1_DDR_CMD_EXEC_OPT_3 (cont.)

Bits	Name	Description
18:16	ODT_START_DELAY_RD	SW: RW, HW: R This delay only applies to the Rank ODT and not the controller ODT. Specifies the delay in ddr1x clock cycles between the DDR Read command and the ODT being driven high. Typically for PCDDR2 devices for reads, this should be set to (Read latency - tAOND) and for PCDDR3 devices for reads, this must be set to (Read Latency - (Write Latency - 2)) for optimal settings. The above indicates the maximum value allowed for the ODT signal to be turned on/driven high w.r.t the read CAS command. Note that a value of "0" indicates that the ODT signal is turned on 1 cycle before the read CAS command. A value of "1" indicates that the ODT signal is turned on in the same cycle as the read CAS command and so on. The difference between the maximum value and the value programmed might need to be added as additional incremental delays to DDR_SM_TIMING_0[DLY_RD_DIFF_RANK], DDR_DRAM_TIMING_2[WR_TO_RD_DLY_DIFF_RANK] to avoid cases where in there is overlap among the different ODT signals. The values verified are MAX and MAX-1.
15:13	ODT_OFF_DELAY	SW: RW, HW: R This delay specifies the ODT off memory timing parameter for rank ODT. For PCDDR2, if DDR_CMD_EXEC_OPT_0[PWR_DOWN_EN] is 1'b0 then program this to the timing parameter, tAOFD. For PCDDR2, if DDR_CMD_EXEC_OPT_0[PWR_DOWN_EN] is 1'b1 then program this to MAX(tAOFD, tANPD). For PCDDR3, this is to be programmed to "Write Latency -2", which is ODTLoff.
12:10	ODTH8	SW: RW, HW: R Specifies the timing parameter ODTH8 (for PCDDR3) in ddr1x clock cycles. If using PCDDR2, leave this as POR.
9	EN_ODT_SWITCH_RANK_UNAVAIL	SW: RW, HW: R This only applies in multi-rank systems. When enabled, the design will automatically turn ON the same rank's odt on a write (if not already configured) if the other rank's odt should have been turned on, but it can't as the other rank is in self refresh or power down (If EN_ODT_POWER_DOWN is 1'b1, then the only scenario where the dynamic switch is enabled is when the other rank is in self refresh). 0x0: Disable (default) 0x1: Enable
8	EN_ODT_POWER_DOWN	SW: RW, HW: R If set, then ODT will be driven to a rank (if required - based on ODT configuration) in powerdown mode. The optimal setting is for this bit to be enabled. 0x0: Disable 0x1: Enable (default)

EBI1_CH1_DDR_CMD_EXEC_OPT_3 (cont.)

Bits	Name	Description
7:6	ODT_EXTEND_DELAY_WR	SW: RW, HW: R Specifies the number of ddr1x clock cycles after the write completes should the rank's Rtt ODT resistance be turned off. The optimal case is "01". Additional delays might require the write to read same/diff rank timer delays to be increased. The difference between the value programmed and the optimal settings might need to be added as additional incremental delays to DDR_DRAM_TIMING_2[tOST], DDR_DRAM_TIMING_2[WR_TO_RD_DLY_DIFF_RANK] to avoid cases where in there is overlap among the different ODT signals. The values verified are "01" and "10". 0x0: Reserved 0x1: 1 clock cycle later (default) 0x2: 2 clock cycles later 0x3: 3 clock cycles later
5:4	ODT_EXTEND_DELAY_RD	SW: RW, HW: R Specifies the number of ddr1x clock cycles after the read completes should the rank's Rtt ODT resistance be turned off. The optimal case is "01". Additional delays might require the write to read same/diff rank timer delays to be increased. The difference between the value programmed and the optimal settings might need to be added as additional incremental delays to DDR_SM_TIMING_0[DLY_RD_DIFF_RANK], DDR_DRAM_TIMING_2[tRTW_SAME_RANK] and DDR_DRAM_TIMING_2[tRTW_DIFF_RANK] to avoid cases where in there is overlap among the different ODT signals. The values verified are "01" and "10". 0x0: Reserved 0x1: 1 clock cycle later (default) 0x2: 2 clock cycles later 0x3: 3 clock cycles later
3:1	TANPD	SW: RW, HW: R This specifies the memory timing parameter tANPD in ddr1x clock cycles. For PCDDR2 devices, program this to the timing parameter tANPD, for PCDDR3 devices, this needs to be programmed to WL - 1 (as per PCDDR3 spec).
0	DLL_CNTL_PCHG_PD	SW: RW, HW: R This field only applies to PCDDR3 devices. It indicates the mode register setting for MR0 bit 12. A value "0" represents that the DLL is frozen when precharge powerdown is entered, while a value "1" represents that the DLL is enabled during precharge powerdown. This is used to determine the ODT to be used (synchronous/asynchronous)

0x00D8004C EBI1_CH1_DDR_CMD_EXEC_OPT_4

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Command Execution Optimization Register 4.

This register has the programmable idle timer for entering powerdown and the DDR bus efficiency optimization timer.

EBI1_CH1_DDR_CMD_EXEC_OPT_4

Bits	Name	Description
31:24	PWR_DOWN_IDLE_TIMER	SW: RW, HW: R Count idle ddr1x cycles before entering powerdown/clockstop/clostop-powerdown. This is only valid if powerdown/clockstop/clockstop-powerdown is enabled via the DDR_CMD_EXEC_OPT_0 CSR. A value of 0 indicates that the powerdown/clockstop/clockstop-powerdown will be entered immediately when idle. 0x0: Disable (default)
23:0	RESERVED_23_0	

0x00D80050 EBI1_CH1_DDR_SM_TIMING_0

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00001000

DDR State Machine Timing Register 0

The fields in this register control the behavior of the Column State Machine.

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EBI1_CH1_DDR_SM_TIMING_0

Bits	Name	Description
31:15	RESERVED_31_15	

EBI1_CH1_DDR_SM_TIMING_0 (cont.)

Bits	Name	Description
14:12	DLY_RD_DIFF_RANK	SW: RW, HW: R Delays read to read when going to different ranks. For LPDDR1/2 devices (or PCDDR2/3 with ODT disabled), this can be set to MAX(1, RU((tHZ(DQ)max - tLZ(DQ)min)/tck) for optimal setting as these devices do not have ODT. tck here represents the time period for the fastest DDR1x clock frequency which will be used. The optimal value of this CSR is 4 cycles for PCDDR2/3, if Read Rank ODT (i.e DDR_CMD_EXEC_OPT_3[RANK0/1_ODT_ON_RD_RANK0/1]) is enabled. This accounts for the difference in the ODT off max and min timing, the requirement that Rtt needs to be off half cycle before read preamble, etc. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles
11	RD_INT_BY_RD	SW: RW, HW: R Indicates whether Read Interrupt by Read is allowed. This field needs to be set depending on the specific SDRAM device present. Use "Allowed" for LPDDR1/2 and PCDDR2. Use "Not Allowed" for PCDDR3. 0x1: Allowed 0x0: Not Allowed (default)
10	WR_INT_BY_WR	SW: RW, HW: R Indicates whether Write Interrupt by Write is allowed. This field needs to be set depending on the specific SDRAM device present. Use "Allowed" for LPDDR1/2 and PCDDR2. Use "Not Allowed" for PCDDR3. 0x1: Allowed 0x0: Not Allowed (default)
9	RD_INT_BY_BST	SW: RW, HW: R Indicates whether Read Interrupt by Burst Terminate is allowed. This field needs to be set depending on the specific SDRAM device present. Use "Allowed" for LPDDR1/2. Use "Not Allowed" for PCDDR2/3. 0x1: Allowed 0x0: Not Allowed (default)
8	WR_INT_BY_BST	SW: RW, HW: R Indicates whether Write Interrupt by Burst Terminate is allowed. This field needs to be set depending on the specific SDRAM device present. Use "Allowed" for LPDDR2. Use "Not Allowed" for LPDDR1 and PCDDR2/3. 0x1: Allowed 0x0: Not Allowed (default)

EBI1_CH1_DDR_SM_TIMING_0 (cont.)

Bits	Name	Description
7:6	WR_INT_RD_OR_PRECHG_MODE	SW: RW, HW: R Indicates the interruption mode to be allowed for write transactions when followed by Precharge or Reads.This field needs to be set depending on the specific SDRAM device present. Use "Interrupt with no delay" for LPDDR1 devices. Use "Non Interrupting" for PCDDR2/3 and LPDDR2-S2/S4. This basically sets the starting point for twr and twtr timers. 0x0: Int with no dly (default) 0x1: Int with single cc dly (Not Supported) 0x2: Non Interrupting 0x3: Reserved
5:4	RESERVED_5_4	
3:2	INT_BOUNDARY	SW: RW, HW: R Determines when the interrupting/concatenating command can be issued. This field needs to be set depending on the specific SDRAM device present. Use "Every Cycle" for LPDDR1 and LPDDR2-S2 devices. Use "Every 2 cycles" for LPDDR2-S4 and PCDDR2 devices. For PCDDR3 devices, the above fields would indicate that interruption is not allowed. Hence the value used here is not relevant. 0x0: Every Cycle (default) 0x1: Every 2 cycles 0x2: RESERVED_1 0x3: RESERVED_2
1:0	RESERVED_1_0	

0x00D80054 EBI1_CH1_DDR_SM_TIMING_1

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000004

DDR State Machine Timing Register 1

This register is used to control the behavior of the Column state machine.

EBI1_CH1_DDR_SM_TIMING_1

Bits	Name	Description
31:24	RESERVED_31_24	

EBI1_CH1_DDR_SM_TIMING_1 (cont.)

Bits	Name	Description
23:20	MEM_START_BURST_RD	SW: RW, HW: R Specifies the starting column address restrictions. This field needs to be set depending on the specific SDRAM device. Note that "interleaved" mode of addressing at the SDRAM device is not being supported. For LPDDR1/2 (all burst lengths) and PCDDR2 (memory BL of 4) use "0000". For PCDDR3 (memory BL of 8) & PCDDR2 (memory BL of 8) use "0011". For PCDDR3 OTF burst mode, this field is a don't care. Others : Reserved 0x0: Address_0_2_4_6_etc (default) 0x3: Address_0_4_etc 0xF: Address_0_only
19:16	MEM_START_BURST_WR	SW: RW, HW: R Specifies the starting column address restrictions. This field needs to be set depending on the specific SDRAM device. Note that "interleaved" mode of addressing at the SDRAM device is not being supported. For LPDDR1/2 (all burst lengths) and PCDDR2 (memory BL of 4) use "0000". For PCDDR2 (memory BL of 8) use "0011" and for PCDDR3 (memory BL of 8) use "1111". For PCDDR3 OTF burst mode, this field is a don't care. Others : Reserved 0x0: Address_0_2_4_6_etc (default) 0x3: Address_0_4_etc 0xF: Address_0_only
15:14	SYS_TIMING_MODE	SW: RW, HW: R Specifies the command interface timing relative to the chip select. This is necessary to provide an option to guarantee an additional cycle for the more heavily command interface signals to propagate to the RAMs and settle (to meet input setup requirements) before being clocked in. This is not applicable for LPDDR2. 0x0: 1T (default: Address and command can be driven in the same cycle as the chip select.) 0x1: 2T (Address and command must be driven at least 1 cycle before chip select is asserted) 0x2: RESERVED_1 0x3: RESERVED_2
13:8	RESERVED_13_8	
7	USE_ORIG_BL	SW: RW, HW: R Indicates if original or effective burst length should be used when computing timing between column commands. This field needs to be set depending on the specific SDRAM device. For LPDDR1/2, use "effective" and for PCDDR2/3, use "original". 0x1: Original 0x0: Effective (default)
6	RESERVED_6	

EBI1_CH1_DDR_SM_TIMING_1 (cont.)

Bits	Name	Description
5	ON_THE_FLY_MODE	SW: RW, HW: R Indicates that the memory burst mode selected is OTF (on-the-fly) mode. This field is only applicable for PCDDR3 SDRAM devices. 0x1: Allowed 0x0: Not Allowed (default)
4	DRIVE_WR_DQS_EARLY	SW: RW, HW: R Indicates if DQS needs to be toggled a cycle before the write data gets driven. This means that the first piece of write data will be driven on the 2nd rising edge of the Data strobe. This field needs to be set depending on the specific SDRAM device present. This is only "enabled" for PCDDR3 devices. 0x1: Enabled 0x0: Disabled (default)
3:0	BURST_LENGTH	SW: RW, HW: R Specified as Memory Burst Length. This must be in sync with the value programmed in SDRAM's mode register. For PCDDR3, memory BL of 8 ("0100" setting) and On-the-fly (OTF) mode are supported. For PCDDR3 OTF mode program CSR - DDR_SM_TIMING_1[ON_THE_FLY_MODE]. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: BL of 4 0x3: RESERVED_3 0x4: BL of 8 (default) 0x5: RESERVED_4 0x6: RESERVED_5 0x7: RESERVED_6 0x8: BL of 16 0x9: RESERVED_7 0xA: RESERVED_8 0xB: RESERVED_9 0xC: RESERVED_10 0xD: RESERVED_11 0xE: RESERVED_12 0xF: RESERVED_13

0x00D80058 EBI1_CH1_DDR_DRAM_TIMING_0

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x44301003

DDR DRAM Timing Register 0

This register contains parameters which are specified by the memory vendor in ns. The alternate register is DDR_DRAM_TIMING_0_ALT

This register holds the SDRAM timing parameters. The value of the settings is in clock cycles and may vary from one SDRAM vendor to another. The value that should be selected for each field is:

the number_of_clock_cycles of the vendor's specified value.

An example:

When the vendor's specification states tRCD = 44nS and the SDRAM clock rate = 166 MHz, the calculations are:

1. 1/166 MHz = 6nS.
2. 44nS/6nS = 7.33 clocks.
3. 7.33 clocks rounds up to 8 clocks.

Therefore, the value of RASmin_timer should be written as 4'b1000.

EBI1_CH1_DDR_DRAM_TIMING_0

Bits	Name	Description
31:29	TRTP	SW: RW, HW: R This is not the same as the memory timing parameter tRTP. Number of Additional clock cycles between a Read and a Precharge command to the same page with actual BL/2 as the initial base delay. This needs to be set depending on the memory device present. For LPDDR, this needs to be set to at least 2 cycles. For LPDDR2-S2, use MAX(2, "tRTP (memory timing parameter in ddr1x clock cycles) -1") For LPDDR2-S4, use MAX(2, "tRTP (memory timing parameter in clock cycles) -2") For PCDDR2, use MAX(2, "tRTP (memory timing parameter in clock cycles) -2") For PCDDR3, use MAX(2, "tRTP (memory timing parameter in clock cycles) -4") 0x0: RESERVED_1 0x1: RESERVED_2 0x2: Additional 2 clock cycles (default) 0x3: Additional 3 clock cycles 0x4: Additional 4 clock cycles 0x5: Additional 5 clock cycles 0x6: Additional 6 clock cycles 0x7: Additional 7 clock cycles

EBI1_CH1_DDR_DRAM_TIMING_0 (cont.)

Bits	Name	Description
28:24	TFAW	SW: RW, HW: R Programmable rolling window during which the number of activations should not exceed the CSR field - max_num_activations_tFAW. This needs to be set based on the specific SDRAM device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: RESERVED_4 0x4: MIN_CC (4 cycles default)
23:20	TRCD	SW: RW, HW: R Number of clock cycles from activate to column command (same bank). This needs to be set based on the specific SDRAM device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)
19:16	RESERVED_19_16	
15:12	TRRD	SW: RW, HW: R Number of clock cycles between Activate to Activate (different banks on same chip select). This needs to be set based on the specific SDRAM device. 0x0: RESERVED 0x1: MIN_CC (1 cycle default)
11:9	PWR_DOWN_ODT_OFF_MAX_MIN_DIFF	SW: RW, HW: R Number of clock cycles specifying the difference in the power down ODT off max/min timing parameter. For PCDDR2 & PCDDR3, this is rounded up version in ddr1x clock cycles of (tAOFPDmax - tAOFPDmin).
8:7	RESERVED_8_7	
6:5	TZQCL_MSB	SW: RW, HW: R The complete value of tZQCL timer is {tZQCL_MSB, tZQCL}. tZQCL is from DDR_DRAM_TIMING_7 CSR. Number of ddr1x clock cycles required for the long calibration sequence to execute. ZQ Calibration commands are only supported by LPDDR2 and PCDDR3 devices. For LPDDR2, this is the timing parameter - tZQCL and for PCDDR3, this is the timing parameter tZQoper.
4:0	TRAS_MIN	SW: W, HW: R Number of clocks cycles between Active and Precharge (same bank). This needs to be set based on the specific SDRAM device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)

0x00D8005C EBI1_CH1_DDR_DRAM_TIMING_1

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x000FF000

DDR Timing Parameters Register 1.

EBI1_CH1_DDR_DRAM_TIMING_1

Bits	Name	Description
31:30	RESERVED_31_30	
29	INCL_DARF_MAX_NUM_ACT_RANK1	SW: RW, HW: R NOT SUPPORTED. If set, then a DARF command is included in the maximum number of activations for tFAW window. This needs to be set based on the specific SDRAM device. For LPDDR2 devices with 8-banks, this field needs to be set to 1. For other devices, this field is set to 0. 0x0: Do not include (default) 0x1: Include
28	INCL_DARF_MAX_NUM_ACT_RANK0	SW: RW, HW: R NOT SUPPORTED. If set, then a DARF command is included in the maximum number of activations for tFAW window. This needs to be set based on the specific SDRAM device. For LPDDR2 devices with 8-banks, this field needs to be set to 1. For other devices, this field is set to 0. 0x0: Do not include (default) 0x1: Include
27:20	RESERVED_27_20	
19:16	MAX_NUM_ACT_RANK1	SW: RW, HW: R This indicates the maximum number of activations allowed in the TFAW rolling window. This needs to be set based on the specific SDRAM device. For LPDDR1 devices, LPDDR2 devices (with 4 banks) & PCDDR2 devices (with 4 banks), leave this as POR. For others (PCDDR3, LPDDR2 (8 bank devices) & PCDDR2 (8 bank devices)), the optimal value is "0100". 0xF: 15 (default)
15:12	MAX_NUM_ACT_RANK0	SW: RW, HW: R This indicates the maximum number of activations allowed in the TFAW rolling window. This needs to be set based on the specific SDRAM device. For LPDDR1 devices, LPDDR2 devices (with 4 banks) & PCDDR2 devices (with 4 banks), leave this as POR. For others (PCDDR3, LPDDR2 (8 bank devices) & PCDDR2 (8 bank devices)), the optimal value is "0100". 0xF: 15 (default)

EBI1_CH1_DDR_DRAM_TIMING_1 (cont.)

Bits	Name	Description
11:8	MAX_NUM_REFRESHES_TREFBW	SW: RW, HW: R This indicates the maximum number of refreshes allowed in the TREFBW rolling window. This applies to LPDDR2 as a means to limit the maximum current consumption. Typically, for LPDDR2, up to 8 all-bank refreshes are permitted in the tREFBW rolling window. For non-LPDDR2 devices, this field should be disabled. 0x0: Disabled (default) 0x1: RESERVED_1 0x2: RESERVED_2 0x3: 3 refreshes 0x4: 4 refreshes 0x5: 5 refreshes 0x6: 6 refreshes 0x7: 7 refreshes 0x8: 8 refreshes 0x9: RESERVED_3 0xA: RESERVED_4 0xB: RESERVED_5 0xC: RESERVED_6 0xD: RESERVED_7 0xE: RESERVED_8 0xF: RESERVED_9
7	RESERVED_7	
6:4	TMRD_READS	SW: RW, HW: R Number of clocks from Mode register set (read) to next valid command. This needs to be set based on the specific SDRAM device. Please note that the actual tmrd_read observed will be several cycles beyond the programmed value (implementation detail)
3	RESERVED_3	
2:0	TMRD_WRITES	SW: RW, HW: R Number of clocks from Mode register set (write) to next valid command. This needs to be set based on the specific SDRAM device. Please note that the actual tmrd_write observed will be several cycles beyond the programmed value (implementation detail)

0x00D80060 EBI1_CH1_DDR_DRAM_TIMING_2

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0xD2080220

DDR Timing Parameters Register 2.

EBI1_CH1_DDR_DRAM_TIMING_2

Bits	Name	Description
31:21	TRAS_MAX	SW: RW, HW: R tRASmax timer. The number of XO clock cycles before the page is closed. This needs to be loaded with the Trasmax value specified by the vendor minus 70 ddr1x clock cycles minus 6 tcxo clock cycles minus DDR_DRAM_TIMING_7[tZQCL] (if ZQCAL is used) ddr1x clock cycles. The ddr1x clock period used for computing the offset needs to be based on the minimum ddr1x clock frequency used, especially in cases wherein the ddr1x clock frequency is changed. Note that this value is specified as number of tcxo clock cycles & hence the above needs to be computed in absolute time and then divided by the XO clock period.
20:18	TCKE	SW: RW, HW: R Minimum CKE pulse (low or high) width. This needs to be set based on the specific SDRAM device present. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
17:15	RESERVED_17_15	Reserved
14:12	WR_TO_RD_DLY_DIFF_RANK	SW: RW, HW: R Additional sync time when crossing ranks. For PCDDR2/3, if the other rank write ODT is enabled (i.e DDR_CMD_EXEC_OPT_3[RANK0_ODT_ON_WR_RANK1] or DDR_CMD_EXEC_OPT_3[RANK1_ODT_ON_WR_RANK0]) then, the value programmed must be at least 3 cycles. This is to account for the difference in the ODT off max and min timing, the requirement that Rtt needs to be off half cycle before read preamble, etc. 0x0: 0 Cycles (default) 0x1: 1 Cycle 0x2: 2 Cycles 0x3: 3 Cycles 0x4: 4 Cycles 0x5: 5 Cycles 0x6: 6 Cycles 0x7: 7 Cycles
11	RESERVED_11	Reserved\
10:8	TRTW_SAME_RANK	SW: RW, HW: R 0x0: 0 Cycles 0x1: 1 Cycle 0x2: 2 Cycles (default) 0x3: 3 Cycles 0x4: 4 Cycles 0x5: 5 Cycles 0x6: 6 Cycles 0x7: 7 Cycles

EBI1_CH1_DDR_DRAM_TIMING_2 (cont.)

Bits	Name	Description
7	RESERVED_7	Reserved\
6:4	TRTW_DIFF_RANK	SW: RW, HW: R 0x0: RESERVED_1 0x1: RESERVED_2 0x2: 2 Cycles (default) 0x3: 3 Cycles 0x4: 4 Cycles 0x5: 5 Cycles 0x6: 6 Cycles 0x7: 7 Cycles
3	RESERVED_3	Reserved
2:0	TOST	SW: RW, HW: R ODT Switching time when crossing ranks for write column commands. For LPDDR1/2 devices, (or PCDDR2/3 with ODT disabled) this can be set to "000" for optimal settings as these devices do not have ODT. The optimal value of this CSR is 2 cycles for PCDDR2/3, if write rank ODT (DDR_CMD_EXEC_OPT_3[RANK0/1_ODT_ON_WR_RANK0/1]) is enabled. 0x0: 0 Cycles (default) 0x1: 1 Cycle 0x2: 2 Cycles 0x3: 3 Cycles 0x4: 4 Cycles 0x5: 5 Cycles 0x6: 6 Cycles 0x7: 7 Cycles

0x00D80064 EBI1_CH1_DDR_DRAM_TIMING_3

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x01000603

DDR Timing Parameters Register 3

This register contains parameters which are specified by the memory vendor in ns. The alternate/shadow register is DDR_DRAM_TIMING_3_ALT and is used during HW frequency switching.

EBI1_CH1_DDR_DRAM_TIMING_3

Bits	Name	Description
31:28	PD_EXIT_DURATION_ODT	SW: RW, HW: R This specifies the amount of time after a powerdown exit (which qualifies as asynchronous ODT for PCDDR2/3 devices) for which the column commands will be blocked to avoid large ODT on/off timing ranges. For PCDDR3 devices, this needs to be programmed to the timing parameter tXPDLL delay in ddr1x clock cycles. For PCDDR2 devices, this needs to be programmed to the timing parameter tAXPD delay in ddr1x clock cycles. For LPDDR1/2 devices, leave this field as POR value. The MSB value of this timer is PD_EXIT_DURATION_ODT_MSB.
27:24	TWTR	SW: RW, HW: R tWTR delay in clock cycles. 0x1: 1Cycle (default)
23	PD_EXIT_DURATION_ODT_MSB	SW: RW, HW: R The MSB bit for PD_EXIT_DURATION_ODT. This is required for PCDDR3 at higher frequencies.
22:19	TWR	SW: RW, HW: R Number of clocks from last data word to precharge
18:9	TXSRD	SW: RW, HW: R Number of clock cycles between self refresh exit and next valid Read command. The value is based on the specific SDRAM device present. For PCDDR3, this needs to be programmed with tXSDLL timing parameter. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)
8	RESERVED_8	Reserved
7:0	TXSNR	SW: RW, HW: R Number of clock cycles between self refresh exit and next valid Non-Read command. The value is based on the specific SDRAM device present. For LPDDR1/2 devices, the value programmed in TXSNR should be the same as in TXSRD. The different parameters are required for SDRAM devices with DLL's - PCDDR2/3. For PCDDR3, this needs to be programmed with tXS timing parameter. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)

0x00D80068 EBI1_CH1_DDR_DRAM_TIMING_4

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x02022220

DDR Timing Parameters Register 4

This register contains parameters which are specified by the memory vendor in ns. The alternate/shadow register is DDR_DRAM_TIMING_4_ALT and is used during HW frequency switch.

EBI1_CH1_DDR_DRAM_TIMING_4

Bits	Name	Description
31:24	TRFC	SW: RW, HW: R Number of clock cycles between auto-refresh command and the next activate command. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
23:20	TMOD	SW: RW, HW: R Specifies the timing parameter TMOD in ddr1x clock cycles for PCDDR2/3 devices.
19:16	TXPNR_ACT_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next valid non-read command. This value gets used only if the Power down state was active power down. This distinction is required for PCDDR devices where in a slow/fast exit option in the Mode Register could potentially mean different timers for read commands (which require a DLL) Vs. a non-read command. For PCDDR2, program this to "tXPNR" if available, else set to "tXP". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. For LPDDR1/2 program this to "tXPNR" if available, else set to "tXP". For PCDDR3, set this to "tXP". 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)

EBI1_CH1_DDR_DRAM_TIMING_4 (cont.)

Bits	Name	Description
15:12	TXPR_ACT_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next read command. This value gets used only if the Power down state was active power down. For PCDDR2, if Mode register for "Active Power Down Exit Time" is programmed to "fast exit", set this to memory timing parameter "tXARD", else program this to "tXARDS". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. For LPDDR1/2, program this to "tXPR" if available, else set to "tXP". For PCDDR3, set this to "tXP". 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
11:8	TXPNR_PCHG_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next non-read command. This value gets used only if the Power down state was precharge power down. For PCDDR3, if ODT is enabled and the Mode register for "DLL control for Precharge PD" is programmed to "fast exit", set this to memory timing parameter "tXPDLL", else program this to "tXP". For LPDDR1/2 & PCDDR2, program this to "tXPNR" if available, else set to "tXP". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. The MSB bit for this is from TXPNR_PCHG_PWR_DOWN_MSB. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
7:4	TXPR_PCHG_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next read command. This value gets used only if the Power down state was precharge power down. For PCDDR3, if Mode register for "DLL control for Precharge PD" is programmed to "fast exit", set this to memory timing parameter "tXP", else program this to "tXPDLL". For LPDDR1/2 & PCDDR2, program this to "tXPNR" if available, else set to "tXP". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. The MSB bit for this is from TXPR_PCHG_PWR_DOWN_MSB. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
3:2	RESERVED_3_2	Reserved
1	TXPNR_PCHG_PWR_DOWN_MSB	SW: RW, HW: R The MSB bit for TXPNR_PCHG_PWR_DOWN. This is required for PCDDR3 at higher frequencies.
0	TXPR_PCHG_PWR_DOWN_MSB	SW: RW, HW: R The MSB bit for TXPR_PCHG_PWR_DOWN. This is required for PCDDR3 at higher frequencies.

0x00D8006C EBI1_CH1_DDR_DRAM_TIMING_5

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00003033

DDR Timing Parameters Register 5

This register contains parameters which are specified by the memory vendor in ns. The alternate/shadow register is DDR_DRAM_TIMING_5_ALT and is used during HW frequency switch.

EBI1_CH1_DDR_DRAM_TIMING_5

Bits	Name	Description
31:24	SELF_RFSH_MIN_DURATION	SW: RW, HW: R This specifies the minimum number of ddr1x clock cycles the SDRAM device is required to remain in self refresh mode once a self refresh command is registered. For LPDDR1, this is specified as tRFC, for LPDDR2, this is specified as tCKESR, for PCDDR2/3, this is specified as tCKE. Based on current implementation, the design waits this CSR field plus DDR_DRAM_TIMING_5[CLK_RESTART_BEFORE_SELF_RFSH_EXIT] plus 2 ddr1x cycles at least before coming out of self refresh.
23	RESERVED_23	Reserved
22:20	CLK_STOP_AFTER_SELF_RFSH_ENTRY	SW: RW, HW: R This specifies the minimum number of ddr1x clock cycles after the Self Refresh command is registered that the external clock to the memory device needs to run before it can be turned off. For LPDDR1/2 and PCDDR2 SDRAM devices, this should be set to "1", for PCDDR3 SDRAM devices, this should be set to "tCKSRE"
19:16	CLK_RESTART_BEFORE_SELF_RFSH_EXIT	SW: RW, HW: R This specifies the minimum number of ddr1x clock cycles the memory clock is required to be stable/re-started before CKE can go high to indicate a self refresh exit. Based on the memory device alone, for LPDDR1, this is at least "1", for LPDDR2, this needs to be set to at least 2 clock cycles. For PCDDR2 SDRAM devices, this should be set to "1", for PCDDR3 SDRAM devices, this should be set to "tCKSRX". This CSR field represents the lower 4 bits. The upper 4 bits are in CLK_RESTART_BEFORE_SR_EXIT_UPPER CSR field below. If the cur_mode in the pads is enabled and the system is configured to dynamically turn off the cur_mode during self refresh, then the 8-bit timer needs to be programmed such that it provides at least 100ns of pad settling time.

EBI1_CH1_DDR_DRAM_TIMING_5 (cont.)

Bits	Name	Description
15:12	TRP_AB	SW: RW, HW: R Number of clocks from all bank precharge to Activate (same bank). This needs to be set based on the specific SDRAM device. For LPDDR1, PCDDR3 & 4-bank PCDDR2 devices, set this to timing parameter tRP. For 8-bank PCDDR2 devices, set this to tRP + 1*tck (in clock cycles). For LPDDR2 devices, set this to timing parameter tRPab. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)
11:8	CLK_RESTART_BEFORE_SR_EXIT_UPPER	SW: RW, HW: R These bits are the upper 4 bits for the CLK_RESTART_BEFORE_SELF_RFSH_EXIT CSR field above. The timer is 8 bits wide. If the cur_mode in the pads is enabled and the system is configured to dynamically turn off the cur_mode during self refresh, then the 8-bit timer needs to be programmed such that it provides at least 100ns of pad settling time.
7:4	TRP_PB	SW: RW, HW: R Number of clocks from per bank precharge to Activate (same bank). This needs to be set based on the specific SDRAM device. For LPDDR1, PCDDR3 & PCDDR2 devices, set this to timing parameter tRP. For LPDDR2 devices, set this to timing parameter tRPpb. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)

EBI1_CH1_DDR_DRAM_TIMING_5 (cont.)

Bits	Name	Description
3:0	RD_LATENCY	SW: RW, HW: R Actual Rd Latency (from Chip select assertion to the clock edge where read data is expected - This will not be exactly equal to CAS latency from memory specs) For LPDDR1, use Read latency of 3(fixed), for LPDDR2, use Read latency of memory device + RU(tdqsckmax/tck) (RU - round up) where tck is the time period of the current ddr1x clock frequency of operation. For PCDDR2/3 devices, use the read latency of the device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: 2 cycles 0x3: 3 cycles (default) 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

0x00D80070 EBI1_CH1_DDR_DRAM_TIMING_6

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x10102000

DDR Timing Parameters Register 6.

If DDR_CMD_EXEC_OPT_2[UPDATE_MEM_LATENCY_ON_FREQ_SWITCH] is set, then WR_LATENCY is a frequency dependent field.The alternate CSR field for WR_LATENCY below is DDR_UPDATE_FREQ_CHANGE_ALT[WR_LATENCY].

EBI1_CH1_DDR_DRAM_TIMING_6

Bits	Name	Description
31:28	WR_LATENCY	SW: RW, HW: R Actual Write Latency (from Chip select assertion to the clock edge where write data is driven - This will not be exactly equal to tWL latency from memory specs). For LPDDR1, use Write latency of 1 (fixed), for LPDDR2, use Write latency of device parameter tWL + 1. For PCDDR2/3 devices, use the write latency of the device. 0x0: RESERVED 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
27:24	RESERVED_27_24	Reserved
23:20	RESTART_CLK_PWR_DOWN_EXIT	SW: RW, HW: R Number of clock cycles required for the clock to be stable before the SDRAM device exits power-down mode. This only applies if the clock was stopped during power down. For LPDDR1/2, this needs to be set to at least 2 cycles. 0x0: RESERVED 0x1: MIN_CC (1 cycle default)
19	RESERVED_19	Reserved
18:16	STOP_CLK_PWR_DOWN_ENTRY	SW: RW, HW: R Number of clock cycles required for the clock to be stable after the SDRAM device enters power-down mode. For minimum memory timings, for LPDDR1, this can be set to "000" or higher; for LPDDR2-S2/S4, this can be set to "001" or higher. 0x7: RESERVED
15:14	RESERVED_15_14	Reserved

EBI1_CH1_DDR_DRAM_TIMING_6 (cont.)

Bits	Name	Description
13:12	TSRR	SW: RW, HW: R Number of clock cycles between MRS for SRR and Read command. SRR is an LPDDR1 feature only. 0x0: 0 Cycles 0x1: 1 Cycle 0x2: 2 Cycles (default) 0x3: 3 Cycles
11:0	RESERVED_11_0	Reserved

0x00D80074 EBI1_CH1_DDR_DRAM_TIMING_7

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00011212

DDR Timing Parameters Register 7

This register contains parameters which are specified by the memory vendor in ns. The alternate/shadow register is DDR_DRAM_TIMING_7_ALT and gets used during HW frequency switch.

EBI1_CH1_DDR_DRAM_TIMING_7

Bits	Name	Description
31:24	TZQCL	SW: RW, HW: R The complete value of tZQCL timer is {tZQCL_MSB, tZQCL}. tZQCL_MSB is from DDR_DRAM_TIMING_0 CSR. Number of ddr1x clock cycles required for the long calibration sequence to execute. ZQ Calibration commands are only supported by LPDDR2 and PCDDR3 devices. For LPDDR2, this is the timing parameter - tZQCL and for PCDDR3, this is the timing parameter tZQoper.
23:17	TZQCS	SW: RW, HW: R Number of ddr1x clock cycles required for the short calibration sequence to execute. ZQ Calibration commands are only supported by LPDDR2 and PCDDR3 devices. For LPDDR2, this is the timing parameter - tZQCS and for PCDDR3, this is the timing parameter tZQCS.
16	PAD_LOW_POWER_MODE	SW: RW, HW: R SW needs to indicate the power mode based on the frequency of operation. 0x0: Low Power Mode 0x1: High Power Mode (default)

EBI1_CH1_DDR_DRAM_TIMING_7 (cont.)

Bits	Name	Description
15:12	DLY_RD_CAPTURE	SW: RW, HW: R Enables the read capture window n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
11:8	EXT_RD_CAPTURE	SW: RW, HW: R Extends the read capture window to account for board delays for getting read data from memory. For simulation, this needs to be set to at least 2 + DDR_IO_STAGE (design parameter) pipleline delay. 0x0: 0 cycles 0x1: 1 cycle 0x2: 2 cycles (default) 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

EBI1_CH1_DDR_DRAM_TIMING_7 (cont.)

Bits	Name	Description
7:4	DLY_IE_START	SW: RW, HW: R Enables the DQ/DQS pad input enable window n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
3:0	EXT_IE_WINDOW	SW: RW, HW: R Extends the DQS/DQ pad input enable window to account for board delays for getting read data from memory. For simulation, this needs to be set to at least 1 cycle. 0x0: 0 cycles 0x1: 1 cycle 0x2: 2 cycles (default) 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

0x00D80078 EBI1_CH1_DDR_DRAM_TIMING_8

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x01010101

DDR Timing Parameters Register 8

The alternate/shadow register is DDR_DRAM_TIMING_8_ALT and gets used during HW frequency switch. This CSR has the start delay and the config delay controls for the external RCW (Read Capture Window) used for DQS qualification window generation in the PHY.

EBI1_CH1_DDR_DRAM_TIMING_8

Bits	Name	Description
31:30	RESERVED_31_30	Reserved
29:28	RCW_CFG_COARSE_DLY_DATA_BYTE3	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle
27:24	RCW_START_DLY_BYTE3	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
23:22	RESERVED_23_22	Reserved
21:20	RCW_CFG_COARSE_DLY_DATA_BYTE2	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH1_DDR_DRAM_TIMING_8 (cont.)

Bits	Name	Description
19:16	RCW_START_DLY_BYTE2	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
15:14	RESERVED_15_14	Reserved
13:12	RCW_CFG_COARSE_DLY_DATA_BYTE1	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH1_DDR_DRAM_TIMING_8 (cont.)

Bits	Name	Description
11:8	RCW_START_DLY_BYTE1	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
7:6	RESERVED_7_6	Reserved
5:4	RCW_CFG_COARSE_DLY_DATA_BYTE0	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH1_DDR_DRAM_TIMING_8 (cont.)

Bits	Name	Description
3:0	RCW_START_DLY_BYTE0	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

0x00D8007C EBI1_CH1_DDR_DRAM_TIMING_9

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Timing Parameters Register 9

The alternate/shadow register is DDR_DRAM_TIMING_9_ALT and gets used during HW frequency switch. This CSR has the start delay and the config delay controls for the external RCW (Read Capture Window) used for DQS qualification window generation in the PHY.

EBI1_CH1_DDR_DRAM_TIMING_9

Bits	Name	Description
31:24	RCW_CFG_FINE_DLY_DATA_BYTE3	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.
23:16	RCW_CFG_FINE_DLY_DATA_BYTE2	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.

EBI1_CH1_DDR_DRAM_TIMING_9 (cont.)

Bits	Name	Description
15:8	RCW_CFG_FINE_DLY_DATA_BYTE1	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.
7:0	RCW_CFG_FINE_DLY_DATA_BYTE0	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.

0x00D80080 EBI1_CH1_DDR_DRAM_TIMING_0_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x44301003

DDR DRAM Timing Register 0_ALT

This register contains parameters which are specified by the memory vendor in ns. The alternate/shadow register is DDR_DRAM_TIMING_0 and gets used during HW frequency switch.

This register holds the SDRAM timing parameters. The value of the settings is in clock cycles and may vary from one SDRAM vendor to another. The value that should be selected for each field is:

the number_of_clock_cycles of the vendor's specified value.

An example:

When the vendor's specification states tRCD = 44nS and the SDRAM clock rate = 166 MHz, the calculations are:

1. 1/166 MHz = 6nS.
2. 44nS/6nS = 7.33 clocks.
3. 7.33 clocks rounds up to 8 clocks.

Therefore, the value of RASmin_timer should be written as 4'b1000.

EBI1_CH1_DDR_DRAM_TIMING_0_ALT

Bits	Name	Description
31:29	TRTP	SW: RW, HW: R This is not the same as the memory timing parameter tRTP. Number of Additional clock cycles between a Read and a Precharge command to the same page with actual BL/2 as the initial base delay. This needs to be set depending on the memory device present. For LPDDR, this needs to be set to at least 2 cycles. For LPDDR2-S2, use MAX(2, "tRTP (memory timing parameter in ddr1x clock cycles) -1") For LPDDR2-S4, use MAX(2, "tRTP (memory timing parameter in clock cycles) -2") For PCDDR2, use MAX(2, "tRTP (memory timing parameter in clock cycles) -2") For PCDDR3, use MAX(2, "tRTP (memory timing parameter in clock cycles) -4") 0x0: RESERVED_1 0x1: RESERVED_2 0x2: Additional 2 clock cycles (default) 0x3: Additional 3 clock cycles 0x4: Additional 4 clock cycles 0x5: Additional 5 clock cycles 0x6: Additional 6 clock cycles 0x7: Additional 7 clock cycles
28:24	TFAW	SW: RW, HW: R Programmable rolling window during which the number of activations should not exceed the CSR field - max_num_activations_tFAW. This needs to be set based on the specific SDRAM device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: RESERVED_4 0x4: MIN_CC (4 cycles default)
23:20	TRCD	SW: RW, HW: R Number of clock cycles from activate to column command (same bank). This needs to be set based on the specific SDRAM device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)
19:16	RESERVED_19_16	

EBI1_CH1_DDR_DRAM_TIMING_0_ALT (cont.)

Bits	Name	Description
15:12	TRRD	SW: RW, HW: R Number of clock cycles between Activate to Activate (different banks on same chip select). This needs to be set based on the specific SDRAM device. 0x0: RESERVED 0x1: MIN_CC (1 cycle default)
11:9	PWR_DOWN_ODT_OFF_MAX_MIN_DIFF	SW: RW, HW: R Number of clock cycles specifying the difference in the power down ODT off max/min timing parameter. For PCDDR2 & PCDDR3, this is rounded up version in ddr1x clock cycles of (tAOFPDmax - tAOFPDmin).
8:7	RESERVED_8_7	
6:5	TZQCL_MSB	SW: RW, HW: R The complete value of tZQCL timer is {tZQCL_MSB, tZQCL}. tZQCL is from DDR_DRAM_TIMING_7 CSR. Number of ddr1x clock cycles required for the long calibration sequence to execute. ZQ Calibration commands are only supported by LPDDR2 and PCDDR3 devices. For LPDDR2, this is the timing parameter - tZQCL and for PCDDR3, this is the timing parameter tZQoper.
4:0	TRAS_MIN	SW: W, HW: R Number of clocks cycles between Active and Precharge (same bank). This needs to be set based on the specific SDRAM device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)

0x00D80084 EBI1_CH1_DDR_DRAM_TIMING_3_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x01000603

DDR Timing Parameters Register 3_ALT

This register contains parameters which are specified by the memory vendor in ns. The alternate/shadow register is DDR_DRAM_TIMING_3 and gets used during HW frequency switch.

EBI1_CH1_DDR_DRAM_TIMING_3_ALT

Bits	Name	Description
31:28	PD_EXIT_DURATION_ODT	SW: RW, HW: R This specifies the amount of time after a powerdown exit (which qualifies as asynchronous ODT for PCDDR2/3 devices) for which the column commands will be blocked to avoid large ODT on/off timing ranges. For PCDDR3 devices, this needs to be programmed to the timing parameter tXPDLL delay in ddr1x clock cycles. For PCDDR2 devices, this needs to be programmed to the timing parameter tAXPD delay in ddr1x clock cycles. For LPDDR1/2 devices, leave this field as POR value. The MSB value of this timer is PD_EXIT_DURATION_ODT_MSB.
27:24	TWTR	SW: RW, HW: R tWTR delay in clock cycles. 0x1: 1Cycle (default)
23	PD_EXIT_DURATION_ODT_MSB	SW: RW, HW: R The MSB bit for PD_EXIT_DURATION_ODT. This is required for PCDDR3 at higher frequencies.
22:19	TWR	SW: RW, HW: R Number of clocks from last data word to precharge
18:9	TXSRD	SW: RW, HW: R Number of clock cycles between self refresh exit and next valid Read command. The value is based on the specific SDRAM device present. For PCDDR3, this needs to be programmed with tXSDLL timing parameter. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)
8	RESERVED_8	Reserved
7:0	TXSNR	SW: RW, HW: R Number of clock cycles between self refresh exit and next valid Non-Read command. The value is based on the specific SDRAM device present. For LPDDR1/2 devices, the value programmed in TXSNR should be the same as in TXSRD. The different parameters are required for SDRAM devices with DLL's - PCDDR2/3. For PCDDR3, this needs to be programmed with tXS timing parameter. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)

0x00D80088 EBI1_CH1_DDR_DRAM_TIMING_4_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x02022220

DDR Timing Parameters Register 4_ALT

This register contains parameters which are specified by the memory vendor in ns. The alternate/shadow register is DDR_DRAM_TIMING_4 and gets used during HW frequency switch.

EBI1_CH1_DDR_DRAM_TIMING_4_ALT

Bits	Name	Description
31:24	TRFC	SW: RW, HW: R Number of clock cycles between auto-refresh command and the next activate command. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
23:20	TMOD	SW: RW, HW: R Specifies the timing parameter TMOD in ddr1x clock cycles for PCDDR2/3 devices.
19:16	TXPNR_ACT_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next valid non-read command. This value gets used only if the Power down state was active power down. This distinction is required for PCDDR devices where in a slow/fast exit option in the Mode Register could potentially mean different timers for read commands (which require a DLL) Vs. a non-read command. For PCDDR2, program this to "tXPNR" if available, else set to "tXP". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. For LPDDR1/2 program this to "tXPNR" if available, else set to "tXP". For PCDDR3, set this to "tXP". 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)

EBI1_CH1_DDR_DRAM_TIMING_4_ALT (cont.)

Bits	Name	Description
15:12	TXPR_ACT_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next read command. This value gets used only if the Power down state was active power down. For PCDDR2, if Mode register for "Active Power Down Exit Time" is programmed to "fast exit", set this to memory timing parameter "tXARD", else program this to "tXARDS". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. For LPDDR1/2, program this to "tXPR" if available, else set to "tXP". For PCDDR3, set this to "tXP". 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
11:8	TXPNR_PCHG_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next non-read command. This value gets used only if the Power down state was precharge power down. For PCDDR3, if ODT is enabled and the Mode register for "DLL control for Precharge PD" is programmed to "fast exit", set this to memory timing parameter "tXPDLL", else program this to "tXP". For LPDDR1/2 & PCDDR2, program this to "tXPNR" if available, else set to "tXP". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. The MSB bit for this is from TXPNR_PCHG_PWR_DOWN_MSB. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
7:4	TXPR_PCHG_PWR_DOWN	SW: RW, HW: R Number of clock cycles between power down exit and next read command. This value gets used only if the Power down state was precharge power down. For PCDDR3, if Mode register for "DLL control for Precharge PD" is programmed to "fast exit", set this to memory timing parameter "tXP", else program this to "tXPDLL". For LPDDR1/2 & PCDDR2, program this to "tXPNR" if available, else set to "tXP". Additionally for PCDDR2 devices, if ODT is enabled then the value in this field needs to be >= tAXPD. The MSB bit for this is from TXPR_PCHG_PWR_DOWN_MSB. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: MIN_CC (2 cycles default)
3:2	RESERVED_3_2	Reserved
1	TXPNR_PCHG_PWR_DOWN_MSB	SW: RW, HW: R The MSB bit for TXPNR_PCHG_PWR_DOWN. This is required for PCDDR3 at higher frequencies.
0	TXPR_PCHG_PWR_DOWN_MSB	SW: RW, HW: R The MSB bit for TXPR_PCHG_PWR_DOWN. This is required for PCDDR3 at higher frequencies.

0x00D8008C EBI1_CH1_DDR_DRAM_TIMING_5_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00003033

DDR Timing Parameters Register 5_ALT

This register contains parameters which are specified by the memory vendor in ns. The alternate/shadow register is DDR_DRAM_TIMING_5 and gets used during HW frequency switch.

EBI1_CH1_DDR_DRAM_TIMING_5_ALT

Bits	Name	Description
31:24	SELF_RFSH_MIN_DURATION	SW: RW, HW: R This specifies the minimum number of ddr1x clock cycles the SDRAM device is required to remain in self refresh mode once a self refresh command is registered. For LPDDR1, this is specified as tRFC, for LPDDR2, this is specified as tCKESR, for PCDDR2/3, this is specified as tCKE. Based on current implementation, the design waits this CSR field plus DDR_DRAM_TIMING_5[CLK_RESTART_BEFORE_SELF_RFSH_EXIT] plus 2 ddr1x cycles at least before coming out of self refresh.
23	RESERVED_23	Reserved
22:20	CLK_STOP_AFTER_SELF_RFSH_ENTRY	SW: RW, HW: R This specifies the minimum number of ddr1x clock cycles after the Self Refresh command is registered that the external clock to the memory device needs to run before it can be turned off. For LPDDR1/2 and PCDDR2 SDRAM devices, this should be set to "1", for PCDDR3 SDRAM devices, this should be set to "tCKSRE"
19:16	CLK_RESTART_BEFORE_SELF_RFSH_EXIT	SW: RW, HW: R This specifies the minimum number of ddr1x clock cycles the memory clock is required to be stable/re-started before CKE can go high to indicate a self refresh exit. Based on the memory device alone, for LPDDR1, this is at least "1", for LPDDR2, this needs to be set to at least 2 clock cycles. For PCDDR2 SDRAM devices, this should be set to "1", for PCDDR3 SDRAM devices, this should be set to "tCKSRX". This CSR field represents the lower 4 bits. The upper 4 bits are in CLK_RESTART_BEFORE_SR_EXIT_UPPER CSR field below. If the cur_mode in the pads is enabled and the system is configured to dynamically turn off the cur_mode during self refresh, then the 8-bit timer needs to be programmed such that it provides at least 100ns of pad settling time.

EBI1_CH1_DDR_DRAM_TIMING_5_ALT (cont.)

Bits	Name	Description
15:12	TRP_AB	SW: RW, HW: R Number of clocks from all bank precharge to Activate (same bank). This needs to be set based on the specific SDRAM device. For LPDDR1, PCDDR3 & 4-bank PCDDR2 devices, set this to timing parameter tRP. For 8-bank PCDDR2 devices, set this to tRP + 1*tck (in clock cycles). For LPDDR2 devices, set this to timing parameter tRPab. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)
11:8	CLK_RESTART_BEFORE_SR_EXIT_UPPER	SW: RW, HW: R These bits are the upper 4 bits for the CLK_RESTART_BEFORE_SELF_RFSH_EXIT CSR field above. The timer is 8 bits wide. If the cur_mode in the pads is enabled and the system is configured to dynamically turn off the cur_mode during self refresh, then the 8-bit timer needs to be programmed such that it provides at least 100ns of pad settling time.
7:4	TRP_PB	SW: RW, HW: R Number of clocks from per bank precharge to Activate (same bank). This needs to be set based on the specific SDRAM device. For LPDDR1, PCDDR3 & PCDDR2 devices, set this to timing parameter tRP. For LPDDR2 devices, set this to timing parameter tRPpb. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: RESERVED_3 0x3: MIN_CC (3 cycles default)

EBI1_CH1_DDR_DRAM_TIMING_5_ALT (cont.)

Bits	Name	Description
3:0	RD_LATENCY	SW: RW, HW: R Actual Rd Latency (from Chip select assertion to the clock edge where read data is expected - This will not be exactly equal to CAS latency from memory specs) For LPDDR1, use Read latency of 3(fixed), for LPDDR2, use Read latency of memory device + RU(tdqsckmax/tck) (RU - round up) where tck is the time period of the current ddr1x clock frequency of operation. For PCDDR2/3 devices, use the read latency of the device. 0x0: RESERVED_1 0x1: RESERVED_2 0x2: 2 cycles 0x3: 3 cycles (default) 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

0x00D80090 EBI1_CH1_DDR_DRAM_TIMING_7_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00011212

DDR Timing Parameters Register 7_ALT

This register contains parameters which are specified by the memory vendor in ns. The alternate/shadow register is DDR_DRAM_TIMING_7 and gets used during HW frequency switch.

EBI1_CH1_DDR_DRAM_TIMING_7_ALT

Bits	Name	Description
31:24	TZQCL	SW: RW, HW: R The complete value of tZQCL timer is {tZQCL_MSB, tZQCL}. tZQCL_MSB is from DDR_DRAM_TIMING_0_ALT CSR. Number of ddr1x clock cycles required for the long calibration sequence to execute. ZQ Calibration commands are only supported by LPDDR2 and PCDDR3 devices. For LPDDR2, this is the timing parameter - tZQCL and for PCDDR3, this is the timing parameter tZQoper.
23:17	TZQCS	SW: RW, HW: R Number of ddr1x clock cycles required for the short calibration sequence to execute. ZQ Calibration commands are only supported by LPDDR2 and PCDDR3 devices. For LPDDR2, this is the timing parameter - tZQCS and for PCDDR3, this is the timing parameter tZQCS.
16	PAD_LOW_POWER_MODE	SW: RW, HW: R SW needs to indicate the power mode based on the frequency of operation. 0x0: Low Power Mode 0x1: High Power Mode (default)
15:12	DLY_RD_CAPTURE	SW: RW, HW: R Enables the read capture window n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

EBI1_CH1_DDR_DRAM_TIMING_7_ALT (cont.)

Bits	Name	Description
11:8	EXT_RD_CAPTURE	SW: RW, HW: R Extends the read capture window to account for board delays for getting read data from memory. For simulation, this needs to be set to at least 2 + DDR_IO_STAGE (design parameter) pipleline delay. 0x0: 0 cycles 0x1: 1 cycle 0x2: 2 cycles (default) 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
7:4	DLY_IE_START	SW: RW, HW: R Enables the DQ/DQS pad input enable window n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

EBI1_CH1_DDR_DRAM_TIMING_7_ALT (cont.)

Bits	Name	Description
3:0	EXT_IE_WINDOW	SW: RW, HW: R Extends the DQS/DQ pad input enable window to account for board delays for getting read data from memory. For simulation, this needs to be set to at least 1 cycle. 0x0: 0 cycles 0x1: 1 cycle 0x2: 2 cycles (default) 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

0x00D80094 EBI1_CH1_DDR_DRAM_TIMING_8_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x01010101

DDR Timing Parameters Register 8_ALT

The alternate/shadow register is DDR_DRAM_TIMING_8 and gets used during HW frequency switch. This CSR has the start delay and the config delay controls for the external RCW (Read Capture Window) used for DQS qualification window generation in the PHY.

EBI1_CH1_DDR_DRAM_TIMING_8_ALT

Bits	Name	Description
31:30	RESERVED_31_30	Reserved
29:28	RCW_CFG_COARSE_DLY_DATA_BYTE3	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH1_DDR_DRAM_TIMING_8_ALT (cont.)

Bits	Name	Description
27:24	RCW_START_DLY_BYTE3	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
23:22	RESERVED_23_22	Reserved
21:20	RCW_CFG_COARSE_DLY_DATA_BYTE2	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH1_DDR_DRAM_TIMING_8_ALT (cont.)

Bits	Name	Description
19:16	RCW_START_DLY_BYTE2	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
15:14	RESERVED_15_14	Reserved
13:12	RCW_CFG_COARSE_DLY_DATA_BYTE1	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH1_DDR_DRAM_TIMING_8_ALT (cont.)

Bits	Name	Description
11:8	RCW_START_DLY_BYTE1	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
7:6	RESERVED_7_6	Reserved
5:4	RCW_CFG_COARSE_DLY_DATA_BYTE0	SW: RW, HW: R This value controls the coarse delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device. 0x0: No delay (default) 0x1: 1/4 Cycle 0x2: 1/2 Cycle 0x3: 3/4 Cycle

EBI1_CH1_DDR_DRAM_TIMING_8_ALT (cont.)

Bits	Name	Description
3:0	RCW_START_DLY_BYTE0	SW: RW, HW: R Enables the external RCW n cycles from the CAS cycle for the read command. 0x0: Reserved 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles

0x00D80098 EBI1_CH1_DDR_DRAM_TIMING_9_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Timing Parameters Register 9_ALT

The alternate/shadow register is DDR_DRAM_TIMING_9 and gets used during HW frequency switch. This CSR has the start delay and the config delay controls for the external RCW (Read Capture Window) used for DQS qualification window generation in the PHY.

EBI1_CH1_DDR_DRAM_TIMING_9_ALT

Bits	Name	Description
31:24	RCW_CFG_FINE_DLY_DATA_BYTE3	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.
23:16	RCW_CFG_FINE_DLY_DATA_BYTE2	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.

EBI1_CH1_DDR_DRAM_TIMING_9_ALT (cont.)

Bits	Name	Description
15:8	RCW_CFG_FINE_DLY_DATA_BYTE1	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.
7:0	RCW_CFG_FINE_DLY_DATA_BYTE0	SW: RW, HW: R This value controls the fine-grain delay which will be applied by the PHY for the external RCW signal for precise DQS capture from the PCDDR3 DRAM device.

0x00D8009C EBI1_CH1_DDR_UPDATE_FREQ_CHANGE_ALT

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x10000000

DDR Update Frequency Change ALT register.

This register contains parameters which are dependent on the frequency of operation. The fields in this register are valid only if DDR_CMD_EXEC_OPT_2[UPDATE_MEM_LATENCY_ON_FREQ_SWITCH] is set.

The original CSR field for WR_LATENCY below is DDR_DRAM_TIMING_6[WR_LATENCY].

The original CSR field for ODT_START_DELAY_RD/WR below is DDR_CMD_EXEC_OPT_3[ODT_START_DELAY_RD/WR].

The original CSR field for ODT_OFF_DELAY below is DDR_CMD_EXEC_OPT_3[ODT_OFF_DELAY].

The original CSR field for tANPD below is DDR_CMD_EXEC_OPT_3[tANPD].

EBI1_CH1_DDR_UPDATE_FREQ_CHANGE_ALT

Bits	Name	Description
31:28	WR_LATENCY	SW: RW, HW: R Actual Write Latency (from Chip select assertion to the clock edge where write data is driven - This will not be exactly equal to tWL latency from memory specs). For LPDDR1, use Write latency of 1 (fixed), for LPDDR2, use Write latency of device parameter tWL + 1. For PCDDR2/3 devices, use the write latency of the device. 0x0: RESERVED 0x1: 1 cycle (default) 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles 0x8: 8 cycles 0x9: 9 cycles 0xA: 10 cycles 0xB: 11 cycles 0xC: 12 cycles 0xD: 13 cycles 0xE: 14 cycles 0xF: 15 cycles
27:22	RESERVED_27_22	Reserved
21:19	ODT_START_DELAY_WR	SW: RW, HW: R This delay only applies to the Rank ODT and not the controller ODT. Specifies the delay in ddr1x clock cycles between the DDR Write command and the ODT being driven high. Typically for PCDDR2 devices for writes, this should be set to (Write latency - tAOND) and for PCDDR3 devices for writes, this must be set to "1" for optimal settings. The above indicates the maximum value allowed for the ODT signal to be turned on/driven high w.r.t the write CAS command. Note that a value of "0" indicates that the ODT signal is turned on 1 cycle before the write CAS command. A value of "1" indicates that the ODT signal is turned on in the same cycle as the write CAS command and so on. The difference between the maximum value and the value programmed is required to be added as additional incremental delays to DDR_DRAM_TIMING_2[tOST], DDR_DRAM_TIMING_2[tRTW_SAME_RANK] and DDR_DRAM_TIMING_2[tRTW_DIFF_RANK] to avoid cases where in there is overlap among the different ODT signals. The values verified are MAX and MAX-1.

EBI1_CH1_DDR_UPDATE_FREQ_CHANGE_ALT (cont.)

Bits	Name	Description
18:16	ODT_START_DELAY_RD	SW: RW, HW: R This delay only applies to the Rank ODT and not the controller ODT. Specifies the delay in ddr1x clock cycles between the DDR Read command and the ODT being driven high. Typically for PCDDR2 devices for reads, this should be set to (Read latency - tAOND) and for PCDDR3 devices for reads, this must be set to (Read Latency - (Write Latency - 2)) for optimal settings. The above indicates the maximum value allowed for the ODT signal to be turned on/driven high w.r.t the read CAS command. Note that a value of "0" indicates that the ODT signal is turned on 1 cycle before the read CAS command. A value of "1" indicates that the ODT signal is turned on in the same cycle as the read CAS command and so on. The difference between the maximum value and the value programmed might need to be added as additional incremental delays to DDR_SM_TIMING_0[DLY_RD_DIFF_RANK], DDR_DRAM_TIMING_2[WR_TO_RD_DLY_DIFF_RANK] to avoid cases where in there is overlap among the different ODT signals. The values verified are MAX and MAX-1.
15:13	ODT_OFF_DELAY	SW: RW, HW: R This delay specifies the ODT off memory timing parameter for rank ODT. For PCDDR2, if DDR_CMD_EXEC_OPT_0[PWR_DOWN_EN] is 1'b0 then program this to the timing parameter, tAOFD. For PCDDR2, if DDR_CMD_EXEC_OPT_0[PWR_DOWN_EN] is 1'b1 then program this to MAX(tAOFD, tANPD). For PCDDR3, this is to be programmed to "Write Latency -2", which is ODTLoff.
12:4	RESERVED_12_4	Reserved
3:1	TANPD	SW: RW, HW: R This specifies the memory timing parameter tANPD in ddr1x clock cycles. For PCDDR2 devices, program this to the timing parameter tANPD, for PCDDR3 devices, this needs to be programmed to WL - 1 (as per PCDDR3 spec).
0	RESERVED_0	Reserved

0x00D800A0 EBI1_CH1_DDR_AUTO_RFSH_CNTL

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00001007

DDR Refresh Control Register.

This register configures the refresh operating mode of the DDR SDRAM controller.

EBI1_CH1_DDR_AUTO_RFSH_CNTL

Bits	Name	Description
31:28	RESERVED_31_28	
27:24	COUNT_RFSH_AHEAD	SW: RW, HW: R Number of refresh cycles ahead allowed. A value of '0' disables the refresh ahead mechanism. For all SDRAM devices, the max value allowed for Auto Refresh mode is 7. 0000 : (default) 0x1: Ahead of 1 0x2: Ahead of 2 0x3: Ahead of 3 0x4: Ahead of 4 0x5: Ahead of 5 0x6: Ahead of 6 0x7: Ahead of 7 0x8: RESERVED_1 0x9: RESERVED_2 0xA: RESERVED_3 0xB: RESERVED_4 0xC: RESERVED_5 0xD: RESERVED_6 0xE: RESERVED_7 0xF: RESERVED_8
23	TEMP_ADJUST_RFSH	SW: RW, HW: R When used, sdTemp pin inputs automatically adjust the refresh rate. 0x0: ignore (default) 0x1: use
22:14	TREFI	SW: RW, HW: R Number of clock cycle delay (in tcxo clock cycles) between auto-refresh commands (when MODE_AUTO_RFSH is set to autoRef) or directed auto-refresh commands (when MODE_AUTO_RFSH is set to directedAutoRef). This is required to be set to the "desired tREFI" -1 tcxo cycles.
13:12	MODE_AUTO_RFSH	SW: RW, HW: R Specifies the refresh mode. For normal operation, this needs to be set to "01". 0x0: no refreshing 0x1: autoRef (default) 0x2: RESERVED_1 0x3: RESERVED_2
11:3	RESERVED_11_3	

EBI1_CH1_DDR_AUTO_RFSH_CNTL (cont.)

Bits	Name	Description
2:0	REFRESH_IDLE_ACROSS_RANKS	SW: RW, HW: R Number of clock cycles between auto-refresh commands across ranks. This is to avoid cases wherein the auto refreshes to 2 ranks occur concurrently/too close which might cause a current spike. 0x0: RESERVED 0x1: 1 cycle 0x2: 2 cycles 0x3: 3 cycles 0x4: 4 cycles 0x5: 5 cycles 0x6: 6 cycles 0x7: 7 cycles (default)

0x00D800A8 EBI1_CH1_DDR_SELF_RFSH_CNTL

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000200

DDR SDRAM Self-Refresh Control Register

EBI1_CH1_DDR_SELF_RFSH_CNTL

Bits	Name	Description
31:28	RESERVED_31_28	Reserved
27	HW_SELF_RFSH_EN_RANK1	SW: RW, HW: R Enables HW to look for no activity for rank1 and trigger an idle timer specified based on the value of HW_SELF_RFSH_TIMER. If there is no activity still and the timer expires, the HW will initiate entry to self refresh mode. 0x0: Disabled (default) 0x1: Enabled
26	HW_SELF_RFSH_EN_RANK0	SW: RW, HW: R Enables HW to look for no activity for rank0 and trigger an idle timer specified based on the value of HW_SELF_RFSH_TIMER. If there is no activity still and the timer expires, the HW will initiate entry to self refresh mode. 0x0: Disabled (default) 0x1: Enabled
25:20	RESERVED_25_20	

EBI1_CH1_DDR_SELF_RFSH_CNTL (cont.)

Bits	Name	Description
19:8	HW_SELF_RFSH_TIMER	SW: RW, HW: R Count idle tcxo cycles before entering self refresh. The timer is based on XO clock frequency. Valid only when HW_SELF_RFSH_EN is set. 'h000 : RESERVED 'h001 : RESERVED 'h002 : 2 cycles (default)
7:0	RESERVED_7_0	

0x00D800B0 EBI1_CH1_DDR_PMON_EVENT_CNTL0

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x3EF87BFF

DDR SDRAM Performance Monitor Event Control Register

EBI1_CH1_DDR_PMON_EVENT_CNTL0

Bits	Name	Description
31	RESERVED_31	
30	EVENTS_ENABLE	SW: RW, HW: R Global Event Enable bit
29:28	EVENT0_TRANS_MATCH	SW: RW, HW: R Counts the number of AXI Read or Write transactions or both. 0x0: Reserved 0x1: Read 0x2: Write 0x3: Read_or_Write (default)
27:25	EVENT0_PRIORITY_MATCH	SW: RW, HW: R Additional Match on priority value/range for Event0 0x0: Reserved 0x1: PVAL0 0x2: PVAL1 0x3: PVAL0_or_PVAL1 0x4: PVAL2 0x5: PVAL0_or_PVAL2 0x6: PVAL1_or_PVAL2 0x7: PVAL0_or_PVAL1_or_PVAL2 (default)

EBI1_CH1_DDR_PMON_EVENT_CNTL0 (cont.)

Bits	Name	Description
24	EVENT0_CMD_STARVED_MATCH	SW: RW, HW: R Additional Match on command starved for Event0. Note that command starvation is only applicable to read transactions 0x1: Match_Enable 0x0: Ignore (default)
23:21	EVENT0_PAGE_ATTR_MATCH	SW: RW, HW: R Additional Match on whether the transaction is a page hit or miss or conflict for Event0 0x0: Reserved 0x1: HIT 0x2: MISS 0x3: HIT_or_MISS 0x4: CONFLICT 0x5: HIT_or_CONFLICT 0x6: MISS_or_CONFLICT 0x7: HIT_or_MISS_or_CONFLICT (default)
20:19	EVENT0_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event0 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
18:11	EVENT0_BANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to which bank(s) for Event0 Others : Similar decode for all 8 banks 0x0: Reserved 0x1: Bank0 0x2: Bank1 0x3: Bank0_or_Bank1 0x4: Bank2 0x5: Bank0_or_Bank2 0x6: Bank1_or_Bank2 0x7: Bank0_or_Bank1_or_Bank2 0x8: Bank3 0x9: Bank0_or_Bank3 0xA: Bank1_or_Bank3 0xB: Bank0_or_Bank1_or_Bank3 0xC: Bank2_or_Bank3 0xD: Bank0_or_Bank2_or_Bank3 0xE: Bank1_or_Bank2_or_Bank3 0xF: Any_Banks0_3 (default)
10	RESERVED_10	

EBI1_CH1_DDR_PMON_EVENT_CNTL0 (cont.)

Bits	Name	Description
9:2	EVENT12_TRANS_MATCH	SW: RW, HW: R Counts the number of DDR1x clock cycles where in the rank is refreshed ahead and matches one or more of the following. Bit 0 indicates if Rfsh Ahead val of 0 is matched Bit 1 indicates if Rfsh Ahead val of 1 is matched Bit 2 indicates if Rfsh Ahead val of 2 is matched Bit 3 indicates if Rfsh Ahead val of 3 is matched Bit 4 indicates if Rfsh Ahead val of 4 is matched Bit 5 indicates if Rfsh Ahead val of 5 is matched Bit 6 indicates if Rfsh Ahead val of 6 is matched Bit 7 indicates if Rfsh Ahead val of 7 is matched **NOTE** A combination of 1's in the vector indicates an OR condition. e.g., 0000_1110 indicates a required refresh ahead range of 1-3. 0xFF: Any Rfsh Ahead (default)
1:0	EVENT12_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event12 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)

0x00D800B4 EBI1_CH1_DDR_PMON_EVENT0_MID_MATCH

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR SDRAM Performance Monitor Event0 MID Match Register

EBI1_CH1_DDR_PMON_EVENT0_MID_MATCH

Bits	Name	Description
31:16	EVENT0_MID_VAL_MATCH	SW: RW, HW: R Match the MID value for Event0. This is only applicable/useful if the transaction type match is a read. For writes this field will be ignored.
15:0	EVENT0_MID_MATCH_EN_MASK	SW: RW, HW: R Match enable mask for MID for Event0

0x00D800B8 EBI1_CH1_DDR_PMON_EVENT_CNTL1

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x3EF87800

DDR SDRAM Performance Monitor Event Control Register

EBI1_CH1_DDR_PMON_EVENT_CNTL1

Bits	Name	Description
31:30	RESERVED_31_30	
29:28	EVENT1_TRANS_MATCH	SW: RW, HW: R Counts the number of AXI Read or Write transactions or both. 0x0: Reserved 0x1: Read 0x2: Write 0x3: Read_or_Write (default)
27:25	EVENT1_PRIORITY_MATCH	SW: RW, HW: R Additional Match on priority value/range for Event1 0x0: Reserved 0x1: PVAL0 0x2: PVAL1 0x3: PVAL0_or_PVAL1 0x4: PVAL2 0x5: PVAL0_or_PVAL2 0x6: PVAL1_or_PVAL2 0x7: PVAL0_or_PVAL1_or_PVAL2 (default)
24	EVENT1_CMD_STARVED_MATCH	SW: RW, HW: R Additional Match on command starved for Event1. Note that command starvation is only applicable to read transactions 0x1: Match_Enable 0x0: Ignore (default)
23:21	EVENT1_PAGE_ATTR_MATCH	SW: RW, HW: R Additional Match on whether the transaction is a page hit or miss or conflict for Event1 0x0: Reserved 0x1: HIT 0x2: MISS 0x3: HIT_or_MISS 0x4: CONFLICT 0x5: HIT_or_CONFLICT 0x6: MISS_or_CONFLICT 0x7: HIT_or_MISS_or_CONFLICT (default)

EBI1_CH1_DDR_PMON_EVENT_CNTL1 (cont.)

Bits	Name	Description
20:19	EVENT1_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event1 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
18:11	EVENT1_BANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to which bank(s) for Event1 Others : Similar decode for all 8 banks 0x0: Reserved 0x1: Bank0 0x2: Bank1 0x3: Bank0_or_Bank1 0x4: Bank2 0x5: Bank0_or_Bank2 0x6: Bank1_or_Bank2 0x7: Bank0_or_Bank1_or_Bank2 0x8: Bank3 0x9: Bank0_or_Bank3 0xA: Bank1_or_Bank3 0xB: Bank0_or_Bank1_or_Bank3 0xC: Bank2_or_Bank3 0xD: Bank0_or_Bank2_or_Bank3 0xE: Bank1_or_Bank2_or_Bank3 0xF: Any_Banks0_3 (default)
10:0	RESERVED_10_0	

0x00D800BC EBI1_CH1_DDR_PMON_EVENT1_MID_MATCH

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR SDRAM Performance Monitor Event1 MID Match Register

EBI1_CH1_DDR_PMON_EVENT1_MID_MATCH

Bits	Name	Description
31:16	EVENT1_MID_VAL_MATCH	SW: RW, HW: R Match the MID value for Event1. This is only applicable/useful if the transaction type match is a read. For writes this field will be ignored.

EBI1_CH1_DDR_PMON_EVENT1_MID_MATCH (cont.)

Bits	Name	Description
15:0	EVENT1_MID_MATCH_EN_MASK	SW: RW, HW: R Match enable mask for MID for Event1

0x00D800C0 EBI1_CH1_DDR_PMON_EVENT_CNTL2

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x3EF87FFE

DDR SDRAM Performance Monitor Event Control Register

EBI1_CH1_DDR_PMON_EVENT_CNTL2

Bits	Name	Description
31:30	RESERVED_31_30	
29:28	EVENT2_TRANS_MATCH	SW: RW, HW: R Counts the number of AXI Read or Write transactions or both. 0x0: Reserved 0x1: Read 0x2: Write 0x3: Read_or_Write (default)
27:25	EVENT2_PRIORITY_MATCH	SW: RW, HW: R Additional Match on priority value/range for Event2 0x0: Reserved 0x1: PVAL0 0x2: PVAL1 0x3: PVAL0_or_PVAL1 0x4: PVAL2 0x5: PVAL0_or_PVAL2 0x6: PVAL1_or_PVAL2 0x7: PVAL0_or_PVAL1_or_PVAL2 (default)
24	EVENT2_CMD_STARVED_MATCH	SW: RW, HW: R Additional Match on command starved for Event2. Note that command starvation is only applicable to read transactions 0x1: Match_Enable 0x0: Ignore (default)

EBI1_CH1_DDR_PMON_EVENT_CNTL2 (cont.)

Bits	Name	Description
23:21	EVENT2_PAGE_ATTR_MATCH	SW: RW, HW: R Additional Match on whether the transaction is a page hit or miss or conflict for Event2 0x0: Reserved 0x1: HIT 0x2: MISS 0x3: HIT_or_MISS 0x4: CONFLICT 0x5: HIT_or_CONFLICT 0x6: MISS_or_CONFLICT 0x7: HIT_or_MISS_or_CONFLICT (default)
20:19	EVENT2_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event2 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
18:11	EVENT2_BANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to which bank(s) for Event2 Others : Similar decode for all 8 banks 0x0: Reserved 0x1: Bank0 0x2: Bank1 0x3: Bank0_or_Bank1 0x4: Bank2 0x5: Bank0_or_Bank2 0x6: Bank1_or_Bank2 0x7: Bank0_or_Bank1_or_Bank2 0x8: Bank3 0x9: Bank0_or_Bank3 0xA: Bank1_or_Bank3 0xB: Bank0_or_Bank1_or_Bank3 0xC: Bank2_or_Bank3 0xD: Bank0_or_Bank2_or_Bank3 0xE: Bank1_or_Bank2_or_Bank3 0xF: Any_Banks0_3 (default)

EBI1_CH1_DDR_PMON_EVENT_CNTL2 (cont.)

Bits	Name	Description
10:8	EVENT13_TRANS_MATCH	SW: RW, HW: R Counts the number of DDR1x clock cycles where in the rank(s) is in one or more of the following states - clock stop, power down, self refresh, idle, etc. 0x0: Reserved 0x1: Clock_Stop 0x2: Pwr_Down 0x3: Clock_Stop_or_Pwr_Down 0x4: Clock_Stop_and_Pwr_Down 0x5: Hardware Self_Refresh 0x6: Software Self_Refresh 0x7: Idle (default)
7:6	EVENT13_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event13 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
5:3	EVENT14_TRANS_MATCH	SW: RW, HW: R Counts the number of DDR1x clock cycles where in the rank(s) is in one or more of the following states - clock stop, power down, self refresh, idle, etc. 0x0: Reserved 0x1: Clock_Stop 0x2: Pwr_Down 0x3: Clock_Stop_or_Pwr_Down 0x4: Clock_Stop_and_Pwr_Down 0x5: Hardware Self_Refresh 0x6: Software Self_Refresh 0x7: Idle (default)
2:1	EVENT14_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event14 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
0	RESERVED_0	

0x00D800C4 EBI1_CH1_DDR_PMON_EVENT2_MID_MATCH

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR SDRAM Performance Monitor Event2 MID Match Register

EBI1_CH1_DDR_PMON_EVENT2_MID_MATCH

Bits	Name	Description
31:16	EVENT2_MID_VAL_MATCH	SW: RW, HW: R Match the MID value for Event2. This is only applicable/useful if the transaction type match is a read. For writes this field will be ignored.
15:0	EVENT2_MID_MATCH_EN_MASK	SW: RW, HW: R Match enable mask for MID for Event2

0x00D800C8 EBI1_CH1_DDR_PMON_EVENT_CNTL3

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x3EF87F30

DDR SDRAM Performance Monitor Event Control Register

EBI1_CH1_DDR_PMON_EVENT_CNTL3

Bits	Name	Description
31:30	RESERVED_31_30	
29:28	EVENT3_TRANS_MATCH	SW: RW, HW: R Counts the number of AXI Read or Write transactions or both. 0x0: Reserved 0x1: Read 0x2: Write 0x3: Read_or_Write (default)
27:25	EVENT3_PRIORITY_MATCH	SW: RW, HW: R Additional Match on priority value/range for Event3 0x0: Reserved 0x1: PVAL0 0x2: PVAL1 0x3: PVAL0_or_PVAL1 0x4: PVAL2 0x5: PVAL0_or_PVAL2 0x6: PVAL1_or_PVAL2 0x7: PVAL0_or_PVAL1_or_PVAL2 (default)

EBI1_CH1_DDR_PMON_EVENT_CNTL3 (cont.)

Bits	Name	Description
24	EVENT3_CMD_STARVED_MATCH	SW: RW, HW: R Additional Match on command starved for Event3. Note that command starvation is only applicable to read transactions 0x1: Match_Enable 0x0: Ignore (default)
23:21	EVENT3_PAGE_ATTR_MATCH	SW: RW, HW: R Additional Match on whether the transaction is a page hit or miss or conflict for Event3 0x0: Reserved 0x1: HIT 0x2: MISS 0x3: HIT_or_MISS 0x4: CONFLICT 0x5: HIT_or_CONFLICT 0x6: MISS_or_CONFLICT 0x7: HIT_or_MISS_or_CONFLICT (default)
20:19	EVENT3_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event3 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
18:11	EVENT3_BANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to which bank(s) for Event3 Others : Similar decode for all 8 banks 0x0: Reserved 0x1: Bank0 0x2: Bank1 0x3: Bank0_or_Bank1 0x4: Bank2 0x5: Bank0_or_Bank2 0x6: Bank1_or_Bank2 0x7: Bank0_or_Bank1_or_Bank2 0x8: Bank3 0x9: Bank0_or_Bank3 0xA: Bank1_or_Bank3 0xB: Bank0_or_Bank1_or_Bank3 0xC: Bank2_or_Bank3 0xD: Bank0_or_Bank2_or_Bank3 0xE: Bank1_or_Bank2_or_Bank3 0xF: Any_Banks0_3 (default)

EBI1_CH1_DDR_PMON_EVENT_CNTL3 (cont.)

Bits	Name	Description
10:8	EVENT15_TRANS_MATCH	SW: RW, HW: R Counts the number of DDR1x clock cycles where in the rank(s) is in one or more of the following states - clock stop, power down, self refresh, idle, etc. 0x0: Reserved 0x1: Clock_Stop 0x2: Pwr_Down 0x3: Clock_Stop_or_Pwr_Down 0x4: Clock_Stop_and_Pwr_Down 0x5: Hardware Self_Refresh 0x6: Software Self_Refresh 0x7: Idle (default)
7:6	RESERVED_7_6	
5:4	EVENT15_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event15 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
3:0	RESERVED_3_0	

0x00D800CC EBI1_CH1_DDR_PMON_EVENT3_MID_MATCH

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR SDRAM Performance Monitor Event3 MID Match Register

EBI1_CH1_DDR_PMON_EVENT3_MID_MATCH

Bits	Name	Description
31:16	EVENT3_MID_VAL_MATCH	SW: RW, HW: R Match the MID value for Event3. This is only applicable/useful if the transaction type match is a read. For writes this field will be ignored.
15:0	EVENT3_MID_MATCH_EN_MASK	SW: RW, HW: R Match enable mask for MID for Event3

0x00D800D0 EBI1_CH1_DDR_PMON_EVENT_CNTL4

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x7F30F000

DDR SDRAM Performance Monitor Event Control Register

EBI1_CH1_DDR_PMON_EVENT_CNTL4

Bits	Name	Description
31	RESERVED_31	
30:24	EVENT10_TRANS_MATCH	SW: RW, HW: R Counts the number of memory transactions which match the following. Use Bit 0 to indicate if Activates are to be included. Use Bit 1 to indicate if Reads are to be included. Use Bit 2 to indicate if Writes are to be included. Use Bit 3 to indicate if Bst's are to be included. Use Bit 4 to indicate if Auto Refreshes are included Use Bit 5 to indicate if Precharge All is included. Use Bit 6 to indicate if Per-Bank Precharge is included. **NOTE** A combination of 1's in the vector indicates an OR condition. e.g., 0000_011 indicates match condition would trigger on an Activate or Read command. 0000_000 : Reserved 1111_1111 : All of the above memory commands (default)
23:22	RESERVED_23_22	
21:20	EVENT10_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event10 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)

EBI1_CH1_DDR_PMON_EVENT_CNTL4 (cont.)

Bits	Name	Description
19:12	EVENT10_BANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to which bank(s) for Event10 Others : Similar decode for all 8 banks 0x0: Reserved 0x1: Bank0 0x2: Bank1 0x3: Bank0_or_Bank1 0x4: Bank2 0x5: Bank0_or_Bank2 0x6: Bank1_or_Bank2 0x7: Bank0_or_Bank1_or_Bank2 0x8: Bank3 0x9: Bank0_or_Bank3 0xA: Bank1_or_Bank3 0xB: Bank0_or_Bank1_or_Bank3 0xC: Bank2_or_Bank3 0xD: Bank0_or_Bank2_or_Bank3 0xE: Bank1_or_Bank2_or_Bank3 0xF: Any_Banks0_3 (default)
11:0	RESERVED_11_0	

0x00D800D4 EBI1_CH1_DDR_PMON_EVENT_CNTL5

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x7F30F000

DDR SDRAM Performance Monitor Event Control Register

EBI1_CH1_DDR_PMON_EVENT_CNTL5

Bits	Name	Description
31	RESERVED_31	

EBI1_CH1_DDR_PMON_EVENT_CNTL5 (cont.)

Bits	Name	Description
30:24	EVENT11_TRANS_MATCH	SW: RW, HW: R Counts the number of memory transactions which match the following. Use Bit 0 to indicate if Activates are to be included. Use Bit 1 to indicate if Reads are to be included. Use Bit 2 to indicate if Writes are to be included. Use Bit 3 to indicate if Bst's are to be included. Use Bit 4 to indicate if Auto Refreshes are included Use Bit 5 to indicate if Precharge All is included. Use Bit 6 to indicate if Per-Bank Precharge is included. **NOTE** A combination of 1's in the vector indicates an OR condition. e.g., 0000_011 indicates match condition would trigger on an Activate or Read command. 0000_000: Reserved 1111_111: All of the above memory commands (default)
23:22	RESERVED_23_22	
21:20	EVENT11_RANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to Rank 0/1 for Event11 0x0: Reserved 0x1: Rank0 0x2: Rank1 0x3: Rank0_or_Rank1 (default)
19:12	EVENT11_BANK_MATCH	SW: RW, HW: R Additional Match on whether the transaction is to which bank(s) for Event11 Others : Similar decode for all 8 banks 0x0: Reserved 0x1: Bank0 0x2: Bank1 0x3: Bank0_or_Bank1 0x4: Bank2 0x5: Bank0_or_Bank2 0x6: Bank1_or_Bank2 0x7: Bank0_or_Bank1_or_Bank2 0x8: Bank3 0x9: Bank0_or_Bank3 0xA: Bank1_or_Bank3 0xB: Bank0_or_Bank1_or_Bank3 0xC: Bank2_or_Bank3 0xD: Bank0_or_Bank2_or_Bank3 0xE: Bank1_or_Bank2_or_Bank3 0xF: Any_Banks0_3 (default)
11:0	RESERVED_11_0	

0x00D800D8 EBI1_CH1_DDR_TEST_MUX

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR SDRAM Test Bus Mux Register

The following are the contents of the 32-bit test bus for each test bus select value. This only applies if the test bus is enabled.

- test_bus_sel == rd_vld_cmdptr0 (Hierarchy: hsddrx_ddrValidGen.sv)

assign o_testbus_rd_vld_cmdptr0 = {rank_ready_cs, i_rdcmdptrfifo_cmdptr, i_rdcmdptrfifo_empty, i_rdcmdptrfifo_rd_en, rdvalid_ddr_noptr, rdvalid_ddr_early, i_rdvalid_ddr_clear, 1'b0};

- test_bus_sel == rd_vld_cmdptr1 (Hierarchy: hsddrx_ddrValidGen.sv)

assign o_testbus_rd_vld_cmdptr1 = {rank_ready_cs, i_rdcmdptrfifo_cmdptr, i_rdcmdptrfifo_empty, i_rdcmdptrfifo_rd_en, rdvalid_ddr_noptr, i_rdvalid_ddr_set_toggle, copy_valid_ddr_clear_toggle, 1'b0};

- test_bus_sel == wr_vld_cmdptr (Hierarchy: hsddrx_ddrValidGen.sv)

assign o_testbus_wr_vld_cmdptr = {i_wrcmdptrfifo_cmdptr, i_wrcmdptrfifo_empty, i_wrcmdptrfifo_rd_en, i_wrvalid_ddr_clear, wrcmdptr_received_D, {11{1'b0}}};

- test_bus_sel == rd_runnable (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_rd_runnable = {rank_ready_csn, i_rdcmdptrfifo_cmdptr, i_rdcmdptrfifo_empty, rdcmdptrfifo_rd_en, rdvalid_ddr, rd_no_mem_runnable_axi_vec, rd_runnable_axi_vec, 1'b0};

- test_bus_sel == wr_runnable (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_wr_runnable = {rank_ready_csn, i_wrcmdptrfifo_cmdptr, i_wrcmdptrfifo_empty, wrcmdptrfifo_rd_en, wrvalid_ddr, wr_runnable_axi_vec, mod_runnable_exist_csn, interrupt, 6'b000000};

- test_bus_sel == ahb_csr (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_ahb_csr = {i_csr_addr[19:0], i_csr_req, i_csr_sync_mode, i_csr_wr, csr_ack, rank_ready_csn, 6'b000000};

- test_bus_sel == cmd_arbiter (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_cmd_arbiter = {reset_ddr_1x, rank_ready_csn, i_rdcmdptrfifo_empty, rdcmdptrfifo_rd_en, i_wrcmdptrfifo_empty, wrcmdptrfifo_rd_en, req_act_cmd, req_col_cmd_fsm, col_sel_wr_rd_cmdbuf, req_col_cmd, req_manual_cmd, req_precharge_cmd, loc_req_refresh_cmd, loc_self_refresh_req, grant_act_cmd, grant_col_cmd, grant_manual_cmd, grant_precharge_cmd, loc_grant_refresh_cmd, loc_self_refresh_grant, loc_in_self_refresh, loc_ddr_cke, loc_ddr_drive_ck, 2'b00};

- test_bus_sel == act_pchg_rfsh_addr (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_act_pchg_rfsh_addr = {rank_ready_csn, loc_rank_idle_exclude_rfsh, page_open_valid, page_close_valid, refresh_cmd_valid, loc_cmd_bank_addr, loc_cmd_rank_addr, cmd_row_addr};

- test_bus_sel == col_addr (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_col_addr = {rank_ready_csn, loc_rank_idle_exclude_rfsh, ddr_ca_even, loc_ddr_ba, loc_ddr_cs_n, req_col_cmd_fsm, col_sel_wr_rd_cmdbuf, req_col_cmd, drive_col_bst, drive_col_cmd, issue_srr_req, loc_in_dpd};

- test_bus_sel == act_algorithm0 (Hierarchy: hsddrx_actReqGen.sv)

assign o_testbus_act_algorithm0 = {i_rank_ready_cs, valid_act_runnable_rd_vec, valid_act_runnable_wr_vec, i_block_ddr_act_col_cmds_urg_rfsh_srr, i_block_ddr_cmds_urg_rfsh_srr, i_ddr_cmd_bus_idle_req, o_req_act_cmd, i_loc_cmd_bank_addr, i_loc_cmd_rank_addr};

- test_bus_sel == act_algorithm1 (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_act_algorithm1 = {rank_ready_csn, req_act_cmd, act_sel_wr_rd_cmdbuf, act_rdcmdbuf_ptr, act_wrcmdbuf_ptr, loc_cmd_bank_addr, loc_cmd_rank_addr, block_ddr_cmds_urg_rfsh_srr, block_ddr_act_col_cmds_urg_rfsh_srr, ddr_cmd_bus_idle_req, {9{1'b0}}};

- test_bus_sel == pchg_algorithm (Hierarchy: hsddrx_prechargeReqGen.sv)

assign o_testbus_pchg_algorithm = {i_rank_ready_cs, loc_precharge_bank_addr, precharge_rank_addr, req_precharge_all, o_req_precharge_cmd, i_block_ddr_cmds_urg_rfsh_srr, i_ddr_cmd_bus_idle_req, avail_valid_precharge_req_urg_refresh, avail_valid_precharge_req_trasmax_timer, avail_valid_precharge_req_page_mgmt_timer, avail_valid_precharge_req_srr, avail_valid_precharge_req_rank_idle, avail_valid_precharge_req_resource_unavail, loc_rank_available_cmd_exec, prefer_writes, selected_rd_cmdptr_precharge_res_unavail, selected_wr_cmdptr_precharge_res_unavail, loc_rank_idle_timer_expired, {5{1'b0}}};

- test_bus_sel == rfsh_algorithm0 (Hierarchy: hsddrx_refreshReqGen.sv)

assign o_testbus_rfsh_algorithm0 = {refresh_all_bank_mode, loc_grant_refresh_cmd, loc_sync_refresh_req_pend, loc_refresh_ahead_counter, loc_urgent_refresh_req_valid, 1'b0};

- test_bus_sel == rfsh_algorithm1 (Hierarchy: hsddrx_refreshReqGen.sv)

assign o_testbus_rfsh_algorithm1 = {loc_refresh_bank_addr, loc_req_refresh_cmd, loc_update_refresh_rate, loc_refresh_interval_timer};

- test_bus_sel == axi_col_algorithm (Hierarchy: hsddrx_colReqGen.sv)

assign o_testbus_axi_col_algorithm = {i_rank_ready_cs, col_rd_cmdptr, col_wr_cmdptr, no_col_req, col_sel_wr_rd_cmdbuf[0], req_col_cmd_fsm, i_col_cmd_en, i_ddr_cmd_bus_idle_req, i_rd_idle_req, i_wr_idle_req, valid_runnable_col_rd_vec, valid_runnable_col_wr_vec, wait_hp_req};

- test_bus_sel == manual_cmd_algorithm (Hierarchy: hsddrx_manualReqGen.sv)

assign o_testbus_manual_cmd_algorithm = {i_rank_ready_cs, 1'b0,o_manual_cmd_enc, loc_manual_cmd_rank_en, o_req_manual_cmd, i_grant_manual_cmd, loc_rank_idle, loc_in_dpd, loc_dpd_valid_cs, valid_dpd_entry, 16'h0000};

- test_bus_sel == self_rfsh_algorithm0 (Hierarchy: hsddrx_selfRefresh.sv)

assign o_testbus_self_rfsh_algorithm0 = {2'b00,current_state,2'b00,next_state, 1'b0,sw_self_rfsh_valid_req, 1'b0,self_refresh_req, 1'b0,i_self_refresh_grant, 1'b0,rank_available_cmd_exec, 1'b0,wakeup_sr, 1'b0,in_self_refresh, 1'b0,sr_exit_non_rd_expired, 1'b0,sr_exit_rd_expired, 1'b0,pend_self_refresh_req, 1'b0,i_ddr_cke, 1'b0,i_ddr_drive_ck, 1'b0,valid_sw_self_refresh_exit};

- test_bus_sel == self_rfsh_algorithm1 (Hierarchy: hsddrx_selfRefresh.sv)

assign o_testbus_self_rfsh_algorithm1 = {2'b00,current_state,2'b00,next_state, 1'b0,hw_self_rfsh_valid_req, 1'b0,self_refresh_req, 1'b0,i_self_refresh_grant, 1'b0,rank_available_cmd_exec, 1'b0,wakeup_sr, 1'b0,in_self_refresh, 1'b0,sr_exit_non_rd_expired, 1'b0,sr_exit_rd_expired, 1'b0,pend_self_refresh_req, 1'b0,i_ddr_cke, 1'b0,i_ddr_drive_ck, 1'b0,hw_self_refresh_idle_timer_expired};

- test_bus_sel == clock_stop_pwr_dwn (Hierarchy: hsddrx_clockStopPowerDown.sv)

assign o_testbus_cspd = {2'b00,current_state,2'b00,next_state, 1'b0,enter_clock_stop, 1'b0,enter_power_down, 1'b0,ddr_cke_cspd, 1'b0,ddr_drive_ck_cspd, 1'b0,i_ddr_cke, 1'b0,i_ddr_drive_ck, {12{1'b0}}};

- test_bus_sel == rank_timers (Hierarchy: hsddrx_ddrRankTimers.sv)

assign o_testbus_rank_timers = {4'b0000,i_cmd_bank_addr, 1'b0,i_cmd_rank_addr, i_page_open_valid, i_refresh_cmd_valid, 1'b0,loc_perbank_rfsh_satisfied_vec, 1'b0,loc_tRRD_satisfied_vec, {8{1'b0}},4'b0000,tRFC_satisfied_vec};

- test_bus_sel == open_pages_table0 (Hierarchy: hsddrx_openPagesTable.sv)

assign o_testbus_open_pages_table0 = {{8{1'b0}}, 4'b0000, opt_col_cmd_in_progress_Q[0],{8{1'b0}}, 4'b0000, opt_valid_Q[0]};

- test_bus_sel == open_pages_table1 (Hierarchy: hsddrx_openPagesTable.sv)

assign o_testbus_open_pages_table1 = {{8{1'b0}}, 4'b0000, opt_one_trans_exec_Q[0],

{8{1'b0}}, 4'b0000, opt_valid_Q[0]};

- test_bus_sel == cdc_iocal_req_ack (Hierarchy: hsddrx_iocalcdcIntf.sv)

  assign o_testbus_cdc_iocal_cdc_req = {i_rank_ready_cs, sync_cdc_update_req_ca, sync_cdc_update_req_rd, sync_cdc_update_req_wr, sync_iocal_update_req_ctrl, sync_iocal_update_req_data, loc_cdc_update_ack_ca, loc_cdc_update_ack_rd, loc_cdc_update_ack_wr, loc_iocal_update_ack_ctrl, loc_iocal_update_ack_data, ddr_cmd_bus_idle_req, rd_idle_req, wr_idle_req, i_act_cmd_rdy_calib, i_col_cmd_rdy_calib, i_manual_cmd_rdy_calib, 1'b0, i_rddata_rdy_calib, 1'b0, i_wrdata_rdy_calib, i_col_req_idle, i_req_col_cmd_fsm, i_col_sel_wr_rd_cmdbuf, i_grant_act_cmd, i_grant_col_cmd, i_grant_precharge_cmd, 1'b0,i_grant_refresh_cmd, 1'b0,i_grant_self_refresh_cmd};

- test_bus_sel == mem_cmd_gen0 (Hierarchy: hsddrx_memCmdGen.sv)

assign o_testbus_mem_cmd_gen0 = {i_rank_ready_cs, i_req_col_cmd_fsm, alen_counter_Q, axi_col_trans_aburst_req_Q, axi_col_trans_addr_byte_Q, axi_col_trans_alen_Q, axi_col_trans_asize_Q, axi_col_trans_readmerge_Q, axi_col_trans_wr_Q, mem_bl_count_Q, loc_col_cmd_en, loc_mem_cmd_valid, i_mem_cmd_accept, loc_mem_bl_dw_valid_serial, mem_cmd_cas_in_prog, mod_mem_cmd_last_cas, mem_col_last_beat_cmd_early};

- test_bus_sel == mem_cmd_gen1 (Hierarchy: hsddrx_memCmdGen.sv)

assign o_testbus_mem_cmd_gen1 = {i_rank_ready_cs, i_req_col_cmd_fsm, axi_col_trans_aburst_req_Q, 1'b0,axi_col_trans_addr_bank_Q, axi_col_trans_addr_col_Q, axi_col_trans_addr_rank_Q, axi_col_trans_addr_row_Q};

- test_bus_sel == col_fsm0 (Hierarchy: hsddrx_colFsm.sv)

assign o_testbus_col_fsm0 = {i_rank_ready_cs, current_state, next_state, i_req_col_cmd_fsm, i_mem_cmd_cas_in_prog, i_mem_cmd_valid, mem_cmd_accept, i_mem_col_last_beat_cmd_reg, i_mem_col_write, i_timing_satisfied, i_use_bst_cmd_to_int_rd, i_use_bst_cmd_to_int_wr, i_use_next_rd_cmd_to_int, i_use_next_wr_cmd_to_int, drive_col_bst, drive_col_rd, drive_col_wr, req_col_cmd, 1'b0};

- test_bus_sel == col_fsm1 (Hierarchy: hsddrx_colFsm.sv)

assign o_testbus_col_fsm1 = {current_state, next_state, i_req_col_cmd_fsm, i_mem_cmd_cas_in_prog, mem_cmd_accept, load_multiT_timer, i_multiT_timer_expired, mem_cmd_valid_rd, mem_cmd_valid_wr, i_use_bst_cmd_to_int_rd, i_use_bst_cmd_to_int_wr, i_use_next_rd_cmd_to_int, i_use_next_wr_cmd_to_int, drive_col_bst_cs, drive_col_bst_except_cs, drive_col_rd_cs, drive_col_rd_except_cs, drive_col_wr_cs, drive_col_wr_except_cs, req_col_cmd};

- test_bus_sel == col_cmd_int_cntl (Hierarchy: hsddrx_colCmdInterruptCtrl.sv)

assign o_testbus_col_cmd_int_cntl = {qual_almost_expired_bl_dw, cmd_int_qual, curr_cmd_can_be_int, expired_bl_dw, i_mem_cmd_valid, i_mem_col_rank, i_mem_col_write, i_mem_col_valid_curr_cmd, i_mem_col_rank_curr_cmd, i_mem_col_write_curr_cmd, int_boundary_met, int_every_cycle, int_every_fourth_cycle, int_every_second_cycle, loc_use_bst_cmd_to_int_rd, loc_use_bst_cmd_to_int_wr, rd_cmd_int_by_rd, wr_cmd_int_by_wr, 14{1'b0}}};

- test_bus_sel == wr_data (Hierarchy: hsddrx_wrDataCtrl.sv)

assign o_testbus_wrdata = {i_rank_ready_cs, i_req_col_cmd_fsm, i_drive_col_wr, tburst_expired_wr, i_drive_col_wr_cs, start_bl_cnt, stop_bl_cnt, stop_bl_cnt_reg, drive_col_wr, ddr_drive_wr_dqs, ddr_wr_2dm, loc_load_tWR_valid, wrdatabuf_request, loc_wrdatabuf_firstword, loc_wrdatabuf_cmdptr, loc_wrdatabuf_lineptr, loc_wrdatabuf_wordptr, 2'b00};

- test_bus_sel == rd_data (Hierarchy: hsddrx_rdData.v & hsddrx_rdDataCtrl.sv)

assign o_testbus_rddata1 = {tburst_expired_rd, capture_rd_fifo_wen, loc_pad_ie_dq, loc_pad_ie_dqs, loc_rd_data_keep_throw_fifo_wdata, loc_rd_data_keep_throw_fifo_wen, ie_capture_cntr_expired, ie_start_dly_cntr_expired, rd_data_capture_cntr_expired, rd_data_dly_cntr_expired, bst_col_cmd_reg, rd_col_cmd_reg, srr_rd_cmd_reg};

assign o_testbus_rddata0 = {capture_rd_fifo_empty, i_capture_rd_fifo_wen, 1'b0, 1'b0, {8{1'b0}}};

assign testbus_rddata = {testbus_rddata1,testbus_rddata0};

- test_bus_sel == ddr_bus0 (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_ddr_bus0 = {rank_ready_csn, ddr_ca_even, loc_ddr_ba, ddr_cas_n, ddr_cke, loc_ddr_cs_n, ddr_drive_ck, ddr_drive_wr_dqs, ddr_ras_n, ddr_we_n, pad_ie_dq, pad_oe_dq, pad_ie_dqs, pad_oe_dqs, 1'b0};

- test_bus_sel == ddr_bus1 (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_ddr_bus1 = {rank_ready_csn, loc_ddr_ba, ddr_cas_n, ddr_cke, loc_ddr_cs_n, ddr_drive_ck, ddr_drive_wr_dqs, ddr_ras_n, ddr_we_n, pad_ie_dq, pad_oe_dq, pad_ie_dqs, pad_oe_dqs, loc_ddr_odt, loc_pad_odt_dq, loc_pad_odt_dqs, loc_ddr_reset_n, loc_ddr_wr_2dm, 1'b0};

- test_bus_sel == ddr_bus2 (Hierarchy: hsddrx_ddrCntl.sv)

assign testbus_ddr_bus2 = {ddr_ca_even, ddr_ca_odd, pad_ie_dq, pad_oe_dq};

EBI1_CH1_DDR_TEST_MUX

Bits	Name	Description
31	ENABLE	SW: RW, HW: R Test Bus Enable. 0x0: Disable (ddr_test_bus drives 32'b0 default) 0x1: Enable (ddr_test_bus drives selected signals)
30:6	RESERVED_30_6	

EBI1_CH1_DDR_TEST_MUX (cont.)

Bits	Name	Description
5:0	TEST_BUS_SEL	SW: RW, HW: R Selects internally generated signals for observation on the ddr_test_bus. 0x0: rd_vld_cmdptr0 0x1: rd_vld_cmdptr1 0x2: wr_vld_cmdptr 0x3: rd_runnable 0x4: wr_runnable 0x5: ahb_csr 0x6: cmd_arbiter 0x7: act_pchg_rfsh_addr 0x8: col_addr 0x9: act_algorithm0 0xA: act_algorithm1 0xB: pchg_algorithm 0xC: rfsh_algorithm0 0xD: rfsh_algorithm1 0xE: axi_col_algorithm 0xF: manual_cmd_algorithm 0x10: self_rfsh_algorithm0 0x11: self_rfsh_algorithm1 0x12: clock_stop_pwr_dwn 0x13: rank_timers 0x14: open_pages_table0 0x15: open_pages_table1 0x16: cdc_iocal_req_ack 0x17: mem_cmd_gen0 0x18: mem_cmd_gen1 0x19: col_fsm0 0x1A: col_fsm1 0x1B: col_cmd_int_cntl 0x1C: wr_data 0x1D: rd_data 0x1E: ddr_bus0 0x1F: ddr_bus1 0x20: ddr_bus2

0x00D80100 EBI1_CH1_DDR_MRW0_HW_FREQ_SWITCH

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Write Control for HW Frequency Switch Register

This register is used/valid as part of HW based frequency switch if DDR_CMD_EXEC_OPT_2[UPDATE_MEM_LATENCY_ON_FREQ_SWITCH] is set.There is no rank select field as the mode register write command goes to all initialized ranks. If the memory latencies are required to be changed as part of frequency switching, SW would be required to program the correct Read/Write latency in the corresponding _ALT registers and also program this register to have HW perform an MRW with the updated latency values when a frequency switch request is being processed.

EBI1_CH1_DDR_MRW0_HW_FREQ_SWITCH

Bits	Name	Description
31:24	MRW_ADDR	SW: RW, HW: R Specify which mode register to access. Note that LPDDR2 supports up to 256 Mode registers. Hence the programmed MR_ADDR needs to be valid based on the specific SDRAM device. 0000_0000: MR (Mode Register or SR for LPDDR1) 0000_0001: EMR1 (Extended Mode Register 1) 0000_0010: EMR2 (Extended Mode Register 2) 0000_0011: EMR2 (Extended Mode Register 3) .....
23:21	RESERVED_23_21	
20	MRW_VALID	SW: RW, HW: R Indicates if the contents of this register are valid.
19:16	RESERVED_19_16	
15:0	MRW_DATA	SW: RW, HW: R Data for Mode Register Writes. SW needs to program the mode register based on the specific SDRAM device as the mapping of the 16-bits is different for different SDRAM device types.

0x00D80104 EBI1_CH1_DDR_MRW1_HW_FREQ_SWITCH

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Mode Register Write Control for HW Frequency Switch Register

This register is used/valid as part of HW based frequency switch if DDR_CMD_EXEC_OPT_2[UPDATE_MEM_LATENCY_ON_FREQ_SWITCH] is set.There is no rank select field as the mode register write command goes to all initialized ranks. If the memory latencies are required to be changed as part of frequency switching, SW would be required to program the correct Read/Write latency in the corresponding _ALT registers and also program this register to have HW perform an MRW with the updated latency values when a frequency switch request is being processed.

EBI1_CH1_DDR_MRW1_HW_FREQ_SWITCH

Bits	Name	Description
31:24	MRW_ADDR	SW: RW, HW: R Specify which mode register to access. Note that LPDDR2 supports up to 256 Mode registers. Hence the programmed MR_ADDR needs to be valid based on the specific SDRAM device. 0000_0000: MR (Mode Register or SR for LPDDR1) 0000_0001: EMR1 (Extended Mode Register 1) 0000_0010: EMR2 (Extended Mode Register 2) 0000_0011: EMR2 (Extended Mode Register 3) .....
23:21	RESERVED_23_21	
20	MRW_VALID	SW: RW, HW: R Indicates if the contents of this register are valid.
19:16	RESERVED_19_16	
15:0	MRW_DATA	SW: RW, HW: R Data for Mode Register Writes. SW needs to program the mode register based on the specific SDRAM device as the mapping of the 16-bits is different for different SDRAM device types.

0x00D80120 EBI1_CH1_DDR_DQCAL_RDATA_RANK1

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR DQ Calibration Read Data Register for Rank1

This register contains the DRAM mode register contents for a DQ calibration command triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] to Rank1. This is used to capture the read data from the SDRAM device's mode register for a read DQ calibration command for LPDDR2 or an MPR read command for PCDDR3. The DQS data bits 0, 8, 16 and 24 are only captured on each DQS edge. Hence for a memory burst length of 4 (LPDDR2 DQ calibration), only 16:0 bits of the field below have valid data. In case of PCDDR3 MPR read command (memory burst length of 8), all 32 bits of the field below are valid.

EBI1_CH1_DDR_DQCAL_RDATA_RANK1

Bits	Name	Description
31:0	DQCAL_RDATA	SW: R, HW: W Data for DQ Calibration Read for Rank1. The data captures the lowest bit for each byte across the memory burst. For example, each cycle of memory burst is 8 bytes of data - 1 bit for each byte is captured which is 8 bits for every cycle of DQS.

0x00D80124 EBI1_CH1_DDR_DQCAL_RDATA_RANK0

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR DQ Calibration Read Data Register for Rank0

This register contains the DRAM mode register contents for a DQ calibration command triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] to Rank0. This is used to capture the read data from the SDRAM device's mode register for a read DQ calibration command for LPDDR2 or an MPR read command for PCDDR3. The DQS data bits 0, 8, 16 and 24 are only captured on each DQS edge. Hence for a memory burst length of 4 (LPDDR2 DQ calibration), only 16:0 bits of the field below have valid data. In case of PCDDR3 MPR read command (memory burst length of 8), all 32 bits of the field below are valid.

EBI1_CH1_DDR_DQCAL_RDATA_RANK0

Bits	Name	Description
31:0	DQCAL_RDATA	SW: R, HW: W Data for DQ Calibration Read for Rank1. The data captures the lowest bit for each byte across the memory burst. For example, each cycle of memory burst is 8 bytes of data - 1 bit for each byte is captured which is 8 bits for every cycle of DQS.

0x00D80130 EBI1_CH1_DDR_DQCAL_STATUS_RANK1

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR DQ Calibration Status Register for Rank1

EBI1_CH1_DDR_DQCAL_STATUS_RANK1

Bits	Name	Description
31	DQCAL_COMPARE_BYTE3	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE3) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS
30	DQCAL_COMPARE_BYTE2	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE2) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS
29	DQCAL_COMPARE_BYTE1	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE1) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS
28	DQCAL_COMPARE_BYTE0	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE0) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS

EBI1_CH1_DDR_DQCAL_STATUS_RANK1 (cont.)

Bits	Name	Description
27	RESERVED_27	
26:24	NUM_DQS_PE_EDGES_RECD_BYTE3	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
23	RESERVED_23	
22:20	NUM_DQS_PE_EDGES_RECD_BYTE2	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
19	RESERVED_19	

EBI1_CH1_DDR_DQCAL_STATUS_RANK1 (cont.)

Bits	Name	Description
18:16	NUM_DQS_PE_EDGES_RECD_BYTE1	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
15	RESERVED_15	
14:12	NUM_DQS_PE_EDGES_RECD_BYTE0	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
11:9	NUM_DQS_NE_EDGES_RECD_BYTE3	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges

EBI1_CH1_DDR_DQCAL_STATUS_RANK1 (cont.)

Bits	Name	Description
8:6	NUM_DQS_NE_EDGES_RECD_BYTE2	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
5:3	NUM_DQS_NE_EDGES_RECD_BYTE1	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
2:0	NUM_DQS_NE_EDGES_RECD_BYTE0	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges

0x00D80134 EBI1_CH1_DDR_DQCAL_STATUS_RANK0

Type: Read
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR DQ Calibration Status Register for Rank0

EBI1_CH1_DDR_DQCAL_STATUS_RANK0

Bits	Name	Description
31	DQCAL_COMPARE_BYTE3	Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE3) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS
30	DQCAL_COMPARE_BYTE2	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE2) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS
29	DQCAL_COMPARE_BYTE1	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE1) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS

EBI1_CH1_DDR_DQCAL_STATUS_RANK0 (cont.)

Bits	Name	Description
28	DQCAL_COMPARE_BYTE0	SW: R, HW: W Indicates whether the DQ calibration command for LPDDR2 or PCDDR3 triggered via DDR_MR_CNTL_WDATA[RD_DQCAL] resulted in an expected pattern comparison pass/fail. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. SW also needs to ensure that the number of DQS edges received (NUM_DQS_EDGES_RECD_BYTE0) were correct. A valid pass is only when number of DQS edges received were correct and the PASS comparison read. 0x0: FAIL 0x1: PASS
27	RESERVED_27	
26:24	NUM_DQS_PE_EDGES_RECD_BYTE3	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
23	RESERVED_23	
22:20	NUM_DQS_PE_EDGES_RECD_BYTE2	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
19	RESERVED_19	

EBI1_CH1_DDR_DQCAL_STATUS_RANK0 (cont.)

Bits	Name	Description
18:16	NUM_DQS_PE_EDGES_RECD_BYTE1	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
15	RESERVED_15	
14:12	NUM_DQS_PE_EDGES_RECD_BYTE0	SW: R, HW: W Indicates the number of DQS PE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
11:9	NUM_DQS_NE_EDGES_RECD_BYTE3	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges

EBI1_CH1_DDR_DQCAL_STATUS_RANK0 (cont.)

Bits	Name	Description
8:6	NUM_DQS_NE_EDGES_RECD_BYTE2	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
5:3	NUM_DQS_NE_EDGES_RECD_BYTE1	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges
2:0	NUM_DQS_NE_EDGES_RECD_BYTE0	SW: R, HW: W Indicates the number of DQS NE edges received for the DQ calibration command. The value in this CSR field is valid when HW de-asserts RD_DQCAL indicating that the command completed. Note that for LPDDR2, the DQ calibration command has a memory burst length of 4 whereas the equivalent MPR read command for PCDDR3 has a memory burst length of 8. 0x0: None 0x1: 1 Positive Edge 0x2: 2 Positive Edges 0x3: 3 Positive Edges 0x4: 4 Positive Edges 0x5: 5 Positive Edges 0x6: 6 Positive Edges 0x7: 7 or more Positive Edges

0x00D80140 EBI1_CH1_DDR_RCW_RESET_AND_CNTL

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR RCW Async Reset & Control Register

This register controls the async reset for the generated RCW (Read capture window for DQS) signal for DQS qualification in the PHY. It also includes a global disable control which results in the external RCW signal being driven always to 1'b1.

EBI1_CH1_DDR_RCW_RESET_AND_CNTL

Bits	Name	Description
31:28	RESERVED_31_28	
27	RCW_ASYNC_RESET_BYTE3	SW: RW, HW: R SW control for the async reset for the flops in the RCW generation circuit for PHY data byte3. SW writes this field to 1'b1 if the flops in the PHY are required to be reset. HW will assert reset for a few cycles and then de-assert. Sw need not write this to 1'b0. The read value will always be 1'b0. 0x0: RESET OFF (default) 0x1: RESET ON
26	RCW_ASYNC_RESET_BYTE2	SW: RW, HW: R SW control for the async reset for the flops in the RCW generation circuit for PHY data byte3. SW writes this field to 1'b1 if the flops in the PHY are required to be reset. HW will assert reset for a few cycles and then de-assert.. Sw need not write this to 1'b0. The read value will always be 1'b0. 0x0: RESET OFF (default) 0x1: RESET ON
25	RCW_ASYNC_RESET_BYTE1	SW: RW, HW: R SW control for the async reset for the flops in the RCW generation circuit for PHY data byte3. SW writes this field to 1'b1 if the flops in the PHY are required to be reset. HW will assert reset for a few cycles and then de-assert. Sw need not write this to 1'b0. The read value will always be 1'b0. 0x0: RESET OFF (default) 0x1: RESET ON
24	RCW_ASYNC_RESET_BYTE0	SW: RW, HW: R SW control for the async reset for the flops in the RCW generation circuit for PHY data byte3. SW writes this field to 1'b1 if the flops in the PHY are required to be reset. HW will assert reset for a few cycles and then de-assert. Sw need not write this to 1'b0. The read value will always be 1'b0. 0x0: RESET OFF (default) 0x1: RESET ON
23:17	RESERVED_23_17	

EBI1_CH1_DDR_RCW_RESET_AND_CNTL (cont.)

Bits	Name	Description
16	RCW_ENABLE	SW: RW, HW: R When set to 1'b0, the external RCW (Read capture window) for precise DQS qualification is always driven to 1'b1 for all data bytes. When enabled (required only for PCDDR3), the design will send out an RCW pulse equal to the memory BL/2 -1 cycles to the PHY data bytes. 0x0: Disable (default) 0x1: Enable
15:1	RESERVED_15_1	
0	RD_FIFO_CNTL_DBG_EN	SW: RW, HW: R When set to 1'b1, this will match the previous design behavior wherein the read data keep/throw is written for MRR commands. If this field is set, then RCW_ENABLE must be disabled. 0x0: Disable (default) 0x1: Enable

0x00D80200 EBI1_CH1_DDR_ENHPRI_EN

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Enable Register.

This register is used to enable and configure enable enhanced prioritization of read and write commands within the DDR controller.

EBI1_CH1_DDR_ENHPRI_EN

Bits	Name	Description
31	ENHANCED_PRI_EN	SW: RW, HW: R Enables enhanced transaction prioritization mode. When enabled the priority of read and write transactions within the DDR controller can be modified to more quickly resolve blocking conditions and minimize worse case latencies. When this feature is enabled is it required that read command starvation be disabled by programming DDR_CMD_EXEC_OPT_0[RDCMD_STARVATION_TIMER] = 0. 0x0: Disable (default) 0x1: Enable
30	RD_PRI_AGING_EN	When enabled the DDR priority of read commands increases the longer they remaining unserviced. The priority adjustment is set through the DDR_ENHPRI_RDn registers. 0x0: Disable (default) 0x1: Enable

EBI1_CH1_DDR_ENHPRI_EN (cont.)

Bits	Name	Description
29	WR_PRI_AGING_EN	When enabled the DDR priority of write commands increases the longer they remaining unserviced. The priority adjustment is set through the DDR_ENHPRI_WRn registers. 0x0: Disable (default) 0x1: Enable
28	RESERVED_28	
27	ADJ_PRI_RDBLOCKING	SW: RW, HW: R When enabled the AXI priority of a read command blocking acceptance of write data is replaced with the value in the PRI_RDBLOCKING field. 0x0: Disable (default) 0x1: Enable
26	ADJ_PRI_RDMERGE	SW: RW, HW: R When enabled a read merge is considered to be blocking write data and its priority is replaced with the value in the PRI_RDBLOCKING field. 0x0: Disable (default) 0x1: Enable
25:24	PRI_RDBLOCKING	AXI priority for blocking read commands 0x0: AXI priority Level 0 (default) 0x1: AXI priority Level 1 0x2: AXI priority Level 2 0x3: AXI priority Level 3
23	ADJ_PRI_WRBLOCKING	SW: RW, HW: R When enabled the AXI priority of a write command blocking acceptance of write data or execution of a subsequent read is replaced with the value in the PRI_RDBLOCKING field. 0x0: Disable (default) 0x1: Enable
22	RESERVED_22	
21:20	PRI_WRBLOCKING	AXI priority for blocking write commands 0x0: AXI priority Level 0 (default) 0x1: AXI priority Level 1 0x2: AXI priority Level 2 0x3: AXI priority Level 3
19:16	RESERVED_19_16	

EBI1_CH1_DDR_ENHPRI_EN (cont.)

Bits	Name	Description
15:8	CONFLICT_BLOCK_HIT	SW: RW, HW: R When not disabled a page conflict of the given priority level(s) blocks any new command presented to the DDR controller from being a page hit to the same rank/bank as the conflict. Others : All combinations of priorities are legal. 0x0: Disabled 0x1: Priority 0 0x2: Priority 1 0x3: Priorities 0 and 1 0x4: Priority 2 0x8: Priority 3 0x10: Priority 4 0x20: Priority 5 0x40: Priority 6 0x80: Priority 7
7:0	RESERVED_7_0	

0x00D80224 EBI1_CH1_DDR_ENHPRI_RD1

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 1.

Number of cycles for a read command to attain DDR priority level 1.

EBI1_CH1_DDR_ENHPRI_RD1

Bits	Name	Description
31:7	RESERVED_31_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 0 becomes DDR priority 1.

0x00D80228 EBI1_CH1_DDR_ENHPRI_RD2

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 2.

Number of cycles for a read command to attain DDR priority level 2.

EBI1_CH1_DDR_ENHPRI_RD2

Bits	Name	Description
31:7	RESERVED_31_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 0 becomes DDR priority 2.

0x00D8022C EBI1_CH1_DDR_ENHPRI_RD3

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 3.

Number of cycles for a read command to attain DDR priority level 3.

EBI1_CH1_DDR_ENHPRI_RD3

Bits	Name	Description
31:15	RESERVED_31_15	
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 1 becomes DDR priority 3.
7	RESERVED_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 0 becomes DDR priority 3.

0x00D80230 EBI1_CH1_DDR_ENHPRI_RD4

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 4.

Number of cycles for a read command to attain DDR priority level 4.

EBI1_CH1_DDR_ENHPRI_RD4

Bits	Name	Description
31:15	RESERVED_31_15	

EBI1_CH1_DDR_ENHPRI_RD4 (cont.)

Bits	Name	Description
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 1 becomes DDR priority 4.
7	RESERVED_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 0 becomes DDR priority 4.

0x00D80234 EBI1_CH1_DDR_ENHPRI_RD5

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 5.

Number of cycles for a read command to attain DDR priority level 5.

EBI1_CH1_DDR_ENHPRI_RD5

Bits	Name	Description
31:23	RESERVED_31_23	
22:16	CYCLES_AXIPRI2	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 2 becomes DDR priority 5.
15	RESERVED_15	
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 1 becomes DDR priority 5.
7	RESERVED_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 0 becomes DDR priority 5.

0x00D80238 EBI1_CH1_DDR_ENHPRI_RD6

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 6.

Number of cycles for a read command to attain DDR priority level 6.

EBI1_CH1_DDR_ENHPRI_RD6

Bits	Name	Description
31:23	RESERVED_31_23	
22:16	CYCLES_AXIPRI2	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 2 becomes DDR priority 6.
15	RESERVED_15	
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 1 becomes DDR priority 6.
7	RESERVED_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 0 becomes DDR priority 6.

0x00D8023C EBI1_CH1_DDR_ENHPRI_RD7

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Read Latency 7.

Number of cycles for a read command to attain DDR priority level 7.

EBI1_CH1_DDR_ENHPRI_RD7

Bits	Name	Description
31	RESERVED_31	
30:24	CYCLES_AXIPRI3	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 3 becomes DDR priority 7.
23	RESERVED_23	
22:16	CYCLES_AXIPRI2	SW: RW, HW: R DDR cycles divided by 8 after which a read with AXI priority 2 becomes DDR priority 7.
15	RESERVED_15	
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which7a read with AXI priority 1 becomes DDR priority 7.

EBI1_CH1_DDR_ENHPRI_RD7 (cont.)

Bits	Name	Description
7	RESERVED_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a read with priority 0 becomes DDR priority 7.

0x00D80248 EBI1_CH1_DDR_ENHPRI_WR2

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Write Latency 2.

Number of cycles for a write command to attain DDR priority level 2.

EBI1_CH1_DDR_ENHPRI_WR2

Bits	Name	Description
31:7	RESERVED_31_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a write with AXI priority 0 becomes DDR priority 2.

0x00D80250 EBI1_CH1_DDR_ENHPRI_WR4

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Write Latency 4.

Number of cycles for a write command to attain DDR priority level 4.

EBI1_CH1_DDR_ENHPRI_WR4

Bits	Name	Description
31:15	RESERVED_31_15	
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which a write with AXI priority 1 becomes DDR priority 4.
7	RESERVED_7	

EBI1_CH1_DDR_ENHPRI_WR4 (cont.)

Bits	Name	Description
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a write with AXI priority 0 becomes DDR priority 4.

0x00D80258 EBI1_CH1_DDR_ENHPRI_WR6

Type: Read/Write
Clock: RUNALWAYSCLK
Reset State: 0x00000000

DDR Enhanced command Priority Write Latency 6.

Number of cycles for a write command to attain DDR priority level 6.

EBI1_CH1_DDR_ENHPRI_WR6

Bits	Name	Description
31:23	RESERVED_31_23	
22:16	CYCLES_AXIPRI2	SW: RW, HW: R DDR cycles divided by 8 after which a write with AXI priority 2 becomes DDR priority 6.
15	RESERVED_15	
14:8	CYCLES_AXIPRI1	SW: RW, HW: R DDR cycles divided by 8 after which a write with AXI priority 1 becomes DDR priority 6.
7	RESERVED_7	
6:0	CYCLES_AXIPRI0	SW: RW, HW: R DDR cycles divided by 8 after which a write with AXI priority 0 becomes DDR priority 6.

13.3.1.6 Loop-back Selftest Registers

This section contains the registers that are related to loop-back selftest logic. They control the loop-back path and logic behaviors. They also provide a mechanism to read out the MISR signature registers for software to compare the results.

0x00DD0000 EBI1_CH1_LBST_CNTL

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

LBST logic control register.

EBI1_CH1_LBST_CNTL

Bits	Name	Description
31	FORCE_DRIVE_DQS	SW : RW Force DIM to drive memory dqs 0x0: stop forcing to drive DQS 0x1: start driving always
30	FORCE_DRIVE_CK	SW : RW Force DIM to drive memory clock 0x0: stop forcing to drive CK 0x1: start driving always
29	CLR_CNTR_DQ_ALL	SW : W Writing '1' to this bit will clear all the counters for DQ 0x0: no action 0x1: clear the counter
28	CLR_CNTR_CA_ALL	SW : W Writing '1' to this bit will clear all the counters for CA 0x0: no action 0x1: clear the counter
27	RESET_FIFO	SW : W Write '1' to this bit clear the DQ and CA FIFO 0x0: no action 0x1: reset FIFO
26	SHIFT_PRPG_DQ	SW : RW Control if DQ PRPG should be shifting 0x0: no shifting PRPG 0x1: start shifting PRPG
25	SHIFT_PRPG_CA	SW : RW Control if CA PRPG should be shifting 0x0: no shifting PRPG 0x1: start shifting PRPG
24	DATA_SRC_CA	SW : RW Data source for command and address: 0x0: from DDR controller 0x1: from LBST CA PRPG
23:22	DATA_SRC_DQ	SW : RW Data source for read data: 0x0: from DDR controller 0x1: from LBST DQ PRPGs 0x2: Dynamicall switching in read/write.

EBI1_CH1_LBST_CNTL (cont.)

Bits	Name	Description
21:20	FIFO_WE_DQ	SW : RW WE for CA FIFOs and DQ FIFOs 0x0: Write is disabled on all FIFOs 0x1: Write disabled on DQ FIFOs, enabled on CA FIFOs. 0x2: Write enabled all FIFOs 0x3: Dynamicall switching in read/write on DQ FIFOs. Always enabled on CA FIFOs
19	FORCE_OE_DQ	SW : RW Control DQ's OE if FORCE_MODE_DQ == 1 0x0: Force DQ IE to be 0 0x1: Force DQ IE to be 1
18	FORCE_IE_DQ	SW : RW Control DQ's IE if FORCE_MODE_DQ == 1 0x0: Force DQ IE to be 0 0x1: Force DQ IE to be 1
17	FORCE_MODE_DQ	SW : RW DQ's IE/OE is either controlled by DDR controller or by the FORCE_IE_DQ, FORCE_OE_DQ 0x0: Controlled by DDR controller 0x1: Manually controlled by LBST logic
16	FORCE_IE_CA	SW : RW Force IE to turn on on all the command/address pads 0x0: Stop forcing IE 0x1: Force to turn on
15:14	READ_BURST	SW : RW Controls numbers of data burst per matching read command: 0x0: 4 burst of data 0x1: 8 burst of data 0x2: 16 burst of data 0x3: unused
13	IGNORE_IDLE_CMD	SW : RW Controls whether IDLE command will be ignored in MISR operation 0x0: Don't ignore zero data 0x1: Ignore zero data
12	IGNORE_ZERO_DQ	SW : RW Controls whether zero data will be ignored or not in MISR operation 0x0: Don't ignore zero data 0x1: Ignore zero data

EBI1_CH1_LBST_CNTL (cont.)

Bits	Name	Description
11:10	MISR_TRIG_DQ	SW : RW Specify condition that triggers shifting of DQ MISR: 0x0: When DQ FIFO is not empty 0x1: by matching command 0x2: by external shift enable bit 0x3: CSR controlled enable. Turned on by writing to START_SHIFT_PRPG. Turned off by writing to STOP_SHIFT_PRPG.
9:8	MISR_TRIG_CA	SW : RW Specify condition that triggers shifting of CA MISR: 0x0: when CMD FIFO is not empty and command matches 0x1: unused 0x2: by external shift enable bit 0x3: CSR controlled enable. Turned on by writing to START_SHIFT_PRPG. Turned off by writing to STOP_SHIFT_PRPG.
7:6	MISR_MODE_DQ	SW : RW Operating mode for DQ MISRs 0x0: Hold 0x1: Parallel-in parallel-out FF buffer 0x2: LFSR 0x3: Shift register only
5:4	MISR_MODE_CA	SW : RW Operating mode for CA MISR 0x0: Hold 0x1: Parallel-in parallel-out FF buffer 0x2: LFSR 0x3: Shift register only
3:2	LB_MODE_DQ	SW : RW Controls loop-back path within DIMs for write data 0x0: Normal functional mode 0x1: External loop-back mode 0x2: Do not use. 0x3: Internal loop-back mode
1	LB_CK_SEL_CA	SW : RW Controls which of the 2 memory clocks is used in command/address loop back 0x0: use rank 0's clock 0x1: use rank 1's clock
0	LB_MODE_CA	SW : RW Controls loop-back path within DIMs for command/address 0x0: path is disabled 0x1: path is enabled

0x00DD0004 EBI1_CH1_LBST_MISR_CA

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

LBST MISR register for command & address. Software can either read out this register to get the signature results, or write to this register to set up the seed for PRPG.

EBI1_CH1_LBST_MISR_CA

Bits	Name	Description
31:0	MISR_VAL	SW : RW MISR value

0x00DD0008 EBI1_CH1_LBST_MISR_DQ_EVEN

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

LBST MISR register for even data burst. Software can either read out this register to get the signature results, or write to this register to set up the seed for PRPG.

EBI1_CH1_LBST_MISR_DQ_EVEN

Bits	Name	Description
31:0	MISR_VAL	SW : RW MISR value

0x00DD000C EBI1_CH1_LBST_MISR_DQ_ODD

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

LBST MISR register for odd data burst. Software can either read out this register to get the signature results, or write to this register to set up the seed for PRPG.

EBI1_CH1_LBST_MISR_DQ_ODD

Bits	Name	Description
31:0	MISR_VAL	SW : RW MISR value

0x00DD0010 EBI1_CH1_LBST_COUNT_CA_ALL

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

This register displays the CA counter value. The counter counts number of all the looped-back commands burst. In SDR command mode, a burst equals to one DRAM command shots. In DDR mode, a burst equals to two DRAM command shots. The counter freezes at 0xFFFF.

EBI1_CH1_LBST_COUNT_CA_ALL

Bits	Name	Description
31:0	COUNT	SW : RW Counter value

0x00DD0014 EBI1_CH1_LBST_COUNT_CA_CMPR

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

This register displays the CA counter value. The counter counts number of all the looped-back commands burst that match the compare value and enable conditions. In SDR command mode, a burst equals to one DRAM command shots. In DDR mode, a burst equals to two DRAM command shots. The counter freezes at 0xFFFF.

EBI1_CH1_LBST_COUNT_CA_CMPR

Bits	Name	Description
31:0	COUNT	SW : R/W Counter value

0x00DD0018 EBI1_CH1_LBST_COUNT_DQ_ALL

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

This register displays the DQ counter value. The counter counts number of all the looped-back DQ data. One DQ data cycle equals to two DQ bursts. The counter freezes at 0xFFFF.

EBI1_CH1_LBST_COUNT_DQ_ALL

Bits	Name	Description
31:0	COUNT	SW : R/W Counter value

0x00DD001C EBI1_CH1_LBST_COUNT_DQ_CMPR

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

This register displays the DQ counter value. The counter counts number of all the looped-back DQ data cycle that are non-zero if the IGNORE_ZERO_DATA in LBST_CNTL is turned on. One DQ data cycle equals to two DQ bursts. The counter freezes at 0xFFFF.

EBI1_CH1_LBST_COUNT_DQ_CMPR

Bits	Name	Description
31:0	COUNT	SW : R/W Counter value

0x00DD0030 EBI1_CH1_LBST_CMPR_VAL_CA_EVEN

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

The command/address compare value for even address burst. If the looped-back CA match the compare value after the LBST_CMPR_EN_CA_EVEN is applied, the matching condition can be used to trigger read data generation. It will also increment the CA compare counter.

EBI1_CH1_LBST_CMPR_VAL_CA_EVEN

Bits	Name	Description
31:29	RESERVED_31_29	
28:8	CMPR_CA	SW : RW Compare value for command/address. Bit definition varies depending on the DRAM technologies.
7:6	CMPR_RESET_N	SW : RW Compare value for RESET_N of both ranks.
5:4	CMPR_CS_N	SW : RW Compare value for CS_N of both ranks.

EBI1_CH1_LBST_CMPR_VAL_CA_EVEN (cont.)

Bits	Name	Description
3:2	CMPR_CKE	SW : RW Compare value for CKE of both ranks.
1:0	CMPR_ODT	SW : RW Compare value for ODT of both ranks.

0x00DD0034 EBI1_CH1_LBST_CMPR_VAL_CA_ODD

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

The command/address compare value for odd address burst. If the looped-back CA match the compare value after the LBST_CMPR_EN_CA_ODD is applied, the matching condition can be used to trigger read data generation. It will also increment the CA compare counter.

EBI1_CH1_LBST_CMPR_VAL_CA_ODD

Bits	Name	Description
31:18	RESERVED_31_18	
17:8	CMPR_CA	SW : RW Compare value for odd command/address in LPDDR2 mode.
7:0	RESERVED_7_0	

0x00DD0038 EBI1_CH1_LBST_CMPR_EN_CA_EVEN

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

The command/address compare Enable for even address burst. The Enable bits of corresponding DRAM command/address bits match the definitions in LBST_CMPR_VAL_CA_EVEN.

EBI1_CH1_LBST_CMPR_EN_CA_EVEN

Bits	Name	Description
31	CMPR_NOT	SW : RW Inverse the compare condition so a match means NOT equal to the compare value and enable conditions.
30:29	RESERVED_30_29	

EBI1_CH1_LBST_CMPR_EN_CA_EVEN (cont.)

Bits	Name	Description
28:8	CMPR_EN_CA	SW : RW Enable bit for command/address compare. 0x0: don't care. 0x1: compare enabled.
7:0	CMPR_EN_CMD	SW : RW Enable bit for command compare. 0x0: don't care. 0x1: compare enabled.

0x00DD003C EBI1_CH1_LBST_CMPR_EN_CA_ODD

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

The command/address compare Enable for odd address burst. The Enable bits of corresponding DRAM command/address bits match the definitions in LBST_CMPR_VAL_CA_ODD.

EBI1_CH1_LBST_CMPR_EN_CA_ODD

Bits	Name	Description
31:18	RESERVED_31_18	
17:8	CMPR_EN_CA	SW : RW Enable bit for command/address compare. 0x0: don't care. 0x1: compare enabled.
7:0	RESERVED_7_0	

0x00DD0040 EBI1_CH1_LBST_CNTL2

Type: Read/Write
Clock: CLK_DDR_1X
Reset State: 0x00000000

LBST logic control register 2.

EBI1_CH1_LBST_CNTL2

Bits	Name	Description
31:2	RESERVED_31_2	

EBI1_CH1_LBST_CNTL2 (cont.)

Bits	Name	Description
1	IGNORE_DM	SW : RW When the loop-back data is written into MISR, This bit controls whether the DM bits are used to mask off the data (to force it to zero) or not. 0x0: consider DM bits. Zero the data only when DM is asserted 0x1: Ignore DM bits. Always take the data bit directly
0	MODE_SYNC_DRIVE_PRPG	SW : RW Controls the flop delay along the i_drive_prpg input path. 0x0: i_drive_prpg is feed into a DDR_1x demet directly 0x1: i_drive_prpg is going through 5-stage XO flops then goes to DDR_1x demet

13.4 DIM D00 DQ Registers (0x1A700000 DIM_D00_REG_BASE)

This section describes the D00 DIM TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1A700000 DIM_D00_DIM_DQ_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_DQ_TOP_CFG register configures the following:

DIM_DQ_TOP_CFG

DIM_D00_DIM_DQ_TOP_CFG

Bits	Name	Description
26	CDC_LDO_EN	Enablement of CDC LDO 1’b1 : Enabled 1’b0 : Disabled LDO and power provided from switches (default)
25	CDC_SWITCH_RC_EN	Enablement of CDC power RC (LPF) switch 1’b1 : Enabled 1’b0 : Disabled (default)
24	CDC_SWITCH_BYPASS_OFF	Enablement of CDC power bypass switch 1’b1 : Disabled 1’b0 : Enabled (default)
16	RCW_EN	Enablement of the Read Capture Window 1’b1 : Enable the RCW 1’b0 : Disabled (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1 : from Read CDCCAL 1’b0 : from Write CDCCAL (default)
12	DEBUG_BUS_EN	1’b1 : Enables the debug bus functionality 1’b0 : Disables the debug bus and drives all ’0’s on debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_dq[5:0] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend

DIM_D00_DIM_DQ_TOP_CFG (cont.)

Bits	Name	Description
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1'b0) 1'b1 : with pipe extend (default) 1'b0 : without pipe extend
0	WR_CLK_SEL	Write clock select 1'b1 : With write CDC (default) 1'b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1A700004 DIM_D00_DIM_DQ_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_DQ_HW_INFO register configures the following:

DIM_DQ_HW_INFO

DIM_D00_DIM_DQ_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1A700008 DIM_D00_DIM_DQ_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_DQ_HW_VERSION register configures the following:

DIM_DQ_HW_VERSION

DIM_D00_DIM_DQ_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.
27:16	MINOR	Minor version indicates expanded functionary, backward compatible.
15:0	STEP	Step indicates HW change which is not intended to impact SW compatibility.

0x1A700010 DIM_D00_DIM_DQ_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG0 register configures the following:

DIM_DQ_PAD_CFG0

DIM_D00_DIM_DQ_PAD_CFG0

Bits	Name	Description
31	DQ_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	DQ_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	DQ_LV_MODE	Mode select for high/low voltage regime
28	DQ_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQ_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQ_PULL_B	Input pull control
21:20	DQ_NSLEW	Slew rate control bits for output path NMOS
17:16	DQ_PSLEW	Slew rate control bits for output path PMOS
13:12	DQ_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQ_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	DQ_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQ_ROUT	Impedance control bit settings for output driver
2:0	DQ_DCC	Duty cycle correction bits for output path

0x1A700014 DIM_D00_DIM_DQ_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG1 register configures the following:

DIM_DQ_PAD_CFG1

DIM_D00_DIM_DQ_PAD_CFG1

Bits	Name	Description
31	DQS_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
30	DQS_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	DQS_LV_MODE	Mode select for high/low voltage regime
28	DQS_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQS_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQS_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	DQS_NSLEW	Slew rate control bits for output path NMOS
17:16	DQS_PSLEW	Slew rate control bits for output path PMOS
13:12	DQS_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQS_PRXDEL	Delay control bits to increase strength of PMOS input drive
7	DQS_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQS_ROUT	Impedance control bit settings for output driver
2:0	DQS_DCC	Duty cycle correction bits for output path

0x1A700018 DIM_D00_DIM_DQ_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_DQ_PAD_CFG2 register configures the following:

DIM_DQ_PAD_CFG2

DIM_D00_DIM_DQ_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1A700020 DIM_D00_DIM_DQ_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x1000FF11

The DIM_DQ_PAD_CFG3 register configures the following:

DIM_DQ_PAD_CFG3

DIM_D00_DIM_DQ_PAD_CFG3

Bits	Name	Description
28	DQS_DIFF_MODE	DQS output mode control 1’b1 : differential output (default) 1’b0 : single-ended output; _n output is HIZ
27	RCW_ODT_ENA1	Enable ODT for RCW pad (when hp_mode=1)
26	RCW_ODT_ENA0	Enable ODT for RCW pad (when hp_mode=0)
25:24	RCW_ODT	Impedance control for on-die termination on RCW pad
23	DQ_ODT_ENA1	Enable ODT for DQ pads (when hp_mode=1)
22	DQ_ODT_ENA0	Enable ODT for DQ pads (when hp_mode=0)
21:20	DQ_ODT	Impedance control for on-die termination on DQ pads
19	DQS_ODT_ENA1	Enable ODT for DQS pad (when hp_mode=1)
18	DQS_ODT_ENA0	Enable ODT for DQS pad (when hp_mode=0)

DIM_D00_DIM_DQ_PAD_CFG3 (cont.)

Bits	Name	Description
17:16	DQS_ODT	Impedance control for on-die termination on DQS pad
15:8	DQ_IE_OE	Enable both input receiver and output driver for all DQ pads
5	RCW_IE_OE	Enable both input receiver and output driver for RCW pad
4	DQS_IE_OE	Enable both input receiver and output driver for DQS pad
1	DM_IE	Input received enable for DM pad
0	DM_OE	Output driver enable for DM pad

0x1A700024 DIM_D00_DIM_DQ_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG4 register configures the following:

DIM_DQ_PAD_CFG4

DIM_D00_DIM_DQ_PAD_CFG4

Bits	Name	Description
31	RCW_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	RCW_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	RCW_LV_MODE	Mode select for high/low voltage regime
25:24	RCW_PULL_B	Input pull control
21:20	RCW_NSLEW	Slew rate control bits for output path NMOS
17:16	RCW_PSLEW	Slew rate control bits for output path PMOS
13:12	RCW_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	RCW_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	RCW_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	RCW_ROUT	Impedance control bit settings for output driver
2:0	RCW_DCC	Duty cycle correction bits for output path

0x1A700030 DIM_D00_DIM_DQ_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG0 register configures the following:

DIM_DQ_CDC_CTLR_CFG0

DIM_D00_DIM_DQ_CDC_CTLR_CFG0

Bits	Name	Description
25	STAGGER_CAL_ENA	1'b1: Stagger calibration of write and read CDCs once after the other to reduce peak voltage drop. 1'b0: Both write and read CDCs calibrated simultaneously This bit is introduced on the x2 core, so not present on x0 and x1 versions of DIM/PHY.
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1A700034 DIM_D00_DIM_DQ_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG1 register configures the following:

DIM_DQ_CDC_CTLR_CFG1

DIM_D00_DIM_DQ_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unit step and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1

0x1A700038 DIM_D00_DIM_DQ_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG0 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG0

DIM_D00_DIM_DQ_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic auto-calibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic auto-calibration interval based on sleep clock.

0x1A70003C DIM_D00_DIM_DQ_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG1 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG1

DIM_D00_DIM_DQ_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic auto-calibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic auto-calibration interval based on reference clock.

0x1A700040 DIM_D00_DIM_DQ_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_REFCOUNT_CFG register configures the following:

DIM_DQ_CDC_REFCOUNT_CFG

DIM_D00_DIM_DQ_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1A700044 DIM_D00_DIM_DQ_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_DQ_CDC_COARSE_CAL_CFG configures the following:

DIM_DQ_CDC_COARSE_CAL_CFG

DIM_D00_DIM_DQ_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1A700048 DIM_D00_DIM_DQ_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_RSVD_CFG register configures the following:

DIM_DQ_CDC_RSVD_CFG

DIM_D00_DIM_DQ_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1A70004C DIM_D00_DIM_DQ_RD_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_OFFSET_CFG register configures the following:

DIM_DQ_RD_CDC_OFFSET_CFG

DIM_D00_DIM_DQ_RD_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1A700050 DIM_D00_DIM_DQ_RD_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_DELAY_CFG register configures the following:

DIM_DQ_RD_CDC_DELAY_CFG

DIM_D00_DIM_DQ_RD_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1A700054 DIM_D00_DIM_DQ_RD_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_RD_CDC_SW_MODE_CFG

DIM_D00_DIM_DQ_RD_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1A700058 DIM_D00_DIM_DQ_RD_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_TEST_CFG register configures the following:

DIM_DQ_RD_CDC_TEST_CFG

DIM_D00_DIM_DQ_RD_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1’b1: Test outputs from the main DDA are connected to the CDC test ports 1’b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1’b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1’b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1’b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1’b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1’b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1’b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1A70005C DIM_D00_DIM_DQ_RD_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_RD_CDC_SW_OVRD_CFG

DIM_D00_DIM_DQ_RD_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1’b1 to start the reference window. Write 1’b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1’b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1’b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1’b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1’b1 written to this bit puts delay array 0 in delay-mode

DIM_D00_DIM_DQ_RD_CDC_SW_OVRD_CFG (cont.)

Bits	Name	Description
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1A700060 DIM_D00_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SLAVE_DDA_CFG register configures the following:

DIM_DQ_RD_CDC_SLAVE_DDA_CFG

DIM_D00_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Bits	Name	Description
17	SLAV_DDA_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit-step count 1'b0: Programmed offset is added/subtracted from the unit-step count
16	SLAV_DDA_OFFSET_SIGN	1'b1: Offset is subtracted from the unit-step count. This subtraction feature is not supported on x0 and x1 PHY cores (bit RESERVED). Supported on the x2 core version. 1'b0: Offset is added to the unit-step count
15:12	SLAVE_DDA_OFFSET	unit-step offset for slave DDA.
10:0	SLAVE_DDA_DELAY	Delay required from slave DDA programmed in pico seconds.

0x1A700070 DIM_D00_DIM_DQ_RD_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_RD_CDC_STATUS0 register configures the following:

DIM_DQ_RD_CDC_STATUS0

DIM_D00_DIM_DQ_RD_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. **NOTE** The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1A700074 DIM_D00_DIM_DQ_RD_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS1 register configures the following:

DIM_DQ_RD_CDC_STATUS1

DIM_D00_DIM_DQ_RD_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1A700078 DIM_D00_DIM_DQ_RD_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_RD_CDC_STATUS2 register configures the following:

DIM_DQ_RD_CDC_STATUS2

DIM_D00_DIM_DQ_RD_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1A70007C DIM_D00_DIM_DQ_RD_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS3 register configures the following:

DIM_DQ_RD_CDC_STATUS3

DIM_D00_DIM_DQ_RD_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration

DIM_D00_DIM_DQ_RD_CDC_STATUS3 (cont.)

Bits	Name	Description
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1A700080 DIM_D00_DIM_DQ_RD_CDC_STATUS4

Type: Read
Clock: HCLK
Reset State: 0x000000FF

The DIM_DQ_RD_CDC_STATUS4 register configures the following:

DIM_DQ_RD_CDC_STATUS4

DIM_D00_DIM_DQ_RD_CDC_STATUS4

Bits	Name	Description
7:4	SLAVE_DDA_DA1_TAPS	Number if unit taps applied to delay array 1 of slave DDA
3:0	SLAVE_DDA_DA0_TAPS	Number if unit taps applied to delay array 0 of slave DDA

0x1A7000AC DIM_D00_DIM_DQ_WR_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_OFFSET_CFG register configures the following:

DIM_DQ_WR_CDC_OFFSET_CFG

DIM_D00_DIM_DQ_WR_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1’b1: The programmed offset is directly loaded as subunit count 1’b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1’b1: Offset is subtracted from the subunit count 1’b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1’b1: The programmed offset is directly loaded as unit step count 1’b0: Programmed offset is added/subtracted from the unit step count

DIM_D00_DIM_DQ_WR_CDC_OFFSET_CFG (cont.)

Bits	Name	Description
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1A7000B0 DIM_D00_DIM_DQ_WR_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_DELAY_CFG register configures the following:

DIM_DQ_WR_CDC_DELAY_CFG

DIM_D00_DIM_DQ_WR_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1A7000B4 DIM_D00_DIM_DQ_WR_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_WR_CDC_SW_MODE_CFG

DIM_D00_DIM_DQ_WR_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.

DIM_D00_DIM_DQ_WR_CDC_SW_MODE_CFG (cont.)

Bits	Name	Description
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1A7000B8 DIM_D00_DIM_DQ_WR_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_TEST_CFG register configures the following:

DIM_DQ_WR_CDC_TEST_CFG

DIM_D00_DIM_DQ_WR_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1A7000BC DIM_D00_DIM_DQ_WR_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_WR_CDC_SW_OVRD_CFG

DIM_D00_DIM_DQ_WR_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1A7000D0 DIM_D00_DIM_DQ_WR_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_WR_CDC_STATUS0 register configures the following:

DIM_DQ_WR_CDC_STATUS0

DIM_D00_DIM_DQ_WR_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1A7000D4 DIM_D00_DIM_DQ_WR_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS1 register configures the following:

DIM_DQ_WR_CDC_STATUS1

DIM_D00_DIM_DQ_WR_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1A7000D8 DIM_D00_DIM_DQ_WR_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_WR_CDC_STATUS2 register configures the following:

DIM_DQ_WR_CDC_STATUS2

DIM_D00_DIM_DQ_WR_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1A7000DC DIM_D00_DIM_DQ_WR_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS3 register configures the following:

DIM_DQ_WR_CDC_STATUS3

DIM_D00_DIM_DQ_WR_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration

DIM_D00_DIM_DQ_WR_CDC_STATUS3 (cont.)

Bits	Name	Description
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1A700100 DIM_D00_DIM_DQ_DQ_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQ_IOC_SLV_CFG register configures the following:

DIM_DQ_DQ_IOC_SLV_CFG

DIM_D00_DIM_DQ_DQ_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1A700104 DIM_D00_DIM_DQ_DQ_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQ_IOC_SLV_STATUS register configures the following:

DIM_CA_CA_IOC_SLV_STATUS

DIM_D00_DIM_DQ_DQ_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

0x1A700110 DIM_D00_DIM_DQ_DQS_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQS_IOC_SLV_CFG register configures the following:

DIM_DQ_DQS_IOC_SLV_CFG

DIM_D00_DIM_DQ_DQS_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1A700114 DIM_D00_DIM_DQ_DQS_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQS_IOC_SLV_STATUS register configures the following:

DIM_DQ_DQS_IOC_SLV_STATUS

DIM_D00_DIM_DQ_DQS_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

13.5 DIM D01 DQ Registers (0x1A800000 DIM_D01_REG_BASE)

This section describes the D01 DIM DQ TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1A800000 DIM_D01_DIM_DQ_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_DQ_TOP_CFG register configures the following:

DIM_DQ_TOP_CFG

DIM_D01_DIM_DQ_TOP_CFG

Bits	Name	Description
26	CDC_LDO_EN	Enablement of CDC LDO 1’b1 : Enabled 1’b0 : Disabled LDO and power provided from switches (default)
25	CDC_SWITCH_RC_EN	Enablement of CDC power RC (LPF) switch 1’b1 : Enabled 1’b0 : Disabled (default)
24	CDC_SWITCH_BYPASS_OFF	Enablement of CDC power bypass switch 1’b1 : Disabled 1’b0 : Enabled (default)
16	RCW_EN	Enablement of the Read Capture Window 1’b1 : Enable the RCW 1’b0 : Disabled (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1 : from Read CDCCAL 1’b0 : from Write CDCCAL (default)
12	DEBUG_BUS_EN	1’b1 : Enables the debug bus functionality 1’b0 : Disables the debug bus and drives all ’0’s on debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_dq[5:0] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend

DIM_D01_DIM_DQ_TOP_CFG (cont.)

Bits	Name	Description
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1'b0) 1'b1 : with pipe extend (default) 1'b0 : without pipe extend
0	WR_CLK_SEL	Write clock select 1'b1 : With write CDC (default) 1'b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1A800004 DIM_D01_DIM_DQ_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_DQ_HW_INFO register configures the following:

DIM_DQ_HW_INFO

DIM_D01_DIM_DQ_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1A800008 DIM_D01_DIM_DQ_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_DQ_HW_VERSION register configures the following:

DIM_DQ_HW_VERSION

DIM_D01_DIM_DQ_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.

DIM_D01_DIM_DQ_HW_VERSION (cont.)

Bits	Name	Description
27:16	MINOR	Minor version indicates expanded functionary, backward compatible.
15:0	STEP	Step indicates HW change which is not intended to impact SW compatibility.

0x1A800010 DIM_D01_DIM_DQ_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG0 register configures the following:

DIM_DQ_PAD_CFG0

DIM_D01_DIM_DQ_PAD_CFG0

Bits	Name	Description
31	DQ_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	DQ_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	DQ_LV_MODE	Mode select for high/low voltage regime
28	DQ_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQ_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQ_PULL_B	Input pull control
21:20	DQ_NSLEW	Slew rate control bits for output path NMOS
17:16	DQ_PSLEW	Slew rate control bits for output path PMOS
13:12	DQ_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQ_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	DQ_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQ_ROUT	Impedance control bit settings for output driver
2:0	DQ_DCC	Duty cycle correction bits for output path

0x1A800014 DIM_D01_DIM_DQ_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG1 register configures the following:

DIM_DQ_PAD_CFG1

DIM_D01_DIM_DQ_PAD_CFG1

Bits	Name	Description
31	DQS_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
30	DQS_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	DQS_LV_MODE	Mode select for high/low voltage regime
28	DQS_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQS_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQS_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	DQS_NSLEW	Slew rate control bits for output path NMOS
17:16	DQS_PSLEW	Slew rate control bits for output path PMOS
13:12	DQS_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQS_PRXDEL	Delay control bits to increase strength of PMOS input drive
7	DQS_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQS_ROUT	Impedance control bit settings for output driver
2:0	DQS_DCC	Duty cycle correction bits for output path

0x1A800018 DIM_D01_DIM_DQ_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_DQ_PAD_CFG2 register configures the following:

DIM_DQ_PAD_CFG2

DIM_D01_DIM_DQ_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1A800020 DIM_D01_DIM_DQ_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x1000FF11

The DIM_DQ_PAD_CFG3 register configures the following:

DIM_DQ_PAD_CFG3

DIM_D01_DIM_DQ_PAD_CFG3

Bits	Name	Description
28	DQS_DIFF_MODE	DQS output mode control 1’b1 : differential output (default) 1’b0 : single-ended output; _n output is HIZ
27	RCW_ODT_ENA1	Enable ODT for RCW pad (when hp_mode=1)
26	RCW_ODT_ENA0	Enable ODT for RCW pad (when hp_mode=0)
25:24	RCW_ODT	Impedance control for on-die termination on RCW pad

DIM_D01_DIM_DQ_PAD_CFG3 (cont.)

Bits	Name	Description
23	DQ_ODT_ENA1	Enable ODT for DQ pads (when hp_mode=1)
22	DQ_ODT_ENA0	Enable ODT for DQ pads (when hp_mode=0)
21:20	DQ_ODT	Impedance control for on-die termination on DQ pads
19	DQS_ODT_ENA1	Enable ODT for DQS pad (when hp_mode=1)
18	DQS_ODT_ENA0	Enable ODT for DQS pad (when hp_mode=0)
17:16	DQS_ODT	Impedance control for on-die termination on DQS pad
15:8	DQ_IE_OE	Enable both input receiver and output driver for all DQ pads
5	RCW_IE_OE	Enable both input receiver and output driver for RCW pad
4	DQS_IE_OE	Enable both input receiver and output driver for DQS pad
1	DM_IE	Input received enable for DM pad
0	DM_OE	Output driver enable for DM pad

0x1A800024 DIM_D01_DIM_DQ_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG4 register configures the following:

DIM_DQ_PAD_CFG4

DIM_D01_DIM_DQ_PAD_CFG4

Bits	Name	Description
31	RCW_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	RCW_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	RCW_LV_MODE	Mode select for high/low voltage regime
25:24	RCW_PULL_B	Input pull control
21:20	RCW_NSLEW	Slew rate control bits for output path NMOS
17:16	RCW_PSLEW	Slew rate control bits for output path PMOS
13:12	RCW_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	RCW_PRXDEL	Delay control bits to increase strength of PMOS input driver

DIM_D01_DIM_DQ_PAD_CFG4 (cont.)

Bits	Name	Description
7	RCW_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	RCW_ROUT	Impedance control bit settings for output driver
2:0	RCW_DCC	Duty cycle correction bits for output path

0x1A800030 DIM_D01_DIM_DQ_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG0 register configures the following:

DIM_DQ_CDC_CTLR_CFG0

DIM_D01_DIM_DQ_CDC_CTLR_CFG0

Bits	Name	Description
25	STAGGER_CAL_ENA	1’b1: Stagger calibration of write and read CDCs once after the other to reduce peak voltage drop. 1’b0: Both write and read CDCs calibrated simultaneously This bit is introduced on the x2 core, so not present on x0 and x1 versions of DIM/PHY.
24	TRACKING_CAL_ENA	1’b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1’b0: Periodic calibration triggers cause full recalibration
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1’b0: Tracking calibration uses previous Target_count value. 1’b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1’b0: unitstep and subunit caps are from calibration or SW settings 1’b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1’b1: Enables periodic auto calibration 1’b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.

DIM_D01_DIM_DQ_CDC_CTLR_CFG0 (cont.)

Bits	Name	Description
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1A800034 DIM_D01_DIM_DQ_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG1 register configures the following:

DIM_DQ_CDC_CTLR_CFG1

DIM_D01_DIM_DQ_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.

DIM_D01_DIM_DQ_CDC_CTLR_CFG1 (cont.)

Bits	Name	Description
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1

0x1A800038 DIM_D01_DIM_DQ_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG0 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG0

DIM_D01_DIM_DQ_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1’b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1’b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.
16	TIMER_ENA	1’b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1’b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1A80003C DIM_D01_DIM_DQ_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG1 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG1

DIM_D01_DIM_DQ_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1A800040 DIM_D01_DIM_DQ_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_REFCOUNT_CFG register configures the following:

DIM_DQ_CDC_REFCOUNT_CFG

DIM_D01_DIM_DQ_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1A800044 DIM_D01_DIM_DQ_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_DQ_CDC_COARSE_CAL_CFG configures the following:

DIM_DQ_CDC_COARSE_CAL_CFG

DIM_D01_DIM_DQ_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1A800048 DIM_D01_DIM_DQ_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_RSVD_CFG register configures the following:

DIM_DQ_CDC_RSVD_CFG

DIM_D01_DIM_DQ_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1A80004C DIM_D01_DIM_DQ_RD_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_OFFSET_CFG register configures the following:

DIM_DQ_RD_CDC_OFFSET_CFG

DIM_D01_DIM_DQ_RD_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1’b1: The programmed offset is directly loaded as subunit count 1’b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1’b1: Offset is subtracted from the subunit count 1’b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset

DIM_D01_DIM_DQ_RD_CDC_OFFSET_CFG (cont.)

Bits	Name	Description
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1A800050 DIM_D01_DIM_DQ_RD_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_DELAY_CFG register configures the following:

DIM_DQ_RD_CDC_DELAY_CFG

DIM_D01_DIM_DQ_RD_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1A800054 DIM_D01_DIM_DQ_RD_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_RD_CDC_SW_MODE_CFG

DIM_D01_DIM_DQ_RD_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1A800058 DIM_D01_DIM_DQ_RD_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_TEST_CFG register configures the following:

DIM_DQ_RD_CDC_TEST_CFG

DIM_D01_DIM_DQ_RD_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1A80005C DIM_D01_DIM_DQ_RD_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_RD_CDC_SW_OVRD_CFG

DIM_D01_DIM_DQ_RD_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1A800060 DIM_D01_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SLAVE_DDA_CFG register configures the following:

DIM_DQ_RD_CDC_SLAVE_DDA_CFG

DIM_D01_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Bits	Name	Description
17	SLAV_DDA_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit-step count 1'b0: Programmed offset is added/subtracted from the unit-step count
16	SLAV_DDA_OFFSET_SIGN	1'b1: Offset is subtracted from the unit-step count. This subtraction feature is not supported on x0 and x1 PHY cores (bit RESERVED). Supported on the x2 core version. 1'b0: Offset is added to the unit-step count
15:12	SLAVE_DDA_OFFSET	unit-step offset for slave DDA.
10:0	SLAVE_DDA_DELAY	Delay required from slave DDA programmed in pico seconds.

0x1A800070 DIM_D01_DIM_DQ_RD_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_RD_CDC_STATUS0 register configures the following:

DIM_DQ_RD_CDC_STATUS0

DIM_D01_DIM_DQ_RD_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count

DIM_D01_DIM_DQ_RD_CDC_STATUS0 (cont.)

Bits	Name	Description
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1A800074 DIM_D01_DIM_DQ_RD_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS1 register configures the following:

DIM_DQ_RD_CDC_STATUS1

DIM_D01_DIM_DQ_RD_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1A800078 DIM_D01_DIM_DQ_RD_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_RD_CDC_STATUS2 register configures the following:

DIM_DQ_RD_CDC_STATUS2

DIM_D01_DIM_DQ_RD_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1A80007C DIM_D01_DIM_DQ_RD_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS3 register configures the following:

DIM_DQ_RD_CDC_STATUS3

DIM_D01_DIM_DQ_RD_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1A800080 DIM_D01_DIM_DQ_RD_CDC_STATUS4

Type: Read
Clock: HCLK
Reset State: 0x000000FF

The DIM_DQ_RD_CDC_STATUS4 register configures the following:

DIM_DQ_RD_CDC_STATUS4

DIM_D01_DIM_DQ_RD_CDC_STATUS4

Bits	Name	Description
7:4	SLAVE_DDA_DA1_TAPS	Number if unit taps applied to delay array 1 of slave DDA
3:0	SLAVE_DDA_DA0_TAPS	Number if unit taps applied to delay array 0 of slave DDA

0x1A8000AC DIM_D01_DIM_DQ_WR_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_OFFSET_CFG register configures the following:

DIM_DQ_WR_CDC_OFFSET_CFG

DIM_D01_DIM_DQ_WR_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1A8000B0 DIM_D01_DIM_DQ_WR_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_DELAY_CFG register configures the following:

DIM_DQ_WR_CDC_DELAY_CFG

DIM_D01_DIM_DQ_WR_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates

DIM_D01_DIM_DQ_WR_CDC_DELAY_CFG (cont.)

Bits	Name	Description
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1A8000B4 DIM_D01_DIM_DQ_WR_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_WR_CDC_SW_MODE_CFG

DIM_D01_DIM_DQ_WR_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1A8000B8 DIM_D01_DIM_DQ_WR_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_TEST_CFG register configures the following:

DIM_DQ_WR_CDC_TEST_CFG

DIM_D01_DIM_DQ_WR_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1A8000BC DIM_D01_DIM_DQ_WR_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_WR_CDC_SW_OVRD_CFG

DIM_D01_DIM_DQ_WR_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode

DIM_D01_DIM_DQ_WR_CDC_SW_OVRD_CFG (cont.)

Bits	Name	Description
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1A8000D0 DIM_D01_DIM_DQ_WR_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_WR_CDC_STATUS0 register configures the following:

DIM_DQ_WR_CDC_STATUS0

DIM_D01_DIM_DQ_WR_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count

DIM_D01_DIM_DQ_WR_CDC_STATUS0 (cont.)

Bits	Name	Description
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1A8000D4 DIM_D01_DIM_DQ_WR_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS1 register configures the following:

DIM_DQ_WR_CDC_STATUS1

DIM_D01_DIM_DQ_WR_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1A8000D8 DIM_D01_DIM_DQ_WR_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_WR_CDC_STATUS2 register configures the following:

DIM_DQ_WR_CDC_STATUS2

DIM_D01_DIM_DQ_WR_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1A8000DC DIM_D01_DIM_DQ_WR_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS3 register configures the following:

DIM_DQ_WR_CDC_STATUS3

DIM_D01_DIM_DQ_WR_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1A800100 DIM_D01_DIM_DQ_DQ_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQ_IOC_SLV_CFG register configures the following:

DIM_DQ_DQ_IOC_SLV_CFG

DIM_D01_DIM_DQ_DQ_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	

DIM_D01_DIM_DQ_DQ_IOC_SLV_CFG (cont.)

Bits	Name	Description
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1A800104 DIM_D01_DIM_DQ_DQ_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQ_IOC_SLV_STATUS register configures the following:

DIM_CA_CA_IOC_SLV_STATUS

DIM_D01_DIM_DQ_DQ_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

0x1A800110 DIM_D01_DIM_DQ_DQS_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQS_IOC_SLV_CFG register configures the following:

DIM_DQ_DQS_IOC_SLV_CFG

DIM_D01_DIM_DQ_DQS_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	

DIM_D01_DIM_DQ_DQS_IOC_SLV_CFG (cont.)

Bits	Name	Description
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1A800114 DIM_D01_DIM_DQ_DQS_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQS_IOC_SLV_STATUS register configures the following:

DIM_DQ_DQS_IOC_SLV_STATUS

DIM_D01_DIM_DQ_DQS_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

13.6 DIM D02 DQ Registers (0x1A900000 DIM_D02_REG_BASE)

This section describes the D02 DIM DQ TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1A900000 DIM_D02_DIM_DQ_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_DQ_TOP_CFG register configures the following:

DIM_DQ_TOP_CFG

DIM_D02_DIM_DQ_TOP_CFG

Bits	Name	Description
26	CDC_LDO_EN	Enablement of CDC LDO 1’b1 : Enabled 1’b0 : Disabled LDO and power provided from switches (default)
25	CDC_SWITCH_RC_EN	Enablement of CDC power RC (LPF) switch 1’b1 : Enabled 1’b0 : Disabled (default)
24	CDC_SWITCH_BYPASS_OFF	Enablement of CDC power bypass switch 1’b1 : Disabled 1’b0 : Enabled (default)
16	RCW_EN	Enablement of the Read Capture Window 1’b1 : Enable the RCW 1’b0 : Disabled (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1 : from Read CDCCAL 1’b0 : from Write CDCCAL (default)
12	DEBUG_BUS_EN	1’b1 : Enables the debug bus functionality 1’b0 : Disables the debug bus and drives all ’0’s on debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_dq[5:0] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend

DIM_D02_DIM_DQ_TOP_CFG (cont.)

Bits	Name	Description
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1'b0) 1'b1 : with pipe extend (default) 1'b0 : without pipe extend
0	WR_CLK_SEL	Write clock select 1'b1 : With write CDC (default) 1'b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1A900004 DIM_D02_DIM_DQ_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_DQ_HW_INFO register configures the following:

DIM_DQ_HW_INFO

DIM_D02_DIM_DQ_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1A900008 DIM_D02_DIM_DQ_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_DQ_HW_VERSION register configures the following:

DIM_DQ_HW_VERSION

DIM_D02_DIM_DQ_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.

DIM_D02_DIM_DQ_HW_VERSION (cont.)

Bits	Name	Description
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1A900010 DIM_D02_DIM_DQ_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG0 register configures the following:

DIM_DQ_PAD_CFG0

DIM_D02_DIM_DQ_PAD_CFG0

Bits	Name	Description
31	DQ_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	DQ_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	DQ_LV_MODE	Mode select for high/low voltage regime
28	DQ_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQ_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQ_PULL_B	Input pull control
21:20	DQ_NSLEW	Slew rate control bits for output path NMOS
17:16	DQ_PSLEW	Slew rate control bits for output path PMOS
13:12	DQ_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQ_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	DQ_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQ_ROUT	Impedance control bit settings for output driver
2:0	DQ_DCC	Duty cycle correction bits for output path

0x1A900014 DIM_D02_DIM_DQ_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG1 register configures the following:

DIM_DQ_PAD_CFG1

DIM_D02_DIM_DQ_PAD_CFG1

Bits	Name	Description
31	DQS_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
30	DQS_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	DQS_LV_MODE	Mode select for high/low voltage regime
28	DQS_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQS_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQS_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	DQS_NSLEW	Slew rate control bits for output path NMOS
17:16	DQS_PSLEW	Slew rate control bits for output path PMOS
13:12	DQS_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQS_PRXDEL	Delay control bits to increase strength of PMOS input drive
7	DQS_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQS_ROUT	Impedance control bit settings for output driver
2:0	DQS_DCC	Duty cycle correction bits for output path

0x1A900018 DIM_D02_DIM_DQ_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_DQ_PAD_CFG2 register configures the following:

DIM_DQ_PAD_CFG2

DIM_D02_DIM_DQ_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1A900020 DIM_D02_DIM_DQ_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x1000FF11

The DIM_DQ_PAD_CFG3 register configures the following:

DIM_DQ_PAD_CFG3

DIM_D02_DIM_DQ_PAD_CFG3

Bits	Name	Description
28	DQS_DIFF_MODE	DQS output mode control 1’b1 : differential output (default) 1’b0 : single-ended output; _n output is HIZ
27	RCW_ODT_ENA1	Enable ODT for RCW pad (when hp_mode=1)
26	RCW_ODT_ENA0	Enable ODT for RCW pad (when hp_mode=0)
25:24	RCW_ODT	Impedance control for on-die termination on RCW pad
23	DQ_ODT_ENA1	Enable ODT for DQ pads (when hp_mode=1)
22	DQ_ODT_ENA0	Enable ODT for DQ pads (when hp_mode=0)
21:20	DQ_ODT	Impedance control for on-die termination on DQ pads
19	DQS_ODT_ENA1	Enable ODT for DQS pad (when hp_mode=1)
18	DQS_ODT_ENA0	Enable ODT for DQS pad (when hp_mode=0)

DIM_D02_DIM_DQ_PAD_CFG3 (cont.)

Bits	Name	Description
17:16	DQS_ODT	Impedance control for on-die termination on DQS pad
15:8	DQ_IE_OE	Enable both input receiver and output driver for all DQ pads
5	RCW_IE_OE	Enable both input receiver and output driver for RCW pad
4	DQS_IE_OE	Enable both input receiver and output driver for DQS pad
1	DM_IE	Input received enable for DM pad
0	DM_OE	Output driver enable for DM pad

0x1A900024 DIM_D02_DIM_DQ_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG4 register configures the following:

DIM_DQ_PAD_CFG4

DIM_D02_DIM_DQ_PAD_CFG4

Bits	Name	Description
31	RCW_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	RCW_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	RCW_LV_MODE	Mode select for high/low voltage regime
25:24	RCW_PULL_B	Input pull control
21:20	RCW_NSLEW	Slew rate control bits for output path NMOS
17:16	RCW_PSLEW	Slew rate control bits for output path PMOS
13:12	RCW_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	RCW_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	RCW_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	RCW_ROUT	Impedance control bit settings for output driver
2:0	RCW_DCC	Duty cycle correction bits for output path

0x1A900030 DIM_D02_DIM_DQ_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG0 register configures the following:

DIM_DQ_CDC_CTLR_CFG0

DIM_D02_DIM_DQ_CDC_CTLR_CFG0

Bits	Name	Description
25	STAGGER_CAL_ENA	1'b1: Stagger calibration of write and read CDCs once after the other to reduce peak voltage drop. 1'b0: Both write and read CDCs calibrated simultaneously This bit is introduced on the x2 core, so not present on x0 and x1 versions of DIM/PHY.
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1A900034 DIM_D02_DIM_DQ_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG1 register configures the following:

DIM_DQ_CDC_CTLR_CFG1

DIM_D02_DIM_DQ_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1

0x1A900038 DIM_D02_DIM_DQ_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG0 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG0

DIM_D02_DIM_DQ_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1A90003C DIM_D02_DIM_DQ_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG1 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG1

DIM_D02_DIM_DQ_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1A900040 DIM_D02_DIM_DQ_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_REFCOUNT_CFG register configures the following:

DIM_DQ_CDC_REFCOUNT_CFG

DIM_D02_DIM_DQ_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1A900044 DIM_D02_DIM_DQ_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_DQ_CDC_COARSE_CAL_CFG configures the following:

DIM_DQ_CDC_COARSE_CAL_CFG

DIM_D02_DIM_DQ_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1A900048 DIM_D02_DIM_DQ_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_RSVD_CFG register configures the following:

DIM_DQ_CDC_RSVD_CFG

DIM_D02_DIM_DQ_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1A90004C DIM_D02_DIM_DQ_RD_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_OFFSET_CFG register configures the following:

DIM_DQ_RD_CDC_OFFSET_CFG

DIM_D02_DIM_DQ_RD_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1A900050 DIM_D02_DIM_DQ_RD_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_DELAY_CFG register configures the following:

DIM_DQ_RD_CDC_DELAY_CFG

DIM_D02_DIM_DQ_RD_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1A900054 DIM_D02_DIM_DQ_RD_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_RD_CDC_SW_MODE_CFG

DIM_D02_DIM_DQ_RD_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1A900058 DIM_D02_DIM_DQ_RD_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_TEST_CFG register configures the following:

DIM_DQ_RD_CDC_TEST_CFG

DIM_D02_DIM_DQ_RD_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1’b1: Test outputs from the main DDA are connected to the CDC test ports 1’b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1’b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1’b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1’b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1’b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1’b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1’b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1A90005C DIM_D02_DIM_DQ_RD_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_RD_CDC_SW_OVRD_CFG

DIM_D02_DIM_DQ_RD_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1’b1 to start the reference window. Write 1’b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1’b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1’b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1’b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1’b1 written to this bit puts delay array 0 in delay-mode

DIM_D02_DIM_DQ_RD_CDC_SW_OVRD_CFG (cont.)

Bits	Name	Description
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1A900060 DIM_D02_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SLAVE_DDA_CFG register configures the following:

DIM_DQ_RD_CDC_SLAVE_DDA_CFG

DIM_D02_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Bits	Name	Description
17	SLAV_DDA_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit-step count 1'b0: Programmed offset is added/subtracted from the unit-step count
16	SLAV_DDA_OFFSET_SIGN	1'b1: Offset is subtracted from the unit-step count. This subtraction feature is not supported on x0 and x1 PHY cores (bit RESERVED). Supported on the x2 core version. 1'b0: Offset is added to the unit-step count
15:12	SLAVE_DDA_OFFSET	unit-step offset for slave DDA.
10:0	SLAVE_DDA_DELAY	Delay required from slave DDA programmed in pico seconds.

0x1A900070 DIM_D02_DIM_DQ_RD_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_RD_CDC_STATUS0 register configures the following:

DIM_DQ_RD_CDC_STATUS0

DIM_D02_DIM_DQ_RD_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1A900074 DIM_D02_DIM_DQ_RD_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS1 register configures the following:

DIM_DQ_RD_CDC_STATUS1

DIM_D02_DIM_DQ_RD_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1A900078 DIM_D02_DIM_DQ_RD_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_RD_CDC_STATUS2 register configures the following:

DIM_DQ_RD_CDC_STATUS2

DIM_D02_DIM_DQ_RD_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1A90007C DIM_D02_DIM_DQ_RD_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS3 register configures the following:

DIM_DQ_RD_CDC_STATUS3

DIM_D02_DIM_DQ_RD_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration

DIM_D02_DIM_DQ_RD_CDC_STATUS3 (cont.)

Bits	Name	Description
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1A900080 DIM_D02_DIM_DQ_RD_CDC_STATUS4

Type: Read
Clock: HCLK
Reset State: 0x000000FF

The DIM_DQ_RD_CDC_STATUS4 register configures the following:

DIM_DQ_RD_CDC_STATUS4

DIM_D02_DIM_DQ_RD_CDC_STATUS4

Bits	Name	Description
7:4	SLAVE_DDA_DA1_TAPS	Number if unit taps applied to delay array 1 of slave DDA
3:0	SLAVE_DDA_DA0_TAPS	Number if unit taps applied to delay array 0 of slave DDA

0x1A9000AC DIM_D02_DIM_DQ_WR_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_OFFSET_CFG register configures the following:

DIM_DQ_WR_CDC_OFFSET_CFG

DIM_D02_DIM_DQ_WR_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1’b1: The programmed offset is directly loaded as subunit count 1’b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1’b1: Offset is subtracted from the subunit count 1’b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1’b1: The programmed offset is directly loaded as unit step count 1’b0: Programmed offset is added/subtracted from the unit step count

DIM_D02_DIM_DQ_WR_CDC_OFFSET_CFG (cont.)

Bits	Name	Description
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1A9000B0 DIM_D02_DIM_DQ_WR_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_DELAY_CFG register configures the following:

DIM_DQ_WR_CDC_DELAY_CFG

DIM_D02_DIM_DQ_WR_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1A9000B4 DIM_D02_DIM_DQ_WR_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_WR_CDC_SW_MODE_CFG

DIM_D02_DIM_DQ_WR_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.

DIM_D02_DIM_DQ_WR_CDC_SW_MODE_CFG (cont.)

Bits	Name	Description
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1A9000B8 DIM_D02_DIM_DQ_WR_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_TEST_CFG register configures the following:

DIM_DQ_WR_CDC_TEST_CFG

DIM_D02_DIM_DQ_WR_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1A9000BC DIM_D02_DIM_DQ_WR_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_WR_CDC_SW_OVRD_CFG

DIM_D02_DIM_DQ_WR_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1A9000D0 DIM_D02_DIM_DQ_WR_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_WR_CDC_STATUS0 register configures the following:

DIM_DQ_WR_CDC_STATUS0

DIM_D02_DIM_DQ_WR_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1A9000D4 DIM_D02_DIM_DQ_WR_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS1 register configures the following:

DIM_DQ_WR_CDC_STATUS1

DIM_D02_DIM_DQ_WR_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1A9000D8 DIM_D02_DIM_DQ_WR_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_WR_CDC_STATUS2 register configures the following:

DIM_DQ_WR_CDC_STATUS2

DIM_D02_DIM_DQ_WR_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1A9000DC DIM_D02_DIM_DQ_WR_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS3 register configures the following:

DIM_DQ_WR_CDC_STATUS3

DIM_D02_DIM_DQ_WR_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration

DIM_D02_DIM_DQ_WR_CDC_STATUS3 (cont.)

Bits	Name	Description
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1A900100 DIM_D02_DIM_DQ_DQ_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQ_IOC_SLV_CFG register configures the following:

DIM_DQ_DQ_IOC_SLV_CFG

DIM_D02_DIM_DQ_DQ_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1A900104 DIM_D02_DIM_DQ_DQ_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQ_IOC_SLV_STATUS register configures the following:

DIM_CA_CA_IOC_SLV_STATUS

DIM_D02_DIM_DQ_DQ_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

0x1A900110 DIM_D02_DIM_DQ_DQS_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQS_IOC_SLV_CFG register configures the following:

DIM_DQ_DQS_IOC_SLV_CFG

DIM_D02_DIM_DQ_DQS_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1A900114 DIM_D02_DIM_DQ_DQS_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQS_IOC_SLV_STATUS register configures the following:

DIM_DQ_DQS_IOC_SLV_STATUS

DIM_D02_DIM_DQ_DQS_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

13.7 DIM D03 DQ Registers (0x1AA00000 DIM_D03_REG_BASE)

This section describes the D03 DIM DQ TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1AA00000 DIM_D03_DIM_DQ_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_DQ_TOP_CFG register configures the following:

DIM_DQ_TOP_CFG

DIM_D03_DIM_DQ_TOP_CFG

Bits	Name	Description
26	CDC_LDO_EN	Enablement of CDC LDO 1’b1 : Enabled 1’b0 : Disabled LDO and power provided from switches (default)
25	CDC_SWITCH_RC_EN	Enablement of CDC power RC (LPF) switch 1’b1 : Enabled 1’b0 : Disabled (default)
24	CDC_SWITCH_BYPASS_OFF	Enablement of CDC power bypass switch 1’b1 : Disabled 1’b0 : Enabled (default)
16	RCW_EN	Enablement of the Read Capture Window 1’b1 : Enable the RCW 1’b0 : Disabled (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1 : from Read CDCCAL 1’b0 : from Write CDCCAL (default)
12	DEBUG_BUS_EN	1’b1 : Enables the debug bus functionality 1’b0 : Disables the debug bus and drives all ’0’s on debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_dq[5:0] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend

DIM_D03_DIM_DQ_TOP_CFG (cont.)

Bits	Name	Description
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1'b0) 1'b1 : with pipe extend (default) 1'b0 : without pipe extend
0	WR_CLK_SEL	Write clock select 1'b1 : With write CDC (default) 1'b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1AA00004 DIM_D03_DIM_DQ_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_DQ_HW_INFO register configures the following:

DIM_DQ_HW_INFO

DIM_D03_DIM_DQ_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1AA00008 DIM_D03_DIM_DQ_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_DQ_HW_VERSION register configures the following:

DIM_DQ_HW_VERSION

DIM_D03_DIM_DQ_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.

DIM_D03_DIM_DQ_HW_VERSION (cont.)

Bits	Name	Description
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1AA00010 DIM_D03_DIM_DQ_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG0 register configures the following:

DIM_DQ_PAD_CFG0

DIM_D03_DIM_DQ_PAD_CFG0

Bits	Name	Description
31	DQ_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	DQ_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	DQ_LV_MODE	Mode select for high/low voltage regime
28	DQ_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQ_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQ_PULL_B	Input pull control
21:20	DQ_NSLEW	Slew rate control bits for output path NMOS
17:16	DQ_PSLEW	Slew rate control bits for output path PMOS
13:12	DQ_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQ_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	DQ_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQ_ROUT	Impedance control bit settings for output driver
2:0	DQ_DCC	Duty cycle correction bits for output path

0x1AA00014 DIM_D03_DIM_DQ_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG1 register configures the following:

DIM_DQ_PAD_CFG1

DIM_D03_DIM_DQ_PAD_CFG1

Bits	Name	Description
31	DQS_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
30	DQS_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	DQS_LV_MODE	Mode select for high/low voltage regime
28	DQS_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQS_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQS_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	DQS_NSLEW	Slew rate control bits for output path NMOS
17:16	DQS_PSLEW	Slew rate control bits for output path PMOS
13:12	DQS_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQS_PRXDEL	Delay control bits to increase strength of PMOS input drive
7	DQS_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQS_ROUT	Impedance control bit settings for output driver
2:0	DQS_DCC	Duty cycle correction bits for output path

0x1AA00018 DIM_D03_DIM_DQ_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_DQ_PAD_CFG2 register configures the following:

DIM_DQ_PAD_CFG2

DIM_D03_DIM_DQ_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1AA00020 DIM_D03_DIM_DQ_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x1000FF11

The DIM_DQ_PAD_CFG3 register configures the following:

DIM_DQ_PAD_CFG3

DIM_D03_DIM_DQ_PAD_CFG3

Bits	Name	Description
28	DQS_DIFF_MODE	DQS output mode control 1’b1 : differential output (default) 1’b0 : single-ended output; _n output is HIZ
27	RCW_ODT_ENA1	Enable ODT for RCW pad (when hp_mode=1)
26	RCW_ODT_ENA0	Enable ODT for RCW pad (when hp_mode=0)
25:24	RCW_ODT	Impedance control for on-die termination on RCW pad
23	DQ_ODT_ENA1	Enable ODT for DQ pads (when hp_mode=1)
22	DQ_ODT_ENA0	Enable ODT for DQ pads (when hp_mode=0)
21:20	DQ_ODT	Impedance control for on-die termination on DQ pads
19	DQS_ODT_ENA1	Enable ODT for DQS pad (when hp_mode=1)
18	DQS_ODT_ENA0	Enable ODT for DQS pad (when hp_mode=0)

DIM_D03_DIM_DQ_PAD_CFG3 (cont.)

Bits	Name	Description
17:16	DQS_ODT	Impedance control for on-die termination on DQS pad
15:8	DQ_IE_OE	Enable both input receiver and output driver for all DQ pads
5	RCW_IE_OE	Enable both input receiver and output driver for RCW pad
4	DQS_IE_OE	Enable both input receiver and output driver for DQS pad
1	DM_IE	Input received enable for DM pad
0	DM_OE	Output driver enable for DM pad

0x1AA00024 DIM_D03_DIM_DQ_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG4 register configures the following:

DIM_DQ_PAD_CFG4

DIM_D03_DIM_DQ_PAD_CFG4

Bits	Name	Description
31	RCW_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	RCW_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	RCW_LV_MODE	Mode select for high/low voltage regime
25:24	RCW_PULL_B	Input pull control
21:20	RCW_NSLEW	Slew rate control bits for output path NMOS
17:16	RCW_PSLEW	Slew rate control bits for output path PMOS
13:12	RCW_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	RCW_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	RCW_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	RCW_ROUT	Impedance control bit settings for output driver
2:0	RCW_DCC	Duty cycle correction bits for output path

0x1AA00030 DIM_D03_DIM_DQ_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG0 register configures the following:

DIM_DQ_CDC_CTLR_CFG0

DIM_D03_DIM_DQ_CDC_CTLR_CFG0

Bits	Name	Description
25	STAGGER_CAL_ENA	1'b1: Stagger calibration of write and read CDCs once after the other to reduce peak voltage drop. 1'b0: Both write and read CDCs calibrated simultaneously This bit is introduced on the x2 core, so not present on x0 and x1 versions of DIM/PHY.
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1AA00034 DIM_D03_DIM_DQ_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG1 register configures the following:

DIM_DQ_CDC_CTLR_CFG1

DIM_D03_DIM_DQ_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1

0x1AA00038 DIM_D03_DIM_DQ_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG0 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG0

DIM_D03_DIM_DQ_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1AA0003C DIM_D03_DIM_DQ_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG1 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG1

DIM_D03_DIM_DQ_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1AA00040 DIM_D03_DIM_DQ_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_REFCOUNT_CFG register configures the following:

DIM_DQ_CDC_REFCOUNT_CFG

DIM_D03_DIM_DQ_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1AA00044 DIM_D03_DIM_DQ_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_DQ_CDC_COARSE_CAL_CFG configures the following:

DIM_DQ_CDC_COARSE_CAL_CFG

DIM_D03_DIM_DQ_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1AA00048 DIM_D03_DIM_DQ_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_RSVD_CFG register configures the following:

DIM_DQ_CDC_RSVD_CFG

DIM_D03_DIM_DQ_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1AA0004C DIM_D03_DIM_DQ_RD_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_OFFSET_CFG register configures the following:

DIM_DQ_RD_CDC_OFFSET_CFG

DIM_D03_DIM_DQ_RD_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AA00050 DIM_D03_DIM_DQ_RD_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_DELAY_CFG register configures the following:

DIM_DQ_RD_CDC_DELAY_CFG

DIM_D03_DIM_DQ_RD_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AA00054 DIM_D03_DIM_DQ_RD_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_RD_CDC_SW_MODE_CFG

DIM_D03_DIM_DQ_RD_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AA00058 DIM_D03_DIM_DQ_RD_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_TEST_CFG register configures the following:

DIM_DQ_RD_CDC_TEST_CFG

DIM_D03_DIM_DQ_RD_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1’b1: Test outputs from the main DDA are connected to the CDC test ports 1’b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1’b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1’b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1’b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1’b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1’b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1’b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AA0005C DIM_D03_DIM_DQ_RD_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_RD_CDC_SW_OVRD_CFG

DIM_D03_DIM_DQ_RD_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1’b1 to start the reference window. Write 1’b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1’b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1’b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1’b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1’b1 written to this bit puts delay array 0 in delay-mode

DIM_D03_DIM_DQ_RD_CDC_SW_OVRD_CFG (cont.)

Bits	Name	Description
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AA00060 DIM_D03_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SLAVE_DDA_CFG register configures the following:

DIM_DQ_RD_CDC_SLAVE_DDA_CFG

DIM_D03_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Bits	Name	Description
17	SLAV_DDA_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit-step count 1'b0: Programmed offset is added/subtracted from the unit-step count
16	SLAV_DDA_OFFSET_SIGN	1'b1: Offset is subtracted from the unit-step count. This subtraction feature is not supported on x0 and x1 PHY cores (bit RESERVED). Supported on the x2 core version. 1'b0: Offset is added to the unit-step count
15:12	SLAVE_DDA_OFFSET	unit-step offset for slave DDA.
10:0	SLAVE_DDA_DELAY	Delay required from slave DDA programmed in pico seconds.

0x1AA00070 DIM_D03_DIM_DQ_RD_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_RD_CDC_STATUS0 register configures the following:

DIM_DQ_RD_CDC_STATUS0

DIM_D03_DIM_DQ_RD_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AA00074 DIM_D03_DIM_DQ_RD_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS1 register configures the following:

DIM_DQ_RD_CDC_STATUS1

DIM_D03_DIM_DQ_RD_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AA00078 DIM_D03_DIM_DQ_RD_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_RD_CDC_STATUS2 register configures the following:

DIM_DQ_RD_CDC_STATUS2

DIM_D03_DIM_DQ_RD_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AA0007C DIM_D03_DIM_DQ_RD_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS3 register configures the following:

DIM_DQ_RD_CDC_STATUS3

DIM_D03_DIM_DQ_RD_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration

DIM_D03_DIM_DQ_RD_CDC_STATUS3 (cont.)

Bits	Name	Description
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AA00080 DIM_D03_DIM_DQ_RD_CDC_STATUS4

Type: Read
Clock: HCLK
Reset State: 0x000000FF

The DIM_DQ_RD_CDC_STATUS4 register configures the following:

DIM_DQ_RD_CDC_STATUS4

DIM_D03_DIM_DQ_RD_CDC_STATUS4

Bits	Name	Description
7:4	SLAVE_DDA_DA1_TAPS	Number if unit taps applied to delay array 1 of slave DDA
3:0	SLAVE_DDA_DA0_TAPS	Number if unit taps applied to delay array 0 of slave DDA

0x1AA000AC DIM_D03_DIM_DQ_WR_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_OFFSET_CFG register configures the following:

DIM_DQ_WR_CDC_OFFSET_CFG

DIM_D03_DIM_DQ_WR_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1’b1: The programmed offset is directly loaded as subunit count 1’b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1’b1: Offset is subtracted from the subunit count 1’b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1’b1: The programmed offset is directly loaded as unit step count 1’b0: Programmed offset is added/subtracted from the unit step count

DIM_D03_DIM_DQ_WR_CDC_OFFSET_CFG (cont.)

Bits	Name	Description
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AA000B0 DIM_D03_DIM_DQ_WR_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_DELAY_CFG register configures the following:

DIM_DQ_WR_CDC_DELAY_CFG

DIM_D03_DIM_DQ_WR_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AA000B4 DIM_D03_DIM_DQ_WR_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_WR_CDC_SW_MODE_CFG

DIM_D03_DIM_DQ_WR_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.

DIM_D03_DIM_DQ_WR_CDC_SW_MODE_CFG (cont.)

Bits	Name	Description
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AA000B8 DIM_D03_DIM_DQ_WR_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_TEST_CFG register configures the following:

DIM_DQ_WR_CDC_TEST_CFG

DIM_D03_DIM_DQ_WR_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AA000BC DIM_D03_DIM_DQ_WR_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_WR_CDC_SW_OVRD_CFG

DIM_D03_DIM_DQ_WR_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AA000D0 DIM_D03_DIM_DQ_WR_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_WR_CDC_STATUS0 register configures the following:

DIM_DQ_WR_CDC_STATUS0

DIM_D03_DIM_DQ_WR_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AA000D4 DIM_D03_DIM_DQ_WR_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS1 register configures the following:

DIM_DQ_WR_CDC_STATUS1

DIM_D03_DIM_DQ_WR_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AA000D8 DIM_D03_DIM_DQ_WR_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_WR_CDC_STATUS2 register configures the following:

DIM_DQ_WR_CDC_STATUS2

DIM_D03_DIM_DQ_WR_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AA000DC DIM_D03_DIM_DQ_WR_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS3 register configures the following:

DIM_DQ_WR_CDC_STATUS3

DIM_D03_DIM_DQ_WR_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration

DIM_D03_DIM_DQ_WR_CDC_STATUS3 (cont.)

Bits	Name	Description
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AA00100 DIM_D03_DIM_DQ_DQ_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQ_IOC_SLV_CFG register configures the following:

DIM_DQ_DQ_IOC_SLV_CFG

DIM_D03_DIM_DQ_DQ_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1AA00104 DIM_D03_DIM_DQ_DQ_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQ_IOC_SLV_STATUS register configures the following:

DIM_CA_CA_IOC_SLV_STATUS

DIM_D03_DIM_DQ_DQ_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

0x1AA00110 DIM_D03_DIM_DQ_DQS_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQS_IOC_SLV_CFG register configures the following:

DIM_DQ_DQS_IOC_SLV_CFG

DIM_D03_DIM_DQ_DQS_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1AA00114 DIM_D03_DIM_DQ_DQS_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQS_IOC_SLV_STATUS register configures the following:

DIM_DQ_DQS_IOC_SLV_STATUS

DIM_D03_DIM_DQ_DQS_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

13.8 DIM C00 CA Registers (0x1AB00000 DIM_C00_REG_BASE)

This section describes the C00 DIM CA TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1AB00000 DIM_C00_DIM_CA_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_CA_TOP_CFG register configures the following:

DIM_CA_TOP_CFG

DIM_C00_DIM_CA_TOP_CFG

Bits	Name	Description
20	IOCAL_CTLR_SEL	Select source of PCNT/NCNT/PNCNT_VALID 1’b1: external 1’b0: internal (default)
16	SDR_MODE_EN	1’b1 : Enables SDR mode on address bus 1’b0 : Enables DDR mode on address bus (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1: From IOCAL 1’b0: From CDCCAL (default)
12	DEBUG_BUS_EN	1’b1: Enables the debug bus functionality 1’b0: Disables the debug bus and drives all ’0’s on the debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_ca[7:5] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1’b0) 1’b1 : with pipe extend (default) 1’b0: without pipe extend
0	WR_CLK_SEL	Write clock select 1’b1 : With write CDC (default) 1’b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1AB00004 DIM_C00_DIM_CA_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_CA_HW_INFO register configures the following:

DIM_CA_HW_INFO

DIM_C00_DIM_CA_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1AB00008 DIM_C00_DIM_CA_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_CA_HW_VERSION register configures the following:

DIM_CA_HW_VERSION

DIM_C00_DIM_CA_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1AB00010 DIM_C00_DIM_CA_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_CA_PAD_CFG0 register configures the following:

DIM_CA_PAD_CFG0

DIM_C00_DIM_CA_PAD_CFG0

Bits	Name	Description
31	CA_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	CA_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	CA_LV_MODE	Mode pin for high/low voltage regime
28	CA_ODT_ENA	Enable bit for on-die termination
27:26	CA_ODT	Impedance control bit settings for on-die termination
25:24	CA_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	CA_NSLEW	Slew rate control bits for output path NMOS
17:16	CA_PSLEW	Slew rate control bits for output path PMOS
13:12	CA_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	CA_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	CA_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	CA_ROUT	Impedance control bit settings for output driver
2:0	CA_DCC	Duty cycle correction bits for output path

0x1AB00014 DIM_C00_DIM_CA_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0220440

The DIM_CA_PAD_CFG1 register configures the following:

DIM_CA_PAD_CFG1

DIM_C00_DIM_CA_PAD_CFG1

Bits	Name	Description
31	CK_DDR_MODE1	Mode select for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
30	CK_DDR_MODE0	Mode select for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	CK_LV_MODE	Mode select for high/low voltage regime
28	CK_CMFB_ENA	Common mode feedback loop enable
27	CK_ODT_ENA1	Enable bit for on-die termination (when hp_mode = 1'b1)
26	CK_ODT_ENA	Enable bit for on-die termination (when hp_mode = 1'b0) Bit field name missing '0' for APQ8064 SW compatibility.
25:24	CK_ODT	Impedance control bit settings for on-die termination
21:20	CK_NSLEW	Slew rate control bits for output path NMOS
17:16	CK_PSLEW	Slew rate control bits for output path PMOS
13	CK_CUR_MODE1	Current/Voltage mode selection (when hp_mode = 1'b1) 1'b1 : Current mode 1'b0 : Voltage mode (default)
12	CK_CUR_MODE0	Current/Voltage mode selection (when hp_mode = 1'b0) 1'b1 : Current mode 1'b0 : Voltage mode (default)
10:8	CK_I_DRV	Control bit settings for bias current
7	CK_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	CK_ROUT	Impedance control bit settings for output driver
2:0	CK_DCC	Duty cycle correction bits for output path

0x1AB00018 DIM_C00_DIM_CA_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_CA_PAD_CFG2 register configures the following:

DIM_CA_PAD_CFG2

DIM_C00_DIM_CA_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1AB0001C DIM_C00_DIM_CA_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x00300000

The DIM_CA_PAD_CFG3 register configures the following:

DIM_CA_PAD_CFG3

DIM_C00_DIM_CA_PAD_CFG3

Bits	Name	Description
31:30	CS_N_IE	
29:28	CS_N_OE	
25	CK_IE	
24	CK_OE	
23:22	CKE_IE	
21:20	CKE_OE	
19:10	CA_IE	
9:0	CA_OE	

0x1AB00020 DIM_C00_DIM_CA_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_PAD_CFG4 register configures the following:

DIM_CA_PAD_CFG4

DIM_C00_DIM_CA_PAD_CFG4

Bits	Name	Description
31:30	CS_N_OE_DYN_ENA	Enable dynamic control of CS_N OE 1'b1: Dynamic control enabled and CS_N_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CS_N OE gated by CA_PAD_CFG3 bits Note: This register should not be set in external loopback mode since it will change the IE contol source.
29:28	CS_N_OE_DYN	Dynamic OE control for each of the CS_N outputs, OR-ed with common controller OE.
25	RESERVED_1	
24	RESERVED_2	
23:22	CKE_OE_DYN_ENA	Enable dynamic control of CKE OE 1'b1: Dynamic control enabled and CKE_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CKE OE gated by CA_PAD_CFG3 bits
21:20	CKE_OE_DYN	Dynamic OE control for each of the CA outputs, OR-ed with common controller OE.
19:10	CA_OE_DYN_ENA	Enable dynamic control of CA OE 1'b1: Dynamic control enabled and CA_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CA OE gated by CA_PAD_CFG3 bits
9:0	CA_OE_DYN	Dynamic OE control for each of the CA outputs, OR-ed with common controller OE.

0x1AB00030 DIM_C00_DIM_CA_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CTLR_CFG0 register configures the following:

DIM_CA_CDC_CTLR_CFG0

DIM_C00_DIM_CA_CDC_CTLR_CFG0

Bits	Name	Description
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1AB00034 DIM_C00_DIM_CA_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CTLR_CFG1 register configures the following:

DIM_CA_CDC_CTLR_CFG1

DIM_C00_DIM_CA_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1

0x1AB00038 DIM_C00_DIM_CA_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CAL_TIMER_CFG0 register configures the following:

DIM_CA_CDC_CAL_TIMER_CFG0

DIM_C00_DIM_CA_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.

DIM_C00_DIM_CA_CDC_CAL_TIMER_CFG0 (cont.)

Bits	Name	Description
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1AB0003C DIM_C00_DIM_CA_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CAL_TIMER_CFG1 register configures the following:

DIM_CA_CDC_CAL_TIMER_CFG1

DIM_C00_DIM_CA_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1AB00040 DIM_C00_DIM_CA_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_REFCOUNT_CFG register configures the following:

DIM_CA_CDC_REFCOUNT_CFG

DIM_C00_DIM_CA_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1AB00044 DIM_C00_DIM_CA_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_CA_CDC_COARSE_CAL_CFG configures the following:

DIM_CA_CDC_COARSE_CAL_CFG

DIM_C00_DIM_CA_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1AB00048 DIM_C00_DIM_CA_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_RSVD_CFG register configures the following:

DIM_CA_CDC_RSVD_CFG

DIM_C00_DIM_CA_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1AB0004C DIM_C00_DIM_CA_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_OFFSET_CFG register configures the following:

DIM_CA_CDC_OFFSET_CFG

DIM_C00_DIM_CA_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AB00050 DIM_C00_DIM_CA_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_DELAY_CFG register configures the following:

DIM_CA_CDC_DELAY_CFG

DIM_C00_DIM_CA_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates

DIM_C00_DIM_CA_CDC_DELAY_CFG (cont.)

Bits	Name	Description
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AB00054 DIM_C00_DIM_CA_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_SW_MODE_CFG register configures the following:

DIM_CA_CDC_SW_MODE_CFG

DIM_C00_DIM_CA_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AB00058 DIM_C00_DIM_CA_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_TEST_CFG register configures the following:

DIM_CA_CDC_TEST_CFG

DIM_C00_DIM_CA_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AB0005C DIM_C00_DIM_CA_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_TEST_CFG register configures the following:

DIM_CA_CDC_SW_OVRD_CFG

DIM_C00_DIM_CA_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode

DIM_C00_DIM_CA_CDC_SW_OVRD_CFG (cont.)

Bits	Name	Description
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AB00070 DIM_C00_DIM_CA_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_CA_CDC_STATUS0 register configures the following:

DIM_CA_CDC_STATUS0

DIM_C00_DIM_CA_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count

DIM_C00_DIM_CA_CDC_STATUS0 (cont.)

Bits	Name	Description
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AB00074 DIM_C00_DIM_CA_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_STATUS1 register configures the following:

DIM_CA_CDC_STATUS1

DIM_C00_DIM_CA_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AB00078 DIM_C00_DIM_CA_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_CA_CDC_STATUS2 register configures the following:

DIM_CA_CDC_STATUS2

DIM_C00_DIM_CA_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AB0007C DIM_C00_DIM_CA_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_STATUS3 register configures the following:

DIM_CA_CDC_STATUS3

DIM_C00_DIM_CA_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AB000E0 DIM_C00_DIM_CA_IOC_CTLR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_CFG register configures the following:

DIM_CA_IOC_CTLR_CFG

DIM_C00_DIM_CA_IOC_CTLR_CFG

Bits	Name	Description
31	CAL_NOW	SW : RW Set this bit to 1’b1 will cause the IO calibration starts immediately. This bit has to be cleared after the calibration has been done. 0x0: no-op 0x1: start IOCal immediately
30	IO_CAL_AUTO	Periodic auto calibration mode. Writing a ’1’ to this bit will trigger periodic auto calibration with the period specified in IOC_CTLR_TIMER_CFG register. If ’0’, it disables the timer based on sleep clock. Note that this does not impact the timer based on fixed frequency clock (ffclk).
29	IO_CAL_FF_TIMER_EN	Fixed Frequency Timer mode. Writing a ’1’ to this bit will set the timer running off tcxo clock. If ’0’, it disables the timer based on fixed frequency clock.
28	IO_CAL_BANDGAP_DYN_CTRL	Enable dynamic control of the bandgap element: This low-power feature is only available on x2 core. Bit reserved for x0/x1 cores. 1’b1: Enabled - bandgap element turned on only during IO calibration or when current mode is enabled. 1’b0: Disabled (default) - bandgap element turned on/off statically based on BANDHGAP_ENA0/1 bits.
25	SW_FFCLK_ON	Writing a ’1’ to this field will turn on the fixed frequency (xo) clock on signal
24	LV_MODE	SW : RW Enable/Disable low-voltage mode (MIF2 pad only) 0x0: 1.8V 0x1: non-1.8V
20:16	MARGIN_LOAD	SW : RW If the difference between the current IOCal result is greater than the last result by the number specified here, then the IOCal controller will request value update to DDR controller. 0x0: always update
13:12	IMP_SEL	SW : RW Select bits to choose which impedance to calibrate to
10	PN_SEL_CA	SW : RW Enables loading of HW calibrated values for ca pads. Writing a ’1’ to this bit would let the IOCAL to request traffic stall on ca pads when it is time to update the pads with the new value.
9	PN_SEL_DATA	SW : RW Enables loading of HW calibrated values for dq/dqs pads. Writing a ’1’ to this bit would let the IOCAL to request traffic stall on data pads when it is time to update the pads with the new value.

DIM_C00_DIM_CA_IOC_CTLR_CFG (cont.)

Bits	Name	Description
8	CAL_USE_LAST	SW : RW Select the initial value to start IO calibration 0x0: start from a fixed values specified in IOC_CTLR_PNCNT_CFG (default) 0x1: start from previous IOCal PNCNT results
6:4	SAMPLE_POINT	SW : RW Specify number of samples per measure point 0x0: 1 0x1: 3 0x2: 5 0x3: 7 0x4: 9 0x5: 11 0x6: 13 0x7: 15
3	DDR_MODE1	
2	DDR_MODE0	
1	BANDGAP_ENA1	SW : RW Pin to enable bandgap independent of diff_ctl 0x0: disable 0x1: enable
0	BANDGAP_ENA0	SW : RW Pin to enable bandgap independent of diff_ctl 0x0: disable 0x1: enable

0x1AB000E4 DIM_C00_DIM_CA_IOC_CTLR_PNCNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_CFG register configures the following:

This register contains the initial value for the next calibration to start from. Softwave can set the hardware to either start calibration from a fixed value or from previous results. If software chooses to use fixed value by setting CAN_USE_LAST in register IOC_CTLR_CFG to be 0, then the values in this register will be used.

DIM_CA_IOC_CTLR_CFG

DIM_C00_DIM_CA_IOC_CTLR_PNCNT_CFG

Bits	Name	Description
12:8	NCNT_INIT_CSR	SW : RW Starting PCNT value used in calibration. Only take effect when CAN_USE_LAST is asserted
4:0	PCNT_INIT_CSR	SW : RW Starting NCNT value used in calibration. Only take effect when CAN_USE_LAST is asserted

0x1AB000E8 DIM_C00_DIM_CA_IOC_CTLR_TIMER_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_TIMER_CFG register configures the following:

DIM_CA_IOC_CTLR_TIMER_CFG

DIM_C00_DIM_CA_IOC_CTLR_TIMER_CFG

Bits	Name	Description
31:16	TIMER_PERIOD	SW : RW Recalibration Period. The period is measured in timer clock cycles. Typically it's a 32kHz clock. The minimum period that can be programmed is 3. 0,1,2: Invalid values
15:0	FF_TIMER_PERIOD	SW : RW Recalibration Period for the timer running of xo clock. 0x0: Invalid

0x1AB000EC DIM_C00_DIM_CA_IOC_CTLR_TIMER_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_TIMER_STATUS register configures the following:

DIM_CA_IOC_CTLR_TIMER_STATUS

DIM_C00_DIM_CA_IOC_CTLR_TIMER_STATUS

Bits	Name	Description
15:0	TIMER_STATUS	Current Auto Calibration Timer value. As this register is written in sleep clock domain and read in xo clock domain and no hardware synchronization in place, It is required by the software to read this register 4 times to get the correct value.

0x1AB000F0 DIM_C00_DIM_CA_IOC_CTLR_CHAR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_ CHAR_CFGregister configures the following:

This register is used by hardware verification software only. It provides a mechanism to allow software to bypass the internal calibration state machine and directly access the IOCAL pad inputs.

IDIM_CA_IOC_CTLR_CHAR_CFG

DIM_C00_DIM_CA_IOC_CTLR_CHAR_CFG

Bits	Name	Description
16	SM_BYP_ENA	SW : RW Characterization Bypass Path Enable 0x0: Non-bypass: State Machine Controls IOCAL pad inputs (default) 0x1: bypass: This register controls IOCal pad inputs
15	SM_BYP_N_ENA	SW : RW IO CAL Characterization n_enable: 0x0: de-asserted (default) 0x1: asserted
12:8	SM_BYP_NCNT	SW : RW IO CAL Characterization ncnt value. 0x0: count 0 (default)
7	SM_BYP_P_ENA	SW : RW IO CAL Characterization p_enable: 0x0: de-asserted (default) 0x1: asserted
4:0	SM_BYP_PCNT	SW : RW IO CAL Characterization pcnt value. 0x0: count 0 (default)

0x1AB000F4 DIM_C00_DIM_CA_IOC_CTLR_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00011010

The DIM_CA_IOC_CTLR_STATUS register configures the following:

DIM_CA_IOC_CTLR_STATUS

DIM_C00_DIM_CA_IOC_CTLR_STATUS

Bits	Name	Description
31	INIT_IOCAL_DONE	SW : R The very first IO Calibration is finished This bit is stiky. once it becomes 1'b1 until software writes it back to 0. 0x0: Init-cal never done 0x1: Init-cal finished
18	IOCAL_DONE_D	SW : R IO Calibration is finished 0x0: in progress 0x1: finished
17	IOCAL_BUSY	SW : R Status of calibration State machine 0x0: idle 0x1: busy
16	SYNC_COMP	SW : R comp value from IOCal pad
12:8	NCNT_HOLD	SW : R Current NCNT value used
4:0	PCNT_HOLD	SW : R Current PCNT value used

0x1AB00100 DIM_C00_DIM_CA_CA_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_CA_CA_IOC_SLV_CFG register configures the following:

This register specifies the overriding pcnt and ncnt values. Overriding mode is controlled by PNCNT_HW_LOAD_EN bit in this register.

DIM_CA_CA_IOC_SLV_CFG

DIM_C00_DIM_CA_CA_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	Select PCNT/NCNT Source for pads. This is the mux control that chooses either auto calibrated value or the software override value. 0x0: override (default) 0x1: auto cal
28:24	NCNT_SW_VAL	SW : RW NCNT Override Value for the pads
20:16	PCNT_SW_VAL	SW : RW PCNT Override Value for the pads
15	NCNT_OFFSET_SIGN	controls if the NOFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
12:8	NCNT_SW_OFFSET	SW : RW The offiset applied on top of NCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)
7	PCNT_OFFSET_SIGN	controls if the POFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
4:0	PCNT_SW_OFFSET	SW : RW The offiset applied on top of PCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)

0x1AB00104 DIM_C00_DIM_CA_CA_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_CA_CA_IOC_SLV_STATUS register configures the following:

DIM_CA_CA_IOC_SLV_STATUS

DIM_C00_DIM_CA_CA_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	The final NCNT value that is applied to the pads.
4:0	PAD_PCNT	The final PCNT value that is applied to the pads.

0x1AB00110 DIM_C00_DIM_CA_CK_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_CA_CK_IOC_SLV_CFG register configures the following:

DIM_CA_CK_IOC_SLV_CFG

DIM_C00_DIM_CA_CK_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	Select PCNT/NCNT Source for pads. This is the mux control that chooses either auto calibrated value or the software override value. 0x0: override (default) 0x1: auto cal
28:24	NCNT_SW_VAL	SW : RW NCNT Override Value for the pads
20:16	PCNT_SW_VAL	SW : RW PCNT Override Value for the pads
15	NCNT_OFFSET_SIGN	controls if the NOFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
12:8	NCNT_SW_OFFSET	SW : RW The offiset applied on top of NCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)
7	PCNT_OFFSET_SIGN	controls if the POFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
4:0	PCNT_SW_OFFSET	SW : RW The offiset applied on top of PCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)

0x1AB00114 DIM_C00_DIM_CA_CK_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_CA_CK_IOC_SLV_STATUS register configures the following:

DIM_CA_CK_IOC_SLV_STATUS

DIM_C00_DIM_CA_CK_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	The final NCNT value that is applied to the pads.
4:0	PAD_PCNT	The final PCNT value that is applied to the pads.

13.9 DIM D10 DQ Registers (0x1AC00000 DIM_D10_REG_BASE)

This section describes the D10 DIM DQ TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1AC00000 DIM_D10_DIM_DQ_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_DQ_TOP_CFG register configures the following:

DIM_DQ_TOP_CFG

DIM_D10_DIM_DQ_TOP_CFG

Bits	Name	Description
26	CDC_LDO_EN	Enablement of CDC LDO 1’b1 : Enabled 1’b0 : Disabled LDO and power provided from switches (default)
25	CDC_SWITCH_RC_EN	Enablement of CDC power RC (LPF) switch 1’b1 : Enabled 1’b0 : Disabled (default)
24	CDC_SWITCH_BYPASS_OFF	Enablement of CDC power bypass switch 1’b1 : Disabled 1’b0 : Enabled (default)
16	RCW_EN	Enablement of the Read Capture Window 1’b1 : Enable the RCW 1’b0 : Disabled (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1 : from Read CDCCAL 1’b0 : from Write CDCCAL (default)
12	DEBUG_BUS_EN	1’b1 : Enables the debug bus functionality 1’b0 : Disables the debug bus and drives all ’0’s on debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_dq[5:0] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend

DIM_D10_DIM_DQ_TOP_CFG (cont.)

Bits	Name	Description
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1'b0) 1'b1 : with pipe extend (default) 1'b0 : without pipe extend
0	WR_CLK_SEL	Write clock select 1'b1 : With write CDC (default) 1'b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1AC00004 DIM_D10_DIM_DQ_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_DQ_HW_INFO register configures the following:

DIM_DQ_HW_INFO

DIM_D10_DIM_DQ_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1AC00008 DIM_D10_DIM_DQ_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_DQ_HW_VERSION register configures the following:

DIM_DQ_HW_VERSION

DIM_D10_DIM_DQ_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.

DIM_D10_DIM_DQ_HW_VERSION (cont.)

Bits	Name	Description
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1AC00010 DIM_D10_DIM_DQ_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG0 register configures the following:

DIM_DQ_PAD_CFG0

DIM_D10_DIM_DQ_PAD_CFG0

Bits	Name	Description
31	DQ_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	DQ_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	DQ_LV_MODE	Mode select for high/low voltage regime
28	DQ_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQ_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQ_PULL_B	Input pull control
21:20	DQ_NSLEW	Slew rate control bits for output path NMOS
17:16	DQ_PSLEW	Slew rate control bits for output path PMOS
13:12	DQ_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQ_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	DQ_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQ_ROUT	Impedance control bit settings for output driver
2:0	DQ_DCC	Duty cycle correction bits for output path

0x1AC00014 DIM_D10_DIM_DQ_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG1 register configures the following:

DIM_DQ_PAD_CFG1

DIM_D10_DIM_DQ_PAD_CFG1

Bits	Name	Description
31	DQS_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
30	DQS_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	DQS_LV_MODE	Mode select for high/low voltage regime
28	DQS_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQS_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQS_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	DQS_NSLEW	Slew rate control bits for output path NMOS
17:16	DQS_PSLEW	Slew rate control bits for output path PMOS
13:12	DQS_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQS_PRXDEL	Delay control bits to increase strength of PMOS input drive
7	DQS_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQS_ROUT	Impedance control bit settings for output driver
2:0	DQS_DCC	Duty cycle correction bits for output path

0x1AC00018 DIM_D10_DIM_DQ_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_DQ_PAD_CFG2 register configures the following:

DIM_DQ_PAD_CFG2

DIM_D10_DIM_DQ_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1AC00020 DIM_D10_DIM_DQ_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x1000FF11

The DIM_DQ_PAD_CFG3 register configures the following:

DIM_DQ_PAD_CFG3

DIM_D10_DIM_DQ_PAD_CFG3

Bits	Name	Description
28	DQS_DIFF_MODE	DQS output mode control 1’b1 : differential output (default) 1’b0 : single-ended output; _n output is HIZ
27	RCW_ODT_ENA1	Enable ODT for RCW pad (when hp_mode=1)
26	RCW_ODT_ENA0	Enable ODT for RCW pad (when hp_mode=0)
25:24	RCW_ODT	Impedance control for on-die termination on RCW pad
23	DQ_ODT_ENA1	Enable ODT for DQ pads (when hp_mode=1)
22	DQ_ODT_ENA0	Enable ODT for DQ pads (when hp_mode=0)
21:20	DQ_ODT	Impedance control for on-die termination on DQ pads
19	DQS_ODT_ENA1	Enable ODT for DQS pad (when hp_mode=1)
18	DQS_ODT_ENA0	Enable ODT for DQS pad (when hp_mode=0)

DIM_D10_DIM_DQ_PAD_CFG3 (cont.)

Bits	Name	Description
17:16	DQS_ODT	Impedance control for on-die termination on DQS pad
15:8	DQ_IE_OE	Enable both input receiver and output driver for all DQ pads
5	RCW_IE_OE	Enable both input receiver and output driver for RCW pad
4	DQS_IE_OE	Enable both input receiver and output driver for DQS pad
1	DM_IE	Input received enable for DM pad
0	DM_OE	Output driver enable for DM pad

0x1AC00024 DIM_D10_DIM_DQ_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG4 register configures the following:

DIM_DQ_PAD_CFG4

DIM_D10_DIM_DQ_PAD_CFG4

Bits	Name	Description
31	RCW_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	RCW_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	RCW_LV_MODE	Mode select for high/low voltage regime
25:24	RCW_PULL_B	Input pull control
21:20	RCW_NSLEW	Slew rate control bits for output path NMOS
17:16	RCW_PSLEW	Slew rate control bits for output path PMOS
13:12	RCW_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	RCW_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	RCW_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	RCW_ROUT	Impedance control bit settings for output driver
2:0	RCW_DCC	Duty cycle correction bits for output path

0x1AC00030 DIM_D10_DIM_DQ_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG0 register configures the following:

DIM_DQ_CDC_CTLR_CFG0

DIM_D10_DIM_DQ_CDC_CTLR_CFG0

Bits	Name	Description
25	STAGGER_CAL_ENA	1'b1: Stagger calibration of write and read CDCs once after the other to reduce peak voltage drop. 1'b0: Both write and read CDCs calibrated simultaneously This bit is introduced on the x2 core, so not present on x0 and x1 versions of DIM/PHY.
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1AC00034 DIM_D10_DIM_DQ_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG1 register configures DIM_DQ_CDC_CTLR_CFG1.

DIM_D10_DIM_DQ_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1

0x1AC00038 DIM_D10_DIM_DQ_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG0 register configures DIM_DQ_CDC_CAL_TIMER_CFG0.

DIM_D10_DIM_DQ_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1AC0003C DIM_D10_DIM_DQ_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG1 register configures DIM_DQ_CDC_CAL_TIMER_CFG1.

DIM_D10_DIM_DQ_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1AC00040 DIM_D10_DIM_DQ_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_REFCOUNT_CFG register configures DIM_DQ_CDC_REFCOUNT_CFG.

DIM_D10_DIM_DQ_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1AC00044 DIM_D10_DIM_DQ_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_DQ_CDC_COARSE_CAL_CFG configures DIM_DQ_CDC_COARSE_CAL_CFG.

DIM_D10_DIM_DQ_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1AC00048 DIM_D10_DIM_DQ_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_RSVD_CFG register configures DIM_DQ_CDC_RSVD_CFG.

DIM_D10_DIM_DQ_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1AC0004C DIM_D10_DIM_DQ_RD_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_OFFSET_CFG register configures DIM_DQ_RD_CDC_OFFSET_CFG.

DIM_D10_DIM_DQ_RD_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AC00050 DIM_D10_DIM_DQ_RD_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_DELAY_CFG register configures DIM_DQ_RD_CDC_DELAY_CFG.

DIM_D10_DIM_DQ_RD_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AC00054 DIM_D10_DIM_DQ_RD_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_MODE_CFG register configures DIM_DQ_RD_CDC_SW_MODE_CFG.

DIM_D10_DIM_DQ_RD_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1’b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AC00058 DIM_D10_DIM_DQ_RD_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_TEST_CFG register configures DIM_DQ_RD_CDC_TEST_CFG.

DIM_D10_DIM_DQ_RD_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1’b1: Test outputs from the main DDA are connected to the CDC test ports 1’b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1’b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1’b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1’b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1’b0 : CDC test ports disabled

DIM_D10_DIM_DQ_RD_CDC_TEST_CFG (cont.)

Bits	Name	Description
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AC0005C DIM_D10_DIM_DQ_RD_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_OVRD_CFG register configures DIM_DQ_RD_CDC_SW_OVRD_CFG.

DIM_D10_DIM_DQ_RD_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AC00060 DIM_D10_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SLAVE_DDA_CFG register configures DIM_DQ_RD_CDC_SLAVE_DDA_CFG.

DIM_D10_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Bits	Name	Description
17	SLAV_DDA_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit-step count 1'b0: Programmed offset is added/subtracted from the unit-step count
16	SLAV_DDA_OFFSET_SIGN	1'b1: Offset is subtracted from the unit-step count. This subtraction feature is not supported on x0 and x1 PHY cores (bit RESERVED). Supported on the x2 core version. 1'b0: Offset is added to the unit-step count
15:12	SLAVE_DDA_OFFSET	unit-step offset for slave DDA.
10:0	SLAVE_DDA_DELAY	Delay required from slave DDA programmed in pico seconds.

0x1AC00070 DIM_D10_DIM_DQ_RD_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_RD_CDC_STATUS0 register configures DIM_DQ_RD_CDC_STATUS0.

DIM_D10_DIM_DQ_RD_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AC00074 DIM_D10_DIM_DQ_RD_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS1 register configures DIM_DQ_RD_CDC_STATUS1.

DIM_D10_DIM_DQ_RD_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.

DIM_D10_DIM_DQ_RD_CDC_STATUS1 (cont.)

Bits	Name	Description
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AC00078 DIM_D10_DIM_DQ_RD_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_RD_CDC_STATUS2 register configures DIM_DQ_RD_CDC_STATUS2.

DIM_D10_DIM_DQ_RD_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AC0007C DIM_D10_DIM_DQ_RD_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS3 register configures DIM_DQ_RD_CDC_STATUS3.

DIM_D10_DIM_DQ_RD_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AC00080 DIM_D10_DIM_DQ_RD_CDC_STATUS4

Type: Read
Clock: HCLK
Reset State: 0x000000FF

The DIM_DQ_RD_CDC_STATUS4 register configures DIM_DQ_RD_CDC_STATUS4.

DIM_D10_DIM_DQ_RD_CDC_STATUS4

Bits	Name	Description
7:4	SLAVE_DDA_DA1_TAPS	Number if unit taps applied to delay array 1 of slave DDA
3:0	SLAVE_DDA_DA0_TAPS	Number if unit taps applied to delay array 0 of slave DDA

0x1AC000AC DIM_D10_DIM_DQ_WR_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_OFFSET_CFG register configures DIM_DQ_WR_CDC_OFFSET_CFG.

DIM_D10_DIM_DQ_WR_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AC000B0 DIM_D10_DIM_DQ_WR_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_DELAY_CFG register configures DIM_DQ_WR_CDC_DELAY_CFG.

DIM_D10_DIM_DQ_WR_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AC000B4 DIM_D10_DIM_DQ_WR_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_MODE_CFG register configures DIM_DQ_WR_CDC_SW_MODE_CFG.

DIM_D10_DIM_DQ_WR_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AC000B8 DIM_D10_DIM_DQ_WR_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_TEST_CFG register configures DIM_DQ_WR_CDC_TEST_CFG.

DIM_D10_DIM_DQ_WR_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AC000BC DIM_D10_DIM_DQ_WR_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_OVRD_CFG register configures DIM_DQ_WR_CDC_SW_OVRD_CFG.

DIM_D10_DIM_DQ_WR_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode

DIM_D10_DIM_DQ_WR_CDC_SW_OVRD_CFG (cont.)

Bits	Name	Description
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AC000D0 DIM_D10_DIM_DQ_WR_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_WR_CDC_STATUS0 register configures DIM_DQ_WR_CDC_STATUS0.

DIM_D10_DIM_DQ_WR_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.

DIM_D10_DIM_DQ_WR_CDC_STATUS0 (cont.)

Bits	Name	Description
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AC000D4 DIM_D10_DIM_DQ_WR_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS1 register configures DIM_DQ_WR_CDC_STATUS1.

DIM_D10_DIM_DQ_WR_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AC000D8 DIM_D10_DIM_DQ_WR_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_WR_CDC_STATUS2 register configures DIM_DQ_WR_CDC_STATUS2.

DIM_D10_DIM_DQ_WR_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AC000DC DIM_D10_DIM_DQ_WR_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS3 register configures DIM_DQ_WR_CDC_STATUS3.

DIM_D10_DIM_DQ_WR_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AC00100 DIM_D10_DIM_DQ_DQ_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQ_IOC_SLV_CFG register configures DIM_DQ_DQ_IOC_SLV_CFG.

DIM_D10_DIM_DQ_DQ_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	

DIM_D10_DIM_DQ_DQ_IOC_SLV_CFG (cont.)

Bits	Name	Description
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1AC00104 DIM_D10_DIM_DQ_DQ_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQ_IOC_SLV_STATUS register configures DIM_CA_CA_IOC_SLV_STATUS.

DIM_D10_DIM_DQ_DQ_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

0x1AC00110 DIM_D10_DIM_DQ_DQS_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQS_IOC_SLV_CFG register configures DIM_DQ_DQS_IOC_SLV_CFG.

DIM_D10_DIM_DQ_DQS_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1AC00114 DIM_D10_DIM_DQ_DQS_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQS_IOC_SLV_STATUS register configures DIM_DQ_DQS_IOC_SLV_STATUS.

DIM_D10_DIM_DQ_DQS_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

13.10 DIM D11 DQ Registers (0x1AD00000 DIM_D11_REG_BASE)

This section describes the D11 DIM DQ TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1AD00000 DIM_D11_DIM_DQ_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_DQ_TOP_CFG register configures the following:

DIM_DQ_TOP_CFG

DIM_D11_DIM_DQ_TOP_CFG

Bits	Name	Description
26	CDC_LDO_EN	Enablement of CDC LDO 1’b1 : Enabled 1’b0 : Disabled LDO and power provided from switches (default)
25	CDC_SWITCH_RC_EN	Enablement of CDC power RC (LPF) switch 1’b1 : Enabled 1’b0 : Disabled (default)
24	CDC_SWITCH_BYPASS_OFF	Enablement of CDC power bypass switch 1’b1 : Disabled 1’b0 : Enabled (default)
16	RCW_EN	Enablement of the Read Capture Window 1’b1 : Enable the RCW 1’b0 : Disabled (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1 : from Read CDCCAL 1’b0 : from Write CDCCAL (default)
12	DEBUG_BUS_EN	1’b1 : Enables the debug bus functionality 1’b0 : Disables the debug bus and drives all ’0’s on debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_dq[5:0] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend

DIM_D11_DIM_DQ_TOP_CFG (cont.)

Bits	Name	Description
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1'b0) 1'b1 : with pipe extend (default) 1'b0 : without pipe extend
0	WR_CLK_SEL	Write clock select 1'b1 : With write CDC (default) 1'b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1AD00004 DIM_D11_DIM_DQ_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_DQ_HW_INFO register configures the following:

DIM_DQ_HW_INFO

DIM_D11_DIM_DQ_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1AD00008 DIM_D11_DIM_DQ_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_DQ_HW_VERSION register configures the following:

DIM_DQ_HW_VERSION

DIM_D11_DIM_DQ_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.

DIM_D11_DIM_DQ_HW_VERSION (cont.)

Bits	Name	Description
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1AD00010 DIM_D11_DIM_DQ_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG0 register configures the following:

DIM_DQ_PAD_CFG0

DIM_D11_DIM_DQ_PAD_CFG0

Bits	Name	Description
31	DQ_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	DQ_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	DQ_LV_MODE	Mode select for high/low voltage regime
28	DQ_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQ_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQ_PULL_B	Input pull control
21:20	DQ_NSLEW	Slew rate control bits for output path NMOS
17:16	DQ_PSLEW	Slew rate control bits for output path PMOS
13:12	DQ_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQ_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	DQ_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQ_ROUT	Impedance control bit settings for output driver
2:0	DQ_DCC	Duty cycle correction bits for output path

0x1AD00014 DIM_D11_DIM_DQ_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG1 register configures the following:

DIM_DQ_PAD_CFG1

DIM_D11_DIM_DQ_PAD_CFG1

Bits	Name	Description
31	DQS_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
30	DQS_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	DQS_LV_MODE	Mode select for high/low voltage regime
28	DQS_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQS_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQS_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	DQS_NSLEW	Slew rate control bits for output path NMOS
17:16	DQS_PSLEW	Slew rate control bits for output path PMOS
13:12	DQS_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQS_PRXDEL	Delay control bits to increase strength of PMOS input drive
7	DQS_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQS_ROUT	Impedance control bit settings for output driver
2:0	DQS_DCC	Duty cycle correction bits for output path

0x1AD00018 DIM_D11_DIM_DQ_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_DQ_PAD_CFG2 register configures the following:

DIM_DQ_PAD_CFG2

DIM_D11_DIM_DQ_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1AD00020 DIM_D11_DIM_DQ_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x1000FF11

The DIM_DQ_PAD_CFG3 register configures the following:

DIM_DQ_PAD_CFG3

DIM_D11_DIM_DQ_PAD_CFG3

Bits	Name	Description
28	DQS_DIFF_MODE	DQS output mode control 1’b1 : differential output (default) 1’b0 : single-ended output; _n output is HIZ
27	RCW_ODT_ENA1	Enable ODT for RCW pad (when hp_mode=1)
26	RCW_ODT_ENA0	Enable ODT for RCW pad (when hp_mode=0)
25:24	RCW_ODT	Impedance control for on-die termination on RCW pad
23	DQ_ODT_ENA1	Enable ODT for DQ pads (when hp_mode=1)
22	DQ_ODT_ENA0	Enable ODT for DQ pads (when hp_mode=0)
21:20	DQ_ODT	Impedance control for on-die termination on DQ pads
19	DQS_ODT_ENA1	Enable ODT for DQS pad (when hp_mode=1)
18	DQS_ODT_ENA0	Enable ODT for DQS pad (when hp_mode=0)

DIM_D11_DIM_DQ_PAD_CFG3 (cont.)

Bits	Name	Description
17:16	DQS_ODT	Impedance control for on-die termination on DQS pad
15:8	DQ_IE_OE	Enable both input receiver and output driver for all DQ pads
5	RCW_IE_OE	Enable both input receiver and output driver for RCW pad
4	DQS_IE_OE	Enable both input receiver and output driver for DQS pad
1	DM_IE	Input received enable for DM pad
0	DM_OE	Output driver enable for DM pad

0x1AD00024 DIM_D11_DIM_DQ_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG4 register configures the following:

DIM_DQ_PAD_CFG4

DIM_D11_DIM_DQ_PAD_CFG4

Bits	Name	Description
31	RCW_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	RCW_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	RCW_LV_MODE	Mode select for high/low voltage regime
25:24	RCW_PULL_B	Input pull control
21:20	RCW_NSLEW	Slew rate control bits for output path NMOS
17:16	RCW_PSLEW	Slew rate control bits for output path PMOS
13:12	RCW_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	RCW_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	RCW_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	RCW_ROUT	Impedance control bit settings for output driver
2:0	RCW_DCC	Duty cycle correction bits for output path

0x1AD00030 DIM_D11_DIM_DQ_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG0 register configures the following:

DIM_DQ_CDC_CTLR_CFG0

DIM_D11_DIM_DQ_CDC_CTLR_CFG0

Bits	Name	Description
25	STAGGER_CAL_ENA	1'b1: Stagger calibration of write and read CDCs once after the other to reduce peak voltage drop. 1'b0: Both write and read CDCs calibrated simultaneously This bit is introduced on the x2 core, so not present on x0 and x1 versions of DIM/PHY.
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1AD00034 DIM_D11_DIM_DQ_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG1 register configures the following:

DIM_DQ_CDC_CTLR_CFG1

DIM_D11_DIM_DQ_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1

0x1AD00038 DIM_D11_DIM_DQ_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG0 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG0

DIM_D11_DIM_DQ_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1AD0003C DIM_D11_DIM_DQ_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG1 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG1

DIM_D11_DIM_DQ_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1AD00040 DIM_D11_DIM_DQ_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_REFCOUNT_CFG register configures the following:

DIM_DQ_CDC_REFCOUNT_CFG

DIM_D11_DIM_DQ_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1AD00044 DIM_D11_DIM_DQ_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_DQ_CDC_COARSE_CAL_CFG configures the following:

DIM_DQ_CDC_COARSE_CAL_CFG

DIM_D11_DIM_DQ_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1AD00048 DIM_D11_DIM_DQ_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_RSVD_CFG register configures the following:

DIM_DQ_CDC_RSVD_CFG

DIM_D11_DIM_DQ_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1AD0004C DIM_D11_DIM_DQ_RD_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_OFFSET_CFG register configures the following:

DIM_DQ_RD_CDC_OFFSET_CFG

DIM_D11_DIM_DQ_RD_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AD00050 DIM_D11_DIM_DQ_RD_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_DELAY_CFG register configures the following:

DIM_DQ_RD_CDC_DELAY_CFG

DIM_D11_DIM_DQ_RD_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AD00054 DIM_D11_DIM_DQ_RD_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_RD_CDC_SW_MODE_CFG

DIM_D11_DIM_DQ_RD_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AD00058 DIM_D11_DIM_DQ_RD_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_TEST_CFG register configures the following:

DIM_DQ_RD_CDC_TEST_CFG

DIM_D11_DIM_DQ_RD_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AD0005C DIM_D11_DIM_DQ_RD_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_RD_CDC_SW_OVRD_CFG

DIM_D11_DIM_DQ_RD_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode

DIM_D11_DIM_DQ_RD_CDC_SW_OVRD_CFG (cont.)

Bits	Name	Description
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AD00060 DIM_D11_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SLAVE_DDA_CFG register configures the following:

DIM_DQ_RD_CDC_SLAVE_DDA_CFG

DIM_D11_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Bits	Name	Description
17	SLAV_DDA_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit-step count 1'b0: Programmed offset is added/subtracted from the unit-step count
16	SLAV_DDA_OFFSET_SIGN	1'b1: Offset is subtracted from the unit-step count. This subtraction feature is not supported on x0 and x1 PHY cores (bit RESERVED). Supported on the x2 core version. 1'b0: Offset is added to the unit-step count
15:12	SLAVE_DDA_OFFSET	unit-step offset for slave DDA.
10:0	SLAVE_DDA_DELAY	Delay required from slave DDA programmed in pico seconds.

0x1AD00070 DIM_D11_DIM_DQ_RD_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_RD_CDC_STATUS0 register configures the following:

DIM_DQ_RD_CDC_STATUS0

DIM_D11_DIM_DQ_RD_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AD00074 DIM_D11_DIM_DQ_RD_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS1 register configures the following:

DIM_DQ_RD_CDC_STATUS1

DIM_D11_DIM_DQ_RD_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AD00078 DIM_D11_DIM_DQ_RD_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_RD_CDC_STATUS2 register configures the following:

DIM_DQ_RD_CDC_STATUS2

DIM_D11_DIM_DQ_RD_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AD0007C DIM_D11_DIM_DQ_RD_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS3 register configures the following:

DIM_DQ_RD_CDC_STATUS3

DIM_D11_DIM_DQ_RD_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration

DIM_D11_DIM_DQ_RD_CDC_STATUS3 (cont.)

Bits	Name	Description
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AD00080 DIM_D11_DIM_DQ_RD_CDC_STATUS4

Type: Read
Clock: HCLK
Reset State: 0x000000FF

The DIM_DQ_RD_CDC_STATUS4 register configures the following:

DIM_DQ_RD_CDC_STATUS4

DIM_D11_DIM_DQ_RD_CDC_STATUS4

Bits	Name	Description
7:4	SLAVE_DDA_DA1_TAPS	Number if unit taps applied to delay array 1 of slave DDA
3:0	SLAVE_DDA_DA0_TAPS	Number if unit taps applied to delay array 0 of slave DDA

0x1AD000AC DIM_D11_DIM_DQ_WR_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_OFFSET_CFG register configures the following:

DIM_DQ_WR_CDC_OFFSET_CFG

DIM_D11_DIM_DQ_WR_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1’b1: The programmed offset is directly loaded as subunit count 1’b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1’b1: Offset is subtracted from the subunit count 1’b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1’b1: The programmed offset is directly loaded as unit step count 1’b0: Programmed offset is added/subtracted from the unit step count

DIM_D11_DIM_DQ_WR_CDC_OFFSET_CFG (cont.)

Bits	Name	Description
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AD000B0 DIM_D11_DIM_DQ_WR_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_DELAY_CFG register configures the following:

DIM_DQ_WR_CDC_DELAY_CFG

DIM_D11_DIM_DQ_WR_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AD000B4 DIM_D11_DIM_DQ_WR_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_WR_CDC_SW_MODE_CFG

DIM_D11_DIM_DQ_WR_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.

DIM_D11_DIM_DQ_WR_CDC_SW_MODE_CFG (cont.)

Bits	Name	Description
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AD000B8 DIM_D11_DIM_DQ_WR_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_TEST_CFG register configures the following:

DIM_DQ_WR_CDC_TEST_CFG

DIM_D11_DIM_DQ_WR_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AD000BC DIM_D11_DIM_DQ_WR_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_WR_CDC_SW_OVRD_CFG

DIM_D11_DIM_DQ_WR_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AD000D0 DIM_D11_DIM_DQ_WR_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_WR_CDC_STATUS0 register configures the following:

DIM_DQ_WR_CDC_STATUS0

DIM_D11_DIM_DQ_WR_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AD000D4 DIM_D11_DIM_DQ_WR_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS1 register configures the following:

DIM_DQ_WR_CDC_STATUS1

DIM_D11_DIM_DQ_WR_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AD000D8 DIM_D11_DIM_DQ_WR_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_WR_CDC_STATUS2 register configures the following:

DIM_DQ_WR_CDC_STATUS2

DIM_D11_DIM_DQ_WR_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AD000DC DIM_D11_DIM_DQ_WR_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS3 register configures the following:

DIM_DQ_WR_CDC_STATUS3

DIM_D11_DIM_DQ_WR_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration

DIM_D11_DIM_DQ_WR_CDC_STATUS3 (cont.)

Bits	Name	Description
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AD00100 DIM_D11_DIM_DQ_DQ_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQ_IOC_SLV_CFG register configures the following:

DIM_DQ_DQ_IOC_SLV_CFG

DIM_D11_DIM_DQ_DQ_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1AD00104 DIM_D11_DIM_DQ_DQ_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQ_IOC_SLV_STATUS register configures the following:

DIM_CA_CA_IOC_SLV_STATUS

DIM_D11_DIM_DQ_DQ_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

0x1AD00110 DIM_D11_DIM_DQ_DQS_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQS_IOC_SLV_CFG register configures the following:

DIM_DQ_DQS_IOC_SLV_CFG

DIM_D11_DIM_DQ_DQS_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1AD00114 DIM_D11_DIM_DQ_DQS_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQS_IOC_SLV_STATUS register configures the following:

DIM_DQ_DQS_IOC_SLV_STATUS

DIM_D11_DIM_DQ_DQS_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

13.11 DIM D12 DQ Registers (0x1AE00000 DIM_D12_REG_BASE)

This section describes the D12 DIM DQ TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1AE00000 DIM_D12_DIM_DQ_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_DQ_TOP_CFG register configures the following:

DIM_DQ_TOP_CFG

DIM_D12_DIM_DQ_TOP_CFG

Bits	Name	Description
26	CDC_LDO_EN	Enablement of CDC LDO 1’b1 : Enabled 1’b0 : Disabled LDO and power provided from switches (default)
25	CDC_SWITCH_RC_EN	Enablement of CDC power RC (LPF) switch 1’b1 : Enabled 1’b0 : Disabled (default)
24	CDC_SWITCH_BYPASS_OFF	Enablement of CDC power bypass switch 1’b1 : Disabled 1’b0 : Enabled (default)
16	RCW_EN	Enablement of the Read Capture Window 1’b1 : Enable the RCW 1’b0 : Disabled (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1 : from Read CDCCAL 1’b0 : from Write CDCCAL (default)
12	DEBUG_BUS_EN	1’b1 : Enables the debug bus functionality 1’b0 : Disables the debug bus and drives all ’0’s on debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_dq[5:0] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend

DIM_D12_DIM_DQ_TOP_CFG (cont.)

Bits	Name	Description
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1'b0) 1'b1 : with pipe extend (default) 1'b0 : without pipe extend
0	WR_CLK_SEL	Write clock select 1'b1 : With write CDC (default) 1'b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1AE00004 DIM_D12_DIM_DQ_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_DQ_HW_INFO register configures the following:

DIM_DQ_HW_INFO

DIM_D12_DIM_DQ_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1AE00008 DIM_D12_DIM_DQ_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_DQ_HW_VERSION register configures the following:

DIM_DQ_HW_VERSION

DIM_D12_DIM_DQ_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.

DIM_D12_DIM_DQ_HW_VERSION (cont.)

Bits	Name	Description
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1AE00010 DIM_D12_DIM_DQ_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG0 register configures the following:

DIM_DQ_PAD_CFG0

DIM_D12_DIM_DQ_PAD_CFG0

Bits	Name	Description
31	DQ_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	DQ_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	DQ_LV_MODE	Mode select for high/low voltage regime
28	DQ_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQ_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQ_PULL_B	Input pull control
21:20	DQ_NSLEW	Slew rate control bits for output path NMOS
17:16	DQ_PSLEW	Slew rate control bits for output path PMOS
13:12	DQ_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQ_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	DQ_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQ_ROUT	Impedance control bit settings for output driver
2:0	DQ_DCC	Duty cycle correction bits for output path

0x1AE00014 DIM_D12_DIM_DQ_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG1 register configures the following:

DIM_DQ_PAD_CFG1

DIM_D12_DIM_DQ_PAD_CFG1

Bits	Name	Description
31	DQS_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
30	DQS_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	DQS_LV_MODE	Mode select for high/low voltage regime
28	DQS_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQS_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQS_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	DQS_NSLEW	Slew rate control bits for output path NMOS
17:16	DQS_PSLEW	Slew rate control bits for output path PMOS
13:12	DQS_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQS_PRXDEL	Delay control bits to increase strength of PMOS input drive
7	DQS_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQS_ROUT	Impedance control bit settings for output driver
2:0	DQS_DCC	Duty cycle correction bits for output path

0x1AE00018 DIM_D12_DIM_DQ_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_DQ_PAD_CFG2 register configures the following:

DIM_DQ_PAD_CFG2

DIM_D12_DIM_DQ_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1AE00020 DIM_D12_DIM_DQ_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x1000FF11

The DIM_DQ_PAD_CFG3 register configures the following:

DIM_DQ_PAD_CFG3

DIM_D12_DIM_DQ_PAD_CFG3

Bits	Name	Description
28	DQS_DIFF_MODE	DQS output mode control 1’b1 : differential output (default) 1’b0 : single-ended output; _n output is HIZ
27	RCW_ODT_ENA1	Enable ODT for RCW pad (when hp_mode=1)
26	RCW_ODT_ENA0	Enable ODT for RCW pad (when hp_mode=0)
25:24	RCW_ODT	Impedance control for on-die termination on RCW pad
23	DQ_ODT_ENA1	Enable ODT for DQ pads (when hp_mode=1)
22	DQ_ODT_ENA0	Enable ODT for DQ pads (when hp_mode=0)
21:20	DQ_ODT	Impedance control for on-die termination on DQ pads
19	DQS_ODT_ENA1	Enable ODT for DQS pad (when hp_mode=1)
18	DQS_ODT_ENA0	Enable ODT for DQS pad (when hp_mode=0)

DIM_D12_DIM_DQ_PAD_CFG3 (cont.)

Bits	Name	Description
17:16	DQS_ODT	Impedance control for on-die termination on DQS pad
15:8	DQ_IE_OE	Enable both input receiver and output driver for all DQ pads
5	RCW_IE_OE	Enable both input receiver and output driver for RCW pad
4	DQS_IE_OE	Enable both input receiver and output driver for DQS pad
1	DM_IE	Input received enable for DM pad
0	DM_OE	Output driver enable for DM pad

0x1AE00024 DIM_D12_DIM_DQ_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG4 register configures the following:

DIM_DQ_PAD_CFG4

DIM_D12_DIM_DQ_PAD_CFG4

Bits	Name	Description
31	RCW_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	RCW_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	RCW_LV_MODE	Mode select for high/low voltage regime
25:24	RCW_PULL_B	Input pull control
21:20	RCW_NSLEW	Slew rate control bits for output path NMOS
17:16	RCW_PSLEW	Slew rate control bits for output path PMOS
13:12	RCW_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	RCW_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	RCW_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	RCW_ROUT	Impedance control bit settings for output driver
2:0	RCW_DCC	Duty cycle correction bits for output path

0x1AE00030 DIM_D12_DIM_DQ_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG0 register configures the following:

DIM_DQ_CDC_CTLR_CFG0

DIM_D12_DIM_DQ_CDC_CTLR_CFG0

Bits	Name	Description
25	STAGGER_CAL_ENA	1'b1: Stagger calibration of write and read CDCs once after the other to reduce peak voltage drop. 1'b0: Both write and read CDCs calibrated simultaneously This bit is introduced on the x2 core, so not present on x0 and x1 versions of DIM/PHY.
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1AE00034 DIM_D12_DIM_DQ_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG1 register configures the following:

DIM_DQ_CDC_CTLR_CFG1

DIM_D12_DIM_DQ_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1

0x1AE00038 DIM_D12_DIM_DQ_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG0 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG0

DIM_D12_DIM_DQ_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1AE0003C DIM_D12_DIM_DQ_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG1 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG1

DIM_D12_DIM_DQ_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1AE00040 DIM_D12_DIM_DQ_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_REFCOUNT_CFG register configures the following:

DIM_DQ_CDC_REFCOUNT_CFG

DIM_D12_DIM_DQ_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1AE00044 DIM_D12_DIM_DQ_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_DQ_CDC_COARSE_CAL_CFG configures the following:

DIM_DQ_CDC_COARSE_CAL_CFG

DIM_D12_DIM_DQ_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1AE00048 DIM_D12_DIM_DQ_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_RSVD_CFG register configures the following:

DIM_DQ_CDC_RSVD_CFG

DIM_D12_DIM_DQ_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1AE0004C DIM_D12_DIM_DQ_RD_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_OFFSET_CFG register configures the following:

DIM_DQ_RD_CDC_OFFSET_CFG

DIM_D12_DIM_DQ_RD_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AE00050 DIM_D12_DIM_DQ_RD_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_DELAY_CFG register configures the following:

DIM_DQ_RD_CDC_DELAY_CFG

DIM_D12_DIM_DQ_RD_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AE00054 DIM_D12_DIM_DQ_RD_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_RD_CDC_SW_MODE_CFG

DIM_D12_DIM_DQ_RD_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AE00058 DIM_D12_DIM_DQ_RD_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_TEST_CFG register configures the following:

DIM_DQ_RD_CDC_TEST_CFG

DIM_D12_DIM_DQ_RD_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AE0005C DIM_D12_DIM_DQ_RD_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_RD_CDC_SW_OVRD_CFG

DIM_D12_DIM_DQ_RD_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode

DIM_D12_DIM_DQ_RD_CDC_SW_OVRD_CFG (cont.)

Bits	Name	Description
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AE00060 DIM_D12_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SLAVE_DDA_CFG register configures the following:

DIM_DQ_RD_CDC_SLAVE_DDA_CFG

DIM_D12_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Bits	Name	Description
17	SLAV_DDA_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit-step count 1'b0: Programmed offset is added/subtracted from the unit-step count
16	SLAV_DDA_OFFSET_SIGN	1'b1: Offset is subtracted from the unit-step count. This subtraction feature is not supported on x0 and x1 PHY cores (bit RESERVED). Supported on the x2 core version. 1'b0: Offset is added to the unit-step count
15:12	SLAVE_DDA_OFFSET	unit-step offset for slave DDA.
10:0	SLAVE_DDA_DELAY	Delay required from slave DDA programmed in pico seconds.

0x1AE00070 DIM_D12_DIM_DQ_RD_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_RD_CDC_STATUS0 register configures the following:

DIM_DQ_RD_CDC_STATUS0

DIM_D12_DIM_DQ_RD_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AE00074 DIM_D12_DIM_DQ_RD_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS1 register configures the following:

DIM_DQ_RD_CDC_STATUS1

DIM_D12_DIM_DQ_RD_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AE00078 DIM_D12_DIM_DQ_RD_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_RD_CDC_STATUS2 register configures the following:

DIM_DQ_RD_CDC_STATUS2

DIM_D12_DIM_DQ_RD_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AE0007C DIM_D12_DIM_DQ_RD_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS3 register configures the following:

DIM_DQ_RD_CDC_STATUS3

DIM_D12_DIM_DQ_RD_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration

DIM_D12_DIM_DQ_RD_CDC_STATUS3 (cont.)

Bits	Name	Description
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AE00080 DIM_D12_DIM_DQ_RD_CDC_STATUS4

Type: Read
Clock: HCLK
Reset State: 0x000000FF

The DIM_DQ_RD_CDC_STATUS4 register configures the following:

DIM_DQ_RD_CDC_STATUS4

DIM_D12_DIM_DQ_RD_CDC_STATUS4

Bits	Name	Description
7:4	SLAVE_DDA_DA1_TAPS	Number if unit taps applied to delay array 1 of slave DDA
3:0	SLAVE_DDA_DA0_TAPS	Number if unit taps applied to delay array 0 of slave DDA

0x1AE000AC DIM_D12_DIM_DQ_WR_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_OFFSET_CFG register configures the following:

DIM_DQ_WR_CDC_OFFSET_CFG

DIM_D12_DIM_DQ_WR_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1’b1: The programmed offset is directly loaded as subunit count 1’b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1’b1: Offset is subtracted from the subunit count 1’b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1’b1: The programmed offset is directly loaded as unit step count 1’b0: Programmed offset is added/subtracted from the unit step count

DIM_D12_DIM_DQ_WR_CDC_OFFSET_CFG (cont.)

Bits	Name	Description
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AE000B0 DIM_D12_DIM_DQ_WR_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_DELAY_CFG register configures the following:

DIM_DQ_WR_CDC_DELAY_CFG

DIM_D12_DIM_DQ_WR_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AE000B4 DIM_D12_DIM_DQ_WR_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_WR_CDC_SW_MODE_CFG

DIM_D12_DIM_DQ_WR_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.

DIM_D12_DIM_DQ_WR_CDC_SW_MODE_CFG (cont.)

Bits	Name	Description
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AE000B8 DIM_D12_DIM_DQ_WR_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_TEST_CFG register configures the following:

DIM_DQ_WR_CDC_TEST_CFG

DIM_D12_DIM_DQ_WR_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AE000BC DIM_D12_DIM_DQ_WR_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_WR_CDC_SW_OVRD_CFG

DIM_D12_DIM_DQ_WR_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AE000D0 DIM_D12_DIM_DQ_WR_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_WR_CDC_STATUS0 register configures the following:

DIM_DQ_WR_CDC_STATUS0

DIM_D12_DIM_DQ_WR_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AE000D4 DIM_D12_DIM_DQ_WR_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS1 register configures the following:

DIM_DQ_WR_CDC_STATUS1

DIM_D12_DIM_DQ_WR_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AE000D8 DIM_D12_DIM_DQ_WR_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_WR_CDC_STATUS2 register configures the following:

DIM_DQ_WR_CDC_STATUS2

DIM_D12_DIM_DQ_WR_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AE000DC DIM_D12_DIM_DQ_WR_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS3 register configures the following:

DIM_DQ_WR_CDC_STATUS3

DIM_D12_DIM_DQ_WR_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration

DIM_D12_DIM_DQ_WR_CDC_STATUS3 (cont.)

Bits	Name	Description
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AE00100 DIM_D12_DIM_DQ_DQ_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQ_IOC_SLV_CFG register configures the following:

DIM_DQ_DQ_IOC_SLV_CFG

DIM_D12_DIM_DQ_DQ_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1AE00104 DIM_D12_DIM_DQ_DQ_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQ_IOC_SLV_STATUS register configures the following:

DIM_CA_CA_IOC_SLV_STATUS

DIM_D12_DIM_DQ_DQ_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

0x1AE00110 DIM_D12_DIM_DQ_DQS_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQS_IOC_SLV_CFG register configures the following:

DIM_DQ_DQS_IOC_SLV_CFG

DIM_D12_DIM_DQ_DQS_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1AE00114 DIM_D12_DIM_DQ_DQS_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQS_IOC_SLV_STATUS register configures the following:

DIM_DQ_DQS_IOC_SLV_STATUS

DIM_D12_DIM_DQ_DQS_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

13.12 LPA IF Registers (0x28100000 LPA_IF_BASE)

This section contains the LPAIF registers.

13.12.1 LPA Interface registers

The LPA_IF address map is divided into 14, 4 KB regions to allow MPU protection of audio interface control, mixer, each interrupt control register set and each DMA channel. The 4 KB regions and contents are summarized in the table below:

Address Range	Contents
Addr: 0x0000 - 0x0FFF	Audio Interfaces: PCM, I2S, Digital Mic, VFR sel, spare
Addr: 0x1000 - 0x1FFF	Write DMA Loopback & Mix Control, Test mode
Addr: 0x2000 - 0x2FFF	Mixer Control Register
Addr: 0x3000 - 0x3FFF	Interrupt control and status for audio_out0_irq
Addr: 0x4000 - 0x4FFF	Interrupt control and status for audio_out1_irq
Addr: 0x5000 - 0x5FFF	Interrupt control and status for audio_out2_irq
Addr: 0x6000 - 0x6FFF	Read DMA channel 0 control and status
Addr: 0x7000 - 0x7FFF	Read DMA channel 1 control and status
Addr: 0x8000 - 0x8FFF	Read DMA channel 2 control and status
Addr: 0x9000 - 0x9FFF	Read DMA channel 3 control and status
Addr: 0xA000 - 0xAFFF	Read DMA channel 4 control and status
Addr: 0xB000 - 0xBFFF	Write DMA channel 5 control and status
Addr: 0xC000 - 0xCFFF	Write DMA channel 6 control and status
Addr: 0xD000 - 0xDFFF	Write DMA channel 7 control and status
Addr: 0xE000 - 0xEFFF	Write DMA channel 8 control and status

13.12.1.1 PCM Interface

This section describes the control registers for the PCM interface.

NOTE The reset for the PCM interface comes from the clock controller in LPASS. The logic in the PCM interface is reset synchronously so a clock must be present to get a clean startup. Each time the PCM interface is started, SW should:

1. set the LPASS clock control such that the valid clock is selected and if the clock is external, it must be running
2. write to LPASS clock control to issue a reset to the PCM interface
3. Configure the PCM control register (LPAIF_PCM_CTL)
4. release the reset (PCM setting must not be changed unless reset is asserted or the PCM clock is off as there is no enable bit)

0x28100000 LPAIF_PCM_CTL

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0006_8000

Control registers for the PCM interface.

LPAIF_PCM_CTL

Bits	Name	Description
31:19	RESERVED	
18	CTRL_DATA_OE	SW: RW, HW: R When set, the PCM block will tri-state the data out signal except when the PCM block is driving the active slot. This is necessary only when multiple masters are connected to the same data line. When clear, the PCM block will drive the data signal at all times and must be the only master.
17:15	RATE	SW: RW, HW: R These bits define the number of bits clocks per PCM frame for long and short frame sync formats. This will allow the APQ to support PCM rates other than 2.048 MHz (PCM Mode) and 128 kHz (AUX PCM mode). These bits MUST ALWAYS be set regardless of whether the SYNC_SRC is set for EXTERNAL or INTERNAL. The number of slots available per frame is the number of bits per frame divided by the number of bits per slot (TPCM_WIDTH and RPCM WIDTH). The number of bits per frame is common between the transmit and receive data but the slot width and slot selection is independent. Assuming a desired frame rate of 8 kHz: 0x0: 8 (64 kHZ) 0x1: 16 (128 kHz, AUX PCM mode) 0x2: 32 (256 kHz) 0x3: 64 (512 kHZ) 0x4: 128 (1024 kHZ) 0x5: 256 (2048 kHZ , PCM mode, default value)
14	LOOPBACK	SW: RW, HW: R When set, the PCM DOUT is looped back to PCM DIN internally.
13	SYNC_SRC	SW: RW, HW: R When set, the PCM block will generate a sync signal to drive offchip and for internal use. When cleared, the PCM block will use an external sync. The type of sync generated or expected is selected by AUX_MODE. 0x0: EXTERNAL 0x1: INTERNAL

LPAIF_PCM_CTL (cont.)

Bits	Name	Description
12	AUX_MODE	SW: RW, HW: R Selects between PCM (short sync) and Aux PCM (long sync) modes. In short sync mode, the sync pulse is one clock period wide and comes before the MSB of the first slot. In long sync mode, the sync pulse has a 50% duty cycle and its rising edge is coincident with the MSB of the first slot: 0x0: PCM 0x1: AUX
11	RPCM_WIDTH	SW: RW, HW: R Selects between 8 and 16 bit samples in the incoming stream: 0x0: 8_bit 0x1: 16_bit
10	TPCM_WIDTH	SW: RW, HW: R Selects between 8 and 16 bit samples in the outgoing stream: 0x0: 8_bit 0x1: 16_bit
9:5	RPCM_SLOT	SW: RW, HW: R Specifies the incoming slot to use in the PCM stream. The number of slots available per frame is the number of bits per frame divided by the number of bits per slot (TPCM_WIDTH and RPCM WIDTH). The number of bits per frame is common between the transmit and receive data but the slot width and slot selection is independent. 00000 = (slot0, first slot) 00001 = (slot1, second slot) ... 11111 = (slot31, 32nd slot)
4:0	TPCM_SLOT	SW: RW, HW: R Specifies the outgoing slot to use in the PCM stream. The number of slots available per frame is the number of bits per frame divided by the number of bits per slot (TPCM_WIDTH and RPCM WIDTH). The number of bits per frame is common between the transmit and receive data but the slot width and slot selection is independent. 00000 = (slot0, first slot) 00001 = (slot1, second slot) ... 11111 = (slot31, 32nd slot)

13.12.1.2 I2S Interfaces

This section contains the control registers for the 5 I2S interfaces in LPA_IF. The control register is identical for each interface although some fields are unused by hardware. The table below details how each of these registers map to the I2S interfaces and which fields are applicable:

Index(a)	I2S Interface	Notes
0	Codec Speaker	SPKR_MODE must be set to SD0 MIC_EN, MIC_MODE, MIC_MONO and LOOPBACK fields are unused for this instance.
1	Codec Mic	MIC_MODE must be set to SD0, SD1 or QUAD01 SPKR_EN, SPKR_MODE, and SPKR_MONO fields are unused for this instance. Loopback mode applies.
2	MI2S (8 Channel)	All fields supported. Loopback mode applies.
3	Secondary Speaker	SPKR_MODE must be set to SD0 MIC_EN, MIC_MODE, MIC_MONO and LOOPBACK fields are unused for this instance.
4	Secondary Mic	MIC_MODE must be set to SD0 SPKR_EN, SPKR_MODE, and SPKR_MONO fields are unused for this instance. Loopback mode applies.

NOTE The resets for the I2S interfaces come from the clock controller in LPASS. The logic in the I2S interfaces is reset synchronously so a clock must be present to get a clean startup. Each time one of the I2S interfaces is started, SW should:

1. Set the LPASS clock control such that the valid clock is selected. If the clock is external, it must be running.
2. Write to LPASS clock control to issue a reset to the I2S interface.
3. Release the reset.
4. Configure the relevant LPAIF_I2S_CTLa register.
5. Set the relevant enable bit (MIC_EN or SPKR_EN) as part of the same write or after setting the other control bits.
6. Do not change settings while relevant enable bit is set.

0x28100004+0x4*a LPAIF_I2S_CTLa, a=[0..4]

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0004

LPAIF_I2S_CTLa

Bits	Name	Description
31:16	RESERVED	

LPAIF_I2S_CTLa (cont.)

Bits	Name	Description
15	LOOPBACK	SW: RW, HW: R Loopback control bit. 0x0: DISABLE 0x1: ENABLE (only applicable to a=1=codec_mic, a=2=mi2s, & a=4=sec mic. If ENABLE is set for a=1, codec speaker is looped back to both wires of codec mic. For a=2, mi2s is looped back on itself. For a=4 sec speaker is looped backed to sec mic)
14	SPKR_EN	SW: RW, HW: R Enable for the speaker direction operation (out of the APQ). I2S interface will start transmitting serial data when enabled and trying to access a read DMA channel. Set the enable after the other control bits (speaker related, bit_width, ws_src) are configured. Disable before changing the other bits. 0x0: DISABLE 0x1: ENABLE
13:10	SPKR_MODE	SW: RW, HW: R Controls which I2S lines are used (if supported by HW) and multichannel operation 0x0: NONE 0x1: SD0 (data sent to SD0 only- stereo or mono) 0x2: SD1 (data sent to SD1 only- stereo or mono) 0x3: SD2 (data sent to SD2 only- stereo or mono) 0x4: SD3 (data sent to SD3 only- stereo or mono) 0x5: QUAD01 (SD0 & SD1 = quad channel mode) 0x6: QUAD23 (SD2 & SD3 = quad channel mode) 0x7: 6CH (SD0, SD1 & SD2 = 6 channel mode) 0x8: 8CH (SD0, SD1, SD2 & SD3 = 8 channel mode)
9	SPKR_MONO	SW: RW, HW: R In mono mode, the speaker path of I2S (out of APQ) will take each mono sample from memory and transmit it during both the right and left portions of the word select. Only applicable when a single I2S line is used in SPKR_MODE. 0x0: STEREO 0x1: MONO
8	MIC_EN	SW: RW, HW: R Enable for the microphone direction operation (into the APQ). I2S interface will start capturing data when enabled and trying to access a write DMA channel. Set the enable after the other control bits (mic related, bit_width, ws_src) are configured. Disable before changing the other bits. 0x0: DISABLE 0x1: ENABLE

LPAIF_I2S_CTLa (cont.)

Bits	Name	Description
7:4	MIC_MODE	SW: RW, HW: R Controls which I2S lines are used (if supported by HW) and multichannel operation 0x0: NONE 0x1: SD0 (data taken from SD0 only- stereo or mono) 0x2: SD1 (data taken from SD1 only- stereo or mono) 0x3: SD2 (data taken from SD2 only- stereo or mono) 0x4: SD3 (data taken from SD3 only- stereo or mono) 0x5: QUAD01 (SD0 & SD1 = quad channel mode) 0x6: QUAD23 (SD2 & SD3 = quad channel mode) 0x7: 6CH (SD0, SD1 & SD2 = 6 channel mode) 0x8: 8CH (SD0, SD1, SD2 & SD3 = 8 channel mode)
3	MIC_MONO	SW: RW, HW: R Controls whether only the left word is stored in memory (mono) or the left and right words are stored (stereo). In mono mode, the data in the right portion of WS is ignored. Only applicable when a single I2S line is used in MIC_MODE. 0x0: STEREO 0x1: MONO
2	WS_SRC	SW: RW, HW: R Controls the source of the word select, internally generated or taken from outside. Does not affect the clock. Master/Slave bit clock mode is controlled in LPASS clk_ctl. 0x0: INT (master mode) 0x1: EXT (slave mode)
1:0	BIT_WIDTH	SW: RW, HW: R Controls the bit width of the I2S samples 0x0: 16 0x1: 24 0x2: 32 0x3: RESERVED

13.12.1.3 Digital Mic Control

Registers to control the 4 digital mic pathis in LPA_IF.

NOTE Digital Mic cannot operate at the same time as the codec mic I2S interface. Enabling digital mic operation will mux the codec mic I2S interface out.

0x28100018 LPAIF_DMIC_CTL

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

Register which is common to all 4 digital mic data pathis.

This section contains the control registers for the 4 digital mic data pathis (left0, right0, left1 and right1). The control registers is identical for each path. The table below details how each of these registers map to the digital mic data pathis and which fields are applicable:

Index(a)	Digital Mic Path	Notes
0	left0	connected to data0_in pin of LPA_IF, sampled on the rising edge of the clock.
1	right0	connected to data0_in pin of LPA_IF, sampled on the falling edge of the clock
2	left1	connected to data1_in pin of LPA_IF, sampled on the rising edge of the clock.
3	right1	connected to data1_in pin of LPA_IF, sampled on the falling edge of the clock

LPAIF_DMIC_CTL

Bits	Name	Description
31:5	RESERVED	
4	EN	SW: RW, HW: R Enable Digital mic operation. NOTE: Enabling digital mic operation will mux the codec mic I2S interface out. Digital mics will start capturing data when enabled and trying to access a write DMA channel. Set the enable after the other control bits (mic related, bit_width, ws_src) are configured. Disable before changing the other bits. Enable after write DMA channel is configured and enabled. 0x0: DISABLE 0x1: ENABLE
3:1	DMIC_MODE	SW: RW, HW: R Controls which digital mics are used and multichannel operation 0x0: NONE 0x1: LEFT0 (data taken data0_in on rise edge - mono) 0x2: RIGHT0 (data taken data0_in on fall edge- mono) 0x3: LEFT1 (data taken data1_in on rise edge - mono) 0x4: RIGHT1 (data taken data1_in on fall edge - mono) 0x5: STEREO0 (LEFT0 & RIGHT0 = 2 channel mode) 0x6: STEREO1 (LEFT1 & RIGHT1 = 2 channel mode) 0x7: QUAD (4 channel mode)
0	BIT_WIDTH	SW: RW, HW: R Controls the bit width of the dmic samples 0x0: 16 0x1: 20

0x2810001C+ 0x4*a LPAIF_DMIC_VOL_CTLa, a=[0..3]

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_FF00

LPAIF_DMIC_VOL_CTLa

Bits	Name	Description
31:21	RESERVED	
20	UPDATE_STATUS	SW: R, HW: W Status of gain update. If set after writing a 1 to UPDATE_GAIN, gain has not been applied yet. Do not update gain value until this value reads back as '0'. 0x0: COMPLETE 0x1: PENDING (timeout or zero crossing)
19	UPDATE_GAIN	SW: W, HW: R Controls the loading of the gain value. The new gain value will not be applied until a 1 is written to this bit. 0x0: NO 0x1: YES (issue command to accept new gain)
18	TX_HPF_BP	SW: RW, HW: R When set(1) bypass TX DC blocking in digital mic datapath. 0x0: DC_BLOCK 0x1: BYPASS_DC_BLOCK
17	DMIC_GAIN_BP	SW: RW, HW: R When set (1), bypass DMIC gain stage post CIC. 0x0: GAIN 0x1: BYPASS_GAIN
16	MUTE_EN	SW: RW, HW: R When set(1), Mutes the output of this path. 0x0: NORMAL 0x1: MUTE
15:8	TIMEOUT_VAL	SW: RW, HW: R .Timeout value for gain application. Gain is normally applied at zero crossing. If zero crossing is not detected before timer expires, gain will be applied anyway. Timeout in Seconds = (256 * TIMEOUT_VAL + 255) / SampleRate 0xFF: DEFAULT (65535 samples = 1.37 sec @ 48 kHz)
7:0	GAIN	SW: RW, HW: R Channel Gain. 8 bit signed value representing gain in dB. Supported range = 0xAC (-84 dB) to 0x23 (35 dB) Examples: multiply by 1.0 = 0x00 = 0 dB multiply by 0.5 = 0xFA = -6 dB multiply by 2.0 = 0x06 = 6 dB 0x0: DEFAULT (=0 dB)

13.12.1.4 Vocoder Frame Reference Select

Register to select the source of the vocoder frame reference as either the modem subsystem (internal) or an external pin.

0x2810002C LPAIF_EXT_VFR

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

Select internal or external vocoder frame reference

LPAIF_EXT_VFR

Bits	Name	Description
31:1	RESERVED	
0	SEL	SW: RW, HW: R When set, the vocoder frame reference will be from an external pin. When cleared, the internal vocoder frame reference from the modem will be used (default). 0x0: INTERNAL 0x1: EXTERNAL

13.12.1.5 Spare Register

Spare register for possible ECOs.

0x28100030 LPAIF_SPARE

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

Spare register

LPAIF_SPARE

Bits	Name	Description
31:0	SPARE	

13.12.1.6 Write DMA Loopback and Mixout

This register is used to block or allow each write DMA channel from using Loopback modes or MIXOUT. The bit corresponding to a DMA channel is not set and the "AUDIO_INTF" field in the

LPA_DMA_CTLa register is set to MIXOUT, LOOPBACK1 or LOOPBACK2, the HW will force the effective value back to NONE.

0x28101000 LPAIF_WRDMA_LPBK_MIX

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_000F

Enable write DMAs to use loopback or mixout modes.

LPAIF_WRDMA_LPBK_MIX

Bits	Name	Description
31:4	RESERVED	
3	CH8	SW: RW, HW: R Control weather write dma channel 8 can be used for loopback or mixout operation. 0x0: BLOCK (loopback or mixout is not allowed) 0x1: ALLOW (dma channel can be used for loopback or mixout)
2	CH7	SW: RW, HW: R Control weather write dma channel 7 can be used for loopback or mixout operation. 0x0: BLOCK (loopback or mixout is not allowed) 0x1: ALLOW (dma channel can be used for loopback or mixout)
1	CH6	SW: RW, HW: R Control weather write dma channel 6 can be used for loopback or mixout operation. 0x0: BLOCK (loopback or mixout is not allowed) 0x1: ALLOW (dma channel can be used for loopback or mixout)
0	CH5	SW: RW, HW: R Control weather write dma channel 5 can be used for loopback or mixout operation. 0x0: BLOCK (loopback or mixout is not allowed) 0x1: ALLOW (dma channel can be used for loopback or mixout)

13.12.1.7 Debug Control

This control register is used to bring out various internal nodes to the testbus for debug.

0x28101004 LPAIF_DEBUG_CTL

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

Select signals for test modem.

LPAIF_DEBUG_CTL

Bits	Name	Description
31:5	RESERVED	
4	TESTMODE	SW: RW, HW: R Enable test mode. If not set, SEL field will have no effect and testbus will be driven to 0s. 0x0: OFF (not in test mode) 0x1: ON (in test mode)
3:0	TESTSEL	SW: RW, HW: R Select which function is brought out to the test bus for visibility. 0x0: CH0 (DMA Ch 0 - RD DMA) 0x1: CH1 (DMA Ch 1 - RD DMA) 0x2: CH2 (DMA Ch 2 - RD DMA) 0x3: CH3 (DMA Ch 3 - RD DMA) 0x4: CH4 (DMA Ch 4 - RD DMA) 0x5: CH5 (DMA Ch 5 - WR DMA) 0x6: CH6 (DMA Ch 6 - WR DMA) 0x7: CH7 (DMA Ch 7 - WR DMA) 0x8: CH8 (DMA Ch 8 - WR DMA) 0x9: MIXER 0xA: CODEC_SPKR 0xB: CODEC_MIC 0xC: MI2S 0xD: SEC_SPKR 0xE: SEC_MIC 0xF: DMIC

13.12.1.8 Mixer control

The LPA_IF block contains 1 linear mixer which can be fed by 2 Read DMA engines simultaneously. This register is used to select which read DMA channels feed the mixer.

NOTE The output of the mixer will be connected to the audio interace (AUDIO_INTF field of the LPAIF_DMA_CTLa register) of the DMA channel connected to Port 0 if both ports are configured. If only Port 1 is configured, the output of the mixer will be connected to the audio interlace of the DMA channel connected to Port 1. If the audio interface of the DMA channel assigned to Port 1 does not match the audio interface of Port 0, the output of this DMA channel assigned to Port 1 will NOT be connected to the mixer. (i.e., the AUDIO_INTF must match for the 2 DMA channels selected to feed the mixer).

If adding the mixer to an existing, running audio stream:

Setup a 2nd Read DMA channel (B)

Enable Read DMA channel (B)

NOTE Poll channel B FIFO_WORDCNT field of the LPAIF_DMA_PER_CNTa register until it reaches programmed watermark

Configure LPAIF_MIXER_CTL register:

set port 0 to channel A (existing stream)

set port1 to channel B (new stream)

0x28102000 LPAIF_MIXER_CTL

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

Enable mixer / selects which DMA channels will feed the mixer.

LPAIF_MIXER_CTL

Bits	Name	Description
31:11	RESERVED	
10	OVR_DET	SW: R, HW: W Clear mixer overflow detection bit. OVR_DET bit will be set if ever the addition of 2 inputs exceeded max neg or pos value for current bit width. 0x0: OK (no overflow has occurred since reset or last OVR_CLR) 0x1: YES (overflow occurred since reset or last OVR_CLR. If SAT_EN was set, outputs were saturated.)
9	OVR_CLR	SW: W, HW: R Clear mixer overflow detection bit. Overflow detection bit (OVR_DET above) will be set if ever the addition of 2 inputs exceeds max neg or pos value for current bit width. A single write with a ’1’ in this bit will clear the OVR_DET bit. 0x0: NO (do not clear status) 0x1: YES (clear overflow/saturation status)
8	SAT_EN	SW: RW, HW: R Enables mixer to saturate outputs if addition of inputs exceeds max neg or pos value for current bit width. 0x0: DISABLE (outputs will overflow/change sign) 0x1: ENABLE (saturate to max pos or neg value)
7:6	BIT_WIDTH	SW: RW, HW: R Determines the bit width of the samples to be mixed 0x0: 8 (only for PCM i/f) 0x1: 16 0x2: 24 (8 lsbs are pass through from port 0) 0x3: 32

LPAIF_MIXER_CTL (cont.)

Bits	Name	Description
5:3	PORT1_CH	SW: RW, HW: R Determines which (if any) read DMA channel should be connected to port 1 of the mixer 0x0: NONE (disable port 1) 0x1: CHAN0 0x2: CHAN1 0x3: CHAN2 0x4: CHAN3 0x5: CHAN4
2:0	PORT0_CH	SW: RW, HW: R Determines which (if any) read DMA channel should be connected to port 0 of the mixer. 0x0: NONE (disable port 0) 0x1: CHAN0 0x2: CHAN1 0x3: CHAN2 0x4: CHAN3 0x5: CHAN4

13.12.1.9 Audio Interrupt Registers

The audio interrupt control registers support each of the interrupt sources generating interrupts on either of 3interrupt outputs audio_irq_out0, audio_irq_out1, audio_irq_out2. Each interrupt output has its own enable, status, clear, force and raw status register. These registers support the following functionality:

- poll raw status of interrupt source even if not enabled
- force an interrupt
- clearing the interrupt source clears it if forced or actual source caused it
- enable for each interrupt source and for interrupt output
- reading the interrupt status determines which enabled interrupts are asserted
- the same value can be written back to clear these interrupts

The registers below apply to the 3 interrupt outputs. Each register type occurs 3 times, once for each interrupt output based on an index "a" as shown below. a = 0 is for audio_irq_out0, a=1 is for audio_irq_out1 and a=2 is for audio_irq_out2.

0x28103000+ 0x1000*a LPAIF_IRQ_ENa, a=[0..2]

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

Interrupt enables. The definition of the fields are as follows:

ERR_CHX = When set, enables a bus error (AHB) on channel X to cause an interrupt

OVR_CHX = When set, enables an overrun on channel X to cause an interrupt. (Applicable to write DMA channels 5-8)

UNDR_CHX= When set, enables an underrun on channel X to cause an interrupt. (Applicable to read DMA channels 0-4)

PER_CHX= When set, enables channel X reaching of the period count to cause an interrupt.

LPAIF_IRQ_ENa

Bits	Name	Description
31:28	RESERVED	
27	FRM_REF	SW: RW, HW: R When set, the detection of the rising edge of the vocoder frame reference will cause and interrupt.
26	ERR_CH8	SW: RW, HW: R
25	OVR_CH8	SW: RW, HW: R
24	PER_CH8	SW: RW, HW: R
23	ERR_CH7	SW: RW, HW: R
22	OVR_CH7	SW: RW, HW: R
21	PER_CH7	SW: RW, HW: R
20	ERR_CH6	SW: RW, HW: R
19	OVR_CH6	SW: RW, HW: R
18	PER_CH6	SW: RW, HW: R
17	ERR_CH5	SW: RW, HW: R
16	OVR_CH5	SW: RW, HW: R
15	PER_CH5	SW: RW, HW: R
14	ERR_CH4	SW: RW, HW: R
13	UNDR_CH4	SW: RW, HW: R
12	PER_CH4	SW: RW, HW: R
11	ERR_CH3	SW: RW, HW: R
10	UNDR_CH3	SW: RW, HW: R
9	PER_CH3	SW: RW, HW: R
8	ERR_CH2	SW: RW, HW: R
7	UNDR_CH2	SW: RW, HW: R
6	PER_CH2	SW: RW, HW: R

LPAIF_IRQ_ENa (cont.)

Bits	Name	Description
5	ERR_CH1	SW: RW, HW: R
4	UNDR_CH1	SW: RW, HW: R
3	PER_CH1	SW: RW, HW: R
2	ERR_CH0	SW: RW, HW: R
1	UNDR_CH0	SW: RW, HW: R
0	PER_CH0	SW: RW, HW: R

0x28103004+ 0x1000*a LPAIF_IRQ_STATa, a=[0..2]

Type: Read
Clock: CC_LPAIF_HCLK

Interrupt status . A bit set in this status register indicates the interrupt event occurred AND it is enabled in LPAIF_IRQ_ENx for this interrupt output. Typical interrupt handling operation would read this register, note the interrupt sources, and write the value read back to the LPAIF_IRQ_CLRa register to clear the interrupts.

Interrupt status. The definition of the fields are as follows:

ERR_CHX = When set, a bus error (AHB) occurred on channel X and is enabled.

OVR_CHX = When set, an overrun occurred on channel X and is enabled. (Applicable to write DMA channels 5-8)

UNDR_CHX= When set, an underrun occurred on channel X and is enabled. (Applicable to read DMA channels 0-4)

PER_CHX= When set, channel X reached the period count and is enabled.

LPAIF_IRQ_STATa

Bits	Name	Description
31:28	RESERVED	
27	FRM_REF	SW: R, HW: W When set, the rising edge of the vocoder frame reference occurred and is enabled.
26	ERR_CH8	SW: R, HW: W
25	OVR_CH8	SW: R, HW: W
24	PER_CH8	SW: R, HW: W
23	ERR_CH7	SW: R, HW: W
22	OVR_CH7	SW: R, HW: W

LPAIF_IRQ_STATa (cont.)

Bits	Name	Description
21	PER_CH7	SW: R, HW: W
20	ERR_CH6	SW: R, HW: W
19	OVR_CH6	SW: R, HW: W
18	PER_CH6	SW: R, HW: W
17	ERR_CH5	SW: R, HW: W
16	OVR_CH5	SW: R, HW: W
15	PER_CH5	SW: R, HW: W
14	ERR_CH4	SW: R, HW: W
13	UNDR_CH4	SW: R, HW: W
12	PER_CH4	SW: R, HW: W
11	ERR_CH3	SW: R, HW: W
10	UNDR_CH3	SW: R, HW: W
9	PER_CH3	SW: R, HW: W
8	ERR_CH2	SW: R, HW: W
7	UNDR_CH2	SW: R, HW: W
6	PER_CH2	SW: R, HW: W
5	ERR_CH1	SW: R, HW: W
4	UNDR_CH1	SW: R, HW: W
3	PER_CH1	SW: R, HW: W
2	ERR_CH0	SW: R, HW: W
1	UNDR_CH0	SW: R, HW: W
0	PER_CH0	SW: R, HW: W

0x28103008+ 0x1000*a LPAIF_IRQ_RAW_STATa, a=[0..2]

Type: Read
Clock: CC_LPAIF_HCLK

Raw status of the interrupt sources. A bit set in this status register indicates the interrupt event occurred whether it was enabled or not. This register can be used for polling operations or debug. The raw status is cleared when the a ’1’ is written to the corresponding bit in the LPAIF_IRQ_CLEARa register.

Interrupt raw status. The definition of the fields are as follows:

ERR_CHX = When set, a bus error (AHB) occurred on channel X regardless of enable.

OVR_CHX = When set, an overrun occurred on channel X regardless of enable. (Applicable to write DMA channels 5-8)

UNDR_CHX= When set, an underrun occurred on channel X regardless of enable. (Applicable to read DMA channels 0-4)

PER_CHX= When set, channel X reached the period count regardless of enable.

LPAIF_IRQ_RAW_STATa

Bits	Name	Description
31:28	RESERVED	
27	FRM_REF	SW: R, HW: W When set, the rising edge of the vocoder frame reference occurred regardless of enable.
26	ERR_CH8	SW: R, HW: W
25	OVR_CH8	SW: R, HW: W
24	PER_CH8	SW: R, HW: W
23	ERR_CH7	SW: R, HW: W
22	OVR_CH7	SW: R, HW: W
21	PER_CH7	SW: R, HW: W
20	ERR_CH6	SW: R, HW: W
19	OVR_CH6	SW: R, HW: W
18	PER_CH6	SW: R, HW: W
17	ERR_CH5	SW: R, HW: W
16	OVR_CH5	SW: R, HW: W
15	PER_CH5	SW: R, HW: W
14	ERR_CH4	SW: R, HW: W
13	UNDR_CH4	SW: R, HW: W
12	PER_CH4	SW: R, HW: W
11	ERR_CH3	SW: R, HW: W
10	UNDR_CH3	SW: R, HW: W
9	PER_CH3	SW: R, HW: W
8	ERR_CH2	SW: R, HW: W
7	UNDR_CH2	SW: R, HW: W
6	PER_CH2	SW: R, HW: W
5	ERR_CH1	SW: R, HW: W
4	UNDR_CH1	SW: R, HW: W

LPAIF_IRQ_RAW_STATa (cont.)

Bits	Name	Description
3	PER_CH1	SW: R, HW: W
2	ERR_CH0	SW: R, HW: W
1	UNDR_CH0	SW: R, HW: W
0	PER_CH0	SW: R, HW: W

0x2810300C+ 0x1000*a LPAIF_IRQ_CLEARa, a=[0..2]

Type: Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

Writing a 1 to a bit in this register will clear the latched interrupt event regardless of whether it is enabled for interrupt source 0 or interrupt source 1. The clear function is independent between interrupt source 0 and interrupt source 1. The corresponding bit in LPAIF_IRQ_RAW_STATa and LPAIF_IRQ_STATa will be cleared by writing a ’1’ to a bit in this register.

Interrupt clear. The definition of the fields are as follows:

ERR_CHX = Writing a 1 will clear the bus error detection for channel X.

OVR_CHX = Writing a 1 will clear the overrun detection for channel X. (Applicable to write DMA channels 5-8)

UNDR_CHX= Writing a 1 will clear the underrun detection for channel X. (Applicable to read DMA channels 0-4)

PER_CHX= Writing a 1 will clear the period count detection for channel X.

LPAIF_IRQ_CLEARa

Bits	Name	Description
31:28	RESERVED	
27	FRM_REF	SW: W, HW: R Writing a 1 will clear the vocoder frame reference detection.
26	ERR_CH8	SW: W, HW: R
25	OVR_CH8	SW: W, HW: R
24	PER_CH8	SW: W, HW: R
23	ERR_CH7	SW: W, HW: R
22	OVR_CH7	SW: W, HW: R
21	PER_CH7	SW: W, HW: R
20	ERR_CH6	SW: W, HW: R

LPAIF_IRQ_CLEARa (cont.)

Bits	Name	Description
19	OVR_CH6	SW: W, HW: R
18	PER_CH6	SW: W, HW: R
17	ERR_CH5	SW: W, HW: R
16	OVR_CH5	SW: W, HW: R
15	PER_CH5	SW: W, HW: R
14	ERR_CH4	SW: W, HW: R
13	UNDR_CH4	SW: W, HW: R
12	PER_CH4	SW: W, HW: R
11	ERR_CH3	SW: W, HW: R
10	UNDR_CH3	SW: W, HW: R
9	PER_CH3	SW: W, HW: R
8	ERR_CH2	SW: W, HW: R
7	UNDR_CH2	SW: W, HW: R
6	PER_CH2	SW: W, HW: R
5	ERR_CH1	SW: W, HW: R
4	UNDR_CH1	SW: W, HW: R
3	PER_CH1	SW: W, HW: R
2	ERR_CH0	SW: W, HW: R
1	UNDR_CH0	SW: W, HW: R
0	PER_CH0	SW: W, HW: R

0x28103010+ 0x1000*a LPAIF_IRQ_FORCEa, a=[0..2]

Type: Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

Writing a 1 to a bit in this register will force the corresponding condition as if it were generated by HW. If enabled for the corresponding interrupt output, the condition will cause an interrupt. All the registers (clear, raw_status, enable, status) operate as if the condition were caused by HW. Useful for ISR development and testing. The forced condition is cleared by writing a 1 to the corresponding bit in LPAIF_IRQ_CLRx. Writing a 0 to a bit in this register has no effect.

Interrupt force. The definition of the fields are as follows:

ERR_CHX = Writing a 1 will force a bus error condition for channel X.

OVR_CHX = Writing a 1 will force an underrun condition for channel X. (Applicable to write DMA channels 5-8)

UNDR_CHX= Writing a 1 will force an underrun condition for channel X. (Applicable to read DMA channels 0-4)

PER_CHX= Writing a 1 will force a period count expired condition for channel X.

LPAIF_IRQ_FORCEa

Bits	Name	Description
31:28	RESERVED	
27	FRM_REF	SW: W, HW: R Writing a 1 will force the vocoder frame reference detection.
26	ERR_CH8	SW: W, HW: R
25	OVR_CH8	SW: W, HW: R
24	PER_CH8	SW: W, HW: R
23	ERR_CH7	SW: W, HW: R
22	OVR_CH7	SW: W, HW: R
21	PER_CH7	SW: W, HW: R
20	ERR_CH6	SW: W, HW: R
19	OVR_CH6	SW: W, HW: R
18	PER_CH6	SW: W, HW: R
17	ERR_CH5	SW: W, HW: R
16	OVR_CH5	SW: W, HW: R
15	PER_CH5	SW: W, HW: R
14	ERR_CH4	SW: W, HW: R
13	UNDR_CH4	SW: W, HW: R
12	PER_CH4	SW: W, HW: R
11	ERR_CH3	SW: W, HW: R
10	UNDR_CH3	SW: W, HW: R
9	PER_CH3	SW: W, HW: R
8	ERR_CH2	SW: W, HW: R
7	UNDR_CH2	SW: W, HW: R
6	PER_CH2	SW: W, HW: R
5	ERR_CH1	SW: W, HW: R
4	UNDR_CH1	SW: W, HW: R
3	PER_CH1	SW: W, HW: R

LPAIF_IRQ_FORCEa (cont.)

Bits	Name	Description
2	ERR_CH0	SW: W, HW: R
1	UNDR_CH0	SW: W, HW: R
0	PER_CH0	SW: W, HW: R

13.12.1.10 Audio DMA Registers

The DMA channels can be allocated as follows:

Table 13-6 DMA Channel Allocation

Channel	Audio Direction	AHB Operation
Channel 0	Speaker	Read
Channel 1	Speaker	Read
Channel 2	Speaker	Read
Channel 3	Speaker	Read
Channel 4	Speaker	Read
Channel 5	Microphone	Write
Channel 6	Microphone	Write
Channel 7	Microphone	Write
Channel 8	Microphone	Write

Only 1 DMA channel can be connected to a speaker audio interface. If the user does program 2 Read DMA channels to the same interface, the lowest number channel will have priority. The only exception is when 2 read DMA channels feed the same interface via the mixer (LPAIF_MIXER_CTL).

Loopback mode is when samples pulled from memory by a Read DMA channel are looped back to a Write DMA Channel and written back to memory bypassing any audio HW block. Write DMA channels should be disabled before their corresponding read DMA channel in loopback mode to prevent invalid samples from being written to memory.

In loopback mode, the read channel must be programmed to a running audio interface. The audio interface will determine the rate of the transfers.

NOTE Only write DMA channels should be programmed to loopback in the AUDIO_INTF field.

DMA channels have a fixed assignment for loopback except for channel 8 which can be programmed to take read data from Channel 3 or Channel4:

Channel 0 -> Channel 5

Channel 1 -> Channel 6

Channel 2 -> Channel 7

Channel 3 -> Channel 8 or

Channel 4 -> Channel 8

The registers below apply to the 9 DMA channels. Each register type is repeated 9 times, once for each channel based on an index "a" as shown below. a = 0 is for channel 0 ... a=8 for channel 8.'

0x28106000+ 0x1000*a LPAIF_DMA_CTLa, a=[0..8]

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

Control register for DMA Channel "a"

LPAIF_DMA_CTLa

Bits	Name	Description
31:12	RESERVED	
11	BURST_EN	SW: RW, HW: R When set, DMA engine issue 4 beat AHB transactions (INCR4) instead of singles to the AHB bus. NOTE: Do NOT change BURST_EN while DMA channel is enabled. READ DMA: DMA cannot start a new burst until current FIFO depth is < 5 since FIFO is 8 deep and there must be room for all 4 beats Watermark should be programmed to >4. As soon as depth < 4 and less than the watermark, DMA will fetch 4 more words. Recommendation: If application is low latency/low speed, use shallow watermark and SINGLEs else use watermark of >4 and INCR4. WRITE DMA: DMA cannot start a burst until at least 4 samples are in the FIFO. Watermark for write DMA is the FIFO depth you do not wish to reach. If using INCR4, set watermark for 8. 0x0: SINGLE 0x1: INCR4

LPAIF_DMA_CTLa (cont.)

Bits	Name	Description
10:8	WPSCNT	SW: RW, HW: R Sets the number of 32 bit words per audio sample. This field is required to ensure data is routed to the proper audio channel. 0x0: ONE (mono, 16 bit stereo) 0x1: TWO (16 bit 4 channel, 32/24/20 bit stereo) 0x2: THREE (16 bit 6 channel) 0x3: FOUR (16 bit 8 channel, 32/24/20 bit 4 channel) 0x5: SIX (32/24/20 bit 6 channel) 0x7: EIGHT (32/24/20 bit 8 channel) 0x4: RESERVED_1 0x6: RESERVED_2
7:4	AUDIO_INTF	SW: RW, HW: R This field selects the audio interface supported by this DMA channel. Only 1 DMA channel shall be programmed to a speaker audio interface at any given time. In loopback, samples pulled from memory by Channel 0-4 are looped back to Channel 5-8 and written back to memory bypassing any audio HW block. In loopback mode, the sample rate will be dictated by the audio hw interface selected for Channel 0-4 therefore a valid, running audio interface must be selected for Channel 0-4. 0x0: NONE (DMA channel is unused) 0x1: CODEC (primary I2S interface) 0x2: PCM 0x3: SEC_I2S (secondary I2S interface) 0x4: MI2S (8 channel I2S interface) 0x5: HDMI (internal HDMI block, channels 0-4 only) 0x6: MIXOUT (mixer output, channels 5-8 only) 0x7: LOOPBACK1 (channel 0->5, 1->6,2->7,3->8 channels 5-8 only) 0x8: LOOPBACK2 (channel 4->8, valid for channel 8 only)
3:1	FIFO_WATERMRK	SW: RW, HW: R Sets a limit on the number of 32-bit words in the DMA FIFO (a watermark). The watermark for read channels (Ch 0-4) sets a limit on the number of 32 bit words the DMA will try to keep in the FIFO. The watermark for write channels (Ch 5-8) sets the FIFO depth that will generate an overrun interrupt. 0x0: 1 0x1: 2 0x2: 3 0x3: 4 0x4: 5 0x5: 6 0x6: 7 0x7: 8

LPAIF_DMA_CTLa (cont.)

Bits	Name	Description
0	ENABLE	SW: RW, HW: R Enable DMA channel. A channel which performs AHB reads (Channel 0-4) will immediately begin fetching data from the base address when enabled. A channel which performs AHB writes (Channel 5-8) will wait until a 32-bit word has been placed in the FIFO by the audio HW block and will then start storing them at the base address. Therefore, the DMA channel should be enabled before the audio HW block. 0x0: OFF 0x1: ON

0x28106004+ 0x1000*a LPAIF_DMA_BASEa, a=[0..8]

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

Base address for channel "a". Note that the base address is restricted to multiples of 16 bytes to prevent a burst access from ever crossing a 1024 byte boundary.

LPAIF_DMA_BASEa

Bits	Name	Description
31:4	BASE_ADDR	SW: RW, HW: R Base address of the circular buffer. When enabled, the DMA channel will start accesses at this address.
3:0	RESERVED	All buffers must start on a 16 byte boundary so these bits are ignored and the forced to 0 by HW.

0x28106008+ 0x1000*a LPAIF_DMA_BUFF_LENa, a=[0..8]

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0003

Buffer length for channel "a". Note that the buffer length is restricted to multiples of 16 bytes such that and integer number of INCR4 bursts will always exist in a buffer. The 2 LSBs of the length are effectively forced to 1s. e.g. Setting the LENGTH field (19:2) to 0s will result in a buffer length of 4 32 bit words.

LPAIF_DMA_BUFF_LENa

Bits	Name	Description
31:20	RESERVED_1	
19:2	LENGTH	SW: RW, HW: R Defines the size of the circular buffer in memory. Circular buffer will have BUFF_LEN+1 32-bit words. When enabled, the DMA channel will start at BASE_ADDR and roll over at BASE_ADDR+(BUFF_LEN)*4. This register directly controls the rollover value for the buffer counter (BUFF_CNT) i.e., a value of 4095 here will result in a 4096 length buffer. This field sets the 18 most significant bits of BUFF_LEN. The 2 LSBs are always 1s.
1:0	RESERVED_2	The minimum buffer length and size increment is 16 bytes so these bits are ignored and the forced to 1s by HW. These bits will read back as 1s.

0x2810600C+ 0x1000*a LPAIF_DMA_CURR_ADDRa, a=[0..8]

Type: Read
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

LPAIF_DMA_CURR_ADDRa

Bits	Name	Description
31:0	ADDR	SW: RW, HW: W Reads return next 32-bit word address to be used by the DMA channel.

0x28106010+ 0x1000*a LPAIF_DMA_PER_LENa, a=[0..8]

Type: Read/Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

LPAIF_DMA_PER_LENa

Bits	Name	Description
31:20	RESERVED	

LPAIF_DMA_PER_LENa (cont.)

Bits	Name	Description
19:0	LENGTH	SW: RW, HW: R Period Length. Defines the length of a periodic software interrupt in "32-bit words". Interrupt will be generated when PER_CHx is set in LPAIF_IRQ_ENx and the number of 32-bit words defined by PER_LEN has been written or read. This register directly controls the rollover value for the period counter (PER_CNT) ie a value of 4095 here will result in a 4096 32-bit words per period. PER_CNT rolls over at PER_LEN. (i.e., a value of 4095 here will result in an interrupt every 4096 32-bit words)

0x28106014+ 0x1000*a LPAIF_DMA_PER_CNTa, a=[0..8]

Type: Read
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

LPAIF_DMA_PER_CNTa

Bits	Name	Description
31:25	RESERVED	
24	FORMAT_ERR	SW: R, HW: W When set, the DMA engine has detected a problem with the programmed value for WPSCNT. For Read DMA channels, FORMAT_ERR indicates that the buffer length did not contain an integer number of samples. e.g. If WPSCNT is set for 8 words per sample, a format error will occur if the buffer length is set for 260 words. For Write DMA channels, FORMAT_ERR indicates that the WPSCNT field rollover did not match the cnt indicator from the audio interface (e.g. WPSCNT is set for 8 words per sample but audio interface is only using 2 words per sample). It can also indicate the buffer length did not contain a integer number of samples.

LPAIF_DMA_PER_CNTa (cont.)

Bits	Name	Description
23:20	FIFO_WORDCNT	SW: R, HW: W Returns the current number of 32bit words in the FIFO. If INCR4 bursts are not enabled via BURST_EN, the FIFO_WORDCNT ideally will return 0 for write channels and FIFO_WATERMRK for read channels. If bursts are enabled, the write DMAs will accumulate 4 write samples before attempting to push them to memory and the read DMAs will wait until the FIFO_WORDCNT is less than 5 before attempting to read more samples from memory. 0x0: 0 0x1: 1 0x2: 2 0x3: 3 0x4: 4 0x5: 5 0x6: 6 0x7: 7 0x8: 8
19:0	PER_CNT	SW: R, HW: W A counter which determines when software will receive a DMA interrupt. Interrupt will be generated when PER_CHx is set in LPAIF_IRQ_ENx and PER_CNT = PER_LEN. This counter is incremented when the DMA address is incremented but need not roll over at the same point as the address counter. PER_CNT is reset when DMA channel is disabled.

0x28106018+ 0x1000*a LPAIF_DMA_FRMa, a=[0..8]

Type: Read
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

LPAIF_DMA_FRMa

Bits	Name	Description
31:25	RESERVED	
24	FRAME_UPDATE	SW: R, HW: W When set indicates that a vocoder frame reference (VOC_FRM_REF) has been detected (since last reset or clear command)

LPAIF_DMA_FRMa (cont.)

Bits	Name	Description
23:20	FRAME_FIFO	SW: R, HW: W The number of 32-bit words in the FIFO when the VOC_FRM_REF was detected. 0x0: 0 0x1: 1 0x2: 2 0x3: 3 0x4: 4 0x5: 5 0x6: 6 0x7: 7 0x8: 8
19:0	FRAME_CNT	SW: R, HW: W PER_CNT when the vocoder frame reference was detected.

0x2810601C+ 0x1000*a LPAIF_DMA_FRMCLRa, a=[0..8]

Type: Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

LPAIF_DMA_FRMCLRa

Bits	Name	Description
31:1	RESERVED	
0	FRAME_CLR	SW: W, HW: R Writing a one to this bit clears the capture value (FRAME_CNT) and clears the FRAME_UPDATE status bit in LPAIF_DMA_FRMa.

0x28106020+ 0x1000*a LPAIF_DMA_SET_BUFF_CNTa, a=[0..8]

Type: Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

LPAIF_DMA_SET_BUFF_CNTa

Bits	Name	Description
31:20	RESERVED	
19:0	CNT	SW: W, HW: R For Test Only: Writing to this register allows the user to preload the buffer counter (BUFF_CNT) with the CNT value. See LPAIF_DMA_LENa and LPAIF_DMA_CURR_ADDRa

0x28106024+ 0x1000*a LPAIF_DMA_SET_PER_CNTa, a=[0..8]

Type: Write
Clock: CC_LPAIF_HCLK
Reset State: 0x0000_0000

LPAIF_DMA_SET_PER_CNTa

Bits	Name	Description
31:23	RESERVED	
19:0	CNT	SW: W, HW: R For Test Only: Writing to this register allows the user to preload the period count (PER_CNT) with the CNT value. See LPAIF_DMA_PER_CNTa and LPAIF_DMA_PER_LENa.

13.13 DIM D13 DQ Registers (0x1AF00000 DIM_D13_REG_BASE)

This section describes the D13 DIM DQ TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1AF00000 DIM_D13_DIM_DQ_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_DQ_TOP_CFG register configures the following:

DIM_DQ_TOP_CFG

DIM_D13_DIM_DQ_TOP_CFG

Bits	Name	Description
26	CDC_LDO_EN	Enablement of CDC LDO 1’b1 : Enabled 1’b0 : Disabled LDO and power provided from switches (default)
25	CDC_SWITCH_RC_EN	Enablement of CDC power RC (LPF) switch 1’b1 : Enabled 1’b0 : Disabled (default)
24	CDC_SWITCH_BYPASS_OFF	Enablement of CDC power bypass switch 1’b1 : Disabled 1’b0 : Enabled (default)
16	RCW_EN	Enablement of the Read Capture Window 1’b1 : Enable the RCW 1’b0 : Disabled (default)
13	DEBUG_BUS_SEL	Debug bus source select 1’b1 : from Read CDCCAL 1’b0 : from Write CDCCAL (default)
12	DEBUG_BUS_EN	1’b1 : Enables the debug bus functionality 1’b0 : Disables the debug bus and drives all ’0’s on debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_dq[5:0] 1’b1 : from cdc test outputs 1’b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1’b1) 1’b1 : with pipe extend (default) 1’b0 : without pipe extend

DIM_D13_DIM_DQ_TOP_CFG (cont.)

Bits	Name	Description
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1'b0) 1'b1 : with pipe extend (default) 1'b0 : without pipe extend
0	WR_CLK_SEL	Write clock select 1'b1 : With write CDC (default) 1'b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1AF00004 DIM_D13_DIM_DQ_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_DQ_HW_INFO register configures the following:

DIM_DQ_HW_INFO

DIM_D13_DIM_DQ_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1AF00008 DIM_D13_DIM_DQ_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_DQ_HW_VERSION register configures the following:

DIM_DQ_HW_VERSION

DIM_D13_DIM_DQ_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.

DIM_D13_DIM_DQ_HW_VERSION (cont.)

Bits	Name	Description
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1AF00010 DIM_D13_DIM_DQ_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG0 register configures the following:

DIM_DQ_PAD_CFG0

DIM_D13_DIM_DQ_PAD_CFG0

Bits	Name	Description
31	DQ_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	DQ_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	DQ_LV_MODE	Mode select for high/low voltage regime
28	DQ_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQ_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQ_PULL_B	Input pull control
21:20	DQ_NSLEW	Slew rate control bits for output path NMOS
17:16	DQ_PSLEW	Slew rate control bits for output path PMOS
13:12	DQ_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQ_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	DQ_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQ_ROUT	Impedance control bit settings for output driver
2:0	DQ_DCC	Duty cycle correction bits for output path

0x1AF00014 DIM_D13_DIM_DQ_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG1 register configures the following:

DIM_DQ_PAD_CFG1

DIM_D13_DIM_DQ_PAD_CFG1

Bits	Name	Description
31	DQS_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
30	DQS_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	DQS_LV_MODE	Mode select for high/low voltage regime
28	DQS_ODT_ENA	Unused - ODT controlled by PAD_CFG3
27:26	DQS_ODT	Unused - ODT controlled by PAD_CFG3
25:24	DQS_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	DQS_NSLEW	Slew rate control bits for output path NMOS
17:16	DQS_PSLEW	Slew rate control bits for output path PMOS
13:12	DQS_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	DQS_PRXDEL	Delay control bits to increase strength of PMOS input drive
7	DQS_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	DQS_ROUT	Impedance control bit settings for output driver
2:0	DQS_DCC	Duty cycle correction bits for output path

0x1AF00018 DIM_D13_DIM_DQ_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_DQ_PAD_CFG2 register configures the following:

DIM_DQ_PAD_CFG2

DIM_D13_DIM_DQ_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1AF00020 DIM_D13_DIM_DQ_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x1000FF11

The DIM_DQ_PAD_CFG3 register configures the following:

DIM_DQ_PAD_CFG3

DIM_D13_DIM_DQ_PAD_CFG3

Bits	Name	Description
28	DQS_DIFF_MODE	DQS output mode control 1’b1 : differential output (default) 1’b0 : single-ended output; _n output is HIZ
27	RCW_ODT_ENA1	Enable ODT for RCW pad (when hp_mode=1)
26	RCW_ODT_ENA0	Enable ODT for RCW pad (when hp_mode=0)
25:24	RCW_ODT	Impedance control for on-die termination on RCW pad
23	DQ_ODT_ENA1	Enable ODT for DQ pads (when hp_mode=1)
22	DQ_ODT_ENA0	Enable ODT for DQ pads (when hp_mode=0)
21:20	DQ_ODT	Impedance control for on-die termination on DQ pads
19	DQS_ODT_ENA1	Enable ODT for DQS pad (when hp_mode=1)
18	DQS_ODT_ENA0	Enable ODT for DQS pad (when hp_mode=0)

DIM_D13_DIM_DQ_PAD_CFG3 (cont.)

Bits	Name	Description
17:16	DQS_ODT	Impedance control for on-die termination on DQS pad
15:8	DQ_IE_OE	Enable both input receiver and output driver for all DQ pads
5	RCW_IE_OE	Enable both input receiver and output driver for RCW pad
4	DQS_IE_OE	Enable both input receiver and output driver for DQS pad
1	DM_IE	Input received enable for DM pad
0	DM_OE	Output driver enable for DM pad

0x1AF00024 DIM_D13_DIM_DQ_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_DQ_PAD_CFG4 register configures the following:

DIM_DQ_PAD_CFG4

DIM_D13_DIM_DQ_PAD_CFG4

Bits	Name	Description
31	RCW_DDR_MODE1	Mode pin for DDR (when hp_mode = 1’b1) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
30	RCW_DDR_MODE0	Mode pin for DDR (when hp_mode = 1’b0) 1’b1 :DDR2 modes (default) 1’b0 : DDR1 modes
29	RCW_LV_MODE	Mode select for high/low voltage regime
25:24	RCW_PULL_B	Input pull control
21:20	RCW_NSLEW	Slew rate control bits for output path NMOS
17:16	RCW_PSLEW	Slew rate control bits for output path PMOS
13:12	RCW_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	RCW_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	RCW_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	RCW_ROUT	Impedance control bit settings for output driver
2:0	RCW_DCC	Duty cycle correction bits for output path

0x1AF00030 DIM_D13_DIM_DQ_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG0 register configures the following:

DIM_DQ_CDC_CTLR_CFG0

DIM_D13_DIM_DQ_CDC_CTLR_CFG0

Bits	Name	Description
25	STAGGER_CAL_ENA	1'b1: Stagger calibration of write and read CDCs once after the other to reduce peak voltage drop. 1'b0: Both write and read CDCs calibrated simultaneously This bit is introduced on the x2 core, so not present on x0 and x1 versions of DIM/PHY.
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1AF00034 DIM_D13_DIM_DQ_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CTLR_CFG1 register configures the following:

DIM_DQ_CDC_CTLR_CFG1

DIM_D13_DIM_DQ_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1

0x1AF00038 DIM_D13_DIM_DQ_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG0 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG0

DIM_D13_DIM_DQ_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1AF0003C DIM_D13_DIM_DQ_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_CAL_TIMER_CFG1 register configures the following:

DIM_DQ_CDC_CAL_TIMER_CFG1

DIM_D13_DIM_DQ_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1AF00040 DIM_D13_DIM_DQ_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_REFCOUNT_CFG register configures the following:

DIM_DQ_CDC_REFCOUNT_CFG

DIM_D13_DIM_DQ_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1AF00044 DIM_D13_DIM_DQ_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_DQ_CDC_COARSE_CAL_CFG configures the following:

DIM_DQ_CDC_COARSE_CAL_CFG

DIM_D13_DIM_DQ_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1AF00048 DIM_D13_DIM_DQ_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_CDC_RSVD_CFG register configures the following:

DIM_DQ_CDC_RSVD_CFG

DIM_D13_DIM_DQ_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1AF0004C DIM_D13_DIM_DQ_RD_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_OFFSET_CFG register configures the following:

DIM_DQ_RD_CDC_OFFSET_CFG

DIM_D13_DIM_DQ_RD_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AF00050 DIM_D13_DIM_DQ_RD_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_DELAY_CFG register configures the following:

DIM_DQ_RD_CDC_DELAY_CFG

DIM_D13_DIM_DQ_RD_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AF00054 DIM_D13_DIM_DQ_RD_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_RD_CDC_SW_MODE_CFG

DIM_D13_DIM_DQ_RD_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AF00058 DIM_D13_DIM_DQ_RD_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_TEST_CFG register configures the following:

DIM_DQ_RD_CDC_TEST_CFG

DIM_D13_DIM_DQ_RD_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AF0005C DIM_D13_DIM_DQ_RD_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_RD_CDC_SW_OVRD_CFG

DIM_D13_DIM_DQ_RD_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode

DIM_D13_DIM_DQ_RD_CDC_SW_OVRD_CFG (cont.)

Bits	Name	Description
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AF00060 DIM_D13_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_SLAVE_DDA_CFG register configures the following:

DIM_DQ_RD_CDC_SLAVE_DDA_CFG

DIM_D13_DIM_DQ_RD_CDC_SLAVE_DDA_CFG

Bits	Name	Description
17	SLAV_DDA_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit-step count 1'b0: Programmed offset is added/subtracted from the unit-step count
16	SLAV_DDA_OFFSET_SIGN	1'b1: Offset is subtracted from the unit-step count. This subtraction feature is not supported on x0 and x1 PHY cores (bit RESERVED). Supported on the x2 core version. 1'b0: Offset is added to the unit-step count
15:12	SLAVE_DDA_OFFSET	unit-step offset for slave DDA.
10:0	SLAVE_DDA_DELAY	Delay required from slave DDA programmed in pico seconds.

0x1AF00070 DIM_D13_DIM_DQ_RD_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_RD_CDC_STATUS0 register configures the following:

DIM_DQ_RD_CDC_STATUS0

DIM_D13_DIM_DQ_RD_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AF00074 DIM_D13_DIM_DQ_RD_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS1 register configures the following:

DIM_DQ_RD_CDC_STATUS1

DIM_D13_DIM_DQ_RD_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AF00078 DIM_D13_DIM_DQ_RD_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_RD_CDC_STATUS2 register configures the following:

DIM_DQ_RD_CDC_STATUS2

DIM_D13_DIM_DQ_RD_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AF0007C DIM_D13_DIM_DQ_RD_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_RD_CDC_STATUS3 register configures the following:

DIM_DQ_RD_CDC_STATUS3

DIM_D13_DIM_DQ_RD_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration

DIM_D13_DIM_DQ_RD_CDC_STATUS3 (cont.)

Bits	Name	Description
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AF00080 DIM_D13_DIM_DQ_RD_CDC_STATUS4

Type: Read
Clock: HCLK
Reset State: 0x000000FF

The DIM_DQ_RD_CDC_STATUS4 register configures the following:

DIM_DQ_RD_CDC_STATUS4

DIM_D13_DIM_DQ_RD_CDC_STATUS4

Bits	Name	Description
7:4	SLAVE_DDA_DA1_TAPS	Number if unit taps applied to delay array 1 of slave DDA
3:0	SLAVE_DDA_DA0_TAPS	Number if unit taps applied to delay array 0 of slave DDA

0x1AF000AC DIM_D13_DIM_DQ_WR_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_OFFSET_CFG register configures the following:

DIM_DQ_WR_CDC_OFFSET_CFG

DIM_D13_DIM_DQ_WR_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count

DIM_D13_DIM_DQ_WR_CDC_OFFSET_CFG (cont.)

Bits	Name	Description
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1AF000B0 DIM_D13_DIM_DQ_WR_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_DELAY_CFG register configures the following:

DIM_DQ_WR_CDC_DELAY_CFG

DIM_D13_DIM_DQ_WR_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1AF000B4 DIM_D13_DIM_DQ_WR_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_MODE_CFG register configures the following:

DIM_DQ_WR_CDC_SW_MODE_CFG

DIM_D13_DIM_DQ_WR_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.

DIM_D13_DIM_DQ_WR_CDC_SW_MODE_CFG (cont.)

Bits	Name	Description
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1'b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1AF000B8 DIM_D13_DIM_DQ_WR_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_TEST_CFG register configures the following:

DIM_DQ_WR_CDC_TEST_CFG

DIM_D13_DIM_DQ_WR_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1AF000BC DIM_D13_DIM_DQ_WR_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_SW_OVRD_CFG register configures the following:

DIM_DQ_WR_CDC_SW_OVRD_CFG

DIM_D13_DIM_DQ_WR_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1AF000D0 DIM_D13_DIM_DQ_WR_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_DQ_WR_CDC_STATUS0 register configures the following:

DIM_DQ_WR_CDC_STATUS0

DIM_D13_DIM_DQ_WR_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1AF000D4 DIM_D13_DIM_DQ_WR_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS1 register configures the following:

DIM_DQ_WR_CDC_STATUS1

DIM_D13_DIM_DQ_WR_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1AF000D8 DIM_D13_DIM_DQ_WR_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_DQ_WR_CDC_STATUS2 register configures the following:

DIM_DQ_WR_CDC_STATUS2

DIM_D13_DIM_DQ_WR_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1AF000DC DIM_D13_DIM_DQ_WR_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_DQ_WR_CDC_STATUS3 register configures the following:

DIM_DQ_WR_CDC_STATUS3

DIM_D13_DIM_DQ_WR_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration

DIM_D13_DIM_DQ_WR_CDC_STATUS3 (cont.)

Bits	Name	Description
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1AF00100 DIM_D13_DIM_DQ_DQ_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQ_IOC_SLV_CFG register configures the following:

DIM_DQ_DQ_IOC_SLV_CFG

DIM_D13_DIM_DQ_DQ_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1AF00104 DIM_D13_DIM_DQ_DQ_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQ_IOC_SLV_STATUS register configures the following:

DIM_CA_CA_IOC_SLV_STATUS

DIM_D13_DIM_DQ_DQ_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

0x1AF00110 DIM_D13_DIM_DQ_DQS_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_DQ_DQS_IOC_SLV_CFG register configures the following:

DIM_DQ_DQS_IOC_SLV_CFG

DIM_D13_DIM_DQ_DQS_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	
28:24	NCNT_SW_VAL	
20:16	PCNT_SW_VAL	
15	NCNT_OFFSET_SIGN	
12:8	NCNT_SW_OFFSET	
7	PCNT_OFFSET_SIGN	
4:0	PCNT_SW_OFFSET	

0x1AF00114 DIM_D13_DIM_DQ_DQS_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_DQ_DQS_IOC_SLV_STATUS register configures the following:

DIM_DQ_DQS_IOC_SLV_STATUS

DIM_D13_DIM_DQ_DQS_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	Impedance calibration bit settings for NMOS
4:0	PAD_PCNT	Impedance calibration bit settings for PMOS

13.14 DIM C10 CA Registers (0x1B000000 DIM_C10_REG_BASE)

This section describes the C10 DIM CA TOP configuration registers. These registers allow software to configure the core and obtain status information from it.

Only 32-bit word accesses are supported. Byte and half-word accesses are not supported.

0x1B000000 DIM_C10_DIM_CA_TOP_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000031

The DIM_CA_TOP_CFG register configures the following:

DIM_CA_TOP_CFG

DIM_C10_DIM_CA_TOP_CFG

Bits	Name	Description
20	IOCAL_CTLR_SEL	Select source of PCNT/NCNT/PNCNT_VALID 1'b1: external 1'b0: internal (default)
16	SDR_MODE_EN	1'b1 : Enables SDR mode on address bus 1'b0 : Enables DDR mode on address bus (default)
13	DEBUG_BUS_SEL	Debug bus source select 1'b1: From IOCAL 1'b0: From CDCCAL (default)
12	DEBUG_BUS_EN	1'b1: Enables the debug bus functionality 1'b0: Disables the debug bus and drives all '0's on the debug bus (default)
8	CDC_TEST_EN	smt/cdc_test mux select for smt_ca[7:5] 1'b1 : from cdc test outputs 1'b0 : from smt inputs (default)
5	WR_PIPE_EXTEND1	Write pipe extend select (when hp_mode = 1'b1) 1'b1 : with pipe extend (default) 1'b0 : without pipe extend
4	WR_PIPE_EXTEND0	Write pipe extend select (when hp_mode = 1'b0) 1'b1 : with pipe extend (default) 1'b0: without pipe extend
0	WR_CLK_SEL	Write clock select 1'b1 : With write CDC (default) 1'b0 : Bypass write CDC, write clock from cdiv2 phi2 output

0x1B000004 DIM_C10_DIM_CA_HW_INFO

Type: Read
Clock: HCLK
Reset State: 0x00013007

The DIM_CA_HW_INFO register configures the following:

DIM_CA_HW_INFO

DIM_C10_DIM_CA_HW_INFO

Bits	Name	Description
31:20	RESERVED	Read all zeros
19:16	CORE_ID	Core ID like LPDDR2, PCDDR3, etc.
15:12	MAJOR_REV	Major code revision
11:8	BRANCH_REV	Branch code revision
7:0	MINOR_REV	Minor code revision

0x1B000008 DIM_C10_DIM_CA_HW_VERSION

Type: Read
Clock: HCLK
Reset State: 0x10040001

The DIM_CA_HW_VERSION register configures the following:

DIM_CA_HW_VERSION

DIM_C10_DIM_CA_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Major version indicates different interface version, not backward compatible if changed.
27:16	MINOR	Minor version indicates expanded functionality, backward compatible.
15:0	STEP	Step indicates HW change which is not intented to impact SW compatibility.

0x1B000010 DIM_C10_DIM_CA_PAD_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0xE0222240

The DIM_CA_PAD_CFG0 register configures the following:

DIM_CA_PAD_CFG0

DIM_C10_DIM_CA_PAD_CFG0

Bits	Name	Description
31	CA_DDR_MODE1	Mode pin for DDR (when hp_mode = 1'b1) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
30	CA_DDR_MODE0	Mode pin for DDR (when hp_mode = 1'b0) 1'b1 :DDR2 modes (default) 1'b0 : DDR1 modes
29	CA_LV_MODE	Mode pin for high/low voltage regime
28	CA_ODT_ENA	Enable bit for on-die termination
27:26	CA_ODT	Impedance control bit settings for on-die termination
25:24	CA_PULL	Input pull control 2'b00 : no pull (default) 2'b01 : pull down 2'b10 : keeper 2'b11 : pull up
21:20	CA_NSLEW	Slew rate control bits for output path NMOS
17:16	CA_PSLEW	Slew rate control bits for output path PMOS
13:12	CA_NRXDEL	Delay control bits to increase strength of NMOS input drive
9:8	CA_PRXDEL	Delay control bits to increase strength of PMOS input driver
7	CA_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	CA_ROUT	Impedance control bit settings for output driver
2:0	CA_DCC	Duty cycle correction bits for output path

0x1B000014 DIM_C10_DIM_CA_PAD_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0xE0220440

The DIM_CA_PAD_CFG1 register configures the following:

DIM_CA_PAD_CFG1

DIM_C10_DIM_CA_PAD_CFG1

Bits	Name	Description
31	CK_DDR_MODE1	Mode select for DDR (when hp_mode = 1'b1) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
30	CK_DDR_MODE0	Mode select for DDR (when hp_mode = 1'b0) 1'b1 : DDR2 modes (default) 1'b0 : DDR1 modes
29	CK_LV_MODE	Mode select for high/low voltage regime
28	CK_CMFB_ENA	Common mode feedback loop enable
27	CK_ODT_ENA1	Enable bit for on-die termination (when hp_mode = 1'b1)
26	CK_ODT_ENA	Enable bit for on-die termination (when hp_mode = 1'b0) Bit field name missing '0' for APQ8064 SW compatibility.
25:24	CK_ODT	Impedance control bit settings for on-die termination
21:20	CK_NSLEW	Slew rate control bits for output path NMOS
17:16	CK_PSLEW	Slew rate control bits for output path PMOS
13	CK_CUR_MODE1	Current/Voltage mode selection (when hp_mode = 1'b1) 1'b1 : Current mode 1'b0 : Voltage mode (default)
12	CK_CUR_MODE0	Current/Voltage mode selection (when hp_mode = 1'b0) 1'b1 : Current mode 1'b0 : Voltage mode (default)
10:8	CK_I_DRV	Control bit settings for bias current
7	CK_VM_SHIFT_ENA	VM (voltage at output of on-die termination) shift enable bit
6:4	CK_ROUT	Impedance control bit settings for output driver
2:0	CK_DCC	Duty cycle correction bits for output path

0x1B000018 DIM_C10_DIM_CA_PAD_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x1000000A

The DIM_CA_PAD_CFG2 register configures the following:

DIM_CA_PAD_CFG2

DIM_C10_DIM_CA_PAD_CFG2

Bits	Name	Description
29	VREF_LDO_ENA	Enable VREF pad LDO Must be 0 for x2 core as there is no internal LDO
28	VREF_PASSGATE_ENA	Enable pass gate from padsig to vref_int pin (default 1)
27:24	VREF_SP_OUT	Unused
21:18	VREF_SP_IN	Unused
17	VREF_BYPASS_ENA	Enable bypass gate from resistive divider to vref_int pin
16	VREF_RDIV_ENA	Enable resistive divider for VREF voltage control
13:8	VREF_PULLDN_SPEED_CNTL	Unused
5:0	VREF_LEVEL_CNTL	Control over the VREF voltage level through resistive divider

0x1B00001C DIM_C10_DIM_CA_PAD_CFG3

Type: Read/Write
Clock: HCLK
Reset State: 0x00300000

The DIM_CA_PAD_CFG3 register configures the following:

DIM_CA_PAD_CFG3

DIM_C10_DIM_CA_PAD_CFG3

Bits	Name	Description
31:30	CS_N_IE	
29:28	CS_N_OE	
25	CK_IE	
24	CK_OE	
23:22	CKE_IE	
21:20	CKE_OE	
19:10	CA_IE	
9:0	CA_OE	

0x1B000020 DIM_C10_DIM_CA_PAD_CFG4

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_PAD_CFG4 register configures the following:

DIM_CA_PAD_CFG4

DIM_C10_DIM_CA_PAD_CFG4

Bits	Name	Description
31:30	CS_N_OE_DYN_ENA	Enable dynamic control of CS_N OE 1'b1: Dynamic control enabled and CS_N_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CS_N OE gated by CA_PAD_CFG3 bits Note: This register should not be set in external loopback mode since it will change the IE contol source.
29:28	CS_N_OE_DYN	Dynamic OE control for each of the CS_N outputs, OR-ed with common controller OE.
25	RESERVED_1	
24	RESERVED_2	
23:22	CKE_OE_DYN_ENA	Enable dynamic control of CKE OE 1'b1: Dynamic control enabled and CKE_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CKE OE gated by CA_PAD_CFG3 bits
21:20	CKE_OE_DYN	Dynamic OE control for each of the CA outputs, OR-ed with common controller OE.
19:10	CA_OE_DYN_ENA	Enable dynamic control of CA OE 1'b1: Dynamic control enabled and CA_OE_DYN[n] bits are OR-ed with common OE from controller 1'b0: (default) Dynamic control disabled, CA OE gated by CA_PAD_CFG3 bits
9:0	CA_OE_DYN	Dynamic OE control for each of the CA outputs, OR-ed with common controller OE.

0x1B000030 DIM_C10_DIM_CA_CDC_CTLR_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CTLR_CFG0 register configures the following:

DIM_CA_CDC_CTLR_CFG0

DIM_C10_DIM_CA_CDC_CTLR_CFG0

Bits	Name	Description
24	TRACKING_CAL_ENA	1'b1: Relationship between subunits and oscillator count is learnt and used for tracking calibration. 1'b0: Periodic calibration triggers cause full recalibration
23:20	OSC_COUNT_ERR_TOLERANCE	Magnitude of the difference between oscillator count and target count when the algorithm assumes convergence and stops further search.
19	TRACK_CALIB_MODE	1'b0: Tracking calibration uses previous Target_count value. 1'b1 Accurate mode: Target_count is recomputed at the start of tracking calibration
18	FULL_DELAY	1'b0: unitstep and subunit caps are from calibration or SW settings 1'b1: All unit step and subunit caps are selected for the delay arrays.
17	HW_AUTOCAL_ENA	1'b1: Enables periodic auto calibration 1'b0: Periodic calibration is disabled
16	SW_TRIG_FULL_CALIB	A low to high transition on this register bit triggers the CDC calibration state machine to initiate full calibration of the standby delay array. Also resets tracking mode for the delay arrays.
13:12	OSC_PRE_DIV	The factor by which the raw oscillator frequency is divided before being given to the counting logic. 2'b00 Divide by 1 2'b01 Divide by 2 2'b10 Divide by 4 2'b11 Divide by 8
10:0	TMUX_CHAR	Cchar is a characterized constant equal to the ratio of output mux offset delay to average unit step delay. This register is programmed by multiplying the constant with 1024 and rounding to the nearest integer. E.g. if Cchar = 0.67, RO(0.67 * 1024) = 686, hence program TMUX_CHAR = 11'h2AE

0x1B000034 DIM_C10_DIM_CA_CDC_CTLR_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CTLR_CFG1 register configures the following:

DIM_CA_CDC_CTLR_CFG1

DIM_C10_DIM_CA_CDC_CTLR_CFG1

Bits	Name	Description
26:24	OSC_COUNT_DELAY	Number of oscillator cycles from the end of reference gate signal to assertion of oscillation counter done. Legal values are from 0 to 4.
22:20	STANDBY_DELAY	This is the number of reference clock cycles from when a newly calibrated delay array is made active to when the current active delay array is put into standby mode. 3'b0: Disables the counter. Hardware waits for explicit acknowledgement of delay array switch from CDC. Others: Explicit acknowledgement mode is disabled and the counter is used
18:16	DEL_MODE_DELAY	Number of reference clock cycles between putting a newly calibrated delay array in delay mode to selecting it as the active delay array. The minimum allowed value is 1
14:12	OSC_MODE_DELAY	Number of reference clock cycles between putting a delay array in oscillator mode to starting the oscillation counter. This delay is allowed for the oscillations to stabilize through the delay array. The minimum allowed value is 1
10:8	DECODER_DELAY	Number of reference clock cycles allowed for unitstep and subunit counts to be encoded into the unit and finecap select lines on the DDA. The minimum allowed value is 1.
6:4	DIVIDER_DELAY	Number of reference clock cycles allowed for arithmetic division operations. The minimum allowed value is 1
2:0	MULTIPLIER_DELAY	Number of reference clock cycles allowed for arithmetic multiplication operations. The minimum allowed value is 1

0x1B000038 DIM_C10_DIM_CA_CDC_CAL_TIMER_CFG0

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CAL_TIMER_CFG0 register configures the following:

DIM_CA_CDC_CAL_TIMER_CFG0

DIM_C10_DIM_CA_CDC_CAL_TIMER_CFG0

Bits	Name	Description
24	INVALID_TIMER_ENA	1'b1 : Enable the timer counting number of missed calibration intervals after which the CDC is invalid. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.

DIM_C10_DIM_CA_CDC_CAL_TIMER_CFG0 (cont.)

Bits	Name	Description
23:20	INVALID_TIMER_VAL	Number of missed calibration intervals after which CDC invalid state is asserted.
16	TIMER_ENA	1'b1 : Enables 32 KHz sleep clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
15:0	TIMER_VAL	Count value for periodic autocalibration interval based on sleep clock.

0x1B00003C DIM_C10_DIM_CA_CDC_CAL_TIMER_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_CAL_TIMER_CFG1 register configures the following:

DIM_CA_CDC_CAL_TIMER_CFG1

DIM_C10_DIM_CA_CDC_CAL_TIMER_CFG1

Bits	Name	Description
12	FF_TIMER_ENA	1'b1 : Enables reference clock based periodic autocalibration timer. 1'b0 : Timer disabled A low to high transition on this register bit loads the timer with programmed value below.
9:0	FF_TIMER_VAL	Count value for periodic autocalibration interval based on reference clock.

0x1B000040 DIM_C10_DIM_CA_CDC_REFCOUNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_REFCOUNT_CFG register configures the following:

DIM_CA_CDC_REFCOUNT_CFG

DIM_C10_DIM_CA_CDC_REFCOUNT_CFG

Bits	Name	Description
31:16	TREF	Reference clock period programmed in pico seconds.
13:8	CCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during coarse calibration. Maximum supported value is 59.
5:0	FCAL_REF_COUNT	Number of reference clock cycles used for oscillation counts during fine calibration. Maximum supported value is 59

0x1B000044 DIM_C10_DIM_CA_CDC_COARSE_CAL_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The register DIM_CA_CDC_COARSE_CAL_CFG configures the following:

DIM_CA_CDC_COARSE_CAL_CFG

DIM_C10_DIM_CA_CDC_COARSE_CAL_CFG

Bits	Name	Description
12:8	CCAL_SUBUNIT_CAPS	Subunit count needed for an effective unit step count of 32 during coarse calibration. This value is also used by software oscillator mode.
5:0	CCAL_UNITSTEPS	unitstep count needed for an effective unit step count of 32 during coarse calibration.

0x1B000048 DIM_C10_DIM_CA_CDC_RSVD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_RSVD_CFG register configures the following:

DIM_CA_CDC_RSVD_CFG

DIM_C10_DIM_CA_CDC_RSVD_CFG

Bits	Name	Description
15:0	TEMP_FIELD	Reserved register

0x1B00004C DIM_C10_DIM_CA_CDC_OFFSET_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_OFFSET_CFG register configures the following:

DIM_CA_CDC_OFFSET_CFG

DIM_C10_DIM_CA_CDC_OFFSET_CFG

Bits	Name	Description
20	SUBUNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as subunit count 1'b0: Programmed offset is added/subtracted from the subunit count
19	SUBUNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the subunit count 1'b0: Offset is added to the subunit count
16:12	SUBUNIT_OFFSET	Software subunit offset
8	UNIT_OFFSET_MODE	1'b1: The programmed offset is directly loaded as unit step count 1'b0: Programmed offset is added/subtracted from the unit step count
7	UNIT_OFFSET_SIGN	1'b1: Offset is subtracted from the unitstep count 1'b0: Offset is added to the unitstep count
5:0	UNIT_OFFSET	Software unitstep offset

0x1B000050 DIM_C10_DIM_CA_CDC_DELAY_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_DELAY_CFG register configures the following:

DIM_CA_CDC_DELAY_CFG

DIM_C10_DIM_CA_CDC_DELAY_CFG

Bits	Name	Description
28	TARGET_COUNT_ENA	1'b1: Enable software specified Target_count for calibration instead of value calculated by hardware. 1'b0: Hardware computed Target_count used.
27:16	TARGET_COUNT	Software specified Target_count to which the state machine calibrates

DIM_C10_DIM_CA_CDC_DELAY_CFG (cont.)

Bits	Name	Description
11:0	DELAY_VAL	Delay required from CDC programmed in pico seconds. This value has to be greater than the minimum delay supported by DDA Tmin.

0x1B000054 DIM_C10_DIM_CA_CDC_SW_MODE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_SW_MODE_CFG register configures the following:

DIM_CA_CDC_SW_MODE_CFG

DIM_C10_DIM_CA_CDC_SW_MODE_CFG

Bits	Name	Description
3	SW_DEL_MODE	A low to high transition on this register bit puts the delay array selected by SW_DA_SEL into delay mode and connects it to the DDA output. This register has to remain set for the duration of SW controlled delay mode.
2	SW_OSC_MODE	Reserved register.
1	SW_DA_SEL	Selects the delay array inside DDA during software delay or oscillator mode.
0	SW_LOAD	1’b1: Enable loading of the software offsets from the offset configuration register. This register has to remain set for the duration of SW mode operation.

0x1B000058 DIM_C10_DIM_CA_CDC_TEST_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_TEST_CFG register configures the following:

DIM_CA_CDC_TEST_CFG

DIM_C10_DIM_CA_CDC_TEST_CFG

Bits	Name	Description
3	CDC_SEL_DDA_TEST	1'b1: Test outputs from the main DDA are connected to the CDC test ports 1'b0: Test outputs from the slave DDA are connected to the CDC test ports
2	CDC_OSC_TEST_EN	1'b1: A divided version of the oscillator clock is made available on CDC test port OSC_TEST. 1'b0 : Raw oscillator clock frequency is made available on CDC test port OSC_TEST if CDC_TEST_EN register is set.
1	CDC_TEST_EN	1'b1: Enables CDC test outputs. Oscillator clock on OSC_TEST if CDC_OSC_TEST_EN = 0, CDC input on CDC_TEST_OUT1, CDC output on CDC_TEST_OUT2 if CDC_OUT_ONTEST2 = 1 1'b0 : CDC test ports disabled
0	CDC_OUT_ONTEST2	1'b1: CDC output is made available on CDC_TEST_OUT2 if CDC_TEST_EN = 1 1'b0: CDC input is available on CDC_TEST_OUT2 if CDC_TEST_EN = 1

0x1B00005C DIM_C10_DIM_CA_CDC_SW_OVRD_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_TEST_CFG register configures the following:

DIM_CA_CDC_SW_OVRD_CFG

DIM_C10_DIM_CA_CDC_SW_OVRD_CFG

Bits	Name	Description
16	SW_REF_GATE	Write 1'b1 to start the reference window. Write 1'b0 to end the reference window. Number of reference cycle in the window will be reported in SW_REF_GATE_COUNT in CDC_STATUS0
11	SW_OVRD_DA1_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in oscillator-mode
10	SW_OVRD_DA1_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 1 in delay-mode
9	SW_OVRD_DA0_OSC_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in oscillator-mode
8	SW_OVRD_DA0_IN_EN	In software override mode, 1'b1 written to this bit puts delay array 0 in delay-mode

DIM_C10_DIM_CA_CDC_SW_OVRD_CFG (cont.)

Bits	Name	Description
3	SW_OVRD_CDC_COUNTER_RST	1'b1 written to this bit resets the oscillation counter. Follow this with 1'b0 before setting reference gate.
2	SW_OVRD_LOAD_DA_SEL	In software override mode, this bit select the delay array to which unit and subunit offset values from CDC_OFFSET_CFG register will be loaded.
1	SW_OVRD_ACTV_DA_SEL	In software override mode, this register selects the delay array connected to the CDC output
0	SW_OVRD_ENA	1'b1 written to this bit puts the CDC interface in software override mode where the below register bits control the CDC. 1'b0: CDC is under hardware control

0x1B000070 DIM_C10_DIM_CA_CDC_STATUS0

Type: Read
Clock: HCLK
Reset State: 0x0000000C

The DIM_CA_CDC_STATUS0 register configures the following:

DIM_CA_CDC_STATUS0

DIM_C10_DIM_CA_CDC_STATUS0

Bits	Name	Description
26:24	CDC_ERROR_CODE	Error code for internal errors: 3'b000: No error 3'b001: Programmed delay less than Tmux 3'b010: Programmed delay less than Tmin 3'b011: Unit-step overflow: Overflow during fine calibration. Desired delay cannot be realized even when all unit-steps are selected. 3'b100: Unit-step underflow 3'b101: Unit-step overflow: Overflow during coarse calibration. Estimated unit steps needed to realize the desired delay are greater than the total number of unit-steps in design. Note: The CDC_ERROR_CODE is not a sticky register and is updated after each CDC calibration.
23:16	SW_REF_GATE_COUNT	Number of reference clock cycles in the software generated oscillation gate window during SW override mode
15:4	OSC_COUNT	Current value of oscillator count

DIM_C10_DIM_CA_CDC_STATUS0 (cont.)

Bits	Name	Description
3	CURR_SEL_DA	This bit indicates the current active delay array connected to the output. 1'b0 : DA0 is selected 1'b1 : DA1 is selected
2	CTLR_SM_IDLE	1'b1 Indicates that the calibration state machine is idle 1'b0 indicates calibration state machine is busy
1	OSC_DONE	This status register is set after oscillations count is finished by CDC. It gets reset when a new oscillator count is started.
0	CALIBRATION_DONE	1'b1 indicates that calibration is done and CURR_SUBUNIT_STEPS, CURR_UNIT_STEPS status registers are valid.

0x1B000074 DIM_C10_DIM_CA_CDC_STATUS1

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_STATUS1 register configures the following:

DIM_CA_CDC_STATUS1

DIM_C10_DIM_CA_CDC_STATUS1

Bits	Name	Description
27:16	CURR_DELAY_VALUE	HW Computed value of current delay after calibration by the state machine. This register is valid of CALIBRATION_DONE status bit is set.
11:0	CURR_TMUX_DELAY	Current value of output mux offset delay computed by HW.

0x1B000078 DIM_C10_DIM_CA_CDC_STATUS2

Type: Read
Clock: HCLK
Reset State: 0x10331033

The DIM_CA_CDC_STATUS2 register configures the following:

DIM_CA_CDC_STATUS2

DIM_C10_DIM_CA_CDC_STATUS2

Bits	Name	Description
28:24	DA1_SUBUNITS	Current value of subunit cap settings applied to delay array 1
21:16	DA1_UNITSTEPS	Current value of unit steps applied to delay array 1
12:8	DA0_SUBUNITS	Current value of subunit cap settings applied to delay array 0
5:0	DA0_UNITSTEPS	Current value of unit steps applied to delay array 0

0x1B00007C DIM_C10_DIM_CA_CDC_STATUS3

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_CDC_STATUS3 register configures the following:

DIM_CA_CDC_STATUS3

DIM_C10_DIM_CA_CDC_STATUS3

Bits	Name	Description
31:24	NUM_OF_OSC_ITER	Number of oscillator iterations before convergence was achieved during tracking
23:12	COUNT_ERROR	Difference between target and actual oscillator counts at the start of tracking calibration
11:0	CURR_TARGET_COUNT	HW computed value of current Target_count used by the calibration state machine.

0x1B0000E0 DIM_C10_DIM_CA_IOC_CTLR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_CFG register configures the following:

DIM_CA_IOC_CTLR_CFG

DIM_C10_DIM_CA_IOC_CTLR_CFG

Bits	Name	Description
31	CAL_NOW	SW : RW Set this bit to 1’b1 will cause the IO calibration starts immediately. This bit has to be cleared after the calibration has been done. 0x0: no-op 0x1: start IOCal immediately
30	IO_CAL_AUTO	Periodic auto calibration mode. Writing a ’1’ to this bit will trigger periodic auto calibration with the period specified in IOC_CTLR_TIMER_CFG register. If ’0’, it disables the timer based on sleep clock. Note that this does not impact the timer based on fixed frequency clock (ffclk).
29	IO_CAL_FF_TIMER_EN	Fixed Frequency Timer mode. Writing a ’1’ to this bit will set the timer running off tcxo clock. If ’0’, it disables the timer based on fixed frequency clock.
28	IO_CAL_BANDGAP_DYN_CTRL	Enable dynamic control of the bandgap element: This low-power feature is only available on x2 core. Bit reserved for x0/x1 cores. 1’b1: Enabled - bandgap element turned on only during IO calibration or when current mode is enabled. 1’b0: Disabled (default) - bandgap element turned on/off statically based on BANDHGAP_ENA0/1 bits.
25	SW_FFCLK_ON	Writing a ’1’ to this field will turn on the fixed frequency (xo) clock on signal
24	LV_MODE	SW : RW Enable/Disable low-voltage mode (MIF2 pad only) 0x0: 1.8V 0x1: non-1.8V
20:16	MARGIN_LOAD	SW : RW If the difference between the current IOCal result is greater than the last result by the number specified here, then the IOCal controller will request value update to DDR controller. 0x0: always update
13:12	IMP_SEL	SW : RW Select bits to choose which impedance to calibrate to
10	PN_SEL_CA	SW : RW Enables loading of HW calibrated values for ca pads. Writing a ’1’ to this bit would let the IOCAL to request traffic stall on ca pads when it is time to update the pads with the new value.
9	PN_SEL_DATA	SW : RW Enables loading of HW calibrated values for dq/dqs pads. Writing a ’1’ to this bit would let the IOCAL to request traffic stall on data pads when it is time to update the pads with the new value.

DIM_C10_DIM_CA_IOC_CTLR_CFG (cont.)

Bits	Name	Description
8	CAL_USE_LAST	SW : RW Select the initial value to start IO calibration 0x0: start from a fixed values specified in IOC_CTLR_PNCNT_CFG (default) 0x1: start from previous IOCal PNCNT results
6:4	SAMPLE_POINT	SW : RW Specify number of samples per measure point 0x0: 1 0x1: 3 0x2: 5 0x3: 7 0x4: 9 0x5: 11 0x6: 13 0x7: 15
3	DDR_MODE1	
2	DDR_MODE0	
1	BANDGAP_ENA1	SW : RW Pin to enable bandgap independent of diff_ctl 0x0: disable 0x1: enable
0	BANDGAP_ENA0	SW : RW Pin to enable bandgap independent of diff_ctl 0x0: disable 0x1: enable

0x1B0000E4 DIM_C10_DIM_CA_IOC_CTLR_PNCNT_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_CFG register configures the following:

This register contains the initial value for the next calibration to start from. Softwave can set the hardware to either start calibration from a fixed value or from previous results. If software chooses to use fixed value by setting CAN_USE_LAST in register IOC_CTLR_CFG to be 0, then the values in this register will be used.

DIM_CA_IOC_CTLR_CFG

DIM_C10_DIM_CA_IOC_CTLR_PNCNT_CFG

Bits	Name	Description
12:8	NCNT_INIT_CSR	SW : RW Starting PCNT value used in calibration. Only take effect when CAN_USE_LAST is asserted
4:0	PCNT_INIT_CSR	SW : RW Starting NCNT value used in calibration. Only take effect when CAN_USE_LAST is asserted

0x1B0000E8 DIM_C10_DIM_CA_IOC_CTLR_TIMER_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_TIMER_CFG register configures the following:

DIM_CA_IOC_CTLR_TIMER_CFG

DIM_C10_DIM_CA_IOC_CTLR_TIMER_CFG

Bits	Name	Description
31:16	TIMER_PERIOD	SW : RW Recalibration Period. The period is measured in timer clock cycles. Typically it's a 32kHz clock. The minimum period that can be programmed is 3. 0,1,2: Invalid values
15:0	FF_TIMER_PERIOD	SW : RW Recalibration Period for the timer running of xo clock. 0x0: Invalid

0x1B0000EC DIM_C10_DIM_CA_IOC_CTLR_TIMER_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_TIMER_STATUS register configures the following:

DIM_CA_IOC_CTLR_TIMER_STATUS

DIM_C10_DIM_CA_IOC_CTLR_TIMER_STATUS

Bits	Name	Description
15:0	TIMER_STATUS	Current Auto Calibration Timer value. As this register is written in sleep clock domain and read in xo clock domain and no hardware synchronization in place, It is required by the software to read this register 4 times to get the correct value.

0x1B0000F0 DIM_C10_DIM_CA_IOC_CTLR_CHAR_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

The DIM_CA_IOC_CTLR_ CHAR_CFGregister configures the following:

This register is used by hardware verification software only. It provides a mechanism to allow software to bypass the internal calibration state machine and directly access the IOCAL pad inputs.

IDIM_CA_IOC_CTLR_CHAR_CFG

DIM_C10_DIM_CA_IOC_CTLR_CHAR_CFG

Bits	Name	Description
16	SM_BYP_ENA	SW : RW Characterization Bypass Path Enable 0x0: Non-bypass: State Machine Controls IOCAL pad inputs (default) 0x1: bypass: This register controls IOCal pad inputs
15	SM_BYP_N_ENA	SW : RW IO CAL Characterization n_enable: 0x0: de-asserted (default) 0x1: asserted
12:8	SM_BYP_NCNT	SW : RW IO CAL Characterization ncnt value. 0x0: count 0 (default)
7	SM_BYP_P_ENA	SW : RW IO CAL Characterization p_enable: 0x0: de-asserted (default) 0x1: asserted
4:0	SM_BYP_PCNT	SW : RW IO CAL Characterization pcnt value. 0x0: count 0 (default)

0x1B0000F4 DIM_C10_DIM_CA_IOC_CTLR_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00011010

The DIM_CA_IOC_CTLR_STATUS register configures the following:

DIM_CA_IOC_CTLR_STATUS

DIM_C10_DIM_CA_IOC_CTLR_STATUS

Bits	Name	Description
31	INIT_IOCAL_DONE	SW : R The very first IO Calibration is finished This bit is stiky. once it becomes 1'b1 until software writes it back to 0. 0x0: Init-cal never done 0x1: Init-cal finished
18	IOCAL_DONE_D	SW : R IO Calibration is finished 0x0: in progress 0x1: finished
17	IOCAL_BUSY	SW : R Status of calibration State machine 0x0: idle 0x1: busy
16	SYNC_COMP	SW : R comp value from IOCal pad
12:8	NCNT_HOLD	SW : R Current NCNT value used
4:0	PCNT_HOLD	SW : R Current PCNT value used

0x1B000100 DIM_C10_DIM_CA_CA_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_CA_CA_IOC_SLV_CFG register configures the following:

This register specifies the overriding pcnt and ncnt values. Overriding mode is controlled by PNCNT_HW_LOAD_EN bit in this register.

DIM_CA_CA_IOC_SLV_CFG

DIM_C10_DIM_CA_CA_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	Select PCNT/NCNT Source for pads. This is the mux control that chooses either auto calibrated value or the software override value. 0x0: override (default) 0x1: auto cal
28:24	NCNT_SW_VAL	SW : RW NCNT Override Value for the pads
20:16	PCNT_SW_VAL	SW : RW PCNT Override Value for the pads
15	NCNT_OFFSET_SIGN	controls if the NOFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
12:8	NCNT_SW_OFFSET	SW : RW The offiset applied on top of NCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)
7	PCNT_OFFSET_SIGN	controls if the POFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
4:0	PCNT_SW_OFFSET	SW : RW The offiset applied on top of PCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)

0x1B000104 DIM_C10_DIM_CA_CA_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_CA_CA_IOC_SLV_STATUS register configures the following:

DIM_CA_CA_IOC_SLV_STATUS

DIM_C10_DIM_CA_CA_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	The final NCNT value that is applied to the pads.
4:0	PAD_PCNT	The final PCNT value that is applied to the pads.

0x1B000110 DIM_C10_DIM_CA_CK_IOC_SLV_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x10100000

The DIM_CA_CK_IOC_SLV_CFG register configures the following:

DIM_CA_CK_IOC_SLV_CFG

DIM_C10_DIM_CA_CK_IOC_SLV_CFG

Bits	Name	Description
31	PNCNT_HW_LOAD_EN	Select PCNT/NCNT Source for pads. This is the mux control that chooses either auto calibrated value or the software override value. 0x0: override (default) 0x1: auto cal
28:24	NCNT_SW_VAL	SW : RW NCNT Override Value for the pads
20:16	PCNT_SW_VAL	SW : RW PCNT Override Value for the pads
15	NCNT_OFFSET_SIGN	controls if the NOFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
12:8	NCNT_SW_OFFSET	SW : RW The offiset applied on top of NCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)
7	PCNT_OFFSET_SIGN	controls if the POFFSET is added for subtracted on top of calibration result 0x0: Add 0x1: Subtract
4:0	PCNT_SW_OFFSET	SW : RW The offiset applied on top of PCNT value from calibration before it gets sent to IO pads 0x0: count 0 (default)

0x1B000114 DIM_C10_DIM_CA_CK_IOC_SLV_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00001010

The DIM_CA_CK_IOC_SLV_STATUS register configures the following:

DIM_CA_CK_IOC_SLV_STATUS

DIM_C10_DIM_CA_CK_IOC_SLV_STATUS

Bits	Name	Description
12:8	PAD_NCNT	The final NCNT value that is applied to the pads.
4:0	PAD_PCNT	The final PCNT value that is applied to the pads.

14 Multi-Media Subsystem Registers

14.1 Overview

Table 14-1 Multi_Media_Sub_System Bases

Base Name	Parent	Address
MMSS_AHB_NS	MMSS_CC_BASE	0x04000000
A_MFC_SW_RESET	MFC_BASE	0x04400000
A_MFCV1080P_MGEN_VERSION	MFC_BASE	0x04400000
A_MFCV1080P_ENH_DMI_CFG	MFC_BASE	0x04400000
A_JPEG_HW_VERSION	GEMINI_BASE	0x04600000
MIPI_DSI_1_DSI1_CTRL	MIPI_DSI_1_BASE	0x04700000
MIPI_DSI_2_DSI2_CTRL	MIPI_DSI_2_BASE	0x05800000
HDMI_CTRL	HDMI_TX_BASE	0x04A00000
IMEM_MMSS_IMEM_CONFIG	IMEM_MMSS_BASE	0x04B00000
IMEM_MMSS_MPU_PRTn_RACR	IMEM_MMSS_BASE	0x04B00000
ROTATOR_INTR_ENABLE	ROTATOR_BASE	0x04E00000
TV_ENC_CTL	TV_ENC_BASE	0x04F00000
JPEG_CTRL_COMMON	JPEGD_BASE	0x05000000
MDP_HW_VERSION	MDP_BASE	0x05100000
VPE_SYNC_CONFIG_0	VPE_BASE	0x05300000
MMSS_FPB_APU_RGn_ACR	MMSS_APU_BASE	0x05400000
MMSS_SFPB_CTRL_STATUS	MMSS_SFPB_CFG_BASE	0x05700000
VCAP_VCAP_HW_VERSION	VCAP_BASE	0x05900000
VCAP_SMMU_VCAP_M2VCBRn	SMMU_VCAP_BASE	0x07200000
JPEGD_SMMU_JPEGD_M2VCBRn	SMMU_JPEGD_BASE	0x07300000
VPE_SMMU_VPE_M2VCBRn	SMMU_VPE_BASE	0x07400000
MDP4_0_SMMU_MDP0_M2VCBRn	SMMU_MDP4_0_BASE	0x07500000
MDP4_1_SMMU_MDP1_M2VCBRn	SMMU_MDP4_1_BASE	0x07600000
ROT_SMMU_ROT_M2VCBRn	SMMU_ROTATOR_BASE	0x07700000
IJPEG_SMMU_IJPEG_M2VCBRn	SMMU_JPEG_BASE	0x07800000
VFE_SMMU_VFE_M2VCBRn	SMMU_VFE_BASE	0x07900000

Table 14-1 Multi_Media_Sub_System Bases (cont.)

Base Name	Parent	Address
SS1080P_0_SMMU_VCODEC_A_M2VCBRn	SMMU_SS1080P_0_BASE	0x07A00000
SS1080P_1_SMMU_VCODEC_B_M2VCBRn	SMMU_SS1080P_1_BASE	0x07B00000
GFX3D_SMMU_GFX3D_M2VCBRn	SMMU_GFX3D_BASE	0x07C00000
GFX3D1_SMMU_GFX3D1_M2VCBRn	SMMU_GFX3D1_BASE	0x07D00000
SMMU_SFPB_CFG_SFPB_CTRL_STATUS	SMMU_SFPB_CFG_DUMMY_BASE	0x07F00000

14.2 MM SS Clocks registers (0x04000000 MMSS_CC_BASE)

This section contains the Multi-Media Subsystem (MMSS) Clocks registers.

14.2.1 MMSS AHB AXI Clock registers

Clock selection, programming, and gating are under AXI9 control.

0x04000004 MMSS_AHB_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The AHB_NS controls the source selection and configuration of the clocks in the AHB domain.

MMSS_AHB_NS

Bits	Name	Description
31:22	RESERVED_1	Reserved bits
21	CLKCTL_RST0	The reset bit for the hm_arm_clk_ctl res0 0x0: Not Active 0x1: Active
20	CLKCTL_RST1	The reset bit for the hm_arm_clk_ctl res1 0x0: Not Active 0x1: Active
19:18	RESERVED_2	Do not use for APQ8064 (previously used for CLK_DIV_VAL)
17	RESERVED_3	Do not use for APQ8064 (previously used for CLK_SRC_SEL)
16:15	RESERVED_4	Reserved bits
14	CLK_OUT_SEL	This field selects the clk source of the AHB hm_arm_crc 0x0: SRC0 0x1: SRC1

MMSS_AHB_NS (cont.)

Bits	Name	Description
13:10	SRC1_DIV	Divide value for the src1_div pin of AHB hm_arm_crc. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
9:6	SRC0_DIV	Divide value for the src0_div pin of AHB hm_arm_crc. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
5:3	SRC1_SEL	This field selects the output of the clock source 1 MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

MMSS_AHB_NS (cont.)

Bits	Name	Description
2:0	SRC0_SEL	This field selects the output of the clock source 0 MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x04000008 MMSS_AHB_EN

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x00000003

The AHB_EN controls the CXC enable of the clocks in the AHB domain.

MMSS_AHB_EN

Bits	Name	Description
31	FAB_AHB_CLK_EN	This bit enables the fab_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
30	MMSS_FPB_HALT_CTRL_SEL	This is the hardware clock halt control for mmss_fpb_clk. 0x1: Hardware 0x0: Software
29	APU_AHB_HALT_CTRL_SEL	This is the hardware clock halt control for apu_ahb_clk. 0x1: Hardware 0x0: Software
28	APU_AHB_CLK_EN	This bit enables the apu_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
27	RESERVED_1	Removed for APQ8064.
26	SMMU_AHB_HALT_CTRL_SEL	This is the hardware clock halt control smmu_ahb_clk. 0x1: Hardware 0x0: Software
25	RESERVED_2	Removed for APQ8064.

MMSS_AHB_EN (cont.)

Bits	Name	Description
24	AMP_AHB_CLK_EN	This bit enables the amp_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
23	RESERVED_3	Do not use for APQ8064 (previously used for SMI0_AHB_CLK_EN)
22	DSI2_S_AHB_CLK_EN	This bit enables the dsi2_s_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
21	JPEGD_AHB_CLK_EN	This bit enables the jpegd_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
20	RESERVED_4	Do not use for APQ8064 (previously used for csi1_ahb_clk_en)
19	RESERVED	Removed for APQ8064
18	DSI_S_AHB_CLK_EN	This bit enables the dsi1_s_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
17	DSI2_M_AHB_CLK_EN	This bit enables the dsi2_m_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
16	VPE_AHB_CLK_EN	This bit enables the vpe_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
15	SMMU_AHB_CLK_EN	This bit enables the smmu_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
14	HDMI_M_AHB_CLK_EN	This bit enables the hdmi_m_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
13	VFE_AHB_CLK_EN	This bit enables the vfe_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

MMSS_AHB_EN (cont.)

Bits	Name	Description
12	ROT_AHB_CLK_EN	This bit enables the rot_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
11	VCODEC_AHB_CLK_EN	This bit enables the vcodec_ahb_clk. 0x1: Enabled 0x0: Disabled
10	MDP_AHB_CLK_EN	This bit enables the mdp_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
9	DSI_M_AHB_CLK_EN	This bit enables the dsi1_m_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
8	DSI2_M_AHB_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for dsi2_m_ahb_clk. 0x1: Hardware 0x0: Software
7	CSI_AHB_CLK_EN	This bit enables the csi_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
6	IMEM_AHB_CLK_EN	This bit enables the imem_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
5	IJPEG_AHB_CLK_EN	This bit enables the ijpeg_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
4	HDMI_S_AHB_CLK_EN	This bit enables the hdmi_s_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
3	GFX3D_AHB_CLK_EN	This bit enables the gfx3d_ahb_clk. 0x1: Enabled 0x0: Disabled
2	REVERSED	Removed for APQ8064

MMSS_AHB_EN (cont.)

Bits	Name	Description
1	MMSS_FPB_CLK_EN	This bit enables the mmss_fpb_clk during SW mode (The corresponding halt_ctrl_sel should be set to 0x0); During SW mode, do not set this bit to 0x0 otherwise mmss will hang and will need reset. By default this bit is set to 0x1. 0x1: Enabled 0x0: Disabled
0	SFPB_CLK_GATING_SW_CTRL	Default to 1, to bypass the HW clock gating of system fpb. 0x1: Software 0x0: Hardware

0x04000038 MMSS_AHB_EN2

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x000007F9

The AHB_EN controls the CXC enable of the clocks in the AHB domain.

MMSS_AHB_EN2

Bits	Name	Description
31	FAB_AHB_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for fab_ahb_clk. 0x1: Hardware 0x0: Software
30	IJPEG_AHB_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for ijpeg_ahb_clk. 0x1: Hardware 0x0: Software
29	RESERVED_1	Removed for APQ8064
28	RESERVED_2	Removed for APQ8064
27	GFX3D_AHB_HALT_CTRL_SEL	This is the hardware clock halt control for gfx3d_ahb_clk. 0x1: Hardware 0x0: Software
26	VCODEC_AHB_HALT_CTRL_SEL	This is the hardware clock halt control for vcodec_ahb_clk. 0x1: Hardware 0x0: Software
25	ROT_AHB_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for rot_ahb_clk. 0x1: Hardware 0x0: Software

MMSS_AHB_EN2 (cont.)

Bits	Name	Description
24	VPE_AHB_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for vpe_ahb_clk. 0x1: Hardware 0x0: Software
23	VFE_AHB_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for vfe_ahb_clk. 0x1: Hardware 0x0: Software
22	HDMI_S_AHB_HALT_CTRL_SEL	This is the hardware clock halt control for hdmi_s_ahb_clk. 0x1: Hardware 0x0: Software
21	HDMI_M_AHB_HALT_CTRL_SEL	This is the hardware clock halt control for hdmi_m_ahb_clk. 0x1: Hardware 0x0: Software
20	DSI_S_AHB_HALT_CTRL_SEL	This is the hardware clock halt control for dsi1_s_ahb_clk. 0x1: Hardware 0x0: Software
19	DSI_M_AHB_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for dsi1_m_ahb_clk. 0x1: Hardware 0x0: Software
18	AMP_AHB_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for amp_ahb_clk. 0x1: Hardware 0x0: Software
17	RESERVED_3	Do not use for APQ8064 (previously used for csi1_ahb_halt_ctrl_sel)
16	CSI_AHB_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for csi_ahb_clk. 0x1: Hardware 0x0: Software
15	DSI2_S_AHB_HALT_CTRL_SEL	This is the hardware clock halt control for dsi2_s_ahb_clk. 0x1: Hardware 0x0: Software
14	RESERVED_4	Do not use for APQ8064 (previously used for SMI0_AHB_HALT_CTRL_SEL)
13	MDP_AHB_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for mdp_ahb_clk. 0x1: Hardware 0x0: Software

MMSS_AHB_EN2 (cont.)

Bits	Name	Description
12	IMEM_AHB_HALT_CTRL_SEL	This is the hardware clock halt control for imem_ahb_clk. 0x1: Hardware 0x0: Software
11	JPEGD_AHB_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for jpegd_ahb_clk. 0x1: Hardware 0x0: Software
10:7	VFE_AHB_W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to '1111' equals 18 clock-cycle-delay. This is default set to 0xF.
6:3	VFE_AHB_S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to '1111' equals 18 clock-cycle-delay. This is default set to 0xF.
2	VFE_AHB_FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
1	VFE_AHB_FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
0	VFE_AHB_FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated

0x04000248 MMSS_AHB_EN3

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The AHB_EN3 controls the CXC enable of the clocks in the AHB domain.

MMSS_AHB_EN3

Bits	Name	Description
31:2	RESERVED	Reserved bits
1	VCAP_AHB_CLK_EN	This bit enables the vcap_ahb_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
0	VCAP_AHB_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for vcap_ahb_clk. 0x1: Hardware 0x0: Software

0x0400000C MMSS_AHB_INV

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The AHB_INV controls the CXC invert of the clocks in the AHB domain.

MMSS_AHB_INV

Bits	Name	Description
31:29	RESERVED_1	Reserved bits
28	VCAP_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
27	MMSS_FPB_AON_CLK_INV	This bit inverts the always on fpb clk. 0x1: Inverted 0x0: Not Inverted
26	APU_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
25	RESERVED_2	Removed for APQ8064.
24	AMP_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
23	RESERVED_3	Do not use for APQ8064 (previous used for SMI0_AHB_CLK_INV)

MMSS_AHB_INV (cont.)

Bits	Name	Description
22	DSI2_S_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
21	JPEGD_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
20	RESERVED_4	Do not use for APQ8064 (previously used for csi1_ahb_clk_inv)
19	MMSS_FPB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
18	DSI_S_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
17	CAM_AHB_CLK_INV	Do not use for APQ8064 (previously used for cam_ahb_clk_inv)
16	VPE_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
15	SMMU_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
14	HDMI_M_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
13	VFE_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
12	ROT_AHB_CLK_INV	This bit inverts the clk rot_ahb_clk. 0x1: Inverted 0x0: Not inverted
11	VCODEC_AHB_CLK_INV	This bit inverts the vcodec_ahb_clk. 0x1: Inverted 0x0: Not inverted
10	MDP_AHB_CLK_INV	This bit inverts the mdp_ahb_clk. 0x1: Inverted 0x0: Not inverted
9	DSI_M_AHB_CLK_INV	This bit inverts the dsi1_m_ahb_clk. 0x1: Inverted 0x0: Not inverted

MMSS_AHB_INV (cont.)

Bits	Name	Description
8	DSI2_M_AHB_CLK_INV	This bit inverts the dsi2_m_ahb_clk. 0x1: Inverted 0x0: Not inverted
7	CSI_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
6	IMEM_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
5	IJPEG_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
4	HDMI_S_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
3	GFX3D_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted
2	RESERVED_5	Removed for APQ8064
1	RESERVED_6	Removed for APQ8064
0	FAB_AHB_CLK_INV	This bit inverts the clk. 0x1: Inverted 0x0: Not inverted

0x04000014 MMSS_AXI_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The AXI_NS controls the source selection and configuration of the clocks in the AXI domain.

MMSS_AXI_NS

Bits	Name	Description
31:27	RESERVED_1	Reserved bits
26	RESERVED_2	Do not use for APQ8064 (previously used for DDR_FSM_CLK_EN)
25	RESERVED_3	Do not use for APQ8064 (previously used for DDR_FSM_CLK_INV)

MMSS_AXI_NS (cont.)

Bits	Name	Description
24	CLKCTL_RST0	The reset bit for the hm_arm_clk_ctl res0 0x0: Not Active 0x1: Active
23	CLKCTL_RST1	The reset bit for the hm_arm_clk_ctl res1 0x0: Not Active 0x1: Active
22:21	RESERVED_4	Do not use for APQ8064 (previously used for CLK_DIV2_VAL)
20	FAB_CORE_HALT_CTRL_SEL	This is the hardware clock halt control for the fab_core_clk. 0x1: Hardware 0x0: Software
19:18	CLK_DIV_VAL	This field selects divider value for cdiv (to divide the source axi clk (666Mhz)) 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
17	RESERVED	Do not use for APQ8064 (previously used for CLK_SRC_SEL)
16	FAB_CORE_CLK_INV	This bit inverts the fab_core_clk. 0x1: Inverted 0x0: Not inverted
15	FAB_CORE_CLK_EN	This bit enables the fab_core_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
14	CLK_OUT_SEL	This bit selects between src0 and src1 clock source of the axi hm_arm root cell. 0x1: src1 0x0: src0

MMSS_AXI_NS (cont.)

Bits	Name	Description
13:10	SRC1_DIV	This field selects the modulo-N divide value for the axi src clk. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
9:6	SRC0_DIV	This field selects the modulo-N divide value for the axi src clk. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
5:3	SRC1_SEL	This field selects the output of the clock source 1 MUX. Source 100 and 101 are ECO for using MMPLL3. 0x0: pxo 0x1: mmccpll0_src 0x2: gccperfpll_src 0x3: mmccpll1_src 0x4: mmccpll3_early 0x5: mmccpll3_src 0x6: clk_test_se 0x7: pll_test_se

MMSS_AXI_NS (cont.)

Bits	Name	Description
2:0	SRC0_SEL	This field selects the output of the clock source 0 MUX. Source 100 and 101 are ECO for using MMPLL3. 0x0: pxo 0x1: mmccpll0_src 0x2: gccperfpll_src 0x3: mmccpll1_src 0x4: mmccpll3_early 0x5: mmccpll3_src 0x6: clk_test_se 0x7: pll_test_se

0x04000018 MMSS_MAXI_EN

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x7F9

The MAXI_EN controls the CXC enable of the Master clocks in the AXI domain.

MMSS_MAXI_EN

Bits	Name	Description
31	RESERVED_1	Reserved bits
30	RESERVED_2	Do not use for APQ8064 (Previously used for ROOT_AXI_CLK_INV)
29	RESERVED_3	Do not use for APQ8064 (Previously used for ROOT_AXI_HALT_CTRL_SEL)
28	RESERVED_4	Do not use for APQ8064 (Previously used for ROOT_AXI_CLK_EN)
27	JPEGD_AXI_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control jpegd_axi_clk. 0x1: Hardware 0x0: Software
26	FAB_MSP_AXI_CLK_EN	This bit enables the fab_msp_axi clocks. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
25	JPEGD_AXI_CLK_EN	This bit enables the jpegd_axi_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

MMSS_MAXI_EN (cont.)

Bits	Name	Description
24	GMEM_AXI_CLK_EN	This bit enables the gmem_axi_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
23	MDP_AXI_CLK_EN	This bit enables the mdp_axi_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
22	IMEM_AXI_CLK_EN	Clock enable bit for the imem_axi_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
21	IJPEG_AXI_CLK_EN	Clock enable bit ijpeg_axi_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
20	GFX3D_AXI_CLK_EN	This bit is not used.
19	VCODEC_AXI_CLK_EN	Clock enable bit vcodec_axi_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
18	VFE_AXI_CLK_EN	This bit enables the VFE AXI clocks. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
17	FAB_MSP_AXI_HALT_CTRL_SEL	This is the hardware clock halt control for fab_msp_axi_clk. 0x1: Hardware 0x0: Software
16	MDP_AXI_HALT_CTRL_SEL	This is the hardware clock halt control for mdp_axi_clk. 0x1: Hardware 0x0: Software
15	IMEM_AXI_HALT_CTRL_SEL	This is the hardware clock halt control for imem_axi_clk. 0x1: Hardware 0x0: Software
14	GMEM_AXI_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control for gmem_axi_clk. 0x1: Hardware 0x0: Software
13	VCODEC_AXI_HALT_CTRL_SEL	This is the hardware clock halt control for vcodec_axi_clk. 0x1: Hardware 0x0: Software

MMSS_MAXI_EN (cont.)

Bits	Name	Description
12	VFE_AXI_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control vfe_axi_clk. 0x1: Hardware 0x0: Software
11	IJPEG_AXI_HALT_CTRL_SEL	This is the hardware clock halt control for ijpeg_axi_clk. 0x1: Hardware 0x0: Software
10:7	MDP_AXI_W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
6:3	MDP_AXI_S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
2	MDP_AXI_FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
1	MDP_AXI_FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
0	MDP_AXI_FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated

0x04000020 MMSS_MAXI_EN2

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x3027FCFF

The MAXI_EN controls the CXC enable of the Master clocks in the AXI domain.

MMSS_MAXI_EN2

Bits	Name	Description
31	RESERVED_1	Do not use for APQ8064 (previously used for SMI_2X_AXI_CLK_INV)
30	RESERVED_2	Do not use for APQ8064 (previously used for SMI_2X_AXI_CLK_EN)
29	AXI_ROOT_EN	This bit enables the async_clk_r_ena of axi root cell. Default is set to 0x1. 0x1: enabled 0x0: disabled
28	VCODEC_AXI_FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
27	VPE_AXI_HALT_CTRL_SEL	This is the hardware clock halt control for vpe_axi_clk. 0x1: Hardware 0x0: Software
26	VPE_AXI_CLK_EN	This bit enables the clocks. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
25	ROT_AXI_HALT_CTRL_SEL	This is the hardware clock halt control for rot_axi_clk. 0x1: Hardware 0x0: Software
24	ROT_AXI_CLK_EN	Clock enable bit. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
23	SMI_AXI_CLK_INV	Do not use for APQ8064 (previously used for smi_axi_clk_inv)
22	SMI_AXI_CLK_EN	Do not use for APQ8064 (previously used for smi_axi_clk_en)
21	GMEM_AXI_FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated

MMSS_MAXI_EN2 (cont.)

Bits	Name	Description
20	GMEM_AXI_FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
19	GMEM_AXI_FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
18:15	GMEM_AXI_W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
14:11	GMEM_AXI_S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
10	IMEM_AXI_FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
9	IMEM_AXI_FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
8	IMEM_AXI_FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running

MMSS_MAXI_EN2 (cont.)

Bits	Name	Description
7:4	IMEM_AXI_W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
3:0	IMEM_AXI_S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.

0x0400002C MMSS_MAXI_EN3

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0200400

The MAXI_EN controls the CXC enable of the Master clocks in the AXI domain.

MMSS_MAXI_EN3

Bits	Name	Description
31	RESERVED_1	Do not use for APQ8064 (previously used for vcodec_axi)
30	RESERVED_2	Do not use for APQ8064 (previously used for vcodec_axi)
29:26	RESERVED_3	Do not use for APQ8064 (previously used for vcodec_axi)
25:22	RESERVED_4	Do not use for APQ8064 (previously used for vcodec_axi)
21	VPE_AXI_FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
20	VPE_AXI_FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated

MMSS_MAXI_EN3 (cont.)

Bits	Name	Description
19	VPE_AXI_FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
18:15	VPE_AXI_W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
14:11	VPE_AXI_S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
10	ROT_AXI_FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
9	ROT_AXI_FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
8	ROT_AXI_FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
7:4	ROT_AXI_W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.

MMSS_MAXI_EN3 (cont.)

Bits	Name	Description
3:0	ROT_AXI_S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to '1111' equals18 clock-cycle-delay. This is default set to 0xF.

0x04000114 MMSS_MAXI_EN4

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0027FCFF

The MAXI_EN4 controls the CXC enable of the Master clocks in the AXI domain.

MMSS_MAXI_EN4

Bits	Name	Description
31:26	RESERVED	Reserved bits
25	VCODEC_AXI_A_CLK_EN	This bit enables the VCODEC AXI Aclocks. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
24	VCODEC_AXI_A_HALT_CTRL_SEL	This is the hardware clock halt control for vcodec_axi_A_clk. 0x1: Hardware 0x0: Software
23	VCODEC_AXI_B_CLK_EN	This bit enables the VCODEC AXI B clocks. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
22	VCODEC_AXI_B_HALT_CTRL_SEL	This is the hardware clock halt control for vcodec_axi_B_clk. 0x1: Hardware 0x0: Software
21	VCODEC_B_AXI_FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated

MMSS_MAXI_EN4 (cont.)

Bits	Name	Description
20	VCODEC_B_AXI_FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
19	VCODEC_B_AXI_FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
18:15	VCODEC_B_AXI_W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
14:11	VCODEC_B_AXI_S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
10	VCODEC_A_AXI_FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
9	VCODEC_A_AXI_FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
8	VCODEC_A_AXI_FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running

MMSS_MAXI_EN4 (cont.)

Bits	Name	Description
7:4	VCODEC_A_AXI_W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
3:0	VCODEC_A_AXI_S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.

0x04000244 MMSS_MAXI_EN5

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x9FE4FF

The MAXI_EN5 controls the CXC enable of the Master clocks in the AXI domain.

MMSS_MAXI_EN5

Bits	Name	Description
31:26	RESERVED	Reserved bits
25	GFX3D_AXI_CLK_EN	This bit enables the GFX3D AXIclocks. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
24	GFX3D_AXI_HALT_CTRL_SEL	This is the hardware clock halt control for gfx3d_axi_clk. 0x1: Hardware 0x0: Software
23	GFX3D_AXI_FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
22	GFX3D_AXI_FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated

MMSS_MAXI_EN5 (cont.)

Bits	Name	Description
21	GFX3D_AXI_FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
20:17	GFX3D_AXI_W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
16:13	GFX3D_AXI_S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
12	VCAP_AXI_CLK_EN	This bit enables the VCAP AXIclocks. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
11	VCAP_AXI_HALT_CTRL_SEL	This is the hardware clock halt control for vcap_axi_clk. 0x1: Hardware 0x0: Software
10	VCAP_AXI_FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
9	VCAP_AXI_FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
8	VCAP_AXI_FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running

MMSS_MAXI_EN5 (cont.)

Bits	Name	Description
7:4	VCAP_AXI_W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
3:0	VCAP_AXI_S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.

0x0400001C MMSS_MAXI_INV

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The MAXI_INV controls the CXC invert of the Master clocks in the AXI domain.

MMSS_MAXI_INV

Bits	Name	Description
31:15	RESERVED	Reserved bits
14	VCAP_AXI_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
13	VCODEC_AXI_B_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
12	VCODEC_AXI_A_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
11	VPE_AXI_CLK_INV	This bit inverts the clocks. 0x1: Inverted 0x0: Not Inverted
10	FAB_MSP_AXI_CLK_INV	This bit inverts the clocks. 0x1: Inverted 0x0: Not Inverted
9	JPEGD_AXI_CLK_INV	This bit inverts the clocks. 0x1: Inverted 0x0: Not Inverted

MMSS_MAXI_INV (cont.)

Bits	Name	Description
8	GMEM_AXI_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
7	MDP_AXI_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
6	IMEM_AXI_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
5	IJPEG_AXI_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
4	GFX3D_AXI_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
3	VCODEC_AXI_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
2	ROT_AXI_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
1	VFE_AXI_CLK_INV	This bit inverts the VFE AXI clocks. 0x1: Inverted 0x0: Not Inverted
0	RESERVED_BIT0	Reserved bit

0x04000030 MMSS_SAXI_EN

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x00000000

The SAXI_EN controls the CXC enable of the Slave clocks in the AXI domain.

MMSS_SAXI_EN

Bits	Name	Description
31:14	RESERVED	Reserved bits
13	AXI_S3_FCLK_HALT_CTRL_SEL	Removed for APQ8064

MMSS_SAXI_EN (cont.)

Bits	Name	Description
12	AXI_S2_FCLK_HALT_CTRL_SEL	This is the hardware clock halt control. 0x1: Hardware 0x0: Software
11	AXI_S1_FCLK_HALT_CTRL_SEL	This is the hardware clock halt control. 0x1: Hardware 0x0: Software
10	AXI_S0_FCLK_HALT_CTRL_SEL	This is the hardware clock halt control. 0x1: Hardware 0x0: Software
9	AXI_S3_FCLK_CLK_EN	Removed for APQ8064
8	AXI_S2_FCLK_CLK_EN	This bit enables the clock. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
7	AXI_S1_FCLK_CLK_EN	This bit enables the clock. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
6	AXI_S0_FCLK_CLK_EN	This bit enables the clock. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
5	AXI_S2_HALT_CTRL_SEL	This is the hardware clock halt control. 0x1: Hardware 0x0: Software
4	AXI_S1_HALT_CTRL_SEL	This is the hardware clock halt control. 0x1: Hardware 0x0: Software
3	AXI_S0_HALT_CTRL_SEL	Removed for APQ8064.
2	AXI_S2_CLK_EN	This bit enables the clock. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
1	AXI_S1_CLK_EN	This bit enables the clock. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
0	AXI_S0_CLK_EN	Removed for APQ8064.

0x04000034 MMSS_SAXI_INV

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The SAXI_INV controls the CXC invert of the Slave clocks in the AXI domain.

MMSS_SAXI_INV

Bits	Name	Description
31:8	RESERVED	Reserved bits
7	AXI_S3_FCLK_CLK_INV	Removed for APQ8064.
6	AXI_S2_FCLK_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
5	AXI_S1_FCLK_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
4	AXI_S0_FCLK_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
3	AXI_S3_CLK_INV	Do not use for APQ8064 (previously used for axi_s3_clk_inv)
2	AXI_S2_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
1	AXI_S1_CLK_INV	This bit inverts the clock. 0x1: Inverted 0x0: Not Inverted
0	AXI_S0_CLK_INV	Removed for APQ8064

0x04000040 MMSS_CSI0_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CSI0_CC contains the clock control bits.

MMSS_CSI0_CC

Bits	Name	Description
31:11	RESERVED	Reserved bits

MMSS_CSI0_CC (cont.)

Bits	Name	Description
10	PHY_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for csiphy_clk 0x1: Hardware 0x0: Software
9	CLKPHY_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
8	CLKPHY_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for csi_clk 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000044 MMSS_CSI0_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CSI0_MD contains the M and D values of the M/N:D divider.

MMSS_CSI0_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x04000048 MMSS_CSI0_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CSI0_NS_REG controls the source selection and configuration of the clocks in the CSI domain. It also contains the N value of the DSI M/N:D divider.

MMSS_CSI0_NS

Bits	Name	Description
31:24	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
23:16	RESERVED_1	Reserved bits
15:14	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
13:8	RESERVED_2	Reserved bits
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: gnd 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x04000024 MMSS_CSI1_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CSI1_CC contains the clock control bits.

MMSS_CSI1_CC

Bits	Name	Description
31:11	RESERVED	Reserved bits
10	PHY_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for csiphy_clk 0x1: Hardware 0x0: Software
9	CLKPHY_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
8	CLKPHY_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for csi_clk 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000028 MMSS_CSI1_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CSI1_MD contains the M and D values of the M/N:D divider.

MMSS_CSI1_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x04000010 MMSS_CSI1_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CSI1_NS_REG controls the source selection and configuration of the clocks in the CSI domain. It also contains the N value of the DSI M/N:D divider.

MMSS_CSI1_NS

Bits	Name	Description
31:24	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
23:16	RESERVED_1	Reserved bits
15:14	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
13:8	RESERVED_2	Reserved bits
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED	Reserved bits

MMSS_CSI1_NS (cont.)

Bits	Name	Description
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: gnd 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x0400022C MMSS_CSI2_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CSI2_CC contains the clock control bits.

MMSS_CSI2_CC

Bits	Name	Description
31:11	RESERVED	Reserved bits
10	PHY_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for csiphy_clk 0x1: Hardware 0x0: Software
9	CLKPHY_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
8	CLKPHY_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled

MMSS_CSI2_CC (cont.)

Bits	Name	Description
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for csi_clk 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000230 MMSS_CSI2_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CSI2_MD contains the M and D values of the M/N:D divider.

MMSS_CSI2_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x04000234 MMSS_CSI2_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CSI2_NS_REG controls the source selection and configuration of the clocks in the CSI domain. It also contains the N value of the DSI M/N:D divider.

MMSS_CSI2_NS

Bits	Name	Description
31:24	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
23:16	RESERVED_1	Reserved bits
15:14	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
13:8	RESERVED_2	Reserved bits
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: gnd 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x0400004C MMSS_DSI_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI_CC contains the clock control bits.

MMSS_DSI_CC

Bits	Name	Description
31	FORCE_CORE_ON	Reserved bits (not used for APQ8064)
30	FORCE_PERIPH_ON	Reserved bits (not used for APQ8064)
29	FORCE_PERIPH_OFF	Reserved bits (not used for APQ8064)
28:24	RESERVED_1	Reserved bits
23:20	W	Reserved bits (not used for APQ8064)

MMSS_DSI_CC (cont.)

Bits	Name	Description
19:16	S	Reserved bits (not used for APQ8064)
15:9	RESERVED_2	Reserved bits
8	PMXO_SEL	Removed for APQ8064. Will use PXO directly.
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for dsi_clk 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000050 MMSS_DSI_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI_MD contains the M and D values of the M/N:D divider.

MMSS_DSI_MD

Bits	Name	Description
31:9	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x04000054 MMSS_DSI_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI_NS_REG controls the source selection and configuration of the clocks in the DSI domain. It also contains the N value of the DSI M/N:D divider.

MMSS_DSI_NS

Bits	Name	Description
31:24	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
15:14	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
13:8	RESERVED_1	Reserved bits
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED_2	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: dsi2_phy_pll_out_dsiclk 0x2: gnd 0x3: dsi1_phy_pll_out_dsiclk 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x04000058 MMSS_MISC_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The MISC_CC contains the clock control bits.

MMSS_MISC_CC

Bits	Name	Description
31	FORCE_CORE_ON	Reserved bits (not used for APQ8064)
30	FORCE_PERIPH_ON	Reserved bits (not used for APQ8064)
29	FORCE_PERIPH_OFF	Reserved bits (not used for APQ8064)
28	RESERVED_1	Reserved bits
27	CSI_PIX_CLK_INV	This bit inverts the clock at output of CXC 0x1: Inverted 0x0: Not Inverted
26	CSI_PIX_CLK_EN	This bit enables the csi_pix_clk CXC 0x1: Enabled 0x0: Disabled
25	CSI_PIX_SRC_SEL	Anti-glitch mux select for csi_pix_clk. Note Anti-glitch mux require all the clock sources to be running when switching. 0x0: csi0_clksrc 0x1: csi1_clksrc
24	RESERVED_2	Do not use for APQ8064 (previously used for SMI0_XO_HALT_CTRL_SEL)
23	RESERVED_3	Reserved bit
22	RESERVED_4	Do not use for APQ8064 (previously used for DSI_ESC_HALT_CTRL_SEL)
21	RESERVED_5	Do not use for APQ8064 (previously used for DSI_BYTE_HALT_CTRL_SEL)
20	MDP_VSYNC_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control. 0x1: Hardware 0x0: Software
19:18	HDMI_DIV	This field selects the divide value for hdmi_app_clk. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
17:16	RESERVED_6	Reserved bits
15	RESERVED_7	Reserved bit
14	CSI_RDI_CLK_INV	This bit inverts the clock at output of CXC 0x1: Inverted 0x0: Not Inverted
13	CSI_RDI_CLK_EN	This bit enables the csi_rdi_clk CXC 0x1: Enabled 0x0: Disabled

MMSS_MISC_CC (cont.)

Bits	Name	Description
12	CSI_RDI_SRC_SEL	Anti-glitch mux select for csi_rdi_clk. Note Anti-glitch mux require all the clock sources to be running when switching. 0x0: csi0_clksrc 0x1: csi1_clksrc
11	RESERVED_8	Do not use for APQ8064 (previously used for SMI0_XO_CLK_INV)
10	RESERVED_9	Do not use for APQ8064 (previously used for SMI0_XO_CLK_EN)
9:8	RESERVED_10	Reserved bits
7	MDP_VSYNC_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
6	MDP_VSYNC_CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
5:4	RESERVED_11	Reserved bits
3	RESERVED_12	Do not use for APQ8064 (previously used for DSI_BYTE_CLK_INV)
2	RESERVED_13	Do not use for APQ8064 (previously used for DSI_BYTE_CLK_EN)
1	RESERVED_14	Do not use for APQ8064 (previously used for DSI_ESC_CLK_INV)
0	RESERVED_BIT0	Do not use for APQ8064 (previously used for DSI_ESC_CLK_EN)

0x0400005C MMSS_MISC_CC2

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x00000400

The MISC_CC contains the clock control bits.

MMSS_MISC_CC2

Bits	Name	Description
31	RESERVED_1	Reserved bit
30	RESERVED_2	Do not use for APQ8064 (previously used for DSI_BYTE_FORCE_PERIPH_ON)
29	RESERVED_3	Do not use for APQ8064 (previously used for DSI_BYTE_FORE_PERIPH_OFF)
28	HDMIPLL_MUXSEL	Removed for APQ8064. Will directly use PXO.

MMSS_MISC_CC2 (cont.)

Bits	Name	Description
27:24	RESERVED_4	Do not use for APQ8064 (previously used for BYTECLK_CDIV_VAL)
23	HDMI_APP_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock halt control. 0x1: Hardware 0x0: Software
22	RESERVED_5	Do not use for APQ8064 (previously used for BYTECLK_PMXO_SEL))
21:18	HDMIREF_CDIV_VAL	Reserved bits (Do not use for APQ8064)
17	HDMI_PMXO_SEL	hdmi_pmxo
16	RESERVED_6	Reserved bits
15	RESERVED_7	Do not use for APQ8064 (previously used for SMI0_PMXO_SEL)
14	RESERVED_8	Do not use for APQ8064 (previously used for ESC_PMXO_SEL)
13	VSYNC_PMXO_SEL	Removed for APQ8064. Will directly use PXO.
12	HDMI_APP_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
11	HDMI_APP_CLK_EN	This bit enables the CXC output. 0x1: Enabled 0x0: Disabled
10	RESERVED_9	Do not use for APQ8064 (previously used for DSI_BYTE_FORCE_CORE_ON)
9:6	RESERVED_10	Do not use for APQ8064 (previously used for DSI_BYTE_W)
5:2	RESERVED	Do not use for APQ8064 (previously used for DSI_BYTE_S)
1:0	RESERVED_BIT1_0	Do not use for APQ8064 (previously used for ESCCLK_CDIV_VAL)

0x04000238 MMSS_MISC_CC3

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The MISC_CC3 contains the clock control bits.

MMSS_MISC_CC3

Bits	Name	Description
31:14	RESERVED	Reserved bits

MMSS_MISC_CC3 (cont.)

Bits	Name	Description
13	CSI_PIX_SRC_SEL2	Second Anti-Glitch Mux select. Note Anti-glitch mux require all the clock sources to be running when switching. 0x0: Output of MISC_CC 0x1: csi2_clksrc
12	CSI_RDI_SRC_SEL2	Anti-Glitch Mux select. Note Anti-glitch mux require all the clock sources to be running when switching. 0x0: Output of MISC_CC 0x1: csi2_clksrc
11	CSI_PIX1_CLK_INV	This bit inverts the clock at output of CXC 0x1: Inverted 0x0: Not Inverted
10	CSI_PIX1_CLK_EN	This bit enables the csi_pix_clk CXC 0x1: Enabled 0x0: Disabled
9	CSI_PIX1_SRC_SEL2	Second Anti-Glitch Mux select. Note Anti-glitch mux require all the clock sources to be running when switching. Note: select 0 is not gnd, but should be: Output of MISC_CC3[CSI_PIX1_SRC_SEL] 0x0: gnd 0x1: csi2_clksrc
8	CSI_PIX1_SRC_SEL	Anti-Glitch Mux select. Note Anti-glitch mux require all the clock sources to be running when switching. 0x0: csi0_clksrc 0x1: csi1_clksrc
7	CSI_RDI2_CLK_INV	This bit inverts the clock at output of CXC 0x1: Inverted 0x0: Not Inverted
6	CSI_RDI2_CLK_EN	This bit enables the csi_rdi_clk CXC 0x1: Enabled 0x0: Disabled
5	CSI_RDI2_SRC_SEL2	Second Anti-Glitch Mux select. Note Anti-glitch mux require all the clock sources to be running when switching. Note: select 0 is not gnd, but should be: Output of MISC_CC3[CSI_RDI2_SRC_SEL] 0x0: gnd 0x1: csi2_clksrc
4	CSI_RDI2_SRC_SEL	Anti-Glitch Mux select. Note Anti-glitch mux require all the clock sources to be running when switching. 0x0: csi0_clksrc 0x1: csi1_clksrc
3	CSI_RDI1_CLK_INV	This bit inverts the clock at output of CXC 0x1: Inverted 0x0: Not Inverted

MMSS_MISC_CC3 (cont.)

Bits	Name	Description
2	CSI_RDI1_CLK_EN	This bit enables the csi_rdi1_clk CXC 0x1: Enabled 0x0: Disabled
1	CSI_RDI1_SRC_SEL2	Second Anti-Glitch Mux select. Note Anti-glitch mux require all the clock sources to be running when switching. Note: select 0 is not gnd, but should be: Output of MISC_CC3[CSI_RDI1_SRC_SEL] 0x0: gnd 0x1: csi2_clksrc
0	CSI_RDI1_SRC_SEL	Anti-Glitch Mux select. Note Anti-glitch mux require all the clock sources to be running when switching. 0x0: csi0_clksrc 0x1: csi1_clksrc

0x04000060 MMSS_GFX2D0_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x00000000

The GFX2D0_CC Removed for APQ8064

MMSS_GFX2D0_CC

Bits	Name	Description
31:0	RESERVED	Removed feature for APQ8064

0x04000064 MMSS_GFX2D0_MD0

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The GFX2D0_MD removed for APQ8064.

MMSS_GFX2D0_MD0

Bits	Name	Description
31:0	RESERVED	Removed feature for APQ8064

0x04000068 MMSS_GFX2D0_MD1

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The GFX2D0_MD Removed feature for APQ8064

MMSS_GFX2D0_MD1

Bits	Name	Description
31:0	RESERVED	Removed feature for APQ8064

0x04000070 MMSS_GFX2D0_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The GFX2D0_NS_REG Removed feature for APQ8064.

MMSS_GFX2D0_NS

Bits	Name	Description
31:0	RESERVED	Removed for APQ8064

0x04000074 MMSS_GFX2D1_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x80000000

The GFX2D1_CC Removed for APQ8064

MMSS_GFX2D1_CC

Bits	Name	Description
31:0	RESERVED	Removed feature for APQ8064

0x04000078 MMSS_GFX2D1_MD0

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The GFX2D1_MD Removed for APQ8064.

MMSS_GFX2D1_MD0

Bits	Name	Description
31:0	RESERVED	Removed feature for APQ8064

0x0400006C MMSS_GFX2D1_MD1

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The GFX2D1_MD Removed for APQ8064.

MMSS_GFX2D1_MD1

Bits	Name	Description
31:8	RESERVED	Removed feature for APQ8064

0x0400007C MMSS_GFX2D1_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The GFX2D1_NS_REG removed feature for APQ8064.

MMSS_GFX2D1_NS

Bits	Name	Description
31:0	RESERVED	Removed feature for APQ8064

0x04000080 MMSS_GFX3D_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x9FF00000

The GFX3D_CC contains the clock control bits.

MMSS_GFX3D_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:24	RESERVED_1	Reserved bits
23:20	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
15:12	RESERVED_2	Reserved bits
11	CLK_OUT_SEL	This field selects the modulo-N divide value. 0x0: SRC0 0x1: SRC1

MMSS_GFX3D_CC (cont.)

Bits	Name	Description
10:9	MND_MODE0	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
8	MND_EN0	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
7:6	MND_MODE1	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN1	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for gfx3d_clk 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000084 MMSS_GFX3D_MD0

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The GFX3D_MD contains the M and D values of the M/N:D divider.

MMSS_GFX3D_MD0

Bits	Name	Description
31:8	RESERVED	Reserved bits
7:4	M_VAL	This is the M value for the clock branch's M/N:D divider.
3:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x04000088 MMSS_GFX3D_MD1

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The GFX3D_MD contains the M and D values of the M/N:D divider.

MMSS_GFX3D_MD1

Bits	Name	Description
31:8	RESERVED	Reserved bits
7:4	M_VAL	This is the M value for the clock branch's M/N:D divider.
3:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x0400008C MMSS_GFX3D_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The GFX3D_NS_REG controls the source selection and configuration of the clocks in the GFX3D domain. It also contains the N value of the GFX3D M/N:D divider.

MMSS_GFX3D_NS

Bits	Name	Description
31:24	RESERVED_1	Reserved bits
23	CLKCTL_RST0	The reset bit for the hm_dyn_clk_ctl res0 0x0: Not Active 0x1: Active
22	CLKCTL_RST1	The reset bit for the hm_dyn_clk_ctl res1 0x0: Not Active 0x1: Active

MMSS_GFX3D_NS (cont.)

Bits	Name	Description
21:18	N0_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
17:14	N1_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
13:6	RESERVED_2	Reserved bits
5:3	SRC0_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x5: mmccpll0_src 0x6: clk_test_se 0x7: pll_test_se
2:0	SRC1_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x5: mmccpll0_src 0x6: clk_test_se 0x7: pll_test_se

0x04000098 MMSS_IJPEG_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x9FF00000

The IJPEG_CC contains the clock control bits.

MMSS_IJPEG_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated

MMSS_IJPEG_CC (cont.)

Bits	Name	Description
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:24	RESERVED_1	Reserved bits
23:20	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
15:8	RESERVED_2	Reserved bits
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for ijpeg_clk 0x1: Hardware 0x0: Software
3	IDLE_CTRL_SEL	This is the hardware clock idle control. 0x1: Hardware 0x0: Software

MMSS_IJPEG_CC (cont.)

Bits	Name	Description
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x0400009C MMSS_IJPEG_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The IJPEG_MD contains the M and D values of the M/N:D divider.

MMSS_IJPEG_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x040000A0 MMSS_IJPEG_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The IJPEG_NS_REG controls the source selection and configuration of the clocks in the IJPEG domain. It also contains the N value of the IJPEG M/N:D divider.

MMSS_IJPEG_NS

Bits	Name	Description
31:24	RESERVED_1	Reserved bits
23:16	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.

MMSS_IJPEG_NS (cont.)

Bits	Name	Description
15:12	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
11:8	PRE_DIV_IDLE	This field selects the modulo-N pre-divide value during idle mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED_2	Reserved bits

MMSS_IJPEG_NS (cont.)

Bits	Name	Description
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x040000A4 MMSS_JPEGD_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x9FF00000

The JPEGD_CC contains the clock control bits.

MMSS_JPEGD_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:24	RESERVED_1	Reserved bits

MMSS_JPEGD_CC (cont.)

Bits	Name	Description
23:20	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
15:5	RESERVED_2	Reserved bits
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control jpegd_clk 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x040000AC MMSS_JPEGD_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The JPEGD_NS_REG controls the source selection and configuration of the clocks in the JPEGD domain.

MMSS_JPEGD_NS

Bits	Name	Description
31:16	RESERVED_1	Reserved bits

MMSS_JPEGD_NS (cont.)

Bits	Name	Description
15:12	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
11:8	RESERVED_2	Reserved bits
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x040000C0 MMSS_MDP_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x80FF0000

The MDP_CC contains the clock control bits.

MMSS_MDP_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:25	RESERVED_1	Reserved bits
24	CLK_SRC_SEL	Select clock source. 0x1: hdmipll 0x0: mmss_pll
23:20	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
15:12	RESERVED_2	Reserved bits
11	CLK_OUT_SEL	This field selects the modulo-N divide value. 0x0: SRC0 0x1: SRC1

MMSS_MDP_CC (cont.)

Bits	Name	Description
10:9	MND_MODE0	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
8	MND_EN0	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
7:6	MND_MODE1	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN1	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for mdp_clk 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x040000C4 MMSS_MDP_MD0

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The MDP_MD contains the M and D values of the M/N:D divider.

MMSS_MDP_MD0

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x040000C8 MMSS_MDP_MD1

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The MDP_MD contains the M and D values of the M/N:D divider.

MMSS_MDP_MD1

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x040000D0 MMSS_MDP_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The MDP_NS_REG controls the source selection and configuration of the clocks in the MDP domain. It also contains the N value of the MDP M/N:D divider.

MMSS_MDP_NS

Bits	Name	Description
31	CLKCTL_RST0	The reset bit for the hm_dyn_clk_ctl res0 0x0: Not Active 0x1: Active
30	CLKCTL_RST1	The reset bit for the hm_dyn_clk_ctl res1 0x0: Not Active 0x1: Active
29:22	N0_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.

MMSS_MDP_NS (cont.)

Bits	Name	Description
21:14	N1_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
13:6	RESERVED	Reserved bits
5:3	SRC0_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: gnd 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se
2:0	SRC1_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: gnd 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x0400016C MMSS_MDP_LUT_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x80FF0000

The MDP_LUT_CC contains the clock control bits.

MMSS_MDP_LUT_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated

MMSS_MDP_LUT_CC (cont.)

Bits	Name	Description
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:24	RESERVED_1	Reserved bits
23:20	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
15:5	RESERVED_2	Reserved bits
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for mdp_clk 0x1: Hardware 0x0: Software
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x040000D4 MMSS_PIXEL_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x80000000

This register is not used in APQ8064. Maintained for backward compatibility.

MMSS_PIXEL_CC

Bits	Name	Description
31:0	RESERVED	Do not use for APQ8064

0x04000094 MMSS_DSI2_PIXEL_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI2_PIXEL_CC contains the clock control bits.

MMSS_DSI2_PIXEL_CC

Bits	Name	Description
31:8	RESERVED_1	Reserved bits
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
3	RESERVED_2	Reserved
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted

MMSS_DSI2_PIXEL_CC (cont.)

Bits	Name	Description
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000120 MMSS_PIXEL_CC2

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

This register is not used for APQ8064. Maintained for backward compatibility.

MMSS_PIXEL_CC2

Bits	Name	Description
31:0	RESERVED	Do not use for APQ8064

0x0400003C MMSS_DSI2_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The dsi2_CC contains the clock control bits.

MMSS_DSI2_CC

Bits	Name	Description
31	FORCE_CORE_ON	Reserved bits (not used for APQ8064)
30	FORCE_PERIPH_ON	Reserved bits (not used for APQ8064)
29	FORCE_PERIPH_OFF	Reserved bits (not used for APQ8064)
28:24	RESERVED_1	Reserved bits
23:20	W	Reserved bits (not used for APQ8064)
19:16	S	Reserved bits (not used for APQ8064)
15:9	RESERVED_2	Reserved bits
8	RESERVED_BIT8	Reserved bits to match dsi_cc range

MMSS_DSI2_CC (cont.)

Bits	Name	Description
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for dsi_clk 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x040000A8 MMSS_DSI2_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI2_MD contains the M and D values of the M/N:D divider.

MMSS_DSI2_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x0400012C MMSS_DSI2_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI2_NS_REG controls the source selection and configuration of the clocks in the DSI domain. It also contains the N value of the DSI M/N:D divider.

MMSS_DSI2_NS

Bits	Name	Description
31:24	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
15:14	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
13:8	RESERVED_1	Reserved bits
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED_2	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: dsi2_phy_pll_out_dsiclk 0x2: gnd 0x3: dsi1_phy_pll_out_dsiclk 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x04000264 MMSS_DSI2_PIXEL_CC2

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x1

The DSI2_PIXEL_CC2 contains the clock control bits.

MMSS_DSI2_PIXEL_CC2

Bits	Name	Description
31:4	RESERVED	Reserved bits
3	LVDS_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
2	LVDS_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
1	LVDS_CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
0	DSI2_PCLK_CGC_EN	This bit controls the acgc for the dsi2_pclk. Default is enabled. 0x1: Enabled 0x0: Disabled

0x040000D8 MMSS_PIXEL_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

This register is not used in APQ8064. Maintained for backward compatibility.

MMSS_PIXEL_MD

Bits	Name	Description
31:0	RESERVED	Do not use for APQ8064.

0x040000B8 MMSS_DSI2_PIXEL_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI2_PIXEL_MD contains the M and D values of the M/N:D divider.

MMSS_DSI2_PIXEL_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x040000DC MMSS_PIXEL_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

This register is not used in APQ8064. Maintained for backward compatibility.

MMSS_PIXEL_NS

Bits	Name	Description
31:0	RESERVED	Do not use for APQ8064.

0x040000E4 MMSS_DSI2_PIXEL_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The dsi2_PIXEL_NS_REG controls the source selection and configuration of the clocks in the dsi2_PIXEL domain. It also contains the N value of the dsi2_PIXEL M/N:D divider.

MMSS_DSI2_PIXEL_NS

Bits	Name	Description
31:24	RESERVED_1	Reserved bits
23:16	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.

MMSS_DSI2_PIXEL_NS (cont.)

Bits	Name	Description
15:12	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
11:8	PRE_DIV_IDLE	Reserved
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED_2	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: dsi2_phy_pll_out_dsiclk 0x2: lvdsphy_clk 0x3: dsi1_phy_pll_out_dsiclk 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x04000090 MMSS_DSI1_BYTE_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x80FF0000

The DSI1_BYTE_CC contains the clock control bits.

MMSS_DSI1_BYTE_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:24	RESERVED_1	Reserved bits
23:20	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
15:5	RESERVED_2	Reserved bits
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
3	RESERVED	Reserved bits
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled

MMSS_DSI1_BYTE_CC (cont.)

Bits	Name	Description
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x040000B0 MMSS_DSI1_BYTE_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI1_BYTE_NS_REG controls the source selection and configuration of the clocks in the dsi1 BYTE domain.

MMSS_DSI1_BYTE_NS

Bits	Name	Description
31:16	RESERVED_1	Reserved bits
15:12	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
11:8	PRE_DIV_IDLE	Reserved
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active

MMSS_DSI1_BYTE_NS (cont.)

Bits	Name	Description
6:3	RESERVED_2	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: dsi1_phy_pll_out_byteclk 0x2: dsi2_phy_pll_out_byteclk 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x040000B4 MMSS_DSI2_BYTE_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x80FF0000

The DSI2_BYTE_CC contains the clock control bits.

MMSS_DSI2_BYTE_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:24	RESERVED_1	Reserved bits

MMSS_DSI2_BYTE_CC (cont.)

Bits	Name	Description
23:20	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
15:5	RESERVED_2	Reserved bits
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x040000BC MMSS_DSI2_BYTE_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI2_BYTE_NS_REG controls the source selection and configuration of the clocks in the dsi2 BYTE domain.

MMSS_DSI2_BYTE_NS

Bits	Name	Description
31:16	RESERVED_1	Reserved bits

MMSS_DSI2_BYTE_NS (cont.)

Bits	Name	Description
15:12	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
11:8	PRE_DIV_IDLE	Reserved
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED_2	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: dsi1_phy_pll_out_byteclk 0x2: dsi2_phy_pll_out_byteclk 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x040000CC MMSS_DSI1_ESC_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI1_ESC_CC contains the clock control bits.

MMSS_DSI1_ESC_CC

Bits	Name	Description
31:5	RESERVED	Reserved bits
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x0400011C MMSS_DSI1_ESC_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The dsi1_ESC_NS_REG controls the source selection and configuration of the clocks in the dsi1 ESC domain.

MMSS_DSI1_ESC_NS

Bits	Name	Description
31:16	RESERVED_1	Reserved bits

MMSS_DSI1_ESC_NS (cont.)

Bits	Name	Description
15:12	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
11:8	PRE_DIV_IDLE	Reserved
8:3	RESERVED_2	Reserved bits
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: dsi1_phy_pll_out_byteclk 0x2: dsi2_phy_pll_out_byteclk 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x0400013C MMSS_DSI2_ESC_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI2_ESC_CC contains the clock control bits.

MMSS_DSI2_ESC_CC

Bits	Name	Description
31:5	RESERVED	Reserved bits
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000150 MMSS_DSI2_ESC_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI2_ESC_NS_REG controls the source selection and configuration of the clocks in the dsi2_ESC domain.

MMSS_DSI2_ESC_NS

Bits	Name	Description
31:16	RESERVED_1	Reserved bits

MMSS_DSI2_ESC_NS (cont.)

Bits	Name	Description
15:12	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
11:8	PRE_DIV_IDLE	Reserved bits (Do not use for APQ8064)
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED_2	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: dsi1_phy_pll_out_byteclk 0x2: dsi2_phy_pll_out_byteclk 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x040000E0 MMSS_ROT_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x80FF0000

The ROT_CC contains the clock control bits.

MMSS_ROT_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:24	RESERVED_1	Reserved bits
23:20	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
15:5	RESERVED_2	Reserved bits
4	HALT_CTRL_SEL	This is the hardware clock idle control for rot_clk 0x1: Hardware 0x0: Software
3	RESERVED	Reserved bit
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted

MMSS_ROT_CC (cont.)

Bits	Name	Description
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x040000E8 MMSS_ROT_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The ROT_NS_REG controls the source selection and configuration of the clocks in the ROT domain.

MMSS_ROT_NS

Bits	Name	Description
31	RESERVED_1	Reserved bit
30	CLK_OUT_SEL	This field selects the modulo-N divide value. 0x0: SRC0 0x1: SRC1
29:26	SRC1_DIV	This field selects the modulo-N divide value. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16

MMSS_ROT_NS (cont.)

Bits	Name	Description
25:22	SRC0_DIV	This field selects the modulo-N divide value. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
21:19	SRC1_SEL	This field selects the output of the clock source 1 MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se
18:16	SRC0_SEL	This field selects the output of the clock source 0 MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se
15:8	RESERVED_2	Reserved bits
7	MNCNTR_RST0	The MN reset bit for hm_arm_crc_clk_ctl res0 0x0: Not Active 0x1: Active
6	MNCNTR_RST1	The MN reset bit for hm_arm_crc_clk_ctl res1 0x0: Not Active 0x1: Active
5:1	RESERVED	Reserved bits
0	RESERVED_BIT0	Reserved bit

0x040000EC MMSS_TV_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x00000000

The TV_CC contains the clock control bits.

MMSS_TV_CC

Bits	Name	Description
31	RESERVED_BIT31	Do not use. Removed feature for APQ8064.
30	RESERVED_1	Do not use. Removed feature for APQ8064.
29	RESERVED_2	Do not use. Removed feature for APQ8064.
28:25	RESERVED_3	Reserved bits
24	RESERVED_4	Do not use. Removed feature for APQ8064.
23:20	RESERVED_5	Do not use. Removed feature for APQ8064.
19:16	RESERVED_6	Do not use. Removed feature for APQ8064.
15	RESERVED_7	Do not use. Removed feature for APQ8064.
14	HDMI_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
13	HDMI_CLK_INV	This bit inverts the hdmi_tv_clk. 0x1: Inverted 0x0: Not Inverted
12	HDMI_CLK_EN	This bit enables the hdmi_tv_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
11	RESERVED_8	Do not use. Removed feature for APQ8064.
10	RESERVED_9	Do not use. Removed feature for APQ8064.
9	RESERVED_10	Do not use. removed feature for APQ8064.
8	RESERVED	Do not use. removed feature for APQ8064.
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode

MMSS_TV_CC (cont.)

Bits	Name	Description
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
3	IDLE_CTRL_SEL	Reserved
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	MDP_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	MDP_CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000124 MMSS_TV_CC2

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x000004FF

The TV_CC contains the clock control bits.

MMSS_TV_CC2

Bits	Name	Description
31:18	RESERVED_1	Reserved bits
17	NPL_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
16	NPL_CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
15	RGB_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted

MMSS_TV_CC2 (cont.)

Bits	Name	Description
14	RGB_CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
13	RESERVED_2	Do not use for APQ8064. (previously used for DSUB_HALT_CTRL_SEL)
12	RESERVED_3	Do not use for APQ8064. (previously used for DSUB_CLK_INV)
11	RESERVED_4	Do not use for APQ8064. (previously used for DSUB_CLK_EN)
10	MDP_TV_CLK_FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
9	MDP_TV_CLK_FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
8	MDP_TV_CLK_FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
7:4	MDP_TV_CLK_W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
3:0	MDP_TV_CLK_S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.

0x040000F0 MMSS_TV_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The TV_MD contains the M and D values of the M/N:D divider.

MMSS_TV_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x040000F4 MMSS_TV_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The TV_NS_REG controls the source selection and configuration of the clocks in the TV domain. It also contains the N value of the TV M/N:D divider.

MMSS_TV_NS

Bits	Name	Description
31:24	RESERVED_1	Reserved bits
23:16	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
15:14	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
13:8	RESERVED_2	Reserved bits
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6	TV_CLK_DIV2_EN	MDP_TV_CLK and NPL_TV_CLK selec bit.
5:3	RESERVED	Reserved bits

MMSS_TV_NS (cont.)

Bits	Name	Description
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: lvdsphy clk 0x2: gnd_1 0x3: hdmi phy clk 0x4: mxo 0x5: gnd_2 0x6: clk_test_se 0x7: pll_test_se

0x040000F8 MMSS_VCODEC_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x80FF0000

The VCODEC_CC contains the clock control bits.

MMSS_VCODEC_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. To use inter frame clock gating of 1080P video core, RAMs shall not be set into the sleep mode to avoid CPU to execute undefined instruction at the very first cycle of re-enabled clock. Hence FORCE_CORE_ON and FORCE_PERIPH_ON bits need to be set to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. To use inter frame clock gating of 1080P video core, RAMs shall not be set into the sleep mode to avoid CPU to execute undefined instruction at the very first cycle of re-enabled clock. Hence FORCE_CORE_ON and FORCE_PERIPH_ON bits need to be set to 0x1. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated

MMSS_VCODEC_CC (cont.)

Bits	Name	Description
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:24	RESERVED_1	Reserved bits
23:20	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
15:14	RESERVED_2	Reserved bits
13	CLK_OUT_SEL	This field selects the modulo-N divide value. 0x0: SRC0 0x1: SRC1
12:11	MND_MODE1	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
10	MND_EN1	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
9	PIXEL_CLK_INV	This bit inverts the vcodec_pclk. 0x1: Inverted 0x0: Not inverted
8	PIXEL_CLK_EN	Reserved
7:6	MND_MODE0	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN0	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled

MMSS_VCODEC_CC (cont.)

Bits	Name	Description
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC of vcodec_clk. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the vcodec_pclk and vcodec_clk. (The halt_ctrl_sel should be set to 0 (software mode). 0x1: Enabled 0x0: Disabled

0x040000FC MMSS_VCODEC_MD0

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The VCODEC_MD contains the M and D values of the M/N:D divider.

MMSS_VCODEC_MD0

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x04000128 MMSS_VCODEC_MD1

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The VCODEC_MD contains the M and D values of the M/N:D divider.

MMSS_VCODEC_MD1

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x04000100 MMSS_VCODEC_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The VCODEC_NS_REG controls the source selection and configuration of the clocks in the VCODEC domain. It also contains the N value of the VCODEC M/N:D divider.

MMSS_VCODEC_NS

Bits	Name	Description
31	CLKCTL_RST0	The reset bit for the hm_dyn_clk_ctl res0 0x0: Not Active 0x1: Active
30	CLKCTL_RST1	The reset bit for the hm_dyn_clk_ctl res1 0x0: Not Active 0x1: Active
29:27	SRC1_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x5: mmccpll0_src 0x6: clk_test_se 0x7: pll_test_se
26:19	N1_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
18:11	N0_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
10:3	RESERVED	Reserved bits

MMSS_VCODEC_NS (cont.)

Bits	Name	Description
2:0	SRC0_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x5: mmccpll0_src 0x6: clk_test_se 0x7: pll_test_se

0x0400023C MMSS_VFE_CC2

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x800000FF

The VFE_CC2 contains the clock control bits.

MMSS_VFE_CC2

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running

MMSS_VFE_CC2 (cont.)

Bits	Name	Description
7:4	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to '1111' equals 18 clock-cycle-delay. This is default set to 0xF.
3:0	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to '1111' equals18 clock-cycle-delay. This is default set to 0xF.

0x04000104 MMSS_VFE_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x80FF0000

The VFE_CC contains the clock control bits.

MMSS_VFE_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:24	RESERVED_1	Reserved bits

MMSS_VFE_CC (cont.)

Bits	Name	Description
23:20	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
15	RESERVED_2	Reserved
14	CSI_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
13	CSI_CLK_INV	This bit inverts the csi_clk. 0x1: Inverted 0x0: Not inverted
12	CSI_CLK_EN	This bit enables the csi_clk. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
11	RESERVED_3	Reserved bit
10	RESERVED_4	Reserved bit
9	PAD_REG_CLK_INV	Reserved bit (Do not use for APQ8064)
8	PAD_REG_CLK_EN	Reserved bit (Do not use for APQ8064)
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled

MMSS_VFE_CC (cont.)

Bits	Name	Description
1	CLK_INV	This bit inverts the _clk. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the _clk. 0x1: Enabled 0x0: Disabled

0x04000108 MMSS_VFE_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The VFE_MD contains the M and D values of the M/N:D divider.

MMSS_VFE_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x0400010C MMSS_VFE_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The VFE_NS_REG controls the source selection and configuration of the clocks in the CAMIF domain. It also contains the N value of the VFE M/N:D divider.

MMSS_VFE_NS

Bits	Name	Description
31:24	RESERVED_1	Reserved bits
23:16	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
15:12	RESERVED_2	Reserved bits

MMSS_VFE_NS (cont.)

Bits	Name	Description
11:10	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2
9:8	RESERVED_3	Reserved bits
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED_4	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x04000110 MMSS_VPE_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x80FF0000

The VPE_CC contains the clock control bits.

MMSS_VPE_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated

MMSS_VPE_CC (cont.)

Bits	Name	Description
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:24	RESERVED_1	Reserved bits
23:20	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
15:5	RESERVED_2	Reserved bits
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000118 MMSS_VPE_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The VPE_NS_REG controls the source selection and configuration of the clocks in the VPE domain.

MMSS_VPE_NS

Bits	Name	Description
31:16	RESERVED_1	Reserved bits
15:12	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
11:8	PRE_DIV_IDLE	Reserved
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED_2	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x04000130 MMSS_DSI_PIXEL_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x80FF0000

The DSI_PIXEL_CC contains the clock control bits.

MMSS_DSI_PIXEL_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:24	RESERVED_1	Reserved bits
23:20	W	A 4 bit wake counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle. Setting to ’1111’ equals 18 clock-cycle-delay. This is default set to 0xF.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to ’1111’ equals18 clock-cycle-delay. This is default set to 0xF.
15:8	RESERVED_2	Reserved bits
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled

MMSS_DSI_PIXEL_CC (cont.)

Bits	Name	Description
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
3	IDLE_CTRL_SEL	Reserved
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000134 MMSS_DSI_PIXEL_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI_PIXEL_MD contains the M and D values of the M/N:D divider.

MMSS_DSI_PIXEL_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x04000138 MMSS_DSI_PIXEL_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DSI_PIXEL_NS_REG controls the source selection and configuration of the clocks in the dsi1_PIXEL domain. It also contains the N value of the dsi1_PIXEL M/N:D divider.

MMSS_DSI_PIXEL_NS

Bits	Name	Description
31:24	RESERVED_1	Reserved bits
23:16	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
15:12	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4 0x4: Div-5 0x5: Div-6 0x6: Div-7 0x7: Div-8 0x8: Div-9 0x9: Div-10 0xA: Div-11 0xB: Div-12 0xC: Div-13 0xD: Div-14 0xE: Div-15 0xF: Div-16
11:8	PRE_DIV_IDLE	Reserved
7	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
6:3	RESERVED_2	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: dsi2_phy_pll_out_dsiclk 0x2: gnd 0x3: dsi1_phy_pll_out_dsiclk 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x04000140 MMSS_CAMCLK0_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CAMCLK0_CC contains the clock control bits.

MMSS_CAMCLK0_CC

Bits	Name	Description
31	FORCE_CORE_ON	Reserved bits (not used for APQ8064)
30	FORCE_PERIPH_ON	Reserved bits (not used for APQ8064)
29	FORCE_PERIPH_OFF	Reserved bits (not used for APQ8064)
28:24	RESERVED_1	Reserved bits
23:20	W	Reserved bits (not used for APQ8064)
19:16	S	Reserved bits (not used for APQ8064)
15:9	RESERVED_2	Reserved bits
8	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
3	IDLE_CTRL_SEL	Reserved bit (Do not use for APQ8064)
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000144 MMSS_CAMCLK0_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CAMCLK0_MD contains the M and D values of the M/N:D divider.

MMSS_CAMCLK0_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x04000148 MMSS_CAMCLK0_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CAMCLK0_NS_REG controls the source selection and configuration of the clocks in the CAMCLK domain. It also contains the N value of the CAMCLK0 M/N:D divider.

MMSS_CAMCLK0_NS

Bits	Name	Description
31:24	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
23:16	RESERVED_1	Reserved bits
15:14	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
13:3	RESERVED_2	Reserved bits

MMSS_CAMCLK0_NS (cont.)

Bits	Name	Description
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x04000154 MMSS_CAMCLK1_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CAMCLK1_CC contains the clock control bits.

MMSS_CAMCLK1_CC

Bits	Name	Description
31	FORCE_CORE_ON	Reserved bits (not used for APQ8064)
30	FORCE_PERIPH_ON	Reserved bits (not used for APQ8064)
29	FORCE_PERIPH_OFF	Reserved bits (not used for APQ8064)
28:24	RESERVED_1	Reserved bits
23:20	W	Reserved bits (not used for APQ8064)
19:16	S	Reserved bits (not used for APQ8064)
15:9	RESERVED_2	Reserved bits
8	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled

MMSS_CAMCLK1_CC (cont.)

Bits	Name	Description
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
3	IDLE_CTRL_SEL	Reserved
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000158 MMSS_CAMCLK1_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CAMCLK1_MD contains the M and D values of the M/N:D divider.

MMSS_CAMCLK1_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x0400015C MMSS_CAMCLK1_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CAMCLK1_NS_REG controls the source selection and configuration of the clocks in the CAMCLK domain. It also contains the N value of the CAMCLK1 M/N:D divider.

MMSS_CAMCLK1_NS

Bits	Name	Description
31:24	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
23:16	RESERVED_1	Reserved bits
15:14	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
13:3	RESERVED_2	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x04000220 MMSS_CAMCLK2_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CAMCLK2_CC contains the clock control bits.

MMSS_CAMCLK2_CC

Bits	Name	Description
31	FORCE_CORE_ON	Reserved bits (not used for APQ8064)
30	FORCE_PERIPH_ON	Reserved bits (not used for APQ8064)
29	FORCE_PERIPH_OFF	Reserved bits (not used for APQ8064)
28:24	RESERVED_1	Reserved bits
23:20	W	Reserved bits (not used for APQ8064)
19:16	S	Reserved bits (not used for APQ8064)
15:9	RESERVED_2	Reserved bits

MMSS_CAMCLK2_CC (cont.)

Bits	Name	Description
8	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
3	IDLE_CTRL_SEL	Reserved
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000224 MMSS_CAMCLK2_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CAMCLK2_MD contains the M and D values of the M/N:D divider.

MMSS_CAMCLK2_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x04000228 MMSS_CAMCLK2_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CAMCLK2_NS_REG controls the source selection and configuration of the clocks in the CAMCLK domain. It also contains the N value of the CAMCLK1 M/N:D divider.

MMSS_CAMCLK2_NS

Bits	Name	Description
31:24	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
23:16	RESERVED_1	Reserved bits
15:14	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
13:3	RESERVED_2	Reserved bits
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x04000160 MMSS_CSIPHYTIMER_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CSIPHYTIMER_CC contains the clock control bits.

MMSS_CSIPHYTIMER_CC

Bits	Name	Description
31:13	RESERVED	Reserved bits

MMSS_CSIPHYTIMER_CC (cont.)

Bits	Name	Description
12	CSI2CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
11	CSI2CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
10	CSI1CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
9	CSI1CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
8	MNCNTR_RST	The MN reset bit 0x0: Not Active 0x1: Active
7:6	MND_MODE	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control. 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CSI0CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CSI0CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x04000164 MMSS_CSIPHYTIMER_MD

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CSIPHYTIMER_MD contains the M and D values of the M/N:D divider.

MMSS_CSIPHYTIMER_MD

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	M_VAL	This is the M value for the clock branch's M/N:D divider.
7:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x04000168 MMSS_CSIPHYTIMER_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The CSIPHYTIMER_NS_REG controls the source selection and configuration of the clocks in the CSIPHYTIMER domain. It also contains the N value of the CSIPHYTIMER M/N:D divider.

MMSS_CSIPHYTIMER_NS

Bits	Name	Description
31:24	N_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
23:16	RESERVED_1	Reserved bits
15:14	PRE_DIV_FUNC	This field selects the modulo-N pre-divide value during functional mode of operation. 0x0: Div-1 0x1: Div-2 0x2: Div-3 0x3: Div-4
13:3	RESERVED_2	Reserved bits

MMSS_CSIPHYTIMER_NS (cont.)

Bits	Name	Description
2:0	SRC_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: reserved 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x0400014C MMSS_GCCPERFPLL_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x1

This bit is used to control the CGC that is gating the GCC PERF PLL source. Since the APQ8064 PLL8 is placed far from the mmss cc clock generators, due to power reason this clock source can be gated by SW if needed. By default this clock CGC is 0x1 or enabled.

MMSS_GCCPERFPLL_CTL

Bits	Name	Description
31:2	RESERVED	Reserved bits
1	RESERVED_BIT1	Reserved bit
0	CGC_CLK_EN	gated GCC PERF PLL source clock enable; Default is 0x1. 0x0: disable 0x1: enable

0x04000180 MMSS_GFX2D0_GFS_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x300

GFX2D0 Power Rail control.

MMSS_GFX2D0_GFS_CTL

Bits	Name	Description
31:10	RESERVED_1	Reserved bits

MMSS_GFX2D0_GFS_CTL (cont.)

Bits	Name	Description
9	GFX2D0_GFS_RET	GDS Retention bit. GFS_RET = 0 and GFS_EN = 0 will collapse the power to the core. GFS_RET = 1 and GFS_EN = 0 put core into VDD_MIN stage (aka sleep mode).
8	GFX2D0_GFS_EN	GDS enable bit. GFS_EN = 1 for core operational mode. When GFS_EN = 1, GFS_RET is a don't care.
7:6	RESERVED_2	Reserved
5	GFX2D0_CLAMP	Clamp I/O bit for the core. 1 = clamp, 0 = unclamp
4:0	GFX2D0_GFS_CNT	This is the number of AHB_CLK cycles to delay the assertion of gfs_en_all after the assertion of gfs_en1 when enabling the global distributed switch. Should set to all 1s for safe mode operation. Decreasing the CNT value can reduce latency.

0x04000184 MMSS_GFX2D1_GFS_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x300

GFX2D1 Power Rail control.

MMSS_GFX2D1_GFS_CTL

Bits	Name	Description
31:10	RESERVED_1	Reserved bits
9	GFX2D1_GFS_RET	GDS Retention bit. GFS_RET = 0 and GFS_EN = 0 will collapse the power to the core. GFS_RET = 1 and GFS_EN = 0 put core into VDD_MIN stage (aka sleep mode).
8	GFX2D1_GFS_EN	GDS enable bit. GFS_EN = 1 for core operational mode. When GFS_EN = 1, GFS_RET is a don't care.
7:6	RESERVED_2	Reserved
5	GFX2D1_CLAMP	Clamp I/O bit for the core. 1 = clamp, 0 = unclamp
4:0	GFX2D1_GFS_CNT	This is the number of AHB_CLK cycles to delay the assertion of gfs_en_all after the assertion of gfs_en1 when enabling the global distributed switch. Should set to all 1s for safe mode operation. Decreasing the CNT value can reduce latency.

0x04000188 MMSS_GFX3D_GFS_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x300

GFX3D Power Rail control.

MMSS_GFX3D_GFS_CTL

Bits	Name	Description
31:10	RESERVED_1	Reserved bits
9	GFX3D_GFS_RET	GDS Retention bit. GFS_RET = 0 and GFS_EN = 0 will collapse the power to the core. GFS_RET = 1 and GFS_EN = 0 put core into VDD_MIN stage (aka sleep mode).
8	GFX3D_GFS_EN	GDS enable bit. GFS_EN = 1 for core operational mode. When GFS_EN = 1, GFS_RET is a don't care.
7:6	RESERVED_2	Reserved
5	GFX3D_CLAMP	Clamp I/O bit for the core. 1 = clamp, 0 = unclamp
4:0	GFX3D_GFS_CNT	This is the number of AHB_CLK cycles to delay the assertion of gfs_en_all after the assertion of gfs_en1 when enabling the global distributed switch. Should set to all 1s for safe mode operation. Decreasing the CNT value can reduce latency.

0x0400018C MMSS_ROT_GFS_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x300

ROT Power Rail control.

MMSS_ROT_GFS_CTL

Bits	Name	Description
31:10	RESERVED_1	Reserved bits
9	ROT_GFS_RET	GDS Retention bit. GFS_RET = 0 and GFS_EN = 0 will collapse the power to the core. GFS_RET = 1 and GFS_EN = 0 put core into VDD_MIN stage (aka sleep mode).

MMSS_ROT_GFS_CTL (cont.)

Bits	Name	Description
8	ROT_GFS_EN	GDS enable bit. GFS_EN = 1 for core operational mode. When GFS_EN = 1, GFS_RET is a don't care.
7:6	RESERVED_2	Reserved
5	ROT_CLAMP	Clamp I/O bit for the core. 1 = clamp, 0 = unclamp
4:0	ROT_GFS_CNT	This is the number of AHB_CLK cycles to delay the assertion of gfs_en_all after the assertion of gfs_en1 when enabling the global distributed switch. Should set to all 1s for safe mode operation. Decreasing the CNT value can reduce latency.

0x04000190 MMSS_MDP_GFS_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x300

MDP Power Rail control.

MMSS_MDP_GFS_CTL

Bits	Name	Description
31:10	RESERVED_1	Reserved bits
9	MDP_GFS_RET	GDS Retention bit. GFS_RET = 0 and GFS_EN = 0 will collapse the power to the core. GFS_RET = 1 and GFS_EN = 0 put core into VDD_MIN stage (aka sleep mode).
8	MDP_GFS_EN	GDS enable bit. GFS_EN = 1 for core operational mode. When GFS_EN = 1, GFS_RET is a don't care.
7:6	RESERVED_2	Reserved
5	MDP_CLAMP	Clamp I/O bit for the core. 1 = clamp, 0 = unclamp
4:0	MDP_GFS_CNT	This is the number of AHB_CLK cycles to delay the assertion of gfs_en_all after the assertion of gfs_en1 when enabling the global distributed switch. Should set to all 1s for safe mode operation. Decreasing the CNT value can reduce latency.

0x04000194 MMSS_VED_GFS_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x300

VED Power Rail control.

MMSS_VED_GFS_CTL

Bits	Name	Description
31:10	RESERVED_1	Reserved bits
9	VED_GFS_RET	GDS Retention bit. GFS_RET = 0 and GFS_EN = 0 will collapse the power to the core. GFS_RET = 1 and GFS_EN = 0 put core into VDD_MIN stage (aka sleep mode).
8	VED_GFS_EN	GDS enable bit. GFS_EN = 1 for core operational mode. When GFS_EN = 1, GFS_RET is a don't care.
7:6	RESERVED_2	Reserved
5	VED_CLAMP	Clamp I/O bit for the core. 1 = clamp, 0 = unclamp
4:0	VED_GFS_CNT	This is the number of AHB_CLK cycles to delay the assertion of gfs_en_all after the assertion of gfs_en1 when enabling the global distributed switch. Should set to all 1s for safe mode operation. Decreasing the CNT value can reduce latency.

0x04000198 MMSS_VFE_GFS_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x300

VFE Power Rail control.

MMSS_VFE_GFS_CTL

Bits	Name	Description
31:10	RESERVED_1	Reserved bits
9	VFE_GFS_RET	GDS Retention bit. GFS_RET = 0 and GFS_EN = 0 will collapse the power to the core. GFS_RET = 1 and GFS_EN = 0 put core into VDD_MIN stage (aka sleep mode).

MMSS_VFE_GFS_CTL (cont.)

Bits	Name	Description
8	VFE_GFS_EN	GDS enable bit. GFS_EN = 1 for core operational mode. When GFS_EN = 1, GFS_RET is a don't care.
7:6	RESERVED_2	Reserved
5	VFE_CLAMP	Clamp I/O bit for the core. 1 = clamp, 0 = unclamp
4:0	VFE_GFS_CNT	This is the number of AHB_CLK cycles to delay the assertion of gfs_en_all after the assertion of gfs_en1 when enabling the global distributed switch. Should set to all 1s for safe mode operation. Decreasing the CNT value can reduce latency.

0x0400019C MMSS_VPE_GFS_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x300

VPE Power Rail control.

MMSS_VPE_GFS_CTL

Bits	Name	Description
31:10	RESERVED_1	Reserved bits
9	VPE_GFS_RET	GDS Retention bit. GFS_RET = 0 and GFS_EN = 0 will collapse the power to the core. GFS_RET = 1 and GFS_EN = 0 put core into VDD_MIN stage (aka sleep mode).
8	VPE_GFS_EN	GDS enable bit. GFS_EN = 1 for core operational mode. When GFS_EN = 1, GFS_RET is a don't care.
7:6	RESERVED_2	Reserved
5	VPE_CLAMP	Clamp I/O bit for the core. 1 = clamp, 0 = unclamp
4:0	VPE_GFS_CNT	This is the number of AHB_CLK cycles to delay the assertion of gfs_en_all after the assertion of gfs_en1 when enabling the global distributed switch. Should set to all 1s for safe mode operation. Decreasing the CNT value can reduce latency.

0x040001A0 MMSS_GEMINI_GFS_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x300

Power Rail status.

MMSS_GEMINI_GFS_CTL

Bits	Name	Description
31:10	RESERVED_1	Reserved bits
9	GEMINI_GFS_RET	GDS Retention bit. GFS_RET = 0 and GFS_EN = 0 will collapse the power to the core. GFS_RET = 1 and GFS_EN = 0 put core into VDD_MIN stage (aka sleep mode).
8	GEMINI_GFS_EN	GDS enable bit. GFS_EN = 1 for core operational mode. When GFS_EN = 1, GFS_RET is a don't care.
7:6	RESERVED_2	Reserved
5	GEMINI_CLAMP	Clamp I/O bit for the core. 1 = clamp, 0 = unclamp
4:0	GEMINI_GFS_CNT	This is the number of AHB_CLK cycles to delay the assertion of gfs_en_all after the assertion of gfs_en1 when enabling the global distributed switch. Should set to all 1s for safe mode operation. Decreasing the CNT value can reduce latency.

0x04000254 MMSS_VCAP_GFS_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x020

Power Rail status for VCAP IP. This core is power collapsed and clamped by default.

MMSS_VCAP_GFS_CTL

Bits	Name	Description
31:10	RESERVED_1	Reserved bits
9	VCAP_GFS_RET	GDS Retention bit. GFS_RET = 0 and GFS_EN = 0 will collapse the power to the core. GFS_RET = 1 and GFS_EN = 0 put core into VDD_MIN stage (aka sleep mode). This bit is set to 0x0 by default.

MMSS_VCAP_GFS_CTL (cont.)

Bits	Name	Description
8	VCAP_GFS_EN	GDS enable bit. GFS_EN = 1 for core operational mode. When GFS_EN = 1, GFS_RET is a don't care. This bit is set to 0x0 by default
7:6	RESERVED_2	Reserved
5	VCAP_CLAMP	Clamp I/O bit for the core. 1 = clamp, 0 = unclamp. This bit is set to 0x1 by default
4:0	VCAP_GFS_CNT	This is the number of AHB_CLK cycles to delay the assertion of gfs_en_all after the assertion of gfs_en1 when enabling the global distributed switch. Should set to all 1s for safe mode operation. Decreasing the CNT value can reduce latency.

0x040001A4 MMSS_GFS_CTL_STATUS

Type: Read
Clock: AHB_CLK

Power Rail status.

MMSS_GFS_CTL_STATUS

Bits	Name	Description
31:10	RESERVED	Reserved bits
9	VCAP	Power status for VCAP GFS 0x0: OFF 0x1: ON
8	GEMINI	Power status for GEMINI GFS 0x0: OFF 0x1: ON
7	ROT	Power status for ROT GFS 0x0: OFF 0x1: ON
6	VPE	Power status for VPE GFS 0x0: OFF 0x1: ON
5	GFX3D	Power status for GFX3D GFS 0x0: OFF 0x1: ON
4	MDP	Power status for MDP GFS 0x0: OFF 0x1: ON

MMSS_GFS_CTL_STATUS (cont.)

Bits	Name	Description
3	VED	Power status for VED GFS 0x0: OFF 0x1: ON
2	GFX2D1	Power status for GFX2D1 GFS 0x0: OFF 0x1: ON
1	GFX2D0	Power status for GFX2D0 GFS 0x0: OFF 0x1: ON
0	VFE	Power status for VFE GFS 0x0: OFF 0x1: ON

0x040001A8 MMSS_AXI_FRQSW_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x00000000

This register is not used in APQ8064. Maintained for backward compatibility.

MMSS_AXI_FRQSW_CTL

Bits	Name	Description
31:6	RESERVED_1	Reserved bits
5:0	RESERVED_2	Do not use for APQ8064

0x040001AC MMSS_AXI_CLK_SRC_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

This register is not used in APQ8064. Maintained for Backward compatibility.

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MMSS_AXI_CLK_SRC_CTL

Bits	Name	Description
31:0	RESERVED	Do not use for APQ8064

0x040001B0 MMSS_AXI_FRQSW_STATUS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

This register is not used in APQ8064. Maintained for backward compatibility.

MMSS_AXI_FRQSW_STATUS

Bits	Name	Description
31:0	RESERVED	Do not use for APQ8064

0x04000178 MMSS_VCAP_CC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x80FF0000

The VCAP_CC contains the clock control bits.

MMSS_VCAP_CC

Bits	Name	Description
31	FORCE_CORE_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_nret_n) to power collapse the memory core. This SW bit when set to 0x1 will force the memory core to be powered on and when set to 0x0 will allow the memory core to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x1. 0x1: memory core power is forced on 0x0: memory core is power collapsed when clock is gated
30	FORCE_PERIPH_ON	When the clock is gated using the fxcxc hm, it triggers a signal (slp_ret_n) to power collapse the memory periphery. This SW bit when set to 0x1 will force the memory periphery to be powered on and when set to 0x0 will allow the memory periphery to be power collapsed when clock is gated. During reset, this bit is defaulted to 0x0. 0x1: memory periphery power is forced on 0x0: memory periphery is power collapsed when clock is gated
29	FORCE_PERIPH_OFF	This SW bit when set to 0x1 will force the memory periphery to be powered off and when set to 0x0 will allow the memory periphery to be power on when clock is running. During reset, this bit is defaulted to 0x0. This bit is redundant if the FORCE_PERIPH_ON is set to 0x1. 0x1: memory periphery power is forced powered off 0x0: memory periphery is power on when clock is running
28:24	RESERVED_1	Reserved bits

MMSS_VCAP_CC (cont.)

Bits	Name	Description
23:20	W	A 4 bit sleep counter value; When the async clock halt is disabled, the memory control signal will be turned on immediately, but the clock will remain gated for W clock cycle . Setting to ’1111’ equals 18 clock-cycle-delay.
19:16	S	A 4 bit sleep counter value; When the async clock halt is asserted, the clock will be gated immediately, but the memory control signal will only turn off after S clock cycle. Setting to’1111’ equals18 clock-cycle-delay.
15	RESERVED_2	Reserved bits
14	NPL_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
13	NPL_CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled
12	NPL_HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for vcap_npl_clk 0x1: Hardware 0x0: Software
11	CLK_OUT_SEL	This field selects the modulo-N divide value. 0x0: SRC0 0x1: SRC1
10:9	MND_MODE0	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
8	MND_EN0	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled
7:6	MND_MODE1	This field determines the operational mode of the M/N:D divider. 0x0: Bypass 0x1: Clock swallow mode 0x2: Dual-edge mode 0x3: Single-edge mode
5	MND_EN1	This field enables the M/N:D divider. 0x1: Enabled 0x0: Disabled

MMSS_VCAP_CC (cont.)

Bits	Name	Description
4	HALT_CTRL_SEL	Hardware mode is not supported. Do not set this bit to 0x1. This is the hardware clock idle control for vcap_clk 0x1: Hardware 0x0: Software
2	ROOT_EN	This bit enables the root of the clock tree. 0x1: Enabled 0x0: Disabled
1	CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	CLK_EN	This bit enables the CXC output. (The corresponding halt_ctrl_sel should be set to 0x0 (software mode)). 0x1: Enabled 0x0: Disabled

0x040001EC MMSS_VCAP_MD0

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The VCAP_MD contains the M and D values of the M/N:D divider.

MMSS_VCAP_MD0

Bits	Name	Description
31:8	RESERVED	Reserved bits
7:4	M_VAL	This is the M value for the clock branch's M/N:D divider.
3:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x04000218 MMSS_VCAP_MD1

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The VCAP_MD contains the M and D values of the M/N:D divider.

MMSS_VCAP_MD1

Bits	Name	Description
31:8	RESERVED	Reserved bits
7:4	M_VAL	This is the M value for the clock branch's M/N:D divider.
3:0	D_VAL	This is the NOT(2*D) value for the clock branch's M/N:D divider.

0x0400021C MMSS_VCAP_NS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The VCAP_NS_REG controls the source selection and configuration of the clocks in the VCAP domain. It also contains the N value of the MDP M/N:D divider.

MMSS_VCAP_NS

Bits	Name	Description
31:24	RESERVED_1	Reserved bits
23	CLKCTL_RST0	The reset bit for the hm_dyn_clk_ctl res0 0x0: Not Active 0x1: Active
22	CLKCTL_RST1	The reset bit for the hm_dyn_clk_ctl res1 0x0: Not Active 0x1: Active
21:18	N0_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
17:14	N1_VAL	This is the NOT(N-M) value of the clock branch's M/N:D divider when it is used as either modulo-N divider or as full M/N:D divider.
13:6	RESERVED_2	Reserved bits
5:3	SRC0_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: gnd 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

MMSS_VCAP_NS (cont.)

Bits	Name	Description
2:0	SRC1_SEL	This field selects the output of the clock source MUX. 0x0: pxo 0x1: mmccpll1_src 0x2: gccperfpll_src 0x3: gnd 0x4: mxo 0x6: clk_test_se 0x7: pll_test_se

0x04000170 MMSS_RPM_IRQ_EN

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

This RPM_IRQ_EN is used to enable the IRQ from cores to RPM

MMSS_RPM_IRQ_EN

Bits	Name	Description
31:25	RESERVED	Reserved bits
24	GFX3D_VBIF	Level IRQ for Oxili vbif
23	VCAP_VP	Level IRQ from vcap pad
22	VCAP_VC	Level IRQ from vcap core
21	CSIPHY2	Edge IRQ from csiphy2
20	CSID2	Edge IRQ from csid2
19	VPE	Level IRQ from vpe
18	MFC	Level IRQ from vcodec
17	TVENC	Removed for APQ8064
16	ROTATOR	Level IRQ from rotator
15	MDP	Level IRQ from mdp
14	JPEGD	Level IRQ from jpegd
13	IMEM	Level IRQ from imem
12	HDMI	Level IRQ from hdmi
11	GFX3D	Level IRQ from gfx3d
10	VGC1	Removed for APQ8064
9	VGC0	Removed for APQ8064

MMSS_RPM_IRQ_EN (cont.)

Bits	Name	Description
8	DSI2	Level IRQ from dsi2
7	DSI1	Level IRQ from dsi1
6	VFE	Edge IRQ from vfe
5	JPEG	Edge IRQ from jpeg
4	ISPIF	Edge IRQ from ispif
3	CSID1	Edge IRQ from csid1
2	CSID0	Edge IRQ from csid0
1	CSIPHY1	Edge IRQ from csiphy1
0	CSIPHY0	Edge IRQ from csiphy0

0x04000174 MMSS_RPM_IRQ_STATUS

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

This RPM_IRQ_STATUS is used to read the status of the IRQ from cores to RPM

MMSS_RPM_IRQ_STATUS

Bits	Name	Description
31:25	RESERVED	Reserved bits
24	GFX3D_VBIF	Read Status of IRQ from Oxili vbif
23	VCAP_VP	Read Status of IRQ from vcap pad
22	VCAP_VC	Read Status of IRQ from vcap core
21	CSIPHY2	Read Status of IRQ from csiphy2
20	CSID2	Read Status of IRQ from csid2
19	VPE	Read Status of IRQ from vpe
18	MFC	Read Status of IRQ from vcodec
17	TVENC	Removed for APQ8064
16	ROTATOR	Read Status of IRQ from rotator
15	MDP	Read Status of IRQ from mdp
14	JPEGD	Read Status of IRQ from jpegd
13	IMEM	Read Status of IRQ from imem
12	HDMI	Read Status of IRQ from hdmi

MMSS_RPM_IRQ_STATUS (cont.)

Bits	Name	Description
11	GFX3D	Read Status of IRQ from gfx3d
10	VGC1	Removed for APQ8064
9	VGC0	Removed for APQ8064
8	DSI2	Read Status of IRQ from dsi2
7	DSI1	Read Status of IRQ from dsi1
6	VFE	Read Status of IRQ from vfe
5	JPEG	Read Status of IRQ from jpeg
4	ISPIF	Read Status of IRQ from ispif
3	CSID1	Read Status of IRQ from csid1
2	CSID0	Read Status of IRQ from csid0
1	CSIPHY1	Read Status of IRQ from csiphy1
0	CSIPHY0	Read Status of IRQ from csiphy0

0x0400017C MMSS_RPM_IRQ_CLEAR

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

This RPM_IRQ_CLEAR is used for the edge IRQ. The edge IRQ is converted to level irq, and this bit is used to de-assert the level irq.

MMSS_RPM_IRQ_CLEAR

Bits	Name	Description
31:9	RESERVED	Reserved bits
8	CSIPHY2	clear for csiphy2
7	CSID2	clear for csid2
6	VFE	clear for vfe
5	JPEG	clear for peg
4	ISPIF	clear for ispif
3	CSID1	clear for csid1
2	CSID0	clear for csid0
1	CSIPHY1	clear for csiphy1
0	CSIPHY0	clear for csiphy0

0x040001B4 MMSS_DBG_CFG_REG_HS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DBG_CFG_REG is used for high speed clock debugging.

MMSS_DBG_CFG_REG_HS

Bits	Name	Description
31:7	RESERVED	Reserved bits

MMSS_DBG_CFG_REG_HS (cont.)

Bits	Name	Description
6:1	CLK_SEL	These bits are used to select the clk to be debugged. 0x0: cc_csi0_clk 0x1: cc_csi1_clk 0x2: cc_dsi1_clk 0x3: cc_dsi2_clk 0x4: cc_csi_vfe_clk 0x5: cc_ijpeg_clk 0x6: cc_vfe_clk 0x7: Reserved_07 0x8: Reserved_08 0x9: cc_gfx3d_clk 0xA: cc_jpegd_clk 0xB: cc_vcodec_clk 0xC: cc_axi_s0_clk 0xD: cc_axi_s1_clk 0xE: cc_axi_s2_clk 0xF: cc_fab_core_clk 0x10: cc_fab_msp_axi_clk 0x11: cc_gmem_axi_clk 0x12: cc_ijpeg_axi_clk 0x13: cc_imem_axi_clk 0x14: cc_jpegd_axi_clk 0x15: cc_mdp_axi_clk 0x16: cc_rot_axi_clk 0x17: cc_vcodec_axi_clk 0x18: cc_vfe_axi_clk 0x19: cc_vpe_axi_clk 0x1A: cc_mdp_clk 0x1B: cc_rot_clk 0x1C: cc_vpe_clk 0x1D: cc_hdmi_ref_clk 0x1E: cc_hdmi_tv_clk 0x1F: cc_mdp_tv_clk 0x20: cc_axi_s0_fclk 0x21: cc_axi_s1_fclk 0x22: cc_axi_s2_fclk 0x23: cc_axi_s3_fclk 0x24: cc_csiphy0_clk 0x25: cc_csiphy1_clk 0x26: cc_csi_pix_clk 0x27: cc_csi_rdi_clk 0x28: cc_lut_mdp_clk 0x29: cc_vcodec_A_axi_clk 0x2A: cc_vcodec_B_axi_clk 0x2B: cc_csiphy1_timer_clk 0x2C: cc_csiphy0_timer_clk

MMSS_DBG_CFG_REG_HS (cont.)

Bits	Name	Description
6:1	CLK_SEL (CONTINUED)	0x2D: cc_csi2_clk 0x2E: cc_csiphy2_clk 0x2F: cc_csiphy2_timer_clk 0x30: cc_csi_pix1_clk 0x31: cc_csi_rdi1_clk 0x32: cc_csi_rdi2_clk 0x33: cc_vcap_clk 0x34: cc_vcap_npl_clk 0x36: cc_vcap_axi_clk 0x37: cc_rgc_tv_clk 0x38: cc_npl_tv_clk 0x39: cc_gfx3d_axi_clk
0	DBG_CLK_EN	This bit enables the dbg_clk. 0x1: Enabled 0x0: Disabled

0x040001B8 MMSS_DBG_CFG_REG_LS

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The DBG_CFG_REG is used for low speed clock debugging.

MMSS_DBG_CFG_REG_LS

Bits	Name	Description
31:7	RESERVED	Reserved bits

MMSS_DBG_CFG_REG_LS (cont.)

Bits	Name	Description
6:1	CLK_SEL	These bits are used to select the clk to be debugged. 0x0: cc_dsi1_byte_clk 0x1: cc_dsi2_byte_clk 0x2: cc_camclk1_po 0x3: cc_mdp_dsi1_pclk 0x4: cc_dsi2_pclk 0x5: cc_vcodec_pclk 0x6: cc_amp_ahb_clk 0x7: cc_csi_ahb_clk 0x8: cc_dsi2_s_ahb_clk 0x9: cc_dsi1_m_ahb_clk 0xA: cc_dsi1_s_ahb_clk 0xB: cc_fab_ahb_clk 0xC: Reserved_0C 0xD: Reserved_0D 0xE: cc_gfx3d_ahb_clk 0xF: cc_hdmi_m_ahb_clk 0x10: cc_hdmi_s_ahb_clk 0x11: cc_ijpeg_ahb_clk 0x12: cc_imem_ahb_clk 0x13: cc_jpegd_ahb_clk 0x14: cc_mdp_ahb_clk 0x15: cc_mmss_fpb_clk 0x16: cc_rot_ahb_clk 0x17: cc_dsi1_esc_clk 0x18: cc_smmu_ahb_clk 0x19: Reversed_19 0x1A: cc_vcodec_ahb_clk 0x1B: cc_vfe_ahb_clk 0x1C: cc_vpe_ahb_clk 0x1D: cc_camclk0_po 0x1E: cc_dsi_ref_clk 0x1F: cc_hdmi_app_clk 0x20: cc_mdp_vsync_clk 0x21: Reserved_21 0x22: Reserved_22 0x23: cc_dsi2_esc_clk 0x24: cc_apu_ahb_clk 0x25: cc_mmss_fpb_always_on_clk 0x26: cc_dsi2_m_ahb_clk 0x27: cc_camclk2_po 0x28: cc_vcap_ahb_clk 0x29: cc_dsi2_mdp_pclk 0x2A: cc_lvdsphy_pixel_clk

MMSS_DBG_CFG_REG_LS (cont.)

Bits	Name	Description
0	DBG_CLK_EN	This bit enables the dbg_clk. 0x1: Enabled 0x0: Disabled

0x040001C0 MMSS_SPDM_CYC_CNT

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

MMSS_SPDM_CYC_CNT

Bits	Name	Description
31:14	RESERVED_1	Reserved bits
13	MDP_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
12	MDP_CLK_EN	This bit enables the CXC output. 0x1: Enabled 0x0: Disabled
11	DSI_PCLK_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
10	DSI_PCLK_CLK_EN	This bit enables the CXC output. 0x1: Enabled 0x0: Disabled
9	RESERVED_2	Removed feature for APQ8064.
8	RESERVED	Removed feature for APQ8064.
7	GFX3D_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
6	GFX3D_CLK_EN	This bit enables the CXC output. 0x1: Enabled 0x0: Disabled
5	FAB_AHB_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
4	FAB_AHB_CLK_EN	This bit enables the CXC output. 0x1: Enabled 0x0: Disabled

MMSS_SPDM_CYC_CNT (cont.)

Bits	Name	Description
3	FAB_CORE_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
2	FAB_CORE_CLK_EN	This bit enables the CXC output. 0x1: Enabled 0x0: Disabled
1	VCODEC_CLK_INV	This bit inverts the clock at output of CXC. 0x1: Inverted 0x0: Not inverted
0	VCODEC_CLK_EN	This bit enables the CXC output. 0x1: Enabled 0x0: Disabled

0x040001C4 MMSS_DBG_BUS_CFG_REG

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_BUS_CFG_REG

Bits	Name	Description
31:4	RESERVED	Reserved bits
3:0	BUS_SEL	Debug bus select 0x0: disabled 0x1: vec_a 0x2: vec_b 0x3: vec_c 0x4: vec_d 0x5: vec_e 0x6: vec_f 0x7: vec_g 0x8: vec_h 0x9: vec_i 0xA: vec_def 0xB: vec_j 0xC: vec_k

0x040001C8 MMSS_DBG_BUS_VEC_A

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_BUS_VEC_A

Bits	Name	Description
31	RESERVED_1	Reserved bit
30	MDP0_AXI_CLKON	Read back register for mdp0_axi_clkon
29	MDP1_AXI_CLKON	Read back register for mdp1_axi_clkon
28	VPE_CLK_OFF	Read back register for vpe_clk_off
27	VPE_CLKON	Read back register for vpe_clkon
26	VPE_CLK_SLP_NRET_N	Read back register for vpe_clk_slp_nret_n
25	VPE_CLK_SLP_RET_N	Read back register for vpe_clk_slp_ret_n
24	IJPEG_CLK_OFF	Read back register for ijpeg_clk_off
23	IJPEG_DISABLE	Read back register for ijpeg_disable
22	IJPEG_CLKON	Read back register for ijpeg_clkon
21	IJPEG_CLK_SLP_NRET_N	Read back register for ijpeg_clk_slp_nret_n
20	IJPEG_CLK_SLP_RET_N	Read back register for ijpeg_clk_slp_ret_n
19	JPEGD_CLK_OFF	Read back register for jpegd_clk_off
18	JPEGD_DISABLE	Read back register for jpegd_disable
17	JPEGD_CLKON	Read back register for jpegd_clkon
16	JPEGD_CLK_SLP_NRET_N	Read back register for jpegd_clk_slp_nret_n
15	JPEGD_CLK_SLP_RET_N	Read back register for jpegd_clk_slp_ret_n
14	RESERVED_2	Removed for APQ8064.
13	RESERVED_3	Removed for APQ8064.
12	RESERVED_4	Removed for APQ8064.
11	RESERVED_5	Removed for APQ8064.
10	RESERVED_6	Removed for APQ8064.
9	RESERVED_7	Removed for APQ8064.
8	RESERVED_8	Removed for APQ8064.
7	RESERVED_9	Removed for APQ8064.
6	RESERVED_10	Removed for APQ8064.
5	RESERVED	Removed for APQ8064.
4	GFX3D_CLK_OFF	Read back register for gfx3d_clk_off

MMSS_DBG_BUS_VEC_A (cont.)

Bits	Name	Description
3	GRP_3D_DISABLE	Read back register for grp_3d_disable
2	GFX3D_CLKON	Read back register for gfx3d_clkon
1	GFX3D_CLK_SLP_NRET_N	Read back register for gfx3d_clk_slp_nret_n
0	GFX3D_CLK_SLP_RET_N	Read back register for gfx3d_clk_slp_ret_n

0x040001CC MMSS_DBG_BUS_VEC_B

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_BUS_VEC_B

Bits	Name	Description
31	CSI_VFE_CLK_SLP_NRET_N	Read back register for csi_vfe_clk_slp_nret_n
30	CSI_VFE_CLK_SLP_RET_N	Read back register for csi_vfe_clk_slp_ret_n
29	CSI2_CLK_OFF	Read back register for csi2_clk_off
28	CSI_2_DISABLE	Read back register for csi_2_disable
27	CSI2_CLKON	Read back register for csi2_clkon
26	DSI2_BYTE_CLK_SLP_RET_N	Read back register for dsi2_byte_clk_slp_ret_n
25	HDMI_APP_CLK_OFF	Read back register for hdmi_app_clk_off
24	DSI1_BYTE_CLKON	Read back register for dsi1_byte_clkon
23	DSI2_BYTE_CLKON	Read back register for dsi2_byte_clkon
22	MDP_VSYNC_CLK_OFF	Read back register for mdp_vsync_clk_off
21	DSI1_BYTE_CLK_OFF	Read back register for dsi1_byte_clk_off
20	DSI2_BYTE_CLK_OFF	Read back register for dsi2_byte_clk_off
19	DSI2_BYTE_CLK_SLP_NRET_N	Read back register for dsi2_byte_clk_slp_nret_n
18	MDP_VSYNC_CLKON	Read back register for mdp_vsync_clkon
17	HDMI_APP_CLKON	Read back register for hdmi_app_clkon
16	DSI1_BYTE_CLK_SLP_RET_N	Read back register for dsi1_byte_clk_slp_ret_n
15	DSI1_BYTE_CLK_SLP_NRET_N	Read back register for dsi1_byte_clk_slp_nret_n
14	CSI1_CLK_OFF	Read back register for csi1_clk_off
13	CSI0_CLK_OFF	Read back register for csi0_clk_off
12	CSI_1_DISABLE	Read back register for csi_1_disable

MMSS_DBG_BUS_VEC_B (cont.)

Bits	Name	Description
11	CSI1_CLKON	Read back register for csi1_clkon
10	CSI_0_DISABLE	Read back register for csi_0_disable
9	CSI0_CLKON	Read back register for csi0_clkon
8	CSI_VFE_CLK_OFF	Read back register for csi1_vfe_clk_off
7	SMU_VPE_AHB_CLKON	Read back register for smu_vpe_ahb_clkon
6	VFE_CLK_OFF	Read back register for vfe_clk_off
5	VFE_DISABLE	Read back register for vfe_disable
4	CSI_VFE_CLKON	Read back register for csi1_vfe_clkon
3	SMU_GFX3D_AHB_CLKON	Read back register for smu_gfx3d_ahb_clkon
2	VFE_CLKON	Read back register for vfe_clkon
1	VFE_CLK_SLP_NRET_N	Read back register for vfe_clk_slp_nret_n
0	VFE_CLK_SLP_RET_N	Read back register for vfe_clk_slp_ret_n

0x040001D0 MMSS_DBG_BUS_VEC_C

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_BUS_VEC_C

Bits	Name	Description
31	RESERVED_1	Reserved bits
30	CSIPHY2_CLKON	Readback register for csiphy2_clkon
29	VCODEC_CLK_OFF	Read back register for vcodec_clk_off
28	VCODEC_PCLKON	Read back register for vcodec_pclkon
27	VCODEC_CLKON	Read back register for vcodec_clkon
26	MFC_DISABLE_CODEC	Read back register for mfc_disable_codec
25	VCODEC_CLK_SLP_NRET_N	Read back register for vcodec_clk_slp_nret_n
24	VCODEC_CLK_SLP_RET_N	Read back register for vcodec_clk_slp_ret_n
23	VCODEC_PCLK_OFF	Read back register for vcodec_pclk_off
22	DSI2_CLKON	Read back register for dsi2_clkon
21	DSI2_DISABLE	Read back register for dsi2_disable
20	DSI2_CLK_OFF	Read back register for dsi2_clk_off

MMSS_DBG_BUS_VEC_C (cont.)

Bits	Name	Description
19	DSI2_PIXEL_CLK_OFF	Read back register for dsi2_pixel_clk_off
18	RESERVED_2	Removed for APQ8064
17	RESERVED	Removed for APQ8064
16	DSI2_PCLKON	Read back register for dsi2_pclkon
15	ROT_CLK_OFF	Read back register for rot_clk_off
14	ROT_DISABLE	Read back register for rot_disable
13	ROT_CLKON	Read back register for rot_clkon
12	ROT_CLK_SLP_NRET_N	Read back register for rot_clk_slp_nret_n
11	ROT_CLK_SLP_RET_N	Read back register for rot_clk_slp_ret_n
10	MDP_CLK_OFF	Read back register for mdp_clk_off
9	MDP_CLKON	Read back register for mdp_clkon
8	MDP_CLK_SLP_NRET_N	Read back register for mdp_clk_slp_nret_n
7	MDP_CLK_SLP_RET_N	Read back register for mdp_clk_slp_ret_n
6	DSI1_PIXEL_CLK_OFF	Read back register for dsi1_pixel_clk_off
5	DSI1_PCLKON	Read back register for dsi1_pclkon
4	MDP_DSI1_PCLK_SLP_NRET_N	Read back register for mdp_dsi1_pclk_slp_nret_n
3	MDP_DSI1_PCLK_SLP_RET_N	Read back register for mdp_dsi1_pclk_slp_ret_n
2	DSI1_CLK_OFF	Read back register for dsi1_clk_off
1	DSI1_DISABLE	Read back register for dsi1_disable
0	DSI1_CLKON	Read back register for dsi1_clkon

0x040001D4 MMSS_DBG_BUS_VEC_D

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_BUS_VEC_D

Bits	Name	Description
31	RESERVED_1	Reserved bit
30	RESERVED_2	Reserved bit
29	ROT_GDFS_EN1	Read back register for rot_gdfs_en1
28	GEMINI_GDFS_EN_ALL	Read back register for gemini_gdfs_en_all

MMSS_DBG_BUS_VEC_D (cont.)

Bits	Name	Description
27	GEMINI_GDFS_EN1	Read back register for gemini_gdfs_en1
26	VPE_GDFS_EN_ALL	Read back register for vpe_gdfs_en_all
25	VPE_GDFS_EN1	Read back register for vpe_gdfs_en1
24	GFX3D_GDFS_EN_ALL	Read back register for gfx3d_gdfs_en_all
23	GFX3D_GDFS_EN1	Read back register for gfx3d_gdfs_en1
22	MDP_GDFS_EN_ALL	Read back register for mdp_gdfs_en_all
21	MDP_GDFS_EN1	Read back register for mdp_gdfs_en1
20	VED_GDFS_EN_ALL	Read back register for ved_gdfs_en_all
19	VED_GDFS_EN1	Read back register for ved_gdfs_en1
18	GFX2D1_GDFS_EN_ALL	Read back register for gfx2d1_gdfs_en_all
17	GFX2D1_GDFS_EN1	Read back register for gfx2d1_gdfs_en1
16	GFX2D0_GDFS_EN_ALL	Read back register for gfx2d0_gdfs_en_all
15	GFX2D0_GDFS_EN1	Read back register for gfx2d0_gdfs_en1
14	VFE_GDFS_EN_ALL	Read back register for vfe_gdfs_en_all
13	VFE_GDFS_EN1	Read back register for vfe_gdfs_en1
12	MDP_TV_CLK_OFF	Read back register for mdp_tv_clk_off
11	HDMI_TV_CLK_OFF	Read back register for hdmi_tv_clk_off
10	RESERVED_3	Removed for APQ8064.
9	RESERVED_4	Removed for APQ8064
8	MDP_TV_CLKON	Read back register for mdp_tv_clkon
7	HDMI_TV_CLKON	Read back register for hdmi_tv_clkon
6	RESERVED_5	Removed for APQ8064
5	RESERVED_6	Removed for APQ8064.
4	MDP_TV_CLK_SLP_NRET_N	Read back register for mdp_tv_clk_slp_nret_n
3	MDP_TV_CLK_SLP_RET_N	Read back register for mdp_tv_clk_slp_ret_n
2	RESERVED_7	Removed for APQ8064.
1	RESERVED_8	Removed for APQ8064.
0	ROT_GDFS_EN_ALL	Read back register for rot_gdfs_en_all

0x040001D8 MMSS_DBG_BUS_VEC_E

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_BUS_VEC_E

Bits	Name	Description
31:29	RESERVED	Reserved
28	MDP_AXI_CLK_SLP_NRET_N	Read back register for mdp_axi_clk_slp_nret_n
27	MDP_AXI_CLK_SLP_RET_N	Read back register for mdp_axi_clk_slp_ret_n
26	VPE_AXI_CLK_SLP_NRET_N	Read back register for vpe_axi_clk_slp_nret_n
25	VPE_AXI_CLK_SLP_RET_N	Read back register for vpe_axi_clk_slp_ret_n
24	ROT_AXI_CLK_SLP_NRET_N	Read back register for rot_axi_clk_slp_nret_n
23	ROT_AXI_CLK_SLP_RET_N	Read back register for rot_axi_clk_slp_ret_n
22	GMEM_AXI_SLP_NRET_N	Read back register for gmem_axi_slp_nret_n
21	GMEM_AXI_SLP_RET_N	Read back register for gmem_axi_slp_ret_n
20	IMEM_AXI_SLP_NRET_N	Read back register for imem_axi_slp_nret_n
19	IMEM_AXI_SLP_RET_N	Read back register for imem_axi_slp_ret_n
18	DSI2_M_AHB_CLK_OFF	Read back register for dsi2_m_ahb_clk_off
17	FAB_CORE_CLK_OFF	Read back register for fab_core_clk_off
16	AXI_S3_FCLK_CLK_OFF	Removed for APQ8064.
15	AXI_S2_FCLK_CLK_OFF	Read back register for axi_s2_fclk_clk_off
14	AXI_S1_FCLK_CLK_OFF	Read back register for axi_s1_fclk_clk_off
13	AXI_S0_FCLK_CLK_OFF	Read back register for axi_s0_fclk_clk_off
12	AXI_S2_CLK_OFF	Read back register for axi_s2_clk_off
11	AXI_S1_CLK_OFF	Read back register for axi_s1_clk_off
10	AXI_S0_CLK_OFF	Removed for APQ8064.
9	FAB_MSP_AXI_CLK_OFF	Read back register for fab_msp_axi_clk_off
8	MDP_AXI_CLK_OFF	Read back register for mdp_axi_clk_off
7	IMEM_AXI_CLK_OFF	Read back register for imem_axi_clk_off
6	GMEM_AXI_CLK_OFF	Read back register for gmem_axi_clk_off
5	JPEGD_AXI_CLK_OFF	Read back register for jpegd_axi_clk_off

MMSS_DBG_BUS_VEC_E (cont.)

Bits	Name	Description
4	IJPEG_AXI_CLK_OFF	Read back register for ijpeg_axi_clk_off
3	VCODEC_AXI_CLK_OFF	Read back register for vcodec_axi_clk_off
2	ROT_AXI_CLK_OFF	Read back register for rot_axi_clk_off
1	VPE_AXI_CLK_OFF	Read back register for vpe_axi_clk_off
0	VFE_AXI_CLK_OFF	Read back register for vfe_axi_clk_off

0x040001DC MMSS_DBG_BUS_VEC_F

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_BUS_VEC_F

Bits	Name	Description
31	RESERVED_1	reserved
30	SMU_ROT_AHB_CLKON	Read back register for smu_rot_ahb_clkon
29	FAB_JPEGD_AXI_CLKON	Read back register for fab_jpegd_axi_clkon
28	FAB_ROT_AXI_CLKON	Read back register for fab_rot_axi_clkon
27	FAB_MSP_AXI_CLKON	Read back register for fab_msp_axi_clkon
26	FAB_IJPEG_AXI_CLKON	Read back register for fab_ijpeg_axi_clkon
25	VFE_AHB_CLK_SLP_RET_N	Read back register for vfe_ahb_clk_slp_ret_n
24	VFE_AHB_CLK_SLP_NRET_N	Read back register for vfe_ahb_clk_slp_nret_n
23	RESERVED_2	Removed for APQ8064.
22	SMMU_AHB_CLK_OFF	Read back register for smmu_ahb_clk_off
21	DSI1_S_AHB_CLK_OFF	Read back register for dsi1_s_ahb_clk_off
20	DSI2_S_AHB_CLK_OFF	Read back register for dsi2_s_ahb_clk_off
19	DSI1_M_AHB_CLK_OFF	Read back register for dsi1_m_ahb_clk_off
18	AMP_AHB_CLK_OFF	Read back register for amp_ahb_clk_off
17	SMU_VFE_AHB_CLKON	Read back register for smu_vfe_ahb_clkon
16	CSI_AHB_CLK_OFF	Read back register for csi_ahb_clk_off
15	VPE_AHB_CLK_OFF	Read back register for vpe_ahb_clk_off
14	VFE_AHB_CLK_OFF	Read back register for vfe_ahb_clk_off

MMSS_DBG_BUS_VEC_F (cont.)

Bits	Name	Description
13	ROT_AHB_CLK_OFF	Read back register for rot_ahb_clk_off
12	VCODEC_AHB_CLK_OFF	Read back register for vcodec_ahb_clk_off
11	MDP_AHB_CLK_OFF	Read back register for mdp_ahb_clk_off
10	IMEM_AHB_CLK_OFF	Read back register for imem_ahb_clk_off
9	IJPEG_AHB_CLK_OFF	Read back register for ijpeg_ahb_clk_off
8	APU_AHB_CLK_OFF	Read back register for apu_ahb_clk_off
7	JPEGD_AHB_CLK_OFF	Read back register for jpegd_ahb_clk_off
6	HDMI_S_AHB_CLK_OFF	Read back register for hdmi_s_ahb_clk_off
5	HDMI_M_AHB_CLK_OFF	Read back register for hdmi_m_ahb_clk_off
4	GFX3D_AHB_CLK_OFF	Read back register for gfx3d_ahb_clk_off
3	RESERVED_3	Removed for APQ8064.
2	RESERVED_4	Removed for APQ8064.
1	FAB_AHB_CLK_OFF	Read back register for fab_ahb_clk_off
0	MMSS_FPB_CLK_OFF	Read back register for mmss_fpb_clk_off

0x040001E0 MMSS_DBG_BUS_VEC_G

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_BUS_VEC_G

Bits	Name	Description
31	RESERVED	Reserved
30	IJPEG_AXI_CLKON	Read back register for ijpeg_axi_clkon
29	VFE_AXI_CLKON	Read back register for vfe_axi_clkon
28	VPE_AXI_CLKON	Read back register for vpe_axi_clkon
27	ROT_AXI_CLKON	Read back register for rot_axi_clkon
26	VCODEC_AXI_CLKON	Read back register for vcodec_axi_clkon
25	GMEM_AXI_CLKON	Read back register for gmem_axi_clkon
24	IMEM_AXI_CLKON	Read back register for imem_axi_clkon
23	FAB_MDP_AXI1_CLKON	Read back register for fab_mdp_axi1_clkon
22	FAB_CORE_CLKON	Read back register for fab_core_clkon

MMSS_DBG_BUS_VEC_G (cont.)

Bits	Name	Description
21	AXI_S0_CLKON	Removed for APQ8064.
20	AXI_S1_CLKON	Read back register for axi_s1_clkon
19	AXI_S2_CLKON	Read back register for axi_s2_clkon
18	FAB_S0_CLKON	Read back register for fab_s0_clkon
17	FAB_S1_CLKON	Read back register for fab_s1_clkon
16	FAB_S2_CLKON	Read back register for fab_s2_clkon
15	FAB_S3_CLKON	Removed for APQ8064.
14	SMU_IJPEG_AXI_CLKON	Read back register for smu_ijpeg_axi_clkon
13	SMU_JPEGD_AXI_CLKON	Read back register for smu_jpegd_axi_clkon
12	SMU_MDP0_AXI_CLKON	Read back register for smu_mdp0_axi_clkon
11	SMU_MDP1_AXI_CLKON	Read back register for smu_mdp1_axi_clkon
10	SMU_VCODEC_A_AXI_CLKON	Read back register for smu_vcodec_a_axi_clkon
9	SMU_VCODEC_B_AXI_CLKON	Read back register for smu_vcodec_b_axi_clkon
8	SMU_ROT_AXI_CLKON	Read back register for smu_rot_axi_clkon
7	SMU_VFE_AXI_CLKON	Read back register for smu_vfe_axi_clkon
6	SMU_VPE_AXI_CLKON	Read back register for smu_vpe_axi_clkon
5	FAB_MDP_AXI0_CLKON	Read back register for fab_mdp_axi0_clkon
4	FAB_VCODEC_AXI0_CLKON	Read back register for fab_vcodec_axi0_clkon
3	FAB_VCODEC_AXI1_CLKON	Read back register for fab_vcodec_axi1_clkon
2	FAB_VFE_AXI_CLKON	Read back register for fab_vfe_axi_clkon
1	FAB_VPE_AXI_CLKON	Read back register for fab_vpe_axi_clkon
0	JPEGD_AXI_CLKON	Read back register for jpegd_axi_clkon

0x040001E4 MMSS_DBG_BUS_VEC_H

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_BUS_VEC_H

Bits	Name	Description
31	RESERVED_1	Reserved
30	FAB_AHB_CLKON	Read back register for fab_ahb_clkon
29	HDMI_M_AHB_CLKON	Read back register for hdmi_m_ahb_clkon
28	HDMI_S_AHB_CLKON	Read back register for hdmi_s_ahb_clkon
27	VFE_AHB_CLKON	Read back register for vfe_ahb_clkon
26	VPE_AHB_CLKON	Read back register for vpe_ahb_clkon
25	ROT_AHB_CLKON	Read back register for rot_ahb_clkon
24	VCODEC_AHB_CLKON	Read back register for vcodec_ahb_clkon
23	GFX3D_AHB_CLKON	Read back register for gfx3d_ahb_clkon
22	RESERVED_2	Removed for APQ8064.
21	RESERVED_3	Removed for APQ8064.
20	JPEGD_AHB_CLKON	Read back register for jpegd_ahb_clkon
19	APU_AHB_CLKON	Read back register for apu_ahb_clkon
18	IJPEG_AHB_CLKON	Read back register for ijpeg_ahb_clkon
17	IMEM_AHB_CLKON	Read back register for imem_ahb_clkon
16	MDP_AHB_CLKON	Read back register for mdp_ahb_clkon
15	DSI2_S_AHB_CLKON	Read back register for dsi2_s_ahb_clkon
14	CSI_AHB_CLKON	Read back register for csi_ahb_clkon
13	MMSS_FPB_ALWAYS_ON_CLK_OFF	Read back register for mmss_fpb_always_on_clk_off
12	AMP_AHB_CLKON	Read back register for amp_ahb_clkon
11	DSI1_M_AHB_CLKON	Read back register for dsi1_m_ahb_clkon
10	DSI1_S_AHB_CLKON	Read back register for dsi1_s_ahb_clkon
9	SMMU_AHB_CLKON	Read back register for smmu_ahb_clkon
8	RESERVED_4	Removed for APQ8064
7	RESERVED_5	Removed for APQ8064.
6	RESERVED_6	Removed for APQ8064.
5	SMU_IJPEG_AHB_CLKON	Read back register for smu_ijpeg_ahb_clkon
4	SMU_JPEGD_AHB_CLKON	Read back register for smu_jpegd_ahb_clkon
3	SMU_MDP0_AHB_CLKON	Read back register for smu_mdp0_ahb_clkon
2	SMU_MDP1_AHB_CLKON	Read back register for smu_mdp1_ahb_clkon

MMSS_DBG_BUS_VEC_H (cont.)

Bits	Name	Description
1	SMU_VCODEC_A_AHB_CLKON	Read back register for smu_vcodec_a_ahb_clkon
0	SMU_VCODEC_B_AHB_CLKON	Read back register for smu_vcodec_b_ahb_clkon

0x040001E8 MMSS_DBG_BUS_VEC_I

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_BUS_VEC_I

Bits	Name	Description
31	CAMCLK2_PO_CLK_OFF	Read back register for camclk2_po_clk_off
30	CSI2PHYTIMER_CLKOFF	Read back register for csi2phytimer_clkoff
29	CSIPHY2_CLK_OFF	Read back register for csiphy2_clk_off
28	VCODEC_AXI_B_SLP_NRET_N	Read back register for vcodec_axi_B_slp_nret_n
27	VCODEC_AXI_B_SLP_RET_N	Read back register for vcodec_axi_B_slp_ret_n
26	VCODEC_AXI_A_CLK_OFF	Read back register for vcodec_axi_A_clkoff
25	VCODEC_AXI_B_CLK_OFF	Read back register for vcodec_axi_B_clkoff
24	VCODEC_AXI_A_CLKON	Read back register for vcodec_axi_A_clkon
23	VCODEC_AXI_B_CLKON	Read back register for vcodec_axi_B_clkon
22	CSI1_RDI_CLKOFF	Read back register for csi1_rdi_clkoff
21	CSI0_RDI_CLKOFF	Read back register for csi0_rdi_clkoff
20	CSI1_PIX_CLKOFF	Read back register for csi1_pix_clkoff
19	CSI0_PIX_CLKOFF	Read back register for csi0_pix_clkoff
18	CSI1PHYTIMER_CLKOFF	Read back register for csi1phytimer_clkoff
17	CSI0PHYTIMER_CLKOFF	Read back register for csi0phytimer_clkoff
16	CAMCLK1_PO_CLK_OFF	Read back register for camclk1_po_clk_off
15	CAMCLK0_PO_CLK_OFF	Read back register for camclk0_po_clk_off
14	LUT_MDP_CLKON	Read back register for lut_mdp_clkon
13	LUT_MDP_CLK_OFF	Read back register for lut_mdp_clk_off
12	LUT_MDP_CLK_SLP_RET_N	Read back register for lut_mdp_clk_slp_ret_n

MMSS_DBG_BUS_VEC_I (cont.)

Bits	Name	Description
11	LUT_MDP_CLK_SLP_NRET_N	Read back register for lut_mdp_clk_slp_nret_n
10	CSIPHY1_CLK_OFF	Read back register for csiphy1_clk_off
9	CSIPHY0_CLK_OFF	Read back register for csiphy0_clk_off
8	VCODEC_AXI_A_SLP_RET_N	Read back register for vcodec_axi_A_slp_ret_n
7	CSIPHY1_CLKON	Read back register for csiphy1_clkon
6	VCODEC_AXI_A_SLP_NRET_N	Read back register for vcodec_axi_A_slp_nret_n
5	CSIPHY0_CLKON	Read back register for csiphy0_clkon
4	DSI2_M_AHB_CLKON	Read back register for dsi2_m_ahb_clkon
3	DSI2_ESC_CLK_OFF	Read register for dsi2_esc_clk_offr
2	DSI2_ESC_CLKON	Read register for dsi2_esc_clkon
1	DSI1_ESC_CLK_OFF	Read register for dsi1_esc_clk_offr
0	DSI1_ESC_CLKON	Read register for dsi1_esc_clkon

0x04000240 MMSS_DBG_BUS_VEC_J

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_BUS_VEC_J

Bits	Name	Description
30	GFX3D_AXI_CLK_OFF	Read back debug register
29	SMU_GFX3D_AXI_CLKON	Read back debug register
28	GFX3D_AXI_CLKON	Read back debug register
27	RGB_TV_CLK_OFF	Read back debug register
26	NPL_TV_CLK_OFF	Read back debug register
25	VCAP_NPL_CLK_OFF	Read back debug register
24	VCAP_AXI_CLKON	Read back debug register
23	VCAP_AHB_CLK_OFF	Read back debug register
22	SMU_VCAP_AHB_CLKON	Read back debug register
21	VCAP_AHB_CLKON	Read back debug register
20	VCAP_AXI_CLK_OFF	Read back debug register

MMSS_DBG_BUS_VEC_J (cont.)

Bits	Name	Description
19	SMU_VCAP_AXI_CLKON	Read back debug register
18	FAB_VCAP_AXI_CLKON	Read back debug register
17	VCAP_CLK_SLP_NRET_N	Read back debug register
16	VCAP_CLK_SLP_RET_N	Read back debug register
15	VCAP_CLK_OFF	Read back debug register
14	VCAP_CLKON	Read back debug register
13	VCAP_NPL_CLKON	Read back debug register
12	VCAP_GDFS_EN_ALL	Read back debug register
11	VCAP_GDFS_EN1	Read back debug register
10	CSI0_RDI2_CLKOFF	Read back debug register
9	CSI1_RDI2_CLKOFF	Read back debug register
8	CSI2_RDI2_CLKOFF	Read back debug register
7	CSI0_RDI1_CLKOFF	Read back debug register
6	CSI1_RDI1_CLKOFF	Read back debug register
5	CSI2_RDI1_CLKOFF	Read back debug register
4	CSI0_PIX1_CLKOFF	Read back debug register
3	CSI1_PIX1_CLKOFF	Read back debug register
2	CSI2_PIX1_CLKOFF	Read back debug register
1	CSI2_RDI_CLKOFF	Read back debug register
0	CSI2_PIX_CLKOFF	Read back debug register

0x0400024C MMSS_DBG_BUS_VEC_K

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_BUS_VEC_K

Bits	Name	Description
9	SMU_GFX3D1_AXI_CLKON	Read back debug register
8	SMU_GFX3D1_AHB_CLKON	Read back debug register
7	MDP_P2CLK_OFF	Read back debug register
6	LVDS_CLK_OFF	Read back debug register

MMSS_DBG_BUS_VEC_K (cont.)

Bits	Name	Description
5	LVDSPHY_CLKON	Read back debug register
4	MDP_P2CLKON	Read back debug register
3	GFX3D_AXI_SLP_NRET_N	Read back debug register
2	GFX3D_AXI_SLP_RET_N	Read back debug register
1	VCAP_AXI_SLP_NRET_N	Read back debug register
0	VCAP_AXI_SLP_RET_N	Read back debug register

0x04000268 MMSS_DBG_OXILI

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

MMSS_DBG_OXILI

Bits	Name	Description
31:0	DBG_BITS	Read Only registers for Oxili debug purpose

0x0400026C MMSS_CMD_REG_OXILI

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

MMSS_CMD_REG_OXILI

Bits	Name	Description
31:0	CMD_REG_BITS	Command registers for Oxili debug purpose

0x040001F4 MMSS_DBG_BUS_VEC_DEF

Type: Read Only
Clock: AHB_CLK
Reset State: 0xABCDABCD

MMSS_DBG_BUS_VEC_DEF

Bits	Name	Description
31:0	DEFAULT_DBG_BITS	These are default debug bus bits, set to 0xABCDABCD

0x040001F0 MMSS_FPB_EN

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

This register space is used for fpb always on clock enabling only. Do not use for any other purpose. The fpb always on clock should always be defaulted to enable; if disabled, it may not recover, thus this bit is used only for static power testing purpose.

MMSS_FPB_EN

Bits	Name	Description
0	FPB_ALWAYS_ON_CLK_EN	Caution: This register will disable the fpb_always_on clock and not recoverable. Do not set it to 0x1, unless for power or leakage testing purpose. 0x0: Enable 0x1: Disable

0x040001F8 MMSS_MMSS_COMPILEMEM_ACC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

MMSS_MMSS_COMPILEMEM_ACC

Bits	Name	Description
31:24	RESERVED_BIT31_24	Reserved bits
23:20	SPLRF240	Compiler regfile
19:16	STDSP155	Compiler single port RAM
15:12	LLRF240	Compiler regfile
11:8	STDVROM	Compiler ROM
7:4	LLPDP155	Compiler pseudo dual port RAM
3:0	LLSP155	Compiler single port RAM

0x040001FC MMSS_MMSS_CUSTOMMEM_ACC

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

MMSS_MMSS_CUSTOMMEM_ACC

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:8	HPIMEM	Custom RAM
7:0	RF8441	Custom regfile

0x040001BC MMSS_MMSS_CUSTOMMEM_ARRSTBYN

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x1

MMSS_MMSS_CUSTOMMEM_ARRSTBYN

Bits	Name	Description
0	IMEM	Array standby bit for MMSS IMEM custom memory. This is an active low signal; Default is 0x1

0x04000204 MMSS_SW_RESET_ALL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The SW_RESET_ALL register is used to reset most clock branches.

MMSS_SW_RESET_ALL

Bits	Name	Description
0	SW_RESET_ALL	Setting (1) this bit has the same function as setting all bits in the SW_RESET: 0x0: Not Active 0x1: Active

0x04000208 MMSS_SW_RESET_AXI

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0003FFFF

The SW_RESET_AXI register controls the individual resets to all blocks.

MMSS_SW_RESET_AXI

Bits	Name	Description
31:18	RESERVED	Reserved bits
17	GFX3D_AXI	The reset bit 0x0: Not Active 0x1: Active
16	VCAP_AXI	The reset bit 0x0: Not Active 0x1: Active
15	VPE_AXI	The reset bit 0x0: Not Active 0x1: Active
14	IJPEG_AXI	The reset bit 0x0: Not Active 0x1: Active
13	MDP_AXI	The reset bit 0x0: Not Active 0x1: Active
9	VFE_AXI	The reset bit 0x0: Not Active 0x1: Active
8	SP_AXI	The reset bit 0x0: Not Active 0x1: Active
7	VCODEC_AXI	The reset bit 0x0: Not Active 0x1: Active
6	ROT_AXI	The reset bit 0x0: Not Active 0x1: Active
5	VCODEC_AXI_A	The reset bit 0x0: Not Active 0x1: Active
4	VCODEC_AXI_B	The reset bit 0x0: Not Active 0x1: Active
3	FAB_S3_AXI	The reset bit 0x0: Not Active 0x1: Active

MMSS_SW_RESET_AXI (cont.)

Bits	Name	Description
2	FAB_S2_AXI	The reset bit 0x0: Not Active 0x1: Active
1	FAB_S1_AXI	The reset bit 0x0: Not Active 0x1: Active
0	FAB_S0_AXI	The reset bit 0x0: Not Active 0x1: Active

0x0400020C MMSS_SW_RESET_AHB

Type: Write/Read
Clock: AHB_CLK
Reset State: 0xFFFFFFFF

The SW_RESET_AHB register controls the individual resets to all blocks.

MMSS_SW_RESET_AHB

Bits	Name	Description
31	SMMU_GFX3D_AHB	The reset bit 0x0: Not Active 0x1: Active
30	SMMU_VPE_AHB	The reset bit 0x0: Not Active 0x1: Active
29	SMMU_VFE_AHB	The reset bit 0x0: Not Active 0x1: Active
28	SMMU_ROT_AHB	The reset bit 0x0: Not Active 0x1: Active
27	SMMU_VCODEC_B_AHB	The reset bit 0x0: Not Active 0x1: Active
26	SMMU_VCODEC_A_AHB	The reset bit 0x0: Not Active 0x1: Active

MMSS_SW_RESET_AHB (cont.)

Bits	Name	Description
25	SMMU_MDP1_AHB	The reset bit 0x0: Not Active 0x1: Active
24	SMMU_MDP0_AHB	The reset bit 0x0: Not Active 0x1: Active
23	SMMU_JPEGD_AHB	The reset bit 0x0: Not Active 0x1: Active
22	SMMU_IJPEG_AHB	The reset bit 0x0: Not Active 0x1: Active
21	RESERVED_1	Removed for APQ8064
20	REVERSED	Removed for APQ8064
19	RESERVED_2	Do not use for APQ8064. (previously used for SMI0_AHB)
18	APU_AHB	The reset bit 0x0: Not Active 0x1: Active
17	CSI_AHB	The reset bit 0x0: Not Active 0x1: Active
16	RESERVED_3	Do not use for APQ8064 (previously used for CSI1_AHB)
15	RESERVED_4	Removed for APQ8064.
14	VPE_AHB	The reset bit 0x0: Not Active 0x1: Active
13	FABRIC_AHB	The reset bit 0x0: Not Active 0x1: Active
12	RESERVED_5	Removed for APQ8064
11	RESERVED_6	Removed for APQ8064
10	GFX3D_AHB	The reset bit 0x0: Not Active 0x1: Active
9	HDMI_AHB	The reset bit 0x0: Not Active 0x1: Active

MMSS_SW_RESET_AHB (cont.)

Bits	Name	Description
8	IMEM_AHB	The reset bit 0x0: Not Active 0x1: Active
7	IJPEG_AHB	The reset bit 0x0: Not Active 0x1: Active
6	DSI_M_AHB	The reset bit 0x0: Not Active 0x1: Active
5	DSI_S_AHB	The reset bit 0x0: Not Active 0x1: Active
4	JPEGD_AHB	The reset bit 0x0: Not Active 0x1: Active
3	MDP_AHB	The reset bit 0x0: Not Active 0x1: Active
2	ROT_AHB	The reset bit 0x0: Not Active 0x1: Active
1	VCODEC_AHB	The reset bit 0x0: Not Active 0x1: Active
0	VFE_AHB	The reset bit 0x0: Not Active 0x1: Active

0x04000200 MMSS_SW_RESET_AHB2

Type: Write/Read
Clock: AHB_CLK
Reset State: 0xF

The SW_RESET_AHB register controls the individual resets to all blocks.

MMSS_SW_RESET_AHB2

Bits	Name	Description
3	SMMU_VCAP_AHB	The reset bit 0x0: Not Active 0x1: Active
2	VCAP_AHB	The reset bit 0x0: Not Active 0x1: Active
1	DSI2_M_AHB	The reset bit 0x0: Not Active 0x1: Active
0	DSI2_S_AHB	The reset bit 0x0: Not Active 0x1: Active

0x04000210 MMSS_SW_RESET_CORE

Type: Write/Read
Clock: AHB_CLK
Reset State: 0xFFFFFFFF

The SW_RESET_CORE register controls the individual resets to all blocks.

MMSS_SW_RESET_CORE

Bits	Name	Description
31	CSIPHY2_CLK	The reset bit 0x0: Not Active 0x1: Active
30	CSI_PIX1_CLK	The reset bit 0x0: Not Active 0x1: Active
29	CSIPHY0_CLK	The reset bit 0x0: Not Active 0x1: Active
28	CSIPHY1_CLK	The reset bit 0x0: Not Active 0x1: Active
27	CSI_RDI_CLK	The reset bit 0x0: Not Active 0x1: Active

MMSS_SW_RESET_CORE (cont.)

Bits	Name	Description
26	CSI_PIX_CLK	The reset bit 0x0: Not Active 0x1: Active
25	DSI2_CORE	The reset bit 0x0: Not Active 0x1: Active
24	VFE_CSI_CORE	The reset bit 0x0: Not Active 0x1: Active
23	RESERVED_1	Do not use for APQ8064 (previously used for vfe_csi1_core)
22	RESERVED_2	Do not use for APQ8064 (previously used for SMI0_CORE)
21	MDP_CORE	The reset bit 0x0: Not Active 0x1: Active
20	AMP_CORE	The reset bit 0x0: Not Active 0x1: Active
19	JPEGD_CORE	The reset bit 0x0: Not Active 0x1: Active
18	CSI1_CORE	The reset bit 0x0: Not Active 0x1: Active
17	VPE_CORE	The reset bit 0x0: Not Active 0x1: Active
16	FABRIC_CORE	The reset bit 0x0: Not Active 0x1: Active
15	VFE_CORE	The reset bit 0x0: Not Active 0x1: Active
14	RESERVED_3	Removed for APQ8064
13	RESERVED_4	Removed for APQ8064
12	GFX3D_CORE	The reset bit 0x0: Not Active 0x1: Active

MMSS_SW_RESET_CORE (cont.)

Bits	Name	Description
11	HDMI_CORE	The reset bit 0x0: Not Active 0x1: Active
10	IMEM_CORE	The reset bit 0x0: Not Active 0x1: Active
9	IJPEG_CORE	The reset bit 0x0: Not Active 0x1: Active
8	CSI0_CORE	The reset bit 0x0: Not Active 0x1: Active
7	DSI_CORE	The reset bit 0x0: Not Active 0x1: Active
6	VCODEC_CORE	The reset bit 0x0: Not Active 0x1: Active
5	RESERVED	Do not use for APQ8064 (previously used for MDP_PCLK)
4	MDP_TV_CORE	The reset bit 0x0: Not Active 0x1: Active
3	MDP_VSYNC_CORE	The reset bit 0x0: Not Active 0x1: Active
2	ROT_CORE	The reset bit 0x0: Not Active 0x1: Active
1	TV_HDMI_CORE	The reset bit 0x0: Not Active 0x1: Active
0	RESERVED_0	Removed for APQ8064

0x04000214 MMSS_SW_RESET_CORE2

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x1F

The SW_RESET_CORE register controls the individual resets to all blocks.

MMSS_SW_RESET_CORE2

Bits	Name	Description
31:4	RESERVED	Reserved Bits
4	VCAP_NPL_CORE	The reset bit 0x0: Not Active 0x1: Active
3	VCAP_CORE	The reset bit 0x0: Not Active 0x1: Active
2	CSI2_CORE	The reset bit 0x0: Not Active 0x1: Active
1	CSI_RDI1_CLK	The reset bit 0x0: Not Active 0x1: Active
0	CSI_RDI2_CLK	The reset bit 0x0: Not Active 0x1: Active

0x04000300 MMSS_PLL0_MODE

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The PLL_MODE configures and controls the PLL. All register bits are clear (0) on RESOUT.

MMSS_PLL0_MODE

Bits	Name	Description
31:5	RESERVED	Reserved bits
4	PLL_REF_XO_SEL	Specify the reference XO to be used 0x0: PXO (24.576Mhz) 0x1: MXO (27Mhz)
3	PLLTEST	Set(1) this bit to enter the PLL test mode. Clear (0) this bit for the normal mode.
2	RESET_N	Low asserted reset for the digital logic in the PLL. This includes the MND dividers and integer divider.
1	BYPASSNL	Clear (0) to bypass the PLL (PLLOUT is then identical to the input reference). Set (1) to use the PLL. Default is clear (0) at RESOUT (different from previous APQs)

MMSS_PLL0_MODE (cont.)

Bits	Name	Description
0	OUTCTRL	Set (1) to activate the PLL's output (the analog circuitry is active but the output is not). Set (1) will enable the following PLL's output: nPLLOUT_LV_MAIN (if MAIN output enabled PLL0_CONFIG[23]) nPLLOUT_LV_BIST (If BIST output enabled PLL0_TEST_CTL[13]) nPLLOUT_LV_AUX (If AUX output enabled PLL0_TEST_CTL[12]) Clear (0) to disable the PLL's output and save power. Clears (0) at RESOUT.

0x04000304 MMSS_PLL0_L_VAL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The SR_PLL implements the following frequency equation:

PLLOUT_LV_MAIN=CK_IN*(1/PRE_DIV)*(L+M/N)*(1/POST_DIV)

CK_IN is the input reference frequency (XO)

PRE_DIV can be either 1 or 2

POST_DIV can be either 1,2,4, or 8

The value of the PLL_L_VAL is the given value of L for the SR_PLL frequency equation.

MMSS_PLL0_L_VAL

Bits	Name	Description
31:10	RESERVED	Reserved bits
9:0	PLL_L	This register contains the 6-bit L value in the PLL's fractional division ratio.

0x04000308 MMSS_PLL0_M_VAL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The value of the PLL_M_VAL is the given value of M for the SR_PLL frequency equation.

MMSS_PLL0_M_VAL

Bits	Name	Description
31:19	RESERVED	UNUSED
18:0	PLL_M	This register contains the 19-bit M value of the PLL's numerator value in the fractional division ratio.

0x0400030C MMSS_PLL0_N_VAL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The value of the PLL_N_VAL is the given value of N for the SR_PLL frequency equation.

MMSS_PLL0_N_VAL

Bits	Name	Description
31:19	RESERVED	UNUSED
18:0	PLL_N	This register contains the 19-bit N value of the PLL's denominator value in the fractional division ratio.

0x04000310 MMSS_PLL0_CONFIG

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The field descriptions show the mapping from 45nm NT wrapper PLL0_CONFIG register to SRPLL input, PLL_CONFIG_CTL. Some bits of PLL_CONFIG_CTL come from PLL0_TEST_CTL.

The PLL0_CONFIG register is used for the PLL0 (SR PLL) for:

- Enable the main output
- Setup integer or fractional mode
- Setup the Post divider ratio
- Setup the Pre divider ratio
- Select the appropriate VCO, depending on the generated frequency

MMSS_PLL0_CONFIG

Bits	Name	Description
31:28	RESERVED_BITS31_28	PLL0_CONFIG(31:30) maps to PLL_CONFIG_CTL(27:26) PLL0_CONFIG(29) maps to PLL_CONFIG_CTL(23) PLL0_CONFIG(28) maps to PLL_CONFIG_CTL(15)
27	EARLY_OUT_ENA	PLL0_CONFIG(27) : PLL_CONFIG_CTL(3) PLLOUT_LV_EARLY enable 0x0: Disable 0x1: Enable
26	CLK33_OUT_SEL	Not Used
25	CLK33_OUT_ENA	Not Used
24	OUT_SEL	Not Used
23	MAIN_OUT_ENA	PLL0_CONFIG(23) : PLL_CONFIG_CTL(0) PLLOUT_LV_MAIN enable 0x0: Disable 0x1: Enable
22	MN_ACCUM_ENA	PLL0_CONFIG(22) : PLL_CONFIG_CTL(14) PLL fractional mode control 0x0: Disable 0x1: Enable
21:20	PLLOUT_DIVIDE	PLL0_CONFIG(21:20) : PLL_CONFIG_CTL(8:7) PLL Post-divider control 0x0: Divide by 1 (use this setting when sending reference clock to output) 0x1: Divide by 2 0x2: Divide by 4 0x3: Invalid
19	PRE_DIVIDE	PLL0_CONFIG(19) : PLL_CONFIG_CTL(6) PLL pre-divider control 0x0: Divide by 1 0x1: Divide by 2
18	INTERNAL_BIT18	Not Used
17:16	VCO	PLL0_CONFIG(17) : PLL_CONFIG_CTL(9) VCO Selection PLL0_CONFIG(16) : Not Used 0x0: Select 100 - 500 MHz VCO 0x1: Select 400 - 1400 MHz VCO
15	INTERNAL_BIT15	Not Used
14:0	INTERNAL_BITS14_0	Not Used

0x04000314 MMSS_PLL0_TEST_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The PLL0_TEST_CTL register is used to enable the TEST, BIST and AUX outputs of PLL0 (SRPLL). The field descriptions show the mapping from 45nm NT wrapper PLL0_TEST_CTL register to SR PLL inputs, PLL_TEST_CTL and PLL_CONFIG_CTL.

MMSS_PLL0_TEST_CTL

Bits	Name	Description
31:19	RESERVED_BITS31_19	PLL0_TEST_CTL(31:30) maps to PLL_CONFIG_CTL(25:24) PLL0_TEST_CTL(29:28) maps to PLL_CONFIG_CTL(21:20) PLL0_TEST_CTL(27:26) maps to PLL_CONFIG_CTL(19:18) PLL0_TEST_CTL(25:24) maps to PLL_CONFIG_CTL(17:16) PLL0_TEST_CTL(23:22) maps to PLL_CONFIG_CTL(13:12) PLL0_TEST_CTL(21) maps to PLL_CONFIG_CTL(11) PLL0_TEST_CTL(20) maps to PLL_TEST_CTL(9) PLL0_TEST_CTL(19) : Not Used
18:17	INTERNAL_BITS18_17	PLL0_TEST_CTL(18:17) : Not Used
16	INTERNAL_BIT16	PLL0_TEST_CTL(16) : PLL_CONFIG_CTL(5) Output clock polarity 0x0: Do not invert output 0x1: Invert output
15	INTERNAL_BIT15	PLL0_TEST_CTL(15) : PLL_CONFIG_CTL(4) PLLOUT_LV_TEST enable 0x0: Disable 0x1: Enable
14	RESERVED_BIT14	PLL0_TEST_CTL(14) : Not used. See PLL0_L_VAL(14) that maps to PLL_TEST_CTL(14)
13	PLLOUT_BIST_ENABLE	PLL0_TEST_CTL(13) : PLL_CONFIG_CTL(2) PLLOUT_LV_BIST enable 0x0: Disable 0x1: Enable (must be enabled to use noise generator)

MMSS_PLL0_TEST_CTL (cont.)

Bits	Name	Description
12	PLLOUT_AUX_ENABLE	PLL0_TEST_CTL(12) : PLL_CONFIG_CTL(1) PLLOUT_LV_AUX enable 0x0: Disable 0x1: Enable

MMSS_PLL0_TEST_CTL (cont.)

Bits	Name	Description
11:0	INTERNAL_BITS11_0	PLL0_TEST_CTL(11) : Not Used PLL0_TEST_CTL(10) : PLL_TEST_CTL(8) Charge pump external bias control PLL0_TEST_CTL(9:8) : PLL_CONFIG_CTL(29:28) PFD force bits PLL0_TEST_CTL(9) = Force PFD up PLL0_TEST_CTL(8) = Force PFD down PLL0_TEST_CTL(7) : PLL_TEST_CTL(7) DTEST signal select PLL0_TEST_CTL(6) : PLL_TEST_CTL(6) ATEST amplifier bypass control PLL0_TEST_CTL(5:4) : PLL_TEST_CTL(5:4) ATEST1 signal select Force PLL filter voltage externally (set PLL_TEST_CTL(6) to 1) PLL0_TEST_CTL(3:2) : PLL_TEST_CTL(3:2) ATEST0 signal select PLL0_TEST_CTL(1) : PLL_TEST_CTL(1) ATEST1 Control PLL0_TEST_CTL(0) : PLL_TEST_CTL(0) ATEST0 Control 0x0: Disable 0x1: Enable 0x0: Normal operation_1 0x1: Force PFD UP -> 1 0x0: Normal operation_2 0x1: Force PFD DN -> 1 0x0: Select clock detect signal 0x1: Select feedback divider output signal 0x0: Do not bypass ATEST buffer amplifier 0x1: Bypass ATEST buffer amplifier 0x0: Observe Nwell reference (set PLL_TEST_CTL6 to 0) 0x1: Observe regulator output (set PLL_TEST_CTL6 to 0) 0x2: Observe PLL filter voltage (set PLL_TEST_CTL6 to 0) 0x3: Supply noise measurement mode 0x0: Provide external bias current to charge pump (set PLL_TEST_CTL8 to 1) 0x1: Observe ICO test current (set PLL_TEST_CTL9 to 1) 0x2: Observe bandgap test current 0x3: VSSA 0x0: Disable ATEST1 0x1: Enable ATEST1 0x0: Disable ATEST0 0x1: Enable ATEST0

0x04000318 MMSS_PLL0_STATUS

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

For backward compatibility, NT-PLL fields are maintained.

MMSS_PLL0_STATUS

Bits	Name	Description
15:0	PLL_STATUS	This register contains signals from the PLL's STATUS port. It is used to observe various 'status' values within the PLL.

0x0400031C MMSS_PLL1_MODE

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The PLL_MODE configures and controls the PLL. All register bits are clear (0) on RESOUT.

MMSS_PLL1_MODE

Bits	Name	Description
31:5	RESERVED	Reserved bits
4	PLL_REF_XO_SEL	Specify the reference XO to be used 0x0: PXO (24.576Mhz) 0x1: MXO (27Mhz)
3	PLLTEST	Set (1) this bit to enter the PLL test mode. Clear (0) this bit for the normal mode.
2	RESET_N	Low asserted reset for the digital logic in the PLL. This includes the MND dividers and integer divider.
1	BYPASSNL	Clear (0) to bypass the PLL (PLLOUT is then identical to the input reference). Set (1) to use the PLL. Default is clear (0) at RESOUT (different from previous APQs)

MMSS_PLL1_MODE (cont.)

Bits	Name	Description
0	OUTCTRL	Set (1) to activate the PLL's output (the analog circuitry is active but the output is not). Set (1) will enable the following PLL's output: n PLLOUT_LV_MAIN (if MAIN output enabled PLL0_CONFIG[23]) n PLLOUT_LV_BIST (If BIST output enabled PLL0_TEST_CTL[13]) n PLLOUT_LV_AUX (If AUX output enabled PLL0_TEST_CTL[12]) Clear (0) to disable the PLL's output and save power. Clears (0) at RESOUT.

0x04000320 MMSS_PLL1_L_VAL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The SR_PLL implements the following frequency equation:

PLLOUT_LV_MAIN=CK_IN*(1/PRE_DIV)*(L+M/N)*(1/POST_DIV)

Where:

- CK_IN is the input reference frequency (XO)
- PRE_DIV can be either 1 or 2
- POST_DIV can be either 1,2,4, or 8

The value of the PLL_L_VAL is the given value of L for the SR_PLL frequency equation.

MMSS_PLL1_L_VAL

Bits	Name	Description
31:10	RESERVED	Reserved bits
9:0	PLL_L	This register contains the 6-bit L value in the PLL's fractional division ratio.

0x04000324 MMSS_PLL1_M_VAL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The value of the PLL_M_VAL is the given value of M for the SR_PLL frequency equation.

MMSS_PLL1_M_VAL

Bits	Name	Description
31:19	RESERVED	Reserved bits
18:0	PLL_M	This register contains the 19-bit M value of the PLL's numerator value in the fractional division ratio.

0x04000328 MMSS_PLL1_N_VAL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The value of the PLL_N_VAL is the given value of N for the SR_PLL frequency equation.

MMSS_PLL1_N_VAL

Bits	Name	Description
18:0	PLL_N	This register contains the 19-bit N value of the PLL's denominator value in the fractional division ratio.

0x0400032C MMSS_PLL1_CONFIG

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The field descriptions show the mapping from 45nm NT wrapper PLL1_CONFIG register to SRPLL input, PLL_CONFIG_CTL. Some bits of PLL_CONFIG_CTL come from PLL1_TEST_CTL.

The PLL1_CONFIG register is used for the PLL1 (SR PLL) to:

- Enable the main output
- Set up integer or fractional mode
- Set up the Post divider ratio
- Set up the Pre divider ratio
- Select the appropriate VCO depending on the generated frequency

MMSS_PLL1_CONFIG

Bits	Name	Description
31:28	RESERVED_BITS31_28	PLL1_CONFIG(31:30) maps to PLL_CONFIG_CTL(27:26) PLL1_CONFIG(29) maps to PLL_CONFIG_CTL(23) PLL1_CONFIG(28) maps to PLL_CONFIG_CTL(15)
27	EARLY_OUT_ENA	PLL1_CONFIG(27) : PLL_CONFIG_CTL(3) PLLOUT_LV_EARLY enable 0x0: Disable 0x1: Enable
26	CLK33_OUT_SEL	Not Used
25	CLK33_OUT_ENA	Not Used
24	OUT_SEL	Not Used
23	MAIN_OUT_ENA	PLL1_CONFIG(23) : PLL_CONFIG_CTL(0) PLLOUT_LV_MAIN enable 0x0: Disable 0x1: Enable
22	MN_ACCUM_ENA	PLL1_CONFIG(22) : PLL_CONFIG_CTL(14) PLL fractional mode control 0x0: Disable 0x1: Enable
21:20	PLLOUT_DIVIDE	PLL1_CONFIG(21:20) : PLL_CONFIG_CTL(8:7) PLL Post-divider control 0x0: Divide by 1 (use this setting when sending reference clock to output) 0x1: Divide by 2 0x2: Divide by 4 0x3: Invalid
19	PRE_DIVIDE	PLL1_CONFIG(19) : PLL_CONFIG_CTL(6) PLL pre-divider control 0x0: Divide by 1 0x1: Divide by 2
18	INTERNAL_BIT18	Not Used
17:16	VCO	PLL1_CONFIG(17) : PLL_CONFIG_CTL(9) VCO Selection PLL1_CONFIG(16) : Not Used 0x0: Select 100 - 500 MHz VCO 0x1: Select 400 - 1400 MHz VCO
15	INTERNAL_BIT15	Not Used
14:0	INTERNAL_BITS14_0	Not Used

0x04000330 MMSS_PLL1_TEST_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The PLL1_TEST_CTL register is used to enable the TEST, BIST and AUX outputs of PLL1 (SRPLL). The field descriptions show the mapping from 45nm NT wrapper PLL1_TEST_CTL register to SR PLL inputs, PLL_TEST_CTL and PLL_CONFIG_CTL.

The PLL TEST_CTL register is used to enable the TEST, BIST and AUX outputs of PLL (SR PLL).

MMSS_PLL1_TEST_CTL

Bits	Name	Description
31:19	RESERVED_BITS31_19	PLL1_TEST_CTL(31:30) maps to PLL_CONFIG_CTL(25:24) PLL1_TEST_CTL(29:28) maps to PLL_CONFIG_CTL(21:20) PLL1_TEST_CTL(27:26) maps to PLL_CONFIG_CTL(19:18) PLL1_TEST_CTL(25:24) maps to PLL_CONFIG_CTL(17:16) PLL1_TEST_CTL(23:22) maps to PLL_CONFIG_CTL(13:12) PLL1_TEST_CTL(21) maps to PLL_CONFIG_CTL(11) PLL1_TEST_CTL(20) maps to PLL_TEST_CTL(9) PLL1_TEST_CTL(19) : Not Used
18:17	INTERNAL_BITS18_17	PLL1_TEST_CTL(18:17) : Not Used
16	INTERNAL_BIT16	PLL1_TEST_CTL(16) : PLL_CONFIG_CTL(5) Output clock polarity 0x0: Do not invert output 0x1: Invert output
15	INTERNAL_BIT15	PLL1_TEST_CTL(15) : PLL_CONFIG_CTL(4) PLLOUT_LV_TEST enable 0x0: Disable 0x1: Enable
14	RESERVED_BIT14	PLL1_TEST_CTL(14) : Not used. See PLL1_L_VAL(14) that maps to PLL_TEST_CTL(14)
13	PLLOUT_BIST_ENABLE	PLL1_TEST_CTL(13) : PLL_CONFIG_CTL(2) PLLOUT_LV_BIST enable 0x0: Disable 0x1: Enable (must be enabled to use noise generator)

MMSS_PLL1_TEST_CTL (cont.)

Bits	Name	Description
12	PLLOUT_AUX_ENABLE	PLL1_TEST_CTL(12) : PLL_CONFIG_CTL(1) PLLOUT_LV_AUX enable 0x0: Disable 0x1: Enable

MMSS_PLL1_TEST_CTL (cont.)

Bits	Name	Description
11:0	INTERNAL_BITS11_0	PLL1_TEST_CTL(11) : Not Used PLL1_TEST_CTL(10) : PLL_TEST_CTL(8) Charge pump external bias control PLL1_TEST_CTL(9:8) : PLL_CONFIG_CTL(29:28) PFD force bits PLL1_TEST_CTL(9) = Force PFD up PLL1_TEST_CTL(8) = Force PFD down PLL1_TEST_CTL(7) : PLL_TEST_CTL(7) DTEST signal select PLL1_TEST_CTL(6) : PLL_TEST_CTL(6) ATEST amplifier bypass control PLL1_TEST_CTL(5:4) : PLL_TEST_CTL(5:4) ATEST1 signal select Force PLL filter voltage externally (set PLL_TEST_CTL(6) to 1) PLL1_TEST_CTL(3:2) : PLL_TEST_CTL(3:2) ATEST0 signal select PLL1_TEST_CTL(1) : PLL_TEST_CTL(1) ATEST1 Control PLL1_TEST_CTL(0) : PLL_TEST_CTL(0) ATEST0 Control 0x0: Disable 0x1: Enable 0x0: Normal operation_1 0x1: Force PFD UP -> 1 0x0: Normal operation_2 0x1: Force PFD DN -> 1 0x0: Select clock detect signal 0x1: Select feedback divider output signal 0x0: Do not bypass ATEST buffer amplifier 0x1: Bypass ATEST buffer amplifier 0x0: Observe Nwell reference (set PLL_TEST_CTL6 to 0) 0x1: Observe regulator output (set PLL_TEST_CTL6 to 0) 0x2: Observe PLL filter voltage (set PLL_TEST_CTL6 to 0) 0x3: Supply noise measurement mode 0x0: Provide external bias current to charge pump (set PLL_TEST_CTL8 to 1) 0x1: Observe ICO test current (set PLL_TEST_CTL9 to 1) 0x2: Observe bandgap test current 0x3: VSSA 0x0: Disable ATEST1 0x1: Enable ATEST1 0x0: Disable ATEST0 0x1: Enable ATEST0

0x04000334 MMSS_PLL1_STATUS

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

For backward compatibility, NT-PLL fields are maintained.

MMSS_PLL1_STATUS

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:0	PLL_STATUS	This register contains signals from the PLL's STATUS port. It is used to observe various 'status' values within the PLL.

0x04000338 MMSS_PLL3_MODE

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The PLL_MODE configures and controls the PLL. All register bits are clear (0) on RESOUT.

MMSS_PLL3_MODE

Bits	Name	Description
31:5	RESERVED	Reserved bits
4	PLL_REF_XO_SEL	Specify the reference XO to be used 0x0: PXO (24.576Mhz) 0x1: MXO (27Mhz)
3	PLLTEST	0x1 Set(1) this bit to enter the PLL test mode. 0x0 Clear (0) this bit for the normal mode.
2	RESET_N	Low asserted reset for the digital logic in the PLL. This includes the MND dividers and integer divider.
1	BYPASSNL	0x0 Clear (0) to bypass the PLL (PLLOUT is then identical to the input reference). 0x1 Set (1) to use the PLL. Default is clear (0) at RESOUT (different from previous APQs)

MMSS_PLL3_MODE (cont.)

Bits	Name	Description
0	OUTCTRL	0x1 Set (1) to activate the PLL's output (the analog circuitry is active but the output is not). 0x1 Set (1) will enable the following PLL's output: - PLLOUT_LV_MAIN (if MAIN output enabled PLL0_CONFIG[23]) - PLLOUT_LV_BIST (If BIST output enabled PLL0_TEST_CTL[13]) - PLLOUT_LV_AUX (If AUX output enabled PLL0_TEST_CTL[12]) 0x0 Clear (0) to disable the PLL's output and save power. Clears (0) at RESOUT.

0x0400033C MMSS_PLL3_L_VAL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The SR_PLL implements the following frequency equation:

PLLOUT_LV_MAIN=CK_IN*(1/PRE_DIV)*(L+M/N)*(1/POST_DIV)

Where:

- CK_IN is the input reference frequency (XO)
- PRE_DIV can be either 1 or 2
- POST_DIV can be either 1,2,4, or 8

The value of the PLL_L_VAL is the given value of L for the SR_PLL frequency equation.

MMSS_PLL3_L_VAL

Bits	Name	Description
31:10	RESERVED	Reserved bits
9:0	PLL_L	This register contains the 6-bit L value in the PLL's fractional division ratio.

0x04000340 MMSS_PLL3_M_VAL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The value of the PLL_M_VAL is the given value of M for the SR_PLL frequency equation.

MMSS_PLL3_M_VAL

Bits	Name	Description
31:19	RESERVED	Reserved bits
18:0	PLL_M	This register contains the 19-bit M value of the PLL's numerator value in the fractional division ratio.

0x04000344 MMSS_PLL3_N_VAL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The value of the PLL_N_VAL is the given value of N for the SR_PLL frequency equation.

MMSS_PLL3_N_VAL

Bits	Name	Description
18:0	PLL_N	This register contains the 19-bit N value of the PLL's denominator value in the fractional division ratio.

0x04000348 MMSS_PLL3_CONFIG

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The field descriptions show the mapping from 45nm NT wrapper PLL3_CONFIG register to SRPLL input, PLL_CONFIG_CTL. Some bits of PLL_CONFIG_CTL come from PLL3_TEST_CTL.

The PLL_CONFIG register is used for the PLL (SR PLL) to:

- Enable the main output
- Set up integer or fractional mode
- Set up the Post divider ratio
- Se tup the Pre divider ratio
- Select the appropriate VCO, depending on the generated frequency

MMSS_PLL3_CONFIG

Bits	Name	Description
31:28	RESERVED_BITS31_28	PLL3_CONFIG(31:30) maps to PLL_CONFIG_CTL(27:26) PLL3_CONFIG(29) maps to PLL_CONFIG_CTL(23) PLL3_CONFIG(28) maps to PLL_CONFIG_CTL(15)
27	EARLY_OUT_ENA	PLL3_CONFIG(27) : PLL_CONFIG_CTL(3) PLLOUT_LV_EARLY enable 0x0: Disable 0x1: Enable
26	CLK33_OUT_SEL	Not Used
25	CLK33_OUT_ENA	Not Used
24	OUT_SEL	Not Used
23	MAIN_OUT_ENA	PLL3_CONFIG(23) : PLL_CONFIG_CTL(0) PLLOUT_LV_MAIN enable 0x0: Disable 0x1: Enable
22	MN_ACCUM_ENA	PLL3_CONFIG(22) : PLL_CONFIG_CTL(14) PLL fractional mode control 0x0: Disable 0x1: Enable
21:20	PLLOUT_DIVIDE	PLL3_CONFIG(21:20) : PLL_CONFIG_CTL(8:7) PLL Post-divider control 0x0: Divide by 1 (use this setting when sending reference clock to output) 0x1: Divide by 2 0x2: Divide by 4 0x3: Invalid
19	PRE_DIVIDE	PLL3_CONFIG(19) : PLL_CONFIG_CTL(6) PLL pre-divider control 0x0: Divide by 1 0x1: Divide by 2
18	INTERNAL_BIT18	Not Used
17:16	VCO	PLL3_CONFIG(17) : PLL_CONFIG_CTL(9) VCO Selection PLL3_CONFIG(16) : Not Used 0x0: Select 100 - 500 MHz VCO 0x1: Select 400 - 1400 MHz VCO
15	INTERNAL_BIT15	Not Used
14:0	INTERNAL_BITS14_0	Not Used

0x0400034C MMSS_PLL3_TEST_CTL

Type: Write/Read
Clock: AHB_CLK
Reset State: 0x0

The PLL3_TEST_CTL register is used to enable the TEST, BIST and AUX outputs of PLL3 (SRPLL). The field descriptions show the mapping from 45nm NT wrapper PLL3_TEST_CTL register to SR PLL inputs, PLL_TEST_CTL and PLL_CONFIG_CTL.

MMSS_PLL3_TEST_CTL

Bits	Name	Description
31:19	RESERVED_BITS31_19	PLL3_TEST_CTL(31:30) maps to PLL_CONFIG_CTL(25:24) PLL3_TEST_CTL(29:28) maps to PLL_CONFIG_CTL(21:20) PLL3_TEST_CTL(27:26) maps to PLL_CONFIG_CTL(19:18) PLL3_TEST_CTL(25:24) maps to PLL_CONFIG_CTL(17:16) PLL3_TEST_CTL(23:22) maps to PLL_CONFIG_CTL(13:12) PLL3_TEST_CTL(21) maps to PLL_CONFIG_CTL(11) PLL3_TEST_CTL(20) maps to PLL_TEST_CTL(9) PLL3_TEST_CTL(19) : Not Used
18:17	INTERNAL_BITS18_17	PLL3_TEST_CTL(18:17) : Not Used
16	INTERNAL_BIT16	PLL3_TEST_CTL(16) : PLL_CONFIG_CTL(5) Output clock polarity 0x0: Do not invert output 0x1: Invert output
15	INTERNAL_BIT15	PLL3_TEST_CTL(15) : PLL_CONFIG_CTL(4) PLLOUT_LV_TEST enable 0x0: Disable 0x1: Enable
14	RESERVED_BIT14	PLL3_TEST_CTL(14) : Not used. See PLL3_L_VAL(14) that maps to PLL_TEST_CTL(14)
13	PLLOUT_BIST_ENABLE	PLL3_TEST_CTL(13) : PLL_CONFIG_CTL(2) PLLOUT_LV_BIST enable 0x0: Disable 0x1: Enable (must be enabled to use noise generator)

MMSS_PLL3_TEST_CTL (cont.)

Bits	Name	Description
12	PLLOUT_AUX_ENABLE	PLL3_TEST_CTL(12) : PLL_CONFIG_CTL(1) PLLOUT_LV_AUX enable 0x0: Disable 0x1: Enable

MMSS_PLL3_TEST_CTL (cont.)

Bits	Name	Description
11:0	INTERNAL_BITS11_0	PLL3_TEST_CTL(11) : Not Used PLL3_TEST_CTL(10) : PLL_TEST_CTL(8) Charge pump external bias control PLL3_TEST_CTL(9:8) : PLL_CONFIG_CTL(29:28) PFD force bits PLL3_TEST_CTL(9) = Force PFD up PLL3_TEST_CTL(8) = Force PFD down PLL3_TEST_CTL(7) : PLL_TEST_CTL(7) DTEST signal select PLL3_TEST_CTL(6) : PLL_TEST_CTL(6) ATEST amplifier bypass control PLL3_TEST_CTL(5:4) : PLL_TEST_CTL(5:4) ATEST1 signal select Force PLL filter voltage externally (set PLL_TEST_CTL(6) to 1) PLL3_TEST_CTL(3:2) : PLL_TEST_CTL(3:2) ATEST0 signal select PLL3_TEST_CTL(1) : PLL_TEST_CTL(1) ATEST1 Control PLL3_TEST_CTL(0) : PLL_TEST_CTL(0) ATEST0 Control 0x0: Disable 0x1: Enable 0x0: Normal operation_1 0x1: Force PFD UP -> 1 0x0: Normal operation_2 0x1: Force PFD DN -> 1 0x0: Select clock detect signal 0x1: Select feedback divider output signal 0x0: Do not bypass ATEST buffer amplifier 0x1: Bypass ATEST buffer amplifier 0x0: Observe Nwell reference (set PLL_TEST_CTL6 to 0) 0x1: Observe regulator output (set PLL_TEST_CTL6 to 0) 0x2: Observe PLL filter voltage (set PLL_TEST_CTL6 to 0) 0x3: Supply noise measurement mode 0x0: Provide external bias current to charge pump (set PLL_TEST_CTL8 to 1)

MMSS_PLL3_TEST_CTL (cont.)

Bits	Name	Description
11:0	INTERNAL_BITS11_0 (continued)	PLL3_TEST_CTL(11) : Not Used PLL3_TEST_CTL(10) : PLL_TEST_CTL(8) Charge pump external bias control PLL3_TEST_CTL(9:8) : PLL_CONFIG_CTL(29:28) PFD force bits PLL3_TEST_CTL(9) = Force PFD up PLL3_TEST_CTL(8) = Force PFD down PLL3_TEST_CTL(7) : PLL_TEST_CTL(7) DTEST signal select PLL3_TEST_CTL(6) : PLL_TEST_CTL(6) ATEST amplifier bypass control PLL3_TEST_CTL(5:4) : PLL_TEST_CTL(5:4) ATEST1 signal select Force PLL filter voltage externally (set PLL_TEST_CTL(6) to 1) PLL3_TEST_CTL(3:2) : PLL_TEST_CTL(3:2) ATEST0 signal select PLL3_TEST_CTL(1) : PLL_TEST_CTL(1) ATEST1 Control PLL3_TEST_CTL(0) : PLL_TEST_CTL(0) ATEST0 Control 0x0: Disable 0x1: Enable 0x0: Normal operation_1 0x1: Force PFD UP -> 1 0x0: Normal operation_2 0x1: Force PFD DN -> 1 0x0: Select clock detect signal 0x1: Select feedback divider output signal 0x0: Do not bypass ATEST buffer amplifier 0x1: Bypass ATEST buffer amplifier 0x0: Observe Nwell reference (set PLL_TEST_CTL6 to 0) 0x1: Observe regulator output (set PLL_TEST_CTL6 to 0) 0x2: Observe PLL filter voltage (set PLL_TEST_CTL6 to 0) 0x3: Supply noise measurement mode 0x0: Provide external bias current to charge pump (set PLL_TEST_CTL8 to 1)

0x04000350 MMSS_PLL3_STATUS

Type: Read Only
Clock: AHB_CLK
Reset State: 0x0

For backward compatibility, NT-PLL fields are maintained.

MMSS_PLL3_STATUS

Bits	Name	Description
31:16	RESERVED	Reserved bits
15:0	PLL_STATUS	This register contains signals from the PLL's STATUS port. It is used to observe various status values within the PLL.

14.3 MFC Registers (0x04400000 MFC_BASE)

14.3.1 MFC Software Reset Registers

0x04400000 A_MFC_SW_RESET

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x000003fe

Soft reset for each module in MFC

0: Reset

1: Release

RISC to Host Interrupt Register

A_MFC_SW_RESET

Bits	Name	Description
9	RSTN_RG_MPEG2	Soft reset for RG_MPEG2
8	RSTN_RG_MPEG4	Soft reset for RG_MPEG4
7	RSTN_RG_VC1	Soft reset for RG_VC1
6	RSTN_RG_H264	Soft reset for RG_H264
5	RSTN_RG_COMMON	Soft reset for RG_COMMON and RG_DECCOM
4	RSTN_DMX	Soft reset for DMX 0
3	RSTN_VI	Soft reset for VI
2	RSTN_MFCCORE	Soft reset for MFC core
1	RSTN_MC	Soft reset for MC
0	RSTN_RISC	Soft reset for RISC core

0x04400008 A_MFC_RISC_HOST_INT

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

This interrupt is asserted when RISC CPU writes a set of requests into a MFC_RISC_HOST_INT register and put "1" into Interrupt bit (bit0). Then host CPU checks the MFC_RISC_HOST_INT register and properly processes ISR (interrupt service routine) and clears the Interrupt bit (bit0).

Host2Risc command register

A_MFC_RISC_HOST_INT

Bits	Name	Description
0	INTERRUPT	0: Interrupt Clear 1: This register may become `1' by RISC in MFC.

0x04400030 A_MFC_HOST2RISC_COMMAND

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Host can send command to Risc using HOST2RISC Command register when open instance or close instance.

RISC2HOST Arg Registers

A_MFC_HOST2RISC_COMMAND

Bits	Name	Description
31:0	HOST2RISC_COMMAND	Host to Risc Command register. 0: Empty 1: Open Instance 2: Close Instance 3: System Init

0x04400034 A_MFC_HOST2RISC_ARG1

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

The first argument of the host command.

A_MFC_HOST2RISC_ARG1

Bits	Name	Description
31:0	HOST2RISC_ARG1	- When HOST2RISC_COMMAND is "open instance", HOST2RISC_ARG is Codec Type. <Codec Type> 0 H.264 Decoding 1 VC1 Advanced Profile Decoding 2 MPEG4 / DivX / XVid Decoding 3 MPEG1/MPEG2 Decoding 4 H.263 Decoding 5 VC1 Simple/Main Profile Decoding 6 DivX 3.11 Decoding 7

0x04400038 A_MFC_HOST2RISC_ARG2

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

The second argument of the host command.

A_MFC_HOST2RISC_ARG2

Bits	Name	Description
31:0	HOST2RISC_ARG2	Reserved register

0x0440003C A_MFC_HOST2RISC_ARG3

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

The third argument of the host command.

A_MFC_HOST2RISC_ARG3

Bits	Name	Description
31:0	HOST2RISC_ARG3	Reserved register

0x04400040 A_MFC_HOST2RISC_ARG4

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

The fourth argument of the host command.

RISC2HOST Command Registers

A_MFC_HOST2RISC_ARG4

Bits	Name	Description
31:0	HOST2RISC_ARG4	Reserved register

0x04400044 A_MFC_RISC2HOST_COMMAND

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Risc can respond to host using RISC2HOST command register when open instance or close instance.

RISC2HOST Arg Registers

A_MFC_RISC2HOST_COMMAND

Bits	Name	Description
31:0	RISC2HOST_COMMAND	0: Empty 1: OPEN_CH_RET 2 : CLOSE_CH_RET 3 : ERROR_RET 4 : SEQ_DONE_RET 5 : FRAME_DONE_RET 6

0x04400048 A_MFC_RISC2HOST_ARG1

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

This register is used with RISC2HOST command register.

A_MFC_RISC2HOST_ARG1

Bits	Name	Description
31:0	INSTANCE_ID	Instance ID

0x0440004C A_MFC_RISC2HOST_ARG2

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

The second argument of the host command.

A_MFC_RISC2HOST_ARG2

Bits	Name	Description
31:0	MFC_RISC2HOST_ARG2	Reserved register

0x04400050 A_MFC_RISC2HOST_ARG3

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

The third argument of the host command.

A_MFC_RISC2HOST_ARG3

Bits	Name	Description
31:0	MFC_RISC2HOST_ARG3	Reserved register

0x04400054 A_MFC_RISC2HOST_ARG4

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

The fourth argument of the host command.

Firmware Version Information Registers

A_MFC_RISC2HOST_ARG4

Bits	Name	Description
31:0	MFC_RISC2HOST_ARG4	Reserved register

0x04400058 A_MFC_FIRMWARE_VERSION

Type: Read
Clock: AHB_CLOCK
Reset State: 0x00000000

This register shows a version of Firmware.

Firmware Status Register

A_MFC_FIRMWARE_VERSION

Bits	Name	Description
23:16	YEAR	Year: 00
15:8	MONTH	Month: 1
7:0	DAY	Day: 1

0x04400080 A_MFC_FIRMWARE_STATUS

Type: Read
Clock: AHB_CLOCK
Reset State: 0x00000000

Firmware status for a stream.

Number of Master Port Register

A_MFC_FIRMWARE_STATUS

Bits	Name	Description
0	FIRMWARE_STATUS	0: Not Ready 1: Ready

0x04400B14 A_MFC_NUM_MASTER

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Number of used masters

Channel A DRAM Base Address Register

A_MFC_NUM_MASTER

Bits	Name	Description
0	MFC_NUM_MASTER	Number of used master 0: One master 1: Two masters

0x04400508 A_MFC_MC_DRAMBASE_ADDR_A

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xD3000000

DRAM base address which indicates the base address of total memory map of MFC IP.

Channel B DRAM Base Address Register

A_MFC_MC_DRAMBASE_ADDR_A

Bits	Name	Description
31:17	MC_DRAMBASE_ADDR	DRAM base address (in 128 kBytes boundary) This must be aligned by 128KByte. MFC's access range is from DRAMBASE_ADDR_A to DRAMBASE_ADDR_A + 256MByte through Port_A

0x0440050C A_MFC_MC_DRAMBASE_ADDR_B

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x23000000

DRAM base address which indicates the base address of total memory map of MFC IP.

MC (Memory Controller) Status Register

A_MFC_MC_DRAMBASE_ADDR_B

Bits	Name	Description
31:17	MC_DRAMBASE_ADDR	DRAM base address (in 128 kBytes boundary) This must be aligned by 128KByte. MFC's access range is from DRAMBASE_ADDR_A to DRAMBASE_ADDR_B + 256MByte through Port_B

0x04400510 A_MFC_MC_STATUS

Type: Read
Clock: AHB_CLOCK
Reset State: 0x0000000X

Bus Arbiter's status. This register can be used to check whether Bus is busy or not before resetting MFC IP.

RISC Instruction Base Selection Register

A_MFC_MC_STATUS

Bits	Name	Description
1	MC_BUSY_B	Busy at Channel B 1: busy 0: idle
0	MC_BUSY_A	Busy at Channel A 1: busy 0: idle

0x04400514 A_MFC_MC_RS_IBASE

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_MC_RS_IBASE

Bits	Name	Description
0	MC_RS_IBASE	0: Channel A 1: Channel B

0x04400604 A_MFC_COMMON_BASE_ADDR_1

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_1

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400608 A_MFC_COMMON_BASE_ADDR_2

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_2

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440060C A_MFC_COMMON_BASE_ADDR_3

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_3

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400610 A_MFC_COMMON_BASE_ADDR_4

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_4

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400614 A_MFC_COMMON_BASE_ADDR_5

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_5

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400618 A_MFC_COMMON_BASE_ADDR_6

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_6

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440061C A_MFC_COMMON_BASE_ADDR_7

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_7

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400620 A_MFC_COMMON_BASE_ADDR_8

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_8

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400624 A_MFC_COMMON_BASE_ADDR_9

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_9

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400628 A_MFC_COMMON_BASE_ADDR_10

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_10

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440062C A_MFC_COMMON_BASE_ADDR_11

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_11

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400630 A_MFC_COMMON_BASE_ADDR_12

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_12

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400634 A_MFC_COMMON_BASE_ADDR_13

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_13

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400638 A_MFC_COMMON_BASE_ADDR_14

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_14

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440063C A_MFC_COMMON_BASE_ADDR_15

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_15

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400640 A_MFC_COMMON_BASE_ADDR_16

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_16

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400644 A_MFC_COMMON_BASE_ADDR_17

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_17

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400648 A_MFC_COMMON_BASE_ADDR_18

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_18

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440064C A_MFC_COMMON_BASE_ADDR_19

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_19

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400650 A_MFC_COMMON_BASE_ADDR_20

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_20

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400654 A_MFC_COMMON_BASE_ADDR_21

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_21

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400658 A_MFC_COMMON_BASE_ADDR_22

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_22

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440065C A_MFC_COMMON_BASE_ADDR_23

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_23

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400660 A_MFC_COMMON_BASE_ADDR_24

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_24

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400664 A_MFC_COMMON_BASE_ADDR_25

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_25

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400668 A_MFC_COMMON_BASE_ADDR_26

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_26

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440066C A_MFC_COMMON_BASE_ADDR_27

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_27

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400670 A_MFC_COMMON_BASE_ADDR_28

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_28

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400674 A_MFC_COMMON_BASE_ADDR_29

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_29

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400678 A_MFC_COMMON_BASE_ADDR_30

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_30

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440067C A_MFC_COMMON_BASE_ADDR_31

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_31

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400680 A_MFC_COMMON_BASE_ADDR_32

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_32

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400684 A_MFC_COMMON_BASE_ADDR_33

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_33

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400688 A_MFC_COMMON_BASE_ADDR_34

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_34

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440068C A_MFC_COMMON_BASE_ADDR_35

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_35

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400690 A_MFC_COMMON_BASE_ADDR_36

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_36

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400694 A_MFC_COMMON_BASE_ADDR_37

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_37

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400698 A_MFC_COMMON_BASE_ADDR_38

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_38

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440069C A_MFC_COMMON_BASE_ADDR_39

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_39

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006A0 A_MFC_COMMON_BASE_ADDR_40

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_40

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006A4 A_MFC_COMMON_BASE_ADDR_41

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_41

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006A8 A_MFC_COMMON_BASE_ADDR_42

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_42

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006AC A_MFC_COMMON_BASE_ADDR_43

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_43

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006B0 A_MFC_COMMON_BASE_ADDR_44

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_44

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006B4 A_MFC_COMMON_BASE_ADDR_45

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_45

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006B8 A_MFC_COMMON_BASE_ADDR_46

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_46

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006BC A_MFC_COMMON_BASE_ADDR_47

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_47

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006C0 A_MFC_COMMON_BASE_ADDR_48

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_48

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006C4 A_MFC_COMMON_BASE_ADDR_49

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_49

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006C8 A_MFC_COMMON_BASE_ADDR_50

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_50

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006CC A_MFC_COMMON_BASE_ADDR_51

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_51

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006D0 A_MFC_COMMON_BASE_ADDR_52

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_52

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006D4 A_MFC_COMMON_BASE_ADDR_53

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_53

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006D8 A_MFC_COMMON_BASE_ADDR_54

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_54

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006DC A_MFC_COMMON_BASE_ADDR_55

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_55

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006E0 A_MFC_COMMON_BASE_ADDR_56

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_56

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006E4 A_MFC_COMMON_BASE_ADDR_57

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_57

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006E8 A_MFC_COMMON_BASE_ADDR_58

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_58

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006EC A_MFC_COMMON_BASE_ADDR_59

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_59

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006F0 A_MFC_COMMON_BASE_ADDR_60

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_60

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006F4 A_MFC_COMMON_BASE_ADDR_61

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_61

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006F8 A_MFC_COMMON_BASE_ADDR_62

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_62

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044006FC A_MFC_COMMON_BASE_ADDR_63

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

For Port_B : Common Base Registers 64 - 127

A_MFC_COMMON_BASE_ADDR_63

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400700 A_MFC_COMMON_BASE_ADDR_64

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_64

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400704 A_MFC_COMMON_BASE_ADDR_65

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_65

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400708 A_MFC_COMMON_BASE_ADDR_66

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_66

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440070C A_MFC_COMMON_BASE_ADDR_67

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_67

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400710 A_MFC_COMMON_BASE_ADDR_68

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_68

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400714 A_MFC_COMMON_BASE_ADDR_69

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_69

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400718 A_MFC_COMMON_BASE_ADDR_70

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_70

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440071C A_MFC_COMMON_BASE_ADDR_71

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_71

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400720 A_MFC_COMMON_BASE_ADDR_72

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_72

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400724 A_MFC_COMMON_BASE_ADDR_73

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_73

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400728 A_MFC_COMMON_BASE_ADDR_74

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_74

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440072C A_MFC_COMMON_BASE_ADDR_75

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_75

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400730 A_MFC_COMMON_BASE_ADDR_76

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_76

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400734 A_MFC_COMMON_BASE_ADDR_77

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_77

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400738 A_MFC_COMMON_BASE_ADDR_78

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_78

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440073C A_MFC_COMMON_BASE_ADDR_79

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_79

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400740 A_MFC_COMMON_BASE_ADDR_80

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_80

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400744 A_MFC_COMMON_BASE_ADDR_81

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_81

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400748 A_MFC_COMMON_BASE_ADDR_82

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_82

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440074C A_MFC_COMMON_BASE_ADDR_83

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_83

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400750 A_MFC_COMMON_BASE_ADDR_84

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_84

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400754 A_MFC_COMMON_BASE_ADDR_85

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_85

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400758 A_MFC_COMMON_BASE_ADDR_86

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_86

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440075C A_MFC_COMMON_BASE_ADDR_87

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_87

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400760 A_MFC_COMMON_BASE_ADDR_88

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_88

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400764 A_MFC_COMMON_BASE_ADDR_89

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_89

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400768 A_MFC_COMMON_BASE_ADDR_90

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_90

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440076C A_MFC_COMMON_BASE_ADDR_91

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_91

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400770 A_MFC_COMMON_BASE_ADDR_92

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_92

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400774 A_MFC_COMMON_BASE_ADDR_93

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_93

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400778 A_MFC_COMMON_BASE_ADDR_94

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_94

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440077C A_MFC_COMMON_BASE_ADDR_95

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_95

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400780 A_MFC_COMMON_BASE_ADDR_96

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_96

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400784 A_MFC_COMMON_BASE_ADDR_97

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_97

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400788 A_MFC_COMMON_BASE_ADDR_98

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_98

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440078C A_MFC_COMMON_BASE_ADDR_99

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_99

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400790 A_MFC_COMMON_BASE_ADDR_100

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_100

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400794 A_MFC_COMMON_BASE_ADDR_101

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_101

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400798 A_MFC_COMMON_BASE_ADDR_102

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_102

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x0440079C A_MFC_COMMON_BASE_ADDR_103

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_103

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007A0 A_MFC_COMMON_BASE_ADDR_104

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_104

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007A4 A_MFC_COMMON_BASE_ADDR_105

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_105

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007A8 A_MFC_COMMON_BASE_ADDR_106

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_106

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007AC A_MFC_COMMON_BASE_ADDR_107

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_107

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007B0 A_MFC_COMMON_BASE_ADDR_108

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_108

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007B4 A_MFC_COMMON_BASE_ADDR_109

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_109

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007B8 A_MFC_COMMON_BASE_ADDR_110

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_110

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007BC A_MFC_COMMON_BASE_ADDR_111

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_111

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007C0 A_MFC_COMMON_BASE_ADDR_112

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_112

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007C4 A_MFC_COMMON_BASE_ADDR_113

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_113

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007C8 A_MFC_COMMON_BASE_ADDR_114

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_114

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007CC A_MFC_COMMON_BASE_ADDR_115

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_115

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007D0 A_MFC_COMMON_BASE_ADDR_116

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_116

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007D4 A_MFC_COMMON_BASE_ADDR_117

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_117

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007D8 A_MFC_COMMON_BASE_ADDR_118

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_118

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007DC A_MFC_COMMON_BASE_ADDR_119

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_119

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007E0 A_MFC_COMMON_BASE_ADDR_120

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_120

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007E4 A_MFC_COMMON_BASE_ADDR_121

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_121

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007E8 A_MFC_COMMON_BASE_ADDR_122

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_122

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007EC A_MFC_COMMON_BASE_ADDR_123

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_123

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007F0 A_MFC_COMMON_BASE_ADDR_124

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_124

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007F4 A_MFC_COMMON_BASE_ADDR_125

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_125

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007F8 A_MFC_COMMON_BASE_ADDR_126

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

A_MFC_COMMON_BASE_ADDR_126

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x044007FC A_MFC_COMMON_BASE_ADDR_127

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0xXXXXXXXX

Picture Width in Pixel Register

A_MFC_COMMON_BASE_ADDR_127

Bits	Name	Description
16:0	BASE_ADDR	Codec common memory region start address

0x04400818 A_MFC_HSIZE_PX

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Frame width at encoder.

Picture Height in Pixel Register

A_MFC_HSIZE_PX

Bits	Name	Description
12:0	FRAME_WIDTH	Coded width of frame

0x0440081C A_MFC_MC_VSIZE_PX

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Indicate height size of Picture. In interlaced-field coding mode, FRAME_HEIGHT is coded height of field. In progressive or interlaced-frame coding mode, FRAME_HEIGHT is coded height of frame at encoder.

Profile Register

A_MFC_MC_VSIZE_PX

Bits	Name	Description
12:0	FRAME_HEIGHT	Coded height of frame (field or frame)

0x04400830 A_MFC_PROFILE

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Profile and Version Control at encoder only.

Picture Structure Register

A_MFC_PROFILE

Bits	Name	Description
15:8	LEVEL	Level control register Ex) 3.1 = 8'd31

A_MFC_PROFILE (cont.)

Bits	Name	Description
5:0	PROFILE	<MPEG4> [5:4] standard selection control 0: MPEG-4 1: DivX 2: H.263, MP4 short header 3: Reserved When [5:4] == 2'd0 (MPEG-4) [0] MPEG4_PROFILE 0: Simple Profile 1: Advanced Simple Profile <H.264> [4] 8x8 enable flag (don't-care for encoding) [3:2] Chroma IDC (1 for encoding) [1: 0] profile 0: Main profile 1: High profile 2 : Baseline profile Other bits must set to be 0.

0x0440083C A_MFC_PICTURE_STRUCT

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Picture Field/Frame flag register. This register is used at encoder only.

Loop Filter Control Register

A_MFC_PICTURE_STRUCT

Bits	Name	Description
0	FIELD	<H.264, VC-1, MPEG-2> 0: Frame picture 1: Field picture <MPEG-4> 0: Frame picture only

0x04400848 A_MFC_LF_CONTROL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

This register is used at encoder only.

H.264 Loop Filter Alpha Offset Register

A_MFC_LF_CONTROL

Bits	Name	Description
1:0	LF_CONTROL	<H.264> [1:0] Loop Filter Disable Indicator from bitstream <MPEG-4> [1] Reserved [0] DF enable 1: Enable 0: Disable

0x0440084C A_MFC_LF_ALPHA_OFF

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Loop Filter Alpha Offset. This register is used at encoder only.

H.264 Loop Filter Beta Offset Register

A_MFC_LF_ALPHA_OFF

Bits	Name	Description
4:0	LF_ALPHAS_OFF	Loop filter alpha offset from bitstream

0x04400850 A_MFC_LF_BETA_OFF

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Loop Filter Beta Offset. This register is used at encoder only.

Pixel Cache Control Register

A_MFC_LF_BETA_OFF

Bits	Name	Description
4:0	LF_BETA_OFF	Loop filter beta offset from bitstream

0x04400A00 A_MFC_PIXEL_CACHE_CTRL0

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Pixel cache control register 0.

Auxiliary Host Command Base Register for Channel 0

A_MFC_PIXEL_CACHE_CTRL0

Bits	Name	Description
0	PIXEL_CACHE_EN	Pixel cache on/off 1: cache on 0: cache off This value can be changed at every frame decoding.

0x04400B18 A_MFC_CH0_HOST_WR_ADR

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

points to a space of shared memory consisting of multiple commands which host can write for channel 0.

Auxiliary RISC Response Base Register for Channel 0

A_MFC_CH0_HOST_WR_ADR

Bits	Name	Description
31:0	MFC_CH0_HOST_WR_ADR	Host set address register for writing command at channel 0. The address points to a space of shared memory consisting of multiple commands which host can write. The detailed structure of the shared memory is to be defined.

0x04400B1C A_MFC_CH0_HOST_RD_ADR

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Points to a space of shared memory consisting of multiple responses which host can read for channel 0.

Auxiliary Host Command Base Register for Channel 1

A_MFC_CH0_HOST_RD_ADR

Bits	Name	Description
31:0	MFC_CH0_HOST_RD_ADR	Host set address register for reading response at channel 0. The address points to a space of shared memory consisting of multiple responses which host can read. The detailed structure of the shared memory is to be defined.

0x04400B20 A_MFC_CH1_HOST_WR_ADR

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Points to a space of shared memory consisting of multiple commands which host can write for channel 1.

Auxiliary RISC Response Base Register for Channel 1

A_MFC_CH1_HOST_WR_ADR

Bits	Name	Description
31:0	MFC_CH1_HOST_WR_ADR	Host set address register for writing command at channel 1. The address points to a space of shared memory consisting of multiple commands which host can write. The detailed structure of the shared memory is to be defined.

0x04400B24 A_MFC_CH1_HOST_RD_ADR

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Points to a space of shared memory consisting of multiple responses which host can read for channel 1.

QP Plane Address Register

A_MFC_CH1_HOST_RD_ADR

Bits	Name	Description
31:0	MFC_CH1_HOST_RD_ADR	Host set address register for reading response at channel 1. The address points to a space of shared memory consisting of multiple responses which host can read. The detailed structure of the shared memory is to be defined.

0x04400C30 A_MFC_QP_OFFSEET

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Offset from DPB start at decoder. 1 unit = 64 bit

QP Save Feature Enable Register

A_MFC_QP_OFFSEET

Bits	Name	Description
31:0	MFC_QP_OFFSET	When MFC_QP_OUT_EN is `1', Luma DPB have to include area for QP's information. In this case, QP's information will be written from DPB + MFC_QP_OFFSET.

0x04400C34 A_MFC_QP_OUT_EN

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

QP save enable at decoder

If "MFC_QP_OUT_EN" is 1, Quantization value of each MB will be written in DPB area. Its address is calculated followings:

x_pos = [0...(img_hsize_mb-1)];

y_pos = frame ’ [0...(img_vsize_mb-1)] :

top ’ [0, 2, 4 ...(img_vsize_mb*2-2)] :

[1, 3, 5 ...(img_vsize_mb*2-1)] ;

< I_XSIZE >

if (img_hsize_mb < 64) I_XSIZE = 64

else if ((img_hsize_mb & 0x3f)!=0) I_XSIZE = ((img_hsize_mb>>6)<<6) + 64

```
    else I_XSIZE = img_hsize_mb
< I_XSIZE >
    if (frame) begin
    if(img_vsize_mb < 32) I_YSIZE = 32
    else if((img_vsize_mb & 0x1f)!=0) I_YSIZE = ((img_vsize_mb>>5)<<5) + 32 + 32
    else I_YSIZE = img_vsize_mb + 32
    end
    else begin
    if(img_vsize_mb < 16) I_YSIZE = 32
    else if((img_vsize_mb & 0x1f)!=0) I_YSIZE = ((img_vsize_mb>>4)<<5) + 32 + 32
    else I_YSIZE = (img_vsize_mb<<1) + 32
    end
pixel_x_m1 = I_XSIZE -1 ;
pixel_y_m1 = I_YSIZE -1 ;
roundup_x = ((pixel_x_m1)/16/8 + 1) ;
roundup_y = ((pixel_x_m1)/16/4 + 1) ;
x_addr = x_pos/4;
linear_addr0 = (((y_pos & 0x1f) <<4) |(x_addr & 0xf ) ) << 2 ;
linear_addr1 = (((y_pos >> 6) & 0xff) * roundup_x + ((x_addr >> 5) & 0x7f)) ;
    if( ((x_addr >> 5) & 0x1) == ((y_pos >> 5) & 0x1))
    bank_addr = ((x_addr >> 4) & 0x1);
    else
    bank_addr = 0x2 | ((x_addr >> 4) & 0x1);
physical_addr = DRAM_BASE + DPB_OFFSET + QP_OFFSET +
    (linear_addr1 <<13) | (bank_addr << 11)| linear_addr0 ;
qp_save_range = (pixel_y_minus[5]==0) ' pixel_y_minus[14:6] * roundup_x +
pixel_x_minus[14:8] +1:
    roundup_x * roundup_y;
```

Channel and Stream Interface Registers

There are two channel sets to communicate between host and MFC V5. Each channel 0 / 1 has two kind of registers. One is for response from MFC V5 like as MFC_SI_RTN_CHID and 15 numbers of MFC_COMMON_SI_RG. The other is for command from Host like as MFC_SI_CH_INST_ID and 15 numbers of MFC_COMMON_CH_RG.

Return CH0 Instance ID Register

A_MFC_QP_OUT_EN

Bits	Name	Description
0	MFC_QP_OUT_EN	0: QP out disable 1: QP out enable

0x04402000 A_MFC_SI_RTN_CHID

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Common SI Register 1-15

A_MFC_SI_RTN_CHID

Bits	Name	Description
31:0	RTN_CHID	Return Channel Instance ID which is used to identify which Channel's operation is done

0x04402008 A_MFC_COMMON_SI_RG_2

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_2

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_2	Return MFC's status after processing.

0x0440200C A_MFC_COMMON_SI_RG_3

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_3

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_3	Return MFC's status after processing.

0x04402010 A_MFC_COMMON_SI_RG_4

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_4

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_4	Return MFC's status after processing.

0x04402014 A_MFC_COMMON_SI_RG_5

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_5

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_5	Return MFC's status after processing.

0x04402018 A_MFC_COMMON_SI_RG_6

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_6

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_6	Return MFC's status after processing.

0x0440201C A_MFC_COMMON_SI_RG_7

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_7

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_7	Return MFC's status after processing.

0x04402020 A_MFC_COMMON_SI_RG_8

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_8

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_8	Return MFC's status after processing.

0x04402024 A_MFC_COMMON_SI_RG_9

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_9

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_9	Return MFC's status after processing.

0x04402028 A_MFC_COMMON_SI_RG_10

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_10

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_10	Return MFC's status after processing.

0x0440202C A_MFC_COMMON_SI_RG_11

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_11

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_11	Return MFC's status after processing.

0x04402030 A_MFC_COMMON_SI_RG_12

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_12

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_12	Return MFC's status after processing.

0x04402034 A_MFC_COMMON_SI_RG_13

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_13

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_13	Return MFC's status after processing.

0x04402038 A_MFC_COMMON_SI_RG_14

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_SI_RG_14

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_14	Return MFC's status after processing.

0x0440203C A_MFC_COMMON_SI_RG_15

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

NOTE The registers from 0x2040 to 0x207C have the same functionality as those from 0x2080 to 0x20BC. The registers from 0x2040 to 0x207C are used for channel 0 and those from 0x2080 to 0x20BC are for channel 1. They are used by both encoder and decoder with different meanings.

CH0 Instance ID Register

A_MFC_COMMON_SI_RG_15

Bits	Name	Description
31:0	MFC_COMMON_SI_RG_15	Return MFC's status after processing.

0x04402040 A_MFC_SI_CH0_INST_ID

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Common CH0 Register 1-15

A_MFC_SI_CH0_INST_ID

Bits	Name	Description
17:16	CH_DEC_TYPE	CH0 decoding control [1:0] 1: Sequence Header Decoding 2 : Frame Decoding/Encoding 3 : Last Frame Decoding/Encoding
15:0	CH_INST_ID	Instance ID for Codec

0x04402044 A_MFC_COMMON_CH0_RG_1

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_1

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_1	Set the value of MFC processing

0x04402048 A_MFC_COMMON_CH0_RG_2

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_2

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_2	Set the value of MFC processing

0x0440204C A_MFC_COMMON_CH0_RG_3

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_3

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_3	Set the value of MFC processing

0x04402050 A_MFC_COMMON_CH0_RG_4

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_4

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_4	Set the value of MFC processing

0x04402054 A_MFC_COMMON_CH0_RG_5

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_5

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_5	Set the value of MFC processing

0x04402058 A_MFC_COMMON_CH0_RG_6

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_6

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_6	Set the value of MFC processing

0x0440205C A_MFC_COMMON_CH0_RG_7

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_7

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_7	Set the value of MFC processing

0x04402060 A_MFC_COMMON_CH0_RG_8

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_8

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_8	Set the value of MFC processing

0x04402064 A_MFC_COMMON_CH0_RG_9

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_9

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_9	Set the value of MFC processing

0x04402068 A_MFC_COMMON_CH0_RG_10

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_10

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_10	Set the value of MFC processing

0x0440206C A_MFC_COMMON_CH0_RG_11

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_11

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_11	Set the value of MFC processing

0x04402070 A_MFC_COMMON_CH0_RG_12

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_12

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_12	Set the value of MFC processing

0x04402074 A_MFC_COMMON_CH0_RG_13

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_13

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_13	Set the value of MFC processing

0x04402078 A_MFC_COMMON_CH0_RG_14

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH0_RG_14

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_15	Set the value of MFC processing

0x0440207C A_MFC_COMMON_CH0_RG_15

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

CH1 Instance ID Register

A_MFC_COMMON_CH0_RG_15

Bits	Name	Description
31:0	MFC_COMMON_CH0_RG_15	Set the value of MFC processing

0x04402080 A_MFC_SI_CH1_INST_ID

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Common SI Register 1 - 15 CH 1

A_MFC_SI_CH1_INST_ID

Bits	Name	Description
17:16	CH_DEC_TYPE	CH1 decoding control [1:0] 1: Sequence Header Decoding 2 : Frame Decoding/Encoding 3 : Last Frame Decoding/Encoding
15:0	CH_INST_ID	Instance ID for Codec

0x04402088 A_MFC_COMMON_CH1_RG_2

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_2

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_2	Return MFC's status after processing.

0x0440208C A_MFC_COMMON_CH1_RG_3

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_3

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_3	Return MFC's status after processing.

0x04402090 A_MFC_COMMON_CH1_RG_4

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_4

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_4	Return MFC's status after processing.

0x04402094 A_MFC_COMMON_CH1_RG_5

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_5

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_5	Return MFC's status after processing.

0x04402098 A_MFC_COMMON_CH1_RG_6

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_6

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_6	Return MFC's status after processing.

0x0440209C A_MFC_COMMON_CH1_RG_7

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_7

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_7	Return MFC's status after processing.

0x044020A0 A_MFC_COMMON_CH1_RG_8

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_8

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_8	Return MFC's status after processing.

0x044020A4 A_MFC_COMMON_CH1_RG_9

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_9

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_9	Return MFC's status after processing.

0x044020A8 A_MFC_COMMON_CH1_RG_10

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_10

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_10	Return MFC's status after processing.

0x044020AC A_MFC_COMMON_CH1_RG_11

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_11

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_11	Return MFC's status after processing.

0x044020B0 A_MFC_COMMON_CH1_RG_12

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_12

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_12	Return MFC's status after processing.

0x044020B4 A_MFC_COMMON_CH1_RG_13

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_13

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_13	Return MFC's status after processing.

0x044020B8 A_MFC_COMMON_CH1_RG_14

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

A_MFC_COMMON_CH1_RG_14

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_14	Return MFC's status after processing.

0x044020BC A_MFC_COMMON_CH1_RG_15

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

NOTE The registers from 0x2040 to 0x207C have the same functionality as those from 0x20C0 to 0x20FC. The registers from 0x2040 to 0x207C are used for channel 0 and those from 0x20C0 to 0x20FC are for channel 1.

Encoded Data Formatter Unit Registers

Upper Stream Buffer Full Register

A_MFC_COMMON_CH1_RG_15

Bits	Name	Description
31:0	MFC_COMMON_CH1_RG_15	Return MFC's status after processing.

0x0440C004 A_STR_BF_U_FULL_0

Type: Read
Clock: AHB_CLOCK
Reset State: 0x00000000

Upper Stream Buffer Empty Register

A_STR_BF_U_FULL_0

Bits	Name	Description
0	BUFFER_U_FULL_L	Stream buffer status register - EDFU indicates upper buffer full status to external host. (1 = full)

0x0440C008 A_STR_BF_U_EMPTY_0

Type: Write
Clock: AHB_CLOCK
Reset State: 0x00000000

(Auto clear register)

Lower Stream Buffer Full Register.

A_STR_BF_U_EMPTY_0

Bits	Name	Description
0	BUFFER_U_EMPTY	Upper stream buffer clear register. The host should clear the buffer after it read data in the buffer.

0x0440C00C A_STR_BF_L_FULL_0

Type: Read
Clock: AHB_CLOCK
Reset State: 0x00000000

Lower Stream Buffer Empty Register

A_STR_BF_L_FULL_0

Bits	Name	Description
0	BUFFER_L_FULL_L	Stream buffer status register - EDFU indicates lower buffer full status to external host. (1 = full)

0x0440C010 A_STR_BF_L_EMPTY_0

Type: Write
Clock: AHB_CLOCK
Reset State: 0x00000000

(Auto clear register)

EDFU Status Register

A_STR_BF_L_EMPTY_0

Bits	Name	Description
0	BUFFER_L_EMPTY	Lower stream buffer clear register. The host should clear the buffer after it read data in the buffer.

0x0440C018 A_STR_BF_STATUS

Type: Read
Clock: AHB_CLOCK
Reset State: 0x00000000

(Auto clear register)

EDFU Stream Control Register

A_STR_BF_STATUS

Bits	Name	Description
8	ACTIVE_BUFFER	1: lower buffer 0: upper buffer

A_STR_BF_STATUS (cont.)

Bits	Name	Description
4	ENC_INT4	Encoding is done (including flashing out the bit-stream FIFO)
3	ENC_INT3	Both upper and lower buffers are full. The upper buffer must be read first.
2	ENC_INT2	Lower buffer is full.
1	ENC_INT1	Both upper and lower buffers are full. The lower buffer must be read first.
0	ENC_INT0	Upper buffer is full.

0x0440C054 A_EDFU_SF_EPB_ON_CTL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

EDFU control register

A_EDFU_SF_EPB_ON_CTL

Bits	Name	Description
1	STEAM_ENDIAN	0: Little-endian 1 : Big-endian
0	EPB_ON_CTRL	Insert EPB byte count value per frame. Valid at H.264 only 0: Automatically EPB insertion off 1 : Automatically EPB insertion on

0x0440C058 A_EDFU_SF_BUF_CTRL

Type: Write
Clock: AHB_CLOCK
Reset State: 0x00000000

(Auto clear register)

Stream Buffer Mode Control Register at Encoding

A_EDFU_SF_BUF_CTRL

Bits	Name	Description
2	EDFU_MC_INIT	1: Init EDFU_MC module
1	BUF_RESET	1: Buffer reset command 0: Normal operation

A_EDFU_SF_BUF_CTRL (cont.)

Bits	Name	Description
0	BUF_FLUSH	1: Buffer flush command 0: Normal operation

0x0440C05C A_STR_BF_MODE_CTRL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

EDFU fifo level control register

Picture Type Control Register

A_STR_BF_MODE_CTRL

Bits	Name	Description
0	STR_BF_MODE_CTRL	1: Stream buffer frame mode 0: Stream buffer double buffer mode.

0x0440C504 A_ENC_PIC_TYPE_CTRL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

. Used for H.264 encoder.

B-Picture Recon Picture Writing Control Register

A_ENC_PIC_TYPE_CTRL

Bits	Name	Description
18	ENC_PIC_TYPE_USE	1: Use ENC_PIC_TYPE_CTRL [17:0] register value for picture type setting 0: Use 0x083C (MFC_PICTURE_TYPE register)
17:16	B_FRM_CTRL	The number of B-code. 2'h0 : The number of B-code is zero. 2'h1 : The number of B-code is one. 2'h2 : The number of B-code is two. 2'h3 : Reserved.

A_ENC_PIC_TYPE_CTRL (cont.)

Bits	Name	Description
15:0	I_FRM_CTRL	16'h0 : all sequence is P frame 16'h1 : all sequence is I frame 16'h2 : I - P - I - P 16'h3 : I - P - P - I

0x0440C508 A_ENC_B_RECON_WRITE_ON

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

B-frame reconstructed data write control register (Default : 0. This is for just debugging. If you want this register to be `1', add this area in memory map.)

Multi-slice control register

A_ENC_B_RECON_WRITE_ON

Bits	Name	Description
0	B_RECON_ON	0: Disable recon data write at B-frame 1: Enable recon data write at B-frame

0x0440C50C A_ENC_MSLICE_CTR

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Macroblock Number of Multi-slice Setting Register

A_ENC_MSLICE_CTR

Bits	Name	Description
2:1	MSLICE_MODE	0: Multi slicing is done by MB count 1: Multi slicing is done by byte count
0	MSLICE_ENA	0: One slice per frame 1: Enable of resync marker or multi slice.

0x0440C510 A_ENC_MSLICE_MB

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

One slice size setting register when multi-slice is enabled. Fixed macroblock number of multi-slice setting register.

Byte Number of Multi-slice Setting Register

A_ENC_MSLICE_MB

Bits	Name	Description
15:0	MSLICE_MB	The number of macroblock in one slice when MSLICE_MODE = 0 and MSLICE_ENA = 1.

0x0440C514 A_ENC_MSLICE_BYTE

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

One slice size setting register when multi-slice is enabled. Byte count number of multi-slice setting register.

Circular Intra refresh macroblock setting register

A_ENC_MSLICE_BYTE

Bits	Name	Description
31:0	MSLICE_BYTE	The number of byte count in one slice when MSLICE_MODE = 1 and MSLICE_ENA = 1.

0x0440C518 A_ENC_CIR_CTRL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Intra refresh macroblock setting register

Memory Structure of Current Frame Settuing Register

A_ENC_CIR_CTRL

Bits	Name	Description
15:0	CIR_NUM	Number of intra-refresh macroblock.

0x0440C51C A_ENC_MAP_FOR_CUR

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Memory structure setting register of current frame.

Padding Value Control Register

A_ENC_MAP_FOR_CUR

Bits	Name	Description
1:0	ENC_MAP_FOR_CUR	Memory structure of macroblock 0: Linear mode. 3 : 64x32 tiled mode

0x0440C520 A_ENC_PADDING_CTRL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Padding Control Register.

Encoder Interrupt Status Register

A_ENC_PADDING_CTRL

Bits	Name	Description
31	PAD_CTRL_ON	0: Use boundary pixel for current image padding in case that its image size is not multiple by 16. 1: Use this register's value for current image padding
23:16	CR_PAD_VAL	Value for original CR image's padding when PAD_CTRL_ON is 1.
15:8	CB_PAD_VAL	Value for original CB image's padding when PAD_CTRL_ON is 1.
7:0	LUMA_PAD_VAL	Value for original LUMA image's padding when PAD_CTRL_ON is 1.

0x0440C524 A_ENC_INT_STATUS

Type: Read
Clock: AHB_CLOCK
Reset State: 0x00000000

Interrupt status register at encoder

Encoder Interrupt Mask Register

A_ENC_INT_STATUS

Bits	Name	Description
4	ENT_INT4	Stream data writes done to external memory
3	ENT_INT3	End of lower buffer writing and waiting for empty status of upper buffer.
2	ENT_INT2	End of lower buffer writing and continue to upper buffer area.
1	ENT_INT1	End of upper buffer writing and waiting for empty status of lower buffer.
0	ENT_INT0	End of upper buffer writing and continue to lower buffer area.

0x0440C528 A_ENC_INT_MASK

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Interrupt Bit Mask Register - When bit value is 1, interrupt will be generated.

Encoder Intra Mode Bias Register

A_ENC_INT_MASK

Bits	Name	Description
4	ENT_INT4	1: enable ENC_INT4 0: disable ENC_INT4
3	ENT_INT3	1: enable ENC_INT3 0: disable ENC_INT3
2	ENT_INT2	1: enable ENC_INT2 0: disable ENC_INT2
1	ENT_INT1	1: enable ENC_INT1 0: disable ENC_INT1
0	ENT_INT0	1: enable ENC_INT0 0: disable ENC_INT0

0x0440C588 A_ENC_COMMON_INTRA_BIAS

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Intra mode bias register for the macro block mode decision.

Encoder Bi-Directional Mode Bias Register

A_ENC_COMMON_INTRA_BIAS

Bits	Name	Description
15:0	ENC_COMMON_INTRA_BIAS	This register is used in favor of the intra mode in the weigjhted macro block mode decision.

0x0440C58C A_ENC_COMMON_BI_DIRECT_BIAS

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Bi-directional mode bias register for the macro block mode decision.

Encoder Reference Frame Number Register

A_ENC_COMMON_BI_DIRECT_BIAS

Bits	Name	Description
15:0	ENC_COMMON_BI_DIRECT_BIAS	This register is used against the bi-directional mode in the weighted macro block mode decision.

0x0440C530 A_ENC_REF_NUM_SEL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Number of reference frame for encoding control register. Maximum 2 reference frame is supported.

Rate Control Configuration Register

A_ENC_REF_NUM_SEL

Bits	Name	Description
0	REF_NUM_SEL	0: 1 reference frame 1: 2 reference frame

0x0440C5A0 A_ENC_RC_CONFIG

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Configuration of Rate Control block.

RC Frame Rate Register

A_ENC_RC_CONFIG

Bits	Name	Description
9	FR_RC_EN	Frame level rate control enable 0: Disable Frame level rate control by F/W 1: Enable Frame level rate control by F/W
8	MB_RC_EN	Macroblock level rate control enable 0: Disable MB level rate control by H/W 1: Enable MB level rate control by H/W
5:0	FRAME_QP	Frame QP (quantization parameter) is used for the QP of the first macroblock in a frame. This value is in the range of 0 to 51. The QP of the next macroblocks can be changed as the following table according to the value of FR_RC_EN and MB_RC_EN. Case BIT[9:8] 2'b00 : Constant QP is applied to all macroblocks. 2'b01 : The QP of the next macroblocks can vary with macroblock adaptive scaling. 2'b10 : The QP of the next macroblocks can be changed by the difference between the numbers of target bit and generated bit during the encoding a picture. But macroblock adaptive scaling is not applied. 2'b11 : The QP of the next macroblocks can be changed by the difference between the numbers of target bit and generated bit during the encoding a picture. It also can vary with macroblock adaptive scaling.

0x0440C5A4 A_RC_FRAME_RATE

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Frame rate for the frame level RC.

RC Bit Rate Register

A_RC_FRAME_RATE

Bits	Name	Description
7:0	FRAME_RATE	Frames per second. `0' is forbidden. Valid only when Frame level RC is enabled.

0x0440C5A8 A_RC_BIT_RATE

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Frame rate for the frame level RC.

RC Quantizer Parameter Boundary Register

A_RC_BIT_RATE

Bits	Name	Description
7:0	BIT_RATE	Bits per second. `0' is forbidden. Valid only when Frame level RC is enabled.

0x0440C5AC A_RC_QBOUND

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Maximum and minimum value of the quantization parameter.

Reaction Coefficient Register

A_RC_QBOUND

Bits	Name	Description
13:8	MAX_QP	Maximum quantization parameter.

A_RC_QBOUND (cont.)

Bits	Name	Description
7:0	MIN_QP	Minimum quantization parameter.

0x0440C5B0 A_RC_RPARA

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Rate control reaction coefficient.

Macroblock Level Rate Control Register

A_RC_RPARA

Bits	Name	Description
15:0	REACT_PARA	Rate control reaction coefficient. `0' is forbidden. Notes: - Valid only when the Frame level RC is enabled. - For tight CBR, this field must be small. (ex. 2

0x0440C5B4 A_RC_MB_CTRL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Control the macroblock adaptive scaling features.

NOTE Valid only when the Macroblock level RC is enabled.

Internal Reference Quantization Scale Register

A_RC_MB_CTRL

Bits	Name	Description
3	DARK_DISABLE	Disable Dark Region Adaptive feature. 0: Enable Dark Region Adaptive feature. QP of dark MB may not be smaller than frame QP although it is smooth, static or it has small activity. 1: Disable Dark Region Adaptive feature.

A_RC_MB_CTRL (cont.)

Bits	Name	Description
2	SMOOTH_DISABLE	Disable Smooth Region Adaptive feature. 0: Enable Smooth Region Adaptive feature. QP of smooth MB may be smaller than frame QP. 1: Disable Smooth Region Adaptive feature.
1	STATIC_DISABLE	Disable Static Region Adaptive feature. 0: Enable Static Region Adaptive feature. QP of static MB may be smaller than frame QP. 1: Disable Static Region Adaptive feature.
0	ACT_DISABLE	Disable MB Activity Adaptive feature. 0: Enable MB Activity Adaptive feature. QP of MB that has small activity may be smaller than frame QP and QP of MB that has large activity may be larger than frame QP 1: Disable MB Activity Adaptive feature.

0x0440C5B8 A_RC_QOUT

Type: Read
Clock: AHB_CLOCK
Reset State: 0x00000000

Final frame quantization parameter.

NOTE QP_OUT can be referenced for the frame quantization parameter (FRAME_QP) of the next frame.

H.264 Encode Register

A_RC_QOUT

Bits	Name	Description
5:0	QP_OUT	Final frame quantization parameter (FRAME_QP) referenced for encoding the last macroblock of the current picture

0x0440D004 A_H264_ENC_ENTRP_MODE

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

H.264 Entropy Register - Entropy coding mode.

H.264 Loop Filter Alpha Offset Register

A_H264_ENC_ENTRP_MODE

Bits	Name	Description
0	H264_ENC_ENTRP_MODE	0: CAVLC. 1: CABAC.

0x0440D008 A_H264_ENC_LF_ALPHA_OFFSET

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Loop filter alpha offset.

H.264 Loop Filter Beta Offset Register

A_H264_ENC_LF_ALPHA_OFFSET

Bits	Name	Description
4:0	H264_ENC_LF_ALPHA_OFFSET	Loop filter alpha offset.

0x0440D00C A_H264_ENC_LF_BETA_OFFSET

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Loop filter alpha offset.

H.264 Number of Reference Register

A_H264_ENC_LF_BETA_OFFSET

Bits	Name	Description
4:0	H264_ENC_LF_BETA_OFFSET	Loop filter beta offset.

0x0440D010 A_H264_ENC_NUM_OF_REF

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

The maximum number of reference pictures.

H.264 Active Number of Reference Register

A_H264_ENC_NUM_OF_REF

Bits	Name	Description
4:0	H264_ENC_NUM_OF_REF	The maximum number of reference pictures.

0x0440D014 A_H264_ENC_ACTIVE_NUM_OF_REF

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

The number of reference pictures.

H.264 Inter Weighted Parameter Register

A_H264_ENC_ACTIVE_NUM_OF_REF

Bits	Name	Description
9:5	REF_IDX_L0_MINUS1	number_ref_idx_l0_active_minus1.
4:0	REF_IDX_L1_MINUS1	number_ref_idx_l1_active_minus1.

0x0440D01C A_H264_ENC_MDINTER_WEIGHT

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

For calculation of cost value, inter weighted parameter for mode decision.

H.264 Intra Weighted Parameter Register

A_H264_ENC_MDINTER_WEIGHT

Bits	Name	Description
4:0	H264_ENC_MDINTER_WEIGHT	If interSAD < MDInterWeightPPS, select the inter mode.

0x0440D020 A_H264_ENC_MDINTRA_WEIGHT

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

For calculation of cost value, intera weighted parameter for mode decision.

H.264 Motion Vector Enable in INTRA Register

A_H264_ENC_MDINTRA_WEIGHT

Bits	Name	Description
4:0	H264_ENC_MDINTRA_WEIGHT	If interSAD < intraSAD + MDIntraWeightPPS, select the inter mode

0x0440D024 A_H264_ENC_INTRAMV_EN

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Motion vector enable in INTRA slice for rate control.

H.264 Direct Mode Register

A_H264_ENC_INTRAMV_EN

Bits	Name	Description
0	H264_ENC_INTRAMV_EN	0: Off 1: On

0x0440D028 A_H264_ENC_DIREC8X8_INF_FLAG

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Specifies the method used in the derivation process for luma motion vector for B_Skip, B_Direct_16x16 and B_Direct_8x8.

H.264 LIST0 Field Information Register

A_H264_ENC_DIREC8X8_INF_FLAG

Bits	Name	Description
0	H264_ENC_DIRECT8X8_INF_FLAG	Specifies the method used in the derivation process for luma motion vector for B_Skip, B_Direct_16x16 and B_Direct_8x8.

0x0440D02C A_H264_ENC_LIST0_TOP_FIELD

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Information of top/bottom field of selected reference picture.

H.264 LIST1 Field Information Register

A_H264_ENC_LIST0_TOP_FIELD

Bits	Name	Description
0	ENC_LIST0_TOP_FIELD	Information of list0 top/bottom field of selected reference picture. 1: Field 0: Frame

0x0440D030 A_H264_ENC_LIST1_TOP_FIELD

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Information of top/bottom field of selected reference picture.

H.264 8X8 Transform Enable Flag Register

A_H264_ENC_LIST1_TOP_FIELD

Bits	Name	Description
0	ENC_LIST1_TOP_FIELD	Information of list1 top/bottom field of selected reference picture. 1: Field 0: Frame

0x0440D034 A_H264_ENC_TRANS_8X8_FLAG

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

n 8x8 transform enable flag in PPS at high profile.

Encode MV Info On Register

A_H264_ENC_TRANS_8X8_FLAG

Bits	Name	Description
0	ENC_TRANS_8X8_FLAG	0: Disable 1: Enable

0x0440D140 A_MBINFO_ON

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

- Dump MB Info to address location specified by MBINFO_ADDR register (0x0720).

MPEG-4 Quarter Pixel Interpolation Register

A_MBINFO_ON

Bits	Name	Description
0	ENC_MBINFO_ON	0: Disable 1: Enable

0x0440E008 A_MPEG4_ENC_QUART_PXL

Type: Read/Write
Clock: AHB_CLOCK
Reset State: 0x00000000

Quarter pel interpolation control register

A_MPEG4_ENC_QUART_PXL

Bits	Name	Description
0	MPEG4_QUART_PXL	0: Quarter pixel search disable. 1: Quarter pixel search enable.

14.4 MFCV1080P Registers (0x04400000 MFC_BASE)

0x04480000 A_MFCV1080P_MGEN_VERSION

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x0000001D

A_MFCV1080P_MGEN_VERSION

Bits	Name	Description
7:0	VERSION	HW version of mgen2axi core being used. (R29)

0x04480004 A_MFCV1080P_MGEN_AXI_AOOORD

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

A_MFCV1080P_MGEN_AXI_AOOORD

Bits	Name	Description
0	AXI_AOOORD	"Out of order" enable for reads, 1 bit per client. If zero, the AXI bus and slaves must ensure that all reads from that client are completed in the order they are requested from the client. 0x0: RESET_VAL

0x04480008 A_MFCV1080P_MGEN_AXI_AOOOWR

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

A_MFCV1080P_MGEN_AXI_AOOOWR

Bits	Name	Description
0	AXI_AOOOWR	"Out of order" enable for writes from client 4w+0. If zero, the AXI bus and slaves must ensure that all writes from this client are completed in the order they are requested from the client. 0x0: RESET_VAL

0x0448000C A_MFCV1080P_MGEN_AXI_ATYPE

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000006

A_MFCV1080P_MGEN_AXI_ATYPE

Bits	Name	Description
3:0	AXI_TYPE	The value to drive on ATYPE signal, 4 bits per client. Probably one of these: 0110 - Normal, Cacheable, Writeback, Write-allocate, Non-shared. 0111 - same as above except Shared 0110 - RESET_VAL

0x04480010 A_MFCV1080P_MGEN_AXI_AREQPRIORITY

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

A_MFCV1080P_MGEN_AXI_AREQPRIORITY

Bits	Name	Description
1:0	AXI_AREQPRIORITY	Request priority, 2 bits per client. This value is driven onto AXI bus only, not used internally when for client arbitration. 0x0: RESET_VAL

0x04480014 A_MFCV1080P_MGEN_AXI_CTL

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

A_MFCV1080P_MGEN_AXI_CTL

Bits	Name	Description
31	AXI_INTR_CLR	When set (1), MFCV1080P_MGEN_AXI_STATUS. AXI_ERR_INTR & AXI_WDTIMEOUT_INTR is cleared. It has to be explicitly cleared to capture the next AXI ERR/WDTIMEOUT interrupt. 0x0: RESET VAL
20:17	AXI_WDTIMEOUT_LOG2	Write data timeout value in log2 format.The actual timeout value is power of 2 of this specified log2 value.

A_MFCV1080P_MGEN_AXI_CTL (cont.)

Bits	Name	Description
16	AXI_HALT_ON_WDTIMEOUT	When set (1), write data timeout behaves like "halt on error". Wdtimeout_halt will go high and remain high until AXI reset and wdtimeout_stb (glitch-free strobe) will be high in the first cycle.
12	AXI_HALT_ON_WR_ERR	When set (1), a write error response from AXI (on bresp) acts like a HALT_REQ and also disables all ARB-XIN interfaces - instead, fake write data to AXI (zero write enables) and discard read data from AXI. SW should wait for HALT_ACK and then reset the core.
8	AXI_HALT_ON_RD_ERR	When set (1), an read error response from AXI (on rresp) acts like a HALT_REQ and also disables all ARB-XIN interfaces - instead, fake write data to AXI (zero write enables) and discard read data from AXI. SW should wait for HALT_ACK and then reset the core.
4	AXI_RESET	When set (1), the AXI master port is held in reset. The clock that it uses may be turned off. 0x0: RESET_VAL
0	AXI_HALT_REQ	When set (1), this core will not issue any additional AXI requests. This bit should not be reset to 0 until HALT_ACK is 1. 0x0: RESET_VAL

0x04480018 A_MFCV1080P_MGEN_AXI_STATUS

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000030

AXI_A & AXI_B statuses are located at [4n] & [4n+1] respectively.

A_MFCV1080P_MGEN_AXI_STATUS

Bits	Name	Description
13:12	AXI_WDTIMEOUT_INTR	Indicates AXI_WDTIMEOUT interrupt has occurred. It stays on until MFCV1080P_MGEN_AXI_CTL.AXI_INTR_CLR is set (1).
9:8	AXI_ERR_INTR	Indicates AXI_ERR interrupt has occurred. It stays on until MFCV1080P_MGEN_AXI_CTL.AXI_INTR_CLR is set (1).
5:4	AXI_IDLE	Indicates that the AXI master port is idle (no pending requests on AXI).
1:0	AXI_HALT_ACK	Indicates that the halt request was completed (no more pending requests). This will remain high until this arbiter is reset.

0x0448001C A_MFCV1080P_MGEN_AXI_ERROR_INFO_AXI_A

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000000

A_MFCV1080P_MGEN_AXI_ERROR_INFO_AXI_A

Bits	Name	Description
16	AXI_WDTIMEOUT	Indicates that an AXI write data timeout has occurred since the last AXI reset, and it was treated the same as a write error response with AXI_HALT_ON_WR_ERR=1. SW should wait for HALT_ACK and then reset the core.
11	AXI_ERR	Indicates an AXI error occurred since the last AXI reset. The AXI_ERR interrupt status may be more useful than this bit.
10	AXI_ERR_TYPE	The type of the last error that occurred. 0x0: axi_rresp 0x1: axi_bresp (has priority over rresp if happen same time)
9:8	AXI_RESP	The value of axi_rresp or axi_bresp when the last error occurred.
7:4	AXI_MID	The value on axi_rmid or axi_bmid when the last error occurred.
3:0	AXI_TID	The value on axi_rtid or axi_btid when the last error occurred.

0x04480020 A_MFCV1080P_MGEN_AXI_ERROR_INFO_AXI_B

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000000

A_MFCV1080P_MGEN_AXI_ERROR_INFO_AXI_B

Bits	Name	Description
16	AXI_WDTIMEOUT	Indicates that an AXI write data timeout has occurred since the last AXI reset, and it was treated the same as a write error response with AXI_HALT_ON_WR_ERR=1. SW should wait for HALT_ACK and then reset the core.
11	AXI_ERR	Indicates an AXI error occurred since the last AXI reset. The AXI_ERR interrupt status may be more useful than this bit.
10	AXI_ERR_TYPE	The type of the last error that occurred. 0x0: axi_rresp 0x1: axi_bresp (has priority over rresp if happen same time)
9:8	AXI_RESP	The value of axi_rresp or axi_bresp when the last error occurred.
7:4	AXI_MID	The value on axi_rmid or axi_bmid when the last error occurred.
3:0	AXI_TID	The value on axi_rtid or axi_btid when the last error occurred.

0x04480024 A_MFCV1080P_MGEN_AXI_TEST_CTL

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

A_MFCV1080P_MGEN_AXI_TEST_CTL

Bits	Name	Description
24	AXI_RD_LAT_REP_EN	1 bit per arb. when enabled, each beat of read data is replaced with the read access latency (of AXI cycles from request til read data returned) 0x0: RESET_VAL
20	AXI_LSFR_EN	1 bit per arb, when enabled the AXI response is "faked" (all reads complete in order) and read data is generated using LFSR. During test, some arbs may use real data, while others use random data. THIS FEATURE IS NOT IMPLEMENTED, WILL BE DROPPED. 0x0: RESET_VAL
16	AXI_MISR_RES	1 bit per arb, need to write 1 and then write 0
12	AXI_MISR_EN	1 bit per arb 0x0: RESET_VAL
8	AXI_MISR_WD	1 bit per arb, to select misr input 0x0: read data (coming back from AXI) 0x1: write data (going to AXI)
7	AXI_CTR_EN	Enable all profiling counters 0x0: RESET_VAL
6	AXI_CTR_RES	Reset all profiling counters (they are also reset by AXI_RESET)
5:4	AXI_TEST_ARB_SEL_1_0	Select which arbiter to drive AXI_TEST_OUT.
3:0	AXI_TEST_OUT_SEL_3_0	Select which test data is read via AXI_TEST_OUT. 0x0: num read bursts (32 bits) 0x1: total read BW (32 bits - up to 68GB) 0x2: max outstanding reads (8 bits) 0x3: avg wait for read accept (10 bits over 128 reads) 0x4: min read latency (16 bits) 0x5: max read latency (16 bits) 0x6: avg read latency (16 bits over 1K read beats) 0x8: num write bursts (32 bits) 0x9: total write BW (32 bits - up to 68GB) 0xA: max outstanding writes (8 bits) 0xB: avg wait for write accept (10 bits over 128 writes) 0xC: MISR signature word 0 0xD: MISR signature word 1 0xE: MISR signature word 2 0xF: MISR signature word 3

0x04480028 A_MFCV1080P_MGEN_AXI_TEST_OUT_AXI_A

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000000

A_MFCV1080P_MGEN_AXI_TEST_OUT_AXI_A

Bits	Name	Description
31:0	AXI_TEST_OUT	The output selected by AXI_TEST_CTL reg. There are 4 registers to allow 128 bit data.

0x0448002C A_MFCV1080P_MGEN_AXI_TEST_OUT_AXI_B

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000000

A_MFCV1080P_MGEN_AXI_TEST_OUT_AXI_B

Bits	Name	Description
31:0	AXI_TEST_OUT	The output selected by AXI_TEST_CTL reg. There are 4 registers to allow 128 bit data.

0x04480030 A_MFCV1080P_TESTMODE_CTL

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00010000

A_MFCV1080P_TESTMODE_CTL

Bits	Name	Description
31	ENABLE	Enable test mdoe 0x0: disable 0x1: enable
30	CONST_VAL	Output constant instead of selected test bus Based on Select[1:0] When "00", test bus output = 0xBB55_1080 When "01", test bus output = 0x5555_5555 When "10", test bus output = 0xAAAA_AAAA When "11", test bus output = MFCV1080p_TESTMODE_CTL 0x0: Normal test bus output 0x1: Enable constant value

A_MFCV1080P_TESTMODE_CTL (cont.)

Bits	Name	Description
19:12	MFCV_1080P_VERSION	POR value indicates mfcv_1080p core version being used. However, this 8 bit field can be reprogrammed to any value as general purpose register afterward.
11:8	MGEN2MAXI_DATA_SEL	MGEN2MAXI Data select [3:0]
7	MGEN2MAXI_XIN_SEL	MGEN2MAXI Xin select (when MGEN2MAXI_ARB = 0) 0x0: Xin0 port "01" 0x1: Xin1 port "10"
6	MGEN2MAXI_ARB_SEL	MGEN2MAXI Arb select 0x0: Select Xin port 0x1: Select Arb port
5:4	MGEN2MAXI_TESTBUS_SEL	MGEN2MAXI test bus select 0x0: test bus 1 (core clock) 0x1: test bus 2 (axi clock) 0x2: axi_test_out_1 0x3: axi_test_out_2
3	AHB2AHB_TESTBUS_SEL	AHB2AHB test bus select 0x0: Slave bus "01" 0x1: Master bus "10"
2	MGEN2MAXI_AXI_SEL	Select mgen2maxi test bus from AXI_A or AXI_B port 0x0: AXI_A 0x1: AXI_B
1:0	SELECT	Select test bus from different modules 0x0: AHB2AHB 0x1: MGEN2MAXI 0x2: ENHANCE BLK - AHB2AHB 0x3: EHNANCE BLK - PIXEL CACHE

0x04480034 A_MFCV1080P_MGEN_XBAR_IN_RD_WR_LIM

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00001010

A_MFCV1080P_MGEN_XBAR_IN_RD_WR_LIM

Bits	Name	Description
15:8	XBAR_IN_RD_LIM	The maximum number of pending reads from each client. Must be less than or equal to the HW parameter that limits the same. Default is 16 and range is [0,32].

A_MFCV1080P_MGEN_XBAR_IN_RD_WR_LIM (cont.)

Bits	Name	Description
7:0	XBAR_IN_WR_LIM	The maximum number of pending writes from each client. Must be less than or equal to the HW parameter that limits the same. Default is 16 and range is [0,32].

0x04480038 A_MFCV1080P_MGEN_XBAR_OUT_RD_WR_LIM

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00001010

A_MFCV1080P_MGEN_XBAR_OUT_RD_WR_LIM

Bits	Name	Description
15:8	XBAR_OUT_RD_LIM	The maximum number of pending reads from each client. Must be less than or equal to the HW parameter that limits the same. Default is 16 and range is [0,32].
7:0	XBAR_OUT_WR_LIM	The maximum number of pending writes from each client. Must be less than or equal to the HW parameter that limits the same. Default is 16 and range is [0,32].

0x0448003C A_MFCV1080P_MGEN_XBAR_OUT_MAX_BURST

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000303

A_MFCV1080P_MGEN_XBAR_OUT_MAX_BURST

Bits	Name	Description
15:8	XBAR_OUT_MAX_RD_BURST	The maximum number of read beats minus 1 allowed on the AXI bus (arbiter outputs). Must be less the HW parameter that limits the same. Default is 3 and range is [0,8].
7:0	XBAR_OUT_MAX_WR_BURST	The maximum number of write beats minus 1 allowed on the AXI bus (arbiter outputs). Must be less the HW parameter that limits the same. Default is 3 and range is [0,8].

14.5 MFCV1080P Registers (0x04400000 MFC_BASE)

0x044C0000 A_MFCV1080P_ENH_DMI_CFG

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register is used to configure direct access to the local memory. To use this register, the core must not be in use to ensure stability of the contents of the memory.

Ram list:

CACHE_TAG (count: 8): 48x64

CACHE_FIFO_0 (count: 1): 64x64

CACHE_FIFO_1 (count: 1) : 64x33

CACHE_DATA (count: 2): 768x64

A_MFCV1080P_ENH_DMI_CFG

Bits	Name	Description
8	AUTO_INC_EN	Set (1) to auto-increment MFCV1080P_ENH_DMI_ADDR by 1 anytime MFCV1080P_ENH_DMI_DATA_LO is written or read.
3:0	DMI_RAM_SEL	This bit field is used to specify the video local memory for direct memory access. 0x0: NO_MEMORY 0x1: CACHE_TAG0 0x2: CACHE_TAG1 0x3: CACHE_TAG2 0x4: CACHE_TAG3 0x5: CACHE_TAG4 0x6: CACHE_TAG5 0x7: CACHE_TAG6 0x8: CACHE_TAG7 0x9: CACHE_FIFO_0 0xA: CACHE_FIFO_1 0xB: CACHE_DATA0 0xC: CACHE_DATA1

0x044C0004 A_MFCV1080P_ENH_DMI_ADDR

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register is used to specify the address of the memory to read/write through MFCV1080P_ENH_DMI_DATA_HI/MFCV1080P_ENH_DMI_DATA_LO.

A_MFCV1080P_ENH_DMI_ADDR

Bits	Name	Description
10:0	DMI_ADDR	This bit field specifies the local memory address of the core.

0x044C0008 A_MFCV1080P_ENH_DMI_DATA_HI

Type: Read/Write
Clock: VIDEO_CLOCK
Read Wait States:MFCV1080P_ENH_DMI_DATA_LO followed by MFCV1080P_ENH_DMI_DATA_HI
Reset State: 0x00000000

This register represents the upper 32 bits of the DMI data. The following order needs to be followed for accessing the data registers:

Write: MFCV1080P_ENH_DMI_DATA_HI followed by MFCV1080P_ENH_DMI_DATA_LO

A_MFCV1080P_ENH_DMI_DATA_HI

Bits	Name	Description
31:0	DMI_DATA_HI	This register represents the upper 32 bits of the DMI data. When this register is written, the value of this register is registered and prepared to be written into the upper 32-bits of the memory selected by DMI_RAM_SEL field in the MFCV1080P_ENH_DMI_CFG register. The actual write to the memory is triggered by a write to MFCV1080P_ENH_DMI_DATA_LO. When this register is read, it returns the upper 32 bits of the memory data accessed by the previous MFCV1080P_ENH_DMI_DATA_LO.

0x044C000C A_MFCV1080P_ENH_DMI_DATA_LO

Type: Read/Write
Clock: VIDEO_CLOCK
Read Wait States:MFCV1080P_ENH_DMI_DATA_LO followed by MFCV1080P_ENH_DMI_DATA_HI
Reset State: 0x00000000

This register represents the lower 32 bits of the DMI data. The following order needs to be followed for accessing the data registers:

Write: MFCV1080P_ENH_DMI_DATA_HI followed by MFCV1080P_ENH_DMI_DATA_LO

A_MFCV1080P_ENH_DMI_DATA_LO

Bits	Name	Description
31:0	DMI_DATA_LO	This register represents the lower 32 bits of the DMI data. When this register is written, the value of this register is written into the lower 32 bits of the memory selected by MFCV1080P_ENH_DMI_CFG[3:0]. If the memory is wider than 32 bits, the upper 32 bits can be prepared by writing to MFCV1080P_ENH_DMI_DATA_HI. When this register is read, it returns the lower 32 bits of the memory data.

0x044C0010 A_MFCV1080P_ENH_TEST_BUS_CFG

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register configures the test bus selection in the enhancement block.

A_MFCV1080P_ENH_TEST_BUS_CFG

Bits	Name	Description
4:0	PIX_CACHE_TB_SEL	(00000) Selects the constant 0xDA1CAC4E (00001) Selects the request handler testbus (00010) Selects the preprocessor testbus (00011) Selects the index tag generator testbus (00100) Selects the tags lookup testbus0 (00101) Selects the tags lookup testbus1 (00110) Selects the tags lookup testbus2 (00111) Selects the tags lookup testbus3 (01000) Selects the tag ram 0 control logic testbus (01001) Selects the tag ram 1 control logic testbus (01010) Selects the tag ram 2 control logic testbus (01011) Selects the tag ram 3 control logic testbus (01100) Selects the tag ram 4 control logic testbus (01101) Selects the tag ram 5 control logic testbus (01110) Selects the tag ram 6 control logic testbus (01111) Selects the tag ram 7 control logic testbus (10000) Selects the request generator testbus (10001) Selects the command fifo testbus (10010) Selects the data handler testbus0 (10011) Selects the data handler testbus1 (10100) Selects the data handler testbus2 (10101) Selects the statistics tracker testbus (10110) Selects the configuration register (MFCV1080P_ENH_PIX_CACHE_MISR_CFG) on the testbus

0x044C0014 A_MFCV1080P_ENH_SW_RESET

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register can be used to reset the pixel cache block and/or the CRIF registers in the enhance block. The Resets must be asserted for at least 1 cycle before it can be de-asserted.

A_MFCV1080P_ENH_SW_RESET

Bits	Name	Description
1	PIX_CACHE_SW_RESET	Set (1) to assert reset to the Pixel Cache block
0	CRIF_RESET	Set (1) to assert reset to the Enhance block CRIF registers

0x044C0018 A_MFCV1080P_ENH_PIX_CACHE_CFG

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000018

This register is used for pixel cache control that may get programmed every Frame.

A_MFCV1080P_ENH_PIX_CACHE_CFG

Bits	Name	Description
12	CACHE_HALT	(0) Clear cache halt (1) Set cache halt
9:8	PAGE_SIZE	Ensure that prefetches do not cross PAGE_SIZE boundary (00) 1K page (01) 2K page (10) 4K page (11) Reserved
5	STATISTICS_OFF	(0) Enable statistics capture (1) Disable statistics capture
4	CACHE_PORT_SELECT	(0) Use cache on port A (1) Use cache on port B
3	PREFETCH_EN	(0) Disable prefetch (1) Enable prefetch
2	SS_TILE_FORMAT	(0) External memory content is arranged in SS 4x2MB tile mode (1) External memory content is arranged in SS linear mode NOTE: This bit is disabled and set to 0 because 1080p core only supports tile mode in decoding.
1	CACHE_EN	(0) Cache is disabled, SS core interacts directly with AXI (1) Cache is enabled, SS core interacts with cache, and cache interacts with AXI
0	CACHE_TAG_CLEAR	This bit clears the tags for the cache. If the tags are cleared, everything inside the pixel cache is considered invalid. The bit must be de-asserted (0) after being set (1). If this bit is left as set (1), the tags will always be cleared and cache will consider all requests to be misses.

0x044C001C A_MFCV1080P_ENH_PIX_CACHE_FRAME_SIZE

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

Trigger: Cache Tag Clear

This is a double-buffered register, and it specifies the dimensions of a reconstructed frame. The maximum width and height that is supported is 1920x1088.

A_MFCV1080P_ENH_PIX_CACHE_FRAME_SIZE

Bits	Name	Description
26:16	FRAME_HEIGHT	Height in pixels of the reference frame.
10:0	FRAME_WIDTH	Width in pixels of the reference frame.

0x044C0020 A_MFCV1080P_ENH_PIX_CACHE_FRAME_RANGE

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

Trigger: Cache Tag Clear

This is a double-buffered register, and it specifies the amount of memory occupied by a reconstructed frame.

A_MFCV1080P_ENH_PIX_CACHE_FRAME_RANGE

Bits	Name	Description
17:0	LINEAR_LUMA	SS linear mode: number of dwords in 1 luma frame
15:8	TILE_LUMA	SS 4x2MB tile mode: number of 8K pages in 1 luma frame
7:0	TILE_CHROMA	SS 4x2MB tile mode: number of 8K pages in 1 chroma frame

0x044C0024+4*n A_MFCV1080P_ENH_PIX_CACHE_LUMA_BASE_ADDRn, n=[0..18]

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0xFFFFFFF8

Trigger: Cache Tag Clear

These are double-buffered registers, and they supply the base luma addresses of the DPB regions. When not used, it should be programmed to 0xFFFFFFF8.

A_MFCV1080P_ENH_PIX_CACHE_LUMA_BASE_ADDRn

Bits	Name	Description
31:3	ADDR	Luma regions's base starting address

0x044C0070+ 4*n A_MFCV1080P_ENH_PIX_CACHE_CHROMA_BASE_ADDRn, n=[0..18]

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0xFFFFFFF8

Trigger: Cache Tag Clear

These are double-buffered registers, and they supply the base chroma addresses of the DPB regions. When not used, it should be programmed to 0xFFFFFFF8.

A_MFCV1080P_ENH_PIX_CACHE_CHROMA_BASE_ADDRn

Bits	Name	Description
31:3	ADDR	Chroma regions's base starting address

0x044C00BC A_MFCV1080P_ENH_PIX_CACHE_STATUS

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000001

This register provide the status of the pixel cache.

A_MFCV1080P_ENH_PIX_CACHE_STATUS

Bits	Name	Description
0	IDLE	Asserts when the pixel cache is idle

0x044C00C0 A_MFCV1080P_ENH_PIX_CACHE_ACCESS_MISS_STAT

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register counts the number of misses for the data cache. The counter is reset to 0 using the cache tag clear signal.

A_MFCV1080P_ENH_PIX_CACHE_ACCESS_MISS_STAT

Bits	Name	Description
31:0	MISS_COUNT	Number of cache misses after the cache was last cleared

0x044C00C4 A_MFCV1080P_ENH_PIX_CACHE_ACCESS_HIT_STAT

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register counts the number of hits for the data cache. The counter is reset to 0 using the cache tag clear signal.

A_MFCV1080P_ENH_PIX_CACHE_ACCESS_HIT_STAT

Bits	Name	Description
31:0	HIT_COUNT	Number of cache hits after the cache was last cleared

0x044C00C8 A_MFCV1080P_ENH_PIX_CACHE_AXI_REQ_STAT

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register counts the number of AXI requests generated from the cache. The counter is reset to 0 using the cache tag clear signal.

A_MFCV1080P_ENH_PIX_CACHE_AXI_REQ_STAT

Bits	Name	Description
31:0	AXI_REQUEST_COUNT	Number of AXI requests generated

0x044C00CC A_MFCV1080P_ENH_PIX_CACHE_CORE_REQ_STAT

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register counts the number of Core requests going into the cache. The counter is reset to 0 using the cache tag clear signal.

A_MFCV1080P_ENH_PIX_CACHE_CORE_REQ_STAT

Bits	Name	Description
31:0	CORE_REQUEST_COUNT	Number of Core requests detected

0x044C00D0 A_MFCV1080P_ENH_PIX_CACHE_AXI_BUS_STAT

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register counts the number of data beats (dwords) received from the AXI. The counter is reset to 0 using the cache tag clear signal.

A_MFCV1080P_ENH_PIX_CACHE_AXI_BUS_STAT

Bits	Name	Description
31:0	AXI_BEAT_COUNT	Number of data beats received from the AXI

0x044C00D4 A_MFCV1080P_ENH_PIX_CACHE_CORE_BUS_STAT

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register counts the number of data beats (dwords) sent to the core. The counter is reset to 0 using the cache tag clear signal.

A_MFCV1080P_ENH_PIX_CACHE_CORE_BUS_STAT

Bits	Name	Description
31:0	CORE_BEAT_COUNT	Number of data beats sent to the SS core

0x044C00D8 A_MFCV1080P_ENH_PIX_CACHE_MISR_CFG

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register controls the test MISR.

A_MFCV1080P_ENH_PIX_CACHE_MISR_CFG

Bits	Name	Description
31:8	COUNTER	Maximum number of requests/data to feed into MISR. A value of 0 indicates no maximum
7:4	ID	Only transactions using this ID will be feed into the MISR
3	IGNORE_ID	(0) Use ID field to filter the requests/data going into the MISR (1) Ignore the ID field and feed all requests/data into MISR

A_MFCV1080P_ENH_PIX_CACHE_MISR_CFG (cont.)

Bits	Name	Description
2:1	INPUT_SEL	(00) Apply MISR to requests going into pixel cache (01) Apply MISR to requests generated by pixel cache (10) Apply MISR to data going into pixel cache from AXI (11) Apply MISR to data coming out of pixel cache to the core
0	MISR_EN	(0) MISR is disabled (1) MISR is enabled

0x044C00DC +4*n A_MFCV1080P_ENH_PIX_CACHE_MISR_SIGNATUREn, n=[0..1]

Type: Read
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register indicates the current test MISR signature. Different signatures are given depending on the MISR configuration, and they should be verified against the c-model.

MISR on requests:

MISR_SIGNATURE0: signature of request addresses

MISR_SIGNATURE1: signature of request burst sizes

MISR on data:

MISR_SIGNATURE0: signature of data's lower 32-bits

MISR_SIGNATURE1: signature of data's upper 32-bits

A_MFCV1080P_ENH_PIX_CACHE_MISR_SIGNATUREn

Bits	Name	Description
31:0	SIGNATURE	MISR signature

0x044C00E4 A_MFCV1080P_ENH_PIX_CACHE_SPARE_REG

Type: Read/Write
Clock: VIDEO_CLOCK
Reset State: 0x00000000

This register is a spare register. It is for future use

A_MFCV1080P_ENH_PIX_CACHE_SPARE_REG

Bits	Name	Description
31:0	SPARE_REG_VALUE	Future use

14.6 Gemini JPEG Registers (0x04600000 GEMINI_BASE)

This section provides information for the Gemini JPEG core registers.

14.6.1 AHB registers

The following registers are programmable through the Peripheral Bus AHB interface. The AHB register interface uses a request-ack protocol to hold the bus until the read data is valid so wait states are not applicable.

14.6.1.1 Gemini top registers

0x04600000 A_JPEG_HW_VERSION

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 1200

This register can be read to allow SW to identify the HW version of the GEMINI core.

A_JPEG_HW_VERSION

Bits	Name	Description
19:16	CORE_VERSION	This value identifies the generation of the Gemini core.
15:8	MAJOR_VERSION	This value represents the major version of the Gemini core.
7:0	MINOR_VERSION	This value represents the minor version of the Gemini core.

0x04600004 A_JPEG_RESET_CMD

Type: Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register is used to reset the hardware to a known state. A composite interrupt is generated when all the resets are completed. A second reset command should not be issued until the reset acknowledge is received from the first command

Note that this register is a command register - writes to this register produced strobe commands to the HW.

A_JPEG_RESET_CMD

Bits	Name	Description
31	RESET_BYPASS	When set 1, the reset controller is bypassed and SW must manually assert / de-assert reset to each clock domain using the *_DOMAIN_RESET fields. The individual functional module reset is inactive. No reset done interrupt is generated. When clear 0, the reset controller for the individual functional module is active, and the *_DOMAIN_RESET fields are not meaningful. A reset done interrupt is generated.
30	BUS_DOMAIN_RESET	This bit is used to manually assert/de-assert reset to the BUS clock domain registers.
29	JPEG_DOMAIN_RESET	This bit is used to manually assert/de-assert reset to the JPEG clock domain registers
18	CLKONIDLE_RESET	Writing a '1' causes a reset to be issued to the clkon_clkidle control block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
15	CORE_RESET	Writing a '1' causes a reset to be issued to the core. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
14	BUS_STATS_RESET	Writing a '1' causes a reset to be issued to the bus stats block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
13	BUS_MISR_RESET	Writing a '1' causes a reset to be issued to the bus MISR. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
12	TESTGEN_RESET	Writing a '1' causes a reset to be issued to the test generator block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
11	REGISTER_RESET	Writing a '1' causes a reset to be issued to the register block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
10	VFE_INTERFACE_RESET	Writing a '1' causes a reset to be issued to the VFE interface block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
9	BRIDGE_RESET	Writing a '1' causes a reset to be issued to the bus bridge block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
8	WRITE_ENGINE_RESET	Writing a '1' causes a reset to be issued to the write engine block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.

A_JPEG_RESET_CMD (cont.)

Bits	Name	Description
7	FETCH_ENGINE_RESET	Writing a '1' causes a reset to be issued to the fetch engine block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
6	STATS_RESET	Writing a '1' causes a reset to be issued to the stats block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
5	HUFFMAN_RESET	Writing a '1' causes a reset to be issued to the Huffman block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
4	ZIGZAG_RESET	Writing a '1' causes a reset to be issued to the zigzag block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
3	RLE_RESET	Writing a '1' causes a reset to be issued to the RLE block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
2	FSC_RESET	Writing a '1' causes a reset to be issued to the File Size Control Block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.
1	QUANTIZER_RESET	Writing a '1' causes a reset to be issued to the quantizer block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.This bit resets the quantization/inverse quantization module hardware.
0	DCT_RESET	Writing a '1' causes a reset to be issued to the DCT block. Writing '0' has no effect. When the reset is complete an interrupt is generated back to the GEMINI interrupt controller.This bit resets the DCT/IDCT module hardware.

0x04600008 A_JPEG_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register controls the data path configuration for the GEMINI JPEG pipeline.

Rotation is not supported for real-time JPEG.

A_JPEG_CFG

Bits	Name	Description
29	ASSERT_JPEGCLKIDLE	These bits are used in conjunction with Bit 18. When jpegclkidle is under SW control, these bits indicate the value which the HW drives on jpegclkidle. 0x0: JPEGCLKIDLE driven to 0 0x1: JPEGCLKIDLE driven to 1
28	DEASSERT_AXICLKON	These bits are used in conjunction with Bit 18. When axiclkon is under SW control, these bits indicate the value which the HW drives on axiclkon. 0x0: AXICLKON driven to 1 0x1: AXICLKON driven to 0
26:25	MODE	These bits indicate the operation the HW is to perform. 0x0: Real-time JPEG Encode 0x1: Offline JPEG Encode 0x2: Real-time Frame Rotation 0x3: Invalid
24:23	JPEG_FORMAT	These bits indicate the input image format. 0x0: Invalid 0x1: H1V2 0x2: H2V1 0x3: H2V2
22	WE_INPUT_SEL	These bits select the input for the GEMINI Write Engine. 0x0: JPEG Pipeline 0x1: Fetch Engine
21	JPEG_INPUT_SEL	These bits select the input for the GEMINI JPEG pipeline. 0x0: Fetch Engine 0x1: HW Test Generator
20	FE_INPUT_SEL	These bits select the input bus width for the GEMINI Fetch Engine. 0x0: 64 bit bus 0x1: 32 bit bus
18	CLKONIDLE_ENABLE	This bit enables/disables the clkon_clkidle HW control block. When HW control is disabled, SW has control of the values driven for the CLKONIDLE signals from the core. 0x0: CLKONIDLE HW control disabled. 0x1: CLKONIDLE HW control enabled.
17	TESTBUS_ENABLE	This bit enables the Gemini core testbus output.
16	HBFC_ENABLE	This bit enables HW control of the HBFC vote signal.
14	BUS_STATS_ENABLE	This bit enables/disables the BUS Stats block. 0x0: BUS Stats disabled. 0x1: BUS Stats enabled.

A_JPEG_CFG (cont.)

Bits	Name	Description
13	BUS_MISR_ENABLE	This bit enables/disables the BUS MISR block. 0x0: BUS MISR disabled. 0x1: BUS MISR enabled.
12	TESTGEN_ENABLE	This bit enables/disables the TESTGEN block. 0x0: TESTGEN disabled. 0x1: TESTGEN enabled.
10	VFE_INTERFACE_ENABLE	This bit enables/disables the VFE interface block. 0x0: VFE interface disabled. 0x1: VFE interface enabled.
9	IMEM_MODE_DISABLE	This bit enables/disables the IMEM address generation block that is used in the case of single IMEM instead of pingpong IMEM mode. 0x0: IMEM FIFO Based address generation. 0x1: IMEM Ping Pong address generation.
8	WE_ENABLE	This bit enables/disables the write engine block. 0x0: Write Engine disabled. 0x1: Write Engine enabled.
7	FE_ENABLE	This bit enables/disables the fetch engine block. 0x0: Fetch Engine disabled. 0x1: Fetch Engine enabled.
6	STATS_ENABLE	This bit enables/disables the STATS module in the GEMINI JPEG pipeline. 0x0: STATS disabled. 0x1: STATS enabled.
5	HUFFMAN_ENABLE	This bit enables/disables the HUFFMAN module in the GEMINI JPEG pipeline. 0x0: Huffman disabled. 0x1: Huffman enabled.
4	ZIGZAG_ENABLE	This bit enables/disables the ZIGZAG module in the GEMINI JPEG pipeline. 0x0: ZIGZAG disabled. 0x1: ZIGZAG enabled.
3	RLE_ENABLE	This bit enables/disables the Run Length Encoding module in the GEMINI JPEG pipeline. 0x0: RLE disabled. 0x1: RLE enabled.
2	FSC_ENABLE	This bit enables/disables the File Size Control block. 0x0: FSC disabled. 0x1: FSC enabled.

A_JPEG_CFG (cont.)

Bits	Name	Description
1	QUANTIZER_ENABLE	This bit enables/disables the QUANTIZER module in the GEMINI JPEG pipeline. 0x0: QUANTIZER disabled. 0x1: QUANTIZER enabled.
0	DCT_ENABLE	This bit enables/disables the DCT module in the GEMINI JPEG pipeline. 0x0: DCT disabled. 0x1: DCT enabled.

0x0460000C A_JPEG_REALTIME_CMD

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register allows the ARM to initiate and halt reads for real-time JPEG processing.

SW will write the REALTIME_COMMAND prior to enabling the source of the data to be encoded.

This register allows for stopping the VFE-Gemini interface via an immediate stop or a clean stop on a frame boundary. An immediate stop requires issuing a VFE_INTERFACE_RESET via the JPEG_RESET_CMD before enabling the VFE Interface again.

Note that this register is a command register - writes to this register produced strobe commands to the HW.

A_JPEG_REALTIME_CMD

Bits	Name	Description
1:0	REALTIME_COMMAND	The following commands are used to enable/disable fetches for real-time JPEG processing. 0x0: Disable fetch at the end of the current frame boundary. 0x1: Enable fetch at the start of the next frame boundary. 0x3: Disable fetch immediately.

0x04600010 A_JPEG_REALTIME_STATUS

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0001

This register can be read to determine the state of the VFE interface.

A_JPEG_REALTIME_STATUS

Bits	Name	Description
0	REALTIME_STATUS	This bit indicates the current status of the VFE interface. ' When set (1), the VFE interface is idle. ' When clear (0), the VFE interface is monitoring VFE signals.

14.6.1.2 Gemini interrupt registers

0x04600014 A_JPEG_IRQ_MASK

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0400

This register allows SW to control which set of events will trigger an ARM IRQ.

A_JPEG_IRQ_MASK

Bits	Name	Description
31:0	MASK	This mask is used to enable/disable an interrupt source for the GEMINI interrupt to the ARM. ' When a bit is set (1) , the interrupt source is enabled. ' When the bit is not set (0), the interrupt source is disabled. JPEG_irq_src(0) <= frame_done_irq JPEG_irq_src(1) <= fe_rd_done_irq JPEG_irq_src(2) <= fe_realtime_overflow_irq JPEG_irq_src(3) <= fe_vfe_overflow_irq JPEG_irq_src(4) <= we_y_pingpong_irq JPEG_irq_src(5) <= we_cbcr_pingpong_irq JPEG_irq_src(6) <= we_y_buffer_overflow_irq JPEG_irq_src(7) <= we_cbcr_buffer_overflow_irq JPEG_irq_src(8) <= we_ch0_data_fifo_overflow_irq JPEG_irq_src(9) <= we_ch1_data_fifo_overflow_irq JPEG_irq_src(10) <= reset_ack_irq; JPEG_irq_src(11) <= bus_error_irq; JPEG_irq_src(12) <= violation_irq;

0x04600018 A_JPEG_IRQ_CLEAR

Type: Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_IRQ_CLEAR

Bits	Name	Description
31:0	CLEAR	This register is used to clear an interrupt source. ' Setting (1) a bit clears the interrupt status in JPEG_IRQ_STATUS. ' Clearing (0) a bit has no effect. JPEG_irq_src(0) <= frame_done_irq JPEG_irq_src(1) <= fe_rd_done_irq JPEG_irq_src(2) <= fe_realtime_overflow_irq JPEG_irq_src(3) <= fe_vfe_overflow_irq JPEG_irq_src(4) <= we_y_pingpong_irq JPEG_irq_src(5) <= we_cbcr_pingpong_irq JPEG_irq_src(6) <= we_y_buffer_overflow_irq JPEG_irq_src(7) <= we_cbcr_buffer_overflow_irq JPEG_irq_src(8) <= we_ch0_data_fifo_overflow_irq JPEG_irq_src(9) <= we_ch1_data_fifo_overflow_irq JPEG_irq_src(10) <= reset_ack_irq; JPEG_irq_src(11) <= bus_error_irq; JPEG_irq_src(12) <= violation_irq;

0x0460001C A_JPEG_IRQ_STATUS

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_IRQ_STATUS

Bits	Name	Description
31:0	STATUS	This register shows the raw status of the interrupts that were triggered. JPEG_irq_src(0) <= frame_done_irq JPEG_irq_src(1) <= fe_rd_done_irq JPEG_irq_src(2) <= fe_realtime_overflow_irq JPEG_irq_src(3) <= fe_vfe_overflow_irq JPEG_irq_src(4) <= we_y_pingpong_irq JPEG_irq_src(5) <= we_cbcr_pingpong_irq JPEG_irq_src(6) <= we_y_buffer_overflow_irq JPEG_irq_src(7) <= we_cbcr_buffer_overflow_irq JPEG_irq_src(8) <= we_ch0_data_fifo_overflow_irq JPEG_irq_src(9) <= we_ch1_data_fifo_overflow_irq JPEG_irq_src(10) <= reset_ack_irq; JPEG_irq_src(11) <= bus_error_irq; JPEG_irq_src(12) <= violation_irq;

14.6.1.3 Gemini bus registers

0x04600020 A_JPEG_BUS_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

Not used Halcyon.

A_JPEG_BUS_CFG

Bits	Name	Description
0	OOOWR_ENABLE	This bit indicates to the bus slave that data from the HW core write master out to memory does not need to be processed in a strict order. For AHB based systems, this bit has no effect. 0x0: HW core write master requires the bus slave to process write data requests in the order output by HW core. 0x1: HW core write master does not require the bus slave to process write data requests in the order output by HW core.

0x04600024 A_JPEG_BUS_CMD

Type: Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register is used to halt the bridge.

Note that this register is a command register - writes to this register produced strobe commands to the HW

A_JPEG_BUS_CMD

Bits	Name	Description
0	HALT_REQ	Write a '1' to this bit to halt the bus bridge. The HALT_ACK status bit will be set to '1' after the bridge has stopped transferring data.

0x04600028 A_JPEG_BUS_STATUS

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0002

A_JPEG_BUS_STATUS

Bits	Name	Description
5:4	SLAVE_ID_ERROR	These bits indicate the slave ID of the accessed slaves that is returning an AXI error interrupt. When this error occurs, software will have to clear the AXI error interrupt, apply the AXI halt request, and then reset the AXI bridge upon the receipt of halt acknowledgement to recover from the error condition.
1	BUS_IDLE	This field reports the current state of the bus/bridge. ' When set (1), bus/bridge is IDLE ' When clear (0), bus/bridge is ACTIVE.
0	HALT_ACK	This field reports the bus/bridge acknowledgement following a halt request to the bus/bridge. ' When set (1), halt request acknowledged.

0x0460002C A_JPEG_BUS_MISR_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

The Gemini core implements a 64-bit bus MISR to allow checking of data to and from the core at the core/chip boundary. In the case where the input to the MISR is not 32-bits (APPS bus data or address lines), the HW sets the 32 MSB input values to the MISR to "0" to compute the signature.

A_JPEG_BUS_MISR_CFG

Bits	Name	Description
18:17	MISR_SIG_SEL	This bit determines which bits of the MISR signature to read. 0x0: Read 32 LSBs of the MISR signature. 0x1: Read 32 MSBs of the MISR signature. 0x2: Undefined._1 0x3: Undefined._2
16	MISR_READ_SEL	This bit determines which MISR signature to read. 0x0: Read MISR0 signature. 0x1: Read MISR1 signature.
11:10	MISR1_SRC	When the core is used in an AXI based system, the LSBs of AID of the master for which the MISR is to be computed on is programmed here. When the core is used in an AHB based system, this field takes on the following meaning: 0x0: FE Transaction 0x1: WE Transaction 0x2: Undefined._1 0x3: Undefined._2 0x0: Sample APPS-IMEM bus port. 0x1: Sample APPS bus port. 0x2: Undefined._3 0x3: Undefined._4
9:8	MISR1_INPUT_SEL	Bus MISR Sampling Transaction Mode 0x0: Sample Bus Write Data 0x1: Sample Bus Read Data 0x2: Sample Bus Write Address 0x3: Sample Bus Read Address
3:2	MISR0_SRC	When the core is used in an AXI based system, the LSBs of AID of the master for which the MISR is to be computed on is programmed here. When the core is used in an AHB based system, this field takes on the following meaning: 0x0: FE Transaction 0x1: WE Transaction 0x2: Undefined._1 0x3: Undefined._2 0x0: Sample APPS-IMEM bus port. 0x1: Sample APPS bus port. 0x2: Undefined._3 0x3: Undefined._4

A_JPEG_BUS_MISR_CFG (cont.)

Bits	Name	Description
1:0	MISR0_INPUT_SEL	Bus MISR Sampling Transaction Mode 0x0: Sample Bus Write Data 0x1: Sample Bus Read Data 0x2: Sample Bus Write Address 0x3: Sample Bus Read Address

0x04600030 A_JPEG_BUS_MISR_READ_VALUE

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register returns the lower 32-bits of the bus MISR signature.

A_JPEG_BUS_MISR_READ_VALUE

Bits	Name	Description
31:0	BUS_MISR_VALUE	This register is used to read 32-bits of the bus MISR signature. The 32-bits that are read are determined by the settings in the JPEG_BUS_MISR_CFG register.

14.6.1.4 Status registers

0x04600034 A_JPEG_STATUS_ENCODE_OUTPUT_SIZE

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

Reading this register after receiving the frame_done_irq will return the total number of bytes used to encode the input image. The read value includes the addition of the EOI and restart markers. This register is updated at the end of each frame.

A_JPEG_STATUS_ENCODE_OUTPUT_SIZE

Bits	Name	Description
27:0	OUTPUT_SIZE_BYTES	Total number of bytes used to encode the input frame.

14.6.1.5 Fetch engine registers

The Fetch Engine reads MCUs from memory to feed the JPEG pipeline. It supports reads of 8-bit YCbCr data in H2V2, H2V1, and H1V2 formats.

0x04600038 A_JPEG_FE_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_FE_CFG

Bits	Name	Description
19:18	FE_AREQP_STARVE	This field sets the Master Request Priority (AREQPRIORITY) value to be driven to the FABRIC when the HW determines it is starved for read bandwidth. Not used for Halcyon. 0x0: Normal 0x1: High 0x2: Higher 0x3: Highest
17:16	FE_AREQP_DEFAULT	This field sets the Master Request Priority (AREQPRIORITY) value to be driven to the FABRIC when the HW determines it is not starved for read bandwidth. Not used for Halcyon. 0x0: Normal 0x1: High 0x2: Higher 0x3: Highest
6	CBCR_ORDER	This bit indicates to the HW how CbCr pixels are packed in memory. 0x0: Cb pixel is in the least significant bit of the word. 0x1: Cr pixel is in the least significant bit of the word.
5:4	FE_BURST_LENGTH	This field sets the length of the burst. 0x0: Invalid_1 0x1: burst length 4 0x2: burst length 8 0x3: Invalid_2

A_JPEG_FE_CFG (cont.)

Bits	Name	Description
2:0	BYTE_ORDERING	These bits control the byte swapping in a 64-bit input word for JPEG processing. 0x0: Input Word: [63:0]. 0x1: Input Word: [55:48] & [63:56] & [39:32] & [47:40] & [23:16] & [31:24] & [7:0] & [15:8]. 0x2: Input Word: [47:40] & [39:32] & [63:56] & [55:48] & [15:8] & [7:0] & [31:24] & [23:16]. 0x3: Input Word: [39:32] & [47:40] & [55:48] & [63:56] & [7:0] & [15:8] & [23:16] & [31:24]. 0x4: Input Word: [31:0] &[63:32]. 0x5: Input Word: [23:16] & [31:24] & [7:0] & [15:8] & [55:48] & [63:56] & [39:32] & [47:40]. 0x6: Input Word: [15:8] & [7:0] & [31:24] & [23:16] & [47:40] & [39:32] & [63:56] & [55:48]. 0x7: Input Word: [0:63].

0x0460003C A_JPEG_FE_FRAME_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register is programmed with the input image size to be encoded, in units of MCUs.

This register allows support for up to 512 MCUs for the horizontal frame dimension.

This register allows support for up to 512 MCUs to be programmed for the vertical frame dimension.

A_JPEG_FE_FRAME_CFG

Bits	Name	Description
25:16	FRAME_HEIGHT_MCUS	This field is programmed with number of MCUs in the vertical direction that are in the image to be encoded, minus one. Hence, a frame with a height of N MCUs would be programmed with the value N-1.
9:0	FRAME_WIDTH_MCUS	This field is programmed with number of MCUs in the horizontal direction that are in the image to be encoded, minus one. Hence, a frame with a width of N MCUs would be programmed with the value N-1.

0x04600040 A_JPEG_FE_OUTPUT_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register is used to program the order of the two set sequence of luma/chroma blocks to be output to the JPEG processing pipeline as well as configure the FE to output fetched data in tile format or line format. The JPEG processing pipeline accepts two pixels per cycle, where each pixel is from a different 8x8 block of the same type of block (either both luma or both chroma).

The table below shows the values that could be used to program this register for typical input image formats.

Image Format	PERIOD / BLOCK_PATTERN
H2V1	N = 2 / XX01
H2V2	N = 3 / X011
H1V2	N = 2 / XX01

Block Cycle	Y Pair / CbCr Pair
0	Bit 0
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7

A_JPEG_FE_OUTPUT_CFG

Bits	Name	Description
16	TILE_LINE_FORMAT	This field configures how the data should be read from the FE internal RAMs. For JPEG encode, this field must be set to 0. ’ When set (1), read is line based. ’ When clear (0), read is tile based.
10:8	PERIOD	This value represents the number of 8x8 block cycles the hardware repeats the programmed block pattern sequence. A period of N should be programmed as N-1.

A_JPEG_FE_OUTPUT_CFG (cont.)

Bits	Name	Description
7:0	BLOCK_PATTERN	This field gives the 8x8 block sequence that is fed to the JPEG processing pipeline. ' When set (1), a pair of luma blocks are output to the JPEG processing on the associated block cycle bit. ' When clear (0), a pair of chroma blocks are output to the JPEG processing on the associated block cycle bit.

0x04600044 A_JPEG_FE_FRAME_ROTATION_CFG

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

JPEG frame rotation on the input image is specified by this register.

A_JPEG_FE_FRAME_ROTATION_CFG

Bits	Name	Description
1:0	FE_FRAME_ROTATION	This field specifies how order at which the fetch engine will read data from memory. 0x0: 0 Degree Rotation 0x1: 90 Degree Rotation 0x2: 180 Degree Rotation 0x3: 270 Degree Rotation

0x04600048 A_JPEG_FE_Y_FRAME_ROTATION_START

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

MCU fetch order within a frame is specified by this register. The rotation within a frame is specified by the following equation in terms of the order that MCUs are fetched. This register is intended to be used for off-line JPEG processing and should be programmed to 0 when HW is configured for real-time JPEG encode.

This register should be programmed as follows to perform 0, 90, 180, and 270 degree frame rotation, where FRAME_WIDTH_MCUS and FRAME_HEIGHT_MCUS are the values programmed in the FE_FRAME_CFG registers and Hx = 2 for H2VX input image format, Hx = 1 for H1VX input image format, Vx = 2 for HXV2 input image format, and Vx=1 for HXV1 input image format:

Rotation	FE_START_OFFSET Y Values
0	0
90	FRAME_WIDTH_MCUS * Hx * 8
180	FRAME_WIDTH_MCUS * Hx * 8 + (FRAME_HEIGHT_MCUS * Vx * 8) * (FRAME_WIDTH_MCUS+1) * Hx * 8
270	(FRAME_HEIGHT_MCUS * Vx * 8) * (FRAME_WIDTH_MCUS+1) * Hx * 8

A_JPEG_FE_Y_FRAME_ROTATION_START

Bits	Name	Description
25:0	FE_START_OFFSET	This field specifies the first MCU address location to fetch for the Y component.

0x0460004C A_JPEG_FE_CBCR_FRAME_ROTATION_START

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

MCU rotation within a frame is specified by this register. The rotation within a frame is specified by the following equation in terms of the order that MCUs are fetched. This register is intended to be used for off-line JPEG processing.

This register should be programmed as follows to perform 0, 90, 180, and 270 degree frame rotation, where FRAME_WIDTH_MCUS and FRAME_HEIGHT_MCUS are the values programmed in the FE_FRAME_CFG registers and Hx = 2 and Vx = 1:

Rotation	FE_START_OFFSET CbCr Value
0	0
90	FRAME_WIDTH_MCUS * Hx * 8
180	FRAME_WIDTH_MCUS * Hx * 8 + (FRAME_HEIGHT_MCUS * Vx * 8) * (FRAME_WIDTH_MCUS+1) * Hx * 8
270	(FRAME_HEIGHT_MCUS * Vx * 8) * (FRAME_WIDTH_MCUS+1) * Hx * 8

A_JPEG_FE_CBCR_FRAME_ROTATION_START

Bits	Name	Description
25:0	FE_START_OFFSET	This field specifies the first MCU address location to fetch for the Y component.

0x04600050 A_JPEG_FE_Y_FRAME_JUMP_OFFSET

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

MCU rotation within a frame is specified by this register. The rotation within a frame is specified by the following equation in terms of the order that MCUs are fetched. This register is intended to be used for off-line JPEG processing and should be programmed to 0 when the HW is configured for real-time JPEG.

For 0 or 180 degree rotation, the Y_ROW_JUMP_OFFSET is to be programmed as

8 * Hx * ((FRAME_WIDTH_MCUS+1) * (8*Vx-1) + 1)

For 90 or 270 degree rotation, the Y_ROW_JUMP_OFFSET is to be programmed as

8 * Hx * (FRAME_HEIGHT_MCUS * 8 * Vx * (FRAME_WIDTH_MCUS+1) + 1)

FRAME_HEIGHT_MCUS and FRAME_WIDTH_MCUS are the values programmed in the FE_FRAME_CFG register.

A_JPEG_FE_Y_FRAME_JUMP_OFFSET

Bits	Name	Description
26:0	Y_ROW_JUMP_OFFSET	This field gives the row jump offset for the FE to calculate the address to jump to after reading the luma component of an MCU row.

0x04600054 A_JPEG_FE_CBCR_FRAME_JUMP_OFFSET

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

MCU rotation within a frame is specified by this register. The rotation within a frame is specified by the following equation in terms of the order that MCUs are fetched. This register is intended to be used for off-line JPEG processing and should be programmed to 0 when the HW is configured for real-time JPEG.

For 0 or 180 degree rotation, the CBCR_FRAME_JUMP_OFFSET is to be programmed as

8 * Hx * ((FRAME_WIDTH_MCUS+1) * (8*Vx-1) + 1)

For 90 or 270 degree rotation, the CBCR_FRAME_JUMP_OFFSET is to be programmed as

8 * Hx * (FRAME_HEIGHT_MCUS * 8 * Vx * (FRAME_WIDTH_MCUS+1) + 1)

FRAME_HEIGHT_MCUS and FRAME_WIDTH_MCUS are the values programmed in the FE_FRAME_CFG register. Hx = 2, and Vx = 1 for CBCR_FRAME_JUMP_OFFSET register programming.

A_JPEG_FE_CBCR_FRAME_JUMP_OFFSET

Bits	Name	Description
26:0	CBCR_ROW_JUMP_OFFSET	This field gives the row jump offset for the FE to calculate the address to jump to after reading the chroma component of an MCU row.

0x04600058 A_JPEG_FE_BLOCK_ROTATION_CFG

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

Pixel rotation within an 8x8 block is specified by this register. Three SW parameters define what order the pixel data within a block is pushed to the JPEG pipeline.

The following table lists the programmed values to perform 0, 90, 180, and 270 degree rotation.

Register Field				
	0^o	90^o	180^o	270^o
PIXEL_START_OFFSET	0	7	63	56
PIXEL_H_INCREMENT	+1	+8	-1	-8
PIXEL_V_INCREMENT	+8	-1	-8	+1

A_JPEG_FE_BLOCK_ROTATION_CFG

Bits	Name	Description
25:24	BLOCK_ROTATION	This field specifies the order for which the fetch engine will order the data to the DCT. In general, this field should be programmed to match the JPEG encode orientation. 0x0: 0 Degree Rotation 0x1: 90 Degree Rotation 0x2: 180 Degree Rotation 0x3: 270 Degree Rotation
21:16	PIXEL_START_OFFSET	MCU_FIRST_PIXEL_OFFSET can take values from 0 to 63.
12:8	PIXEL_H_INCREMENT	This field should be programmed to a value between -8 and 8. The value programmed is a two's complement value. -1 would be programmed as 11111, -2 is programmed as 11110,...6 is programmed as 00110, 7 is programmed as 00111.
4:0	PIXEL_V_INCREMENT	This field should be programmed to a value between -8 and 8. The value programmed is a two's complement value. -1 would be programmed as 11111, -2 is programmed as 11110,...6 is programmed as 00110, 7 is programmed as 00111.

0x0460005C A_JPEG_FE_BURST_MASK

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register sets the burst mask on fetches from memory.

A_JPEG_FE_BURST_MASK

Bits	Name	Description
15:8	CBCR_BURST_MASK	Burst mask setting for CbCr fetches.
7:0	Y_BURST_MASK	Burst mask setting for Y fetches.

0x04600060 A_JPEG_FE_Y_WRITE_MASK_0

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register sets the Y write mask on FE burst cycles 0 and 1.

A_JPEG_FE_Y_WRITE_MASK_0

Bits	Name	Description
31:16	Y_WRITE_MASK_1	Write mask setting for Y.
15:0	Y_WRITE_MASK_0	Write mask setting for Y.

0x04600064 A_JPEG_FE_Y_WRITE_MASK_1

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register sets the Y write mask on FE burst cycles 2 and 3.

A_JPEG_FE_Y_WRITE_MASK_1

Bits	Name	Description
31:16	Y_WRITE_MASK_3	Write mask setting for Y.
15:0	Y_WRITE_MASK_2	Write mask setting for Y.

0x04600068 A_JPEG_FE_Y_WRITE_MASK_2

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register sets the Y write mask on FE burst cycles 4 and 5.

A_JPEG_FE_Y_WRITE_MASK_2

Bits	Name	Description
31:16	Y_WRITE_MASK_5	Write mask setting for Y.
15:0	Y_WRITE_MASK_4	Write mask setting for Y.

0x0460006C A_JPEG_FE_Y_WRITE_MASK_3

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register sets the Y write mask on FE burst cycles 6 and 7.

A_JPEG_FE_Y_WRITE_MASK_3

Bits	Name	Description
31:16	Y_WRITE_MASK_7	Write mask setting for Y.
15:0	Y_WRITE_MASK_6	Write mask setting for Y.

0x04600070 A_JPEG_FE_CBCR_WRITE_MASK_0

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register sets the CbCr write mask on FE burst cycles 0 and 1.

A_JPEG_FE_CBCR_WRITE_MASK_0

Bits	Name	Description
31:16	CBCR_WRITE_MASK_1	Write mask setting for CBCR.
15:0	CBCR_WRITE_MASK_0	Write mask setting for CBCR.

0x04600074 A_JPEG_FE_CBCR_WRITE_MASK_1

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register sets the CbCr write mask on FE burst cycles 2 and 3.

A_JPEG_FE_CBCR_WRITE_MASK_1

Bits	Name	Description
31:16	CBCR_WRITE_MASK_3	Write mask setting for CBCR.
15:0	CBCR_WRITE_MASK_2	Write mask setting for CBCR.

0x04600078 A_JPEG_FE_CBCR_WRITE_MASK_2

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register sets the CbCr write mask on FE burst cycles 4 and 5.

A_JPEG_FE_CBCR_WRITE_MASK_2

Bits	Name	Description
31:16	CBCR_WRITE_MASK_5	Write mask setting for CBCR.
15:0	CBCR_WRITE_MASK_4	Write mask setting for CBCR.

0x0460007C A_JPEG_FE_CBCR_WRITE_MASK_3

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register sets the CbCr write mask on FE burst cycles 6 and 7.

A_JPEG_FE_CBCR_WRITE_MASK_3

Bits	Name	Description
31:16	CBCR_WRITE_MASK_7	Write mask setting for CBCR.
15:0	CBCR_WRITE_MASK_6	Write mask setting for CBCR.

0x04600080 A_JPEG_FE_BUFFER_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register is set with the number of MCU rows in each read buffer. For real-time JPEG encode, these registers would be set to either 2 or 1 for MCU_ROWS_Y, and 1 for MCU_ROWS_CBCR.

A_JPEG_FE_BUFFER_CFG

Bits	Name	Description
28:16	CBCR_MCU_ROWS	This field is programmed with the number of MCU Rows minus 1 held in each CbCr Buffer. A value of N rows is programmed as N-1.
12:0	Y_MCU_ROWS	This field is programmed with number of MCU Rows minus 1 held in each Y Buffer. A value of N rows is programmed as N-1.

0x04600084 A_JPEG_FE_Y_PING_ADDR

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

GEMINI must fetch data from IMEM or external memory. The read ping-pong buffers are defined by a starting address and a buffer size. At startup, data is read from the memory location based on the address defined by PING_START_ADDR.

Once the last address defined by JPEG_FE_BUFFER_CFG is reached, the ping-pong buffers automatically switch so that subsequent data is read from to the address defined by the PONG_START_ADDR.

The buffer switch process repeat until the entire frame, as defined in JPEG_FE_CFG has been read.

NOTE When a buffer is switched over, an interrupt is generated. This mechanism allows the definition of the last used buffer to be updated so that it is not overwritten the next time that it is used.

A_JPEG_FE_Y_PING_ADDR

Bits	Name	Description
31:0	FE_Y_PING_START_ADDR	Ping buffer start address. Must be a multiple of 8.

0x04600088 A_JPEG_FE_Y_PONG_ADDR

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_FE_Y_PONG_ADDR

Bits	Name	Description
31:0	FE_Y_PONG_START_ADDR	Pong buffer start address. Must be a multiple of 8.

0x0460008C A_JPEG_FE_CBCR_PING_ADDR

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_FE_CBCR_PING_ADDR

Bits	Name	Description
31:0	FE_CBCR_PING_START_ADDR	Ping buffer start address. Must be a multiple of 8.

0x04600090 A_JPEG_FE_CBCR_PONG_ADDR

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_FE_CBCR_PONG_ADDR

Bits	Name	Description
31:0	FE_CBCR_PONG_START_ADDR	Pong buffer start address. Must be a multiple of 8.

0x04600094 A_JPEG_FE_CMD

Type: Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register allows SW the capability to reset the memory pointers to where data is read from. It also initiates HW fetches for off-line JPEG encode.

Note that this register is a command register - writes to this register produced strobe commands to the HW

A_JPEG_FE_CMD

Bits	Name	Description
1	FE_READ_GO_CMD	Writing to this bit initiates fetches for off-line JPEG processing. ' When set (1), triggers a request to fetch data for off-line JPEG encoding. ' Clearing the bit (0), has no effect.
0	FE_BUFFER_RELOAD_CMD	This field is used to reload and reset the read channel address to start from the PING address buffer. The value in this field is strictly a strobe (pulse) based value, and there is no registering of this value. ' When set (1), triggers a request to reset buffer pointers. ' Clearing the bit (0), has no effect.

14.6.1.6 Write Engine registers

0x04600098 A_JPEG_WE_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

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A_JPEG_WE_CFG

Bits	Name	Description
19:18	WE_AREQP_STARVE	This field sets the Master Request Priority (AREQPRIORITY) value to be driven to the FABRIC when the HW determines it is starved for write bandwidth. Not used for Halcyon. 0x0: Normal 0x1: High 0x2: Higher 0x3: Highest

A_JPEG_WE_CFG (cont.)

Bits	Name	Description
17:16	WE_AREQP_DEFAULT	This field sets the Master Request Priority (AREQPRIORITY) value to be driven to the FABRIC when the HW determines it is not starved for write bandwidth. Not used for Halcyon. 0x0: Normal 0x1: High 0x2: Higher 0x3: Highest
11	WE_OUTPUT_DISABLE	This field is used to disable the WE output to the bridge. ’ When set (1), WE output to bridge is disabled. ’ When clear(0), WE output to bridge is enabled.
10	WE_BS_DISABLE	This field is used to disable the byte stuff function. This field should always be programmed to "0" when the HW is configured for JPEG encoding. For frame rotation this bit must be programmed to "1". ’ When set (1), WE byte stuff/marker insert is disabled. ’ When clear(0), WE byte stuff/marker insert is enabled.
9:8	WE_BP_INPUT_SEL	This field sets the input to the WE 64-bit bitpacker. This field should be programmed to "00" when the HW is configured for JPEG encoding or Frame Rotation. Currently this is used for debug purposes only. 0x0: WE byte stuff/marker insert output 0x1: Ch0 huffman output 0x2: Ch1 huffman output 0x3: Not defined
5:4	WE_BURST_LENGTH	This field sets the length of the burst. This value must be set to "00" for inline frame rotation. 0x0: burst length 2 (Not supported for 32-bit bus systems) 0x1: burst length 4 0x2: burst length 8 0x3: burst length 16
2:0	BYTE_ORDERING	These bits control the byte swapping in one word of the compressed output. 0x0: Output Word: [63:0]. 0x1: Output Word: [55:48] & [63:56] & [39:32] & [47:40] & [23:16] & [31:24] & [7:0] & [15:8]. 0x2: Output Word: [47:40] & [39:32] & [63:56] & [55:48] & [15:8] & [7:0] & [31:24] & [23:16]. 0x3: Output Word: [39:32] & [47:40] & [55:48] & [63:56] & [7:0] & [15:8] & [23:16] & [31:24]. 0x4: Output Word: [31:0] &[63:32]. 0x5: Output Word: [23:16] & [31:24] & [7:0] & [15:8] & [55:48] & [63:56] & [39:32] & [47:40]. 0x6: Output Word: [15:8] & [7:0] & [31:24] & [23:16] & [47:40] & [39:32] & [63:56] & [55:48]. 0x7: Output Word: [0:63].

0x0460009C A_JPEG_WE_FRAME_ROTATION_CFG

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

JPEG frame rotation on the input image is specified by this register.

A_JPEG_WE_FRAME_ROTATION_CFG

Bits	Name	Description
1:0	WE_FRAME_ROTATION	This field specifies how order at which the write engine will write data to memory. 0x0: 0 Degree Rotation 0x1: 90 Degree Rotation 0x2: 180 Degree Rotation 0x3: 270 Degree Rotation

0x046000A0 A_JPEG_WE_Y_FRAME_ROTATION_START0

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

This register should be programmed as follows to perform 0, 90, 180, and 270 degree frame rotation, where FRAME_WIDTH_MCUS and FRAME_HEIGHT_MCUS are the values programmed in the FE_FRAME_CFG registers and Hx = 2 for H2VX input image format, Hx = 1 for H1VX input image format, Vx = 2 for HXV2 input image format, and Vx=1 for HXV1 input image format:

Rotation	H2V1	H2V2
0	0	0
90	FRAME_HEIGHT_MCUS *(FRAME_WIDTH_MCUS-8)	FRAME_HEIGHT_MCUS *(FRAME_WIDTH_MCUS-8)
180	FRAME_WIDTH_MCUS -16	FRAME_WIDTH_MCUS *8
270	FRAME_HEIGHT_MCUS -16	FRAME_HEIGHT_MCUS-16

A_JPEG_WE_Y_FRAME_ROTATION_START0

Bits	Name	Description
23:3	WE_Y_START_OFFSET0	This field specifies the first MCU address location to write to for the Y component.

0x046000A4 A_JPEG_WE_Y_FRAME_ROTATION_START1

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

This register should be programmed as follows to perform 0, 90, 180, and 270 degree frame rotation, where FRAME_WIDTH_MCUS and FRAME_HEIGHT_MCUS are the values programmed in the FE_FRAME_CFG registers and Hx = 2 for H2VX input image format, Hx = 1 for H1VX input image format, Vx = 2 for HXV2 input image format, and Vx=1 for HXV1 input image format:

Rotation	H2V1	H2V2
0	0	0
90	FRAME_HEIGHT_MCUS *(FRAME_WIDTH_MCUS-8)	FRAME_HEIGHT_MCUS *(FRAME_WIDTH_MCUS-8)
180	FRAME_WIDTH_MCUS -16	FRAME_WIDTH_MCUS *8
270	FRAME_HEIGHT_MCUS -16	FRAME_HEIGHT_MCUS-16

A_JPEG_WE_Y_FRAME_ROTATION_START1

Bits	Name	Description
23:3	WE_Y_START_OFFSET1	This field specifies the first MCU address location to write to for the Y component.

0x046000A8 A_JPEG_WE_CBCR_FRAME_ROTATION_START0

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

Viewfinder frame rotation is specified by this register.

This register should be programmed as follows to perform 0, 90, 180, and 270 degree frame rotation, where FRAME_WIDTH_MCUS and FRAME_HEIGHT_MCUS are the values programmed in the FE_FRAME_CFG registers and Hx = 2 and Vx = 1:

Rotation	WE_START_OFFSET CbCr Value
0	0
90	FRAME_WIDTH_MCUS * Hx * 8
180	FRAME_WIDTH_MCUS * Hx * 8 + (FRAME_HEIGHT_MCUS * Vx * 8) * (FRAME_WIDTH_MCUS+1) * Hx * 8
270	(FRAME_HEIGHT_MCUS * Vx * 8) * (FRAME_WIDTH_MCUS+1) * Hx * 8

A_JPEG_WE_CBCR_FRAME_ROTATION_START0

Bits	Name	Description
23:3	WE_CBCR_START_OFFSET0	This field specifies the first MCU address location to write the Ycomponent.

0x046000AC A_JPEG_WE_CBCR_FRAME_ROTATION_START1

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

Viewfinder frame rotation is specified by this register.

This register should be programmed as follows to perform 0, 90, 180, and 270 degree frame rotation, where FRAME_WIDTH_MCUS and FRAME_HEIGHT_MCUS are the values programmed in the FE_FRAME_CFG registers and Hx = 2 and Vx = 1:

Rotation	WE_START_OFFSET CbCr Value
0	0
90	FRAME_WIDTH_MCUS * Hx * 8
180	FRAME_WIDTH_MCUS * Hx * 8 + (FRAME_HEIGHT_MCUS * Vx * 8) * (FRAME_WIDTH_MCUS+1) * Hx * 8
270	(FRAME_HEIGHT_MCUS * Vx * 8) * (FRAME_WIDTH_MCUS+1) * Hx * 8

A_JPEG_WE_CBCR_FRAME_ROTATION_START1

Bits	Name	Description
23:3	WE_CBCR_START_OFFSET1	This field specifies the first MCU address location to write the Ycomponent.

0x046000B0 A_JPEG_WE_Y_FRAME_JUMP_OFFSET0

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

Viewfinder frame rotation is specified by this register.

Table to be added here.

A_JPEG_WE_Y_FRAME_JUMP_OFFSET0

Bits	Name	Description
23:3	WE_Y_JUMP_OFFSET0	This field gives the row jump offset for the WE to calculate the address to jump to after reading the luma component of an MCU row.

0x046000B4 A_JPEG_WE_Y_FRAME_JUMP_OFFSET1

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

Viewfinder frame rotation is specified by this register.

Table to be added here.

A_JPEG_WE_Y_FRAME_JUMP_OFFSET1

Bits	Name	Description
23:3	WE_Y_JUMP_OFFSET1	This field gives the row jump offset for the WE to calculate the address to jump to after reading the luma component of an MCU row.

0x046000B8 A_JPEG_WE_CBCR_FRAME_JUMP_OFFSET0

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

Viewfinder frame rotation is specified by this register

Table to be added here.

A_JPEG_WE_CBCR_FRAME_JUMP_OFFSET0

Bits	Name	Description
23:3	WE_CBCR_JUMP_OFFSET0	This field gives the row jump offset for the WE to calculate the address to jump to after reading the chroma component of an MCU row.

0x046000BC A_JPEG_WE_CBCR_FRAME_JUMP_OFFSET1

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

Viewfinder frame rotation is specified by this register

Table to be added here.

A_JPEG_WE_CBCR_FRAME_JUMP_OFFSET1

Bits	Name	Description
23:3	WE_CBCR_JUMP_OFFSET1	This field gives the row jump offset for the WE to calculate the address to jump to after reading the chroma component of an MCU row.

0x046000C0 A_JPEG_WE_Y_THRESHOLD

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

This threshold is used to determine when to stall and de-assert stall on reads during JPEG encoding or viewfinder frame rotation. If the buffer level within the WE exceeds the threshold, the HW will stall data from the FE on an MCU boundary.

Recommended HW settings for this register when the HW is configured for JEPG encoding are given below:

WE_THRESHOLD Field	Real-time Setting	Offline Setting
WE_ASSERT_STALL_TH	0x1FF	0x190
WE_DEASSERT_STALL_TH	0x1FF	0x16A

A_JPEG_WE_Y_THRESHOLD

Bits	Name	Description
24:16	WE_DEASSERT_STALL_TH	Threshold is specified in 16 byte increments. HW will de-assert stall upon detection of buffer level falling below this threshold.
8:0	WE_ASSERT_STALL_TH	Threshold is specified in 16 byte increments. HW will assert stall upon detection of buffer level exceeding this threshold.

0x046000C4 A_JPEG_WE_CBCR_THRESHOLD

Type: Read/Write
Clock: REG_CLK
Reset State: 0x0000 0000

This threshold is used to determine when to stall and de-assert stall on chroma reads during viewfinder rotation. If the buffer level within the WE exceeds the threshold, the HW will stall data from the FE on an MCU boundary.

Recommended HW settings for this register are given below:

WE_THRESHOLD Field	Real-time Setting	Offline Setting
WE_ASSERT_STALL_TH	0x1FF	0x190
WE_DEASSERT_STALL_TH	0x1FF	0x16A

A_JPEG_WE_CBCR_THRESHOLD

Bits	Name	Description
24:16	WE_DEASSERT_STALL_TH	Threshold is specified in 16 byte increments. HW will de-assert stall upon detection of buffer level falling below this threshold.
8:0	WE_ASSERT_STALL_TH	Threshold is specified in 16 byte increments. HW will assert stall upon detection of buffer level exceeding this threshold.

0x046000C8 A_JPEG_WE_Y_PING_BUFFER_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

Buffer write pointers are switched between the ping and pong buffers when the buffers are full as determined by the BUFFER_LENGTH field. Write pointers will not be updated on frame boundaries. For JPEG encoding, only the WE_Y_PING_ADDR and WE_CBCR_PONG_ADDR buffers are used to determine where the resulting bit stream generated by the HW is written.

During JPEG encode, there may be potentially more than one encoded frame per buffer. See Section 2.2 for how SW can determine the location of frames within a single/multiple buffers based on hardware reporting. The Y Ping and CbCr Ping buffers are the same size, and the Y Pong and Y CbCr buffers are the same size. The Ping and Pong Buffer sizes do not have to be the same size.The value programmed in this register must be a multiple of 4*WE_BURST_LENGTH bytes. For example, when the WE_BURST_LENGTH is set to select a burst of 4, the buffer length must be a multiple of 4*4=16.

A_JPEG_WE_Y_PING_BUFFER_CFG

Bits	Name	Description
22:0	WE_BUFFER_LENGTH	This field sets the length of the ping buffer in bytes.

0x046000CC A_JPEG_WE_Y_PONG_BUFFER_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

The value programmed in this register must be a multiple of 16 bytes.

A_JPEG_WE_Y_PONG_BUFFER_CFG

Bits	Name	Description
22:0	WE_BUFFER_LENGTH	This field sets the length of the pong buffer in bytes.

0x046000D0 A_JPEG_WE_CBCR_PING_BUFFER_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

The value programmed in this register must be a multiple of 16 bytes.

A_JPEG_WE_CBCR_PING_BUFFER_CFG

Bits	Name	Description
22:0	WE_BUFFER_LENGTH	This field sets the length of the ping buffer in bytes.

0x046000D4 A_JPEG_WE_CBCR_PONG_BUFFER_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

The value programmed in this register must be a multiple of 16 bytes.

A_JPEG_WE_CBCR_PONG_BUFFER_CFG

Bits	Name	Description
22:0	WE_BUFFER_LENGTH	This field sets the length of the pong buffer in bytes.

0x046000D8 A_JPEG_WE_Y_PING_ADDR

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_WE_Y_PING_ADDR

Bits	Name	Description
31:3	WE_Y_PING_START_ADDR	Bus address at the start of the ping buffer. Must be a multiple of 8. This register is double buffered.

0x046000DC A_JPEG_WE_Y_PONG_ADDR

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_WE_Y_PONG_ADDR

Bits	Name	Description
31:3	WE_Y_PONG_START_ADDR	Bus address at the start of the ping buffer. Must be a multiple of 8. This register is double buffered

0x046000E0 A_JPEG_WE_CBCR_PING_ADDR

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_WE_CBCR_PING_ADDR

Bits	Name	Description
31:3	WE_CBCR_PING_START_ADDR	Bus address at the start of the ping buffer. Must be a multiple of 8.

0x046000E4 A_JPEG_WE_CBCR_PONG_ADDR

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_WE_CBCR_PONG_ADDR

Bits	Name	Description
31:3	WE_CBCR_PONG_START_ADDR	Bus address at the start of the ping buffer. Must be a multiple of 8.

0x046000E8 A_JPEG_WE_Y_UB_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

Gemini implements a unified buffer. The dimension of the unified buffer is 512x128 bits or 8KB. Each intended active write channel must have its latency buffer pre-allocated by software prior to being active. The allocation of latency buffer is done by programming JPEG_WE_*_UB_CFG registers. Each write channel must not overwrite the other write channel's buffer location. When JPEG mode is used, this register should be configured with WE_Y_UB_OFFSET set to 0 and WE_Y_UB_DEPTH set to the maximum possible value.

A_JPEG_WE_Y_UB_CFG

Bits	Name	Description
24:16	WE_Y_UB_DEPTH	This field sets the unified buffer offset from address zero of unified buffer. The value is programmed starting from 0. Program a value of n means n. Minimum is 0 double word offset (or the first address location of unified buffer) and maximum is 511 double word offset (or the last address location of unified buffer).
8:0	WE_Y_UB_OFFSET	This field sets the unified buffer depth in terms of double words (128 bits). The value is programmed starting from 0. Program a value of N means (N + 1). Minimum is 1 double word and maximum is 512 double words.

0x046000EC A_JPEG_WE_CBCR_UB_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

When JPEG mode is used, the register values in this register are ignored by the HW.

A_JPEG_WE_CBCR_UB_CFG

Bits	Name	Description
24:16	WE_CBCR_UB_DEPTH	This field sets the unified buffer offset from address zero of unified buffer. The value is programmed starting from 0. Program a value of n means n. Minimum is 0 double word offset (or the first address location of unified buffer) and maximum is 511 double word offset (or the last address location of unified buffer).
8:0	WE_CBCR_UB_OFFSET	This field sets the unified buffer depth in terms of double words (128 bits). The value is programmed starting from 0. Program a value of N means (N + 1). Minimum is 1 double word and maximum is 512 double words.

0x046000F0 A_JPEG_WE_CMD

Type: Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register allows SW the capability to reset the memory pointers to where data is written to.

Note that this register is a command register - writes to this register produced strobe commands to the HW

A_JPEG_WE_CMD

Bits	Name	Description
0	WE_BUFFER_RELOAD_CMD	This field is used to reload and reset the write channel address to start from the PING address buffer. The value in this field is strictly a strobe (pulse) based value, and there is no registering of this value.

14.6.1.7 JPEG Encode registers

0x046000F4 A_JPEG_ENCODE_CFG

Type: Write/Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register configures the JPEG encode path. The Huffman encode look up table is controlled by this register. This register also controls the restart marker interval. Allowable restart marker intervals are from 0 to 65535.

A_JPEG_ENCODE_CFG

Bits	Name	Description
16	HUFFMAN_SEL	This field determines whether HW uses a default Huffman table or a customized Huffman table. If a custom Huffman table is to be used, SW must load the Huffman table via the DMI registers. If the default Huffman table is to be used, there is no need for software to load the Huffman table. ' When set (1), HW selects a customized Huffman table for JPEG processing. ' When clear (0), HW selects the default Huffman table for JPEG processing.
15:0	RST_MARKER_PERIOD	Number of MCUs between Restart (RST) marker insertion. When programmed to 0000, restart marker insertion is disabled. A value of N MCUs between restart markers is programmed as N.

14.6.1.8 Statistics registers

This section describes the registers which can be used for JPEG statistics collection. For reference, in a typical 8MP image, there are approximately 127,896 8x8 blocks. Hence, there are 127,896 Y DC coefficients, 127,896 CbCr DC coefficients, 8,057,448 Y AC coefficients, and 8,057,448 CbCr AC coefficients.

0x046000F8 A_JPEG_ENCODE_STATS_DC_BITS_Y

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

Reading this register after receiving the frame_done_irq will return the total number of bits used to encode the luma DC coefficients.

A_JPEG_ENCODE_STATS_DC_BITS_Y

Bits	Name	Description
28:0	ENC_DC_BITS_Y	Number of bits expanded on coding the DC coefficients.

0x046000FC A_JPEG_ENCODE_STATS_DC_BITS_CBCR

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

Reading this register after receiving the frame_done_irq will return the total number of bits used to encode the chroma DC coefficients.

A_JPEG_ENCODE_STATS_DC_BITS_CBCR

Bits	Name	Description
28:0	ENC_DC_BITS_CBCR	Number of bits expanded on coding the chroma DC coefficients.

0x04600100 A_JPEG_ENCODE_STATS_AC_BITS_Y

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

Reading this register after receiving the frame_done_irq will return the total number of bits used to encode the luma AC coefficients. With a 512 x 512 H2V2 MCU image, there are approximately 210 * 210 * 6 * 26 * 23 = 6 * 229 bits.

A_JPEG_ENCODE_STATS_AC_BITS_Y

Bits	Name	Description
29:0	ENC_AC_BITS_Y	Number of bits expanded on coding the AC luma coefficients.

0x04600104 A_JPEG_ENCODE_STATS_AC_BITS_CBCR

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

Reading this register after receiving the frame_done_irq will return the total number of bits used to encode the chroma AC coefficients.

A_JPEG_ENCODE_STATS_AC_BITS_CBCR

Bits	Name	Description
29:0	ENC_AC_BITS_CBCR	Number of bits expanded on coding the AC chroma coefficients.

0x04600108 A_JPEG_ENCODE_STATS_NONZERO_AC_Y

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

Reading this register after receiving the frame_done_irq will return the total number of nonzero luma AC coefficients. A maximum of 67,108,864 non-zero coefficients can be reported by this register.

A_JPEG_ENCODE_STATS_NONZERO_AC_Y

Bits	Name	Description
25:0	ENC_NONZERO_AC_Y	Number of non-zero AC coefficients for luma.

0x0460010C A_JPEG_ENCODE_STATS_NONZERO_AC_CBCR

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

Reading this register after receiving the frame_done_irq will return the total number of nonzero chroma AC coefficients. A maximum of 67,108,864 non-zero coefficients can be reported by this register.

A_JPEG_ENCODE_STATS_NONZERO_AC_CBCR

Bits	Name	Description
25:0	ENC_NONZERO_AC_CBCR	Number of non-zero AC coefficients for chroma.

14.6.1.9 File Size Control registers

This section describes the registers that are used for file size control. These registers need to be programmed only when File Size Control functionality is enabled. With File Size Control, the image is divided into 16 horizontal or 16 vertical regions. SW must specify the bit budget for each of these regions, as well as the number of MCU rows per region.

0x04600110 A_JPEG_ENCODE_FSC_REGION_SIZE

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register establishes the region size in number of MCU rows.

A_JPEG_ENCODE_FSC_REGION_SIZE

Bits	Name	Description
8	HV_REGION	This field determines whether the vertical sequencing. ' When set (1), regions are vertical with respect to the original input image orientation. ' When clear (0), regions are horizontal with respect to the original input image orientation.
4:0	REGION_SIZE	This value is programmed to the number of MCU rows. If there are N MCU rows per region, this register should be programmed as N-1. This implies that there is a minimum setting on 1 MCU row per region.

0x04600114 A_JPEG_ENCODE_FSC_BUDGET_0

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register establishes the bit budget for regions 0 through 3. If a field within the budget register is programmed with the value N, the bit budget is 16*N for the region.

A_JPEG_ENCODE_FSC_BUDGET_0

Bits	Name	Description
31:24	BUDGET_REGION3	These bits specify the bit budget for region 3.
23:16	BUDGET_REGION2	These bits specify the bit budget for region 2.
15:8	BUDGET_REGION1	These bits specify the bit budget for region 1.
7:0	BUDGET_REGION0	These bits specify the bit budget for region 0.

0x04600118 A_JPEG_ENCODE_FSC_BUDGET_1

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register establishes the bit budget for regions 4 through 7.

A_JPEG_ENCODE_FSC_BUDGET_1

Bits	Name	Description
31:24	BUDGET_REGION7	These bits specify the bit budget for region 7.
23:16	BUDGET_REGION6	These bits specify the bit budget for region 6.
15:8	BUDGET_REGION5	These bits specify the bit budget for region 5.
7:0	BUDGET_REGION4	These bits specify the bit budget for region 4.

0x0460011C A_JPEG_ENCODE_FSC_BUDGET_2

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register establishes the bit budget for regions 8 through 11.

A_JPEG_ENCODE_FSC_BUDGET_2

Bits	Name	Description
31:24	BUDGET_REGION11	These bits specify the bit budget for region 11.
23:16	BUDGET_REGION10	These bits specify the bit budget for region 10.
15:8	BUDGET_REGION9	These bits specify the bit budget for region 9.
7:0	BUDGET_REGION8	These bits specify the bit budget for region 8.

0x04600120 A_JPEG_ENCODE_FSC_BUDGET_3

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register establishes the bit budget for regions 12 through 15.

A_JPEG_ENCODE_FSC_BUDGET_3

Bits	Name	Description
31:24	BUDGET_REGION15	These bits specify the bit budget for region 15.
23:16	BUDGET_REGION14	These bits specify the bit budget for region 14.
15:8	BUDGET_REGION13	These bits specify the bit budget for region 13.
7:0	BUDGET_REGION12	These bits specify the bit budget for region 12.

14.6.1.10 DMI registers

SW loads the quantization and Huffman LUTs. These tables are loaded via the DMI registers.

0x04600124 A_JPEG_DMI_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

HW implementation requires the used of two identical Huffman LUTS. Writing to either of the Huffman LUTs results in writing both LUTS simultaneously. HW reads from each Huffman LUT independently.

A_JPEG_DMI_CFG

Bits	Name	Description
2	AUTO_INC_EN	Setting (1) this bit auto-increments JPEG_DMI_ADDR by 1 anytime JPEG_DMI_DATA_LO is written to or read from.
1:0	DMI_RAM_SEL	This bit field is used to select the GEMINI local memory for direct memory access. 0x0: No memory selected 0x1: Quantization LUT RAM 0x2: Huffman LUT0 RAM 0x3: Huffman LUT1 RAM

0x04600128 A_JPEG_DMI_ADDR

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_DMI_ADDR

Bits	Name	Description
9:0	DMI_ADDR	This bit field specifies the address for the RAM selected by DMI_RAM_SEL.

0x0460012C A_JPEG_DMI_DATA_LO

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_DMI_DATA_LO

Bits	Name	Description
31:0	DMI_DATA_LO	This register represents the lower 32 bits of the DMI data. When this register is written, the value of this register is written into the lower 32 bits of the memory selected by JPEG_DMI_CFG. If the memory is wider than 32 bits, the upper 32 bits can be prepared by writing to JPEG_DMI_DATA_HI. When this register is read, it returns the lower 32 bits of the memory data.

14.6.1.11 Test generator registers

0x04600130 A_JPEG_TESTGEN_CFG

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A hardware test generator resides at the input to the JPEG pipeline. In test mode, the output of the test generator is used to drive the JPEG pipeline as opposed to the Fetch Engine. This register configures the HW testgen block.

A_JPEG_TESTGEN_CFG

Bits	Name	Description
28:20	TESTGEN_BLOCKS	Number of 8x8 pixel blocks to generate and feed to JPEG pipeline. This value should always be programmed to an even value.
18	TESTGEN_DC_MODE	This field selects whether the DC input value to the testgen block is generated randomly every 8x8 block or whether it is fed directly from the software regs. 0x0: HW controlled 0x1: SW register controlled
17	TESTGEN_AC_MODE	This field selects whether the AC input value to the testgen block is generated randomly every 8x8 block or whether it is fed directly from the software regs. 0x0: HW controlled 0x1: SW register controlled

A_JPEG_TESTGEN_CFG (cont.)

Bits	Name	Description
15:8	TESTGEN_DC	This field is the 8-bit signed DC value which the testgen will use to compute each pixel value when testgen_dc_mode =1.
6:0	TESTGEN_AC_MAG	This field is the 7-bit AC magnitude which the testgen will use to compute each pixel value when testgen_ac_mode =1.

0x04600134 A_JPEG_TESTGEN_SEED

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A hardware test generator resides at the input to the JPEG pipeline. In test mode, the output of the test generator is used to drive the JPEG pipeline as opposed to the Fetch Engine. This register sets the seed of the PN generator.

A_JPEG_TESTGEN_SEED

Bits	Name	Description
15:0	TESTGEN_SEED	The field is programmed with the seed value for the TESTGEN PN pixel generator.

0x04600138 A_JPEG_TESTGEN_CMD

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_TESTGEN_CMD

Bits	Name	Description
0	TESTGEN_START_CMD	This field initiates the test generator machine. The value in this field is strictly a strobe (pulse) based value, and there is no registering of this value. 0x0: Clearing this bit has no effect 0x1: Trigger a request to start the HW test generator

14.6.1.12 JPEG Performance Monitor and Debug Registers

0x0460013C A_JPEG_MONITOR_STATUS_0

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0007 ffff

This register returns the minimum number of JPEG clock cycles between MCU strobes from the VFE Interface. To clear this value, SW must reset the VFE interface.

The worst case buffer is 16 lines deep, and the longest line time is given with a 2MP sensor. At 15 fps, each line would be 66ms/1200 = 55us in duration. An MCU strobe would be expected every 16*55us = .88 ms. The JPEG clock is specified to run at max frequency of 170 MHz, or a clock period of 5.8ns. Hence, there are .88ms/5.8ns = 151,724 JPEG clock cycles expected between MCU strobes. This register supports up a count up to 524,288 clock cycles.

A_JPEG_MONITOR_STATUS_0

Bits	Name	Description
18:0	STB_TO_STB_CNT	Minimum number of JPEG clock cycles between MCU strobes.

0x04600140 A_JPEG_MONITOR_STATUS_1

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register returns the maximum WE FIFO usage during encoding as well as additional status bits. The FIFO level value fields are updated at the end of the frame. The underflow and overflow bits are set should any of the events occur. The event status bits are not expected during normal operation.

A_JPEG_MONITOR_STATUS_1

Bits	Name	Description
19	EOI_OVERFLOW	When '1', this bit indicates that the EOI strobe coming out of the bus_wr_intf may be corrupted. This is caused when 2 EOI tokens are present in the Unified Buffer at any given time.
18	EOF_OVERFLOW	When '1', this bit indicates that a PING PONG buffer switch may have been corrupted. This is caused when two ping-pong buffer switch tokens are present in the unified buffer at any given time.
17	CH1_FIFO_UNDERFLOW	When '1', this status bit indicates an underflow condition occurred on the ch1 WE FIFO.

A_JPEG_MONITOR_STATUS_1 (cont.)

Bits	Name	Description
16	CH0_FIFO_UNDERFLOW	When '1', this status bit indicates an underflow condition occurred on the ch0 WE FIFO.
13:8	CH1_FIFO_LEVEL	Max number of words held in ch1 WE FIFO.
5:0	CH0_FIFO_LEVEL	Max number of words held in ch0 WE FIFO.

0x04600144 A_JPEG_MONITOR_STATUS_2

Type: Read
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register reports the number of read transactions to IMEM and the maximum total number of bus cycles required for the reported number of read transactions. The value reported is over one IMEM buffer period. This register should be read only when the bus is inactive.

A_JPEG_MONITOR_STATUS_2

Bits	Name	Description
31:14	TRANS_BUS_CYCLES	Bus transaction cycles over one IMEM buffer period
13:0	TRANS_CNT	Bus transaction count over one IMEM buffer period

14.6.1.13 Test bus registers

0x04600148 A_JPEG_TESTBUS_SEL

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

This register controls the selection of the GEMINI test bus output. The top level of the chip must also be configured to MUX out the proper test bus to the chip pads.

A_JPEG_TESTBUS_SEL

Bits	Name	Description
9:8	DOMAIN_SEL	These bits set the selection for the output on the TESTBUS for visibility and debugging. 0x0: "01124110" 0x3: "FEEDBEEF" 0x1: JPEG_CLK Test Bus 0x2: BUS_CLK Test Bus
4:0	BUS_SEL	These bits select which bus on a clock domain is output on the TESTBUS. For JPEG CLK testbus, the selections are: For BUS CLK testbus, the selections are: 5'b00011: 5'b00100: 5'b00101: 5'b00110: 5'b00111: 5'b01000: 5'b01001: 5'b01010: 5'b01011: 5'b01100: 0x0: VFE Interface Block Test Bus 0x1: Fetch Engine Block Test Bus 0 0x2: Fetch Engine Block Test Bus 1 0x3: Fetch Engine Block Test Bus 2 0x4: DCT Block Test Bus 0x5: Quantizer Block Test Bus 0x6: FSC Block Test Bus 0x7: ZigZag Block Test Bus 0x8: Run Length Encoder Block Test Bus 0x9: Huffman Block Test Bus 0xA: Statistics Block Test Bus 0xB: Write Engine Block Test Bus 0 0xC: Write Engine Block Test Bus 1 0xD: Write Engine Block Test Bus 2 0xE: Write Engine Block Test Bus 3 0xF: IRQ Block 0x10: IMEM FIFO Addressing Channel 0 Test Bus 0x11: IMEM FIFO Addressing Channel 1 Test Bus 0x0: Bridge Testbus 1 0x1: Bridge Testbus 2 0x2: Bus MISR Test Bus

0x0460014C A_JPEG_SPARE

Type: Read/Write
Clock: REG_CLK
Read Wait States:0
Reset State: 0x0000 0000

A_JPEG_SPARE

Bits	Name	Description
31:0	SPARE	Spare register

14.7 MIPI DSI1 Registers (0x04700000 MIPI_DSI_1_BASE)

0x04700000 MIPI_DSI_1_DSI1_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Control Register provides general control to the protocol, lane management and PHY layers.

MIPI_DSI_1_DSI1_CTRL

Bits	Name	Description
31	RESERVED_1	
30	NEW_INTERLEAVE_MODE_EN	unused (Enable new interleave mode with H/W arbitration between long commands and BLLP periods.) 0x0: disable 0x1: enable
29:28	PACKET_BYTE_MSB_LSB_FLIP	Swap the bit ordering of each byte of a packet 0x0: no swap (bit 0 is lsb, bit 7 is msb) 0x1: swap each byte of payload (bit 0 is msb, bit 7 is lsb) 0x2: swap each byte of packet (bit 0 is msb, bit 7 is lsb) 0x3: reserved
27	RESERVED_2	
26	DEBUG_MODE_EN	Enable debug mode for supporting non-compliant panels 0x0: disable 0x1: enable
25	RESERVED_3	
24	CRC_CHK_EN	Enable CRC verification of the received packets 0x0: Disable 0x1: Enable
23:21	RESERVED_4	
20	ECC_CHK_EN	Enable ECC verification of the received packets 0x0: Disable 0x1: Enable
19:9	RESERVED_5	
8	CLKLN_EN	Enable clock lane of the PHY 0x0: Disable DSI PHY Clock Lane 0x1: Enable DSI PHY Clock Lane
7	DLN3_EN	Enable data lane 3 of the PHY 0x0: Disable DSI PHY Data Lane 3 0x1: Enable DSI PHY Data Lane 3

MIPI_DSI_1_DSI1_CTRL (cont.)

Bits	Name	Description
6	DLN2_EN	Enable data lane 2 of the PHY 0x0: Disable DSI PHY Data Lane 2 0x1: Enable DSI PHY Data Lane 2
5	DLN1_EN	Enable data lane 1 of the PHY 0x0: Disable DSI PHY Data Lane 1 0x1: Enable DSI PHY Data Lane 1
4	DLN0_EN	Enable data lane 0 of the PHY 0x0: Disable DSI PHY Data Lane 0 0x1: Enable DSI PHY Data Lane 0
3	RESERVED_6	
2	CMD_MODE_EN	Enable the Command Mode Engine. 0x0: Disable DSI Command Mode Engine 0x1: Enable DSI Command Mode Engine
1	VIDEO_MODE_EN	Enable the Video Mode Engine. 0x0: Disable DSI Video Mode Engine 0x1: Enable DSI Video Mode Engine
0	DSI_EN	Enable the DSI controller. 0x0: Disable DSI Controller 0x1: Enable DSI controller

0x04700004 MIPI_DSI_1_DSI1_STATUS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Status Register provides status of the DSI controller

MIPI_DSI_1_DSI1_STATUS

Bits	Name	Description
31	INTERLEAVE_OP_CONTENTION_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
31	INTERLEAVE_OP_CONTENTION	READ ONLY. The controller generates command mode packets and video mode packets at the same time (i.e.: the command mode packets are longer than one BLLP period)
30:7	RESERVED	
6	PHY_RESET_BUSY	READ ONLY. DSI interface is busy sending the panel reset through the link
5	GENERIC_TRIGGER_BUSY	READ ONLY. DSI interface is busy sending the generic trigger through the link

MIPI_DSI_1_DSI1_STATUS (cont.)

Bits	Name	Description
4	BTA_BUSY	READ ONLY. DSI interface is busy waiting for read response, acknowledge or tearing effect signal from the peripheral
3	VIDEO_MODE_ENGINE_BUSY	READ ONLY. Video Mode Engine is busy sending data from display engine
2	CMD_MODE_MDP_BUSY	READ ONLY. Command Mode Engine is busy sending data from display engine
1	CMD_MODE_DMA_BUSY	READ ONLY. Command Mode Engine is busy sending data from memory or reading data from the display panel
0	CMD_MODE_ENGINE_BUSY	READ ONLY. Command Mode Engine Busy

0x04700008 MIPI_DSI_1_DSI1_FIFO_STATUS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x11111000

Status of FIFOs in the DSI controller

MIPI_DSI_1_DSI1_FIFO_STATUS

Bits	Name	Description
31	RESERVED_1	
30	DLN3_HS_FIFO_OVERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
30	DLN3_HS_FIFO_OVERFLOW	READ ONLY. The FIFO of Lane 3 overflows
29	DLN3_HS_FIFO_FULL	READ ONLY. The FIFO of Lane 3 is full
28	DLN3_HS_FIFO_EMPTY	READ ONLY. The FIFO of Lane 3 is empty
27	RESERVED_2	
26	DLN2_HS_FIFO_OVERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
26	DLN2_HS_FIFO_OVERFLOW	READ ONLY. The FIFO for HS data on Lane 2 overflows
25	DLN2_HS_FIFO_FULL	READ ONLY. The FIFO for HS data on Lane 2 is full
24	DLN2_HS_FIFO_EMPTY	READ ONLY. The FIFO for HS data on Lane 2 is empty
23	RESERVED_3	
22	DLN1_HS_FIFO_OVERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear this bit

MIPI_DSI_1_DSI1_FIFO_STATUS (cont.)

Bits	Name	Description
22	DLN1_HS_FIFO_OVERFLOW	READ ONLY. The FIFO of Lane 1 overflows
21	DLN1_HS_FIFO_FULL	READ ONLY. The FIFO of Lane 1 is full
20	DLN1_HS_FIFO_EMPTY	READ ONLY. The FIFO of Lane 1 is empty
19	RESERVED_4	
18	DLN0_HS_FIFO_OVERFLOW	READ ONLY. The FIFO for HS data on Lane 0 overflows
18	DLN0_HS_FIFO_OVERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
17	DLN0_HS_FIFO_FULL	READ ONLY. The FIFO for HS data on Lane 0 is full
16	DLN0_HS_FIFO_EMPTY	READ ONLY. The FIFO for HS data on Lane 0 is empty
15	RESERVED_5	
14	DLN0_LP_FIFO_OVERFLOW_CLR	WRITE ONLY. unused
14	DLN0_LP_FIFO_OVERFLOW	READ ONLY. unused
13	DLN0_LP_FIFO_FULL	READ ONLY. The FIFO for LP data on Lane 0 is full
12	DLN0_LP_FIFO_EMPTY	READ ONLY. The FIFO for LP data on Lane 0 is empty
11	RESERVED_6	
10	CMD_DMA_FIFO_UNDERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
10	CMD_DMA_FIFO_UNDERFLOW	READ ONLY. The Command mode engine dmafifo underflows
9	CMD_DMA_FIFO_WR_WATERMARK_REACH_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
9	CMD_DMA_FIFO_WR_WATERMARK_REACH	READ ONLY. The Command mode engine dmafifo write watermark is reached
8	CMD_DMA_FIFO_RD_WATERMARK_REACH_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
8	CMD_DMA_FIFO_RD_WATERMARK_REACH	READ ONLY. The Command mode engine dmafifo read watermark is reached
7	CMD_MDP_FIFO_UNDERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear the underflow bit
7	CMD_MDP_FIFO_UNDERFLOW	READ ONLY. Command mode engine MDP fifo underflows
6:4	RESERVED_7	
3	VIDEO_MDP_FIFO_UNDERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear the underflow bit

MIPI_DSI_1_DSI1_FIFO_STATUS (cont.)

Bits	Name	Description
3	VIDEO_MDP_FIFO_UNDERFLOW	READ ONLY. Video fifo underflows
2:1	RESERVED_8	
0	VIDEO_MDP_FIFO_OVERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear the overflow bit
0	VIDEO_MDP_FIFO_OVERFLOW	READ ONLY. Video mode engine fifo overflows

0x0470000C MIPI_DSI_1_DSI1_VIDEO_MODE_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00008000

DSI Video Mode Engine Control Register

MIPI_DSI_1_DSI1_VIDEO_MODE_CTRL

Bits	Name	Description
31:29	RESERVED_1	
28	PULSE_MODE_OPT	Select pulse mode option 0x0: no HSA and HE following VS/VE packet 0x1: send HSA and HE following VS/VE packet
27:25	RESERVED_2	
24	HFP_PWR_MODE	Select power mode during the HFP period 0x0: send blanking packets in High Speed mode 0x1: low power stop mode (LP-11)
23:21	RESERVED_3	
20	HBP_PWR_MODE	Select power mode during the HBP period 0x0: send blanking packets in High Speed mode 0x1: low power stop mode (LP-11)
19:17	RESERVED_4	
16	HSA_PWR_MODE	Select power mode during the HSA period 0x0: send blanking packets in High Speed mode 0x1: low power stop mode (LP-11)
15	EOF_BLLP_PWR_MODE	Select power mode for the BLLP of the last line of a frame 0x0: send blanking packets during BLLP in high speed mode and block Command Mode packets 0x1: low power stop mode (LP-11 or let Command Mode Engine send packets in HS or LP mode)

MIPI_DSI_1_DSI1_VIDEO_MODE_CTRL (cont.)

Bits	Name	Description
14:13	RESERVED_5	
12	BLLP_PWR_MODE	DSI Power Mode for packets sent during BLLP period 0x0: send blanking packets during BLLP in high speed mode and block Command Mode packets 0x1: low power stop mode (LP-11 or let Command Mode Engine send packets in HS or LP mode)
11:10	RESERVED_6	
9:8	TRAFFIC_MODE	DSI video mode traffic sequence 0x0: non-burst mode with sync pulses 0x1: non-burst mode with sync start events 0x2: burst mode 0x3: reserved
7:6	RESERVED_7	
5:4	DST_FORMAT	Pixel format. If there is interleaved Command Mode pixel packets (generated from MDP), the pixel depth of the Command Mode pixel packet should be greater or equal to the pixel depth of the Video mode pixel packet. 0x0: RGB565 0x1: RGB666_1 (packed) 0x2: RGB666_2 (loosely packed) 0x3: RGB888
3:2	RESERVED_8	
1:0	VC	Virtual channel identifier

0x04700010 MIPI_DSI_1_DSI1_VIDEO_MODE_SYNC_DATATYPE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x31211101

DSI Video Mode Sync Datatype Register

MIPI_DSI_1_DSI1_VIDEO_MODE_SYNC_DATATYPE

Bits	Name	Description
31:30	RESERVED_1	
29:24	HE	Specify the data type of a hsync end packet
23:22	RESERVED_2	
21:16	HS	Specify the data type of a hsync start packet
15:14	RESERVED_3	

MIPI_DSI_1_DSI1_VIDEO_MODE_SYNC_DATATYPE (cont.)

Bits	Name	Description
13:8	VE	Specify the data type of a vsync end packet
7:6	RESERVED_4	
5:0	VS	Specify the data type of a vsync start packet

0x04700014 MIPI_DSI_1_DSI1_VIDEO_MODE_PIXEL_DATATYPE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x3E2E1E0E

DSI Video Mode Pixel Datatype Register

MIPI_DSI_1_DSI1_VIDEO_MODE_PIXEL_DATATYPE

Bits	Name	Description
31:30	RESERVED_1	
29:24	RGB888	Specify the datatype of an RGB888 pixel stream packet
23:22	RESERVED_2	
21:16	RGB666	Specify the datatype of a loosely-packed RGB666 pixel stream packet
15:14	RESERVED_3	
13:8	RGB666_PACKED	Specify the datatype of a packed RGB666 pixel stream packet
7:6	RESERVED_4	
5:0	RGB565	Specify the datatype of an RGB565 pixel stream packet

0x04700018 MIPI_DSI_1_DSI1_VIDEO_MODE_BLANKING_DATATYPE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00001900

DSI Video Mode Blanking Packet Datatype Register

MIPI_DSI_1_DSI1_VIDEO_MODE_BLANKING_DATATYPE

Bits	Name	Description
31:14	RESERVED	
13:8	BLANK_PKT_DATATYPE	Specify the datatype of a blanking packet

MIPI_DSI_1_DSI1_VIDEO_MODE_BLANKING_DATATYPE (cont.)

Bits	Name	Description
7:0	BLANK_PKT_DATA	This byte will be repeated in the payload portion of the blanking packet

0x0470001C MIPI_DSI_1_DSI1_VIDEO_MODE_DATA_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Video Mode Data Control Register

MIPI_DSI_1_DSI1_VIDEO_MODE_DATA_CTRL

Bits	Name	Description
31:15	RESERVED_1	
14:12	RGB_SWAP	Swaps the R, G, and B channels of the dst pixels. This field should be used when different R,G, and B orderings are required. For example, if RGB_SWAP = 1 , RGB565 will become RBG556. 0x0: RGB 0x1: RBG 0x2: BGR 0x3: BRG 0x4: GRB 0x5: GBR 0x6: reserved_1 0x7: reserved_2
11:9	RESERVED_2	
8	B_SEL	Bit Swaps the B Channel of the dst pixel. This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
7:5	RESERVED_3	
4	G_SEL	Bit Swaps the G Channel of the dst pixel. This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
3:1	RESERVED_4	

MIPI_DSI_1_DSI1_VIDEO_MODE_DATA_CTRL (cont.)

Bits	Name	Description
0	R_SEL	Bit Swaps the R Channel of the dst pixel. This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap

0x04700020 MIPI_DSI_1_DSI1_VIDEO_MODE_ACTIVE_H

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Active Horizontal Display Region register.

The Active_H_Disp register defines the horizontal characteristics of the active window. (NOTE: video mode parameters are 0-based.)

MIPI_DSI_1_DSI1_VIDEO_MODE_ACTIVE_H

Bits	Name	Description
31:28	RESERVED_1	
27:16	ACTIVE_H_END	ACTIVE_H_END field tells the video mode engine where the horizontal viewing area ends (minus one) in pixel clock cycle relative to the horizontal sync signal.
15:12	RESERVED_2	
11:0	ACTIVE_H_START	ACTIVE_H_START field tells the video mode engine where the horizontal viewing area starts (minus one) in pixel clock cycle relative to the horizontal sync signal.

0x04700024 MIPI_DSI_1_DSI1_VIDEO_MODE_ACTIVE_V

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

CRTC Active Vertical Display Region register.

The Active_V_Disp register defines the vertical characteristics of the active window. (NOTE: video mode parameters are 0-based.)

MIPI_DSI_1_DSI1_VIDEO_MODE_ACTIVE_V

Bits	Name	Description
31:28	RESERVED_1	
27:16	ACTIVE_V_END	ACTIVE_V_END field tells the video mode engine where the horizontal viewing area ends (minus one) in lines relative to the vertical sync signal
15:12	RESERVED_2	
11:0	ACTIVE_V_START	ACTIVE_V_START field tells the video mode engine where the vertical viewing area starts (minus one) in lines relative to the vertical sync signal

0x04700028 MIPI_DSI_1_DSI1_VIDEO_MODE_TOTAL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Total Scan Area register.

TOTAL register defines the size of the total possible scanning area (NOTE: video mode parameters are 0-based.)

MIPI_DSI_1_DSI1_VIDEO_MODE_TOTAL

Bits	Name	Description
31:28	RESERVED_1	
27:16	VIDEO_V_TOTAL	Number of lines in one frame minus one. This value is equivalent to the period of the vertical sync
15:12	RESERVED_2	
11:0	VIDEO_H_TOTAL	Number of pixels in one scan line (horizontal line) of the LCD controller minus one. This value is equivalent to the period of the horizontal sync signal (in pixel clock cycles).

0x0470002C MIPI_DSI_1_DSI1_VIDEO_MODE_HSYNC

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HSync Control register which controls the horizontal screen position at which a horizontal sync packet is sent by the DSI controller to the panel. (NOTE: video mode parameters are 0-based.)

MIPI_DSI_1_DSI1_VIDEO_MODE_HSYNC

Bits	Name	Description
31:28	RESERVED_1	
27:16	HS_END	The position (minus one) where the horizontal sync ends in one line.
15:12	RESERVED_2	
11:0	HS_START	The position (minus one) where the horizontal sync starts in one line.

0x04700030 MIPI_DSI_1_DSI1_VIDEO_MODE_VSYNC

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

VSync Control register which controls the horizontal screen position at which a vertical sync packet is sent by the DSI controller to the panel. (NOTE: video mode parameters are 0-based.)

MIPI_DSI_1_DSI1_VIDEO_MODE_VSYNC

Bits	Name	Description
31:28	RESERVED_1	
27:16	VS_END	The position (minus one) where the vertical sync ends in one line.
15:12	RESERVED_2	
11:0	VS_START	The position (minus one) where the vertical sync starts in one line.

0x04700034 MIPI_DSI_1_DSI1_VIDEO_MODE_VSYNC_VPOS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

VSync Control register which controls the vertical screen position at which a vertical sync packet is sent by the DSI controller to the panel. (NOTE: video mode parameters are 0-based.)

MIPI_DSI_1_DSI1_VIDEO_MODE_VSYNC_VPOS

Bits	Name	Description
31:28	RESERVED_1	
27:16	VS_VPOS_END	The line (minus one) where the vertical sync ends in one frame.

MIPI_DSI_1_DSI1_VIDEO_MODE_VSYNC_VPOS (cont.)

Bits	Name	Description
15:12	RESERVED_2	
11:0	VS_VPOS_START	The line (minus one) where the vertical sync starts in one frame.

0x04700038 MIPI_DSI_1_DSI1_COMMAND_MODE_DMA_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Command Mode Control Register for DMA data control

MIPI_DSI_1_DSI1_COMMAND_MODE_DMA_CTRL

Bits	Name	Description
31	BROADCAST_EN	Enable the DSI core to send packets from DMA at the same time with the other core (this bit has to be set for the other DSI core as well). If broadcast is enable, the core needs to wait until both cores have fetched entire command buffer before start sending dma packets. When this bit is set, the command buffer size (DSI_DMA_CMD_LENGTH) must be less than 0x200 bytes. 0x0: disable 0x1: enable
30	BROADCAST_MASTER	Indicate whether this core is the master or slave 0x0: this core is the slave 0x1: this core is the master
29	RESERVED_1	
28	EMBEDDED_MODE	Select packet_type, BTA settings and packet header information 0x0: from the register 0x1: from the frame buffer
27	RESERVED_2	
26	POWER_MODE	Select power mode for data transmission of both embedded and non-embedded commands 0x0: high speed mode 0x1: low power mode
25	RESERVED	
24	PACKET_TYPE	Select packet type for non-embedded commands 0x0: short packet 0x1: long packet
23:22	VC	Virtual channel identifier for pixel data or non-embedded commands
21:16	DT	Data type for pixel data or non-embedded commands

MIPI_DSI_1_DSI1_COMMAND_MODE_DMA_CTRL (cont.)

Bits	Name	Description
15:0	WC	Exact number of bytes in one packet for pixel data or non-embedded commands

0x0470003C MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x06100006

DSI Command Mode Control Register for MDP data control

MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_CTRL

Bits	Name	Description
31	LINE_SPLIT	Break a line into small packets 0x0: no split 0x1: split
30:28	RGB_SWAP1	Swaps the R, G, and B channels of the dst pixels for stream 1 (if STREAM1_DST_FORMAT_SEL = 1, otherwise rgb swap for stream1 is defined by RGB_SWAP). This field should be used when different R,G, and B orderings are required. For example, if RGB_SWAP = 1 , RGB565 will become RBG556. 0x0: RGB 0x1: RBG 0x2: BGR 0x3: BRG 0x4: GRB 0x5: GBR 0x6: reserved_1 0x7: reserved_2
27:24	DST_FORMAT1	Pixel format for stream 1 (if STREAM1_DST_FORMAT_SEL = 1, otherwise pixel format for stream1 is defined by DST_FORMAT) - 0 = RGB111 - 1 = reserved - 2 = reserved - 3 = RGB332 (data_src_width must be in multiple of 2 pixels) - 4 = RGB444 (data_src_width must be in multiple of 2 pixels) - 5 = reserved - 6 = RGB565 - 7 = RGB666 - 8 = RGB888 others = reserved

MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_CTRL (cont.)

Bits	Name	Description
23:20	INTERLEAVE_MAX	Maximum number of Command Mode RGB packets to send within one horizontal blanking period of the Video Mode frame (sw must ensure that they can fit in one BLLP period)
19	RESERVED_1	
18:16	RGB_SWAP	Swaps the R, G, and B channels of the dst pixels. This field should be used when different R,G, and B orderings are required. For example, if RGB_SWAP = 1 , RGB565 will become RBG556. 0x0: RGB 0x1: RBG 0x2: BGR 0x3: BRG 0x4: GRB 0x5: GBR 0x6: reserved_1 0x7: reserved_2
15	STREAM1_DST_FORMAT_SEL	Pixel format selection for stream 1. If MDP sends two streams to DSI and these streams have different output formats, then the pixel clock must be set according to the smallest pixel depth between the two. Otherwise, underflow may occur. Ex.: If stream0 is in RGB888 and stream1 is in RGB565, then pixel clock must be greater than dsiclk/2. 0x0: DST_FORMAT (same as stream0) 0x1: DST_FORMAT1
14	RESERVED_2	
13	B_SEL1	Bit Swaps the B Channel of the dst pixel for stream 1 (if STREAM1_DST_FORMAT_SEL = 1, otherwise bit swap for stream1 is defined by B_SEL). This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
12	B_SEL	Bit Swaps the B Channel of the dst pixel. This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
11:10	RESERVED	

MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_CTRL (cont.)

Bits	Name	Description
9	G_SEL1	Bit Swaps the G Channel of the dst pixel for stream 1 (if STREAM1_DST_FORMAT_SEL = 1, otherwise bit swap for stream1 is defined by G_SEL). This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
8	G_SEL	Bit Swaps the G Channel of the dst pixel. This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
7	BYTE_MSB_LSB_FLIP1	Swap the bit ordering of each byte of the dst pixel for stream 1 (if STREAM1_DST_FORMAT_SEL = 1, otherwise the byte endian is defined by BYTE_MSB_LSB_FLIP). 0x0: bit 0 is lsb, bit 7 is msb 0x1: bit 0 is msb, bit 0 is lsb
6	BYTE_MSB_LSB_FLIP	Swap the bit ordering of each byte of the dst pixel (this is done after the RGB swap and R/G/B_SEL). 0x0: bit 0 is lsb, bit 7 is msb 0x1: bit 0 is msb, bit 0 is lsb
5	R_SEL1	Bit Swap the R Channel of the dst pixel for stream 1 (if STREAM1_DST_FORMAT_SEL = 1, otherwise bit swap for stream1 is defined by R_SEL). This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
4	R_SEL	Bit Swap the R Channel of the dst pixel. This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000, then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap

MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_CTRL (cont.)

Bits	Name	Description
3:0	DST_FORMAT	Destination pixel format. For video mode operation interleave with MDP pixel packets, this is required: command mode pixel depth >= video mode pixel depth (check video mode pixel format in DSI_VIDEO_MODE_PIXEL_DATATYPE) - 0 = RGB111 - 1 = reserved - 2 = reserved - 3 = RGB332 (data_src_width must be in multiple of 2 pixels) - 4 = RGB444 (data_src_width must be in multiple of 2 pixels) - 5 = reserved - 6 = RGB565 - 7 = RGB666 - 8 = RGB888 others = reserved

0x04700040 MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_DCS_CMD_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00003C2C

This register controls DCS command insertion to MDP data

MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_DCS_CMD_CTRL

Bits	Name	Description
31:18	RESERVED	
17	INSERT_DCS_COMMAND2	Indicate whether a DCS command has to be inserted as the first byte of the payload of the pixel data packet of the stream NOT selected by COMMAND_MODE_DMA_STREAM_SEL 0x0: no command is inserted 0x1: value in the DCS_COMMAND field will be inserted
16	INSERT_DCS_COMMAND	Indicate whether a DCS command has to be inserted as the first byte of payload of the pixel data packet 0x0: no command is inserted 0x1: value in the DCS_COMMAND field will be inserted
15:8	WR_MEM_CONTINUE	DCS command for write_memory_continue
7:0	WR_MEM_START	DCS command for write_memory_start

0x04700044 MIPI_DSI_1_DSI1_DMA_CMD_OFFSET

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Command Offset Register

MIPI_DSI_1_DSI1_DMA_CMD_OFFSET

Bits	Name	Description
31:0	CMD_OFFSET	Memory offset (in bytes) for DSI command, qword aligned, i.e.: bit 2:0 are tied to 0. This value has to be multiple of 8. NOTE: Bits 0:2 of this field are preset in the factory to 0. You cannot change the setting of bits 0:2.

0x04700048 MIPI_DSI_1_DSI1_DMA_CMD_LENGTH

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Command Length Register

MIPI_DSI_1_DSI1_DMA_CMD_LENGTH

Bits	Name	Description
31:24	RESERVED	
23:0	CMD_LENGTH	Number of commands (in bytes). This value has to be multiple of 4.

0x0470004C MIPI_DSI_1_DSI1_DMA_FIFO_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI DMA FIFO Control Register

MIPI_DSI_1_DSI1_DMA_FIFO_CTRL

Bits	Name	Description
31:6	RESERVED_1	

MIPI_DSI_1_DSI1_DMA_FIFO_CTRL (cont.)

Bits	Name	Description
5:4	READ_WATERMARK	Allow fifo reads for a packet when the number of unread entries is above this watermark or larger than the packet size (read_watermark has to be smaller than or equal to write_watermark) 0x0: FIFO is 1/2 full 0x1: FIFO is 3/4 full 0x2: FIFO is 7/8 full 0x3: FIFO is 15/16 full
3:2	RESERVED_2	
1:0	WRITE_WATERMARK	Fills FIFO under the following conditions 0x0: FIFO is 1/2 empty 0x1: FIFO is 1/4 empty 0x2: FIFO is 1/8 empty 0x3: FIFO is 1/16 empty

0x04700050 MIPI_DSI_1_DSI1_DMA_NULL_PACKET_DATA

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000900

DSI DMA Null Packet Data Register

MIPI_DSI_1_DSI1_DMA_NULL_PACKET_DATA

Bits	Name	Description
31:14	RESERVED	
13:8	NULL_DATATYPE	Datatype of null packet
7:0	NULL_DATA	This byte will be repeated in the payload portion of the embedded null packet

0x04700054 MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_STREAM0_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI MDP stream 0 control register

MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_STREAM0_CTRL

Bits	Name	Description
31:16	MDP0_WC	Exact number of Word (byte) count for one packet
15:10	RESERVED_1	
9:8	MDP0_VC	Virtual channel
7:6	RESERVED_2	
5:0	MDP0_DT	Packet data type

0x04700058 MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_STREAM0_TOTAL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI MDP stream 0 frame dimension (NOTE: unlike video mode parameters which are 0-based, these parameters in command mode are 1-based, i.e.: the actual number of pixels are set.)

MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_STREAM0_TOTAL

Bits	Name	Description
31:28	RESERVED_1	
27:16	MDP0_V_TOTAL	Number of lines in 1 frame
15:12	RESERVED_2	
11:0	MDP0_H_TOTAL	Number of pixels in 1 line

0x0470005C MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_STREAM1_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI MDP stream 1 control register

MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_STREAM1_CTRL

Bits	Name	Description
31:16	MDP1_WC	Exact number of word (byte) count for one packet
15:10	RESERVED_1	
9:8	MDP1_VC	Virtual channel

MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_STREAM1_CTRL (cont.)

Bits	Name	Description
7:6	RESERVED_2	
5:0	MDP1_DT	Packet data type

0x04700060 MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_STREAM1_TOTAL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI MDP stream 1frame dimension (NOTE: unlike video mode parameters which are 0-based, these parameters in command mode are 1-based, i.e.: the actual number of pixels are set.)

MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_STREAM1_TOTAL

Bits	Name	Description
31:28	RESERVED_1	
27:16	MDP1_V_TOTAL	Exact number of lines in 1 frame
15:12	RESERVED_2	
11:0	MDP1_H_TOTAL	Exact number of pixels in 1 line

0x04700064 MIPI_DSI_1_DSI1_ACK_ERR_STATUS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Error Report Register stores errors and acknowledge from the DSI display module.

This register stores errors from the error report packet and error in the ECC and CRC of the returned packet

MIPI_DSI_1_DSI1_ACK_ERR_STATUS

Bits	Name	Description
31:29	RESERVED_1	
28	ACK_CLR	WRITE ONLY. clear ACK by writing a ’1’ and then a ’0’ to this bit
28	ACK	READ ONLY. Transmission acknowledged by the DSI display module
27:25	RESERVED_2	

MIPI_DSI_1_DSI1_ACK_ERR_STATUS (cont.)

Bits	Name	Description
24	ERROR	READ ONLY. There is an error report returned from the DSI display module (or-ed error bits 0 - 15)
24	ERROR_CLR	WRITE ONLY. clear ERROR by writing a ’1’ and then a ’0’ to this bit
23	RDBK_INCOMPLETE_PACKET_ERR	READ ONLY. Received incomplete read packet
23	RDBK_INCOMPLETE_PACKET_ERR_CLR	WRITE ONLY. clear RDBK_INCOMPLETE_PACKET_ERR by writing a ’1’ and then a ’0’ to this bit
22:21	RESERVED_3	
20	RDBK_DATA_CRC_ERR_CLR	WRITE ONLY. clear RDBK_DATA_CRC_ERR by writing a ’1’ and then a ’0’ to this bit
20	RDBK_DATA_CRC_ERR	READ ONLY. Incorrect CRC detected in read packet
19:18	RESERVED_4	
17	RDBK_DATA_MULTI_ECC_ERR_CLR	WRITE ONLY. clear RDBK_DATA_MULTI_ECC_ERR by writing a ’1’ and then a ’0’ to this bit
17	RDBK_DATA_MULTI_ECC_ERR	READ ONLY. Multi-bit ECC detected in read packet and not corrected
16	RDBK_DATA_ECC_ERR_CLR	WRITE ONLY. clear RDBK_DATA_ECC_ERR by writing a ’1’ and then a ’0’ to this bit
16	RDBK_DATA_ECC_ERR	READ ONLY. Single bit ECC error detected in read packet and corrected by DSI controller
15	PANEL_SPECIFIC_ERR	READ ONLY. This bit correspond to bit 15 (DSI protocol violation) of the error report. Please refer to the meaning by this description rather than by the name of the register field
15	PANEL_SPECIFIC_ERR_CLR	WRITE ONLY. Clear PANEL_SPECIFIC_ERR by writing a ’1’ and then a ’0’ to this bit
14	RESERVED	
13	PROTOCOL_VIOLATION_CLR	WRITE ONLY. Clear Protocol violation by writing a ’1’ and then a ’0’ to this bit
13	PROTOCOL_VIOLATION	READ ONLY. This bit corresponds to bit 13 (invalid transmission length) of the error report. Please refer to the meaning by this description rather than by the name of the register field.
12	VC_ERR_CLR	WRITE ONLY. clear VC_ERR by writing a ’1’ and then a ’0’ to this bit
12	VC_ERR	READ ONLY. Invalid virtual channel ID detected by the DSI display module
11	DT_ERR_CLR	WRITE ONLY. Clear DT_ERR by writing a ’1’ and then a ’0’ to this bit
11	DT_ERR	READ ONLY. DSI data type not recognized by the DSI display module

MIPI_DSI_1_DSI1_ACK_ERR_STATUS (cont.)

Bits	Name	Description
10	CRC_ERR	READ ONLY. Checksum error for long packet detected by the DSI display module
10	CRC_ERR_CLR	WRITE ONLY. Clear CRC_ERR by writing a ’1’ and then a ’0’ to this bit
9	MULTI_ECC_ERR_CLR	WRITE ONLY. Clear MULTI_ECC_ERR by writing a ’1’ and then a ’0’ to this bit
9	MULTI_ECC_ERR	READ ONLY. Multi-bit ECC detected and not corrected by the DSI display module
8	ECC_ERR_CLR	WRITE ONLY. Clear ECC_ERR by writing a ’1’ and then a ’0’ to this bit
8	ECC_ERR	READ ONLY. Single bit ECC detected and corrected by the DSI display module
7	CONTENTION	READ ONLY. Contention Detected by Peripheral
7	CONTENTION_CLR	WRITE ONLY. Clear CONTENTION by writing a ’1’ and then a ’0’ to this bit
6	FALSE_CTRL_ERR_CLR	WRITE ONLY. Clear FALSE_CTRL_ERR by writing a ’1’ and then a ’0’ to this bit
6	FALSE_CTRL_ERR	READ ONLY. False Control Error detected by the DSI display module
5	TIMEOUT_CLR	WRITE ONLY. Clear TIMEOUT by writing a ’1’ and then a ’0’ to this bit
5	TIMEOUT	READ ONLY. Timeout error (Low Power forward transmission, bus turn around, High Speed reverse transmission) detected by the DSI display module
4	LP_ERR	READ ONLY. Low-power transmit sync error detected by the DSI display module
4	LP_ERR_CLR	WRITE ONLY. Clear LP_ERR by writing a ’1’ and then a ’0’ to this bit
3	ESC_ERR_CLR	WRITE ONLY. Clear ESC_ERR by writing a ’1’ and then a ’0’ to this bit
3	ESC_ERR	READ ONLY. Escape Mode Entry Command Error detected by the DSI display module
2	EOT_ERR_CLR	WRITE ONLY. Clear EOT_ERR by writing a ’1’ and then a ’0’ to this bit
2	EOT_ERR	READ ONLY. EoT Sync Error detected by the DSI display module
1	SOT_SYNC_ERR	READ ONLY. SoT Sync Error detected by the DSI display module
1	SOT_SYNC_ERR_CLR	WRITE ONLY. Clear SOT_SYNC_ERR by writing a ’1’ and then a ’0’ to this bit
0	SOT_ERR_CLR	WRITE ONLY. Clear SOT_ERR by writing a ’1’ and then a ’0’ to this bit

MIPI_DSI_1_DSI1_ACK_ERR_STATUS (cont.)

Bits	Name	Description
0	SOT_ERR	READ ONLY. SoT Error detected by the DSI display module

0x04700068 MIPI_DSI_1_DSI1_RDBK_DATA0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Read Data 0 Register

MIPI_DSI_1_DSI1_RDBK_DATA0

Bits	Name	Description
31:0	RD_DATA0	READ ONLY. Data returned from the DSI display module

0x0470006C MIPI_DSI_1_DSI1_RDBK_DATA1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Read Data 1 Register

MIPI_DSI_1_DSI1_RDBK_DATA1

Bits	Name	Description
31:0	RD_DATA1	READ ONLY. Data returned from the DSI display module

0x04700070 MIPI_DSI_1_DSI1_RDBK_DATA2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Read Data 2 Register

MIPI_DSI_1_DSI1_RDBK_DATA2

Bits	Name	Description
31:0	RD_DATA2	READ ONLY. Data returned from the DSI display module

0x04700074 MIPI_DSI_1_DSI1_RDBK_DATA3

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Read Data 3 Register

MIPI_DSI_1_DSI1_RDBK_DATA3

Bits	Name	Description
31:0	RD_DATA3	READ ONLY. Data returned from the DSI display module

0x04700078 MIPI_DSI_1_DSI1_RDBK_DATATYPE0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x22211211

DSI Read Response Datatype Register 0

MIPI_DSI_1_DSI1_RDBK_DATATYPE0

Bits	Name	Description
31:30	RESERVED_1	
29:24	DCS_SHORT_RD_2_BYTE	Specify the datatype of a DCS short read response with 2 byte returned
23:22	RESERVED_2	
21:16	DCS_SHORT_RD_1_BYTE	Specify the datatype of a DCS short read response with 1 byte returned
15:14	RESERVED_3	
13:8	GENERIC_SHORT_RD_2_BYTE	Specify the datatype of a generic short read response with 2 byte returned
7:6	RESERVED_4	
5:0	GENERIC_SHORT_RD_1_BYTE	Specify the datatype of a generic short read response with 1 byte returned

0x0470007C MIPI_DSI_1_DSI1_RDBK_DATATYPE1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x001C1A02

DSI Read Response Datatype Register 1

MIPI_DSI_1_DSI1_RDBK_DATATYPE1

Bits	Name	Description
31:22	RESERVED_1	
21:16	DCS_LONG_RD	Specify the datatype of a DCS long read response
15:14	RESERVED_2	
13:8	GENERIC_LONG_RD	Specify the datatype of a generic long read response
7:6	RESERVED	
5:0	ERROR_REPORT	Specify the datatype of an acknowledge with error report

0x04700080 MIPI_DSI_1_DSI1_TRIG_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Trigger Control Register

When DSI is enabled and CRTC1 or 2 is used for other non-DSI panels, the display engine path trigger must be set to manual internal, otherwise the CRTC will be stalled

MIPI_DSI_1_DSI1_TRIG_CTRL

Bits	Name	Description
31	TE_SEL	Select TE path 0x0: Tearing effect_1 (external trigger returns from data link) 0x1: Tearing effect_2 (external trigger returns from a dedicated pin)
30:29	RESERVED_1	
28	COMMAND_MODE_DMA_MDP_ORDER	This bit field indicates whether DMA or MDP path will win the arbitration if both requests the link at the same time 0x0: DMA has higher priority than display processor 0x1: Display processor has higher priority than DMA
27:25	RESERVED_2	
24	COMMAND_MODE_MDP_REQ_ORDER	If PHY TE is required for one of the MDP stream while the other stream is ready to transmit, this field determines which will win the arbitration 0x0: Command Mode MDP PHY TE request has higher priority than Command Mode MDP data transmission request 0x1: Command Mode MDP Data transmission request has higher priority than Command Mode MDP PHY TE request
23:9	RESERVED_3	

MIPI_DSI_1_DSI1_TRIG_CTRL (cont.)

Bits	Name	Description
8	COMMAND_MODE_DMA_STREAM_SEL	If COMMAND_MODE_DMA_TRIGGER_SEL = SOF/EOF or both COMMAND_MODE_DMA_TRIGGER_SEL and COMMAND_MODE_MDP_TRIGGER_SEL = TE or sw+TE, the Command Mode DMA path is triggered at frame boundary of the MDP stream selected by this bit 0x0: stream 0 0x1: stream 1
7	RESERVED_4	
6:4	COMMAND_MODE_MDP_TRIGGER_SEL	TRIGGER_SEL field is used to select which trigger is used for Command Mode display processor path. (The stream to be triggered is selected by COMMAND_MODE_DMA_STREAM_SEL) 0x0: none 0x1: reserved_1 0x2: TE 0x3: reserved_2 0x4: sw trigger 0x5: reserved_3 0x6: sw trigger and TE 0x7: reserved_4
3	RESERVED	
2:0	COMMAND_MODE_DMA_TRIGGER_SEL	DMA_TRIGGER_SEL field is used to select which trigger is used for Command Mode DMA path. 0x0: none 0x1: Start/end of frame (determined by COMMAND_MODE_DMA_MDP_ORDER) 0x2: TE 0x3: reserved_1 0x4: sw trigger 0x5: sw trigger and start/end of frame (COMMAND_MODE_DMA_MDP_ORDER) 0x6: sw trigger and TE 0x7: reserved_2

0x04700084 MIPI_DSI_1_DSI1_EXT_MUX

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI External Pin Mux Register - select IO pin for tearing effect and panel reset

MIPI_DSI_1_DSI1_EXT_MUX

Bits	Name	Description
31:20	EXT_TE_HSYNC_TOTAL	Defines the total number of hsync per frame
19:8	EXT_TE_HSYNC_TRIG_CNT	Defines the number of hsync needed to trigger the engine if TE_MODE is set to 1
7	EXT_TE_POL	Polarity of external tearing effect signal 0x0: TE occurs at the rising edge 0x1: TE occurs at the falling edge
6	RESERVED	
5:4	EXT_TE_MODE	Select TE mode 0x0: vsync_1 (edge detection) 0x1: vsync_2 (pulse width detection) 0x2: vsync and hsync combin_1 (edge detection) 0x3: vsync and hsync combin_2 (pulse width detection)
3:0	EXT_TE_MUX	Input port for external tearing effect (external trigger). Valid range: 0 to 1

0x04700088 MIPI_DSI_1_DSI1_EXT_TE_PULSE_DETECT_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI External Tearing Effect Pulse Width Detection Control Register

MIPI_DSI_1_DSI1_EXT_TE_PULSE_DETECT_CTRL

Bits	Name	Description
31:16	TE_VSYNC_MIN_WIDTH	Defines the minimum width (in escclk) of the vsync pulse in the TE signal
15:0	TE_HSYNC_MAX_WIDTH	Defines the maximum width (in escclk) of the hsync pulse in the TE signal

0x0470008C MIPI_DSI_1_DSI1_CMD_MODE_DMA_SW_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Command Mode DMA Software Trigger Register

MIPI_DSI_1_DSI1_CMD_MODE_DMA_SW_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Software can start a DMA trigger for the Command Mode engine by writing a 1 to this bit

0x04700090 MIPI_DSI_1_DSI1_CMD_MODE_MDP_SW_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Command Mode Display Processor Path Software Trigger Register

MIPI_DSI_1_DSI1_CMD_MODE_MDP_SW_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Software can start an MPD trigger for the Command Mode engine by writing a 1 to this bit

0x04700094 MIPI_DSI_1_DSI1_CMD_MODE_BTA_SW_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Command Mode Bus-Turn-Around Software Trigger Register

MIPI_DSI_1_DSI1_CMD_MODE_BTA_SW_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Software can start a BTA trigger for the Command Mode engine by writing a 1 to this bit

0x04700098 MIPI_DSI_1_DSI1_RESET_SW_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Reset Software Trigger Register

MIPI_DSI_1_DSI1_RESET_SW_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Software can trigger reset through the data link by writing a 1 to this bit

0x0470009C MIPI_DSI_1_DSI1_MISR_CMD_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI miser control for command mode operation - misr is collected for packets output from packetizer

MIPI_DSI_1_DSI1_MISR_CMD_CTRL

Bits	Name	Description
31:29	RESERVED_1	
28	EN	enable Command Mode misr accumulation (all the misr's are reset to 0 when it is disable)
27:25	RESERVED_2	
24	WIDTH_SEL	misr width of packets generated fronm dma, mdp stream 0 and mdp stream1 data 0x0: generate misr in 8 bits 0x1: generate misr in 16 bits
23:16	MDP_STREAM1_MISR	READ ONLY. 8-bit misr for packets generated from MDP stream 1
15:8	MDP_STREAM0_MISR	READ ONLY. 8-bit misr for packets generated from MDP stream 0
7:0	DMA_MISR	READ ONLY. 8-bit misr for packets generated from memory

0x047000A0 MIPI_DSI_1_DSI1_MISR_VIDEO_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI miser control for video mode operation - misr is collected for packets output from packetizer

MIPI_DSI_1_DSI1_MISR_VIDEO_CTRL

Bits	Name	Description
31:29	RESERVED_1	
28	STOP_EN	Select misr accumulation restart or stop after N frame (specified in MAX_FRAME_COUNT) 0x0: auto reset every N frame 0x1: stop after N frames
27:25	RESERVED_2	
24	WIDTH_SEL	misr width of packets generated fronm dma, mdp stream 0 and mdp stream1 data 0x0: generate misr in 8 bits 0x1: generate misr in 16 bits
23:17	RESERVED	
16	EN	Enable Video Mode misr accumulation (the misr is reset to 0 when it is disable)
15:8	MAX_FRAME_COUNT	Internal misr is reset when the number of frames generated by the video mode engine reaches this number and the MISR field in this register is updated before the reset.
7:0	MISR	READ ONLY. misr for video mode packets

0x047000A4 MIPI_DSI_1_DSI1_LANE_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Lane Status Register

MIPI_DSI_1_DSI1_LANE_STATUS

Bits	Name	Description
31:17	RESERVED_1	
16	DLN0_DIRECTION	READ ONLY. Indicate transmission direction of Data Lane 0 0x0: forward 0x1: reverse
15:13	RESERVED_2	
12	CLKLN_ULPS_ACTIVE_NOT	READ ONLY. Indicate whether Clock Lane is in Ultra-Low power state 0x0: ulps active 0x1: ulps not active

MIPI_DSI_1_DSI1_LANE_STATUS (cont.)

Bits	Name	Description
11	DLN3_ULPS_ACTIVE_NOT	READ ONLY. Indicate whether Data Lane 3 is in Ultra-Low power state 0x0: ulps active 0x1: ulps not active
10	DLN2_ULPS_ACTIVE_NOT	READ ONLY. Indicate whether Data Lane 2 is in Ultra-Low power state 0x0: ulps active 0x1: ulps not active
9	DLN1_ULPS_ACTIVE_NOT	READ ONLY. Indicate whether Data Lane 1 is in Ultra-Low power state 0x0: ulps active 0x1: ulps not active
8	DLN0_ULPS_ACTIVE_NOT	READ ONLY. Indicate whether Data Lane 0 is in Ultra-Low power state 0x0: ulps active 0x1: ulps not active
7:5	RESERVED	
4	CLKLN_STOPSTATE	READ ONLY. Indicate whether Clock Lane is in Stop state 0x0: active state 0x1: stop state
3	DLN3_STOPSTATE	READ ONLY. Indicate whether Data Lane 3 is in Stop state 0x0: active state 0x1: stop state
2	DLN2_STOPSTATE	READ ONLY. Indicate whether Data Lane 2 is in Stop state 0x0: active state 0x1: stop state
1	DLN1_STOPSTATE	READ ONLY. Indicate whether Data Lane 1 is in Stop state 0x0: active state 0x1: stop state
0	DLN0_STOPSTATE	READ ONLY. Indicate whether Data Lane 0 is in Stop state 0x0: active state 0x1: stop state

0x047000A8 MIPI_DSI_1_DSI1_LANE_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Lane Control Register

MIPI_DSI_1_DSI1_LANE_CTRL

Bits	Name	Description
31:29	RESERVED_1	
28	CLKLN_HS_FORCE_REQUEST	Force Clock Lane to enter HS mode always
27:21	RESERVED_2	
20	CLKLN_FORCE_TX_STOP	Force Clock Lane to go into transmit mode and the lane module state machine is forced into the Stop state
19	DLN3_FORCE_TX_STOP	Force Data Lane 3 to go into transmit mode and the lane module state machine is forced into the Stop state
18	DLN2_FORCE_TX_STOP	Force Data Lane 2 to go into transmit mode and the lane module state machine is forced into the Stop state
17	DLN1_FORCE_TX_STOP	Force Data Lane 1 to go into transmit mode and the lane module state machine is forced into the Stop state
16	DLN0_FORCE_TX_STOP	Force Data Lane 0 to go into transmit mode and the lane module state machine is forced into the Stop state
15:13	RESERVED_3	
12	CLKLN_ULPS_EXIT	Request Clock Lane to exit Ultra-Low power state
11	DLN3_ULPS_EXIT	Request Data Lane 3 to exit Ultra-Low power state
10	DLN2_ULPS_EXIT	Request Data Lane 2 to exit Ultra-Low power state
9	DLN1_ULPS_EXIT	Request Data Lane 1 to exit Ultra-Low power state
8	DLN0_ULPS_EXIT	Request Data Lane 0 to exit Ultra-Low power state
7:5	RESERVED_4	
4	CLKLN_ULPS_REQUEST	Request Clock Lane to enter Ultra-Low power state
3	DLN3_ULPS_REQUEST	Request Data Lane 3 to enter Ultra-Low power state
2	DLN2_ULPS_REQUEST	Request Data Lane 2 to enter Ultra-Low power state
1	DLN1_ULPS_REQUEST	Request Data Lane 1 to enter Ultra-Low power state
0	DLN0_ULPS_REQUEST	Request Data Lane 0 to enter Ultra-Low power state

0x047000AC MIPI_DSI_1_DSI1_LANE_SWAP_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Lane Swapping Control Register

MIPI_DSI_1_DSI1_LANE_SWAP_CTRL

Bits	Name	Description
31:3	RESERVED	
2:0	DLN_SWAP_SEL	PHY lane mapping for data lane 0, 1, 2, 3 output from the DSI controller - 000 = 0, 1, 2, 3 - 001 = 3, 0, 1, 2 - 010 = 2, 3, 0, 1 - 011 = 1, 2, 3, 0 - 100 = 0, 3, 2, 1 - 101 = 1, 0, 3, 2 - 110 = 2, 1, 0, 3 - 111 = 3, 2, 1, 0

0x047000B0 MIPI_DSI_1_DSI1_DLN0_PHY_ERR

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00088888

DSI PHY Error Register - reports errors returned from the PHY. If the mask bit for a specific error is set to 1, turn request will be de-asserted if the corresponding error occurs and controller will wait for the link to return to forward stopstate.

NOTE Turn request abort/interrupt will be generated if the mask field(s) in DSI_DLN0_PHY_ERR is set to 1. (Interrupt will be generated if the mask field(s) in DSI_INT_CTRL is set to 1; error status will be generated if the mask field(s) in DSI_ERR_INT_MASK0 is set to 0).

MIPI_DSI_1_DSI1_DLN0_PHY_ERR

Bits	Name	Description
31:20	RESERVED_1	
19	DLN0_ERR_CONTENTION_LP1_MASK	Option for controller to ignore this error 0x0: no action 0x1: abort turn request if error occurs
18:17	RESERVED_2	
16	DLN0_ERR_CONTENTION_LP1	READ ONLY. Contention detected while lane 0 is driven high
16	DLN0_ERR_CONTENTION_LP1_CLR	WRITE ONLY. Clear DLN0_ERR_CONTENTION_LP1 by writing a ’1’ to this field

MIPI_DSI_1_DSI1_DLN0_PHY_ERR (cont.)

Bits	Name	Description
15	DLN0_ERR_CONTENTION_LP0_MASK	Option for controller to ignore this error 0x0: no action 0x1: abort turn request if error occurs
14:13	RESERVED_3	
12	DLN0_ERR_CONTENTION_LP0_CLR	WRITE ONLY. Clear DLN0_ERR_CONTENTION_LP0 by writing a ’1’ to this field
12	DLN0_ERR_CONTENTION_LP0	READ ONLY. Contention detected while lane 0 is driven low
11	DLN0_ERR_CONTROL_MASK	Option for controller to ignore this error 0x0: no action 0x1: abort turn request if error occurs
10:9	RESERVED_4	
8	DLN0_ERR_CONTROL_CLR	WRITE ONLY. Clear DLN0_ERR_CONTROL by writing a ’1’ to this field
8	DLN0_ERR_CONTROL	READ ONLY. An incorrect line state sequence is detected
7	DLN0_ERR_SYNC_ESC_MASK	Option for controller to ignore this error 0x0: no action 0x1: abort turn request if error occurs
6:5	RESERVED_5	
4	DLN0_ERR_SYNC_ESC_CLR	WRITE ONLY. Clear DLN0_ERR_SYNC_ESC by writing a ’1’ to this field
4	DLN0_ERR_SYNC_ESC	READ ONLY. Number of bits received during a low power data transmission is not a multiple of eight when the transmission ends
3	DLN0_ERR_ESC_MASK	Option for controller to ignore this error 0x0: no action 0x1: abort turn request if error occurs
2:1	RESERVED_6	
0	DLN0_ERR_ESC_CLR	WRITE ONLY. Clear DLN0_ERR_ESC by writing a ’1’ to this field
0	DLN0_ERR_ESC	READ ONLY. Unrecognized escape entry command received

0x047000B4 MIPI_DSI_1_DSI1_LP_TIMER_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0xFFFFFFFF

DSI Timeout Control Register for Low Power Mode Transmission

MIPI_DSI_1_DSI1_LP_TIMER_CTRL

Bits	Name	Description
31:16	BTA_TO	Bus turn-around timeout (in escclk)
15:0	LP_RX_TO	Low power transmission reverse timeout (in Escclk)

0x047000B8 MIPI_DSI_1_DSI1_HS_TIMER_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000FFFF

DSI Timeout Control Register for High Speed Mode Transmission

MIPI_DSI_1_DSI1_HS_TIMER_CTRL

Bits	Name	Description
31:29	RESERVED_1	
28	HS_TX_TO_STOP_EN	Stop High Speed Transmission immediately at timeout
27:20	RESERVED_2	
19:16	TIMER_RESOLUTION	Control all 3 timeout counter increment steps by power of 2 of this field. Ex.: 0 = increment every escclk; - 1 = increment every 2 escclk; - 3 = increment every 8 escclk;
15:0	HS_TX_TO	High speed transmission timeout (in escclk)

0x047000BC MIPI_DSI_1_DSI1_TIMEOUT_STATUS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Timeout Status Register

MIPI_DSI_1_DSI1_TIMEOUT_STATUS

Bits	Name	Description
31:9	RESERVED_1	
8	BTA_TIMEOUT_CLR	WRITE ONLY. Writing a 1 will clear this bit
8	BTA_TIMEOUT	READ ONLY. Indicates Bus Turnaround timeout

MIPI_DSI_1_DSI1_TIMEOUT_STATUS (cont.)

Bits	Name	Description
7:5	RESERVED_2	
4	LP_RX_TIMEOUT_CLR	WRITE ONLY. Writing a 1 will clear this bit
4	LP_RX_TIMEOUT	READ ONLY. Indicates Low Power reverse transmission timeout
3:1	RESERVED	
0	HS_TX_TIMEOUT_CLR	WRITE ONLY. Writing a 1 will clear this bit
0	HS_TX_TIMEOUT	READ ONLY. Indicates High Speed forward transmission timeout

0x047000C0 MIPI_DSI_1_DSI1_CLKOUT_TIMING_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI PHY Clock Lane Timing Control Register

MIPI_DSI_1_DSI1_CLKOUT_TIMING_CTRL

Bits	Name	Description
31:14	RESERVED_1	
13:8	T_CLK_POST	Number of byteclk cycles (minus one) that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to Low Power mode
7:6	RESERVED_2	
5:0	T_CLK_PRE	Number of byteclk cycles (minus one) that the high speed clock shall be driven prior to any associated Data Lane beginning the transition from Low Power to High Speed mode

0x047000C4 MIPI_DSI_1_DSI1_EOT_PACKET

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x010F0F08

DSI EOT Packet Register - packet to append at the end of a High Speed Data Burst

MIPI_DSI_1_DSI1_EOT_PACKET

Bits	Name	Description
31:24	ECC	ECC of the EOT packet

MIPI_DSI_1_DSI1_EOT_PACKET (cont.)

Bits	Name	Description
23:8	WC	Word count of the EOT packet
7:0	DI	Data identifier (virtual channel and datatype) of the EOT packet

0x047000C8 MIPI_DSI_1_DSI1_EOT_PACKET_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI EOT Packet Control Register

MIPI_DSI_1_DSI1_EOT_PACKET_CTRL

Bits	Name	Description
31:5	RESERVED_1	
4	RX_EOT_IGNORE	Specify whether the controller should ignore the EOT packet if it is received from reverse transmission 0x0: do not ignore 0x1: ignore
3:1	RESERVED_2	
0	TX_EOT_APPEND	Specify whether the EOT packet has to be appended at the end of each forward High Speed data burst 0x0: do not append 0x1: append

0x047000CC MIPI_DSI_1_DSI1_GENERIC_ESC_TX_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Generic Escape Mode Trigger Register

MIPI_DSI_1_DSI1_GENERIC_ESC_TX_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Software can trigger a generic escape mode command through DISP_DSIPHY_DLN0_TX_TRIGGER_ESC[3] by writing a 1 to this bit

0x047000D0 MIPI_DSI_1_DSI1_CAM_BIST_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display MIPI BIST Control. To start the BIST, all cam bist configuration should be done first, then CAM_BIST_EN should be set to 1 and lastly set DSI_CAM_BIST_START to 1. To stop or modify the cam bist configuration, program the DSI_CAM-BIST_* registers in reverse sequence (i.e.: start by writing DSI_CAM_BIST_START to 0).

MIPI_DSI_1_DSI1_CAM_BIST_CTRL

Bits	Name	Description
31:5	RESERVED_1	
4	CRC_EN	Enable CRC calculation for the CSI packets 0x0: disable 0x1: enable
3:2	RESERVED_2	
1	CAM_BIST_EN	- 1 Enables MIPI CSI BIST
0	CAM_BIST_RESET	- 1 Resets MIPI CSI BIST

0x047000D4 MIPI_DSI_1_DSI1_CAM_BIST_FRAME_SIZE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display Mipi BIST Video Frame Vertical and Horizontal size

MIPI_DSI_1_DSI1_CAM_BIST_FRAME_SIZE

Bits	Name	Description
31:16	CAM_V_SIZE	Vertical Size
15:0	CAM_H_SIZE	Horizontal Size

0x047000D8 MIPI_DSI_1_DSI1_CAM_BIST_BLOCK_SIZE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display Mipi BIST Video Block Vertical and Horizontal size

MIPI_DSI_1_DSI1_CAM_BIST_BLOCK_SIZE

Bits	Name	Description
31:16	RESERVED	
15:8	CAM_V_SIZE	Vertical Size
7:0	CAM_H_SIZE	Horizontal Size

0x047000DC MIPI_DSI_1_DSI1_CAM_BIST_FRAME_CONFIG

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display Mipi BIST Video Frame format

MIPI_DSI_1_DSI1_CAM_BIST_FRAME_CONFIG

Bits	Name	Description
31:25	RESERVED	
24	CAM_BIST_VIDEO_FRMT	- 0= YUV 4:2:2 8 bits 1= RAW 8 bits
23:16	CAM_FRAME_REPEAT	Reserved (Number of frame sequence NOT to be repeated)
15:0	CAM_BLANKING_CYCLES	Video scan Vertical and Horizontal Blanking cycle

0x047000E0 MIPI_DSI_1_DSI1_CAM_BIST_LSFR_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display MIPI BIST generator random numbers generator control

MIPI_DSI_1_DSI1_CAM_BIST_LSFR_CTRL

Bits	Name	Description
31:27	RESERVED	
26	CAM_V_LSFR_EN	(Unused) V component shift register enable
25	CAM_U_LSFR_EN	(Unused) U component shift register enable
24	CAM_Y_LSFR_EN	(Unused) Y component shift register enable
23:16	CAM_V_LSFR_POLYNOMIAL	V component polynomial

MIPI_DSI_1_DSI1_CAM_BIST_LSFR_CTRL (cont.)

Bits	Name	Description
15:8	CAM_U_LSFR_POLYNOMIAL	U component polynomial
7:0	CAM_Y_LSFR_POLYNOMIAL	Y component polynomial

0x047000E4 MIPI_DSI_1_DSI1_CAM_BIST_LSFR_INIT

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display MIPI BIST generator random numbers initial values

MIPI_DSI_1_DSI1_CAM_BIST_LSFR_INIT

Bits	Name	Description
31:24	RESERVED	
23:16	CAM_V_INIT_LSFR_VAL	V component shift register initial value
15:8	CAM_U_INIT_LSFR_VAL	U component shift register initial value
7:0	CAM_Y_INIT_LSFR_VAL	Y component shift register initial value

0x047000E8 MIPI_DSI_1_DSI1_CAM_BIST_START

Type: Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display MIPI BIST Start Stop control

MIPI_DSI_1_DSI1_CAM_BIST_START

Bits	Name	Description
31:1	RESERVED	
0	CAM_BIST_START	WRITE ONLY. Start and stop BIST. This field should be changed when CAM_BIST_EN = 1. When this field is set to 1, the BIST runs continuously. When this field is set to 0, the BIST will turn off at the end of the current frame. 0x0: Stop 0x1: Start

0x047000EC MIPI_DSI_1_DSI1_CAM_BIST_STATUS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display MIPI BIST BUSY

MIPI_DSI_1_DSI1_CAM_BIST_STATUS

Bits	Name	Description
31:5	RESERVED_1	
4	CAM_BIST_DONE	READ ONLY. MIPI BIST done for 1 frame
4	CAM_BIST_DONE_CLR	WRITE ONLY. Writing a 1 will clear the done bit
3:1	RESERVED_2	
0	CAM_BIST_STATUS_BUSY	READ ONLY. MIPI BIST status bit

0x04700108 MIPI_DSI_1_DSI1_ERR_INT_MASK0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x13FF3BFF

DSI Error Interrupt Enable Register - enable any event to drive the error status (DSI_INT_CTRL.DSI_ERROR_STAT). If the DSI_INT_CTRL.DSI_ERROR_MASK is set to 1, interrupt will be generated.

NOTE Interrupt will be generated if the mask field(s) in DSI_INT_CTRL is set to 1; error status will be generated if the mask field(s) in DSI_ERR_INT_MASK0 is set to 0.

MIPI_DSI_1_DSI1_ERR_INT_MASK0

Bits	Name	Description
31:29	RESERVED_1	
28	DPHY_DSIPLL_UNLOCK_MASK	Mask dsipll unlock (to avoid sending out unnecessary interrupts, set this bit to 1 before dsipll locks) 0x0: allow generation of error status 0x1: no error status generated
27:26	RESERVED_2	

MIPI_DSI_1_DSI1_ERR_INT_MASK0 (cont.)

Bits	Name	Description
25	DLN0_ERR_CONTENTION_LP1_MASK	Mask contention while data lane 0 is driven high interrupt (DSI_DLN0_PHY_ERR reg, bit 16) 0x0: allow generation of error status (this should be set when dsipll is ready or when dsipll bypass is set to 1) 0x1: no error status generated
24	DLN0_ERR_CONTENTION_LP0_MASK	Mask contention while data lane 0 is driven low interrupt (DSI_DLN0_PHY_ERR reg, bit 12) 0x0: allow generation of error status 0x1: no error status generated
23	DLN0_ERR_CONTROL_MASK	Mask incorrect LP RX state sequence interrupt (DSI_DLN0_PHY_ERR reg, bit 8) 0x0: allow generation of error status 0x1: no error status generated
22	DLN0_ERR_SYNC_ESC_MASK	Mask LP RX data that is not byte-aligned interrupt (DSI_DLN0_PHY_ERR reg, bit 4) 0x0: allow generation of error status 0x1: no error status generated
21	DLN0_ERR_ESC_MASK	Mask incorrect LP RX escape entry interrupt (DSI_DLN0_PHY_ERR reg, bit 0) 0x0: allow generation of error status 0x1: no error status generated
20	DLN0_LP_FIFO_OVERFLOW_MASK	unused (Mask Lane Layer Low Power FIFO for data lane 0 interrupt (DSI_FIFO_STATUS reg, bit 14)) 0x0: allow generation of error status 0x1: no error status generated
19	DLN3_HS_FIFO_OVERFLOW_MASK	Mask Lane Layer High Speed FIFO for data lane 3 interrupt (DSI_STATUS reg, bit 30) 0x0: allow generation of error status 0x1: no error status generated
18	DLN2_HS_FIFO_OVERFLOW_MASK	Mask Lane Layer High Speed FIFO for data lane 2 interrupt (DSI_STATUS reg, bit 26) 0x0: allow generation of error status 0x1: no error status generated
17	DLN1_HS_FIFO_OVERFLOW_MASK	Mask Lane Layer High Speed FIFO for data lane 1 interrupt (DSI_FIFO_STATUS reg, bit 22) 0x0: allow generation of error status 0x1: no error status generated
16	DLN0_HS_FIFO_OVERFLOW_MASK	Mask Lane Layer High Speed FIFO for data lane 0 interrupt (DSI_FIFO_STATUS reg, bit 18) 0x0: allow generation of error status 0x1: no error status generated
15:14	RESERVED_3	

MIPI_DSI_1_DSI1_ERR_INT_MASK0 (cont.)

Bits	Name	Description
13	VID_MDP_FIFO_UNDERFLOW_MASK	Mask Video Mode Engine FIFO underflow interrupt (DSI_FIFO_STATUS reg, bit 3) 0x0: allow generation of error status 0x1: no error status generated
12	VID_MDP_FIFO_OVERFLOW_MASK	Mask Video Mode Engine FIFO overflow interrupt (DSI_FIFO_STATUS reg, bit 0) 0x0: allow generation of error status 0x1: no error status generated
11	CMD_MDP_FIFO_UNDERFLOW_MASK	Mask Display Engine FIFO underflow interrupt (DSI_FIFO_STATUS reg, bit 7) 0x0: allow generation of error status 0x1: no error status generated
10	RESERVED_4	
9	CMD_DMA_FIFO_UNDERFLOW_MASK	Mask Command mode dma FIFO underflow interrupt (DSI_FIFO_STATUS reg, bit 10) 0x0: allow generation of error status 0x1: no error status generated
8	INTERLEAVE_OP_CONTENTION_MASK	Mask interleave operation contention interrupt (DSI_STATUS reg, bit 31) 0x0: allow generation of error status 0x1: no error status generated
7	BTA_TO_MASK	Mask bus turnaround timeout interrupt (DSI_TIMEOUT_STATUS reg, bit 8) 0x0: allow generation of error status 0x1: no error status generated
6	HS_TX_TO_MASK	Mask High Speed forward transmission timeout interrupt (DSI_TIMEOUT_STATUS reg, bit 0) 0x0: allow generation of error status 0x1: no error status generated
5	LP_RX_TO_MASK	Mask Low Power reverse transmission timeout interrupt (DSI_TIMEOUT_STATUS reg, bit 4) 0x0: allow generation of error status 0x1: no error status generated
4	ERROR_PACKET_MASK	Mask error packet returned from peripheral interrupt (DSI_ACK_ERR_STATUS reg, bit 24) 0x0: allow generation of error status 0x1: no error status generated
3	RDBK_INCOMPLETE_PACKET_ERR_MASK	Mask incomplete read packet error interrupt (DSI_ACK_ERR_STATUS reg, bit 23) 0x0: allow generation of error status 0x1: no error status generated

MIPI_DSI_1_DSI1_ERR_INT_MASK0 (cont.)

Bits	Name	Description
2	RDBK_DATA_CRC_ERR_MASK	Mask crc error in the read packet interrupt (DSI_ACK_ERR_STATUS reg, bit 20) 0x0: allow generation of error status 0x1: no error status generated
1	RDBK_DATA_MULTI_ECC_ERR_MASK	Mask multi bit ecc error in the read packet interrupt (DSI_ACK_ERR_STATUS reg, bit 17) 0x0: allow generation of error status 0x1: no error status generated
0	RDBK_DATA_ECC_ERR_MASK	Mask single bit ecc error in the read packet interrupt (DSI_ACK_ERR_STATUS reg, bit 16) 0x0: allow generation of error status 0x1: no error status generated

0x0470010C MIPI_DSI_1_DSI1_INT_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x02200202

DSI Interrupt Control Register.

NOTE Interrupt will be generated if the mask field(s) in DSI_INT_CTRL is set to 1; error status will be generated if the mask field(s) in DSI_ERR_INT_MASK0 is set to 0.

MIPI_DSI_1_DSI1_INT_CTRL

Bits	Name	Description
31:26	RESERVED_1	
25	DSI_ERROR_MASK	DSI Error Mask. If set to 1, interrupt generation is enabled. 0x0: no interrupt generated 0x1: allow generation of interrupt
24	DSI_ERROR_AK	WRITE ONLY. DSI Error Acknowledge. If set to 1, status and interrupt is cleared.
24	DSI_ERROR_STAT	READ ONLY. DSI Error status. Set when the DSI Error has happened.
23:22	RESERVED_2	
21	DSI_BTA_DONE_MASK	DSI BTA Done Mask. If set to 1, interrupt generation is enabled. 0x0: no interrupt generated 0x1: allow generation of interrupt

MIPI_DSI_1_DSI1_INT_CTRL (cont.)

Bits	Name	Description
20	DSI_BTA_DONE_STAT	READ ONLY. DSI BTA Done Status (sw triggered BTA, embedded BTA or BTA generated for TE). Set when a bus turnaround has completed.
20	DSI_BTA_DONE_AK	WRITE ONLY. DSI BTA Done Acknowledge. If set to 1, status and interrupt is cleared.
19:18	RESERVED_3	
17	DSI_VIDEO_MODE_DONE_MASK	DSI Video Mode Engine path Done Mask. If set to 1, interrupt generation is enabled. 0x0: no interrupt generated 0x1: allow generation of interrupt
16	DSI_VIDEO_MODE_DONE_AK	WRITE ONLY. DSI Video Mode Engine path Done Acknowledge. If set to 1, status and interrupt is cleared.
16	DSI_VIDEO_MODE_DONE_STAT	READ ONLY. DSI Video Mode Engine status. Set when the DSI Video Mode Engine has finished transferring data to the panel.
15:10	RESERVED_4	
9	DSI_CMD_MODE_MDP_DONE_MASK	DSI Command Mode Engine MDP path Done Mask. If set to 1, interrupt generation is enabled. 0x0: no interrupt generated 0x1: allow generation of interrupt
8	DSI_CMD_MODE_MDP_DONE_STAT	READ ONLY. DSI Command Mode Engine MDP path status. Set when the DSI Command Mode Engine has finished transferring deng data to the panel.
8	DSI_CMD_MODE_MDP_DONE_AK	WRITE ONLY. DSI Command Mode Engine MDP path Done Acknowledge. If set to 1, status and interrupt is cleared.
7:2	RESERVED	
1	DSI_CMD_MODE_DMA_DONE_MASK	DSI Command Mode Engine DMA path Done Mask. If set to 1, interrupt generation is enabled. 0x0: no interrupt generated 0x1: allow generation of interrupt
0	DSI_CMD_MODE_DMA_DONE_AK	WRITE ONLY. DSI Command Mode Engine DMA path Done Acknowledge. If set to 1, status and interrupt is cleared.
0	DSI_CMD_MODE_DMA_DONE_STAT	READ ONLY. DSI Command Mode Engine DMA status. Set when the DSI Command Mode Engine has finished transferring dma data to the panel.

0x04700110 MIPI_DSI_1_DSI1_IOBIST_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI IOBIST Control Register

MIPI_DSI_1_DSI1_IOBIST_CTRL

Bits	Name	Description

31:0	DSI_IOBIST_CTRL	This register has 2 modes of operation: command and timing mode. All configuration fields should be written first, then enable (bit 0) should be set to 1 next and start (bit 5) is set to 1 last.
		
		COMMAND MODE
		bit 0 = DSI IOBIST ENABLE. Active high;
		bit 5 = IOBIST start. Active high;
		bit 6 = Select power mode for data transfer.
		- 0 = high speed (HS), 1 = low power (LP)
		bit 7 = Data pattern mode.
		- 0 = Use data pattern word, 1 = PRBS pattern.
		bit 10:8 = multiple of finite random run (N): if bit 12 is finite, the finite run is 256 x (N+1) runs for HS PRBS and user data, or 16 x (N+1) for LP PRBS
		bit 12 = Infinite run
		- 0 for infinite; 1 for 256 x (N+1) runs of HS PRBS, 16 x (N+1) runs of LP PRBS, 256 x (N+1) runs of HS user data, or 8 runs of LP user data.
		bit 14:13 = DSIBIST_DSIPHY_LANE_SWAP, select which lane is used as lane0 for LPDT:
		- 0 = DLN0
		- 1 = DLN1
		- 2 = DLN2
		- 3 = DLN3
		bit 15 = Select instruction type
		- 0 = command mode, 1 = DSI timing control mode.
		bit 23:16 = data pattern byte (used when bit 7 is set to 0)
		other bits = reserved
		
		TIMING MODE
		bit 0 = DSI IOBIST ENABLE. Active high;
		bit 5 = IOBIST start. Active high;
		bit 15 = Select instruction type
		- 0 = command mode, 1 = DSI timing control mode.
		(If you write one DSI timing data with the select instruction type == 1, you have to change the select instruction type from 1 to 0 for timing data latch control.)
		bit 23:16 = DSI timing data;
		bit 28:24 = DSI timing register selection:
		- 0x10 = DSI_T_CLK_PRE (data width[5:0])
		- 0x11 = DSI_T_CLK_POST (data width[5:0])

0x04700114 MIPI_DSI_1_DSI1_SOFT_RESET

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI soft reset Register

MIPI_DSI_1_DSI1_SOFT_RESET

Bits	Name	Description
31:1	RESERVED	
0	DSI_SOFT_RESET	Resets all internal logic in dsiclk, pclk, byteclk, escclk, ahbm_hclk domain. All enable bits in DSI_CTRL should be already set to 0 when exiting soft reset (DSI_SOFT_RESET changing from 1 to 0). The dynamic clocks should be forced on when DSI_SOFT_RESET is set to 1. (This reset does not apply to DSI registers which are in ahbs_hclk domain.)

0x04700118 MIPI_DSI_1_DSI1_CLK_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Clock Control Register. The dynamic clocks should be forced on when DSI_SOFT_RESET is set to 1 or when DSI_EN is changed from 1 to 0.

MIPI_DSI_1_DSI1_CLK_CTRL

Bits	Name	Description
31:18	RESERVED_1	
17:16	DSI_DSICLK_HYSTERISIS1_CTRL	DSI DSICLK Hysterisis Control
15:14	DSI_AHBM_HCLK_HYSTERISIS1_CTRL	DSI AHBM_HCLK Hysterisis Control
13:12	DSI_AHBS_HCLK_HYSTERISIS1_CTRL	unused
11	DSI_FORCE_ON_DYN_BYTECLK	DSI Dynamic BYTECLK Clock Branch Force On. Set to one to always force on this clock branch.
10	DSI_FORCE_ON_DYN_DSICLK	DSI Dynamic DSICLK Clock Branch Force On. Set to one to always force on this clock branch.
9	DSI_FORCE_ON_DYN_AHBM_HCLK	DSI Dynamic AHBM_HCLK (MCLK) Clock Branch Force On. Set to one to always force on this clock branch.

MIPI_DSI_1_DSI1_CLK_CTRL (cont.)

Bits	Name	Description
8	DSI_FORCE_ON_DYN_AHBS_HCLK	DSI Dynamic AHBS_HCLK (REGCLK)Clock Branch Force On. Set to one to always force on this clock branch.
7:6	RESERVED_2	
5	DSI_ESCCLK_ON	Turns on/off ESCCLK for the DSI. If set to 1, clock is ON.
4	DSI_BYTECLK_ON	Turns on/off BYTECLK for the DSI. If set to 1, clock is ON.
3	DSI_DSICLK_ON	Turns on/off DSICLK for the DSI. If set to 1, clock is ON.
2	DSI_PCLK_ON	Turns on/off PCLK for the DSI. If set to 1, clock is ON.
1	DSI_AHBM_SCLK_ON	Turns on/off AHBM_HCLK for the DSI. If set to 1, clock is ON.
0	DSI_AHBS_HCLK_ON	Turns on/off AHBS_HCLK for the DSI. If set to 1, clock is ON.

0x0470011C MIPI_DSI_1_DSI1_CLK_STATUS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Clock Status Register

MIPI_DSI_1_DSI1_CLK_STATUS

Bits	Name	Description
31:17	RESERVED_1	
16	DSIPLL_UNLOCKED_CLR	WRITE ONLY. Write only. Clear dsipll_unlocked status by writing to this register field
16	DSIPLL_UNLOCKED	READ ONLY. Read only. Dsi pll unlock status 0x0: dsipll not unlocked 0x1: dsipll unlocked
15:10	RESERVED_2	
9	DSI_AON_PCLK_ACTIVE	READ ONLY. DSI Always ON PCLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
8	DSI_AON_ESCCLK_ACTIVE	READ ONLY. DSI Always ON ESCCLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
7	DSI_DYN_BYTECLK_ACTIVE	READ ONLY. DSI Dynamic BYTECLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
6	DSI_AON_BYTECLK_ACTIVE	READ ONLY. DSI Always ON BYTECLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.

MIPI_DSI_1_DSI1_CLK_STATUS (cont.)

Bits	Name	Description
5	DSI_DYN_DSICLK_ACTIVE	READ ONLY. DSI Dynamic DSICLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
4	DSI_AON_DSICLK_ACTIVE	READ ONLY. DSI Always ON DSICLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
3	DSI_DYN_AHBS_HCLK_ACTIVE	READ ONLY. DSI Dynamic AHBS_HCLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
2	DSI_AON_AHBS_HCLK_ACTIVE	READ ONLY. DSI Always ON AHBS_HCLK Active Status. Read-only field that shows the status of this clock branch.If set to one, clock is on. If set to zero, clock is off.
1	DSI_DYN_AHBM_HCLK_ACTIVE	READ ONLY. DSI Dynamic AHBM_HCLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
0	DSI_AON_AHBM_HCLK_ACTIVE	READ ONLY. DSI Always ON AHBM_HCLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.

0x04700120 MIPI_DSI_1_DSI1_DEBUG_BUS_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI debug bus control Register

MIPI_DSI_1_DSI1_DEBUG_BUS_CTRL

Bits	Name	Description
31:14	RESERVED_1	
13:12	DEBUG_MUX	debug mux select within the selected block
11:10	RESERVED_2	

MIPI_DSI_1_DSI1_DEBUG_BUS_CTRL (cont.)

Bits	Name	Description
9:4	DEBUG_SEL	debug bus block select - 0-4: pclk domain debug signals; - 5-9: escclk domain debug signals - 10-19: byteclk domain debug signals - 20-29: dsiclk domain debug signals - 30-34: mclk domain debug signals - 35-39: dphy domain debug signals - 40-42: regclk domain debug signals - 43-59: reserved - 60: fixed pattern 0xFFFFFFFF - 61: fixed pattern 0xAAAAAAAA - 62: fixed pattern 0x55555555 - 63: fixed pattern 0xAF50_F50A
3:1	RESERVED	
0	DEBUG_BUS_EN	debug bus enable, the debug bus is cleared to 0 when debug bus is disable.

0x04700124 MIPI_DSI_1_DSI1_DEBUG_BUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI debug bus Register

MIPI_DSI_1_DSI1_DEBUG_BUS

Bits	Name	Description
31:0	DEBUG_BUS	READ ONLY. Value on the selected debug bus

0x04700128 MIPI_DSI_1_DSI1_PHY_SW_RESET

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI PHY SW Reset Register

MIPI_DSI_1_DSI1_PHY_SW_RESET

Bits	Name	Description
31:25	RESERVED_1	

MIPI_DSI_1_DSI1_PHY_SW_RESET (cont.)

Bits	Name	Description
24	PHY_REGULATOR_HW_RESET	THIS BIT IS ONLY USED IN DSI CORE 1. PHY software reset for the regulator. A reset pulse is issued by writing 1 followed by a 0 to this bit.
23:17	RESERVED_2	
16	PHY_LN_HW_RESET	PHY software reset for the LANES. A reset pulse is issued by writing 1 followed by a 0 to this bit.
15:9	RESERVED_3	
8	PHY_PLL_HW_RESET	PHY software reset for the PLL. A reset pulse is issued by writing 1 followed by a 0 to this bit.
7:5	RESERVED_4	
4	PHY_SW_RESET_POL	Polarity of all reset signals for PHY PLL, LANES and regulator. - 0 = active high; - 1 = active low
3:1	RESERVED	
0	PHY_SW_RESET	PHY hardware reset for all PHY PLL, LANES and REGULATOR (for DSI CORE 1 only). A reset pulse is issued by writing 1 followed by a 0 to this bit.

0x0470012C MIPI_DSI_1_DSI1_AXI2AHB_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI AXI to AHB bridge control Register

MIPI_DSI_1_DSI1_AXI2AHB_CTRL

Bits	Name	Description
31:1	RESERVED	
0	MSM_ACCUMULATE_EN	Read data accumulate enable - 1 = allows for all read data to be returned prior to feeding it out - 0 = returns read data immediately

0x04700130 MIPI_DSI_1_DSI1_MISR_CMD_MDP0_32BIT

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0xFFFFFFFF

DSI Command MDP stream 0 32-bit misr

MIPI_DSI_1_DSI1_MISR_CMD_MDP0_32BIT

Bits	Name	Description
31:0	MISR	READ ONLY. 32-bit misr for packets generated from MDP stream 0

0x04700134 MIPI_DSI_1_DSI1_MISR_CMD_MDP1_32BIT

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0xFFFFFFFF

DSI Command MDP stream 0 32-bit misr

MIPI_DSI_1_DSI1_MISR_CMD_MDP1_32BIT

Bits	Name	Description
31:0	MISR	READ ONLY. 32-bit misr for packets generated from MDP stream 0

0x04700138 MIPI_DSI_1_DSI1_MISR_CMD_DMA_32BIT

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0xFFFFFFFF

DSI Command dma 32-bit misr

MIPI_DSI_1_DSI1_MISR_CMD_DMA_32BIT

Bits	Name	Description
31:0	MISR	READ ONLY. 32-bit misr for packets generated from memory

0x0470013C MIPI_DSI_1_DSI1_MISR_VIDEO_32BIT

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0xFFFFFFFF

DSI Video Mode 32-bit misr

MIPI_DSI_1_DSI1_MISR_VIDEO_32BIT

Bits	Name	Description
31:0	MISR	READ ONLY. 32-bit misr for packets generated from MDP's DSI Video Mode stream

0x04700140 MIPI_DSI_1_DSI1_LANE_MISR_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Lane MISR control

MIPI_DSI_1_DSI1_LANE_MISR_CTRL

Bits	Name	Description
31:1	RESERVED	
0	EN	Enable MISR calculation of the lane data at the output of the lane distribution layer 0x0: disable 0x1: enable

0x04700144 MIPI_DSI_1_DSI1_LANE0_MISR

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000FFFF

DSI Lane 0 MISR value

MIPI_DSI_1_DSI1_LANE0_MISR

Bits	Name	Description
31:16	RESERVED	
15:0	MISR	READ ONLY. MISR value of the lane data at the output of the lane distribution layer

0x04700148 MIPI_DSI_1_DSI1_LANE1_MISR

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000FFFF

DSI Lane 1 MISR value

MIPI_DSI_1_DSI1_LANE1_MISR

Bits	Name	Description
31:16	RESERVED	
15:0	MISR	READ ONLY. MISR value of the lane data at the output of the lane distribution layer

0x0470014C MIPI_DSI_1_DSI1_LANE2_MISR

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000FFFF

DSI Lane 2 MISR value

MIPI_DSI_1_DSI1_LANE2_MISR

Bits	Name	Description
31:16	RESERVED	
15:0	MISR	READ ONLY. MISR value of the lane data at the output of the lane distribution layer

0x04700150 MIPI_DSI_1_DSI1_LANE3_MISR

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000FFFF

DSI Lane 3 MISR value

MIPI_DSI_1_DSI1_LANE3_MISR

Bits	Name	Description
31:16	RESERVED	
15:0	MISR	READ ONLY. MISR value of the lane data at the output of the lane distribution layer

0x04700158 MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI test pattern generator control register

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CTRL

Bits	Name	Description
31:18	RESERVED_1	
17:16	CMD_DMA_PATTERN_SEL	Test pattern for command mode dma data 0x0: PRBS pattern generated from polynomial and init value 0x1: incremental starting from init value 0x2: fixed to init value 0x3: reserved
15:14	RESERVED_2	
13:12	CMD_MDP_STREAM1_PATTERN_SEL	Test pattern for command mode pixel (MDP) stream1 data 0x0: PRBS pattern generated from polynomial and init value 0x1: incremental starting from init value 0x2: fixed to init value 0x3: reserved
11:10	RESERVED_3	
9:8	CMD_MDP_STREAM0_PATTERN_SEL	Test pattern for command mode pixel (MDP) stream0 data 0x0: PRBS pattern generated from polynomial and init value 0x1: incremental starting from init value 0x2: fixed to init value 0x3: reserved
7:6	RESERVED_4	
5:4	VIDEO_PATTERN_SEL	Test pattern for video mode operation 0x0: PRBS pattern generated from polynomial and init value 0x1: incremental starting from init value 0x2: fixed to init value 0x3: reserved
3:1	RESERVED	

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CTRL (cont.)

Bits	Name	Description
0	EN	DSI test pattern enable. This is the global enable of the pattern generator. Once this bit is set to 1, it is ready to generate data for video mode, command mode pixel or dma data. Video mode data is started by DSI*_TEST_PATTERN_GEN_VIDEO_ENABLE; Command mode pixel data can be started by DSI*_TEST_PATTERN_GEN_CMD_STREAM[01]_TRIGGER or triggered by the trigger source set in COMMAND_MODE_MDP_TRIGGER_SEL; Command mode dma data is generated when a memory read request is received (the application layer will generate memory read request when it is triggered by the trigger source set in COMMAND_MODE_DMA_TRIGGER_SEL). Note: for Command dma data, only use the pattern generator in DMA non-embedded mode only (DSI*_COMMAND_MODE_DMA_CTRL.embedded_mode set to 0) because the pattern generator only generates a test pattern for payload.

0x0470015C MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_VIDEO_POLY

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Polynomial of the Video mode test pattern generator

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_VIDEO_POLY

Bits	Name	Description
31:24	RESERVED	
23:0	POLYNOMIAL	- 24-bit LSFR polynomial applied for pixel data

0x04700160 MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_VIDEO_INIT_VAL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Initial value of the Video mode test pattern generator

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_VIDEO_INIT_VAL

Bits	Name	Description
31:24	RESERVED	

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_VIDEO_INIT_VAL (cont.)

Bits	Name	Description
23:0	INIT_VAL	- 24-bit initial value applied for pixel data

0x04700164 MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_MDP_STREAM0_POLY

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Polynomial of the Command mode test pattern generator for stream0

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_MDP_STREAM0_POLY

Bits	Name	Description
31:24	RESERVED	
23:0	POLYNOMIAL	- 24-bit LSFR polynomial applied for pixel data

0x04700168 MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_MDP_INIT_VAL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Initial value of the Command mode test pattern generator for stream0

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_MDP_INIT_VAL0

Bits	Name	Description
31:24	RESERVED	
23:0	INIT_VAL	- 24-bit initial value applied for pixel data

0x0470016C MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_MDP_STREAM1_POLY

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Polynomial of the Command mode test pattern generator for stream1

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_MDP_STREAM1_POLY

Bits	Name	Description
31:24	RESERVED	
23:0	POLYNOMIAL	- 24-bit LSFR polynomial applied for pixel data

0x04700170 MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_MDP_INIT_VAL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Initial value of the Command mode test pattern generator for stream1

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_MDP_INIT_VAL1

Bits	Name	Description
31:24	RESERVED	
23:0	INIT_VAL	- 24-bit initial value applied for pixel data

0x04700174 MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_DMA_POLY

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Polynomial of the Command mode test pattern generator for dma data

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_DMA_POLY

Bits	Name	Description
31:0	POLYNOMIAL	- 32-bit LSFR polynomial applied for dma data

0x04700178 MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_DMA_INIT_VAL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Initial value of the Command mode test pattern generator for dma

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_DMA_INIT_VAL

Bits	Name	Description
31:0	INIT_VAL	- 32-bit initial value applied for dma data

0x0470017C MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_VIDEO_ENABLE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Enable test pattern for video mode

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_VIDEO_ENABLE

Bits	Name	Description
31:1	RESERVED	
0	EN	Enable video stream test pattern. Once this bit is set to 1, the pattern generator will start generating video stream 0x0: disable 0x1: enable

0x04700180 MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_STREAM0_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Trigger test pattern for Command MDP stream0

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_STREAM0_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Writing this bit will trigger a frame for command MDP stream 0

0x04700184 MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_STREAM1_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Trigger test pattern for Command MDP stream1

MIPI_DSI_1_DSI1_TEST_PATTERN_GEN_CMD_STREAM1_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Writing this bit will trigger a frame for command MDP stream 1.

0x04700190 MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_IDLE_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Idle insertion between Command MDP packets.

MIPI_DSI_1_DSI1_COMMAND_MODE_MDP_IDLE_CTRL

Bits	Name	Description
31:14	RESERVED_1	
13:12	EN	Enable idle insertion between Command Mode MDP packets 0x0: disable 0x1: insert idle for stream0 0x2: insert idle for stream1 0x3: insertion idle for both streams
11:10	RESERVED_2	
9:0	LENGTH	Number of dsiclk cycles of idle time to insert between Command Mode MDP packets. This idle counter is added in the application layer. To ensure the DSI link will go into stopstate between Command Mode MDP packets, the LENGTH must be long enough to cover the time the link takes to switch between High Speed mode to Low Power mode (LP11).

0x047001F0 MIPI_DSI_1_DSI1_VERSION

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x02000104

DSI Version Register

MIPI_DSI_1_DSI1_VERSION

Bits	Name	Description
31:24	MAJOR_VERSION	READ ONLY. DSI major version number ex.: 2 for DSI 2.0

MIPI_DSI_1_DSI1_VERSION (cont.)

Bits	Name	Description
23:16	MINOR_VERSION	READ ONLY. DSI minor version number ex.: 0 for DSI 2.0
15:8	PHY_VERSION	READ ONLY. PHY version that this core supports - 0 = 45nm PHY - 1 = 28nm PHY
7:4	RESERVED	
3:0	CONFIG	READ ONLY. DSI configuration - 2 = this version can support up to 2 lanes - 4 = this version can support up to 4 lanes

0x04700200 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

NOTE The preferred names for all DSIPHY_PLL_CTRL_n registers would be DSIPHY_PLL_CFGn.

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_0

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5	DSIPLL_BYPASS	Output Clock Control (Debug Purpose). When it is '1', the output clocks will be generated from reference clock. When it is '0', output clocks will be generated from PLL VCO clock. Normal operational mode setting is 0 Power up value is 0
4	DSIPLL_OPEN_LOOP	Open Loop Setting. When this bit is set to 1, the Lock Time is significantly reduced compared to lock time in closed loop mode. 0=Closed Loop Mode - 1= Open Loop Mode Normal operational mode setting is 0. Power up value is 0
3	DSIPLL_PWR_MODE	PLL const-gm bias select - 0: Resistor div bias is selected - 1: PLL Const-gm bias is selected Normal operational mode setting is 0. Power up value is 0
2	RESERVED_BITS2	

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_0 (cont.)

Bits	Name	Description
1	DSIPLL_SWCAL_EN	S/W Calibration Enable Control. If the bit is '1', then the PLL will ignore CAL_MODE and perform S/W calibration. VCO OFFSET and SLOPE will be set by MAN_OFFSET and MAN_SLOPE.We are not using the SW calibration anymore. So this bit should be set to '0'. Normal operational mode setting is 0. Power up value is 0
0	DSIPLL_PLL_EN	PLL Enable Signal. Analog power down. - 1 = Normal Mode of operation - 0 = Power Down State Normal operational mode setting is 1. Power up value is 0

0x04700204 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000000E

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPLL_DIV_FB_7_0	- 11 bit Feed back divider Ratio. {DSIPHY_PLL_CTRL_2[DSIPLL_DIV_FB_10_8], DSIPLL_DIV_FB_7_0} - 000_0000_0000 = div by 1 - 000_0000_0001 = div by 2 - 000_0000_0010 = div by 3 ... 111_1111_1111 = div by 2048 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 0000_1110

0x04700208 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000030

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_2

Bits	Name	Description
31:7	RESERVED_BITS31_7	

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_2 (cont.)

Bits	Name	Description
6:4	DSIPLL_UNLOCK_RES	Unlock Detector Resolution Setting. 000: unlock=1 if 1 mismatch between ref_clk and fb_clk - 001: unlock=1 if 2 consecutive mismatches between ref_clk and fb_clk - 010: unlock=1 if 3 consecutive mismatches between ref_clk and fb_clk ... - 111: unlock=1 if 8 consecutive mismatches between ref_clk and fb_clk Normal operational mode setting is 011. Power up value is 011
3	RESERVED_BITS3	
2:0	DSIPLL_DIV_FB_10_8	- 11 bit Feed back divider Ratio. {DSIPLL_DIV_FB_10_8,DSIPHY_PLL_CTRL_1[DSIPLL_DIV_FB_7_0]} - 000_0000_0000 = div by 1 - 000_0000_0001 = div by 2 - 000_0000_0010 = div by 3 ... 111_1111_1111 = div by 2048 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 000

0x0470020C MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_3

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	DSIPLL_CAL_MODE	Calibration Mode Setting. - 00 :Skip calibration and use I_MAN_OFFSET and I_MAN_SLOPE for VCO. - 01/10/11 : Perform calibration for both OFFSET and SLOPE settings Normal operational mode setting is 11 Power up value is 11

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_3 (cont.)

Bits	Name	Description
5:0	DSIPLL_DIV_REF	Reference Divider Ratio. 000000 : div by 1 - 000001 : div by 2 - 000010 : div by 3 - 000011 : div by 4 ... - 111111 : div by 64 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 00_0000

0x04700210 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_4

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700214 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000040

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_5

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	DSIPLL_LF_R	Loop Filter Resistor R setting. 000: 100K - 001: 75K - 010: 50K - 011: 35K - 100: 25K - 101: 20K - 110: 12K - 111: 8K Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 100
3:0	RESERVED_BITS3_0	

0x04700218 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_6

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000003

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_6

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	DSIPLL_LF_C2	Loop Filter Capacitor C2 setting.(3+B2*18+B1*9+B0*6) 000: 3pF - 001: 9pF - 010: 12pF - 011: 18pF - 100: 21pF - 101: 27pF - 110: 30pF - 111: 36pF Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 000
3:0	DSIPLL_LF_C1	Loop Filter Capacitor C1 setting.(20+B3*130+B2*60+B1*25+B0*15) 0000: 20pF - 0001: 35pF - 0010 : 45pF - 0011 : 60pF - 0100: 80pF - 0101: 95pF - 0110: 105pF - 0111:120pF - 1000: 150pF - 1001: 165pF - 1010: 175pF - 1011: 190pF - 1100: 210pF - 1101:225pF - 1110: 235pF - 1111: 250pF Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 0011

0x0470021C MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_7

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000062

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_7

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	DSIPLL_DIGITAL_WAITTIME	PLL Digital wait time setting. 00 : 6 REF_CLK cycles - 01 :11 REF_CLK cycles - 10 : 23 REF_CLK cycles - 11 : 52 REF_CLK cycles Normal operational mode setting is 11. Power up value is 11
4:3	RESERVED_BITS4_3	
2:0	DSIPLL_CP	Charge Pump Current setting. 000 : 5uA - 001 : 10uA - 010 : 12.5uA - 011 : 17.5uA - 100 : 20uA - 101 : 25uA - 110 : 27.5uA - 111 : 32.5uA Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 010

0x04700220 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_8

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000040

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_8

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	DSIPLL_UNLOCK_DET_SEL	- 0: use negedge(50% phase detect) - 1: use posedge(100% phase detect) Normal operational mode setting is 0. Power up value is 0

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_8 (cont.)

Bits	Name	Description
6:4	DSIPLL_VREF_CONF	These bits sets the Vtune value in PLL Open Loop Mode. - 000: Vtune=0.50v - 001: Vtune=0.55v - 010: Vtune=0.60v - 011: Vtune=0.65v - 100: Vtune=0.70v - 101: Vtune=0.75v - 110: Vtune=0.80v - 111: Vtune=0.85v The preferred name for this register bit field would be DSIPLL_VTUNE_CONF. Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 100
3:0	DSIPLL_OUT_DIV1	Output Divider setting for oCLK1 (Bitclk). This is a high frequency clock and it goes to clock layer. 0000: div by1 - 0001: div by2 - 0010: div by3 - 0011: div by4 ... - 1111: div by16 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. The preferred name for this register bit field would be DSIPLL_OUT_DIV_BITCLK. Power up value is 0000

0x04700224 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_9

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000007

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_9

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_9 (cont.)

Bits	Name	Description
7:0	DSIPLL_OUT_DIV2	Output Divider setting for oCLK2. This is pixel clock going to DSI Controller. 00000000: div by1 - 00000001: div by2 - 00000010: div by3 - 00000011: div by4 ... - 11111111: div by256 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. The preferred name for this register bit field would be DSIPLL_OUT_DIV_BYTECLK. Power up value is 0000_0111

0x04700228 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_10

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000007

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_10

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPLL_OUT_DIV3	Output Divider setting for oCLK3. This is a test clock going to DSI Controller. - 00000000: div by1 - 00000001: div by2 - 00000010: div by3 - 00000011: div by4 ... - 11111111: div by256 The preferred name for this register bit field would be DSIPLL_OUT_DIV_DSICLK. Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 0000_0111

0x0470022C MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_11

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_11

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	DSIPLL_SVS_MODE	SVS. Mode Enable - 0: Normal operation mode - 1: SVS. operation mode In SVS. mode, bit clock, byte clock and dsi clock will be half the frequency of normal operation mode. Normal operational mode setting is 0. Power up value is 0
3:0	RESERVED_BITS3_0	

0x04700230 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_12

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000001A

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_12

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4:0	DSIPLL_MAN_OFFSET	Manual setting for VCO offset Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power on Reset value is 1_1010

0x04700234 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_13

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_13

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2:0	DSIPLL_MAN_SLOPE	Manual setting for VCO slope Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 000

0x04700238 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_14

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_14

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	PLL_SW_RESET	RESET for Digital blocks except control registers. Active high signal. - 1: Assertion - 0: De-assertion Normal operational mode setting is 0. Power up value is 0
0	FORCE_PLL_READY	- 0: PLL_READY from PLL Lock detect will be used - 1: PLL_READY from PLL Lock detect will be bypassed. In other words it will force the PLL_READY to high. This bit is only used as a back up in case the PLL LOCKDETECTOR does not operate correctly. Power up value is 0 Normal value is 0.

0x0470023C MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_15

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000002

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_15

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	RESERVED_BITS2	
1	DSIPLL_IBIAS_CAL_EN	PLL Ibias Calibration Enable - 0: Ibias Calibration disabled - 1: Ibias Calibration enabled Normal operational mode setting is 1 Power up value is 1
0	RESERVED_BITS0	

0x04700240 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_16

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_16

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPLL_CL_LOCKTIME_7_0	Closed Loop Lock time counter value. It specifies the Lock time in number of reference clock cycles after the reference divider. The minimum time required is 50us. Lock Time=cl_locktime<15:0>*ref_cycle_time Normal operational mode setting: 0 Power up value is 0

0x04700244 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_17

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000020

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_17

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPLL_CL_LOCKTIME_15_8	Closed Loop Lock time counter value. It specifies the Lock time in number of reference clock cycles after the reference divider. The minimum time required is 50us Lock Time=cl_locktime<15:0>*ref_cycle_time. Normal operational mode setting: 0010_0000 Power up value is 0010_0000

0x04700248 MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_18

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_18

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_18 (cont.)

Bits	Name	Description
7:0	DSIPLL_OL_LOCKTIME_7_0	Open Loop Lock time. It specifies the lock time in number of reference clock cycles after the reference divider. The minimum time required is 5us. Normal operational mode setting is 1000_1000. Power up value is 0000_0000

0x0470024C MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_19

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000002

MIPI_DSI_1_DSI1_DSIPHY_PLL_CTRL_19

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	DSIPLL_SWCAL_DONE	We are not using SW Calibration anymore. So this bit should be set to '0'. Normal operational mode setting is 0. Power up value is 0
1:0	DSIPLL_OL_LOCKTIME_9_8	Open Loop Lock time. It specifies the lock time in number of reference clock cycles after the reference divider. The minimum time required is 5us. Normal operational mode setting is 00. Power up value is 10

0x04700250 MIPI_DSI_1_DSI1_DSIPHY_PLL_TEST_EFUSE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_TEST_EFUSE

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5	PLLPHY_EFUSE_OVRRIDE_SEL	- 0: Use EFUSE value selected by PLLPHY_DRVSTR_EFUSE_SEL - 1: Override with PLLPHY_EFUSE value. Power up value is 0
4	PLLPHY_DRVSTR_EFUSE_SEL	- 1: Select the efuse used for datalane impedence calibration - 0: Select dedicated PLL calibration efuse Power up value is 0

MIPI_DSI_1_DSI1_DSIPHY_PLL_TEST_EFUSE (cont.)

Bits	Name	Description
3:0	PLLPHY_EFUSE	efuse override value Power up value is 0000

0x04700254 MIPI_DSI_1_DSI1_DSIPHY_PLL_TEST_SANITY_CHECK

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_TEST_SANITY_CHECK

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DSIPLL_SANITY_CHECK	- 1: PLL clock frequency based on power up value. OUTCLK1 = 810MHz, OUTCLK2=OUTCLK3=(OUTCLK1/8). 0: PLL clock frequency based on PLL software configuration Normal operational mode setting is 0. Power up value is 0

0x04700258 MIPI_DSI_1_DSI1_DSIPHY_PLL_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_PLL_DEBUG_SEL	Refer to table at the end of the PLL section to see detailed description of debug bus selections: Debug bus grouping

0x0470025C MIPI_DSI_1_DSI1_RESERVED_PLL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_RESERVED_PLL

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700260 MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000020

MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6	DSIPLL_REF_POLY_SEL	- 0: Poly select is disabled - 1: Poly select is enabled Power up value is 0
5	DSIPLL_OTA_BIAS_SEL	- 0: OTA replica bias is disabled - 1: OTA replica bias is enabled Power up value is 1
4:1	DSIPLL_ANA_TESTMUX_SELECT	PLL Analog Test Mux Select bits Normal operational mode setting is 0000. Power up value is 0000 0x0: Uncalibrated bias current 0x1: Calibrated bias current
0	DSIPLL_ANA_TESTMUX_ENABLE	PLL Analog Test Mux Enable Normal operational mode setting is 0. Power up value is 0

0x04700264 MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL1

Bits	Name	Description
31:5	RESERVED_BITS31_5	

MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL1 (cont.)

Bits	Name	Description
4:1	DSIPLL_DIGCLK_TESTMUX_SELECT	PLL Digital CLK Test Mux Select bits Normal operational mode setting is 0000. Power up value is 0000 0x0: VCO clock 0x1: PLL unlock detect 0x2: Byte clock 0x3: Divided reference clock 0x4: Reference clock 0x5: Feedback clock 0x6: DSI clock 0x7: VCO clock div 2
0	DSIPLL_DIGCLK_TESTMUX_EN	PLL Digital CLK Test Mux Enable Normal operational mode setting is 0. Power up value is 0

0x04700268 MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x0470026C MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL3

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700270 MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL4

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700274 MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL5

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700278 MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL6

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL6

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x0470027C MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL7

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_CTRL7

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700280 MIPI_DSI_1_DSI1_DSIPHY_PLL_RDY

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_RDY

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	PLL_RDY	READ ONLY. monitor pll_rdy Power up value is 0

0x04700284 MIPI_DSI_1_DSI1_DSIPHY_PLL_DBGBUS_STATUS0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_DBGBUS_STATUS0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_PLL_DEBUG_BUS_7_0	READ ONLY. Power up value is 0000_0000

0x04700288 MIPI_DSI_1_DSI1_DSIPHY_PLL_DBGBUS_STATUS1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_DBGBUS_STATUS1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_PLL_DEBUG_BUS_15_8	READ ONLY. Power up value is 0000_0000

0x0470028C MIPI_DSI_1_DSI1_DSIPHY_PLL_DBGBUS_STATUS2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_DBGBUS_STATUS2

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_PLL_DEBUG_BUS_23_16	READ ONLY. Power up value is 0000_0000

0x04700290 MIPI_DSI_1_DSI1_DSIPHY_PLL_DBGBUS_STATUS3

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_DBGBUS_STATUS3

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_PLL_DEBUG_BUS_31_24	READ ONLY. Power up value is 0000_0000

0x04700294 MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_STATUS0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_STATUS0

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700298 MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_STATUS1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_STATUS1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x0470029C MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_STATUS2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_PLL_ANA_STATUS2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700300 MIPI_DSI_1_DSI1_DSIPHY_LN0_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

MIPI_DSI_1_DSI1_DSIPHY_LN0_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	DSIPHY_HSTX_SLEW	DSIPHY Slew Rate Control Normal operational mode setting is 11. Power up value is 11
5	RESERVED_BITS5	
4:0	DSIPHY_HSTX_DLY	This has been de-featured since LLDR Power up value is 0_0000

0x04700304 MIPI_DSI_1_DSI1_DSIPHY_LN0_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_1_DSI1_DSIPHY_LN0_CFG1 (cont.)

Bits	Name	Description
7:5	DSIPHY_PEMPH_STRBOT	Determines how many Pre-Emphasis branches for the bottom termination are enabled. Normal operational mode setting is 000. Power up value is 000.
4	RESERVED_BITS4	
3:1	DSIPHY_PEMPH_STRTOP	Determines how many Pre-Emphasis branches for the top termination are enabled Normal operational mode setting is 000. Power up value is 000.
0	DSIPHY_PEMPH_EN	Enable Signal for Driver Pre-Emphasis.0: Pre-Emphasis is Disabled -1: Pre-Emphasis is Enabled Normal operational mode setting is 0. Power up value is 0

0x04700308 MIPI_DSI_1_DSI1_DSIPHY_LN0_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_CFG2

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:4	DSIPHY_LPTX_SLEW	LPTX slew rate control To enable or disable LPTX-P and LPTX-N independently during test-mode. In functional mode(test_mode=0) if LPTX_EN is high, both LPTX-P and LPTX-N are on. When test_mode=1 and test_mode_hstx_en=0, DSIPHY_LPTX_SLEW[0] enables/disables LPTX-P for a value of 1/0 respectively, while DSIPHY_LPTX_SLEW[1] enables/disables LPTX-N for a value of 1/0 respectively. Power up value is 00
3:0	DSIPHY_LPRX_DLY	- 3:2 : Escape Clock pulse width adjustment - 1:0 : Escape Clock Delay element. Power up value is 0000

0x0470030C MIPI_DSI_1_DSI1_DSIPHY_LN0_TEST_DATAPATH

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_TEST_DATAPATH

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	ANE_BYPASS_EN	Enables analog near-end loopback Power up value is 0
6:4	DMUX_LP_SEL	Mux select for testing purposes - 0xx: Mission Mode - 100: LPRX to LPTX - 110: CDRX to LPTX - 111: REG_TEST to LPTX Power up value is 000
3:2	DMUX_HS_SEL	Mux select for testing purposes - 01: PLL_TEST_CLK to HSTX - 11: Adjacent HSRX signal to HSTX Power up value is 00 0x0: Mission Mode
1	TEST_MODE_HSTX_EN	Enable HSTX when test_mode=1: Power up value is 0
0	FORCE_TEST_MODE	When this bit is set to 1, Enable software control bits of lptx, hstx, lprx, or cdrx for testing purposes Power up value is 0

0x04700310 MIPI_DSI_1_DSI1_DSIPHY_LN0_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_1_DSI1_DSIPHY_LN0_DEBUG_SEL (cont.)

Bits	Name	Description
7:0	DSIPHY_DEBUG_SEL	DSIPHY Data Lane Debug Bus Select Refer to table at the end of the PHY SWI section to see detailed description of Lane debug bus selections. (Debug bus grouping) **Note 1**: Lane debug bus can be observed only when DSIPHY_GLBL_DIGTOP_DEBUG_SEL[DSIPHY_GLBL_DIGTOP_DEBUG_SEL] is set to 8'bxxxx_x11x **Note 2**: Only 1 lane at a time should be selected. Ensure all other lane debug bus mux select is set to 0. Normal operational mode setting is 0000_0000. Power up value is 0000_0000

0x04700314 MIPI_DSI_1_DSI1_DSIPHY_LN0_TEST_STR0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_TEST_STR0

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DSIPHY_STR_VALUE_OVERRIDE	- 0: Calibrated value - 1: Strength override value, DSIPHY_LNn_TEST_STR1 Power up value is 0

0x04700318 MIPI_DSI_1_DSI1_DSIPHY_LN0_TEST_STR1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_TEST_STR1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP	Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT	Power up value is 0000

0x0470031C MIPI_DSI_1_DSI1_DSIPHY_LN0_BIST_CTL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_BIST_CTL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	MISR_SIG_READ	- 11: Select MISR1 - MISR signature for the valid DATA read from TX FIFO - 10: Select MISR0 - MISR signature for the valid DATA write to TX FIFO - 00 or 01: Select BIST error count Power up value is 00
4	MISR_SIG_CLEAR	- 1: Clear both MISR to default signature value 16hFFFF Power up value is 0
3	RESERVED_BIT3	
2	BIST_RX_PRBS_ERROR_INJECT	- 1: Inject Error pattern into RX checker. Power up value is 0
1	BIST_RX_PRBS_GEN_SHORT	- 1:Pattern length is 2^8 - 0:Pattern is generated continuously until bist_rx_prbs_chk_en is disabled Normal operational mode setting is 0 Power up value is 0
0	DSIPHY_ERROR_CLR	- 1: Clear Error count. Power up value is 0

0x04700320 MIPI_DSI_1_DSI1_DSIPHY_LN0_BIST_CTL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_BIST_CTL1

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	DSIPHY_HSRX_TERM_EN	- 1: Enable cross termination for HSRX in BIST mode. Power up value is 0
0	DSIPHY_HSRX_EN	- 1: Enable HSRX in BIST mode. Power up value is 0

0x04700324 MIPI_DSI_1_DSI1_DSIPHY_LN0_RESERVED2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_RESERVED2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700328 MIPI_DSI_1_DSI1_DSIPHY_LN0_BIST_RXCHK_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_BIST_RXCHK_STATUS

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	CHECK_DONE	READ ONLY. This bit is set when the prbs checker is done for short pattern Power up value is 0
1	RXCHK_HEADER_SEL	READ ONLY. PRBS checker Header sel control signal Power up value is 0
0	RXCHK_PRBS_START	READ ONLY. PRBS checker PRBS START control signal. Power up value is 0

0x0470032C MIPI_DSI_1_DSI1_DSIPHY_LN0_HSTX_STR_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_HSTX_STR_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP_STATUS	READ ONLY. Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT_STATUS	READ ONLY. Power up value is 0000

0x04700330 MIPI_DSI_1_DSI1_RESERVED1_PHY_LN0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_RESERVED1_PHY_LN0

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700334 MIPI_DSI_1_DSI1_RESERVED2_PHY_LN0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_RESERVED2_PHY_LN0

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700338 MIPI_DSI_1_DSI1_DSIPHY_LN0_BIST_MISR_STAT0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_BIST_MISR_STAT0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_7_0	READ ONLY. Power up value is 0000_0000

0x0470033C MIPI_DSI_1_DSI1_DSIPHY_LN0_BIST_MISR_STAT1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN0_BIST_MISR_STAT1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_15_8	READ ONLY. Power up value is 0000_0000

0x04700340 MIPI_DSI_1_DSI1_DSIPHY_LN1_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

MIPI_DSI_1_DSI1_DSIPHY_LN1_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	DSIPHY_HSTX_SLEW	DSIPHY Slew Rate Control Normal operational mode setting is 11. Power up value is 11
5	RESERVED_BITS5	
4:0	DSIPHY_HSTX_DLY	This has been de-featured since LLDR Power up value is 0_0000

0x04700344 MIPI_DSI_1_DSI1_DSIPHY_LN1_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:5	DSIPHY_PEMPH_STRBOT	Determines how many Pre-Emphasis branches for the bottom termination are enabled. Normal operational mode setting is 000. Power up value is 000.
4	RESERVED_BITS4	
3:1	DSIPHY_PEMPH_STRTOP	Determines how many Pre-Emphasis branches for the top termination are enabled Normal operational mode setting is 000. Power up value is 000.

MIPI_DSI_1_DSI1_DSIPHY_LN1_CFG1 (cont.)

Bits	Name	Description
0	DSIPHY_PEMPH_EN	Enable Signal for Driver Pre-Emphasis. 0: Pre-Emphasis is Disabled -1: Pre-Emphasis is Enabled Normal operational mode setting is 0. Power up value is 0

0x04700348 MIPI_DSI_1_DSI1_DSIPHY_LN1_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_CFG2

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:4	DSIPHY_LPTX_SLEW	LPTX slew rate control To enable or disable LPTX-P and LPTX-N independently during test-mode. In functional mode(test_mode=0) if LPTX_EN is high, both LPTX-P and LPTX-N are on. When test_mode=1 and test_mode_hstx_en=0, DSIPHY_LPTX_SLEW[0] enables/disables LPTX-P for a value of 1/0 respectively, while DSIPHY_LPTX_SLEW[1] enables/disables LPTX-N for a value of 1/0 respectively. Power up value is 00
3:0	DSIPHY_LPRX_DLY	- 3:2 : Escape Clock pulse width adjustment - 1:0 : Escape Clock Delay element. Power up value is 0000

0x0470034C MIPI_DSI_1_DSI1_DSIPHY_LN1_TEST_DATAPATH

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_TEST_DATAPATH

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	ANE_BYPASS_EN	Enables analog near-end loopback Power up value is 0

MIPI_DSI_1_DSI1_DSIPHY_LN1_TEST_DATAPATH (cont.)

Bits	Name	Description
6:4	DMUX_LP_SEL	Mux select for testing purposes - 0xx: Mission Mode - 100: LPRX to LPTX - 110: CDRX to LPTX - 111: REG_TEST to LPTX Power up value is 000
3:2	DMUX_HS_SEL	Mux select for testing purposes - 01: PLL_TEST_CLK to HSTX - 11: Adjacent HSRX signal to HSTX Power up value is 00 0x0: Mission Mode
1	TEST_MODE_HSTX_EN	Enable HSTX when test_mode=1: Power up value is 0
0	FORCE_TEST_MODE	When this bit is set to 1, Enable software control bits of lptx, hstx, lprx, or cdrx for testing purposes Power up value is 0

0x04700350 MIPI_DSI_1_DSI1_DSIPHY_LN1_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_DEBUG_SEL	DSIPHY Data Lane Debug Bus Select Refer to table at the end of the PHY SWI section to see detailed description of Lane debug bus selections: Debug bus grouping **Note 1**: Lane debug bus can be observed only when DSIPHY_GLBL_DIGTOP_DEBUG_SEL[DSIPHY_GLBL_DIGTOP_DEBUG_SEL] is set to 8'bxxxx_x11x **Note 2**: Only 1 lane at a time should be selected. Ensure all other lane debug bus mux select is set to 0. Normal operational mode setting is 0000_0000. Power up value is 0000_0000

0x04700354 MIPI_DSI_1_DSI1_DSIPHY_LN1_TEST_STR0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_TEST_STR0

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DSIPHY_STR_VALUE_OVERRIDE	- 0: Calibrated value - 1: Strength override value, DSIPHY_LNn_TEST_STR1 Power up value is 0

0x04700358 MIPI_DSI_1_DSI1_DSIPHY_LN1_TEST_STR1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_TEST_STR1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP	Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT	Power up value is 0000

0x0470035C MIPI_DSI_1_DSI1_DSIPHY_LN1_BIST_CTL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_BIST_CTL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	MISR_SIG_READ	- 11: Select MISR1 - MISR signature for the valid DATA read from TX FIFO - 10: Select MISR0 - MISR signature for the valid DATA write to TX FIFO - 00 or 01: Select BIST error count Power up value is 00

MIPI_DSI_1_DSI1_DSIPHY_LN1_BIST_CTL0 (cont.)

Bits	Name	Description
4	MISR_SIG_CLEAR	- 1: Clear both MISR to default signature value 16hFFFF Power up value is 0
3	RESERVED_BIT3	
2	BIST_RX_PRBS_ERROR_INJECT	- 1: Inject Error pattern into RX checker. Power up value is 0
1	BIST_RX_PRBS_GEN_SHORT	- 1:Pattern length is 2^8 - 0:Pattern is generated continuously until bist_rx_prbs_chk_en is disabled Normal operational mode setting is 0 Power up value is 0
0	DSIPHY_ERROR_CLR	- 1: Clear Error count. Power up value is 0

0x04700360 MIPI_DSI_1_DSI1_DSIPHY_LN1_BIST_CTL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_BIST_CTL1

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	DSIPHY_HSRX_TERM_EN	- 1: Enable cross termination for HSRX in BIST mode. Power up value is 0
0	DSIPHY_HSRX_EN	- 1: Enable HSRX in BIST mode. Power up value is 0

0x04700364 MIPI_DSI_1_DSI1_DSIPHY_LN1_RESERVED2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_RESERVED2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700368 MIPI_DSI_1_DSI1_DSIPHY_LN1_BIST_RXCHK_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_BIST_RXCHK_STATUS

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	CHECK_DONE	READ ONLY. This bit is set when the prbs checker is done for short pattern Power up value is 0
1	RXCHK_HEADER_SEL	READ ONLY. PRBS checker Header sel control signal Power up value is 0
0	RXCHK_PRBS_START	READ ONLY. PRBS checker PRBS START control signal. Power up value is 0

0x0470036C MIPI_DSI_1_DSI1_DSIPHY_LN1_HSTX_STR_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_HSTX_STR_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP_STATUS	READ ONLY. Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT_STATUS	READ ONLY. Power up value is 0000

0x04700370 MIPI_DSI_1_DSI1_RESERVED1_PHY_LN1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_RESERVED1_PHY_LN1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700374 MIPI_DSI_1_DSI1_RESERVED2_PHY_LN1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_RESERVED2_PHY_LN1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700378 MIPI_DSI_1_DSI1_DSIPHY_LN1_BIST_MISR_STAT0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_BIST_MISR_STAT0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_7_0	READ ONLY. Power up value is 0000_0000

0x0470037C MIPI_DSI_1_DSI1_DSIPHY_LN1_BIST_MISR_STAT1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN1_BIST_MISR_STAT1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_15_8	READ ONLY. Power up value is 0000_0000

0x04700380 MIPI_DSI_1_DSI1_DSIPHY_LN2_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

MIPI_DSI_1_DSI1_DSIPHY_LN2_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	DSIPHY_HSTX_SLEW	DSIPHY Slew Rate Control Normal operational mode setting is 11. Power up value is 11
5	RESERVED_BITS5	
4:0	DSIPHY_HSTX_DLY	This has been de-featured since LLDR Power up value is 0_0000

0x04700384 MIPI_DSI_1_DSI1_DSIPHY_LN2_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:5	DSIPHY_PEMPH_STRBOT	Determines how many Pre-Emphasis branches for the bottom termination are enabled. Normal operational mode setting is 000. Power up value is 000.
4	RESERVED_BITS4	
3:1	DSIPHY_PEMPH_STRTOP	Determines how many Pre-Emphasis branches for the top termination are enabled Normal operational mode setting is 000. Power up value is 000.
0	DSIPHY_PEMPH_EN	Enable Signal for Driver Pre-Emphasis. 0: Pre-Emphasis is Disabled -1: Pre-Emphasis is Enabled Normal operational mode setting is 0. Power up value is 0

0x04700388 MIPI_DSI_1_DSI1_DSIPHY_LN2_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_CFG2

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:4	DSIPHY_LPTX_SLEW	LPTX slew rate control To enable or disable LPTX-P and LPTX-N independently during test-mode. In functional mode(test_mode=0) if LPTX_EN is high, both LPTX-P and LPTX-N are on. When test_mode=1 and test_mode_hstx_en=0, DSIPHY_LPTX_SLEW[0] enables/disables LPTX-P for a value of 1/0 respectively, while DSIPHY_LPTX_SLEW[1] enables/disables LPTX-N for a value of 1/0 respectively. Power up value is 00
3:0	DSIPHY_LPRX_DLY	- 3:2 : Escape Clock pulse width adjustment - 1:0 : Escape Clock Delay element. Power up value is 0000

0x0470038C MIPI_DSI_1_DSI1_DSIPHY_LN2_TEST_DATAPATH

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_TEST_DATAPATH

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	ANE_BYPASS_EN	Enables analog near-end loopback Power up value is 0
6:4	DMUX_LP_SEL	Mux select for testing purposes - 0xx: Mission Mode - 100: LPRX to LPTX - 110: CDRX to LPTX - 111: REG_TEST to LPTX Power up value is 000
3:2	DMUX_HS_SEL	Mux select for testing purposes - 01: PLL_TEST_CLK to HSTX - 11: Adjacent HSRX signal to HSTX Power up value is 00 0x0: Mission Mode
1	TEST_MODE_HSTX_EN	Enable HSTX when test_mode=1: Power up value is 0

MIPI_DSI_1_DSI1_DSIPHY_LN2_TEST_DATAPATH (cont.)

Bits	Name	Description
0	FORCE_TEST_MODE	When this bit is set to 1, enable software control bits of lptx, hstx, lprx, or cdrx for testing purposes Power up value is 0

0x04700390 MIPI_DSI_1_DSI1_DSIPHY_LN2_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_DEBUG_SEL	DSIPHY Data Lane Debug Bus Select Refer to table at the end of the PHY SWI section to see detailed description of Lane debug bus selections: Debug bus grouping **Note 1**: Lane debug bus can be observed only when DSIPHY_GLBL_DIGTOP_DEBUG_SEL[DSIPHY_GLBL_DIGTOP_DEBUG_SEL] is set to 8'bxxxx_x11x **Note 2**: Only 1 lane at a time should be selected. Ensure all other lane debug bus mux select is set to 0. Normal operational mode setting is 0000_0000. Power up value is 0000_0000

0x04700394 MIPI_DSI_1_DSI1_DSIPHY_LN2_TEST_STR0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_TEST_STR0

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DSIPHY_STR_VALUE_OVERRIDE	- 0: Calibrated value - 1: Strength override value, DSIPHY_LNn_TEST_STR1 Power up value is 0

0x04700398 MIPI_DSI_1_DSI1_DSIPHY_LN2_TEST_STR1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_TEST_STR1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP	Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT	Power up value is 0000

0x0470039C MIPI_DSI_1_DSI1_DSIPHY_LN2_BIST_CTL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_BIST_CTL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	MISR_SIG_READ	- 11: Select MISR1 - MISR signature for the valid DATA read from TX FIFO - 10: Select MISR0 - MISR signature for the valid DATA write to TX FIFO - 00 or 01: Select BIST error count Power up value is 00
4	MISR_SIG_CLEAR	- 1: Clear both MISR to default signature value 16hFFFF Power up value is 0
3	RESERVED_BIT3	
2	BIST_RX_PRBS_ERROR_INJECT	- 1: Inject Error pattern into RX checker. Power up value is 0
1	BIST_RX_PRBS_GEN_SHORT	- 1:Pattern length is 2^8 - 0:Pattern is generated continuously until bist_rx_prbs_chk_en is disabled Normal operational mode setting is 0 Power up value is 0
0	DSIPHY_ERROR_CLR	- 1: Clear Error count. Power up value is 0

0x047003A0 MIPI_DSI_1_DSI1_DSIPHY_LN2_BIST_CTL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_BIST_CTL1

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	DSIPHY_HSRX_TERM_EN	- 1: Enable cross termination for HSRX in BIST mode. Power up value is 0
0	DSIPHY_HSRX_EN	- 1: Enable HSRX in BIST mode. Power up value is 0

0x047003A4 MIPI_DSI_1_DSI1_DSIPHY_LN2_RESERVED2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_RESERVED2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x047003A8 MIPI_DSI_1_DSI1_DSIPHY_LN2_BIST_RXCHK_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_BIST_RXCHK_STATUS

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	CHECK_DONE	READ ONLY. This bit is set when the prbs checker is done for short pattern Power up value is 0
1	RXCHK_HEADER_SEL	READ ONLY. PRBS checker Header sel control signal Power up value is 0
0	RXCHK_PRBS_START	READ ONLY. PRBS checker PRBS START control signal. Power up value is 0

0x047003AC MIPI_DSI_1_DSI1_DSIPHY_LN2_HSTX_STR_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_HSTX_STR_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP_STATUS	READ ONLY. Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT_STATUS	READ ONLY. Power up value is 0000

0x047003B0 MIPI_DSI_1_DSI1_RESERVED1_PHY_LN2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_RESERVED1_PHY_LN2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x047003B4 MIPI_DSI_1_DSI1_RESERVED2_PHY_LN2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_RESERVED2_PHY_LN2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x047003B8 MIPI_DSI_1_DSI1_DSIPHY_LN2_BIST_MISR_STAT0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_BIST_MISR_STAT0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_7_0	READ ONLY. Power up value is 0000_0000

0x047003BC MIPI_DSI_1_DSI1_DSIPHY_LN2_BIST_MISR_STAT1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN2_BIST_MISR_STAT1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_15_8	READ ONLY. Power up value is 0000_0000

0x047003C0 MIPI_DSI_1_DSI1_DSIPHY_LN3_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

MIPI_DSI_1_DSI1_DSIPHY_LN3_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	DSIPHY_HSTX_SLEW	DSIPHY Slew Rate Control Normal operational mode setting is 11. Power up value is 11
5	RESERVED_BITS5	
4:0	DSIPHY_HSTX_DLY	This has been de-featured since LLDR Power up value is 0_0000

0x047003C4 MIPI_DSI_1_DSI1_DSIPHY_LN3_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:5	DSIPHY_PEMPH_STRBOT	Determines how many Pre-Emphasis branches for the bottom termination are enabled. Normal operational mode setting is 000. Power up value is 000.
4	RESERVED_BITS4	
3:1	DSIPHY_PEMPH_STRTOP	Determines how many Pre-Emphasis branches for the top termination are enabled Normal operational mode setting is 000. Power up value is 000.
0	DSIPHY_PEMPH_EN	Enable Signal for Driver Pre-Emphasis.0: Pre-Emphasis is Disabled -1: Pre-Emphasis is Enabled Normal operational mode setting is 0. Power up value is 0

0x047003C8 MIPI_DSI_1_DSI1_DSIPHY_LN3_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_CFG2

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:4	DSIPHY_LPTX_SLEW	LPTX slew rate control To enable or disable LPTX-P and LPTX-N independently during test-mode. In functional mode(test_mode=0) if LPTX_EN is high, both LPTX-P and LPTX-N are on. When test_mode=1 and test_mode_hstx_en=0, DSIPHY_LPTX_SLEW[0] enables/disables LPTX-P for a value of 1/0 respectively, while DSIPHY_LPTX_SLEW[1] enables/disables LPTX-N for a value of 1/0 respectively. Power up value is 00
3:0	DSIPHY_LPRX_DLY	- 3:2 : Escape Clock pulse width adjustment - 1:0 : Escape Clock Delay element. Power up value is 0000

0x047003CC MIPI_DSI_1_DSI1_DSIPHY_LN3_TEST_DATAPATH

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_TEST_DATAPATH

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	ANE_BYPASS_EN	Enables analog near-end loopback Power up value is 0
6:4	DMUX_LP_SEL	Mux select for testing purposes - 0xx: Mission Mode - 100: LPRX to LPTX - 110: CDRX to LPTX - 111: REG_TEST to LPTX Power up value is 000
3:2	DMUX_HS_SEL	Mux select for testing purposes - 01: PLL_TEST_CLK to HSTX - 11: Adjacent HSRX signal to HSTX Power up value is 00 0x0: Mission Mode
1	TEST_MODE_HSTX_EN	Enable HSTX when test_mode=1: Power up value is 0
0	FORCE_TEST_MODE	When this bit is set to 1, Enable software control bits of lptx, hstx, lprx, or cdrx for testing purposes Power up value is 0

0x047003D0 MIPI_DSI_1_DSI1_DSIPHY_LN3_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_1_DSI1_DSIPHY_LN3_DEBUG_SEL (cont.)

Bits	Name	Description
7:0	DSIPHY_DEBUG_SEL	DSIPHY Data Lane Debug Bus Select Refer to table at the end of the PHY SWI section to see detailed description of Lane debug bus selections: Debug bus grouping **Note 1**: Lane debug bus can be observed only when DSIPHY_GLBL_DIGTOP_DEBUG_SEL[DSIPHY_GLBL_DIGTOP_DEBUG_SEL] is set to 8'bxxxx_x11x **Note 2**: Only 1 lane at a time should be selected. Ensure all other lane debug bus mux select is set to 0. Normal operational mode setting is 0000_0000. Power up value is 0000_0000

0x047003D4 MIPI_DSI_1_DSI1_DSIPHY_LN3_TEST_STR0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_TEST_STR0

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DSIPHY_STR_VALUE_OVERRIDE	- 0: Calibrated value - 1: Strength override value, DSIPHY_LNn_TEST_STR1 Power up value is 0

0x047003D8 MIPI_DSI_1_DSI1_DSIPHY_LN3_TEST_STR1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_TEST_STR1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP	Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT	Power up value is 0000

0x047003DC MIPI_DSI_1_DSI1_DSIPHY_LN3_BIST_CTL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_BIST_CTL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	MISR_SIG_READ	- 11: Select MISR1 - MISR signature for the valid DATA read from TX FIFO - 10: Select MISR0 - MISR signature for the valid DATA write to TX FIFO - 00 or 01: Select BIST error count Power up value is 00
4	MISR_SIG_CLEAR	- 1: Clear both MISR to default signature value 16hFFFF Power up value is 0
3	RESERVED_BIT3	
2	BIST_RX_PRBS_ERROR_INJECT	- 1: Inject Error pattern into RX checker. Power up value is 0
1	BIST_RX_PRBS_GEN_SHORT	- 1:Pattern length is 2^8 - 0:Pattern is generated continuously until bist_rx_prbs_chk_en is disabled Normal operational mode setting is 0 Power up value is 0
0	DSIPHY_ERROR_CLR	- 1: Clear Error count. Power up value is 0

0x047003E0 MIPI_DSI_1_DSI1_DSIPHY_LN3_BIST_CTL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_BIST_CTL1

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	DSIPHY_HSRX_TERM_EN	- 1: Enable cross termination for HSRX in BIST mode. Power up value is 0
0	DSIPHY_HSRX_EN	- 1: Enable HSRX in BIST mode. Power up value is 0

0x047003E4 MIPI_DSI_1_DSI1_DSIPHY_LN3_RESERVED2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_RESERVED2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x047003E8 MIPI_DSI_1_DSI1_DSIPHY_LN3_BIST_RXCHK_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_BIST_RXCHK_STATUS

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	CHECK_DONE	READ ONLY. This bit is set when the prbs checker is done for short pattern. Power up value is 0
1	RXCHK_HEADER_SEL	READ ONLY. PRBS checker Header sel control signal Power up value is 0
0	RXCHK_PRBS_START	READ ONLY. PRBS checker PRBS START control signal. Power up value is 0

0x047003EC MIPI_DSI_1_DSI1_DSIPHY_LN3_HSTX_STR_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_HSTX_STR_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP_STATUS	READ ONLY. Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT_STATUS	READ ONLY. Power up value is 0000

0x047003F0 MIPI_DSI_1_DSI1_RESERVED1_PHY_LN3

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_RESERVED1_PHY_LN3

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x047003F4 MIPI_DSI_1_DSI1_RESERVED2_PHY_LN3

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_RESERVED2_PHY_LN3

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x047003F8 MIPI_DSI_1_DSI1_DSIPHY_LN3_BIST_MISR_STAT0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_BIST_MISR_STAT0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_7_0	READ ONLY. Power up value is 0000_0000

0x047003FC MIPI_DSI_1_DSI1_DSIPHY_LN3_BIST_MISR_STAT1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LN3_BIST_MISR_STAT1

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_1_DSI1_DSIPHY_LN3_BIST_MISR_STAT1 (cont.)

Bits	Name	Description
7:0	DSIPHY_BISTCHKERR_MISRSIG_15_8	READ ONLY. Power up value is 0000_0000

0x04700400 MIPI_DSI_1_DSI1_DSIPHY_LNCK_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

MIPI_DSI_1_DSI1_DSIPHY_LNCK_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	DSIPHY_HSTX_SLEW	DSIPHY Slew Rate Control Normal operational mode setting is 11. Power up value is 11
5	RESERVED_BITS5	
4:0	DSIPHY_HSTX_DLY	This has been de-featured since LLDR Power up value is 0_0000

0x04700404 MIPI_DSI_1_DSI1_DSIPHY_LNCK_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:5	DSIPHY_PEMPH_STRBOT	Determines how many Pre-Emphasis branches for the bottom termination are enabled. Normal operational mode setting is 000. Power up value is 000.
4	RESERVED_BITS4	
3:1	DSIPHY_PEMPH_STRTOP	Determines how many Pre-Emphasis branches for the top termination are enabled. Normal operational mode setting is 000. Power up value is 000.

MIPI_DSI_1_DSI1_DSIPHY_LNCK_CFG1 (cont.)

Bits	Name	Description
0	DSIPHY_PEMPH_EN	Enable Signal for Driver Pre-Emphasis. 0: Pre-Emphasis is Disabled -1: Pre-Emphasis is Enabled Normal operational mode setting is 0. Power up value is 0

0x04700408 MIPI_DSI_1_DSI1_DSIPHY_LNCK_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_CFG2

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:4	DSIPHY_LPTX_SLEW	LPTX slew rate control To enable or disable LPTX-P and LPTX-N independently during test-mode. In functional mode(test_mode=0) if LPTX_EN is high, both LPTX-P and LPTX-N are on. When test_mode=1 and test_mode_hstx_en=0, DSIPHY_LPTX_SLEW[0] enables/disables LPTX-P for a value of 1/0 respectively, while DSIPHY_LPTX_SLEW[1] enables/disables LPTX-N for a value of 1/0 respectively. Power up value is 00
3:0	DSIPHY_LPRX_DLY	- 3:2 : Escape Clock pulse width adjustment - 1:0 : Escape Clock Delay element. Power up value is 0000

0x0470040C MIPI_DSI_1_DSI1_DSIPHY_LNCK_TEST_DATAPATH

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_TEST_DATAPATH

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	ANE_BYPASS_EN	Enables analog near-end loopback Power up value is 0

MIPI_DSI_1_DSI1_DSIPHY_LNCK_TEST_DATAPATH (cont.)

Bits	Name	Description
6:4	DMUX_LP_SEL	Mux select for testing purposes - 0xx: Mission Mode - 100: LPRX to LPTX - 110: CDRX to LPTX - 111: REG_TEST to LPTX Power up value is 00
3:2	DMUX_HS_SEL	Mux select for testing purposes - 01: PLL_TEST_CLK to HSTX - 11: Adjacent HSRX signal to HSTX Power up value is 00 0x0: Mission Mode
1	TEST_MODE_HSTX_EN	Enable HSTX when test_mode=1: Power up value is 0
0	FORCE_TEST_MODE	When this bit is set to 1, Enable software control bits of lptx, hstx, lprx, or cdrx for testing purposes Power up value is 0

0x04700410 MIPI_DSI_1_DSI1_DSIPHY_LNCK_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_DEBUG_SEL	DSIPHY Data Lane Debug Bus Select Refer to Table at the end of the PHY SWI section to see detailed description of Clock lane debug bus selections: Debug bus grouping **Note 1**: Lane debug bus can be observed only when DSIPHY_GLBL_DIGTOP_DEBUG_SEL[DSIPHY_GLBL_DIGTOP_DEBUG_SEL] is set to 8'bxxxx_x11x **Note 2**: Only 1 lane at a time should be selected. Ensure all other lane debug bus mux select is set to 0. Normal operational mode setting is 0000_0000. Power up value is 0000_0000

0x04700414 MIPI_DSI_1_DSI1_DSIPHY_LNCK_TEST_STR0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_TEST_STR0

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DSIPHY_STR_VALUE_OVERRIDE	- 0: Calibrated value - 1: Strength override value, DSIPHY_LNn_TEST_STR1 Power up value is 0

0x04700418 MIPI_DSI_1_DSI1_DSIPHY_LNCK_TEST_STR1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_TEST_STR1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP	Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT	Power up value is 0000

0x0470041C MIPI_DSI_1_DSI1_DSIPHY_LNCK_BIST_CTL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_BIST_CTL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	MISR_SIG_READ	- 11: Select MISR1 - MISR signature for the valid DATA read from TX FIFO - 10: Select MISR0 - MISR signature for the valid DATA write to TX FIFO - 00 or 01: Select BIST error count Power up value is 00

MIPI_DSI_1_DSI1_DSIPHY_LNCK_BIST_CTL0 (cont.)

Bits	Name	Description
4	MISR_SIG_CLEAR	- 1: Clear both MISR to default signature value 16'hFFFF Power up value is 0
3	RESERVED_BITS3	
2	BIST_RX_PRBS_ERROR_INJECT	- 1: Inject Error pattern into RX checker. Power up value is 0
1	BIST_RX_PRBS_GEN_SHORT	- 1:Pattern length is 2^8 - 0:Pattern is generated continuously until bist_rx_prbs_chk_en is disabled Normal operational mode setting is 0 Power up value is 0
0	DSIPHY_ERROR_CLR	- 1: Clear Error count. Power up value is 0

0x04700420 MIPI_DSI_1_DSI1_DSIPHY_LNCK_BIST_CTL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_BIST_CTL1

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	DSIPHY_HSRX_TERM_EN	- 1: Enable cross termination for HSRX in BIST mode. Power up value is 0
0	DSIPHY_HSRX_EN	- 1: Enable HSRX in BIST mode. Power up value is 0

0x04700424 MIPI_DSI_1_DSI1_DSIPHY_LNCK_RESERVED1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_RESERVED1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700428 MIPI_DSI_1_DSI1_DSIPHY_LNCK_BIST_RXCHK_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_BIST_RXCHK_STATUS

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	CHECK_DONE	READ ONLY. This bit is set when the prbs checker is done for short pattern. Power up value is 0
1	RXCHK_HEADER_SEL	READ ONLY. PRBS checker Header sel control signal Power up value is 0
0	RXCHK_PRBS_START	READ ONLY. PRBS checker PRBS START control signal. Power up value is 0

0x0470042C MIPI_DSI_1_DSI1_DSIPHY_LNCK_HSTX_STR_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_HSTX_STR_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP_STATUS	READ ONLY. Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT_STATUS	READ ONLY. Power up value is 0000

0x04700430 MIPI_DSI_1_DSI1_RESERVED1_PHY_LNCK

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_RESERVED1_PHY_LNCK

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700434 MIPI_DSI_1_DSI1_RESERVED2_PHY_LNCK

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_RESERVED2_PHY_LNCK

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700438 MIPI_DSI_1_DSI1_DSIPHY_LNCK_BIST_MISR_STAT0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_BIST_MISR_STAT0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_7_0	READ ONLY. Power up value is 0000_0000

0x0470043C MIPI_DSI_1_DSI1_DSIPHY_LNCK_BIST_MISR_STAT1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LNCK_BIST_MISR_STAT1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_15_8	READ ONLY. Power up value is 0000_0000

0x04700440 MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000018

NOTE The preffered name for all global DSIPHY_TIMING_CTRL_n registers is DSIPHY_GLBL_TIMING_CTRL_n.

MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_CLK_ZERO	DSIPHY tCLK-ZERO Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0001_1000. Power up value is 0b0001_1000

0x04700444 MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000004

MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_CLK_TRAIL	DSIPHY tCLK-TRAIL Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0000_0100. Power up value is 0b0000_0100

0x04700448 MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000007

MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_2

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_CLK_PREPARE	DSIPHY tCLK-PREPARE Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0000_0111. Power up value is 0b0000_0111

0x0470044C MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_3

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700450 MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000008

MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_4

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_HS_EXIT	DSIPHY tHS-EXIT Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0000_1000. Power up value is 0b0000_1000

0x04700454 MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000018

MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_5

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_HS_ZERO	DSIPHY tHS-ZERO Timing Parameter. Due to design implementation limitation, tHS-ZERO has to be set greater than 24 (>24). Set to 24 for typical operation and above 24 when HS settle time need to be expended. Any value set between 0 and 24 will cause un-expected high speed data transfer behavior such as data loss or miss sync pattern. Normal operational mode setting is 0b0001_1000. Note: Each bit increment represents 1UI time delay increment Power up value is 0b0001_1000

0x04700458 MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_6

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000009

MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_6

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_HS_PREPARE	DSIPHY tHS-PREPARE Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0000_1001. Power up value is 0b0000_1001

0x0470045C MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_7

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000008

MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_7

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_HS_TRAIL	DSIPHY tHS-TRAIL Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0000_1000. Power up value is 0b0000_1000

0x04700460 MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_8

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000001

MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_8

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_HS_RQST	DSIPHY tHS-RQST Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0000_0001. Power up value is 0b0000_0001

0x04700464 MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_9

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000013

MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_9

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	DSIPHY_T_TA_SURE	DSIPHY tTA-SURE Timing Parameter. Due to design implementation limit, tTA-SURE has to be set greater than 1 (>1). Set to 2 for typical operation and above 2 if bus turn-around time need to be expended. Any value set to 0 or 1 will cause un-expected behavior during bus direction turn around process. NOTE: Power up value must be reconfigured to operational mode setting, i.e., a minimum of 010 Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 010 Power up value is 001
3	RESERVED_BITS3	
2:0	DSIPHY_T_TA_GO	DSIPHY tTA-GO Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 011. Power up value is 011

0x04700468 MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_10

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000004

MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_10

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2:0	DSIPHY_T_TA_GET	DSIPHY tTA-GET Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b100. Power up value is 0b100

0x0470046C MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_11

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_TIMING_CTRL_11

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_TRIG3_CMD	DSIPHY TX Escape Trigger[3] programmable command sequence Normal operational mode setting is 0b0000_0000. Power up value is 0b0000_0000

0x04700470 MIPI_DSI_1_DSI1_DSIPHY_CTRL_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

NOTE : The preferred name for this register is DSIPHY_GLBL_PWR_CFG

MIPI_DSI_1_DSI1_DSIPHY_CTRL_0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6	DSIPHY_DIGTOP_PWRDN_B	Digital Control block Power Down. - 1---Normal operation - 0---Digital block power down mode Power up value is 0
5	RESERVED_BITS5	
4	DSIPHY_DLN3_SHUTDOWNB	DSIPHY Data Lane 3 Power Down. 1: Normal operation - 0: Data LN3 NPL Block powerdown Note: Preferred name for *_SHUTDOWNB bits are *_PWRDN_B Normal operational mode setting is 1. Power up value is 0
3	DSIPHY_DLN2_SHUTDOWNB	DSIPHY Data Lane 2 Power Down. - 1: Normal operation - 0: Data LN2 NPL Block powerdown Note: Preferred name for *_SHUTDOWNB bits are *_PWRDN_B Normal operational mode setting is 1. Power up value is 0

MIPI_DSI_1_DSI1_DSIPHY_CTRL_0 (cont.)

Bits	Name	Description
2	DSIPHY_CLK_SHUTDOWNB	DSIPHY Clock Lane Power Down. 1: Normal operation - 0: NPL Block powerdown Note: Preferred name for *_SHUTDOWNB bits are *_PWRDN_B Normal operational mode setting is 1. Power up value is 0
1	DSIPHY_DLN1_SHUTDOWNB	DSIPHY Data Lane 1Power Down. - 1: Normal operation - 0: Data LN1 NPL Block powerdown Note: Preferred name for *_SHUTDOWNB bits are *_PWRDN_B Normal operational mode setting is 1. Power up value is 0
0	DSIPHY_DLN0_SHUTDOWNB	DSIPHY Data Lane 0 Power Down. 1: Normal operation - 0: Data LN0 NPL Block powerdown Note: Preferred name for *_SHUTDOWNB bits are *_PWRDN_B Normal operational mode setting is 1. Power up value is 0

0x04700474 MIPI_DSI_1_DSI1_DSIPHY_CTRL_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

NOTE : Preferred name for this register is DSIPHY_GLBL_RESET_CFG

MIPI_DSI_1_DSI1_DSIPHY_CTRL_1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	DSIPHY_SW_RESET	RESET for Digital blocks except control registers. Active high signal. - 1: Assertion - 0: De-assertion Normal operational mode setting is 0. Power up value is 0
6:0	RESERVED_BITS6_0	

0x04700478 MIPI_DSI_1_DSI1_DSIPHY_CTRL_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_CTRL_2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x0470047C MIPI_DSI_1_DSI1_DSIPHY_CTRL_3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000010

MIPI_DSI_1_DSI1_DSIPHY_CTRL_3

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	DSIPHY_BITCLK_HS_SEL	- 0: bitclk from left side, - 1: bitclk from right side Power up value is 1
3:0	RESERVED_BITS3_0	

0x04700480 MIPI_DSI_1_DSI1_DSIPHY_STRENGTH_CTRL_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_STRENGTH_CTRL_0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_STR_LP_N	- 0000: 2-9.5 pF load. - 0010: 9.5-18 pF load - 0100: 18-25 pF load. - 0110: 25-35 pF load. - 1100: 35-65 pF load. - 1111: 65-70 pF load. Operational mode value is 1111 Power up value is 0000

MIPI_DSI_1_DSI1_DSIPHY_STRENGTH_CTRL_0 (cont.)

Bits	Name	Description
3:0	DSIPHY_STR_LP_P	- 0000: 2-9.5 pF load. - 0010: 9.5-18 pF load - 0100: 18-25 pF load. - 0110: 25-35 pF load. - 1100: 35-65 pF load. - 1111: 65-70 pF load. Operational mode value is 1111 Power up value is 0000

0x04700484 MIPI_DSI_1_DSI1_DSIPHY_STRENGTH_CTRL_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_STRENGTH_CTRL_1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04700488 MIPI_DSI_1_DSI1_DSIPHY_STRENGTH_CTRL_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

NOTE The preferred name of this register is DSIPHY_GLBL_LPRX_CFG

MIPI_DSI_1_DSI1_DSIPHY_STRENGTH_CTRL_2

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	DSIPHY_LN_CTRL_2	Enable for Low Power Receiver.1: LP RX is enabled -0: LP RX is disabled Note; The preferred name for this register bit should be DSIPHY_LPRX_EN Power up value is 0
1	DSIPHY_LN_CTRL_1	Enable for Contention Detection Receiver.1: CD RX is enabled. -0: CD RX is disabled Note : The preferred name for this register bit should be DSIPHY_CDRX_EN Power up value is 0

MIPI_DSI_1_DSI1_DSIPHY_STRENGTH_CTRL_2 (cont.)

Bits	Name	Description
0	RESERVED_BITS0	

0x0470048C MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL0

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5	BIST_LP_EN_FIXPAT	send one of selected 32 fixed pattern to LPTD path Power up value is 0
4:3	RESERVED_BITS4_3	
2:1	BIST_TX_PATSEL	selection of 2 bist pattern types. - 01---Fixed Pattern - 1x---Channel Test Pattern - 00---not used Normal operational mode setting is 00. Power up value is 00
0	BIST_EN_TX_PRBS	Power up value is 0

0x04700490 MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL1

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	BIST_TX_TEST_PAT_SEL	selection of channel test pattern generation. - 00 : Medium Frequency Pattern(0011_0011, 1100_1100) - 01 : Low Frequency Pattern(1110_0011, 0001_1100) - 10 : High Frequency Pattern(0101_0101,1010_1010) - 11 : not used Normal operational mode setting is 00. Power up value is 00

MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL1 (cont.)

Bits	Name	Description
4:0	BIST_TX_FIXPAT_SEL	- 32 fixed pattern selection Normal operational mode setting is 00000. Power up value is 00000 <sel> : <bist_fixedpat(7:0)> - 00000: 0000_0101 - 00001: 1111_1010 - 00010: 1111_1111 - 00011: 0000_0000 - 00100: 0011_0011 - 00101: 0101_0101 - 00110: 0001_0001 - 00111: 1110_1110 - 01000: 1111_0100 - 01001: 0000_1010 - 01010: 0000_0110 - 01011: 0111_0111 - 01100: 0001_1100 - 01101: 1110_0011 - 01110: 1100_0001 - 01111: 0011_1110 - 10000: 1111_1010 - 10001: 0000_0101 - 10010: 0000_0000 - 10011: 1111_1111 - 10100: 0011_0011 - 10101: 1010_1010 - 10110: 1110_1110 - 10111: 0001_0001 - 11000: 1111_0100 - 11001: 1111_0100 - 11010: 1111_1001 - 11011: 1000_1000 - 11100: 1110_0011 - 11101: 1110_0011 - 11110: 1100_0001 - 11111: 1100_0001

0x04700494 MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000B1

MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL2

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BIST_PRBS_POLY	full programmable prbs pattern. Default pattern is 1 + x4 + x5 + x7 Normal operational mode setting is 1011_0001 Power up value is 1011_0001

0x04700498 MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000FF

MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL3

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BIST_PRBS_SEED	rx data seed to compare w/ input data and start rx side prbs gen (tx_prbs_seed_sel has to be set to 1) Invalid values: 0x00 and 0x1F Normal operational mode setting is 1111_1111 Power up value is 1111_1111

0x0470049C MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL4

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	DSIPHY_BIST_LNCK_HS_REQUEST	DSIPHY_BIST_LNCK_HS_REQUEST set to 1 and any of DSIPHY_BIST_SEL[3:0] being set, starts Clock lane TX request for Clock lane HS data transition sequence. Prior to setting this bit, any of DSIPHY_BIST_SEL[3:0] must be set for at least 3 ESCCLK cycles Normal operational mode setting is 0. Power up value is 0

MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL4 (cont.)

Bits	Name	Description
3:0	DSIPHY_BIST_SEL	DSIPHY_BIST_SEL<i> set to one indicates the data lane is enabled for PHY BIST. Any one of the data lane bist_sel is on will automatically enable the clock lane. Default is set to zero, data lane will be enabled by controller. Note: for 45nm, data lane enable must go through DSI controller software control register. DSIPHY_BIST_SEL only indicates the HS TX byte data either from BIST pattern generator or from controller. For 28nm, DSIPH_BIST_SEL[3:0] os OR-ed with lane enable control driven by controller to eliminate the dependence to controller for PHY BIST. Normal operational mode setting is 0000. Power up value is 0000

0x047004A0 MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_BIST_CTRL5

Bits	Name	Description
31:4	RESERVED_BITS31_4	
3:0	BIST_RX_PRBS_CHK_EN	bist_rx_prbs_chk_en<i> is BIST prbs checker enable for each data lane. <0> enable DL0 checker, <1> enable DL1, <2> enable DL2 checker, <3> enable DL3. To enable bist check must to make sure en_tx_prbs is set to 0. (rx checker state machine start to set header sel to high, patgen start to send header).It also goes to pad_dataln as hsrx_en.Setting this bit to high also turns the high speed receiver on. each receiver lane has its own BIST PRBS checker. Normal operational mode setting is 0000. Power up value is 0000

0x047004A4 MIPI_DSI_1_DSI1_DSIPHY_GLBL_MISR_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_GLBL_MISR_CTRL

Bits	Name	Description
31:4	RESERVED_BITS31_4	

MIPI_DSI_1_DSI1_DSIPHY_GLBL_MISR_CTRL (cont.)

Bits	Name	Description
3:0	DSIPHY_MISR_EN	DSIPHY_MISR_en<i> is MISR enable for each data lane <i>. Power up value is 0000

0x047004A8 MIPI_DSI_1_DSI1_DSIPHY_GLBL_TEST_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_GLBL_TEST_CTRL

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6	TEST_ESC_CLK_SEL	-0: Mission mode. Select escclk from mmss_cc -1: escclk from test refclk div2. Power up value is 0
5:4	TEST_BYTECLK_SEL	- 00 : Mission mode. Select bytclk from cc - 01: Tied to ground. - 10 : byteclk from test byteclk1. - 11: byteclk from test byteclk 2. Power up value is 00
3	RESERVED_BITS3	
2:1	PLL_TEST_MODE_SEL	- 00: send bitclk to clock lane pad - 01: send the byteclk to clock lane pad - 10: send escclk to clock lane pad - 11: send the pn_rxhs_clk to clock lane pad Power up value is 00
0	DSIPHY_PLL_TESTMODE	Power up value is 0

0x047004AC MIPI_DSI_1_DSI1_DSIPHY_GLBL_DIGTOP_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_GLBL_DIGTOP_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DIGTOP_DEBUG_SEL	Refer to table at the end of the PHY SWI section to see detailed description of digital top debug bus selections.

0x047004B0 MIPI_DSI_1_DSI1_DSIPHY_LDO_CNTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_LDO_CNTRL

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:3	LDO_VREF_SEL	DSIPHY Regulator Reference Select. Selects the value of reference voltage for the DSIPHY LDO Regulator. When LDO_VREF_DIV_EN = 1 - 000 : 0.400V - 001 : 0.415V - 010 : 0.385V - 011 : 0.370V - 100 : 0.430V - 101 : 0.445V - 110 : 0.460V - 111 : 0.475V When LDO_VREF_CGM_EN = 1 - 000 : 0.400V - 001 : 0.415V - 010 : 0.385V - 011 : 0.370V - 100 : 0.430V - 101 : 0.430V - 110 : 0.430V - 111 : 0.430V Note: LDO_VREF_CGM_EN and LDO_VREF_DIV_EN both cannot be 1. Setting both to 1 will disable both CGM_EN and DIV_EN Normal operational mode setting is 000 Power up value is 000
2	LDO_VREF_DIV_EN	To enable resistor divider as reference voltage Power up value is 0
1	LDO_VREF_CGM_EN	To enable Constant Gm as reference voltage Power up value is 0
0	LDO_MODE_EN	LDO Mode. DSIPHY Regulator Enable. - 1: DSIPHY Regulator is enabled. - 0: DSIPHY Regulator is disabled. Normal operational mode setting is 0. DSIPHY_REGULATOR_CTRL_0[DSIPHY_REG_EN] must be set to 0 when LDO_MODE_EN is set to 1 Power up value is 0

0x047004B4 MIPI_DSI_1_DSI1_DSIPHY_DEBUG_RESERVED0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_DEBUG_RESERVED0

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x047004B8 MIPI_DSI_1_DSI1_DSIPHY_DEBUG_RESERVED1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_DEBUG_RESERVED1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x047004BC MIPI_DSI_1_DSI1_DSIPHY_DEBUG_RESERVED2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_DEBUG_RESERVED2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x047004C0 MIPI_DSI_1_DSI1_DSIPHY_GLBL_STATUS_DEBUG_BUS0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_GLBL_STATUS_DEBUG_BUS0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DEBUG_BUS_7_0	

0x047004C4 MIPI_DSI_1_DSI1_DSIPHY_GLBL_STATUS_DEBUG_BUS1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_GLBL_STATUS_DEBUG_BUS1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DEBUG_BUS_15_8	

0x047004C8 MIPI_DSI_1_DSI1_DSIPHY_GLBL_STATUS_DEBUG_BUS2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_GLBL_STATUS_DEBUG_BUS2

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DEBUG_BUS_23_16	

0x047004CC MIPI_DSI_1_DSI1_DSIPHY_GLBL_STATUS_DEBUG_BUS3

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_GLBL_STATUS_DEBUG_BUS3

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DEBUG_BUS_31_24	

0x04700500 MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CTRL_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CTRL_0

Bits	Name	Description
31:4	RESERVED_BITS31_4	
3:1	DSIPHY_REG_REF_SEL	DSIPHY Regulator Reference Select. Selects the value of reference voltage for the DSIPHY DCDC Regulator. When DSIPHY_REGULATOR_TEST[DIV_EN] = 1 - 000 : 0.400V - 001 : 0.415V - 010 : 0.385V - 011 : 0.370V - 100 : 0.430V - 101 : 0.445V - 110 : 0.460V - 111 : 0.475V When DSIPHY_REGULATOR_TEST[NP_CGM_EN] = 1 - 000 : 0.400V - 001 : 0.415V - 010 : 0.385V - 011 : 0.370V - 100 : 0.430V - 101 : 0.430V - 110 : 0.430V - 111 : 0.430V Note: NP_CGM_EN and DIV_EN both cannot be 1. Setting both to 1 will disable both CGM_EN and DIV_EN Normal operational mode setting is 000 Power up value is 000
0	DSIPHY_REG_EN	DC DC Mode. DSIPHY Regulator Enable. - 1: DSIPHY Regulator is enabled. - 0: DSIPHY Regulator is disabled. Normal operational mode setting is 1 and DSIPHY_LDO_CNTRL[LDO_MODE_EN] must be set to 0 Power up value is 0

0x04700504 MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CTRL_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000000A

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CTRL_1

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CTRL_1 (cont.)

Bits	Name	Description
7:0	DSIPHY_REG_CONTMODE0_CYCLES	DSIPHY Continuous Mode Cycle Control. Used to control the number of cycles of continue mode 1. Normal operational mode setting is 0000_1010 Power up value is 0000_1010

0x04700508 MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CTRL_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000004

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CTRL_2

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_REG_CONTMODEI_CYCLES	DSIPHY Continuous Mode I Cycle Control. Used to control the number of cycles of continuous mode 1 and 2. Normal operational mode setting is 0000_0100 Power up value is 0000_0100

0x0470050C MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CTRL_3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CTRL_3

Bits	Name	Description
31:4	RESERVED_BITS31_4	
3:0	DSIPHY_REG_CLK_DIV_RATIO	DSIPHY REFCLK CLOCK DIVIDER Selection Bits. 0000 : div by1 - 0001 : div by2 - 0010 : div by3 . . . 1111--- div by16 Power up value is 0000

0x04700510 MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CTRL_4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CTRL_4

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5	DIV_EN	To enable resistor divider as reference voltage Power up value is 0
4	NP_CGM_ENABLE	To enable constant Gm as reference voltage Power up value is 0
3:0	RESERVED_BITS3_0	

0x04700514 MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_TEST

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_TEST

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	DSIPHY_REG_TEST_EN	Amux select bit.0: HIGH Z 1:Send comparator inputs to MIPI_DSI_LDO pin Normal operational mode setting is 0 Power up value is 0
6:1	RESERVED_BITS6_1	
0	DSIPHY_REG_TEST_SEL	Selects which input of the comparator probe. -0: Reference Voltage(negative input comparator) -1: Positive input of comparator Normal operational mode setting is 0 Power up value is 0

0x04700518 MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CAL_PWR_CFG

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CAL_PWR_CFG

Bits	Name	Description
31:5	RESERVED_BITS31_5	

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CAL_PWR_CFG (cont.)

Bits	Name	Description
4	SW_RESET	RESET for Digital blocks except control registers. Active high signal. - 1: Assertion - 0: De-assertion Normal operational mode setting is 0. Power up value is 0
3:2	RESERVED_BITS3_2	
1	DSIPHY_CAL_PWRDN_B	Digital Control block Power Down. - 1: Normal calibration operation - 0: Digital Control block powerdown Normal operational mode setting is 1 Power up value is 0
0	DSIPHY_REG_PWRDN_B	DSIPHY Regulator NPL Power Down. -1: Normal operation.Note: After the Regulator power down bit be set from ’1’ to ’0’ (powerup), regulator takes minimum 250uS worst case to charge up the external capacitor for MIPI DC/DC converter. -0: Regulator NPL Block powerdown Normal operational mode setting is 1 Power up value is 0

0x0470051C MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CAL_TEST

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CAL_TEST

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	CAL_COMP_TEST_SEL	Field is Reserved and not being used.

0x04700520 MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CAL_TPA

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CAL_TPA

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CAL_TPA (cont.)

Bits	Name	Description
7:4	DIGITAL_TESTMUX_SEL	Normal operational mode setting is 0000 Power up value is 0000 0x0: DCDC mode Comparator output to MIPI_DSI_D*N 0x1: Output of PWM programmable Clock divider 0x2: Not used
3:0	ANALOG_TESTMUX_SEL	Normal operational mode setting is 0000 Power up value is 0000 0x0: ATEST mux outputs HiZ 0x2: DCDC mode Comparator inputs to MIPI_DSI_LDO 0x3: PLL Bias Current to MIPI_DSI_LDO

0x04700524 MIPI_DSI_1_DSI1_DSIPHY_REG_CAL_DBG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_REG_CAL_DBG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	CAL_DEBUG_SEL	Refer to table at the end of the REG SWI section to see detailed description of digital top debug bus selections. Normal operational mode setting is 0000 Power up value is 0000
3:0	REG_DEBUG_SEL	Refer to table at the end of the REG SWI section to see detailed description of digital top debug bus selections. Normal operational mode setting is 00 Power up value is 00

0x04700528 MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_TRIGGER

Bits	Name	Description
31:1	RESERVED_BITS31_1	

MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_TRIGGER (cont.)

Bits	Name	Description
0	TRIGGER	Trigger the hw calibration of the pull-up and pull-down strength for the High-speed transmitters. Normal operational mode setting is 0 Power up value is 0

0x0470052C MIPI_DSI_1_DSI1_DSIPHY_CAL_SW_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_CAL_SW_CFG0

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	SW_CAL_TX_BOT_EN	High speed transmitter pull-down strength calibration enable. Normal operational mode setting is 0 Power up value is 0
3:1	RESERVED_BITS3_1	
0	SW_CAL_TX_TOP_EN	High speed transmitter pull-up strength calibration enable. Normal operational mode setting is 0 Power up value is 0

0x04700530 MIPI_DSI_1_DSI1_DSIPHY_CAL_SW_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_CAL_SW_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	SW_CAL_TX_BOT_STR	High speed transmitter pull-down strength setting. - 1111=Strongest - 0000=Weakest strength. Normal operational mode setting is 0000 Power up value is 0000

MIPI_DSI_1_DSI1_DSIPHY_CAL_SW_CFG1 (cont.)

Bits	Name	Description
3:0	SW_CAL_TX_TOP_STR	High speed transmitter pull-up strength setting. - 1111=Strongest - 0000=Weakest strength. Normal operational mode setting is 0000 Power up value is 0000

0x04700534 MIPI_DSI_1_DSI1_DSIPHY_CAL_SW_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_CAL_SW_CFG2

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	CALIBRATION_SEL	Select calibration mode - 0:hardware control - 1: software control Normal operational mode setting is 0 Power up value is 0

0x04700538 MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000001

MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_CFG0

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	CAL_POLYR_MODE	DSIPHY Poly Resistor Select. To enable the Poly Resistor to be used for impedance calibration. When asserted, the MIPI_DSI_LDO pin will be connected to the reference poly resistor. Note: DSIPHY_REGULATOR_CTRL_0[DSIPH_REG_EN] must be set to 0 before asserting CAL_POLYR_MODE Normal operational mode setting is 0 Power up value is 0
3:1	RESERVED_BITS3_1	

MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_CFG0 (cont.)

Bits	Name	Description
0	HW_CAL_EN	To enable the hardware calibration Normal operational mode setting is 1 Power up value is 1

0x0470053C MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000005A

MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	LOWER_THRESHOLD	If number of 1s out of samples of CAL_WEAK (Comparator output signal) is below this value, strength will be incremented Normal operational mode setting is 0101 Power up value is 0101
3:0	UPPER_THRESHOLD	If number of 1s out of samples of CAL_WEAK (Comparator output signal) is above this value, strength will be incremented Normal operational mode setting is 1010 Power up value is 1010

0x04700540 MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000010

MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_CFG2

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4:0	PC_STR_TOO_WEAK_COUNT	Number of samples of CAL_WEAK (Comparator output signal) to take for each loop. This is used for counting the samples of analog calibrator compactor output str_too_weak signal. The sample counter are based on dsi pll refclk cycle. This register value must be set greater than UPPER_THRESHOLD in order to have correct HW calibration sequence. Normal operational mode setting is 1_0000 Power up value is 1_0000

0x04700544 MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_CFG3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000000A

MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_CFG3

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	COMPARATOR_SETTLE_TIME_7_0	Number of ESCCLK cycles to wait before taking another set of 16 samples of CAL_WEAK (Comparator output signal) Normal operational mode setting is 0000_1010 Power up value is 0000_1010

0x04700548 MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_CFG4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_CAL_HW_CFG4

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	COMPARATOR_SETTLE_TIME_9_8	Number of ESCCLK cycles to wait before taking another set of 16 samples of CAL_WEAK (Comparator output signal) Normal operational mode setting is 00 Power up value is 00

0x0470054C MIPI_DSI_1_DSI1_DSIPHY_CAL_TEST_EFUSE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_CAL_TEST_EFUSE

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_EFUSE_OVERRIDE_VALUE	DSIPHY EFUSE Override Value Normal operational mode setting is 0000 Power up value is 0000

MIPI_DSI_1_DSI1_DSIPHY_CAL_TEST_EFUSE (cont.)

Bits	Name	Description
3:2	RESERVED_BITS3_2	
1:0	DSIPHY_EFUSE_OVERRIDE	- 00: no override; - 01: DSIPHY_EFUSE_OVERRIDE_VALUE over write efuse; - 1x: DSIPHY_EFUSE_OVERRIDE_VALUE over write efuse mapping value to reference impedance. Normal operational mode setting is 00 Power up value is 00

0x04700550 MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CAL_STATUS0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CAL_STATUS0

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	HW_CALIBRATOR_BUSY	READ ONLY. To monitor hardware calibration status -1: Calibration in progress -0: Calibration complete
3:1	RESERVED_BITS3_1	
0	PC_STR_TOO_WEAK	READ ONLY. To monitor CAL_WEAK (Comparator output signal)

0x04700554 MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CAL_STATUS1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_REGULATOR_CAL_STATUS1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	HW_CAL_BOT_STR	READ ONLY. Bottom calibrated impedance strength value. Stable after calibration is complete
3:0	HW_CAL_TOP_STR	READ ONLY. Top calibrated impedance strength value. Stable after calibration is complete

0x04700558 MIPI_DSI_1_DSI1_DSIPHY_REG_CAL_DBG_STAT0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_REG_CAL_DBG_STAT0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DEBUG_BUS_7_0	READ ONLY. Refer to descriptive debug bus table below

0x0470055C MIPI_DSI_1_DSI1_DSIPHY_REG_CAL_DBG_STAT1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_1_DSI1_DSIPHY_REG_CAL_DBG_STAT1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DEBUG_BUS_15_8	READ ONLY. Refer to descriptive debug bus table below

14.8 MIPI DSI2 Registers (0x05800000 MIPI_DSI_2_BASE)

This section contains the MIPI DSI2 registers.

0x05800000 MIPI_DSI_2_DSI2_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Control Register provides general control to the protocol, lane management and PHY layers.

MIPI_DSI_2_DSI2_CTRL

Bits	Name	Description
31	RESERVED_1	
30	NEW_INTERLEAVE_MODE_EN	unused (Enable new interleave mode with H/W arbitration between long commands and BLLP periods.) 0x0: disable 0x1: enable
29:28	PACKET_BYTE_MSB_LSB_FLIP	Swap the bit ordering of each byte of a packet 0x0: no swap (bit 0 is lsb, bit 7 is msb) 0x1: swap each byte of payload (bit 0 is msb, bit 7 is lsb) 0x2: swap each byte of packet (bit 0 is msb, bit 7 is lsb) 0x3: reserved
27	RESERVED_2	
26	DEBUG_MODE_EN	Enable debug mode for supporting non-compliant panels 0x0: disable 0x1: enable
25	RESERVED_3	
24	CRC_CHK_EN	Enable CRC verification of the received packets 0x0: Disable 0x1: Enable
23:21	RESERVED_4	
20	ECC_CHK_EN	Enable ECC verification of the received packets 0x0: Disable 0x1: Enable
19:9	RESERVED_5	
8	CLKLN_EN	Enable clock lane of the PHY 0x0: Disable DSI PHY Clock Lane 0x1: Enable DSI PHY Clock Lane

MIPI_DSI_2_DSI2_CTRL (cont.)

Bits	Name	Description
7	DLN3_EN	Enable data lane 3 of the PHY 0x0: Disable DSI PHY Data Lane 3 0x1: Enable DSI PHY Data Lane 3
6	DLN2_EN	Enable data lane 2 of the PHY 0x0: Disable DSI PHY Data Lane 2 0x1: Enable DSI PHY Data Lane 2
5	DLN1_EN	Enable data lane 1 of the PHY 0x0: Disable DSI PHY Data Lane 1 0x1: Enable DSI PHY Data Lane 1
4	DLN0_EN	Enable data lane 0 of the PHY 0x0: Disable DSI PHY Data Lane 0 0x1: Enable DSI PHY Data Lane 0
3	RESERVED_6	
2	CMD_MODE_EN	Enable the Command Mode Engine. 0x0: Disable DSI Command Mode Engine 0x1: Enable DSI Command Mode Engine
1	VIDEO_MODE_EN	Enable the Video Mode Engine. 0x0: Disable DSI Video Mode Engine 0x1: Enable DSI Video Mode Engine
0	DSI_EN	Enable the DSI controller. 0x0: Disable DSI Controller 0x1: Enable DSI controller

0x05800004 MIPI_DSI_2_DSI2_STATUS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Status Register provides status of the DSI controller

MIPI_DSI_2_DSI2_STATUS

Bits	Name	Description
31	INTERLEAVE_OP_CONTENTION_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
31	INTERLEAVE_OP_CONTENTION	READ ONLY. The controller generates command mode packets and video mode packets at the same time (i.e.: the command mode packets are longer than one BLLP period)
30:7	RESERVED	

MIPI_DSI_2_DSI2_STATUS (cont.)

Bits	Name	Description
6	PHY_RESET_BUSY	READ ONLY. DSI interface is busy sending the panel reset through the link
5	GENERIC_TRIGGER_BUSY	READ ONLY. DSI interface is busy sending the generic trigger through the link
4	BTA_BUSY	READ ONLY. DSI interface is busy waiting for read response, acknowledge or tearing effect signal from the peripheral
3	VIDEO_MODE_ENGINE_BUSY	READ ONLY. Video Mode Engine is busy sending data from display engine
2	CMD_MODE_MDP_BUSY	READ ONLY. Command Mode Engine is busy sending data from display engine
1	CMD_MODE_DMA_BUSY	READ ONLY. Command Mode Engine is busy sending data from memory or reading data from the display panel
0	CMD_MODE_ENGINE_BUSY	READ ONLY. Command Mode Engine Busy

0x05800008 MIPI_DSI_2_DSI2_FIFO_STATUS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x11111000

Status of FIFOs in the DSI controller

MIPI_DSI_2_DSI2_FIFO_STATUS

Bits	Name	Description
31	RESERVED_1	
30	DLN3_HS_FIFO_OVERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
30	DLN3_HS_FIFO_OVERFLOW	READ ONLY. The FIFO of Lane 3 overflows
29	DLN3_HS_FIFO_FULL	READ ONLY. The FIFO of Lane 3 is full
28	DLN3_HS_FIFO_EMPTY	READ ONLY. The FIFO of Lane 3 is empty
27	RESERVED_2	
26	DLN2_HS_FIFO_OVERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
26	DLN2_HS_FIFO_OVERFLOW	READ ONLY. The FIFO for HS data on Lane 2 overflows
25	DLN2_HS_FIFO_FULL	READ ONLY. The FIFO for HS data on Lane 2 is full

MIPI_DSI_2_DSI2_FIFO_STATUS (cont.)

Bits	Name	Description
24	DLN2_HS_FIFO_EMPTY	READ ONLY. The FIFO for HS data on Lane 2 is empty
23	RESERVED_3	
22	DLN1_HS_FIFO_OVERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
22	DLN1_HS_FIFO_OVERFLOW	READ ONLY. The FIFO of Lane 1 overflows
21	DLN1_HS_FIFO_FULL	READ ONLY. The FIFO of Lane 1 is full
20	DLN1_HS_FIFO_EMPTY	READ ONLY. The FIFO of Lane 1 is empty
19	RESERVED_4	
18	DLN0_HS_FIFO_OVERFLOW	READ ONLY. The FIFO for HS data on Lane 0 overflows
18	DLN0_HS_FIFO_OVERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
17	DLN0_HS_FIFO_FULL	READ ONLY. The FIFO for HS data on Lane 0 is full
16	DLN0_HS_FIFO_EMPTY	READ ONLY. The FIFO for HS data on Lane 0 is empty
15	RESERVED_5	
14	DLN0_LP_FIFO_OVERFLOW_CLR	WRITE ONLY. unused
14	DLN0_LP_FIFO_OVERFLOW	READ ONLY. unused
13	DLN0_LP_FIFO_FULL	READ ONLY. The FIFO for LP data on Lane 0 is full
12	DLN0_LP_FIFO_EMPTY	READ ONLY. The FIFO for LP data on Lane 0 is empty
11	RESERVED_6	
10	CMD_DMA_FIFO_UNDERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
10	CMD_DMA_FIFO_UNDERFLOW	READ ONLY. The Command mode engine dmafifo underflows
9	CMD_DMA_FIFO_WR_WATERMARK_REACH_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
9	CMD_DMA_FIFO_WR_WATERMARK_REACH	READ ONLY. The Command mode engine dmafifo write watermark is reached
8	CMD_DMA_FIFO_RD_WATERMARK_REACH_CLR	WRITE ONLY. writing a 1 to this field will clear this bit
8	CMD_DMA_FIFO_RD_WATERMARK_REACH	READ ONLY. The Command mode engine dmafifo read watermark is reached
7	CMD_MDP_FIFO_UNDERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear the underflow bit

MIPI_DSI_2_DSI2_FIFO_STATUS (cont.)

Bits	Name	Description
7	CMD_MDP_FIFO_UNDERFLOW	READ ONLY. Command mode engine MDP fifo underflows
6:4	RESERVED_7	
3	VIDEO_MDP_FIFO_UNDERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear the underflow bit
3	VIDEO_MDP_FIFO_UNDERFLOW	READ ONLY. Video fifo underflows
2:1	RESERVED_8	
0	VIDEO_MDP_FIFO_OVERFLOW_CLR	WRITE ONLY. writing a 1 to this field will clear the overflow bit
0	VIDEO_MDP_FIFO_OVERFLOW	READ ONLY. Video mode engine fifo overflows

0x0580000C MIPI_DSI_2_DSI2_VIDEO_MODE_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00008000

DSI Video Mode Engine Control Register

MIPI_DSI_2_DSI2_VIDEO_MODE_CTRL

Bits	Name	Description
31:29	RESERVED_1	
28	PULSE_MODE_OPT	Select pulse mode option 0x0: no HSA and HE following VS/VE packet 0x1: send HSA and HE following VS/VE packet
27:25	RESERVED_2	
24	HFP_PWR_MODE	Select power mode during the HFP period 0x0: send blanking packets in High Speed mode 0x1: low power stop mode (LP-11)
23:21	RESERVED_3	
20	HBP_PWR_MODE	Select power mode during the HBP period 0x0: send blanking packets in High Speed mode 0x1: low power stop mode (LP-11)
19:17	RESERVED_4	

MIPI_DSI_2_DSI2_VIDEO_MODE_CTRL (cont.)

Bits	Name	Description
16	HSA_PWR_MODE	Select power mode during the HSA period 0x0: send blanking packets in High Speed mode 0x1: low power stop mode (LP-11)
15	EOF_BLLP_PWR_MODE	Select power mode for the BLLP of the last line of a frame 0x0: send blanking packets during BLLP in high speed mode and block Command Mode packets 0x1: low power stop mode (LP-11 or let Command Mode Engine send packets in HS or LP mode)
14:13	RESERVED_5	
12	BLLP_PWR_MODE	DSI Power Mode for packets sent during BLLP period 0x0: send blanking packets during BLLP in high speed mode and block Command Mode packets 0x1: low power stop mode (LP-11 or let Command Mode Engine send packets in HS or LP mode)
11:10	RESERVED_6	
9:8	TRAFFIC_MODE	DSI video mode traffic sequence 0x0: non-burst mode with sync pulses 0x1: non-burst mode with sync start events 0x2: burst mode 0x3: reserved
7:6	RESERVED_7	
5:4	DST_FORMAT	Pixel format. If there is interleaved Command Mode pixel packets (generated from MDP), the pixel depth of the Command Mode pixel packet should be greater or equal to the pixel depth of the Video mode pixel packet. 0x0: RGB565 0x1: RGB666_1 (packed) 0x2: RGB666_2 (loosely packed) 0x3: RGB888
3:2	RESERVED_8	
1:0	VC	Virtual channel identifier

0x05800010 MIPI_DSI_2_DSI2_VIDEO_MODE_SYNC_DATATYPE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x31211101

DSI Video Mode Sync Datatype Register

MIPI_DSI_2_DSI2_VIDEO_MODE_SYNC_DATATYPE

Bits	Name	Description
31:30	RESERVED_1	
29:24	HE	Specify the datatype of a hsync end packet
23:22	RESERVED_2	
21:16	HS	Specify the datatype of a hsync start packet
15:14	RESERVED_3	
13:8	VE	Specify the datatype of a vsync end packet
7:6	RESERVED_4	
5:0	VS	Specify the datatype of a vsync start packet

0x05800014 MIPI_DSI_2_DSI2_VIDEO_MODE_PIXEL_DATATYPE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x3E2E1E0E

DSI Video Mode Pixel Datatype Register

MIPI_DSI_2_DSI2_VIDEO_MODE_PIXEL_DATATYPE

Bits	Name	Description
31:30	RESERVED_1	
29:24	RGB888	Specify the datatype of an RGB888 pixel stream packet
23:22	RESERVED_2	
21:16	RGB666	Specify the datatype of a loosely-packed RGB666 pixel stream packet
15:14	RESERVED_3	
13:8	RGB666_PACKED	Specify the datatype of a packed RGB666 pixel stream packet
7:6	RESERVED_4	
5:0	RGB565	Specify the datatype of an RGB565 pixel stream packet

0x05800018 MIPI_DSI_2_DSI2_VIDEO_MODE_BLANKING_DATATYPE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00001900

DSI Video Mode Blanking Packet Datatype Register

MIPI_DSI_2_DSI2_VIDEO_MODE_BLANKING_DATATYPE

Bits	Name	Description
31:14	RESERVED	
13:8	BLANK_PKT_DATATYPE	Specify the datatype of a blanking packet
7:0	BLANK_PKT_DATA	This byte will be repeated in the payload portion of the blanking packet

0x0580001C MIPI_DSI_2_DSI2_VIDEO_MODE_DATA_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Video Mode Data Control Register

MIPI_DSI_2_DSI2_VIDEO_MODE_DATA_CTRL

Bits	Name	Description
31:15	RESERVED_1	
14:12	RGB_SWAP	Swaps the R, G, and B channels of the dst pixels. This field should be used when different R,G, and B orderings are required. For example, if RGB_SWAP = 1 , RGB565 will become RBG556. 0x0: RGB 0x1: RBG 0x2: BGR 0x3: BRG 0x4: GRB 0x5: GBR 0x6: reserved_1 0x7: reserved_2
11:9	RESERVED_2	
8	B_SEL	Bit Swaps the B Channel of the dst pixel. This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
7:5	RESERVED_3	

MIPI_DSI_2_DSI2_VIDEO_MODE_DATA_CTRL (cont.)

Bits	Name	Description
4	G_SEL	Bit Swaps the G Channel of the dst pixel. This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
3:1	RESERVED_4	
0	R_SEL	Bit Swaps the R Channel of the dst pixel. This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap

0x05800020 MIPI_DSI_2_DSI2_VIDEO_MODE_ACTIVE_H

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Active Horizontal Display Region register.

The Active_H_Disp register defines the horizontal characteristics of the active window. (NOTE: video mode parameters are 0-based.)

MIPI_DSI_2_DSI2_VIDEO_MODE_ACTIVE_H

Bits	Name	Description
31:28	RESERVED_1	
27:16	ACTIVE_H_END	ACTIVE_H_END field tells the video mode engine where the horizontal viewing area ends (minus one) in pixel clock cycle relative to the horizontal sync signal.
15:12	RESERVED_2	
11:0	ACTIVE_H_START	ACTIVE_H_START field tells the video mode engine where the horizontal viewing area starts (minus one) in pixel clock cycle relative to the horizontal sync signal.

0x05800024 MIPI_DSI_2_DSI2_VIDEO_MODE_ACTIVE_V

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

CRTC Active Vertical Display Region register.

The Active_V_Disp register defines the vertical characteristics of the active window. (NOTE: video mode parameters are 0-based.)

MIPI_DSI_2_DSI2_VIDEO_MODE_ACTIVE_V

Bits	Name	Description
31:28	RESERVED_1	
27:16	ACTIVE_V_END	ACTIVE_V_END field tells the video mode engine where the horizontal viewing area ends (minus one) in lines relative to the vertical sync signal
15:12	RESERVED_2	
11:0	ACTIVE_V_START	ACTIVE_V_START field tells the video mode engine where the vertical viewing area starts (minus one) in lines relative to the vertical sync signal

0x05800028 MIPI_DSI_2_DSI2_VIDEO_MODE_TOTAL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Total Scan Area register.

TOTAL register defines the size of the total possible scanning area (NOTE: video mode parameters are 0-based.)

MIPI_DSI_2_DSI2_VIDEO_MODE_TOTAL

Bits	Name	Description
31:28	RESERVED_1	
27:16	VIDEO_V_TOTAL	Number of lines in one frame minus one. This value is equivalent to the period of the vertical sync
15:12	RESERVED_2	
11:0	VIDEO_H_TOTAL	Number of pixels in one scan line (horizontal line) of the LCD controller minus one. This value is equivalent to the period of the horizontal sync signal (in pixel clock cycles).

0x0580002C MIPI_DSI_2_DSI2_VIDEO_MODE_HSYNC

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HSync Control register which controls the horizontal screen position at which a horizontal sync packet is sent by the DSI controller to the panel. (NOTE: video mode parameters are 0-based.)

MIPI_DSI_2_DSI2_VIDEO_MODE_HSYNC

Bits	Name	Description
31:28	RESERVED_1	
27:16	HS_END	The position (minus one) where the horizontal sync ends in one line.
15:12	RESERVED_2	
11:0	HS_START	The position (minus one) where the horizontal sync starts in one line.

0x05800030 MIPI_DSI_2_DSI2_VIDEO_MODE_VSYNC

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

VSync Control register which controls the horizontal screen position at which a vertical sync packet is sent by the DSI controller to the panel. (NOTE: video mode parameters are 0-based.)

MIPI_DSI_2_DSI2_VIDEO_MODE_VSYNC

Bits	Name	Description
31:28	RESERVED_1	
27:16	VS_END	The position (minus one) where the vertical sync ends in one line.
15:12	RESERVED_2	
11:0	VS_START	The position (minus one) where the vertical sync starts in one line.

0x05800034 MIPI_DSI_2_DSI2_VIDEO_MODE_VSYNC_VPOS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

VSync Control register which controls the vertical screen position at which a vertical sync packet is sent by the DSI controller to the panel. (NOTE: video mode parameters are 0-based.)

MIPI_DSI_2_DSI2_VIDEO_MODE_VSYNC_VPOS

Bits	Name	Description
31:28	RESERVED_1	

MIPI_DSI_2_DSI2_VIDEO_MODE_VSYNC_VPOS (cont.)

Bits	Name	Description
27:16	VS_VPOS_END	The line (minus one) where the vertical sync ends in one frame.
15:12	RESERVED_2	
11:0	VS_VPOS_START	The line (minus one) where the vertical sync starts in one frame.

0x05800038 MIPI_DSI_2_DSI2_COMMAND_MODE_DMA_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Command Mode Control Register for DMA data control

MIPI_DSI_2_DSI2_COMMAND_MODE_DMA_CTRL

Bits	Name	Description
31	BROADCAST_EN	Enable the DSI core to send packets from DMA at the same time with the other core (this bit has to be set for the other DSI core as well). If broadcast is enable, the core needs to wait until both cores have fetched entire command buffer before start sending dma packets. When this bit is set, the command buffer size (DSI_DMA_CMD_LENGTH) must be less than 0x200 bytes. 0x0: disable 0x1: enable
30	BROADCAST_MASTER	Indicate whether this core is the master or slave 0x0: this core is the slave 0x1: this core is the master
29	RESERVED_1	
28	EMBEDDED_MODE	Select packet_type, BTA settings and packet header information 0x0: from the register 0x1: from the frame buffer
27	RESERVED_2	
26	POWER_MODE	Select power mode for data transmission of both embedded and non-embedded commands 0x0: high speed mode 0x1: low power mode
25	RESERVED	
24	PACKET_TYPE	Select packet type for non-embedded commands 0x0: short packet 0x1: long packet
23:22	VC	Virtual channel identifier for pixel data or non-embedded commands

MIPI_DSI_2_DSI2_COMMAND_MODE_DMA_CTRL (cont.)

Bits	Name	Description
21:16	DT	Data type for pixel data or non-embedded commands
15:0	WC	Exact number of bytes in one packet for pixel data or non-embedded commands

0x0580003C MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x06100006

DSI Command Mode Control Register for MDP data control

MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_CTRL

Bits	Name	Description
31	LINE_SPLIT	Break a line into small packets 0x0: no split 0x1: split
30:28	RGB_SWAP1	Swaps the R, G, and B channels of the dst pixels for stream 1 (if STREAM1_DST_FORMAT_SEL = 1, otherwise rgb swap for stream1 is defined by RGB_SWAP). This field should be used when different R,G, and B orderings are required. For example, if RGB_SWAP = 1 , RGB565 will become RBG556. 0x0: RGB 0x1: RBG 0x2: BGR 0x3: BRG 0x4: GRB 0x5: GBR 0x6: reserved_1 0x7: reserved_2
27:24	DST_FORMAT1	Pixel format for stream 1 (if STREAM1_DST_FORMAT_SEL = 1, otherwise pixel format for stream1 is defined by DST_FORMAT) - 0 = RGB111 - 1 = reserved - 2 = reserved - 3 = RGB332 (data_src_width must be in multiple of 2 pixels) - 4 = RGB444 (data_src_width must be in multiple of 2 pixels) - 5 = reserved - 6 = RGB565 - 7 = RGB666 - 8 = RGB888 others = reserved

MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_CTRL (cont.)

Bits	Name	Description
23:20	INTERLEAVE_MAX	Maximum number of Command Mode RGB packets to send within one horizontal blanking period of the Video Mode frame (sw must ensure that they can fit in one BLLP period)
19	RESERVED_1	
18:16	RGB_SWAP	Swaps the R, G, and B channels of the dst pixels. This field should be used when different R,G, and B orderings are required. For example, if RGB_SWAP = 1, RGB565 will become RBG556. 0x0: RGB 0x1: RBG 0x2: BGR 0x3: BRG 0x4: GRB 0x5: GBR 0x6: reserved_1 0x7: reserved_2
15	STREAM1_DST_FORMAT_SEL	Pixel format selection for stream 1. If MDP sends two streams to DSI and these streams have different output formats, then the pixel clock must be set according to the smallest pixel depth between the two. Otherwise, underflow may occur. Ex.: If stream0 is in RGB888 and stream1 is in RGB565, then pixel clock must be greater than dsiclk/2. 0x0: DST_FORMAT (same as stream0) 0x1: DST_FORMAT1
14	RESERVED_2	
13	B_SEL1	Bit Swaps the B Channel of the dst pixel for stream 1 (if STREAM1_DST_FORMAT_SEL = 1, otherwise bit swap for stream1 is defined by B_SEL). This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
12	B_SEL	Bit Swaps the B Channel of the dst pixel. This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
11:10	RESERVED	

MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_CTRL (cont.)

Bits	Name	Description
9	G_SEL1	Bit Swaps the G Channel of the dst pixel for stream 1 (if STREAM1_DST_FORMAT_SEL = 1, otherwise bit swap for stream1 is defined by G_SEL). This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
8	G_SEL	Bit Swaps the G Channel of the dst pixel. This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
7	BYTE_MSB_LSB_FLIP1	Swap the bit ordering of each byte of the dst pixel for stream 1 (if STREAM1_DST_FORMAT_SEL = 1, otherwise the byte endian is defined by BYTE_MSB_LSB_FLIP). 0x0: bit 0 is lsb, bit 7 is msb 0x1: bit 0 is msb, bit 0 is lsb
6	BYTE_MSB_LSB_FLIP	Swap the bit ordering of each byte of the dst pixel (this is done after the RGB swap and R/G/B_SEL). 0x0: bit 0 is lsb, bit 7 is msb 0x1: bit 0 is msb, bit 0 is lsb
5	R_SEL1	Bit Swaps the R Channel of the dst pixel for stream 1 (if STREAM1_DST_FORMAT_SEL = 1, otherwise bit swap for stream1 is defined by R_SEL). This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap
4	R_SEL	Bit Swaps the R Channel of the dst pixel. This field is used to reverse the ordering of the bits that is output for the color red. For example, for RGB888 color format, if the red component is 10000000 then if this field is enabled, 00000001 is output. 0x0: no swap 0x1: swap

MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_CTRL (cont.)

Bits	Name	Description
3:0	DST_FORMAT	Destination pixel format. For video mode operation interleave with MDP pixel packets, this is required: command mode pixel depth >= video mode pixel depth (check video mode pixel format in DSI_VIDEO_MODE_PIXEL_DATATYPE) - 0 = RGB111 - 1 = reserved - 2 = reserved - 3 = RGB332 (data_src_width must be in multiple of 2 pixels) - 4 = RGB444 (data_src_width must be in multiple of 2 pixels) - 5 = reserved - 6 = RGB565 - 7 = RGB666 - 8 = RGB888 others = reserved

0x05800040 MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_DCS_CMD_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00003C2C

This register controls DCS command insertion to MDP data

MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_DCS_CMD_CTRL

Bits	Name	Description
31:18	RESERVED	
17	INSERT_DCS_COMMAND2	Indicate whether a DCS command has to be inserted as the first byte of the payload of the pixel data packet of the stream NOT selected by COMMAND_MODE_DMA_STREAM_SEL 0x0: no command is inserted 0x1: value in the DCS_COMMAND field will be inserted
16	INSERT_DCS_COMMAND	Indicate whether a DCS command has to be inserted as the first byte of payload of the pixel data packet 0x0: no command is inserted 0x1: value in the DCS_COMMAND field will be inserted
15:8	WR_MEM_CONTINUE	DCS command for write_memory_continue
7:0	WR_MEM_START	DCS command for write_memory_start

0x05800044 MIPI_DSI_2_DSI2_DMA_CMD_OFFSET

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Command Offset Register

MIPI_DSI_2_DSI2_DMA_CMD_OFFSET

Bits	Name	Description
31:0	CMD_OFFSET	Memory offset (in bytes) for DSI command, qword aligned, i.e.: bit 2:0 are tied to 0. This value has to be multiple of 8. NOTE: Bits 0:2 of this field are preset in the factory to 0. You cannot change the setting of bits 0:2.

0x05800048 MIPI_DSI_2_DSI2_DMA_CMD_LENGTH

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Command Length Register

MIPI_DSI_2_DSI2_DMA_CMD_LENGTH

Bits	Name	Description
31:24	RESERVED	
23:0	CMD_LENGTH	Number of commands (in bytes). This value has to be multiple of 4.

0x0580004C MIPI_DSI_2_DSI2_DMA_FIFO_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI DMA FIFO Control Register

MIPI_DSI_2_DSI2_DMA_FIFO_CTRL

Bits	Name	Description
31:6	RESERVED_1	

MIPI_DSI_2_DSI2_DMA_FIFO_CTRL (cont.)

Bits	Name	Description
5:4	READ_WATERMARK	Allow fifo reads for a packet when the number of unread entries is above this watermark or larger than the packet size (read_watermark has to be smaller than or equal to write_watermark) 0x0: FIFO is 1/2 full 0x1: FIFO is 3/4 full 0x2: FIFO is 7/8 full 0x3: FIFO is 15/16 full
3:2	RESERVED_2	
1:0	WRITE_WATERMARK	Fills FIFO under the following conditions 0x0: FIFO is 1/2 empty 0x1: FIFO is 1/4 empty 0x2: FIFO is 1/8 empty 0x3: FIFO is 1/16 empty

0x05800050 MIPI_DSI_2_DSI2_DMA_NULL_PACKET_DATA

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000900

DSI DMA Null Packet Data Register

MIPI_DSI_2_DSI2_DMA_NULL_PACKET_DATA

Bits	Name	Description
31:14	RESERVED	
13:8	NULL_DATATYPE	Datatype of null packet
7:0	NULL_DATA	This byte will be repeated in the payload portion of the embedded null packet

0x05800054 MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_STREAM0_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI MDP stream 0 control register

MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_STREAM0_CTRL

Bits	Name	Description
31:16	MDP0_WC	Exact number of Word (byte) count for one packet
15:10	RESERVED_1	
9:8	MDP0_VC	Virtual channel
7:6	RESERVED_2	
5:0	MDP0_DT	Packet data type

0x05800058 MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_STREAM0_TOTAL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI MDP stream 0 frame dimension (NOTE: unlike video mode parameters which are 0-based, these parameters in command mode are 1-based, i.e.: the actual number of pixels are set.)

MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_STREAM0_TOTAL

Bits	Name	Description
31:28	RESERVED_1	
27:16	MDP0_V_TOTAL	Number of lines in 1 frame
15:12	RESERVED_2	
11:0	MDP0_H_TOTAL	Number of pixels in 1 line

0x0580005C MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_STREAM1_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI MDP stream 1 control register

MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_STREAM1_CTRL

Bits	Name	Description
31:16	MDP1_WC	Exact number of word (byte) count for one packet
15:10	RESERVED_1	
9:8	MDP1_VC	Virtual channel

MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_STREAM1_CTRL (cont.)

Bits	Name	Description
7:6	RESERVED_2	
5:0	MDP1_DT	Packet data type

0x05800060 MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_STREAM1_TOTAL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI MDP stream 1frame dimension (NOTE: unlike video mode parameters which are 0-based, these parameters in command mode are 1-based, i.e.: the actual number of pixels are set.)

MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_STREAM1_TOTAL

Bits	Name	Description
31:28	RESERVED_1	
27:16	MDP1_V_TOTAL	Exact number of lines in 1 frame
15:12	RESERVED_2	
11:0	MDP1_H_TOTAL	Exact number of pixels in 1 line

0x05800064 MIPI_DSI_2_DSI2_ACK_ERR_STATUS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Error Report Register stores errors and acknowledge from the DSI display module.

This register stores errors from the error report packet and error in the ECC and CRC of the returned packet

MIPI_DSI_2_DSI2_ACK_ERR_STATUS

Bits	Name	Description
31:29	RESERVED_1	
28	ACK_CLR	WRITE ONLY. clear ACK by writing a ’1’ and then a ’0’ to this bit
28	ACK	READ ONLY. Transmission acknowledged by the DSI display module
27:25	RESERVED_2	

MIPI_DSI_2_DSI2_ACK_ERR_STATUS (cont.)

Bits	Name	Description
24	ERROR	READ ONLY. There is an error report returned from the DSI display module (or-ed error bits 0 - 15)
24	ERROR_CLR	WRITE ONLY. clear ERROR by writing a ’1’ and then a ’0’ to this bit
23	RDBK_INCOMPLETE_PACKET_ERR	READ ONLY. Received incomplete read packet
23	RDBK_INCOMPLETE_PACKET_ERR_CLR	WRITE ONLY. clear RDBK_INCOMPLETE_PACKET_ERR by writing a ’1’ and then a ’0’ to this bit
22:21	RESERVED_3	
20	RDBK_DATA_CRC_ERR_CLR	WRITE ONLY. clear RDBK_DATA_CRC_ERR by writing a ’1’ and then a ’0’ to this bit
20	RDBK_DATA_CRC_ERR	READ ONLY. Incorrect CRC detected in read packet
19:18	RESERVED_4	
17	RDBK_DATA_MULTI_ECC_ERR_CLR	WRITE ONLY. clear RDBK_DATA_MULTI_ECC_ERR by writing a ’1’ and then a ’0’ to this bit
17	RDBK_DATA_MULTI_ECC_ERR	READ ONLY. Multi-bit ECC detected in read packet and not corrected
16	RDBK_DATA_ECC_ERR_CLR	WRITE ONLY. clear RDBK_DATA_ECC_ERR by writing a ’1’ and then a ’0’ to this bit
16	RDBK_DATA_ECC_ERR	READ ONLY. Single bit ECC error detected in read packet and corrected by DSI controller
15	PANEL_SPECIFIC_ERR	READ ONLY. This bit correspond to bit 15 (DSI protocol violation) of the error report. Please refer to the meaning by this description rather than by the name of the register field
15	PANEL_SPECIFIC_ERR_CLR	WRITE ONLY. Clear PANEL_SPECIFIC_ERR by writing a ’1’ and then a ’0’ to this bit
14	RESERVED	
13	PROTOCOL_VIOLATION_CLR	WRITE ONLY. Clear Protocol violation by writing a ’1’ and then a ’0’ to this bit
13	PROTOCOL_VIOLATION	READ ONLY. This bit correspond to bit 13 (invalid transmission length) of the error report. Please refer to the meaning by this description rather than by the name of the register field.
12	VC_ERR_CLR	WRITE ONLY. clear VC_ERR by writing a ’1’ and then a ’0’ to this bit
12	VC_ERR	READ ONLY. Invalid virtual channel ID detected by the DSI display module
11	DT_ERR_CLR	WRITE ONLY. clear DT_ERR by writing a ’1’ and then a ’0’ to this bit
11	DT_ERR	READ ONLY. DSI data type not recognized by the DSI display module

MIPI_DSI_2_DSI2_ACK_ERR_STATUS (cont.)

Bits	Name	Description
10	CRC_ERR	READ ONLY. Checksum error for long packet detected by the DSI display module
10	CRC_ERR_CLR	WRITE ONLY. clear CRC_ERR by writing a ’1’ and then a ’0’ to this bit
9	MULTI_ECC_ERR_CLR	WRITE ONLY. clear MULTI_ECC_ERR by writing a ’1’ and then a ’0’ to this bit
9	MULTI_ECC_ERR	READ ONLY. Multi-bit ECC detected and not corrected by the DSI display module
8	ECC_ERR_CLR	WRITE ONLY. clear ECC_ERR by writing a ’1’ and then a ’0’ to this bit
8	ECC_ERR	READ ONLY. Single bit ECC detected and corrected by the DSI display module
7	CONTENTION	READ ONLY. Contention Detected by Peripheral
7	CONTENTION_CLR	WRITE ONLY. clear CONTENTION by writing a ’1’ and then a ’0’ to this bit
6	FALSE_CTRL_ERR_CLR	WRITE ONLY. clear FALSE_CTRL_ERR by writing a ’1’ and then a ’0’ to this bit
6	FALSE_CTRL_ERR	READ ONLY. False Control Error detected by the DSI display module
5	TIMEOUT_CLR	WRITE ONLY. clear TIMEOUT by writing a ’1’ and then a ’0’ to this bit
5	TIMEOUT	READ ONLY. timeout error (Low Power forward transmission, bus turn around, High Speed reverse transmission) detected by the DSI display module
4	LP_ERR	READ ONLY. Low-power transmit sync error detected by the DSI display module
4	LP_ERR_CLR	WRITE ONLY. clear LP_ERR by writing a ’1’ and then a ’0’ to this bit
3	ESC_ERR_CLR	WRITE ONLY. clear ESC_ERR by writing a ’1’ and then a ’0’ to this bit
3	ESC_ERR	READ ONLY. Escape Mode Entry Command Error detected by the DSI display module
2	EOT_ERR_CLR	WRITE ONLY. clear EOT_ERR by writing a ’1’ and then a ’0’ to this bit
2	EOT_ERR	READ ONLY. EoT Sync Error detected by the DSI display module
1	SOT_SYNC_ERR	READ ONLY. SoT Sync Error detected by the DSI display module
1	SOT_SYNC_ERR_CLR	WRITE ONLY. clear SOT_SYNC_ERR by writing a ’1’ and then a ’0’ to this bit
0	SOT_ERR_CLR	WRITE ONLY. clear SOT_ERR by writing a ’1’ and then a ’0’ to this bit

MIPI_DSI_2_DSI2_ACK_ERR_STATUS (cont.)

Bits	Name	Description
0	SOT_ERR	READ ONLY. SoT Error detected by the DSI display module

0x05800068 MIPI_DSI_2_DSI2_RDBK_DATA0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Read Data 0 Register

MIPI_DSI_2_DSI2_RDBK_DATA0

Bits	Name	Description
31:0	RD_DATA0	READ ONLY. Data returned from the DSI display module

0x0580006C MIPI_DSI_2_DSI2_RDBK_DATA1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Read Data 1 Register

MIPI_DSI_2_DSI2_RDBK_DATA1

Bits	Name	Description
31:0	RD_DATA1	READ ONLY. Data returned from the DSI display module

0x05800070 MIPI_DSI_2_DSI2_RDBK_DATA2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Read Data 2 Register

MIPI_DSI_2_DSI2_RDBK_DATA2

Bits	Name	Description
31:0	RD_DATA2	READ ONLY. Data returned from the DSI display module

0x05800074 MIPI_DSI_2_DSI2_RDBK_DATA3

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Read Data 3 Register

MIPI_DSI_2_DSI2_RDBK_DATA3

Bits	Name	Description
31:0	RD_DATA3	READ ONLY. Data returned from the DSI display module

0x05800078 MIPI_DSI_2_DSI2_RDBK_DATATYPE0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x22211211

DSI Read Response Datatype Register 0

MIPI_DSI_2_DSI2_RDBK_DATATYPE0

Bits	Name	Description
31:30	RESERVED_1	
29:24	DCS_SHORT_RD_2_BYTE	Specify the datatype of a DCS short read response with 2 byte returned
23:22	RESERVED_2	
21:16	DCS_SHORT_RD_1_BYTE	Specify the datatype of a DCS short read response with 1 byte returned
15:14	RESERVED_3	
13:8	GENERIC_SHORT_RD_2_BYTE	Specify the datatype of a generic short read response with 2 byte returned
7:6	RESERVED_4	
5:0	GENERIC_SHORT_RD_1_BYTE	Specify the datatype of a generic short read response with 1 byte returned

0x0580007C MIPI_DSI_2_DSI2_RDBK_DATATYPE1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x001C1A02

DSI Read Response Datatype Register 1

MIPI_DSI_2_DSI2_RDBK_DATATYPE1

Bits	Name	Description
31:22	RESERVED_1	
21:16	DCS_LONG_RD	Specify the datatype of a DCS long read response
15:14	RESERVED_2	
13:8	GENERIC_LONG_RD	Specify the datatype of a generic long read response
7:6	RESERVED	
5:0	ERROR_REPORT	Specify the datatype of an acknowledge with error report

0x05800080 MIPI_DSI_2_DSI2_TRIG_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Trigger Control Register

When DSI is enabled and CRTC1 or 2 is used for other non-DSI panels, the display engine path trigger must be set to manual internal, otherwise the CRTC will be stalled

MIPI_DSI_2_DSI2_TRIG_CTRL

Bits	Name	Description
31	TE_SEL	Select TE path 0x0: Tearing effect_1 (external trigger returns from data link) 0x1: Tearing effect_2 (external trigger returns from a dedicated pin)
30:29	RESERVED_1	
28	COMMAND_MODE_DMA_MDP_ORDER	This bit field indicates whether DMA or MDP path will win the arbitration if both requests the link at the same time 0x0: DMA has higher priority than display processor 0x1: Display processor has higher priority than DMA
27:25	RESERVED_2	
24	COMMAND_MODE_MDP_REQ_ORDER	If PHY TE is required for one of the MDP stream while the other stream is ready to transmit, this field determines which will win the arbitration 0x0: Command Mode MDP PHY TE request has higher priority than Command Mode MDP data transmission request 0x1: Command Mode MDP Data transmission request has higher priority than Command Mode MDP PHY TE request
23:9	RESERVED_3	

MIPI_DSI_2_DSI2_TRIG_CTRL (cont.)

Bits	Name	Description
8	COMMAND_MODE_DMA_STREAM_SEL	If COMMAND_MODE_DMA_TRIGGER_SEL = SOF/EOF or both COMMAND_MODE_DMA_TRIGGER_SEL and COMMAND_MODE_MDP_TRIGGER_SEL = TE or sw+TE, the Command Mode DMA path is triggered at frame boundary of the MDP stream selected by this bit 0x0: stream 0 0x1: stream 1
7	RESERVED_4	
6:4	COMMAND_MODE_MDP_TRIGGER_SEL	TRIGGER_SEL field is used to select which trigger is used for Command Mode display processor path. (The stream to be triggered is selected by COMMAND_MODE_DMA_STREAM_SEL) 0x0: none 0x1: reserved_1 0x2: TE 0x3: reserved_2 0x4: sw trigger 0x5: reserved_3 0x6: sw trigger and TE 0x7: reserved_4
3	RESERVED	
2:0	COMMAND_MODE_DMA_TRIGGER_SEL	DMA_TRIGGER_SEL field is used to select which trigger is used for Command Mode DMA path. 0x0: none 0x1: Start/end of frame (determined by COMMAND_MODE_DMA_MDP_ORDER) 0x2: TE 0x3: reserved_1 0x4: sw trigger 0x5: sw trigger and start/end of frame (COMMAND_MODE_DMA_MDP_ORDER) 0x6: sw trigger and TE 0x7: reserved_2

0x05800084 MIPI_DSI_2_DSI2_EXT_MUX

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI External Pin Mux Register - select IO pin for tearing effect and panel reset

MIPI_DSI_2_DSI2_EXT_MUX

Bits	Name	Description
31:20	EXT_TE_HSYNC_TOTAL	Defines the total number of hsync per frame
19:8	EXT_TE_HSYNC_TRIG_CNT	Defines the number of hsync needed to trigger the engine if TE_MODE is set to 1
7	EXT_TE_POL	Polarity of external tearing effect signal 0x0: TE occurs at the rising edge 0x1: TE occurs at the falling edge
6	RESERVED	
5:4	EXT_TE_MODE	Select TE mode 0x0: vsync_1 (edge detection) 0x1: vsync_2 (pulse width detection) 0x2: vsync and hsync combin_1 (edge detection) 0x3: vsync and hsync combin_2 (pulse width detection)
3:0	EXT_TE_MUX	Input port for external tearing effect (external trigger). Valid range: 0 to 1

0x05800088 MIPI_DSI_2_DSI2_EXT_TE_PULSE_DETECT_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI External Tearing Effect Pulse Width Detection Control Register

MIPI_DSI_2_DSI2_EXT_TE_PULSE_DETECT_CTRL

Bits	Name	Description
31:16	TE_VSYNC_MIN_WIDTH	Defines the minimum width (in escclk) of the vsync pulse in the TE signal
15:0	TE_HSYNC_MAX_WIDTH	Defines the maximum width (in escclk) of the hsync pulse in the TE signal

0x0580008C MIPI_DSI_2_DSI2_CMD_MODE_DMA_SW_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Command Mode DMA Software Trigger Register

MIPI_DSI_2_DSI2_CMD_MODE_DMA_SW_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Software can start a DMA trigger for the Command Mode engine by writing a 1 to this bit

0x05800090 MIPI_DSI_2_DSI2_CMD_MODE_MDP_SW_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Command Mode Display Processor Path Software Trigger Register

MIPI_DSI_2_DSI2_CMD_MODE_MDP_SW_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Software can start an MPD trigger for the Command Mode engine by writing a 1 to this bit

0x05800094 MIPI_DSI_2_DSI2_CMD_MODE_BTA_SW_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Command Mode Bus-Turn-Around Software Trigger Register

MIPI_DSI_2_DSI2_CMD_MODE_BTA_SW_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Software can start a BTA trigger for the Command Mode engine by writing a 1 to this bit

0x05800098 MIPI_DSI_2_DSI2_RESET_SW_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Reset Software Trigger Register

MIPI_DSI_2_DSI2_RESET_SW_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Software can trigger reset through the data link by writing a 1 to this bit

0x0580009C MIPI_DSI_2_DSI2_MISR_CMD_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI miser control for command mode operation - misr is collected for packets output from packetizer

MIPI_DSI_2_DSI2_MISR_CMD_CTRL

Bits	Name	Description
31:29	RESERVED_1	
28	EN	enable Command Mode misr accumulation (all the misr's are reset to 0 when it is disable)
27:25	RESERVED_2	
24	WIDTH_SEL	misr width of packets generated fronm dma, mdp stream 0 and mdp stream1 data 0x0: generate misr in 8 bits 0x1: generate misr in 16 bits
23:16	MDP_STREAM1_MISR	READ ONLY. 8-bit misr for packets generated from MDP stream 1
15:8	MDP_STREAM0_MISR	READ ONLY. 8-bit misr for packets generated from MDP stream 0
7:0	DMA_MISR	READ ONLY. 8-bit misr for packets generated from memory

0x058000A0 MIPI_DSI_2_DSI2_MISR_VIDEO_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI miser control for video mode operation - misr is collected for packets output from packetizer

MIPI_DSI_2_DSI2_MISR_VIDEO_CTRL

Bits	Name	Description
31:29	RESERVED_1	
28	STOP_EN	select misr accumulation restart or stop after N frame (specified in MAX_FRAME_COUNT) 0x0: auto reset every N frame 0x1: stop after N frames
27:25	RESERVED_2	
24	WIDTH_SEL	misr width of packets generated fronm dma, mdp stream 0 and mdp stream1 data 0x0: generate misr in 8 bits 0x1: generate misr in 16 bits
23:17	RESERVED	
16	EN	enable Video Mode misr accumulation (the misr is reset to 0 when it is disable)
15:8	MAX_FRAME_COUNT	internal misr is reset when the number of frames generated by the video mode engine reaches this number and the MISR field in this register is updated before the reset
7:0	MISR	READ ONLY. misr for video mode packets

0x058000A4 MIPI_DSI_2_DSI2_LANE_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Lane Status Register

MIPI_DSI_2_DSI2_LANE_STATUS

Bits	Name	Description
31:17	RESERVED_1	
16	DLN0_DIRECTION	READ ONLY. Indicate transmission direction of Data Lane 0 0x0: forward 0x1: reverse
15:13	RESERVED_2	
12	CLKLN_ULPS_ACTIVE_NOT	READ ONLY. Indicate whether Clock Lane is in Ultra-Low power state 0x0: ulps active 0x1: ulps not active

MIPI_DSI_2_DSI2_LANE_STATUS (cont.)

Bits	Name	Description
11	DLN3_ULPS_ACTIVE_NOT	READ ONLY. Indicate whether Data Lane 3 is in Ultra-Low power state 0x0: ulps active 0x1: ulps not active
10	DLN2_ULPS_ACTIVE_NOT	READ ONLY. Indicate whether Data Lane 2 is in Ultra-Low power state 0x0: ulps active 0x1: ulps not active
9	DLN1_ULPS_ACTIVE_NOT	READ ONLY. Indicate whether Data Lane 1 is in Ultra-Low power state 0x0: ulps active 0x1: ulps not active
8	DLN0_ULPS_ACTIVE_NOT	READ ONLY. Indicate whether Data Lane 0 is in Ultra-Low power state 0x0: ulps active 0x1: ulps not active
7:5	RESERVED	
4	CLKLN_STOPSTATE	READ ONLY. Indicate whether Clock Lane is in Stop state 0x0: active state 0x1: stop state
3	DLN3_STOPSTATE	READ ONLY. Indicate whether Data Lane 3 is in Stop state 0x0: active state 0x1: stop state
2	DLN2_STOPSTATE	READ ONLY. Indicate whether Data Lane 2 is in Stop state 0x0: active state 0x1: stop state
1	DLN1_STOPSTATE	READ ONLY. Indicate whether Data Lane 1 is in Stop state 0x0: active state 0x1: stop state
0	DLN0_STOPSTATE	READ ONLY. Indicate whether Data Lane 0 is in Stop state 0x0: active state 0x1: stop state

0x058000A8 MIPI_DSI_2_DSI2_LANE_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Lane Control Register

MIPI_DSI_2_DSI2_LANE_CTRL

Bits	Name	Description
31:29	RESERVED_1	
28	CLKLN_HS_FORCE_REQUEST	Force Clock Lane to enter HS mode always
27:21	RESERVED_2	
20	CLKLN_FORCE_TX_STOP	Force Clock Lane to go into transmit mode and the lane module state machine is forced into the Stop state
19	DLN3_FORCE_TX_STOP	Force Data Lane 3 to go into transmit mode and the lane module state machine is forced into the Stop state
18	DLN2_FORCE_TX_STOP	Force Data Lane 2 to go into transmit mode and the lane module state machine is forced into the Stop state
17	DLN1_FORCE_TX_STOP	Force Data Lane 1 to go into transmit mode and the lane module state machine is forced into the Stop state
16	DLN0_FORCE_TX_STOP	Force Data Lane 0 to go into transmit mode and the lane module state machine is forced into the Stop state
15:13	RESERVED_3	
12	CLKLN_ULPS_EXIT	Request Clock Lane to exit Ultra-Low power state
11	DLN3_ULPS_EXIT	Request Data Lane 3 to exit Ultra-Low power state
10	DLN2_ULPS_EXIT	Request Data Lane 2 to exit Ultra-Low power state
9	DLN1_ULPS_EXIT	Request Data Lane 1 to exit Ultra-Low power state
8	DLN0_ULPS_EXIT	Request Data Lane 0 to exit Ultra-Low power state
7:5	RESERVED_4	
4	CLKLN_ULPS_REQUEST	Request Clock Lane to enter Ultra-Low power state
3	DLN3_ULPS_REQUEST	Request Data Lane 3 to enter Ultra-Low power state
2	DLN2_ULPS_REQUEST	Request Data Lane 2 to enter Ultra-Low power state
1	DLN1_ULPS_REQUEST	Request Data Lane 1 to enter Ultra-Low power state
0	DLN0_ULPS_REQUEST	Request Data Lane 0 to enter Ultra-Low power state

0x058000AC MIPI_DSI_2_DSI2_LANE_SWAP_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Lane Swapping Control Register

MIPI_DSI_2_DSI2_LANE_SWAP_CTRL

Bits	Name	Description
31:3	RESERVED	
2:0	DLN_SWAP_SEL	PHY lane mapping for data lane 0, 1, 2, 3 output from the DSI controller - 000 = 0, 1, 2, 3 - 001 = 3, 0, 1, 2 - 010 = 2, 3, 0, 1 - 011 = 1, 2, 3, 0 - 100 = 0, 3, 2, 1 - 101 = 1, 0, 3, 2 - 110 = 2, 1, 0, 3 - 111 = 3, 2, 1, 0

0x058000B0 MIPI_DSI_2_DSI2_DLN0_PHY_ERR

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00088888

DSI PHY Error Register - reports errors returned from the PHY. If the mask bit for a specific error is set to 1, turn request will be de-asserted if the corresponding error occurs and controller will wait for the link to return to forward stopstate.

NOTE Turn request abort/interrupt will be generated if the mask field(s) in DSI_DLN0_PHY_ERR is set to 1. (Interrupt will be generated if the mask field(s) in DSI_INT_CTRL is set to 1; error status will be generated if the mask field(s) in DSI_ERR_INT_MASK0 is set to 0).

MIPI_DSI_2_DSI2_DLN0_PHY_ERR

Bits	Name	Description
31:20	RESERVED_1	
19	DLN0_ERR_CONTENTION_LP1_MASK	Option for controller to ignore this error 0x0: no action 0x1: abort turn request if error occurs
18:17	RESERVED_2	
16	DLN0_ERR_CONTENTION_LP1	READ ONLY. Contention detected while lane 0 is driven high
16	DLN0_ERR_CONTENTION_LP1_CLR	WRITE ONLY. Clear DLN0_ERR_CONTENTION_LP1 by writing a ’1’ to this field

MIPI_DSI_2_DSI2_DLN0_PHY_ERR (cont.)

Bits	Name	Description
15	DLN0_ERR_CONTENTION_LP0_MASK	Option for controller to ignore this error 0x0: no action 0x1: abort turn request if error occurs
14:13	RESERVED_3	
12	DLN0_ERR_CONTENTION_LP0_CLR	WRITE ONLY. Clear DLN0_ERR_CONTENTION_LP0 by writing a ’1’ to this field
12	DLN0_ERR_CONTENTION_LP0	READ ONLY. Contention detected while lane 0 is driven low
11	DLN0_ERR_CONTROL_MASK	Option for controller to ignore this error 0x0: no action 0x1: abort turn request if error occurs
10:9	RESERVED_4	
8	DLN0_ERR_CONTROL_CLR	WRITE ONLY. Clear DLN0_ERR_CONTROL by writing a ’1’ to this field
8	DLN0_ERR_CONTROL	READ ONLY. An incorrect line state sequence is detected
7	DLN0_ERR_SYNC_ESC_MASK	Option for controller to ignore this error 0x0: no action 0x1: abort turn request if error occurs
6:5	RESERVED_5	
4	DLN0_ERR_SYNC_ESC_CLR	WRITE ONLY. Clear DLN0_ERR_SYNC_ESC by writing a ’1’ to this field
4	DLN0_ERR_SYNC_ESC	READ ONLY. Number of bits received during a low power data transmission is not a multiple of eight when the transmission ends
3	DLN0_ERR_ESC_MASK	Option for controller to ignore this error 0x0: no action 0x1: abort turn request if error occurs
2:1	RESERVED_6	
0	DLN0_ERR_ESC_CLR	WRITE ONLY. Clear DLN0_ERR_ESC by writing a ’1’ to this field
0	DLN0_ERR_ESC	READ ONLY. Unrecognized escape entry command received

0x058000B4 MIPI_DSI_2_DSI2_LP_TIMER_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0xFFFFFFFF

DSI Timeout Control Register for Low Power Mode Transmission

MIPI_DSI_2_DSI2_LP_TIMER_CTRL

Bits	Name	Description
31:16	BTA_TO	Bus turn-around timeout (in escclk)
15:0	LP_RX_TO	Low power transmission reverse timeout (in Escclk)

0x058000B8 MIPI_DSI_2_DSI2_HS_TIMER_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000FFFF

DSI Timeout Control Register for High Speed Mode Transmission

MIPI_DSI_2_DSI2_HS_TIMER_CTRL

Bits	Name	Description
31:29	RESERVED_1	
28	HS_TX_TO_STOP_EN	Stop High Speed Transmission immediately at timeout
27:20	RESERVED_2	
19:16	TIMER_RESOLUTION	Control all 3 timeout counter increment steps by power of 2 of this field. Ex.: 0 = increment every escclk; - 1 = increment every 2 escclk; - 3 = increment every 8 escclk;
15:0	HS_TX_TO	High speed transmission timeout (in escclk)

0x058000BC MIPI_DSI_2_DSI2_TIMEOUT_STATUS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Timeout Status Register

MIPI_DSI_2_DSI2_TIMEOUT_STATUS

Bits	Name	Description
31:9	RESERVED_1	
8	BTA_TIMEOUT_CLR	WRITE ONLY. writing a 1 will clear this bit
8	BTA_TIMEOUT	READ ONLY. Indicates Bus Turnaround timeout

MIPI_DSI_2_DSI2_TIMEOUT_STATUS (cont.)

Bits	Name	Description
7:5	RESERVED_2	
4	LP_RX_TIMEOUT_CLR	WRITE ONLY. writing a 1 will clear this bit
4	LP_RX_TIMEOUT	READ ONLY. Indicates Low Power reverse transmission timeout
3:1	RESERVED	
0	HS_TX_TIMEOUT_CLR	WRITE ONLY. writing a 1 will clear this bit
0	HS_TX_TIMEOUT	READ ONLY. Indicates High Speed forward transmission timeout

0x058000C0 MIPI_DSI_2_DSI2_CLKOUT_TIMING_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI PHY Clock Lane Timing Control Register

MIPI_DSI_2_DSI2_CLKOUT_TIMING_CTRL

Bits	Name	Description
31:14	RESERVED_1	
13:8	T_CLK_POST	Number of byteclk cycles (minus one) that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to Low Power mode
7:6	RESERVED_2	
5:0	T_CLK_PRE	Number of byteclk cycles (minus one) that the high speed clock shall be driven prior to any associated Data Lane beginning the transition from Low Power to High Speed mode

0x058000C4 MIPI_DSI_2_DSI2_EOT_PACKET

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x010F0F08

DSI EOT Packet Register - packet to append at the end of a High Speed Data Burst

MIPI_DSI_2_DSI2_EOT_PACKET

Bits	Name	Description
31:24	ECC	ECC of the EOT packet

MIPI_DSI_2_DSI2_EOT_PACKET (cont.)

Bits	Name	Description
23:8	WC	Word count of the EOT packet
7:0	DI	Data identifier (virtual channel and datatype) of the EOT packet

0x058000C8 MIPI_DSI_2_DSI2_EOT_PACKET_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI EOT Packet Control Register

MIPI_DSI_2_DSI2_EOT_PACKET_CTRL

Bits	Name	Description
31:5	RESERVED_1	
4	RX_EOT_IGNORE	Specify whether the controller should ignore the EOT packet if it is received from reverse transmission 0x0: do not ignore 0x1: ignore
3:1	RESERVED_2	
0	TX_EOT_APPEND	Specify whether the EOT packet has to be appended at the end of each forward High Speed data burst 0x0: do not append 0x1: append

0x058000CC MIPI_DSI_2_DSI2_GENERIC_ESC_TX_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Generic Escape Mode Trigger Register

MIPI_DSI_2_DSI2_GENERIC_ESC_TX_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Software can trigger a generic escape mode command through DISP_DSIPHY_DLN0_TX_TRIGGER_ESC[3] by writing a 1 to this bit

0x058000D0 MIPI_DSI_2_DSI2_CAM_BIST_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display MIPI BIST Control. To start the BIST, all cam bist configuration should be done first, then CAM_BIST_EN should be set to 1 and lastly set DSI_CAM_BIST_START to 1. To stop or modify the cam bist configuration, program the DSI_CAM-BIST_* registers in reverse sequence (i.e.: start by writing DSI_CAM_BIST_START to 0).

MIPI_DSI_2_DSI2_CAM_BIST_CTRL

Bits	Name	Description
31:5	RESERVED_1	
4	CRC_EN	Enable CRC calculation for the CSI packets 0x0: disable 0x1: enable
3:2	RESERVED_2	
1	CAM_BIST_EN	- 1 Enables MIPI CSI BIST
0	CAM_BIST_RESET	- 1 Resets MIPI CSI BIST

0x058000D4 MIPI_DSI_2_DSI2_CAM_BIST_FRAME_SIZE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display Mipi BIST Video Frame Vertical and Horizontal size

MIPI_DSI_2_DSI2_CAM_BIST_FRAME_SIZE

Bits	Name	Description
31:16	CAM_V_SIZE	Vertical Size
15:0	CAM_H_SIZE	Horizontal Size

0x058000D8 MIPI_DSI_2_DSI2_CAM_BIST_BLOCK_SIZE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display Mipi BIST Video Block Vertical and Horizontal size

MIPI_DSI_2_DSI2_CAM_BIST_BLOCK_SIZE

Bits	Name	Description
31:16	RESERVED	
15:8	CAM_V_SIZE	Vertical Size
7:0	CAM_H_SIZE	Horizontal Size

0x058000DC MIPI_DSI_2_DSI2_CAM_BIST_FRAME_CONFIG

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display Mipi BIST Video Frame format

MIPI_DSI_2_DSI2_CAM_BIST_FRAME_CONFIG

Bits	Name	Description
31:25	RESERVED	
24	CAM_BIST_VIDEO_FRMT	- 0= YUV 4:2:2 8 bits 1= RAW 8 bits
23:16	CAM_FRAME_REPEAT	Reserved (Number of frame sequence NOT to be repeated)
15:0	CAM_BLANKING_CYCLES	Video scan Vertical and Horizontal Blanking cycle

0x058000E0 MIPI_DSI_2_DSI2_CAM_BIST_LSFR_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display MIPI BIST generator random numbers generator control

MIPI_DSI_2_DSI2_CAM_BIST_LSFR_CTRL

Bits	Name	Description
31:27	RESERVED	
26	CAM_V_LSFR_EN	(Unused) V component shift register enable
25	CAM_U_LSFR_EN	(Unused) U component shift register enable
24	CAM_Y_LSFR_EN	(Unused) Y component shift register enable
23:16	CAM_V_LSFR_POLYNOMIAL	V component polynomial

MIPI_DSI_2_DSI2_CAM_BIST_LSFR_CTRL (cont.)

Bits	Name	Description
15:8	CAM_U_LSFR_POLYNOMIAL	U component polynomial
7:0	CAM_Y_LSFR_POLYNOMIAL	Y component polynomial

0x058000E4 MIPI_DSI_2_DSI2_CAM_BIST_LSFR_INIT

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display MIPI BIST generator random numbers initial values

MIPI_DSI_2_DSI2_CAM_BIST_LSFR_INIT

Bits	Name	Description
31:24	RESERVED	
23:16	CAM_V_INIT_LSFR_VAL	V component shift register initial value
15:8	CAM_U_INIT_LSFR_VAL	U component shift register initial value
7:0	CAM_Y_INIT_LSFR_VAL	Y component shift register initial value

0x058000E8 MIPI_DSI_2_DSI2_CAM_BIST_START

Type: Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display MIPI BIST Start Stop control

MIPI_DSI_2_DSI2_CAM_BIST_START

Bits	Name	Description
31:1	RESERVED	
0	CAM_BIST_START	WRITE ONLY. Start and stop BIST. This field should be changed when CAM_BIST_EN = 1. When this field is set to 1, the BIST runs continuously. When this field is set to 0, the BIST will turn off at the end of the current frame. 0x0: Stop 0x1: Start

0x058000EC MIPI_DSI_2_DSI2_CAM_BIST_STATUS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Display MIPI BIST BUSY

MIPI_DSI_2_DSI2_CAM_BIST_STATUS

Bits	Name	Description
31:5	RESERVED_1	
4	CAM_BIST_DONE	READ ONLY. MIPI BIST done for 1 frame
4	CAM_BIST_DONE_CLR	WRITE ONLY. Writing a 1 will clear the done bit
3:1	RESERVED_2	
0	CAM_BIST_STATUS_BUSY	READ ONLY. MIPI BIST status bit

0x05800108 MIPI_DSI_2_DSI2_ERR_INT_MASK0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x13FF3BFF

DSI Error Interrupt Enable Register - enable any event to drive the error status (DSI_INT_CTRL.DSI_ERROR_STAT). If the DSI_INT_CTRL.DSI_ERROR_MASK is set to 1, interrupt will be generated.

NOTE Interrupt will be generated if the mask field(s) in DSI_INT_CTRL is set to 1; error status will be generated if the mask field(s) in DSI_ERR_INT_MASK0 is set to 0.

MIPI_DSI_2_DSI2_ERR_INT_MASK0

Bits	Name	Description
31:29	RESERVED_1	
28	DPHY_DSIPLL_UNLOCK_MASK	Mask dsipll unlock (to avoid sending out unnecessary interrupts, set this bit to 1 before dsipll locks) 0x0: allow generation of error status 0x1: no error status generated
27:26	RESERVED_2	

MIPI_DSI_2_DSI2_ERR_INT_MASK0 (cont.)

Bits	Name	Description
25	DLN0_ERR_CONTENTION_LP1_MASK	Mask contention while data lane 0 is driven high interrupt (DSI_DLN0_PHY_ERR reg, bit 16) 0x0: allow generation of error status (this should be set when dsipll is ready or when dsipll bypass is set to 1) 0x1: no error status generated
24	DLN0_ERR_CONTENTION_LP0_MASK	Mask contention while data lane 0 is driven low interrupt (DSI_DLN0_PHY_ERR reg, bit 12) 0x0: allow generation of error status 0x1: no error status generated
23	DLN0_ERR_CONTROL_MASK	Mask incorrect LP RX state sequence interrupt (DSI_DLN0_PHY_ERR reg, bit 8) 0x0: allow generation of error status 0x1: no error status generated
22	DLN0_ERR_SYNC_ESC_MASK	Mask LP RX data that is not byte-aligned interrupt (DSI_DLN0_PHY_ERR reg, bit 4) 0x0: allow generation of error status 0x1: no error status generated
21	DLN0_ERR_ESC_MASK	Mask incorrect LP RX escape entry interrupt (DSI_DLN0_PHY_ERR reg, bit 0) 0x0: allow generation of error status 0x1: no error status generated
20	DLN0_LP_FIFO_OVERFLOW_MASK	unused (Mask Lane Layer Low Power FIFO for data lane 0 interrupt (DSI_FIFO_STATUS reg, bit 14)) 0x0: allow generation of error status 0x1: no error status generated
19	DLN3_HS_FIFO_OVERFLOW_MASK	Mask Lane Layer High Speed FIFO for data lane 3 interrupt (DSI_STATUS reg, bit 30) 0x0: allow generation of error status 0x1: no error status generated
18	DLN2_HS_FIFO_OVERFLOW_MASK	Mask Lane Layer High Speed FIFO for data lane 2 interrupt (DSI_STATUS reg, bit 26) 0x0: allow generation of error status 0x1: no error status generated
17	DLN1_HS_FIFO_OVERFLOW_MASK	Mask Lane Layer High Speed FIFO for data lane 1 interrupt (DSI_FIFO_STATUS reg, bit 22) 0x0: allow generation of error status 0x1: no error status generated
16	DLN0_HS_FIFO_OVERFLOW_MASK	Mask Lane Layer High Speed FIFO for data lane 0 interrupt (DSI_FIFO_STATUS reg, bit 18) 0x0: allow generation of error status 0x1: no error status generated
15:14	RESERVED_3	

MIPI_DSI_2_DSI2_ERR_INT_MASK0 (cont.)

Bits	Name	Description
13	VID_MDP_FIFO_UNDERFLOW_MASK	Mask Video Mode Engine FIFO underflow interrupt (DSI_FIFO_STATUS reg, bit 3) 0x0: allow generation of error status 0x1: no error status generated
12	VID_MDP_FIFO_OVERFLOW_MASK	Mask Video Mode Engine FIFO overflow interrupt (DSI_FIFO_STATUS reg, bit 0) 0x0: allow generation of error status 0x1: no error status generated
11	CMD_MDP_FIFO_UNDERFLOW_MASK	Mask Display Engine FIFO underflow interrupt (DSI_FIFO_STATUS reg, bit 7) 0x0: allow generation of error status 0x1: no error status generated
10	RESERVED_4	
9	CMD_DMA_FIFO_UNDERFLOW_MASK	Mask Command mode dma FIFO underflow interrupt (DSI_FIFO_STATUS reg, bit 10) 0x0: allow generation of error status 0x1: no error status generated
8	INTERLEAVE_OP_CONTENTION_MASK	Mask interleave operation contention interrupt (DSI_STATUS reg, bit 31) 0x0: allow generation of error status 0x1: no error status generated
7	BTA_TO_MASK	Mask bus turnaround timeout interrupt (DSI_TIMEOUT_STATUS reg, bit 8) 0x0: allow generation of error status 0x1: no error status generated
6	HS_TX_TO_MASK	Mask High Speed forward transmission timeout interrupt (DSI_TIMEOUT_STATUS reg, bit 0) 0x0: allow generation of error status 0x1: no error status generated
5	LP_RX_TO_MASK	Mask Low Power reverse transmission timeout interrupt (DSI_TIMEOUT_STATUS reg, bit 4) 0x0: allow generation of error status 0x1: no error status generated
4	ERROR_PACKET_MASK	Mask error packet returned from peripheral interrupt (DSI_ACK_ERR_STATUS reg, bit 24) 0x0: allow generation of error status 0x1: no error status generated
3	RDBK_INCOMPLETE_PACKET_ERR_MASK	Mask incomplete read packet error interrupt (DSI_ACK_ERR_STATUS reg, bit 23) 0x0: allow generation of error status 0x1: no error status generated

MIPI_DSI_2_DSI2_ERR_INT_MASK0 (cont.)

Bits	Name	Description
2	RDBK_DATA_CRC_ERR_MASK	Mask crc error in the read packet interrupt (DSI_ACK_ERR_STATUS reg, bit 20) 0x0: allow generation of error status 0x1: no error status generated
1	RDBK_DATA_MULTI_ECC_ERR_MASK	Mask multi bit ecc error in the read packet interrupt (DSI_ACK_ERR_STATUS reg, bit 17) 0x0: allow generation of error status 0x1: no error status generated
0	RDBK_DATA_ECC_ERR_MASK	Mask single bit ecc error in the read packet interrupt (DSI_ACK_ERR_STATUS reg, bit 16) 0x0: allow generation of error status 0x1: no error status generated

0x0580010C MIPI_DSI_2_DSI2_INT_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x02200202

DSI Interrupt Control Register.

NOTE Interrupt will be generated if the mask field(s) in DSI_INT_CTRL is set to 1; error status will be generated if the mask field(s) in DSI_ERR_INT_MASK0 is set to 0.

MIPI_DSI_2_DSI2_INT_CTRL

Bits	Name	Description
31:26	RESERVED_1	
25	DSI_ERROR_MASK	DSI Error Mask. If set to 1, interrupt generation is enabled. 0x0: no interrupt generated 0x1: allow generation of interrupt
24	DSI_ERROR_AK	WRITE ONLY. DSI Error Acknowledge. If set to 1, status and interrupt is cleared.
24	DSI_ERROR_STAT	READ ONLY. DSI Error status. Set when the DSI Error has happened.
23:22	RESERVED_2	
21	DSI_BTA_DONE_MASK	DSI BTA Done Mask. If set to 1, interrupt generation is enabled. 0x0: no interrupt generated 0x1: allow generation of interrupt

MIPI_DSI_2_DSI2_INT_CTRL (cont.)

Bits	Name	Description
20	DSI_BTA_DONE_STAT	READ ONLY. DSI BTA Done Status (sw triggered BTA, embedded BTA or BTA generated for TE). Set when a bus turnaround has completed.
20	DSI_BTA_DONE_AK	WRITE ONLY. DSI BTA Done Acknowledge. If set to 1, status and interrupt is cleared.
19:18	RESERVED_3	
17	DSI_VIDEO_MODE_DONE_MASK	DSI Video Mode Engine path Done Mask. If set to 1, interrupt generation is enabled. 0x0: no interrupt generated 0x1: allow generation of interrupt
16	DSI_VIDEO_MODE_DONE_AK	WRITE ONLY. DSI Video Mode Engine path Done Acknowledge. If set to 1, status and interrupt is cleared.
16	DSI_VIDEO_MODE_DONE_STAT	READ ONLY. DSI Video Mode Engine status. Set when the DSI Video Mode Engine has finished transferring data to the panel.
15:10	RESERVED_4	
9	DSI_CMD_MODE_MDP_DONE_MASK	DSI Command Mode Engine MDP path Done Mask. If set to 1, interrupt generation is enabled. 0x0: no interrupt generated 0x1: allow generation of interrupt
8	DSI_CMD_MODE_MDP_DONE_STAT	READ ONLY. DSI Command Mode Engine MDP path status. Set when the DSI Command Mode Engine has finished transferring deng data to the panel.
8	DSI_CMD_MODE_MDP_DONE_AK	WRITE ONLY. DSI Command Mode Engine MDP path Done Acknowledge. If set to 1, status and interrupt is cleared.
7:2	RESERVED	
1	DSI_CMD_MODE_DMA_DONE_MASK	DSI Command Mode Engine DMA path Done Mask. If set to 1, interrupt generation is enabled. 0x0: no interrupt generated 0x1: allow generation of interrupt
0	DSI_CMD_MODE_DMA_DONE_AK	WRITE ONLY. DSI Command Mode Engine DMA path Done Acknowledge. If set to 1, status and interrupt is cleared.
0	DSI_CMD_MODE_DMA_DONE_STAT	READ ONLY. DSI Command Mode Engine DMA status. Set when the DSI Command Mode Engine has finished transferring dma data to the panel.

0x05800110 MIPI_DSI_2_DSI2_IOBIST_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI IOBIST Control Register

MIPI_DSI_2_DSI2_IOBIST_CTRL

Bits	Name	Description

31:0	DSI_IOBIST_CTRL	This register has 2 modes of operation: command and timing mode. All configuration fields should be written first, then enable (bit 0) should be set to 1 next and start (bit 5) is set to 1 last.
		
		COMMAND MODE
		bit 0 = DSI IOBIST ENABLE. Active high;
		bit 5 = IOBIST start. Active high;
		bit 6 = Select power mode for data transfer.
		- 0 = high speed (HS), 1 = low power (LP)
		bit 7 = Data pattern mode.
		- 0 = Use data pattern word, 1 = PRBS pattern.
		bit 10:8 = multiple of finite random run (N): if bit 12 is finite, the finite run is 256 x (N+1) runs for HS PRBS and user data, or 16 x (N+1) for LP PRBS
		bit 12 = Infinite run
		- 0 for infinite; 1 for 256 x (N+1) runs of HS PRBS, 16 x (N+1) runs of LP PRBS, 256 x (N+1) runs of HS user data, or 8 runs of LP user data.
		bit 14:13 = DSIBIST_DSIPHY_LANE_SWAP, select which lane is used as lane0 for LPDT:
		- 0 = DLN0
		- 1 = DLN1
		- 2 = DLN2
		- 3 = DLN3
		bit 15 = Select instruction type
		- 0 = command mode, 1 = DSI timing control mode.
		bit 23:16 = data pattern byte (used when bit 7 is set to 0)
		other bits = reserved
		
		TIMING MODE
		bit 0 = DSI IOBIST ENABLE. Active high;
		bit 5 = IOBIST start. Active high;
		bit 15 = Select instruction type
		- 0 = command mode, 1 = DSI timing control mode.
		(If you write one DSI timing data with the select instruction type == 1, you have to change the select instruction type from 1 to 0 for timing data latch control.)
		bit 23:16 = DSI timing data;
		bit 28:24 = DSI timing register selection:
		- 0x10 = DSI_T_CLK_PRE (data width[5:0])
		- 0x11 = DSI_T_CLK_POST (data width[5:0])

0x05800114 MIPI_DSI_2_DSI2_SOFT_RESET

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI soft reset Register

MIPI_DSI_2_DSI2_SOFT_RESET

Bits	Name	Description
31:1	RESERVED	
0	DSI_SOFT_RESET	Resets all internal logic in dsiclk, pclk, byteclk, escclk, ahbm_hclk domain. All enable bits in DSI_CTRL shoud be already set to 0 when exiting soft reset (DSI_SOFT_RESET changing from 1 to 0). The dynamic clocks should be forced on when DSI_SOFT_RESET is set to 1. (This reset does not apply to DSI registers which are in ahbs_hclk domain.)

0x05800118 MIPI_DSI_2_DSI2_CLK_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Clock Control Register. The dynamic clocks should be forced on when DSI_SOFT_RESET is set to 1 or when DSI_EN is changed from 1 to 0

MIPI_DSI_2_DSI2_CLK_CTRL

Bits	Name	Description
31:18	RESERVED_1	
17:16	DSI_DSICLK_HYSTERISIS1_CTRL	DSI DSICLK Hysterisis Control
15:14	DSI_AHBM_HCLK_HYSTERISIS1_CTRL	DSI AHBM_HCLK Hysterisis Control
13:12	DSI_AHBS_HCLK_HYSTERISIS1_CTRL	unused
11	DSI_FORCE_ON_DYN_BYTECLK	DSI Dynamic BYTECLK Clock Branch Force On. Set to one to always force on this clock branch.
10	DSI_FORCE_ON_DYN_DSICLK	DSI Dynamic DSICLK Clock Branch Force On. Set to one to always force on this clock branch.
9	DSI_FORCE_ON_DYN_AHBM_HCLK	DSI Dynamic AHBM_HCLK (MCLK) Clock Branch Force On. Set to one to always force on this clock branch.

MIPI_DSI_2_DSI2_CLK_CTRL (cont.)

Bits	Name	Description
8	DSI_FORCE_ON_DYN_AHBS_HCLK	DSI Dynamic AHBS_HCLK (REGCLK)Clock Branch Force On. Set to one to always force on this clock branch.
7:6	RESERVED_2	
5	DSI_ESCCLK_ON	Turns on/off ESCCLK for the DSI. If set to 1, clock is ON.
4	DSI_BYTECLK_ON	Turns on/off BYTECLK for the DSI. If set to 1, clock is ON.
3	DSI_DSICLK_ON	Turns on/off DSICLK for the DSI. If set to 1, clock is ON.
2	DSI_PCLK_ON	Turns on/off PCLK for the DSI. If set to 1, clock is ON.
1	DSI_AHBM_SCLK_ON	Turns on/off AHBM_HCLK for the DSI. If set to 1, clock is ON.
0	DSI_AHBS_HCLK_ON	Turns on/off AHBS_HCLK for the DSI. If set to 1, clock is ON.

0x0580011C MIPI_DSI_2_DSI2_CLK_STATUS

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Clock Status Register

MIPI_DSI_2_DSI2_CLK_STATUS

Bits	Name	Description
31:17	RESERVED_1	
16	DSIPLL_UNLOCKED_CLR	WRITE ONLY. Write only. Clear dsipll_unlocked status by writing to this register field
16	DSIPLL_UNLOCKED	READ ONLY. Read only. Dsi pll unlock status 0x0: dsipll not unlocked 0x1: dsipll unlocked
15:10	RESERVED_2	
9	DSI_AON_PCLK_ACTIVE	READ ONLY. DSI Always ON PCLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
8	DSI_AON_ESCCLK_ACTIVE	READ ONLY. DSI Always ON ESCCLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
7	DSI_DYN_BYTECLK_ACTIVE	READ ONLY. DSI Dynamic BYTECLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
6	DSI_AON_BYTECLK_ACTIVE	READ ONLY. DSI Always ON BYTECLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.

MIPI_DSI_2_DSI2_CLK_STATUS (cont.)

Bits	Name	Description
5	DSI_DYN_DSICLK_ACTIVE	READ ONLY. DSI Dynamic DSICLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
4	DSI_AON_DSICLK_ACTIVE	READ ONLY. DSI Always ON DSICLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
3	DSI_DYN_AHBS_HCLK_ACTIVE	READ ONLY. DSI Dynamic AHBS_HCLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
2	DSI_AON_AHBS_HCLK_ACTIVE	READ ONLY. DSI Always ON AHBS_HCLK Active Status. Read-only field that shows the status of this clock branch.If set to one, clock is on. If set to zero, clock is off.
1	DSI_DYN_AHBM_HCLK_ACTIVE	READ ONLY. DSI Dynamic AHBM_HCLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.
0	DSI_AON_AHBM_HCLK_ACTIVE	READ ONLY. DSI Always ON AHBM_HCLK Active Status. Read-only field that shows the status of this clock branch. If set to one, clock is on. If set to zero, clock is off.

0x05800120 MIPI_DSI_2_DSI2_DEBUG_BUS_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI debug bus control Register

MIPI_DSI_2_DSI2_DEBUG_BUS_CTRL

Bits	Name	Description
31:14	RESERVED_1	
13:12	DEBUG_MUX	debug mux select within the selected block
11:10	RESERVED_2	

MIPI_DSI_2_DSI2_DEBUG_BUS_CTRL (cont.)

Bits	Name	Description
9:4	DEBUG_SEL	debug bus block select - 0-4: pclk domain debug signals; - 5-9: escclk domain debug signals - 10-19: byteclk domain debug signals - 20-29: dsiclk domain debug signals - 30-34: mclk domain debug signals - 35-39: dphy domain debug signals - 40-42: regclk domain debug signals - 43-59: reserved - 60: fixed pattern 0xFFFFFFFF - 61: fixed pattern 0xAAAAAAAA - 62: fixed pattern 0x55555555 - 63: fixed pattern 0xAF50_F50A
3:1	RESERVED	
0	DEBUG_BUS_EN	debug bus enable, the debug bus is cleared to 0 when debug bus is disable

0x05800124 MIPI_DSI_2_DSI2_DEBUG_BUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI debug bus Register

MIPI_DSI_2_DSI2_DEBUG_BUS

Bits	Name	Description
31:0	DEBUG_BUS	READ ONLY. value on the selected debug bus

0x05800128 MIPI_DSI_2_DSI2_PHY_SW_RESET

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI PHY SW Reset Register

MIPI_DSI_2_DSI2_PHY_SW_RESET

Bits	Name	Description
31:25	RESERVED_1	

MIPI_DSI_2_DSI2_PHY_SW_RESET (cont.)

Bits	Name	Description
24	PHY_REGULATOR_HW_RESET	THIS BIT IS ONLY USED IN DSI CORE 1. PHY software reset for the regulator. A reset pulse is issued by writing 1 followed by a 0 to this bit.
23:17	RESERVED_2	
16	PHY_LN_HW_RESET	PHY software reset for the LANES. A reset pulse is issued by writing 1 followed by a 0 to this bit.
15:9	RESERVED_3	
8	PHY_PLL_HW_RESET	PHY software reset for the PLL. A reset pulse is issued by writing 1 followed by a 0 to this bit.
7:5	RESERVED_4	
4	PHY_SW_RESET_POL	polarity of all reset signals for PHY PLL, LANES and regulator. - 0 = active high; - 1 = active low
3:1	RESERVED	
0	PHY_SW_RESET	PHY hardware reset for all PHY PLL, LANES and REGULATOR (for DSI CORE 1 only). A reset pulse is issued by writing 1 followed by a 0 to this bit.

0x0580012C MIPI_DSI_2_DSI2_AXI2AHB_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI AXI to AHB bridge control Register

MIPI_DSI_2_DSI2_AXI2AHB_CTRL

Bits	Name	Description
31:1	RESERVED	
0	MSM_ACCUMULATE_EN	Read data accumulate enable - 1 = allows for all read data to be returned prior to feeding it out - 0 = returns read data immediately

0x05800130 MIPI_DSI_2_DSI2_MISR_CMD_MDP0_32BIT

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0xFFFFFFFF

DSI Command MDP stream 0 32-bit misr

MIPI_DSI_2_DSI2_MISR_CMD_MDP0_32BIT

Bits	Name	Description
31:0	MISR	READ ONLY. 32-bit misr for packets generated from MDP stream 0

0x05800134 MIPI_DSI_2_DSI2_MISR_CMD_MDP1_32BIT

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0xFFFFFFFF

DSI Command MDP stream 0 32-bit misr

MIPI_DSI_2_DSI2_MISR_CMD_MDP1_32BIT

Bits	Name	Description
31:0	MISR	READ ONLY. 32-bit misr for packets generated from MDP stream 0

0x05800138 MIPI_DSI_2_DSI2_MISR_CMD_DMA_32BIT

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0xFFFFFFFF

DSI Command dma 32-bit misr

MIPI_DSI_2_DSI2_MISR_CMD_DMA_32BIT

Bits	Name	Description
31:0	MISR	READ ONLY. 32-bit misr for packets generated from memory

0x0580013C MIPI_DSI_2_DSI2_MISR_VIDEO_32BIT

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0xFFFFFFFF

DSI Video Mode 32-bit misr

MIPI_DSI_2_DSI2_MISR_VIDEO_32BIT

Bits	Name	Description
31:0	MISR	READ ONLY. 32-bit misr for packets generated from MDP's DSI Video Mode stream

0x05800140 MIPI_DSI_2_DSI2_LANE_MISR_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI Lane MISR control

MIPI_DSI_2_DSI2_LANE_MISR_CTRL

Bits	Name	Description
31:1	RESERVED	
0	EN	Enable MISR calculation of the lane data at the output of the lane distribution layer 0x0: disable 0x1: enable

0x05800144 MIPI_DSI_2_DSI2_LANE0_MISR

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000FFFF

DSI Lane 0 MISR value

MIPI_DSI_2_DSI2_LANE0_MISR

Bits	Name	Description
31:16	RESERVED	
15:0	MISR	READ ONLY. MISR value of the lane data at the output of the lane distribution layer

0x05800148 MIPI_DSI_2_DSI2_LANE1_MISR

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000FFFF

DSI Lane 1 MISR value

MIPI_DSI_2_DSI2_LANE1_MISR

Bits	Name	Description
31:16	RESERVED	
15:0	MISR	READ ONLY. MISR value of the lane data at the output of the lane distribution layer

0x0580014C MIPI_DSI_2_DSI2_LANE2_MISR

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000FFFF

DSI Lane 2 MISR value

MIPI_DSI_2_DSI2_LANE2_MISR

Bits	Name	Description
31:16	RESERVED	
15:0	MISR	READ ONLY. MISR value of the lane data at the output of the lane distribution layer

0x05800150 MIPI_DSI_2_DSI2_LANE3_MISR

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000FFFF

DSI Lane 3 MISR value

MIPI_DSI_2_DSI2_LANE3_MISR

Bits	Name	Description
31:16	RESERVED	
15:0	MISR	READ ONLY. MISR value of the lane data at the output of the lane distribution layer

0x05800158 MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DSI test pattern generator control register

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CTRL

Bits	Name	Description
31:18	RESERVED_1	
17:16	CMD_DMA_PATTERN_SEL	test pattern for command mode dma data 0x0: PRBS pattern generated from polynomial and init value 0x1: incremental starting from init value 0x2: fixed to init value 0x3: reserved
15:14	RESERVED_2	
13:12	CMD_MDP_STREAM1_PATTERN_SEL	test pattern for command mode pixel (MDP) stream1 data 0x0: PRBS pattern generated from polynomial and init value 0x1: incremental starting from init value 0x2: fixed to init value 0x3: reserved
11:10	RESERVED_3	
9:8	CMD_MDP_STREAM0_PATTERN_SEL	test pattern for command mode pixel (MDP) stream0 data 0x0: PRBS pattern generated from polynomial and init value 0x1: incremental starting from init value 0x2: fixed to init value 0x3: reserved
7:6	RESERVED_4	
5:4	VIDEO_PATTERN_SEL	test pattern for video mode operation 0x0: PRBS pattern generated from polynomial and init value 0x1: incremental starting from init value 0x2: fixed to init value 0x3: reserved
3:1	RESERVED	

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CTRL (cont.)

Bits	Name	Description
0	EN	DSI test pattern enable. This is the global enable of the pattern generator. Once this bit is set to 1, it is ready to generate data for video mode, command mode pixel or dma data. Video mode data is started by DSI*_TEST_PATTERN_GEN_VIDEO_ENABLE; Command mode pixel data can be started by DSI*_TEST_PATTERN_GEN_CMD_STREAM[01]_TRIGGER or triggered by the trigger source set in COMMAND_MODE_MDP_TRIGGER_SEL; Command mode dma data is generated when a memory read request is received (the application layer will generate memory read request when it is triggered by the trigger source set in COMMAND_MODE_DMA_TRIGGER_SEL). Note: for Command dma data, only use the pattern generator in DMA non-embedded mode only (DSI*_COMMAND_MODE_DMA_CTRL.embedded_mode set to 0) because the pattern generator only generates a test pattern for payload.

0x0580015C MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_VIDEO_POLY

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Polynomial of the Video mode test pattern generator

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_VIDEO_POLY

Bits	Name	Description
31:24	RESERVED	
23:0	POLYNOMIAL	- 24-bit LSFR polynomial applied for pixel data

0x05800160 MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_VIDEO_INIT_VAL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Initial value of the Video mode test pattern generator

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_VIDEO_INIT_VAL

Bits	Name	Description
31:24	RESERVED	

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_VIDEO_INIT_VAL (cont.)

Bits	Name	Description
23:0	INIT_VAL	- 24-bit initial value applied for pixel data

0x05800164 MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_MDP_STREAM0_POLY

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Polynomial of the Command mode test pattern generator for stream0

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_MDP_STREAM0_POLY

Bits	Name	Description
31:24	RESERVED	
23:0	POLYNOMIAL	- 24-bit LSFR polynomial applied for pixel data

0x05800168 MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_MDP_INIT_VAL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Initial value of the Command mode test pattern generator for stream0

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_MDP_INIT_VAL0

Bits	Name	Description
31:24	RESERVED	
23:0	INIT_VAL	- 24-bit initial value applied for pixel data

0x0580016C MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_MDP_STREAM1_POLY

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Polynomial of the Command mode test pattern generator for stream1

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_MDP_STREAM1_POLY

Bits	Name	Description
31:24	RESERVED	
23:0	POLYNOMIAL	- 24-bit LSFR polynomial applied for pixel data

0x05800170 MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_MDP_INIT_VAL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Initial value of the Command mode test pattern generator for stream1

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_MDP_INIT_VAL1

Bits	Name	Description
31:24	RESERVED	
23:0	INIT_VAL	- 24-bit initial value applied for pixel data

0x05800174 MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_DMA_POLY

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Polynomial of the Command mode test pattern generator for dma data

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_DMA_POLY

Bits	Name	Description
31:0	POLYNOMIAL	- 32-bit LSFR polynomial applied for dma data

0x05800178 MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_DMA_INIT_VAL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Initial value of the Command mode test pattern generator for dma

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_DMA_INIT_VAL

Bits	Name	Description
31:0	INIT_VAL	- 32-bit initial value applied for dma data

0x0580017C MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_VIDEO_ENABLE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Enable test pattern for video mode

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_VIDEO_ENABLE

Bits	Name	Description
31:1	RESERVED	
0	EN	enable video stream test pattern. Once this bit is set to 1, the pattern generator will start generating video stream 0x0: disable 0x1: enable

0x05800180 MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_STREAM0_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Trigger test pattern for Command MDP stream0

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_STREAM0_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Writing this bit will trigger a frame for command MDP stream 0

0x05800184 MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_STREAM1_TRIGGER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Trigger test pattern for Command MDP stream1

MIPI_DSI_2_DSI2_TEST_PATTERN_GEN_CMD_STREAM1_TRIGGER

Bits	Name	Description
31:1	RESERVED	
0	SW_TRIGGER	Writing this bit will trigger a frame for command MDP stream 1

0x05800190 MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_IDLE_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Idle insertion between Command MDP packets

MIPI_DSI_2_DSI2_COMMAND_MODE_MDP_IDLE_CTRL

Bits	Name	Description
31:14	RESERVED_1	
13:12	EN	enable idle insertion between Command Mode MDP packets 0x0: disable 0x1: insert idle for stream0 0x2: insert idle for stream1 0x3: insertion idle for both streams
11:10	RESERVED_2	
9:0	LENGTH	Number of dsiclk cycles of idle time to insert between Command Mode MDP packets. This idle counter is added in the application layer. To ensure the DSI link will go into stopstate between Command Mode MDP packets, the LENGTH must be long enough to cover the time the link takes to switch between High Speed mode to Low Power mode (LP11).

0x058001F0 MIPI_DSI_2_DSI2_VERSION

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x02000104

DSI Version Register

MIPI_DSI_2_DSI2_VERSION

Bits	Name	Description
31:24	MAJOR_VERSION	READ ONLY. DSI major version number ex.: 2 for DSI 2.0

MIPI_DSI_2_DSI2_VERSION (cont.)

Bits	Name	Description
23:16	MINOR_VERSION	READ ONLY. DSI minor version number ex.: 0 for DSI 2.0
15:8	PHY_VERSION	READ ONLY. PHY version that this core supports - 0 = 45nm PHY - 1 = 28nm PHY
7:4	RESERVED	
3:0	CONFIG	READ ONLY. DSI configuration - 2 = this version can support up to 2 lanes - 4 = this version can support up to 4 lanes

0x05800200 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

NOTE The preferred names for all DSIPHY_PLL_CTRL_n registers would be DSIPHY_PLL_CFGn.

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_0

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5	DSIPLL_BYPASS	Output Clock Control (Debug Purpose). When it is '1', the output clocks will be generated from reference clock. When it is '0', output clocks will be generated from PLL VCO clock. Normal operational mode setting is 0 Power up value is 0
4	DSIPLL_OPEN_LOOP	Open Loop Setting. When this bit is set to 1, the Lock Time is significantly reduced compared to lock time in closed loop mode. 0=Closed Loop Mode - 1= Open Loop Mode Normal operational mode setting is 0. Power up value is 0
3	DSIPLL_PWR_MODE	PLL const-gm bias select - 0: Resistor div bias is selected - 1: PLL Const-gm bias is selected Normal operational mode setting is 0. Power up value is 0
2	RESERVED_BITS2	

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_0 (cont.)

Bits	Name	Description
1	DSIPLL_SWCAL_EN	S/W Calibration Enable Control. If the bit is '1', then the PLL will ignore CAL_MODE and perform S/W calibration. VCO OFFSET and SLOPE will be set by MAN_OFFSET and MAN_SLOPE.We are not using the SW calibration anymore. So this bit should be set to '0'. Normal operational mode setting is 0. Power up value is 0
0	DSIPLL_PLL_EN	PLL Enable Signal. Analog power down. - 1 = Normal Mode of operation - 0 = Power Down State Normal operational mode setting is 1. Power up value is 0

0x05800204 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000000E

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPLL_DIV_FB_7_0	- 11 bit Feed back divider Ratio. {DSIPHY_PLL_CTRL_2[DSIPLL_DIV_FB_10_8], DSIPLL_DIV_FB_7_0} - 000_0000_0000 = div by 1 - 000_0000_0001 = div by 2 - 000_0000_0010 = div by 3 ... 111_1111_1111 = div by 2048 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 0000_1110

0x05800208 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000030

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_2

Bits	Name	Description
31:7	RESERVED_BITS31_7	

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_2 (cont.)

Bits	Name	Description
6:4	DSIPLL_UNLOCK_RES	Unlock Detector Resolution Setting. 000: unlock=1 if 1 mismatch between ref_clk and fb_clk - 001: unlock=1 if 2 consecutive mismatches between ref_clk and fb_clk - 010: unlock=1 if 3 consecutive mismatches between ref_clk and fb_clk ... - 111: unlock=1 if 8 consecutive mismatches between ref_clk and fb_clk Normal operational mode setting is 011. Power up value is 011
3	RESERVED_BITS3	
2:0	DSIPLL_DIV_FB_10_8	- 11 bit Feed back divider Ratio. {DSIPLL_DIV_FB_10_8,DSIPHY_PLL_CTRL_1[DSIPLL_DIV_FB_7_0]} - 000_0000_0000 = div by 1 - 000_0000_0001 = div by 2 - 000_0000_0010 = div by 3 ... 111_1111_1111 = div by 2048 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 000

0x0580020C MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_3

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	DSIPLL_CAL_MODE	Calibration Mode Setting. - 00 :Skip calibration and use I_MAN_OFFSET and I_MAN_SLOPE for VCO. - 01/10/11 : Perform calibration for both OFFSET and SLOPE settings Normal operational mode setting is 11 Power up value is 11

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_3 (cont.)

Bits	Name	Description
5:0	DSIPLL_DIV_REF	Reference Divider Ratio. 000000 : div by 1 - 000001 : div by 2 - 000010 : div by 3 - 000011 : div by 4 ... - 111111 : div by 64 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 00_0000

0x05800210 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_4

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800214 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000040

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_5

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	DSIPLL_LF_R	Loop Filter Resistor R setting. 000: 100K - 001: 75K - 010: 50K - 011: 35K - 100: 25K - 101: 20K - 110: 12K - 111: 8K Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 100
3:0	RESERVED_BITS3_0	

0x05800218 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_6

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000003

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_6

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	DSIPLL_LF_C2	Loop Filter Capacitor C2 setting.(3+B2*18+B1*9+B0*6) 000: 3pF - 001: 9pF - 010: 12pF - 011: 18pF - 100: 21pF - 101: 27pF - 110: 30pF - 111: 36pF Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 000
3:0	DSIPLL_LF_C1	Loop Filter Capacitor C1 setting.(20+B3*130+B2*60+B1*25+B0*15) 0000: 20pF - 0001: 35pF - 0010 : 45pF - 0011 : 60pF - 0100: 80pF - 0101: 95pF - 0110: 105pF - 0111:120pF - 1000: 150pF - 1001: 165pF - 1010: 175pF - 1011: 190pF - 1100: 210pF - 1101:225pF - 1110: 235pF - 1111: 250pF Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 0011

0x0580021C MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_7

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000062

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_7

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	DSIPLL_DIGITAL_WAITTIME	PLL Digital wait time setting. 00 : 6 REF_CLK cycles - 01 :11 REF_CLK cycles - 10 : 23 REF_CLK cycles - 11 : 52 REF_CLK cycles Normal operational mode setting is 11. Power up value is 11
4:3	RESERVED_BITS4_3	
2:0	DSIPLL_CP	Charge Pump Current setting. 000 : 5uA - 001 : 10uA - 010 : 12.5uA - 011 : 17.5uA - 100 : 20uA - 101 : 25uA - 110 : 27.5uA - 111 : 32.5uA Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 010

0x05800220 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_8

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000040

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_8

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	DSIPLL_UNLOCK_DET_SEL	- 0: use negedge(50% phase detect) - 1: use posedge(100% phase detect) Normal operational mode setting is 0. Power up value is 0

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_8 (cont.)

Bits	Name	Description
6:4	DSIPLL_VREF_CONF	These bits sets the Vtune value in PLL Open Loop Mode. - 000: Vtune=0.50v - 001: Vtune=0.55v - 010: Vtune=0.60v - 011: Vtune=0.65v - 100: Vtune=0.70v - 101: Vtune=0.75v - 110: Vtune=0.80v - 111: Vtune=0.85v The preferred name for this register bit field would be DSIPLL_VTUNE_CONF. Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 100
3:0	DSIPLL_OUT_DIV1	Output Divider setting for oCLK1 (Bitclk). This is a high frequency clock and it goes to clock layer. 0000: div by1 - 0001: div by2 - 0010: div by3 - 0011: div by4 ... - 1111: div by16 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. The preferred name for this register bit field would be DSIPLL_OUT_DIV_BITCLK. Power up value is 0000

0x05800224 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_9

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000007

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_9

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_9 (cont.)

Bits	Name	Description
7:0	DSIPLL_OUT_DIV2	Output Divider setting for oCLK2. This is pixel clock going to DSI Controller. 00000000: div by1 - 00000001: div by2 - 00000010: div by3 - 00000011: div by4 ... - 11111111: div by256 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. The preferred name for this register bit field would be DSIPLL_OUT_DIV_BYTECLK. Power up value is 0000_0111

0x05800228 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_10

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000007

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_10

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPLL_OUT_DIV3	Output Divider setting for oCLK3. This is a test clock going to DSI Controller. - 00000000: div by1 - 00000001: div by2 - 00000010: div by3 - 00000011: div by4 ... - 11111111: div by256 The preferred name for this register bit field would be DSIPLL_OUT_DIV_DSICLK. Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 0000_0111

0x0580022C MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_11

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_11

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	DSIPLL_SVS_MODE	SVS. Mode Enable - 0: Normal operation mode - 1: SVS. operation mode In SVS. mode, bit clock, byte clock and dsi clock will be half the frequency of normal operation mode. Normal operational mode setting is 0. Power up value is 0
3:0	RESERVED_BITS3_0	

0x05800230 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_12

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000001A

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_12

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4:0	DSIPLL_MAN_OFFSET	Manual setting for VCO offset Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power on Reset value is 1_1010

0x05800234 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_13

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_13

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2:0	DSIPLL_MAN_SLOPE	Manual setting for VCO slope Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power up value is 000

0x05800238 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_14

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_14

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	PLL_SW_RESET	RESET for Digital blocks except control registers. Active high signal. - 1: Assertion - 0: De-assertion Normal operational mode setting is 0. Power up value is 0
0	FORCE_PLL_READY	- 0: PLL_READY from PLL Lock detect will be used - 1: PLL_READY from PLL Lock detect will be bypassed. In other words it will force the PLL_READY to high. This bit is only used as a back up in case the PLL LOCKDETECTOR does not operate correctly. Power up value is 0 Normal value is 0.

0x0580023C MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_15

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000002

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_15

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	RESERVED_BITS2	
1	DSIPLL_IBIAS_CAL_EN	PLL Ibias Calibration Enable - 0: Ibias Calibration disabled - 1: Ibias Calibration enabled Normal operational mode setting is 1 Power up value is 1
0	RESERVED_BITS0	

0x05800240 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_16

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_16

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPLL_CL_LOCKTIME_7_0	Closed Loop Lock time counter value. It specifies the Lock time in number of reference clock cycles after the reference divider. The minimum time required is 50us. Lock Time=cl_locktime<15:0>*ref_cycle_time Normal operational mode setting: 0 Power up value is 0

0x05800244 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_17

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000020

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_17

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPLL_CL_LOCKTIME_15_8	Closed Loop Lock time counter value. It specifies the Lock time in number of reference clock cycles after the reference divider. The minimum time required is 50us Lock Time=cl_locktime<15:0>*ref_cycle_time. Normal operational mode setting: 0010_0000 Power up value is 0010_0000

0x05800248 MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_18

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_18

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_18 (cont.)

Bits	Name	Description
7:0	DSIPLL_OL_LOCKTIME_7_0	Open Loop Lock time. It specifies the lock time in number of reference clock cycles after the reference divider. The minimum time required is 5us. Normal operational mode setting is 1000_1000. Power up value is 0000_0000

0x0580024C MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_19

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000002

MIPI_DSI_2_DSI2_DSIPHY_PLL_CTRL_19

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	DSIPLL_SWCAL_DONE	We are not using SW Calibration anymore. So this bit should be set to '0'. Normal operational mode setting is 0. Power up value is 0
1:0	DSIPLL_OL_LOCKTIME_9_8	Open Loop Lock time. It specifies the lock time in number of reference clock cycles after the reference divider. The minimum time required is 5us. Normal operational mode setting is 00. Power up value is 10

0x05800250 MIPI_DSI_2_DSI2_DSIPHY_PLL_TEST_EFUSE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_TEST_EFUSE

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5	PLLPHY_EFUSE_OVRRIDE_SEL	- 0: Use EFUSE value selected by PLLPHY_DRVSTR_EFUSE_SEL - 1: Override with PLLPHY_EFUSE value. Power up value is 0
4	PLLPHY_DRVSTR_EFUSE_SEL	- 1: Select the efuse used for datalane impedence calibration - 0: Select dedicated PLL calibration efuse Power up value is 0

MIPI_DSI_2_DSI2_DSIPHY_PLL_TEST_EFUSE (cont.)

Bits	Name	Description
3:0	PLLPHY_EFUSE	efuse override value Power up value is 0000

0x05800254 MIPI_DSI_2_DSI2_DSIPHY_PLL_TEST_SANITY_CHECK

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_TEST_SANITY_CHECK

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DSIPLL_SANITY_CHECK	- 1: PLL clock frequency based on power up value. OUTCLK1 = 810MHz, OUTCLK2=OUTCLK3=(OUTCLK1/8). 0: PLL clock frequency based on PLL software configuration Normal operational mode setting is 0. Power up value is 0

0x05800258 MIPI_DSI_2_DSI2_DSIPHY_PLL_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_PLL_DEBUG_SEL	Refer to Table at the end of the PLL section to see detailed description of debug bus selections: (MDP_LVDSPHY_PLL_ANA_STATUS2)

0x0580025C MIPI_DSI_2_DSI2_RESERVED_PLL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_RESERVED_PLL

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800260 MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000020

MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6	DSIPLL_REF_POLY_SEL	- 0: Poly select is disabled - 1: Poly select is enabled Power up value is 0
5	DSIPLL_OTA_BIAS_SEL	- 0: OTA replica bias is disabled - 1: OTA replica bias is enabled Power up value is 1
4:1	DSIPLL_ANA_TESTMUX_SELECT	PLL Analog Test Mux Select bits Normal operational mode setting is 0000. Power up value is 0000 0x0: Uncalibrated bias current 0x1: Calibrated bias current
0	DSIPLL_ANA_TESTMUX_ENABLE	PLL Analog Test Mux Enable Normal operational mode setting is 0. Power up value is 0

0x05800264 MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL1

Bits	Name	Description
31:5	RESERVED_BITS31_5	

MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL1 (cont.)

Bits	Name	Description
4:1	DSIPLL_DIGCLK_TESTMUX_SELECT	PLL Digital CLK Test Mux Select bits Normal operational mode setting is 0000. Power up value is 0000 0x0: VCO clock 0x1: PLL unlock detect 0x2: Byte clock 0x3: Divided reference clock 0x4: Reference clock 0x5: Feedback clock 0x6: DSI clock 0x7: VCO clock div 2
0	DSIPLL_DIGCLK_TESTMUX_EN	PLL Digital CLK Test Mux Enable Normal operational mode setting is 0. Power up value is 0

0x05800268 MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x0580026C MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL3

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800270 MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL4

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800274 MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL5

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800278 MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL6

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL6

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x0580027C MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL7

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_CTRL7

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800280 MIPI_DSI_2_DSI2_DSIPHY_PLL_RDY

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_RDY

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	PLL_RDY	READ ONLY. monitor pll_rdy Power up value is 0

0x05800284 MIPI_DSI_2_DSI2_DSIPHY_PLL_DBGBUS_STATUS0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_DBGBUS_STATUS0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_PLL_DEBUG_BUS_7_0	READ ONLY. Power up value is 0000_0000

0x05800288 MIPI_DSI_2_DSI2_DSIPHY_PLL_DBGBUS_STATUS1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_DBGBUS_STATUS1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_PLL_DEBUG_BUS_15_8	READ ONLY. Power up value is 0000_0000

0x0580028C MIPI_DSI_2_DSI2_DSIPHY_PLL_DBGBUS_STATUS2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_DBGBUS_STATUS2

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_PLL_DEBUG_BUS_23_16	READ ONLY. Power up value is 0000_0000

0x05800290 MIPI_DSI_2_DSI2_DSIPHY_PLL_DBGBUS_STATUS3

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_DBGBUS_STATUS3

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_PLL_DEBUG_BUS_31_24	READ ONLY. Power up value is 0000_0000

0x05800294 MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_STATUS0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_STATUS0

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800298 MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_STATUS1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_STATUS1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x0580029C MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_STATUS2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_PLL_ANA_STATUS2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800300 MIPI_DSI_2_DSI2_DSIPHY_LN0_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

MIPI_DSI_2_DSI2_DSIPHY_LN0_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	DSIPHY_HSTX_SLEW	DSIPHY Slew Rate Control Normal operational mode setting is 11. Power up value is 11
5	RESERVED_BITS5	
4:0	DSIPHY_HSTX_DLY	This has been de-featured since LLDR Power up value is 0_0000

0x05800304 MIPI_DSI_2_DSI2_DSIPHY_LN0_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_2_DSI2_DSIPHY_LN0_CFG1 (cont.)

Bits	Name	Description
7:5	DSIPHY_PEMPH_STRBOT	Determines how many Pre-Emphasis branches for the bottom termination are enabled. Normal operational mode setting is 000. Power up value is 000.
4	RESERVED_BITS4	
3:1	DSIPHY_PEMPH_STRTOP	Determines how many Pre-Emphasis branches for the top termination are enabled Normal operational mode setting is 000. Power up value is 000.
0	DSIPHY_PEMPH_EN	Enable Signal for Driver Pre-Emphasis.0: Pre-Emphasis is Disabled -1: Pre-Emphasis is Enabled Normal operational mode setting is 0. Power up value is 0

0x05800308 MIPI_DSI_2_DSI2_DSIPHY_LN0_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_CFG2

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:4	DSIPHY_LPTX_SLEW	LPTX slew rate control To enable or disable LPTX-P and LPTX-N independently during test-mode. In functional mode(test_mode=0) if LPTX_EN is high, both LPTX-P and LPTX-N are on. When test_mode=1 and test_mode_hstx_en=0, DSIPHY_LPTX_SLEW[0] enables/disables LPTX-P for a value of 1/0 respectively, while DSIPHY_LPTX_SLEW[1] enables/disables LPTX-N for a value of 1/0 respectively. Power up value is 00
3:0	DSIPHY_LPRX_DLY	- 3:2 : Escape Clock pulse width adjustment - 1:0 : Escape Clock Delay element. Power up value is 0000

0x0580030C MIPI_DSI_2_DSI2_DSIPHY_LN0_TEST_DATAPATH

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_TEST_DATAPATH

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	ANE_BYPASS_EN	Enables analog near-end loopback Power up value is 0
6:4	DMUX_LP_SEL	Mux select for testing purposes - 0xx: Mission Mode - 100: LPRX to LPTX - 110: CDRX to LPTX - 111: REG_TEST to LPTX Power up value is 000
3:2	DMUX_HS_SEL	Mux select for testing purposes - 01: PLL_TEST_CLK to HSTX - 11: Adjacent HSRX signal to HSTX Power up value is 00 0x0: Mission Mode
1	TEST_MODE_HSTX_EN	Enable HSTX when test_mode=1: Power up value is 0
0	FORCE_TEST_MODE	When this bit is set to 1, Enable software control bits of lptx, hstx, lprx, or cdrx for testing purposes Power up value is 0

0x05800310 MIPI_DSI_2_DSI2_DSIPHY_LN0_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_2_DSI2_DSIPHY_LN0_DEBUG_SEL (cont.)

Bits	Name	Description
7:0	DSIPHY_DEBUG_SEL	DSIPHY Data Lane Debug Bus Select Refer to Table at the end of the PHY SWI section to see detailed description of Lane debug bus selections: MDP_LVDSPHY_PLL_ANA_STATUS2 **Note 1**: Lane debug bus can be observed only when DSIPHY_GLBL_DIGTOP_DEBUG_SEL[DSIPHY_GLBL_DIGTOP_DEBUG_SEL] is set to 8'bxxxx_x11x **Note 2**: Only 1 lane at a time should be selected. Ensure all other lane debug bus mux select is set to 0. Normal operational mode setting is 0000_0000. Power up value is 0000_0000

0x05800314 MIPI_DSI_2_DSI2_DSIPHY_LN0_TEST_STR0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_TEST_STR0

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DSIPHY_STR_VALUE_OVERRIDE	- 0: Calibrated value - 1: Strength override value, DSIPHY_LNn_TEST_STR1 Power up value is 0

0x05800318 MIPI_DSI_2_DSI2_DSIPHY_LN0_TEST_STR1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_TEST_STR1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP	Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT	Power up value is 0000

0x0580031C MIPI_DSI_2_DSI2_DSIPHY_LN0_BIST_CTL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_BIST_CTL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	MISR_SIG_READ	- 11: Select MISR1 - MISR signature for the valid DATA read from TX FIFO - 10: Select MISR0 - MISR signature for the valid DATA write to TX FIFO - 00 or 01: Select BIST error count Power up value is 00
4	MISR_SIG_CLEAR	- 1: Clear both MISR to default signature value 16hFFFF Power up value is 0
3	RESERVED_BIT3	
2	BIST_RX_PRBS_ERROR_INJECT	- 1: Inject Error pattern into RX checker. Power up value is 0
1	BIST_RX_PRBS_GEN_SHORT	- 1:Pattern length is 2^8 - 0:Pattern is generated continuously until bist_rx_prbs_chk_en is disabled Normal operational mode setting is 0 Power up value is 0
0	DSIPHY_ERROR_CLR	- 1: Clear Error count. Power up value is 0

0x05800320 MIPI_DSI_2_DSI2_DSIPHY_LN0_BIST_CTL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_BIST_CTL1

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	DSIPHY_HSRX_TERM_EN	- 1: Enable cross termination for HSRX in BIST mode. Power up value is 0
0	DSIPHY_HSRX_EN	- 1: Enable HSRX in BIST mode. Power up value is 0

0x05800324 MIPI_DSI_2_DSI2_DSIPHY_LN0_RESERVED2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_RESERVED2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800328 MIPI_DSI_2_DSI2_DSIPHY_LN0_BIST_RXCHK_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_BIST_RXCHK_STATUS

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	CHECK_DONE	READ ONLY. This bit is set when the prbs checker is done for short pattern Power up value is 0
1	RXCHK_HEADER_SEL	READ ONLY. PRBS checker Header sel control signal Power up value is 0
0	RXCHK_PRBS_START	READ ONLY. PRBS checker PRBS START control signal. Power up value is 0

0x0580032C MIPI_DSI_2_DSI2_DSIPHY_LN0_HSTX_STR_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_HSTX_STR_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP_STATUS	READ ONLY. Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT_STATUS	READ ONLY. Power up value is 0000

0x05800330 MIPI_DSI_2_DSI2_RESERVED1_PHY_LN0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_RESERVED1_PHY_LN0

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800334 MIPI_DSI_2_DSI2_RESERVED2_PHY_LN0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_RESERVED2_PHY_LN0

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800338 MIPI_DSI_2_DSI2_DSIPHY_LN0_BIST_MISR_STAT0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_BIST_MISR_STAT0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_7_0	READ ONLY. Power up value is 0000_0000

0x0580033C MIPI_DSI_2_DSI2_DSIPHY_LN0_BIST_MISR_STAT1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN0_BIST_MISR_STAT1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_15_8	READ ONLY. Power up value is 0000_0000

0x05800340 MIPI_DSI_2_DSI2_DSIPHY_LN1_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

MIPI_DSI_2_DSI2_DSIPHY_LN1_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	DSIPHY_HSTX_SLEW	DSIPHY Slew Rate Control Normal operational mode setting is 11. Power up value is 11
5	RESERVED_BITS5	
4:0	DSIPHY_HSTX_DLY	This has been de-featured since LLDR Power up value is 0_0000

0x05800344 MIPI_DSI_2_DSI2_DSIPHY_LN1_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:5	DSIPHY_PEMPH_STRBOT	Determines how many Pre-Emphasis branches for the bottom termination are enabled. Normal operational mode setting is 000. Power up value is 000.
4	RESERVED_BITS4	
3:1	DSIPHY_PEMPH_STRTOP	Determines how many Pre-Emphasis branches for the top termination are enabled Normal operational mode setting is 000. Power up value is 000.

MIPI_DSI_2_DSI2_DSIPHY_LN1_CFG1 (cont.)

Bits	Name	Description
0	DSIPHY_PEMPH_EN	Enable Signal for Driver Pre-Emphasis.0: Pre-Emphasis is Disabled -1: Pre-Emphasis is Enabled Normal operational mode setting is 0. Power up value is 0

0x05800348 MIPI_DSI_2_DSI2_DSIPHY_LN1_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_CFG2

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:4	DSIPHY_LPTX_SLEW	LPTX slew rate control To enable or disable LPTX-P and LPTX-N independently during test-mode. In functional mode(test_mode=0) if LPTX_EN is high, both LPTX-P and LPTX-N are on. When test_mode=1 and test_mode_hstx_en=0, DSIPHY_LPTX_SLEW[0] enables/disables LPTX-P for a value of 1/0 respectively, while DSIPHY_LPTX_SLEW[1] enables/disables LPTX-N for a value of 1/0 respectively. Power up value is 00
3:0	DSIPHY_LPRX_DLY	- 3:2 : Escape Clock pulse width adjustment - 1:0 : Escape Clock Delay element. Power up value is 0000

0x0580034C MIPI_DSI_2_DSI2_DSIPHY_LN1_TEST_DATAPATH

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_TEST_DATAPATH

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	ANE_BYPASS_EN	Enables analog near-end loopback Power up value is 0

MIPI_DSI_2_DSI2_DSIPHY_LN1_TEST_DATAPATH (cont.)

Bits	Name	Description
6:4	DMUX_LP_SEL	Mux select for testing purposes - 0xx: Mission Mode - 100: LPRX to LPTX - 110: CDRX to LPTX - 111: REG_TEST to LPTX Power up value is 000
3:2	DMUX_HS_SEL	Mux select for testing purposes - 01: PLL_TEST_CLK to HSTX - 11: Adjacent HSRX signal to HSTX Power up value is 00 0x0: Mission Mode
1	TEST_MODE_HSTX_EN	Enable HSTX when test_mode=1: Power up value is 0
0	FORCE_TEST_MODE	When this bit is set to 1, Enable software control bits of lptx, hstx, lprx, or cdrx for testing purposes Power up value is 0

0x05800350 MIPI_DSI_2_DSI2_DSIPHY_LN1_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_DEBUG_SEL	DSIPHY Data Lane Debug Bus Select Refer to Table at the end of the PHY SWI section to see detailed description of Lane debug bus selections: MDP_LVDSPHY_PLL_ANA_STATUS2 **Note 1**: Lane debug bus can be observed only when DSIPHY_GLBL_DIGTOP_DEBUG_SEL[DSIPHY_GLBL_DIGTOP_DEBUG_SEL] is set to 8'bxxxx_x11x **Note 2**: Only 1 lane at a time should be selected. Ensure all other lane debug bus mux select is set to 0. Normal operational mode setting is 0000_0000. Power up value is 0000_0000

0x05800354 MIPI_DSI_2_DSI2_DSIPHY_LN1_TEST_STR0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_TEST_STR0

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DSIPHY_STR_VALUE_OVERRIDE	- 0: Calibrated value - 1: Strength override value, DSIPHY_LNn_TEST_STR1 Power up value is 0

0x05800358 MIPI_DSI_2_DSI2_DSIPHY_LN1_TEST_STR1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_TEST_STR1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP	Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT	Power up value is 0000

0x0580035C MIPI_DSI_2_DSI2_DSIPHY_LN1_BIST_CTL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_BIST_CTL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	MISR_SIG_READ	- 11: Select MISR1 - MISR signature for the valid DATA read from TX FIFO - 10: Select MISR0 - MISR signature for the valid DATA write to TX FIFO - 00 or 01: Select BIST error count Power up value is 00

MIPI_DSI_2_DSI2_DSIPHY_LN1_BIST_CTL0 (cont.)

Bits	Name	Description
4	MISR_SIG_CLEAR	- 1: Clear both MISR to default signature value 16hFFFF Power up value is 0
3	RESERVED_BIT3	
2	BIST_RX_PRBS_ERROR_INJECT	- 1: Inject Error pattern into RX checker. Power up value is 0
1	BIST_RX_PRBS_GEN_SHORT	- 1:Pattern length is 2^8 - 0:Pattern is generated continuously until bist_rx_prbs_chk_en is disabled Normal operational mode setting is 0 Power up value is 0
0	DSIPHY_ERROR_CLR	- 1: Clear Error count. Power up value is 0

0x05800360 MIPI_DSI_2_DSI2_DSIPHY_LN1_BIST_CTL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_BIST_CTL1

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	DSIPHY_HSRX_TERM_EN	- 1: Enable cross termination for HSRX in BIST mode. Power up value is 0
0	DSIPHY_HSRX_EN	- 1: Enable HSRX in BIST mode. Power up value is 0

0x05800364 MIPI_DSI_2_DSI2_DSIPHY_LN1_RESERVED2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_RESERVED2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800368 MIPI_DSI_2_DSI2_DSIPHY_LN1_BIST_RXCHK_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_BIST_RXCHK_STATUS

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	CHECK_DONE	READ ONLY. This bit is set when the prbs checker is done for short pattern Power up value is 0
1	RXCHK_HEADER_SEL	READ ONLY. PRBS checker Header sel control signal Power up value is 0
0	RXCHK_PRBS_START	READ ONLY. PRBS checker PRBS START control signal. Power up value is 0

0x0580036C MIPI_DSI_2_DSI2_DSIPHY_LN1_HSTX_STR_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_HSTX_STR_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP_STATUS	READ ONLY. Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT_STATUS	READ ONLY. Power up value is 0000

0x05800370 MIPI_DSI_2_DSI2_RESERVED1_PHY_LN1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_RESERVED1_PHY_LN1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800374 MIPI_DSI_2_DSI2_RESERVED2_PHY_LN1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_RESERVED2_PHY_LN1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800378 MIPI_DSI_2_DSI2_DSIPHY_LN1_BIST_MISR_STAT0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_BIST_MISR_STAT0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_7_0	READ ONLY. Power up value is 0000_0000

0x0580037C MIPI_DSI_2_DSI2_DSIPHY_LN1_BIST_MISR_STAT1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN1_BIST_MISR_STAT1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_15_8	READ ONLY. Power up value is 0000_0000

0x05800380 MIPI_DSI_2_DSI2_DSIPHY_LN2_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

MIPI_DSI_2_DSI2_DSIPHY_LN2_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	DSIPHY_HSTX_SLEW	DSIPHY Slew Rate Control Normal operational mode setting is 11. Power up value is 11
5	RESERVED_BITS5	
4:0	DSIPHY_HSTX_DLY	This has been de-featured since LLDR Power up value is 0_0000

0x05800384 MIPI_DSI_2_DSI2_DSIPHY_LN2_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:5	DSIPHY_PEMPH_STRBOT	Determines how many Pre-Emphasis branches for the bottom termination are enabled. Normal operational mode setting is 000. Power up value is 000.
4	RESERVED_BITS4	
3:1	DSIPHY_PEMPH_STRTOP	Determines how many Pre-Emphasis branches for the top termination are enabled Normal operational mode setting is 000. Power up value is 000.
0	DSIPHY_PEMPH_EN	Enable Signal for Driver Pre-Emphasis.0: Pre-Emphasis is Disabled -1: Pre-Emphasis is Enabled Normal operational mode setting is 0. Power up value is 0

0x05800388 MIPI_DSI_2_DSI2_DSIPHY_LN2_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_CFG2

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:4	DSIPHY_LPTX_SLEW	LPTX slew rate control To enable or disable LPTX-P and LPTX-N independently during test-mode. In functional mode(test_mode=0) if LPTX_EN is high, both LPTX-P and LPTX-N are on. When test_mode=1 and test_mode_hstx_en=0, DSIPHY_LPTX_SLEW[0] enables/disables LPTX-P for a value of 1/0 respectively, while DSIPHY_LPTX_SLEW[1] enables/disables LPTX-N for a value of 1/0 respectively. Power up value is 00
3:0	DSIPHY_LPRX_DLY	- 3:2 : Escape Clock pulse width adjustment - 1:0 : Escape Clock Delay element. Power up value is 0000

0x0580038C MIPI_DSI_2_DSI2_DSIPHY_LN2_TEST_DATAPATH

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_TEST_DATAPATH

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	ANE_BYPASS_EN	Enables analog near-end loopback Power up value is 0
6:4	DMUX_LP_SEL	Mux select for testing purposes - 0xx: Mission Mode - 100: LPRX to LPTX - 110: CDRX to LPTX - 111: REG_TEST to LPTX Power up value is 000
3:2	DMUX_HS_SEL	Mux select for testing purposes - 01: PLL_TEST_CLK to HSTX - 11: Adjacent HSRX signal to HSTX Power up value is 00 0x0: Mission Mode
1	TEST_MODE_HSTX_EN	Enable HSTX when test_mode=1: Power up value is 0

MIPI_DSI_2_DSI2_DSIPHY_LN2_TEST_DATAPATH (cont.)

Bits	Name	Description
0	FORCE_TEST_MODE	When this bit is set to 1, Enable software control bits of lptx, hstx, lprx, or cdrx for testing purposes Power up value is 0

0x05800390 MIPI_DSI_2_DSI2_DSIPHY_LN2_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_DEBUG_SEL	DSIPHY Data Lane Debug Bus Select Refer to Table at the end of the PHY SWI section to see detailed description of Lane debug bus selections: MDP_LVDSPHY_PLL_ANA_STATUS2 **Note 1**: Lane debug bus can be observed only when DSIPHY_GLBL_DIGTOP_DEBUG_SEL[DSIPHY_GLBL_DIGTOP_DEBUG_SEL] is set to 8'bxxxx_x11x **Note 2**: Only 1 lane at a time should be selected. Ensure all other lane debug bus mux select is set to 0. Normal operational mode setting is 0000_0000. Power up value is 0000_0000

0x05800394 MIPI_DSI_2_DSI2_DSIPHY_LN2_TEST_STR0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_TEST_STR0

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DSIPHY_STR_VALUE_OVERRIDE	- 0: Calibrated value - 1: Strength override value, DSIPHY_LNn_TEST_STR1 Power up value is 0

0x05800398 MIPI_DSI_2_DSI2_DSIPHY_LN2_TEST_STR1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_TEST_STR1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP	Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT	Power up value is 0000

0x0580039C MIPI_DSI_2_DSI2_DSIPHY_LN2_BIST_CTL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_BIST_CTL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	MISR_SIG_READ	- 11: Select MISR1 - MISR signature for the valid DATA read from TX FIFO - 10: Select MISR0 - MISR signature for the valid DATA write to TX FIFO - 00 or 01: Select BIST error count Power up value is 00
4	MISR_SIG_CLEAR	- 1: Clear both MISR to default signature value 16hFFFF Power up value is 0
3	RESERVED_BIT3	
2	BIST_RX_PRBS_ERROR_INJECT	- 1: Inject Error pattern into RX checker. Power up value is 0
1	BIST_RX_PRBS_GEN_SHORT	- 1:Pattern length is 2^8 - 0:Pattern is generated continuously until bist_rx_prbs_chk_en is disabled Normal operational mode setting is 0 Power up value is 0
0	DSIPHY_ERROR_CLR	- 1: Clear Error count. Power up value is 0

0x058003A0 MIPI_DSI_2_DSI2_DSIPHY_LN2_BIST_CTL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_BIST_CTL1

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	DSIPHY_HSRX_TERM_EN	- 1: Enable cross termination for HSRX in BIST mode. Power up value is 0
0	DSIPHY_HSRX_EN	- 1: Enable HSRX in BIST mode. Power up value is 0

0x058003A4 MIPI_DSI_2_DSI2_DSIPHY_LN2_RESERVED2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_RESERVED2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x058003A8 MIPI_DSI_2_DSI2_DSIPHY_LN2_BIST_RXCHK_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_BIST_RXCHK_STATUS

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	CHECK_DONE	READ ONLY. This bit is set when the prbs checker is done for short pattern Power up value is 0
1	RXCHK_HEADER_SEL	READ ONLY. PRBS checker Header sel control signal Power up value is 0
0	RXCHK_PRBS_START	READ ONLY. PRBS checker PRBS START control signal. Power up value is 0

0x058003AC MIPI_DSI_2_DSI2_DSIPHY_LN2_HSTX_STR_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_HSTX_STR_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP_STATUS	READ ONLY. Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT_STATUS	READ ONLY. Power up value is 0000

0x058003B0 MIPI_DSI_2_DSI2_RESERVED1_PHY_LN2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_RESERVED1_PHY_LN2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x058003B4 MIPI_DSI_2_DSI2_RESERVED2_PHY_LN2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_RESERVED2_PHY_LN2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x058003B8 MIPI_DSI_2_DSI2_DSIPHY_LN2_BIST_MISR_STAT0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_BIST_MISR_STAT0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_7_0	READ ONLY. Power up value is 0000_0000

0x058003BC MIPI_DSI_2_DSI2_DSIPHY_LN2_BIST_MISR_STAT1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN2_BIST_MISR_STAT1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_15_8	READ ONLY. Power up value is 0000_0000

0x058003C0 MIPI_DSI_2_DSI2_DSIPHY_LN3_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

MIPI_DSI_2_DSI2_DSIPHY_LN3_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	DSIPHY_HSTX_SLEW	DSIPHY Slew Rate Control Normal operational mode setting is 11. Power up value is 11
5	RESERVED_BITS5	
4:0	DSIPHY_HSTX_DLY	This has been de-featured since LLDR Power up value is 0_0000

0x058003C4 MIPI_DSI_2_DSI2_DSIPHY_LN3_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:5	DSIPHY_PEMPH_STRBOT	Determines how many Pre-Emphasis branches for the bottom termination are enabled. Normal operational mode setting is 000. Power up value is 000.
4	RESERVED_BITS4	
3:1	DSIPHY_PEMPH_STRTOP	Determines how many Pre-Emphasis branches for the top termination are enabled Normal operational mode setting is 000. Power up value is 000.
0	DSIPHY_PEMPH_EN	Enable Signal for Driver Pre-Emphasis.0: Pre-Emphasis is Disabled -1: Pre-Emphasis is Enabled Normal operational mode setting is 0. Power up value is 0

0x058003C8 MIPI_DSI_2_DSI2_DSIPHY_LN3_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_CFG2

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:4	DSIPHY_LPTX_SLEW	LPTX slew rate control To enable or disable LPTX-P and LPTX-N independently during test-mode. In functional mode(test_mode=0) if LPTX_EN is high, both LPTX-P and LPTX-N are on. When test_mode=1 and test_mode_hstx_en=0, DSIPHY_LPTX_SLEW[0] enables/disables LPTX-P for a value of 1/0 respectively, while DSIPHY_LPTX_SLEW[1] enables/disables LPTX-N for a value of 1/0 respectively. Power up value is 00
3:0	DSIPHY_LPRX_DLY	- 3:2 : Escape Clock pulse width adjustment - 1:0 : Escape Clock Delay element. Power up value is 0000

0x058003CC MIPI_DSI_2_DSI2_DSIPHY_LN3_TEST_DATAPATH

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_TEST_DATAPATH

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	ANE_BYPASS_EN	Enables analog near-end loopback Power up value is 0
6:4	DMUX_LP_SEL	Mux select for testing purposes - 0xx: Mission Mode - 100: LPRX to LPTX - 110: CDRX to LPTX - 111: REG_TEST to LPTX Power up value is 000
3:2	DMUX_HS_SEL	Mux select for testing purposes - 01: PLL_TEST_CLK to HSTX - 11: Adjacent HSRX signal to HSTX Power up value is 00 0x0: Mission Mode
1	TEST_MODE_HSTX_EN	Enable HSTX when test_mode=1: Power up value is 0
0	FORCE_TEST_MODE	When this bit is set to 1, Enable software control bits of lptx, hstx, lprx, or cdrx for testing purposes Power up value is 0

0x058003D0 MIPI_DSI_2_DSI2_DSIPHY_LN3_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_2_DSI2_DSIPHY_LN3_DEBUG_SEL (cont.)

Bits	Name	Description
7:0	DSIPHY_DEBUG_SEL	DSIPHY Data Lane Debug Bus Select Refer to Table at the end of the PHY SWI section to see detailed description of Lane debug bus selections: MDP_LVDSPHY_PLL_ANA_STATUS2 **Note 1**: Lane debug bus can be observed only when DSIPHY_GLBL_DIGTOP_DEBUG_SEL[DSIPHY_GLBL_DIGTOP_DEBUG_SEL] is set to 8'bxxxx_x11x **Note 2**: Only 1 lane at a time should be selected. Ensure all other lane debug bus mux select is set to 0. Normal operational mode setting is 0000_0000. Power up value is 0000_0000

0x058003D4 MIPI_DSI_2_DSI2_DSIPHY_LN3_TEST_STR0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_TEST_STR0

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DSIPHY_STR_VALUE_OVERRIDE	- 0: Calibrated value - 1: Strength override value, DSIPHY_LNn_TEST_STR1 Power up value is 0

0x058003D8 MIPI_DSI_2_DSI2_DSIPHY_LN3_TEST_STR1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_TEST_STR1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP	Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT	Power up value is 0000

0x058003DC MIPI_DSI_2_DSI2_DSIPHY_LN3_BIST_CTL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_BIST_CTL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	MISR_SIG_READ	- 11: Select MISR1 - MISR signature for the valid DATA read from TX FIFO - 10: Select MISR0 - MISR signature for the valid DATA write to TX FIFO - 00 or 01: Select BIST error count Power up value is 00
4	MISR_SIG_CLEAR	- 1: Clear both MISR to default signature value 16hFFFF Power up value is 0
3	RESERVED_BIT3	
2	BIST_RX_PRBS_ERROR_INJECT	- 1: Inject Error pattern into RX checker. Power up value is 0
1	BIST_RX_PRBS_GEN_SHORT	- 1:Pattern length is 2^8 - 0:Pattern is generated continuously until bist_rx_prbs_chk_en is disabled Normal operational mode setting is 0 Power up value is 0
0	DSIPHY_ERROR_CLR	- 1: Clear Error count. Power up value is 0

0x058003E0 MIPI_DSI_2_DSI2_DSIPHY_LN3_BIST_CTL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_BIST_CTL1

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	DSIPHY_HSRX_TERM_EN	- 1: Enable cross termination for HSRX in BIST mode. Power up value is 0
0	DSIPHY_HSRX_EN	- 1: Enable HSRX in BIST mode. Power up value is 0

0x058003E4 MIPI_DSI_2_DSI2_DSIPHY_LN3_RESERVED2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_RESERVED2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x058003E8 MIPI_DSI_2_DSI2_DSIPHY_LN3_BIST_RXCHK_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_BIST_RXCHK_STATUS

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	CHECK_DONE	READ ONLY. This bit is set when the prbs checker is done for short pattern Power up value is 0
1	RXCHK_HEADER_SEL	READ ONLY. PRBS checker Header sel control signal Power up value is 0
0	RXCHK_PRBS_START	READ ONLY. PRBS checker PRBS START control signal. Power up value is 0

0x058003EC MIPI_DSI_2_DSI2_DSIPHY_LN3_HSTX_STR_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_HSTX_STR_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP_STATUS	READ ONLY. Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT_STATUS	READ ONLY. Power up value is 0000

0x058003F0 MIPI_DSI_2_DSI2_RESERVED1_PHY_LN3

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_RESERVED1_PHY_LN3

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x058003F4 MIPI_DSI_2_DSI2_RESERVED2_PHY_LN3

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_RESERVED2_PHY_LN3

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x058003F8 MIPI_DSI_2_DSI2_DSIPHY_LN3_BIST_MISR_STAT0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_BIST_MISR_STAT0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_7_0	READ ONLY. Power up value is 0000_0000

0x058003FC MIPI_DSI_2_DSI2_DSIPHY_LN3_BIST_MISR_STAT1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LN3_BIST_MISR_STAT1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_15_8	READ ONLY. Power up value is 0000_0000

0x05800400 MIPI_DSI_2_DSI2_DSIPHY_LNCK_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

MIPI_DSI_2_DSI2_DSIPHY_LNCK_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	DSIPHY_HSTX_SLEW	DSIPHY Slew Rate Control Normal operational mode setting is 11. Power up value is 11
5	RESERVED_BITS5	
4:0	DSIPHY_HSTX_DLY	This has been de-featured since LLDR Power up value is 0_0000

0x05800404 MIPI_DSI_2_DSI2_DSIPHY_LNCK_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:5	DSIPHY_PEMPH_STRBOT	Determines how many Pre-Emphasis branches for the bottom termination are enabled. Normal operational mode setting is 000. Power up value is 000.
4	RESERVED_BITS4	
3:1	DSIPHY_PEMPH_STRTOP	Determines how many Pre-Emphasis branches for the top termination are enabled. Normal operational mode setting is 000. Power up value is 000.

MIPI_DSI_2_DSI2_DSIPHY_LNCK_CFG1 (cont.)

Bits	Name	Description
0	DSIPHY_PEMPH_EN	Enable Signal for Driver Pre-Emphasis.0: Pre-Emphasis is Disabled -1: Pre-Emphasis is Enabled Normal operational mode setting is 0. Power up value is 0

0x05800408 MIPI_DSI_2_DSI2_DSIPHY_LNCK_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_CFG2

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:4	DSIPHY_LPTX_SLEW	LPTX slew rate control To enable or disable LPTX-P and LPTX-N independently during test-mode. In functional mode(test_mode=0) if LPTX_EN is high, both LPTX-P and LPTX-N are on. When test_mode=1 and test_mode_hstx_en=0, DSIPHY_LPTX_SLEW[0] enables/disables LPTX-P for a value of 1/0 respectively, while DSIPHY_LPTX_SLEW[1] enables/disables LPTX-N for a value of 1/0 respectively. Power up value is 00
3:0	DSIPHY_LPRX_DLY	- 3:2 : Escape Clock pulse width adjustment - 1:0 : Escape Clock Delay element. Power up value is 0000

0x0580040C MIPI_DSI_2_DSI2_DSIPHY_LNCK_TEST_DATAPATH

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_TEST_DATAPATH

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	ANE_BYPASS_EN	Enables analog near-end loopback Power up value is 0

MIPI_DSI_2_DSI2_DSIPHY_LNCK_TEST_DATAPATH (cont.)

Bits	Name	Description
6:4	DMUX_LP_SEL	Mux select for testing purposes - 0xx: Mission Mode - 100: LPRX to LPTX - 110: CDRX to LPTX - 111: REG_TEST to LPTX Power up value is 00
3:2	DMUX_HS_SEL	Mux select for testing purposes - 01: PLL_TEST_CLK to HSTX - 11: Adjacent HSRX signal to HSTX Power up value is 00 0x0: Mission Mode
1	TEST_MODE_HSTX_EN	Enable HSTX when test_mode=1: Power up value is 0
0	FORCE_TEST_MODE	When this bit is set to 1, Enable software control bits of lptx, hstx, lprx, or cdrx for testing purposes Power up value is 0

0x05800410 MIPI_DSI_2_DSI2_DSIPHY_LNCK_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_DEBUG_SEL	DSIPHY Data Lane Debug Bus Select Refer to Table at the end of the PHY SWI section to see detailed description of Clock lane debug bus selections: MDP_LVDSPHY_PLL_ANA_STATUS2 **Note 1:** Lane debug bus can be observed only when DSIPHY_GLBL_DIGTOP_DEBUG_SEL[DSIPHY_GLBL_DIGTOP_DEBUG_SEL] is set to 8'bxxxx_x11x **Note 2**: Only 1 lane at a time should be selected. Ensure all other lane debug bus mux select is set to 0. Normal operational mode setting is 0000_0000. Power up value is 0000_0000

0x05800414 MIPI_DSI_2_DSI2_DSIPHY_LNCK_TEST_STR0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_TEST_STR0

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DSIPHY_STR_VALUE_OVERRIDE	- 0: Calibrated value - 1: Strength override value, DSIPHY_LNn_TEST_STR1 Power up value is 0

0x05800418 MIPI_DSI_2_DSI2_DSIPHY_LNCK_TEST_STR1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_TEST_STR1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP	Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT	Power up value is 0000

0x0580041C MIPI_DSI_2_DSI2_DSIPHY_LNCK_BIST_CTL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_BIST_CTL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	MISR_SIG_READ	- 11: Select MISR1 - MISR signature for the valid DATA read from TX FIFO - 10: Select MISR0 - MISR signature for the valid DATA write to TX FIFO - 00 or 01: Select BIST error count Power up value is 00

MIPI_DSI_2_DSI2_DSIPHY_LNCK_BIST_CTL0 (cont.)

Bits	Name	Description
4	MISR_SIG_CLEAR	- 1: Clear both MISR to default signature value 16'hFFFF Power up value is 0
3	RESERVED_BITS3	
2	BIST_RX_PRBS_ERROR_INJECT	- 1: Inject Error pattern into RX checker. Power up value is 0
1	BIST_RX_PRBS_GEN_SHORT	- 1:Pattern length is 2^8 - 0:Pattern is generated continuously until bist_rx_prbs_chk_en is disabled Normal operational mode setting is 0 Power up value is 0
0	DSIPHY_ERROR_CLR	- 1: Clear Error count. Power up value is 0

0x05800420 MIPI_DSI_2_DSI2_DSIPHY_LNCK_BIST_CTL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_BIST_CTL1

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	DSIPHY_HSRX_TERM_EN	- 1: Enable cross termination for HSRX in BIST mode. Power up value is 0
0	DSIPHY_HSRX_EN	- 1: Enable HSRX in BIST mode. Power up value is 0

0x05800424 MIPI_DSI_2_DSI2_DSIPHY_LNCK_RESERVED1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_RESERVED1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800428 MIPI_DSI_2_DSI2_DSIPHY_LNCK_BIST_RXCHK_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_BIST_RXCHK_STATUS

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	CHECK_DONE	READ ONLY. This bit is set when the prbs checker is done for short pattern Power up value is 0
1	RXCHK_HEADER_SEL	READ ONLY. PRBS checker Header sel control signal Power up value is 0
0	RXCHK_PRBS_START	READ ONLY. PRBS checker PRBS START control signal. Power up value is 0

0x0580042C MIPI_DSI_2_DSI2_DSIPHY_LNCK_HSTX_STR_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_HSTX_STR_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_HSTX_STR_HSTOP_STATUS	READ ONLY. Power up value is 0000
3:0	DSIPHY_HSTX_STR_HSBOT_STATUS	READ ONLY. Power up value is 0000

0x05800430 MIPI_DSI_2_DSI2_RESERVED1_PHY_LNCK

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_RESERVED1_PHY_LNCK

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800434 MIPI_DSI_2_DSI2_RESERVED2_PHY_LNCK

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_RESERVED2_PHY_LNCK

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800438 MIPI_DSI_2_DSI2_DSIPHY_LNCK_BIST_MISR_STAT0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_BIST_MISR_STAT0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_7_0	READ ONLY. Power up value is 0000_0000

0x0580043C MIPI_DSI_2_DSI2_DSIPHY_LNCK_BIST_MISR_STAT1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LNCK_BIST_MISR_STAT1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_BISTCHKERR_MISRSIG_15_8	READ ONLY. Power up value is 0000_0000

0x05800440 MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000018

NOTE The preferred name for all global DSIPHY_TIMING_CTRL_n registers is DSIPHY_GLBL_TIMING_CTRL_n.

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_CLK_ZERO	DSIPHY tCLK-ZERO Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0001_1000. Power up value is 0b0001_1000

0x05800444 MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000004

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_CLK_TRAIL	DSIPHY tCLK-TRAIL Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0000_0100. Power up value is 0b0000_0100

0x05800448 MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000007

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_2

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_2 (cont.)

Bits	Name	Description
7:0	DSIPHY_T_CLK_PREPARE	DSIPHY tCLK-PREPARE Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0000_0111. Power up value is 0b0000_0111

0x0580044C MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_3

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800450 MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000008

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_4

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_HS_EXIT	DSIPHY tHS-EXIT Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0000_1000. Power up value is 0b0000_1000

0x05800454 MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000018

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_5

Bits	Name	Description
31:8	RESERVED_BITS31_8	

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_5 (cont.)

Bits	Name	Description
7:0	DSIPHY_T_HS_ZERO	DSIPHY tHS-ZERO Timing Parameter. Due to design implementation limitation, tHS-ZERO has to be set greater than 24 (>24). Set to 24 for typical operation and above 24 when HS settle time need to be expended. Any value set between 0 and 24 will cause un-expected high speed data transfer behavior such as data loss or miss sync pattern. Normal operational mode setting is 0b0001_1000. Note: Each bit increment represents 1UI time delay increment Power up value is 0b0001_1000

0x05800458 MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_6

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000009

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_6

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_HS_PREPARE	DSIPHY tHS-PREPARE Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0000_1001. Power up value is 0b0000_1001

0x0580045C MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_7

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000008

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_7

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_HS_TRAIL	DSIPHY tHS-TRAIL Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0000_1000. Power up value is 0b0000_1000

0x05800460 MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_8

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000001

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_8

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_T_HS_RQST	DSIPHY tHS-RQST Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b0000_0001. Power up value is 0b0000_0001

0x05800464 MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_9

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000013

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_9

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	DSIPHY_T_TA_SURE	DSIPHY tTA-SURE Timing Parameter. Due to design implementation limit, tTA-SURE has to be set greater than 1 (>1). Set to 2 for typical operation and above 2 if bus turn-around time need to be expended. Any value set to 0 or 1 will cause un-expected behavior during bus direction turn around process. NOTE: Power up value must be reconfigured to operational mode setting, i.e., a minimum of 010 Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 010 Power up value is 001
3	RESERVED_BITS3	
2:0	DSIPHY_T_TA_GO	DSIPHY tTA-GO Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 011. Power up value is 011

0x05800468 MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_10

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000004

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_10

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2:0	DSIPHY_T_TA_GET	DSIPHY tTA-GET Timing Parameter Note: Each bit increment represents 1UI time delay increment Normal operational mode setting is 0b100. Power up value is 0b100

0x0580046C MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_11

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_TIMING_CTRL_11

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DSIPHY_TRIG3_CMD	DSIPHY TX Escape Trigger[3] programmable command sequence Normal operational mode setting is 0b0000_0000. Power up value is 0b0000_0000

0x05800470 MIPI_DSI_2_DSI2_DSIPHY_CTRL_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

NOTE : The preferred name for this register is DSIPHY_GLBL_PWR_CFG

MIPI_DSI_2_DSI2_DSIPHY_CTRL_0

Bits	Name	Description
31:7	RESERVED_BITS31_7	

MIPI_DSI_2_DSI2_DSIPHY_CTRL_0 (cont.)

Bits	Name	Description
6	DSIPHY_DIGTOP_PWRDN_B	Digital Control block Power Down. - 1---Normal operation - 0---Digital block power down mode Power up value is 0
5	RESERVED_BITS5	
4	DSIPHY_DLN3_SHUTDOWNB	DSIPHY Data Lane 3 Power Down. 1: Normal operation - 0: Data LN3 NPL Block powerdown Note: Preferred name for *_SHUTDOWNB bits are *_PWRDN_B Normal operational mode setting is 1. Power up value is 0
3	DSIPHY_DLN2_SHUTDOWNB	DSIPHY Data Lane 2 Power Down. - 1: Normal operation - 0: Data LN2 NPL Block powerdown Note: Preferred name for *_SHUTDOWNB bits are *_PWRDN_B Normal operational mode setting is 1. Power up value is 0
2	DSIPHY_CLK_SHUTDOWNB	DSIPHY Clock Lane Power Down. 1: Normal operation - 0: NPL Block powerdown Note: Preferred name for *_SHUTDOWNB bits are *_PWRDN_B Normal operational mode setting is 1. Power up value is 0
1	DSIPHY_DLN1_SHUTDOWNB	DSIPHY Data Lane 1Power Down. - 1: Normal operation - 0: Data LN1 NPL Block powerdown Note: Preferred name for *_SHUTDOWNB bits are *_PWRDN_B Normal operational mode setting is 1. Power up value is 0
0	DSIPHY_DLN0_SHUTDOWNB	DSIPHY Data Lane 0 Power Down. 1: Normal operation - 0: Data LN0 NPL Block powerdown Note: Preferred name for *_SHUTDOWNB bits are *_PWRDN_B Normal operational mode setting is 1. Power up value is 0

0x05800474 MIPI_DSI_2_DSI2_DSIPHY_CTRL_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

NOTE : Preferred name for this register is DSIPHY_GLBL_RESET_CFG

MIPI_DSI_2_DSI2_DSIPHY_CTRL_1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	DSIPHY_SW_RESET	RESET for Digital blocks except control registers. Active high signal. - 1: Assertion - 0: De-assertion Normal operational mode setting is 0. Power up value is 0
6:0	RESERVED_BITS6_0	

0x05800478 MIPI_DSI_2_DSI2_DSIPHY_CTRL_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_CTRL_2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x0580047C MIPI_DSI_2_DSI2_DSIPHY_CTRL_3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000010

MIPI_DSI_2_DSI2_DSIPHY_CTRL_3

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	DSIPHY_BITCLK_HS_SEL	- 0: bitclk from left side, - 1: bitclk from right side Power up value is 1
3:0	RESERVED_BITS3_0	

0x05800480 MIPI_DSI_2_DSI2_DSIPHY_STRENGTH_CTRL_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_STRENGTH_CTRL_0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DSIPHY_STR_LP_N	- 0000: 2-9.5 pF load. - 0010: 9.5-18 pF load - 0100: 18-25 pF load. - 0110: 25-35 pF load. - 1100: 35-65 pF load. - 1111: 65-70 pF load. Operational mode value is 1111 Power up value is 0000
3:0	DSIPHY_STR_LP_P	- 0000: 2-9.5 pF load. - 0010: 9.5-18 pF load - 0100: 18-25 pF load. - 0110: 25-35 pF load. - 1100: 35-65 pF load. - 1111: 65-70 pF load. Operational mode value is 1111 Power up value is 0000

0x05800484 MIPI_DSI_2_DSI2_DSIPHY_STRENGTH_CTRL_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_STRENGTH_CTRL_1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x05800488 MIPI_DSI_2_DSI2_DSIPHY_STRENGTH_CTRL_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

NOTE The preferred name of this register is DSIPHY_GLBL_LPRX_CFG

MIPI_DSI_2_DSI2_DSIPHY_STRENGTH_CTRL_2

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	DSIPHY_LN_CTRL_2	Enable for Low Power Receiver.1: LP RX is enabled -0: LP RX is disabled Note; The preferred name for this register bit should be DSIPHY_LPRX_EN Power up value is 0
1	DSIPHY_LN_CTRL_1	Enable for Contention Detection Receiver.1: CD RX is enabled. -0: CD RX is disabled Note : The preferred name for this register bit should be DSIPHY_CDRX_EN Power up value is 0
0	RESERVED_BITS0	

0x0580048C MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL0

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5	BIST_LP_EN_FIXPAT	send one of selected 32 fixed pattern to LPTD path Power up value is 0
4:3	RESERVED_BITS4_3	
2:1	BIST_TX_PATSEL	selection of 2 bist pattern types. - 01---Fixed Pattern - 1x---Channel Test Pattern - 00---not used Normal operational mode setting is 00. Power up value is 00
0	BIST_EN_TX_PRBS	Power up value is 0

0x05800490 MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL1

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	BIST_TX_TEST_PAT_SEL	selection of channel test pattern generation. - 00 : Medium Frequency Pattern(0011_0011, 1100_1100) - 01 : Low Frequency Pattern(1110_0011, 0001_1100) - 10 : High Frequency Pattern(0101_0101,1010_1010) - 11 : not used Normal operational mode setting is 00. Power up value is 00
4:0	BIST_TX_FIXPAT_SEL	- 32 fixed pattern selection Normal operational mode setting is 00000. Power up value is 00000 <sel> : <bist_fixedpat(7:0)> - 00000: 0000_0101 - 00001: 1111_1010 - 00010: 1111_1111 - 00011: 0000_0000 - 00100: 0011_0011 - 00101: 0101_0101 - 00110: 0001_0001 - 00111: 1110_1110 - 01000: 1111_0100 - 01001: 0000_1010 - 01010: 0000_0110 - 01011: 0111_0111 - 01100: 0001_1100 - 01101: 1110_0011 - 01110: 1100_0001 - 01111: 0011_1110 - 10000: 1111_1010 - 10001: 0000_0101 - 10010: 0000_0000 - 10011: 1111_1111 - 10100: 0011_0011 - 10101: 1010_1010 - 10110: 1110_1110 - 10111: 0001_0001 - 11000: 1111_0100 - 11001: 1111_0100 - 11010: 1111_1001 - 11011: 1000_1000 - 11100: 1110_0011 - 11101: 1110_0011 - 11110: 1100_0001 - 11111: 1100_0001

0x05800494 MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000B1

MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL2

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BIST_PRBS_POLY	full programable prbs pattern. Default pattern is 1 + x4 + x5 + x7 Normal operational mode setting is 1011_0001 Power up value is 1011_0001

0x05800498 MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000FF

MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL3

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BIST_PRBS_SEED	rx data seed to compare w/ input data and start rx side prbs gen (tx_prbs_seed_sel has to be set to 1) Invalid values: 0x00 and 0x1F Normal operational mode setting is 1111_1111 Power up value is 1111_1111

0x0580049C MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL4

Bits	Name	Description
31:5	RESERVED_BITS31_5	

MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL4 (cont.)

Bits	Name	Description
4	DSIPHY_BIST_LNCK_HS_REQUEST	DSIPHY_BIST_LNCK_HS_REQUEST set to 1 and any of DSIPHY_BIST_SEL[3:0] being set, starts Clock lane TX request for Clock lane HS data transition sequence. Prior to setting this bit, any of DSIPHY_BIST_SEL[3:0] must be set for at least 3 ESCCLK cycles Normal operational mode setting is 0. Power up value is 0
3:0	DSIPHY_BIST_SEL	DSIPHY_BIST_SEL<i> set to one indicates the data lane is enabled for PHY BIST. Any one of the data lane bist_sel is on will automatically enable the clock lane. Default is set to zero, data lane will be enabled by controller. Note: for 45nm, data lane enable must go through DSI controller software control register. DSIPHY_BIST_SEL only indicates the HS TX byte data either from BIST pattern generator or from controller. For 28nm, DSIPH_BIST_SEL[3:0] os OR-ed with lane enable control driven by controller to eliminate the dependence to controller for PHY BIST. Normal operational mode setting is 0000. Power up value is 0000

0x058004A0 MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_BIST_CTRL5

Bits	Name	Description
31:4	RESERVED_BITS31_4	
3:0	BIST_RX_PRBS_CHK_EN	bist_rx_prbs_chk_en<i> is BIST prbs checker enable for each data lane. <0> enable DL0 checker, <1> enable DL1, <2> enable DL2 checker, <3> enable DL3. To enable bist check must to make sure en_tx_prbs is set to 0. (rx checker state machine start to set header sel to high, patgen start to send header).It also goes to pad_dataln as hsrx_en.Setting this bit to high also turns the high speed receiver on. each receiver lane has its own BIST PRBS checker. Normal operational mode setting is 0000. Power up value is 0000

0x058004A4 MIPI_DSI_2_DSI2_DSIPHY_GLBL_MISR_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_GLBL_MISR_CTRL

Bits	Name	Description
31:4	RESERVED_BITS31_4	
3:0	DSIPHY_MISR_EN	DSIPHY_MISR_en<i> is MISR enable for each data lane <i>. Power up value is 0000

0x058004A8 MIPI_DSI_2_DSI2_DSIPHY_GLBL_TEST_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_GLBL_TEST_CTRL

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6	TEST_ESC_CLK_SEL	-0: Mission mode. Select escclk from mmss_cc -1: escclk from test refclk div2. Power up value is 0
5:4	TEST_BYTECLK_SEL	- 00 : Mission mode. Select bytclk from cc - 01: Tied to ground. - 10 : byteclk from test byteclk1. - 11: byteclk from test byteclk 2. Power up value is 00
3	RESERVED_BITS3	
2:1	PLL_TEST_MODE_SEL	- 00: send bitclk to clock lane pad - 01: send the byteclk to clock lane pad - 10: send escclk to clock lane pad - 11: send the pn_rxhs_clk to clock lane pad Power up value is 00
0	DSIPHY_PLL_TESTMODE	Power up value is 0

0x058004AC MIPI_DSI_2_DSI2_DSIPHY_GLBL_DIGTOP_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_GLBL_DIGTOP_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DIGTOP_DEBUG_SEL	Refer to Table at the end of the PHY SWI section to see detailed description of digital top debug bus selections.

0x058004B0 MIPI_DSI_2_DSI2_DSIPHY_LDO_CNTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_LDO_CNTRL

Bits	Name	Description
31:6	RESERVED_BITS31_6	

MIPI_DSI_2_DSI2_DSIPHY_LDO_CNTRL (cont.)

Bits	Name	Description
5:3	LDO_VREF_SEL	DSIPHY Regulator Reference Select. Selects the value of reference voltage for the DSIPHY LDO Regulator. When LDO_VREF_DIV_EN = 1 - 000 : 0.400V - 001 : 0.415V - 010 : 0.385V - 011 : 0.370V - 100 : 0.430V - 101 : 0.445V - 110 : 0.460V - 111 : 0.475V When LDO_VREF_CGM_EN = 1 - 000 : 0.400V - 001 : 0.415V - 010 : 0.385V - 011 : 0.370V - 100 : 0.430V - 101 : 0.430V - 110 : 0.430V - 111 : 0.430V Note: LDO_VREF_CGM_EN and LDO_VREF_DIV_EN both cannot be 1. Setting both to 1 will disable both CGM_EN and DIV_EN Normal operational mode setting is 000 Power up value is 000
2	LDO_VREF_DIV_EN	To enable resistor divider as reference voltage Power up value is 0
1	LDO_VREF_CGM_EN	To enable Constant Gm as reference voltage Power up value is 0
0	LDO_MODE_EN	LDO Mode. DSIPHY Regulator Enable. - 1: DSIPHY Regulator is enabled. - 0: DSIPHY Regulator is disabled. Normal operational mode setting is 0. DSIPHY_REGULATOR_CTRL_0[DSIPHY_REG_EN] must be set to 0 when LDO_MODE_EN is set to 1 Power up value is 0

0x058004B4 MIPI_DSI_2_DSI2_DSIPHY_DEBUG_RESERVED0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_DEBUG_RESERVED0

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x058004B8 MIPI_DSI_2_DSI2_DSIPHY_DEBUG_RESERVED1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_DEBUG_RESERVED1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x058004BC MIPI_DSI_2_DSI2_DSIPHY_DEBUG_RESERVED2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_DEBUG_RESERVED2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x058004C0 MIPI_DSI_2_DSI2_DSIPHY_GLBL_STATUS_DEBUG_BUS0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_GLBL_STATUS_DEBUG_BUS0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DEBUG_BUS_7_0	

0x058004C4 MIPI_DSI_2_DSI2_DSIPHY_GLBL_STATUS_DEBUG_BUS1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_GLBL_STATUS_DEBUG_BUS1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DEBUG_BUS_15_8	

0x058004C8 MIPI_DSI_2_DSI2_DSIPHY_GLBL_STATUS_DEBUG_BUS2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_GLBL_STATUS_DEBUG_BUS2

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DEBUG_BUS_23_16	

0x058004CC MIPI_DSI_2_DSI2_DSIPHY_GLBL_STATUS_DEBUG_BUS3

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

MIPI_DSI_2_DSI2_DSIPHY_GLBL_STATUS_DEBUG_BUS3

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DEBUG_BUS_31_24	

14.9 HDMI TX Registers (0x04A00000 HDMI_TX_BASE)

This section contains the HDMI TX registers.

0x04A00000 HDMI_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000002

HDMI block control

HDMI_CTRL

Bits	Name	Description
31:21	RESERVED_1	
20	RB_SWITCH_EN	Switch Red and Blue encoding position on TMDS output
19:3	RESERVED_2	
2	ENC_REQUIRED	- 1=Encryption required on TMDS output - 0=Encryption NOT required on TMDS output Bit has NO effect once HDCP is enabled since cipher will encrypt data
1	HDMI_DVI_SEL	- 0=DVI, 1=HDMI
0	ENABLE	- 0= Disable HDMI block, 1= Enable HDMI block 0x0: Disable 0x1: Enable

0x04A00018 HDMI_PKT_BLK_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000011

HDMI Packet Block Control

HDMI_PKT_BLK_CTRL

Bits	Name	Description
31:30	RESERVED_1	
29:16	H_CNT_OVERRIDE_VAL	H_CNT value to use if H_CNT_OVERRIDE_EN=1
15:10	RESERVED_2	

HDMI_PKT_BLK_CTRL (cont.)

Bits	Name	Description
9	ERROR_MASK	Set to 1 to enable hdmi error interrupt
8	ERROR_ACK	WRITE ONLY. Write 1 to clear error status.
7	RESERVED_3	
6	H_CNT_OVERRIDE_EN	Set to '1' to override hardware-computed H_COUNT value with value in register 0x0: Disable 0x1: Enable
5	RESERVED_4	
4	PKT_GEN_VERSION	Select which version of packet generation to use 0x0: Older Version, fill only the Vblank with data island (Debug only) 0x1: Fill blank with data islands
3:1	RESERVED	
0	KEEPOUT_MODE	Select which KEEPOUT mode after VSYNC when PKT_GEN_VERSION field is set to 1 0x0: No new packets (except GC is sent between rising edge of VSYNC and 650 pixels after rising edge of VSYNC.) 0x1: No packet is sent between 509 to 650 pixels after rising edge of VSYNC

0x04A0001C HDMI_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Status Fields

HDMI_STATUS

Bits	Name	Description
31:28	RESERVED_1	
27	ERROR_INT	READ ONLY. HDMI error status flag is a masked OR of audio packet error, vbi packet error and audio fifo overflow.
26:21	RESERVED_2	
20	VBI_PKT_ERROR	READ ONLY. Indicates that VBI packet transmission was interrupted. Possible causes include audio packet transmission start, in which case the number of VBI packets on a line must be reduced, or overlapping VBI packets with active video, in which case the VBI line number selection must be adjusted to put the data on a vertical blank line.

HDMI_STATUS (cont.)

Bits	Name	Description
19:17	RESERVED_3	
16	AUDIO_PKT_ERROR	READ ONLY. Indicates that audio packet transmission was interrupted. Possible causes include video or VBI transmission start, in which case AUDIO_PACKETS_PER_LINE must be reduced or the pixel rate increased.
15:1	RESERVED_4	
0	ACTIVE_AVMUTE	READ ONLY. Active copy HDMI_GC.AVMUTE field. Active copy is updated on a framestart.

0x04A00020 HDMI_AUDIO_PKT_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000010

HDMI Audio Packet Control

HDMI_AUDIO_PKT_CTRL

Bits	Name	Description
31	RESERVED_1	
26	CS_60958_UPDATE	Write 1 to atomically update double-buffered 60958 Channel Status registers on next 60958 frame start
25:21	RESERVED_2	
20:16	AUDIO_PKTS_PER_LINE	Set the number of audio packets to transmit per line. Must be set to allow more than the number of samples received per line of video to be transmitted, and less than or equal to the maximum number of packets that can be transmitted per line (see HDMI functional description for equations to calculate max and min values). (Only used with HDMI_CTRL.PKT_GEN_VERSION=0; 'dont_care' otherwise)
15	RESERVED_3	
14	AUDIO_TEST_MODE	- 0 selects random number data; 1 selects ramp generator data 0x0: Disable 0x1: Enable
13	RESERVED_4	
12	AUDIO_TEST_EN	Set to 1 to send test data instead of audio samples from Audio block. The TMDS random number generator has to be enabled to generate the random samples. 0x0: Disable 0x1: Enable

HDMI_AUDIO_PKT_CTRL (cont.)

Bits	Name	Description
11:9	RESERVED_5	
8	RESERVED_6	
5:4	AUDIO_DELAY_EN	Select min audio delay after end of video line. 0x0: No delay beyond minimum required 0x1: 58 clocks 0x2: 56 clocks 0x3: Reserved
3:1	RESERVED	
0	AUDIO_SAMPLE_SEND	Set to 1 to enable transmission of Audio packets. Packet transmission begins on the next frame. 0x0: Disable Audio Packet Transmission 0x1: Enable Audio Packet Transmission

0x04A00024 HDMI_ACR_PKT_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00010000

HDMI Audio Clock Regen Packet Control

HDMI_ACR_PKT_CTRL

Bits	Name	Description
31	AUDIO_PRIORITY	ACR and audio sample packet priority 0x0: ACR packet has higher priority than AUDIO sample packet 0x1: AUDIO sample packet has higher priority than ACR packet
30:19	RESERVED_1	
18:16	N_MULTIPLE	ACR N multiple to use when SELECT filed not=0 0x0: reserved_1 0x1: x1 0x2: x2 0x3: reserved_2 0x4: x4 0x5: reserved_3 0x6: reserved_4 0x7: reserved_5
15:13	RESERVED_2	

HDMI_ACR_PKT_CTRL (cont.)

Bits	Name	Description
12	AUTO_SEND	Set to 1 to enable hardware transmission of ACR packets when new CTS value is available. Also causes CTS value to be zeroed out when an ACR packet is transmitted and no new CTS value is available. 0x0: Disable 0x1: Enable
11:9	RESERVED_3	
8	SOURCE	Select source for N and CTS values for audio clock regeneration. 0x0: Use hardware-generated CTS value 0x1: Use CTS value selected (based on audio sample rate from set written by software)
7:6	RESERVED_4	
5:4	SELECT	Select which N/CTS combination to use for ACR packet transmission. 0x0: Hardware Selected 0x1: ACR_32 0x2: ACR_44 0x3: ACR_48
3:2	RESERVED	
1	CONT	Determine whether to send Audio Clock Regeneration packet(s) once or every frame. 0x0: Disable Audio Clock Regeneration Packet Transmission 0x1: Enable Audio Clock Regeneration Packet Transmission
0	SEND	Set to 1 to enable transmission of Audio Clock Regeneration packets. Packet transmission begins when audio is enabled. 0x0: Disable Audio Clock Regeneration Packet Transmission 0x1: Enable Audio Clock Regeneration Packet Transmission

0x04A00028 HDMI_VBI_PKT_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00002000

HDMI Null, General Control and ISRC Packet Control

HDMI_VBI_PKT_CTRL

Bits	Name	Description
31:30	RESERVED_1	
29:24	ACP_LINE	Select line number to send ACP packet on.

HDMI_VBI_PKT_CTRL (cont.)

Bits	Name	Description
23:22	RESERVED_2	
21:16	ISRC_LINE	Select line number to send ISRC packets on.
15:14	RESERVED_3	
13	ACP_SOURCE	Select source for ACP packet 0x0: Audio block (Memory) 0x1: HDMI registers (written by software)
12	ACP_SEND	Set to 1 to enable transmission of Audio Content Protection packets. The ACP packet is sent in every frame when it is enabled. 0x0: Disable Audio Content Protection Packet Transmission 0x1: Enable Audio Content Protection Packet Transmission
11:10	RESERVED_4	
9	ISRC_CONT	Determine whether to send ISRC packet(s) once or every frame. 0x0: Send ISRC Packet on next frame only 0x1: Send ISRC Packet on every frame
8	ISRC_SEND	Set to 1 to enable transmission of ISRC packet(s). Packet transmission begins on the next frame. 0x0: Disable ISRC Packet Transmission 0x1: Enable ISRC Packet Transmission
7:6	RESERVED_5	
5	GC_CONT	Determine whether to send General Control packet(s) once or every frame. 0x0: Send General Control Packet on next frame only 0x1: Send General Control Packet on every frame
4	GC_SEND	Set to 1 to enable transmission of General Control packet(s). Packet transmission begins on the next frame. 0x0: Disable General Control Packet Transmission 0x1: Enable General Control Packet Transmission
3:1	RESERVED_6	
0	NULL_SEND	Set to 1 to enable transmission of Null packets to ensure maximum time between packet transmission' requirement is met. Null packets are inserted on line 2 if no other packet types are enabled for that line. (Only used with HDMI_CTRL.PKT_GEN_VERSION=0; don't_care otherwise) 0x0: Disable Null Packet Transmission 0x1: Enable Null Packet Transmission

0x04A0002C HDMI_INFOFRAME_CTRL0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000040

HDMI InfoFrame Packet Control

HDMI_INFOFRAME_CTRL0

Bits	Name	Description
31:14	RESERVED_1	
13	VENSPEC_INFO_CONT	Determine whether to send Vendor specific InfoFrame packet(s) once or every frame. 0x0: Send Vendor Specific InfoFrame Packet on next frame only 0x1: Send Vendor Specific InfoFrame Packet on every frame
12	VENSPEC_INFO_SEND	Set to 1 to enable transmission of Vendor specific InfoFrame packets. Packet transmission begins on the next frame. 0x0: Disable Vendor Specific InfoFrame Packet Transmission 0x1: Enable Vendor Specific InfoFrame Packet Transmission
11	RESERVED_2	
10	RESERVED_3	
9	RESERVED_4	
8	RESERVED_5	
7	AUDIO_INFO_UPDATE	Write 1 to automatically update double-buffered AUDIO_INFO registers on next frame / field start
6	AUDIO_INFO_SOURCE	Select source for Audio information fields which can be controlled by hardware. 0x0: Audio block 0x1: HDMI registers (written by software)
5	AUDIO_INFO_CONT	Determine whether to send Audio InfoFrame packet(s) once or every frame. 0x0: Send Audio InfoFrame Packet on next frame only 0x1: Send Audio InfoFrame Packet on every frame
4	AUDIO_INFO_SEND	Set to 1 to enable transmission of Audio InfoFrame packets. Packet transmission begins on the next frame. 0x0: Disable Audio InfoFrame Packet Transmission 0x1: Enable Audio InfoFrame Packet Transmission
3:2	RESERVED_6	
1	AVI_INFO_CONT	Determine whether to send AVI InfoFrame packet(s) once or every frame. 0x0: Send AVI InfoFrame Packet on next frame only 0x1: Send AVI InfoFrame Packet on every frame

HDMI_INFOFRAME_CTRL0 (cont.)

Bits	Name	Description
0	AVI_INFO_SEND	Set to 1 to enable transmission of AVI InfoFrame packets. Packet transmission begins on the next frame. 0x0: Disable AVI InfoFrame Packet Transmission 0x1: Enable AVI InfoFrame Packet Transmission

0x04A00030 HDMI_INFOFRAME_CTRL1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI InfoFrame Packet Control

HDMI_INFOFRAME_CTRL1

Bits	Name	Description
31:30	RESERVED_1	
29:24	VENSPEC_INFO_LINE	Select line number to send Vendor Specific InfoFrame packets on.
23:22	RESERVED_2	
21:16	RESERVED_3	
13:8	AUDIO_INFO_LINE	Select line number to send Audio InfoFrame packets on.
7:6	RESERVED_4	
5:0	AVI_INFO_LINE	Select line number to send AVI InfoFrame packets on.

0x04A00034 HDMI_GEN_PKT_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic Packet Control

HDMI_GEN_PKT_CTRL

Bits	Name	Description
31:30	RESERVED_1	
29:24	GENERIC1_LINE	Select line number to send Generic1 packets on.
23:22	RESERVED_2	
21:16	GENERIC0_LINE	Select line number to send Generic0 packets on.

HDMI_GEN_PKT_CTRL (cont.)

Bits	Name	Description
15:6	RESERVED_3	
5	GENERIC1_CONT	Determine whether to send Generic1 packet(s) once or every frame. 0x0: Send Generic1 Packet on next frame only 0x1: Send Generic1 Packet on every frame
4	GENERIC1_SEND	Set to 1 to enable transmission of Generic1 packets. Packet transmission begins on the next frame. 0x0: Disable Generic1 Packet Transmission 0x1: Enable Generic1 Packet Transmission
3	RESERVED_4	
2	GENERIC0_UPDATE	Write 1 to automatically update double-buffered HDMI_GENERIC_0 registers on next frame / field start
1	GENERIC0_CONT	Determine whether to send Generic0 packet(s) once or every frame. 0x0: Send Generic0 Packet on next frame only 0x1: Send Generic0 Packet on every frame
0	GENERIC0_SEND	Set to 1 to enable transmission of Generic0 packets. Packet transmission begins on the next frame. 0x0: Disable Generic0 Packet Transmission 0x1: Enable Generic0 Packet Transmission

0x04A0003C HDMI_ACP

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Audio Content Protection Packet Contents

HDMI_ACP

Bits	Name	Description
31:24	RESERVED_1	
23:16	TYPE_DEPENDENT_BYTE1	Bytes 1 of the body of the ACP packet
15:8	TYPE_DEPENDENT_BYTE0	Bytes 0 of the body of the ACP packet
7:2	RESERVED_2	
1:0	TYPE	ACP type for the ACP header

0x04A00040 HDMI_GC

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI General Control Packet Contents

HDMI_GC

Bits	Name	Description
31:13	RESERVED_1	
12	GC_DEFAULT	This field is used to program the Default field for deep color in GC packet.
11:8	GC_PP	This field is used to program the Pixel Packing Phase for deep color in GC packet.
7:4	GC_CD	This field is used to program the Color Depth for deep color in GC packet.
3:1	RESERVED_2	
0	AVMUTE	AVMUTE field for GC packet.

0x04A00044 HDMI_AUDIO_PKT_CTRL2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000011

HDMI Packet Control 2

HDMI_AUDIO_PKT_CTRL2

Bits	Name	Description
31:12	RESERVED_1	
11:8	RESERVED_2	
4	RESERVED_3	
1	LAYOUT_SEL	Layout select used when LAYOUT_OVRD = 1
0	RESERVED_4	

0x04A00048 HDMI_ISRC1_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ISRC1 Packet Header Contents

HDMI_ISRC1_0

Bits	Name	Description
31:8	RESERVED_1	
7	ISRC_VALID	Set this bit only when data located in ISRC_Status field and UPC_EAN_ISRC_xx field are valid. When source cannot obtain complete data for these fields, ISRC_Valid may be 0.
6	ISRC_CONTINUE	If subsequent ISRC2 packet is transmitted, set this field =1 else set = 0.
5:3	RESERVED_2	
2:0	ISRC_STATUS	This field needs to be set according to the DVD specifications for Read-only Disc, Part4. refer to HDMI Spec for more details

0x04A0004C HDMI_ISRC1_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ISRC1 Packet Body Contents

HDMI_ISRC1_1

Bits	Name	Description
31:24	UPC_EAN_ISRC3	UPC/EAN or ISRC byte 3
23:16	UPC_EAN_ISRC2	UPC/EAN or ISRC byte 2
15:8	UPC_EAN_ISRC1	UPC/EAN or ISRC byte 1
7:0	UPC_EAN_ISRC0	UPC/EAN or ISRC byte 0

0x04A00050 HDMI_ISRC1_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ISRC1 Packet Body Contents, cont'd

HDMI_ISRC1_2

Bits	Name	Description
31:24	UPC_EAN_ISRC7	UPC/EAN or ISRC byte 7
23:16	UPC_EAN_ISRC6	UPC/EAN or ISRC byte 6
15:8	UPC_EAN_ISRC5	UPC/EAN or ISRC byte 5
7:0	UPC_EAN_ISRC4	UPC/EAN or ISRC byte 4

0x04A00054 HDMI_ISRC1_3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ISRC1 Packet Body Contents, cont'd

HDMI_ISRC1_3

Bits	Name	Description
31:24	UPC_EAN_ISRC11	UPC/EAN or ISRC byte 11
23:16	UPC_EAN_ISRC10	UPC/EAN or ISRC byte 10
15:8	UPC_EAN_ISRC9	UPC/EAN or ISRC byte 9
7:0	UPC_EAN_ISRC8	UPC/EAN or ISRC byte 8

0x04A00058 HDMI_ISRC1_4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ISRC1 Packet Body Contents, cont'd

HDMI_ISRC1_4

Bits	Name	Description
31:24	UPC_EAN_ISRC15	UPC/EAN or ISRC byte 15
23:16	UPC_EAN_ISRC14	UPC/EAN or ISRC byte 14
15:8	UPC_EAN_ISRC13	UPC/EAN or ISRC byte 13
7:0	UPC_EAN_ISRC12	UPC/EAN or ISRC byte 12

0x04A0005C HDMI_ISRC2_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ISRC2 Packet Body Contents

HDMI_ISRC2_0

Bits	Name	Description
31:24	UPC_EAN_ISRC19	UPC/EAN or ISRC byte 19
23:16	UPC_EAN_ISRC18	UPC/EAN or ISRC byte 18
15:8	UPC_EAN_ISRC17	UPC/EAN or ISRC byte 17
7:0	UPC_EAN_ISRC16	UPC/EAN or ISRC byte 16

0x04A00060 HDMI_ISRC2_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ISRC2 Packet Body Contents, cont'd

HDMI_ISRC2_1

Bits	Name	Description
31:24	UPC_EAN_ISRC23	UPC/EAN or ISRC byte 23
23:16	UPC_EAN_ISRC22	UPC/EAN or ISRC byte 22
15:8	UPC_EAN_ISRC21	UPC/EAN or ISRC byte 21
7:0	UPC_EAN_ISRC20	UPC/EAN or ISRC byte 20

0x04A00064 HDMI_ISRC2_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ISRC2 Packet Body Contents, cont'd

HDMI_ISRC2_2

Bits	Name	Description
31:24	UPC_EAN_ISRC27	UPC/EAN or ISRC byte 27
23:16	UPC_EAN_ISRC26	UPC/EAN or ISRC byte 26
15:8	UPC_EAN_ISRC25	UPC/EAN or ISRC byte 25
7:0	UPC_EAN_ISRC24	UPC/EAN or ISRC byte 24

0x04A00068 HDMI_ISRC2_3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ISRC2 Packet Body Contents, cont'd

HDMI_ISRC2_3

Bits	Name	Description
31:24	UPC_EAN_ISRC31	UPC/EAN or ISRC byte 31
23:16	UPC_EAN_ISRC30	UPC/EAN or ISRC byte 30
15:8	UPC_EAN_ISRC29	UPC/EAN or ISRC byte 29
7:0	UPC_EAN_ISRC28	UPC/EAN or ISRC byte 28

0x04A0006C HDMI_AVI_INFO0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI AVI InfoFrame Packet Body Contents. Please refer to CEA_861-D/E/F, spec for more details on the fields

HDMI_AVI_INFO0

Bits	Name	Description
31	IT_CONTENT	IT content indicating picture is composed according to common IT practices
30:28	EXTENDED_COLORIMETRY	extended colorimetery bits that describe optional encodings
27:26	QUANTIZATION	Indicates current quantization range corresponds to default range

HDMI_AVI_INFO0 (cont.)

Bits	Name	Description
25:24	NON_UNIFORM_SCALE	Non uniform picture scaling for AVI info packet SC0 and SC1 fields
23:22	COLORIMETRY	Colorimetry field AVI info packet C0, C1 fields
21:20	PICTURE_ASPECT_RATIO	Picture aspect ratio for AVI info packet M0, M1 fields
19:16	ACTIVE_FORMAT_RATIO	Active format Aspect ratio for AVI info packet R0..R3 fields
15	PB1_RSVD	Reserved Bit
14:13	RGB_OR_YCBCR	RGB to YCbCr indicator for AVI info packet Y0, Y1 fields 0x0: RGB 0x1: YCbCr 4:2:2 0x2: YCbCr 4:4:4 0x3: Reserved
12	ACTIVE_INFO_PRES	Active information present for AVI info packet A field
11:10	BAR_INFO	Bar info data valid for AVI info packet B field
9:8	SCAN_INFO	Scan information for AVI info packet S field.
7:0	CHECKSUM	Checksum

0x04A00070 HDMI_AVI_INFO1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI AVI InfoFrame Packet Body Contents, Cont'd, Please refer to CEA_861-D/E/F, spec for more details on the fields

HDMI_AVI_INFO1

Bits	Name	Description
31:16	TOP	Upper and Lower byte for the line number of End of TOP bar in AVI info Packet
15:12	PB5_RSVD	Packet byte 5, bits[7:5] reserved bits for AVI info frame packet
11:8	PR	Pixel repetition factor fields for AVI info packet. Do not use for infoframe version 1
7	PB4_RSVD	Packet byte 4 bit [7] reserved bit for AVI infoframe packet
6:0	VIC	Video format Identification fields for AVI info packet, Do not use for infoframe version 1

0x04A00074 HDMI_AVI_INFO2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI AVI InfoFrame Packet Body Contents, Cont'd, Please refer to CEA_861-D/E/F, spec for more details on the fields

HDMI_AVI_INFO2

Bits	Name	Description
31:16	LEFT	Upper and Lower byte for the line number of End of LEFT bar in AVI info Packet
15:0	BOTTOM	Upper and Lower byte for the line number of Start of BOTTOM bar in AVI info Packet

0x04A00078 HDMI_AVI_INFO3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x02000000

HDMI AVI InfoFrame Packet Body Contents, Cont'd, Please refer to CEA_861-D/E/F, spec for more details on the fields

HDMI_AVI_INFO3

Bits	Name	Description
31:24	VERSION	AVI infoframe version number.
23:16	RESERVED	
15:0	RIGHT	Upper and Lower byte for the line number of Start of RIGHT bar in AVI info Packet

0x04A00084 HDMI_GENERIC0_HDR

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic0 Packet Header

HDMI_GENERIC0_HDR

Bits	Name	Description
31:24	RESERVED	
23:16	HB2	HDMI Generic0 Packet Header Byte 2
15:8	HB1	HDMI Generic0 Packet Header Byte 1
7:0	HB0	HDMI Generic0 Packet Header Byte 0

0x04A00088 HDMI_GENERIC0_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic0 Packet Body Contents

HDMI_GENERIC0_0

Bits	Name	Description
31:24	BYTE3	HDMI Generic0 Packet Body Byte 3
23:16	BYTE2	HDMI Generic0 Packet Body Byte 2
15:8	BYTE1	HDMI Generic0 Packet Body Byte 1
7:0	BYTE0	HDMI Generic0 Packet Body Byte 0

0x04A0008C HDMI_GENERIC0_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic0 Packet Body Contents, Cont'd

HDMI_GENERIC0_1

Bits	Name	Description
31:24	BYTE7	HDMI Generic0 Packet Body Byte 7
23:16	BYTE6	HDMI Generic0 Packet Body Byte 6
15:8	BYTE5	HDMI Generic0 Packet Body Byte 5
7:0	BYTE4	HDMI Generic0 Packet Body Byte 4

0x04A00090 HDMI_GENERIC0_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic0 Packet Body Contents, Cont'd

HDMI_GENERIC0_2

Bits	Name	Description
31:24	BYTE11	HDMI Generic0 Packet Body Byte 11
23:16	BYTE10	HDMI Generic0 Packet Body Byte 10
15:8	BYTE9	HDMI Generic0 Packet Body Byte 9
7:0	BYTE8	HDMI Generic0 Packet Body Byte 8

0x04A00094 HDMI_GENERIC0_3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic0 Packet Body Contents, Cont'd

HDMI_GENERIC0_3

Bits	Name	Description
31:24	BYTE15	HDMI Generic0 Packet Body Byte 15
23:16	BYTE14	HDMI Generic0 Packet Body Byte 14
15:8	BYTE13	HDMI Generic0 Packet Body Byte 13
7:0	BYTE12	HDMI Generic0 Packet Body Byte 12

0x04A00098 HDMI_GENERIC0_4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic0 Packet Body Contents, Cont'd

HDMI_GENERIC0_4

Bits	Name	Description
31:24	BYTE19	HDMI Generic0 Packet Body Byte 19
23:16	BYTE18	HDMI Generic0 Packet Body Byte 18
15:8	BYTE17	HDMI Generic0 Packet Body Byte 17
7:0	BYTE16	HDMI Generic0 Packet Body Byte 16

0x04A0009C HDMI_GENERIC0_5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic0 Packet Body Contents, Cont'd

HDMI_GENERIC0_5

Bits	Name	Description
31:24	BYTE23	HDMI Generic0 Packet Body Byte 23
23:16	BYTE22	HDMI Generic0 Packet Body Byte 22
15:8	BYTE21	HDMI Generic0 Packet Body Byte 21
7:0	BYTE20	HDMI Generic0 Packet Body Byte 20

0x04A000A0 HDMI_GENERIC0_6

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic0 Packet Body Contents, Cont'd

HDMI_GENERIC0_6

Bits	Name	Description
31:24	BYTE27	HDMI Generic0 Packet Body Byte 27
23:16	BYTE26	HDMI Generic0 Packet Body Byte 26
15:8	BYTE25	HDMI Generic0 Packet Body Byte 25
7:0	BYTE24	HDMI Generic0 Packet Body Byte 24

0x04A000A4 HDMI_GENERIC1_HDR

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic1 Packet Header

HDMI_GENERIC1_HDR

Bits	Name	Description
31:24	RESERVED	
23:16	HB2	HDMI Generic1 Packet Header Byte 2
15:8	HB1	HDMI Generic1 Packet Header Byte 1
7:0	HB0	HDMI Generic1 Packet Header Byte 0

0x04A000A8 HDMI_GENERIC1_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic1 Packet Body Contents

HDMI_GENERIC1_0

Bits	Name	Description
31:24	BYTE3	HDMI Generic1 Packet Body Byte 3
23:16	BYTE2	HDMI Generic1 Packet Body Byte 2
15:8	BYTE1	HDMI Generic1 Packet Body Byte 1
7:0	BYTE0	HDMI Generic1 Packet Body Byte 0

0x04A000AC HDMI_GENERIC1_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic1 Packet Body Contents, Cont’d

HDMI_GENERIC1_1

Bits	Name	Description
31:24	BYTE7	HDMI Generic1 Packet Body Byte 7
23:16	BYTE6	HDMI Generic1 Packet Body Byte 6
15:8	BYTE5	HDMI Generic1 Packet Body Byte 5
7:0	BYTE4	HDMI Generic1 Packet Body Byte 4

0x04A000B0 HDMI_GENERIC1_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic1 Packet Body Contents, Cont'd

HDMI_GENERIC1_2

Bits	Name	Description
31:24	BYTE11	HDMI Generic1 Packet Body Byte 11
23:16	BYTE10	HDMI Generic1 Packet Body Byte 10
15:8	BYTE9	HDMI Generic1 Packet Body Byte 9
7:0	BYTE8	HDMI Generic1 Packet Body Byte 8

0x04A000B4 HDMI_GENERIC1_3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic1 Packet Body Contents, Cont'd

HDMI_GENERIC1_3

Bits	Name	Description
31:24	BYTE15	HDMI Generic1 Packet Body Byte 15
23:16	BYTE14	HDMI Generic1 Packet Body Byte 14
15:8	BYTE13	HDMI Generic1 Packet Body Byte 13
7:0	BYTE12	HDMI Generic1 Packet Body Byte 12

0x04A000B8 HDMI_GENERIC1_4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic1 Packet Body Contents, Cont'd

HDMI_GENERIC1_4

Bits	Name	Description
31:24	BYTE19	HDMI Generic1 Packet Body Byte 19
23:16	BYTE18	HDMI Generic1 Packet Body Byte 18
15:8	BYTE17	HDMI Generic1 Packet Body Byte 17
7:0	BYTE16	HDMI Generic1 Packet Body Byte 16

0x04A000BC HDMI_GENERIC1_5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic1 Packet Body Contents, Cont'd

HDMI_GENERIC1_5

Bits	Name	Description
31:24	BYTE23	HDMI Generic1 Packet Body Byte 23
23:16	BYTE22	HDMI Generic1 Packet Body Byte 22
15:8	BYTE21	HDMI Generic1 Packet Body Byte 21
7:0	BYTE20	HDMI Generic1 Packet Body Byte 20

0x04A000C0 HDMI_GENERIC1_6

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Generic1 Packet Body Contents, Cont'd

HDMI_GENERIC1_6

Bits	Name	Description
31:24	BYTE27	HDMI Generic1 Packet Body Byte 27
23:16	BYTE26	HDMI Generic1 Packet Body Byte 26
15:8	BYTE25	HDMI Generic1 Packet Body Byte 25
7:0	BYTE24	HDMI Generic1 Packet Body Byte 24

0x04A000C4 HDMI_ACR_32_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ACR values for 32 kHz sample rate

HDMI_ACR_32_0

Bits	Name	Description
31:12	CTS_32	CTS value for 32 kHz audio sample rate
11:1	RESERVED	
0	CTS_32_FRAC	CTS fractional value for 32 KHz audio sample rate

0x04A000C8 HDMI_ACR_32_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ACR values for 32 kHz sample rate

HDMI_ACR_32_1

Bits	Name	Description
31:20	RESERVED	
19:0	N_32	N value for 32 kHz audio sample rate

0x04A000CC HDMI_ACR_44_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ACR values for 44.1 kHz sample rate & multiples

HDMI_ACR_44_0

Bits	Name	Description
31:12	CTS_44	CTS value for 44.1 kHz audio sample rate
11:0	RESERVED	

0x04A000D0 HDMI_ACR_44_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ACR values for 44.1 kHz sample rate & multiples

HDMI_ACR_44_1

Bits	Name	Description
31:20	RESERVED	
19:0	N_44	N value for 44.1 kHz audio sample rate

0x04A000D4 HDMI_ACR_48_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ACR values for 48 kHz sample rate & multiples

HDMI_ACR_48_0

Bits	Name	Description
31:12	CTS_48	CTS value for 48 kHz audio sample rate
11:0	RESERVED	

0x04A000D8 HDMI_ACR_48_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI ACR values for 48 kHz sample rate & multiples

HDMI_ACR_48_1

Bits	Name	Description
31:20	RESERVED	
19:0	N_48	N value for 48 kHz audio sample rate

0x04A000E4 HDMI_AUDIO_INFO0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000170

HDMI Audio InfoFrame Packet Body Contents

HDMI_AUDIO_INFO0

Bits	Name	Description
31:24	RESERVED_1	
23:16	CHECKSUM_OFFSET	Offset for hardware calculated checksum
15:11	RESERVED_2	
10:8	CC	Used only AUDIO_INFO_SOURCE field = 1
7:0	CHECKSUM	Used only AUDIO_INFO_SOURCE field = 1

0x04A000E8 HDMI_AUDIO_INFO1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Audio InfoFrame Packet Body Contents, Cont'd

HDMI_AUDIO_INFO1

Bits	Name	Description
31:16	RESERVED_1	

HDMI_AUDIO_INFO1 (cont.)

Bits	Name	Description
15	DM_INH	Down mixing inhibit bits for audio info frame packet. refer to the CEA 861-D/E/F spec for details
14:11	LSV	Level shift value (for down-mixing) for audio info frames. refer to the CEA 861-D/E/F spec for details
10:8	RESERVED_2	
7:0	CA	Channel/speaker allocation bits for infoframe packets for all 8 channels.Not valid for compressed streams

0x04A000EC HDMI_60958_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x10000000

HDMI 60958 Audio Sample Packet Info. Please refer to IEC60958 audio standard spec for more details

HDMI_60958_0

Bits	Name	Description
31:30	RESERVED	
29:28	CLOCK_ACCURACY	- 29th and 30th Left (L) Channel status bits for IEC60958 frame's 192 blocks
27:24	SAMPLING_FREQUENCY	Used only AUDIO_INFO_SOURCE field = 1, 25th to 28th Left (L) Channel status bits for IEC60958 frame's 192 blocks
23:20	CHANNEL_NUMBER_L	- 21st to 24th Left (L) Channel status bits for IEC60958 frame's 192 blocks
19:16	SOURCE_NUMBER	- 17th to 20th Left (L) Channel status bits for IEC60958 frame's 192 blocks
15:8	CATEGORY_CODE	Eight to 16th Left (L) Channel status bits for IEC60958 frame's 192 blocks
7:6	MODE	Sixth/seventh Left (L) Channel status bits for IEC60958 frame's 192 blocks
5:3	D	Fourth/Fifth Left (L) Channel status bits for IEC60958 frame's 192 blocks
2	C	Third Left (L) Channel status bit for IEC60958 frame's 192 blocks
1	B	Second Left (L) Channel status bit for IEC60958 frame's 192 blocks
0	A	First Left (L) Channel status bit for IEC60958 frame's 192 blocks

0x04A000F0 HDMI_60958_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI 60958 Audio Sample Packet Info

HDMI_60958_1

Bits	Name	Description
31:26	RESERVED_1	
25	USER_R	
24	USER_L	
23:20	CS_CHANNEL_NUMBER_R	- 21st to 24th Right (R) Channel status bits for IEC60958 frame's 192 blocks
19	RESERVED_2	
18	VALID_R	Right channel valid bit for HDMI packet
17	RESERVED_3	
16	VALID_L	Left channel valid bit for HDMI packet
15:8	RESERVED_4	
7:4	CS_ORIG_SAMPLE_FREQ	Used only if HDMI_AUDIO_INFO_SOURCE = 1, 37th to 40th Left (L) Channel status bits for IEC60958 frame's 192 blocks
3:0	CS_WORD_LENGTH	Used only if HDMI_AUDIO_INFO_SOURCE = 1, 33rd to 36th Left (L) Channel status bits for IEC60958 frame's 192 blocks

0x04A00108 HDMI_60958_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI 60958 Audio Sample Packet Info

HDMI_60958_2

Bits	Name	Description
31:24	RESERVED	
23:20	CS_CHANNEL_NUM_7	Channel Number field to send in channel 7 audio sample channel status for layout 1.
19:16	CS_CHANNEL_NUM_6	Channel Number field to send in channel 6 audio sample channel status for layout 1.

HDMI_60958_2 (cont.)

Bits	Name	Description
15:12	CS_CHANNEL_NUM_5	Channel Number field to send in channel 5 audio sample channel status for layout 1.
11:8	CS_CHANNEL_NUM_4	Channel Number field to send in channel 4 audio sample channel status for layout 1.
7:4	CS_CHANNEL_NUM_3	Channel Number field to send in channel 3 audio sample channel status for layout 1.
3:0	CS_CHANNEL_NUM_2	Channel Number field to send in channel 2 audio sample channel status for layout 1.

0x04A0016C HDMI_VENSPEC_INFO0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000006

Program the fields of Vendor Specific Info frame packets.

HDMI_VENSPEC_INFO0

Bits	Name	Description
31:29	RESERVED	
28	HDMI_3D_MPRESENT	This field programs the 3D META_PRESENT field as described in Vendor specific Info frame packet body.
27:24	HDMI_3D_STRUCT	This field programs the 3D_STRUCTURE field as described in Vendor specific Info frame packet body.
23:16	HDMI_VIC	This field programs the HDMI_VIC in Vendor Specific Info frame packet body. This VIC is proprietary to HDMI LLc.
15:8	VENSPEC_CHECKSUM	
7:5	VID_FORMAT	This field programs the video format in the packet body.
4:0	LENGTH	this field programs the length field in the Vendor specific infoframe packet header. Defaulted to 6 because as per HDMI 1.4a spec, the mandatory 3D formats can be supported by 6 packet bytes in the packet body.

0x04A00170

HDMI_VENSPEC_INFO1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Program the fields of Vendor Specific Info frame packets.

HDMI_VENSPEC_INFO1

Bits	Name	Description
31:24	VENSPEC_PB9	This field programs the byte 9 of Vendor specific Info frame packet body.
23:16	VENSPEC_PB8	This field programs the byte 8 of Vendor specific Info frame packet body.
15:12	RESERVED	
11:7	HDMI_3D_MDATA_LEN	This field programs the 3D_METADATE_LEN field as described in Vendor specific Info frame packet body.
6:4	HDMI_3D_MDATA_TYPE	This field programs the 3D_METADATA_TYPE field as described in Vendor specific Info frame packet body.
3:0	HDMI_3D_EXT_DAT	

0x04A00174 HDMI_VENSPEC_INFO2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Program the fields of Vendor Specific Info frame packets.

HDMI_VENSPEC_INFO2

Bits	Name	Description
31:24	VENSPEC_PB13	This field programs the byte 13 of Vendor specific Info frame packet body.
23:16	VENSPEC_PB12	This field programs the byte 12 of Vendor specific Info frame packet body.
15:8	VENSPEC_PB11	This field programs the byte 11 of Vendor specific Info frame packet body.
7:0	VENSPEC_PB10	

0x04A00178 HDMI_VENSPEC_INFO3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Program the fields of Vendor Specific Info frame packets.

HDMI_VENSPEC_INFO3

Bits	Name	Description
31:24	VENSPEC_PB17	This field programs the byte 17 of Vendor specific Info frame packet body.
23:16	VENSPEC_PB16	This field programs the byte 16 of Vendor specific Info frame packet body.
15:8	VENSPEC_PB15	This field programs the byte 15 of Vendor specific Info frame packet body.
7:0	VENSPEC_PB14	

0x04A0017C HDMI_VENSPEC_INFO4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Program the fields of Vendor Specific Info frame packets.

HDMI_VENSPEC_INFO4

Bits	Name	Description
31:24	VENSPEC_PB21	This field programs the byte 21 of Vendor specific Info frame packet body.
23:16	VENSPEC_PB20	This field programs the byte 20 of Vendor specific Info frame packet body.
15:8	VENSPEC_PB19	This field programs the byte 19 of Vendor specific Info frame packet body.
7:0	VENSPEC_PB18	

0x04A00180 HDMI_VENSPEC_INFO5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Program the fields of Vendor Specific Info frame packets.

HDMI_VENSPEC_INFO5

Bits	Name	Description
31:24	VENSPEC_PB25	This field programs the byte 25 of Vendor specific Info frame packet body.
23:16	VENSPEC_PB24	This field programs the byte 24 of Vendor specific Info frame packet body.
15:8	VENSPEC_PB23	This field programs the byte 23 of Vendor specific Info frame packet body.
7:0	VENSPEC_PB22	

0x04A00184 HDMI_VENSPEC_INFO6

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Program the fields of Vendor Specific Info frame packets.

HDMI_VENSPEC_INFO6

Bits	Name	Description
31:16	RESERVED	
15:8	VENSPEC_PB27	This field programs the byte 27 of Vendor specific Info frame packet body.
7:0	VENSPEC_PB26	

0x04A001D0 HDMI_AUDIO_CFG

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000040

This register is used to configure the HDMI audio engine. This register enables the audio engine, configures the number of audio channels and the audio fifo watermarks.

HDMI_AUDIO_CFG

Bits	Name	Description
31:12	RESERVED_1	

HDMI_AUDIO_CFG (cont.)

Bits	Name	Description
11	SAMP_PRE_EN	- 0 = Sample present for 4 and 6 channel will be all 1 and sample flat for unused channels will be 1. 1= Sample present for unused channels will be 0. Sample flat for unused channels will be 0.
10	HBR_EN	- 0 = Disable High Bit Rate audio packet Header. 1 = Enable High Bit Rate audio packet Header.
9	PAYLOAD_PACK_EN	Enable audio data payload packing by HDMI core. 0= Software packs the audio data payload as per IEC60958 format. 1= HDMI core does the packing of payload bits to hdmi audio data. The bits inserted are V= valid, U=User, C= Channel Select, P = parity. When enabled this will also insert the B bit mentioned in HDMI audio packet header. For more information on V,U,C,P bits please refer to IEC60958 spec. Programming V, U, C bits will be through HDMI_60958_0, HDMI_60958_1 and HDMI_60958_2 registers.
8	SMPL_DEFER_MODE	Enable the deferring of transmission of audio samples in active region when ACR packet also needs to be transmitted on the same line. This mode is used when transmitting 176.4Khz or 192 Khz audio on VGA, 480P and 576P video resolutions. 0= Disable, 1 = enable.
7:4	FIFO_WATERMARK	Watermark for HDMI fifo - 0x0 =request when empty - 0x1= when 1 empty slot - 0x2=when 2 empty slots - 0x3= when 3 slots empty - 0x4= when 4 empty slots - 0x5= when 5 empty slots - 0x6= when 6 empty slots - 0x7= when 7 empty slots - 0x8= when fifo is fully empty.
3:2	CHANNEL_NUM	Number of Audio Channels 0x0= 8 channel - 0x1= 4 channel - 0x2 = 6 channel
1	RESERVED_2	
0	ENABLE	Enable the audio engine - 0 = Disabled - 1= Enabled.

0x04A00204 HDMI_DEBUG

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Debug register

HDMI_DEBUG

Bits	Name	Description
31:0	DEBUG	HDMI debug register, DEBUG[4] when enabled, will make Sample present for LAYOUT 1 programmable. SAMPLE_PRESENT will be the value programmed in DEBUG[3:0]. DEBUG[31:5] are reserved.

0x04A00208 HDMI_USEC_REFTIMER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000004A

Microsecond reference timer

HDMI_USEC_REFTIMER

Bits	Name	Description
31:17	RESERVED	
16	REFTIMER_ENABLE	Enable the reference timer 0x0: Disable 0x1: Enable
15:0	REFTIMER	Value to set the register in order to generate a strobe every microsecond. This register counts on HDCP application clock

0x04A0020C HDMI_DDC_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Control Register for DDC operations

HDMI_DDC_CTRL

Bits	Name	Description
31	RESERVED_1	
21:20	TRANSACTION_CNT	Number of transactions to be done in current transfer. 0x0: transaction0 only 0x1: transaction0, transaction1 0x2: transaction0, transaction1, transaction2 0x3: transaction0, transaction1, transaction2, transaction3

HDMI_DDC_CTRL (cont.)

Bits	Name	Description
19:7	RESERVED_2	
6	RESERVED_3	
4	RESERVED_4	
3	SW_STATUS_RESET	Write 1 to reset HDMI_DDC_SW_STATUS flags, will reset SW_DONE, ABORTED, TIMEOUT, SW_INTERRUPTED, BUFFER_OVERFLOW, STOPPED_ON_NACK, NACK0, NACK1, NACK2, NACK3
2	SEND_RESET	Set to 1 to send reset sequence (9 clocks with no data) at start of transfer. This sequence is sent after GO is written to 1, before the first transaction only.
1	SOFT_RESET	Write 1 to reset DDC controller
0	GO	WRITE ONLY. Write 1 to start DDC transfer.

0x04A00210 HDMI_DDC_ARBITRATION

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000001

Configure arbitration between hardware and software use of the HDMI_DDC engine

HDMI_DDC_ARBITRATION

Bits	Name	Description
31:13	RESERVED_1	
12	ABORT_SW_XFER	WRITE ONLY. Write 1 to abort current SW transfer (send stop if transfer has started)
11:9	RESERVED_2	
8	ABORT_HW_XFER	WRITE ONLY. Write 1 to abort current HW transfer (send stop if transfer has started)
7:6	RESERVED_3	
5	NO_RESTART_SW_GO	Set to 1 to disable restart of software DDC transaction that was interrupted by hardware. Typically this bit should be 0, unless there is a problem with the DDC restart mechanism. When this bit is set to 0, the SW_DONE bit will not be set if hardware interrupts the software transfer.
4	NO_QUEUED_SW_GO	Set to 1 to disable queuing of software DDC GO. If this bit is set, then if software writes GO while DDC is in use by hardware, the GO request will be ignored and the SW_INTERRUPTED bit set.
3:2	RESERVED_4	

HDMI_DDC_ARBITRATION (cont.)

Bits	Name	Description
1:0	SW_PRIORITY	Sets priority for software DDC requests. This setting applies only when HDCP is using DDC bus and software also wants to use the same DDC bus 0x0: Normal - If NO_QUEUED_SW_GO = 0, software DDC transaction will be queued after HW DDC. If NO_QUEUED_SW_GO = 1, software DDC transaction is not queued, in this case, software have to poll for HW_DONE doing any DDC transaction 0x1: High - Software always interrupts HW DDC if HDCP is using the same DDC bus, HW DDC will automatically resume once software DDC is completed 0x2: Reserved_1 0x3: Reserved_2

0x04A00214 HDMI_DDC_INT_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DDC Interrupt Control register

HDMI_DDC_INT_CTRL

Bits	Name	Description
31:7	RESERVED_1	
6	HW_DONE_MASK	DDC Mask bit for HW_DDC_DONE_INT. Set to 1 to enable interrupt.
5	HW_DONE_ACK	WRITE ONLY. DDC Acknowledge bit for HW_DDC_DONE_INT. Write 1 to clear interrupt.
4	HW_DONE_INT	READ ONLY. DDC HW_DONE interrupt status
3	RESERVED_2	
2	SW_DONE_MASK	Mask bit for SW_DONE_INT. Set to 1 to enable interrupt.
1	SW_DONE_ACK	WRITE ONLY. Acknowledge bit for SW_DONE_INT. Write 1 to clear interrupt.
0	SW_DONE_INT	READ ONLY. SW_DONE interrupt status

0x04A00218 HDMI_DDC_SW_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Status fields for HDMI_DDC engine

HDMI_DDC_SW_STATUS

Bits	Name	Description
31:19	RESERVED_1	
18	SW_REQ	READ ONLY. Software requests use of HDMI_DDC interface (indicates that request is pending - i.e., queued). Cleared when request becomes active or by ABORT_SW_XFER.
17:16	RESERVED_2	
15	SW_NACK3	READ ONLY. Indicates that DDC slave did not issue an acknowledge during the fourth SW transaction. Cleared on GO.
14	SW_NACK2	READ ONLY. Indicates that DDC slave did not issue an acknowledge during the third SW transaction. Cleared on GO.
13	SW_NACK1	READ ONLY. Indicates that DDC slave did not issue an acknowledge during the second SW transaction. Cleared on GO.
12	SW_NACK0	READ ONLY. Indicates that DDC slave did not issue an acknowledge during the first SW transaction. Cleared on GO.
11	RESERVED_3	
10	RESERVED_4	
8	SW_STOPPED_ON_NACK	READ ONLY. Indicates that SW transfer was interrupted due to NACK when STOP_ON_NACK=1. Cleared on GO.
7	SW_BUFFER_OVERFLOW	READ ONLY. Indicates that buffer overflow occurred during SW transfer, stopping transfer. Cleared on GO.
6	SW_INTERRUPTED	READ ONLY. Indicates that SW transfer was interrupted by hardware request. Cleared on GO.
5	SW_TIMEOUT	READ ONLY. Indicates that timeout condition occurred during SW transfer, stopping transfer. Cleared on GO.
4	SW_ABORTED	READ ONLY. Indicates that abort request occurred during SW transfer, stopping transfer. Cleared on GO.
3	RESERVED	
2	SW_DONE	READ ONLY. Set on completion of SW transfer. Cleared by writing HDMI_DDC_INT_CTRL.SW_DONE_ACK to 1

HDMI_DDC_SW_STATUS (cont.)

Bits	Name	Description
1:0	SW_STATUS	READ ONLY. Current SW status of HDMI_DDC 0x0: Idle 0x1: In use by SW 0x2: In use by HW 0x3: Reserved

0x04A0021C HDMI_DDC_HW_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Status fields for HDMI_DDC engine

HDMI_DDC_HW_STATUS

Bits	Name	Description
31:18	RESERVED_1	
17	HW_URG	READ ONLY. Indicates that hardware DDC request is urgent (used by arbitration logic).
16	HW_REQ	READ ONLY. Hardware requests use of HDMI_DDC interface (indicates that request is pending - i.e., queued). Cleared when request becomes active or by ABORT_HW_XFER.
15:4	RESERVED_2	
3	HW_DONE	READ ONLY. Set on completion of HW transfer. Cleared by writing HW_DONE_ACK to 1
2	RESERVED	
1:0	HW_STATUS	READ ONLY. Current HW status of HDMI_DDC 0x0: Idle 0x1: In use by SW 0x2: In use by HW 0x3: Reserved

0x04A00220 HDMI_DDC_SPEED

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000002

DDC speed setting

HDMI_DDC_SPEED

Bits	Name	Description
31:16	PRESCALE	prescale = (m * xtal_frequency) / (desired_i2c_speed), where m is multiply factor, default: m = 1
15:5	RESERVED_1	
4	DIS_FILTER_IN_STALL	Determines whether dout_filter will be disabled when receiver is clock stalling. 0x0: Disable 0x1: Don't Disable
3:2	RESERVED_2	
1:0	THRESHOLD	Select threshold to use to determine whether value sampled on SDA is a 1 or 0. Specified in terms of the ratio between the number of sampled ones and the total number of times SDA is sampled. * 0x0: >0 0x1: 1/4 of total samples 0x2: 1/2 of total samples 0x3: 3/4 of total samples

0x04A00224 HDMI_DDC_SETUP

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

DDC SETUP

HDMI_DDC_SETUP

Bits	Name	Description
31:24	TIME_LIMIT	Time limit, in units of 256 DDC fast reference (TOCLK) pulses, to wait before timeout when clock is stalled by external device.
23:16	INTRA_XFER_DELAY	Use to specify delay between transactions in units of DDC reference.
15:8	INTRA_BYTE_DELAY	Use to specify delay between bytes in units of DDC reference.
7	CLK_DRIVE_EN	Select whether SCL pad is pulled up or driven high - 0:Pullup by external resistor - 1:DDC pads drive SCL high 0x0: Pullup by external resistor 0x1: DDC pads drive SCL
6:2	RESERVED	

HDMI_DDC_SETUP (cont.)

Bits	Name	Description
1	DATA_DRIVE_SEL	Select number of clocks to drive SDA high - 0:Drive for 10 SCLKs - 1:Drive for 20 SCLKs 0x0: Drive for 10MCLKs 0x1: 20MCLKS
0	DATA_DRIVE_EN	Select whether SDA pad is pulled up or driven high - 0:Pullup by external resistor - 1:DDC pads drive SDA high 0x0: Pullup by external resistor 0x1: DDC pads drive SDA

0x04A00228 HDMI_DDC_TRANS0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Configuration for first transaction

HDMI_DDC_TRANS0

Bits	Name	Description
31:24	RESERVED_1	
23:16	CNT0	Byte count for first transaction (excluding the first byte, which is usually the address).
15:14	RESERVED_2	
13	STOP0	Determines whether a stop bit will be sent after the first transaction 0x0: NO STOP 0x1: STOP
12	START0	Determines whether a start bit will be sent before the first transaction 0x0: NO START 0x1: START
11:9	RESERVED_3	
8	STOP_ON_NACK0	Determines whether the current transfer will stop if a NACK is received during the first transaction (current transaction always stops). 0x0: STOP CURRENT TRANSACTION, GO TO NEXT TRANSACTION 0x1: STOP ALL TRANSACTIONS, SEND STOP BIT
7:1	RESERVED_4	

HDMI_DDC_TRANS0 (cont.)

Bits	Name	Description
0	RW0	Read/write indicator for first transaction - set to 0 for write, 1 for read. This bit only controls HDMI_DDC behavior - the R/W bit in the transaction is programmed into the DDC buffer as the LSB of the address byte. 0x0: WRITE 0x1: READ

0x04A0022C HDMI_DDC_TRANS1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Configuration for second transaction

HDMI_DDC_TRANS1

Bits	Name	Description
31:24	RESERVED_1	
23:16	CNT1	Byte count for second transaction (excluding the first byte, which is usually the address).
15:14	RESERVED_2	
13	STOP1	Determines whether a stop bit will be sent after the second transaction 0x0: NO STOP 0x1: STOP
12	START1	Determines whether a start bit will be sent before the second transaction 0x0: NO START 0x1: START
11:9	RESERVED_3	
8	STOP_ON_NACK1	Determines whether the current transfer will stop if a NACK is received during the second transaction (current transaction always stops). 0x0: STOP CURRENT TRANSACTION, GO TO NEXT TRANSACTION 0x1: STOP ALL TRANSACTIONS, SEND STOP BIT
7:1	RESERVED_4	

HDMI_DDC_TRANS1 (cont.)

Bits	Name	Description
0	RW1	Read/write indicator for second transaction - set to 0 for write, 1 for read. This bit only controls HDMI_DDC behavior - the R/W bit in the transaction is programmed into the DDC buffer as the LSB of the address byte. 0x0: WRITE 0x1: READ

0x04A00230 HDMI_DDC_TRANS2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Configuration for third transaction

HDMI_DDC_TRANS2

Bits	Name	Description
31:24	RESERVED_1	
23:16	CNT2	Byte count for third transaction (excluding the first byte, which is usually the address).
15:14	RESERVED_2	
13	STOP2	Determines whether a stop bit will be sent after the third transaction 0x0: NO STOP 0x1: STOP
12	START2	Determines whether a start bit will be sent before the third transaction 0x0: NO START 0x1: START
11:9	RESERVED_3	
8	STOP_ON_NACK2	Determines whether the current transfer will stop if a NACK is received during the third transaction (current transaction always stops). 0x0: STOP CURRENT TRANSACTION, GO TO NEXT TRANSACTION 0x1: STOP ALL TRANSACTIONS, SEND STOP BIT
7:1	RESERVED_4	

HDMI_DDC_TRANS2 (cont.)

Bits	Name	Description
0	RW2	Read/write indicator for third transaction - set to 0 for write, 1 for read. This bit only controls HDMI_DDC behavior - the R/W bit in the transaction is programmed into the DDC buffer as the LSB of the address byte. 0x0: WRITE 0x1: READ

0x04A00234 HDMI_DDC_TRANS3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Configuration for fourth transaction

HDMI_DDC_TRANS3

Bits	Name	Description
31:24	RESERVED_1	
23:16	CNT3	Byte count for fourth transaction (excluding the first byte, which is usually the address).
15:14	RESERVED_2	
13	STOP3	Determines whether a stop bit will be sent after the fourth transaction 0x0: NO STOP 0x1: STOP
12	START3	Determines whether a start bit will be sent before the fourth transaction 0x0: NO START 0x1: START
11:9	RESERVED_3	
8	STOP_ON_NACK3	Determines whether the current transfer will stop if a NACK is received during the fourth transaction (current transaction always stops). 0x0: STOP CURRENT TRANSACTION, GO TO NEXT TRANSACTION 0x1: STOP ALL TRANSACTIONS, SEND STOP BIT
7:1	RESERVED_4	

HDMI_DDC_TRANS3 (cont.)

Bits	Name	Description
0	RW3	Read/write indicator for fourth transaction - set to 0 for write, 1 for read. This bit only controls HDMI_DDC behavior - the R/W bit in the transaction is programmed into the DDC buffer as the LSB of the address byte. 0x0: WRITE 0x1: READ

0x04A00238 HDMI_DDC_DATA

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

This register is used to read or write the DDC buffer

HDMI_DDC_DATA

Bits	Name	Description
31	INDEX_WRITE	WRITE ONLY. To write index field, set this bit to 1 while writing HDMI_DDC_DATA.
30:24	RESERVED_1	
23:16	INDEX	Use to set index into DDC buffer for next read or current write, or to read index of current read or next write. Writable only when INDEX_WRITE=1.
15:8	DATA	Use to fill or read the DDC buffer
7:1	RESERVED_2	
0	DATA_RW	Select whether buffer access will be a read or write. For writes, address auto-increments on write to HDMI_DDC_DATA. For reads, address auto-increments on reads to HDMI_DDC_DATA. 0x0: Write 0x1: Read

0x04A00250 HPD_INT_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HPD status

HPD_INT_STATUS

Bits	Name	Description
31:9	RESERVED_1	
8	RX_INT_STATUS	READ ONLY. Panel rx interrupt status
7:2	RESERVED_2	
1	SENSE	READ ONLY. Panel connection status 0x0: panel disconnected on HPD 0x1: panel connected on HPD
0	INT_STATUS	READ ONLY. Panel interrupt status

0x04A00254 HPD_INT_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HPD interrupt control

HPD_INT_CTRL

Bits	Name	Description
31:10	RESERVED_1	
9	RCV_PLUGIN_DET_MASK	receiver plug in interrupt mask. When programmed to 1,RCV_PLUGIN_DET_INT will toggle the interrupt line
8:6	RESERVED_2	
5	RX_INT_EN	panel rx interrupt enable 0x0: Disable 0x1: Enable
4	RX_INT_ACK	WRITE ONLY. Panel rx interrupt ack
3	RESERVED	
2	INT_EN	Panel interrupt control 0x0: Disable 0x1: Enable
1	INT_POLARITY	Panel interrupt polarity 0x0: generate interrupt on disconnect 0x1: generate interrupt on connect
0	INT_ACK	WRITE ONLY. Panel interrupt ack

0x04A00258 HPD_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x10FA09C4

HPD timer control

HPD_CTRL

Bits	Name	Description
31:29	RESERVED_1	
28	ENABLE	HPD circuit enable 0x0: Disable 0x1: Enable
27:26	RESERVED_2	
25:16	RX_INT_TIMER	Amount of time in microseconds HPD line must be de-asserted for an rx event
15:13	RESERVED	
12:0	CONNECTION_TIMER	Amount of time in microseconds HPD line must be asserted/de-asserted for a connect/disconnect

0x04A00268 HDMI_CRC_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000010

HDMI CRC control

HDMI_CRC_CTRL

Bits	Name	Description
31:9	RESERVED_1	
8	USE_PRE_N_GUARD_BAND	Indicates whether preamble and guard band should be used in CRC calculation 0x0: Do not use preamble 0x1: Use Preamble
7:4	CRC_FRAMES	Number of frame the CRC needs to be calculated for, Default is one frame. Option to program CRC calculation for 16 frames and stop.
3:1	RESERVED_2	

HDMI_CRC_CTRL (cont.)

Bits	Name	Description
0	CRC_EN	Enables CRC calculation on next VSYNC 0x0: crc disable 0x1: crc Enable

0x04A0026C HDMI_VID_CRC

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Video CRC

HDMI_VID_CRC

Bits	Name	Description
31:30	RESERVED	
29:0	CRC	READ ONLY. Video CRC

0x04A00270 HDMI_AUD_CRC

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Audio CRC

HDMI_AUD_CRC

Bits	Name	Description
31	RESERVED	
30:0	CRC	READ ONLY. Audio CRC

0x04A00274 HDMI_VBI_CRC

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

VBI CRC

HDMI_VBI_CRC

Bits	Name	Description
31	RESERVED	
30:0	CRC	READ ONLY. VBI CRC

0x04A0027C HDMI_DDC_REF

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00010005

DDC reference clock generation

HDMI_DDC_REF

Bits	Name	Description
31:17	RESERVED	
16	REFTIMER_ENABLE	Enable the timer 0x0: Disable 0x1: Enable
15:0	REFTIMER	Value to set the register in order to generate DDC strobe. This register counts on HDCP application clock

0x04A00284 HDCP_SW_UPPER_AKSV

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

SW injected AKSV

HDCP_SW_UPPER_AKSV

Bits	Name	Description
31:8	RESERVED	
7:0	UPPER_AKSV	This is the upper 8 bits of the SW injected AKSV value(AKSV[39:32]) read from the EFUSE. It's needed for HDCP authentication and must be written before enabling HDCP.

0x04A00288 HDCP_SW_LOWER_AKSV

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

SW injected AKSV

HDCP_SW_LOWER_AKSV

Bits	Name	Description
31:0	LOWER_AKSV	This is the lower 32 bits of the SW injected AKSV value(AKSV[31:0]) read from the EFUSE. It's needed for HDCP authentication and must be written before enabling HDCP.

0x04A0028C HDMI_CEC_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

CEC Block Control

HDMI_CEC_CTRL

Bits	Name	Description
31:10	RESERVED_1	
9	LINE_OE	Output Enable for CEC line
8:4	FRAME_SIZE	Size of CEC frame
3	RESERVED_2	
2	SOFT_RESET	Write 1 to soft reset the CEC engine
1	SEND_TRIG	Write Trigger for CEC writes
0	ENABLE	- 0 = CEC is Disabled - 1 = CEC is Enabled 0x0: Disable 0x1: Enable

0x04A00290 HDMI_CEC_WR_DATA

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

CEC Read/Write Data

HDMI_CEC_WR_DATA

Bits	Name	Description
31:16	RESERVED_1	
15:8	DATA	WRITE ONLY. CEC Write Data
7:1	RESERVED_2	
0	FRAME_TYPE	- 0 = Single Follower - 1 = Broadcast message

0x04A00294 HDMI_CEC_RETRANSMIT

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

CEC Re-transmit frame

HDMI_CEC_RETRANSMIT

Bits	Name	Description
31:8	RESERVED_1	
7:4	NUM	Number of programmable times the frame needs to be retransmitted
3:1	RESERVED_2	
0	ENABLE	- 0 = Disabled - 1 = Enabled 0x0: Disable 0x1: Enable

0x04A00298 HDMI_CEC_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

CEC Status

HDMI_CEC_STATUS

Bits	Name	Description
31:12	RESERVED_1	
11:8	FRAME_RETRANSMIT	READ ONLY. Number of times frame has been retransmitted
7:4	ERROR	READ ONLY. 0=No Error - 1=No ACK - 2=read 0 or 1 invalid - 3=arbitration failed
3	FRAME_DONE	READ ONLY. 0=Frame Not Done - 1=Frame Done
2	RESERVED_2	
1:0	STATUS	READ ONLY. 00=IDLE - 01=USED

0x04A0029C HDMI_CEC_INT

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

CEC Interrupt

HDMI_CEC_INT

Bits	Name	Description
31:8	RESERVED	
7	FRAME_RD_DONE_MASK	- 0=Interrupt Disabled - 1=Interrupt Enabled for FRAME_READ_DONE
6	FRAME_RD_DONE_ACK	WRITE ONLY. Acknowledge bit for FRAME_READ_DONE
6	FRAME_RD_DONE_INT	READ ONLY. CEC FRAME_READ_DONE status
5	MONITOR_MASK	- 0=Interrupt Disabled - 1=Interrupt Enabled for MONITOR_INT
4	MONITOR_INT	READ ONLY. CEC MONITOR_INT status
4	MONITOR_ACK	WRITE ONLY. Acknowledge bit for MONITOR_INT
3	FRAME_ERROR_MASK	- 0=Interrupt Disabled - 1=Interrupt Enabled for FRAME_ERROR
2	FRAME_ERROR_INT	READ ONLY. CEC FRAME_ERROR status
2	FRAME_ERROR_ACK	WRITE ONLY. Acknowledge bit for FRAME_ERROR

HDMI_CEC_INT (cont.)

Bits	Name	Description
1	FRAME_WR_DONE_MASK	- 0=Interrupt Disabled - 1=Interrupt Enabled for FRAME_WRITE_DONE
0	FRAME_WR_DONE_ACK	WRITE ONLY. Acknowledge bit for FRAME_WRITE_DONE
0	FRAME_WR_DONE_INT	READ ONLY. CEC FRAME_WRITE_DONE status

0x04A002A0 HDMI_CEC_ADDR

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

CEC Logical Address

HDMI_CEC_ADDR

Bits	Name	Description
31:8	RESERVED	
7:0	LOGICAL_ADDR	CEC Logical Address

0x04A002A4 HDMI_CEC_TIME

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

CEC Signal Free Time

HDMI_CEC_TIME

Bits	Name	Description
31:16	RESERVED_1	
15:7	SIGNAL_FREE_TIME	Signal Free Time counter
6:1	RESERVED_2	
0	ENABLE	- 0 = Signal Free Time counter Disabled - 1 = Signal Free Time counter Enabled 0x0: Disable 0x1: Enable

0x04A002A8 HDMI_CEC_REFTIMER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000004A

Microsecond reference timer

HDMI_CEC_REFTIMER

Bits	Name	Description
31:17	RESERVED	
16	REFTIMER_ENABLE	Enable the reference timer 0x0: Disable 0x1: Enable
15:0	REFTIMER	Value to set the register in order to generate a strobe every microsecond. This register counts on application clock

0x04A002AC HDMI_CEC_RD_DATA

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

CEC read data

HDMI_CEC_RD_DATA

Bits	Name	Description
31:13	RESERVED	
12:8	FRAME_SIZE	READ ONLY. Read data frame size
7:0	DATA	READ ONLY. CEC Read data

0x04A002B0 HDMI_CEC_RD_FILTER

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

CEC read filter

HDMI_CEC_RD_FILTER

Bits	Name	Description
31:16	RESERVED_1	
15:4	FILTER_TIME	Number of application clocks the transition on CEC line to be filtered. Max is 4096 clocks
3:1	RESERVED_2	
0	FILTER_EN	CEC read filter enable. 0= disable, 1 - enable filter 0x0: Disable 0x1: Enable

0x04A002B4 HDMI_ACTIVE_H

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Active Horizontal Information

HDMI_ACTIVE_H

Bits	Name	Description
31:28	RESERVED_1	
27:16	END	Horizontal end
15:12	RESERVED_2	
11:0	START	Horizontal start

0x04A002B8 HDMI_ACTIVE_V

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Active Vertical Information

HDMI_ACTIVE_V

Bits	Name	Description
31:28	RESERVED_1	
27:16	END	Vertical end
15:12	RESERVED_2	

HDMI_ACTIVE_V (cont.)

Bits	Name	Description
11:0	START	Vertical start

0x04A002BC HDMI_ACTIVE_V_F2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Active vertical information for field 2.This only takes effect if INTERLACED_EN field in HDMI_FRAME_CTRL register is enabled

HDMI_ACTIVE_V_F2

Bits	Name	Description
31:28	RESERVED_1	
27:16	END_F2	Vertical end for field2
15:12	RESERVED_2	
11:0	START_F2	Vertical start for Field2

0x04A002C0 HDMI_TOTAL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Total Horizontal and Vertical Active Counts

HDMI_TOTAL

Bits	Name	Description
31:28	RESERVED_1	
27:16	V_TOTAL	Vertical Total
15:12	RESERVED_2	
11:0	H_TOTAL	Horizontal Total

0x04A002C4 HDMI_V_TOTAL_F2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Total Vertical Count for field 2. This only takes effect if INTERLACED_EN field in HDMI_FRAME_CTRL register is enabled

HDMI_V_TOTAL_F2

Bits	Name	Description
31:12	RESERVED	
11:0	V_TOTAL_F2	Vertical total for field2

0x04A002C8 HDMI_FRAME_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI frame control for SYNC and data

HDMI_FRAME_CTRL

Bits	Name	Description
31	INTERLACED_EN	Interlaced or progressive enable bit 0x0: Frame in progressive 0x1: Frame is interlaced
30	RESERVED_1	
29	HSYNC_HDMI_POL	HSYNC polarity fed to HDMI core 0x0: Active Hi Hsync, detect the rising edge of hsync 0x1: Active lo Hsync, Detect the falling edge of Hsync
28	VSYNC_HDMI_POL	VSYNC polarity fed to HDMI core 0x0: Active Hi Vsync, detect the rising edge of vsync 0x1: Active Lo Vsync, Detect the falling edge of Vsync
27:16	VCNT_DEF	Vertical Default. This should match the initial vcount for the FIRST frame from the display engine. For engines that are capable of beginning in the middle of a frame it should be set to that value otherwise it should be set to ZERO
15:13	RESERVED_2	
12	RGB_MUX_SEL	Mux to control the input data format from mdp 0x0: mdp4 input is RGB 0x1: mdp4 input is BGR

HDMI_FRAME_CTRL (cont.)

Bits	Name	Description
11:0	HCNT_DEF	Horizontal Default. This should match the initial hcount for the FIRST frame from the display engine. For engines that are capable of beginning in the middle of a frame it should be set to that value otherwise it should be set to ZERO

0x04A002CC HDMI_AUD_INT

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI Audio interrupt for fifo underrun and sample drop incase the sample count coming from lpass does not match the one in audio

HDMI_AUD_INT

Bits	Name	Description
31:4	RESERVED	
3	AUD_SAM_DROP_MASK	Audio sample drop interrupt mask. When 1 written to this bit, it AUD_SAM_DROP_INT interrupt will toggle the interrupt line
2	AUD_SAM_DROP_INT	READ ONLY. Audio sample drop interrupt. This goes hi when the audio data tag coming in from lpass does not match the count in audio engine
2	AUD_SAM_DROP_ACK	WRITE ONLY. Audio sample drop interrupt acknowledge. When 1 written to this bit, it will generate a pulse to clear the AUD_SAM_DROP_INT
1	AUD_FIFO_URUN_MASK	Audio fifo underrun interrupt mask. When 1 written to this bit, it AUD_FIFO_URUN_INT interrupt will toggle the interrupt line
0	AUD_FIFO_URUN_ACK	WRITE ONLY. Audio fifo underrun interrupt acknowledge. When 1 written to this bit, it will generate a pulse to clear the AUD_FIFO_URUN_INT
0	AUD_FIFO_URUN_INT	READ ONLY. Audio fifo underrun interrupt. This goes hi when the audio fifo requests the data put there is no request and all the fifo entries are drained out

0x04A002D0 HDMI_DEBUG_BUS_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Debug bus control register

HDMI_DEBUG_BUS_CTRL

Bits	Name	Description
31:16	DEBUG_BUS	READ ONLY. Debug bus register read
15:10	RESERVED_1	
9:4	DEBUG_SEL	Select the group of signals to be selected on debug bus, for Testing purpose 0x3D = 0xAAAA 0x3E = 0x5555, 0x3F = 0xFA05.
3:1	RESERVED_2	
0	DEBUG_BUS_EN	Enable Debug Bus 0=disable, 1= Enable

0x04A002D4 HDMI_PHY_CTRL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI PHY control register

HDMI_PHY_CTRL

Bits	Name	Description
31:18	RESERVED_1	
17	PLL_UNLOCK_DET_MASK	PLL_UNLOCK_DET_INT interrupt enable. Set 1 to enable interrupt.
16	PLL_UNLOCK_DET_ACK	WRITE ONLY. Acknowledge for the PLL_UNLOCK_DET interrupt. Write 1 to clear
15	PLL_UNLOCK_DET_INT	READ ONLY. PLL in the HDMI PHY has unlocked. Set to 1 when unlock has been detected.
14:4	RESERVED_2	
3	SW_RESET_POL	Polarity of reset sent to HDMI PHY - 0= Active HIGH - 1=Active LOW
2	SW_RESET	Reset value sent to HDMI PHY
1	SW_RESET_PLL_POL	Polarity of reset sent to HDMI PHY PLL - 0= Active HIGH - 1=Active LOW
0	SW_RESET_PLL	Reset value sent to HDMI PHY PLL

0x04A002DC HDMI_CEC_WR_RANGE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x88888888

HDMI CEC write bit range programming. This register will give the flexibility to vary the start bit/bit 0 and 1 bits to be transmitted to be of various width. This register will also give flexibility to vary the signal free time for various states mentioned in CEC spec.

HDMI_CEC_WR_RANGE

Bits	Name	Description
31:28	SF_INIT_NEW_FRAME	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x150 0=0x140, 1=0x145, 2=0x14A, 3=0x14B, 4= 0x14C, 5=0x14D, 6=0x14E, 7=0x14F, 8=0x150, 9=0x151, 10= 0x152, 11=0x153, 12=0x154, 13=0x155, 14=0x158, 15=0x15F.
27:24	SF_INIT_RETRANS	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x90, 0=0x80, 1=0x85, 2=0x8A, 3=0x8B, 4= 0x8C, 5=0x8D, 6=0x8E, 7=0x8F, 8=0x90, 9=0x91, 10= 0x92, 11=0x93, 12=0x94, 13=0x95, 14=0x98, 15=0x9F.
23:20	SF_NEW_INIT	Default to 0x8, When the count with granularity of 0.05 ms reaches 0xF0, 0=0xE0, 1=0xE5, 2=0xEA, 3=0xEB, 4= 0xEC, 5=0xED, 6=0xEE, 7=0xEF, 8=0xF0, 9=0xF1, 10= 0xF2, 11=0xF3, 12 =0xF4, 13 =0xF5,14=0xF8, 15=0xFF.
19:16	BIT_1_LO	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x0A,0=0x2, 1=0x3, 2=0x4, 3=0x5, 4= 0x6, 5=0x7, 6=0x8, 7=0x09, 8=0x0A,9=0xB, 10= 0xC, 11=0xD, 12 =0xE, 13 =0xF,14=0x10, 15=0x12.
15:12	BIT_0_LO	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x1C, 0=0x12, 1=0x14, 2=0x16, 3=0x17, 4= 0x18, 5=0x19, 6=0x1A, 7=0x1B, 8=0x1C,9=0x1D, 10= 0x1E, 11=0x1F, 12 =0x20, 13 =0x22,14=0x24, 15=0x28.
11:8	BIT_TOTAL	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x30,0=0x22, 1=0x23, 2=0x28, 3=0x2B, 4=0x2C,5=0x2D, 5=0x2E, 6=0x2F, 8=0x30, 9=0x32, 10=0x34, 11=0x35, 12=0x36, 13=0x37, 14=0x38, 15=0x40.
7:4	START_LO	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x4A,0= 0x40, 1=0x42, 2=0x44, 3=0x45, 4=0x46, 5=0x47, 6=0x48, 7=0x49, 8=0x4A, 9=0x4B, 10=0x4C, 11=0x4d, 12=0x4e, 13=0x50, 14=0x52,15 = 0x55.
3:0	START_TOTAL	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x5A, 0 = 0x50, 1= 0x52, 2=0x54, 3=0x55, 4=0x56, 5=0x57, 6=0x58, 7=0x59, 8=0x5A, 9=0x5B, 10=0x5C, 11=0x5d, 12=0x5e, 13=0x60, 14=0x62,15 = 0x65.

0x04A002E0 HDMI_CEC_RD_RANGE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x30888888

HDMI CEC read bit range programming. This register will give the flexibility to vary validity check of bit 0 and 1 bits to be read, with various width.

HDMI_CEC_RD_RANGE

Bits	Name	Description
31	RESERVED	
30:24	READ_ACK_START	Default to 0x30, when the count of granularity 0.05m ms reaches 0x30, design takes over the CEC line to acknowledge
23:20	READ_BIT_RANGE_LO	Default to 0x8, When the count with granularity of 0.05 ms reaches 0xF 0 = 0x7, 1= 0x8, 2=0x9, 3=0xa, 4=0xb, 5=0xc, 6=0xd, 7=0xe, 8=0xf, 9=0x10, 10=0x11, 11=0x12, 12=0x13, 13=0x14, 14=0x15, 15= 0x16.
19:16	READ_BIT_RANGE_HI	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x16 0 = 0xe, 1= 0xf, 2=0x10, 3=0x11, 4=0x12, 5=0x13, 6=0x14, 7=0x15, 8=0x16, 9=0x17, 10=0x18, 11=0x19, 12=0x1a, 13=0x1b, 14=0x1c, 15= 0x1d.
15:12	BIT_1_ERR_RANGE_HI	Default to 0x8, When the count with granularity of 0.05 ms reaches 0xf 0 = 0x7, 1= 0x8, 2=0x9, 3=0xa, 4=0xb, 5=0xc, 6=0xd, 7=0xe, 8=0xf, 9=0x10, 10=0x11, 11=0x12, 12=0x13, 13=0x14, 14=0x15, 15= 0x16.
11:8	BIT_1_ERR_RANGE_LO	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x8 0 = 0x0, 1= 0x1, 2=0x2, 3=0x3, 4=0x4, 5=0x5, 6=0x6, 7=0x7, 8=0x8, 9=0x9, 10=0xa, 11=0xb, 12=0xc, 13=0xd, 14=0xe, 15= 0xf.
7:4	BIT_0_ERR_RANGE_HI	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x22 0 = 0x1a, 1= 0x1b, 2=0x1c, 3=0x1d, 4=0x1e, 5=0x1F, 6=0x20, 7=0x21, 8=0x22, 9=0x23, 10=0x24, 11=0x25, 12=0x26, 13=0x27, 14=0x28, 15= 0x29.
3:0	BIT_0_ERR_RANGE_LO	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x1A. 0 = 0x10, 1= 0x12, 2=0x14, 3=0x15, 4=0x16, 5=0x17, 6=0x18, 7=0x19, 8=0x1A, 9=0x1B, 10=0x1C, 11=0x1d, 12=0x1e, 13=0x1f, 14=0x20, 15= 0x21.

0x04A002E4 HDMI_VERSION

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x02010000

HDMI Version number register

HDMI_VERSION

Bits	Name	Description
31:24	MAJOR_VERSION	READ ONLY. This read only field is the major version of HDMI controller. For this design the major version is set to 2
23:16	MINOR_VERSION	READ ONLY. This read only field is the minor version of HDMI controller. For this design the minor version is set to 0
15:0	RESERVED	

0x04A002E8 HDMI_PHY_BIST_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI PHY BIST control register

HDMI_PHY_BIST_0

Bits	Name	Description
31	ENABLE	Global loopback testing enabled to mux onto TMDS lines
30:26	TX_FIXED_PAT_SEL	Pattern select for the pseudo-random bit sequence
25:16	TX_PRBS_POLY	Polynomial of BIST
15:14	TX_PSEL	Bist Channel RGB pattern selection
13:4	TX_PRBS_SEED	BIST seed
3	TX_PRBS_SEED_SEL	PRBS SEED selection
2:1	TX_PATGEN_MODE	Select pattern generator mode. 00=PRBS mode, 01 = 10-bit fixed pattern mode, 10 = 20 bit programmable mode, 11= TMDS mode (or iterative 32 fixed pattern
0	TX_EN_PATGEN	Transmitter Enable for the pseudo-random bit sequence

0x04A002EC HDMI_PHY_BIST_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI PHY BIST control register

HDMI_PHY_BIST_1

Bits	Name	Description
31:27	RESERVED_1	
26	RX_PRBS_GEN_SHORT	BIST checker gen short
25	RX_PRBS_ERR_EN	BIST checker error enable
24	RX_EN_PRBS_CHK	BIST checker enable
23:4	TX_PROG_PAT_20B	- 20 bit programmable pattern
3	RESERVED_2	
2:0	TX_BIST_SEL	Bist Channel selection

0x04A002F0 HDMI_PHY_BIST_2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI PHY BIST control register

HDMI_PHY_BIST_2

Bits	Name	Description
31:18	RESERVED	
17	PRBS_CHK_DONE	READ ONLY. PRBS checker done flag
16	PRBS_CHK_ERR_FLAG	READ ONLY. PRBS checker error flag
15:0	PRBS_CHK_ERR	READ ONLY. PRBS checker error status

0x04A00400 HDMI_PHY_REG_0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000001B

HDMI_PHY_REG_0

Bits	Name	Description
31:8	RESERVED_BITS31_8	

HDMI_PHY_REG_0 (cont.)

Bits	Name	Description
7:6	DESER_SEL	Deserializer selection - 00: ch0-data, ch2-5X clk, ch1-1X clk - 01: ch1-data, ch2-5X clk, ch0-1X clk - 10: ch2-data, ch0-5X clk, ch1-1X clk - 11: Three tx data channels are under test, no loop back Normal operational mode setting is 00 Default value is 00
5:3	DESER_DEL_CTRL	Deserializer programmable delay control - 000: Shortest Delay - 111: Longest Delay (50ps/step) Normal operational mode setting is 011 Default value is 011

2:0	AMUX_OUT_SEL	Analog Mux output selection
		if amux_pad_ena = 1 then:
		- 000: Vbg_1p20v_test
		- 001: 0
		- 010: Iref_50uA_test
		- 011: VDDX_pll_reg_test
		- 100: 0
		- 101: pll_atest
		- 110: 0
		- 111: ib_50u<2>
		if amux_pad_ena = 0 then:
		high impedance output
		Normal operational mode setting is 011
		Default value is 011

0x04A00404 HDMI_PHY_REG_1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000F2

HDMI_PHY_REG_1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	DTEST_MUX_SEL	Dtest mux output selection - 4’b0100 : digital_top dtest signal - 4’b0111 : pll_pixel_clk anything else: 0 Normal operational mode setting is 1111 Default value is 1111

HDMI_PHY_REG_1 (cont.)

Bits	Name	Description
3	RESERVED3	Not used in 28nm (reserved for PLL_GAIN_SEL in 45nm) Normal operational mode setting is 0 Default value is 0
2:0	OUTVOL_SWING_CTRL	.Tx Driver output swing control (Differential Output Swing) - 000: 0.74V - 111:1.9V Normal operational mode setting is 010 Default value is 010

0x04A00408 HDMI_PHY_REG_2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000007F

HDMI_PHY_REG_2

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	RCV_SENSE_EN	RX connection detect enable 0: Disable 1: Enable Normal operational mode setting is 0 Default value is 0
6	PD_PWRGEN	Power-down control of powergen block. 0: Power On 1: Power Down Normal operational mode setting is 0 Default value is 1
5	RESERVED5	Not used in 28nm (reserved for PD_PLL in 45nm) Normal operational mode setting is 0 Default value is 1
4	PD_DRIVE_4	ch2 driver powerdown (preferred name PD_CH2_DRV) Normal operational mode setting is 0 Default value is 1
3	PD_DRIVE_3	ch1 driver powerdown (preferred name PD_CH1_DRV) Normal operational mode setting is 0 Default value is 1
2	PD_DRIVE_2	ch0 driver powerdown (preferred name PD_CH0_DRV) Normal operational mode setting is 0 Default value is 1
1	PD_DRIVE_1	clock driver powerdown (preferred name PD_CLK_DRV) Normal operational mode setting is 0 Default value is 1

HDMI_PHY_REG_2 (cont.)

Bits	Name	Description
0	PD_DESER	Deserialzier power down control Normal operational mode setting is 1 Default value is 1

0x04A0040C HDMI_PHY_REG_3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000003E

HDMI_PHY_REG_3

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6	AMUX_PAD_EN	TPA enable Normal operational mode setting is 0 Default value is 0
5	PD_EM	Emphasize powerdown Normal operational mode setting is 0 Default value is 1
4	PD_CH2_SER	ch2 serializer powerdown Normal operational mode setting is 0 Default value is 1
3	PD_CH1_SER	ch1 serializer powerdown Normal operational mode setting is 0 Default value is 1
2	PD_CH0_SER	ch0 serializer powerdown Normal operational mode setting is 0 Default value is 1
1	PD_CLK_SER	clock serializer powerdown Normal operational mode setting is 0 Default value is 1
0	RESERVED0	Not used in 28nm (reserved for PD_ENABLE in 45nm) Normal operational mode setting is 0 Default value is 0

0x04A00410 HDMI_PHY_REG_4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_4

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	FALL_EDGE_SEL	Fall edge select of serializer Normal operational mode setting is 0 Default value is 0
3	DMUX_PDA_ENA	Dmux enable Normal operational mode setting is 0 Default value is 0
2:0	EM_EN	IDAC PD Normal operational mode setting is 000 Default value is 000

0x04A00414 HDMI_PHY_REG_5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_5

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BIST_PRBS_CFG0	if PATGEN_MODE == 00, this byte is going to be prbs_seed[7:0], otherwise it will be 8 lower bits of first programmable-pattern

0x04A00418 HDMI_PHY_REG_6

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_6

Bits	Name	Description
31:2	RESERVED_BITS31_2	

HDMI_PHY_REG_6 (cont.)

Bits	Name	Description
1:0	BIST_PRBS_CFG1	if PATGEN_MODE == 00, this byte is going to be prbs_seed[9:8], otherwise it will be 2 upper bits of first programmable-pattern

0x04A0041C HDMI_PHY_REG_7

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_7

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BIST_PRBS_CFG2	if PATGEN_MODE == 00, this byte is going to be prbs_poly[7:0], otherwise it will be 8 lower bits of second programmable-pattern

0x04A00420 HDMI_PHY_REG_8

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_8

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	BIST_PRBS_CFG3	if PATGEN_MODE == 00, this byte is going to be prbs_poly[9:8], otherwise it will be 2 upper bits of second programmable-pattern

0x04A00424 HDMI_PHY_REG_9

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_9

Bits	Name	Description
31:8	RESERVED_BITS31_8	

HDMI_PHY_REG_9 (cont.)

Bits	Name	Description
7:3	RESERVED_7_3	Not used in 28nm TX_P10B_SEL Select fixed data patter; refer to appended LUT Normal operational mode setting is 00000 Default value is 00000
2	RESERVED2	Not used in 28nm TX_PRBS10B_SEL tx_prbs10_sel (when tx_fixpat_itr is 0): Choose between PRBS/fixed data pattern. High for PRBS, Data from BIST (TX PRBS Patgen) to be observed at Tx output; long_itr (when tx_fixpat_itr is 1) 1: the 32 fix pattern iterate continue until tx_en_fixpath_itr is disabled. 0 (default), the 32 fix pattern iterate once only; Normal operational mode setting is 0 Default value is 0
1	RESERVED1	Not used in 28nm TX_EN_PRBS10B Enable TX PRBS Patgen. PRBS to be observed at Tx output when tx_prbs10_sel is 1 and tx_fixpat_itr is 0. Normal operational mode setting is 0 Default value is 0
0	RESERVED0	Not used in 28nm TX_FIXPAT_ITR - 1: enable 32 fix pattern iteration, 0: select one of 32 fixed pattern based on tx_p10b_sel[4:0] value Normal operational mode setting is 0 Default value is 0

0x04A00428 HDMI_PHY_REG_10

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_10

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	BIST_ERROR_CLEAR	bist_error_clear clears the upper 13 bits of the error_count register. A rising edge of rx_en_prbs_chk will clear the lower 3 bits of the error_count status register 0--- default 1--- clears upper 13 bits of error_count Normal operational mode setting is 0 Default value is 0

HDMI_PHY_REG_10 (cont.)

Bits	Name	Description
6:5	RESERVED6_5	not used in 28nm RX_PRBS_SEED_SEL Select the seed used in PRBS generation, CHK will follow 00: 10'b10_1011_0010 01: 10'b11_0100_0111 10: 10'b01_1111_0101 11: 10'b10_0001_0000 Normal operational mode setting is 00 Default value is 00
4	RX_EN_PRBS_CHK	Enable the self PRBS checker at the end of LBK path Normal operational mode setting is 0 Default value is 0
3	RESERVED3	not used in 28nm TX_PRBS_SEED_SEL - 0: use same seed select as prbs_seed[9:0] - 1: use default seed 10b'1111_1111 Normal operational mode setting is 0 Default value is 0
2:0	TX_BIST_SEL	TX_BIST_SEL[i] =0: tx data on chan[i] comes from core TX_BIST_SEL[i] =1: tx data on chan[i] comes from BIST patgen Normal operational mode setting is 000 Default value is 000

0x04A0042C HDMI_PHY_REG_11

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_11

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	PIX_CLK_INV_SEL	Preferred name: BIST_CLK_SEL select the clock for BIST operation; - 0: BIST is operated using external clock (hdmi_phy_pixel_clk, which comes from controller) - 1: BIST is operated using internal clock which is generated inside the PHY Normal operational mode setting is 0 Default value is 0
3:2	RESERVED3_2	Normal operational mode setting is 0 Default value is 0

HDMI_PHY_REG_11 (cont.)

Bits	Name	Description
1	RX_PRBS_GEN_SHORT	Length of the PRBD data; High for short pattern Normal operational mode setting is 0 Default value is 0
0	RX_PRBS_ERR_EN	Inject error data at the output of PRBS data generator Normal operational mode setting is 0 Default value is 0

0x04A00430 HDMI_PHY_REG_12

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000007

HDMI_PHY_REG_12

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	PWRDN_B	Global power-down signal for HDMI PHY (excluding PLL block); this is an active low signal, i.e., when PWRDN_B = 0, PHY is in power-down mode. CSR is still accessible Normal operational mode setting is 1 Default value is 0
6	PD_ASIC_CTRL	RESERVED Normal operational mode setting is 0 Default value is 0
5	PHY_SW_RESET	Reset PHY digital state machine. 1: all PHY digital is reset except control register. Normal operational mode setting is 0 Default value is 0
4	FORCE_LOCK	- 1: force the pll_rdy to high Normal operational mode setting is 0 Default value is 0
3:2	RESERVED3_2	not used in 28nm LOOK_STABLE_TIME - 00: 256 refclk cycle, e.g., 256 x 1000/148.5MHz
1	RESERVED1	not used in 28nm PLL_LOCK_DETECT_EN -0: reset pll lock state, phy_rdy goes low1: 0->1 start relock control. Normal operational mode setting is 1 Default value is 1

HDMI_PHY_REG_12 (cont.)

Bits	Name	Description
0	RETIMING_ENABLE	Rising edge of re-time enable will re-lock the re-time logic. 0 - Disable the re-timer logic (read path disabled) 1 - Enable the re-time logic (rising edge causes the read gray-code address generation to re-lock to the write path) Normal operational mode setting is 1 Default value is 1

0x04A00434 HDMI_PHY_REG_BIST_CFG

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_BIST_CFG

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:3	FIXED_PAT_SEL	selection of bist fixed-pattern Normal operational mode setting is 00000 Default value is 00000
2:1	PATGEN_MODE	pattern generator mode: - 00: prbs pattern - 01: 10-bit fixed pattern - 10: 20-bit programmable pattern - 11: tmds iterative mode Normal operational mode setting is 00 Default value is 00
0	EN_PATGEN	enable BIST pattern generator Normal operational mode setting is 0 Default value is 0

0x04A00438 HDMI_PHY_DEBUG_BUS_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_DEBUG_BUS_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	

HDMI_PHY_DEBUG_BUS_SEL (cont.)

Bits	Name	Description
7:0	DEBUG_BUS_SEL	selection of bist debug bus case (DEBUG_BUS_SEL[1:0]) - 3'b000: hdmi_phy_tx_debug_bus = 32'd0; - 3'b001: hdmi_phy_tx_debug_bus = swi_sanity_bus; - 3'b010: hdmi_phy_tx_debug_bus = tx_debug; - 3'b011: hdmi_phy_tx_debug_bus = test_debug; - 3'b100: hdmi_phy_tx_debug_bus = misc_debug; default: hdmi_phy_tx_debug_bus = 32'b0; endcase where tx_debug = {dft_pixel_clk, dft_pll_tx_clk, data_ch2, data_ch1, data_ch0}; test_debug = {13'b0, dft_inputs, dft_bist_clk, lbk_clk, lbk_data_in}; misc_debug = {2'b0, pd_pwrgen, pd_deser, pd_drv_ch, pd_drv_clk, pd_ser_ch, pd_ser_clk, pd_em, phy_rdy, prbs_chk_done, prbs_chk_err_flag, prbs_chk_err}; Normal operational mode setting is 00000000 Default value is 00000000

0x04A0043C HDMI_PHY_REG_MISC0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_MISC0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	DTEST_BUS_SEL	selection of dtest mux case (DTEST_BUS_SEL[3:0]) - 4'b0000 : dtest = 0; - 4'b0001 : dtest = pll_lock; - 4'b0010 : dtest = prbs_chk_done; - 4'b0011 : dtest = prbs_chk_err_flag; - 4'b0100 : dtest = prbs_chk_err[0]; - 4'b0101 : dtest = data_ch0[0]; - 4'b0110 : dtest = data_ch1[0]; - 4'b0111 : dtest = data_ch2[0]; - 4'b1000 : dtest = lbk_data_in[0]; default : dtest = 0; endcase Normal operational mode setting is 00000000 Default value is 00000000

0x04A00440 HDMI_PHY_REG_13

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_13

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BIST_ERROR_7TO0	READ ONLY. PRBS checker error counter LSB Normal operational mode setting is 00000000 Default value is 00000000

0x04A00444 HDMI_PHY_REG_14

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_14

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BIST_ERROR_15TO8	READ ONLY. PRBS checker error counter MSB Normal operational mode setting is 00000000 Default value is 00000000

0x04A00448 HDMI_PHY_REG_15

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_REG_15

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	BIST_CHECK_DONE	READ ONLY. Normal operational mode setting is 0 Default value is 0
3:1	RESERVED3_1	READ ONLY. Normal operational mode setting is 0 Default value is 0

HDMI_PHY_REG_15 (cont.)

Bits	Name	Description
0	RDY	READ ONLY. Indicate the PHY status for initialization. High for ready Normal operational mode setting is 0 Default value is 0

0x04A0044C HDMI_PHY_DEBUS_BUS0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_DEBUS_BUS0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	RESERVED_1	
3:1	DEBUG_BUS0	READ ONLY. Normal operational mode setting is 0 Default value is 0
0	RESERVED_2	

0x04A00450 HDMI_PHY_DEBUS_BUS1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_DEBUS_BUS1

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	RESERVED_1	
3:1	DEBUG_BUS1	READ ONLY. Normal operational mode setting is 0 Default value is 0
0	RESERVED_2	

0x04A00454 HDMI_PHY_DEBUS_BUS2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_DEBUS_BUS2

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	RESERVED_1	
3:1	DEBUG_BUS2	READ ONLY. Normal operational mode setting is 0 Default value is 0
0	RESERVED_2	

0x04A00458 HDMI_PHY_DEBUS_BUS3

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_DEBUS_BUS3

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	RESERVED_1	
3:1	DEBUG_BUS3	READ ONLY. Normal operational mode setting is 0 Default value is 0
0	RESERVED_2	

0x04A00500 HDMI_PHY_PLL_REFCLK_CFG

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000002

HDMI_PHY_PLL_REFCLK_CFG

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	PLL_VCO_DIV	Normal operational mode setting is 000 Default value is 0000

HDMI_PHY_PLL_REFCLK_CFG (cont.)

Bits	Name	Description
3	DBLR_EN	Normal operational mode setting is 0 Default value is 0
2:1	CLK0_DIV	Normal operational mode setting is 01 Default value is 01
0	REF_DIV2_EN	- 1: divide the SR PLL by 2 Normal operational mode setting is 0 Default value is 0

0x04A00504 HDMI_PHY_PLL_CHRG_PUMP_CFG

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000002

HDMI_PHY_PLL_CHRG_PUMP_CFG

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6	DISABLE_CP	Charge pump matching circuit 0: Enable 1: Disable Normal operational mode setting is 0 Default value is 0
5:4	PLL_CP_PMIS	Charge pump pmos mis-match current Normal operational mode setting is 00 Default value is 00
3:2	PLL_CP_NMIS	Charge pump nmos mis-match current Normal operational mode setting is 00 Default value is 00
1:0	CP_IDAC_D	Charge charge pump current Normal operational mode setting is 10 Default value is 10

0x04A00508 HDMI_PHY_PLL_LOOP_FLT_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_LOOP_FLT_CFG0

Bits	Name	Description
31:6	RESERVED_BITS31_6	

HDMI_PHY_PLL_LOOP_FLT_CFG0 (cont.)

Bits	Name	Description
5:1	I_R_SEL	loop filter resistance selection Normal operational mode setting is 10000 Default value is 00000
0	BYP_P2	- 0: Enble C3 1: Bypass C3 Normal operational mode setting is 0 Default value is 0

0x04A0050C HDMI_PHY_PLL_LOOP_FLT_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000033

HDMI_PHY_PLL_LOOP_FLT_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	I_C2_SEL	loop filter C2 selection Normal operational mode setting is 0011 Default value is 0011
3:0	I_C1_SEL	loop filter C1 selection Normal operational mode setting is 0011 Default value is 0011

0x04A00510 HDMI_PHY_PLL_IDAC_ADJ_CFG

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000002B

HDMI_PHY_PLL_IDAC_ADJ_CFG

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:0	I_VI_IDAC	VCO frequency sub-banding Normal operational mode setting is 0101011 Default value is 0101011

0x04A00514 HDMI_PHY_PLL_I_VI_KVCO_CFG

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000006

HDMI_PHY_PLL_I_VI_KVCO_CFG

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4:0	I_VI_KVCO	Kvco selection Normal operational mode setting is 00110 Default value is 00110

0x04A00518 HDMI_PHY_PLL_PWRDN_B

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000003

HDMI_PHY_PLL_PWRDN_B

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	PD_ASIC	RESERVED, not used anymore Normal operational mode setting is 0 Default value is 0
3	PLL_PWRDN_B	Global power-down signal for PLL; this is an active low signal, i.e., when PLL_PWRDN_B = 0, PLL is in power-down mode. CSR is still accessible Normal operational mode setting is 1 Default value is 0
2	REG_VTEST_EN	PLL regulator test voltage output 0: tri-state 1: feed through Normal operational mode setting is 0 Default value is 0
1	PD_PLL	PLL power down Normal operational mode setting is 0 Default value is 1
0	PD_PLL_REG	RESERVED, not used anymore Normal operational mode setting is 1 Default value is 1

0x04A0051C HDMI_PHY_PLL_SDM_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000076

HDMI_PHY_PLL_SDM_CFG0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6	SDM_BYP	Bypass SDM (integer N mode) Normal operational mode setting is 1 Default value is 1
5:0	BYP_DIV	Integer N mode divider value Normal operational mode setting is 110110 Default value is 110110

0x04A00520 HDMI_PHY_PLL_SDM_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000004C

HDMI_PHY_PLL_SDM_CFG1

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6	DITHER_EN	Enable dithering Normal operational mode setting is 1 Default value is 1
5:0	DC_OFFSET	Fractional N mode divider integer portion Normal operational mode setting is 001100 Default value is 001100

0x04A00524 HDMI_PHY_PLL_SDM_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_SDM_CFG2

Bits	Name	Description
31:8	RESERVED_BITS31_8	

HDMI_PHY_PLL_SDM_CFG2 (cont.)

Bits	Name	Description
7:0	FREQ_SEED0	Fractional N mode divider fractional portion, bits 7:0 Normal operational mode setting is 00000000 Default value is 00000000

0x04A00528 HDMI_PHY_PLL_SDM_CFG3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000C0

HDMI_PHY_PLL_SDM_CFG3

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	FREQ_SEED_1	Fractional N mode divider fractional portion, bits 15:8 Normal operational mode setting is 11000000 Default value is 11000000

0x04A0052C HDMI_PHY_PLL_SDM_CFG4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_SDM_CFG4

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	FREQ_SEED_2	Fractional N mode divider fractional portion, bits 17:16 Normal operational mode setting is 00 Default value is 00

0x04A00530 HDMI_PHY_PLL_SSC_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000009A

HDMI_PHY_PLL_SSC_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	SSC_BYP	Spread-Spectrum Clock generation Normal operational mode setting is 1 Default value is 1
6:0	KDIV	Triangular SSC clock frequency Normal operational mode setting is 0011010 Default value is 0011010

0x04A00534 HDMI_PHY_PLL_SSC_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_SSC_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	TRIANGULAR_INCR0	SSC triangle incr, bits 7:0 Normal operational mode setting is 00000000 Default value is 00000000

0x04A00538 HDMI_PHY_PLL_SSC_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_SSC_CFG2

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	TRIANGULAR_INCR1	SSC triangle incr, bits 9:8 Normal operational mode setting is 00 Default value is 00

0x04A0053C HDMI_PHY_PLL_SSC_CFG3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000020

HDMI_PHY_PLL_SSC_CFG3

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6	TRIANGULAR_TESTMODE	Test for SIN shape SSC Normal operational mode setting is 0 Default value is 0
5:0	TRIANGULAR_STEPS	SSC triangle steps Normal operational mode setting is 100000 Default value is 100000

0x04A00540 HDMI_PHY_PLL_LOCKDET_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000010

HDMI_PHY_PLL_LOCKDET_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	PLL_LCKDET_MCNT	mpll lock detect maximum count value for the fref and fdiv counters Normal operational mode setting is 00010000 Default value is 00010000

0x04A00544 HDMI_PHY_PLL_LOCKDET_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000001A

HDMI_PHY_PLL_LOCKDET_CFG1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	PLL_LOCKDET_WAIT	Number of cycles to wait (2 cycles incremental) Normal operational mode setting is 00011010 Default value is 00011010

0x04A00548 HDMI_PHY_PLL_LOCKDET_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000000D

HDMI_PHY_PLL_LOCKDET_CFG2

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	PLL_SW_RESET	PLL software reset; resets all blocks except CSR Normal operational mode setting is 0 Default value is 0
6	FORCE_PLL_LOCK	Force PLL lockdet signal become high Normal operational mode setting is 0 Default value is 0
5:2	PLL_LOCKDET_PPM	PPM setting Normal operational mode setting is 0011 Default value is 0011
1	PLL_LOCKDET_CTRL	control phy_tx_lockdet Normal operational mode setting is 0 Default value is 0
0	PLL_LOCKDET_EN	Enable lockdet Normal operational mode setting is 1 Default value is 1

0x04A0054C HDMI_PHY_PLL_VCOCAL_CFG0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000000E6

HDMI_PHY_PLL_VCOCAL_CFG0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	I_VCO_FREQ0	Target Calibration VCO frequency, bits 7:0 Normal operational mode setting is 11100110 Default value is 11100110

0x04A00550 HDMI_PHY_PLL_VCOCAL_CFG1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000002

HDMI_PHY_PLL_VCOCAL_CFG1

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2:0	I_VCO_FREQ1	Target Calibration VCO frequency, bits 10:8 Normal operational mode setting is 010 Default value is 010

0x04A00554 HDMI_PHY_PLL_VCOCAL_CFG2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000002B

HDMI_PHY_PLL_VCOCAL_CFG2

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	I_KV_COUNT0	Target Calibration KVCO Use This equation: KV_COUNT = kvco *vdd/6, bits 7:0 Normal operational mode setting is 00101011 Default value is 00101011

0x04A00558 HDMI_PHY_PLL_VCOCAL_CFG3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_VCOCAL_CFG3

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	I_KV_COUNT1	Target Calibration KVCO Use This equation: KV_COUNT = kvco *vdd/6, bits 9:8 Normal operational mode setting is 00 Default value is 00

0x04A0055C HDMI_PHY_PLL_VCOCAL_CFG4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000086

HDMI_PHY_PLL_VCOCAL_CFG4

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	I_DIV_REF0	Reference divider number to get to 5us measurement period, bits 7:0 Normal operational mode setting is 10000110 Default value is 10000110

0x04A00560 HDMI_PHY_PLL_VCOCAL_CFG5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_VCOCAL_CFG5

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	I_DIV_REF1	Reference divider number to get to 5us measurement period, bits 9:8 Normal operational mode setting is 00 Default value is 00

0x04A00564 HDMI_PHY_PLL_VCOCAL_CFG6

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000033

HDMI_PHY_PLL_VCOCAL_CFG6

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	I_OPEN_LOOP	Configure PLL in open loop mode Normal operational mode setting is 0 Default value is 0

HDMI_PHY_PLL_VCOCAL_CFG6 (cont.)

Bits	Name	Description
6:5	I_WAITTIME	Idle time for VCO frequency adjustment during Calibration Normal operational mode setting is 01 Default value is 01
4:2	I_VREF_CONF	Calibration Reference voltage setting Normal operational mode setting is 100 Default value is 100
1:0	I_CAL_MODE	Calibration Mode Normal operational mode setting is 11 Default value is 11

0x04A00568 HDMI_PHY_PLL_VCOCAL_CFG7

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_VCOCAL_CFG7

Bits	Name	Description
31:1	RESERVED_BITS31_1	N/A
0	I_POS_KVSLP	Slope polarity of KVCO Normal operational mode setting is 0 Default value is 0

0x04A0056C HDMI_PHY_PLL_DEBUG_SEL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	

HDMI_PHY_PLL_DEBUG_SEL (cont.)

Bits	Name	Description
7:0	PLL_DEBUG_SEL	case (PLL_DEBUG_SEL[1:0]) - 2'b00: pll_debug_bus = 32'd0; - 2'b01: pll_debug_bus = {8'b0, swi_sanity_bus}; - 2'b10: pll_debug_bus = {8'b0, digital_debug}; - 2'b11: pll_debug_bus = {8'b0, analog_debug}; endcase where: digital_debug = {ssc_div, pll_lockdet, O_DEBUG}; analog_debug = {15'b0, pll_sleep_b, O_PD_MPLL, pll_pwrdn_b, reset_pll_int, fref_clk_div2, fdiv_clk_div2, fref_clk, fdiv_clk, I_VCOCLK_DIV5}; Normal operational mode setting is 00000000 Default value is 00000000

0x04A00570 HDMI_PHY_PLL_MISC0

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_MISC0

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04A00574 HDMI_PHY_PLL_MISC1

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_MISC1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04A00578 HDMI_PHY_PLL_MISC2

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_MISC2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04A0057C HDMI_PHY_PLL_MISC3

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_MISC3

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04A00580 HDMI_PHY_PLL_MISC4

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_MISC4

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04A00584 HDMI_PHY_PLL_MISC5

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_MISC5

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04A00588 HDMI_PHY_PLL_MISC6

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_MISC6

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04A0058C HDMI_PHY_PLL_DEBUG_BUS0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_DEBUG_BUS0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	O_DEBUG0	READ ONLY. Default value is 00000000

0x04A00590 HDMI_PHY_PLL_DEBUG_BUS1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_DEBUG_BUS1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	O_DEBUG1	READ ONLY. Default value is 00000000

0x04A00594 HDMI_PHY_PLL_DEBUG_BUS2

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_DEBUG_BUS2

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	O_DEBUG2	READ ONLY. Default value is 0

0x04A00598 HDMI_PHY_PLL_STATUS0

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_STATUS0

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	PLL_LOCKDET	READ ONLY. Status of pll_lockdet signal Default value is 0

0x04A0059C HDMI_PHY_PLL_STATUS1

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

HDMI_PHY_PLL_STATUS1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x04A00360 CEC_COMPL_CTL

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Programming to enable/disable compliance related features

CEC_COMPL_CTL

Bits	Name	Description
31:4	RESERVED	

CEC_COMPL_CTL (cont.)

Bits	Name	Description
3	RD_BIT_COUNT_RESET_ENABLE	Enable change to reset bit counter in total bit read errors
2	WR_BIT_COUNT_RESET_ENABLE	Enable change to reset bit counter in transmission errors
1	WRITE_CHECK_ENABLE	Enable changes to delay comparison of CEC_IO_OE and CEC_IO_Y for compliance of CEC 7.1-3
0	BIT_TOTAL_ERR_ENABLE	Enable changes to hold line low following bit total error in compliance of CEC 9.5-1

0x04A00364 CEC_RD_START_RANGE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x88888888

Start bit range programming for CEC read machine

CEC_RD_START_RANGE

Bits	Name	Description
31:28	READ_STR_TOT_ERR_HI	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x5E 0 = 0x4, 1= 0x18, 2=0x0A, 3=0x1A, 4=0x2A, 5=0x3A, 6=0x4A, 7=0x50, 8=0x5E, 9=0x60, 10=0x62, 11=0x64, 12=0x68, 13=0x6A, 14=0x6E, 15= 0x70.
27:24	READ_STR_TOT_ERR_LO	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x56 0 = 0x4, 1= 0x18, 2=0x0A, 3=0x1A, 4=0x2A, 5=0x3A, 6=0x4A, 7=0x50, 8=0x56, 9=0x58, 10=0x5A, 11=0x5C, 12=0x60, 13=0x62, 14=0x68, 15= 0x70.
23:20	READ_STR_0_ERR_HI	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x4E 0 = 0x4, 1= 0x18, 2=0x2A, 3=0x30, 4=0x38, 5=0x3A, 6=0x40, 7=0x46, 8=0x4E, 9=0x50, 10=0x52, 11=0x54, 12=0x56, 13=0x58, 14=0x5A, 15= 0x5E.
19:16	READ_STR_0_ERR_LO	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x46 0 = 0x4, 1= 0x18, 2=0x2A, 3=0x30, 4=0x38, 5=0x3A, 6=0x40, 7=0x44, 8=0x46, 9=0x4A, 10=0x4E, 11=0x54, 12=0x56, 13=0x58, 14=0x5A, 15= 0x5E.
15:12	READ_STR_TOT_HI	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x5E 0 = 0x4, 1= 0x18, 2=0x0A, 3=0x1A, 4=0x2A, 5=0x3A, 6=0x4A, 7=0x50, 8=0x5E, 9=0x60, 10=0x62, 11=0x64, 12=0x68, 13=0x6A, 14=0x6E, 15= 0x70.
11:8	READ_STR_TOT_LO	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x56 0 = 0x4, 1= 0x18, 2=0x0A, 3=0x1A, 4=0x2A, 5=0x3A, 6=0x4A, 7=0x50, 8=0x56, 9=0x58, 10=0x5A, 11=0x5C, 12=0x60, 13=0x62, 14=0x68, 15= 0x70.

CEC_RD_START_RANGE (cont.)

Bits	Name	Description
7:4	READ_STR_0_HI	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x4E 0 = 0x4, 1= 0x18, 2=0x2A, 3=0x30, 4=0x38, 5=0x3A, 6=0x40, 7=0x46, 8=0x4E, 9=0x50, 10=0x52, 11=0x54, 12=0x56, 13=0x58, 14=0x5A, 15= 0x5E.
3:0	READ_STR_0_LO	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x46 0 = 0x4, 1= 0x18, 2=0x2A, 3=0x30, 4=0x38, 5=0x3A, 6=0x40, 7=0x44, 8=0x46, 9=0x4A, 10=0x4E, 11=0x54, 12=0x56, 13=0x58, 14=0x5A, 15= 0x5E.

0x04A00368 CEC_RD_TOTAL_RANGE

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000088

Total bit range programming for CEC read machine

CEC_RD_TOTAL_RANGE

Bits	Name	Description
31:8	RESERVED	
7:4	READ_TOT_ERR_HI	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x37 0 = 0x4, 1= 0x18, 2=0x1A, 3=0x28, 4=0x2A, 5=0x30, 6=0x32, 7=0x24, 8=0x37, 9=0x3A, 10=0x40, 11=0x4A, 12=0x50, 13=0x5A, 14=0x60, 15= 0x6A.
3:0	READ_TOT_ERR_LO	Default to 0x8, When the count with granularity of 0.05 ms reaches 0x22 0 = 0x4, 1= 0x08, 2=0x0X, 3=0x10, 4=0x12, 5=0x16, 6=0x1A, 7=0x1E, 8=0x22, 9=0x26, 10=0x2A, 11=0x3A, 12=0x4A, 13=0x5A, 14=0x60, 15= 0x6A.

0x04A0036C CEC_RD_ERR_RESP_LO

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000004A

CEC read response low time period

CEC_RD_ERR_RESP_LO

Bits	Name	Description
31:7	RESERVED	
6:0	READ_ERR_RESP_LO	Default 0x4A, When the count with granularity of 0.05ms reaches 0x4A, This is ot hold the line low when the total bit time has error

0x04A00370 CEC_WR_CHECK_CONFIG

Type: Read/Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000001

CEC write check for line contention configuration

CEC_WR_CHECK_CONFIG

Bits	Name	Description
31:3	RESERVED	
2:0	WRITE_CHECK_COUNT	Default 0x1. Program in counts of how many reference clock pulses later the check for line contention is done. 0x1 = 100us. 0x2 = 150us. 0x3 = 200us. 0x4 = 250us (max rise time as per CEC spec). Disable WRITE_CHECK_ENABLE for 50us check.

14.10 IMEM MM SS Registers (0x04B00000 IMEM_MMSS_BASE)

This section contains the IMEM registers.

14.10.1 IMEM Configuration register

0x04B00000 IMEM_MMSS_IMEM_CONFIG

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00000001

General configuration register for IMEM. This register sets the IMEM accessibility for Graphics and AXI.

Power up value is based on parameters provided.

NOTE

a. All banks are 8k x 64 in size.

b. GRP and AXI memory configurations are 64-bits wide.

c. If Graphics interface is not required, set the IMEM_CONFIG_POR parameter to all AXI setting (2'b01).

IMEM_MMSS_IMEM_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	IMEM_CONFIG	(Graphics Interface = 256kbytes) (AXI Interface (and trace) = 256kbytes) (Graphics Interface = 128kbytes) (AXI Interface (and trace) = 128kbytes) Banks 0 and 1 are allocated to Graphics. Banks 2 and 3 are allocated to AXI. (Graphics Interface = 128kbytes) (AXI Interface (and trace) = 128kbytes) Banks 0 and 1 are allocated to AXI. Banks 2 and 3 are allocated to Graphics. SW : RW, HW: R 0x0: All graphics (Dedicated all to Graphics) 0x1: All axi (Dedicated all to AXI) 0x2: 0_1_Graphics_2_3_AXI 0x3: 0_1_AXI_2_3_Graphics

14.10.2 IMEM AXI Trace Configuration register

0x04B00004 IMEM_MMSS_IMEM_AXI_TRACE_CONFIG

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00000000

This register is used to enable and control the AXI trace to IMEM.

IMEM_MMSS_IMEM_AXI_TRACE_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	AXI_TRACE_ADDR_WRAP_EN	1-Enables AXI trace address to wrap
0	AXI_TRACE_EN	1-Enables AXI trace to IMEM

0x04B00008 IMEM_MMSS_IMEM_AXI_TRACE_ADDR_CNTR

Type: Read
Clock: CORE_CLOCK
Reset State: 0x00000000

This register is used to read the AXI Trace Address counter value.

IMEM_MMSS_IMEM_AXI_TRACE_ADDR_CNTR

Bits	Name	Description
31:16	RESERVED_BITS31_16	
15:0	AXI_TRACE_ADDR_CNTR	Current AXI Trace address

0x04B0000C IMEM_MMSS_IMEM_AXI_TRACE_WRAP_STATUS

Type: Read
Clock: CORE_CLOCK
Reset State: 0x00000000

This register is used to read the AXI Trace Address wrap status bit.

IMEM_MMSS_IMEM_AXI_TRACE_WRAP_STATUS

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	AXI_TRACE_WRAP_STATUS	0x1: AXI trace address wrapped 0x0: AXI trace address not wrapped

0x04B00010 IMEM_MMSS_IMEM_AXI_BASE_ADDR_OFFSET

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00002E00

This register is used to set the AXI Base Address offset value in order to relocate the IMEM AXI memory within the space allowed by the interconnect. The POR value of this register is based on the parameter - IMEM_BASE_ADDRESS. In case of MPSS, this is set to 0x5800. This should be set to the upper 16 bits of the Imem base address. Based on the size of the Imem, the relevant bits of this register are used for decoding the address.

IMEM_MMSS_IMEM_AXI_BASE_ADDR_OFFSET

Bits	Name	Description
31:16	RESERVED_BITS31_16	
15:0	IMEM_AXI_BASE_ADDRESS_OFFSET	IMEM AXI base address offset for decode

14.10.3 IMEM Syndrome registers

0x04B00020 IMEM_MMSS_IMEM_ERR_ADDRESS_MS

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x000000000000

The IMEM_ERR_ADDRESS_MS register contains the upper bits of the address of the request that caused the bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, it will be locked until bit 8 of the ERR_CODE register is written to clear the error.

IMEM_MMSS_IMEM_ERR_ADDRESS_MS

Bits	Name	Description
31:16	RESERVED_BITS31_16	

IMEM_MMSS_IMEM_ERR_ADDRESS_MS (cont.)

Bits	Name	Description
15:0	ERROR_ADDRESS_31_16	Bits 31:16 of the address of the request that caused the bus error.

0x04B00024 IMEM_MMSS_IMEM_ERR_ADDRESS_LS

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x00000000

The IMEM_ERR_ADDRESS_LS register contains the lower bits of the address of the request that caused the AXI GE bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, the register will be locked until bit 8 of the ERR_CODE register is written to clear the error.

IMEM_MMSS_IMEM_ERR_ADDRESS_LS

Bits	Name	Description
31:16	RESERVED_BITS31_16	
15:3	ERROR_ADDRESS_15_3	Bits 15:3 of the address of the request that caused the bus error
2:0	RESERVED_BITS2_0	Reserved if not implemented otherwise include with error address.

0x04B00028 IMEM_MMSS_IMEM_ERR_APACKET_MS

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x00000000

The IMEM_ERR_APACKET_MS register provides various data about the request that caused the AXI GE bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, it will be locked until bit 8 of the ERR_CODE register is written to clear the error.

IMEM_MMSS_IMEM_ERR_APACKET_MS

Bits	Name	Description
31:20	RESERVED_BITS31_20	
19:18	ERROR_ALOCK_1_0	The ALOCK of the request that caused the bus error
17	ERROR_ABURST	The ABURST of the request that caused the bus error
16:12	ERROR_PORTID_4_0	The Port ID of the request that caused the bus error.
11:5	ERROR_ATID_6_0	The Transfer ID of the request that caused the bus error.

IMEM_MMSS_IMEM_ERR_APACKET_MS (cont.)

Bits	Name	Description
4	ERROR_AWRITE	The awrite of the request that caused bus error
3:0	ERROR_ALEN	The burst length of the request that caused bus error

0x04B0002C IMEM_MMSS_IMEM_ERR_APACKET_LS

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x00000000

The IMEM_ERR_APACKET_LS register provides various data about the request that caused the AXI GE bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, the register will be locked until bit 8 of the ERR_CODE register is written to clear the error.

IMEM_MMSS_IMEM_ERR_APACKET_LS

Bits	Name	Description
31:24	RESERVED_BITS31_24	
19:9	ERROR_AMID_10_0	The master ID of the request that caused the bus error (The higher order bits will be set to 0 for MID width < 7)
8:5	ERROR_ATYPE_3_0	The ATYPE of the request that caused the bus error
4	ERROR_APROTNS	The APROTNS of the request that caused the bus error
3:0	RESERVED_BITS_3_0	

0x04B00030 IMEM_MMSS_IMEM_ERR_CODE

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00000000

The IMEM_ERR_CODE register provides additional data about the bus error. This register will be updated by hardware upon the detection of an MPU error or address decode error. Once set, the register will be locked until bit 8 of the ERR_CODE register is written to clear the error.

Additionally, each slave or AXI interconnect which is capable of detecting an error is also required to have a single programmable register which can be used to optionally interrupt the ARM9 or Scorpion Processor core. This interrupt mechanism is required since write transfers may be posted on the bus and the AXI transfer may complete prior to the occurrence of the error in the AXI interconnect or slave device. The interrupt from the AXI interconnect and the AXI slave devices will be directed to both the modem and application processor's interrupt controllers. The interrupt output of the slave device shall be driven from bit 3 of the ERR_CODE register above. To clear the interrupt, it will be necessary to clear the ERR_CODE register by writing to bit 8

(ERROR_CLEAR) of the ERR_CODE register. This will clear the ERROR field (bit 3) and also unlock the ERR_ADDRESS, ERR_APACKET, and ERR_CODE registers so that a subsequent error can be recoded in these registers.

IMEM_MMSS_IMEM_ERR_CODE

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8	ERROR_CLEAR	Writing a ’1’ to this bit will clear the bus error status bit.
7:4	RESERVED_BIT7_4	
3	ERROR	Error Status bit to indicate that an error has occurred.
2	RESERVED_BIT2	
1	MPU_ERROR	0x1: memory protection error: This should be ignored, as XPU has separate syndrome registers for this indication.
0	ADDRESS_DECODE_ERRO R	0x1: slave address decode error

0x04B00034 IMEM_MMSS_IMEM_ERR_IRQ_MSK

Type: Read/Write
Clock: CORE_CLOCK
Reset State: 0x00000001

This register is used to block decoder interrupt to ARM9 or Scorpion. Note that even if this is disabled, xpu can still drive interrupts.

IMEM_MMSS_IMEM_ERR_IRQ_MSK

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	PROCESSOR_IRQ_MASK	1 disables bus error interrupt to Processor

0x04B00040 IMEM_MMSS_IMEM_CLK_ON_EN

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x00000000

This register is used to enable/disable the clock_on circuitry. If disabled, clock on is always high.

IMEM_MMSS_IMEM_CLK_ON_EN

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	AHB_CLK_ON_EN	1 will enable ahb clkon to go low
0	AXI_CLK_ON_EN	1 will enable the timer countdown

0x04B00044 IMEM_MMSS_IMEM_CLK_ON_TIME

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x000003FF

This register sets the starting time for a binary countdown in clock cycles.

IMEM_MMSS_IMEM_CLK_ON_TIME

Bits	Name	Description
31:10	RESERVED_BITS31_1	
9:0	CLK_ON_TIME_9_0	10 bits to count down from, for a max of 1024

0x04B00048 IMEM_MMSS_IMEM_FSCGC_TIMERS

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x000000FF

This register sets the starting time for a binary countdown in clock cycles.

IMEM_MMSS_IMEM_FSCGC_TIMERS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	WAKEUP_COUNTER_3_0	4 bit count down, must be 20ns
3:0	TO_SLEEP_COUNTER_3_0	4 bit count down, must be 20ns

0x04B0004C IMEM_MMSS_IMEM_FSCGC_CONTROL

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x0000003F

Controls for head switch and periphery within IMEM.

IMEM_MMSS_IMEM_FSCGC_CONTROL

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8:6	HALT_CLOCK_2_0	Gates the clock to individual RAMS
5:3	CORE_ON_2_0	RAM Core will remain on if this is 1 (for individual rams)
2:0	PERIF_ON_2_0	RAM Periphery will remain on if this is 1 (for individual rams)

0x04B00050 IMEM_MMSS_IMEM_EX_FSCGC_CONTROL

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x0000FFFF

Controls for head switch and perfory outside of IMEM.

IMEM_MMSS_IMEM_EX_FSCGC_CONTROL

Bits	Name	Description
31:22	RESERVED_BITS31_22	
23:16	HALT_CLOCK_7_0	Gates the clock to individual RAMS
15:8	CORE_ON_7_0	RAM Core will remain on if this is 1 (for individual rams)
7:0	PERIF_ON_7_0	RAM Periphery will remain on if this is 1 (for individual rams)

0x04B00054 IMEM_MMSS_IMEM_RAM_CONFIG

Type: Read/Write
Clock: BUS_CLOCK
Reset State: 0x00000004

This register configures the access to the GMEM.

IMEM_MMSS_IMEM_RAM_CONFIG

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	EX_RAM_CLK_EN	GMEM async FIFO clock enable

IMEM_MMSS_IMEM_RAM_CONFIG (cont.)

Bits	Name	Description
1:0	EX_RAM_CONFIG_1_0	External ram access configuration 0x0: No GMEM allocated to A_2 0x1: 256K of GMEM allocated to AXI 0x2: All GMEM allocated to _2

14.10.4 Internal Memory Misc

0x04B00038 IMEM_MMSS_IMEM_MEM_ACC_CFG

Type: Read Only
Clock: CORE_CLOCK
Reset State: 0x00000000

This register is used to configure the acc pins of the RAM for programming the sense amp.

IMEM_MMSS_IMEM_MEM_ACC_CFG

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	ACC_CFG	

14.11 IMEM MM SS XPU Registers (0x04B00000 IMEM_MMSS_BASE)

This section contains the IMEM XPU registers.

0x04B01000+ 4*n IMEM_MMSS_MPU_PRTn_RACR, n=[0..3]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU. These registers include a single bit per VMID granting read access

IMEM_MMSS_MPU_PRTn_RACR

Bits	Name	Description
31:0	RE	Read enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read access to the registers in the associated resource group.

0x04B01400+ 4*n IMEM_MMSS_MPU_PRTn_WACR, n=[0..3]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

These registers exist only for the case when MPU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type MPU.

IMEM_MMSS_MPU_PRTn_WACR

Bits	Name	Description
31:0	WE	Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID write access to the registers in the associated resource group.

0x04B01800+ 4*n IMEM_MMSS_MPU_PRTn_START, n=[0..3]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition Start Address Register. This register contains the start address of the partition. Only the bit numbers indicated by MPU_IDR[MSb] through MPU_IDR[LSb] are valid and physically exist.

IMEM_MMSS_MPU_PRTn_START

Bits	Name	Description
31:25	RESERVED_31_25	Reserved
24:12	ADDR	MPU Partition Start Address
11:0	RESERVED_11_0	Reserved

0x04B01C00+4*n IMEM_MMSS_MPU_PRTn_END, n=[0..3]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Partition End Address Register. This register contains the start address of the partition.Only the bit numbers indicated by MPU_IDR[MSB] through MPU_IDR[LSB] are valid and physically exist.

IMEM_MMSS_MPU_PRTn_END

Bits	Name	Description
31:25	RESERVED_31_25	Reserved
24:12	ADDR	MPU Partition End Address
11:0	RESERVED_11_0	Reserved

0x04B01F80 IMEM_MMSS_MPU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

MPU Configuration Register: This register includes fields governing various MPU behaviors.

IMEM_MMSS_MPU_CR

Bits	Name	Description
31:2	RESERVED31_2	Reserved

IMEM_MMSS_MPU_CR (cont.)

Bits	Name	Description
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set MPU_ESR. MPU_EAR and MPU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set MPU_ESR. MPU_EAR and MPU_ESYNR0 updated with address and syndrome of error.
2	MPUEIE	MPU Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the MPU. Interrupt output is asserted if MPU_CR[MPUEIE] = 1 and any bit is set in MPU_ESR.
1	MPUERE	MPU Error Report Enable. MPUERE = 0 causes the MPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master. MPUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective MPU port. Errors from either port are terminated by the MPU as RAZ/WI Both client and configuration port errors are recorded in MPU_ESR, independent of the value of MPU_CR[MPUERE]
0	MPUE	MPU Enable. Governs whether MPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures MPU and the MID to VMID mapping tables.

0x04B01F84 IMEM_MMSS_MPU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the MPU, for both the client port and the configuration port. Client port addresses are 32 bits width and configuration port addresses are 12 bits wide (the width of the configuration address port).

IMEM_MMSS_MPU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x04B01F88 IMEM_MMSS_MPU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the MPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the MPU's interrupt output (when enabled by MPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the MPU_ESYNRn registers, which are merely the "syndrome" of an error indicated by MPU_ESR.

IMEM_MMSS_MPU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x04B01F8C IMEM_MMSS_MPU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Restore Register. This register is an aliased address for the MPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

IMEM_MMSS_MPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while MPU_ESR[CFG, CLIENT] still non-zero. MPU_EAR and MPU_ESYNRn registers (and MPU_ESR itself, except for the MULTI bit) "lock" upon first error, MPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while MPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error associated with a client port request.
0	CFG	Configuration Port Error. Indicates error associated with a configuration port request.

0x04B01F90 IMEM_MMSS_MPU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

IMEM_MMSS_MPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x04B01F94 IMEM_MMSS_MPU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the MPU, for both the client port and the configuration port.

IMEM_MMSS_MPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x04B01FF4 IMEM_MMSS_MPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

MPU Revision Register: This register provides major/minor revision codes for the implementation.

IMEM_MMSS_MPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x04B01FF8 IMEM_MMSS_MPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x180C2C03

MPU ID Register: Read-only register that defines various configuration attributes of the MPU instance.

IMEM_MMSS_MPU_IDR

Bits	Name	Description
31:29	RESERVED31_29	Reserved
28:24	MSB	Indicates most significant address bit number used in START/END address comparisons.
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used in START/END address comparisons.
15:14	RESERVED15_12	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only MPU_PRTn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate MPU_PRTn_RACR and MPU_PRTn_WACR registers govern read vs. write access. For single VMID, MPU_PRTn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields

IMEM_MMSS_MPU_IDR (cont.)

Bits	Name	Description
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. MPU_PRTn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMD type access control. MPU_PRTn_xACR registers include separate bit per VMID (32 bits) for governing access.
9	RESERVED9	Reserved
8:0	NPRT	Number of partitions. Indicates the number of partitions (minus 1) supported by the MPU. Values range from 0-223 (1-224 partitions)

0x04B01FFC IMEM_MMSS_MPU_MPU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

MPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the MPU (including the MPU_MPU_ACR itself).

IMEM_MMSS_MPU_MPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the MPU's 4KB address region (including the MPU_MPU_ACR itself). For single VMID type MPUs (MPU_IDR[MV] = 0) the MPU_MPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

14.12 ROTATOR Registers (0x04E00000 ROTATOR_BASE)

This section describes the Rotator registers (also know as Offline Rotator). All Rotator registers are accessible by the ARM CPU through the Slow Peripheral Bus APQ interface. For read accesses, the number of cycles before data is available is variable depending on the register being read. The APQ register interface uses a request-ack protocol to hold the bus until the read data is valid, so wait states are not applicable. Writes to these registers take effect immediately.

The registers are grouped into distinct groups, according to their function.

- Interrupts (0x0000 - 0x002C)
- Operation Control Registers (0x0030 - 0x007C)
- Clock Control Registers (0x0080 - 0x008C)
- MGEN2MAXI control registers (0x00400 - 0x004FC)
- Rotator Sub-Block Registers (0x1000 - 0xFFFF)
- Command Registers (0x1000 - 0x1FFF)
- Tile Fetch Registers (0x2000 - 0x2FFF)
- Test Misr Registers (0xD000 - 0xDFFF)

14.12.1 Interrupt registers

0x04E00020 ROTATOR_INTR_ENABLE

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_INTR_ENABLE register is used to enable the ROTATOR interrupts.

ROTATOR_INTR_ENABLE

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2:0	INTR_ENABLE	Setting (1) a specific bit will enable the respective interrupt source within the ROTATOR to send a level interrupt out of the ROTATOR. Clearing (0) that bit will disable it from generating the ROTATOR interrupt. Bit0: Rotator done Bit 1: AXI Bus Error Bit 2 : DMI buffer Acknowledge

0x04E00024 ROTATOR_INTR_STATUS

Type: Read
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_INTR_STATUS register is the ROTATOR interrupt status register.

ROTATOR_INTR_STATUS

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2:0	INTR_STATUS	When an ROTATOR interrupt occurs, then reading this register will indicate what caused the interrupt since that each bit indicates the source of the interrupt that had happened. If multiple interrupt sources had happened, then multiple bits of this register will be. Bit0: Rotator done Bit 1: AXI Bus Error Bit 2 : DMI buffer Acknowledge

0x04E00028 ROTATOR_INTR_CLEAR

Type: Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_INTR_CLEAR register is used to clear the ROTATOR interrupts.

ROTATOR_INTR_CLEAR

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2:0	INTR_CLEAR	To clear the interrupt, make sure the interrupt has occurred, and then clear (0) this bit. Setting (1) a specific bit will clear the respective interrupt. A read from this register would indicate if the respective interrupt source is cleared (the bit is set (1)). So, at power up, it would read all 1's. Bit0: Rotator done Bit 1: AXI Bus Error Bit 2 : DMI buffer Acknowledge

14.12.2 Operation control registers

0x04E00030 ROTATOR_START

Type: Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_START register is used to kick start the image rotation..

ROTATOR_START

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	ROTATE_START	A write to this register will start the image rotation.

0x04E00034 ROTATOR_INTF_EN

Type: Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_INTF_SEL register is used to enable DMI and Context Queue interface.

This register is expected to program before kicking off Rotator.

ROTATOR_INTF_EN

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28	DMI_BUF_UPDATE_DIS	This bit is for supporting synchronization of multiple DMI buffer switching events to multiple of MDP pipes. if the bit is ’1’, current DMI buffer switching will be pended and it will be issued when next frame with the bit is ’0’.
27	RESERVED_BIT27	
26:24	MDP_PIPE_ID	MDP PIPE ID selection that the context input will be connected proper DMI interface if the DMI enable is set. 0x7: Non-DMI case for Context only 0x6: Rotator context connects to MDP DMA_E DMI interface 0x5: Rotator context connects to MDP DMA_S DMI interface 0x4: Rotator context connects to MDP DMA_P DMI interface 0x3: Rotator context connects to MDP RGB2 DMI interface 0x2: Rotator context connects to MDP RGB1 DMI interface 0x1: Rotator context connects to MDP VG2 DMI interface 0x0: Rotator context connects to MDP VG1 DMI interface

ROTATOR_INTF_EN (cont.)

Bits	Name	Description
23:22	RESERVED_BITS23_22	
21:20	CONTEXT_ID	Context ID selection for context start (0
19	RESERVED_BIT19	
18	CONTEXT_SKIP_DMA_E_EN	decide how to deal with next frame in context queue if rotator DMI buffers are full and MDP pipe displaying rate is slower than rotator. 0x1: skip mode 0x0: no skip mode
17	CONTEXT_SKIP_DMA_S_EN	decide how to deal with next frame in context queue if rotator DMI buffers are full and MDP pipe displaying rate is slower than rotator. 0x1: skip mode 0x0: no skip mode
16	CONTEXT_SKIP_DMA_P_EN	decide how to deal with next frame in context queue if rotator DMI buffers are full and MDP pipe displaying rate is slower than rotator. 0x1: skip mode 0x0: no skip mode
15	CONTEXT_SKIP_RGB2_EN	decide how to deal with next frame in context queue if rotator DMI buffers are full and MDP pipe displaying rate is slower than rotator. 0x1: skip mode 0x0: no skip mode
14	CONTEXT_SKIP_RGB1_EN	decide how to deal with next frame in context queue if rotator DMI buffers are full and MDP pipe displaying rate is slower than rotator. 0x1: skip mode 0x0: no skip mode
13	CONTEXT_SKIP_VG2_EN	decide how to deal with next frame in context queue if rotator DMI buffers are full and MDP pipe displaying rate is slower than rotator. 0x1: skip mode 0x0: no skip mode
12	CONTEXT_SKIP_VG1_EN	decide how to deal with next frame in context queue if rotator DMI buffers are full and MDP pipe displaying rate is slower than rotator. 0x1: skip mode 0x0: no skip mode
11	RESERVED_BIT11	
10	DMI_MDP_DMA_E_EN	DMI enable between Rotator and MDP DMA_E
9	DMI_MDP_DMA_S_EN	DMI enable between Rotator and MDP DMA_S
8	DMI_MDP_DMA_P_EN	DMI enable between Rotator and MDP DMA_P
7	DMI_MDP_RGB2_EN	DMI enable between Rotator and MDP RGB2
6	DMI_MDP_RGB1_EN	DMI enable between Rotator and MDP RGB1
5	DMI_MDP_VG2_EN	DMI enable between Rotator and MDP VG2
4	DMI_MDP_VG1_EN	DMI enable between Rotator and MDP VG1

ROTATOR_INTF_EN (cont.)

Bits	Name	Description
3	DMI_VG1_BUF0_CON	DMI VG1 output buffer0 mapping control 0x0: using non-dmi output buffer 0x1: using dmi output buffer
2	CONTEXT_OUT_BUF_CON	Context queue output buffer control 0x0: all context input is mapped to one output buffer and it is not shadowed when context queue only 0x1: output buffer is shadowed to have decided output for each of context input when using context queue.
1	DMI_RESET	DMI interface Software reset that DMI will be initialized by driving DMI_RESET to 1 when rotator is not busy and DMI_RESET status has to turn to 0 by manually. DMI reset sequence for rotator and MDP is reset MDP DMI firstly and hold reset status then, reset Rotator DMI is recommended. 0x1: DMI interface reset
0	CONTEXT_QUEUE_EN	Context Queue enable

0x04E00038 ROTATOR_DISPLAY_STATUS

Type: Read
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_DISPLAY_STATUS register is used to indicate the idle state of various blocks in the ROTATOR.

ROTATOR_DISPLAY_STATUS

Bits	Name	Description
31:19	RESERVED_BITS31_19	
18	CONTEXT_QUEUE_ACTIVE	Indicates the Context Queue is active
17	DMI_DMA_E_ACTIVE	Indicates the DMI DMA_E is active
16	DMI_DMA_S_ACTIVE	Indicates the DMI DMA_S is active
15	DMI_DMA_P_ACTIVE	Indicates the DMI DMA_P is active
14	DMI_RGB2_ACTIVE	Indicates the DMI RGB2 is active
13	DMI_RGB1_ACTIVE	Indicates the DMI RGB1 is active
12	DMI_VG2_ACTIVE	Indicates the DMI VG2 is active
11	DMI_VG1_ACTIVE	Indicates the DMI VG1 is active
10	DOWN_SCALE_ACTIVE	Indicates the down scaler is active
9	PIX_ROT_ACTIVE	Indicates the pixel rotation is active

ROTATOR_DISPLAY_STATUS (cont.)

Bits	Name	Description
8	CLKCTL_ACTIVE	Indicates the clock control is active
7	TFETCH_ACTIVE	Indicates the tile fetch is active
6	UPSAMPLE_ACTIVE	Indicates the upsample is active
5	ROTATE_ACTIVE	Indicates the rotate is active
4	DOWNSAMPLE_ACTIVE	Indicates the downsample is active
3	PACKER_ACTIVE	Indicates the packer is active
2	DMA_WR_ACTIVE	Indicates the dma_wr is active
1	DMA_RD_ACTIVE	Indicates the dma_rd is active
0	ROTATOR_ACTIVE	Rotator processing in progress. When a image is being processed or pending processing, this bit is set (1). When image processing has completed, this bit is cleared (0).

0x04E0003C ROTATOR_DMI_BUF_CON

Type: Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_01555

The ROTATOR_DMI_BUF_CON register is used to initialize the maximum number of buffer ID in each DMI interface. DMI doesn't allow to use one buffer because rotator is written output image by tile rotation order and MDP pipe fetches image by raster order.

ROTATOR_DMI_BUF_CON

Bits	Name	Description
31:14	RESERVED_BITS31_14	
13:12	MAX_BUF_ID_DMI_DMA_E	MDP DMA_E DMI Maximum number of BUF ID - 1 (1
11:10	MAX_BUF_ID_DMI_DMA_S	MDP DMA_S DMI Maximum number of BUF ID - 1 (1
9:8	MAX_BUF_ID_DMI_DMA_P	MDP DMA_P DMI Maximum number of BUF ID - 1 (1
7:6	MAX_BUF_ID_DMI_RGB2	MDP RGB2 DMI Maximum number of BUF ID - 1 (1
5:4	MAX_BUF_ID_DMI_RGB1	MDP RGB1 DMI Maximum number of BUF ID -1 (1
3:2	MAX_BUF_ID_DMI_VG2	MDP VG2 DMI Maximum number of BUF ID - 1 (1
1:0	MAX_BUF_ID_DMI_VG1	MDP VG1 DMI Maximum number of BUF ID - 1(1

0x04E00040 ROTATOR_CONN_STATUS

Type: Read
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_CONN_STATUS register is indicated current connection of DMI between Rotator and MDP is being rotated that is updated by rotator start event.

ROTATOR_CONN_STATUS

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	MDP_PIPE_BUF_ID	DMI MDP PIPE BUF ID[1:0]
4:2	MDP_PIPE_ID	DMI MDP PIPE destination ID 0x7: Non-DMI 0x6: MDP DMA_E 0x5: MDP DMA_S 0x4: MDP DMA_P 0x3: MDP RGB2 0x2: MDP RGB1 0x1: MDP VG2 0x0: MDP VG1
1:0	CONTEXT_ID	Context ID 0x3: context3 0x2: context2 0x1: context1 0x0: context0

0x04E00044 ROTATOR_CONN_QUEUE_STATUS

Type: Read
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_CONN_QUEUE_STATUS register is indicated queued connection of DMI between Rotator and MDP that is updated by rotator start event.

ROTATOR_CONN_QUEUE_STATUS

Bits	Name	Description
31	QUEUE3_FULL	it is indicated Queue3 Full/Empty. 0x1: Queue0 is full 0x0: Queue0 is empty

ROTATOR_CONN_QUEUE_STATUS (cont.)

Bits	Name	Description
30:29	QUEUE3_MDP_PIPE_BUF_ID	DMI MDP PIPE BUF ID[1:0] for Queue3 2 0x3: Context only
28:26	QUEUE3_MDP_PIPE_ID	DMI MDP PIPE destination ID for Queue3 0x7: Non-DMI 0x6: MDP DMA_E 0x5: MDP DMA_S 0x4: MDP DMA_P 0x3: MDP RGB2 0x2: MDP RGB1 0x1: MDP VG2 0x0: MDP VG1
25:24	QUEUE3_CONTEXT_ID	Context ID for Queue3
23	QUEUE2_FULL	it is indicated Queue2 Full/Empty. 0x1: Queue0 is full 0x0: Queue0 is empty
22:21	QUEUE2_MDP_PIPE_BUF_ID	DMI MDP PIPE BUF ID[1:0] for Queue2 2 0x3: Context only
20:18	QUEUE2_MDP_PIPE_ID	DMI MDP PIPE destination ID for Queue2 0x7: Non-DMI 0x6: MDP DMA_E 0x5: MDP DMA_S 0x4: MDP DMA_P 0x3: MDP RGB2 0x2: MDP RGB1 0x1: MDP VG2 0x0: MDP VG1
17:16	QUEUE2_CONTEXT_ID	Context ID for Queue2
15	QUEUE1_FULL	it is indicated Queue1 Full/Empty. 0x1: Queue0 is full 0x0: Queue0 is empty
14:13	QUEUE1_MDP_PIPE_BUF_ID	DMI MDP PIPE BUF ID[1:0] for Queue1 2 0x3: Non-DMI

ROTATOR_CONN_QUEUE_STATUS (cont.)

Bits	Name	Description
12:10	QUEUE1_MDP_PIPE_ID	DMI MDP PIPE destination ID for Queue1 0x7: Non-DMI 0x6: MDP DMA_E 0x5: MDP DMA_S 0x4: MDP DMA_P 0x3: MDP RGB2 0x2: MDP RGB1 0x1: MDP VG2 0x0: MDP VG1
9:8	QUEUE1_CONTEXT_ID	Context ID for Queue1
7	QUEUE0_FULL	it is indicated Queue0 Full/Empty. 0x1: Queue0 is full 0x0: Queue0 is empty
6:5	QUEUE0_MDP_PIPE_BUF_ID	DMI MDP PIPE BUF ID[1:0] for Queue0 2 0x3: Non-DMI
4:2	QUEUE0_MDP_PIPE_ID	DMI MDP PIPE destination ID for Queue0 0x7: Non-DMI 0x6: MDP DMA_E 0x5: MDP DMA_S 0x4: MDP DMA_P 0x3: MDP RGB2 0x2: MDP RGB1 0x1: MDP VG2 0x0: MDP VG1
1:0	QUEUE0_CONTEXT_ID	Context ID for Queue0

0x04E00048 ROTATOR_CONN_DONE_STATUS

Type: Read
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_CONN_STATUS register is indicated current connection of DMI between Rotator and MDP that will be updated by rotator start event.

ROTATOR_CONN_DONE_STATUS

Bits	Name	Description
31:7	RESERVED_BITS31_7	

ROTATOR_CONN_DONE_STATUS (cont.)

Bits	Name	Description
6:5	MDP_PIPE_BUF_ID	DMI MDP PIPE BUF ID[1:0] 2 0x3: Non-DMI
4:2	MDP_PIPE_ID	DMI MDP PIPE destination ID 0x7: Non-DMI 0x6: MDP DMA_E 0x5: MDP DMA_S 0x4: MDP DMA_P 0x3: MDP RGB2 0x2: MDP RGB1 0x1: MDP VG2 0x0: MDP VG1
1:0	CONTEXT_ID	Context ID

0x04E0004C ROTATOR_CONN_QUEUE_DONE_STATUS

Type: Read
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_CONN_QUEUE_STATUS register is indicated queued connection of DMI between Rotator and MDP that is updated by rotator done event.

ROTATOR_CONN_QUEUE_DONE_STATUS

Bits	Name	Description
31	QUEUE3_FULL	it is indicated Queue3 Full/Empty. 0x1: Queue0 is full 0x0: Queue0 is empty
30:29	QUEUE3_MDP_PIPE_BUF_ID	DMI MDP PIPE BUF ID[1:0] for Queue3 2 0x3: Non-DMI
28:26	QUEUE3_MDP_PIPE_ID	DMI MDP PIPE destination ID for Queue3 0x7: Non-DMI 0x6: MDP DMA_E 0x5: MDP DMA_S 0x4: MDP DMA_P 0x3: MDP RGB2 0x2: MDP RGB1 0x1: MDP VG2 0x0: MDP VG1
25:24	QUEUE3_CONTEXT_ID	Context ID for Queue3

ROTATOR_CONN_QUEUE_DONE_STATUS (cont.)

Bits	Name	Description
23	QUEUE2_FULL	it is indicated Queue2 Full/Empty. 0x1: Queue0 is full 0x0: Queue0 is empty
22:21	QUEUE2_MDP_PIPE_BUF_ID	DMI MDP PIPE BUF ID[1:0] for Queue2 2 0x3: Non-DMI
20:18	QUEUE2_MDP_PIPE_ID	DMI MDP PIPE destination ID for Queue2 0x7: Non-DMI 0x6: MDP DMA_E 0x5: MDP DMA_S 0x4: MDP DMA_P 0x3: MDP RGB2 0x2: MDP RGB1 0x1: MDP VG2 0x0: MDP VG1
17:16	QUEUE2_CONTEXT_ID	Context ID for Queue2
15	QUEUE1_FULL	it is indicated Queue1 Full/Empty. 0x1: Queue0 is full 0x0: Queue0 is empty
14:13	QUEUE1_MDP_PIPE_BUF_ID	DMI MDP PIPE BUF ID[1:0] for Queue1 2 0x3: Non-DMI
12:10	QUEUE1_MDP_PIPE_ID	DMI MDP PIPE destination ID for Queue1 0x7: Non-DMI 0x6: MDP DMA_E 0x5: MDP DMA_S 0x4: MDP DMA_P 0x3: MDP RGB2 0x2: MDP RGB1 0x1: MDP VG2 0x0: MDP VG1
9:8	QUEUE1_CONTEXT_ID	Context ID for Queue1
7	QUEUE0_FULL	it is indicated Queue0 Full/Empty. 0x1: Queue0 is full 0x0: Queue0 is empty
6:5	QUEUE0_MDP_PIPE_BUF_ID	DMI MDP PIPE BUF ID[1:0] for Queue0 2 0x3: Non-DMI

ROTATOR_CONN_QUEUE_DONE_STATUS (cont.)

Bits	Name	Description
4:2	QUEUE0_MDP_PIPE_ID	DMI MDP PIPE destination ID for Queue0 0x7: Non-DMI 0x6: MDP DMA_E 0x5: MDP DMA_S 0x4: MDP DMA_P 0x3: MDP RGB2 0x2: MDP RGB1 0x1: MDP VG2 0x0: MDP VG1
1:0	QUEUE0_CONTEXT_ID	Context ID for Queue0

0x04E00050 ROTATOR_MAX_BURST_SIZE

Type: Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0044

The register is used to modify the maximum burst size of the internal core bus write and read clients. For best performance program the beat size to 16 for Reads and Write. The burst size of 16 is assuming the client data width of 64 bits per beat.

NOTE This register should be written only when Rotator is completely idle.

ROTATOR_MAX_BURST_SIZE

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	MAX_RDBURST_SIZE	Maximum read burst beat size 0x4: 16 (default it is not supported if source image is samsung tile format and using fast yuv mode that HW will be automatically changed setting value to 8 if programming max_rdburst_size to 16) 0x2: 8 0x1: 4 (it is not supported if source image is samsung tile format and using fast yuv mode that HW will be automatically changed setting value to 8 if programming max_rdburst_size to 4)
3	RESERVED_BIT3	
2:0	MAX_WRBURST_SIZE	Maximum write burst beat size 0x4: 16 (default) 0x2: 8 0x1: 4

0x04E00054 ROTATOR_DMI_BUF_PEND_STATUS

Type: Read
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The register is indicated pended DMI buffer information for concurrent DMI buffer switching updating to MDP pipes that will be transferred to MDP pip at the rotation done which was rotated without DMI_INTF_EN.DMI_BUF_UPDATE_DIS = 1 register setting.

ROTATOR_DMI_BUF_PEND_STATUS

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:25	PEND_DMI_MDP_DMA_E_BUF_ID	pended buffer id
24	PEND_DMI_MDP_DMA_E_BUF	it is indicated the buffer updating (switching) event is pended or not. 0x1: pended MDP DMA_E buffer updating 0x0: no pending it
23	RESERVED_BIT23	
22:21	PEND_DMI_MDP_DMA_S_BUF_ID	pended buffer id
20	PEND_DMI_MDP_DMA_S_BUF	it is indicated the buffer updating (switching) event is pended or not. 0x1: pended MDP DMA_S buffer updating 0x0: no pending it
19	RESERVED_BIT19	
18:17	PEND_DMI_MDP_DMA_P_BUF_ID	pended buffer id
16	PEND_DMI_MDP_DMA_P_BUF	it is indicated the buffer updating (switching) event is pended or not. 0x1: pended MDP DMA_P buffer updating 0x0: no pending it
15	RESERVED_BIT15	
14:13	PEND_DMI_MDP_RGB2_BUF_ID	pended buffer id
12	PEND_DMI_MDP_RGB2_BUF	it is indicated the buffer updating (switching) event is pended or not. 0x1: pended MDP RGB2 buffer updating 0x0: no pending it
11	RESERVED_BIT11	
10:9	PEND_DMI_MDP_RGB1_BUF_ID	pended buffer id

ROTATOR_DMI_BUF_PEND_STATUS (cont.)

Bits	Name	Description
8	PEND_DMI_MDP_RGB1_BUF	it is indicated the buffer updating (switching) event is pended or not. 0x1: pended MDP RGB1 buffer updating 0x0: no pending it
7	RESERVED_BIT7	
6:5	PEND_DMI_MDP_VG2_BUF_ID	pended buffer id
4	PEND_DMI_MDP_VG2_BUF	it is indicated the buffer updating (switching) event is pended or not. 0x1: pended MDP VG2 buffer updating 0x0: no pending it
3	RESERVED_BIT3	
2:1	PEND_DMI_MDP_VG1_BUF_ID	pended buffer id
0	PEND_DMI_MDP_VG1_BUF	it is indicated the buffer updating (switching) event is pended or not. 0x1: pended MDP VG1 buffer updating 0x0: no pending it

0x04E00058 ROTATOR_CONTEXT_FLUSH

Type: Read
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The register is used to flush all of queued up contexts in Context Queue that will be removed all of queues right away if rotator is idle. otherwise, remove all of queues after finishing current frame rotation.

ROTATOR_CONTEXT_FLUSH

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	DMI_FLUSH_EN	DMI Flush option 0x1: Remove all the queue in context queue and initialize DMI also when CONTEXT_QUEUE_FLUSH is ’1’. (it requires MDP DMI initialization manually by DMI_RESET to sync 2 DMI buffer numbering between Rotator DMI and MDP DMI) 0x0: Remove all the queue in context queue only when CONTEXT_QUEUE_FLUSH is ’1’.
0	CONTEXT_QUEUE_FLUSH	Flush all of pended context start control in queue. the value will be reset after flushing queue

0x04E0005C ROTATOR_DMI_BUF_VALID_STATUS

Type: Read
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The register shows how many DMI buffers are valid for each of MDP pipe. The valid counter will be decreased by rotator DMI buffer switching event and is increased by DMI buffer acknowledge from MDP pipe. rotator also provides DMI buffer Acknowledge interrupt source that SW needs to check the status for next DMI buffer switching event.

ROTATOR_DMI_BUF_VALID_STATUS

Bits	Name	Description
31:14	RESERVED_BITS31_14	
13:12	DMI_DMA_E_BUF_VALID	Indicates how many buffers are available for DMI for MDP DMA_E. 0x3: 3 DMI buffers are available for next DMI buffer switching 0x2: 2 DMI buffers are available for next DMI buffer switching 0x1: 1 DMI buffer is available for next DMI buffer switching 0x0: not valid DMI buffer
11:10	DMI_DMA_S_BUF_VALID	Indicates how many buffers are available for DMI for MDP DMA_S. 0x3: 3 DMI buffers are available for next DMI buffer switching 0x2: 2 DMI buffers are available for next DMI buffer switching 0x1: 1 DMI buffer is available for next DMI buffer switching 0x0: not valid DMI buffer
9:8	DMI_DMA_P_BUF_VALID	Indicates how many buffers are available for DMI for MDP DMA_P. 0x3: 3 DMI buffers are available for next DMI buffer switching 0x2: 2 DMI buffers are available for next DMI buffer switching 0x1: 1 DMI buffer is available for next DMI buffer switching 0x0: not valid DMI buffer
7:6	DMI_RGB2_BUF_VALID	Indicates how many buffers are available for DMI for MDP RGB2. 0x3: 3 DMI buffers are available for next DMI buffer switching 0x2: 2 DMI buffers are available for next DMI buffer switching 0x1: 1 DMI buffer is available for next DMI buffer switching 0x0: not valid DMI buffer
5:4	DMI_RGB1_BUF_VALID	Indicates how many buffers are available for DMI for MDP RGB1. 0x3: 3 DMI buffers are available for next DMI buffer switching 0x2: 2 DMI buffers are available for next DMI buffer switching 0x1: 1 DMI buffer is available for next DMI buffer switching 0x0: not valid DMI buffer
3:2	DMI_VG2_BUF_VALID	Indicates how many buffers are available for DMI for MDP VG2. 0x3: 3 DMI buffers are available for next DMI buffer switching 0x2: 2 DMI buffers are available for next DMI buffer switching 0x1: 1 DMI buffer is available for next DMI buffer switching 0x0: not valid DMI buffer

ROTATOR_DMI_BUF_VALID_STATUS (cont.)

Bits	Name	Description
1:0	DMI_VG1_BUF_VALID	Indicates how many buffers are available for DMI for MDP VG1. 0x3: 3 DMI buffers are available for next DMI buffer switching 0x2: 2 DMI buffers are available for next DMI buffer switching 0x1: 1 DMI buffer is available for next DMI buffer switching 0x0: not valid DMI buffer

0x04E00060 ROTATOR_DMI_FREE_RUN_EN

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The register is option for non-blocking rotator DMI mode that rotator will transfer buffer switching event through DMI whenever rotator is done for rotation and MDP pipe will pick up latest buffer id if MDP DMI is also non-blocking mode. The mode is not recommended because the mode will consume more power and bandwidth if rotator frame rate is faster than mdp pipe frame rate.

To save more power and bandwidth, using Context replace function + rotator DMI blocking mode + mdp DMI blocking mode is recommended for rotator frame rate is faster than mdp pipe frame rate case.

ROTATOR_DMI_FREE_RUN_EN

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6	DMI_MDP_DMA_E_FREE_RUN_EN	MDP DMA_E dmi free running enable 0x1: updated rotated buffer information to MDP pipe regardless of DMI acknowledge from the MDP pipe that DMI in MDP has to be programmed to skip mode. 0x0: check DMI acknowledge from MDP pipe to update new rotated buffer.
5	DMI_MDP_DMA_S_FREE_RUN_EN	MDP DMA_S dmi free running enable 0x1: updated rotated buffer information to MDP pipe regardless of DMI acknowledge from the MDP pipe that DMI in MDP has to be programmed to skip mode. 0x0: check DMI acknowledge from MDP pipe to update new rotated buffer.
4	DMI_MDP_DMA_P_FREE_RUN_EN	MDP DMA_Pdmi free running enable 0x1: updated rotated buffer information to MDP pipe regardless of DMI acknowledge from the MDP pipe that DMI in MDP has to be programmed to skip mode. 0x0: check DMI acknowledge from MDP pipe to update new rotated buffer.

ROTATOR_DMI_FREE_RUN_EN (cont.)

Bits	Name	Description
3	DMI_MDP_RGB2_FREE_RUN_EN	MDP RGB2 dmi free running enable 0x1: updated rotated buffer information to MDP pipe regardless of DMI acknowledge from the MDP pipe that DMI in MDP has to be programmed to skip mode. 0x0: check DMI acknowledge from MDP pipe to update new rotated buffer.
2	DMI_MDP_RGB1_FREE_RUN_EN	MDP RGB1 dmi free running enable 0x1: updated rotated buffer information to MDP pipe regardless of DMI acknowledge from the MDP pipe that DMI in MDP has to be programmed to skip mode. 0x0: check DMI acknowledge from MDP pipe to update new rotated buffer.
1	DMI_MDP_VG2_FREE_RUN_EN	MDP VG2 dmi free running enable 0x1: updated rotated buffer information to MDP pipe regardless of DMI acknowledge from the MDP pipe that DMI in MDP has to be programmed to skip mode. 0x0: check DMI acknowledge from MDP pipe to update new rotated buffer.
0	DMI_MDP_VG1_FREE_RUN_EN	MDP VG1 dmi free running enable 0x1: updated rotated buffer information to MDP pipe regardless of DMI acknowledge from the MDP pipe that DMI in MDP has to be programmed to skip mode. 0x0: check DMI acknowledge from MDP pipe to update new rotated buffer.

0x04E00070 ROTATOR_HW_VERSION

Type: Read Only
Clock: CC_ROTATOR_CLK
Reset State: 0x0102030A

The ROTATOR_HW_VERSION register contains the major and minor versions and release number of the ROTATOR core.

ROTATOR_HW_VERSION

Bits	Name	Description
31:24	MAJOR_VERSION	ROTATOR core major version.
23:16	MINOR_VERSION	ROTATOR core minor version.
15:8	RELEASE_PHASE	ROTATOR core release phase.
7:0	REVISION	ROTATOR core revision number.

0x04E00074 ROTATOR_SW_RESET

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_SW_RESET register is used to reset the blocks inside ROTATOR.

ROTATOR_SW_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	SW_RESET	Self cleared when reset sequence is completed. 0x1: Rotator SW reset.

0x04E00084 ROTATOR_SW_SCRATCHPAD_TEST_REG

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

This 32-bit register can be used by display software driver as a scratch pad register. It doesn't control or monitor any functionality within ROTATOR core. It can also be used to see whether the value written to this register is also seen on the Rotator testbus. Refer to the TEST MISR SW register section on how to select this register to see its value on the testbus.

ROTATOR_SW_SCRATCHPAD_TEST_REG

Bits	Name	Description
31:0	SCRATCHPAD	Scratch pad register space for software. One can also see the value written to this register on the testbus

14.12.3 Clock control registers

0x04E00100 ROTATOR_CGC_EN

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_01FF

The ROTATOR_CGC_EN register is used to enable the automatic functional clock gating mechanism inside the ROTATOR, where the clocks are gated depending on the operation mode. Each bit is assigned to a gated clock tree. For maximum power saving, leave all bits at 1 during initialization. To force a block to have the clock on always regardless of the operation scenario, set the associated enable bit to 0.

ROTATOR_CGC_EN

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8	CONTEXT_QUEUE	Enable auto functional gating on CONTEXT_QUEUE clock
7	DMI	Enable auto functional gating on DMI clock
6	PIXROT	Enable auto functional gating on pixel rotator clock
5	DOWNSCALER	Enable auto functional gating on Downscaler clock
4	AXI	Enable auto functional gating on AXI interface clock
3	DOWNSAMPLE	Enables auto functional gating on Downsample clock.
2	ROTATE	Enables auto functional gating on Rotate clock.
1	UPSAMPLE	Enables auto functional gating on Upsample clock.
0	TOP	Enables auto functional gating on top clock.

14.12.4 MGEN2MAXI control registers

NOTE1: Registers in this section (mGEN2mAXI) are only for future 8K APQs that use Rotator.

NOTE2: Program the mgen2maxi registers only when Rotator is in idle mode.

NOTE3: The following registers are defined for 2 generic clients (1 read + 1write) and 1 AXI r0p0++ master port.

XBAR_IN0 - Rotator read;

XBAR_IN1- Rotator write;

0x04E00400 ROTATOR_XBAR_IN_RD_LIM

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0008

The maximum number of pending reads from each client is programmed in this register.

ROTATOR_XBAR_IN_RD_LIM

Bits	Name	Description
31:4	RESERVED31_4	This field has no function and should be set to zero for future compatibility
3:0	XBAR_IN0_RD_LIM	The maximum number of pending reads from each client. Must be <= the HW parameter that limits the same. Range [0,8]

0x04E00404 ROTATOR_XBAR_IN_WR_LIM

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0008

The maximum number of pending writes from each client is programmed in this register.

ROTATOR_XBAR_IN_WR_LIM

Bits	Name	Description
31:4	RESERVED31_4	This field has no function and should be set to zero for future compatibility
3:0	XBAR_IN1_WR_LIM	The maximum number of pending writes from each client. Must be <= the HW parameter that limits the same. Range [0,8]

0x04E00408 ROTATOR_XBAR_OUT_RD_LIM

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0008

The maximum number of pending reads from Rotator's AXI Master port is programmed in this register.

ROTATOR_XBAR_OUT_RD_LIM

Bits	Name	Description
31:4	RESERVED31_4	This field has no function and should be set to zero for future compatibility
3:0	XBAR_OUT_RD_LIM	The maximum number of pending reads from the ROTATOR Master. Must be <= the HW parameter that limits the same. Range [0,8]

0x04E0040C ROTATOR_XBAR_OUT_WR_LIM

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0008

The maximum number of pending writes from Rotator's AXI Master port is programmed in this register.

ROTATOR_XBAR_OUT_WR_LIM

Bits	Name	Description
31:4	RESERVED31_4	This field has no function and should be set to zero for future compatibility
3:0	XBAR_OUT_WR_LIM	The maximum number of pending writes from the ROTATOR Master. Must be <= the HW parameter that limits the same. Range [0,8]

0x04E00410 ROTATOR_XBAR_OUT_MAX_BURST

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0008_0008

The maximum number of pending writes from Rotator's AXI Master port is programmed in this register.

ROTATOR_XBAR_OUT_MAX_BURST

Bits	Name	Description
31:20	RESERVED31_20	This field has no function and should be set to zero for future compatibility
19:16	XBAR_OUT_MAX_RD_BURST	The maximum number of read beats minus 1 (128 bits per beat) allowed on the AXI bus (arbiter outputs). Must be < the HW parameter that limits the same. Range [0,8]
15:4	RESERVED15_4	This field has no function and should be set to zero for future compatibility
3:0	XBAR_OUT_MAX_WR_BURST	The maximum number of write beats minus 1 (128 bits per beat) allowed on the AXI bus (arbiter outputs). Must be < the HW parameter that limits the same. Range [0,8]

0x04E00414 ROTATOR_XBAR_ARB_CTL

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

Each arbiter can be programmed to utilize fixed priority (higher client numbers have higher priority) or last-client-granted (default when fixed priority is not enabled.

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ROTATOR_XBAR_ARB_CTL

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility
0	FIXED_PRIOR_EN	Enables fixed priority arbitration. If enabled, CLIENT_LIM setting is ignored. When disabled, last-client granted scheme is used for arbitration utilizing the CLIENT_LIM

0x04E00418 ROTATOR_XBAR_ARB_FIXED_PRIOR_LIST

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0001

The priority list contains a list of client numbers with the highest priority client on the left side (MSBs). The length of the priority list is [1:0] to support 2 clients encoded using one bit each.

ROTATOR_XBAR_ARB_FIXED_PRIOR_LIST

Bits	Name	Description
31:2	RESERVED31_2	This field has no function and should be set to zero for future compatibility
1:0	FIXED_PRIOR_LIST	Default priority - Client0(read) >Client1(write)

0x04E0041C ROTATOR_XBAR_ARB_CLIENT_LIM

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0088

The maximum number of (consecutive grants - 1) to one client before allowing requests from other clients. This is used for last-client-granted arbitration, but not fixed priority arbitration. NOTE: A client may receive more than this number of consecutive grants if no other clients are making requests to the same arbiter.

ROTATOR_XBAR_ARB_CLIENT_LIM

Bits	Name	Description
31:8	RESERVED31_8	This field has no function and should be set to zero for future compatibility
7:4	CLIENT1_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]

ROTATOR_XBAR_ARB_CLIENT_LIM (cont.)

Bits	Name	Description
3:0	CLIENT0_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]

0x04E00420 ROTATOR_XBAR_AXI_AOOORD

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0001

When a request is granted by the arbiter, AOOORD signal (AXI r0p0++) may be controlled on a per-client basis.

ROTATOR_XBAR_AXI_AOOORD

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility
0	AXI_AOOORD	'Out of order' enable for reads, one bit per read client. If zero, the AXI bus and slaves must ensure that all reads from that client are completed in the order they are requested from the client.

0x04E00424 ROTATOR_XBAR_AXI_AOOOWR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0001

When a request is granted by the arbiter, AOOOWR signal (AXI r0p0++) may be controlled on a per-client basis.

ROTATOR_XBAR_AXI_AOOOWR

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility
0	AXI_AOOOWR	'Out of order' enable for writes, one bit per write client. If zero, the AXI bus and slaves must ensure that all writes from this client are completed in the order they are requested from the client.

0x04E00428 ROTATOR_XBAR_AXI_ATYPE

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0044

When a request is granted by the arbiter, ATYPE signal (AXI r0p0++) may be controlled on a per-client basis. ATYPE indicates the memory type and attributes of an access.

ROTATOR_XBAR_AXI_ATYPE

Bits	Name	Description
31:8	RESERVED31_8	This field has no function and should be set to zero for future compatibility
7:0	AXI_ATYPE	The value to drive on ATYPE signal, 4 bits per client: 0x4: Normal, Non-cacheable, Non-shared 0x6: Normal, Cacheable, Writeback, Write-allocate, Non-shared 0x7: Normal, Cacheable, Writeback, Write-allocate, Shared

0x04E0042C ROTATOR_XBAR_AXI_AREQPRIORITY

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

When a request is granted by the arbiter, AREQPRIORITY signal (AXI r0p0++) may be controlled on a per-client basis.

ROTATOR_XBAR_AXI_AREQPRIORITY

Bits	Name	Description
31:4	RESERVED31_4	This field has no function and should be set to zero for future compatibility
3:0	AXI_AREQPRIORITY	Request priority, 2 bits per client. This value is driven onto AXI bus only, not used internally for client arbitration. These two bits of relative priority can be decoded as shown below. ’00’ - normal ’01’ - high ’10’ - higher ’11’ - highest.

0x04E00430 ROTATOR_XBAR_AXI_APROTNS

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

NOTE This register is RESERVED. AXI signal 'aprotns' is tied to one (non-secure) at MMSS level for Rotator AXI Master port. This tie in MMSS overrides the value set by this register.

ROTATOR_XBAR_AXI_APROTNS

Bits	Name	Description
31:2	RESERVED31_2	This field has no function and should be set to zero for future compatibility
1:0	AXI_APROTNS	(RESERVED) Enable 'non-secure' bus access, one bit per client. If zero, the corresponding client accesses are secure accesses.

0x04E00440 ROTATOR_XBAR_AXI_ERROR_CTL

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_XBAR_AXI_ERROR_CTL

Bits	Name	Description
31:9	RESERVED31_9	This field has no function and should be set to zero for future compatibility
8	AXI_ERR_CLR	One bit per AXI master port. When AXI error occurs, SW can read the error info and then can assert this bit (for 1+ AXI cycles) to clear the AXI error and enable next AXI error to be captured.
7:5	RESERVED7_5	This field has no function and should be set to zero for future compatibility
4	AXI_HALT_ON_WR_ERR	When set (1), a write error response from AXI (on bresp) acts like a HALT_REQ and also disables all ARB-XIN interfaces - instead, fake write data to AXI (zero write enables) and discard read data from AXI. SW should wait for AXI_IDLE (or HALT_ACK) and then reset the core.
3:1	RESERVED3_1	This field has no function and should be set to zero for future compatibility
0	AXI_HALT_ON_RD_ERR	When set (1), a read error response from AXI (on rresp) acts like a HALT_REQ and also disables all ARB-XIN interfaces - instead, fake write data to AXI (zero write enables) and discard read data from AXI. SW should wait for AXI_IDLE (or HALT_ACK) and then reset the core.

0x04E00444 ROTATOR_XBAR_AXI_ERROR_INFO

Type: Read
Clock: CC_ROTATOR_CLK
Reset State: Undefined

ROTATOR_XBAR_AXI_ERROR_INFO

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11	AXI_ERR	Indicates than an AXI error occurred since the last AXI reset. The AXI error interrupt status may be more useful than this bit.
10	AXI_ERR_TYPE	The type of the last error that occurred. 0x0: axi_rresp 0x1: axi_bresp (has priority over rresp if happens at same time)
9:8	AXI_RESP	The value of axi_rresp or axi_bresp when the last error occurred.
7:5	RESERVED	This field has no function and should be set to zero for future compatibility
4	AXI_MID	The value on axi_rmid or axi_bmid when the last error occurred.
3:0	AXI_TID	The value on axi_rtid or axi_btid when the last error occurred.

0x04E00448 ROTATOR_XBAR_AXI_WDATA_TIMEOUT_CTL

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_00F0

ROTATOR_XBAR_AXI_WDATA_TIMEOUT_CTL

Bits	Name	Description
31:8	RESERVED31_8	This field has no function and should be set to zero for future compatibility
7:4	WDTIMEOUT_LOG2	Bit number of the 16-bit time waiting counter that indicates timeout.
3:1	RESERVED3_1	This field has no function and should be set to zero for future compatibility
0	AXI_HALT_WDTIMEOUT	When set (1), this will generate a "halt" (similar to HALT_ON_WR_ERR) if the core is not able to provide a write data burst to AXI within a SW specified time after the previous write data burst was sent. This is either because client does not provide write data fast enough or AXI is not accepting write data fast enough.

0x04E0044C ROTATOR_XBAR_AXI_STATUS

Type: Read
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0001

ROTATOR_XBAR_AXI_STATUS

Bits	Name	Description
31:5	RESERVED31_5	This field has no function and should be set to zero for future compatibility
4	WDATA_TIMEOUT_HALT	Indicates that AXI halt occurred because of write data timeout. Once asserted will remain high till AXI reset.
3:1	RESERVED3_1	This field has no function and should be set to zero for future compatibility
0	AXI_IDLE	Indicates that the AXI master port is idle (no pending requests on AXI).

0x04E00450 ROTATOR_XBAR_AXI_PROFILE_CTL

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

Each arbiter includes bandwidth counters, min & max latency counters, a MISR for capturing AXI write data, and an LFSR for generating AXI read data (faking the response from AXI slaves).

ROTATOR_XBAR_AXI_PROFILE_CTL

Bits	Name	Description
31:25	RESERVED31_25	This field has no function and should be set to zero for future compatibility
24	RD_LAT_REP_EN	When enabled, each beat of read data is replaced with the read access latency (of AXI cycles from request until read data is returned)
23:17	RESERVED23_17	This field has no function and should be set to zero for future compatibility
16	MISR_RES	Mgen2maxi MISR Reset. Need to write 1 and then write 0
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility
12	MISR_EN	Enable the Misr in mgen2maxi
11:9	RESERVED11_9	This field has no function and should be set to zero for future compatibility

ROTATOR_XBAR_AXI_PROFILE_CTL (cont.)

Bits	Name	Description
8	MISR_WD	select misr input 0x0: read data (coming back from AXI) 0x1: write data (going to AXI)
7	CTR_EN	Enable all profiling counters
6	CTR_RES	Reset all profiling counters (they are also reset by AXI_RESET)
5:4	RESERVED5_4	This field has no function and should be set to zero for future compatibility
3:0	TEST_OUT_SEL	Select which test data is read via ROTATOR_AXI_PROFILE_OUT. 0x0: num read bursts (32 bits) 0x1: total read BW (32 bits - up to 68GB) 0x2: max outstanding reads (8 bits) 0x3: avg wait for read accept (10 bits over 128 reads) 0x4: min read latency (16 bits) 0x5: max read latency (16 bits) 0x6: avg read latency (16 bits over 1K read beats) 0x8: num write bursts (32 bits) 0x9: total write BW (32 bits - up to 68GB) 0xA: max outstanding writes (8 bits) 0xB: avg wait for write accept (10 bits over 128 writes) 0xC: MISR signature word 0 0xD: MISR signature word 1 0xE: MISR signature word 2 0xF: MISR signature word 3

0x04E00454 ROTATOR_XBAR_AXI_PROFILE_OUT

Type: Read
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_XBAR_AXI_PROFILE_OUT

Bits	Name	Description
31:0	AXI_TEST_OUT	The output selected by ROTATOR_AXI_PROFILE_CTL reg.

14.12.5 Rotator Sub-Block Registers

0x04E01010 ROTATOR_PROFILE_EN

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_PROFILE_EN

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	EN	Enable the ROI cycle counter for profiling

0x04E01014 ROTATOR_PROFILE_COUNT

Type: Read Only
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_PROFILE_COUNT

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	TOTAL_CYCLE	Total cycle count in a ROI, from new ROI to last pixel out of Packer (Rotator goes back to Idle)

0x04E01108 ROTATOR_SRC_SIZE

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0020_0020

If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_SRC_SIZE

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_H	Height of input ROI image that needs to be fetched in pixel, including any amount of over-fetching/under-fetching necessary.
15:13	RESERVED_BITS15_13	

ROTATOR_SRC_SIZE (cont.)

Bits	Name	Description
12:0	SRC_W	Width of input ROI image that needs to be fetched in pixel, including any amount of over-fetching/under-fetching necessary.

0x04E0110C ROTATOR_SRCP0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRCP0_ADDR

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format or planar color0 plane

0x04E01110 ROTATOR_SRCP1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_SRCP1_ADDR

Bits	Name	Description
31:0	SRCP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format or planar color1 plane

0x04E01114 ROTATOR_SRCP2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_SRCP2_ADDR

Bits	Name	Description
31:0	SRCP2_ADDR	Base byte address of the Image's planar color2 plane

0x04E01118 ROTATOR_SRCP3_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRCP3_ADDR

Bits	Name	Description
31:0	SRCP3_ADDR	Base byte address of the Image's color3 component (alpha) used in pseudo planar + alpha format or planar

0x04E0111C ROTATOR_SRC_YSTRIDE1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0080

If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_SRC_YSTRIDE1

Bits	Name	Description
31	RESERVED_BIT31	
30:16	SRCP1_YSTRIDE	Plane 1 y stride in bytes.
15	RESERVED_BIT15	
14:0	SRCP0_YSTRIDE	Plane 0 y stride in bytes.

0x04E01120 ROTATOR_SRC_YSTRIDE2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_SRC_YSTRIDE2

Bits	Name	Description
31	RESERVED_BIT31	
30:16	SRCP3_YSTRIDE	Plane 3 y stride in bytes.
15	RESERVED_BIT15	
14:0	SRCP2_YSTRIDE	Plane 2 y stride in bytes.

0x04E01124 ROTATOR_SRC_FORMAT

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0042_67FF

If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_SRC_FORMAT

Bits	Name	Description
31	RESERVED_BIT31	
30:29	FRAME_FORMAT	0x0: Linear Frame (default) 0x1: RESERVED 0x2: 64x32 super-tile, YCbCr 420 non folding
28:26	RESERVED_BITS28_26	
25:24	FORMAT_CONV	0x0: No format conversion 0x1: ARGB32bpp to RGB24bpp 0x2: RESERVED_1 0x3: RESERVED_2
23:22	FETCH_TILE_SIZE	Specify the fetch tile size. 0x0: RESERVED_1 0x1: 64x64 (default) 0x2: RESERVED_2 0x3: RESERVED_3
21	RESERVED_BITS_21	
20:19	FETCH_PLANES	Determines the number of planes to fetch and write back. When this parameter is set to planer format the output of Rotator is forced to write out a Pseudo planar format. When this parameter is set to fetch H2V1 422 interleaved format the output of Rotator is forced to write back 422 Pseudo planar format. For all the other cases the Rotators output write back format is same as the input fetch format. 0x0: Interleaved 0x1: Planar 0x2: Pseudo planar
18	UNPACK_ALIGN	0x0: To LSB 0x1: To MSB
17	UNPACK_TIGHT	0x0: Loose 0x1: Tight
16:13	UNPACK_COUNT	Valid unpacking pattern count: 0 = 1 component, 1 = 2 components, ..., 15 = 16 components. Unpacking pattern only applies to the interleaved plane (chroma plane in pseudo-planar).
12:11	RESERVED_BITS12_11	Reserved for backward compatibility.

ROTATOR_SRC_FORMAT (cont.)

Bits	Name	Description
10:9	SRC_BPP	Effective source byte per pixel: 0 = 1 byte, 1 = 2 bytes, 2 = 3 bytes, 3 = 4 bytes. This is only used when unpacking the interleaved plane.
8	SRCC3_EN	0x1: Source has alpha
7:6	SRCC3_BITS	Number of bits for component 3 (alpha) input, this is not used for dither: 0 = RESERVED, 1 = RESERVED, 2 = RESERVED, 3 = 8 bits.
5:4	SRCC2_BITS	Number of bits for component 2 (R / Cr) input: 0 = RESERVED, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	SRCC1_BITS	Number of bits for component 1 (B / Cb) input: 0 = RESERVED, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	SRCC0_BITS	Number of bits for component 0 (G / luma) input: 0 = RESERVED, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x04E01128 ROTATOR_SRC_UNPACK_PATTERN1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0302_0001

Unpacking pattern, maximum of 4 pattern elements starting from LSB to MSB (0 to 4). Default is ARGB or C3-C2-C0-C1. If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_SRC_UNPACK_PATTERN1

Bits	Name	Description
31:26	RESERVED31_26	
25:24	ELEMENT3	0x0: C0 0x1: C1 0x2: C2 0x3: C3
23:18	RESERVED23_18	
17:16	ELEMENT2	0x0: C0 0x1: C1 0x2: C2 0x3: C3
15:10	RESERVED15_10	
9:8	ELEMENT1	0x0: C0 0x1: C1 0x2: C2 0x3: C3

ROTATOR_SRC_UNPACK_PATTERN1 (cont.)

Bits	Name	Description
7:2	RESERVED7_2	
1:0	ELEMENT0	0x0: C0 0x1: C1 0x2: C2 0x3: C3

0x04E01138 ROTATOR_SUB_BLOCK_CFG

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_SUB_BLOCK_CFG

Bits	Name	Description
31:24	RESERVED_BIT31_24	
23	RESERVED_BIT23	
22:21	RESERVED_BITS22_21	.
20	RESERVED_BIT20	
19:18	SRC_CHROMA_SAMP	Source chroma sampling (used by upsample block): 0x0: 4:4:4/RGB 0x1: H2V1 0x2: H1V2 0x3: 4:2:0.
17:12	RESERVED_BITS17_12	
11:9	ROT_MODE	Rotation mode: Bit 0: Rotate 90 degrees Bit 1: Left/right flip Bit 2: Up/down flip.
8	ROT_EN	Rotate buffer enable. When this bit is set (1), the ping-pong tile buffer is always used independent of the rotation mode.
7:6	RESERVED_BIT7_6	
5	ALPHA_DOWN_SCALE	ALPHA Channel Down-scale option 0x1: using 1/N scaling 0x0: using pixel drop

ROTATOR_SUB_BLOCK_CFG (cont.)

Bits	Name	Description
4	FAST_YUV_TRANS	Fast YUV(YCbCr) data transaction 0x1: enable Fast yuv transaction for YUV420 planer and psuedo-planer. (not support YUV422 input format) 0x0: using normal YUV transaction (default)
3:2	DOWN_SCALE_V_RATIO	Down Scaling ratio for Vertical 0x3: 1/8 down scaling 0x2: 1/4 down scaling 0x1: 1/2 down scaling 0x0: no down scaling (default)
1:0	DOWN_SCALE_H_RATIO	Down Scaling ratio for Horizontal 0x3: 1/8 down scaling 0x2: 1/4 down scaling 0x1: 1/2 down scaling 0x0: no down scaling (default)

0x04E01154 ROTATOR_OUT_PACK_PATTERN1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0302_0001

If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_OUT_PACK_PATTERN1

Bits	Name	Description
31:26	RESERVED31_26	
25:24	ELEMENT3	0x0: C0 0x1: C1 0x2: C2 0x3: C3
23:18	RESERVED23_18	
17:16	ELEMENT2	0x0: C0 0x1: C1 0x2: C2 0x3: C3
15:10	RESERVED15_10	
9:8	ELEMENT1	0x0: C0 0x1: C1 0x2: C2 0x3: C3

ROTATOR_OUT_PACK_PATTERN1 (cont.)

Bits	Name	Description
7:2	RESERVED7_2	
1:0	ELEMENT0	0x0: C0 0x1: C1 0x2: C2 0x3: C3

0x04E01168 ROTATOR_OUTP0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP0_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E0116C ROTATOR_OUTP1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP1_ADDR

Bits	Name	Description
31:0	DSTP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x04E01170 ROTATOR_OUTP2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP2_ADDR

Bits	Name	Description
31:0	DSTP2_ADDR	Base byte address of the Image's planar color2 plane if using fast_yuv mode for planer YUV420 input

0x04E01174 ROTATOR_OUTP3_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP3_ADDR

Bits	Name	Description
31:0	DSTP3_ADDR	Base byte address of the Image's color3 (alpha) component, used in pseudo planar + alpha format, or planar.

0x04E01178 ROTATOR_OUT_YSTRIDE1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0080

If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_OUT_YSTRIDE1

Bits	Name	Description
31	RESERVED_BIT31	
30:16	DSTP1_YSTRIDE	Plane 1 y stride in bytes.
15	RESERVED_BIT15	
14:0	DSTP0_YSTRIDE	Plane 0 y stride in bytes.

0x04E0117C ROTATOR_OUT_YSTRIDE2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_OUT_YSTRIDE2

Bits	Name	Description
31	RESERVED_BIT31	
30:16	DSTP3_YSTRIDE	Plane 3 y stride in bytes.
15	RESERVED_BIT15	
14:0	DSTP2_YSTRIDE	Plane 2 y stride in bytes

0x04E01200 ROTATOR_SRC_XY

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_SRC_XY

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_Y	Source ROI origin screen Y coordinate (pixel) in the source image (i.e., Y offset of source ROI in the source image).
15:13	RESERVED_BITS15_13	
12:0	SRC_X	Source ROI origin screen X coordinate (pixel) in the source image (i.e., X offset of source ROI in the source image).

0x04E01208 ROTATOR_SRC_IMAGE_SIZE

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0020_0020

If CONTEXT_QUEUE is enable, this register is being used for context0.

ROTATOR_SRC_IMAGE_SIZE

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_IMG_H	Source image height (to determine if lines should be over-fetched or repeated).
15:13	RESERVED_BITS15_13	
12:0	SRC_IMG_W	Source image width (to determine if pixels should be over-fetched or repeated).

0x04E01308 ROTATOR_SRC_SIZE_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0020_0020

ROTATOR_SRC_SIZE_C1 is used for rotator source size for context1.

ROTATOR_SRC_SIZE_C1

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_H	Height of input ROI image that needs to be fetched in pixel, including any amount of over-fetching/under-fetching necessary.
15:13	RESERVED_BITS15_13	
12:0	SRC_W	Width of input ROI image that needs to be fetched in pixel, including any amount of over-fetching/under-fetching necessary.

0x04E0130C ROTATOR_SRCP0_ADDR_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRCP0_ADDR_C1 is context1 rotator source plane0 offset address.

ROTATOR_SRCP0_ADDR_C1

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format or planar color0 plane

0x04E01310 ROTATOR_SRCP1_ADDR_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRCP1_ADDR_C1 is for context1 rotator source plane1 offset address.

ROTATOR_SRCP1_ADDR_C1

Bits	Name	Description
31:0	SRCP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format or planar color1 plane

0x04E01314 ROTATOR_SRCP2_ADDR_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRCP2_ADDR_C1 is for context1 rotator source plane2 offset address.

ROTATOR_SRCP2_ADDR_C1

Bits	Name	Description
31:0	SRCP2_ADDR	Base byte address of the Image's planar color2 plane

0x04E0131C ROTATOR_SRC_YSTRIDE1_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0080

ROTATOR_SRC_YSTRIDE1_C1 is used for context1 rotator plane0 and plane1 Y stride.

ROTATOR_SRC_YSTRIDE1_C1

Bits	Name	Description
31	RESERVED_BIT31	
30:16	SRCP1_YSTRIDE	Plane 1 y stride in bytes.
15	RESERVED_BIT15	
14:0	SRCP0_YSTRIDE	Plane 0 y stride in bytes.

0x04E01320 ROTATOR_SRC_YSTRIDE2_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRC_YSTRIDE1_C1 is used for context1 rotator plane2 Y stride.

ROTATOR_SRC_YSTRIDE2_C1

Bits	Name	Description
31:15	RESERVED_BI31_15	
14:0	SRCP2_YSTRIDE	Plane 2 y stride in bytes.

0x04E01324 ROTATOR_SRC_FORMAT_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0042_67FF

ROTATOR_SRC_FORMAT_C1 is used for context1 rotator source format.

ROTATOR_SRC_FORMAT_C1

Bits	Name	Description
31	RESERVED_BIT31	
30:29	FRAME_FORMAT	0x0: Linear Frame (default) 0x1: RESERVED 0x2: 64x32 super-tile, YCbCr 420 non folding
28:26	RESERVED_BITS_28_26	
25:24	FORMAT_CONV	0x0: No format conversion 0x1: ARGB32bpp to RGB24bpp 0x2: RESERVED_1 0x3: RESERVED_2
23:22	FETCH_TILE_SIZE	Specify the fetch tile size. 0x0: RESERVED_1 0x1: 64x64 (default) 0x2: RESERVED_2 0x3: RESERVED_3
21	RESERVED_BITS_21	
20:19	FETCH_PLANES	Determines the number of planes to fetch and write back. When this parameter is set to planer format the output of Rotator is forced to write out a Pseudo planar format. When this parameter is set to fetch H2V1 422 interleaved format the output of Rotator is forced to write back 422 Pseudo planar format. For all the other cases the Rotators output write back format is same as the input fetch format. 0x0: Interleaved 0x1: Planar 0x2: Pseudo planar
18	UNPACK_ALIGN	0x0: To LSB 0x1: To MSB
17	UNPACK_TIGHT	0x0: Loose 0x1: Tight
16:13	UNPACK_COUNT	Valid unpacking pattern count: 0 = 1 component, 1 = 2 components, ..., 15 = 16 components. Unpacking pattern only applies to the interleaved plane (chroma plane in pseudo-planar).
12:11	RESERVED_BITS12_11	Reserved for backward compatibility.

ROTATOR_SRC_FORMAT_C1 (cont.)

Bits	Name	Description
10:9	SRC_BPP	Effective source byte per pixel: 0 = 1 byte, 1 = 2 bytes, 2 = 3 bytes, 3 = 4 bytes. This is only used when unpacking the interleaved plane.
8	SRCC3_EN	0x1: Source has alpha
7:6	SRCC3_BITS	Number of bits for component 3 (alpha) input, this is not used for dither: 0 = RESERVED, 1 = RESERVED, 2 = RESERVED, 3 = 8 bits.
5:4	SRCC2_BITS	Number of bits for component 2 (R / Cr) input: 0 = RESERVED, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	SRCC1_BITS	Number of bits for component 1 (B / Cb) input: 0 = RESERVED, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	SRCC0_BITS	Number of bits for component 0 (G / luma) input: 0 = RESERVED, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x04E01328 ROTATOR_SRC_UNPACK_PATTERN1_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0302_0001

Unpacking pattern, maximum of 4 pattern elements starting from LSB to MSB (0 to 4) for context1. Default is ARGB or C3-C2-C0-C1.

ROTATOR_SRC_UNPACK_PATTERN1_C1

Bits	Name	Description
31:26	RESERVED31_26	
25:24	ELEMENT3	0x0: C0 0x1: C1 0x2: C2 0x3: C3
23:18	RESERVED23_18	
17:16	ELEMENT2	0x0: C0 0x1: C1 0x2: C2 0x3: C3
15:10	RESERVED15_10	
9:8	ELEMENT1	0x0: C0 0x1: C1 0x2: C2 0x3: C3

ROTATOR_SRC_UNPACK_PATTERN1_C1 (cont.)

Bits	Name	Description
7:2	RESERVED7_2	
1:0	ELEMENT0	0x0: C0 0x1: C1 0x2: C2 0x3: C3

0x04E01338 ROTATOR_SUB_BLOCK_CFG_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SUB_BLOCK_CFG_C1 is used for context1.

ROTATOR_SUB_BLOCK_CFG_C1

Bits	Name	Description
31:24	RESERVED_BIT31_24	
23	RESERVED_BIT23	
22:21	RESERVED_BITS22_21	.
20	RESERVED_BIT20	
19:18	SRC_CHROMA_SAMP	Source chroma sampling (used by upsample block): 0x0: 4:4:4/RGB 0x1: H2V1 0x2: H1V2 0x3: 4:2:0.
17:12	RESERVED_BITS17_12	
11:9	ROT_MODE	Rotation mode: Bit 0: Rotate 90 degrees Bit 1: Left/right flip Bit 2: Up/down flip.
8	ROT_EN	Rotate buffer enable. When this bit is set (1), the ping-pong tile buffer is always used independent of the rotation mode.
7:6	RESERVED_BIT7_6	
5	ALPHA_DOWN_SCALE	ALPHA Channel Down-scale option 0x1: using 1/N scaling 0x0: using pixel drop

ROTATOR_SUB_BLOCK_CFG_C1 (cont.)

Bits	Name	Description
4	FAST_YUV_TRANS	Fast YUV(YCbCr) data transaction <WAVERIDER:NEW:FAST_YUV> 0x1: enable Fast yuv transaction for YUV420 planer and psuedo-planer. 0x0: using normal YUV transaction (default)
3:2	DOWN_SCALE_V_RATIO	Down Scaling ratio for Vertical <WAVERIDER:NEW:DOWN_SCALE> 0x3: 1/8 down scaling 0x2: 1/4 down scaling 0x1: 1/2 down scaling 0x0: no down scaling (default)
1:0	DOWN_SCALE_H_RATIO	Down Scaling ratio for Horizontal <WAVERIDER:NEW:DOWN_SCALE> 0x3: 1/8 down scaling 0x2: 1/4 down scaling 0x1: 1/2 down scaling 0x0: no down scaling (default)

0x04E01354 ROTATOR_OUT_PACK_PATTERN1_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0302_0001

ROTATOR_OUT_PACK_PATTERN1_C1 is used for context1.

ROTATOR_OUT_PACK_PATTERN1_C1

Bits	Name	Description
31:26	RESERVED31_26	
25:24	ELEMENT3	0x0: C0 0x1: C1 0x2: C2 0x3: C3
23:18	RESERVED23_18	
17:16	ELEMENT2	0x0: C0 0x1: C1 0x2: C2 0x3: C3
15:10	RESERVED15_10	

ROTATOR_OUT_PACK_PATTERN1_C1 (cont.)

Bits	Name	Description
9:8	ELEMENT1	0x0: C0 0x1: C1 0x2: C2 0x3: C3
7:2	RESERVED7_2	
1:0	ELEMENT0	0x0: C0 0x1: C1 0x2: C2 0x3: C3

0x04E01368 ROTATOR_OUTP0_ADDR_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

Context1 output address for RGB or Y for Pseudo-planer or Planer.

ROTATOR_OUTP0_ADDR_C1

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E0136C ROTATOR_OUTP1_ADDR_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

Context1 output address for UV for Pseudo-planer or U for Planer.

ROTATOR_OUTP1_ADDR_C1

Bits	Name	Description
31:0	DSTP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x04E01370 ROTATOR_OUTP2_ADDR_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

Context1 output address for V for Planer.

ROTATOR_OUTP2_ADDR_C1

Bits	Name	Description
31:0	DSTP2_ADDR	Base byte address of the Image's planar color2 plane if using fast_yuv mode for planer YUV420 input

0x04E01378 ROTATOR_OUT_YSTRIDE1_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0080

ROTATOR_OUT_YSTRIDE1_C1 is used for context1.

ROTATOR_OUT_YSTRIDE1_C1

Bits	Name	Description
31	RESERVED_BIT31	
30:16	DSTP1_YSTRIDE	Plane 1 y stride in bytes.
15	RESERVED_BIT15	
14:0	DSTP0_YSTRIDE	Plane 0 y stride in bytes.

0x04E0137C ROTATOR_OUT_YSTRIDE2_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0080

ROTATOR_OUT_YSTRIDE2_C1 is used for context1.

ROTATOR_OUT_YSTRIDE2_C1

Bits	Name	Description
31:15	RESERVED_BITS_31_15	
14:0	DSTP2_YSTRIDE	Plane 2y stride in bytes.

0x04E01400 ROTATOR_SRC_XY_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRC_XY_C1 is used for context1.

ROTATOR_SRC_XY_C1

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_Y	Source ROI origin screen Y coordinate (pixel) in the source image (i.e., Y offset of source ROI in the source image).
15:13	RESERVED_BITS15_13	
12:0	SRC_X	Source ROI origin screen X coordinate (pixel) in the source image (i.e., X offset of source ROI in the source image).

0x04E01408 ROTATOR_SRC_IMAGE_SIZE_C1

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0020_0020

ROTATOR_SRC_IMAGE_SIZE_C1 is used for context1.

ROTATOR_SRC_IMAGE_SIZE_C1

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_IMG_H	Source image height (to determine if lines should be over-fetched or repeated).
15:13	RESERVED_BITS15_13	
12:0	SRC_IMG_W	Source image width (to determine if pixels should be over-fetched or repeated).

0x04E01508 ROTATOR_SRC_SIZE_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0020_0020

ROTATOR_SRC_SIZE_C2 is used for rotator source size for context2.

ROTATOR_SRC_SIZE_C2

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_H	Height of input ROI image that needs to be fetched in pixel, including any amount of over-fetching/under-fetching necessary.
15:13	RESERVED_BITS15_13	
12:0	SRC_W	Width of input ROI image that needs to be fetched in pixel, including any amount of over-fetching/under-fetching necessary.

0x04E0150C ROTATOR_SRCP0_ADDR_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRCP0_ADDR_C2 is context2 rotator source plane0 offset address.

ROTATOR_SRCP0_ADDR_C2

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format or planar color0 plane

0x04E01510 ROTATOR_SRCP1_ADDR_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRCP1_ADDR_C2 is for context2 rotator source plane1 offset address.

ROTATOR_SRCP1_ADDR_C2

Bits	Name	Description
31:0	SRCP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format or planar color1 plane

0x04E01514 ROTATOR_SRCP2_ADDR_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRCP2_ADDR_C2 is for context2 rotator source plane2 offset address.

ROTATOR_SRCP2_ADDR_C2

Bits	Name	Description
31:0	SRCP2_ADDR	Base byte address of the Image's planar color2 plane

0x04E0151C ROTATOR_SRC_YSTRIDE1_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0080

ROTATOR_SRC_YSTRIDE1_C2 is used for context2 rotator plane0 and plane1 Y stride.

ROTATOR_SRC_YSTRIDE1_C2

Bits	Name	Description
31	RESERVED_BIT31	
30:16	SRCP1_YSTRIDE	Plane 1 y stride in bytes.
15	RESERVED_BIT15	
14:0	SRCP0_YSTRIDE	Plane 0 y stride in bytes.

0x04E01520 ROTATOR_SRC_YSTRIDE2_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRC_YSTRIDE1_C2 is used for context2 rotator plane2 Y stride.

ROTATOR_SRC_YSTRIDE2_C2

Bits	Name	Description
31:15	RESERVED_BI31_15	
14:0	SRCP2_YSTRIDE	Plane 2 y stride in bytes.

0x04E01524 ROTATOR_SRC_FORMAT_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0042_67FF

ROTATOR_SRC_FORMAT_C2 is used for context2 rotator source format.

ROTATOR_SRC_FORMAT_C2

Bits	Name	Description
31	RESERVED_BIT31	
30:29	FRAME_FORMAT	0x0: Linear Frame (default) 0x1: RESERVED 0x2: 64x32 super-tile, YCbCr 420 non folding
28:26	RESERVED_BITS_28_26	
25:24	FORMAT_CONV	0x0: No format conversion 0x1: ARGB32bpp to RGB24bpp 0x2: RESERVED_1 0x3: RESERVED_2
23:22	FETCH_TILE_SIZE	Specify the fetch tile size. 0x0: RESERVED_1 0x1: 64x64 (default) 0x2: RESERVED_2 0x3: RESERVED_3
21	RESERVED_BITS_21	
20:19	FETCH_PLANES	Determines the number of planes to fetch and write back. When this parameter is set to planer format the output of Rotator is forced to write out a Pseudo planar format. When this parameter is set to fetch H2V1 422 interleaved format the output of Rotator is forced to write back 422 Pseudo planar format. For all the other cases the Rotators output write back format is same as the input fetch format. 0x0: Interleaved 0x1: Planar 0x2: Pseudo planar
18	UNPACK_ALIGN	0x0: To LSB 0x1: To MSB
17	UNPACK_TIGHT	0x0: Loose 0x1: Tight
16:13	UNPACK_COUNT	Valid unpacking pattern count: 0 = 1 component, 1 = 2 components, ..., 15 = 16 components. Unpacking pattern only applies to the interleaved plane (chroma plane in pseudo-planar).
12:11	RESERVED_BITS12_11	Reserved for backward compatibility.

ROTATOR_SRC_FORMAT_C2 (cont.)

Bits	Name	Description
10:9	SRC_BPP	Effective source byte per pixel: 0 = 1 byte, 1 = 2 bytes, 2 = 3 bytes, 3 = 4 bytes. This is only used when unpacking the interleaved plane.
8	SRCC3_EN	0x1: Source has alpha
7:6	SRCC3_BITS	Number of bits for component 3 (alpha) input, this is not used for dither: 0 = RESERVED, 1 = RESERVED, 2 = RESERVED, 3 = 8 bits.
5:4	SRCC2_BITS	Number of bits for component 2 (R / Cr) input: 0 = RESERVED, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	SRCC1_BITS	Number of bits for component 1 (B / Cb) input: 0 = RESERVED, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	SRCC0_BITS	Number of bits for component 0 (G / luma) input: 0 = RESERVED, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x04E01528 ROTATOR_SRC_UNPACK_PATTERN1_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0302_0001

Unpacking pattern, maximum of 4 pattern elements starting from LSB to MSB (0 to 4) for context2. Default is ARGB or C3-C2-C0-C1.

ROTATOR_SRC_UNPACK_PATTERN1_C2

Bits	Name	Description
31:26	RESERVED31_26	
25:24	ELEMENT3	0x0: C0 0x1: C1 0x2: C2 0x3: C3
23:18	RESERVED23_18	
17:16	ELEMENT2	0x0: C0 0x1: C1 0x2: C2 0x3: C3
15:10	RESERVED15_10	
9:8	ELEMENT1	0x0: C0 0x1: C1 0x2: C2 0x3: C3

ROTATOR_SRC_UNPACK_PATTERN1_C2 (cont.)

Bits	Name	Description
7:2	RESERVED7_2	
1:0	ELEMENT0	0x0: C0 0x1: C1 0x2: C2 0x3: C3

0x04E01538 ROTATOR_SUB_BLOCK_CFG_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SUB_BLOCK_CFG_C2 is used for context2.

ROTATOR_SUB_BLOCK_CFG_C2

Bits	Name	Description
31:24	RESERVED_BIT31_24	
23	RESERVED_BIT23	
22:21	RESERVED_BITS22_21	.
20	RESERVED_BIT20	
19:18	SRC_CHROMA_SAMP	Source chroma sampling (used by upsample block): 0x0: 4:4:4/RGB 0x1: H2V1 0x2: H1V2 0x3: 4:2:0.
17:12	RESERVED_BITS17_12	
11:9	ROT_MODE	Rotation mode: Bit 0: Rotate 90 degrees Bit 1: Left/right flip Bit 2: Up/down flip.
8	ROT_EN	Rotate buffer enable. When this bit is set (1), the ping-pong tile buffer is always used independent of the rotation mode.
7:6	RESERVED_BIT7_6	
5	ALPHA_DOWN_SCALE	ALPHA Channel Down-scale option 0x1: using 1/N scaling 0x0: using pixel drop

ROTATOR_SUB_BLOCK_CFG_C2 (cont.)

Bits	Name	Description
4	FAST_YUV_TRANS	Fast YUV(YCbCr) data transaction <WAVERIDER:NEW:FAST_YUV> 0x1: enable Fast yuv transaction for YUV420 planer and psuedo-planer 0x0: using normal YUV transaction (default)
3:2	DOWN_SCALE_V_RATIO	Down Scaling ratio for Vertical <WAVERIDER:NEW:DOWN_SCALE> 0x3: 1/8 down scaling 0x2: 1/4 down scaling 0x1: 1/2 down scaling 0x0: no down scaling (default)
1:0	DOWN_SCALE_H_RATIO	Down Scaling ratio for Horizontal <WAVERIDER:NEW:DOWN_SCALE> 0x3: 1/8 down scaling 0x2: 1/4 down scaling 0x1: 1/2 down scaling 0x0: no down scaling (default)

0x04E01554 ROTATOR_OUT_PACK_PATTERN1_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0302_0001

ROTATOR_OUT_PACK_PATTERN1_C2 is used for context2.

ROTATOR_OUT_PACK_PATTERN1_C2

Bits	Name	Description
31:26	RESERVED31_26	
25:24	ELEMENT3	0x0: C0 0x1: C1 0x2: C2 0x3: C3
23:18	RESERVED23_18	
17:16	ELEMENT2	0x0: C0 0x1: C1 0x2: C2 0x3: C3
15:10	RESERVED15_10	

ROTATOR_OUT_PACK_PATTERN1_C2 (cont.)

Bits	Name	Description
9:8	ELEMENT1	0x0: C0 0x1: C1 0x2: C2 0x3: C3
7:2	RESERVED7_2	
1:0	ELEMENT0	0x0: C0 0x1: C1 0x2: C2 0x3: C3

0x04E01568 ROTATOR_OUTP0_ADDR_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

Context2 output address for RGB or Y for Pseudo-planer or Planer.

ROTATOR_OUTP0_ADDR_C2

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E0156C ROTATOR_OUTP1_ADDR_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

Context2 output address for UV for Pseudo-planer or U for Planer.

ROTATOR_OUTP1_ADDR_C2

Bits	Name	Description
31:0	DSTP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x04E01570 ROTATOR_OUTP2_ADDR_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

Context2 output address for V for Planer.

ROTATOR_OUTP2_ADDR_C2

Bits	Name	Description
31:0	DSTP2_ADDR	Base byte address of the Image's planar color2 plane if using fast_yuv mode for planer YUV420 input

0x04E01578 ROTATOR_OUT_YSTRIDE1_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0080

ROTATOR_OUT_YSTRIDE1_C2 is used for context2.

ROTATOR_OUT_YSTRIDE1_C2

Bits	Name	Description
31	RESERVED_BIT31	
30:16	DSTP1_YSTRIDE	Plane 1 y stride in bytes.
15	RESERVED_BIT15	
14:0	DSTP0_YSTRIDE	Plane 0 y stride in bytes.

0x04E0157C ROTATOR_OUT_YSTRIDE2_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0080

ROTATOR_OUT_YSTRIDE2_C2 is used for context2.

ROTATOR_OUT_YSTRIDE2_C2

Bits	Name	Description
31:15	RESERVED_BITS31_15	
14:0	DSTP2_YSTRIDE	Plane 2y stride in bytes.

0x04E01600 ROTATOR_SRC_XY_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRC_XY_C2 is used for context2.

ROTATOR_SRC_XY_C2

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_Y	Source ROI origin screen Y coordinate (pixel) in the source image (i.e., Y offset of source ROI in the source image).
15:13	RESERVED_BITS15_13	
12:0	SRC_X	Source ROI origin screen X coordinate (pixel) in the source image (i.e., X offset of source ROI in the source image).

0x04E01608 ROTATOR_SRC_IMAGE_SIZE_C2

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0020_0020

ROTATOR_SRC_IMAGE_SIZE_C2 is used for context2.

ROTATOR_SRC_IMAGE_SIZE_C2

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_IMG_H	Source image height (to determine if lines should be over-fetched or repeated).
15:13	RESERVED_BITS15_13	
12:0	SRC_IMG_W	Source image width (to determine if pixels should be over-fetched or repeated).

0x04E01708 ROTATOR_SRC_SIZE_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0020_0020

ROTATOR_SRC_SIZE_C3 is used for rotator source size for context3.

ROTATOR_SRC_SIZE_C3

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_H	Height of input ROI image that needs to be fetched in pixel, including any amount of over-fetching/under-fetching necessary.
15:13	RESERVED_BITS15_13	
12:0	SRC_W	Width of input ROI image that needs to be fetched in pixel, including any amount of over-fetching/under-fetching necessary.

0x04E0170C ROTATOR_SRCP0_ADDR_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRCP0_ADDR_C3 is context3 rotator source plane0 offset address.

ROTATOR_SRCP0_ADDR_C3

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format or planar color0 plane

0x04E01710 ROTATOR_SRCP1_ADDR_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRCP1_ADDR_C3 is for context3 rotator source plane1 offset address.

ROTATOR_SRCP1_ADDR_C3

Bits	Name	Description
31:0	SRCP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format or planar color1 plane

0x04E01714 ROTATOR_SRCP2_ADDR_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRCP2_ADDR_C3 is for context3 rotator source plane2 offset address.

ROTATOR_SRCP2_ADDR_C3

Bits	Name	Description
31:0	SRCP2_ADDR	Base byte address of the Image's planar color2 plane

0x04E0171C ROTATOR_SRC_YSTRIDE1_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0080

ROTATOR_SRC_YSTRIDE1_C3 is used for context3 rotator plane0 and plane1 Y stride.

ROTATOR_SRC_YSTRIDE1_C3

Bits	Name	Description
31	RESERVED_BIT31	
30:16	SRCP1_YSTRIDE	Plane 1 y stride in bytes.
15	RESERVED_BIT15	
14:0	SRCP0_YSTRIDE	Plane 0 y stride in bytes.

0x04E01720 ROTATOR_SRC_YSTRIDE2_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRC_YSTRIDE1_C3 is used for context3 rotator plane2 Y stride.

ROTATOR_SRC_YSTRIDE2_C3

Bits	Name	Description
31:15	RESERVED_BI31_15	
14:0	SRCP2_YSTRIDE	Plane 2 y stride in bytes.

0x04E01724 ROTATOR_SRC_FORMAT_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0042_67FF

ROTATOR_SRC_FORMAT_C3 is used for context3 rotator source format.

ROTATOR_SRC_FORMAT_C3

Bits	Name	Description
31	RESERVED_BIT31	
30:29	FRAME_FORMAT	0x0: Linear Frame (default) 0x1: RESERVED 0x2: 64x32 super-tile, YCbCr 420 non folding
28:26	RESERVED_BITS_28_26	
25:24	FORMAT_CONV	0x0: No format conversion 0x1: ARGB32bpp to RGB24bpp 0x2: RESERVED_1 0x3: RESERVED_2
23:22	FETCH_TILE_SIZE	Specify the fetch tile size. 0x0: RESERVED_1 0x1: 64x64 (default) 0x2: RESERVED_2 0x3: RESERVED_3
21	RESERVED_BITS_21	
20:19	FETCH_PLANES	Determines the number of planes to fetch and write back. When this parameter is set to planer format the output of Rotator is forced to write out a Pseudo planar format. When this parameter is set to fetch H2V1 422 interleaved format the output of Rotator is forced to write back 422 Pseudo planar format. For all the other cases the Rotators output write back format is same as the input fetch format. 0x0: Interleaved 0x1: Planar 0x2: Pseudo planar
18	UNPACK_ALIGN	0x0: To LSB 0x1: To MSB
17	UNPACK_TIGHT	0x0: Loose 0x1: Tight
16:13	UNPACK_COUNT	Valid unpacking pattern count: 0 = 1 component, 1 = 2 components, ..., 15 = 16 components. Unpacking pattern only applies to the interleaved plane (chroma plane in pseudo-planar).
12:11	RESERVED_BITS12_11	Reserved for backward compatibility.

ROTATOR_SRC_FORMAT_C3 (cont.)

Bits	Name	Description
10:9	SRC_BPP	Effective source byte per pixel: 0 = 1 byte, 1 = 2 bytes, 2 = 3 bytes, 3 = 4 bytes. This is only used when unpacking the interleaved plane.
8	SRCC3_EN	0x1: Source has alpha
7:6	SRCC3_BITS	Number of bits for component 3 (alpha) input, this is not used for dither: 0 = RESERVED, 1 = RESERVED, 2 = RESERVED, 3 = 8 bits.
5:4	SRCC2_BITS	Number of bits for component 2 (R / Cr) input: 0 = RESERVED, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	SRCC1_BITS	Number of bits for component 1 (B / Cb) input: 0 = RESERVED, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	SRCC0_BITS	Number of bits for component 0 (G / luma) input: 0 = RESERVED, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x04E01728 ROTATOR_SRC_UNPACK_PATTERN1_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0302_0001

Unpacking pattern, maximum of 4 pattern elements starting from LSB to MSB (0 to 4) for context3. Default is ARGB or C3-C2-C0-C1.

ROTATOR_SRC_UNPACK_PATTERN1_C3

Bits	Name	Description
31:26	RESERVED31_26	
25:24	ELEMENT3	0x0: C0 0x1: C1 0x2: C2 0x3: C3
23:18	RESERVED23_18	
17:16	ELEMENT2	0x0: C0 0x1: C1 0x2: C2 0x3: C3
15:10	RESERVED15_10	
9:8	ELEMENT1	0x0: C0 0x1: C1 0x2: C2 0x3: C3

ROTATOR_SRC_UNPACK_PATTERN1_C3 (cont.)

Bits	Name	Description
7:2	RESERVED7_2	
1:0	ELEMENT0	0x0: C0 0x1: C1 0x2: C2 0x3: C3

0x04E01738 ROTATOR_SUB_BLOCK_CFG_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SUB_BLOCK_CFG_C3 is used for context3.

ROTATOR_SUB_BLOCK_CFG_C3

Bits	Name	Description
31:24	RESERVED_BIT31_24	
23	RESERVED_BIT23	
22:21	RESERVED_BITS22_21	.
20	RESERVED_BIT20	
19:18	SRC_CHROMA_SAMP	Source chroma sampling (used by upsample block): 0x0: 4:4:4/RGB 0x1: H2V1 0x2: H1V2 0x3: 4:2:0.
17:12	RESERVED_BITS17_12	
11:9	ROT_MODE	Rotation mode: Bit 0: Rotate 90 degrees Bit 1: Left/right flip Bit 2: Up/down flip.
8	ROT_EN	Rotate buffer enable. When this bit is set (1), the ping-pong tile buffer is always used independent of the rotation mode.
7:6	RESERVED_BIT7_6	
5	ALPHA_DOWN_SCALE	ALPHA Channel Down-scale option 0x1: using 1/N scaling 0x0: using pixel drop

ROTATOR_SUB_BLOCK_CFG_C3 (cont.)

Bits	Name	Description
4	FAST_YUV_TRANS	Fast YUV(YCbCr) data transaction <WAVERIDER:NEW:FAST_YUV> 0x1: enable Fast yuv transaction for YUV420 planer and psuedo-planer 0x0: using normal YUV transaction (default)
3:2	DOWN_SCALE_V_RATIO	Down Scaling ratio for Vertical <WAVERIDER:NEW:DOWN_SCALE> 0x3: 1/8 down scaling 0x2: 1/4 down scaling 0x1: 1/2 down scaling 0x0: no down scaling (default)
1:0	DOWN_SCALE_H_RATIO	Down Scaling ratio for Horizontal <WAVERIDER:NEW:DOWN_SCALE> 0x3: 1/8 down scaling 0x2: 1/4 down scaling 0x1: 1/2 down scaling 0x0: no down scaling (default)

0x04E01754 ROTATOR_OUT_PACK_PATTERN1_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0302_0001

ROTATOR_OUT_PACK_PATTERN1_C3 is used for context3.

ROTATOR_OUT_PACK_PATTERN1_C3

Bits	Name	Description
31:26	RESERVED31_26	
25:24	ELEMENT3	0x0: C0 0x1: C1 0x2: C2 0x3: C3
23:18	RESERVED23_18	
17:16	ELEMENT2	0x0: C0 0x1: C1 0x2: C2 0x3: C3
15:10	RESERVED15_10	

ROTATOR_OUT_PACK_PATTERN1_C3 (cont.)

Bits	Name	Description
9:8	ELEMENT1	0x0: C0 0x1: C1 0x2: C2 0x3: C3
7:2	RESERVED7_2	
1:0	ELEMENT0	0x0: C0 0x1: C1 0x2: C2 0x3: C3

0x04E01768 ROTATOR_OUTP0_ADDR_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

Context1 output address for RGB or Y for Pseudo-planer or Planer.

ROTATOR_OUTP0_ADDR_C3

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E0176C ROTATOR_OUTP1_ADDR_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

Context3 output address for UV for Pseudo-planer or U for Planer.

ROTATOR_OUTP1_ADDR_C3

Bits	Name	Description
31:0	DSTP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x04E01770 ROTATOR_OUTP2_ADDR_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

Context3 output address for V for Planer.

ROTATOR_OUTP2_ADDR_C3

Bits	Name	Description
31:0	DSTP2_ADDR	Base byte address of the Image's planar color2 plane if using fast_yuv mode for planer YUV420 input

0x04E01778 ROTATOR_OUT_YSTRIDE1_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0080

ROTATOR_OUT_YSTRIDE1_C3 is used for context3.

ROTATOR_OUT_YSTRIDE1_C3

Bits	Name	Description
31	RESERVED_BIT31	
30:16	DSTP1_YSTRIDE	Plane 1 y stride in bytes.
15	RESERVED_BIT15	
14:0	DSTP0_YSTRIDE	Plane 0 y stride in bytes.

0x04E0177C ROTATOR_OUT_YSTRIDE2_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0080

ROTATOR_OUT_YSTRIDE2_C3 is used for context3.

ROTATOR_OUT_YSTRIDE2_C3

Bits	Name	Description
31:15	RESERVED_BITS31_15	
14:0	DSTP2_YSTRIDE	Plane 2y stride in bytes.

0x04E01800 ROTATOR_SRC_XY_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_SRC_XY_C3 is used for context3.

ROTATOR_SRC_XY_C3

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_Y	Source ROI origin screen Y coordinate (pixel) in the source image (i.e., Y offset of source ROI in the source image).
15:13	RESERVED_BITS15_13	
12:0	SRC_X	Source ROI origin screen X coordinate (pixel) in the source image (i.e., X offset of source ROI in the source image).

0x04E01808 ROTATOR_SRC_IMAGE_SIZE_C3

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0020_0020

ROTATOR_SRC_IMAGE_SIZE_C3 is used for context3.

ROTATOR_SRC_IMAGE_SIZE_C3

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_IMG_H	Source image height (to determine if lines should be over-fetched or repeated).
15:13	RESERVED_BITS15_13	
12:0	SRC_IMG_W	Source image width (to determine if pixels should be over-fetched or repeated).

0x04E018F4 ROTATOR_OUTP0_DMI_VG1_BUF0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP0_DMI_VG1_BUF0_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E018F8 ROTATOR_OUTP1_DMI_VG1_BUF0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP1_DMI_VG1_BUF0_ADDR

Bits	Name	Description
31:0	DSTP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x04E018FC ROTATOR_OUTP2_DMI_VG1_BUF0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP2_DMI_VG1_BUF0_ADDR

Bits	Name	Description
31:0	DSTP2_ADDR	Base byte address of the Image's planar color2 plane if using fast_yuv mode for planer YUV420 input.

0x04E01900 ROTATOR_OUTP0_DMI_VG1_BUF1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP0_DMI_VG1_BUF1_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01904 ROTATOR_OUTP1_DMI_VG1_BUF1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP1_DMI_VG1_BUF1_ADDR

Bits	Name	Description
31:0	DSTP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x04E01908 ROTATOR_OUTP2_DMI_VG1_BUF1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP2_DMI_VG1_BUF1_ADDR

Bits	Name	Description
31:0	DSTP2_ADDR	Base byte address of the Image's planar color2 plane if using fast_yuv mode for planer YUV420 input.

0x04E0190C ROTATOR_OUTP0_DMI_VG1_BUF2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP0_DMI_VG1_BUF2_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01910 ROTATOR_OUTP1_DMI_VG1_BUF2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP1_DMI_VG1_BUF2_ADDR

Bits	Name	Description
31:0	DSTP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x04E01914 ROTATOR_OUTP2_DMI_VG1_BUF2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP2_DMI_VG1_BUF2_ADDR

Bits	Name	Description
31:0	DSTP2_ADDR	Base byte address of the Image's planar color2 plane if using fast yuv mode for planer YUV420 input.

0x04E01918 ROTATOR_OUTP0_DMI_VG2_BUF0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP0_DMI_VG2_BUF0_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E0191C ROTATOR_OUTP1_DMI_VG2_BUF0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP1_DMI_VG2_BUF0_ADDR

Bits	Name	Description
31:0	DSTP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x04E01920 ROTATOR_OUTP2_DMI_VG2_BUF0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP2_DMI_VG2_BUF0_ADDR

Bits	Name	Description
31:0	DSTP2_ADDR	Base byte address of the Image's planar color2 plane if using fast yuv mode for planer YUV420 input.

0x04E01924 ROTATOR_OUTP0_DMI_VG2_BUF1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP0_DMI_VG2_BUF1_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01928 ROTATOR_OUTP1_DMI_VG2_BUF1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP1_DMI_VG2_BUF1_ADDR

Bits	Name	Description
31:0	DSTP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x04E0192C ROTATOR_OUTP2_DMI_VG2_BUF1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_OUTP2_DMI_VG2_BUF1_ADDR

Bits	Name	Description
31:0	DSTP2_ADDR	Base byte address of the Image's planar color2 plane if using fast yuv mode for planer YUV420 input.

0x04E01930 ROTATOR_OUTP0_DMI_VG2_BUF2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP VG2 destination buffer2.

ROTATOR_OUTP0_DMI_VG2_BUF2_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01934 ROTATOR_OUTP1_DMI_VG2_BUF2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane1 DMI MDP VG2 destination buffer2.

ROTATOR_OUTP1_DMI_VG2_BUF2_ADDR

Bits	Name	Description
31:0	DSTP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x04E01938 ROTATOR_OUTP2_DMI_VG2_BUF2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane2 DMI MDP VG2 destination buffer2.

ROTATOR_OUTP2_DMI_VG2_BUF2_ADDR

Bits	Name	Description
31:0	DSTP2_ADDR	Base byte address of the Image's planar color2 plane if using fast yuv mode for planer YUV420 input.

0x04E0193C ROTATOR_OUTP0_DMI_RGB1_BUF0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP RGB1 destination buffer0.

ROTATOR_OUTP0_DMI_RGB1_BUF0_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01940 ROTATOR_OUTP0_DMI_RGB1_BUF1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP RGB1 destination buffer1.

ROTATOR_OUTP0_DMI_RGB1_BUF1_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01944 ROTATOR_OUTP0_DMI_RGB1_BUF2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP RGB1 destination buffer2.

ROTATOR_OUTP0_DMI_RGB1_BUF2_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01948 ROTATOR_OUTP0_DMI_RGB2_BUF0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP RGB2 destination buffer0.

ROTATOR_OUTP0_DMI_RGB2_BUF0_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E0194C ROTATOR_OUTP0_DMI_RGB2_BUF1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP RGB2 destination buffer1.

ROTATOR_OUTP0_DMI_RGB2_BUF1_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01950 ROTATOR_OUTP0_DMI_RGB2_BUF2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP RGB2 destination buffer2.

ROTATOR_OUTP0_DMI_RGB2_BUF2_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01954 ROTATOR_OUTP0_DMI_DMA_P_BUF0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP DMA_P destination buffer0.

ROTATOR_OUTP0_DMI_DMA_P_BUF0_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01958 ROTATOR_OUTP0_DMI_DMA_P_BUF1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP DMA_P destination buffer1.

ROTATOR_OUTP0_DMI_DMA_P_BUF1_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E0195C ROTATOR_OUTP0_DMI_DMA_P_BUF2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP DMA_P destination buffer2.

ROTATOR_OUTP0_DMI_DMA_P_BUF2_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01960 ROTATOR_OUTP0_DMI_DMA_S_BUF0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP DMA_S destination buffer0.

ROTATOR_OUTP0_DMI_DMA_S_BUF0_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01964 ROTATOR_OUTP0_DMI_DMA_S_BUF1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP DMA_S destination buffer1.

ROTATOR_OUTP0_DMI_DMA_S_BUF1_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01968 ROTATOR_OUTP0_DMI_DMA_S_BUF2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP DMA_S destination buffer2.<WAVERIDER:NEW:DMI>

ROTATOR_OUTP0_DMI_DMA_S_BUF2_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E0196C ROTATOR_OUTP0_DMI_DMA_E_BUF0_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP DMA_E destination buffer0.

ROTATOR_OUTP0_DMI_DMA_E_BUF0_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01970 ROTATOR_OUTP0_DMI_DMA_E_BUF1_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP DMA_E destination buffer1.

ROTATOR_OUTP0_DMI_DMA_E_BUF1_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E01974 ROTATOR_OUTP0_DMI_DMA_E_BUF2_ADDR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

it is used for plane0 DMI MDP DMA_E destination buffer2.

ROTATOR_OUTP0_DMI_DMA_E_BUF2_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x04E02004 ROTATOR_TFETCH_TEST_MODE

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_TFETCH_TEST_MODE

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	TFETCH_SOLID_FILL	This takes precedence over tfetch_unpack_bypass. If this bit is set (1), the output color is forced to the value written into register 0x20040.This is useful in filling a ROI with a constant color.
0	TFETCH_UNPACK_BYPASS	Setting (1)this bit enables a bypass in the unpacker. Therefore, each data read would be treated as color0, color1, color2, and color3 from lower byte to upper byte.

0x04E02008 ROTATOR_TFETCH_STATUS

Type: Read Only
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_001F

ROTATOR_TFETCH_STATUS

Bits	Name	Description
31:12	RESERVED_BITS31_12	
11:8	FIFO_ERRORS	TileFetch internal FIFO errors. These error bits are pulse catching, and returned to zero when this register is read: Bit 11 = control FIFO error Bit 10 = burstbuf FIFO error Bit 9= line_gen luma FIFO error Bit 8= line_gen chroma FIFO error
7:5	RESERVED_BITS7_5	

ROTATOR_TFETCH_STATUS (cont.)

Bits	Name	Description
4:0	IDLES	TileFetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 4= dma_rd idle Bit 3= ctl idle Bit 2= burstbuf idle Bit 1= unpack idle Bit 0= line_gen idle

0x04E02010 ROTATOR_TFETCH_TILE_COUNT

Type: Read Only
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_TFETCH_TILE_COUNT

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:16	NUM_CHROMA_TILE	Number of chroma tiles in an ROI
15:11	RESERVED_BITS15_11	
10:0	NUM_LUMA_TILE	Number of luma/RGB tiles in an ROI

0x04E02014 ROTATOR_TFETCH_FETCH_COUNT

Type: Read Only
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

ROTATOR_TFETCH_FETCH_COUNT

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	P1_FETCH_COUNT	Plane 1 fetch count in an ROI
15	RESERVED_BIT15	
14:0	P0_FETCH_COUNT	Plane 0 fetch count in an ROI

0x04E02040 ROTATOR_TFETCH_CONSTANT_COLOR

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0xFFFF_FFFF

ROTATOR_TFETCH_CONSTANT_COLOR

Bits	Name	Description
31:24	FORCED_COLOR3	Constant color driven for color3 during color force mode.
23:16	FORCED_COLOR2	Constant color driven for color2 during color force mode.
15:8	FORCED_COLOR1	Constant color driven for color1 during color force mode.
7:0	FORCED_COLOR0	Constant color driven for color0 during color force mode.

14.12.6 Test MISR registers

0x04E0D000 ROTATOR_TEST_MODE_CLK

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_TEST_MODE_CLK register is used to select the test points for a specified ROTATOR block.

ROTATOR_TEST_MODE_CLK

Bits	Name	Description
31:9	RESERVED_BITS31_9	This field has no function and should be set to zero for future compatibility.

ROTATOR_TEST_MODE_CLK (cont.)

Bits	Name	Description
8:4	BLOCK_ID	These bits select the test points for the specified ROTATOR block into the test bus. 0x0: Disabled 0x1: Tile fetch 0x2: Upsample 0x3: Rotate 0x4: packer1a 0x5: packer1b 0x6: Downsample 0x7: cmd 0x8: ebi_gen2axi 0x9: top 0xA: mGEN2mAXI Client0 core clock (Rotator Core read) 0xB: mGEN2mAXI Client1 core clock (Rotator Core write) 0xC: scratchpad reg 0xD: DMI 0xE: Context Queue 0xF: Down Scaler 0x10: Pixel Rotator 0x11: 0x55555555 0x12: 0xAAAAAAAA
3:0	TEST_PT_SEL	These bits select a set of 32-bit test points within a ROTATOR block.

0x04E0D004 ROTATOR_TEST_MISR_RESET_CLK

Type: Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_TEST_MISR_RESET_CLK register is used to reset the MISR state.

ROTATOR_TEST_MISR_RESET_CLK

Bits	Name	Description
31:1	RESERVED_BITS31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_SW_RESET	A write of ’1’ to this address will reset the MISR state. It is a self clearing reset. The reset must be asserted after ROTATOR_TEST_MISR_MODE_CLK is set to a non-zero value. 0x1: MISR reset.

0x04E0D008 ROTATOR_TEST_EXPORT_MISR_CLK

Type: Read-Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_TEST_EXPORT_MISR_CLK register controls what is sent on the testbus. A value of ’0’ (reset value) will send the data that is going into the MISR on the testbus. A value of ’1’ will send the current MISR state onto the testbus. The latter option is typically used for debug purposes. For example, if your final MISR signature failed, you might want to know where it failed (i.e., right in the beginning or somewhere else’)

ROTATOR_TEST_EXPORT_MISR_CLK

Bits	Name	Description
31:1	RESERVED_BITS31_1	Field has no function and should be set to zero for future compatibility.
0	MISR_EXPORT	When clear(0), testbus is driven by what is sent into the MISR. (i.e., What is the result of the MUXing of all the input data streams with ROTATOR_TEST_ MODE_CLK) When set (1), testbus is driven by the current state of the MISR (debug typically)

0x04E0D00C ROTATOR_TEST_MISR_CURR_VAL_CLK

Type: Read-Only
Clock: CC_ROTATOR_CLK
Reset State: Undefined

A read from the address in the ROTATOR_TEST_MISR_CURR_VAL_CLK register will return the current MISR state for this block. Keep in mind that this could change every cycle depending on how it is used.

ROTATOR_TEST_MISR_CURR_VAL_CLK

Bits	Name	Description
31:0	MISR_VAL	It holds the current MISR state.

0x04E0D100 ROTATOR_TEST_MODE_AXI_CLK

Type: Read/Write
Clock: CC_ROTATOR_CLK
Reset State: 0x0000_0000

The ROTATOR_TEST_MODE_AXI_CLK register selects the test points for the specified mgen2maxi clients and master ports. This register is only valid for Rotator core that uses mgen2maxi.

ROTATOR_TEST_MODE_AXI_CLK

Bits	Name	Description
31:6	RESERVED31_6	This field has no function and should be set to zero for future compatibility.
5:4	BLOCK_ID	These bits select the test points for the specified Rotator block into the test bus. 0x0: Disabled 0x1: mGEN2mAXI Client0 (Rotator Core read) 0x2: mGEN2mAXI Client1 (Rotator Core write) 0x3: mGEN2mAXI AXI Arbiter/Master 0
3:0	TEST_PT_SEL	These bits select a set of 32-bit test points within a ROTATOR mgen2maxi block.

14.13 TV ENC Registers (0x04F00000 TV_ENC_BASE)

The TV_ENC registers in this section are accessed by the ARM. Software will be responsible for setting up all the programmable registers contained within the TV Encoder. TV Encoder Control and Timing registers

0x04F00000 TV_ENC_CTL

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00E08FC0

This register contains the basic control and mode registers for the TV_ENC. It is important that the Software must program this register in two steps. In the first step the Software should program all the necessary register bits except the "TV_ENC_EN" bit (which should be in disabled state). The second write to this register should enable the "TV_ENC_EN" bit without touching any other bit in this register. This will ensure that the TV Encoder Block is programmed to a valid state before it is enabled

TV_ENC_CTL

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23	CC_PEDESTAL_EN	0x0: disable pedestal on closed captioning line 0x1: enable pedestal on closed captioning line (default)
22	CHROMA_SAT_EN	This enable is valid only in S-Video Mode. It gives the flexibility to saturate the chroma output (post sinx and dc offset) to 0 or 1023 when saturation bit asserts 0x0: saturate the 10 bit chroma output to 0 0x1: saturate the 10 bit chroma output to1023 (default)
21	SINX_FILTER_EN_CH	This enable is valid only in S-Video Mode. It will enable/disable the Sinx filter on the Cb/Cr channel. 0x0: bypass Sin (x/x correction filter on Chroma Channel) 0x1: enable Sin (x/x correction filter on Chroma Channel default)
20	TV_DAC_TEST_SEL	This bit selects the data that will drive the TV_DAC (TV_ENC output OR the DAC test data specified by TV_DAC_CTL register) 0x0: Select TV Encoder data 0x1: Select DAC test data specified by TV_DAC_CTL
19	S_VIDEO_EN	0x0: disable S-VIDEO channel 0x1: enable S-VIDEO channel

TV_ENC_CTL (cont.)

Bits	Name	Description
18:15	TPG_SEL	0x0: color bar test pattern 100 pc white 0x1: modulated ramp test pattern 0x2: red frame test pattern 0x3: ntsc color bar 75 pc white 0x4: Mono color bar test pattern Black 0x5: Mono color bar test pattern White100 0x6: Mono color bar test pattern Yellow75 0x7: Mono color bar test pattern Cyan75 0x8: Mono color bar test pattern Green75 0x9: Mono color bar test pattern Magenta75 0xA: Mono color bar test pattern Red75 0xB: Mono color bar test pattern Blue75 0xC: Mono color bar test pattern White75 0xD: 100 pc while color bar test pattern with smooth transition
14	NTSCJ	This bit is ignored for all other tv_mode settings. 0x0: NTSC mode when tv_mode = "00" 0x1: NTSC-J mode when tv_mode = "00"
13	PAL60	This bit is ignored for all other tv_mode settings. 0x0: NTSC mode when tv_mode = "00" 0x1: PAL60 mode when tv_mode = "00"
12	OUTPUT_INV	0x0: do not subtract the encoder output from 1024 to invert 0x1: subtract the encoder output from 1024 to invert
11	TEST_PATT_EN	0x0: disable test pattern generator (normal video from MDP) 0x1: enable 75% color bar test pattern output.
10	SINX_FILTER_EN	0x0: bypass Sin (x/x correction filter) 0x1: enable Sin (x/x correction filter)
9	CB_FILTER_EN	0x0: bypass Cb channel LPF 0x1: enable Cb channel LPF
8	CR_FILTER_EN	0x0: bypass Cr channel LPF 0x1: enable Cr channel LPF
7	Y_FILTER_EN	0x0: bypass Y channel LPF 0x1: enable Y channel LPF
6	Y_FILTER_SEL	0x0: Select Y low pass filter w/o notch 0x1: Select Y low pass filter w/ notch
5	RESERVED_BIT5	
4	CGMS_EN	0x0: disable CGMS insertion 0x1: enable CGMS insertion
3	CC_EN	0x0: disable closed captioning 0x1: enable closed captioning

TV_ENC_CTL (cont.)

Bits	Name	Description
2	TV_ENC_EN	This register turns off/on the encoder. 0x0: TV_ENC off 0x1: TV_ENC on
1:0	TV_MODE	This register defines the TV standard and the corresponding sub-carrier frequency. See bit 13 for differentiation of mode 00. 0x0: NTSC-M, PAL60 (3.57954545 Mhz) 0x1: PAL-M (3.57961149 Mhz) 0x2: PAL-B,D,G,H,I, PAL-N (non-Argentina 4.3361875 Mhz) 0x3: PAL-N (Argentina 3.582055625 Mhz)

0x04F00004 TV_LEVEL

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register defines the DC level offset for the encoder. This is typically 16, although may be changed to satisfy the output driver swing. Translates into the sync level.

TV_LEVEL

Bits	Name	Description
31:20	BLANK_LEVEL_CHROMA	Blanking level to be added to the Chroma Channel (pre sinx filter) during the S-Video mode. This value won't affect the chroma channel when TV_ENC is in composite mode.
19	RESERVED_BIT19	
18:8	DC_OFFSET_CHROMA	DC offset of chroma output (Valid only when S-Video is enabled)
7:0	DC_OFFSET	DC offset of output (in practice, the sync level)

0x04F00008 TV_GAIN

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x0081B697

This register defines the independent gain factors for the 8 bit Y, Cr, and Cb channels. Each gain is a 8 bit value that represents an 8 bit fraction (0.8). This format gives the channel gains a range of 0 to 0.99609375. The normal gain values for PAL and NTSC are from 0.752 down to 0.504 so the range of the register allows for scaling above and below the normal amount.

TV_GAIN

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	CB_GAIN	8 bit Cb channel gain (0.8 fixed point format).
15:8	CR_GAIN	8 bit Cr channel gain (0.8 fixed point format).
7:0	Y_GAIN	8 bit Y channel gain (0.8 fixed point format).

0x04F0000C TV_OFFSET

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x008080F0

This register defines the independent offset factors for the 8 bit Y, Cr, and Cb channels. Each offset is a 8 bit 2's complement number. For normal operation, the Cr and Cb offsets should be set to 0x80 (-128) and the Y offset should be set to 0xF0 (-16)

TV_OFFSET

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	CB_OFFSET	2's complement 8 bit Cb channel offset.
15:8	CR_OFFSET	2's complement 8 bit Cr channel offset.
7:0	Y_OFFSET	2's complement 8 bit Y channel offset.

0x04F00010 TV_CGMS

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00012345

This register defines the 20 bit CGMS value that is driven on lines 20 and 283 when the CGMS mode is enabled.

TV_CGMS

Bits	Name	Description
31:20	RESERVED_BITS31_20	
19:0	CGMS_DATA	20 bit CGMS data value

0x04F00014 TV_SYNC_1

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x0020009E

This register defines the horizontal front porch and sync times with respect to a 27MHz clock.

TV_SYNC_1

Bits	Name	Description
31:25	RESERVED_BITS31_25	
24:16	HFP	Defines end of horizontal front porch with respect to the 27MHz clock.
15:9	RESERVED_BITS15_9	
8:0	HSYNC	Defines end of horizontal sync with respect to the 27Mhz clock.

0x04F00018 TV_SYNC_2

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x011306B4

This register defines the horizontal blanking and line times with respect to a 27MHz clock.

TV_SYNC_2

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	HBLANK	Defines end of horizontal blanking with respect the 27Mhz clock.
15:11	RESERVED_BITS16_11	
10:0	HTOTAL	Defines horizontal line length with respect to the 27Mhz clock.

0x04F0001C TV_SYNC_3

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x0006000C

This register defines the vertical front porch and sync times with respect to HLINES.

TV_SYNC_3

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	VFP	Defines End of vertical front porch in terms of HLines.
15:10	RESERVED_BITS15_10	
9:0	VSYNC	Defines End of vertical sync in terms of HLines.

0x04F00020 TV_SYNC_4

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x0028020D

This register defines the vertical blank and vertical total lines with respect to HLines.

TV_SYNC_4

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	VBLANK	Defines End of vertical blank in terms of HLines.
15:10	RESERVED_BITS15_10	
9:0	VTOTAL	Defines End of vertical Field in terms of Hlines.

0x04F00024 TV_SYNC_5

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x005E02FB

This register defines the equalization and serration end times with respect to a 27Mhz clock.

TV_SYNC_5

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	EQU	Defines End of Horizontal Equalization with respect to a 27Mhz clock
15:10	RESERVED_BITS15_10	
9:0	SERR	Defines End of Horizontal Serration with respect to a 27Mhz clock

0x04F00028 TV_SYNC_6

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x0006000C

This register defines the start and end of the serration pulses with respect to the number of HLines.

TV_SYNC_6

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	V_SERR_START	Defines Start of Serration Pulses in terms of HLines.
15:8	RESERVED_BITS15_8	
7:0	V_SERR_END	Defines Start of Serration Pulses in terms of HLines.

0x04F0002C TV_SYNC_7

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x000000012

This register defines the start and end of the equalization pulses with respect to the number of HLines. The pulse interval includes all equalization pulses with serration pulses embedded.

TV_SYNC_7

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	PULSE_START	Defines Start of Equalization in terms of HLines
15:8	RESERVED_BITS15_8	
7:0	PULSE_END	Defines End of Equalization in terms of HLines.

0x04F00030 TV_BURST_V1

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x0013020D

This register defines the vertical half line counts where burst is present in the first color field. The start and end points are inclusive.

TV_BURST_V1

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	START	Defines Start of Chroma Burst in terms of HLines
15:10	RESERVED_BITS15_10	
9:0	END	Defines End of Chroma Burst in terms of HLines.

0x04F00034 TV_BURST_V2

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x0014020C

This register defines the vertical half line counts where burst is present in the second color field. The start and end points are inclusive.

TV_BURST_V2

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	START	Defines Start of Chroma Burst in terms of HLines
15:10	RESERVED_BITS15_10	
9:0	END	Defines End of Chroma Burst in terms of HLines.

0x04F00038 TV_BURST_V3

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x0013020D

This register defines the vertical half line counts where burst is present in the third color field. The start and end points are inclusive.

TV_BURST_V3

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	START	Defines Start of Chroma Burst in terms of HLines
15:10	RESERVED_BITS15_10	
9:0	END	Defines End of Chroma Burst in terms of HLines.

0x04F0003C TV_BURST_V4

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x0014020C

This register defines the vertical half line counts where burst is present in the fourth color field. The start and end points are inclusive.

TV_BURST_V4

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	START	Defines Start of Chroma Burst in terms of HLines
15:10	RESERVED_BITS15_10	
9:0	END	Defines End of Chroma Burst in terms of HLines.

0x04F00040 TV_BURST_H

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00AE00F2

This register defines the horizontal start and stop points of color burst. These values need to be changed for each tv mode.

TV_BURST_H

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	START	Defines Start of Chroma Burst w.r.t. 27 MHz clock.
15:10	RESERVED_BITS15_10	
9:0	END	Defines End of Chroma Burst w.r.t. 27 MHz clock.

0x04F00044 TV_SOL_REQ_ODD

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00280208

This register defines the first and last lines with SOL_REQ_WR pulses in terms of full lines in the frame. This register refers specifically to the odd field.

TV_SOL_REQ_ODD

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	REQ_START	Defines first line with sol_wr_req w.r.t. full lines.
15:10	RESERVED_BITS15_10	
9:0	REQ_END	Defines last line with sol_wr_req w.r.t. full lines.

0x04F00048 TV_SOL_REQ_EVEN

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00290209

This register defines the first and last lines with SOL_REQ_WR pulses in terms of full lines in the frame. This register refers specifically to the even field.

TV_SOL_REQ_EVEN

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	REQ_START	Defines first line with sol_wr_req w.r.t. full lines.
15:10	RESERVED_BITS15_10	
9:0	REQ_END	Defines last line with sol_wr_req w.r.t. full lines.

0x04F0004C TV_DAC_TEST_DATA

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register allows a control of the DAC through the tv encoder's peripheral interface.This register is only for test purpose and should never be enabled during the normal mode

TV_DAC_TEST_DATA

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	CHROMA_SVID_DATA	Chroma Data to be output to Chroma DAC (Valid only when S-Video is enabled)
15:10	RESERVED_BITS15_10	

TV_DAC_TEST_DATA (cont.)

Bits	Name	Description
9:0	Y_OR_COMP_DATA	Luma or Composite Value to be output to DAC

0x04F00050 TV_TESTBUS_MUX

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register defines output sent to the debug port.

TV_TESTBUS_MUX

Bits	Name	Description
31:10	RESERVED_BITS31_10	
9:0	SEL	TESTBUS MUX select signal

0x04F00054 TV_TEST_MODE

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register selects whether the testbus signals goes out of TV Encoder block.

TV_TEST_MODE

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1:0	TEST_MODE	TEST MODE select signal 0x0: Disable TV Encoder Test Bus 0x1: Enable TV Encoder Test Bus and MISR calculation 0x2: Enable TV Encoder Test_1 0x3: Enable TV Encoder Test_2

0x04F00058 TV_TEST_MISR_RESET

Type: Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register resets the registers within the MISR engine.

TV_TEST_MISR_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	MISR_RESET	MISR engine can only be reset by writing this bit from the SW. The power-up reset cannot reset the MISR engine. Hence, it is required that SW resets the MISR engine before enabling the test MISR.

0x04F0005C TV_TEST_EXPORT_MISR

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register drives the MISR signature onto the testbus.

TV_TEST_EXPORT_MISR

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	EXPORT_MISR	Drives the signature onto the testbus. When the test_mode is not meant for MISR calculation, SW should not attempt to drive MISR signature with this command set.

0x04F00060 TV_TEST_MISR_CURR_VAL

Type: Read
Clock: CC_TV_ENC_CLK
Reset State: Unknown

This register drives the MISR signature onto the testbus.

TV_TEST_MISR_CURR_VAL

Bits	Name	Description
31:0	MISR_CURR_VAL	Current MISR signature value. This is read directly off this register. Another way is to export this value onto the testbus. Software needs to apply a MISR reset before reading this value; otherwise, the initial value is unknown.

0x04F00064 TV_TEST_SOF_CFG

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register contains programmable SOF count and one bit for force MISR test bus enable.

TV_TEST_SOF_CFG

Bits	Name	Description
31	FORCE_TESTBUS_EN	This bit allows software to allow the test MISR signature on all the time. This enable bit takes precedence over the enable generated by the SOF programmable counter hardware. Needless to say, force_testbus_en will only be useful when the test MISR is in the correct test mode.
30:3	RESERVED_BITS30_3	
2:0	TEST_SOF_PROG_CNT	When the actual SOF counts goes beyond this threshold, hardware will shut the test MISR signature registration off until software applies a test MISR reset or a regular reset via the clock block.

0x04F00068 TV_ADV_BURST_H

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register defines the horizontal start points of a color burst when advanced burst start is enabled (colorstripe lines only). These values need to be changed for each tv mode.

TV_ADV_BURST_H

Bits	Name	Description
31:10	RESERVED_BITS31_10	
9:0	START	Defines Advanced Start of Chroma Burst w.r.t. 27 MHz clock.

0x04F0006C TV_HW_VERSION

Type: Read Only
Clock: CC_TV_ENC_CLK
Reset State: 0x0201030C

The TV_HW_VERSION register contains the major and minor versions and release number of the TV_ENC core.

TV_HW_VERSION

Bits	Name	Description
31:24	MAJOR_VERSION	TV_ENC core major version
23:16	MINOR_VERSION	TV_ENC core minor version
15:8	RELEASE_PHASE	TV_ENC core release phase
7:0	REVISION	TV_ENC core revision number

14.13.1 TV Encoder Macrovision Registers

0x04F00070 TV_ENC_MV_CTL_REG0

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000004

Copy Protection process control register (On/Off/Mode byte)

TV_ENC_MV_CTL_REG0

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5	N0_5	VBI Pulse On/Off 0x0: VBI Pulses Off 0x1: VBI Pulses On
4	N0_4	End of Field Back Porch Pulses On/Off 0x0: End of Field Back Porch Pulses Off 0x1: End of Field Back Porch Pulses On
3	N0_3	This register turns off/on the Macrovision Colorstripe Process 0x0: Colorstripe process off 0x1: Colorstripe process on
2	N0_2	AGC pulse normal (Amplitude cycling) static mode select (Cycling = Default = 1)
1	N0_1	Sync amplitude reduction outside VBI 0x0: Sync Amplitude reduction outside VBI is Off 0x1: Sync Amplitude reduction outside VBI is On
0	N0_0	Sync amplitude reduction inside VBI 0x0: Sync Amplitude reduction inside VBI is Off 0x1: Sync Amplitude reduction inside VBI is On

0x04F00074 TV_ENC_MV_REG1

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

For a given field this register specifies the first line number with the modified burst in the first stripe. It also defines the spacing between the first line with modified burst in first stripe and first line with modified burst in second stripe.

TV_ENC_MV_REG1

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:24	N4	Spacing between first line with modified burst in first stripe and first line with modified burst in second stripe; Field2/Odd Field
23:22	RESERVED_BITS23_22	
21:16	N3	First line with modified burst in first stripe; Field 2/Odd field
15:14	RESERVED_BITS15_14	
13:8	N2	Spacing between first line with modified burst in first stripe and first line with modified burst in second stripe; Field1/Even Field
7:6	RESERVED_BITS7_6	
5:0	N1	First line with modified burst in first stripe; Field 1/Even field

0x04F00078 TV_ENC_MV_REG2

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register defines the colorstripe spacing, after second strip. It also defines the number of colorstripes per field and Number of lines per colorstripe

TV_ENC_MV_REG2

Bits	Name	Description
31:18	RESERVED_BITS31_18	
17:16	N7	Number of lines per colorstripe
15:11	RESERVED_BITS15_11	
10:8	N6	Number of colorstripes per field
7:3	RESERVED_BITS7_3	
2:0	N5	Colorstripe spacing, after second stripe

0x04F0007C TV_ENC_MV_REG3

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register defines the Pseudo-sync pulse duration, First pseudo-sync pulse location and Pseudo-sync pulse spacing.

TV_ENC_MV_REG3

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:16	N10	Pseudo-sync pulse spacing
15:14	RESERVED_BITS15_14	
13:8	N9	First pseudo-sync pulse location
7:6	RESERVED_BITS7_6	
5:0	N8	Pseudo-sync pulse duration

0x04F00080 TV_ENC_MV_REG4

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register specifies the line numbers for which the Pseudo-sync/AGC pulses will be included (Line Formats A +B)

TV_ENC_MV_REG4

Bits	Name	Description
31:15	RESERVED_BITS31_15	
14:0	N11	Line Number selection for PS/AGC pulses (Line Formats A + B)

0x04F00084 TV_ENC_MV_REG5

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register specifies the line numbers for which the Pseudo-sync/AGC pulses will be included has Line Format A or Line Format B

TV_ENC_MV_REG5

Bits	Name	Description
31:15	RESERVED_BITS31_15	
14:0	N12	Line Number selection for PS/AGC pulses (Line FormatB)

0x04F00088 TV_ENC_MV_REG6

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register allows us to control the individual Pseudo-sync/AGC pulse On/Off for line format A

TV_ENC_MV_REG6

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	N13_LOC8	PSP and AGC On/Off in 8th location for format A 0x0: PSP and AGC is Off in 8th location 0x1: PSP and AGC is On in 8th location
6	N13_LOC7	PSP and AGC On/Off in 7th location for format A 0x0: PSP and AGC is Off in 7th location 0x1: PSP and AGC is On in 7th location
5	N13_LOC6	PSP and AGC On/Off in 6th location for format A 0x0: PSP and AGC is Off in 6th location 0x1: PSP and AGC is On in 6th location
4	N13_LOC5	PSP and AGC On/Off in 5th location for format A 0x0: PSP and AGC is Off in 5th location 0x1: PSP and AGC is On in 5th location
3	N13_LOC4	PSP and AGC On/Off in 4th location for format A 0x0: PSP and AGC is Off in 4th location 0x1: PSP and AGC is On in 4th location
2	N13_LOC3	PSP and AGC On/Off in 3rd location for format A 0x0: PSP and AGC is Off in 3rd location 0x1: PSP and AGC is On in 3rd location
1	N13_LOC2	PSP and AGC On/Off in 2st location for format A 0x0: PSP and AGC is Off in 2nd location 0x1: PSP and AGC is On in 2nd location
0	N13_LOC1	PSP and AGC On/Off in 1st location for format A 0x0: PSP and AGC is Off in 1st location 0x1: PSP and AGC is On in 1st location

0x04F0008C TV_ENC_MV_REG7

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register allows us to control the individual Pseudo-sync/AGC pulse On/Off for line format B

TV_ENC_MV_REG7

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	N14_LOC8	PSP and AGC On/Off in 8th location for format B 0x0: PSP and AGC is Off in 8th location 0x1: PSP and AGC is On in 8th location
6	N14_LOC7	PSP and AGC On/Off in 7th location for format B 0x0: PSP and AGC is Off in 7th location 0x1: PSP and AGC is On in 7th location
5	N14_LOC6	PSP and AGC On/Off in 6th location for format B 0x0: PSP and AGC is Off in 6th location 0x1: PSP and AGC is On in 6th location
4	N14_LOC5	PSP and AGC On/Off in 5th location for format B 0x0: PSP and AGC is Off in 5th location 0x1: PSP and AGC is On in 5th location
3	N14_LOC4	PSP and AGC On/Off in 4th location for format B 0x0: PSP and AGC is Off in 4th location 0x1: PSP and AGC is On in 4th location
2	N14_LOC3	PSP and AGC On/Off in 3rd location for format B 0x0: PSP and AGC is Off in 3rd location 0x1: PSP and AGC is On in 3rd location
1	N14_LOC2	PSP and AGC On/Off in 2st location for format B 0x0: PSP and AGC is Off in 2nd location 0x1: PSP and AGC is On in 2nd location
0	N14_LOC1	PSP and AGC On/Off in 1st location for format B 0x0: PSP and AGC is Off in 1st location 0x1: PSP and AGC is On in 1st location

0x04F00090 TV_ENC_MV_REG8

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register configures the number of end of field Back Porch pulses prior to Vsync and following the Vsync pulse

TV_ENC_MV_REG8

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:4	N15_PRIOR	Adds 0 to 15 back porch pulses according to value of this parameter. The first pulse is inserted in the last line prior to the V-sync pulse, with additional pulses being inserted as required until 15 lines prior to the Vsync pulse when this parameter has value of 0xF
3:0	N15_AFTER	Adds 0 to 15 back porch pulses according to value of this parameter. The first pulse is inserted in the first line following the V-sync pulse, with additional pulses being inserted as required until 15 lines following the Vsync pulse when this parameter has value of 0xF

0x04F00094 TV_ENC_MV_REG9

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register controls whether the Burst Advanced start is On/Off (applicable to colorstripe lines only)

TV_ENC_MV_REG9

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	N16	Burst Advanced Start On/Off (colorstripe lines only) 0x0: Burst Advanced Start is Off 0x1: Burst Advanced Start is On

0x04F00098 TV_ENC_MV_REG10

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register specifies the duration of each zone in the colorburst (applicable only when colorstripe process in On)

TV_ENC_MV_REG10

Bits	Name	Description
31:20	RESERVED_BITS31_20	
19:16	N19	2nd phase switch point to end of burst duration (Zone 3)
15:12	RESERVED_BITS15_12	
11:8	N18	1st to 2nd phase point duration (Zone 2)
7:4	RESERVED_BITS7_4	
3:0	N17	Start of Burst to 1st Phase Switch Point duration (Zone 1)

0x04F0009C TV_ENC_MV_REG11

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register is used for selecting the phase of the sub-carrier within a zone of a color burst. The sub-carries phase switch points create up to 3 zones within the burst. Each zone may incorporate sub-carrier with either normal or modified phase sub-carrier. Each zone may be of normal (unmodified) phase or modified phase as set by this register. A phase discontinuity will only exist between adjacent zones of differing sub-carrier phase. (colorstripe lines only)

TV_ENC_MV_REG11

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	N20_ZONE1	Select the Sub-carrier Phase for Zone 1 0x0: Normal Phase for Zone1 0x1: Modified Phase for Zone1
1	N20_ZONE2	Select the Sub-carrier Phase for Zone 2 0x0: Normal Phase for Zone2 0x1: Modified Phase for Zone2
0	N20_ZONE3	Select the Sub-carrier Phase for Zone 3 0x0: Normal Phase for Zone3 0x1: Modified Phase for Zone3

0x04F000A0 TV_ENC_MV_REG12

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register is used for specifying the modified phase characteristics. For both NTSC and PAL the phase of the sub-carrier may be modified by 180 degrees. In the case of PAL, the phase may also be modified by +90 or -90 degrees compared with the phase which would otherwise be present on that line. Two control bits are used for each of the 5 possible lines which can comprise a colorstripe (10 bits total). (colorstripe lines only)

TV_ENC_MV_REG12

Bits	Name	Description
31:10	RESERVED_BITS31_10	
9:8	N21_LINE1	Colorstripe 1st line phase: 0x0: Normal sub-carrier Phase (Valid for both NTSC and PAL) 0x1: U-axis component inverted in PAL (N/A for NTSC) 0x2: V-axis component inverted in PAL (N/A for NTSC) 0x3: 180 degrees phase inversion (Valid for both NTSC and PAL)
7:6	N21_LINE2	Colorstripe 2nd line phase: 0x0: Normal sub-carrier Phase (Valid for both NTSC and PAL) 0x1: U-axis component inverted in PAL (N/A for NTSC) 0x2: V-axis component inverted in PAL (N/A for NTSC) 0x3: 180 degrees phase inversion (Valid for both NTSC and PAL)
5:4	N21_LINE3	Colorstripe 3rd line phase: 0x0: Normal sub-carrier Phase (Valid for both NTSC and PAL) 0x1: U-axis component inverted in PAL (N/A for NTSC) 0x2: V-axis component inverted in PAL (N/A for NTSC) 0x3: 180 degrees phase inversion (Valid for both NTSC and PAL)
3:2	N21_LINE4	Colorstripe 4th line phase: 0x0: Normal sub-carrier Phase (Valid for both NTSC and PAL) 0x1: U-axis component inverted in PAL (N/A for NTSC) 0x2: V-axis component inverted in PAL (N/A for NTSC) 0x3: 180 degrees phase inversion (Valid for both NTSC and PAL)
1:0	N21_LINE5	Colorstripe 5th line phase: 0x0: Normal sub-carrier Phase (Valid for both NTSC and PAL) 0x1: U-axis component inverted in PAL (N/A for NTSC) 0x2: V-axis component inverted in PAL (N/A for NTSC) 0x3: 180 degrees phase inversion (Valid for both NTSC and PAL)

0x04F000A4 TV_ENC_TEST_CTL_REG13

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000002

This is a control register used for test control purpose only.

TV_ENC_TEST_CTL_REG13

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	MV_PULSE_RAMP_MODE_EN	This bit enables the ramp on the PS, AGC and BP pulse edges. 0x0: disable the ramp mode (default) 0x1: enable the ramp mode
1	DELAY_PHASE_CHANGE_EXT_NTSC	This register bit enables phase change at near zero crossing for NTSC. 0x0: disable enhanced burst_phase_change feature 0x1: enable enhanced burst_phase_change feature (default)
0	DELAY_PHASE_CHANGE_EXT_PAL	This register bit enables phase change at near zero crossing for PAL. 0x0: disable enhanced burst_phase_change feature (default) 0x1: enable enhanced burst_phase_change feature

0x04F000A8 TV_ENC_TEST_REG14

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000030

With this register one can select the different values to enable or disable the burst phase switch point.

TV_ENC_TEST_REG14

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	BURST_PHASE_CHANGE_CNTR_NTSC	Counter to delay change of phase of the color burst in NTSC mode
3	RESERVED_BIT3	
2:0	BURST_PHASE_CHANGE_CNTR_PAL	Counter to delay change of phase of the color burst in NTSC mode

14.13.2 TV Encoder DAC Interface Control Registers

0x04F00100 TV_DAC_INTF_CTL_REG

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

This register contains the various control modes for TV DAC

TV_DAC_INTF_CTL_REG

Bits	Name	Description
31:10	RESERVED_BITS31_10	
9	LOAD_DETECT_EN_PWM_BYPASS	Bypass Pulse Width Modulation (PWM) Load Detect circuit. 0x0: Don't bypass PWM load detect circuit 0x1: Bypass PWM load detect circuit
8	LOAD_DET_ENABLE	Enable/disable load detection, independent of video activity 0x0: Disable load detection 0x1: Enable Load detection
7:6	RESERVED_BITS7_6	
5	DAC_HI	Video 1,2 DAC current select 0x0: 1 mA 0x1: 2 mA
4	REF_IN_SEL	Selects external reference 0x0: don't select external reference 0x1: select external reference
3	R_SET_SEL	Select external V-to-I resistor 0x0: don't select external V-to-I connector 0x1: select external V-toI connector
2	ACTIVE_ROUT_DISABLE	Also known as BUFFER_BYPASS. It enables/disables video1,2 active termination circuitry. In disabled mode, it bypasses the integrated buffer and load detection is not available. The output is voltage mode 0x0: Enable active termination circuitry 0x1: Disable active termination circuitry
1	FILTER_BYPASS	Bypass video 1,2 internal reconstruction filters 0x0: Disable bypass of internal reconstruction filter 0x1: Enable bypass of internal reconstruction filter
0	LEGACY_SEL	Connect single-ended video 1/2 DAC out to video 1/2 out pin 0x0: Do not connect single ended video DAC out to video_out pin 0x1: Connect single ended video DAC out to video_out pin

0x04F00104 TV_DAC_VIDEO_GAIN

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000F0F

This register contains the fine gain adjustment bits for Video DAC1 and DAC2

TV_DAC_VIDEO_GAIN

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12:8	VIDEO2_GAIN	Fine gain adjust bits for Video2
7:5	RESERVED_BITS7_5	
4:0	VIDEO1_GAIN	Fine gain adjust bits for Video1

0x04F00108 TV_DAC_VIDEO3_GAIN

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x0000000F

This register contains the fine gain adjustment bits for Video DAC3

TV_DAC_VIDEO3_GAIN

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4:0	VIDEO3_GAIN	Fine gain adjust bits for Video3

0x04F0010C TV_DAC_INTF_CTL_REG2

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000077

This register contains the various control modes for DSUB DAC

TV_DAC_INTF_CTL_REG2

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10	FILTER_MODE	Enable for filter mode 0x0: set to 0 when in Svideo or composite mode 0x1: set to 1 when in DSUB mode
9	DRIVER_MODE	Enable for driver mode 0x0: set to 0 when in Svideo or composite mode 0x1: set to 1 when in DSUB mode

TV_DAC_INTF_CTL_REG2 (cont.)

Bits	Name	Description
8	SYNC_ON_G_EN	Enable Sync on Green 0x0: disable Sync on Green 0x1: enable Sync on Green
7	RESERVED_BITS7	
6:4	R_SEL	Selects DAC internal load
3	RESERVED_BITS3	
2:0	I_SEL	Selects DAC current. 000 means 1 mA 111 means 15 mA

0x04F00110 TV_DAC_INTF_CTL_REG3

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

The DSUB triple DAC is a generic DAC which can be used for Composite, S-Video or DSUB (mini VGA) mode. This register should be used only when the DSUB triple DAC is in S_video or Composite mode.

In composite mode by default the composite signal is sent over video1 output of the DSUB DAC. Use this register to send the composite signal over the video3 output of the DSUB DAC instead of video1.

In SVideo mode by default the luma is sent over Video1 and Chroma over Video2 output of the DSUB DAC.Use this register to send the luma over Video3 output of the DSUB DAC. The Chroma remains on the Video2 output of the DSUB DAC.

TV_DAC_INTF_CTL_REG3

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	DAC3_EN	0x0: Disable Video3 and enable Video1 (default) 0x1: Enable Video3 and disable Video1

0x04F00114 TV_DAC_INTF_CTL_REG4

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x0000000

This register contains miscellaneous control bits for the DSUB triple DAC

TV_DAC_INTF_CTL_REG4

Bits	Name	Description
31:12	RESERVED_BITS31_12	
11:0	DSUB_CONTROL_BITS	Misc DAC control bits

14.13.3 TV Encoder Interrupt Registers

0x04F00200 TV_INTR_ENABLE

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

The TV_INTR_ENABLE register is used to enable the TV_ENC interrupts

TV_INTR_ENABLE

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:0	INTR_ENABLE	Setting (1) a specific bit will enable the respective interrupt source within the TV to send a level interrupt out of the TV_ENC. Clearing (0) that bit will disable it from generating the TV_ENC interrupt. Bit0: Load present on Video1 Bit1: Load present on Video2 Bit 2 : Load removed on Video1 Bit 3 : Load removed on Video2 Bit 4 : Load present on Video3 Bit 5 : Load removed on Video3

0x04F00204 TV_INTR_STATUS

Type: Read
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

The TV_INTR_STATUS register is the TV_ENC interrupt status register

TV_INTR_STATUS

Bits	Name	Description
31:6	RESERVED_BITS31_6	

TV_INTR_STATUS (cont.)

Bits	Name	Description
5:0	INTR_STATUS	When a TV_ENC interrupt occurs, then reading this register will indicate what caused the interrupt since that each bit indicates the source of the interrupt that had happened. If multiple interrupt sources had happened, then multiple bits of this register will be set Bit0: Load present on Video1 Bit1: Load present on Video2 Bit 2 : Load removed on Video1 Bit 3 : Load removed on Video2 Bit 4 : Load present on Video3 Bit 5 : Load removed on Video3

0x04F00208 TV_INTR_CLEAR

Type: Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000000

The TV_INTR_CLEAR register is used to clear the TV_ENC interrupts

TV_INTR_CLEAR

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:0	INTR_CLEAR	To clear the interrupt, make sure the interrupt has occurred, and then clear the corresponding bit by setting it to 1. This is a write only register. So a read from this register would be all 0's. Bit0: Load present on Video1 Bit1: Load present on Video2 Bit 2 : Load removed on Video1 Bit 3 : Load removed on Video2 Bit 4 : Load present on Video3 Bit 5 : Load removed on Video3

14.13.4 TV Encoder Clock Gating Register

0x04F00250 TV_CGC_ENABLE

Type: Read/Write
Clock: CC_TV_ENC_CLK
Reset State: 0x00000001

The TV_CGC_ENABLE register is used to enable the automatic functional clock gating mechanism inside the TV_ENC core, where the clocks are gated depending on the operation

mode. For maximum power saving leave the register bit set to 1 during initialization. To force the clock to be ON regardless of the operation scenario, set the associated enable bit to 0

TV_CGC_ENABLE

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	TV_CGC_EN	Enables auto functional gating 0x0: disable auto functional gating 0x1: enable auto functional gating (default)

14.14 JPEG Registers (0x05000000 JPEGD_BASE)

This section contains the JPEG registers.

14.14.1 JPEG decoder registers

0x05000000 JPEG_CTRL_COMMON

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG common control register.

JPEG_CTRL_COMMON

Bits	Name	Description
31:5	UNUSED	Unused.
4	JPEG_CTRL_COMMON_ZZ_OVERRIDE_EN	Normally quantization tables are accessed in the JPEG zig zag pattern. This override switch allows the tables to be accessed in raster order, that is, from left to right in a rows from the top to the bottom. 0x0: Disable zig zag override 0x1: Enable zig zag override
3:0	JPEG_CTRL_COMMON_MODE	Controls the current processing mode of the JPEG block. One modes is currently defined. The decode mode (0x0) is the mode in which the JPEG block performs decodes of baseline JPEG scans. 0x0: Decode mode 0x1: Encode mode 0x2: Reserved_1 0x3: Reserved_2 0x4: Reserved_3 0x5: Reserved_4 0x6: Reserved_5 0x7: Reserved_6 0x8: Reserved_7 0x9: Reserved_8 0xA: Reserved_9 0xB: Reserved_10 0xC: Reserved_11 0xD: Reserved_12 0xE: Reserved_13 0xF: Reserved_14

0x05000008 JPEG_CTRL_ENCODE

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG encode control register.

JPEG_CTRL_ENCODE

Bits	Name	Description
31:5	UNUSED_1	Unused.
4	JPEG_CTRL_ENCODE_EOI_MARKER_EN	An option for adding EOI marker at the end of SCAN. 0x0: Stop after JPEG scan completes 0x1: Suffix JPEG scan with EOI marker
3:0	UNUSED_2	Unused.

0x05000010 JPEG_STATUS

Type: Read
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG status register.

JPEG_STATUS

Bits	Name	Description
31:14	UNUSED_1	Unused.
13	JPEG_STATUS_REGISTER_TIMEOUT	This field is set to 1 when JPEG register interface is hanged or overrun JPEG_REGISTER_TIMEOUT setting value. 0x0: No JPEG register interface time-out 0x1: JPEG register interface time-out
12	JPEG_STATUS_DHDQ_EOI	This field is set to 1 when the end-of-image marker is encountered during a decode. 0x0: EOI marker not yet encountered 0x1: EOI marker encountered
11	JPEG_STATUS_DHDQ_ERR_UNESCAPED_FF	This field is set to 1 if during a decode a 0xff sequence is encountered which is not part of a marker and not escaped with 0x00. 0x0: No un-escaped 0xFF in stream 0x1: Encountered 0xFF in stream which was not followed by 0x00

JPEG_STATUS (cont.)

Bits	Name	Description
10	JPEG_STATUS_DHDQ_ERR_INV_HUFFCODE	This field is set to 1 if during a decode a series of bits is encountered which does not conform to a valid Huffman decode value. 0x0: No Huffman error 0x1: Encountered invalid Huffman code in JPEG scan
9	JPEG_STATUS_DHDQ_ERR_INV_MARKER	This field is set to 1 if during a decode a restart marker is expected, and the marker decoded does not look like a restart marker. 0x0: No marker error 0x1: Encountered unknown marker in JPEG scan
8	JPEG_STATUS_DHDQ_ERR_RSTRT_SEQ	This field is set to 1 if during a decode a restart marker is encountered which contains an incorrect count value 0x0: No restart marker sequence error 0x1: Encountered restart marker with incorrect sequence number
7	JPEG_STATUS_DHDQ_ERR_RSTRT_OVRFLW	This field is set to 1 if during a decode the JPEG scan data contains an unexpected RESTART marker. 0x0: No overflow error with restart markers 0x1: Restart marker encountered in unexpected position in scan
6	JPEG_STATUS_DHDQ_ERR_RSTRT_UNDFLW	This field is set to 1 if during a decode the JPEG scan data is missing an expect restart marker. 0x0: No underflow error with restart markers 0x1: Restart missing from expected position in scan
5	JPEG_STATUS_DHDQ_ERR_SCAN_OVRFLW	This field is set to 1 if during a decode the JPEG scan data contains too many bits. 0x0: No overflow in scan data 0x1: JPEG image data contains too many bits
4	JPEG_STATUS_DHDQ_ERR_SCAN_UNDFLW	This field is set to 1 if during a decode the JPEG scan data ends prematurely. 0x0: No underflow in scan data 0x1: JPEG image data ended early
3:0	UNUSED_2	Unused.

0x05000014 JPEG_SOF_REG_0

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG start-of-frame register 0.

JPEG_SOF_REG_0

Bits	Name	Description
31:8	UNUSED	Unused.

JPEG_SOF_REG_0 (cont.)

Bits	Name	Description
7:0	JPEG_SOF_REG_0_NF	This is the number of image components in current frame as defined in CCITT T.81 B.2.2. Currently, 1 or 3 components are supported. It is for decoding.

0x05000018 JPEG_SOF_REG_1

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG start-of-frame register 1.

JPEG_SOF_REG_1

Bits	Name	Description
31:24	UNUSED	Unused.
23:16	JPEG_SOF_REG_1_C	This is the component identifier as defined in CCITT T.81 B.2.2. It is for decoding or encoding.
15:12	JPEG_SOF_REG_1_H	This is the horizontal sampling factor as defined in CCITT T.81 B.2.2. It is for decoding and encoding.
11:8	JPEG_SOF_REG_1_V	This is the vertical sampling factor as defined in CCITT T.81 B.2.2. It is for decoding and encoding.
7:0	JPEG_SOF_REG_1_TQ	This is the destination specifier as defined in CCITT T.81 B.2.2. It is for decoding and encoding.

0x0500001C JPEG_SOF_REG_2

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG start-of-frame register 2.

JPEG_SOF_REG_2

Bits	Name	Description
31:16	JPEG_SOF_REG_2_Y	This is the image height as defined in CCITT T.81 B.2.2. It is for decoding.
15:0	JPEG_SOF_REG_2_X	This is the image width as defined in CCITT T.81 B.2.2. It is for decoding.

0x05000020 JPEG_SOS_REG_0

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG start-of-scan register 0.

JPEG_SOS_REG_0

Bits	Name	Description
31:24	JPEG_SOS_REG_0_NS	Number of components in scan as defined CCITT T.81 B.2.3. It is for encoding.
23:0	UNUSED	Unused.

0x05000024 JPEG_SOS_REG_1

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG start-of-scan register 1.

JPEG_SOS_REG_1

Bits	Name	Description
31:16	UNUSED	Unused.
15:8	JPEG_SOS_REG_1_CS	Component specifier as defined in CCITT T.81 B.2.3. It is for decoding and encoding.
7:4	JPEG_SOS_REG_1_TD	DC entropy coding destination specifier as defined in CCITT T.81 B.2.3. It is for decoding and encoding.
3:0	JPEG_SOS_REG_1_TA	AC entropy coding destination specifier as defined in CCITT T.81 B.2.3. It is for decoding and encoding.

0x05000030 JPEG_QT_IDX

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG quantize table index register. The operation of this register is closely connected to the JPEG_DWT register.

JPEG_QT_IDX

Bits	Name	Description
31:16	UNUSED	Unused.
15:8	JPEG_QT_IDX_TABLE_1	This field works similarly to JPEG_QT_IDX_TABLE_0. Write 0xff to this field to select quantize 1 for subsequent reads from JPEG_DQT. It is for decoding and encoding.
7:0	JPEG_QT_IDX_TABLE_0	This field is used to define an index into quantization table 0 for reading or writing, and is also used to select table 0 for reading. When the value 0xff is written to this field, the index is reset to 0, and subsequent reads from the JPEG_DQT table will come from quantize table 0. When reads take place from JPEG_DQT, this index must be incremented with a separate write operation. When writes to quantize table 0 take place via the JPEG_DQT register, this value is auto incremented. The interpretation of this value is affected by the JPEG_CTRL_COMMON_ZZ_OVERRIDE_EN switch. It is for decoding and encoding.

0x05000034 JPEG_DQT

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG define-quantize-table register. This register is used to read and write values to quantize table, and its operation is closely connected to that of the JPEG_QT_IDX register. When reads take place from this register, the quantize table is selected via a write of 0xff to the corresponding field in JPEG_QT_IDX. For writes, the selected table is specified in the JPEG_DQT_Tq field.

NOTE Reads from this register are only valid if the JPEG block is otherwise idle; during encoding or decoding operations, internal pointers take priority.

JPEG_DQT

Bits	Name	Description
31:28	UNUSED_1	Unused.
27:24	JPEG_DQT_TQ	Quantize table destination identifier as defined by CCITT T.81 B.2.4.1. It is for decoding or encoding.
23:16	UNUSED_2	Unused.
15:0	JPEG_DQT_QK	Quantize table entry as defined by CCITT T.81 B.2.4.1. It is for decoding or encoding.

0x05000040 JPEG_DRI

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG define restart interval register.

JPEG_DRI

Bits	Name	Description
31:16	UNUSED	Unused.
15:0	JPEG_DRI_RI	This is the restart interval as defined by CCITT T.81 B.2.4.4. It is for decoding and encoding.

0x05000050 JPEG_DHT_REG_0

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG define Huffman table register 0.

JPEG_DHT_REG_0

Bits	Name	Description
31:8	UNUSED	Unused.
7:4	JPEG_DHT_REG_0_TH	Huffman table destination specified by CCITT T.81 B.2.4.2. It is for decoding.
3:0	JPEG_DHT_REG_0_TC	Table class as defined by CCITT T.81 B.2.4.2. It is for decoding. 0x0: DC 0x1: AC

0x05000054 JPEG_DHT_IDX

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG define Huffman table index.

JPEG_DHT_IDX

Bits	Name	Description
31:12	UNUSED	Unused.
11:8	JPEG_DHT_IDX_CCC_MAX	Index into the CCC and MAX memory of the Huffman decode table specified by the last write to JPEG_DHT_REG_0. These values are defined in the dHdQ block spec. It is for decoding.
7:0	JPEG_DHT_IDX_VIJ	Index into the VIJ memory of the Huffman decode table specified by the last write to JPEG_DHT_REG_0. The VIJ values are defined by CCITT T.81 B.2.4.2. It is for decoding.

0x05000058 JPEG_DHT_REG_1

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG define Huffman table register 1.

JPEG_DHT_REG_1

Bits	Name	Description
31:24	JPEG_DHT_REG_1_VIJ_0	This is the VIJ value for the Huffman table defined by the last write to JPEG_DHT_REG_0 and the index specified by JPEG_DHT_IDX_VIJ + 3. It is for decoding.
23:16	JPEG_DHT_REG_1_VIJ_1	This is the VIJ value for the Huffman table defined by the last write to JPEG_DHT_REG_0 and the index specified by JPEG_DHT_IDX_VIJ + 2. It is for decoding.
15:8	JPEG_DHT_REG_1_VIJ_2	This is the VIJ value for the Huffman table defined by the last write to JPEG_DHT_REG_0 and the index specified by JPEG_DHT_IDX_VIJ + 1. It is for decoding.
7:0	JPEG_DHT_REG_1_VIJ_3	This is the VIJ value for the Huffman table defined by the last write to JPEG_DHT_REG_0 and the index specified by JPEG_DHT_IDX_VIJ. It is for decoding.

0x0500005C JPEG_DHT_CCC_MAX

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG define Huffman table CCC and maximum.

JPEG_DHT_CCC_MAX

Bits	Name	Description
31:16	JPEG_DHT_CCC_MAX_MAX	The max code value register value as defined in the dHdQ specification for the Huffman table defined by the last write to JPEG_DHT_REG_0 and the index specified by JPEG_DHT_IDX_CCC_MAX. It is for decoding.
15:0	JPEG_DHT_CCC_MAX_CCC	The cumulative code register value as defined by the dHdQ specification for the Huffman table defined by the last write to JPEG_DHT_REG_0 and the index specified by JPEG_DHT_IDX_CCC_MAX. It is for decoding.
15:8	UNUSED	Unused.
7:0	JPEG_DHT_LI	Number of Huffman codes of length 1 to 16. Specifies the number of Huffman codes for each of the 16 possible lengthis allowed by JPEG specification. Li's are the elements of the list BITS. It is for decoding.

0x05000060 JPEG_DEC_SCALE

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG decode scaler control.

JPEG_DEC_SCALE

Bits	Name	Description
31:2	UNUSED	Unused.
1:0	JPEG_DEC_SCALE_RATIO	During JPEG decode, a limited in-line downscale function may be applied to 8x8 blocks as they are produced. The downscale ratio is defined 2 to the power specified in this field down to 1. In case of image with vertical YUV422 sampling factor, only support x1, x2 and x4. 0x0: x1 0x1: x2 0x2: x4 0x3: x8

0x05000064 JPEG_CONVERT

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG format conversion control.

JPEG_CONVERT

Bits	Name	Description
31:24	JPEG_CONVERT_MONO_CB_VALUE	This field sets the value of the cb color component for 4:2:0 gray scale encode format. 0x0: Set this field to the Cb value for monochrome images
23:16	JPEG_CONVERT_MONO_CR_VALUE	This field sets the value of the Cr color component for 4:2:0 monochrome encode format. 0x0: Set this field to the Cr value for monochrome images.
15:13	UNUSED_1	Unused.
12	JPEG_CONVERT_CLAMP_EN	This bit switches on clamping of the decoded pixel data to the range 16-255 to ensure color-key alpha works properly. 0x0: Pass through decoded data 0x1: Clamp all decoded values to [16-255]
11:10	UNUSED_2	Unused.
9	JPEG_CONVERT_CBCR_SWITCH	This field enables the switching of the chroma order from CbCr (default) to CrCb. 0x0: Chroma order - CbCr 0x1: Chroma order - CrCb
8	JPEG_CONVERT_MONOCHROME_EN	This field enables monochrome mode. In this mode all chroma data coming into the block is replaced by the single values stored in JPEG_CONVERT_MONO_CB_VALUE and JPEG_CONVERT_MONO_CR_VALUE. 0x0: Disabled 0x1: Enabled
7:6	JPEG_CONVERT_MEM_ORG	This field specifies the memory organization used by RTDMA (either as a data source or destination). The valid values depend on the format to some degree, for example there is no single-plane (packed) 4:2:0 mode. 0x0: Packed (single-plane) 0x1: nv12 (two-plane) 0x2: Three-plane 0x3: Reserved
5:4	JPEG_CONVERT_422_MCU_TYPE	This field indicates YUV422 sampling factor. 0x0: HY=2, HCb=1, HCr=1, VY=2, VCb=2, VCr=2 0x1: HY=2, HCb=1, HCr=1, VY=1, VCb=1, VCr=1 0x2: HY=1, HCb=1, HCr=1, VY=2, VCb=1, VCr=1
3:2	JPEG_CONVERT_OUTPUT_FORMAT	This field specifies the format of data leaving the convert block. 0x0: Luma only (1 plane) 0x1: 4:1:1 0x2: 4:2:0 0x3: 4:2:2

JPEG_CONVERT (cont.)

Bits	Name	Description
1:0	JPEG_CONVERT_INPUT_FORMAT	This field specifies the format of data entering the convert block. For encoding, this data either comes from the high-speed lower-video pipe or the RTDMA, and goes to the DCT block. The IDCT block is for decoding the source. The output is sent to the RTDMA. Note that 4:1:1 input data may only be input as a decode source and may only be converted to 8-block 4:2:2 organized as 4-wide by 1-high blocks. 0x0: Luma only (1 plane) 0x1: 4:1:1 0x2: 4:2:0 0x3: 4:2:2

0x05000070 JPEG_ENC_BYTE_CNT

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG encode byte counter.

JPEG_ENC_BYTE_CNT

Bits	Name	Description
31:0	JPEG_ENC_BYTE_CNT_TOT	This register indicates the total number of encoded bytes written out during the current encode. This value is reset when a new encode begins. This register may also be written to. Since any value written here will be cleared to zero when JPEG data is written, it can be used for debug purposes to ensure that encodes are proceeding normally.

0x05000080 JPEG_DEBUG

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x4a504547

JPEG debug register.

JPEG_DEBUG

Bits	Name	Description
31:0	JPEG_DEBUG	[Write operation] - 1st write operation: written data[4:0] goes to debug_bus_selection internally. Switch(debug_bus_selection) - 1:{31'd0,pixel_dct RTR} - 3:{31'd0,pixel_rtdma RTR} - 4:{31'd0,pixel_read RTR} - 7:{28'd0,decode RTR, decode RTS, encode RTR, encode RTS} - 19:{24'd0,unescape_ff_err, underflow_err, overflow_err,restart_marker_err, invalid_marker_err, invalid_huffman_err, restart_marker_underflow_err, restart_marker_overflow_err} - 23:current BYTE counter[31:0] or previous frame BYTE counter[31:0] - it will be determined 2nd write operation. - 2nd write operation: written data[3:0]==0 or 1 is selected current or previous BYTE counter. - 0: Previous frame BYTE counter - 1: Current BYTE counter if written data[3:0]==8, then it allows to receive data for DCT debug mode. - 3rd write operation: if 2nd write operation is selected DCT debug mode, the data is used to override data for input of DCT unit. written data[12]:DCT override enable. written data[11:0]:DCT override all of DCT input data. [Read operation] Each of debug information will be read back with proper selection information from 1st write operation.

0x05000084 JPEGD_SPARE

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Spare register.

JPEGD_SPARE

Bits	Name	Description
31:0	JPEGD_SPARE_00	Spare register.

0x05000088 JPEG_REGISTER_TIMEOUT

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x0000FFFF

JPEG register access time-out.

JPEG_REGISTER_TIMEOUT

Bits	Name	Description
31:16	UNUSED	Unused.
15:0	JPEG_TIMEOUT_VALUE	This field specifies the time out value of register interface.

0x05000258 JPEGD_STATUS_BUS_DATA

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEGD debug bus read back register.

JPEGD_STATUS_BUS_DATA

Bits	Name	Description
31:0	STATUS_BUS_DATA	Read back the debug bus output.

0x0500025C JPEGD_STATUS_BUS_CONFIG

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG debug signal selection.

JPEGD_STATUS_BUS_CONFIG

Bits	Name	Description
31:5	UNUSED	Unused.

JPEGD_STATUS_BUS_CONFIG (cont.)

Bits	Name	Description
4:0	STATUS_BUS_SEL	Debug bus output selection. 4 0x0: Not used_1 0x1: Not used_2 0x2: Debug bus check with 32'hAAAAAAAA 0x3: Debug bus check with 32'h55555555

0x05000260 RTDMA_JPEG_AXI_CONFIG

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000024

AXI master configuration register.

RTDMA_JPEG_AXI_CONFIG

Bits	Name	Description
31:12	UNUSED	Unused.
11	OUT_OF_ORDER_WR	Out-of-order in AXI write memory channel. Current version does not support out-of-order operation. 0x0: Disable 0x1: Enable
10	OUT_OF_ORDER_RD	Out-of-order in AXI read memory channels. Current version does not support out-of-order operation. 0x0: Disable 0x1: Enable
9:8	BOUND_LIMIT	Defines the boundary limitation of the address increment. The bursts must not cross 4-kB boundaries. 0x0: 1 k 0x1: 2 k 0x2: 4 k 0x3: No boundary
7:4	PACK_TIMEOUT	Defines the number of idle cycles to wait before incomplete burst is closed.
3:0	PACK_MAX_BLEN	Defines the maximum number of data transfers that occur within each burst. Valid value: 1 <= len <= 15

0x05000264 JPEGD_CLK_CONTROL

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000001F5

JPEGD_CLK_CONTROL

Bits	Name	Description
31:9	UNUSED	Unused.
8	RTDMA_ENCODE_CLKON	0x0: Dynamic HW Clock Gating Enabled 0x1: Always CLock on
7	RTDMA_IDCT_CLKON	0x0: Dynamic HW Clock Gating Enabled 0x1: Always CLock on
6	RTDMA_PIXEL_CLKON	0x0: Dynamic HW Clock Gating Enabled 0x1: Always CLock on
5	RTDMA_WCIF_CLKON	0x0: Dynamic HW Clock Gating Enabled 0x1: Always CLock on
4	AHB_CLKON	0x0: Disable 0x1: Enable
3	JPEG_CLKIDLE	0x0: Disable 0x1: Enable
2	JPEG_CLKON	0x0: Disable 0x1: Enable
1	AXI_CLKIDLE	0x0: Disable 0x1: Enable
0	AXI_CLKON	0x0: Disable 0x1: Enable

0x05000200 RTDMA_JPEG_WR_BUF_CONFIG

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Buffer configuration register.

This register is a non-shadowed register.

RTDMA_JPEG_WR_BUF_CONFIG

Bits	Name	Description
31:5	UNUSED	Unused.

RTDMA_JPEG_WR_BUF_CONFIG (cont.)

Bits	Name	Description
4:2	BUF_FORMAT	Defines the color format of the buffer. 0x0: YUV 4:2:2 0x1: YUV 4:2:0 0x2: Reserved_1 0x3: Reserved_2 0x4: Reserved_3 0x5: Reserved_4 0x6: Byte
1:0	NUM_OF_PLANES	Defines the number of planes per buffer (minus 1 - zero based). This value can be one, two or three planes, depends on format of the buffer.

0x05000204 RTDMA_JPEG_WR_OP

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Defines the primary operations for the normal data write buffer.

This is a shadowed register.

RTDMA_JPEG_WR_OP

Bits	Name	Description
31:5	UNUSED_1	Unused.
4	ALIGN	Set the video plane in the memory to be either left or right qualified-word alignment. 0x0: Left alignment 0x1: Right alignment
3:2	UNUSED_2	Unused.
1	FLIP	Enables vertical flip during transfer. Data is transferred from the video capture port to memory by writing the data in a rotated manor. 0x0: Disable 0x1: Enable
0	MIRROR	Enables horizontal mirroring during transfer. Data is transferred from the video capture port to memory by writing the data in a rotated manor. 0x0: Disable 0x1: Enable

0x05000208 RTDMA_JPEG_WR_BUF_Y_PNTR

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG buffer Y pointer register.

This register defines a pointer in memory to the buffer for the Y plane.

This is a shadowed register.

RTDMA_JPEG_WR_BUF_Y_PNTR

Bits	Name	Description
31:0	PNTR	Defines the value of the video capture port Y buffer pointer. Bits 0:2 of this field are preset in the factory to 0. It is not possible to change the setting of bits 0:2.

0x0500020C RTDMA_JPEG_WR_BUF_U_PNTR

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG buffer U pointer register.

This register defines a pointer in memory to the buffer for the U plane.

This is a shadowed register.

RTDMA_JPEG_WR_BUF_U_PNTR

Bits	Name	Description
31:0	PNTR	Defines the value of the video capture port U buffer pointer. Bits 0:2 of this field are preset in the factory to 0. It is not possible to change the setting of bits 0:2.

0x05000210 RTDMA_JPEG_WR_BUF_V_PNTR

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG buffer V pointer register.

This register defines a pointer in memory to the buffer for the V plane.

This is a shadowed register.

RTDMA_JPEG_WR_BUF_V_PNTR

Bits	Name	Description
31:0	PNTR	Defines the value of the video capture port V buffer pointer. Bits 0:2 of this field are preset in the factory to 0. It is not possible to change the setting of bits 0:2.

0x05000214 RTDMA_JPEG_WR_BUF_PITCH

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG buffer pitch register.

RTDMA_JPEG_BUF_PITCH register defines the pitch for buffer Y. The pitches for buffer U and V are calculated automatically.

RTDMA_JPEG_WR_BUF_PITCH

Bits	Name	Description
31:14	UNUSED	Unused.
13:0	PITCH	Defines the pitch value for the Y buffer. Bits 0:2 of this field are preset in the factory to 0. It is not possible to change the setting of bits 0:2.

0x05000218 RTDMA_JPEG_WR_PLANE_SIZE

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 00000000

JPEG plane size register.

RTDMA_JPEG_WR_PLANE_SIZE

Bits	Name	Description
31:29	UNUSED_1	Unused.
28:16	PLANE_VSIZE	Plane vertical size. Note: PLANE_VSIZE has to be a multiple of BLOCK_VSIZE at RTDMA_JPEG_WR_BLOCK_SIZE. (For Encode and decode)
15:13	UNUSED_2	Unused.

RTDMA_JPEG_WR_PLANE_SIZE (cont.)

Bits	Name	Description
12:0	PLANE_HSIZE	Plane horizontal size. Note: PLANE_HSIZE has to be a multiple of BLOCK_HSIZE at RTDMA_JPEG_WR_BLOCK_SIZE(For Encode and decode)

0x0500021C RTDMA_JPEG_WR_BLOCK_SIZE

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG block size register.

RTDMA_JPEG_WR_BLOCK_SIZE

Bits	Name	Description
31:12	UNUSED	Unused.
11:6	BLOCK_VSIZE	Block vertical size.
5:0	BLOCK_HSIZE	Block horizontal size.

0x05000220 RTDMA_JPEG_WR_BUFFER_SIZE

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG buffer size register.

This register defines the vertical size of the luminance (Y) plane. The size of the chroma (U and V) planes are calculated automatically.

RTDMA_JPEG_WR_BUFFER_SIZE

Bits	Name	Description
31:13	UNUSED	Unused.
12:0	BUFFER_VSIZE	Defines the vertical size (minus one) of the buffer. Current version supports long buffer mode only therefore, BUFFER_VSIZE has to be equal to PLANE_VSIZE.

0x05000224 RTDMA_JPEG_WR_STA_ACK

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG interrupt status/acknowledge register.

RTDMA_JPEG_WR_STA_ACK register is used to obtain status of interrupts and is used to acknowledge (clear) these interrupts when they are triggered. The interrupts can be enabled/disabled.

This is a non-shadowed register.

RTDMA_JPEG_WR_STA_ACK

Bits	Name	Description
31:4	UNUSED	Unused.
3	SW_RESET_ABORT_RDY_ACK	Acknowledgment of SW reset abort ready interrupt. 0x0: No effect 0x1: Reset status bit
3	SW_RESET_ABORT_RDY_STA	SW reset abort ready interrupt status. 0x0: No software reset abort ready interrupt occurred 0x1: Software reset abort ready interrupt occurred
2	ERR_STA	Error interrupt status. 0x0: No error interrupt occurred 0x1: Error interrupt occurred
2	ERR_ACK	Acknowledgment of error interrupt. 0x0: No effect 0x1: Reset status bit
1	EOF_ACK	Acknowledgment of EOF interrupt. 0x0: No effect 0x1: Reset status bit
1	EOF_STA	EOF interrupt status. 0x0: No EOF interrupt occurred 0x1: EOF interrupt occurred
0	SOF_ACK	Acknowledgment of SOF interrupt. 0x0: No effect 0x1: Reset status bit
0	SOF_STA	SOF interrupt status. 0x0: No SOF interrupt occurred 0x1: SOF interrupt occurred

0x05000228 RTDMA_JPEG_WR_INT_EN

Type: Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Interrupt enable register.

RTDMA_JPEG_WR_INT_EN

Bits	Name	Description
31:4	UNUSED	Unused.
3	SW_RESET_ABORT_RDY_EN	SW reset abort ready interrupt enable. 0x0: Interrupt disabled 0x1: Interrupt enabled
2	ERR_EN	Error interrupt enable. 0x0: Interrupt disabled 0x1: Interrupt enabled
1	EOF_EN	EOF interrupt enable. 0x0: Interrupt disabled 0x1: Interrupt enabled
0	SOF_EN	SOF interrupt enable. 0x0: Interrupt disabled 0x1: Interrupt enabled

0x05000100 RTDMA_JPEG_RD_BUF_CONFIG

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG read client buffer configuration register.

This is a non-shadowed register.

RTDMA_JPEG_RD_BUF_CONFIG

Bits	Name	Description
31:5	UNUSED	Unused.

RTDMA_JPEG_RD_BUF_CONFIG (cont.)

Bits	Name	Description
4:2	BUF_FORMAT	Defines the color format of the buffer. 0x0: YUV 4:2:2 0x1: YUV 4:2:0 0x2: Reserved_1 0x3: Reserved_2 0x4: Reserved_3 0x5: Reserved_4 0x6: Byte
1:0	NUM_OF_PLANES	Defines the number of planes per buffer (minus 1 - zero based). This value can be one, two or three planes.

0x05000104 RTDMA_JPEG_RD_BUF_MNGR_BUF_ID_FIFO

Type: Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

The entry of the BUF ID FIFO.

RTDMA_JPEG_RD_BUF_MNGR_BUF_ID_FIFO

Bits	Name	Description
31:5	UNUSED	Unused.
4	BUF_APPLY	Buffer apply attribute. To start JPEG encoding or decoding, this field must to be set.
3	BUF_EOF	Buffer end-of-field attribute. To start JPEG encoding or decoding, this field must to be set.
2	BUF_SOF	Buffer start-of-field attribute. To start JPEG encoding or decoding, this field must to be set.
1:0	RESERVED	Reserved.

0x0500010C RTDMA_JPEG_RD_BUF_Y_PNTR

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG buffer 0 Y pointer register.

This register defines a pointer in memory to the 0 Buffer for the Y plane.

This is a shadowed register.

RTDMA_JPEG_RD_BUF_Y_PNTR

Bits	Name	Description
31:0	PNTR	Defines the value of the video capture port Y buffer pointer with ID 0. Bits 0:2 of this field are preset in the factory to 0. It is not possible to change the setting of bits 0:2.

0x05000110 RTDMA_JPEG_RD_BUF_U_PNTR

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG buffer 0 U pointer register.

This register defines a pointer in memory to the 0 buffer for the U plane.

This is a shadowed register.

RTDMA_JPEG_RD_BUF_U_PNTR

Bits	Name	Description
31:0	PNTR	Defines the value of the video capture port U buffer pointer with ID 0. Bits 0:2 of this field are preset in the factory to 0. It is not possible to change the setting of bits 0:2.

0x05000114 RTDMA_JPEG_RD_BUF_V_PNTR

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG buffer 0 V pointer register.

This register defines a pointer in memory to the 0 buffer for the V plane. This register is a shadowed register.

This is a shadowed register.

RTDMA_JPEG_RD_BUF_V_PNTR

Bits	Name	Description
31:0	PNTR	Defines the value of the video capture port V buffer pointer with ID 0. Bits 0:2 of this field are preset in the factory to 0. It is not possible to change the setting of bits 0:2.

0x05000118 RTDMA_JPEG_RD_BUF_PITCH

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG read buffer pitch register.

RTDMA_VUP_BUF_PITCH register defines the pitch for buffer Y. The pitches for buffer U and V are calculated automatically.

RTDMA_JPEG_RD_BUF_PITCH

Bits	Name	Description
31:14	UNUSED	Unused.
13:0	PITCH	Defines the pitch value for the Y buffer. Bits 0:2 of this field are preset in the factory to 0. It is not possible to change the setting of bits 0:2.

0x0500011C RTDMA_JPEG_RD_PLANE_SIZE

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG buffer plane size.

RTDMA_VUP_PLANE_SIZE register defines the horizontal and vertical dimensions of the image plane that is being transferred.

This is a shadowed register.

RTDMA_JPEG_RD_PLANE_SIZE

Bits	Name	Description
31:29	UNUSED_1	Unused.

RTDMA_JPEG_RD_PLANE_SIZE (cont.)

Bits	Name	Description
28:16	PLANE_VSIZE	Defines the vertical size (minus one) of the image plane. Note: PLANE_VSIZE has to be a multiple of BLOCK_VSIZE at RTDMA_JPEG_RD_BLOCK_SIZE (decode only)
15:13	UNUSED_2	Unused.
12:0	PLANE_HSIZE	Defines the horizontal size (minus one) of the image plane. Note: PLANE_HSIZE has to be a multiple of BLOCK_HSIZE at RTDMA_JPEG_RD_BLOCK_SIZE (decode only).

0x05000120 RTDMA_JPEG_RD_BLOCK_SIZE

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x000003CF

JPEG block size register.

Each image plane is transferred to memory in rectangular blocks. This register defines the horizontal and vertical sizes of the luminance (Y) plane. The size of the chroma (U and V) planes are calculated automatically.

RTDMA_JPEG_RD_BLOCK_SIZE

Bits	Name	Description
31:12	UNUSED	Unused.
11:6	BLOCK_VSIZE	Defines the vertical size (minus one) of the block transferred to memory.
5:0	BLOCK_HSIZE	Defines the horizontal size (minus one) of the block transferred to memory.

0x05000124 RTDMA_JPEG_RD_BUFFER_SIZE

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG buffer size register.

This register defines the vertical size of the luminance (Y) plane. The size of the chroma (U and V) planes are calculated automatically.

RTDMA_JPEG_RD_BUFFER_SIZE

Bits	Name	Description
31:13	UNUSED	Unused.
12:0	BUFFER_VSIZE	Defines the vertical size (minus one) of the buffer. When the format of buffer is defined as 4:2:0 mode, the buffer vertical size should be an even number only. Current version just support long buffer mode only, therefore BUFFER_VSIZE has to be equal to PLANE_VSIZE.

0x05000128 RTDMA_JPEG_RD_STA_ACK

Type: Read/write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

JPEG interrupt status/acknowledge register.

RTDMA_JPEG_RD_STA_ACK register is used to obtain status of interrupts and is used to acknowledge (clear) these interrupts when they are triggered. The interrupts can be enabled/disabled.

This is a shadowed register.

RTDMA_JPEG_RD_STA_ACK

Bits	Name	Description
31:2	UNUSED	Unused.
1	EOF_STA	EOF interrupt status. 0x0: No EOF occurred 0x1: EOF occurred
1	EOF_ACK	EOF interrupt. 0x0: No effect 0x1: Reset status bit
0	SOF_ACK	SOF interrupt. 0x0: No effect 0x1: Reset status bit
0	SOF_STA	SOF interrupt status. 0x0: No SOF occurred 0x1: SOF occurred

0x0500012C RTDMA_JPEG_RD_INT_EN

Type: Write
Clock: AHB_SLAVE_HCLK
Reset State: 0x00000000

Interrupt enable register.

RTDMA_JPEG_RD_INT_EN

Bits	Name	Description
31:2	UNUSED	Unused.
1	EOF_EN	EOF interrupt enable. 0x0: Interrupt disabled 0x1: Interrupt enabled
0	SOF_EN	SOF interrupt enable. 0x0: Interrupt disabled 0x1: Interrupt enabled

14.15 MDP Registers (0x05100000 MDP_BASE)

This section describes the registers of Mobile Display Processor (MDP) version 4. All MDP4 registers are accessible by the ARM CPU through the Peripheral Bus AHB interface. For read accesses, the number of cycles before data is available is variable depending on the register being read.

The registers are grouped into distinct groups, according to their function or individual sub-block/pipe's local register accesses.

NOTE RGB3 and Video/Graphics3 Pipe are used for the border color feature in LM. These two pipes don't have fetch logic and just provide a solid background color for LM0/1. RGB3 is dedicated to LM0 and VG3 to LM1.

- Global general operation (0x00000 - 0x0004C)
- Interrupts (0x00050 - 0x0005C)
- EBI2 LCD parameters (0x00060 - 0x0007C)
- MDDI parameters (0x00090 - 0x0009C) : MDDI registers exist in HW but MDDP interface module has been removed in MDP4.2
- DSI 1 Command Mode parameters (0x000A0 - 0x000AC)
- DSI 2 Command Mode parameters (0x000B0 - 0x000BC)
- Internal memory chip select control register (0x000C0 - 0x000C4)
- Synchronization controls
- VSYNC_CLK registers (0x00100 - 0x001FC)
- MDP_CLK registers (0x00200 - 0x002FC)
- MGEN2MAXI control registers (0x00400 - 0x004FC)
- Overlay Processor settings (0x10000 - 0x8FFFC)
- Layer Mixer 0 (0x10004 - 0x17FFC)
- Layer Mixer 1 (0x18004 - 0x1FFFC)
- Video/Graphics1 Pipe (0x20000 - 0x2FFFC)
- Video/Graphics2 Pipe (0x30000 - 0x3FFFC)
- RGB1 Pipe (0x40000 - 0x4FFFC)
- RGB2 Pipe (0x50000 - 0x5FFFC)
- RGB3 Pipe (0x60000 - 0x6FFFC)
- Video/Graphics3 Pipe (0x70000 - 0x7FFFC)

- Layer Mixer 2 (0x80000 - 0x8FFFC)
- Primary Display Driver settings (0x90000 - 0x9FFFC)
- Secondary Display Driver settings (0xA0000 - 0xAFFFC)
- External Display Driver settings (0xB0000 - 0xBFFFC)
- DSI 2 Video Mode / LCDC Timing Generator (0xC0000 - 0xCFFFC)
- DTV Timing Generator (0xD0000 - 0xDFFFC)
- DSI 1 Video Mode Timing Generator (0xE0000 - 0xEFFFC)
- Test Bus and MISR Access (0xF0000 - 0xFFFFC)
- MDP_CLK (0xF0000 - 0xF00FC)
- HCLK (0xF0100 - 0xF01FC)
- DCLK [P2CLK](0xF0200 - 0xF02FC)
- TV_CLK (0xF0300 - 0xF03FC)
- DSI_PCLK [P1CLK](0xF0400 - 0xF04FC)
- AXI_CLK (0xF0500 - 0xF05FC)

14.15.1 Operation control registers

0x05100000 MDP_HW_VERSION

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0404_0306

The MDP_HW_VERSION register contains the major and minor versions and release number of the MDP core.

MDP_HW_VERSION

Bits	Name	Description
31:24	MAJOR_VERSION	MDP core major version.
23:16	MINOR_VERSION	MDP core minor version.
15:10	REVISION	MDP core revision number.
9:8	RELEASE_PHASE	MDP core release phase.
7:0	RELEASE	MDP core release number.

0x05100004 MDP_OVERLAYPROC0_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

This register is used to start Overlay Processor 0 (output port 0) fetching and processing Note, Overlay Processor 0 is associated strictly with DMA_P and its interfaces. If the Overlay Processor is connected directly to interface output, this start will also trigger interface write.

MDP_OVERLAYPROC0_START

Bits	Name	Description
31:0	OVERLAYPROC0_START	A write to register will start Overlay Processor 0 if the Overlay Processor's output port 0 is in On-Demand mode. Otherwise, the interface vsync automatically starts the processor and a write to this register has no effect, except for the initial start before the interface is enabled; this register could be used to make that initial starts.

0x05100008 MDP_OVERLAYPROC1_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

This register is used to start Overlay Processor 1 (output port 1) fetching and processing. Note, Overlay Processor 1 is associated strictly with DMA_S and DMA_E and its interfaces. If the Overlay Processor1 is connected directly to interface output, this start will also trigger interface write. Regarding selecting control of DMA_S and DMA_E, refer to MDP_OVERLAYPROC1_DMA_MUX_CON(0x18018)

MDP_OVERLAYPROC1_START

Bits	Name	Description
31:0	OVERLAYPROC1_START	A write to register will start Overlay Processor 1 if the Overlay Processor's output port 1 is in On-Demand mode. Otherwise, the interface vsync automatically starts the processor and a write to this register has no effect, except for the initial start before the interface is enabled; this register could be used to make that initial starts.

0x0510000C MDP_DMA_P_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_P_START register is used to start a primary DMA channel transfer.

MDP_DMA_P_START

Bits	Name	Description
31:0	DMA_P_START	A write to this register will start a DMA_P channel transfer which is only useful when output is connected to a smart panel and using Frame Buffer to refresh. If the output is LCDC, for example, DMA transfer is started automatically every vsync and a write to this register has no effect.

0x05100010 MDP_DMA_S_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_S_START register is used to start a secondary DMA channel transfer.

MDP_DMA_S_START

Bits	Name	Description
31:0	DMA_S_START	A write to this register will start a DMA_S channel transfer.

0x05100014 MDP_DMA_E_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_E_START register is used to start a external DMA channel transfer.

MDP_DMA_E_START

Bits	Name	Description
31:0	DMA_E_START	A write to this register will start a DMA_E channel transfer. This register was used to trigger the MDDI in legacy MDP4 but it doesn't do anything in MDP4.2 since MDP4.2 doesn't have smart panel connection in DMA_E. If the output is TV/DTV, for example, DMA transfer is started automatically every vsync and a write to this register has no effect.

0x05100018 MDP_DISPLAY_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DISPLAY_STATUS register is used to indicate the MDP display status.

MDP_DISPLAY_STATUS

Bits	Name	Description
31:12	RESERVED31_12	
11	OVERLAYPROC2_ACTIVE	Overlay Processor 2 is active.
10	DSI_VIDEO_ACTIVE	DSI1 Video interface is active
9	MDDI_E_ACTIVE	Reserved
8	MDDI_S_ACTIVE	DSI_S_CMD active when enabled
7	MDDI_P_ACTIVE	DSI_P_CMD active when enabled
6	DTV_ACTIVE	DTV/TV Enc interface is active.
5	LCDC_ACTIVE	DSI2 Video interface is active.
4	DMA_E_ACTIVE	DMA_E channel is active.
3	DMA_S_ACTIVE	DMA_S channel is active.
2	DMA_P_ACTIVE	DMA_P channel is active
1	OVERLAYPROC1_ACTIVE	Overlay Processor 1 is active.
0	OVERLAYPROC0_ACTIVE	Overlay Processor 0 is active.

0x0510001C MDP_SW_RESET

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_SW_RESET register is used to reset the individual pipes inside MDP.

MDP_SW_RESET

Bits	Name	Description
31:6	RESERVED31_6	
5	OVERLAYPROC2_RESET	Self cleared when reset sequence is completed. 0x1: Overlay2 reset

MDP_SW_RESET (cont.)

Bits	Name	Description
4	DMA_S_RESET	Self cleared when reset sequence is completed. 0x1: DMA_S reset
3	DMA_E_RESET	Self cleared when reset sequence is completed. 0x1: DMA_E reset
2	OVERLAYPROC1_RESET	Self cleared when reset sequence is completed. 0x1: Overlay1 reset
1	DMA_P_RESET	Self cleared when reset sequence is completed. 0x1: DMA_P reset
0	OVERLAYPROC0_RESET	Self cleared when reset sequence is completed. 0x1: Overlay0 reset

0x05100020 MDP_AXI_RD_ARB_CONFIG1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0xFFFF_FFFF

The MDP_AXI_ARB_CONFIG register is used to change how many consecutive grants are allowed by the arbiter to each of the masters. Setting to 0 means only allows 1 grant at a time to the same master, no consecutive grants. Maximum value of 0xf means 16 consecutive grants.

NOTE This register should be written only when MDP is completely IDLE.

MDP_AXI_RD_ARB_CONFIG1

Bits	Name	Description
31:28	MASTER7_WEIGHT	Number of consecutive grants allowed to Master 7 (P cursor).
27:24	MASTER6_WEIGHT	Number of consecutive grants allowed to Master 6 (DMA_P).
23:20	MASTER5_WEIGHT	Number of consecutive grants allowed to Master 5 (VG3).
19:16	MASTER4_WEIGHT	Number of consecutive grants allowed to Master 4 (RGB3).
15:12	MASTER3_WEIGHT	Number of consecutive grants allowed to Master 3 (RGB2).
11:8	MASTER2_WEIGHT	Number of consecutive grants allowed to Master 2 (RGB1).
7:4	MASTER1_WEIGHT	Number of consecutive grants allowed to Master 1 (VG2).
3:0	MASTER0_WEIGHT	Number of consecutive grants allowed to Master 0 (VG1).

0x05100024 MDP_AXI_RD_ARB_CONFIG2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0FFF

The MDP_AXI_ARB_CONFIG register is used to change how many consecutive grants are allowed by the arbiter to each of the masters. Setting to 0 means only allows 1 grant at a time to the same master, no consecutive grants. Maximum value of 0xf means 16 consecutive grants.

NOTE This register should be written only when MDP is completely IDLE.

MDP_AXI_RD_ARB_CONFIG2

Bits	Name	Description
31:12	RESERVED31_12	
11:8	MASTER10_WEIGHT	Number of consecutive grants allowed to Master 10 (E cursor).
7:4	MASTER9_WEIGHT	Number of consecutive grants allowed to Master 9 (DMA_E).
3:0	MASTER8_WEIGHT	Number of consecutive grants allowed to Master 8 (DMA_S).

0x05100028 MDP_AXI_RDMASTER_CONFIG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0001_0000

There are four AXI ports in MDP4 for Halcyon, two for each memory bus system (i.e., EBI0 and EBI1). The bus system is selected by HW automatically based on RD/WR buffer address. MDP_AXI_RDMASTER_CONFIG register selects the port (corresponding to the addressed bus system) that will be used by each MDP internal read master. This register can be changed only when the corresponding read master is idle or when MDP core is idle.

NOTE Each AXI port has a unique Master ID. SW can (a) assign different priorities for these ports in the bus arbiter (e.g) EBI0, Port0 -> High Priority; EBI0, Port1 -> Low Priority; EBI1, Port0 -> High Priority; EBI1, Port1 -> Low Priority and (b) assign MDP internal read masters to these ports based on priority requirements.

NOTE Master IDs for MDP4 AXI ports in Halcyon - 0x1C -> EBI0, Port0; 0x1D -> EBI0, Port1; 0x1E -> EBI1, Port0; 0x1F -> EBI1, Port1;

MDP_AXI_RDMASTER_CONFIG

Bits	Name	Description
31:22	RESERVED31_22	

MDP_AXI_RDMASTER_CONFIG (cont.)

Bits	Name	Description
21:20	MASTER10	DMA_E cursor 0x0: MDP0 Port 0x1: MDP1 Port 0x2: Reserved_1 0x3: Reserved_2
19:18	MASTER9	DMA_E fetch 0x0: MDP0 Port 0x1: MDP1 Port 0x2: Reserved_1 0x3: Reserved_2
17:16	MASTER8	DMA_S fetch 0x0: MDP0 Port 0x1: MDP1 Port 0x2: Reserved_1 0x3: Reserved_2
15:14	MASTER7	DMA_P cursor 0x0: MDP0 Port 0x1: MDP1 Port 0x2: Reserved_1 0x3: Reserved_2
13:12	MASTER6	DMA_P fetch 0x0: MDP0 Port 0x1: MDP1 Port 0x2: Reserved_1 0x3: Reserved_2
11:10	MASTER5	Video/Graphics 3 pipe (Reserved for future support) 0x0: MDP0 Port 0x1: MDP1 Port 0x2: Reserved_1 0x3: Reserved_2
9:8	MASTER4	RGB 3 pipe (Reserved for future support) 0x0: MDP0 Port 0x1: MDP1 Port 0x2: Reserved_1 0x3: Reserved_2
7:6	MASTER3	RGB 2 pipe 0x0: MDP0 Port 0x1: MDP1 Port 0x2: Reserved_1 0x3: Reserved_2

MDP_AXI_RDMASTER_CONFIG (cont.)

Bits	Name	Description
5:4	MASTER2	RGB 1 pipe 0x0: MDP0 Port 0x1: MDP1 Port 0x2: Reserved_1 0x3: Reserved_2
3:2	MASTER1	Video/Graphics 2 pipe 0x0: MDP0 Port 0x1: MDP1 Port 0x2: Reserved_1 0x3: Reserved_2
1:0	MASTER0	Video/Graphics 1 pipe 0x0: MDP0 Port 0x1: MDP1 Port 0x2: Reserved_1 0x3: Reserved_2

0x0510002C MDP_AXI_PORT_CONFIG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_AXI_PORT_CONFIG

Bits	Name	Description
31:4	RESERVED31_4	
3	PORT3_WR_PRIORITY	Gen2AXI bridge 3, rd_wr_priority: default 0 = read has priority.
2	PORT2_WR_PRIORITY	Gen2AXI bridge 2, rd_wr_priority: default 0 = read has priority.
1	PORT1_WR_PRIORITY	Gen2AXI bridge 1, rd_wr_priority: default 0 = read has priority.
0	PORT0_WR_PRIORITY	Gen2AXI bridge 0, rd_wr_priority: default 0 = read has priority.

0x05100030 MDP_AXI_WRMASTER_CONFIG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0004

There are four AXI ports in MDP4 for Halcyon, two for each memory bus system (i.e., EBI0 and EBI1). The bus system is selected by HW automatically based on RD/WR buffer address. MDP_AXI_RDMASTER_CONFIG register selects the port (corresponding to the addressed bus

system) that will be used by each MDP internal write master. This register can be changed only when the corresponding write master is idle or when MDP core is idle.

NOTE Each AXI port has a unique Master ID. SW can (a) assign different priorities for these ports in the bus arbiter (e.g) EBI0, Port0 -> High Priority; EBI0, Port1 -> Low Priority; EBI1, Port0 -> High Priority; EBI1, Port1 -> Low Priority and (b) assign MDP internal write masters to these ports based on priority requirements.

NOTE There is no arbitration between the write masters. Therefore both masters need to be programmed to be mutual exclusive (i.e.) a unique port has to be selected for each write master.

NOTE Master IDs for MDP4 AXI ports in Halcyon - 0x1C -> EBI0, Port0; 0x1D -> EBI0, Port1; 0x1E -> EBI1, Port0; 0x1F -> EBI1, Port1;

MDP_AXI_WRMASTER_CONFIG

Bits	Name	Description
31:4	RESERVED31_4	
3:2	MASTER1	Overlay Processor Out Port 1 0x0: MDP0 Port 0x1: MDP1 Port (default) 0x2: Reserved_1 0x3: Reserved_2
1:0	MASTER0	Overlay Processor Out Port 0 0x0: MDP0 Port (default) 0x1: MDP1 Port 0x2: Reserved_1 0x3: Reserved_2

0x05100034 MDP_MAX_WRBURST_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0044

This register is used to modify the max burst size for the bus write masters. There are only 2 write masters in the MDP.

NOTE This register should be written only when MDP is completely IDLE.

MDP_MAX_WRBURST_SIZE

Bits	Name	Description
31:7	RESERVED31_7	
6:4	MASTER1	Maximum burst beat size for Overlay Processor Out Port 1. Possible values: 0x4: 16 (default) 0x2: 8 0x1: 4
3	RESERVED3	
2:0	MASTER0	Maximum burst beat size for Overlay Processor Out Port 0. Possible values: 0x4: 16 (default) 0x2: 8 0x1: 4

0x05100038 MDP_DISP_INTF_SEL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0008

This register configures the primary, secondary and external interface.

Following charts show all possible External interface connection with pipes.

Note) Since LCDC and DSI 2 video interface are sharing HW module inside MDP4, these two interfaces should be considered as the same interface.

MDP_DISP_INTF_SEL

Bits	Name	Description
31:14	RESERVED31_14	
13:12	E_SEL	External additional interface selection 0x0: DSI 1 Video 0x1: not used_1 0x2: not used_2 0x3: not used_3
11:10	S_SEL	Secondary additional interface selection 0x0: DSI 1 Video or Command 0x1: DSI 2 Video or Command 0x2: not used_1 0x3: not used_2

MDP_DISP_INTF_SEL (cont.)

Bits	Name	Description
9:8	P_SEL	Primary additional interface selection 0x0: DSI 1 Video or Command 0x1: DSI 2 Video or Command 0x2: not used_1 0x3: not used_2
7	DSI_CMD_INTF_SEL	Interface select for the DSI Command mode. If set to 1 it disables the MDDI interface on Primary and Secondary interface 0x0: DSI Command mode is not selected 0x1: DSI Command mode is selected
6	DSI_VIDEO_INTF_SEL	Interface select for the DSI Video mode 0x0: DSI Video interface is not selected 0x1: DSI VIdeo interface is selected
5:4	EXT_INTF_SEL	Overlay Processor 1/DMA_E output interface select: 0x0: DTV 0x1: DSI Video Mode 0x2: Reserved 0x3: TV Encoder (Analog TV)
3:2	SEC_INTF_SEL	DMA_S output interface select: 0x0: Reserved for LCDC RGB or LVDS Interface 0x1: DSI Video Mode 0x2: DSI Command Mode 0x3: Reserved for EBI2
1:0	PRIM_INTF_SEL	Overlay Processor 0/DMA_P output interface select: 0x0: Reserved for LCDC RGB or LVDS Interface 0x1: DSI Video Mode 0x2: DSI Command Mode 0x3: Reserved for EBI2

0x0510003C MDP_SW_SCRATCHPAD_REG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This 32-bit register can be used by display software driver as a scratch pad register. It doesn't control or monitor any functionality within MDP core.

MDP_SW_SCRATCHPAD_REG

Bits	Name	Description
31:0	SCRATCHPAD	Scratch pad register space for software

0x05100040 MDP_CGC_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x003F_FFFF

The MDP_CGC_EN register is used to enable the automatic functional clock gating mechanism inside the MDP, where the clocks are gated depending on the operation mode. Each bit is assigned to a gated clock tree. For maximum power saving, leave all bits at 1 during initialization. To force a block to have the clock on always regardless of the operation scenario, set the associated enable bit to 0.

MDP_CGC_EN

Bits	Name	Description
31:22	RESERVED31_22	
21	LAYER_MIXER2	Enables auto clock gating on Layer Mixer 2output path.
20	DMI	Enables auto clock gating on DMI core clock
19	SPLIT_DISPLAY	Enables auto clock gating on SPLIT_DISPLAY core clock
18	DSI2_CMD	Enables auto clock gating on DSI 2 Command mode core clock
17	DSI_CMD	Enables auto clock gating on DSI 1 Command mode core clock
16	DSI_VIDEO	Enables auto clock gating on DSI 1 Video mode timing generator core clock
15	MISR	Enables auto clock gating on MISR registers
14	MDDI	Reserved for EBI2 : Enables auto clock gating on AHB_M(EBI2) blocks core clocks.
13	AXI	Enables auto clock gating on AXI interface clocks.
12	DTV	Enables auto clock gating on DTV Timing Generator (external display) core clock.
11	LCDC	Enables auto clock gating on DSI 2 Video / LCDC Timing Generator core clock.
10	DMA_E	Enables auto clock gating on DMA_E clock.
9	DMA_S	Enables auto clock gating on DMA_S clock.
8	DMA_P	Enables auto clock gating on DMA_P clock.
7	VG3	Enables auto clock gating on V/G3 pipe. (Reserved for future support)
6	RGB3	Enables auto clock gating on RGB3 pipe. (Reserved for future support)
5	RGB2	Enables auto clock gating on RGB2 pipe.
4	RGB1	Enables auto clock gating on RGB1 pipe.
3	VG2	Enables auto clock gating on V/G2 pipe.

MDP_CGC_EN (cont.)

Bits	Name	Description
2	VG1	Enables auto clock gating on V/G1 pipe.
1	LAYER_MIXER1	Enables auto clock gating on Layer Mixer 1 output path.
0	LAYER_MIXER0	Enables auto clock gating on Layer Mixer 0 output path.

0x05100044 MDP_SEL_TEST_BUS_CLK_DOMAIN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_SEL_TEST_BUS_CLK_DOMAIN register is used to select whether the MDP_TEST_BUS output is driven with selected MDP CLK or HCLK or DSI 2 / LCDC PCLK or TV CLK or DSI 1 PCLK or AXI CLK domain test points.

MDP_SEL_TEST_BUS_CLK_DOMAIN

Bits	Name	Description
31:3	RESERVED31_3	
2:0	SEL_CLK_DOMAIN	0x0: core_clk_domain 0x1: hclk_domain 0x2: pclk_domain 0x3: tv_clk_domain 0x4: dsi_pclk_domain 0x5: axi_clk_domain

0x05100048 MDP_EBI1_ADDR_BASE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

MDP can access memory salves on two bus systems (e.g) EBI0 and EBI1.
MDP_EBI1_ADDR_BASE register defines the top address bits that define the address partition between the two buses

MDP_EBI1_ADDR_BASE

Bits	Name	Description
31:8	RESERVED31_8	
7:0	EBI1_ADDR_BASE	Bits <31..24> of the start address base for EBI1

0x0510004C MDP_MAX_RD_PENDING_CMD_CONFIG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_3333

MDP_MAX_RD_PENDING_CMD_CONFIG register sets the maximum limit for the number of read pending commands per MDP AXI port. This register should be written only when the corresponding AXI port is idle or when MDP is idle.

NOTE Since the read data FIFO in the AXI ports is sized as 48, max. possible pending commands of 8 cannot be supported (at burst size of 16) if MDP core clock frequency is lower than AXI frequency. But if MDP core clk frequency >= AXI clock frequency, max. pending commands for the AXI ports should be increased to 8 (programmed value = 7) for higher performance.

NOTE When MDP core clk frequency < AXI clk frequency, max. pending commands (for all ports) should be 3 (programmed value = 2) to prevent overflow of read data FIFO.

MDP_MAX_RD_PENDING_CMD_CONFIG

Bits	Name	Description
31:16	RESERVED31_16	
15	RESERVED15	
14:12	EBI1_PORT1_RD_CMD	The actual number of pending commands for the AXI port is one more than the programmed value. Default 0x1 means maximum of 2 pending requests.
11	RESERVED11	
10:8	EBI1_PORT0_RD_CMD	The actual number of pending commands for the AXI port is one more than the programmed value. Default 0x1 means maximum of 2 pending requests.
7	RESERVED7	
6:4	EBI0_PORT1_RD_CMD	The actual number of pending commands for the AXI port is one more than the programmed value. Default 0x1 means maximum of 2 pending requests.
3	RESERVED3	
2:0	EBI0_PORT0_RD_CMD	The actual number of pending commands for the AXI port is one more than the programmed value. Default 0x1 means maximum of 2 pending requests.

14.15.2 Interrupt registers

0x05100050 MDP_INTR_ENABLE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_INTR_ENABLE register is used to enable the MDP interrupts. For interrupts generated by histogram block, a further step is required: the appropriate local histogram interrupt enable registers (MDP_*_HIST_INTR_ENABLE) must be programmed.

MDP_INTR_ENABLE

Bits	Name	Description
31:0	INTR_ENABLE	Setting (1) a specific bit will enable the respective interrupt source within the MDP to send a level interrupt out of the MDP. Clearing (0) that bit will disable it from generating the MDP interrupt. Bit0: Overlay Processor 0 processing done Bit1: Overlay Processor 1 processing done Bit 2 : DMA_S transfer done Bit 3 : DMA_E transfer done Bit 4 : DMA_P transfer done Bit 5 : Video/Graphics1 histogram interrupt Bit 6 : Video/Graphics2 histogram interrupt Bit 7 : Primary vsync interrupt Bit 8 : Primary interface under run Bit 9 : External vsync interrupt Bit 10 : External interface under run Bit 11 : Sync primary line (rd_ptr) interrupt Bit 12 : Sync secondary line (rd_ptr) interrupt Bit 13 : Sync external line (rd_ptr) interrupt Bit 14 : Primary output line (wr_ptr) interrupt Bit 15 : Secondary output line (wr_ptr) interrupt Bit 16 : External output line (wr_ptr) interrupt Bit 17 : DMA_P ABL histogram interrupt Bit 18 : AXI port 0 read/write error Bit 19 : AXI port 1 read/write error Bit 20 : AXI port0 write data timeout Bit 21 : AXI port1 write data timeout Bit 22 : Primary DSI Command Autorefresh start interrupt Bit 23 : Secondary DSI Command Autorefresh start interrupt Bit 24 : Reserved Bit 25 : Reserved Bit 26 : DMA_S ABL histogram interrupt Bit 27 : Secondary vsync interrupt Bit 28 : Secondary interface under run Bit 29 : TE interval interrupt Bit 30 : Overlay Processor 2 processing done Bit 31 : LVDS PLL unlocks

0x05100054 MDP_INTR_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_INTR_STATUS register is the MDP interrupt status register.

MDP_INTR_STATUS

Bits	Name	Description
31:0	INTR_STATUS	When an MDP interrupt occurs, then reading this register will indicate what caused the interrupt since that each bit indicates the source of the interrupt that had happened. If multiple interrupt sources had happened, then multiple bits of this register will be. Bit0: Overlay Processor 0 processing done Bit1: Overlay Processor 1 processing done Bit 2 : DMA_S transfer done Bit 3 : DMA_E transfer done Bit 4 : DMA_P transfer done Bit 5 : Video/Graphics1 histogram interrupt Bit 6 : Video/Graphics2 histogram interrupt Bit 7 : Primary vsync interrupt Bit 8 : Primary interface under run Bit 9 : External vsync interrupt Bit 10 : External interface under run Bit 11 : Sync primary line (rd_ptr) interrupt Bit 12 : Sync secondary line (rd_ptr) interrupt Bit 13 : Sync external line (rd_ptr) interrupt Bit 14 : Primary output line (wr_ptr) interrupt Bit 15 : Secondary output line (wr_ptr) interrupt Bit 16 : External output line (wr_ptr) interrupt Bit 17 : DMA_P ABL histogram interrupt Bit 18 : AXI port 0 read/write error Bit 19 : AXI port 1 read/write error Bit 20 : AXI port0 write data timeout Bit 21 : AXI port1 write data timeout Bit 22 : Primary DSI Command Autorefresh start interrupt Bit 23 : Secondary DSI Command Autorefresh start interrupt Bit 24 : Reserved Bit 25 : Reserved Bit 26 : DMA_S ABL histogram interrupt Bit 27 : Secondary vsync interrupt Bit 28 : Secondary interface under run Bit 29 : TE interval interrupt Bit 30 : Overlay Processor 2 processing done Bit 31 : LVDS PLL unlocks

0x05100058 MDP_INTR_CLEAR

Type: Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_INTR_CLEAR register is used to clear all the MDP interrupts, except interrupts generated by the histogram blocks. To clear interrupts generated by histogram blocks, use specific local clear registers (MDP_*_HIST_INTR_CLEAR).

MDP_INTR_CLEAR

Bits	Name	Description
31:0	INTR_CLEAR	To clear the interrupt, make sure the interrupt has occurred, and then clear (0) this bit. Setting (1) a specific bit will clear the respective interrupt. A read from this register would indicate if the respective interrupt source is cleared (the bit is set (1)). So, at power up, it would read all 1's. Bit0: Overlay Processor 0 processing done Bit1: Overlay Processor 1 processing done Bit 2 : DMA_S transfer done Bit 3 : DMA_E transfer done Bit 4 : DMA_P transfer done Bit 5 : Reserved Bit 6 : Reserved Bit 7 : Primary vsync interrupt Bit 8 : Primary interface under run Bit 9 : External vsync interrupt Bit 10 : External interface under run Bit 11 : Sync primary line (rd_ptr) interrupt Bit 12 : Sync secondary line (rd_ptr) interrupt Bit 13 : Sync external line (rd_ptr) interrupt Bit 14 : Primary output line (wr_ptr) interrupt Bit 15 : Secondary output line (wr_ptr) interrupt Bit 16 : External output line (wr_ptr) interrupt Bit 17 : Reserved Bit 18 : AXI port 0 read/write error Bit 19 : AXI port 1 read/write error Bit 20 : AXI port0 write data timeout Bit 21 : AXI port1 write data timeout Bit 22 : Primary DSI Command Autorefresh start interrupt Bit 23 : Secondary DSI Command Autorefresh start interrupt Bit 24 : Reserved Bit 25 : Reserved Bit 26 : Reserved Bit 27 : Secondary vsync interrupt Bit 28 : Secondary interface under run Bit 29 : TE interval interrupt Bit 30 : Overlay Processor 2 processing done Bit 31 : LVDS PLL unlocks

14.15.3 EBI2 registers

MDP4.2 core has EBI2 interface only for core level verification purpose. Do not use EBI2 registers at the chip level.

0x05100060 MDP_EBI2_LCD0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_EBI2_LCD0 register stores the base address of a primary LCD panel connected to EBI2.

MDP_EBI2_LCD0

Bits	Name	Description
31:0	BASE_ADDR	This address is assumed to be at least half-word aligned, so bit [0] is ignored.

0x05100064 MDP_EBI2_LCD1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_EBI2_LCD1 register stores the base address of a secondary LCD panel connected to EBI2.

MDP_EBI2_LCD1

Bits	Name	Description
31:0	BASE_ADDR	This address is assumed to be at least half-word aligned, so bit [0] is ignored.

0x05100068 MDP_EBI2_LCD0_YSTRIDE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_EBI2_LCD0_YSTRIDE register provides the y-stride for a primary panel connected to EBI2

MDP_EBI2_LCD0_YSTRIDE

Bits	Name	Description
31:15	RESERVED_BITS31_15	
14	EBI2_YSTRIDE_EN	In memory mapped devices, if this bit is set (1) it indicates that the display size (width) is larger than the ROI width. When set, ebi2_ystride is used to write to a memory-mapped panel at EBI2_LCD0_ADDR. This bit can also be set to write to an external memory device in EBI2 space for TEST PURPOSES.
13:0	EBI2_YSTRIDE	The ystride of the LCD device attached to ebi2 interface in bytes.

0x0510006C MDP_EBI2_LCD1_YSTRIDE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_EBI2_LCD1_YSTRIDE register provides the y-stride for a secondary panel connected to EBI2

MDP_EBI2_LCD1_YSTRIDE

Bits	Name	Description
31:15	RESERVED_BITS31_15	
14	EBI2_YSTRIDE_EN	In memory mapped devices, if this bit is set (1) it indicates that the display size (width) is larger than the ROI width. When set, ebi2_ystride is used to write to a memory-mapped panel at EBI2_LCD1_ADDR. This bit can also be set to write to an external memory device in EBI2 space for TEST PURPOSES.
13:0	EBI2_YSTRIDE	The ystride of the LCD device attached to ebi2 interface in bytes.

0x05100070 MDP_EBI2_PORTMAP_MODE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_EBI2_PORTMAP_MODE register is the EBI2 LCD portmap mode register.

MDP_EBI2_PORTMAP_MODE

Bits	Name	Description
31:2	RESERVED_BITS31_2	

MDP_EBI2_PORTMAP_MODE (cont.)

Bits	Name	Description
1	LCD1_PORTMAP_MODE	When this bit is set (1), it indicates that the LCD1 on EBI2 requires a port-mapped write. Otherwise, the writes to EBI2 use the regular memory map one starting from the base address.
0	LCD0_PORTMAP_MODE	When this bit is set (1), it indicates that the LCD0 on EBI2 requires a port-mapped write. Otherwise, the writes to EBI2 use the regular memory map one starting from the base address.

14.15.4 DMI registers

0x05100080 MDP_DMI_CON

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x1555_0000

The MDP_PIPE_BUF_CON is used to control DMI interface for each MDP pipe.

MDP_DMI_CON

Bits	Name	Description
31:30	RESERVED31_30	
29:28	DMA_E_NUM_BUF	DMA_E number of buffer -1(0
27:26	DMA_S_NUM_BUF	DMA_S number of buffer -1(0
25:24	DMA_P_NUM_BUF	DMA_P number of buffer -1(0
23:22	RGB2_NUM_BUF	RGB2 number of buffer -1(0
21:20	RGB1_NUM_BUF	RGB1 number of buffer -1(0
19:18	VG2_NUM_BUF	VG2 number of buffer -1(0
17:16	VG1_NUM_BUF	VG1 number of buffer -1(0
15	DMI_SYNC_SEL	DMI frame synchronization source selection 0x1: frame synchronization by DMA pipe start 0x0: frame synchronization by DMA pipe done
14	DMA_E_BUF_SKIP_EN	If the control bit set to `1', DMI interface for DMA_E is only picked up latest DMI buffer ID what rotator DMI sent even if Rotator DMI sent several Buffer IDs that is non-block DMI mode.
13	DMA_S_BUF_SKIP_EN	If the control bit set to `1', DMI interface for DMA_S is only picked up latest DMI buffer ID what rotator DMI sent even if Rotator DMI sent several Buffer IDs that is non-block DMI mode
12	DMA_P_BUF_SKIP_EN	If the control bit set to `1', DMI interface for DMA_P is only picked up latest DMI buffer ID what rotator DMI sent even if Rotator DMI sent several Buffer IDs that is non-block DMI mode

MDP_DMI_CON (cont.)

Bits	Name	Description
11	RGB2_BUF_SKIP_EN	If the control bit set to `1', DMI interface for RGB2 is only picked up latest DMI buffer ID what rotator DMI sent even if Rotator DMI sent several Buffer IDs that is non-block DMI mode
10	RGB1_BUF_SKIP_EN	If the control bit set to `1', DMI interface for RGB1is only picked up latest DMI buffer ID what rotator DMI sent even if Rotator DMI sent several Buffer IDs that is non-block DMI mode
9	VG2_BUF_SKIP_EN	If the control bit set to `1', DMI interface for VG2 is only picked up latest DMI buffer ID what rotator DMI sent even if Rotator DMI sent several Buffer IDs that is non-block DMI mode
8	VG1_BUF_SKIP_EN	If the control bit set to `1', DMI interface for VG1is only picked up latest DMI buffer ID what rotator DMI sent even if Rotator DMI sent several Buffer IDs that is non-block DMI mode
7	DMI_RESET	DMI acknowledge buffer and strobe interface initializes to 0
6	DMA_E_DMI_EN	DMA_E pipe DMI interface enable
5	DMA_S_DMI_EN	DMA_S pipe DMI interface enable
4	DMA_P_DMI_EN	DMA_P pipe DMI interface enable
3	RGB2_DMI_EN	RGB2 pipe DMI interface enable
2	RGB1_DMI_EN	RGB1 pipe DMI interface enable
1	VG2_DMI_EN	VG2 pipe DMI interface enable
0	VG1_DMI_EN	VG1 pipe DMI interface enable

0x05100084 MDP_DMI_BUF_ID_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_PIPE_BUF_ID_STATUS is used to check BUF_ID in each MDP PIPE.

MDP_DMI_BUF_ID_STATUS

Bits	Name	Description
31:14	RESERVED31_14	
13:12	DMA_E_BUF_ID_STATUS	BUF ID is being used in DMA_E pipe
11:10	DMA_S_BUF_ID_STATUS	BUF ID is being used in DMA_S pipe
9:8	DMA_P_BUF_ID_STATUS	BUF ID is being used in DMA_P pipe
7:6	RGB2_BUF_ID_STATUS	BUF ID is being used in RGB2 pipe
5:4	RGB1_BUF_ID_STATUS	BUF ID is being used in RGB1 pipe

MDP_DMI_BUF_ID_STATUS (cont.)

Bits	Name	Description
3:2	VG2_BUF_ID_STATUS	BUF ID is being used in VG2 pipe
1:0	VG1_BUF_ID_STATUS	BUF ID is being used in VG1 pipe

14.15.5 Split Display registers

0x05100088 MDP_SPLIT_DISPLAY_CON

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_SPLIT_DISPLAY_CON is used to control MDP split display.

MDP_SPLIT_DISPLAY_CON

Bits	Name	Description
31:29	RESERVED31_29	
28	DMAP_DMAS_LINE_SPLIT	Static control signal to dictate the even split of an overlay line onto the DMA_P and then DMA_S pathis 0x1: Split the overlay width evenly between DMA_P and DMA_S 0x0: Do not split the incoming overlay between DMA_P and DMA_S
27:16	TE_LINE_INTERVAL_WATERMARK	the watermark is to generate TE interval interrupt if smart panels for split display are not synchronized that MDP will generate TE interval interrupt if TE line interval between 2 smart panels is large then TE_LINE_INTERVAL_WATERMARK value
15:8	RESERVED15_8	
7	PRIM_TIM_SYNC_EN	DSI1 Video Timing generator sync mode enable. If DSI2 Video timing generator is connected to DMA_P pipe and the timing engine has already turned on for dumb panel by MDP_LCDC_EN register prior to tuning on split display enable then, it is required to set to high accompany with split display enable to support exact-sync mode between 2 dumb panels. video split display mode 0x1: Timing generator sync to DSI2 Video timing generator in 0x0: not use sync mode

MDP_SPLIT_DISPLAY_CON (cont.)

Bits	Name	Description
6	SEC_TIM_SYNC_EN	DSI2 Video Timing generator sync mode enable. If DSI1 Video timing generator is connected to DMA_P pipe and the timing engine has already turned on for dumb panel by MDP_DSI_VIDEO_EN register prior to tuning on split display enable then, it is required to set to high accompany with split display enable to support exact-sync mode between 2 dumb panels. split display mode 0x1: Timing generator sync to DSI1 Video timing generator in video 0x0: not use sync mode
5	SPLIT_DISPLAY_EN_DB_DIS	Reserved. This bit must be "1".
4	PRIM_TIM_GEN_SEL	Reserved. This bit must be "0".
3	USE_LAYER_MIX0_2PANEL	Reserved.
2	SMART_PANEL_FREE_RUN	Select Smart Panel operation mode 0x1: Free running mode between 2 panels 0x0: Synchronous mode between 2 panels
1	SPLIT_DISPLAY_TYPE	Type of split display 0x1: Smart Panel (with frame buffer in Panel) 0x0: Dumb Panel (without frame buffer in Panel)
0	SPLIT_DISPLAY_EN	Enable split display. The ownership of 2panels start control and timing generator will be in Layer Mix0 or DMA_P registers.

0x0510008C MDP_TE_LINE_INTERVAL_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TE_LINE_INTERVAL_STATUS is indicated the number of TE line interval between 2 smart panels.

MDP_TE_LINE_INTERVAL_STATUS

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TE_LINE_INTERVAL_STATUS	Status of the number of TE line interval between 2 smart panels.

14.15.6 MDDI parameter registers

MDDI registers exist in HW but MDDI interface has been removed in MDP4.2.

0x05100090 MDP_MDDI_PARAM_WR_SEL

Type: Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_MDDI_PARAM_WR_SEL register is used to select a MDDI type for writing display parameters. It also writes CLIENTID to the selected register.

MDP_MDDI_PARAM_WR_SEL

Bits	Name	Description
31:16	MDDI_VID_CLIENTID	MDDI video client id parameter
15:2	RESERVED15_2	
1:0	MDDI_LD_PARAM_SEL	Parameter register write select: 0x0: Primary MDDI set 0x1: Secondary MDDI set 0x2: External MDDI set

0x05100094 MDP_MDDI_PARAM

Type: Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_MDDI_PARAM register writes the display parameters to the MDDI type selected by MDP_MDDI_PARAM_WR_SEL

MDP_MDDI_PARAM

Bits	Name	Description
31:16	MDDI_VID_FORMAT_DESC	MDDI video format description parameter
15:0	MDDI_PIX_DATA_ATTR	MDDI pixel data attribute parameter

0x05100098 MDP_MDDI_DATA_XFR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_MDDI_DATA_XFR register determines if the data would be sent out of MDDI every cycle or every alternate cycle

MDP_MDDI_DATA_XFR

Bits	Name	Description
31:2	RESERVED31_2	
1	MDDI_DATA_XFR_EXT	Note: For External MDDI 0x0: Alternate cycle data transfer (default) 0x1: Every cycle data transfer
0	MDDI_DATA_XFR_PRIM	Note: For Primary MDDI 0x0: Alternate cycle data transfer (default) 0x1: Every cycle data transfer.

14.15.7 DSI 1 Command Mode parameter registers

0x051000A0 MDP_DSI_CMD_MODE_ID_MAP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0001

The MDP_DSI_COMMAND_MODE_ID_MAP register is used to MAP the DSI ID to Primary and Secondary interface. This is for DSI1 command interface.

NOTE Make sure that the ID selected for Primary and Secondary Interface are mutually exclusive.

MDP_DSI_CMD_MODE_ID_MAP

Bits	Name	Description
31:5	RESERVED31_5	
4	SEC_DSI_CMD_ID	DSI Command ID for Secondary interface. Make sure it is different from the primary ID 0x0: Secondary DSI CMD ID is set to zero (default) 0x1: Secondary DSI CMD ID is set to one
3:1	RESERVED3_1	
0	PRIM_DSI_CMD_ID	DSI Command ID for Primary interface. Make sure it is different from the secondary ID 0x0: Primary DSI CMD ID is set to zero 0x1: Primary DSI CMD ID is set to one (default)

0x051000A4 MDP_DSI_CMD_MODE_TRIGGER_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DSI_COMMAND_MODE_TRIGGER_EN register is used to enable the DSI TRIGGER processing on Primary or Secondary interface. This is for DSI1 command interface.

NOTE Only one DSI trigger is supported at any given time, i.e., the trigger processing can be enabled either for Primary or for Secondary interface but not both at the same time.

MDP_DSI_CMD_MODE_TRIGGER_EN

Bits	Name	Description
31:5	RESERVED31_5	
4	DSI_CMD_TG_INTF_SEL	Takes effect only if DSI_CMD_TG_EN is set to 1. 0x0: Use trigger mode on Primary Interface (default) 0x1: Use trigger mode on Secondary Interface
3:1	RESERVED3_1	
0	DSI_CMD_TG_EN	DSI Command Trigger enable. Set it to 1 to enable trigger processing 0x0: Disable trigger processing (default) 0x1: Enable trigger processing

14.15.8 DSI 2 Command Mode parameter registers

0x051000B0 MDP_DSI2_CMD_MODE_ID_MAP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0001

The MDP_DSI_COMMAND_MODE_ID_MAP register is used to MAP the DSI ID to Primary and Secondary interface.

NOTE Make sure that the ID selected for Primary and Secondary Interface are mutually exclusive.

MDP_DSI2_CMD_MODE_ID_MAP

Bits	Name	Description
31:5	RESERVED31_5	

MDP_DSI2_CMD_MODE_ID_MAP (cont.)

Bits	Name	Description
4	SEC_DSI_CMD_ID	DSI Command ID for Secondary interface. Make sure it is different from the primary ID 0x0: Secondary DSI CMD ID is set to zero (default) 0x1: Secondary DSI CMD ID is set to one
3:1	RESERVED3_1	
0	PRIM_DSI_CMD_ID	DSI Command ID for Primary interface. Make sure it is different from the secondary ID 0x0: Primary DSI CMD ID is set to zero 0x1: Primary DSI CMD ID is set to one (default)

0x051000B4 MDP_DSI2_CMD_MODE_TRIGGER_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DSI_COMMAND_MODE_TRIGGER_EN register is used to enable the DSI TRIGGER processing on Primary or Secondary interface.

NOTE Only one DSI trigger is supported at any given time, i.e., the trigger processing can be enabled either for Primary or for Secondary interface but not both at the same time.

MDP_DSI2_CMD_MODE_TRIGGER_EN

Bits	Name	Description
31:5	RESERVED31_5	
4	DSI_CMD_TG_INTF_SEL	Takes effect only if DSI_CMD_TG_EN is set to 1. 0x0: Use trigger mode on Primary Interface (default) 0x1: Use trigger mode on Secondary Interface
3:1	RESERVED3_1	
0	DSI_CMD_TG_EN	DSI Command Trigger enable. Set it to 1 to enable trigger processing 0x0: Disable trigger processing (default) 0x1: Enable trigger processing

14.15.9 Internal memory chip select advanced control register

0x051000C0 MDP_CS_CONTROL_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The legacy MDP doesn't control internal memory CS (chip select) efficiently in terms of power. This register controls the memory CS control method and can be used for power consumption comparison.

MDP_CS_CONTROL_0

Bits	Name	Description
31:24	RGB2_PIPE_CS_MODE	RGB2 pipe memory CS control mode. Each bit controls different module and `0" is legacy mode and `1' is advanced mode. bit 7 : Reserved bit 6 : Reserved bit 5 : Reserved bit 4 : Reserved bit 3 : Reserved bit 2 : IGC LUT bit1: Scaler bit0: Fetch line buffer
23:16	RGB1_PIPE_CS_MODE	RGB1 pipe memory CS control mode. Each bit controls different module and `0" is legacy mode and `1' is advanced mode. bit 7 : Reserved bit 6 : Reserved bit 5 : Reserved bit 4 : Reserved bit 3 : Reserved bit 2 : IGC LUT bit1: Scaler bit0: Fetch line buffer
15:8	VG2_PIPE_CS_MODE	VG2 pipe memory CS control mode. Each bit controls different module and `0" is legacy mode and `1' is advanced mode. bit 7 : IGC_LUT bit 6 : QSEED bit 5 : Scaler line buffer bit 4 : HIST LUT bit 3 : HIST BIN bit 2 : de-interlace bit1: Upsampler bit 0: Fetch line buffer

MDP_CS_CONTROL_0 (cont.)

Bits	Name	Description
7:0	VG1_PIPE_CS_MODE	VG1 pipe memory CS control mode. Each bit controls different module and `0" is legacy mode and `1' is advanced mode. bit 7 : IGC_LUT bit 6 : QSEED bit 5 : Scaler line buffer bit 4 : HIST LUT bit 3 : HIST BIN bit 2 : de-interlace bit1: Upsampler bit0: Fetch line buffer

0x051000C4 MDP_CS_CONTROL_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The legacy MDP doesn't control internal memory CS (chip select) efficiently in terms of power. This register controls the memory CS control method and can be used for power consumption comparison.

MDP_CS_CONTROL_1

Bits	Name	Description
31:24	LM_PIPE_CS_MODE	LM pipe memory CS control mode. Each bit controls different module and `0" is legacy mode and `1' is advanced mode. bit 7 : Reserved bit 6 : Reserved bit 5 : Reserved bit 4 : Reserved bit 3 : Reserved bit 2 : Reserved bit1: LM1 Packer bit0: LM0 Packer
23:16	DMA_E_PIPE_CS_MODE	DMA_E pipe memory CS control mode. Each bit controls different module and `0" is legacy mode and `1' is advanced mode. bit 7 : Reserved bit 6 : Reserved bit 5 : Reserved bit 4 : Reserved bit 3 : Reserved bit 2 : Deflickering Filter bit1: Cursor Fetch line buffer bit0: Image Fetch line buffer

MDP_CS_CONTROL_1 (cont.)

Bits	Name	Description
15:8	DMA_S_PIPE_CS_MODE	DMA_S pipe memory CS control mode. Each bit controls different module and `0" is legacy mode and `1' is advanced mode. bit 7: Reserved bit 6: Reserved bit 5: Packer bit 4: IGC LUT bit 3: HIST LUT bit 2: HIST BIN bit1: Reserved bit 0: Image Fetch
7:0	DMA_P_PIPE_CS_MODE	DMA_P pipe memory CS control mode. Each bit controls different module and `0" is legacy mode and `1' is advanced mode. bit 7: Reserved bit 6: Reserved bit 5: Packer bit 4: IGC LUT bit 3: HIST LUT bit 2: HIST BIN bit 1: Cursor Fetch bit 0: Image Fetch

0x051000D0 MDP_OVERLAYPROC2_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

This register is used to start Overlay Processor 2 fetching and processing Note, Overlay Processor 2is NOT associated with ANY DMA or external interfaces. The only path for the Overlay Processor 2 is back to memory.

MDP_OVERLAYPROC2_START

Bits	Name	Description
31:0	OVERLAYPROC2_START	A write to register will start Overlay Processor 2 since it is always in On-Demand mode. There is no way to route an interface vsync to kick start Overlay Processor 2. All register programming should be complete before kick starting the operation.

14.15.10 Synchronization registers

0x05100100 MDP_SYNC_CONFIG_P

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0xFFE7_FFFF

The MDP_SYNC_CONFIG_P register is a primary synchronization configuration register.

If the height is greater than 2048, the MDP_SYNC_CONFIG_P_OVERRIDE register must be used.

MDP_SYNC_CONFIG_P

Bits	Name	Description
31:21	HEIGHT	Display height - 1. It is the vertical total number of lines.
20	VSYNC_IN_EN	Setting (1) this bit will sync with the external frame sync input
19	VSYNC_COUNTER_EN	Setting (1) this bit to enable the internal counter
18:0	VSYNC_COUNT	This scale value to be programmed is the ratio of the MDP VSYNC clock frequency to LCD panel frequency divided by the no. of rows (lines) in the LCD panel. For example, if the VSYNC clock is 133 MHz and the LCD is 176 lines (rows) and 220 pixels (columns) at 60 Hz, then the value to be programmed is 133 * 10^6 / (60 * 176) = 12594 That is, it takes 12594 MDP clocks to complete writing one line in the LCD panel.

0x05100104 MDP_SYNC_CONFIG_S

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0xFFE7_FFFF

The MDP_SYNC_CONFIG_S register is a secondary synchronization configuration register.

If the height is greater than 2048, the MDP_SYNC_CONFIG_S_OVERRIDE register must be used.

MDP_SYNC_CONFIG_S

Bits	Name	Description
31:21	HEIGHT	Display height - 1. It is the vertical total number of lines.
20	VSYNC_IN_EN	Setting (1) this bit will sync with external frame sync input
19	VSYNC_COUNTER_EN	Setting (1) this bit will enable the internal counter

MDP_SYNC_CONFIG_S (cont.)

Bits	Name	Description
18:0	VSYNC_COUNT	This scale value to be programmed is the ratio of the MDP VSYNC clock frequency to LCD panel frequency divided by the no. of rows (lines) in the LCD panel. For example, if the VSYNC clock is 133 MHz and the LDC is 176 lines (rows) and 220 pixels (columns) at 60 Hz, then the value to be programmed is 133 * 10^6 / (60 * 176) = 12594 That is, it takes 12594 MDP clocks to complete writing one line in the LCD panel.

0x05100108 MDP_SYNC_CONFIG_E

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0xFFE7_FFFF

The MDP_SYNC_CONFIG_E register is an external synchronization configuration register.

If the height is greater than 2048, the MDP_SYNC_CONFIG_E_OVERRIDE register must be used.

MDP_SYNC_CONFIG_E

Bits	Name	Description
31:21	HEIGHT	Display height - 1. It is the vertical total number of lines.
20	VSYNC_IN_EN	Setting (1) this bit will sync with external frame sync input
19	VSYNC_COUNTER_EN	Setting (1) this bit will enable the internal counter
18:0	VSYNC_COUNT	This scale value to be programmed is the ratio of the MDP VSYNC clock frequency to LCD panel frequency divided by the no. of rows (lines) in the LCD panel. For example, if the VSYNC clock is 133 MHz and the LDC is 176 lines (rows) and 220 pixels (columns) at 60 Hz, then the value to be programmed is 133 * 10^6 / (60 * 176) = 12594 That is, it takes 12594 MDP clocks to complete writing one line in the LCD panel.

0x0510010C MDP_SYNC_WRCOUNT_P

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0000

The MDP_SYNC_STATUS_P register is a primary synchronization status register. Writing to this register loads the line counter and is equivalent to providing a software Vsync.

MDP_SYNC_WRCOUNT_P

Bits	Name	Description
31:28	RESERVED31_28	
27:16	FRAME_COUNT	Writing to this register will load the counter according to the written value.
15:12	RESERVED15_12	
11:0	LINE_COUNT	Writing to this register will load the counter according to the written value.

0x05100110 MDP_SYNC_WRCOUNT_S

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0000

The MDP_SYNC_STATUS_S register is a secondary synchronization status register. Writing to this register loads the line counter and is equivalent to providing a software Vsync.

MDP_SYNC_WRCOUNT_S

Bits	Name	Description
31:28	RESERVED31_28	
27:16	FRAME_COUNT	Writing to this register will load the counter according to the written value.
15:12	RESERVED15_12	
11:0	LINE_COUNT	Writing to this register will load the counter according to the written value.

0x05100114 MDP_SYNC_WRCOUNT_E

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0000

The MDP_SYNC_STATUS_E register is an external synchronization status register. Writing to this register loads the line counter and is equivalent to providing a software Vsync.

MDP_SYNC_WRCOUNT_E

Bits	Name	Description
31:28	RESERVED31_28	

MDP_SYNC_WRCOUNT_E (cont.)

Bits	Name	Description
27:16	FRAME_COUNT	Writing to this register will load the counter according to the written value.
15:12	RESERVED15_12	
11:0	LINE_COUNT	Writing to this register will load the counter according to the written value.

0x05100118 MDP_PRIMARY_VSYNC_OUT_CTRL

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0001

The MDP_PRIMARY_VSYNC_OUT_CTRL register is used to configure the primary vsync output.

MDP_PRIMARY_VSYNC_OUT_CTRL

Bits	Name	Description
31	VSYNC_OUT_EN	Set (1) this bit to enable the vsync pulse Clear (0) this bit to not enable the vsync pulse If vsync pulse is enabled, the enable pin is asserted and sync output is the pulse specified. If vsync pulse is disabled, the enabled ID is de-asserted and sync output is gated to ground.
30	VSYNC_OUT_INVERT	Set (1) this bit to invert the vsync pulse Clear (0) this bit to not invert the vsync pulse If vsync is not inverted, pulse will be active high if vsync is inverted, pulse will be active low Note: This register bit is also used to invert the incoming vsync when there is no external outgoing vsync.
29:20	RESERVED29_20	
19:0	VSYNC_OUT_WIDTH	The cycle count of the pulse width

0x0510011C MDP_SECONDARY_VSYNC_OUT_CTRL

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0001

The MDP_SECONDARY_VSYNC_OUT_CTRL register is used to configure the secondary vsync output.

MDP_SECONDARY_VSYNC_OUT_CTRL

Bits	Name	Description
31	VSYNC_OUT_EN	Set (1) this bit to enable the vsync pulse Clear (0) this bit to not enable the vsync pulse If the vsync pulse is enabled, the enable pin is asserted and the sync output is the pulse specified. If the vsync pulse is disabled, the enabled ID is de-asserted and the sync output is gated to ground.
30	VSYNC_OUT_INVERT	Set (1) this bit to invert the vsync pulse Clear (0) this bit to not invert the vsync pulse If vsync is not inverted, the pulse will be active high If vsync is inverted, the pulse will be active low Note: This register bit is also used to invert the incoming Vsync when there is no external outgoing vsync
29:20	RESERVED29_20	
19:0	VSYNC_OUT_WIDTH	The cycle count of the pulse width

0x05100120 MDP_EXTERNAL_VSYNC_OUT_CTRL

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0001

The MDP_EXTERNAL_VSYNC_OUT_CTRL register is used to configure the external vsync output.

MDP_EXTERNAL_VSYNC_OUT_CTRL

Bits	Name	Description
31	VSYNC_OUT_EN	Set (1) this bit to enable the vsync pulse Clear (0) this bit to not enable the vsync pulse If the vsync pulse is enabled, the enable pin is asserted and the sync output is the pulse specified. If the vsync pulse is disabled, the enabled ID is de-asserted and the sync output is gated to ground.
30	VSYNC_OUT_INVERT	Set (1) this bit to invert the vsync pulse Clear (0) this bit to not invert the vsync pulse If vsync is not inverted, the pulse will be active high If vsync is inverted, the pulse will be active low Note: This register bit is also used to invert the incoming vsync when there is no external outgoing vsync.
29:20	RESERVED29_20	
19:0	VSYNC_OUT_WIDTH	The cycle count of the pulse width

0x05100124 MDP_VSYNC_SEL

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0024

The MDP_VSYNC_SEL register is used to select either the vsyncs from GPIOs or DSI blocks to be used internally as primary, secondary and external vsyncs.

MDP_VSYNC_SEL

Bits	Name	Description
31:9	RESERVED31_9	
8	EXTERNAL_VSYNC_SEL_EXTEND	Bit added to maintain SW compatibility. Detailed information in EXTERNAL_VSYNC_SEL field.
7	SECONDARY_VSYNC_SEL_EXTEND	Bit added to maintain SW compatibility. Detailed information in SECONDARY_VSYNC_SEL field.
6	PRIMARY_VSYNC_SEL_EXTEND	Bit added to maintain SW compatibility. Detailed information in PRIMARY_VSYNC_SEL field.
5:4	EXTERNAL_VSYNC_SEL	External vsync sel If EXTERNAL_VSYNC_SEL_EXTEND = 0 (legacy mode) If EXTERNAL_VSYNC_SEL_EXTEND = 1 (extended mode) 0x0: Vsync primary from GPIO 0x1: Reserved 0x2: Vsync external from GPIO (default) 0x3: External vsync from MDDI block 0x0: Vsync from DSI1 Controller Interface 0x1: Vsync from DSI2 Controller Interface
3:2	SECONDARY_VSYNC_SEL	Secondary vsync sel If SECONDARY_VSYNC_SEL_EXTEND = 0 (legacy mode) If SECONDARY_VSYNC_SEL_EXTEND = 1 (extended mode) 0x0: Vsync0 from GPIO 0x1: Vsync1 from GPIO (default) 0x2: Vsync2 from GPIO 0x3: Secondary vsync from MDDI block 0x0: Vsync from DSI1 Controller Interface 0x1: Vsync from DSI2 Controller Interface
1:0	PRIMARY_VSYNC_SEL	Primary vsync sel If PRIMARY_VSYNC_SEL_EXTEND = 0 (legacy mode) If PRIMARY_VSYNC_SEL_EXTEND = 1 (extended mode) 0x0: Vsync primary from GPIO (default) 0x1: Reserved 0x2: Vsync external from GPIO 0x3: Primary vsync from MDDI block 0x0: Vsync from DSI1 Controller Interface 0x1: Vsync from DSI2 Controller Interface

0x05100128 MDP_PRIM_VSYNC_INIT_VAL

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0000

MDP_PRIM_VSYNC_INIT_VAL defines the value with which the read pointer gets loaded at primary vsync edge.

MDP_PRIM_VSYNC_INIT_VAL

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	PRIM_VSYNC_INIT_VAL	Specify the init value to which the read pointer gets loaded at vsync edge.

0x0510012C MDP_SEC_VSYNC_INIT_VAL

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0000

MDP_SEC_VSYNC_INIT_VAL defines the value with which the read pointer gets loaded at secondary vsync edge.

MDP_SEC_VSYNC_INIT_VAL

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	SEC_VSYNC_INIT_VAL	Specify the init value to which the read pointer gets loaded at vsync edge.

0x05100130 MDP_EXT_VSYNC_INIT_VAL

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0000

MDP_EXT_VSYNC_INIT_VAL defines the value with which the read pointer gets loaded at external vsync edge.

MDP_EXT_VSYNC_INIT_VAL

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	EXT_VSYNC_INIT_VAL	Specify the init value to which the read pointer gets loaded at vsync edge.

0x05100134 MDP_PRIM_VSYNC_OUT_VAL

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0000

MDP_PRIM_VSYNC_OUT_VAL defines the value of the internally generated read pointer at which the primary outgoing vsync is generated.

MDP_PRIM_VSYNC_OUT_VAL

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	PRIM_VSYNC_OUT_VAL	Specify the value of the read pointer at which the outgoing primary vsync is generated.

0x05100138 MDP_SEC_VSYNC_OUT_VAL

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0000

MDP_SEC_VSYNC_OUT_VAL defines the value of the internally generated read pointer at which the secondary outgoing vsync is generated.

MDP_SEC_VSYNC_OUT_VAL

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	SEC_VSYNC_OUT_VAL	Specify the value of the read pointer at which the secondary outgoing vsync is generated.

0x0510013C MDP_EXT_VSYNC_OUT_VAL

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0000

MDP_EXT_VSYNC_OUT_VAL defines the value of the internally generated read pointer at which the external outgoing vsync is generated.

MDP_EXT_VSYNC_OUT_VAL

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	EXT_VSYNC_OUT_VAL	Specify the value of the read pointer at which the external outgoing vsync is generated.

0x05100140 MDP_PRIM_INT_CNT_VAL

Type: Read
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0000

The MDP_PRIM_INT_CNT_VAL register shows the internal line and frame counter for primary vsync.

MDP_PRIM_INT_CNT_VAL

Bits	Name	Description
31:28	RESERVED31_28	
27:16	FRAME_COUNT	Internal frame count value for primary vsync.
15:12	RESERVED15_12	
11:0	LINE_COUNT	Internal line count value for primary vsync.

0x05100144 MDP_SEC_INT_CNT_VAL

Type: Read
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0000

The MDP_SEC_INT_CNT_VAL register shows the internal line and frame counter for secondary vsync.

MDP_SEC_INT_CNT_VAL

Bits	Name	Description
31:28	RESERVED31_28	
27:16	FRAME_COUNT	Internal frame count value for secondary vsync.
15:12	RESERVED15_12	
11:0	LINE_COUNT	Internal line count value for secondary vsync.

0x05100148 MDP_EXT_INT_CNT_VAL

Type: Read
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0000

The MDP_EXT_INT_CNT_VAL register shows the internal line and frame counter for external vsync.

MDP_EXT_INT_CNT_VAL

Bits	Name	Description
31:28	RESERVED31_28	
27:16	FRAME_COUNT	Internal frame count value for the external vsync.
15:12	RESERVED15_12	
11:0	LINE_COUNT	Internal line count value for the external vsync.

0x0510014C MDP_AUTOREFRESH_CONFIG_P

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0001

The MDP_AUTOREFRESH_CONFIG_P register enables primary autorefresh and set the frame count for autorefresh.

MDP_AUTOREFRESH_CONFIG_P

Bits	Name	Description
31:29	RESERVED31_29	
28	ENABLE	Enable autorefresh. 0x0: disable 0x1: enable

MDP_AUTOREFRESH_CONFIG_P (cont.)

Bits	Name	Description
27:12	RESERVED27_12	
11:0	FRAME_NUM	Frame number at which an autorefresh start pulse is generated.

0x05100150 MDP_AUTOREFRESH_CONFIG_S

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0001

The MDP_AUTOREFRESH_CONFIG_S register enables secondary autorefresh and set the frame count for autorefresh.

MDP_AUTOREFRESH_CONFIG_S

Bits	Name	Description
31:29	RESERVED31_29	
28	ENABLE	Enable autorefresh. 0x0: disable 0x1: enable
27:12	RESERVED27_12	
11:0	FRAME_NUM	Frame number at which an autorefresh start pulse is generated.

0x05100154 MDP_SYNC_CONFIG_P_OVERRIDE

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0FFF

This register is used to extend the height field for the MDP_SYNC_CONFIG_P register. When the OVERRIDE bit is set, the height in this register will override the height in MDP_SYNC_CONFIG.

MDP_SYNC_CONFIG_P_OVERRIDE

Bits	Name	Description
31:17	RESERVED31_17	
16	OVERRIDE	Setting this bit will allow the height in this register to override that of the MDP_SYNC_CONFIG_P register.
15:12	RESERVED15_12	
11:0	HEIGHT	Display height - 1. It is the vertical total number of lines.

0x05100158 MDP_SYNC_CONFIG_S_OVERRIDE

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0FFF

This register is used to extend the height field for the MDP_SYNC_CONFIG_S register. When the OVERRIDE bit is set, the height in this register will override the height in MDP_SYNC_CONFIG.

MDP_SYNC_CONFIG_S_OVERRIDE

Bits	Name	Description
31:17	RESERVED31_17	
16	OVERRIDE	Setting this bit will allow the height in this register to override that of the MDP_SYNC_CONFIG_S register.
15:12	RESERVED15_12	
11:0	HEIGHT	Display height - 1. It is the vertical total number of lines.

0x0510015C MDP_SYNC_CONFIG_E_OVERRIDE

Type: Read/Write
Clock: CC_MDP_VSYNC_CLK
Reset State: 0x0000_0FFF

This register is used to extend the height field for the MDP_SYNC_CONFIG_E register. When the OVERRIDE bit is set, the height in this register will override the height in MDP_SYNC_CONFIG.

MDP_SYNC_CONFIG_E_OVERRIDE

Bits	Name	Description
31:17	RESERVED31_17	
16	OVERRIDE	Setting this bit will allow the height in this register to override that of the MDP_SYNC_CONFIG_E register.
15:12	RESERVED15_12	
11:0	HEIGHT	Display height - 1. It is the vertical total number of lines.

0x05100200 MDP_SYNC_THRESH_P

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0010_0000

The MDP_SYNC_THRESH_P register is a primary synchronization threshold register.

MDP_SYNC_THRESH_P

Bits	Name	Description
31:28	RESERVED31_28	
27:16	CONTINUE_THRESHOLD	The minimum number of lines the write pointer needs to be above the read pointer so that it is safe to write to the primary LCD. (This check is not done for the first ROI line write of an update).
15:12	RESERVED15_12	
11:0	START_THRESHOLD	Allows the first ROI line write to an primary LCD update when read pointer is between the range of ROI start line and ROI start line plus this setting.

0x05100204 MDP_SYNC_THRESH_S

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0010_0000

The MDP_SYNC_THRESH_S register is a secondary synchronization threshold register.

MDP_SYNC_THRESH_S

Bits	Name	Description
31:28	RESERVED31_28	
27:16	CONTINUE_THRESHOLD	The minimum number of lines the write pointer needs to be above the read pointer so that it is safe to write to the secondary LCD. (This check is not done for the first ROI line write of an update).
15:12	RESERVED15_12	
11:0	START_THRESHOLD	Allows the first ROI line write to an secondary LCD update when read pointer is between the range of ROI start line and ROI start line plus this setting.

0x05100208 MDP_SYNC_THRESH_E

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0010_0000

The MDP_SYNC_THRESH_E register is an external synchronization threshold register.

MDP_SYNC_THRESH_E

Bits	Name	Description
31:28	RESERVED31_28	
27:16	CONTINUE_THRESHOLD	The minimum number of lines the write pointer needs to be above the read pointer so that it is safe to write to the external LCD. (This check is not done for the first ROI line write of an update).
15:12	RESERVED15_12	
11:0	START_THRESHOLD	Allows the first ROI line write to an external LCD update when read pointer is between the range of ROI start line and ROI start line plus this setting.

0x0510020C MDP_TEAR_CHECK_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEAR_CHECK_EN register is used to enable tearing check on different displays.

MDP_TEAR_CHECK_EN

Bits	Name	Description
31:3	RESERVED31_3	
2	EXTERNAL_TEAR_CHECK_EN	0x0: Disable (default) 0x1: Enable
1	SECONDARY_TEAR_CHECK_EN	0x0: Disable (default) 0x1: Enable
0	PRIMARY_TEAR_CHECK_EN	0x0: Disable (default) 0x1: Enable

0x05100210 MDP_PRIM_START_POS

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_PRIM_START_POS defines the starting y position value for the vsync line counter at every frame (for the primary display).

MDP_PRIM_START_POS

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	START_POS	Specify the y position from which the start_threshold value is added and write is kicked off if the read pointer falls within that region.

0x05100214 MDP_SEC_START_POS

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_SEC_START_POS defines the y position value for the kick off condition (for the secondary display).

MDP_SEC_START_POS

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	START_POS	Specify the y position from which the start_threshold value is added and write is kicked off if the read pointer falls within that region.

0x05100218 MDP_EXT_START_POS

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_EXT_START_POS defines the starting y position value for the vsync line counter at every frame (for the external display).

MDP_EXT_START_POS

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	START_POS	Specify the y position from which the start_threshold value is added and write is kicked off if the read pointer falls within that region.

0x0510021C MDP_PRIMARY_RD_PTR_IRQ

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0FFF

MDP_PRIMARY_RD_PTR_IRQ defines the read pointer of the primary display at which an interrupt has to be generated.

MDP_PRIMARY_RD_PTR_IRQ

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	IRQ_LINE	Specify the read pointer value at which an interrupt has to be generated.

0x05100220 MDP_SECONDARY_RD_PTR_IRQ

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0FFF

MDP_SECONDARY_RD_PTR_IRQ defines the read pointer of the secondary display at which an interrupt has to be generated.

MDP_SECONDARY_RD_PTR_IRQ

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	IRQ_LINE	Specify the read pointer value at which an interrupt has to be generated.

0x05100224 MDP_EXTERNAL_RD_PTR_IRQ

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0FFF

MDP_EXTERNAL_RD_PTR_IRQ defines the read pointer of the external display at which an interrupt has to be generated.

MDP_EXTERNAL_RD_PTR_IRQ

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	IRQ_LINE	Specify the read pointer value at which an interrupt has to be generated.

14.15.11 MGEN2MAXI control registers

NOTE1: The following registers are defined for 11 generic clients (9 read + 2 write) and 2 arbiters (AXI r0p0++ master ports).

Client0 - VG1 read;

Client1 - VG2 read;

Client2 - RGB1 read;

Client3 - RGB2 read;

Client4 - DMA_P Image read;

Client5 - DMA_P Cursor read;

Client6 - DMA_S read;

Client7 - DMA_E Image read;

Client8 - DMA_E Cursor read;

Client9 - Overlay0 write;

Client10 - Overlay1 write

0x05100400 MDP_XBAR_FIXED_ARB_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_07FF

Client requests are assigned to one of the arbiters (AXI master ports) using several possible methods. If none of these methods apply to a particular request, it is sent to arbiter 0.

The first method is fixed arbiter assignment. This allows some or all clients to be forced to a particular AXI master port, for example if you want a dedicated AXI master port for one of the clients. If this is applied to a request, it takes highest priority over the other methods.

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_FIXED_ARB_EN

Bits	Name	Description
31:11	RESERVED31_11	This field has no function and should be set to zero for future compatibility
10:0	FIXED_ARB_EN	Enables fixed arbiter assignment, 1 bit per client.

0x05100404 MDP_XBAR_FIXED_ARB_SEL_RD

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0001_0000

MDP_XBAR_FIXED_ARB_SEL_RD register selects the AXI master port that will be assigned for each internal read client if the corresponding client is enabled by FIXED_ARB_EN.

NOTE This register should be written only when the corresponding read client or MDP core is idle.

MDP_XBAR_FIXED_ARB_SEL_RD

Bits	Name	Description
31:21	RESERVED31_21	
20	CLIENT8	DMA_E cursor 0x0: AXI Port0 0x1: AXI Port1
19	RESERVED19	
18	CLIENT7	DMA_E fetch 0x0: AXI Port0 0x1: AXI Port1
17	RESERVED17	
16	CLIENT6	DMA_S fetch 0x0: AXI Port0 0x1: AXI Port1
15	RESERVED15	
14	CLIENT5	DMA_P cursor 0x0: AXI Port0 0x1: AXI Port1
13	RESERVED13	

MDP_XBAR_FIXED_ARB_SEL_RD (cont.)

Bits	Name	Description
12	CLIENT4	DMA_P fetch 0x0: AXI Port0 0x1: AXI Port1
11:7	RESERVED11_7	
6	CLIENT3	RGB 2 pipe 0x0: AXI Port0 0x1: AXI Port1
5	RESERVED5	
4	CLIENT2	RGB 1 pipe 0x0: AXI Port0 0x1: AXI Port1
3	RESERVED3	
2	CLIENT1	Video/Graphics 2 pipe 0x0: AXI Port0 0x1: AXI Port1
1	RESERVED1	
0	CLIENT0	Video/Graphics 1 pipe 0x0: AXI Port0 0x1: AXI Port1

0x05100408 MDP_XBAR_FIXED_ARB_SEL_WR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0004

MDP_XBAR_FIXED_ARB_SEL_WR register selects the AXI master port that will be assigned for each internal write client if the corresponding client is enabled by FIXED_ARB_EN.

NOTE This register should be written only when the corresponding write client is idle or when MDP core is idle.

MDP_XBAR_FIXED_ARB_SEL_WR

Bits	Name	Description
31:3	RESERVED31_3	
2	CLIENT10	Overlay Processor Out Port 1 0x0: AXI Port0 0x1: AXI Port1

MDP_XBAR_FIXED_ARB_SEL_WR (cont.)

Bits	Name	Description
1	RESERVED1	
0	CLIENT9	Overlay Processor Out Port 0 0x0: AXI Port0 0x1: AXI Port1

0x0510040C MDP_XBAR_ARANGE1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The second method is by address range detection. If enabled and the request's address (or start address if it is a burst) is within the programmed range, the request is assigned to the programmed arbiter and this takes priority over the remaining sorting methods. Two ranges may be programmed - where they overlap, range 1 has priority over range 2. Note that only start address is used - be aware of bursts that may cross the end of the address range.

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_ARANGE1

Bits	Name	Description
31:17	RESERVED31_17	This field has no function and should be set to zero for future compatibility
16	ARANGE1_ARB	The arbiter to assign all requests within address range 1. 0x0: AXI Port 0 0x1: AXI Port1
15:11	RESERVED15_11	This field has no function and should be set to zero for future compatibility
10:0	ARANGE1_EN	Enables address range 1 detection, 1 bit per client.

0x05100410 MDP_XBAR_ARANGE1_BASE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_ARANGE1_BASE

Bits	Name	Description
31:0	ARANGE1_BASE	The base address of address range 1.

0x05100414 MDP_XBAR_ARANGE1_HIGH

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_ARANGE1_HIGH

Bits	Name	Description
31:0	ARANGE1_HIGH	The highest address of address range 1.

0x05100418 MDP_XBAR_ARANGE2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_ARANGE2

Bits	Name	Description
31:17	RESERVED31_17	This field has no function and should be set to zero for future compatibility
16	ARANGE2_ARB	The arbiter to assign all requests within address range 2. 0x0: AXI Port 0 0x1: AXI Port1
15:11	RESERVED15_11	This field has no function and should be set to zero for future compatibility
10:0	ARANGE2_EN	Enables address range 2 detection, 1 bit per client.

0x0510041C MDP_XBAR_ARANGE2_BASE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_ARANGE2_BASE

Bits	Name	Description
31:0	ARANGE2_BASE	The base address of address range 2.

0x05100420 MDP_XBAR_ARANGE2_HIGH

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_ARANGE2_HIGH

Bits	Name	Description
31:0	ARANGE2_HIGH	The highest address of address range 2

0x05100424 MDP_XBAR_ABIT_SORT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The third method is by address bit. When enabled, this will select one of two arbiters, based on the value of a particular address bit. This is useful for address range interleaving - for example, if two memory slaves respond to interleaved address ranges of 1KB each, then address bit 10 can be used to sort requests and achieve 1:1 mapping from AXI master to AXI slave. This can also be used to sort based on two large address ranges as long as they can be separated by a power-of-2 address.

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_ABIT_SORT

Bits	Name	Description
31:25	RESERVED31_25	This field has no function and should be set to zero for future compatibility
24:20	ABIT_NUM	Address bit number (0 to 31) to use for sorting requests.
19	RESERVED19	This field has no function and should be set to zero for future compatibility
18	ABIT_VAL_0	The arbiter number (AXI master port) to assign requests which have that address bit equal to zero. 0x0: AXI Port 0 0x1: AXI Port1
17	RESERVED17	This field has no function and should be set to zero for future compatibility
16	ABIT_VAL_1	The arbiter number (AXI master port) to assign requests which have that address bit equal to one. 0x0: AXI Port 0 0x1: AXI Port1
15:11	RESERVED15_11	This field has no function and should be set to zero for future compatibility
10:0	ABIT_SORT_EN	Enables address bit request sorting, 1 bit per client..

0x05100430 MDP_XBAR_IN_RD_LIM_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0808_0808

The maximum number of pending reads from each client is programmed in this register.

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_IN_RD_LIM_0

Bits	Name	Description
31:28	RESERVED31_28	This field has no function and should be set to zero for future compatibility
27:24	CLIENT3_RD_LIM	The maximum number of pending reads from each client. Must be <= the HW parameter that limits the same. Range [0,8]
23:20	RESERVED23_20	This field has no function and should be set to zero for future compatibility
19:16	CLIENT2_RD_LIM	The maximum number of pending reads from each client. Must be <= the HW parameter that limits the same. Range [0,8]

MDP_XBAR_IN_RD_LIM_0 (cont.)

Bits	Name	Description
15:12	RESERVED15_12	This field has no function and should be set to zero for future compatibility
11:8	CLIENT1_RD_LIM	The maximum number of pending reads from each client. Must be <= the HW parameter that limits the same. Range [0,8]
7:4	RESERVED7_4	This field has no function and should be set to zero for future compatibility
3:0	CLIENT0_RD_LIM	The maximum number of pending reads from each client. Must be <= the HW parameter that limits the same. Range [0,8]

0x05100434 MDP_XBAR_IN_RD_LIM_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0808_0808

The maximum number of pending reads from each client is programmed in this register.

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_IN_RD_LIM_1

Bits	Name	Description
31:28	RESERVED31_28	This field has no function and should be set to zero for future compatibility
27:24	CLIENT7_RD_LIM	The maximum number of pending reads from each client. Must be <= the HW parameter that limits the same. Range [0,8]
23:20	RESERVED23_20	This field has no function and should be set to zero for future compatibility
19:16	CLIENT6_RD_LIM	The maximum number of pending reads from each client. Must be <= the HW parameter that limits the same. Range [0,8]
15:12	RESERVED15_12	This field has no function and should be set to zero for future compatibility
11:8	CLIENT5_RD_LIM	The maximum number of pending reads from each client. Must be <= the HW parameter that limits the same. Range [0,8]
7:4	RESERVED7_4	This field has no function and should be set to zero for future compatibility
3:0	CLIENT4_RD_LIM	The maximum number of pending reads from each client. Must be <= the HW parameter that limits the same. Range [0,8]

0x05100438 MDP_XBAR_IN_RD_LIM_2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0008

The maximum number of pending reads from each client is programmed in this register.

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_IN_RD_LIM_2

Bits	Name	Description
31:4	RESERVED31_4	This field has no function and should be set to zero for future compatibility
3:0	CLIENT8_RD_LIM	The maximum number of pending reads from each client. Must be <= the HW parameter that limits the same. Range [0,8]

0x05100440 MDP_XBAR_IN_WR_LIM

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_1010

The maximum number of pending reads from each client is programmed in this register.

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_IN_WR_LIM

Bits	Name	Description
31:13	RESERVED31_13	This field has no function and should be set to zero for future compatibility
12:8	CLIENT10_WR_LIM	The maximum number of pending writes from each client. Must be <= the HW parameter that limits the same. Range [0,16]
7:5	RESERVED7_5	This field has no function and should be set to zero for future compatibility
4:0	CLIENT9_WR_LIM	The maximum number of pending writes from each client. Must be <= the HW parameter that limits the same. Range [0,16]

0x05100450 MDP_XBAR_OUT_RD_LIM

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_1010

The maximum number of pending reads from each arbiter (AXI master port) is programmed in this register.

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_OUT_RD_LIM

Bits	Name	Description
31:13	RESERVED31_13	This field has no function and should be set to zero for future compatibility
12:8	ARB1_RD_LIM	The maximum number of pending reads from Arbiter 1. Must be <= the HW parameter that limits the same. Range [0,16]
7:5	RESERVED7_5	This field has no function and should be set to zero for future compatibility
4:0	ARB0_RD_LIM	The maximum number of pending reads from Arbiter 0. Must be <= the HW parameter that limits the same. Range [0,16]

0x05100454 MDP_XBAR_OUT_WR_LIM

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_1010

The maximum number of pending writes from each arbiter (AXI master port) is programmed in this register.

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_OUT_WR_LIM

Bits	Name	Description
31:13	RESERVED31_13	This field has no function and should be set to zero for future compatibility
12:8	ARB1_WR_LIM	The maximum number of pending writes from Arbiter 1. Must be <= the HW parameter that limits the same. Range [0,16]
7:5	RESERVED7_5	This field has no function and should be set to zero for future compatibility

MDP_XBAR_OUT_WR_LIM (cont.)

Bits	Name	Description
4:0	ARB0_WR_LIM	The maximum number of pending writes from Arbiter 0. Must be <= the HW parameter that limits the same. Range [0,16]

0x05100458 MDP_XBAR_OUT_MAX_BURST

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0808

The maximum burst length for all arbiters (AXI master ports) is programmed in this register.

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_OUT_MAX_BURST

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:8	MAX_WR_BURST	The maximum number of write beats minus 1 (128 bits per beat) allowed on the AXI bus (arbiter outputs). Must be < the HW parameter that limits the same. Range [0,8]
7:4	RESERVED7_4	This field has no function and should be set to zero for future compatibility
3:0	MAX_RD_BURST	The maximum number of read beats minus 1 (128 bits per beat) allowed on the AXI bus (arbiter outputs). Must be < the HW parameter that limits the same. Range [0,8]

0x05100460 MDP_XBAR_ARB_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Each arbiter can be programmed to utilize fixed priority (higher client numbers have higher priority) or last-client-granted (default when fixed priority is not enabled.

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_ARB_CTL

Bits	Name	Description
31:2	RESERVED31_2	This field has no function and should be set to zero for future compatibility
1:0	FIXED_PRIOR_EN	Enables fixed priority arbitration, one bit per arbiter. If enabled, CLIENT_LIM setting is ignored. When disabled, last-client granted scheme is used for arbitration utilizing the CLIENT_LIM.

0x05100464 MDP_XBAR_ARB_FIXED_PRIOR_LIST_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x3584_79A6

The priority list contains a list of client numbers with the highest priority client on the left side (MSBs). The length of the priority list is [43:0] to support 11 clients encoded using 4 bits.

NOTE This register should be written only when MDP is IDLE

MDP_XBAR_ARB_FIXED_PRIOR_LIST_0

Bits	Name	Description
31:0	PRIOR_LIST	Bits[31:0] of the fixed priority list. Default priority - client0 (VG1) > client1(VG1) > client2(RGB1) > client3(RGB2) > client5(DMA_P cursor) > client8(DMA_E cursor) > client4(DMA_P image) > client7(DMA_E image) > client9(Overlay0 write) > client10(Overlay1 write) > client6(DMA_S).

0x05100468 MDP_XBAR_ARB_FIXED_PRIOR_LIST_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0012

The priority list contains a list of client numbers with the highest priority client on the left side (MSBs). The length of the priority list is [43:0] to support 11 clients encoded using 4 bits.

NOTE This register should be written only when MDP is IDLE.

MDP_XBAR_ARB_FIXED_PRIOR_LIST_1

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	PRIOR_LIST	Bits [43:32] of the fixed priority list. Default priority - client0 (VG1) > client1(VG1) > client2(RGB1) > client3(RGB2) > client5(DMA_P cursor) > client8(DMA_E cursor) > client4(DMA_P image) > client7(DMA_E image) > client9(Overlay0 write) > client10(Overlay1 write) > client6(DMA_S).

0x0510046C MDP_XBAR_ARB_CLIENT_LIM_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0xFFFF_FFFF

The maximum number of (consecutive grants - 1) to one client before allowing requests from other clients. This is used for last-client-granted arbitration, but not fixed priority arbitration. NOTE: A client may receive more than this number of consecutive grants if no other clients are making requests to the same arbiter.

NOTE This register should be written only when MDP is IDLE

MDP_XBAR_ARB_CLIENT_LIM_0

Bits	Name	Description
31:28	CLIENT7_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]
27:24	CLIENT6_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]
23:20	CLIENT5_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]
19:16	CLIENT4_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]
15:12	CLIENT3_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]
11:8	CLIENT2_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]
7:4	CLIENT1_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]
3:0	CLIENT0_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]

0x05100470 MDP_XBAR_ARB_CLIENT_LIM_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0FFF

The maximum number of (consecutive grants - 1) to one client before allowing requests from other clients. This is used for last-client-granted arbitration, but not fixed priority arbitration. NOTE: A client may receive more than this number of consecutive grants if no other clients are making requests to the same arbiter.

NOTE This register should be written only when MDP is IDLE

MDP_XBAR_ARB_CLIENT_LIM_1

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:8	CLIENT10_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]
7:4	CLIENT9_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]
3:0	CLIENT8_LIM	The maximum number of (consecutive grants - 1) to a client before allowing requests from other clients. Range [0, 15]

0x05100480 MDP_XBAR_AXI_AOOORD

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_01FF

When a request is granted by the arbiter, AOOORD signal (AXI r0p0++) may be controlled on a per-client basis.

NOTE This register should be written only when MDP is IDLE

MDP_XBAR_AXI_AOOORD

Bits	Name	Description
31:9	RESERVED31_9	This field has no function and should be set to zero for future compatibility
8:0	AXI_AOOORD	"Out of order" enable for reads, one bit per read client. If zero, the AXI bus and slaves must ensure that all reads from that client are completed in the order they are requested from the client.

0x05100484 MDP_XBAR_AXI_AOOOWR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0003

When a request is granted by the arbiter, AOOOWR signal (AXI r0p0++) may be controlled on a per-client basis.

NOTE This register should be written only when MDP is IDLE

MDP_XBAR_AXI_AOOOWR

Bits	Name	Description
31:2	RESERVED31_2	This field has no function and should be set to zero for future compatibility
1:0	AXI_AOOOWR	"Out of order" enable for writes, one bit per write client. If zero, the AXI bus and slaves must ensure that all writes from this client are completed in the order they are requested from the client.

0x05100488 MDP_XBAR_AXI_ATYPE_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x6666_6666

When a request is granted by the arbiter, ATYPE signal (AXI r0p0++) may be controlled on a per-client basis. ATYPE indicates the memory type and attributes of an access.

NOTE This register should be written only when MDP is IDLE

MDP_XBAR_AXI_ATYPE_0

Bits	Name	Description
31:0	AXI_ATYPE	The value to drive on ATYPE signal, 4 bits per client. Probably one of these: 0x4: Normal, Non-cacheable, Non-shared 0x6: Normal, Cacheable, Writeback, Write-allocate, Non-shared 0x7: Normal, Cacheable, Writeback, Write-allocate, Shared

0x0510048C MDP_XBAR_AXI_ATYPE_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0666

When a request is granted by the arbiter, ATYPE signal (AXI r0p0++) may be controlled on a per-client basis. ATYPE indicates the memory type and attributes of an access.

NOTE This register should be written only when MDP is IDLE

MDP_XBAR_AXI_ATYPE_1

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	AXI_ATYPE	The value to drive on ATYPE signal, 4 bits per client. Probably one of these: 0x4: Normal, Non-cacheable, Non-shared 0x6: Normal, Cacheable, Writeback, Write-allocate, Non-shared 0x7: Normal, Cacheable, Writeback, Write-allocate, Shared

0x05100490 MDP_XBAR_AXI_AREQPRIORITY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00AA

When a request is granted by the arbiter, AREQPRIORITY signal (AXI r0p0++) may be controlled on a per-client basis.

NOTE This register should be written only when MDP is IDLE

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MDP_XBAR_AXI_AREQPRIORITY

Bits	Name	Description
31:22	RESERVED31_22	This field has no function and should be set to zero for future compatibility

MDP_XBAR_AXI_AREQPRIORITY (cont.)

Bits	Name	Description
21:0	AXI_AREQPRIORITY	Request priority, 2 bits per client. This value is driven onto AXI bus only, not used internally for client arbitration. These two bits of relative priority can be decoded as shown below. NOTE: By default, `higher' priority has been assigned for RGB1/2 and VG1/2 assuming direct-out mode is the most common mode of operation. 0x0: normal 0x1: high 0x2: higher 0x3: highest

0x05100494 MDP_XBAR_AXI_APROTNS

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

NOTE This register is RESERVED. AXI signal `aprotns' is tied to one (non-secure) at MMSS level for both MDP4 AXI ports. This tie in MMSS overrides the value set by this register.

MDP_XBAR_AXI_APROTNS

Bits	Name	Description
31:11	RESERVED31_11	This field has no function and should be set to zero for future compatibility
10:0	AXI_APROTNS	(RESERVED) Enable "non-secure" bus access, one bit per client. If zero, the corresponding client accesses are secure accesses.

0x051004B0 MDP_XBAR_AXI_ERROR_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

NOTE This register's parameters should be written only when MDP is IDLE unless otherwise specified.

MDP_XBAR_AXI_ERROR_CTL

Bits	Name	Description
31:10	RESERVED31_10	This field has no function and should be set to zero for future compatibility
9:8	AXI_ERR_CLR	One bit per AXI master port. When AXI error occurs, SW can read the error info and then can assert this bit to clear the AXI error and enable next AXI error to be captured. Note: Write `1' and then `0' when corresponding AXI Port error interrupt is received.
7:6	RESERVED7_6	This field has no function and should be set to zero for future compatibility
5:4	AXI_HALT_ON_WR_ERR	One bit per AXI master port. When set (1), a write error response from AXI (on bresp) acts like a HALT_REQ and also disables all ARB-XIN interfaces - instead, fake write data to AXI (zero write enables) and discard read data from AXI. SW should wait for AXI_IDLE (or HALT_ACK) and then reset the core.
3:2	RESERVED3_2	This field has no function and should be set to zero for future compatibility
1:0	AXI_HALT_ON_RD_ERR	One bit per AXI master port. When set (1), a read error response from AXI (on rresp) acts like a HALT_REQ and also disables all ARB-XIN interfaces - instead, fake write data to AXI (zero write enables) and discard read data from AXI. SW should wait for AXI_IDLE (or HALT_ACK) and then reset the core.

0x051004B4 MDP_XBAR_AXI_PORT0_ERROR_INFO

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

NOTE The contents of this register are valid (for read) only when AXI Port0 error interrupt is received.

MDP_XBAR_AXI_PORT0_ERROR_INFO

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11	AXI_ERR	Indicates than an AXI error occurred since the last AXI reset. The AXI error interrupt status may be more useful than this bit.
10	AXI_ERR_TYPE	The type of the last error that occurred. 0x0: axi_rresp 0x1: axi_bresp (has priority over rresp if happen same time)

MDP_XBAR_AXI_PORT0_ERROR_INFO (cont.)

Bits	Name	Description
9:8	AXI_RESP	The value of axi_rresp or axi_bresp when the last error occurred.
7:4	AXI_MID	The value on axi_rmid or axi_bmid when the last error occurred.
3:0	AXI_TID	The value on axi_rtid or axi_btid when the last error occurred.

0x051004B8 MDP_XBAR_AXI_PORT1_ERROR_INFO

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

NOTE The contents of this register are valid (for read) only when AXI Port1 error interrupt is received.

MDP_XBAR_AXI_PORT1_ERROR_INFO

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11	AXI_ERR	Indicates than an AXI error occurred since the last AXI reset. The AXI error interrupt status may be more useful than this bit.
10	AXI_ERR_TYPE	The type of the last error that occurred. 0x0: axi_rresp 0x1: axi_bresp (has priority over rresp if happen same time)
9:8	AXI_RESP	The value of axi_rresp or axi_bresp when the last error occurred.
7:4	AXI_MID	The value on axi_rmid or axi_bmid when the last error occurred.
3:0	AXI_TID	The value on axi_rtid or axi_btid when the last error occurred.

0x051004C4 MDP_XBAR_AXI_WDATA_TIMEOUT_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00F0

NOTE This register should be written only when MDP is IDLE

MDP_XBAR_AXI_WDATA_TIMEOUT_CTL

Bits	Name	Description
31:8	RESERVED31_8	This field has no function and should be set to zero for future compatibility
7:4	WDTIMEOUT_LOG2	Bit number of the 16-bit time waiting counter that indicates timeout.
3:2	RESERVED3_2	This field has no function and should be set to zero for future compatibility
1:0	AXI_HALT_WDTIMEOUT	One bit per AXI master port. When set (1), this will generate a "halt" (similar to HALT_ON_WR_ERR) if the core is not able to provide a write data burst to AXI within a SW specified time after the previous write data burst was sent. This is either because client does not provide write data fast enough or AXI is not accepting write data fast enough.

0x051004C8 MDP_XBAR_AXI_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0003

MDP_XBAR_AXI_STATUS

Bits	Name	Description
31:6	RESERVED31_6	This field has no function and should be set to zero for future compatibility
5:4	WDATA_TIMEOUT_HALT	Indicates that AXI halt occurred because of write data timeout. Once asserted will remain high till AXI reset. One bit per AXI master port.
3:2	RESERVED3_2	This field has no function and should be set to zero for future compatibility
1:0	AXI_IDLE	Indicates that the AXI master port is idle (no pending requests on AXI). One bit per AXI master port.

0x051004D0 MDP_XBAR_AXI_PROFILE_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Each arbiter includes bandwidth counters, min & max latency counters, a MISR for capturing AXI write data, and an LFSR for generating AXI read data (faking the response from AXI slaves).

NOTE This register should be written only when MDP is IDLE

MDP_XBAR_AXI_PROFILE_CTL

Bits	Name	Description
31:26	RESERVED31_26	This field has no function and should be set to zero for future compatibility
25:24	RD_LAT_REP_EN	1 bit per arb. when enabled, each beat of read data is replaced with the read access latency (of AXI cycles from request till read data returned)
23:18	RESERVED23_18	This field has no function and should be set to zero for future compatibility
17:16	MISR_RES	1 bit per arb, to reset MISR Note: Write `1' and then `0' to reset MISR corresponding to an arbiter.
15:14	RESERVED15_14	This field has no function and should be set to zero for future compatibility
13:12	MISR_EN	1 bit per arb
11:10	RESERVED11_10	This field has no function and should be set to zero for future compatibility
9:8	MISR_WD	1 bit per arb, to select misr input 0x0: read data (coming back from AXI) 0x1: write data (going to AXI)
7	CTR_EN	Enable all profiling counters
6	CTR_RES	Reset all profiling counters (they are also reset by AXI_RESET). Note: Write `1' and then `0' to reset all profiling counters.
5	RESERVED5	This field has no function and should be set to zero for future compatibility
4	TEST_ARB_SEL	Select which arbiter will drive MDP_AXI_PROFILE_OUT. 0x0: Arbiter 0 0x1: Arbiter 1

MDP_XBAR_AXI_PROFILE_CTL (cont.)

Bits	Name	Description
3:0	TEST_OUT_SEL	Select which profile data is read via MDP_AXI_PROFILE_OUT. 0x0: num read bursts (32 bits) 0x1: total read BW (32 bits - up to 68GB) 0x2: max outstanding reads (8 bits) 0x3: avg wait for read accept (10 bits over 128 reads) 0x4: min read latency (16 bits) 0x5: max read latency (16 bits) 0x6: avg read latency (16 bits over 1K read beats) 0x8: num write bursts (32 bits) 0x9: total write BW (32 bits - up to 68GB) 0xA: max outstanding writes (8 bits) 0xB: avg wait for write accept (10 bits over 128 writes) 0xC: MISR signature word 0 0xD: MISR signature word 1 0xE: MISR signature word 2 0xF: MISR signature word 3

0x051004D4 MDP_XBAR_AXI_PROFILE_OUT

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

NOTE The contents of this register are valid (for read) when MDP is IDLE or when the arbiter (AXI Port) selected for profiling is IDLE.

MDP_XBAR_AXI_PROFILE_OUT

Bits	Name	Description
31:0	AXI_TEST_OUT	The output selected by MDP_AXI_PROFILE_CTL reg.

14.15.12 Overlay Processor registers

0x05110000 MDP_OVERLAY_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

Indicates internal idle state of the Overlay Processor.

MDP_OVERLAY_STATUS

Bits	Name	Description
31:9	RESERVED31_9	
8	OVERLAYPROC2_IDLE	Overlay Processor output port 2 path is idle.
7	RGB3_IDLE	RGB3 input pipe idle.
6	RGB2_IDLE	RGB2 input pipe is idle.
5	RGB1_IDLE	RGB1 input pipe is idle.
4	VG3_IDLE	Video/Graphisc3 input pipe idle.
3	VG2_IDLE	Video/Graphisc2 input pipe is idle.
2	VG1_IDLE	Video/Graphisc1 input pipe is idle.
1	OVERLAYPROC1_IDLE	Overlay Processor output port 1 path is idle.
0	OVERLAYPROC0_IDLE	Overlay Processor output port 0 path is idle.

0x051100F0 MDP_LAYERMIXER2_IN_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register describes the input connections to Layer Mixer2. This is Double Buffered. The relevant value is shadowed at every refresh initiation of the associated Overlay Processor for internal used. For example, if VG1 pipe is set to be an input, the selection will be registered at the next Overlay Processor's refresh initiation.

NOTE Connecting multiple pipes' output to the same single Layer Mixer layer's input is prohibited. If by mistake that multiple pipes are connected to the same layer, the most significant field takes priority, i.e., in the order of VG3, RGB3, RGB2, RGB1, VG2, and VG1.

The onus is on SW to prevent duplicate connections of pipelines between source pipelines to LayerMixer2 and LayerMixer0/1. As such care should be taken to correctly MDP_LAYERMIXER2_IN_CFG in relation to MDP_LAYERMIXER_IN_CFG

MDP_LAYERMIXER2_IN_CFG

Bits	Name	Description
31:28	RESERVED31_24	
27:24	BORDER_OUT	LayerMixer2 Border pipe output connection. Others: Reserved 0x0: This pipe is not used 0x9: LayerMixer2 Base layer

MDP_LAYERMIXER2_IN_CFG (cont.)

Bits	Name	Description
23:16	RESERVED23_16	
15:12	RGB2_OUT	RGB 2 pipe output connection 0x0: This pipe is not used 0x9: LayerMixer2 Base layer 0xA: LayerMixer2 Stage 0 FG layer 0xB: LayerMixer2 Stage 1 FG layer 0xC: LayerMixer2 Stage 2 FG layer 0xD: LayerMixer2 Stage 3 FG layer
11:8	RGB1_OUT	RGB 1 pipe output connection 0x0: This pipe is not used 0x9: LayerMixer2 Base layer 0xA: LayerMixer2 Stage 0 FG layer 0xB: LayerMixer2 Stage 1 FG layer 0xC: LayerMixer2 Stage 2 FG layer 0xD: LayerMixer2 Stage 3 FG layer
7:4	VG2_OUT	Video/Graphics 2 pipe output connection 0x0: This pipe is not used 0x9: LayerMixer2 Base layer 0xA: LayerMixer2 Stage 0 FG layer 0xB: LayerMixer2 Stage 1 FG layer 0xC: LayerMixer2 Stage 2 FG layer 0xD: LayerMixer2 Stage 3 FG layer
3:0	VG1_OUT	Video/Graphics 1 pipe output connection 0x0: This pipe is not used 0x9: LayerMixer2 Base layer 0xA: LayerMixer2 Stage 0 FG layer 0xB: LayerMixer2 Stage 1 FG layer 0xC: LayerMixer2 Stage 2 FG layer 0xD: LayerMixer2 Stage 3 FG layer

0x051100F4 MDP_LAYERMIXER_WB_MUX_SEL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Indicates internal idle state of the Overlay Processor.

MDP_LAYERMIXER_WB_MUX_SEL

Bits	Name	Description
31:2	RESERVED31_2	

MDP_LAYERMIXER_WB_MUX_SEL (cont.)

Bits	Name	Description
1	LMIX1_WB_SEL	LayerMixer2 output path connection 0x0: LayerMixer1 is connected to LayerMixer1's AXI writeback path 0x1: LayerMixer2 is connected to LayerMixer1's AXI writeback path
0	LMIX0_WB_SEL	LayerMixer2 output path connection 0x0: LayerMixer0 is connected to LayerMixer0's AXI writeback path 0x1: LayerMixer2 is connected to LayerMixer0's AXI writeback path

0x051100FC MDP_LAYERMIXER_IN_CFG_UPDATE_METHOD

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

.MDP4 assumes layermixer configuration(MDP_LAYERMIXER_IN_CFG) and register flush control (MDP_OVERLAY_REG_FLUSH) are written within same frame but it can't be guaranteed at some circumstance. In MDP4.2, new update method is introduced for the above case but SW should do dummy write at MDP_OVERLAY_REG_FLUSH for smart panel case after changing MDP_LAYERMIXER_IN_CFG, which are not really required for smart panel.

When SW do dummy write on MDP_OVERLAY_REG_FLUSH, the write value should be all zero which does not affect anything.

For dumb panel case, SW shouldn't do any dummy write and just write MDP_OVERLAY_REG_FLUSH when SW wants to do.

MDP_LAYERMIXER_IN_CFG_UPDATE_METHOD

Bits	Name	Description
31:1	RESERVED31_1	
0	NEW_UPDATE_METHOD	Controls MDP_LAYERMIXER_IN_CFG(ox10100) update method 0x0(default) : Update MDP_LAYERMIXER_IN_CFG when SW writes it. (same to mdp4.0/1 behavior) 0x1: Update MDP_LAYERMIXER_IN_CFG when SW writes MDP_OVERLAY_REG_FLUSH (0x18000. SW should do dummy write at MDP_OVERLAY_REG_FLUSH even for smart panel.)

0x05110100 MDP_LAYERMIXER_IN_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register describes the input connections to the Layer Mixers. This is Double Buffered. The relevant value is shadowed at every refresh initiation of the associated Overlay Processor for internal used. For example, if VG1 pipe is set to be an Layer Mixer 0 input, the selection will be registered at the next Overlay Processor 0's refresh initiation.

NOTE Connecting multiple pipes' output to the same single Layer Mixer layer's input is prohibited. If by mistake that multiple pipes are connected to the same layer, the most significant field takes priority, i.e., in the order of VG3, RGB3, RGB2, RGB1, VG2, and VG1.

MDP_LAYERMIXER_IN_CFG

Bits	Name	Description
31:24	RESERVED31_24	
23:20	VG3_OUT	Video/Graphics 3 pipe output connection. Border Color (LayerMixer1) pipe output connection This border color can only be used with LayerMixer1. Others: Reserved 0x0: This pipe is not used 0x9: LayerMixer1 Base layer
19:16	RGB3_OUT	Border Color (LayerMixer0) pipe output connection This border color can only be used withLayerMixer0. Others: Reserved 0x0: This pipe is not used 0x1: LayerMixer0 Base layer
15:12	RGB2_OUT	RGB 2 pipe output connection 0x0: This pipe is not used 0x1: LayerMixer0 Base layer 0x2: LayerMixer0 Stage 0 FG layer 0x3: LayerMixer0 Stage 1 FG layer 0x4: LayerMixer0 Stage 2 FG layer 0x5: LayerMixer0 Stage 3 FG layer 0x9: LayerMixer1 Base layer 0xA: LayerMixer1 Stage 0 FG layer 0xB: LayerMixer1 Stage 1 FG layer 0xC: LayerMixer1 Stage 2 FG layer 0xD: LayerMixer1 Stage 3 FG layer

MDP_LAYERMIXER_IN_CFG (cont.)

Bits	Name	Description
11:8	RGB1_OUT	RGB 1 pipe output connection 0x0: This pipe is not used 0x1: LayerMixer0 Base layer 0x2: LayerMixer0 Stage 0 FG layer 0x3: LayerMixer0 Stage 1 FG layer 0x4: LayerMixer0 Stage 2 FG layer 0x5: LayerMixer0 Stage 3 FG layer 0x9: LayerMixer1 Base layer 0xA: LayerMixer1 Stage 0 FG layer 0xB: LayerMixer1 Stage 1 FG layer 0xC: LayerMixer1 Stage 2 FG layer 0xD: LayerMixer1 Stage 3 FG layer
7:4	VG2_OUT	Video/Graphics 2 pipe output connection 0x0: This pipe is not used 0x1: LayerMixer0 Base layer 0x2: LayerMixer0 Stage 0 FG layer 0x3: LayerMixer0 Stage 1 FG layer 0x4: LayerMixer0 Stage 2 FG layer 0x5: LayerMixer0 Stage 3 FG layer 0x9: LayerMixer1 Base layer 0xA: LayerMixer1 Stage 0 FG layer 0xB: LayerMixer1 Stage 1 FG layer 0xC: LayerMixer1 Stage 2 FG layer 0xD: LayerMixer1 Stage 3 FG layer
3:0	VG1_OUT	Video/Graphics 1 pipe output connection 0x0: This pipe is not used 0x1: LayerMixer0 Base layer 0x2: LayerMixer0 Stage 0 FG layer 0x3: LayerMixer0 Stage 1 FG layer 0x4: LayerMixer0 Stage 2 FG layer 0x5: LayerMixer0 Stage 3 FG layer 0x9: LayerMixer1 Base layer 0xA: LayerMixer1 Stage 0 FG layer 0xB: LayerMixer1 Stage 1 FG layer 0xC: LayerMixer1 Stage 2 FG layer 0xD: LayerMixer1 Stage 3 FG layer

0x05118000 MDP_OVERLAY_REG_FLUSH

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The flush register is used to indicate a pipe/layermixer's registers are all programmed, and are safe to update to the back copy of the double buffered registers. Each pipes/layermixer's flush mask bit will be used only when the associated pipe/layermixer is running at active refresh pull mode, e.g., direct out going to dsi video. In such operation mode, the associated pipe/layermixer's double buffered registers' back copies are updated with the new values at the vsync boundary only when the flush mask bit has already been written a '1'. Each flush mask bit would also returned a `0' once the back copies are updated. Before the back copies are updated, the associate mask bit would returned a `1' if it has been previously written a `1'.

MDP_OVERLAY_REG_FLUSH

Bits	Name	Description
31:8	RESERVED31_8	
7	RESERVED7	Reserved for future VG3 input pipe
6	RESERVED6	Reserved for future RGB3 input pipe
5	RGB2	Set to indicate RGB2 input pipe registers are ready for flush.
4	RGB1	Set to indicate RGB1 input pipe registers are ready for flush.
3	VG2	Set to indicate VG2 input pipe registers are ready for flush.
2	VG1	Set to indicate VG1 input pipe registers are ready for flush.
1	LAYERMIX1	Set to indicate Layer Mixer 1 registers are ready for flush.
0	LAYERMIX0	Set to indicate Layer Mixer 0 registers are ready for flush.

14.15.12.1 Layer Mixer 0

0x05110004 MDP_OVERLAYPROC0_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0003

This register configures the OVERLAY PROCESSOR 0's starting behavior. When the DIRECT_OUT is set, the input pipes that are assigned to this processor will be initiated by the active refresh if the interface selected is dsi video, regardless refresh_mode selection. If going through a Frame Buffer, the pipes for the Overlay Processor can be kick-started by the REFRESH_MODE selected. The value only take effect at the next refresh initiation of the Overlay Processor 0. However, it is not recommended to switch Overlay Processor's mode of operation at tun time, the switch should be done only when an Overlay Processor and its associated interface are in idle.

MDP_OVERLAYPROC0_CFG

Bits	Name	Description
31:6	RESERVED31_6	

MDP_OVERLAYPROC0_CFG (cont.)

Bits	Name	Description
5	CON_WB_MODE	RESERVED.
4	CON_WB_EN	Concurrent display and write back mode selection. Only valid when not in BLT mode and when DIRECT_OUT is 1. 0x0: Disabled 0x1: Enabled
3	BLT_MODE	Puts this Overlay Processor into BLT (MDP3) type of SW operation mode, which means both the Overlay Processor 0 and DMA_P fetch will be fully controlled by the SW. There will be no passing of Frame Buffer pointers between the Overlay Processor 0 and DMA_P. This setting takes priority over REFRESH_MODE and DIRECT_OUT settings.
2:1	REFRESH_MODE	Overlay Processor refresh mode (only valid when not in BLT mode and not in direct-out mode, otherwise don't care): 0x0: On-Demand (software initiated, FrameBuffer push or Direct Out push for smart panel) 0x1: Vsync rate (FrameBuffer pull) 0x2: Vsync/2 rate (FrameBuffer pull) 0x3: Vsync/4 rate (FrameBuffer pull)
0	DIRECT_OUT	Overlay Processor output direction select (only valid when not in BLT mode, otherwise don't care): 0x0: Via FrameBuffer 0x1: Direct to interface (internally refresh_mode is forced to Vsync rate if connected to DSI_VIDEO/LCDC)

0x05110008 MDP_OVERLAYPROC0_OUT_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0020_0020

This register designates the output size of the Overlay Processor 0 and is also used as the Frame Buffer/Active Region size for DMA_P.

MDP_OVERLAYPROC0_OUT_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DST_H	Output ROI height (pixel).
15:12	RESERVED15_12	
11:0	DST_W	Output ROI width (pixel).

0x0511000C MDP_OVERLAYPROC0_FB_ADDR1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This is the 1st Frame Buffer base address (for ping-ponging) that is used when this Overlay Processor is in Frame Buffer mode, where the value is registered and used at every other frame initiation of this Overlay Processor. In other modes, this is the only effective Frame Buffer base address used, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC0_FB_ADDR1

Bits	Name	Description
31:0	ADDR	Starting base byte address for Frame Buffer

0x05110010 MDP_OVERLAYPROC0_FB_Y_STRIDE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_FB_Y_STRIDE register defines the line jump value (in bytes) in the Frame Buffer.

MDP_OVERLAYPROC0_FB_Y_STRIDE

Bits	Name	Description
31:13	RESERVED31_13	
12:0	BUF_Y_STRIDE	Y-stride (or) line jump in bytes in the Frame Buffer.

0x05110014 MDP_OVERLAYPROC0_OPMODE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The FB_FORMAT field is also used by DMA_P to decipher what Frame Buffer format to fetch in FrameBuffer Pull mode of operation.

MDP_OVERLAYPROC0_OPMODE

Bits	Name	Description
31	BYPASS_COLOR3_EN	Enables propagation of color component 3 to the packer 0x1: color3 is taken from register 0x0: color3 is propagated from the pipe
30:3	RESERVED30_3	RESERVED
2	PGC_EN	Panel Gamma Correction enable. If disabled, the colors are mapped linearly from 12-bit to 8-bit.
1:0	FB_FORMAT	This field actually controls memory write back pixel format in LM0 with regard to operation mode (direct with concurrent write back, FB or BLT). If the concurrent write back is enabled, only RGB888 is supported. 0x0: RGB888 0x1: RGB565 0x2: Reserved

0x0511001C MDP_OVERLAYPROC0_FB_ADDR2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This is the 2nd Frame Buffer base address (for ping-ponging) that is used only when this Overlay Processor is in Frame Buffer mode. The value is registered and used at every other frame initiation of this Overlay Processor.

MDP_OVERLAYPROC0_FB_ADDR2

Bits	Name	Description
31:0	ADDR	Starting base byte address for Frame Buffer

0x05110020 MDP_OVERLAYPROC0_PROFILE_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_PROFILE_EN

Bits	Name	Description
31:1	RESERVED31_1	
0	EN	Enable the ROI cycle counter for profiling

0x05110024 MDP_OVERLAYPROC0_PROFILE_COUNT

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_PROFILE_COUNT

Bits	Name	Description
31:24	RESERVED31_24	
23:0	TOTAL_CYCLE	Total cycle count in a ROI, from new ROI to last pixel out of the processor (OVERLAYPROC0 goes back to Idle)

0x05110104 MDP_OVERLAYPROC0_BLEND0_OP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

This register describes the blend operation done by Layer Mixer 0 on Stage 0 FG/BG, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC0_BLEND0_OP

Bits	Name	Description
31:10	RESERVED31_10	
9	BG_TRANSP_EN	BG transparency color check enable. When color matches, the FG pixel is passed; otherwise, the blended result is passed. However, if both FG and BG Transparency checks are enabled and both matches, BG pixel is passed.
8	FG_TRANSP_EN	FG transparency color check enable. When color matches, the BG pixel is passed; otherwise, the blended result is passed.
7	BG_MOD_ALPHA	When set (1), bg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
6	BG_INV_ALPHA	When set (1) the alpha selected by BG_ALPHA_SEL is inverted (1-alpha).
5:4	BG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha
3	FG_MOD_ALPHA	When set (1), fg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.

MDP_OVERLAYPROC0_BLEND0_OP (cont.)

Bits	Name	Description
2	FG_INV_ALPHA	When set (1) the alpha selected by FG_ALPHA_SEL is inverted (1-alpha).
1:0	FG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha

0x05110108 MDP_OVERLAYPROC0_BLEND0_FG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC0_BLEND0_FG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x0511010C MDP_OVERLAYPROC0_BLEND0_BG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC0_BLEND0_BG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x05110110 MDP_OVERLAYPROC0_BLEND0_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND0_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05110114 MDP_OVERLAYPROC0_BLEND0_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND0_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05110118 MDP_OVERLAYPROC0_BLEND0_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND0_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x0511011C MDP_OVERLAYPROC0_BLEND0_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND0_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05110124 MDP_OVERLAYPROC0_BLEND1_OP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

This register describes the blend operation done by Layer Mixer 0 on Stage 1 FG/BG, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC0_BLEND1_OP

Bits	Name	Description
31:10	RESERVED31_10	
9	BG_TRANSP_EN	BG transparency color check enable. When color matches, the FG pixel is passed; otherwise, the blended result is passed. However, if both FG and BG Transparency checks are enabled and both matches, BG pixel is passed.
8	FG_TRANSP_EN	FG transparency color check enable. When color matches, the BG pixel is passed; otherwise, the blended result is passed.
7	BG_MOD_ALPHA	When set (1), bg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
6	BG_INV_ALPHA	When set (1) the alpha selected by BG_ALPHA_SEL is inverted (1-alpha).
5:4	BG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha
3	FG_MOD_ALPHA	When set (1), fg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
2	FG_INV_ALPHA	When set (1) the alpha selected by FG_ALPHA_SEL is inverted (1-alpha).

MDP_OVERLAYPROC0_BLEND1_OP (cont.)

Bits	Name	Description
1:0	FG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha

0x05110128 MDP_OVERLAYPROC0_BLEND1_FG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC0_BLEND1_FG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x0511012C MDP_OVERLAYPROC0_BLEND1_BG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC0_BLEND1_BG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x05110130 MDP_OVERLAYPROC0_BLEND1_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND1_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05110134 MDP_OVERLAYPROC0_BLEND1_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND1_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05110138 MDP_OVERLAYPROC0_BLEND1_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND1_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x0511013C MDP_OVERLAYPROC0_BLEND1_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND1_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05110144 MDP_OVERLAYPROC0_BLEND2_OP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

This register describes the blend operation done by Layer Mixer 0 on Stage 2 FG/BG,, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC0_BLEND2_OP

Bits	Name	Description
31:10	RESERVED31_10	
9	BG_TRANSP_EN	BG transparency color check enable. When color matches, the FG pixel is passed; otherwise, the blended result is passed. However, if both FG and BG Transparency checks are enabled and both matches, BG pixel is passed.
8	FG_TRANSP_EN	FG transparency color check enable. When color matches, the BG pixel is passed; otherwise, the blended result is passed.
7	BG_MOD_ALPHA	When set (1), bg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
6	BG_INV_ALPHA	When set (1) the alpha selected by BG_ALPHA_SEL is inverted (1-alpha).
5:4	BG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha
3	FG_MOD_ALPHA	When set (1), fg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
2	FG_INV_ALPHA	When set (1) the alpha selected by FG_ALPHA_SEL is inverted (1-alpha).

MDP_OVERLAYPROC0_BLEND2_OP (cont.)

Bits	Name	Description
1:0	FG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha

0x05110148 MDP_OVERLAYPROC0_BLEND2_FG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC0_BLEND2_FG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x0511014C MDP_OVERLAYPROC0_BLEND2_BG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC0_BLEND2_BG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x05110150 MDP_OVERLAYPROC0_BLEND2_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND2_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05110154 MDP_OVERLAYPROC0_BLEND2_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND2_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05110158 MDP_OVERLAYPROC0_BLEND2_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND2_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x0511015C MDP_OVERLAYPROC0_BLEND2_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND2_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05110160 MDP_OVERLAYPROC0_BLEND3_OP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

This register describes the blend operation done by Layer Mixer 0 on Stage 0 FG/BG, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC0_BLEND3_OP

Bits	Name	Description
31:10	RESERVED31_10	
9	BG_TRANSP_EN	BG transparency color check enable. When color matches, the FG pixel is passed; otherwise, the blended result is passed. However, if both FG and BG Transparency checks are enabled and both matches, BG pixel is passed.
8	FG_TRANSP_EN	FG transparency color check enable. When color matches, the BG pixel is passed; otherwise, the blended result is passed.
7	BG_MOD_ALPHA	When set (1), bg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
6	BG_INV_ALPHA	When set (1) the alpha selected by BG_ALPHA_SEL is inverted (1-alpha).
5:4	BG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha
3	FG_MOD_ALPHA	When set (1), fg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
2	FG_INV_ALPHA	When set (1) the alpha selected by FG_ALPHA_SEL is inverted (1-alpha).

MDP_OVERLAYPROC0_BLEND3_OP (cont.)

Bits	Name	Description
1:0	FG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha

0x05110164 MDP_OVERLAYPROC0_BLEND3_FG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC0_BLEND3_FG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x05110168 MDP_OVERLAYPROC0_BLEND3_BG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC0_BLEND3_BG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x0511016C MDP_OVERLAYPROC0_BLEND3_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND3_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05110170 MDP_OVERLAYPROC0_BLEND3_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND3_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05110174 MDP_OVERLAYPROC0_BLEND3_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND3_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x05110178 MDP_OVERLAYPROC0_BLEND3_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND3_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05110180 MDP_OVERLAYPROC0_BG_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BG_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05110184 MDP_OVERLAYPROC0_BG_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BG_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05110188 MDP_OVERLAYPROC0_BG_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BG_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x0511018C MDP_OVERLAYPROC0_BG_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BG_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05111000 MDP_OVERLAYPROC0_BLEND0_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000a

MDP_OVERLAYPROC0_BLEND0_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	Internal idles and valids

0x05111004 MDP_OVERLAYPROC0_BLEND0_COLOR3_OUT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND0_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED31_1	
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x05111400 MDP_OVERLAYPROC0_BLEND1_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000a

MDP_OVERLAYPROC0_BLEND1_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	Internal idles and valids

0x05111404 MDP_OVERLAYPROC0_BLEND1_COLOR3_OUT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND1_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED31_1	
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x05111800 MDP_OVERLAYPROC0_BLEND2_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000a

MDP_OVERLAYPROC0_BLEND2_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	Internal idles and valids

0x05111804 MDP_OVERLAYPROC0_BLEND2_COLOR3_OUT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND2_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED31_1	
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x05111C00 MDP_OVERLAYPROC0_BLEND3_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000a

MDP_OVERLAYPROC0_BLEND3_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	Internal idles and valids

0x05111C04 MDP_OVERLAYPROC0_BLEND3_COLOR3_OUT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC0_BLEND3_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED31_1	
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x05114800+ 4*n MDP_OVERLAYPROC0_GC_START_COLOR_0_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component0

MDP_OVERLAYPROC0_GC_START_COLOR_0_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable. typically most of Gamma curve in panel doesn't need all 16stage linear curve that unsed stages have to be programmed to disable stage.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value. each stage start value intends to get input data between 0 and4096 and start value has to be programmed incremental way for 16 stages that for example, stage1 start value has to bigger than stage 0 start value.

0x05114880+ 4*n MDP_OVERLAYPROC0_GC_PARAM_COLOR_0_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component0

MDP_OVERLAYPROC0_GC_PARAM_COLOR_0_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7)
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U3.12)

0x05114900+ 4*n MDP_OVERLAYPROC0_GC_START_COLOR_1_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component1

MDP_OVERLAYPROC0_GC_START_COLOR_1_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x05114980+ 4*n MDP_OVERLAYPROC0_GC_PARAM_COLOR_1_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component1

MDP_OVERLAYPROC0_GC_PARAM_COLOR_1_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset(U8.7)
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U3.12)

0x05114A00+ 4*n MDP_OVERLAYPROC0_GC_START_COLOR_2_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component2

MDP_OVERLAYPROC0_GC_START_COLOR_2_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x05114A80+ 4*n MDP_OVERLAYPROC0_GC_PARAM_COLOR_2_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component2

MDP_OVERLAYPROC0_GC_PARAM_COLOR_2_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U3.12)

0x05115004 MDP_OVERLAYPROC0_LSP_BORDER_COLOR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Least Significant Portion (lower 24 bits of total 36 bits) of border color values

MDP_OVERLAYPROC0_LSP_BORDER_COLOR

Bits	Name	Description
31:28	RESERVED31_28	
27:16	BORDER_COLOR1	Border color value for color 1
15:12	RESERVED15_12	
11:0	BORDER_COLOR0	Border color value for color 0

0x05115008 MDP_OVERLAYPROC0_MSP_BORDER_COLOR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Most Significant Portion (upper 12 bits of total 36 bits) of border color values

MDP_OVERLAYPROC0_MSP_BORDER_COLOR

Bits	Name	Description
31:12	RESERVED31_12	
11:0	BORDER_COLOR2	Border color value for color 2

14.15.12.2 Layer Mixer 1

0x05118004 MDP_OVERLAYPROC1_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0003

This register configures the OVERLAY PROCESSOR 1's starting behavior. When the DIRECT_OUT is set, the input pipes that are assigned to this processor will be initiated by the active refresh if the interface selected is DTV or TV Encoder, regardless refresh_mode selection. If going through a Frame Buffer, the pipes for the Overlay Processor can be kick-started by the REFRESH_MODE selected. The value only take effect at the next refresh initiation of the Overlay Processor 0. However, it is not recommended to switch Overlay Processor's mode of operation at tun time, the switch should be done only when an Overlay Processor and its associated interface are in idle.

MDP_OVERLAYPROC1_CFG

Bits	Name	Description
31:6	RESERVED31_6	

MDP_OVERLAYPROC1_CFG (cont.)

Bits	Name	Description
5	CON_WB_MODE	RESERVED.
4	CON_WB_EN	Concurrent display and write back mode selection. Only valid when not in BLT mode and when DIRECT_OUT is 1. 0x0: Disabled 0x1: Enabled
3	BLT_MODE	Puts this Overlay Processor into BLT (MDP3) type of SW operation mode, which means both the Overlay Processor 1 and DMA_E fetch will be fully controlled by the SW. There will be no passing of Frame Buffer pointers between the Overlay Processor 1 and DMA_E. This setting takes priority over REFRESH_MODE and DIRECT_OUT settings.
2:1	REFRESH_MODE	Overlay Processor refresh mode (only valid when not in BLT mode and not in direct-out mode, otherwise don't care): 0x0: On-Demand (software initiated, FrameBuffer push or Direct Out push for smart panel) 0x1: Vsync rate (FrameBuffer pull) 0x2: Vsync/2 rate (FrameBuffer pull) 0x3: Vsync/4 rate (FrameBuffer pull)
0	DIRECT_OUT	Overlay Processor output direction select (only valid when not in BLT mode, otherwise don't care): 0x0: Via FrameBuffer 0x1: Direct to interface (internally refresh_mode is forced to Vsync rate if connected to LCDC/DTV/TV_Enc)

0x05118008 MDP_OVERLAYPROC1_OUT_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0020_0020

This register designates the output size of the Overlay Processor 1 and is also used as the Frame Buffer/Active Region size for DMA_E or DMA_S.

MDP_OVERLAYPROC1_OUT_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DST_H	Output ROI height (pixel).
15:12	RESERVED15_12	
11:0	DST_W	Output ROI width (pixel).

0x0511800C MDP_OVERLAYPROC1_FB_ADDR1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This is the 1st Frame Buffer base address (for ping-ponging) that is used when this Overlay Processor is in Frame Buffer mode, where the value is registered and used at every other frame initiation of this Overlay Processor. In other modes, this is the only effective Frame Buffer base address used, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC1_FB_ADDR1

Bits	Name	Description
31:0	ADDR	Starting base byte address for Frame Buffer

0x05118010 MDP_OVERLAYPROC1_FB_Y_STRIDE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_FB_Y_STRIDE register defines the line jump value (in bytes) in the Frame Buffer.

MDP_OVERLAYPROC1_FB_Y_STRIDE

Bits	Name	Description
31:13	RESERVED31_13	
12:0	BUF_Y_STRIDE	Y-stride (or) line jump in bytes in the Frame Buffer.

0x05118014 MDP_OVERLAYPROC1_OPMODE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The FB_FORMAT field is also used by DMA_E to decipher what Frame Buffer format to fetch in FrameBuffer Pull mode of operation.

MDP_OVERLAYPROC1_OPMODE

Bits	Name	Description
31	BYPASS_COLOR3_EN	Enables propagation of color component 3 to the packer 0x1: color3 is taken from register 0x0: color3 is propagated from the pipe
30:4	RESERVED30_4	RESERVED
3	INTRLACE_FETCH	Enable interlace fetch for interlace-in and interlace-out mode of operation for all VG pipes on this Overlay Processor. This mode of operation should not be used when any pipes other than VG pipes are involved, i.e., even cursor blend; and it is valid only when Overlay Processor 1 is driving directly to an interlace output interface (DTV or ATV).
2	PGC_EN	Panel Gamma Correction enable. If disabled, the colors are mapped linearly from 12-bit to 8-bit.
1:0	FB_FORMAT	This field actually controls memory write back pixel format in LM1 with regard to operation mode (direct with concurrent write back, FB or BLT). If the concurrent write back is enabled, only RGB888 is supported. 0x0: RGB888 0x1: RGB565 0x2: 422 h2v1 interleaved

0x05118018 MDP_OVERLAYPROC1_DMA_MUX_CON

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0004

This register configures how DMA_S and DMA_E are connected to overlay processor1 pipe.

Following table shows all possible scenarios for MUX selection between DMA_S and DMA_E.

Note) MDP_OVERLAYPROC1_CFG register has to re-program whenever changing Layer Mix1 destination PIPE (MDP_OVERLAYPROC1_DMA_MUX_CON.OVP1_DMA_PIPE_SEL control bit).

MDP_OVERLAYPROC1_DMA_MUX_CON

Bits	Name	Description
31:4	RESERVED31_4	
3	DMA_E_DEST_SEL	DMA_E destination interface selection 0x0: DMA_E destination (default) 0x1: DMA_S destination

MDP_OVERLAYPROC1_DMA_MUX_CON (cont.)

Bits	Name	Description
2	DMA_S_ABL_IN_PIPE_SEL	DMA_S ABL input pipe selection 0x0: DMA_E 0x1: DMA_S (default)
1	DMA_E_BLEND_IN_PIPE_SEL	DMA_E Blend input fetch engine selection 0x0: DMA_E (default) 0x1: DMA_S
0	OVP1_DMA_PIPE_SEL	OVP1 DMA PIPE Selection for Frame Buffer and Direct mode 0x0: DMA_E (default) 0x1: DMA_S

0x0511801C MDP_OVERLAYPROC1_FB_ADDR2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This is the 2nd Frame Buffer base address (for ping-ponging) that is used only when this Overlay Processor is in Frame Buffer mode. The value is registered and used at every other frame initiation of this Overlay Processor.

MDP_OVERLAYPROC1_FB_ADDR2

Bits	Name	Description
31:0	ADDR	Starting base byte address for Frame Buffer

0x05118020 MDP_OVERLAYPROC1_PROFILE_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_PROFILE_EN

Bits	Name	Description
31:1	RESERVED31_1	
0	EN	Enable the ROI cycle counter for profiling

0x05118024 MDP_OVERLAYPROC1_PROFILE_COUNT

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_PROFILE_COUNT

Bits	Name	Description
31:24	RESERVED31_24	
23:0	TOTAL_CYCLE	Total cycle count in a ROI, from new ROI to last pixel out of the processor (OVERLAYPROC1 goes back to Idle)

0x05118104 MDP_OVERLAYPROC1_BLEND0_OP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

This register describes the blend operation done by Layer Mixer 0 on Stage 0 FG/BG, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC1_BLEND0_OP

Bits	Name	Description
31:10	RESERVED31_10	
9	BG_TRANSP_EN	BG transparency color check enable. When color matches, the FG pixel is passed; otherwise, the blended result is passed. However, if both FG and BG Transparency checks are enabled and both matches, BG pixel is passed.
8	FG_TRANSP_EN	FG transparency color check enable. When color matches, the BG pixel is passed; otherwise, the blended result is passed.
7	BG_MOD_ALPHA	When set (1), bg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
6	BG_INV_ALPHA	When set (1) the alpha selected by BG_ALPHA_SEL is inverted (1-alpha).
5:4	BG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha
3	FG_MOD_ALPHA	When set (1), fg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.

MDP_OVERLAYPROC1_BLEND0_OP (cont.)

Bits	Name	Description
2	FG_INV_ALPHA	When set (1) the alpha selected by FG_ALPHA_SEL is inverted (1-alpha).
1:0	FG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha

0x05118108 MDP_OVERLAYPROC1_BLEND0_FG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC1_BLEND0_FG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x0511810C MDP_OVERLAYPROC1_BLEND0_BG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC1_BLEND0_BG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x05118110 MDP_OVERLAYPROC1_BLEND0_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND0_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05118114 MDP_OVERLAYPROC1_BLEND0_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND0_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05118118 MDP_OVERLAYPROC1_BLEND0_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND0_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x0511811C MDP_OVERLAYPROC1_BLEND0_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND0_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05118124 MDP_OVERLAYPROC1_BLEND1_OP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

This register describes the blend operation done by Layer Mixer 0 on Stage 1 FG/BG, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC1_BLEND1_OP

Bits	Name	Description
31:10	RESERVED31_10	
9	BG_TRANSP_EN	BG transparency color check enable. When color matches, the FG pixel is passed; otherwise, the blended result is passed. However, if both FG and BG Transparency checks are enabled and both matches, BG pixel is passed.
8	FG_TRANSP_EN	FG transparency color check enable. When color matches, the BG pixel is passed; otherwise, the blended result is passed.
7	BG_MOD_ALPHA	When set (1), bg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
6	BG_INV_ALPHA	When set (1) the alpha selected by BG_ALPHA_SEL is inverted (1-alpha).
5:4	BG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha
3	FG_MOD_ALPHA	When set (1), fg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
2	FG_INV_ALPHA	When set (1) the alpha selected by FG_ALPHA_SEL is inverted (1-alpha).

MDP_OVERLAYPROC1_BLEND1_OP (cont.)

Bits	Name	Description
1:0	FG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha

0x05118128 MDP_OVERLAYPROC1_BLEND1_FG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC1_BLEND1_FG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x0511812C MDP_OVERLAYPROC1_BLEND1_BG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC1_BLEND1_BG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x05118130 MDP_OVERLAYPROC1_BLEND1_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND1_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05118134 MDP_OVERLAYPROC1_BLEND1_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND1_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05118138 MDP_OVERLAYPROC1_BLEND1_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND1_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x0511813C MDP_OVERLAYPROC1_BLEND1_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND1_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05118144 MDP_OVERLAYPROC1_BLEND2_OP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

This register describes the blend operation done by Layer Mixer 0 on Stage 2 FG/BG, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC1_BLEND2_OP

Bits	Name	Description
31:10	RESERVED31_10	
9	BG_TRANSP_EN	BG transparency color check enable. When color matches, the FG pixel is passed; otherwise, the blended result is passed. However, if both FG and BG Transparency checks are enabled and both matches, BG pixel is passed.
8	FG_TRANSP_EN	FG transparency color check enable. When color matches, the BG pixel is passed; otherwise, the blended result is passed.
7	BG_MOD_ALPHA	When set (1), bg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
6	BG_INV_ALPHA	When set (1) the alpha selected by BG_ALPHA_SEL is inverted (1-alpha).
5:4	BG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha
3	FG_MOD_ALPHA	When set (1), fg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
2	FG_INV_ALPHA	When set (1) the alpha selected by FG_ALPHA_SEL is inverted (1-alpha).

MDP_OVERLAYPROC1_BLEND2_OP (cont.)

Bits	Name	Description
1:0	FG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha

0x05118148 MDP_OVERLAYPROC1_BLEND2_FG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC1_BLEND2_FG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x0511814C MDP_OVERLAYPROC1_BLEND2_BG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC1_BLEND2_BG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x05118150 MDP_OVERLAYPROC1_BLEND2_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND2_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05118154 MDP_OVERLAYPROC1_BLEND2_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND2_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05118158 MDP_OVERLAYPROC1_BLEND2_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND2_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x0511815C MDP_OVERLAYPROC1_BLEND2_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND2_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05118160 MDP_OVERLAYPROC1_BLEND3_OP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

This register describes the blend operation done by Layer Mixer 0 on Stage 0 FG/BG, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC1_BLEND3_OP

Bits	Name	Description
31:10	RESERVED31_10	
9	BG_TRANSP_EN	BG transparency color check enable. When color matches, the FG pixel is passed; otherwise, the blended result is passed. However, if both FG and BG Transparency checks are enabled and both matches, BG pixel is passed.
8	FG_TRANSP_EN	FG transparency color check enable. When color matches, the BG pixel is passed; otherwise, the blended result is passed.
7	BG_MOD_ALPHA	When set (1), bg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
6	BG_INV_ALPHA	When set (1) the alpha selected by BG_ALPHA_SEL is inverted (1-alpha).
5:4	BG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha
3	FG_MOD_ALPHA	When set (1), fg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
2	FG_INV_ALPHA	When set (1) the alpha selected by FG_ALPHA_SEL is inverted (1-alpha).

MDP_OVERLAYPROC1_BLEND3_OP (cont.)

Bits	Name	Description
1:0	FG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha

0x05118164 MDP_OVERLAYPROC1_BLEND3_FG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC1_BLEND3_FG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x05118168 MDP_OVERLAYPROC1_BLEND3_BG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC1_BLEND3_BG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x0511816C MDP_OVERLAYPROC1_BLEND3_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND3_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05118170 MDP_OVERLAYPROC1_BLEND3_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND3_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05118174 MDP_OVERLAYPROC1_BLEND3_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND3_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x05118178 MDP_OVERLAYPROC1_BLEND3_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND3_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05118180 MDP_OVERLAYPROC1_BG_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BG_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05118184 MDP_OVERLAYPROC1_BG_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BG_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05118188 MDP_OVERLAYPROC1_BG_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BG_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x0511818C MDP_OVERLAYPROC1_BG_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BG_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05118200 MDP_OVERLAYPROC1_CSC_CONFIG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_CSC_CONFIG register defines the color correct parameters at the output of the Overlay Processor 1.

MDP_OVERLAYPROC1_CSC_CONFIG

Bits	Name	Description
31:3	RESERVED31_3	
2	COLOR_FMT_OUT	Select the output color format after correction/conversion 0x0: RGB (default) 0x1: YCbCr

MDP_OVERLAYPROC1_CSC_CONFIG (cont.)

Bits	Name	Description
1	COLOR_FMT_IN	Select the input color format for correction/conversion 0x0: RGB (default) 0x1: YCbCr
0	CONVERT_MATRIX_EN	Enable color convert (matrix conversion).

0x05119000 MDP_OVERLAYPROC1_BLEND0_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000a

MDP_OVERLAYPROC1_BLEND0_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	Internal idles and valids

0x05119004 MDP_OVERLAYPROC1_BLEND0_COLOR3_OUT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND0_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED31_1	
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x05119400 MDP_OVERLAYPROC1_BLEND1_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000a

MDP_OVERLAYPROC1_BLEND1_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	Internal idles and valids

0x05119404 MDP_OVERLAYPROC1_BLEND1_COLOR3_OUT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND1_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED31_1	
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x05119800 MDP_OVERLAYPROC1_BLEND2_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000a

MDP_OVERLAYPROC1_BLEND2_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	Internal idles and valids

0x05119804 MDP_OVERLAYPROC1_BLEND2_COLOR3_OUT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND2_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED31_1	

MDP_OVERLAYPROC1_BLEND2_COLOR3_OUT (cont.)

Bits	Name	Description
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x05119C00 MDP_OVERLAYPROC1_BLEND3_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000a

MDP_OVERLAYPROC1_BLEND3_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	Internal idles and valids

0x05119C04 MDP_OVERLAYPROC1_BLEND3_COLOR3_OUT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_BLEND3_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED31_1	
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x0511A400+ 4*n MDP_OVERLAYPROC1_CSC_MV1n, n=[0..8]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_OVERLAYPROC1_CSC_MV1n register contains the set1 matrix vector.

MDP_OVERLAYPROC1_CSC_MV1n

Bits	Name	Description
31:13	RESERVED31_13	
12:0	MV1	MV1 = Matrix vector set1 (s4.9). Matrices are indexed left to right, top to bottom. That is, row 1, col 0 index = 3 (index range - 0 to 8).

0x0511A500+ 4*n MDP_OVERLAYPROC1_CSC_PRE_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_OVERLAYPROC1_CSC_PRE_BV1n register contains the set1 pre-bias vector.

MDP_OVERLAYPROC1_CSC_PRE_BV1n

Bits	Name	Description
31:9	RESERVED31_9	
8:0	PRE_BV1	PRE_BV1= Pre-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x0511A580+ 4*n MDP_OVERLAYPROC1_CSC_POST_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_OVERLAYPROC1_CSC_POST_BV1n register contains the set1 post-bias vector.

MDP_OVERLAYPROC1_CSC_POST_BV1n

Bits	Name	Description
31:9	RESERVED31_9	
8:0	POST_BV1	POST_BV1 = Post-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x0511A600+ 4*n MDP_OVERLAYPROC1_CSC_PRE_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_OVERLAYPROC1_CSC_PRE_LV1n register contains the set1 pre-limit vector.

MDP_OVERLAYPROC1_CSC_PRE_LV1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	PRE_LV1	PRE_LV1 = Pre-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x0511A680+ 4*n MDP_OVERLAYPROC1_CSC_POST_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_OVERLAYPROC1_CSC_POST_LV1n register contains the set1 post-limit vector.

MDP_OVERLAYPROC1_CSC_POST_LV1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	POST_LV1	POST_LV1 = Post-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x0511C800+ 4*n MDP_OVERLAYPROC1_GC_START_COLOR_0_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component0.

MDP_OVERLAYPROC1_GC_START_COLOR_0_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x0511C880+ 4*n MDP_OVERLAYPROC1_GC_PARAM_COLOR_0_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component0.

MDP_OVERLAYPROC1_GC_PARAM_COLOR_0_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U3.12)

0x0511C900+ 4*n MDP_OVERLAYPROC1_GC_START_COLOR_1_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component1.

MDP_OVERLAYPROC1_GC_START_COLOR_1_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x0511C980+ 4*n MDP_OVERLAYPROC1_GC_PARAM_COLOR_1_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component1.

MDP_OVERLAYPROC1_GC_PARAM_COLOR_1_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U3.12)

0x0511CA00+4*n MDP_OVERLAYPROC1_GC_START_COLOR_2_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component2.

MDP_OVERLAYPROC1_GC_START_COLOR_2_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x0511CA80+4*n MDP_OVERLAYPROC1_GC_PARAM_COLOR_2_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component2.

MDP_OVERLAYPROC1_GC_PARAM_COLOR_2_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U3.12)

0x0511D004 MDP_OVERLAYPROC1_LSP_BORDER_COLOR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Least Significant Portion (lower 24 bits of total 36 bits) of border color values.

MDP_OVERLAYPROC1_LSP_BORDER_COLOR

Bits	Name	Description
31:28	RESERVED31_28	
27:16	BORDER_COLOR1	Border color value for color 1
15:12	RESERVED15_12	
11:0	BORDER_COLOR0	Border color value for color 0

0x0511D008 MDP_OVERLAYPROC1_MSP_BORDER_COLOR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Most Significant Portion (upper 12 bits of total 36 bits) of border color values.

MDP_OVERLAYPROC1_MSP_BORDER_COLOR

Bits	Name	Description
31:12	RESERVED31_12	
11:0	BORDER_COLOR2	Border color value for color 2

14.15.12.3 Video/Graphics1 Input Pipe registers

0x05120000 MDP_VG1_SRC_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0020_0020

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_SRC_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	SRC_H	Height of input ROI data
15:12	RESERVED15_12	
11:0	SRC_W	Width of input ROI data

0x05120004 MDP_VG1_SRC_XY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This represents the offset from the top-left corner of the source image. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_SRC_XY

Bits	Name	Description
31:28	RESERVED31_28	
27:16	SRC_Y	Y offset of source ROI in the source image
15:12	RESERVED15_12	
11:0	SRC_X	X offset of source ROI in the source image

0x05120008 MDP_VG1_OUT_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0020_0020

If scale is not enabled, this register value will be ignored, and the hardware assumes that the output size is the same as SRC_SIZE register setting. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_OUT_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DST_H	Height of output ROI data
15:12	RESERVED15_12	

MDP_VG1_OUT_SIZE (cont.)

Bits	Name	Description
11:0	DST_W	Width of output ROI data

0x0512000C MDP_VG1_OUT_XY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This represents the offset from the top-left corner of the base layer image. If this pipe is processing the base layer then this register is all zeros. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_OUT_XY

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DST_Y	Y offset of this layer output in the Frame Buffer
15:12	RESERVED15_12	
11:0	DST_X	X offset of this layer output in the Frame Buffer

0x05120010 MDP_VG1_SRCP0_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_SRCP0_ADDR

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x05120014 MDP_VG1_SRCP1_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_SRCP1_ADDR

Bits	Name	Description
31:0	SRCP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x05120018 MDP_VG1_SRCP2_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_SRCP2_ADDR

Bits	Name	Description
31:0	SRCP2_ADDR	Base byte address of the Image's planar color2 plane.

0x0512001C MDP_VG1_SRCP3_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_SRCP3_ADDR

Bits	Name	Description
31:0	SRCP3_ADDR	Base byte address of the Image's color3 (alpha) component, used in pseudo planar + alpha format, or planar.

0x05120020 MDP_VG1_SRCP0_ADDR_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 1 is used for VG1 pipe.

MDP_VG1_SRCP0_ADDR_1

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x05120024 MDP_VG1_SRCP1_ADDR_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 1 is used for VG1 pipe.

MDP_VG1_SRCP1_ADDR_1

Bits	Name	Description
31:0	SRCP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x05120028 MDP_VG1_SRCP2_ADDR_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 1 is used for VG1 pipe.

MDP_VG1_SRCP2_ADDR_1

Bits	Name	Description
31:0	SRCP2_ADDR	Base byte address of the Image's planar color2 plane.

0x05120030 MDP_VG1_SRCP0_ADDR_2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 2 is used for VG1 pipe.

MDP_VG1_SRCP0_ADDR_2

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x05120034 MDP_VG1_SRCP1_ADDR_2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 2 is used for VG1 pipe.

MDP_VG1_SRCP1_ADDR_2

Bits	Name	Description
31:0	SRCP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x05120038 MDP_VG1_SRCP2_ADDR_2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 2 is used for VG1 pipe.

MDP_VG1_SRCP2_ADDR_2

Bits	Name	Description
31:0	SRCP2_ADDR	Base byte address of the Image's planar color2 plane.

0x05120040 MDP_VG1_SRC_YSTRIDE1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0060

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_SRC_YSTRIDE1

Bits	Name	Description
31	RESERVED31	
30:16	SRCP1_YSTRIDE	Plane 1 y stride in bytes.
15	RESERVED15	
14:0	SRCP0_YSTRIDE	Plane 0 y stride in bytes.

0x05120044 MDP_VG1_SRC_YSTRIDE2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_SRC_YSTRIDE2

Bits	Name	Description
31	RESERVED31	
30:16	SRCP3_YSTRIDE	Plane 3 y stride in bytes.
15	RESERVED15	
14:0	SRCP2_YSTRIDE	Plane 2 y stride in bytes.

0x05120048 MDP_VG1_SSTILE_FRAME_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x02D0_0500

The frame size of a whole super tile format frame is needed to calculate the proper addressing.

The minimum super tile height is 96.

MDP_VG1_SSTILE_FRAME_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	FRAME_H	Video Super Tile format frame height
15:12	RESERVED15_12	
11:0	FRAME_W	Video Super Tile format frame width

0x05120050 MDP_VG1_SRC_FORMAT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0002_44FF

This register describes the input surface for this pipe. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_SRC_FORMAT

Bits	Name	Description
31	RESERVED31	
30:29	FRAME_FORMAT	0x0: Linear, No tile (Default) 0x1: Reserved for ARGB 4x4 tile 0x2: Video in 64x32 supertile, YCbCr 420 PP only
28	SRC_CHROMA_SITE	Source chroma siting. 1 = offsite, 0 = cosite.
27:26	SRC_CHROMA_SAMP	Source chroma sampling: 0x0: 4:4:4/RGB 0x1: H2V1 0x2: H1V2 0x3: 4:2:0.
25:23	RESERVED25_23	
22	SOLID_FILL	If this bit is set (1), Fetch uses the CONSTANT_COLOR register value as its output. Nothing is fetched.
21	VC1_REDUCE	VC1 range reduction enable for YUV source, the reduce range is set by a separate register VC1_RANGE.
20:19	FETCH_PLANES	Determines the number of planes to fetch: 0x0: Interleaved 0x1: Planar 0x2: pseudo planar
18	UNPACK_ALIGN	0x0: To LSB 0x1: To MSB
17	UNPACK_TIGHT	0x0: Loose 0x1: Tight
16:15	RESERVED16_15	
14:13	UNPACK_COUNT	Valid unpacking pattern count: 0 = 1 component,..., 3 = 4 components. Unpacking pattern only applies to the interleaved plane (chroma plane in pseudo-planar).
12	ROT90	Source has been rotated 90 degree
11	RESERVED11	

MDP_VG1_SRC_FORMAT (cont.)

Bits	Name	Description
10:9	SRC_BPP	Effective source byte per pixel: 0 = 1 byte, 1 = 2 bytes, 2 = 3 bytes, 3 = 4 bytes. This is only used when unpacking the interleaved plane.
8	SRCC3_EN	0x1: Source has alpha
7:6	SRCC3	Number of bits for component 3 (alpha) input, this is not used for dither: 0 = 1 bit, 1 = 4 bits, 2 = 6 bits, 3 = 8 bits.
5:4	SRCC2	Number of bits for component 2 (R / Cr) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	SRCC1	Number of bits for component 1 (B / Cb) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	SRCC0	Number of bits for component 0 (G / luma) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x05120054 MDP_VG1_SRC_UNPACK_PATTERN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0302_0001

Unpacking pattern, maximum of 4 pattern elements starting from LSB to MSB (0 to 4). Default is ARGB or C3-C2-C0-C1. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_SRC_UNPACK_PATTERN

Bits	Name	Description
31:26	RESERVED31_26	
25:24	ELEMENT3	0x0: C0 0x1: C1 0x2: C2 0x3: C3
23:18	RESERVED23_18	
17:16	ELEMENT2	0x0: C0 0x1: C1 0x2: C2 0x3: C3
15:10	RESERVED15_10	
9:8	ELEMENT1	0x0: C0 0x1: C1 0x2: C2 0x3: C3

MDP_VG1_SRC_UNPACK_PATTERN (cont.)

Bits	Name	Description
7:2	RESERVED7_2	
1:0	ELEMENT0	0x0: C0 0x1: C1 0x2: C2 0x3: C3

0x05120058 MDP_VG1_OP_MODE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_OP_MODE

Bits	Name	Description
31:20	RESERVED31_20	
19	DEINT_ODD_REF	De-interlace uses Odd field as Reference when set.
18	DEINT_EN	De-interlace enable
17	HIST_LUT_EN	Component 0 LUT enable for histogram enhancement.
16	IGC_LUT_EN	Inverse Gamma Correction LUT enable. If disabled, the colors are mapped linearly from 8-bit to 12-bit.
15	DITHER_EN	Dither enable.
14:13	FLIP_MODE	Flip operation: Bit 1: Left/right flip Bit 2: Up/down flip
12	RESERVED12	
11	CSC_EN	This enables the color matrix conversion.
10	DST_DATA_FORMAT	Color converter output data format setting: 0x0: RGB 0x1: YCbCr
9	SRC_DATA_FORMAT	Color converter input data format setting: 0x0: RGB 0x1: YCbCr
8:6	RESERVED8_6	

MDP_VG1_OP_MODE (cont.)

Bits	Name	Description
5:4	SCALEY_UNIT_SEL	Select Polyphase FIR or M/N filter for Y scaler. M/N should be used at low-end of down-scaling (between 1/8 and 1/4). Pixel Repeat is special scaling mode used for upscale only. Otherwise, QSEED should be selected in other cases. This field must be set to 0x0 when SCALEY_EN is 0x0. 0x0: FIR (QSEED) 0x1: M/N phase-controlled 0x2: Pixel Repeat
3:2	SCALEX_UNIT_SEL	Select Polyphase FIR or M/N filter for X scaler. M/N should be used at low-end of down-scaling (between 1/8 and 1/4). Pixel Repeat is special scaling mode used for upscale only. Otherwise, QSEED should be selected in other cases. This field must be set to 0x0 when SCALEX_EN is 0x0. 0x0: FIR (QSEED) 0x1: M/N phase-controlled 0x2: Pixel Repeat
1	SCALEY_EN	Y scaling enable
0	SCALEX_EN	X scaling enable

0x0512005C MDP_VG1_SCALE_PHASEX_STEP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_SCALE_PHASEX_STEP

Bits	Name	Description
31:0	PHASEX_STEP	X phase step for scaling, which is input width/output width in u3.29, i.e., (src_size / out_size)<<29, phase step of 8 (1/8 scale) is encoded by setting this value to 0 (representing 0x1_0000_0000).

0x05120060 MDP_VG1_SCALE_PHASEY_STEP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_SCALE_PHASEY_STEP

Bits	Name	Description
31:0	PHASEY_STEP	Y phase step for scaling, which is input height/output height in u3.29, i.e., (src_size / out_size)<<29, phase step of 8 (1/8 scale) is encoded by setting this value to 0 (representing 0x1_0000_0000).

0x05120064 MDP_VG1_HIST_LUT_SEL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG1_HIST_LUT_SEL

Bits	Name	Description
31:1	RESERVED31_1	
0	LUT_SEL	Selects which LUT to use for histogram enhancement 0x0: Set1 0x1: Set2

0x05120068 MDP_VG1_DITHER_STRENGTH

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_003F

MDP_VG1_DITHER_STRENGTH

Bits	Name	Description
31:6	RESERVED31_6	
5:4	C2_BITS	Number of MSBits on component 2 (R/Cr) to indicate the dithering boundary: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	C1_BITS	Number of MSBits on component 1 (B/Cb) to indicate the dithering boundary: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	C0_BITS	Number of MSBits on component 0 (G/Y) to indicate the dithering boundary: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x05121000 MDP_VG1_FETCH_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_003F

MDP_VG1_FETCH_STATUS

Bits	Name	Description
31:12	RESERVED31_12	
11:8	FIFO_ERRORS	TileFetch internal FIFO errors. These error bits are pulse catching, and returned to zero when this register is read: Bit 11= control FIFO error Bit 10= burstbuf FIFO error Bit 9= line_gen luma FIFO error Bit 8= line_gen chroma FIFO error
7:6	RESERVED7_6	
5:0	IDLES	TileFetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 5= dma_rd idle Bit 4= ctl idle Bit 3= burstbuf idle Bit 2= unpack idle Bit 1= unpack chroma idle Bit 0= line_gen idle

0x05121004 MDP_VG1_FETCH_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0047

MDP_VG1_FETCH_CFG

Bits	Name	Description
31:9	RESERVED31_9	
8	ADDR_SYNC_MODE	Boundary on which fetch address synchronizes: 0x0: frame (default) 0x1: line
7	FETCH_OPT_EN	Fetch Optimization Enable. Fetch optimization is supported only for interleave RGB formats. This setting is ignored when in others. 0x0: Disable (default) 0x1: Enable

MDP_VG1_FETCH_CFG (cont.)

Bits	Name	Description
6:4	MAX_BURST_SIZE	Maximum burst beat size. Possible values: 0x4: 16 (default) 0x2: 8 0x1: 4
3	RESERVED3	
2:0	REQ_DEPTH_LIMIT	Pending request limit, default max value of 0x7 means maximum pending requests allowed in the design, anything less limits the bus requests to that number + 1.

0x05121008 MDP_VG1_CONSTANT_COLOR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0xFFFF_FFFF

MDP_VG1_CONSTANT_COLOR

Bits	Name	Description
31:24	COLOR3	Constant color driven for color3 during solid fill mode.
23:16	COLOR2	Constant color driven for color2 during solid fill mode.
15:8	COLOR1	Constant color driven for color1 during solid fill mode.
7:0	COLOR0	Constant color driven for color0 during solid fill mode.

0x0512100C MDP_VG1_FETCH_COUNT

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_VG1_FETCH_COUNT

Bits	Name	Description
31:28	RESERVED31_28	
27:16	CHROMA_LINE	Current chroma line number
15:12	RESERVED15_12	
11:0	LUMA_LINE	Current luma line number

0x05121010 MDP_VG1_FETCH_STATISTIC

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_VG1_FETCH_STATISTIC

Bits	Name	Description
31:13	FETCH_KCYCLES	Accumulated kilo-cycles spent in wait for read data in the current frame.
12:0	FETCH_KBYTES	Accumulated KByte received in the current frame.

0x05121020 MDP_VG1_VC1_RANGE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0707

MDP_VG1_VC1_RANGE

Bits	Name	Description
31:11	RESERVED31_11	
10:8	RANGE_MAPUV	Chroma range map for VC1 range reduction, default of 7 is equivalent to setting it for main profile.
7:3	RESERVED7_3	
2:0	RANGE_MAPY	Luma range map for VC1 range reduction, default of 7 is equivalent to setting it for main profile.

0x05122000 MDP_VG1_DEINT_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000F

MDP_VG1_DEINT_STATUS

Bits	Name	Description
31:4	RESERVED31_4	
3:0	IDLES	Internal idles

0x05122004 MDP_VG1_DEINT_DECISION

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0003_0032

MDP_VG1_DEINT_DECISION

Bits	Name	Description
31:19	RESERVED31_19	
18:16	ATTENU	Attenuation (the shift value) for less temporal resolution; valid range is 0
15:11	RESERVED15_11	
10:0	THRESH	Threshold (u11) for de-interlace attenuation decision

0x05122010 MDP_VG1_DEINT_COEFF0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0360_03E0

The MDP_VG1_DEINT_COEFFn registers contain the set of luma filter coefficients, where w3 is for the center pixel, w2 is for (+1, -1) pixels, w1 is for (+2, -2) pixels, and w0 is for (+3, -3) pixels.

MDP_VG1_DEINT_COEFF0

Bits	Name	Description
31:26	RESERVED31_26	
25:16	COEFF1	Luma filter coefficient w1 (s10 Q5).
15:10	RESERVED31_10	
9:0	COEFF0	Luma filter coefficient w0 (s10 Q5).

0x05122014 MDP_VG1_DEINT_COEFF1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0140_0120

The MDP_VG1_DEINT_COEFFn registers contain the set of luma filter coefficients, where w3 is for the center pixel, w2 is for (+1, -1) pixels, w1 is for (+2, -2) pixels, and w0 is for (+3, -3) pixels.

MDP_VG1_DEINT_COEFF1

Bits	Name	Description
31:26	RESERVED31_26	
25:16	COEFF1	Luma filter coefficient w3 (s10 Q5).
15:10	RESERVED31_10	
9:0	COEFF0	Luma filter coefficient w2 (s10 Q5).

0x05123400+ 4*n MDP_VG1_HIST_LUT1n, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG1_HIST_LUT1n registers contains the color lookup values for histogram enhancement set1.

MDP_VG1_HIST_LUT1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	LUT_COLOR0	LUT value for color0.

0x05123800+ 4*n MDP_VG1_HIST_LUT2n, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG1_HIST_LUT2n registers contains the color lookup values for histogram enhancement set2.

MDP_VG1_HIST_LUT2n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	LUT_COLOR0	LUT value for color0.

0x05124400+ 4*n MDP_VG1_CSC_MV1n, n=[0..8]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG1_CSC_MV1n register contains the set1 matrix vector.

MDP_VG1_CSC_MV1n

Bits	Name	Description
31:13	RESERVED31_13	
12:0	MV1	MV1 = Matrix vector set1 (s4.9). Matrices are indexed left to right, top to bottom. That is, row 1, col 0 index = 3 (index range - 0 to 8).

0x05124500+ 4*n MDP_VG1_CSC_PRE_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG1_CSC_PRE_BV1n register contains the set1 pre-bias vector.

MDP_VG1_CSC_PRE_BV1n

Bits	Name	Description
31:9	RESERVED31_9	
8:0	PRE_BV1	PRE_BV1= Pre-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x05124580+ 4*n MDP_VG1_CSC_POST_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG1_CSC_POST_BV1n register contains the set1 post-bias vector.

MDP_VG1_CSC_POST_BV1n

Bits	Name	Description
31:9	RESERVED31_9	
8:0	POST_BV1	POST_BV1 = Post-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x05124600+ 4*n MDP_VG1_CSC_PRE_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG1_CSC_PRE_LV1n register contains the set1 pre-limit vector.

MDP_VG1_CSC_PRE_LV1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	PRE_LV1	PRE_LV1 = Pre-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x05124680+ 4*n MDP_VG1_CSC_POST_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG1_CSC_POST_LV1n register contains the set1 post-limit vector.

MDP_VG1_CSC_POST_LV1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	POST_LV1	POST_LV1 = Post-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x05125000+ 4*n MDP_VG1_IGC_LSP_LUTn, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG1_IGC_LSP_LUTn registers contains contains the Least Significant Portion (lower 24 bits of total 36 bits) of the color lookup values for IGC LUT.

MDP_VG1_IGC_LSP_LUTn

Bits	Name	Description
31:28	RESERVED31_28	

MDP_VG1_IGC_LSP_LUTn (cont.)

Bits	Name	Description
27:16	LUT_COLOR1	LUT value for color1.
15:12	RESERVED15_12	
11:0	LUT_COLOR0	LUT value for color0.

0x05125800+ 4*n MDP_VG1_IGC_MSP_LUTn, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG1_IGC_MSP_LUTn registers contains the most significant portion (color component 2) of the color lookup values for IGC LUT. The whole LUT should be written to in the sequence of LSP write first followed by MSP write, writing from lower address to higher address. Each MSP register write actually triggers the write of whole 36-bit LUT entry into the RAM.

MDP_VG1_IGC_MSP_LUTn

Bits	Name	Description
31:12	RESERVED31_12	
11:0	LUT_COLOR2	LUT value for color2.

0x05126000 MDP_VG1_HIST_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_VG1_HIST_START register kicks off histogram generation.

MDP_VG1_HIST_START

Bits	Name	Description
31:0	HIST_START	A write to this register kicks off histogram generation. Actual accumulation begins at the start of next ROI. Histogram accumulation can be started only when histogram reset sequence is not currently active.

0x05126004 MDP_VG1_HIST_FRAME_CNT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0001

The MDP_VG1_HIST_FRAME_CNT register is used to program the frame count for histogram accumulation.

MDP_VG1_HIST_FRAME_CNT

Bits	Name	Description
31:6	RESERVED31_6	
5:0	FRAME_CNT	Program the number of frames over which the histogram data has to be collected. If the frame count programmed is more than what each 24-bit bin can support, the bin count will saturate at the maximum value. Here are some max. frame counts that can be programmed for different image sizes for a 24-bit bin. XGA (1024 x 768) - 21 WSVGA (1024 x 600) - 27 WVGA (800 x 480) - 43 VGA (640 x 480) - 54

0x0512600C MDP_VG1_HIST_RESET_SEQ_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_VG1_HIST_RESET_SEQ_START kicks off a reset sequence.

MDP_VG1_HIST_RESET_SEQ_START

Bits	Name	Description
31:0	RESET_SEQ_START	Writing to this register kicks off a reset sequence.This reset sequence clears all RAM locations and RAM rd/wr pointers. The reset sequence can be initiated only when histogram generation is not currently active. Note: Functional clock gating will shut off the clock to VG1 sub-blocks when a ROI is not being processed. So VG1 clock should be forced ON for the reset sequence to complete.

0x05126010 MDP_VG1_HIST_CONTROL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG1_HIST_CONTROL register controls histogram operation.

MDP_VG1_HIST_CONTROL

Bits	Name	Description
31:1	RESERVED31_1	
0	AUTO_CLEAR_EN	When set (1), the bin from which data has been read is cleared automatically.

0x05126014 MDP_VG1_HIST_INTR_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG1_HIST_INTR_STATUS register provides histogram interrupt status.

MDP_VG1_HIST_INTR_STATUS

Bits	Name	Description
31:2	RESERVED31_2	
1	HIST_DONE	When set (1) implies histogram generation is complete.
0	RESET_SEQ_DONE	When set (1) implies the reset sequence is complete.

0x05126018 MDP_VG1_HIST_INTR_CLEAR

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_VG1_HIST_INTR_CLEAR is used to clear the interrupts generated by histogram block.

MDP_VG1_HIST_INTR_CLEAR

Bits	Name	Description
31:2	RESERVED31_2	

MDP_VG1_HIST_INTR_CLEAR (cont.)

Bits	Name	Description
1	HIST_DONE	Write (1) to this bit to clear the status.
0	RESET_SEQ_DONE	Write (1) to this bit to clear the status.

0x0512601C MDP_VG1_HIST_INTR_ENABLE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG1_HIST_INTR_ENABLE is used to enable the interrupt sources within the histogram block.

MDP_VG1_HIST_INTR_ENABLE

Bits	Name	Description
31:2	RESERVED31_2	
1	HIST_DONE	Write (1) to this bit to enable the interrupt source.
0	RESET_SEQ_DONE	Write (1) to this bit to enable the interrupt source.

0x05126020 MDP_VG1_HIST_STOP_REQ

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_VG1_HIST_STOP_REQ kicks off a histogram operation stop request which is stopping HIST HW at the end of frame even if the frame count is less than programmed frame count.

MDP_VG1_HIST_STOP_REQ

Bits	Name	Description
31:0	STOP_REQ	Writing to this register kicks off a stop request which is stopping HIST HW at the end of frame even if the processed frame count is less than programmed frame count.

0x05126024 MDP_VG1_HIST_CANCEL_REQ

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_VG1_HIST_CANCEL_REQ kicks off a histogram operation cancel request which is stopping HIST HW at any state rather than RESET state.

MDP_VG1_HIST_CANCEL_REQ

Bits	Name	Description
31:0	CANCEL_REQ	Writing to this register kicks off a cancel request which is stopping HIST HW at any state rather than RESET state.

0x05126028 MDP_VG1_HIST_EXTRA_INFO_0

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x007F_0000

The MDP_VG1_HIST_EXTRA_INFO_0 register provides histogram extra information. These values are only valid when HIST HW are IDLE state and this register values are reset automatically whenever HIST HW starts.

MDP_VG1_HIST_EXTRA_INFO_0

Bits	Name	Description
31	RESERVED31	
30:24	Y_MAX_VALUE	Maximum pixel value for component Y
23	RESERVED23	
22:16	Y_MIN_VALUE	Minimum pixel value for component Y
15:6	RESERVED15_6	
5:0	CUR_FRAME_COUNT	This value provides the processed number of frame from start to HIST_DONE.

0x05126200+4*n MDP_VG1_HIST_LUMA_DATAn, n=[0..127]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG1_HIST_LUMA_DATAn register provides the histogram data corresponding to the luma component.

MDP_VG1_HIST_LUMA_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_LUMA_DATA	Reading this register provides histogram bin data for luma.

0x05128000 MDP_VG1_SCALE_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_03FF

MDP_VG1_SCALE_STATUS

Bits	Name	Description
31:10	RESERVED31_10	
9:0	IDLES	Internal block idles

0x05128100+4*n MDP_VG1_QSEED_TABLE0_n, n=[0..3]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Each MDP_VG1_QSEED_TABLE0_n register space contains 16 table entries of QSEED Table0.

MDP_VG1_QSEED_TABLE0_n

Bits	Name	Description
31:30	ENTRY15	2 bit lookup value of Table0, entry n*16+15
29:28	ENTRY14	2 bit lookup value of Table0, entry n*16+14
27:26	ENTRY13	2 bit lookup value of Table0, entry n*16+13
25:24	ENTRY12	2 bit lookup value of Table0, entry n*16+12
23:22	ENTRY11	2 bit lookup value of Table0, entry n*16+11
21:20	ENTRY10	2 bit lookup value of Table0, entry n*16+10
19:18	ENTRY9	2 bit lookup value of Table0, entry n*16+9
17:16	ENTRY8	2 bit lookup value of Table0, entry n*16+8
15:14	ENTRY7	2 bit lookup value of Table0, entry n*16+7
13:12	ENTRY6	2 bit lookup value of Table0, entry n*16+6
11:10	ENTRY5	2 bit lookup value of Table0, entry n*16+5

MDP_VG1_QSEED_TABLE0_n (cont.)

Bits	Name	Description
9:8	ENTRY4	2 bit lookup value of Table0, entry n*16+4
7:6	ENTRY3	2 bit lookup value of Table0, entry n*16+3
5:4	ENTRY2	2 bit lookup value of Table0, entry n*16+2
3:2	ENTRY1	2 bit lookup value of Table0, entry n*16+1
1:0	ENTRY0	2 bit lookup value of Table0, entry n*16

0x05128200+4*n MDP_VG1_QSEED_TABLE1_n, n=[0..1]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Each MDP_VG1_QSEED_TABLE1_n register space contains 8 table entries of QSEED Table1. When source image is RGB, the gradient calculation is bypassed and only bicubic scaling applies. Thus, in such case, QSEED_TABLE1_0 entry 0 is used to select which bicubic coeffcient table set (out of XTABLE2) to used (U1, D0, D1, or D2 set) per scaling ratio range for X scaling. QSEED_TABLE1_0 entry 1 is used to select which bicubic coeffcient table set (out of YTABLE2) to used per scaling ratio range for Y scaling.

MDP_VG1_QSEED_TABLE1_n

Bits	Name	Description
31:28	ENTRY7	4 bit lookup value of Table1, entry n*8+7
27:24	ENTRY6	4 bit lookup value of Table1, entry n*8+6
23:20	ENTRY5	4 bit lookup value of Table1, entry n*8+5
19:16	ENTRY4	4 bit lookup value of Table1, entry n*8+4
15:12	ENTRY3	4 bit lookup value of Table1, entry n*8+3
11:8	ENTRY2	4 bit lookup value of Table1, entry n*8+2
7:4	ENTRY1	4 bit lookup value of Table1, entry n*8+1
3:0	ENTRY0	4 bit lookup value of Table1, entry n*8

0x05129000+8*n MDP_VG1_QSEED_XTABLE2_LSPn, n=[0..511]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG1_QSEED_TABLE2_LSPn register contains the Least Significant Portion of the whole coefficient word, i.e., coefficients for k-1 and k samples. Note, each coefficient value is aligned to 16-bit word boundary.

MDP_VG1_QSEED_XTABLE2_LSPn

Bits	Name	Description
31:28	RESERVED31_28	
27:16	COEFF1	12 bit (signed) poly-phase scale coefficient for k sample.
15:12	RESERVED15_12	
11:0	COEFF0	12 bit (signed) poly-phase scale coefficient for k-1 sample.

0x05129004+8*n MDP_VG1_QSEED_XTABLE2_MSPn, n=[0..511]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG1_QSEED_TABLE2_MSPn register contains the Most Significant Portion of the whole coefficient word, i.e., coefficients for k+1 and k+2 samples. Note, each coefficient value is aligned to 16-bit word boundary. The FIR coefficient tables should be written to in sequence of LSP write first followed by MSP write, writing from lower address to higher address. Each MSP register write actually triggers the write of whole 48-bit coefficient word into the RAM. There are actually 16 tables of 32 entries (phases) each. They are grouped from table 0 at the lowest addresses (0x27000-0x270fc) to table 15 at the highest addresses (0x27f00-0x27ffc).

MDP_VG1_QSEED_XTABLE2_MSPn

Bits	Name	Description
31:28	RESERVED31_28	
27:16	COEFF3	12 bit (signed) poly-phase scale coefficient for k+2 sample.
15:12	RESERVED15_12	
11:0	COEFF2	12 bit (signed) poly-phase scale coefficient for k+1 sample.

0x0512A000+8*n MDP_VG1_QSEED_YTABLE2_LSPn, n=[0..511]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG1_QSEED_TABLE2_LSPn register contains the Least Significant Portion of the whole coefficient word, i.e., coefficients for k-1 and k samples. Note, each coefficient value is aligned to 16-bit word boundary.

MDP_VG1_QSEED_YTABLE2_LSPn

Bits	Name	Description
31:28	RESERVED31_28	
27:16	COEFF1	12 bit (signed) poly-phase scale coefficient for k sample.
15:12	RESERVED15_12	
11:0	COEFF0	12 bit (signed) poly-phase scale coefficient for k-1 sample.

0x0512A004+ 8*n MDP_VG1_QSEED_YTABLE2_MSPn, n=[0..511]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG1_QSEED_TABLE2_MSPn register contains the Most Significant Portion of the whole coefficient word, i.e., coefficients for k+1 and k+2 samples. Note, each coefficient value is aligned to 16-bit word boundary. The FIR coefficient tables should be written to in sequence of LSP write first followed by MSP write, writing from lower address to higher address. Each MSP register write actually triggers the write of whole 48-bit coefficient word into the RAM. There are actually 16 tables of 32 entries (phases) each. They are grouped from table 0 at the lowest addresses (0x27000-0x270fc) to table 15 at the highest addresses (0x27f00-0x27ffc).

MDP_VG1_QSEED_YTABLE2_MSPn

Bits	Name	Description
31:28	RESERVED31_28	
27:16	COEFF3	12 bit (signed) poly-phase scale coefficient for k+2 sample.
15:12	RESERVED15_12	
11:0	COEFF2	12 bit (signed) poly-phase scale coefficient for k+1 sample.

14.15.12.4 Video/Graphics2 Input Pipe registers

0x05130000 MDP_VG2_SRC_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0020_0020

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_SRC_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	SRC_H	Height of input ROI data
15:12	RESERVED15_12	
11:0	SRC_W	Width of input ROI data

0x05130004 MDP_VG2_SRC_XY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This represents the offset from the top-left corner of the source image. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_SRC_XY

Bits	Name	Description
31:28	RESERVED31_28	
27:16	SRC_Y	Y offset of source ROI in the source image
15:12	RESERVED15_12	
11:0	SRC_X	X offset of source ROI in the source image

0x05130008 MDP_VG2_OUT_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0020_0020

If scale is not enabled, this register value will be ignored, and the hardware assumes that the output size is the same as SRC_SIZE register setting. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_OUT_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DST_H	Height of output ROI data
15:12	RESERVED15_12	

MDP_VG2_OUT_SIZE (cont.)

Bits	Name	Description
11:0	DST_W	Width of output ROI data

0x0513000C MDP_VG2_OUT_XY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This represents the offset from the top-left corner of the base layer image. If this pipe is processing the base layer then this register is all zeros. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_OUT_XY

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DST_Y	Y offset of this layer output in the Frame Buffer
15:12	RESERVED15_12	
11:0	DST_X	X offset of this layer output in the Frame Buffer

0x05130010 MDP_VG2_SRCP0_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_SRCP0_ADDR

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x05130014 MDP_VG2_SRCP1_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_SRCP1_ADDR

Bits	Name	Description
31:0	SRCP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x05130018 MDP_VG2_SRCP2_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_SRCP2_ADDR

Bits	Name	Description
31:0	SRCP2_ADDR	Base byte address of the Image's planar color2 plane.

0x0513001C MDP_VG2_SRCP3_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_SRCP3_ADDR

Bits	Name	Description
31:0	SRCP3_ADDR	Base byte address of the Image's color3 (alpha) component, used in pseudo planar + alpha format, or planar.

0x05130020 MDP_VG2_SRCP0_ADDR_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 1 is used for VG2 pipe.

MDP_VG2_SRCP0_ADDR_1

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x05130024 MDP_VG2_SRCP1_ADDR_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 1 is used for VG2 pipe.

MDP_VG2_SRCP1_ADDR_1

Bits	Name	Description
31:0	SRCP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x05130028 MDP_VG2_SRCP2_ADDR_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 1 is used for VG2 pipe.

MDP_VG2_SRCP2_ADDR_1

Bits	Name	Description
31:0	SRCP2_ADDR	Base byte address of the Image's planar color2 plane.

0x05130030 MDP_VG2_SRCP0_ADDR_2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 2 is used for VG2 pipe.

MDP_VG2_SRCP0_ADDR_2

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane, the luma component plane in pseudo-planar format, or planar color0 plane.

0x05130034 MDP_VG2_SRCP1_ADDR_2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 2 is used for VG2 pipe.

MDP_VG2_SRCP1_ADDR_2

Bits	Name	Description
31:0	SRCP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format, or planar color1 plane.

0x05130038 MDP_VG2_SRCP2_ADDR_2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 2 is used for VG2 pipe.

MDP_VG2_SRCP2_ADDR_2

Bits	Name	Description
31:0	SRCP2_ADDR	Base byte address of the Image's planar color2 plane.

0x05130040 MDP_VG2_SRC_YSTRIDE1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0060

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_SRC_YSTRIDE1

Bits	Name	Description
31	RESERVED31	
30:16	SRCP1_YSTRIDE	Plane 1 y stride in bytes.
15	RESERVED15	
14:0	SRCP0_YSTRIDE	Plane 0 y stride in bytes.

0x05130044 MDP_VG2_SRC_YSTRIDE2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_SRC_YSTRIDE2

Bits	Name	Description
31	RESERVED31	
30:16	SRCP3_YSTRIDE	Plane 3 y stride in bytes.
15	RESERVED15	
14:0	SRCP2_YSTRIDE	Plane 2 y stride in bytes.

0x05130048 MDP_VG2_SSTILE_FRAME_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x02D0_0500

The frame size of a whole super tile format frame is needed to calculate the proper addressing.

The minimum super tile height is 96.

MDP_VG2_SSTILE_FRAME_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	FRAME_H	Video Super Tile format frame height
15:12	RESERVED15_12	
11:0	FRAME_W	Video Super Tile format frame width

0x05130050 MDP_VG2_SRC_FORMAT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0002_44FF

This register describes the input surface for this pipe. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_SRC_FORMAT

Bits	Name	Description
31	RESERVED31	
30:29	FRAME_FORMAT	0x0: Linear, No tile (Default) 0x1: Reserved for ARGB 4x4 tile 0x2: Video in 64x32 supertile, YCbCr 420 only
28	SRC_CHROMA_SITE	Source chroma siting. 1 = offsite, 0 = cosite.
27:26	SRC_CHROMA_SAMP	Source chroma sampling: 0x0: 4:4:4/RGB 0x1: H2V1 0x2: H1V2 0x3: 4:2:0.
25:23	RESERVED25_23	
22	SOLID_FILL	If this bit is set (1), Fetch uses the CONSTANT_COLOR register value as its output. Nothing is fetched.
21	VC1_REDUCE	VC1 range reduction enable for YUV source, the reduce range is set by a separate register in the fetch.
20:19	FETCH_PLANES	Determines the number of planes to fetch: 0x0: Interleaved 0x1: Planar 0x2: pseudo planar
18	UNPACK_ALIGN	0x0: To LSB 0x1: To MSB
17	UNPACK_TIGHT	0x0: Loose 0x1: Tight
16:15	RESERVED16_15	
14:13	UNPACK_COUNT	Valid unpacking pattern count: 0 = 1 component, ..., 3 = 4 components. Unpacking pattern only applies to the interleaved plane (chroma plane in pseudo-planar).
12	ROT90	Source has been rotated 90 degree
11	RESERVED11	

MDP_VG2_SRC_FORMAT (cont.)

Bits	Name	Description
10:9	SRC_BPP	Effective source byte per pixel: 0 = 1 byte, 1 = 2 bytes, 2 = 3 bytes, 3 = 4 bytes. This is only used when unpacking the interleaved plane.
8	SRCC3_EN	0x1: Source has alpha
7:6	SRCC3	Number of bits for component 3 (alpha) input, this is not used for dither: 0 = 1 bit, 1 = 4 bits, 2 = 6 bits, 3 = 8 bits.
5:4	SRCC2	Number of bits for component 2 (R / Cr) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	SRCC1	Number of bits for component 1 (B / Cb) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	SRCC0	Number of bits for component 0 (G / luma) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x05130054 MDP_VG2_SRC_UNPACK_PATTERN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0302_0001

Unpacking pattern, maximum of 4 pattern elements starting from LSB to MSB (0 to 4). Default is ARGB or C3-C2-C0-C1. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_SRC_UNPACK_PATTERN

Bits	Name	Description
31:26	RESERVED31_26	
25:24	ELEMENT3	0x0: C0 0x1: C1 0x2: C2 0x3: C3
23:18	RESERVED23_18	
17:16	ELEMENT2	0x0: C0 0x1: C1 0x2: C2 0x3: C3
15:10	RESERVED15_10	
9:8	ELEMENT1	0x0: C0 0x1: C1 0x2: C2 0x3: C3

MDP_VG2_SRC_UNPACK_PATTERN (cont.)

Bits	Name	Description
7:2	RESERVED7_2	
1:0	ELEMENT0	0x0: C0 0x1: C1 0x2: C2 0x3: C3

0x05130058 MDP_VG2_OP_MODE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_OP_MODE

Bits	Name	Description
31:20	RESERVED31_20	
19	DEINT_ODD_REF	de-interlace uses Odd field as Reference when set.
18	DEINT_EN	de-interlace enable
17	HIST_LUT_EN	Component 0 LUT enable for histogram enhancement.
16	IGC_LUT_EN	Inverse Gamma Correction LUT enable. If disabled, the colors are mapped linearly from 8-bit to 12-bit.
15	DITHER_EN	Dither enable.
14:13	FLIP_MODE	Flip operation: Bit 1: Left/right flip Bit 2: Up/down flip
12	RESERVED12	
11	CSC_EN	This enables the color matrix conversion.
10	DST_DATA_FORMAT	Color converter output data format setting: 0x0: RGB 0x1: YCbCr
9	SRC_DATA_FORMAT	Color converter input data format setting: 0x0: RGB 0x1: YCbCr
8:6	RESERVED8_6	

MDP_VG2_OP_MODE (cont.)

Bits	Name	Description
5:4	SCALEY_UNIT_SEL	Select Polyphase FIR or M/N filter for Y scaler. M/N should be used at low-end of downscaling (between 1/8 and 1/4). Pixel Repeat is special scaling mode used for upscale only. Otherwise, QSEED should be selected in other cases. This field must be set to 0x0 when SCALEY_EN is 0x0. 0x0: FIR (QSEED) 0x1: M/N phase-controlled 0x2: Pixel Repeat
3:2	SCALEX_UNIT_SEL	Select Polyphase FIR or M/N filter for X scaler. M/N should be used at low-end of downscaling (between 1/8 and 1/4). Pixel Repeat is special scaling mode used for upscale only. Otherwise, QSEED should be selected in other cases. This field must be set to 0x0 when SCALEX_EN is 0x0. 0x0: FIR (QSEED) 0x1: M/N phase-controlled 0x2: Pixel Repeat
1	SCALEY_EN	Y scaling enable
0	SCALEX_EN	X scaling enable

0x0513005C MDP_VG2_SCALE_PHASEX_STEP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_SCALE_PHASEX_STEP

Bits	Name	Description
31:0	PHASEX_STEP	X phase step for scaling, which is input width/output width in u3.29, i.e., (src_size / out_size)<<29, phase step of 8 (1/8 scale) is encoded by setting this value to 0 (representing 0x1_0000_0000).

0x05130060 MDP_VG2_SCALE_PHASEY_STEP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_VG2_SCALE_PHASEY_STEP

Bits	Name	Description
31:0	PHASEY_STEP	Y phase step for scaling, which is input height/output height in u3.29, i.e., (src_size / out_size)<<29, phase step of 8 (1/8 scale) is encoded by setting this value to 0 (representing 0x1_0000_0000).

0x05130064 MDP_VG2_HIST_LUT_SEL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation for internal use.

MDP_VG2_HIST_LUT_SEL

Bits	Name	Description
31:1	RESERVED31_1	
0	LUT_SEL	Selects which LUT to use for histogram enhancement 0x0: Set1 0x1: Set2

0x05130068 MDP_VG2_DITHER_STRENGTH

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_003F

MDP_VG2_DITHER_STRENGTH

Bits	Name	Description
31:6	RESERVED31_6	
5:4	C2_BITS	Number of MSBits on component 2 (R/Cr) to indicate the dithering boundary: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	C1_BITS	Number of MSBits on component 1 (B/Cb) to indicate the dithering boundary: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	C0_BITS	Number of MSBits on component 0 (G/Y) to indicate the dithering boundary: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x05131000 MDP_VG2_FETCH_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_003F

MDP_VG2_FETCH_STATUS

Bits	Name	Description
31:12	RESERVED31_12	
11:8	FIFO_ERRORS	TileFetch internal FIFO errors. These error bits are pulse catching, and returned to zero when this register is read: Bit 11= control FIFO error Bit 10= burstbuf FIFO error Bit 9= line_gen luma FIFO error Bit 8= line_gen chroma FIFO error
7:6	RESERVED7_6	
5:0	IDLES	TileFetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 5= dma_rd idle Bit 4= ctl idle Bit 3= burstbuf idle Bit 2= unpack idle Bit 1= unpack chroma idle Bit 0= line_gen idle

0x05131004 MDP_VG2_FETCH_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0047

MDP_VG2_FETCH_CFG

Bits	Name	Description
31:9	RESERVED31_9	
8	ADDR_SYNC_MODE	Boundary on which fetch address synchronizes: 0x0: frame (default) 0x1: line
7	FETCH_OPT_EN	Fetch Optimization Enable. Fetch optimization is supported only for interleave RGB formats. This setting is ignored when in others. 0x0: Disable (default) 0x1: Enable

MDP_VG2_FETCH_CFG (cont.)

Bits	Name	Description
6:4	MAX_BURST_SIZE	Maximum burst beat size. Possible values: 0x4: 16 (default) 0x2: 8 0x1: 4
3	RESERVED3	
2:0	REQ_DEPTH_LIMIT	Pending request limit, default max value of 0x7 means maximum pending requests allowed in the design, anything less limits the bus requests to that number + 1.

0x05131008 MDP_VG2_CONSTANT_COLOR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0xFFFF_FFFF

MDP_VG2_CONSTANT_COLOR

Bits	Name	Description
31:24	COLOR3	Constant color driven for color3 during solid fill mode.
23:16	COLOR2	Constant color driven for color2 during solid fill mode.
15:8	COLOR1	Constant color driven for color1 during solid fill mode.
7:0	COLOR0	Constant color driven for color0 during solid fill mode.

0x0513100C MDP_VG2_FETCH_COUNT

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_VG2_FETCH_COUNT

Bits	Name	Description
31:28	RESERVED31_28	
27:16	CHROMA_LINE	Current chroma line number
15:12	RESERVED15_12	
11:0	LUMA_LINE	Current luma line number

0x05131010 MDP_VG2_FETCH_STATISTIC

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_VG2_FETCH_STATISTIC

Bits	Name	Description
31:13	FETCH_KCYCLES	Accumulated kilo-cycles spent in wait for read data in the current frame.
12:0	FETCH_KBYTES	Accumulated KByte received in the current frame.

0x05131020 MDP_VG2_VC1_RANGE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0707

MDP_VG2_VC1_RANGE

Bits	Name	Description
31:11	RESERVED31_11	
10:8	RANGE_MAPUV	Chroma range map for VC1 range reduction, default of 7 is equivalent to setting it for main profile.
7:3	RESERVED7_3	
2:0	RANGE_MAPY	Luma range map for VC1 range reduction, default of 7 is equivalent to setting it for main profile.

0x05132000 MDP_VG2_DEINT_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000F

MDP_VG2_DEINT_STATUS

Bits	Name	Description
31:4	RESERVED31_4	
3:0	IDLES	Internal idles

0x05132004 MDP_VG2_DEINT_DECISION

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0003_0032

MDP_VG2_DEINT_DECISION

Bits	Name	Description
31:19	RESERVED31_19	
18:16	ATTENU	Attenuation (the shift value) for less temporal resolution; valid range is 0
15:11	RESERVED15_11	
10:0	THRESH	Threshold (u11) for de-interlace attenuation decision

0x05132010 MDP_VG2_DEINT_COEFF0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0360_03E0

The MDP_VG2_DEINT_COEFFn registers contain the set of luma filter coefficients, where w3 is for the center pixel, w2 is for (+1, -1) pixels, w1 is for (+2, -2) pixels, and w0 is for (+3, -3) pixels.

MDP_VG2_DEINT_COEFF0

Bits	Name	Description
31:26	RESERVED31_26	
25:16	COEFF1	Luma filter coefficient w1 (s10 Q5).
15:10	RESERVED31_10	
9:0	COEFF0	Luma filter coefficient w0 (s10 Q5).

0x05132014 MDP_VG2_DEINT_COEFF1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0140_0120

The MDP_VG2_DEINT_COEFFn registers contain the set of luma filter coefficients, where w3 is for the center pixel, w2 is for (+1, -1) pixels, w1 is for (+2, -2) pixels, and w0 is for (+3, -3) pixels.

MDP_VG2_DEINT_COEFF1

Bits	Name	Description
31:26	RESERVED31_26	
25:16	COEFF1	Luma filter coefficient w3 (s10 Q5).
15:10	RESERVED31_10	
9:0	COEFF0	Luma filter coefficient w2 (s10 Q5).

0x05133400+ 4*n MDP_VG2_HIST_LUT1n, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG2_HIST_LUT1n registers contains the color lookup values for histogram enhancement set1.

MDP_VG2_HIST_LUT1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	LUT_COLOR0	LUT value for color0.

0x05133800+ 4*n MDP_VG2_HIST_LUT2n, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG2_HIST_LUT2n registers contains the color lookup values for histogram enhancement set2.

MDP_VG2_HIST_LUT2n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	LUT_COLOR0	LUT value for color0.

0x05134400+ 4*n MDP_VG2_CSC_MV1n, n=[0..8]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG2_CSC_MV1n register contains the set1 matrix vector.

MDP_VG2_CSC_MV1n

Bits	Name	Description
31:13	RESERVED31_13	
12:0	MV1	MV1 = Matrix vector set1 (s4.9). Matrices are indexed left to right, top to bottom. That is, row 1, col 0 index = 3 (index range - 0 to 8).

0x05134500+ 4*n MDP_VG2_CSC_PRE_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG2_CSC_PRE_BV1n register contains the set1 pre-bias vector.

MDP_VG2_CSC_PRE_BV1n

Bits	Name	Description
31:9	RESERVED31_9	
8:0	PRE_BV1	PRE_BV1= Pre-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x05134580+ 4*n MDP_VG2_CSC_POST_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG2_CSC_POST_BV1n register contains the set1 post-bias vector.

MDP_VG2_CSC_POST_BV1n

Bits	Name	Description
31:9	RESERVED31_9	
8:0	POST_BV1	POST_BV1 = Post-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x05134600+ 4*n MDP_VG2_CSC_PRE_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG2_CSC_PRE_LV1n register contains the set1 pre-limit vector.

MDP_VG2_CSC_PRE_LV1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	PRE_LV1	PRE_LV1 = Pre-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x05134680+ 4*n MDP_VG2_CSC_POST_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG2_CSC_POST_LV1n register contains the set1 post-limit vector.

MDP_VG2_CSC_POST_LV1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	POST_LV1	POST_LV1 = Post-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x05135000+ 4*n MDP_VG2_IGC_LSP_LUTn, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG2_IGC_LSP_LUTn registers contains the Least Significant Portion (lower 24 bits of total 36 bits) of the color lookup values for IGC LUT.

MDP_VG2_IGC_LSP_LUTn

Bits	Name	Description
31:28	RESERVED31_28	

MDP_VG2_IGC_LSP_LUTn (cont.)

Bits	Name	Description
27:16	LUT_COLOR1	LUT value for color1.
15:12	RESERVED15_12	
11:0	LUT_COLOR0	LUT value for color0.

0x05135800+4*n MDP_VG2_IGC_MSP_LUTn, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG2_IGC_MSP_LUTn registers contains the most significant portion (color component 2) of the color lookup values for IGC LUT. The whole LUT should be written to in the sequence of LSP write first followed by MSP write, writing from lower address to higher address. Each MSP register write actually triggers the write of whole 36-bit LUT entry into the RAM.

MDP_VG2_IGC_MSP_LUTn

Bits	Name	Description
31:12	RESERVED31_12	
11:0	LUT_COLOR2	LUT value for color2.

0x05136000 MDP_VG2_HIST_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_VG2_HIST_START register kicks off histogram generation.

MDP_VG2_HIST_START

Bits	Name	Description
31:0	HIST_START	A write to this register kicks off histogram generation. Actual accumulation begins at the start of next ROI. Histogram accumulation can be started only when histogram reset sequence is not currently active.

0x05136004 MDP_VG2_HIST_FRAME_CNT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0001

The MDP_VG2_HIST_FRAME_CNT register is used to program the frame count for histogram accumulation.

MDP_VG2_HIST_FRAME_CNT

Bits	Name	Description
31:6	RESERVED31_6	
5:0	FRAME_CNT	Program the number of frames over which the histogram data has to be collected. If the frame count programmed is more than what each 24-bit bin can support, the bin count will saturate at the maximum value. Here are some max. frame counts that can be programmed for different image sizes for a 24-bit bin. XGA (1024 x 768) - 21 WSVGA (1024 x 600) - 27 WVGA (800 x 480) - 43 VGA (640 x 480) - 54

0x0513600C MDP_VG2_HIST_RESET_SEQ_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_VG2_HIST_RESET_SEQ_START kicks off a reset sequence.

MDP_VG2_HIST_RESET_SEQ_START

Bits	Name	Description
31:0	RESET_SEQ_START	Writing to this register kicks off a reset sequence.This reset sequence clears all RAM locations and RAM rd/wr pointers. The reset sequence can be initiated only when histogram generation is not currently active. Note: Functional clock gating will shut off the clock to VG2 sub-blocks when a ROI is not being processed. So VG2 clock should be forced ON for the reset sequence to complete.

0x05136010 MDP_VG2_HIST_CONTROL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG2_HIST_CONTROL register controls histogram operation.

MDP_VG2_HIST_CONTROL

Bits	Name	Description
31:1	RESERVED31_1	
0	AUTO_CLEAR_EN	When set (1), the bin from which data has been read is cleared automatically.

0x05136014 MDP_VG2_HIST_INTR_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG2_HIST_INTR_STATUS register provides histogram interrupt status.

MDP_VG2_HIST_INTR_STATUS

Bits	Name	Description
31:2	RESERVED31_2	
1	HIST_DONE	When set (1) implies histogram generation is complete.
0	RESET_SEQ_DONE	When set (1) implies the reset sequence is complete.

0x05136018 MDP_VG2_HIST_INTR_CLEAR

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_VG2_HIST_INTR_CLEAR is used to clear the interrupts generated by histogram block.

MDP_VG2_HIST_INTR_CLEAR

Bits	Name	Description
31:2	RESERVED31_2	

MDP_VG2_HIST_INTR_CLEAR (cont.)

Bits	Name	Description
1	HIST_DONE	Write (1) to this bit to clear the status.
0	RESET_SEQ_DONE	Write (1) to this bit to clear the status.

0x0513601C MDP_VG2_HIST_INTR_ENABLE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_VG2_HIST_INTR_ENABLE is used to enable the interrupt sources within the histogram block.

MDP_VG2_HIST_INTR_ENABLE

Bits	Name	Description
31:2	RESERVED31_2	
1	HIST_DONE	Write (1) to this bit to enable the interrupt source.
0	RESET_SEQ_DONE	Write (1) to this bit to enable the interrupt source.

0x05136020 MDP_VG2_HIST_STOP_REQ

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_VG2_HIST_STOP_REQ kicks off a histogram operation stop request which is stopping HIST HW at the end of frame even if the frame count is less than programmed frame count.

MDP_VG2_HIST_STOP_REQ

Bits	Name	Description
31:0	STOP_REQ	Writing to this register kicks off a stop request which is stopping HIST HW at the end of frame even if the processed frame count is less than programmed frame count.

0x05136024 MDP_VG2_HIST_CANCEL_REQ

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_VG2_HIST_CANCEL_REQ kicks off a histogram operation cancel request which is stopping HIST HW at any state rather than RESET state.

MDP_VG2_HIST_CANCEL_REQ

Bits	Name	Description
31:0	CANCEL_REQ	Writing to this register kicks off a cancel request which is stopping HIST HW at any state rather than RESET state.

0x05136028 MDP_VG2_HIST_EXTRA_INFO_0

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x007F_0000

The MDP_VG2_HIST_EXTRA_INFO_0 register provides histogram extra information. These values are only valid when HIST HW are IDLE state and this register values are reset automatically whenever HIST HW starts.

MDP_VG2_HIST_EXTRA_INFO_0

Bits	Name	Description
31	RESERVED31	
30:24	Y_MAX_VALUE	Maximum pixel value for component Y
23	RESERVED23	
22:16	Y_MIN_VALUE	Minimum pixel value for compound Y
15:6	RESERVED15_6	
5:0	CUR_FRAME_COUNT	This value provides the processed number of frame from start to HIST_DONE.

0x05136200+4*n MDP_VG2_HIST_LUMA_DATAn, n=[0..127]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG2_HIST_LUMA_DATAn register provides the histogram data corresponding to the luma component.

MDP_VG2_HIST_LUMA_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_LUMA_DATA	Reading this register provides histogram bin data for luma.

0x05138000 MDP_VG2_SCALE_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_03FF

MDP_VG2_SCALE_STATUS

Bits	Name	Description
31:10	RESERVED31_10	
9:0	IDLES	Internal block idles

0x05138100+4*n MDP_VG2_QSEED_TABLE0_n, n=[0..3]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Each MDP_VG2_QSEED_TABLE0_n register space contains 16 table entries of QSEED Table0.

MDP_VG2_QSEED_TABLE0_n

Bits	Name	Description
31:30	ENTRY15	2 bit lookup value of Table0, entry n*16+15
29:28	ENTRY14	2 bit lookup value of Table0, entry n*16+14
27:26	ENTRY13	2 bit lookup value of Table0, entry n*16+13
25:24	ENTRY12	2 bit lookup value of Table0, entry n*16+12
23:22	ENTRY11	2 bit lookup value of Table0, entry n*16+11
21:20	ENTRY10	2 bit lookup value of Table0, entry n*16+10
19:18	ENTRY9	2 bit lookup value of Table0, entry n*16+9
17:16	ENTRY8	2 bit lookup value of Table0, entry n*16+8
15:14	ENTRY7	2 bit lookup value of Table0, entry n*16+7
13:12	ENTRY6	2 bit lookup value of Table0, entry n*16+6
11:10	ENTRY5	2 bit lookup value of Table0, entry n*16+5

MDP_VG2_QSEED_TABLE0_n (cont.)

Bits	Name	Description
9:8	ENTRY4	2 bit lookup value of Table0, entry n*16+4
7:6	ENTRY3	2 bit lookup value of Table0, entry n*16+3
5:4	ENTRY2	2 bit lookup value of Table0, entry n*16+2
3:2	ENTRY1	2 bit lookup value of Table0, entry n*16+1
1:0	ENTRY0	2 bit lookup value of Table0, entry n*16

0x05138200+4*n MDP_VG2_QSEED_TABLE1_n, n=[0..1]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Each MDP_VG2_QSEED_TABLE1_n register space contains 8 table entries of QSEED Table1. When source image is RGB, the gradient calculation is bypassed and only bicubic scaling applies. Thus, in such case, QSEED_TABLE1_0 entry 0 is used to select which bicubic coefficient table set (out of XTABLE2) to used (U1, D0, D1, or D2 set) per scaling ratio range for X scaling. QSEED_TABLE1_0 entry 1 is used to select which bicubic coefficient table set (out of YTABLE2) to used per scaling ratio range for Y scaling.

MDP_VG2_QSEED_TABLE1_n

Bits	Name	Description
31:28	ENTRY7	4 bit lookup value of Table1, entry n*8+7
27:24	ENTRY6	4 bit lookup value of Table1, entry n*8+6
23:20	ENTRY5	4 bit lookup value of Table1, entry n*8+5
19:16	ENTRY4	4 bit lookup value of Table1, entry n*8+4
15:12	ENTRY3	4 bit lookup value of Table1, entry n*8+3
11:8	ENTRY2	4 bit lookup value of Table1, entry n*8+2
7:4	ENTRY1	4 bit lookup value of Table1, entry n*8+1
3:0	ENTRY0	4 bit lookup value of Table1, entry n*8

0x05139000+8*n MDP_VG2_QSEED_XTABLE2_LSPn, n=[0..511]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG2_QSEED_TABLE2_LSPn register contains the Least Significant Portion of the whole coefficient word, i.e., coefficients for k-1 and k samples. Note, each coefficient value is aligned to 16-bit word boundary.

MDP_VG2_QSEED_XTABLE2_LSPn

Bits	Name	Description
31:28	RESERVED31_28	
27:16	COEFF1	12 bit (signed) poly-phase scale coefficient for k sample.
15:12	RESERVED15_12	
11:0	COEFF0	12 bit (signed) poly-phase scale coefficient for k-1 sample.

0x05139004+ 8*n MDP_VG2_QSEED_XTABLE2_MSPn, n=[0..511]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG2_QSEED_TABLE2_MSPn register contains the Most Significant Portion of the whole coefficient word, i.e., coefficients for k+1 and k+2 samples. Note, each coefficient value is aligned to 16-bit word boundary. The FIR coefficient tables should be written to in sequence of LSP write first followed by MSP write, writing from lower address to higher address. Each MSP register write actually triggers the write of whole 48-bit coefficient word into the RAM. There are actually 16 tables of 32 entries (phases) each. They are grouped from table 0 at the lowest addresses (0x37000-0x370fc) to table 15 at the highest addresses (0x37f00-0x37ffc).

MDP_VG2_QSEED_XTABLE2_MSPn

Bits	Name	Description
31:28	RESERVED31_28	
27:16	COEFF3	12 bit (signed) poly-phase scale coefficient for k+2 sample.
15:12	RESERVED15_12	
11:0	COEFF2	12 bit (signed) poly-phase scale coefficient for k+1 sample.

0x0513A000+ 8*n MDP_VG2_QSEED_YTABLE2_LSPn, n=[0..511]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG2_QSEED_TABLE2_LSPn register contains the Least Significant Portion of the whole coefficient word, i.e., coefficients for k-1 and k samples. Note, each coefficient value is aligned to 16-bit word boundary.

MDP_VG2_QSEED_YTABLE2_LSPn

Bits	Name	Description
31:28	RESERVED31_28	
27:16	COEFF1	12 bit (signed) poly-phase scale coefficient for k sample.
15:12	RESERVED15_12	
11:0	COEFF0	12 bit (signed) poly-phase scale coefficient for k-1 sample.

0x0513A004+ 8*n MDP_VG2_QSEED_YTABLE2_MSPn, n=[0..511]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_VG2_QSEED_TABLE2_MSPn register contains the Most Significant Portion of the whole coefficient word, i.e., coefficients for k+1 and k+2 samples. Note, each coefficient value is aligned to 16-bit word boundary. The FIR coefficient tables should be written to in sequence of LSP write first followed by MSP write, writing from lower address to higher address. Each MSP register write actually triggers the write of whole 48-bit coefficient word into the RAM. There are actually 16 tables of 32 entries (phases) each. They are grouped from table 0 at the lowest addresses (0x37000-0x370fc) to table 15 at the highest addresses (0x37f00-0x37ffc).

MDP_VG2_QSEED_YTABLE2_MSPn

Bits	Name	Description
31:28	RESERVED31_28	
27:16	COEFF3	12 bit (signed) poly-phase scale coefficient for k+2 sample.
15:12	RESERVED15_12	
11:0	COEFF2	12 bit (signed) poly-phase scale coefficient for k+1 sample.

14.15.12.5 RGB1 Input Pipe registers

0x05140000 MDP_RGB1_SRC_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0020_0020

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB1_SRC_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	SRC_H	Height of input ROI data
15:12	RESERVED15_12	
11:0	SRC_W	Width of input ROI data

0x05140004 MDP_RGB1_SRC_XY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This represents the offset from the top-left corner of the source image. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB1_SRC_XY

Bits	Name	Description
31:28	RESERVED31_28	
27:16	SRC_Y	Y offset of source ROI in the source image
15:12	RESERVED15_12	
11:0	SRC_X	X offset of source ROI in the source image

0x05140008 MDP_RGB1_OUT_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0020_0020

If scale is not enabled, this register value will be ignored, and the hardware assumes that the output size is the same as SRC_SIZE register setting. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB1_OUT_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DST_H	Height of output ROI data
15:12	RESERVED15_12	

MDP_RGB1_OUT_SIZE (cont.)

Bits	Name	Description
11:0	DST_W	Width of output ROI data

0x0514000C MDP_RGB1_OUT_XY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This represents the offset from the top-left corner of the base layer image. If this pipe is processing the base layer then this register is all zeros. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB1_OUT_XY

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DST_Y	Y offset of this layer output in the Frame Buffer
15:12	RESERVED15_12	
11:0	DST_X	X offset of this layer output in the Frame Buffer

0x05140010 MDP_RGB1_SRCP0_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB1_SRCP0_ADDR

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane.

0x05140014 MDP_RGB1_SRCP0_ADDR_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 1 is used for RGB1 pipe.

MDP_RGB1_SRCP0_ADDR_1

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane.

0x05140018 MDP_RGB1_SRCP0_ADDR_2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 2 is used for RGB1 pipe.

MDP_RGB1_SRCP0_ADDR_2

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane.

0x05140040 MDP_RGB1_SRC_YSTRIDE1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0060

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB1_SRC_YSTRIDE1

Bits	Name	Description
31:15	RESERVED31_15	
14:0	SRCP0_YSTRIDE	Plane 0 y stride in bytes.

0x05140050 MDP_RGB1_SRC_FORMAT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0002_44FF

This register describes the input surface for this pipe. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB1_SRC_FORMAT

Bits	Name	Description
31:23	RESERVED31_23	
22	SOLID_FILL	If this bit is set (1), Fetch uses the CONSTANT_COLOR register value as its output. Nothing is fetched.
21:19	RESERVED21_19	
18	UNPACK_ALIGN	0x0: To LSB 0x1: To MSB
17	UNPACK_TIGHT	0x0: Loose 0x1: Tight
16:15	RESERVED16_15	
14:13	UNPACK_COUNT	Valid unpacking pattern count: 0 = 1 component,..., 3 = 4 components. Unpacking pattern only applies to the interleaved plane (chroma plane in pseudo-planar).
12	RESERVED12	
11	RESERVED11	
10:9	SRC_BPP	Effective source byte per pixel: 0 = 1 byte, 1 = 2 bytes, 2 = 3 bytes, 3 = 4 bytes. This is only used when unpacking the interleaved plane.
8	SRCC3_EN	0x1: Source has alpha
7:6	SRCC3	Number of bits for component 3 (alpha) input, this is not used for dither: 0 = 1 bit, 1 = 4 bits, 2 = 6 bits, 3 = 8 bits.
5:4	SRCC2	Number of bits for component 2 (R / Cr) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	SRCC1	Number of bits for component 1 (B / Cb) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	SRCC0	Number of bits for component 0 (G / luma) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x05140054 MDP_RGB1_SRC_UNPACK_PATTERN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0302_0001

Unpacking pattern, maximum of 4 pattern elements starting from LSB to MSB (0 to 4). Default is ARGB or C3-C2-C0-C1. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB1_SRC_UNPACK_PATTERN

Bits	Name	Description
31:26	RESERVED31_26	
25:24	ELEMENT3	0x0: C0 0x1: C1 0x2: C2 0x3: C3
23:18	RESERVED23_18	
17:16	ELEMENT2	0x0: C0 0x1: C1 0x2: C2 0x3: C3
15:10	RESERVED15_10	
9:8	ELEMENT1	0x0: C0 0x1: C1 0x2: C2 0x3: C3
7:2	RESERVED7_2	
1:0	ELEMENT0	0x0: C0 0x1: C1 0x2: C2 0x3: C3

0x05140058 MDP_RGB1_OP_MODE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB1_OP_MODE

Bits	Name	Description
31:17	RESERVED31_17	
16	IGC_LUT_EN	Inverse Gamma Correction LUT enable. If disabled, the colors are mapped linearly from 8-bit to 12-bit.
15	RESERVED15	
14:13	FLIP_MODE	Flip operation: Bit 1: Left/right flip Bit 2: Up/down flip

MDP_RGB1_OP_MODE (cont.)

Bits	Name	Description
12:5	RESERVED12_5	
4	ENHANCED_MODE_EN	Enables enhanced RGB scaler mode. Turns on bilinear or new algorithm of pixel repeat/drop. When disabled RGB scaler operates in a legacy mode as it was in MDP4.0 and MDP4.1 0x1: enable 0x0: disabled
3	RGB_SCALE_METHOD	Scaling method for rgb components scaling. 0x1: Bilinear. 0x0: Pixel repeat/drop.
2	ALPHA_SCALE_METHOD	Scaling method for alpha component scaling. 0x1: Bilinear. 0x0: Pixel repeat/drop.
1	SCALEY_EN	Y scaling enable
0	SCALEX_EN	X scaling enable

0x0514005C MDP_RGB1_SCALE_PHASEX_STEP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB1_SCALE_PHASEX_STEP

Bits	Name	Description
31:0	PHASEX_STEP	X phase step for scaling, which is input width/output width in u3.29, i.e., (src_size / out_size)<<29.

0x05140060 MDP_RGB1_SCALE_PHASEY_STEP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB1_SCALE_PHASEY_STEP

Bits	Name	Description
31:0	PHASEY_STEP	Y phase step for scaling, which is input height/output height in u3.29, i.e., (src_size / out_size)<<29.

0x05141000 MDP_RGB1_FETCH_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_003F

MDP_RGB1_FETCH_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	TileFetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 5= dma_rd idle Bit 4 =setup idle Bit 3 = ctl idle Bit 2 = burst buf idle Bit 1 = unpack idle Bit 0 = out_gen idle

0x05141004 MDP_RGB1_FETCH_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0047

MDP_RGB1_FETCH_CFG

Bits	Name	Description
31:9	RESERVED31_9	
8	ADDR_SYNC_MODE	Boundary on which fetch address synchronizes: 0x0: frame (default) 0x1: line
7	FETCH_OPT_EN	Fetch Optimization Enable 0x0: Disabled (default) 0x1: Enabled

MDP_RGB1_FETCH_CFG (cont.)

Bits	Name	Description
6:4	MAX_BURST_SIZE	Maximum burst beat size. Possible values: 0x4: 16 (default) 0x2: 8 0x1: 4
3	RESERVED3	
2:0	REQ_DEPTH_LIMIT	Pending request limit, default 0x7 means maximum of 8 pending requests, anything less limits the AXI requests to that number + 1.

0x05141008 MDP_RGB1_CONSTANT_COLOR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0xFFFF_FFFF

MDP_RGB1_CONSTANT_COLOR

Bits	Name	Description
31:24	COLOR3	Constant color driven for color3 during solid fill mode.
23:16	COLOR2	Constant color driven for color2 during solid fill mode.
15:8	COLOR1	Constant color driven for color1 during solid fill mode.
7:0	COLOR0	Constant color driven for color0 during solid fill mode.

0x0514100C MDP_RGB1_FETCH_STATISTIC

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_RGB1_FETCH_STATISTIC

Bits	Name	Description
31:13	FETCH_KCYCLE	Accumulated KCycles spent in wait for read data in the current frame
12:0	FETCH_KBYTES	Accumulated KByte received in the current frame.

0x05145000+ 4*n MDP_RGB1_IGC_LSP_LUTn, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_RGB1_IGC_LSP_LUTn registers contains the Least Significant Portion (lower 24 bits of total 36 bits) of the color lookup values for IGC LUT.

MDP_RGB1_IGC_LSP_LUTn

Bits	Name	Description
31:28	RESERVED31_28	
27:16	LUT_COLOR1	LUT value for color1.
15:12	RESERVED15_12	
11:0	LUT_COLOR0	LUT value for color0.

0x05145800+ 4*n MDP_RGB1_IGC_MSP_LUTn, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_RGB1_IGC_MSP_LUTn registers contains the most significant portion (color component 2) of the color lookup values for IGC LUT. The whole LUT should be written to in the sequence of LSP write first followed by MSP write, writing from lower address to higher address. Each MSP register write actually triggers the write of whole 36-bit LUT entry into the RAM.

MDP_RGB1_IGC_MSP_LUTn

Bits	Name	Description
31:12	RESERVED31_12	
11:0	LUT_COLOR2	LUT value for color2.

14.15.12.6 RGB2 Input Pipe registers

0x05150000 MDP_RGB2_SRC_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0020_0020

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB2_SRC_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	SRC_H	Height of input ROI data
15:12	RESERVED15_12	
11:0	SRC_W	Width of input ROI data

0x05150004 MDP_RGB2_SRC_XY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This represents the offset from the top-left corner of the source image. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB2_SRC_XY

Bits	Name	Description
31:28	RESERVED31_28	
27:16	SRC_Y	Y offset of source ROI in the source image
15:12	RESERVED15_12	
11:0	SRC_X	X offset of source ROI in the source image

0x05150008 MDP_RGB2_OUT_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0020_0020

If scale is not enabled, this register value will be ignored, and the hardware assumes that the output size is the same as SRC_SIZE register setting. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB2_OUT_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DST_H	Height of output ROI data
15:12	RESERVED15_12	

MDP_RGB2_OUT_SIZE (cont.)

Bits	Name	Description
11:0	DST_W	Width of output ROI data

0x0515000C MDP_RGB2_OUT_XY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This represents the offset from the top-left corner of the base layer image. If this pipe is processing the base layer then this register is all zeros. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB2_OUT_XY

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DST_Y	Y offset of this layer output in the Frame Buffer
15:12	RESERVED15_12	
11:0	DST_X	X offset of this layer output in the Frame Buffer

0x05150010 MDP_RGB2_SRCP0_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB2_SRCP0_ADDR

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane.

0x05150014 MDP_RGB2_SRCP0_ADDR_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 1 is used for RGB2 pipe.

MDP_RGB2_SRCP0_ADDR_1

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane.

0x05150018 MDP_RGB2_SRCP0_ADDR_2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 2 is used for RGB2 pipe.

MDP_RGB2_SRCP0_ADDR_2

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane.

0x05150040 MDP_RGB2_SRC_YSTRIDE1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0060

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB2_SRC_YSTRIDE1

Bits	Name	Description
31:15	RESERVED31_15	
14:0	SRCP0_YSTRIDE	Plane 0 y stride in bytes.

0x05150050 MDP_RGB2_SRC_FORMAT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0002_44FF

This register describes the input surface for this pipe. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB2_SRC_FORMAT

Bits	Name	Description
31:23	RESERVED31_23	
22	SOLID_FILL	If this bit is set (1), Fetch uses the CONSTANT_COLOR register value as its output. Nothing is fetched.
21:19	RESERVED21_19	
18	UNPACK_ALIGN	0x0: To LSB 0x1: To MSB
17	UNPACK_TIGHT	0x0: Loose 0x1: Tight
16:15	RESERVED16_15	
14:13	UNPACK_COUNT	Valid unpacking pattern count: 0 = 1 component,..., 3 = 4 components. Unpacking pattern only applies to the interleaved plane (chroma plane in pseudo-planar).
12	RESERVED12	
11	RESERVED11	
10:9	SRC_BPP	Effective source byte per pixel: 0 = 1 byte, 1 = 2 bytes, 2 = 3 bytes, 3 = 4 bytes. This is only used when unpacking the interleaved plane.
8	SRCC3_EN	0x1: Source has alpha
7:6	SRCC3	Number of bits for component 3 (alpha) input, this is not used for dither: 0 = 1 bit, 1 = 4 bits, 2 = 6 bits, 3 = 8 bits.
5:4	SRCC2	Number of bits for component 2 (R / Cr) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	SRCC1	Number of bits for component 1 (B / Cb) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	SRCC0	Number of bits for component 0 (G / luma) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x05150054 MDP_RGB2_SRC_UNPACK_PATTERN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0302_0001

Unpacking pattern, maximum of 4 pattern elements starting from LSB to MSB (0 to 4). Default is ARGB or C3-C2-C0-C1. This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB2_SRC_UNPACK_PATTERN

Bits	Name	Description
31:26	RESERVED31_26	
25:24	ELEMENT3	0x0: C0 0x1: C1 0x2: C2 0x3: C3
23:18	RESERVED23_18	
17:16	ELEMENT2	0x0: C0 0x1: C1 0x2: C2 0x3: C3
15:10	RESERVED15_10	
9:8	ELEMENT1	0x0: C0 0x1: C1 0x2: C2 0x3: C3
7:2	RESERVED7_2	
1:0	ELEMENT0	0x0: C0 0x1: C1 0x2: C2 0x3: C3

0x05150058 MDP_RGB2_OP_MODE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB2_OP_MODE

Bits	Name	Description
31:17	RESERVED31_17	
16	IGC_LUT_EN	Inverse Gamma Correction LUT enable. If disabled, the colors are mapped linearly from 8-bit to 12-bit.
15	RESERVED15	
14:13	FLIP_MODE	Flip operation: Bit 1: Left/right flip Bit 2: Up/down flip

MDP_RGB2_OP_MODE (cont.)

Bits	Name	Description
12:5	RESERVED12_5	
4	ENHANCED_MODE_EN	Enables enhanced RGB scaler mode. Turns on bilinear or new algorithm of pixel repeat/drop. When disabled RGB scaler operates in a legacy mode as it was in MDP4.0 and MDP4.1 0x1: enable 0x0: disable
3	RGB_SCALE_METHOD	Scaling method for rgb components scaling. 0x1: Bilinear. 0x0: Pixel repeat/drop.
2	ALPHA_SCALE_METHOD	Scaling method for alpha component scaling. 0x1: Bilinear. 0x0: Pixel repeat/drop.
1	SCALEY_EN	Y scaling enable
0	SCALEX_EN	X scaling enable

0x0515005C MDP_RGB2_SCALE_PHASEX_STEP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB2_SCALE_PHASEX_STEP

Bits	Name	Description
31:0	PHASEX_STEP	X phase step for scaling, which is input width/output width in u3.29, i.e., (src_size / out_size)<<29.

0x05150060 MDP_RGB2_SCALE_PHASEY_STEP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every pipe start initiation.

MDP_RGB2_SCALE_PHASEY_STEP

Bits	Name	Description
31:0	PHASEY_STEP	Y phase step for scaling, which is input height/output height in u3.29, i.e., (src_size / out_size)<<29.

0x05151000 MDP_RGB2_FETCH_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_003F

MDP_RGB2_FETCH_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	TileFetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 5= dma_rd idle Bit 4 =setup idle Bit 3 = ctl idle Bit 2 = burst buf idle Bit 1 = unpack idle Bit 0 = out_gen idle

0x05151004 MDP_RGB2_FETCH_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0047

MDP_RGB2_FETCH_CFG

Bits	Name	Description
31:9	RESERVED31_9	
8	ADDR_SYNC_MODE	Boundary on which fetch address synchronizes: 0x0: frame (default) 0x1: line
7	FETCH_OPT_EN	Fetch Optimization Enabled 0x0: Disabled (default) 0x1: Enabled

MDP_RGB2_FETCH_CFG (cont.)

Bits	Name	Description
6:4	MAX_BURST_SIZE	Maximum burst beat size. Possible values: 0x4: 16 (default) 0x2: 8 0x1: 4
3	RESERVED3	
2:0	REQ_DEPTH_LIMIT	Pending request limit, default 0x7 means maximum of 8 pending requests, anything less limits the AXI requests to that number + 1.

0x05151008 MDP_RGB2_CONSTANT_COLOR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0xFFFF_FFFF

MDP_RGB2_CONSTANT_COLOR

Bits	Name	Description
31:24	COLOR3	Constant color driven for color3 during solid fill mode.
23:16	COLOR2	Constant color driven for color2 during solid fill mode.
15:8	COLOR1	Constant color driven for color1 during solid fill mode.
7:0	COLOR0	Constant color driven for color0 during solid fill mode.

0x0515100C MDP_RGB2_FETCH_STATISTIC

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_RGB2_FETCH_STATISTIC

Bits	Name	Description
31:13	FETCH_KCYCLE	Accumulated KCycles spent in wait for read data in the current frame
12:0	FETCH_KBYTES	Accumulated KByte received in the current frame.

0x05155000+ 4*n MDP_RGB2_IGC_LSP_LUTn, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_RGB2_IGC_LSP_LUTn registers contains the Least Significant Portion (lower 24 bits of total 36 bits) of the color lookup values for IGC LUT.

MDP_RGB2_IGC_LSP_LUTn

Bits	Name	Description
31:28	RESERVED31_28	
27:16	LUT_COLOR1	LUT value for color1.
15:12	RESERVED15_12	
11:0	LUT_COLOR0	LUT value for color0.

0x05155800+ 4*n MDP_RGB2_IGC_MSP_LUTn, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_RGB2_IGC_MSP_LUTn registers contains the most significant portion (color component 2) of the color lookup values for IGC LUT. The whole LUT should be written to in the sequence of LSP write first followed by MSP write, writing from lower address to higher address. Each MSP register write actually triggers the write of whole 36-bit LUT entry into the RAM.

MDP_RGB2_IGC_MSP_LUTn

Bits	Name	Description
31:12	RESERVED31_12	
11:0	LUT_COLOR2	LUT value for color2.

14.15.12.7 Layer Mixer 2

0x05188004 MDP_OVERLAYPROC2_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0008

This register configures the OVERLAY PROCESSOR 2's starting behavior. There is no way to configure the Overlay Processor 2 to drive a active display which is triggered by the incoming vysnc. As such all registers are reserved.

MDP_OVERLAYPROC2_CFG

Bits	Name	Description
31:6	RESERVED31_6	
5	RESERVED5	CON_WB_MODE CANNOT be tied to active panel.
4	RESERVED4	CON_WB_EN CANNOT be tied to active panel
3	BLT_MODE	Puts this Overlay Processor into BLT (MDP3) type of SW operation mode, which means the Overlay Processor will be fully controlled by the SW.
2:1	RESERVED2_1	REFRESH_MODE CANNOT be tied to active panel
0	RESERVED0	DIRECT_OUT field CANNOT be tied to active panel

0x05188008 MDP_OVERLAYPROC2_OUT_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0020_0020

This register designates the output size of the Overlay Processor 1 and is also used as the Frame Buffer/Active Region size for DMA_E or DMA_S.

MDP_OVERLAYPROC2_OUT_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DST_H	Output ROI height (pixel).
15:12	RESERVED15_12	
11:0	DST_W	Output ROI width (pixel).

0x0518800C MDP_OVERLAYPROC2_FB_ADDR1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This is the 1st Frame Buffer base address (for ping-ponging) that is used when this Overlay Processor is in Frame Buffer mode, where the value is registered and used at every other frame initiation of this Overlay Processor. In other modes, this is the only effective Frame Buffer base address used, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC2_FB_ADDR1

Bits	Name	Description
31:0	ADDR1	Starting base byte address for Frame Buffer. When overlay processor is in pseudo-planer format this register is used for Y plain in Frame buffer

0x05188010 MDP_OVERLAYPROC2_FB_STRIDE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC1_FB_STRIDE register defines the line jump value (in bytes) in the Frame Buffer.

MDP_OVERLAYPROC2_FB_STRIDE

Bits	Name	Description
31:29	RESERVED31_29	RESERVED
28:16	BUF_UV_STRIDE	UV-stride (or) line jump in bytes in the frame buffer. Used for UV components plane only when pseudo-planer write-back is enabled.
15:13	RESERVED15_13	RESERVED
12:0	BUF_Y_STRIDE	Y-stride (or) line jump in bytes in the Frame Buffer.

0x05188014 MDP_OVERLAYPROC2_OPMODE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x8000_0000

This register defines the output format of the Overlay Processor2..

MDP_OVERLAYPROC2_OPMODE

Bits	Name	Description
31	BYPASS_COLOR3_EN	Enables propagation of color component 3 to the packer 0x0: color3 is taken from register 0x1: color3 is propagated from the pipe
30:16	RESERVED30_16	RESERVED
15:8	ALPHA_COMP_XRGB	Programmable alpha component for xRGB write back. Used only in RGB8888 mode
7:5	RESERVED7_5	RESERVED
4	WR_BACK_PP	Enable to write to the frame buffer in YUV420 pseudo planer format. When YUV420PP writeback is required, this register must be set to 0x1 and FB_FORMAT must also be set to 0x2.
3	INTRLACE_FETCH	RESERVED
2	PGC_EN	Panel Gamma Correction enable. If disabled, the colors are mapped linearly from 12-bit to 8-bit.
1:0	FB_FORMAT	This field actually controls memory write back pixel format in LM2 with regard to operation mode. 0x0: RGB888 0x1: RGB565 0x2: 422 h2v1 interleaved 0x3: RGB8888

0x0518801C MDP_OVERLAYPROC2_FB_ADDR2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This is the 2nd Frame Buffer base address (for ping-ponging) that is used only when this Overlay Processor is in Frame Buffer mode. The value is registered and used at every other frame initiation of this Overlay Processor.

MDP_OVERLAYPROC2_FB_ADDR2

Bits	Name	Description
31:0	ADDR2	Starting base byte address for Frame Buffer. When the overlay processor is in pseudo-planer format this register is used for the secondary address of Y plane in the Frame buffer

0x05188020 MDP_OVERLAYPROC2_FB_UV_ADDR1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This is the Frame Buffer base address of the UV plane that is used only when this Overlay Processor is in Frame Buffer mode and pseudo planer output is enabled.

MDP_OVERLAYPROC2_FB_UV_ADDR1

Bits	Name	Description
31:0	UV_ADDR1	Starting base byte address for UV plane of the Frame Buffer

0x05188024 MDP_OVERLAYPROC2_FB_UV_ADDR2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Reserved

MDP_OVERLAYPROC2_FB_UV_ADDR2

Bits	Name	Description
31:0	UV_ADDR2	Second address of the UV stream. Reserved. Not used in the current implementation

0x05188028 MDP_OVERLAYPROC2_PROFILE_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_PROFILE_EN

Bits	Name	Description
31:1	RESERVED31_1	
0	EN	Enable the ROI cycle counter for profiling

0x0518802C MDP_OVERLAYPROC2_PROFILE_COUNT

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_PROFILE_COUNT

Bits	Name	Description
31:24	RESERVED31_24	
23:0	TOTAL_CYCLE	Total cycle count in a ROI, from new ROI to last pixel out of the processor (OVERLAYPROC1 goes back to Idle)

0x05188030 MDP_OVERLAYPROC2_PACK_PATTERN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0302_0100

NOTE The only source for "Color3" comes from ALPHA_COMPONENT provided in the register MDP_OVERLAYPROC2_OPMODE

MDP_OVERLAYPROC2_PACK_PATTERN

Bits	Name	Description
31:26	RESERVED31_26	UNUSED
25:24	ELEMENT3	0x0: Color0; 1:Color1; 2:Color2; 3:Color3
23:18	RESERVED23_18	UNUSED
17:16	ELEMENT2	0x0: Color0; 1:Color1; 2:Color2; 3:Color3
15:10	RESERVED15_10	UNUSED
9:8	ELEMENT1	0x0: Color0; 1:Color1; 2:Color2; 3:Color3
7:2	RESERVED7_2	UNUSED
1:0	ELEMENT0	0x0: Color0; 1:Color1; 2:Color2; 3:Color3

0x05188104 MDP_OVERLAYPROC2_BLEND0_OP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

This register describes the blend operation done by Layer Mixer on Stage 0 FG/BG, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC2_BLEND0_OP

Bits	Name	Description
31:10	RESERVED31_10	
9	BG_TRANSP_EN	BG transparency color check enable. When color matches, the FG pixel is passed; otherwise, the blended result is passed. However, if both FG and BG Transparency checks are enabled and both matches, BG pixel is passed.
8	FG_TRANSP_EN	FG transparency color check enable. When color matches, the BG pixel is passed; otherwise, the blended result is passed.
7	BG_MOD_ALPHA	When set (1), bg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
6	BG_INV_ALPHA	When set (1) the alpha selected by BG_ALPHA_SEL is inverted (1-alpha).
5:4	BG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha
3	FG_MOD_ALPHA	When set (1), fg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
2	FG_INV_ALPHA	When set (1) the alpha selected by FG_ALPHA_SEL is inverted (1-alpha).
1:0	FG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha

0x05188108 MDP_OVERLAYPROC2_BLEND0_FG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC2_BLEND0_FG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x0518810C MDP_OVERLAYPROC2_BLEND0_BG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC2_BLEND0_BG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x05188110 MDP_OVERLAYPROC2_BLEND0_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND0_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05188114 MDP_OVERLAYPROC2_BLEND0_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND0_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05188118 MDP_OVERLAYPROC2_BLEND0_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND0_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x0518811C MDP_OVERLAYPROC2_BLEND0_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND0_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05188124 MDP_OVERLAYPROC2_BLEND1_OP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

This register describes the blend operation done by Layer Mixer 0 on Stage 1 FG/BG, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC2_BLEND1_OP

Bits	Name	Description
31:10	RESERVED31_10	
9	BG_TRANSP_EN	BG transparency color check enable. When color matches, the FG pixel is passed; otherwise, the blended result is passed. However, if both FG and BG Transparency checks are enabled and both matches, BG pixel is passed.
8	FG_TRANSP_EN	FG transparency color check enable. When color matches, the BG pixel is passed; otherwise, the blended result is passed.
7	BG_MOD_ALPHA	When set (1), bg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
6	BG_INV_ALPHA	When set (1) the alpha selected by BG_ALPHA_SEL is inverted (1-alpha).
5:4	BG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha
3	FG_MOD_ALPHA	When set (1), fg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
2	FG_INV_ALPHA	When set (1) the alpha selected by FG_ALPHA_SEL is inverted (1-alpha).
1:0	FG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha

0x05188128 MDP_OVERLAYPROC2_BLEND1_FG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC2_BLEND1_FG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x0518812C MDP_OVERLAYPROC2_BLEND1_BG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC2_BLEND1_BG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x05188130 MDP_OVERLAYPROC2_BLEND1_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND1_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05188134 MDP_OVERLAYPROC2_BLEND1_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND1_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05188138 MDP_OVERLAYPROC2_BLEND1_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND1_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x0518813C MDP_OVERLAYPROC2_BLEND1_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND1_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05188144 MDP_OVERLAYPROC2_BLEND2_OP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

This register describes the blend operation done by Layer Mixer 0 on Stage 2 FG/BG, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC2_BLEND2_OP

Bits	Name	Description
31:10	RESERVED31_10	
9	BG_TRANSP_EN	BG transparency color check enable. When color matches, the FG pixel is passed; otherwise, the blended result is passed. However, if both FG and BG Transparency checks are enabled and both matches, BG pixel is passed.

MDP_OVERLAYPROC2_BLEND2_OP (cont.)

Bits	Name	Description
8	FG_TRANSP_EN	FG transparency color check enable. When color matches, the BG pixel is passed; otherwise, the blended result is passed.
7	BG_MOD_ALPHA	When set (1), bg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
6	BG_INV_ALPHA	When set (1) the alpha selected by BG_ALPHA_SEL is inverted (1-alpha).
5:4	BG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha
3	FG_MOD_ALPHA	When set (1), fg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
2	FG_INV_ALPHA	When set (1) the alpha selected by FG_ALPHA_SEL is inverted (1-alpha).
1:0	FG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha

0x05188148 MDP_OVERLAYPROC2_BLEND2_FG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC2_BLEND2_FG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x0518814C MDP_OVERLAYPROC2_BLEND2_BG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC2_BLEND2_BG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x05188150 MDP_OVERLAYPROC2_BLEND2_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND2_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05188154 MDP_OVERLAYPROC2_BLEND2_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND2_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05188158 MDP_OVERLAYPROC2_BLEND2_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND2_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x0518815C MDP_OVERLAYPROC2_BLEND2_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND2_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05188160 MDP_OVERLAYPROC2_BLEND3_OP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0040

This register describes the blend operation done by Layer Mixer 0 on Stage 0 FG/BG, where this register is Double Buffered and the value takes effect at the next refresh initiation of this Overlay Processor.

MDP_OVERLAYPROC2_BLEND3_OP

Bits	Name	Description
31:10	RESERVED31_10	
9	BG_TRANSP_EN	BG transparency color check enable. When color matches, the FG pixel is passed; otherwise, the blended result is passed. However, if both FG and BG Transparency checks are enabled and both matches, BG pixel is passed.

MDP_OVERLAYPROC2_BLEND3_OP (cont.)

Bits	Name	Description
8	FG_TRANSP_EN	FG transparency color check enable. When color matches, the BG pixel is passed; otherwise, the blended result is passed.
7	BG_MOD_ALPHA	When set (1), bg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
6	BG_INV_ALPHA	When set (1) the alpha selected by BG_ALPHA_SEL is inverted (1-alpha).
5:4	BG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha
3	FG_MOD_ALPHA	When set (1), fg constant alpha modulates the alpha selected by ALPHA_SEL before performing pixel blending.
2	FG_INV_ALPHA	When set (1) the alpha selected by FG_ALPHA_SEL is inverted (1-alpha).
1:0	FG_ALPHA_SEL	Blending alpha select: 0x0: fg constant alpha 0x1: bg constant alpha 0x2: fg per pixel alpha 0x3: bg per pixel alpha

0x05188164 MDP_OVERLAYPROC2_BLEND3_FG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_00FF

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC2_BLEND3_FG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x05188168 MDP_OVERLAYPROC2_BLEND3_BG_ALPHA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The value is shadowed at every refresh initiation of this Overlay Processor for internal used.

MDP_OVERLAYPROC2_BLEND3_BG_ALPHA

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Alpha value for constant alpha blend or modulation alpha.

0x0518816C MDP_OVERLAYPROC2_BLEND3_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND3_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05188170 MDP_OVERLAYPROC2_BLEND3_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND3_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05188174 MDP_OVERLAYPROC2_BLEND3_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND3_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x05188178 MDP_OVERLAYPROC2_BLEND3_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND3_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05188180 MDP_OVERLAYPROC2_BG_TRANSP_LOW0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BG_TRANSP_LOW0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check lower limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check lower limit for Color0

0x05188184 MDP_OVERLAYPROC2_BG_TRANSP_LOW1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BG_TRANSP_LOW1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check lower limit for Color2

0x05188188 MDP_OVERLAYPROC2_BG_TRANSP_HIGH0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BG_TRANSP_HIGH0

Bits	Name	Description
31:28	RESERVED31_28	
27:16	TRANSPARENCY_C1	Transparent color check high limit for Color1
15:12	RESERVED15_12	
11:0	TRANSPARENCY_C0	Transparent color check high limit for Color0

0x0518818C MDP_OVERLAYPROC2_BG_TRANSP_HIGH1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BG_TRANSP_HIGH1

Bits	Name	Description
31:12	RESERVED31_12	
11:0	TRANSPARENCY_C2	Transparent color check high limit for Color2

0x05188200 MDP_OVERLAYPROC2_CSC_CONFIG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_CSC_CONFIG register defines the color correct parameters at the output of the Overlay Processor 2.

MDP_OVERLAYPROC2_CSC_CONFIG

Bits	Name	Description
31:3	RESERVED31_3	
2	COLOR_FMT_OUT	Select the output color format after correction/conversion 0x0: RGB (default) 0x1: YCbCr
1	COLOR_FMT_IN	Select the input color format for correction/conversion 0x0: RGB (default) 0x1: YCbCr
0	CONVERT_MATRIX_EN	Enable color convert (matrix conversion).

0x05189000 MDP_OVERLAYPROC2_BLEND0_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000a

MDP_OVERLAYPROC2_BLEND0_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	Internal idles and valids

0x05189004 MDP_OVERLAYPROC2_BLEND0_COLOR3_OUT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND0_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED31_1	

MDP_OVERLAYPROC2_BLEND0_COLOR3_OUT (cont.)

Bits	Name	Description
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x05189400 MDP_OVERLAYPROC2_BLEND1_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000a

MDP_OVERLAYPROC2_BLEND1_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	Internal idles and valids

0x05189404 MDP_OVERLAYPROC2_BLEND1_COLOR3_OUT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND1_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED31_1	
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x05189800 MDP_OVERLAYPROC2_BLEND2_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000a

MDP_OVERLAYPROC2_BLEND2_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	Internal idles and valids

0x05189804 MDP_OVERLAYPROC2_BLEND2_COLOR3_OUT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND2_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED31_1	
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x05189C00 MDP_OVERLAYPROC2_BLEND3_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000a

MDP_OVERLAYPROC2_BLEND3_STATUS

Bits	Name	Description
31:6	RESERVED31_6	
5:0	IDLES	Internal idles and valids

0x05189C04 MDP_OVERLAYPROC2_BLEND3_COLOR3_OUT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_OVERLAYPROC2_BLEND3_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED31_1	

MDP_OVERLAYPROC2_BLEND3_COLOR3_OUT (cont.)

Bits	Name	Description
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x0518A400+ 4*n MDP_OVERLAYPROC2_CSC_MV1n, n=[0..8]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_OVERLAYPROC1_CSC_MV1n register contains the set1 matrix vector.

MDP_OVERLAYPROC2_CSC_MV1n

Bits	Name	Description
31:13	RESERVED31_13	
12:0	MV1	MV1 = Matrix vector set1 (s4.9). Matrices are indexed left to right, top to bottom. That is, row 1, col 0 index = 3 (index range - 0 to 8).

0x0518A500+ 4*n MDP_OVERLAYPROC2_CSC_PRE_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_OVERLAYPROC1_CSC_PRE_BV1n register contains the set1 pre-bias vector.

MDP_OVERLAYPROC2_CSC_PRE_BV1n

Bits	Name	Description
31:9	RESERVED31_9	
8:0	PRE_BV1	PRE_BV1= Pre-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x0518A580+ 4*n MDP_OVERLAYPROC2_CSC_POST_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_OVERLAYPROC1_CSC_POST_BV1n register contains the set1 post-bias vector.

MDP_OVERLAYPROC2_CSC_POST_BV1n

Bits	Name	Description
31:9	RESERVED31_9	
8:0	POST_BV1	POST_BV1 = Post-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x0518A600+ 4*n MDP_OVERLAYPROC2_CSC_PRE_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_OVERLAYPROC1_CSC_PRE_LV1n register contains the set1 pre-limit vector.

MDP_OVERLAYPROC2_CSC_PRE_LV1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	PRE_LV1	PRE_LV1 = Pre-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x0518A680+ 4*n MDP_OVERLAYPROC2_CSC_POST_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_OVERLAYPROC1_CSC_POST_LV1n register contains the set1 post-limit vector.

MDP_OVERLAYPROC2_CSC_POST_LV1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	POST_LV1	POST_LV1 = Post-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x0518C800+ 4*n MDP_OVERLAYPROC2_GC_START_COLOR_0_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component0.

MDP_OVERLAYPROC2_GC_START_COLOR_0_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x0518C880+ 4*n MDP_OVERLAYPROC2_GC_PARAM_COLOR_0_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component0.

MDP_OVERLAYPROC2_GC_PARAM_COLOR_0_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U3.12)

0x0518C900+ 4*n MDP_OVERLAYPROC2_GC_START_COLOR_1_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component1.

MDP_OVERLAYPROC2_GC_START_COLOR_1_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x0518C980+4*n MDP_OVERLAYPROC2_GC_PARAM_COLOR_1_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component1.

MDP_OVERLAYPROC2_GC_PARAM_COLOR_1_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U3.12)

0x0518CA00+4*n MDP_OVERLAYPROC2_GC_START_COLOR_2_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component2.

MDP_OVERLAYPROC2_GC_START_COLOR_2_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x0518CA80+4*n MDP_OVERLAYPROC2_GC_PARAM_COLOR_2_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component2.

MDP_OVERLAYPROC2_GC_PARAM_COLOR_2_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U3.12)

0x0518D004 MDP_OVERLAYPROC2_LSP_BORDER_COLOR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Least Significant Portion (lower 24 bits of total 36 bits) of border color values.

MDP_OVERLAYPROC2_LSP_BORDER_COLOR

Bits	Name	Description
31:28	RESERVED31_28	
27:16	BORDER_COLOR1	Border color value for color 1
15:12	RESERVED15_12	
11:0	BORDER_COLOR0	Border color value for color 0

0x0518D008 MDP_OVERLAYPROC2_MSP_BORDER_COLOR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Most Significant Portion (upper 12 bits of total 36 bits) of border color values.

MDP_OVERLAYPROC2_MSP_BORDER_COLOR

Bits	Name	Description
31:12	RESERVED31_12	
11:0	BORDER_COLOR2	Border color value for color 2

14.15.13 Primary Display Driver (DMA_P) registers

0x05190000 MDP_DMA_P_CONFIG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_2100

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MDP_DMA_P_CONFIG

Bits	Name	Description
31	RESERVED31	
30	PIGC_EN	Panel Inverse Panel Gamma Correction enable
29	PCC_EN	Polynomial Color Correction enable
28	PGC_EN	Panel Gamma Correction enable
27	BUF_FORMAT_EXTEND	In order to maintain SW backward compatible and support other input formats, this bit is added. Detail description is in the BUF_FORMAT field
26:25	BUF_FORMAT	The fetch buffer format setting (This field is only valid when Overlay Processor 0 is in BLT mode; otherwise this is not used, and the format is taken from FB_FORMAT in MDP_OVERLAYPROC0_OUT_OPMODE): If BUF_FORMAT_EXTEND is 0 (legacy mode + added format) If BUF_FORMAT_EXTEND is 1 (extended mode) 0x0: RGB888 format (Default) 0x1: RGB565 format 0x2: xRGB8888 format <new> 0x3: xRGB1555 format <new> 0x0: Reserved_1 0x1: Reserved_2 0x2: RGBx8888 format <new> 0x3: RGBx5551 format <new>
24	DITHER_EN	Dither enable
23:19	RESERVED23_19	

MDP_DMA_P_CONFIG (cont.)

Bits	Name	Description
18	BIT_MASK_POLARITY	Select the bit mask polarity. 0x0: Masked bits are set to `0' 0x1: Masked bits are set to `1'
17	RESERVED17	
16	COMP2_BIT_FLIP_EN	When set (1) flips all the bits of component2.
15	COMP1_BIT_FLIP_EN	When set (1) flips all the bits of component1.
14	COMP0_BIT_FLIP_EN	When set (1) flips all the bits of component0.
13:8	PACK_PATTERN	Packing pattern used by the packer. 0x21: Data packed as RGB (default) 0x24: Data packed as RBG 0x12: Data packed as BGR 0x18: Data packed as BRG 0x6: Data packed as GBR 0x9: Data packed as GRB
7	PACK_ALIGN	Packing alignment (within a byte) for each color component. This is valid only in parallel LCDC case where the output is packed loose. Not valid for MDDI based LCDC where the output is packed tight. 0x0: LSB (default) 0x1: MSB
6	EBI2_SPLIT_PIX	Set (1) to split one pixel (in 888 format) in to two 12 bit writes. This should be set only if output is to AHB.
5:4	COMP2_OUT	Number of bits for component 2 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).
3:2	COMP1_OUT	Number of bits for component 1 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).
1:0	COMP0_OUT	Number of bits for component 0 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).

0x05190004 MDP_DMA_P_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_SIZE register defines the primary DMA fetch width and height in pixels. This register is only valid when Overlay Processor 0 is in BLT mode; otherwise this is not used, and the size is taken from MDP_OVERLAYPROC0_OUT_SIZE.

MDP_DMA_P_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DMA_H	DMA fetch image height (in pixels). For LCDC, this specifies the active region height also.
15:12	RESERVED15_12	
11:0	DMA_W	DMA fetch image width (in pixels). For LCDC, this specifies the active region width also.

0x05190008 MDP_DMA_P_BUF_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Writing to this register forces an update to the back copy (the copy that is used currently by the DMA_P's fetch) of the frame buffer address. This register should only be done when one needs to override and switch to a new buffer in the middle of a frame. Or, when Overlay Processor 0 is in BLT mode, this address is used for DMA_P in stand-alone fetch decoupled from the Overlay Processor 0. When not in BLT mode, each new DMA_P fetch buffer address would be passed directly from MDP_OVERLAYPROC0_FB_ADDR after the Overlay Processor 0 has finished processing a frame.

MDP_DMA_P_BUF_ADDR

Bits	Name	Description
31:0	BUF_ADDR	Fetch buffer base address (byte-aligned). This defines the start of fetch pixel.

0x0519000C MDP_DMA_P_BUF_Y_STRIDE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_BUF_Y_STRIDE register defines the line jump value (in bytes) in the fetch buffer.This register is only valid when Overlay Processor 0 is in BLT mode; otherwise this is not used, and the size is taken from MDP_OVERLAYPROC0_FB_Y_STRIDE.

MDP_DMA_P_BUF_Y_STRIDE

Bits	Name	Description
31:13	RESERVED31_13	This field has no function and should be set to zero for future compatibility
12:0	BUF_Y_STRIDE	Y-stride (or) line jump value in bytes in the fetch buffer. Irrespective of whether the data is contiguous or non-contiguous, line jump value has to be provided since all the fetch requests are line-based.

0x05190010 MDP_DMA_P_OUT_XY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_OUT_XY

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DMA_OUT_Y	Display (or) screen y coordinate (pixel) where the first line of a ROI will be written. Program this parameter to zero if the output interface is LCDC since all LCDC updates are full screen.
15:12	RESERVED15_12	
11:0	DMA_OUT_X	Display (or) screen x coordinate (pixel) where the first pixel of a ROI will be written. Program this parameter to zero if the output interface is LCDC since all LCDC updates are full screen.

0x05190014 MDP_DMA_P_LINE_COUNT

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_LINE_COUNT

Bits	Name	Description
31:12	RESERVED31_12	
11:0	LINE_COUNT	Provides the line count or write pointer value (read pointer if output to LCDC). This value is w.r.t. display height and not ROI height.

0x05190018 MDP_DMA_P_LINE_IRQ

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0FFF

MDP_DMA_P_LINE_IRQ defines the line count or write_pointer value at which an interrupt has to be generated.

MDP_DMA_P_LINE_IRQ

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	IRQ_LINE	Specify the line count or write pointer value at which an interrupt has to be generated. Specify this value w.r.t. display height and not ROI height.

0x0519001C MDP_DMA_P_MASK_PATTERN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_MASK_PATTERN register defines the pattern that will be used when bit masking is enabled.

MDP_DMA_P_MASK_PATTERN

Bits	Name	Description
31:24	RESERVED31_24	
23:0	BIT_MASK_PATTERN	This pattern is used to mask the pixel bits when bit masking is enabled. If a pattern bit is set (1) the corresponding pixel bit is masked. The pattern is specified as {C2, C1, C0} where each color component is loosely packed according to the output format in to 8-bits and LSB aligned.

0x05190020 MDP_DMA_P_PROFILE_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_PROFILE_EN

Bits	Name	Description
31:1	RESERVED31_1	
0	EN	Enable the ROI cycle counter for profiling

0x05190024 MDP_DMA_P_PROFILE_COUNT

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_PROFILE_COUNT

Bits	Name	Description
31:24	RESERVED31_24	
23:0	TOTAL_CYCLE	Total cycle count (in AXI cycles) in a ROI, from ROI start to last pixel out of Packer (DMA_P goes back to Idle). This count will be reset automatically at the beginning of each ROI start.

0x05190030 MDP_DMA_P_BUF_ADDR_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 1 is used for DMA_P pipe.

MDP_DMA_P_BUF_ADDR_1

Bits	Name	Description
31:0	BUF_ADDR	Fetch buffer base address (byte-aligned). This defines the start of fetch pixel.

0x05190034 MDP_DMA_P_BUF_ADDR_2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

.This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 2 is used for DMA_P pipe.

MDP_DMA_P_BUF_ADDR_2

Bits	Name	Description
31:0	BUF_ADDR	Fetch buffer base address (byte-aligned). This defines the start of fetch pixel.

0x05190040 MDP_DMA_P_CURSOR_FORMAT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_CURSOR_FORMAT

Bits	Name	Description
31:3	RESERVED31_2	
2:0	CURSOR_FORMAT	0x0: ARGB8888 format (Default) 0x1: RGB888 format 0x2: ARGB1555 format 0x3: RGB565 format 0x4: ARGB4444 format 0x5: RGB444 format

0x05190044 MDP_DMA_P_CURSOR_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_CURSOR_SIZE register defines the hardware cursor width and height in pixels.

MDP_DMA_P_CURSOR_SIZE

Bits	Name	Description
31:23	RESERVED31_23	This field has no function and should be set to zero for future compatibility
22:16	CURSOR_H	Cursor height (in lines). Max. supported height = 64 lines.
15:7	RESERVED15_7	This field has no function and should be set to zero for future compatibility
6:0	CURSOR_W	Cursor width (in pixels). Max. supported width = 64 pixels

0x05190048 MDP_DMA_P_CURSOR_BUF_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_CURSOR_BUF_ADDR register defines the cursor buffer address. This register is Double Buffered and the programmed value is latched in to the second buffer every Vsync.

MDP_DMA_P_CURSOR_BUF_ADDR

Bits	Name	Description
31:0	CURSOR_BUF_ADDR	Cursor buffer base address (byte-aligned).

0x0519004C MDP_DMA_P_CURSOR_POSITION

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_CURSOR_POSITION register defines the start x and y positions of the cursor relative to ROI start x and y. This register is Double Buffered and the programmed value is latched in to the second buffer every Vsync.

MDP_DMA_P_CURSOR_POSITION

Bits	Name	Description
31	CURSOR_SIZE_SEL	0x1: Start positions below are of s13 format (if required) 0x0: Start positions below are of s12 format (legacy mode - bit 13 in CURSOR_X_START and CURSOR_Y_START will be ignored.)
30:29	RESERVED30_29	This field has no function and should be set to zero for future compatibility
28:16	CURSOR_Y_START	Define the start (y) position of the cursor relative to ROI start (y). This is a signed value and has to be programmed in (s12 or s13) format depending on CURSOR_SIZE_SEL.
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility
12:0	CURSOR_X_START	Define the start (x) position of the cursor relative to ROI start (x). This is a signed value and has to be programmed in (s12 or s13) format depending on CURSOR_SIZE_SEL.

0x05190060 MDP_DMA_P_CURSOR_BLEND_CONFIG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0002

MDP_DMA_P_CURSOR_BLEND_CONFIG register enables cursor blend and defines some blend parameters.

MDP_DMA_P_CURSOR_BLEND_CONFIG

Bits	Name	Description
31:4	RESERVED31_4	
3	BLEND_TRANSP_EN	Transparency check enable: 0x0: Off (Output is according to blend_alpha_sel blend output.) 0x1: On (Color keying is done on the cursor and blended result specified from the 2 layers is passed if non-matching; otherwise, the background image layer is sent.)
2:1	BLEND_ALPHA_SEL	Blending alpha select: 0x1: Cursor per pixel alpha (Default) 0x2: Constant alpha
0	BLEND_EN	Cursor blend enable (when disabled, output pixels would be the same as the background image pixels).

0x05190064 MDP_DMA_P_CURSOR_BLEND_PARAM

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_CURSOR_BLEND_PARAM

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Constant alpha value.

0x05190068 MDP_DMA_P_CURSOR_BLEND_TRANS_LOW

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_CURSOR_BLEND_TRANS_LOW

Bits	Name	Description
31:24	RESERVED31_24	
23:0	TRANSPARENCY_LOW	Transparent color check lower limit (Color2,Color1,Color0 each 8 bits from MSB to LSB).

0x0519006C MDP_DMA_P_CURSOR_BLEND_TRANS_HIGH

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_CURSOR_BLEND_TRANS_HIGH

Bits	Name	Description
31:24	RESERVED31_24	
23:0	TRANSPARENCY_HIGH	Transparent color check upper limit (Color2,Color1,Color0 each 8 bits from MSB to LSB).

0x05190070 MDP_DMA_P_OP_MODE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_P_OP_MODE register defines the color and gamma correct parameters. This register is Double Buffered and the programmed value is latched in to the second buffer every Vsync.

MDP_DMA_P_OP_MODE

Bits	Name	Description
31:14	RESERVED31_14	
13	PCC_SEL	Selects which set of PCC coefficients to use during processing 0x0: Set1 0x1: Set2
12	CSC_FMT_OUT	Select the output color format after correction/conversion 0x0: RGB (default) 0x1: YCbCr
11	CSC_FMT_IN	Select the input color format for correction/conversion 0x0: RGB (default) 0x1: YCbCr

MDP_DMA_P_OP_MODE (cont.)

Bits	Name	Description
10	LUT_SEL	Selects which LUT to use during processing 0x0: Set1 0x1: Set2
9:4	RESERVED9_4	
3	CONVERT_MATRIX_EN	Enable color convert. This enables the matrix conversion in the convert block.
2	LUT_C2_EN	Component 2 LUT enable.
1	LUT_C1_EN	Component 1 LUT enable.
0	LUT_C0_EN	Component 0 LUT enable.

0x05191000 MDP_DMA_P_FETCH_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000F

MDP_DMA_P_FETCH_STATUS

Bits	Name	Description
31:4	RESERVED31_4	
3:0	IDLES	Fetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 3= dma_rd idle Bit 2= ctl idle Bit 1= burstbuf idle Bit 0= unpack idle

0x05191004 MDP_DMA_P_FETCH_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0047

MDP_DMA_P_FETCH_CFG

Bits	Name	Description
31:8	RESERVED31_8	
7	SYNC_MODE	Boundary on which fetch synchronizes certain registers in BLT mode: 0x0: frame (default) 0x1: line

MDP_DMA_P_FETCH_CFG (cont.)

Bits	Name	Description
6:4	MAX_BURST_SIZE	Maximum burst beat size. Possible values: 0x4: 16 (default) 0x2: 8 0x1: 4
3	RESERVED3	
2:0	REQ_DEPTH_LIMIT	Pending request limit, default 0x7 means maximum of 8 pending requests, anything less limits the AXI requests to that number + 1.

0x05192000 MDP_DMA_P_CUR_FETCH_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000F

MDP_DMA_P_CUR_FETCH_STATUS

Bits	Name	Description
31:4	RESERVED31_4	
3:0	IDLES	Fetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 3= dma_rd idle Bit 2= ctl idle Bit 1= burstbuf idle Bit 0= unpack idle

0x05193400+4*n MDP_DMA_P_CSC_MV1n, n=[0..8]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_CSC_MV1n register contains the set1 matrix vector.

MDP_DMA_P_CSC_MV1n

Bits	Name	Description
31:13	RESERVED31_13	
12:0	MV1	MV1 = Matrix vector set1 (s4.9). Matrices are indexed left to right, top to bottom. That is, row 1, col 0 index = 3 (index range - 0 to 8).

0x05193500+ 4*n MDP_DMA_P_CSC_PRE_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_CSC_PRE_BV1n register contains the set1 pre-bias vector.

P_

MDP_DMA_P_CSC_PRE_BV1n

Bits	Name	Description
31:9	RESERVED31_9	
8:0	PRE_BV1	PRE_BV1= Pre-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x05193580+ 4*n MDP_DMA_P_CSC_POST_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_CSC_POST_BV1n register contains the set1 post-bias vector.

MDP_DMA_P_CSC_POST_BV1n

Bits	Name	Description
31:9	RESERVED31_9	
8:0	POST_BV1	POST_BV1 = Post-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x05193600+ 4*n MDP_DMA_P_CSC_PRE_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_CSC_PRE_LV1n register contains the set1 pre-limit vector.

MDP_DMA_P_CSC_PRE_LV1n

Bits	Name	Description
31:8	RESERVED31_8	

MDP_DMA_P_CSC_PRE_LV1n (cont.)

Bits	Name	Description
7:0	PRE_LV1	PRE_LV1 = Pre-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x05193680+4*n MDP_DMA_P_CSC_POST_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_CSC_POST_LV1n register contains the set1 post-limit vector.

MDP_DMA_P_CSC_POST_LV1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	POST_LV1	POST_LV1 = Post-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x05194800+4*n MDP_DMA_P_DISP_LUT1n, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_P_DISP_LUT1n registers contains the color lookup values for LUT set1.

MDP_DMA_P_DISP_LUT1n

Bits	Name	Description
31:24	RESERVED31_24	
23:16	LUT_COLOR2	LUT value for color2.
15:8	LUT_COLOR1	LUT value for color1.
7:0	LUT_COLOR0	LUT value for color0.

0x05194C00+4*n MDP_DMA_P_DISP_LUT2n, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_P_DISP_LUT2n registers contains the color lookup values for LUT set2.

MDP_DMA_P_DISP_LUT2n

Bits	Name	Description
31:24	RESERVED31_24	
23:16	LUT_COLOR2	LUT value for color2.
15:8	LUT_COLOR1	LUT value for color1.
7:0	LUT_COLOR0	LUT value for color0.

0x05195000 MDP_DMA_P_HIST_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_P_HIST_START register kicks off histogram generation.

MDP_DMA_P_HIST_START

Bits	Name	Description
31:0	HIST_START	A write to this register kicks off histogram generation. Actual accumulation begins at the start of next ROI. Histogram accumulation can be started only when histogram reset sequence is not currently active.

0x05195004 MDP_DMA_P_HIST_FRAME_CNT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0001

The MDP_DMA_P_HIST_FRAME_CNT register is used to program the frame count for histogram accumulation.

MDP_DMA_P_HIST_FRAME_CNT

Bits	Name	Description
31:6	RESERVED31_6	
5:0	FRAME_CNT	Program the number of frames over which the histogram data has to be collected. If the frame count programmed is more than what each 24-bit bin can support, the bin count will saturate at the maximum value. Here are some max. frame counts that can be programmed for different image sizes for a 24-bit bin. XGA (1024 x 768) - 21 WSVGA (1024 x 600) - 27 WVGA (800 x 480) - 43 VGA (640 x 480) - 54

0x05195008 MDP_DMA_P_HIST_BIT_MASK

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x8000_0000

The MDP_DMA_P_HIST_BIT_MASK register specifies which MSBs need to be masked before histogram binning.

MDP_DMA_P_HIST_BIT_MASK

Bits	Name	Description
31	BIT_MASK_POLARITY	If set to (1) masked bits are compared to `1' else compared to `0'
30:2	RESERVED30_2	
1:0	BIT_MASK	Select which MSBs of the input color component have to be masked before histogram binning. The five unmasked MSBs will be used for bin address generation if the polarity of all the masked bits matches BIT_MASK_POLARITY. 0x0: No masking (default) 0x1: Mask one MSB 0x2: Mask two MSBs 0x3: Mask three MSBs

0x0519500C MDP_DMA_P_HIST_RESET_SEQ_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_P_HIST_RESET_SEQ_START kicks off a reset sequence.

MDP_DMA_P_HIST_RESET_SEQ_START

Bits	Name	Description
31:0	RESET_SEQ_START	Writing to this register kicks off a reset sequence.This reset sequence clears all RAM locations and RAM rd/wr pointers. The reset sequence can be initiated only when histogram generation is not currently active. Note: Functional clock gating will shut off the clock to DMA_P sub-blocks when a ROI is not being processed. So DMA_P clock should be forced ON for the reset sequence to complete.

0x05195010 MDP_DMA_P_HIST_CONTROL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_HIST_CONTROL register controls histogram operation.

MDP_DMA_P_HIST_CONTROL

Bits	Name	Description
31:1	RESERVED31_1	
0	AUTO_CLEAR_EN	When set (1), the bin from which data has been read is cleared automatically.

0x05195014 MDP_DMA_P_HIST_INTR_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_HIST_INTR_STATUS register provides histogram interrupt status.

MDP_DMA_P_HIST_INTR_STATUS

Bits	Name	Description
31:2	RESERVED31_2	
1	HIST_DONE	When set (1) implies histogram generation is complete.
0	RESET_SEQ_DONE	When set (1) implies the reset sequence is complete.

0x05195018 MDP_DMA_P_HIST_INTR_CLEAR

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_P_HIST_INTR_CLEAR is used to clear the interrupts generated by histogram block.

MDP_DMA_P_HIST_INTR_CLEAR

Bits	Name	Description
31:2	RESERVED31_2	
1	HIST_DONE	Write (1) to this bit to clear the status.
0	RESET_SEQ_DONE	Write (1) to this bit to clear the status.

0x0519501C MDP_DMA_P_HIST_INTR_ENABLE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_HIST_INTR_ENABLE is used to enable the interrupt sources within the histogram block.

MDP_DMA_P_HIST_INTR_ENABLE

Bits	Name	Description
31:2	RESERVED31_2	
1	HIST_DONE	Write (1) to this bit to enable the interrupt source.
0	RESET_SEQ_DONE	Write (1) to this bit to enable the interrupt source.

0x05195020 MDP_DMA_P_HIST_STOP_REQ

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_P_HIST_STOP_REQ kicks off a histogram operation stop request which is stopping HIST HW at the end of frame even if the frame count is less than programmed frame count.

MDP_DMA_P_HIST_STOP_REQ

Bits	Name	Description
31:0	STOP_REQ	Writing to this register kicks off a stop request which is stopping HIST HW at the end of frame even if the processed frame count is less than programmed frame count.

0x05195024 MDP_DMA_P_HIST_CANCEL_REQ

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_P_HIST_CANCEL_REQ kicks off a histogram operation cancel request which is stopping HIST HW at any state rather than RESET state.

MDP_DMA_P_HIST_CANCEL_REQ

Bits	Name	Description
31:0	CANCEL_REQ	Writing to this register kicks off a cancel request which is stopping HIST HW at any state rather than RESET state.

0x05195028 MDP_DMA_P_HIST_EXTRA_INFO_0

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x007F_0000

The MDP_DMA_P_HIST_EXTRA_INFO_0 register provides histogram extra information. These values are only valid when HIST HW are IDLE state and this register values are reset automatically whenever HIST HW starts.

MDP_DMA_P_HIST_EXTRA_INFO_0

Bits	Name	Description
31	RESERVED31	
30:24	R_MAX_VALUE	Maximum pixel value for component R
23	RESERVED23	
22:16	R_MIN_VALUE	Minimum pixel value for compound R
15:6	RESERVED15_6	
5:0	CUR_FRAME_COUNT	This value provides the processed number of frame from start to HIST_DONE.

0x0519502C MDP_DMA_P_HIST_EXTRA_INFO_1

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x007F_007F

The MDP_DMA_P_HIST_EXTRA_INFO_1 register provides histogram extra information. These values are only valid when HIST HW are IDLE state and this register values are reset automatically whenever HIST HW starts.

MDP_DMA_P_HIST_EXTRA_INFO_1

Bits	Name	Description
31	RESERVED31	
30:24	B_MAX_VALUE	Maximum pixel value for component B
23	RESERVED23	
22:16	B_MIN_VALUE	Minimum pixel value for component B
15	RESERVED15	
14:8	G_MAX_VALUE	Maximum pixel value for component G
7	RESERVED7	
6:0	G_MIN_VALUE	Minimum pixel value for component G

0x05195100+4*n MDP_DMA_P_HIST_R_DATAn, n=[0..31]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_P_HIST_R_DATAn register provides the histogram data corresponding to the color component R.This register field will not be used in MDP4.2 and SW should use new register address which is MDP_DMA_P_128BIN_HIST_R_DATAn

MDP_DMA_P_HIST_R_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_R_DATA	Reading this register provides histogram bin data for component R.

0x05195200+ 4*n MDP_DMA_P_HIST_G_DATAn, n=[0..31]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_P_HIST_G_DATAn register provides the histogram data corresponding to the color component G. This register field will not be used in MDP4.2 and SW should use new register address which is MDP_DMA_P_128BIN_HIST_G_DATAn

MDP_DMA_P_HIST_G_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_G_DATA	Reading this register provides histogram bin data for component G.

0x05195300+ 4*n MDP_DMA_P_HIST_B_DATAn, n=[0..31]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_P_HIST_B_DATAn register provides the histogram data corresponding to the color component B.This register field will not be used in MDP4.2 and SW should use new register address which is MDP_DMA_P_128BIN_HIST_B_DATAn

MDP_DMA_P_HIST_B_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_B_DATA	Reading this register provides histogram bin data for component B.

0x05195400+ 4*n MDP_DMA_P_128BIN_HIST_R_DATAn, n=[0..127]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_P_128BIN_HIST_R_DATAn register provides the histogram data corresponding to the color component R. This register field is extended from 32 to 128.

MDP_DMA_P_128BIN_HIST_R_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_R_DATA	Reading this register provides histogram bin data for component R.

0x05195800+ 4*n MDP_DMA_P_128BIN_HIST_G_DATAn, n=[0..127]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_P_128BIN_HIST_G_DATAn register provides the histogram data corresponding to the color component G. This register field is extended from 32 to 128.

MDP_DMA_P_128BIN_HIST_G_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_G_DATA	Reading this register provides histogram bin data for component G.

0x05195C00+ 4*n MDP_DMA_P_128BIN_HIST_B_DATAn, n=[0..127]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_P_128BIN_HIST_B_DATAn register provides the histogram data corresponding to the color component B.This register field will be extended from 32 to 128.

MDP_DMA_P_128BIN_HIST_B_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_B_DATA	Reading this register provides histogram bin data for component B.

0x05198800+ 4*n MDP_DMA_P_GC_START_COLOR_0_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component0

MDP_DMA_P_GC_START_COLOR_0_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x05198880+ 4*n MDP_DMA_P_GC_PARAM_COLOR_0_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component0.

MDP_DMA_P_GC_PARAM_COLOR_0_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U3.12)

0x05198900+ 4*n MDP_DMA_P_GC_START_COLOR_1_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component1

MDP_DMA_P_GC_START_COLOR_1_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x05198980+ 4*n MDP_DMA_P_GC_PARAM_COLOR_1_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component1

MDP_DMA_P_GC_PARAM_COLOR_1_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U13.2)

0x05198A00+ 4*n MDP_DMA_P_GC_START_COLOR_2_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component2

MDP_DMA_P_GC_START_COLOR_2_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x05198A80+ 4*n MDP_DMA_P_GC_PARAM_COLOR_2_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component2

MDP_DMA_P_GC_PARAM_COLOR_2_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U13.2)

0x05199000+ 4*n MDP_DMA_P_IGC_LSP_LUTn, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_P_IGC_LSP_LUTn registers contains the Least Significant Portion (lower 24 bits of total 36 bits) of the color lookup values for IGC LUT.

MDP_DMA_P_IGC_LSP_LUTn

Bits	Name	Description
31:28	RESERVED31_28	
27:16	LUT_COLOR1	LUT value for color1.
15:12	RESERVED15_12	
11:0	LUT_COLOR0	LUT value for color0.

0x05199800+ 4*n MDP_DMA_P_IGC_MSP_LUTn, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_P_IGC_MSP_LUTn registers contains the most significant portion (color component 2) of the color lookup values for IGC LUT. The whole LUT should be written to in the sequence of LSP write first followed by MSP write, writing from lower address to higher address. Each MSP register write actually triggers the write of whole 36-bit LUT entry into the RAM.

MDP_DMA_P_IGC_MSP_LUTn

Bits	Name	Description
31:12	RESERVED31_12	
11:0	LUT_COLOR2	LUT value for color2.

0x0519A000 MDP_DMA_P_PCC1_R_C

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_P_PCC1_R_C is the red plane constant coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_R_C

Bits	Name	Description
31:16	RESERVED31_16	
15:0	PCC_DATA	Reading this register provides PCC coefficient data (S13.3)

0x0519A004 MDP_DMA_P_PCC1_R_R

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_R_R is the red plane red coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_R_R

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A008 MDP_DMA_P_PCC1_R_G

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_R_G is the red plane green coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_R_G

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A00C MDP_DMA_P_PCC1_R_B

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_R_B is the red plane blue coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_R_B

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A010 MDP_DMA_P_PCC1_R_RR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_R_RR is the red plane red coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_R_RR

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A014 MDP_DMA_P_PCC1_R_GG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_R_GG is the red plane green coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_R_GG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A018 MDP_DMA_P_PCC1_R_BB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_R_BB is the red plane blue coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_R_BB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A01C MDP_DMA_P_PCC1_R_RG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_R_RG is the red plane red green coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_R_RG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A020 MDP_DMA_P_PCC1_R_GB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_R_GB is the red plane green blue coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_R_GB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A024 MDP_DMA_P_PCC1_R_RB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_R_RB is the red plane red blue coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_R_RB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A028 MDP_DMA_P_PCC1_R_RGB_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_R_RGB_0 is the first part of the red plane RGB coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_R_RGB_0

Bits	Name	Description
31:8	RESERVED31_16	
7:0	PCC_DATA	Reading this register provides PCC coefficient data (sign + 7 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x0519A02C MDP_DMA_P_PCC1_R_RGB_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_R_RGB_1 is the second part of the red plane RGB coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_R_RGB_1

Bits	Name	Description
31:0	PCC_DATA	Reading this register provides PCC coefficient data (remaining 32 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x0519A030 MDP_DMA_P_PCC1_G_C

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_G_C is the green plane constant coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_G_C

Bits	Name	Description
31:16	RESERVED31_16	
15:0	PCC_DATA	Reading this register provides PCC coefficient data (S13.3)

0x0519A034 MDP_DMA_P_PCC1_G_R

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_G_C is the green plane red coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_G_R

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A038 MDP_DMA_P_PCC1_G_G

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_G_G is the green plane green coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_G_G

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A03C MDP_DMA_P_PCC1_G_B

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_G_B is the green plane blue coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_G_B

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A040 MDP_DMA_P_PCC1_G_RR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_G_RR is the green plane red coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_G_RR

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A044 MDP_DMA_P_PCC1_G_GG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_G_GG is the green plane green coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_G_GG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A048 MDP_DMA_P_PCC1_G_BB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_G_BB is the green plane blue coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_G_BB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A04C MDP_DMA_P_PCC1_G_RG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_G_RG is the green plane red green coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_G_RG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A050 MDP_DMA_P_PCC1_G_GB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_G_GB is the green plane green blue coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_G_GB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A054 MDP_DMA_P_PCC1_G_RB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_R_RB is the green plane red blue coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_G_RB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A058 MDP_DMA_P_PCC1_G_RGB_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_G_RGB_0 is the first part of the green plane RGB coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_G_RGB_0

Bits	Name	Description
31:8	RESERVED31_16	

MDP_DMA_P_PCC1_G_RGB_0 (cont.)

Bits	Name	Description
7:0	PCC_DATA	Reading this register provides PCC coefficient data (sign + 7 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x0519A05C MDP_DMA_P_PCC1_G_RGB_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_G_RGB_1 is the second part of the green plane RGB coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_G_RGB_1

Bits	Name	Description
31:0	PCC_DATA	Reading this register provides PCC coefficient data (remaining 32 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x0519A060 MDP_DMA_P_PCC1_B_C

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_B_C is the blue plane constant coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_B_C

Bits	Name	Description
31:16	RESERVED31_16	
15:0	PCC_DATA	Reading this register provides PCC coefficient data (S13.3)

0x0519A064 MDP_DMA_P_PCC1_B_R

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_B_C is the blue plane red coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_B_R

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A068 MDP_DMA_P_PCC1_B_G

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_B_G is the blue plane green coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_B_G

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A06C MDP_DMA_P_PCC1_B_B

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_B_B is the blue plane blue coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_B_B

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A070 MDP_DMA_P_PCC1_B_RR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_B_RR is the blue plane red coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_B_RR

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A074 MDP_DMA_P_PCC1_B_GG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_B_GG is the blue plane green coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_B_GG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A078 MDP_DMA_P_PCC1_B_BB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_B_BB is the blue plane blue coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_B_BB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A07C MDP_DMA_P_PCC1_B_RG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_B_RG is the blue plane red green coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_B_RG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A080 MDP_DMA_P_PCC1_B_GB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_B_GB is the blue plane green blue coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_B_GB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A084 MDP_DMA_P_PCC1_B_RB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_B_RB is the blue plane red blue coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_B_RB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A088 MDP_DMA_P_PCC1_B_RGB_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_B_RGB_0 is the first part of the blue plane RGB coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_B_RGB_0

Bits	Name	Description
31:8	RESERVED31_8	
7:0	PCC_DATA	Reading this register provides PCC coefficient data (sign + 7 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x0519A08C MDP_DMA_P_PCC1_B_RGB_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC1_B_RGB_1 is the second part of the blue plane RGB coefficient (set 1) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC1_B_RGB_1

Bits	Name	Description
31:0	PCC_DATA	Reading this register provides PCC coefficient data (remaining 32 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x0519A100 MDP_DMA_P_PCC2_R_C

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_P_PCC2_R_C is the red plane constant coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_R_C

Bits	Name	Description
31:16	RESERVED31_16	

MDP_DMA_P_PCC2_R_C (cont.)

Bits	Name	Description
15:0	PCC_DATA	Reading this register provides PCC coefficient data (S13.3)

0x0519A104 MDP_DMA_P_PCC2_R_R

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_R_R is the red plane red coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_R_R

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A108 MDP_DMA_P_PCC2_R_G

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_R_G is the red plane green coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_R_G

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A10C MDP_DMA_P_PCC2_R_B

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_R_B is the red plane blue coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_R_B

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A110 MDP_DMA_P_PCC2_R_RR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_R_RR is the red plane red coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_R_RR

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A114 MDP_DMA_P_PCC2_R_GG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_R_GG is the red plane green coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_R_GG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A118 MDP_DMA_P_PCC2_R_BB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_R_BB is the red plane blue coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_R_BB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A11C MDP_DMA_P_PCC2_R_RG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_R_RG is the red plane red green coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_R_RG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A120 MDP_DMA_P_PCC2_R_GB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_R_GB is the red plane green blue coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_R_GB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A124 MDP_DMA_P_PCC2_R_RB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_R_RB is the red plane red blue coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_R_RB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A128 MDP_DMA_P_PCC2_R_RGB_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_R_RGB_0 is the first part of the red plane RGB coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_R_RGB_0

Bits	Name	Description
31:8	RESERVED31_16	
7:0	PCC_DATA	Reading this register provides PCC coefficient data (sign + 7 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x0519A12C MDP_DMA_P_PCC2_R_RGB_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_R_RGB_1 is the second part of the red plane RGB coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_R_RGB_1

Bits	Name	Description
31:0	PCC_DATA	Reading this register provides PCC coefficient data (remaining 32 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x0519A130 MDP_DMA_P_PCC2_G_C

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_G_C is the green plane constant coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_G_C

Bits	Name	Description
31:16	RESERVED31_16	
15:0	PCC_DATA	Reading this register provides PCC coefficient data (S13.3)

0x0519A134 MDP_DMA_P_PCC2_G_R

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_G_C is the green plane red coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_G_R

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A138 MDP_DMA_P_PCC2_G_G

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_G_G is the green plane green coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_G_G

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A13C MDP_DMA_P_PCC2_G_B

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_G_B is the green plane blue coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_G_B

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A140 MDP_DMA_P_PCC2_G_RR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_G_RR is the green plane red coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_G_RR

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A144 MDP_DMA_P_PCC2_G_GG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_G_GG is the green plane green coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_G_GG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A148 MDP_DMA_P_PCC2_G_BB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_G_BB is the green plane blue coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_G_BB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A14C MDP_DMA_P_PCC2_G_RG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_G_RG is the green plane red green coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_G_RG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A150 MDP_DMA_P_PCC2_G_GB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_G_GB is the green plane green blue coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_G_GB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A154 MDP_DMA_P_PCC2_G_RB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_R_RB is the green plane red blue coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_G_RB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A158 MDP_DMA_P_PCC2_G_RGB_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_G_RGB_0 is the first part of the green plane RGB coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_G_RGB_0

Bits	Name	Description
31:8	RESERVED31_16	

MDP_DMA_P_PCC2_G_RGB_0 (cont.)

Bits	Name	Description
7:0	PCC_DATA	Reading this register provides PCC coefficient data (sign + 7 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x0519A15C MDP_DMA_P_PCC2_G_RGB_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_G_RGB_1 is the second part of the green plane RGB coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_G_RGB_1

Bits	Name	Description
31:0	PCC_DATA	Reading this register provides PCC coefficient data (remaining 32 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x0519A160 MDP_DMA_P_PCC2_B_C

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_B_C is the blue plane constant coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_B_C

Bits	Name	Description
31:16	RESERVED31_16	
15:0	PCC_DATA	Reading this register provides PCC coefficient data (S13.3)

0x0519A164 MDP_DMA_P_PCC2_B_R

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_B_C is the blue plane red coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_B_R

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A168 MDP_DMA_P_PCC2_B_G

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_B_G is the blue plane green coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_B_G

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A16C MDP_DMA_P_PCC2_B_B

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_B_B is the blue plane blue coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_B_B

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x0519A170 MDP_DMA_P_PCC2_B_RR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_B_RR is the blue plane red coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_B_RR

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A174 MDP_DMA_P_PCC2_B_GG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_B_GG is the blue plane green coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_B_GG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A178 MDP_DMA_P_PCC2_B_BB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_B_BB is the blue plane blue coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_B_BB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A17C MDP_DMA_P_PCC2_B_RG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_B_RG is the blue plane red green coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_B_RG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A180 MDP_DMA_P_PCC2_B_GB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_B_GB is the blue plane green blue coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_B_GB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A184 MDP_DMA_P_PCC2_B_RB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_B_RB is the blue plane red blue coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_B_RB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x0519A188 MDP_DMA_P_PCC2_B_RGB_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_B_RGB_0 is the first part of the blue plane RGB coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_B_RGB_0

Bits	Name	Description
31:8	RESERVED31_8	
7:0	PCC_DATA	Reading this register provides PCC coefficient data (sign + 7 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x0519A18C MDP_DMA_P_PCC2_B_RGB_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_P_PCC2_B_RGB_1 is the second part of the blue plane RGB coefficient (set 2) for the DMA_P Polynomial Color Correction block.

MDP_DMA_P_PCC2_B_RGB_1

Bits	Name	Description
31:0	PCC_DATA	Reading this register provides PCC coefficient data (remaining 32 fractional bits - S1.39 for RGB_0 and RGB_1 field

14.15.14 Secondary Display Driver (DMA_S) registers

0x051A0000 MDP_DMA_S_CONFIG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_2100

MDP_DMA_S_CONFIG

Bits	Name	Description
31	RESERVED31	
30	PIGC_EN	Panel Inverse Panel Gamma Correction enable

MDP_DMA_S_CONFIG (cont.)

Bits	Name	Description
29	PCC_EN	Polynomial Color Correction enable
28	PGC_EN	Panel Gamma Correction enable
27	IBUF_FORMAT_EXTEND	In order to maintain SW backward compatible and support other input formats, this bit added. Detail description is in the IBUF_FORMAT field
26:25	IBUF_FORMAT	The fetch buffer format setting (This field is only valid when Overlay Processor 1is in BLT mode or Overlay Processor 1 is not connected to DMA_S; otherwise this is not used, and the format is taken from FB_FORMAT in MDP_OVERLAYPROC1_OUT_OPMODE): If IBUF_FORMAT_EXTEND is 0 (legacy mode + added format) If IBUF_FORMAT_EXTEND is 1 (extended mode) 0x0: RGB888 format (Default) 0x1: RGB565 format 0x2: xRGB8888 format 0x3: xRGB1555 format <new> 0x0: Reserved_1 0x1: Reserved_2 0x2: RGBx8888 format <new> 0x3: RGBx5551 format <new>
24	DITHER_EN	Dither enable.
23:19	RESERVED23_19	
18	BIT_MASK_POLARITY	Select the bit mask polarity. 0x0: Masked bits are set to `0' 0x1: Masked bits are set to `1'
17	RESERVED17	
16	COMP2_BIT_FLIP_EN	When set (1) flips all the bits of component2.
15	COMP1_BIT_FLIP_EN	When set (1) flips all the bits of component1.
14	COMP0_BIT_FLIP_EN	When set (1) flips all the bits of component0.
13:8	PACK_PATTERN	Packing pattern used by the packer. 0x21: Data packed as RGB (default) 0x24: Data packed as RBG 0x12: Data packed as BGR 0x18: Data packed as BRG 0x6: Data packed as GBR 0x9: Data packed as GRB
7	PACK_ALIGN	Packing alignment (within a byte) for each color component. This is valid only in parallel LCDC case where the output is packed loose. Not valid for MDDI based LCDC where the output is packed tight. 0x0: LSB (default) 0x1: MSB

MDP_DMA_S_CONFIG (cont.)

Bits	Name	Description
6	EBI2_SPLIT_PIX	Set to (1) to split the pixel (in 888 format) into two 12 bit writes. THis bit should only be set if the output interface in AHB.
5:4	COMP2_OUT	Number of bits for component 2 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).
3:2	COMP1_OUT	Number of bits for component 1 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).
1:0	COMP0_OUT	Number of bits for component 0 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).

0x051A0004 MDP_DMA_S_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_S_SIZE register defines the secondary DMA output width and height in pixels.

MDP_DMA_S_SIZE

Bits	Name	Description
31:28	RESERVED31_28	This field has no function and should be set to zero for future compatibility
27:16	DMA_H	DMA output image height (in pixels).
15:12	RESERVED15_12	This field has no function and should be set to zero for future compatibility
11:0	DMA_W	DMA output image width (in pixels).

0x051A0008 MDP_DMA_S_IBUF_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_S_IBUF_ADDR register defines the secondary DMA IBUF address.

MDP_DMA_S_IBUF_ADDR

Bits	Name	Description
31:0	IBUF_ADDR	Intermediate buffer base address (byte-aligned).

0x051A000C MDP_DMA_S_IBUF_Y_STRIDE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_S_IBUF_Y_STRIDE register defines the line jump value (in bytes) in the intermediate buffer.

MDP_DMA_S_IBUF_Y_STRIDE

Bits	Name	Description
31:14	RESERVED31_14	This field has no function and should be set to zero for future compatibility
13:0	IBUF_Y_STRIDE	Y-stride (or) line jump value in bytes in the intermediate buffer. Irrespective of whether the data in IBUF is contiguous or non-contiguous, line jump value has to be provided since all the DMA requests are line requests.

0x051A0010 MDP_DMA_S_OUT_XY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_S_OUT_XY

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DMA_OUT_Y	Screen y coordinate (pixel) where the first line of a ROI will be written.
15:12	RESERVED15_12	
11:0	DMA_OUT_X	Screen x coordinate (pixel) where the first pixel of a ROI will be written.

0x051A0014 MDP_DMA_S_LINE_COUNT

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_S_LINE_COUNT

Bits	Name	Description
31:12	RESERVED31_12	

MDP_DMA_S_LINE_COUNT (cont.)

Bits	Name	Description
11:0	LINE_COUNT	Provides the line count or write pointer value. This value is w.r.t. display height and not ROI height.

0x051A0018 MDP_DMA_S_LINE_IRQ

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0FFF

MDP_DMA_S_LINE_IRQ defines the line count or write_pointer value at which an interrupt has to be generated.

MDP_DMA_S_LINE_IRQ

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	IRQ_LINE	Specify the line count or write pointer value at which an interrupt has to be generated. Specify this value w.r.t. display height and not ROI height.

0x051A001C MDP_DMA_S_MASK_PATTERN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_S_MASK_PATTERN register defines the pattern that will be used when bit masking is enabled.

MDP_DMA_S_MASK_PATTERN

Bits	Name	Description
31:24	RESERVED31_24	
23:0	BIT_MASK_PATTERN	This pattern is used to mask the pixel bits when bit masking is enabled. If a pattern bit is set (1) the corresponding pixel bit is masked. The pattern is specified as {C2, C1, C0} where each color component is loosely packed according to the output format in to 8-bits and LSB aligned.

0x051A0020 MDP_DMA_S_PROFILE_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_S_PROFILE_EN

Bits	Name	Description
31:1	RESERVED31_1	
0	EN	Enable the ROI cycle counter for profiling

0x051A0024 MDP_DMA_S_PROFILE_COUNT

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_S_PROFILE_COUNT

Bits	Name	Description
31:24	RESERVED31_24	
23:0	TOTAL_CYCLE	Total cycle count (in AXI cycles) in a ROI, from ROI start to last pixel out of Packer (DMA_S goes back to Idle). This count will be reset automatically at the beginning of each ROI start.

0x051A0028 MDP_DMA_S_OP_MODE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_S_OP_MODE register defines the color and gamma correct parameters. This register is Double Buffered and the programmed value is latched in to the second buffer every Vsync.

MDP_DMA_S_OP_MODE

Bits	Name	Description
31:14	RESERVED31_14	
13	PCC_SEL	Selects which set of PCC coefficients to use during processing 0x0: Set1 0x1: Set2

MDP_DMA_S_OP_MODE (cont.)

Bits	Name	Description
12	CSC_FMT_OUT	Select the output color format after correction/conversion 0x0: RGB (default) 0x1: YCbCr
11	CSC_FMT_IN	Select the input color format for correction/conversion 0x0: RGB (default) 0x1: YCbCr
10	LUT_SEL	Selects which LUT to use during processing 0x0: Set1 0x1: Set2
9:4	RESERVED9_4	
3	CONVERT_MATRIX_EN	Enable color convert. This enables the matrix conversion in the convert block.
2	LUT_C2_EN	Component 2 LUT enable.
1	LUT_C1_EN	Component 1 LUT enable.
0	LUT_C0_EN	Component 0 LUT enable.

0x051A0030 MDP_DMA_S_IBUF_ADDR_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 1 is used for DMA_S pipe.

MDP_DMA_S_IBUF_ADDR_1

Bits	Name	Description
31:0	IBUF_ADDR	Intermediate buffer base address (byte-aligned).

0x051A0034 MDP_DMA_S_IBUF_ADDR_2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 2 is used for DMA_S pipe.

MDP_DMA_S_IBUF_ADDR_2

Bits	Name	Description
31:0	IBUF_ADDR	Intermediate buffer base address (byte-aligned).

0x051A1000 MDP_DMA_S_FETCH_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000F

MDP_DMA_S_FETCH_STATUS

Bits	Name	Description
31:4	RESERVED31_4	
3:0	IDLES	Fetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 3= dma_rd idle Bit 2= ctl idle Bit 1= burstbuf idle Bit 0= unpack idle

0x051A1004 MDP_DMA_S_FETCH_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0047

MDP_DMA_S_FETCH_CFG

Bits	Name	Description
31:8	RESERVED31_8	
7	SYNC_MODE	Boundary on which fetch synchronizes certain registers in BLT mode: 0x0: frame (default) 0x1: line
6:4	MAX_BURST_SIZE	Maximum burst beat size. Possible values: 0x4: 16 (default) 0x2: 8 0x1: 4
3	RESERVED3	
2:0	REQ_DEPTH_LIMIT	Pending request limit, default 0x7 means maximum of 8 pending requests, anything less limits the AXI requests to that number + 1.

0x051A3400+ 4*n MDP_DMA_S_CSC_MV1n, n=[0..8]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_CSC_MV1n register contains the set1 matrix vector.

MDP_DMA_S_CSC_MV1n

Bits	Name	Description
31:13	RESERVED31_13	
12:0	MV1	MV1 = Matrix vector set1 (s4.9). Matrices are indexed left to right, top to bottom. That is, row 1, col 0 index = 3 (index range - 0 to 8).

0x051A3500+ 4*n MDP_DMA_S_CSC_PRE_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_CSC_PRE_BV1n register contains the set1 pre-bias vector.

P_

MDP_DMA_S_CSC_PRE_BV1n

Bits	Name	Description
31:9	RESERVED31_9	
8:0	PRE_BV1	PRE_BV1= Pre-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x051A3580+ 4*n MDP_DMA_S_CSC_POST_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_CSC_POST_BV1n register contains the set1 post-bias vector.

MDP_DMA_S_CSC_POST_BV1n

Bits	Name	Description
31:9	RESERVED31_9	

MDP_DMA_S_CSC_POST_BV1n (cont.)

Bits	Name	Description
8:0	POST_BV1	POST_BV1 = Post-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x051A3600+ 4*n MDP_DMA_S_CSC_PRE_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_CSC_PRE_LV1n register contains the set1 pre-limit vector.

MDP_DMA_S_CSC_PRE_LV1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	PRE_LV1	PRE_LV1 = Pre-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x051A3680+ 4*n MDP_DMA_S_CSC_POST_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_CSC_POST_LV1n register contains the set1 post-limit vector.

MDP_DMA_S_CSC_POST_LV1n

Bits	Name	Description
31:8	RESERVED31_8	
7:0	POST_LV1	POST_LV1 = Post-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x051A4800+ 4*n MDP_DMA_S_DISP_LUT1n, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_S_DISP_LUT1n registers contains the color lookup values for LUT set1.

MDP_DMA_S_DISP_LUT1n

Bits	Name	Description
31:24	RESERVED31_24	
23:16	LUT_COLOR2	LUT value for color2.
15:8	LUT_COLOR1	LUT value for color1.
7:0	LUT_COLOR0	LUT value for color0.

0x051A4C00+4*n MDP_DMA_S_DISP_LUT2n, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_S_DISP_LUT2n registers contains the color lookup values for LUT set2.

MDP_DMA_S_DISP_LUT2n

Bits	Name	Description
31:24	RESERVED31_24	
23:16	LUT_COLOR2	LUT value for color2.
15:8	LUT_COLOR1	LUT value for color1.
7:0	LUT_COLOR0	LUT value for color0.

0x051A5000 MDP_DMA_S_HIST_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_S_HIST_START register kicks off histogram generation.

MDP_DMA_S_HIST_START

Bits	Name	Description
31:0	HIST_START	A write to this register kicks off histogram generation. Actual accumulation begins at the start of next ROI. Histogram accumulation can be started only when histogram reset sequence is not currently active.

0x051A5004 MDP_DMA_S_HIST_FRAME_CNT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0001

The MDP_DMA_S_HIST_FRAME_CNT register is used to program the frame count for histogram accumulation.

MDP_DMA_S_HIST_FRAME_CNT

Bits	Name	Description
31:6	RESERVED31_6	
5:0	FRAME_CNT	Program the number of frames over which the histogram data has to be collected. If the frame count programmed is more than what each 24-bit bin can support, the bin count will saturate at the maximum value. Here are some max. frame counts that can be programmed for different image sizes for a 24-bit bin. XGA (1024 x 768) - 21 WSVGA (1024 x 600) - 27 WVGA (800 x 480) - 43 VGA (640 x 480) - 54

0x051A5008 MDP_DMA_S_HIST_BIT_MASK

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x8000_0000

The MDP_DMA_S_HIST_BIT_MASK register specifies which MSBs need to be masked before histogram binning.

MDP_DMA_S_HIST_BIT_MASK

Bits	Name	Description
31	BIT_MASK_POLARITY	If set to (1) masked bits are compared to `1' else compared to `0'
30:2	RESERVED30_2	
1:0	BIT_MASK	Select which MSBs of the input color component have to be masked before histogram binning. The five unmasked MSBs will be used for bin address generation if the polarity of all the masked bits matches BIT_MASK_POLARITY. 0x0: No masking (default) 0x1: Mask one MSB 0x2: Mask two MSBs 0x3: Mask three MSBs

0x051A500C MDP_DMA_S_HIST_RESET_SEQ_START

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_S_HIST_RESET_SEQ_START kicks off a reset sequence.

MDP_DMA_S_HIST_RESET_SEQ_START

Bits	Name	Description
31:0	RESET_SEQ_START	Writing to this register kicks off a reset sequence.This reset sequence clears all RAM locations and RAM rd/wr pointers. The reset sequence can be initiated only when histogram generation is not currently active. Note: Functional clock gating will shut off the clock to DMA_P sub-blocks when a ROI is not being processed. So DMA_P clock should be forced ON for the reset sequence to complete.

0x051A5010 MDP_DMA_S_HIST_CONTROL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_HIST_CONTROL register controls histogram operation.

MDP_DMA_S_HIST_CONTROL

Bits	Name	Description
31:1	RESERVED31_1	
0	AUTO_CLEAR_EN	When set (1), the bin from which data has been read is cleared automatically.

0x051A5014 MDP_DMA_S_HIST_INTR_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_HIST_INTR_STATUS register provides histogram interrupt status.

MDP_DMA_S_HIST_INTR_STATUS

Bits	Name	Description
31:2	RESERVED31_2	
1	HIST_DONE	When set (1) implies histogram generation is complete.
0	RESET_SEQ_DONE	When set (1) implies the reset sequence is complete.

0x051A5018 MDP_DMA_S_HIST_INTR_CLEAR

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_P_HIST_INTR_CLEAR is used to clear the interrupts generated by histogram block.

MDP_DMA_S_HIST_INTR_CLEAR

Bits	Name	Description
31:2	RESERVED31_2	
1	HIST_DONE	Write (1) to this bit to clear the status.
0	RESET_SEQ_DONE	Write (1) to this bit to clear the status.

0x051A501C MDP_DMA_S_HIST_INTR_ENABLE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_HIST_INTR_ENABLE is used to enable the interrupt sources within the histogram block.

MDP_DMA_S_HIST_INTR_ENABLE

Bits	Name	Description
31:2	RESERVED31_2	
1	HIST_DONE	Write (1) to this bit to enable the interrupt source.
0	RESET_SEQ_DONE	Write (1) to this bit to enable the interrupt source.

0x051A5020 MDP_DMA_S_HIST_STOP_REQ

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_S_HIST_STOP_REQ kicks off a histogram operation stop request which is stopping HIST HW at the end of frame even if the frame count is less than programmed frame count.

MDP_DMA_S_HIST_STOP_REQ

Bits	Name	Description
31:0	STOP_REQ	Writing to this register kicks off a stop request which is stopping HIST HW at the end of frame even if the processed frame count is less than programmed frame count.

0x051A5024 MDP_DMA_S_HIST_CANCEL_REQ

Type: Write
Clock: CC_MDP_CLK
Reset State: N/A

The MDP_DMA_S_HIST_CANCEL_REQ kicks off a histogram operation cancel request which is stopping HIST HW at any state rather than RESET state.

MDP_DMA_S_HIST_CANCEL_REQ

Bits	Name	Description
31:0	CANCEL_REQ	Writing to this register kicks off a cancel request which is stopping HIST HW at any state rather than RESET state.

0x051A5028 MDP_DMA_S_HIST_EXTRA_INFO_0

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x007F_0000

The MDP_DMA_S_HIST_EXTRA_INFO_0 register provides histogram extra information. These values are only valid when HIST HW are IDLE state and this register values are reset automatically whenever HIST HW starts.

MDP_DMA_S_HIST_EXTRA_INFO_0

Bits	Name	Description
31	RESERVED31	
30:24	R_MAX_VALUE	Maximum pixel value for component R
23	RESERVED23	
22:16	R_MIN_VALUE	Minimum pixel value for component R
15:6	RESERVED15_6	
5:0	CUR_FRAME_COUNT	This value provides the processed number of frame from start to HIST_DONE.

0x051A502C MDP_DMA_S_HIST_EXTRA_INFO_1

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x007F_007F

The MDP_DMA_S_HIST_EXTRA_INFO_1 register provides histogram extra information. These values are only valid when HIST HW are IDLE state and this register values are reset automatically whenever HIST HW starts.

MDP_DMA_S_HIST_EXTRA_INFO_1

Bits	Name	Description
31	RESERVED31	
30:24	B_MAX_VALUE	Maximum pixel value for component B
23	RESERVED23	
22:16	B_MIN_VALUE	Minimum pixel value for component B
15	RESERVED15	
14:8	G_MAX_VALUE	Maximum pixel value for component G
7	RESERVED7	
6:0	G_MIN_VALUE	Minimum pixel value for component G

0x051A5100+4*n MDP_DMA_S_HIST_R_DATAn, n=[0..31]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_S_HIST_R_DATAn register provides the histogram data corresponding to the color component R. This register field will not be used in MDP4.2 and SW should use new register address which is MDP_DMA_S_128BIN_HIST_R_DATAn

MDP_DMA_S_HIST_R_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_R_DATA	Reading this register provides histogram bin data for component R.

0x051A5200+ 4*n MDP_DMA_S_HIST_G_DATAn, n=[0..31]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_S_HIST_G_DATAn register provides the histogram data corresponding to the color component G. This register field will not be used in MDP4.2 and SW should use new register address which is MDP_DMA_S_128BIN_HIST_G_DATAn

MDP_DMA_S_HIST_G_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_G_DATA	Reading this register provides histogram bin data for component G.

0x051A5300+ 4*n MDP_DMA_S_HIST_B_DATAn, n=[0..31]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_S_HIST_B_DATAn register provides the histogram data corresponding to the color component B. This register field will not be used in MDP4.2 and SW should use new register address which is MDP_DMA_S_128BIN_HIST_B_DATAn

MDP_DMA_S_HIST_B_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_B_DATA	Reading this register provides histogram bin data for component B.

0x051A5400+4*n MDP_DMA_S_128BIN_HIST_R_DATAn, n=[0..127]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_S_128BIN_HIST_R_DATAn register provides the histogram data corresponding to the color component R.This register field is extended from 32 to 128.

MDP_DMA_S_128BIN_HIST_R_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_R_DATA	Reading this register provides histogram bin data for component R.

0x051A5800+4*n MDP_DMA_S_128BIN_HIST_G_DATAn, n=[0..127]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_S_128BIN_HIST_G_DATAn register provides the histogram data corresponding to the color component G.This register field is extended from 32 to 128.

MDP_DMA_S_128BIN_HIST_G_DATAn

Bits	Name	Description
31:24	RESERVED31_24	
23:0	HIST_G_DATA	Reading this register provides histogram bin data for component G.

0x051A5C00+4*n MDP_DMA_S_128BIN_HIST_B_DATAn, n=[0..127]

Type: Read
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_S_128BIN_HIST_B_DATAn register provides the histogram data corresponding to the color component B.This register field is extended from 32 to 128.

MDP_DMA_S_128BIN_HIST_B_DATAn

Bits	Name	Description
31:24	RESERVED31_24	

MDP_DMA_S_128BIN_HIST_B_DATAn (cont.)

Bits	Name	Description
23:0	HIST_B_DATA	Reading this register provides histogram bin data for component B.

0x051A8800+ 4*n MDP_DMA_S_GC_START_COLOR_0_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component0.

MDP_DMA_S_GC_START_COLOR_0_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x051A8880+ 4*n MDP_DMA_S_GC_PARAM_COLOR_0_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component0.

MDP_DMA_S_GC_PARAM_COLOR_0_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U3.12)

0x051A8900+4*n MDP_DMA_S_GC_START_COLOR_1_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component1.

MDP_DMA_S_GC_START_COLOR_1_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x051A8980+4*n MDP_DMA_S_GC_PARAM_COLOR_1_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component1.

MDP_DMA_S_GC_PARAM_COLOR_1_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U3.12)

0x051A8A00+4*n MDP_DMA_S_GC_START_COLOR_2_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation enable and stage start value setting for component2.

MDP_DMA_S_GC_START_COLOR_2_STAGEn

Bits	Name	Description
31:17	RESERVED31_17	
16	STAGE_ENABLE	Stage enable.
15:12	RESERVED15_12	
11:0	STAGE_START_VALUE	Stage start value

0x051A8A80+4*n MDP_DMA_S_GC_PARAM_COLOR_2_STAGEn, n=[0..15]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

16 stage of Panel GC linear equation gain and offset setting for component2.

MDP_DMA_S_GC_PARAM_COLOR_2_STAGEn

Bits	Name	Description
31	RESERVED31	
30:16	STAGE_OFFSET	Stage offset (U8.7).
15	RESERVED15	
14:0	STAGE_GAIN	Stage gain (U13.2)

0x051A9000+4*n MDP_DMA_S_IGC_LSP_LUTn, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_S_IGC_LSP_LUTn registers contains the Least Significant Portion (lower 24 bits of total 36 bits) of the color lookup values for IGC LUT.

MDP_DMA_S_IGC_LSP_LUTn

Bits	Name	Description
31:28	RESERVED31_28	
27:16	LUT_COLOR1	LUT value for color1.
15:12	RESERVED15_12	
11:0	LUT_COLOR0	LUT value for color0.

0x051A9800+ 4*n MDP_DMA_S_IGC_MSP_LUTn, n=[0..255]

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: Undefined

The MDP_DMA_S_IGC_MSP_LUTn registers contains the most significant portion (color component 2) of the color lookup values for IGC LUT. The whole LUT should be written to in the sequence of LSP write first followed by MSP write, writing from lower address to higher address. Each MSP register write actually triggers the write of whole 36-bit LUT entry into the RAM.

MDP_DMA_S_IGC_MSP_LUTn

Bits	Name	Description
31:12	RESERVED31_12	
11:0	LUT_COLOR2	LUT value for color2.

0x051AA000 MDP_DMA_S_PCC1_R_C

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_C is the red plane constant coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_R_C

Bits	Name	Description
31:16	RESERVED31_16	
15:0	PCC_DATA	Reading this register provides PCC coefficient data (S13.3)

0x051AA004 MDP_DMA_S_PCC1_R_R

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_C is the red plane red coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_R_R

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA008 MDP_DMA_S_PCC1_R_G

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_G is the red plane green coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_R_G

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA00C MDP_DMA_S_PCC1_R_B

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_B is the red plane blue coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_R_B

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA010 MDP_DMA_S_PCC1_R_RR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_RR is the red plane red coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_R_RR

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA014 MDP_DMA_S_PCC1_R_GG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_GG is the red plane green coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_R_GG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA018 MDP_DMA_S_PCC1_R_BB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_BB is the red plane blue coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_R_BB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA01C MDP_DMA_S_PCC1_R_RG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_RG is the red plane red green coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_R_RG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA020 MDP_DMA_S_PCC1_R_GB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_GB is the red plane green blue coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_R_GB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA024 MDP_DMA_S_PCC1_R_RB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_RB is the red plane red blue coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_R_RB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA028 MDP_DMA_S_PCC1_R_RGB_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_RGB_0 is the first part of the red plane RGB coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_R_RGB_0

Bits	Name	Description
31:8	RESERVED31_16	
7:0	PCC_DATA	Reading this register provides PCC coefficient data (sign + 7 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x051AA02C MDP_DMA_S_PCC1_R_RGB_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_RGB_1 is the second part of the red plane RGB coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_R_RGB_1

Bits	Name	Description
31:0	PCC_DATA	Reading this register provides PCC coefficient data (remaining 32 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x051AA030 MDP_DMA_S_PCC1_G_C

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_G_C is the green plane constant coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_G_C

Bits	Name	Description
31:16	RESERVED31_16	

MDP_DMA_S_PCC1_G_C (cont.)

Bits	Name	Description
15:0	PCC_DATA	Reading this register provides PCC coefficient data (S13.3)

0x051AA034 MDP_DMA_S_PCC1_G_R

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_G_C is the green plane red coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_G_R

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA038 MDP_DMA_S_PCC1_G_G

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_G_G is the green plane green coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_G_G

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA03C MDP_DMA_S_PCC1_G_B

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_G_B is the green plane blue coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_G_B

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA040 MDP_DMA_S_PCC1_G_RR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_G_RR is the green plane red coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_G_RR

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA044 MDP_DMA_S_PCC1_G_GG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_G_GG is the green plane green coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_G_GG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA048 MDP_DMA_S_PCC1_G_BB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_G_BB is the green plane blue coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_G_BB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA04C MDP_DMA_S_PCC1_G_RG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_G_RG is the green plane red green coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_G_RG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA050 MDP_DMA_S_PCC1_G_GB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_G_GB is the green plane green blue coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_G_GB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA054 MDP_DMA_S_PCC1_G_RB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_R_RB is the green plane red blue coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_G_RB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA058 MDP_DMA_S_PCC1_G_RGB_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_G_RGB_0 is the first part of the green plane RGB coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_G_RGB_0

Bits	Name	Description
31:8	RESERVED31_16	
7:0	PCC_DATA	Reading this register provides PCC coefficient data (sign + 7 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x051AA05C MDP_DMA_S_PCC1_G_RGB_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_G_RGB_1 is the second part of the green plane RGB coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_G_RGB_1

Bits	Name	Description
31:0	PCC_DATA	Reading this register provides PCC coefficient data (remaining 32 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x051AA060 MDP_DMA_S_PCC1_B_C

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_B_C is the blue plane constant coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_B_C

Bits	Name	Description
31:16	RESERVED31_16	
15:0	PCC_DATA	Reading this register provides PCC coefficient data (S13.3)

0x051AA064 MDP_DMA_S_PCC1_B_R

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_B_C is the blue plane red coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_B_R

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA068 MDP_DMA_S_PCC1_B_G

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_B_G is the blue plane green coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_B_G

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA06C MDP_DMA_S_PCC1_B_B

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_B_B is the blue plane blue coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_B_B

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA070 MDP_DMA_S_PCC1_B_RR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_B_RR is the blue plane red coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_B_RR

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA074 MDP_DMA_S_PCC1_B_GG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_B_GG is the blue plane green coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_B_GG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA078 MDP_DMA_S_PCC1_B_BB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_B_BB is the blue plane blue coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_B_BB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA07C MDP_DMA_S_PCC1_B_RG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_B_RG is the blue plane red green coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_B_RG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA080 MDP_DMA_S_PCC1_B_GB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_B_GB is the blue plane green blue coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_B_GB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA084 MDP_DMA_S_PCC1_B_RB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_B_RB is the blue plane red blue coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_B_RB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA088 MDP_DMA_S_PCC1_B_RGB_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_B_RGB_0 is the first part of the blue plane RGB coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_B_RGB_0

Bits	Name	Description
31:8	RESERVED31_8	

MDP_DMA_S_PCC1_B_RGB_0 (cont.)

Bits	Name	Description
7:0	PCC_DATA	Reading this register provides PCC coefficient data (sign + 7 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x051AA08C MDP_DMA_S_PCC1_B_RGB_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC1_B_RGB_1 is the second part of the blue plane RGB coefficient (set 1) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC1_B_RGB_1

Bits	Name	Description
31:0	PCC_DATA	Reading this register provides PCC coefficient data (remaining 32 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x051AA100 MDP_DMA_S_PCC2_R_C

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_C is the red plane constant coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_R_C

Bits	Name	Description
31:16	RESERVED31_16	
15:0	PCC_DATA	Reading this register provides PCC coefficient data (S13.3)

0x051AA104 MDP_DMA_S_PCC2_R_R

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_C is the red plane red coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_R_R

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA108 MDP_DMA_S_PCC2_R_G

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_G is the red plane green coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_R_G

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA10C MDP_DMA_S_PCC2_R_B

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_B is the red plane blue coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_R_B

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA110 MDP_DMA_S_PCC2_R_RR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_RR is the red plane red coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_R_RR

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA114 MDP_DMA_S_PCC2_R_GG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_GG is the red plane green coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_R_GG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA118 MDP_DMA_S_PCC2_R_BB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_BB is the red plane blue coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_R_BB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA11C MDP_DMA_S_PCC2_R_RG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_RG is the red plane red green coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_R_RG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA120 MDP_DMA_S_PCC2_R_GB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_GB is the red plane green blue coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_R_GB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA124 MDP_DMA_S_PCC2_R_RB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_RB is the red plane red blue coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_R_RB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA128 MDP_DMA_S_PCC2_R_RGB_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_RGB_0 is the first part of the red plane RGB coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_R_RGB_0

Bits	Name	Description
31:8	RESERVED31_16	
7:0	PCC_DATA	Reading this register provides PCC coefficient data (sign + 7 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x051AA12C MDP_DMA_S_PCC2_R_RGB_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_RGB_1 is the second part of the red plane RGB coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_R_RGB_1

Bits	Name	Description
31:0	PCC_DATA	Reading this register provides PCC coefficient data(remaining 32 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x051AA130 MDP_DMA_S_PCC2_G_C

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_G_C is the green plane constant coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_G_C

Bits	Name	Description
31:16	RESERVED31_16	

MDP_DMA_S_PCC2_G_C (cont.)

Bits	Name	Description
15:0	PCC_DATA	Reading this register provides PCC coefficient data (S13.3)

0x051AA134 MDP_DMA_S_PCC2_G_R

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_G_C is the green plane red coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_G_R

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA138 MDP_DMA_S_PCC2_G_G

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_G_G is the green plane green coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_G_G

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA13C MDP_DMA_S_PCC2_G_B

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_G_B is the green plane blue coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_G_B

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA140 MDP_DMA_S_PCC2_G_RR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_G_RR is the green plane red coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_G_RR

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA144 MDP_DMA_S_PCC2_G_GG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_G_GG is the green plane green coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_G_GG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA148 MDP_DMA_S_PCC2_G_BB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_G_BB is the green plane blue coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_G_BB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA14C MDP_DMA_S_PCC2_G_RG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_G_RG is the green plane red green coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_G_RG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA150 MDP_DMA_S_PCC2_G_GB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_G_GB is the green plane green blue coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_G_GB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA154 MDP_DMA_S_PCC2_G_RB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_R_RB is the green plane red blue coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_G_RB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA158 MDP_DMA_S_PCC2_G_RGB_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_G_RGB_0 is the first part of the green plane RGB coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_G_RGB_0

Bits	Name	Description
31:8	RESERVED31_16	
7:0	PCC_DATA	Reading this register provides PCC coefficient data (sign + 7 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x051AA15C MDP_DMA_S_PCC2_G_RGB_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_G_RGB_1 is the second part of the green plane RGB coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_G_RGB_1

Bits	Name	Description
31:0	PCC_DATA	Reading this register provides PCC coefficient data (remaining 32 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x051AA160 MDP_DMA_S_PCC2_B_C

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_B_C is the blue plane constant coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_B_C

Bits	Name	Description
31:16	RESERVED31_16	
15:0	PCC_DATA	Reading this register provides PCC coefficient data (S13.3)

0x051AA164 MDP_DMA_S_PCC2_B_R

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_B_C is the blue plane red coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_B_R

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA168 MDP_DMA_S_PCC2_B_G

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_B_G is the blue plane green coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_B_G

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA16C MDP_DMA_S_PCC2_B_B

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_B_B is the blue plane blue coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_B_B

Bits	Name	Description
31:17	RESERVED31_17	
16:0	PCC_DATA	Reading this register provides PCC coefficient data (S2.15)

0x051AA170 MDP_DMA_S_PCC2_B_RR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_B_RR is the blue plane red coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_B_RR

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA174 MDP_DMA_S_PCC2_B_GG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_B_GG is the blue plane green coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_B_GG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA178 MDP_DMA_S_PCC2_B_BB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_B_BB is the blue plane blue coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_B_BB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA17C MDP_DMA_S_PCC2_B_RG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_B_RG is the blue plane red green coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_B_RG

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA180 MDP_DMA_S_PCC2_B_GB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_B_GB is the blue plane green blue coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_B_GB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA184 MDP_DMA_S_PCC2_B_RB

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_B_RB is the blue plane red blue coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_B_RB

Bits	Name	Description
31:28	RESERVED31_28	
27:0	PCC_DATA	Reading this register provides PCC coefficient data (S1.27)

0x051AA188 MDP_DMA_S_PCC2_B_RGB_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_B_RGB_0 is the first part of the blue plane RGB coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_B_RGB_0

Bits	Name	Description
31:8	RESERVED31_8	

MDP_DMA_S_PCC2_B_RGB_0 (cont.)

Bits	Name	Description
7:0	PCC_DATA	Reading this register provides PCC coefficient data (sign + 7 fractional bits - S1.39 for RGB_0 and RGB_1 field

0x051AA18C MDP_DMA_S_PCC2_B_RGB_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_S_PCC2_B_RGB_1 is the second part of the blue plane RGB coefficient (set 2) for the DMA_S Polynomial Color Correction block.

MDP_DMA_S_PCC2_B_RGB_1

Bits	Name	Description
31:0	PCC_DATA	Reading this register provides PCC coefficient data (remaining 32 fractional bits - S1.39 for RGB_0 and RGB_1 field

14.15.15 External Display Driver (DMA_E) registers

0x051B0000 MDP_DMA_E_CONFIG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_213f

MDP_DMA_E_CONFIG

Bits	Name	Description
31:27	RESERVED31_27	
26:25	BUF_FORMAT	The fetch buffer format setting (This field is only valid when Overlay Processor 1 is in BLT mode; otherwise this is not used, and the format is taken from FB_FORMAT in MDP_OVERLAYPROC1_OUT_OPMODE): 0x0: RGB888 (Default) 0x1: RGB565 0x2: 422 h2v1 interleaved
24	DEFLKR_EN	Deflicker Filter / Interlacer enable 0x0: disable (default) 0x1: enable
23:19	RESERVED23_19	

MDP_DMA_E_CONFIG (cont.)

Bits	Name	Description
18	BIT_MASK_POLARITY	Select the bit mask polarity. 0x0: Masked bits are set to `0' 0x1: Masked bits are set to `1'
17	RESERVED17	
16	COMP2_BIT_FLIP_EN	When set (1) flips all the bits of component2.
15	COMP1_BIT_FLIP_EN	When set (1) flips all the bits of component1.
14	COMP0_BIT_FLIP_EN	When set (1) flips all the bits of component0.
13:8	PACK_PATTERN	Packing pattern used by the packer. 0x21: Data packed as RGB (default) 0x24: Data packed as RBG 0x12: Data packed as BGR 0x18: Data packed as BRG 0x6: Data packed as GBR 0x9: Data packed as GRB
7	PACK_ALIGN	Packing alignment (within a byte) for each color component. This is valid only in parallel LCDC case where the output is packed loose. Not valid for MDDI based LCDC where the output is packed tight. 0x0: LSB (default) 0x1: MSB
6	RESERVED6	
5:4	COMP2_OUT	Number of bits for component 2 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).
3:2	COMP1_OUT	Number of bits for component 1 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).
1:0	COMP0_OUT	Number of bits for component 0 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).

0x051B0004 MDP_DMA_E_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_SIZE register defines the primary DMA fetch width and height in pixels. This register is only valid when Overlay Processor 1 is in BLT mode; otherwise this is not used, and the size is taken from MDP_OVERLAYPROC1_OUT_SIZE.

MDP_DMA_E_SIZE

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DMA_H	DMA fetch image height (in pixels). For DTV, this specifies the active region height also.
15:12	RESERVED15_12	
11:0	DMA_W	DMA fetch image width (in pixels). For DTV, this specifies the active region width also.

0x051B0008 MDP_DMA_E_BUF_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

Writing to this register forces an update to the back copy (the copy that is used currently by the DMA_E's fetch) of the frame buffer address. This register should only be done when one needs to override and switch to a new buffer in the middle of a frame. Or, when Overlay Processor 0 is in BLT mode, this address is used for DMA_E in stand-alone fetch decoupled from the Overlay Processor 1. When not in BLT mode, each new DMA_E fetch buffer address would be passed directly from MDP_OVERLAYPROC1_FB_ADDR after the Overlay Processor 1 has finished processing a frame.

MDP_DMA_E_BUF_ADDR

Bits	Name	Description
31:0	BUF_ADDR	Fetch buffer base address (byte-aligned). This defines the start of fetch pixel.

0x051B000C MDP_DMA_E_BUF_Y_STRIDE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_BUF_Y_STRIDE register defines the line jump value (in bytes) in the fetch buffer.This register is only valid when Overlay Processor 1 is in BLT mode; otherwise this is not used, and the size is taken from MDP_OVERLAYPROC1_FB_Y_STRIDE.

MDP_DMA_E_BUF_Y_STRIDE

Bits	Name	Description
31:13	RESERVED31_13	This field has no function and should be set to zero for future compatibility
12:0	BUF_Y_STRIDE	Y-stride (or) line jump value in bytes in the fetch buffer. Irrespective of whether the data is contiguous or non-contiguous, line jump value has to be provided since all the fetch requests are line-based.

0x051B0010 MDP_DMA_E_OUT_XY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_OUT_XY

Bits	Name	Description
31:28	RESERVED31_28	
27:16	DMA_OUT_Y	Display (or) screen y coordinate (pixel) where the first line of a ROI will be written. Program this parameter to zero if the output interface is TV/DTV since all TV updates are full screen.
15:12	RESERVED15_12	
11:0	DMA_OUT_X	Display (or) screen x coordinate (pixel) where the first pixel of a ROI will be written. Program this parameter to zero if the output interface is TV/DTV since all TV updates are full screen.

0x051B0014 MDP_DMA_E_LINE_COUNT

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_LINE_COUNT

Bits	Name	Description
31:12	RESERVED31_12	
11:0	LINE_COUNT	Provides the line count or write pointer value (read pointer if output to TV/DTV). This value is w.r.t. display height and not ROI height.

0x051B0018 MDP_DMA_E_LINE_IRQ

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0FFF

MDP_DMA_E_LINE_IRQ defines the line count or write_pointer value at which an interrupt has to be generated.

MDP_DMA_E_LINE_IRQ

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	IRQ_LINE	Specify the line count or write pointer value at which an interrupt has to be generated. Specify this value w.r.t. display height and not ROI height.

0x051B001C MDP_DMA_E_MASK_PATTERN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_MASK_PATTERN register defines the pattern that will be used when bit masking is enabled.

MDP_DMA_E_MASK_PATTERN

Bits	Name	Description
31:24	RESERVED31_24	
23:0	BIT_MASK_PATTERN	This pattern is used to mask the pixel bits when bit masking is enabled. If a pattern bit is set (1) the corresponding pixel bit is masked. The pattern is specified as {C2, C1, C0} where each color component is loosely packed according to the output format in to 8-bits and LSB aligned.

0x051B0020 MDP_DMA_E_PROFILE_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_PROFILE_EN

Bits	Name	Description
31:1	RESERVED31_1	
0	EN	Enable the ROI cycle counter for profiling

0x051B0024 MDP_DMA_E_PROFILE_COUNT

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_PROFILE_COUNT

Bits	Name	Description
31:24	RESERVED31_24	
23:0	TOTAL_CYCLE	Total cycle count (in AXI cycles) in a ROI, from ROI start to last pixel out of Packer (DMA_E goes back to Idle). This count will be reset automatically at the beginning of each ROI start.

0x051B0030 MDP_DMA_E_BUF_ADDR_1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 1 is used for DMA_E pipe.

MDP_DMA_E_BUF_ADDR_1

Bits	Name	Description
31:0	BUF_ADDR	Fetch buffer base address (byte-aligned). This defines the start of fetch pixel.

0x051B0034 MDP_DMA_E_BUF_ADDR_2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is Double Buffered. The register is used in DMI mode when DMI buffer ID 2 is used for DMA_E pipe.

MDP_DMA_E_BUF_ADDR_2

Bits	Name	Description
31:0	BUF_ADDR	Fetch buffer base address (byte-aligned). This defines the start of fetch pixel.

0x051B0040 MDP_DMA_E_CURSOR_FORMAT

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_CURSOR_FORMAT

Bits	Name	Description
31:3	RESERVED31_2	
2:0	CURSOR_FORMAT	0x0: ARGB8888 format (Default) 0x1: RGB888 format 0x2: ARGB1555 format 0x3: RGB565 format 0x4: ARGB4444 format 0x5: RGB444 format

0x051B0044 MDP_DMA_E_CURSOR_SIZE

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_CURSOR_SIZE register defines the hardware cursor width and height in pixels.

MDP_DMA_E_CURSOR_SIZE

Bits	Name	Description
31:23	RESERVED31_23	This field has no function and should be set to zero for future compatibility
22:16	CURSOR_H	Cursor height (in lines). Max. supported height = 64 lines.
15:7	RESERVED15_7	This field has no function and should be set to zero for future compatibility
6:0	CURSOR_W	Cursor width (in pixels). Max. supported width = 64 pixels

0x051B0048 MDP_DMA_E_CURSOR_BUF_ADDR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_CURSOR_BUF_ADDR register defines the cursor buffer address. This register is Double Buffered and the programmed value is latched in to the second buffer every Vsync.

MDP_DMA_E_CURSOR_BUF_ADDR

Bits	Name	Description
31:0	CURSOR_BUF_ADDR	Cursor buffer base address (byte-aligned).

0x051B004C MDP_DMA_E_CURSOR_POSITION

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_CURSOR_POSITION register defines the start x and y positions of the cursor relative to ROI start x and y. This register is Double Buffered and the programmed value is latched in to the second buffer every Vsync.

MDP_DMA_E_CURSOR_POSITION

Bits	Name	Description
31	CURSOR_SIZE_SEL	0x1: Start positions below are of s13 format (if required) 0x0: Start positions below are of s12 format (legacy mode - bit 13 in CURSOR_X_START and CURSOR_Y_START will be ignored.)
30:29	RESERVED30_29	This field has no function and should be set to zero for future compatibility
28:16	CURSOR_Y_START	Define the start (y) position of the cursor relative to ROI start (y). This is a signed value and has to be programmed in (s12 or s13) format, depending on CURSOR_SIZE_SEL.
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility
12:0	CURSOR_X_START	Define the start (x) position of the cursor relative to ROI start (x). This is a signed value and has to be programmed in (s12 or s13) format, depending on CURSOR_SIZE_SEL.

0x051B0060 MDP_DMA_E_CURSOR_BLEND_CONFIG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0002

MDP_DMA_E_CURSOR_BLEND_CONFIG register enables cursor blend and defines some blend parameters.

MDP_DMA_E_CURSOR_BLEND_CONFIG

Bits	Name	Description
31:4	RESERVED31_4	
3	BLEND_TRANSP_EN	Transparency check enable: 0x0: Off (Output is according to blend_alpha_sel blend output.) 0x1: On (Color keying is done on the cursor and blended result specified from the 2 layers is passed if non-matching; otherwise, the background image layer is sent.)
2:1	BLEND_ALPHA_SEL	Blending alpha select: 0x1: Cursor per pixel alpha (Default) 0x2: Constant alpha
0	BLEND_EN	Cursor blend enable (when disabled, output pixels would be the same as the background image pixels).

0x051B0064 MDP_DMA_E_CURSOR_BLEND_PARAM

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_CURSOR_BLEND_PARAM

Bits	Name	Description
31:8	RESERVED31_8	
7:0	CONSTANT_ALPHA	Constant alpha value.

0x051B0068 MDP_DMA_E_CURSOR_BLEND_TRANS_LOW

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_CURSOR_BLEND_TRANS_LOW

Bits	Name	Description
31:24	RESERVED31_24	
23:0	TRANSPARENCY_LOW	Transparent color check lower limit (Color2,Color1,Color0 each 8 bits from MSB to LSB).

0x051B006C MDP_DMA_E_CURSOR_BLEND_TRANS_HIGH

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DMA_E_CURSOR_BLEND_TRANS_HIGH

Bits	Name	Description
31:24	RESERVED31_24	
23:0	TRANSPARENCY_HIGH	Transparent color check upper limit (Color2,Color1,Color0 each 8 bits from MSB to LSB).

0x051B0070 MDP_DMA_E_Y_CLAMP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x00EB_0010

The MDP_DMA_E_Y_CLAMP register contains the 16-bit luna clamp value. The clamping can be disabled by programming a value of x00 in Y_min and xFF in Y_max

MDP_DMA_E_Y_CLAMP

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	Y_MAX	8-bit upper luma clamp value
15:8	RESERVED_BITS15_8	
7:0	Y_MIN	8-bit lower luma clamp value.

0x051B0074 MDP_DMA_E_CB_CLAMP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x00F0_0010

The MDP_DMA_E_CB_CLAMP register contains the 16-bit Cb clamp value.The clamping can be disabled by programming a value of x00 in Cb_min and xFF in Cb_max

MDP_DMA_E_CB_CLAMP

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	CB_MAX	8-bit upper Cb clamp value
15:8	RESERVED_BITS15_8	
7:0	CB_MIN	8-bit lower Cb clamp value.

0x051B0078 MDP_DMA_E_CR_CLAMP

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x00F0_0010

The MDP_DMA_E_CR_CLAMP register contains the 16-bit Cr clamp value. The clamping can be disabled by programming a value of x00 in Cr_min and xFF in Cr_max

MDP_DMA_E_CR_CLAMP

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	CR_MAX	8-bit upper Cr clamp value
15:8	RESERVED_BITS15_8	
7:0	CR_MIN	8-bit lower Cr clamp value.

0x051B1000 MDP_DMA_E_FETCH_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000f

MDP_DMA_E_FETCH_STATUS

Bits	Name	Description
31:4	RESERVED31_4	
3:0	IDLES	Fetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 3= dma_rd idle Bit 2= ctl idle Bit 1 = burstbuf idle Bit 0= unpack idle

0x051B1004 MDP_DMA_E_FETCH_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0047

MDP_DMA_E_FETCH_CFG

Bits	Name	Description
31:8	RESERVED31_8	
7	SYNC_MODE	Boundary on which fetch synchronizes certain registers in BLT mode: 0x0: frame (default) 0x1: line
6:4	MAX_BURST_SIZE	Maximum burst beat size. Possible values: 0x4: 16 (default) 0x2: 8 0x1: 4
3	RESERVED3	
2:0	REQ_DEPTH_LIMIT	Pending request limit, default 0x7 means maximum of 8 pending requests, anything less limits the AXI requests to that number + 1.

0x051B2000 MDP_DMA_E_CUR_FETCH_STATUS

Type: Read
Clock: CC_MDP_CLK
Reset State: 0x0000_000F

MDP_DMA_E_CUR_FETCH_STATUS

Bits	Name	Description
31:4	RESERVED31_4	

MDP_DMA_E_CUR_FETCH_STATUS (cont.)

Bits	Name	Description
3:0	IDLES	Fetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 3= dma_rd idle Bit 2= ctl idle Bit 1= burstbuf idle Bit 0= unpack idle

0x051B3000 MDP_DMA_E_DEFLICK_CONFIG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0080

MDP_DMA_E_DEFLICK_CONFIG

Bits	Name	Description
31:9	RESERVED31_9	
8:0	THRESHOLD	Threshold value for the Sobel filtering (u9)

0x051B3010 MDP_DMA_E_DEFLICK_COEFF0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0180_0040

The MDP_DMA_E_DEFLICK_COEFFn registers contain the set of deflicker filter coefficients, where coeff1 is for the center pixel, coeff0 is for (k-1) pixel and (k+1) pixel. Set 0 is for less than or equal to threshold filtering.

MDP_DMA_E_DEFLICK_COEFF0

Bits	Name	Description
31:26	RESERVED31_26	
25:16	COEFF1	Filter coefficient for k sample (s10).
15:10	RESERVED15_10	
9:0	COEFF0	Filter coefficient for k-1 and k+1 sample (s10).

0x051B3014 MDP_DMA_E_DEFLICK_COEFF1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0100_0080

The MDP_DMA_E_DEFLICK_COEFFn registers contain the set of deflicker filter coefficients, where coeff1 is for the center pixel, coeff0 is for (k-1) pixel and (k+1) pixel. Set 1 is for greater than threshold filtering.

MDP_DMA_E_DEFLICK_COEFF1

Bits	Name	Description
31:26	RESERVED31_26	
25:16	COEFF1	Filter coefficient for k sample (s10).
15:10	RESERVED15_10	
9:0	COEFF0	Filter coefficient for k-1 and k+1 sample (s10).

0x051B4004 MDP_DMA_E_ATV_CC_DATA

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_DMA_E_ATV_CC_DATA register contains the closed caption data for the analog TV OUT Interface

MDP_DMA_E_ATV_CC_DATA

Bits	Name	Description
31:16	CC_DATA_EVEN	CC data for the even field. Driven to the TV encoder at the next start of frame.
15:0	CC_DATA_ODD	CC data for the odd field. Driven to the TV encoder at the next start of frame.

14.15.16 DSI 2 Video / LCDC Timing Generator registers

0x051C0000 MDP_LCDC_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_EN register is used to enable the LCD controller.

NOTE Before enabling this bit make sure that the LCDC interface is selected by appropriately setting the PRIM_INTF_SEL bits in the MDP_DISP_INTF_SEL register.

MDP_LCDC_EN

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility.
0	LCDC_EN	Enable timing generation and kick start LCDC operation. NOTE If LCDC is disabled by SW in the middle of a frame period, internally the hardware will disable LCDC only at the end of the current frame (just before next Vsync).

0x051C0004 MDP_LCDC_HSYNC_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_HSYNC_CTL register defines HSYNC parameters like period and width.

MDP_LCDC_HSYNC_CTL

Bits	Name	Description
31:29	RESERVED31_29	This field has no function and should be set to zero for future compatibility.
28:16	HSYNC_PERIOD	HSYNC period in dot_clk cycles. This is the time between start of hsync pulse and the start of next hsync pulse. Note: hsync_period = Width + h_porch where, Width = Output image width h_porch = (h_back_porch + h_front_porch) h_back_porch starts at the beginning of hsync pulse Please refer to the panel data sheet or VESA specs to obtain accurate values for hsync parameters.
15:12	RESERVED15_12	This field has no function and should be set to zero for future compatibility
11:0	HSYNC_PULSE_WIDTH	HSYNC pulse width in dot_clk cycles.

0x051C0008 MDP_LCDC_VSYNC_PERIOD

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_VSYNC_PERIOD register defines the VSYNC period.

MDP_LCDC_VSYNC_PERIOD

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility.
23:0	VSYNC_PERIOD	VSYNC period in dot_clk cycles. This is the time between start of vsync pulse and the start of next vsync pulse. Note: vsync_period = Height + v_porch where, Height = Output image height v_porch = (v_back_porch + v_front_porch) v_back_porch starts at the beginning of vsync pulse Please refer to the panel data sheet or VESA specs to obtain accurate values for vsync parameters.

0x051C000C MDP_LCDC_VSYNC_PULSE_WIDTH

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_VSYNC_PULSE_WIDTH register defines the VSYNC pulse width.

MDP_LCDC_VSYNC_PULSE_WIDTH

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility.
23:0	VSYNC_PULSE_WIDTH	VSYNC pulse width in dot_clk cycles.

0x051C0010 MDP_LCDC_DISPLAY_HCTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_DISPLAY_HCTL register defines the horizontal display region (active + inactive) which can be obtained from hsync period and horizontal blanking (back and front porch) parameters.

MDP_LCDC_DISPLAY_HCTL

Bits	Name	Description
31:29	RESERVED31_29	This field has no function and should be set to zero for future compatibility
28:16	DISPLAY_END_X	Defines the time period between the start of hsync pulse and the last displayed pixel position in dot_clk cycles. Note: display_end_x = hsync_period - h_front_porch - 1 where, h_porch (dot cycles) = hsync_period - Width h_porch = (h_back_porch + h_front_porch)
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility
12:0	DISPLAY_START_X	Defines the time period between the start of hsync pulse and the first displayed pixel position in dot_clk cycles. Note: display_start_x = h_back_porch where, h_porch (dot cycles) = hsync_period - Width h_porch = (h_back_porch + h_front_porch)

0x051C0014 MDP_LCDC_DISPLAY_V_START

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_DISPLAY_V_START register defines the vertical display region (active + inactive) which can be obtained from vsync period and vertical blanking (back and front porch) parameters.

MDP_LCDC_DISPLAY_V_START

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility

MDP_LCDC_DISPLAY_V_START (cont.)

Bits	Name	Description
23:0	DISPLAY_START_Y	Defines the time period between the start of vsync pulse and the first displayed line position in dot_clk cycles. Note: display_start_y = v_back_porch where, v_porch = vsync_period - Height v_porch = (v_back_porch + v_front_porch)

0x051C0018 MDP_LCDC_DISPLAY_V_END

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_DISPLAY_V_END register defines the vertical display region (active + inactive) which can be obtained from vsync period and vertical blanking (back and front porch) parameters.

MDP_LCDC_DISPLAY_V_END

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	DISPLAY_END_Y	Defines the time period between the start of vsync pulse and the last displayed line position in dot_clk cycles. Note: display_end_y = vsync_period - v_front_porch - 1 where, v_porch = vsync_period - Height v_porch = (v_back_porch + v_front_porch)

0x051C001C MDP_LCDC_ACTIVE_HCTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_ACTIVE_HCTL register defines the horizontal parameters of LCDC active display area.

MDP_LCDC_ACTIVE_HCTL

Bits	Name	Description
31	ACTIVE_H_EN	Horizontal active region enable

MDP_LCDC_ACTIVE_HCTL (cont.)

Bits	Name	Description
30:29	RESERVED30_29	This field has no function and should be set to zero for future compatibility
28:16	ACTIVE_END_X	Defines the time period between the start of hsync pulse and the last active pixel position in dot_clk cycles (a value between `display_start_x' and `display_end_x').
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility.
12:0	ACTIVE_START_X	Defines the time period between the start of hsync pulse and the first active pixel position in dot_clk cycles (a value between `display_start_x' and `display_end_x').

0x051C0020 MDP_LCDC_ACTIVE_V_START

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_ACTIVE_V_START register defines the vertical parameters of LCDC active display area.

MDP_LCDC_ACTIVE_V_START

Bits	Name	Description
31	ACTIVE_V_EN	Vertical active region enable
30:24	RESERVED30_24	This field has no function and should be set to zero for future compatibility
23:0	ACTIVE_START_Y	Defines the time period between the start of vsync pulse and the first active line position in dot_clk cycles (a value between `display_start_y' and `display_end_y').

0x051C0024 MDP_LCDC_ACTIVE_V_END

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_ACTIVE_V_END register defines the vertical parameters of LCDC active display area.

MDP_LCDC_ACTIVE_V_END

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	ACTIVE_END_Y	Defines the time period between the start of vsync pulse and the last active line position in dot_clk cycles (a value between `display_start_y' and `display_end_y').

0x051C0028 MDP_LCDC_BORDER_CLR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_BORDER_CLR register defines border (inactive) area color for LCD display.

MDP_LCDC_BORDER_CLR

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	BORDER_COLOR	Define 24-bit border (background) color value of the inactive region of display. This color value should be packed loose for parallel LCDC and should match the output format, pack pattern and packing alignment defined in MDP_DMA_P_CONFIG. The border color programmed should be packed tight for MDDI based LCDC.

0x051C002C MDP_LCDC_UNDERFLOW_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x8000_0000

MDP_LCDC_UNDERFLOW_CTL register defines the displayed color in case of data underflow and enables the auto recovery mechanism.

MDP_LCDC_UNDERFLOW_CTL

Bits	Name	Description
31	ERR_RECOVERY_EN	Enable auto recovery during error conditions like underflow etc. 0x0: Disable 0x1: Enable (default)
30:24	RESERVED30_24	This field has no function and should be set to zero for future compatibility

MDP_LCDC_UNDERFLOW_CTL (cont.)

Bits	Name	Description
23:0	UNDERFLOW_COLOR	Define the 24 bit color value to be displayed in case of underflow. This color value should be packed loose for parallel LCDC and should match the output format, pack pattern and packing alignment defined in MDP_DMA_P_CONFIG. The border color programmed should be packed tight for MDDI based LCDC.

0x051C0030 MDP_LCDC_HSYNC_SKEW

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_HSYNC_SKEW defines the relative skew between HSYNC and VSYNC active edges.

MDP_LCDC_HSYNC_SKEW

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	HSYNC_SKEW	Define the number of dot_clk cycles HSYNC active edge is delayed from VSYNC active edge

0x051C0034 MDP_LCDC_TEST_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_TEST_CTL controls test pattern generation and defines its parameters.

MDP_LCDC_TEST_CTL

Bits	Name	Description
31	TEST_PATTERN_EN	Enable hardware test pattern generation (color rectangles)

MDP_LCDC_TEST_CTL (cont.)

Bits	Name	Description
30:28	TEST_PATTERN_SEL	Select Test Pattern 0x0: Checkered Pattern (default) 0x1: 16 Grayscale Test Pattern 0x2: 256 Grayscale of Red 0x3: 256 Grayscale of Green 0x4: 256 Grayscale of Blue 0x5: Basic Color Changing pattern 0x6: 100 Pixels of Color Var1 followed by Color Var2 repeating 0x7: Constant 24 bit Color of Color Var1
27:16	RESERVED29_16	This field has no function and should be set to zero for future compatibility
15:8	TPG_VAR1	Color rectangle height (y). Applicable only when TEST_PATTERN_SEL is 0
7:0	TPG_VAR0	Color rectangle width (x) Applicable only when TEST_PATTERN_SEL is 0

0x051C0038 MDP_LCDC_CTL_POLARITY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_CTL_POLARITY register defines the polarity of control signals to the LCD panel.

MDP_LCDC_CTL_POLARITY

Bits	Name	Description
31:3	RESERVED31_3	This field has no function and should be set to zero for future compatibility.
2	DEN_NEG	Data enable polarity 0x0: enable active high (default) 0x1: enable active low
1	VSYNC_NEG	VSYNC polarity: 0x0: VSYNC active high (default) 0x1: VSYNC active low
0	HSYNC_NEG	HSYNC polarity: 0x0: HSYNC active high (default) 0x1: HSYNC active low

0x051C003C MDP_LCDC_TEST_COL_VAR1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x00ff_ffff

MDP_LCDC_TEST_COL_VAR1 defines the color value for Var1. Only used when test pattern 6 o 7 is enabled.

MDP_LCDC_TEST_COL_VAR1

Bits	Name	Description
31:24	RESERVED31_12	This field has no function and should be set to zero for future compatibility
23:0	TPG_COLOR1	24 bit color value for Var 1 in test pattern 6 and constant color in test pattern 7

0x051C0040 MDP_LCDC_TEST_COL_VAR2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_TEST_COL_VAR2 defines the color value for Var2. Only used when test pattern 6.is enabled

MDP_LCDC_TEST_COL_VAR2

Bits	Name	Description
31:24	RESERVED31_12	This field has no function and should be set to zero for future compatibility
23:0	TPG_COLOR2	24 bit color value for Var 2 in test pattern 6

0x051C0044 MDP_LCDC_UNDERFLOW_HIDING_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0006_0FFF

MDP_LCDC_UNDERFLOW_HIDING_CTL register defines maximum lost pixel count value for interrupt generation, underflow hiding feature on/off and reset condition for accumulated lost pixel count value. This register is not Double Buffered and SW is requested to set this register before LCDC enabled. If SW wants to change this control register after LCDC enabled, SW should change this value as soon as VYNC interrupt occurs.

MDP_LCDC_UNDERFLOW_HIDING_CTL

Bits	Name	Description
31:20	RESERVED31_20	This field has no function and should be set to zero for future compatibility.
19	UNDERFLOW_COLOR_SEL	Select display color during underflow situation 0x0: UNDERFLOW_COLOR (default) 0x1: Last pixel color
18	USE_ACCUM_CNT_FOR_INT	Underflow can be detected by accumulated lost pixel count or current lost pixel count. 0x0: current lost pixel count (internal asynchronous counter value debugging purpose) 0x1: accumulated lost pixel count value (default)
17	ACCUM_LOST_PIXEL_CNT_AUTO_CLR_EN	This bit defines reset condition for internal accumulated lost pixel counter. If it is disabled (set to `0'), the internal counter is not cleared by HW so SW can check how many pixels are lost over multiple frames. Accumulated lost pixel counter is reset to zero at the every vsync when this bit is `1'or at the time SW changing this bit from `0' to `1'. 0x0: disable auto clear (debugging purpose) 0x1: enable auto clear at every vsync start time (default)
16	UNDERFLOW_HIDING_EN	Underflow hiding feature on/off, if this is disabled, the underflow interrupt is generated by legacy method. 0x0: Underflow hiding feature off (legacy method, default) 0x1: Underflow hiding feature on
15:12	RESERVED15_12	This field has no function and should be set to zero for future compatibility.
11:0	MAX_LOST_PIXEL_CNT	This value defines the maximum number of lost pixel, if the lost pixel counter (accumulated or current) is greater than this value, underflow interrupt is generated. Since LCDC/DSI2 internal FIFO is 4 pixel based, this field is also 4-pixel based. For example, if this value is 2, the real pixel count is 8. The default value is 0xFFF.

0x051C0048 MDP_LCDC_LOST_PIXEL_CNT_VALUE

Type: Read-Only
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_LOST_PIXEL_CNT gives accumulated lost pixel count value and current lost pixel count value.

MDP_LCDC_LOST_PIXEL_CNT_VALUE

Bits	Name	Description
31:28	RESERVED31_28	This field has no function and should be set to zero for future compatibility.
27:16	CUR_LOST_PIXEL_CNT	This counter value indicates the internal asynchronous counter's output value which is the number of pixels lost at the moment. This value is increased in case pixels is not ready and pixel is supposed to be output to display and is decreased in case pixel data is provided by upper pipe and this lost_pixel counter value is not zero. Since LCDC/DSI2 internal FIFO is 4 pixel based, this field is also 4-pixel based. For example, if this value is 2, the real pixel count is 8.
15:12	RESERVED15_12	This field has no function and should be set to zero for future compatibility.
11:0	ACCUM_LOST_PIXEL_CNT	This counter value indicates the total number of lost pixels. This counter value can be cleared at the every vsync by HW, this is normal mode operation, however it can be programmed to maintain the counter value at the vsync, this mode is mainly debugging purpose so we can check how much pixels are lost in multi-frames. Since LCDC/DSI2 internal FIFO is 4 pixel based, this field is also 4-pixel based. For example, if this value is 2, the real pixel count is 8.

0x051C2000 MDP_LCDC_LVDS_INTF_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_LCDC_LVDS_INTF_CTL register controls the mode of operation of the LVDS interface. Depending whether we are in Single channel (Single Pixel) or Dual channel (Dual Pixel) mode the SW should set the appropriate bits in this register. Finally the SW should enable the LCDC (LCDC_EN bit in MDP_LCDC_EN registers)

NOTE Don't write to these register bits when LCDC_EN bit is set to `1' in MDP_LCDC_EN register

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MDP_LCDC_LVDS_INTF_CTL

Bits	Name	Description
31:18	RESERVED31_18	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_INTF_CTL (cont.)

Bits	Name	Description
17	LVDS_CH2_CLK_LANE_EN	Enable clock lane on channel 2. 0x0: disable 0x1: enable
16	LVDS_CH1_CLK_LANE_EN	Enable clock lane on channel 1. 0x0: disable 0x1: enable
15	LVDS_CH2_DATA_LANE3_EN	Enable data lane 3 on channel 2. 0x0: disable 0x1: enable
14	LVDS_CH2_DATA_LANE2_EN	Enable data lane 2 on channel 2. 0x0: disable 0x1: enable
13	LVDS_CH2_DATA_LANE1_EN	Enable data lane 1on channel 2. 0x0: disable 0x1: enable
12	LVDS_CH2_DATA_LANE0_EN	Enable data lane 0 on channel 2. 0x0: disable 0x1: enable
11	LVDS_CH1_DATA_LANE3_EN	Enable data lane 3 on channel 1. 0x0: disable 0x1: enable
10	LVDS_CH1_DATA_LANE2_EN	Enable data lane 2 on channel 1. 0x0: disable 0x1: enable
9	LVDS_CH1_DATA_LANE1_EN	Enable data lane 1on channel 1. 0x0: disable 0x1: enable
8	LVDS_CH1_DATA_LANE0_EN	Enable data lane 0on channel 1. 0x0: disable 0x1: enable
7	LVDS_EN	Select LVDS output or RGB output. 0x0: RGB output 0x1: LVDS output
6	LVDS_CH2_RES_BIT	LVDS reserved bit on channel 2 in (valid only in 24 bpp mode) 0x0: set the reserved bit to 0 (default) 0x1: set the reserved bit to 1
5	LVDS_CH1_RES_BIT	LVDS reserved bit on channel 1 (valid only in 24 bpp mode) 0x0: set the reserved bit to 0 (default) 0x1: set the reserved bit to 1

MDP_LCDC_LVDS_INTF_CTL (cont.)

Bits	Name	Description
4	LVDS_CH_SWAP	Valid only in LVDS dual channel mode 0x0: Do not swap pixels on Channel1 and Channel2 (default) 0x1: Swap the Channel1 pixel with Channel2 pixel
3	LVDS_RGB_OUT	Specify Which LVDS RGB out Channels to use for 24bpp or 18bpp modes. Each LVDS Channel has 4 sub-channels of seven-bits each 0x0: Use all the four seven-bit sub-channels to pack the 24 bpp pixel and control data. (default) 0x1: Use the lower three seven-bit sub-channels to pack the 18 bpp pixel and control data
2	LVDS_MODE_SEL	One should enable these drives 10 usec after setting the LVDS_BG_EN bit to 1 0x0: Dual Channel mode (default1) 0x1: Single Channel mode
1:0	RESERVED1_0	This field is reserved and should be set to zero for future compatibility

0x051C2004 MDP_LCDC_LVDS_RESERVED1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is reserved.

MDP_LCDC_LVDS_RESERVED1

Bits	Name	Description
31:0	RESERVED31_0	This field is reserved and should be set to zero for future compatibility.

0x051C2008 MDP_LCDC_LVDS_RESERVED2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is reserved

MDP_LCDC_LVDS_RESERVED2

Bits	Name	Description
31:0	RESERVED31_0	This field is reserved and should be set to zero for future compatibility.

0x051C200C MDP_LCDC_LVDS_RESERVED3

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is reserved

MDP_LCDC_LVDS_RESERVED3

Bits	Name	Description
31:0	RESERVED31_0	This field is reserved and should be set to zero for future compatibility.

0x051C2010 MDP_LCDC_LVDS_RESERVED4

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register has the PLL parameters for the LVDS PHY

MDP_LCDC_LVDS_RESERVED4

Bits	Name	Description
31:0	RESERVED31_0	This field is reserved and should be set to zero for future compatibility.

0x051C2014 MDP_LCDC_LVDS_MUX_CTL_FOR_D0_3_TO_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0302_0100

Use the MDP_LCDC_LVDS_MUX_CTL_FOR_D0_3_TO_0 register to select which of the RGB/HS/VS/DE bits drive the LVDS Channel bits D0_3 to D0_0.

NOTE The same mux setting is mirrored to second lvds channel for bits D4_3 to D4_0 in dual LVDS mode

MDP_LCDC_LVDS_MUX_CTL_FOR_D0_3_TO_0

Bits	Name	Description
31:29	RESERVED31_29	This field has no function and should be set to zero for future compatibility.
28:24	LVDS_D0_BIT_3_SEL	Select the bit that drives D0_3 and D4_3 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 (default) 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
23:21	RESERVED23_21	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D0_3_TO_0 (cont.)

Bits	Name	Description
20:16	LVDS_D0_BIT_2_SEL	Select the bit that drives D0_2 and D4_2 output bit 0x0: R0 0x1: R1 0x2: R2 (default) 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D0_3_TO_0 (cont.)

Bits	Name	Description
12:8	LVDS_D0_BIT_1_SEL	Select the bit that drives D0_1 and D4_1 output bit 0x0: R0 0x1: R1 (default) 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
7:5	RESERVED7_5	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D0_3_TO_0 (cont.)

Bits	Name	Description
4:0	LVDS_D0_BIT_0_SEL	Select the bit that drives D0_0 and D4_0 output bit 0x0: R0 (default) 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD

0x051C2018 MDP_LCDC_LVDS_MUX_CTL_FOR_D0_6_TO_4

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0008_0504

Use the MDP_LCDC_LVDS_MUX_CTL_FOR_D0_6_TO_4 register to select which of the RGB/HS/VS/DE bits drive the LVDS Channel bits D0_6 to D0_4.

NOTE The same mux setting is mirrored to second lvds channel for bits D4_6 to D4_4 in dual LVDS mode

MDP_LCDC_LVDS_MUX_CTL_FOR_D0_6_TO_4

Bits	Name	Description
31:21	RESERVED31_21	This field has no function and should be set to zero for future compatibility.
20:16	LVDS_D0_BIT_6_SEL	Select the bit that drives D0_6 and D4_6 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 (default) 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D0_6_TO_4 (cont.)

Bits	Name	Description
12:8	LVDS_D0_BIT_5_SEL	Select the bit that drives D0_5 and D4_5 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 (default) 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
7:5	RESERVED7_5	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D0_6_TO_4 (cont.)

Bits	Name	Description
4:0	LVDS_D0_BIT_4_SEL	Select the bit that drives D0_4 and D4_4 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 (default) 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD

0x051C201C MDP_LCDC_LVDS_MUX_CTL_FOR_D1_3_TO_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0c0b_0a09

Use the MDP_LCDC_LVDS_MUX_CTL_FOR_D1_3_TO_0 register to select which of the RGB/HS/VS/DE bits drive the LVDS Channel bits D1_3 to D1_0.

NOTE The same mux setting is mirrored to second lvds channel for bits D5_3 to D5_0 in dual LVDS mode

MDP_LCDC_LVDS_MUX_CTL_FOR_D1_3_TO_0

Bits	Name	Description
31:29	RESERVED31_29	This field has no function and should be set to zero for future compatibility.
28:24	LVDS_D1_BIT_3_SEL	Select the bit that drives D1_3 and D5_3 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 (default) 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
23:21	RESERVED23_21	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D1_3_TO_0 (cont.)

Bits	Name	Description
20:16	LVDS_D1_BIT_2_SEL	Select the bit that drives D1_2 and D5_2 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 (default) 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D1_3_TO_0 (cont.)

Bits	Name	Description
12:8	LVDS_D1_BIT_1_SEL	Select the bit that drives D1_1 and D5_1 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 (default) 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
7:5	RESERVED7_5	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D1_3_TO_0 (cont.)

Bits	Name	Description
4:0	LVDS_D1_BIT_0_SEL	Select the bit that drives D1_0 and D5_0 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 (default) 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD

0x051C2020 MDP_LCDC_LVDS_MUX_CTL_FOR_D1_6_TO_4

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0011_100d

Use the MDP_LCDC_LVDS_MUX_CTL_FOR_D1_6_TO_4 register to select which of the RGB/HS/VS/DE bits drive the LVDS Channel bits D1_6 to D1_4.

NOTE The same mux setting is mirrored to second lvds channel for bits D5_6 to D5_4 in dual LVDS modes

MDP_LCDC_LVDS_MUX_CTL_FOR_D1_6_TO_4

Bits	Name	Description
31:21	RESERVED31_21	This field has no function and should be set to zero for future compatibility.
20:16	LVDS_D1_BIT_6_SEL	Select the bit that drives D1)6 and D5_6 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 (default) 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D1_6_TO_4 (cont.)

Bits	Name	Description
12:8	LVDS_D1_BIT_5_SEL	Select the bit that drives D1_5 and D5_5 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 (default) 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
7:5	RESERVED7_5	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D1_6_TO_4 (cont.)

Bits	Name	Description
4:0	LVDS_D1_BIT_4_SEL	Select the bit that drives D1_4 and D5_4 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 (default) 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD

0x051C2024 MDP_LCDC_LVDS_MUX_CTL_FOR_D2_3_TO_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x1514_1312

Use the MDP_LCDC_LVDS_MUX_CTL_FOR_D2_3_TO_0 register to select which of the RGB/HS/VS/DE bits drive the LVDS Channel bits D2_3 to D2_0.

NOTE The same mux setting is mirrored to second lvds channel for bits D6_3 to D6_0 in dual LVDS mode

MDP_LCDC_LVDS_MUX_CTL_FOR_D2_3_TO_0

Bits	Name	Description
31:29	RESERVED31_29	This field has no function and should be set to zero for future compatibility.
28:24	LVDS_D2_BIT_3_SEL	Select the bit that drives D2_3 and D6_3 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 (default) 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
23:21	RESERVED23_21	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D2_3_TO_0 (cont.)

Bits	Name	Description
20:16	LVDS_D2_BIT_2_SEL	Select the bit that drives D2_2 and D6_2 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 (default) 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D2_3_TO_0 (cont.)

Bits	Name	Description
12:8	LVDS_D2_BIT_1_SEL	Select the bit that drives D2_1 and D6_1 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 (default) 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
7:5	RESERVED7_5	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D2_3_TO_0 (cont.)

Bits	Name	Description
4:0	LVDS_D2_BIT_0_SEL	Select the bit that drives D2_0 and D6_0 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 (default) 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD

0x051C2028 MDP_LCDC_LVDS_MUX_CTL_FOR_D2_6_TO_4

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x001a_1918

Use the MDP_LCDC_LVDS_MUX_CTL_FOR_D2_6_TO_4 register to select which of the RGB/HS/VS/DE bits drive the LVDS Channel bits D2_6 to D2_4.

NOTE The same mux setting is mirrored to second lvds channel for bits D6_6 to D6_4 in dual LVDS mode

MDP_LCDC_LVDS_MUX_CTL_FOR_D2_6_TO_4

Bits	Name	Description
31:21	RESERVED31_21	This field has no function and should be set to zero for future compatibility.
20:16	LVDS_D2_BIT_6_SEL	Select the bit that drives D2_6 and D6_6 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE (default) 0x1B: RSVD
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D2_6_TO_4 (cont.)

Bits	Name	Description
12:8	LVDS_D2_BIT_5_SEL	Select the bit that drives D2_5 and D6_5 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS. (default) 0x1A: DE 0x1B: RSVD
7:5	RESERVED7_5	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D2_6_TO_4 (cont.)

Bits	Name	Description
4:0	LVDS_D2_BIT_4_SEL	Select the bit that drives D2_4 and D6_4 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS (default) 0x19: VS 0x1A: DE 0x1B: RSVD

0x051C202C MDP_LCDC_LVDS_MUX_CTL_FOR_D3_3_TO_0

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0f0e_0706

Use the MDP_LCDC_LVDS_MUX_CTL_FOR_D3_3_TO_0 register to select which of the RGB/HS/VS/DE bits drive the LVDS Channel bits D3_3 to D3_0.

NOTE The same mux setting is mirrored to second lvds channel for bits D7_3 to D7_0 in dual LVDS mode

MDP_LCDC_LVDS_MUX_CTL_FOR_D3_3_TO_0

Bits	Name	Description
31:29	RESERVED31_29	This field has no function and should be set to zero for future compatibility.
28:24	LVDS_D3_BIT_3_SEL	Select the bit that drives D3_3 and D7_3 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 (default) 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
23:21	RESERVED23_21	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D3_3_TO_0 (cont.)

Bits	Name	Description
20:16	LVDS_D3_BIT_2_SEL	Select the bit that drives D3_2 and D7_2 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 (default) 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D3_3_TO_0 (cont.)

Bits	Name	Description
12:8	LVDS_D3_BIT_1_SEL	Select the bit that drives D3_1 and D7_1 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 (default) 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
7:5	RESERVED7_5	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D3_3_TO_0 (cont.)

Bits	Name	Description
4:0	LVDS_D3_BIT_0_SEL	Select the bit that drives D3_0 and D7_0 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 (default) 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD

0x051C2030 MDP_LCDC_LVDS_MUX_CTL_FOR_D3_6_TO_4

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x001b_1716

Use the MDP_LCDC_LVDS_MUX_CTL_FOR_D3_6_TO_4 register to select which of the RGB/HS/VS/DE bits drive the LVDS Channel bits D3_6 to D3_4.

NOTE The same mux setting is mirrored to second lvds channel for bits D7_6 to D7_4 in dual LVDS mode

MDP_LCDC_LVDS_MUX_CTL_FOR_D3_6_TO_4

Bits	Name	Description
31:21	RESERVED31_21	This field has no function and should be set to zero for future compatibility.
20:16	LVDS_D3_BIT_6_SEL	Select the bit that drives D3_6 and D7_6 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD (default)
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D3_6_TO_4 (cont.)

Bits	Name	Description
12:8	LVDS_D3_BIT_5_SEL	Select the bit that drives D3_5 and D7_5 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 0x17: B7 (default) 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD
7:5	RESERVED7_5	This field has no function and should be set to zero for future compatibility.

MDP_LCDC_LVDS_MUX_CTL_FOR_D3_6_TO_4 (cont.)

Bits	Name	Description
4:0	LVDS_D3_BIT_4_SEL	Select the bit that drives D3)_4 and D7_4 output bit 0x0: R0 0x1: R1 0x2: R2 0x3: R3 0x4: R4 0x5: R5 0x6: R6 0x7: R7 0x8: G0 0x9: G1 0xA: G2 0xB: G3 0xC: G4 0xD: G5 0xE: G6 0xF: G7 0x10: B0 0x11: B1 0x12: B2 0x13: B3 0x14: B4 0x15: B5 0x16: B6 (default) 0x17: B7 0x18: HS 0x19: VS 0x1A: DE 0x1B: RSVD

0x051C2034 MDP_LCDC_LVDS_PHY_RESET

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is reserved

MDP_LCDC_LVDS_PHY_RESET

Bits	Name	Description
31:6	RESERVED31_6	This field is reserved and should be set to zero for future compatibility.

MDP_LCDC_LVDS_PHY_RESET (cont.)

Bits	Name	Description
5	PLL_RESET_POL	polarity of reset signals for LVDS PLL 0x0: active high 0x1: active low
4	PLL_HW_RESET	LVDS hardware reset for LVDS PLL. A reset pulse is issued by writing 1 followed by 0 to this bit.
3:2	RESERVED3_2	This field is reserved and should be set to zero for future compatibility.
1	PHY_RESET_POL	polarity of reset signals for LVDS PHY. 0x0: active high 0x1: active low
0	PHY_HW_RESET	LVDS hardware reset for LVDS PHY. A reset pulse is issued by writing 1 followed by 0 to this bit.

0x051C3000 MDP_LVDSPHY_PLL_CTRL_0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

NOTE The preferred names for all MDP_LVDSPHY_PLL_CTRL_n registers would be MDP_LVDSPHY_PLL_CFGn.

Output Clock Control (Debug Purpose). When it is `1`, the output clocks will be generated from reference clock. When it is '0', output clocks will be generated from PLL VCO clock.

Normal operational mode setting is 0

Power up value is 0

MDP_LVDSPHY_PLL_CTRL_0

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5	LVDSPLL_BYPASS	
4	LVDSPLL_OPEN_LOOP	Open Loop Setting. When this bit is set to 1, the Lock Time is significantly reduced compared to lock time in closed loop mode. 0=Closed Loop Mode 1= Open Loop Mode Normal operational mode setting is 0.

MDP_LVDSPHY_PLL_CTRL_0 (cont.)

Bits	Name	Description
3	LVDSPLL_PWR_MODE	PLL const-gm bias select 0: Resistor div bias is selected 1: PLL Const-gm bias is selected Normal operational mode setting is 0.
2	RESERVED_BITS2	
1	LVDSPLL_SWCAL_EN	S/W Calibration Enable Control. If the bit is `1`, then the PLL will ignore CAL_MODE and perform S/W calibration. VCO OFFSET and SLOPE will be set by MAN_OFFSET and MAN_SLOPE.We are not using the SW calibration anymore. So this bit should be set to '0'. Normal operational mode setting is 0.
0	LVDSPLL_PLL_EN	PLL Enable Signal. Analog power down. 1 = Normal Mode of operation 0 = Power Down State Normal operational mode setting is 1.

0x051C3004 MDP_LVDSPHY_PLL_CTRL_1

Type: Read/Write
Clock: WCLK
Reset State: 0x0000000E

11 bit Feed back divider Ratio. {MDP_LVDSPHY_PLL_CTRL_2[LVDSPLL_DIV_FB_10_8], LVDSPLL_DIV_FB_7_0}

000_0000_0000 = div by 1

000_0000_0001 = div by 2

000_0000_0010 = div by 3

... 111_1111_1111 = div by 2048

Normal operational value: Refer to PLL Frequency programming table in Integration guideline.

Power up value is 0000_1110

MDP_LVDSPHY_PLL_CTRL_1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	LVDSPLL_DIV_FB_7_0	

0x051C3008 MDP_LVDSPHY_PLL_CTRL_2

Type: Read/Write
Clock: WCLK
Reset State: 0x00000030

Unlock Detector Resolution Setting. 000: unlock=1 if 1 mismatch between ref_clk and fb_clk

001: unlock=1 if 2 consecutive mismatches between ref_clk and fb_clk

010: unlock=1 if 3 consecutive mismatches between ref_clk and fb_clk

...

111: unlock=1 if 8 consecutive mismatches between ref_clk and fb_clk

Normal operational mode setting is 011.

Power up value is 000

MDP_LVDSPHY_PLL_CTRL_2

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	LVDSPLL_UNLOCK_RES	
3	RESERVED_BITS3	
2:0	LVDSPLL_DIV_FB_10_8	11 bit Feed back divider Ratio. {LVDSPLL_DIV_FB_10_8,MDP_LVDSPHY_PLL_CTRL_1[LVDSPLL_DIV_FB_7_0]} 000_0000_0000 = div by 1 000_0000_0001 = div by 2 000_0000_0010 = div by 3 ... 111_1111_1111 = div by 2048 Normal operational value: Refer to PLL Frequency programming table in Integration guideline.

0x051C300C MDP_LVDSPHY_PLL_CTRL_3

Type: Read/Write
Clock: WCLK
Reset State: 0x000000C0

Calibration Mode Setting.

00 :Skip calibration and use I_MAN_OFFSET and I_MAN_SLOPE for VCO.

01/10/11 : Perform calibration for both OFFSET and SLOPE settings

Normal operational mode setting is 11

Power up value is 00_0000

MDP_LVDSPHY_PLL_CTRL_3

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:6	LVDSPLL_CAL_MODE	
5:0	LVDSPLL_DIV_REF	Reference Divider Ratio. 000000 : div by 1 000001 : div by 2 000010 : div by 3 000011 : div by 4 ... 111111 : div by 64 Normal operational value: Refer to PLL Frequency programming table in Integration guideline.

0x051C3010 MDP_LVDSPHY_PLL_CTRL_4

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_CTRL_4

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x051C3014 MDP_LVDSPHY_PLL_CTRL_5

Type: Read/Write
Clock: WCLK
Reset State: 0x00000040

Loop Filter Resistor R setting. 000: 100K

001: 75K

010: 50K

011: 35K

100: 25K

101: 20K

110: 12K

111: 8K

Normal operational value: Refer to PLL Frequency programming table in Integration guideline..

MDP_LVDSPHY_PLL_CTRL_5

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	LVDSPLL_LF_R	
3:0	RESERVED_BITS3_0	

0x051C3018 MDP_LVDSPHY_PLL_CTRL_6

Type: Read/Write
Clock: WCLK
Reset State: 0x00000003

Power up value is 0011

MDP_LVDSPHY_PLL_CTRL_6

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:4	LVDSPLL_LF_C2	Loop Filter Capacitor C2 setting.(3+B2*18+B1*9+B0*6) 000: 3pF 001: 9pF 010: 12pF 011: 18pF 100: 21pF 101: 27pF 110: 30pF 111: 36pF Normal operational value: Refer to PLL Frequency programming table in Integration guideline..

MDP_LVDSPHY_PLL_CTRL_6 (cont.)

Bits	Name	Description
3:0	LVDSPLL_LF_C1	Loop Filter Capacitor C1 setting.(20+B3*130+B2*60+B1*25+B0*15) 0000: 20pF 0001: 35pF 0010 : 45pF 0011 : 60pF 0100: 80pF 0101: 95pF 0110: 105pF 0111:120pF 1000: 150pF 1001: 165pF 1010: 175pF 1011: 190pF 1100: 210pF 1101:225pF 1110: 235pF 1111: 250pF Normal operational value: Refer to PLL Frequency programming table in Integration guideline.

0x051C301C MDP_LVDSPHY_PLL_CTRL_7

Type: Read/Write
Clock: WCLK
Reset State: 0x00000062

Power up value is 010

MDP_LVDSPHY_PLL_CTRL_7

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6:5	LVDSPLL_DIGITAL_WAITTIME	PLL Digital wait time setting. 00 : 6 REF_CLK cycles 01 :11 REF_CLK cycles 10 : 23 REF_CLK cycles 11 : 52 REF_CLK cycles Normal operational mode setting is 11.
4:3	RESERVED_BITS4_3	

MDP_LVDSPHY_PLL_CTRL_7 (cont.)

Bits	Name	Description
2:0	LVDSPLL_CP	Charge Pump Current setting. 000 : 5uA 001 : 10uA 010 : 12.5uA 011 : 17.5uA 100 : 20uA 101 : 25uA 110 : 27.5uA 111 : 32.5uA Normal operational value: Refer to PLL Frequency programming table in Integration guideline

0x051C3020 MDP_LVDSPHY_PLL_CTRL_8

Type: Read/Write
Clock: WCLK
Reset State: 0x00000040

Power up value is 0000

MDP_LVDSPHY_PLL_CTRL_8

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LVDSPLL_UNLOCK_DET_SEL	0: use negedge(50% phase detect) 1: use posedge(100% phase detect) Normal operational mode setting is 0.
6:4	LVDSPLL_VREF_CON	These bits sets the Vtune value in PLL Open Loop Mode. 000: Vtune=0.50v 001: Vtune=0.55v 010: Vtune=0.60v 011: Vtune=0.65v 100: Vtune=0.70v 101: Vtune=0.75v 110: Vtune=0.80v 111: Vtune=0.85v The preferred name for this register bit field would be LVDSPLL_VTUNE_CONF. Normal operational value: Refer to PLL Frequency programming table in Integration guideline.

MDP_LVDSPHY_PLL_CTRL_8 (cont.)

Bits	Name	Description
3:0	LVDSPLL_OUT_DIV1	Output Divider setting for oCLK1 (Bitclk). This is a high frequency clock and it goes to clock layer. 0000: div by1 0001: div by2 0010: div by3 0011: div by4 ... 1111: div by16 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. The preferred name for this register bit field would be LVDSPLL_OUT_DIV_BITCLK.

0x051C3024 MDP_LVDSPHY_PLL_CTRL_9

Type: Read/Write
Clock: WCLK
Reset State: 0x00000007

Power up value is 0000_0111

MDP_LVDSPHY_PLL_CTRL_9

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	LVDSPLL_OUT_DIV2	Output Divider setting for oCLK2. This is pixel clock going to DSI Controller. 00000000: div by1 00000001: div by2 00000010: div by3 00000011: div by4 ... 11111111: div by256 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. The preferred name for this register bit field would be LVDSPLL_OUT_DIV_BYTECLK.

0x051C3028 MDP_LVDSPHY_PLL_CTRL_10

Type: Read/Write
Clock: WCLK
Reset State: 0x00000007

Power up value is 0000_0111

MDP_LVDSPHY_PLL_CTRL_10

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	LVDSPLL_OUT_DIV3	Output Divider setting for oCLK3. This is a test clock going to DSI Controller. 00000000: div by1 00000001: div by2 00000010: div by3 00000011: div by4 ... 11111111: div by256 The preferred name for this register bit field would be LVDSPLL_OUT_DIV_DSICLK. Normal operational value: Refer to PLL Frequency programming table in Integration guideline.

0x051C302C MDP_LVDSPHY_PLL_CTRL_11

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_CTRL_11

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4	LVDSPLL_SVS_MODE	SVS. Mode Enable 0: Normal operation mode 1: SVS. operation mode In SVS. mode, bit clock, byte clock and dsi clock will be half the frequency of normal operation mode. Normal operational mode setting is 0.
3:0	RESERVED_BITS3_0	

0x051C3030 MDP_LVDSPHY_PLL_CTRL_12

Type: Read/Write
Clock: WCLK
Reset State: 0x0000001A

MDP_LVDSPHY_PLL_CTRL_12

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4:0	LVDSPLL_MAN_OFFSET	Manual setting for VCO offset Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Power on Reset value is 1_1010

0x051C3034 MDP_LVDSPHY_PLL_CTRL_13

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Power up value is 000

MDP_LVDSPHY_PLL_CTRL_13

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2:0	LVDSPLL_MAN_SLOPE	Manual setting for VCO slope Normal operational value: Refer to PLL Frequency programming table in Integration guideline.

0x051C3038 MDP_LVDSPHY_PLL_CTRL_14

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_CTRL_14

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	PLL_SW_RESET	RESET for Digital blocks except control registers . Active high signal. 1: Assertion 0: De-assertion Normal operational mode setting is 0.

MDP_LVDSPHY_PLL_CTRL_14 (cont.)

Bits	Name	Description
0	FORCE_PLL_READY	0: PLL_READY from PLL Lock detect will be used 1: PLL_READY from PLL Lock detect will be bypassed. In other words it will force the PLL_READY to high. This bit is only used as a back up in case the PLL LOCKDETECTOR does not operate correctly. Power up value is 0. Normal value is 0.

0x051C303C MDP_LVDSPHY_PLL_CTRL_15

Type: Read/Write
Clock: WCLK
Reset State: 0x00000002

MDP_LVDSPHY_PLL_CTRL_15

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	RESERVED_BITS2	
1	LVDSPLL_IBIAS_CAL_EN	PLL Ibias Calibration Enable 0: Ibias Calibration disabled 1: Ibias Calibration enabled Normal operational mode setting is 1
0	RESERVED_BITS0	

0x051C3040 MDP_LVDSPHY_PLL_CTRL_16

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_CTRL_16

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	LVDSPLL_CL_LOCKTIME_7_0	Closed Loop Lock time counter value. It specifies the Lock time in number of reference clock cycles after the reference divider. The minimum time required is 50us. Lock Time=cl_locktime<15:0>*ref_cycle_time Normal operational mode setting: 0. Power up value is 0.

0x051C3044 MDP_LVDSPHY_PLL_CTRL_17

Type: Read/Write
Clock: WCLK
Reset State: 0x00000020

MDP_LVDSPHY_PLL_CTRL_17

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	LVDSPLL_CL_LOCKTIME_15_8	Closed Loop Lock time counter value. It specifies the Lock time in number of reference clock cycles after the reference divider. The minimum time required is 50us Lock Time=cl_locktime<15:0>*ref_cycle_time. Normal operational mode setting: 0010_0000. Power up value is 0010_0000.

0x051C3048 MDP_LVDSPHY_PLL_CTRL_18

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_CTRL_18

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	LVDSPLL_OL_LOCKTIME_7_0	Open Loop Lock time. It specifies the lock time in number of reference clock cycles after the reference divider. The minimum time required is 5us. Normal operational mode setting is 1000_1000. Power up value is 0000_0000.

0x051C304C MDP_LVDSPHY_PLL_CTRL_19

Type: Read/Write
Clock: WCLK
Reset State: 0x00000002

MDP_LVDSPHY_PLL_CTRL_19

Bits	Name	Description
31:3	RESERVED_BITS31_3	

MDP_LVDSPHY_PLL_CTRL_19 (cont.)

Bits	Name	Description
2	LVDSPLL_SWCAL_DONE	We are not using SW Calibration anymore. So this bit should be set to '0'. Normal operational mode setting is 0. Power upi value is 10.
1:0	LVDSPLL_OL_LOCKTIME_9_8	Open Loop Lock time. It specifies the lock time in number of reference clock cycles after the reference divider. The minimum time required is 5us. Normal operational mode setting is 00.

0x051C3050 MDP_LVDSPHY_PLL_TEST_EFUSE

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_TEST_EFUSE

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5	PLLPHY_EFUSE_OVRRIDE_SEL	
4	PLLPHY_DRVSTR_EFUSE_SEL	1: Select the efuse used for data lane impedance calibration 0: Select dedicated PLL calibration efuse
3:0	PLLPHY_EFUSE	efuse override value 0: Use EFUSE value selected by PLLPHY_DRVSTR_EFUSE_SEL 1: Override with PLLPHY_EFUSE value. Power up value is 0000.

0x051C3054 MDP_LVDSPHY_PLL_TEST_SANITY_CHECK

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_TEST_SANITY_CHECK

Bits	Name	Description
31:1	RESERVED_BITS31_1	

MDP_LVDSPHY_PLL_TEST_SANITY_CHECK (cont.)

Bits	Name	Description
0	LVDSPLL_SANITY_CHECK	1: PLL clock frequency based on power up value. OUTCLK1 = 810MHz, OUTCLK2=OUTCLK3=(OUTCLK1/8). 0: PLL clock frequency based on PLL software configuration Normal operational mode setting is 0. Power up value is 0.

0x051C3058 MDP_LVDSPHY_PLL_DEBUG_SEL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_DEBUG_SEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	MDP_LVDSPHY_PLL_DEBUG_SEL	Refer to Table at the end of the PLL section to see detailed description of debug bus selections: Debug bus grouping

0x051C305C RESERVED_PLL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

RESERVED_PLL

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x051C3060 MDP_LVDSPHY_PLL_ANA_CTRL0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000020

MDP_LVDSPHY_PLL_ANA_CTRL0

Bits	Name	Description
31:7	RESERVED_BITS31_7	
6	LVDSPLL_REF_POLY_SEL	0: Poly select is disabled 1: Poly select is enabled

MDP_LVDSPHY_PLL_ANA_CTRL0 (cont.)

Bits	Name	Description
5	LVDSPLL_OTA_BIAS_SEL	0: OTA replica bias is disabled 1: OTA replica bias is enabled
4:1	LVDSPLL_ANA_TESTMUX_SELECT	PLL Analog Test Mux Select bits XX00: Uncalibrated bias current XX01: Calibrated bias current Normal operational mode setting is 0000.
0	LVDSPLL_ANA_TESTMUX_ENABLE	PLL Analog Test Mux Enable Normal operational mode setting is 0. Power up value is 0.

0x051C3064 MDP_LVDSPHY_PLL_ANA_CTRL1

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_ANA_CTRL1

Bits	Name	Description
31:5	RESERVED_BITS31_5	
4:1	LVDSPLL_DIGCLK_TESTMUX_SELECT	PLL Digital CLK Test Mux Select bits X000: VCO clock X001: PLL unlock detect X010: Byte clock X011: Divided reference clock X100: Reference clock X101: Feedback clock X110: DSI clock X111: VCO clock div 2 Normal operational mode setting is 0000.
0	LVDSPLL_DIGCLK_TESTMUX_EN	PLL Digital CLK Test Mux Enable Normal operational mode setting is 0. Power up value is 0.

0x051C3068 MDP_LVDSPHY_PLL_ANA_CTRL2

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_ANA_CTRL2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x051C306C MDP_LVDSPHY_PLL_ANA_CTRL3

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_ANA_CTRL3

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x051C3070 MDP_LVDSPHY_PLL_ANA_CTRL4

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_ANA_CTRL4

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x051C3074 MDP_LVDSPHY_PLL_ANA_CTRL5

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_ANA_CTRL5

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x051C3078 MDP_LVDSPHY_PLL_ANA_CTRL6

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_ANA_CTRL6

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x051C307C MDP_LVDSPHY_PLL_ANA_CTRL7

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_ANA_CTRL7

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x051C3080 MDP_LVDSPHY_PLL_RDY

Type: Read Only
Clock: WCLK
Reset State: 0x00000000

.monitor pll_rdy

Power up value is 0

MDP_LVDSPHY_PLL_RDY

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	PLL_RDY	

0x051C3084 MDP_LVDSPHY_PLL_DBGBUS_STATUS0

Type: Read Only
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_DBGBUS_STATUS0

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	MDP_LVDSPHY_PLL_DEBUG_BUS_7_0	Power up value is 0000_0000

0x051C3088 MDP_LVDSPHY_PLL_DBGBUS_STATUS1

Type: Read Only
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_DBGBUS_STATUS1

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	MDP_LVDSPHY_PLL_DEBUG_BUS_15_8	Power up value is 0000_0000

0x051C308C MDP_LVDSPHY_PLL_DBGBUS_STATUS2

Type: Read Only
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_DBGBUS_STATUS2

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	MDP_LVDSPHY_PLL_DEBUG_BUS_23_16	Power up value is 0000_0000

0x051C3090 MDP_LVDSPHY_PLL_DBGBUS_STATUS3

Type: Read Only
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_DBGBUS_STATUS3

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	MDP_LVDSPHY_PLL_DEBUG_BUS_31_24	Power up value is 0000_0000

0x051C3094 MDP_LVDSPHY_PLL_ANA_STATUS0

Type: Read only
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_ANA_STATUS0

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x051C3098 MDP_LVDSPHY_PLL_ANA_STATUS1

Type: Read only
Clock: WCLK
Reset State: 0x00000000

MDP_LVDSPHY_PLL_ANA_STATUS1

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x051C309C MDP_LVDSPHY_PLL_ANA_STATUS2

Type: Read only
Clock: WCLK
Reset State: 0x00000000

Select	Debug bus grouping	Signal Name	Description
PLL DEBUG BUS			
8'bXXXX000			Default value
	dsiphy_pll_debug_bus[31:0]	32'd0	N/A
8'bXXXX001			Debug bus monitor for sanity check
	dsiphy_pll_debug_bus[31:0]	swi_debug_bus_sanity[32:0]	Debug bus status read back for sanity check
8'bXXXX010			DEBUG_BUS_INT(from DSIPLL_CAL_LOGIC)
	dsiphy_pll_debug_bus[31:16]	16'd0	N/A
	dsiphy_pll_debug_bus[15:0]	cs[3:0]	
		o_pll_en	
		o_cal_en	
		o_wakeup	
		cal_offset[4:0]	
		cal_slope[2:0]	
		nenable	
8'bXXXX011			DEBUG_BUS_INT_1
	dsiphy_pll_debug_bus[31:12]	20'd0	N/A
	dsiphy_pll_debug_bus[11:0]	{tap_pad_hiz_en_tckl, jtag_mode}	
		{i_pll_en, po_cal_en_int, pll_rdy}	
		{nrefclk_unlock, nfbclk_unlock}	
		{pll_unlock, pll_en_valid}	
		i_unlock_det_sel	
		reset_mipi_lockdet	
		pll_lock_det	
8'bXXXX1XX			Reserved
	dsiphy_pll_debug_bus[31:0]	32'd0	N/A

MDP_LVDSPHY_PLL_ANA_STATUS2

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x051C3100 MDP_LVDSPHY_CFG0

Type: Read/write
Clock: HCLK
Reset State: 0x00

LVDSPHY config register 0.

MDP_LVDSPHY_CFG0

Bits	Name	Description
31:8	UNUSED	
7	LVDS_RIGHTCH_PWRDN_B	Shuts down all data lanes, LN4 to LN7, and clock lane, LNCK1, power which includes gating all digital clocks and disables analog block.(Active low) Note: Only Setting both LVDS_RIGHTCH_PWRDN_B & LVDS_LEFTCH_PWRDN_B denotes power collapse mode Default 1'b0 0x0: powered down
6	LVDS_LEFTCH_PWRDN_B	Shuts down all data lanes, LN0 to LN3, and clock lane, LNCK0, power which includes gating all digital clocks and disables analog block.(Active low) Note: Only Setting both LVDS_RIGHTCH_PWRDN_B & LVDS_LEFTCH_PWRDN_B denotes collapse mode Default 1'b0 0x0: powered down
5	LVDSPHY_BITCLK_SEL	Select between bitclk_l and bitclk_r Default 1'b0 0x0: Select bitclk_l 0x1: Select bitclk_r
4	LVDS_TXFF_EN	Enables Data Serialization Default 1'b0
3:1	RESERVED_BITS3_1	N/A
0	LVDSPHY_SW_RESET	LVDSPHY SW reset to reset all Digital logic except the control register. Default 1'b0

0x051C3104 MDP_LVDSPHY_CFG1

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY config register 1.

MDP_LVDSPHY_CFG1

Bits	Name	Description
31:8	UNUSED	
7	LN7_DRVR_EN	This SW bit enables High speed Driver 7 and is ORed with the control signal, lvdsphy_data_lane_en[7] Default 1'b0 0x0: Normal 0x1: Enable Driver
6	LN6_DRVR_EN	This SW bit enables High speed Driver 6 and is ORed with the control signal, lvdsphy_data_lane_en[6] Default 1'b0 0x0: Normal 0x1: Enable Driver
5	LN5_DRVR_EN	This SW bit enables High speed Driver 5 and is ORed with the control signal, lvdsphy_data_lane_en[5] Default 1'b0 0x0: Normal 0x1: Enable Driver
4	LN4_DRVR_EN	This SW bit enables High speed Driver 4 and is ORed with the control signal, lvdsphy_data_lane_en[4] Default 1'b0 0x0: Normal 0x1: Enable Driver
3	LN3_DRVR_EN	This SW bit enables High speed Driver 3 and is ORed with the control signal, lvdsphy_data_lane_en[3] Default 1'b0 0x0: Normal 0x1: Enable Driver
2	LN2_DRVR_EN	This SW bit enables High speed Driver 2 and is ORed with the control signal, lvdsphy_data_lane_en[2] Default 1'b0 0x0: Normal 0x1: Enable Driver

MDP_LVDSPHY_CFG1 (cont.)

Bits	Name	Description
1	LN1_DRVR_EN	This SW bit enables High speed Driver 1 and is ORed with the control signal, lvdsphy_data_lane_en[1] Default 1'b0 0x0: Normal 0x1: Enable Driver
0	LN0_DRVR_EN	This SW bit enables High speed Driver 0 and is ORed with the control signal, lvdsphy_data_lane_en[0] Default 1'b0 0x0: Normal 0x1: Enable Driver

0x051C3108 MDP_LVDSPHY_CFG2

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY config register 2.

MDP_LVDSPHY_CFG2

Bits	Name	Description
31:8	UNUSED	
7	PIXELCLK_SEL	SW Control to select pixelclk input for bist mode directly from the DSI PLL Default 1'b0 0x0: Select lvdsphy_pixel_clk from the MMSS Clock Control 0x1: Select pll_testclk tapped directly from the DSI PLL for BIST mode (completely independent of the controller)
6	LVDS_DIV_REF_EN	Resistor Divider Selection Default 1'b0
5	LVDS_BG_EN	Power Up/Down signal for LVDSPHY. It takes about 10usec to wake up LVDS_TX once this bit is set to 1. Default 1'b0 0x0: LVDS_TX is in power down mode 0x1: Wake up LVDS_TX
4	LVDS_BIAS_EN	Bias Enable Default 1'b0

MDP_LVDSPHY_CFG2 (cont.)

Bits	Name	Description
3:2	LVDS_CLK_PATTERN_SEL	SW Control to select CLOCK pattern. Default 2'b00 0x0: LNCK0: {4,3}, LNCK1: {4,3} 0x1: LNCK0: {4,3}, LNCK1: {3,4} 0x2: LNCK0: {3,4}, LNCK1: {4,3} 0x3: LNCK0: {3,4}, LNCK1: {3,4}
1	LVDS_CLK_DRVR_EN_1	This SW bit enables Clock Driver 1 and is ORed with the control signal, lvdsphy_clk_lane_en[1] Default 1'b0 0x0: Normal 0x1: Enable Clock Driver
0	LVDS_CLK_DRVR_EN_0	This SW bit enables Clock Driver 0 and is ORed with the control signal, lvdsphy_clk_lane_en[0] Default 1'b0 0x0: Normal 0x1: Enable Clock Driver

0x051C310C MDP_LVDSPHY_EFUSE_CFG

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY EFUSE Configuration Register

MDP_LVDSPHY_EFUSE_CFG

Bits	Name	Description
31:8	UNUSED	
7:5	RESERVED_BITS7_5	
4	EFUSE_SEL	To select SW override value for efuse Default 1'b0 0x0: HW efuse value 0x1: SW efuse value
3:0	EFUSE	If selected, SW override for efuse value Default 4'b0000

0x051C3110 MDP_LVDSPHY_SKEW_PGM0

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY Drive parameters for PGM delay control.

MDP_LVDSPHY_SKEW_PGM0

Bits	Name	Description
31:8	UNUSED	
7	RESERVED_BIT7	
6:4	LN1_SKEW_PGM	PGM Delay Control for Driver 1 Allows for (+/-) 200ps skew +25ps delay resolution per LN1_SKEW_PGM Default 1'b000
3	RESERVED_BIT3	N/A
2:0	LN0_SKEW_PGM	PGM Delay Control for Driver 0 Allows for (+/-) 200ps skew +25ps delay resolution per LN0_SKEW_PGM Default 1'b000

0x051C3114 MDP_LVDSPHY_SKEW_PGM1

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY Drive parameters for PGM delay control.

MDP_LVDSPHY_SKEW_PGM1

Bits	Name	Description
31:8	UNUSED	
7	RESERVED_BIT7	
6:4	LN3_SKEW_PGM	PGM Delay Control for Driver 3 Allows for (+/-) 200ps skew +25ps delay resolution per LN3_SKEW_PGM Default 1'b000
3	RESERVED_BIT3	N/A

MDP_LVDSPHY_SKEW_PGM1 (cont.)

Bits	Name	Description
2:0	LN2_SKEW_PGM	PGM Delay Control for Driver 2 Allows for (+/-) 200ps skew +25ps delay resolution per LN2_SKEW_PGM Default 1'b000

0x051C3118 MDP_LVDSPHY_SKEW_PGM2

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY Drive parameters for PGM delay control.

MDP_LVDSPHY_SKEW_PGM2

Bits	Name	Description
31:8	UNUSED	
7	RESERVED_BIT7	
6:4	LNCK1_SKEW_PGM	PGM Delay Control for Clock Driver 1 Allows for (+/-) 200ps skew +25ps delay resolution per LNCK1_SKEW_PGM Default 1'b000
3	RESERVED_BIT3	N/A
2:0	LNCK0_SKEW_PGM	PGM Delay Control for Clock Driver 0 Allows for (+/-) 200ps skew +25ps delay resolution per LNCK0_SKEW_PGM Default 1'b000

0x051C311C MDP_LVDSPHY_SKEW_PGM3

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY Drive parameters for PGM delay control.

MDP_LVDSPHY_SKEW_PGM3

Bits	Name	Description
31:8	UNUSED	

MDP_LVDSPHY_SKEW_PGM3 (cont.)

Bits	Name	Description
7	RESERVED_BIT7	
6:4	LN5_SKEW_PGM	PGM Delay Control for Driver 5 Allows for (+/-) 200ps skew +25ps delay resolution per LN5_SKEW_PGM Default 1'b000
3	RESERVED_BIT3	N/A
2:0	LN4_SKEW_PGM	PGM Delay Control for Driver 4 Allows for (+/-) 200ps skew +25ps delay resolution per LN4_SKEW_PGM Default 1'b000

0x051C3120 MDP_LVDSPHY_SKEW_PGM4

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY Drive parameters for PGM delay control.

MDP_LVDSPHY_SKEW_PGM4

Bits	Name	Description
31:8	UNUSED	
7	RESERVED_BIT7	
6:4	LN7_SKEW_PGM	PGM Delay Control for Driver 7 Allows for (+/-) 200ps skew +25ps delay resolution per LN7_SKEW_PGM Default 1'b000
3	RESERVED_BIT3	N/A
2:0	LN6_SKEW_PGM	PGM Delay Control for Driver 6 Allows for (+/-) 200ps skew +25ps delay resolution per LN6_SKEW_PGM Default 1'b000

0x051C3124 MDP_LVDSPHY_DRVR_PARAM0

Type: Read/Write
Clock: HCLK
Reset State: 0x01

LVDSPHY Drive parameters.

MDP_LVDSPHY_DRVR_PARAM0

Bits	Name	Description
31:8	UNUSED	
7:4	RESERVED_BITS7_4	
3	LVDS_PGM_DELAY_EN	Default 1'b0
2	LVDS_TERM_300_EN	Default 1'b0 0x1: Enabled
1	LVDS_TERM_100_EN	Default 1'b0 0x1: Enabled
0	LVDS_DRVR_SLEW_RATE	LVDS TX output rise/fall time control Default 1'b1 0x0: Off 0x1: On

0x051C3128 MDP_LVDSPHY_DRVR_PARAM1

Type: Read/Write
Clock: HCLK
Reset State: 0x05

LVDSPHY Drive parameters.

MDP_LVDSPHY_DRVR_PARAM1

Bits	Name	Description
31:8	UNUSED	
7:5	LVDS_EQ_CTRLB	Equalizer Control Default 1'b0
4	RESERVED_BIT4	N/A
3:0	LVDS_DRVR_STR_CTL	Drive Swing Control Default 4'b0101

0x051C312C MDP_LVDSPHY_DRVR_PARAM2

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY Drive parameters.

MDP_LVDSPHY_DRVR_PARAM2

Bits	Name	Description
31:8	UNUSED	
7:5	RESERVED_BITS7_5	
4	LVDS_DRVR_EMPH_CLAMP_CTRL	Default 1'b0
3	LVDS_DRVR_EMPH_PULSE_SEL	Default 1'b0
2:1	LVDS_DRVR_EMPH_STR	EMPH Strength Control Default 2'b00 0x0: 0 db 0x1: 1.5db (33%) 0x2: 2.27db (50%) 0x3: 3db (66%)
0	LVDS_DRVR_EMPH_EN	Enable the EMPH Logic Default 1'b0

0x051C3130+ 0x4*n MDP_LVDSPHY_LNn_BIST_CTL0, n=[0..7]

Type: Read/write
Clock: HCLK
Reset State: 0x00

LVDSPHY LN BIST control.

MDP_LVDSPHY_LNn_BIST_CTL0

Bits	Name	Description
31:8	UNUSED	
7	MISR_SIG_READ	Default 1'b0 0x1: Select MISR signature for the valid DATA to serializer 0x0: Select BIST error count
6	MISR_SIG_CLEAR	Default 1'b0 0x1: Clear MISR to default signature value 16hFFFF
5:4	LVDSPHY_TEST_HSTX_MUX_SEL	Default 2'b00 0x0: Select hstx_data path 0x1: Select delayed hstx_data path 0x2: Select adjacent hsrx_data 0x3: Select pll test clock input
3	LVDSPHY_HSRX_EN	Default 1'b0 0x1: Enable HSRX in BIST mode.

MDP_LVDSPHY_LNn_BIST_CTL0 (cont.)

Bits	Name	Description
2	BIST_RX_PRBS_ERROR_INJECT	Default 1'b0 0x1: Inject Error pattern into RX checker.
1	BIST_RX_PRBS_GEN_SHORT	Default 1'b0 0x1: Pattern length is 2^8 0x0: Pattern is generated continuously until bist_rx_prbs_chk_en is disabled
0	LVDSPHY_ERROR_CLR	Default 1'b0 0x1: Clear Error count.

0x051C3150+ 0x4*n MDP_LVDSPHY_LNCKn_BIST_CTL0, n=[0..1]

Type: Read/write
Clock: HCLK
Reset State: 0x00

LVDSPHY Clock Lane BIST control.

MDP_LVDSPHY_LNCKn_BIST_CTL0

Bits	Name	Description
31:8	UNUSED	
7:2	RESERVED_BITS7_2	
1:0	LVDSPHY_TEST_HSTX_MUX_SEL	Default 2'b00 0x0: Select hstx_data path 0x1: Select delayed hstx_data path 0x2: Select adjacent hsrx_data 0x3: Select pll test clock input

0x051C3158 MDP_LVDSPHY_BISTPAT_CTRL0

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY BIST Patgen & MISR Configuration register

MDP_LVDSPHY_BISTPAT_CTRL0

Bits	Name	Description
31:8	UNUSED	

MDP_LVDSPHY_BISTPAT_CTRL0 (cont.)

Bits	Name	Description
7:5	BIST_STATUS_SEL	Select which Lane BIST/MISR status needs to be read. Default 3'b0
4	LVDSPHY_MISR_EN	LVDSPHY_MISR_EN is MISR enable for all data lanes Default 1'b0
3	BIST_SERIALIZER_BYPASS	Enable Serializer bypass mode. Pattern Generator will generator serial data. Default 1'b0 0x0: Parallel BIST data 0x1: Serial BIST data (Bypass Serializer)
2:1	BIST_TX_PATSEL	selection of 2 bist pattern types. Default 2'b00 0x1: Fixed Pattern 0x2: Channel Test Pattern 0x0: Not used
0	BIST_EN_TX_PRBS	Default 1'b0

0x051C315C MDP_LVDSPHY_BISTPAT_CTRL1

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY BIST Patgen Configuration register

MDP_LVDSPHY_BISTPAT_CTRL1

Bits	Name	Description
31:8	UNUSED	
7	LVDSPHY_TEST_HSRX_MUX_SEL	Mux to select between RX input or TX loopback Default 1'b0 0x0: RX 0x1: TX Loopback
6:5	BIST_TX_TEST_PAT_SEL	Selection of channel test pattern generation. Default 2'b00 0x0: Medium Frequency Pattern (0011_0011, 1100_1100) 0x1: Low Frequency Pattern (1110_0011, 0001_1100) 0x2: High Frequency Pattern (0101_0101,1010_1010) 0x3: not used

MDP_LVDSPHY_BISTPAT_CTRL1 (cont.)

Bits	Name	Description
4:0	BIST_TX_FIXPAT_SEL	32 fixed pattern selection Default 5'b00000 <sel> : <bist_fixedpat(7:0)> 0x0: 0000_0101_1 0x1: 1111_1010_1 0x2: 1111_1111_1 0x3: 0000_0000_1 0x4: 0011_0011_1 0x5: 0101_0101 0x6: 0001_0001_1 0x7: 1110_1110_1 0x8: 1111_0100_1 0x9: 0000_1010 0xA: 0000_0110 0xB: 0111_0111 0xC: 0001_1100 0xD: 1110_0011_1 0xE: 1100_0001_1 0xF: 0011_1110 0x10: 1111_1010_2 0x11: 0000_0101_2 0x12: 0000_0000_2 0x13: 1111_1111_2 0x14: 0011_0011_2 0x15: 1010_1010 0x16: 1110_1110_2 0x17: 0001_0001_2 0x18: 1111_0100_2 0x19: 1111_0100_3 0x1A: 1111_1001 0x1B: 1000_1000 0x1C: 1110_0011_2 0x1D: 1110_0011_3 0x1E: 1100_0001_2 0x1F: 1100_0001_3

0x051C3160 MDP_LVDSPHY_BISTPAT_CTRL2

Type: Read/Write
Clock: HCLK
Reset State: 0x59

LVDSPHY BIST Patgen Configuration register

MDP_LVDSPHY_BISTPAT_CTRL2

Bits	Name	Description
31:8	UNUSED	
7	RESERVED_BIT7	
6:0	BIST_PRBS_POLY	Full programmable prbs pattern. Default pattern is 1 + x3 + x4 + x6 Default 8'b101_1001

0x051C3164 MDP_LVDSPHY_BISTPAT_CTRL3

Type: Read/Write
Clock: HCLK
Reset State: 0xFF

LVDSPHY BIST Patgen Configuration register

MDP_LVDSPHY_BISTPAT_CTRL3

Bits	Name	Description
31:8	UNUSED	
7	RESERVED_BIT7	
6:0	BIST_PRBS_SEED	rx data seed to compare w/ input data and start rx side prbs gen (tx_prbs_seed_sel has to be set to 1) Invalid values: 0x00 and 0x1F(need to confirm) Default 7'b111_1111

0x051C3168 MDP_LVDSPHY_BISTPAT_CTRL4

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY BIST Patgen Configuration register

MDP_LVDSPHY_BISTPAT_CTRL4

Bits	Name	Description
31:8	UNUSED	
7:0	LVDSPHY_BIST_SEL	LVDSPHY_BIST_SEL<i> set to one indicates the data lane i is enabled for PHY BIST. Any one of the data lane bist_sel is on will automatically enable the clock lane. Default is set to zero, data lane will be enabled by controller. Default 8'b0000_0000

0x051C316C MDP_LVDSPHY_BISTPAT_CTRL5

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY BIST Patgen Configuration register

MDP_LVDSPHY_BISTPAT_CTRL5

Bits	Name	Description
31:8	UNUSED	
7:0	BIST_RX_PRBS_CHK_EN	BIST_RX_PRBS_CHK_EN<i> is BIST prbs checker enable for each TX Slice. Bit <0> enables TX0 checker and so on. To enable bist check must to make sure BIST_EN_TX_PRBS is set to 0. (rx checker state machine start to set header sel to high, patgen start to send header).It also goes to lvds_tx as hsrx_en.Setting this bit to high also turns the high speed receiver on. Each receiver lane has its own BIST PRBS checker. Default 8'b0000_0000

0x051C3170 MDP_LVDSPHY_DEBUG_SEL

Type: Read/Write
Clock: HCLK
Reset State: 0x00

LVDSPHY Debug bus Selections

MDP_LVDSPHY_DEBUG_SEL

Bits	Name	Description
31:8	UNUSED	
7:0	DEBUG_SEL	Default 8'b0000_0000

0x051C3174+0x4*n MDP_LVDSPHY_LNn_BIST_RXCHK_STAT, n=[0..7]

Type: Read
Clock: HCLK
Reset State: 0x00

LVDSPHY BIST RX Checker Status.

MDP_LVDSPHY_LNn_BIST_RXCHK_STAT

Bits	Name	Description
31:8	UNUSED	
7:3	RESERVED_BITS7_3	
2	CHECK_DONE	This bit is set when the prbs checker is done for short pattern Default 1'b0
1	RXCHK_HEADER_SEL	PRBS checker Header sel control signal Default 1'b0
0	RXCHK_PRBS_START	PRBS checker PRBS START control signal. Default 1'b0

0x051C3194 MDP_LVDSPHY_GLBL_BIST_MISR_STAT0

Type: Read
Clock: HCLK
Reset State: 0x00

LVDSPHY GLBL BIST/MISR Status.

MDP_LVDSPHY_GLBL_BIST_MISR_STAT0

Bits	Name	Description
31:8	UNUSED	
7:0	LVDSPHY_BISTCHKERR_MISRSIG_7_0	Default 8'b0000_0000

0x051C3198 MDP_LVDSPHY_GLBL_BIST_MISR_STAT1

Type: Read
Clock: HCLK
Reset State: 0x00

LVDSPHY GLBL BIST/MISR Status.

MDP_LVDSPHY_GLBL_BIST_MISR_STAT1

Bits	Name	Description
31:8	UNUSED	
7:0	LVDSPHY_BISTCHKERR_MISRSIG_15_8	Default 8'b0000_0000

0x051C319C MDP_LVDSPHY_DEBUG_BUS0

Type: Read
Clock: HCLK
Reset State: 0x00

LVDSPHY Debug bus Status

MDP_LVDSPHY_DEBUG_BUS0

Bits	Name	Description
31:8	UNUSED	
7:0	DEBUG_BUS_7_0	Default 8'b0000_0000

0x051C31A0 MDP_LVDSPHY_DEBUG_BUS1

Type: Read
Clock: HCLK
Reset State: 0x00

LVDSPHY Debug bus Status

MDP_LVDSPHY_DEBUG_BUS1

Bits	Name	Description
31:8	UNUSED	
7:0	DEBUG_BUS_15_8	Default 8'b0000_0000

0x051C31A4 MDP_LVDSPHY_DEBUG_BUS2

Type: Read
Clock: HCLK
Reset State: 0x00

LVDSPHY Debug bus Status

MDP_LVDSPHY_DEBUG_BUS2

Bits	Name	Description
31:8	UNUSED	
7:0	DEBUG_BUS_23_16	Default 8'b0000_0000

0x051C31A8 MDP_LVDSPHY_DEBUG_BUS3

Type: Read
Clock: HCLK
Reset State: 0x00

LVDSPHY Debug bus Status

MDP_LVDSPHY_DEBUG_BUS3

Bits	Name	Description
31:8	UNUSED	
7:0	DEBUG_BUS_31_24	Default 8'b0000_0000

0x051C31AC MDP_LVDSPHY_REVISION_ID0

Type: Read
Clock: HCLK
Reset State: 0x01

LVDSPHY Revision ID

MDP_LVDSPHY_REVISION_ID0

Bits	Name	Description
31:8	UNUSED	
7:4	MINOR_3_0	Indicates expanded functionality. Minor version adds functionality while being backward compatibility for existing features. Default 4'b0000
3:0	MAJOR	Indicates different interface version. Major version changes are not backward compatible. There will be a new Programming Guide document per major revision This is the first major revision for LVDS PHY Default 4'b0001

0x051C31B0 MDP_LVDSPHY_REVISION_ID1

Type: Read
Clock: HCLK
Reset State: 0x00

LVDSPHY Revision ID

MDP_LVDSPHY_REVISION_ID1

Bits	Name	Description
31:8	UNUSED	
7:0	MINOR_11_4	Indicates expanded functionality. Minor version adds functionality while being backward compatibility for existing features. Default 8'b0000_0000

0x051C31B4 MDP_LVDSPHY_REVISION_ID2

Type: Read
Clock: HCLK
Reset State: 0x00

LVDSPHY Revision ID

MDP_LVDSPHY_REVISION_ID2

Bits	Name	Description
31:8	UNUSED	
7:0	STEP_7_0	Indicates a change in the HW which is not intended to impact SW compatibility. Default 8'b0000_0000

0x051C31B8 MDP_LVDSPHY_REVISION_ID3

Type: Read
Clock: HCLK
Reset State: 0x00

LVDSPHY Revision ID

MDP_LVDSPHY_REVISION_ID3

Bits	Name	Description
31:8	UNUSED	
7:0	STEP_15_8	Indicates a change in the HW which is not intended to impact SW compatibility. Default 8'b0000_0000

14.15.17 DTV Timing Generator registers

0x051D0000 MDP_DTV_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_EN register is used to enable DTV timing generator. The timing generator should be enabled only after all the timing registers are programmed.

OTE: Before enabling this bit make sure that the DTV/LCDC interface is selected by appropriately setting the EXT_INTF_SEL bits in the MDP_DISP_INTF_SEL register

MDP_DTV_EN

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility.
0	DTV_EN	Enable timing generation and kick start DTV operation. Note: If DTV is disabled by SW in the middle of a frame period, internally the hardware will disable DTV only at the end of the current frame (just before next Vsync).

0x051D0004 MDP_DTV_HSYNC_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x035a_003e

MDP_DTV_HSYNC_CTL register defines HSYNC parameters like period and width.

MDP_DTV_HSYNC_CTL

Bits	Name	Description
31:29	RESERVED31_29	This field has no function and should be set to zero for future compatibility.

MDP_DTV_HSYNC_CTL (cont.)

Bits	Name	Description
28:16	HSYNC_PERIOD	HSYNC period in dot_clk cycles. This is the time between start of hsync pulse and the start of next hsync pulse. Note: hsync_period = Width + h_porch where, Width = Output image width h_porch = (h_back_porch + h_front_porch) h_back_porch starts at the beginning of hsync pulse Please refer to the panel data sheet or CEA-861-D specs to obtain accurate values for hsync parameters.
15:12	RESERVED15_12	This field has no function and should be set to zero for future compatibility
11:0	HSYNC_PULSE_WIDTH	HSYNC pulse width in dot_clk cycles.

0x051D0008 MDP_DTV_VSYNC_PERIOD_F1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0006_df92

MDP_DTV_VSYNC_PERIOD_F1 register defines the VSYNC period.

MDP_DTV_VSYNC_PERIOD_F1

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility.
23:0	VSYNC_PERIOD_F1	Field1 VSYNC period in dot_clk cycles. In progressive mode this is the time between start of vsync pulse and the start of next vsync pulse Interlace mode this is the time between start of Field1 vsync pulse and the start of Field2 vsync pulse. Note: vsync_period = Height + v_porch where, Height = Output image height v_porch = (v_back_porch + v_front_porch) v_back_porch starts at the beginning of vsync pulse Please refer to the panel data sheet or CEA-861-D specs to obtain accurate values for vsync parameters.

0x051D000C MDP_DTV_VSYNC_PULSE_WIDTH_F1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_141c

MDP_DTV_VSYNC_PULSE_WIDTH_F1 register defines the VSYNC pulse width..

MDP_DTV_VSYNC_PULSE_WIDTH_F1

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility.
23:0	VSYNC_PULSE_WIDTH_F1	Field1 VSYNC pulse width in dot_clk cycles.

0x051D0010 MDP_DTV_VSYNC_PERIOD_F2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_VSYNC_PERIOD_F2 register defines the VSYNC period. This register is valid for Interlace Mode only.

MDP_DTV_VSYNC_PERIOD_F2

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility.
23:0	VSYNC_PERIOD_F2	Field2 VSYNC period in dot_clk cycles. In progressive mode this register is not used Interlace mode this is the time between start of Field2 vsync pulse and the start of Field1 vsync pulse. Note: vsync_period = Height + v_porch where, Height = Output image height v_porch = (v_back_porch + v_front_porch) v_back_porch starts at the beginning of vsync pulse Please refer to the panel data sheet or CEA-861-D specs to obtain accurate values for vsync parameters.

0x051D0014 MDP_DTV_VSYNC_PULSE_WIDTH_F2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_VSYNC_PULSE_WIDTH_F2 register defines the VSYNC pulse width. This register is valid for Interlace Mode only.

MDP_DTV_VSYNC_PULSE_WIDTH_F2

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility.
23:0	VSYNC_PULSE_WIDTH_F2	Field2 VSYNC pulse width in dot_clk cycles. Not valid for Progressive mode

0x051D0018 MDP_DTV_DISPLAY_HCTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0349_007a

MDP_DTV_DISPLAY_HCTL register defines the horizontal display region (active + inactive) which can be obtained from hsync period and horizontal blanking (back and front porch) parameters.

MDP_DTV_DISPLAY_HCTL

Bits	Name	Description
31:29	RESERVED31_29	This field has no function and should be set to zero for future compatibility
28:16	DISPLAY_END_X	Defines the time period between the start of hsync pulse and the last displayed pixel position in dot_clk cycles. Note: display_end_x = hsync_period - h_front_porch - 1 where, h_porch (dot cycles) = hsync_period - Width h_porch = (h_back_porch + h_front_porch)
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility

MDP_DTV_DISPLAY_HCTL (cont.)

Bits	Name	Description
12:0	DISPLAY_START_X	Defines the time period between the start of hsync pulse and the first displayed pixel position in dot_clk cycles. Note: display_start_x = h_back_porch where, h_porch (dot cycles) = hsync_period - Width h_porch = (h_back_porch + h_front_porch)

0x051D001C MDP_DTV_DISPLAY_V_START_F1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_78a8

MDP_DTV_DISPLAY_V_START_F1 register defines the vertical display region (active + inactive) which can be obtained from vsync period and vertical blanking (back and front porch) parameters.

MDP_DTV_DISPLAY_V_START_F1

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	DISPLAY_START_Y_F1	Defines the time period between the field1 start of vsync pulse and the first displayed line position in dot_clk cycles. Note: display_start_y = v_back_porch where, v_porch = vsync_period - Height v_porch = (v_back_porch + v_front_porch)

0x051D0020 MDP_DTV_DISPLAY_V_END_F1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0006_c167

MDP_DTV_DISPLAY_V_END_F1 register defines the vertical display region (active + inactive) which can be obtained from vsync period and vertical blanking (back and front porch) parameters.

MDP_DTV_DISPLAY_V_END_F1

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	DISPLAY_END_Y_F1	Defines the time period between the field1 start of vsync pulse and the last displayed line position in dot_clk cycles. Note: display_end_y = vsync_period - v_front_porch - 1 where, v_porch = vsync_period - Height v_porch = (v_back_porch + v_front_porch)

0x051D0024 MDP_DTV_DISPLAY_V_START_F2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_DISPLAY_V_START_F2 register defines the vertical display region (active + inactive) which can be obtained from vsync period and vertical blanking (back and front porch) parameters.

MDP_DTV_DISPLAY_V_START_F2

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	DISPLAY_START_Y_F2	Defines the time period between the field2 start of vsync pulse and the first displayed line position in dot_clk cycles. Note: display_start_y = v_back_porch where, v_porch = vsync_period - Height v_porch = (v_back_porch + v_front_porch)

0x051D0028 MDP_DTV_DISPLAY_V_END_F2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_DISPLAY_V_END_F2 register defines the vertical display region (active + inactive) which can be obtained from vsync period and vertical blanking (back and front porch) parameters.

MDP_DTV_DISPLAY_V_END_F2

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	DISPLAY_END_Y_F2	Defines the time period between the field2 start of vsync pulse and the last displayed line position in dot_clk cycles. Note: display_end_y = vsync_period - v_front_porch - 1 where, v_porch = vsync_period - Height v_porch = (v_back_porch + v_front_porch)

0x051D002C MDP_DTV_ACTIVE_HCTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_ACTIVE_HCTL register defines the horizontal parameters of DTV active display area.

MDP_DTV_ACTIVE_HCTL

Bits	Name	Description
31	ACTIVE_H_EN	Horizontal active region enable
30:29	RESERVED30_29	This field has no function and should be set to zero for future compatibility
28:16	ACTIVE_END_X	Defines the time period between the start of hsync pulse and the last active pixel position in dot_clk cycles (a value between `display_start_x' and `display_end_x').
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility.
12:0	ACTIVE_START_X	Defines the time period between the start of hsync pulse and the first active pixel position in dot_clk cycles (a value between `display_start_x' and `display_end_x').

0x051D0030 MDP_DTV_ACTIVE_V_START_F1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_ACTIVE_V_START_F1 register defines the vertical parameters of DTV active display area.

MDP_DTV_ACTIVE_V_START_F1

Bits	Name	Description
31	ACTIVE_V_EN	Vertical active region enable
30:24	RESERVED30_24	This field has no function and should be set to zero for future compatibility
23:0	ACTIVE_START_Y_F1	Defines the time period between the start of vsync pulse and the first active line position in dot_clk cycles (a value between `display_start_y' and `display_end_y').

0x051D0034 MDP_DTV_ACTIVE_V_START_F2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_ACTIVE_V_START_F2 register defines the vertical parameters of DTV active display area.

MDP_DTV_ACTIVE_V_START_F2

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	ACTIVE_START_Y_F2	Defines the time period between the start of field2 vsync pulse and the first active line position in dot_clk cycles (a value between `display_start_y' and `display_end_y').

0x051D0038 MDP_DTV_ACTIVE_V_END_F1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_ACTIVE_V_END_F1register defines the vertical parameters of DTV active display area.

MDP_DTV_ACTIVE_V_END_F1

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility

MDP_DTV_ACTIVE_V_END_F1 (cont.)

Bits	Name	Description
23:0	ACTIVE_END_Y_F1	Defines the time period between the start of field1 vsync pulse and the last active line position in dot_clk cycles (a value between `display_start_y' and `display_end_y').

0x051D003C MDP_DTV_ACTIVE_V_END_F2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_ACTIVE_V_END_F2 register defines the vertical parameters of DTV active display area. This register is valid in Interlace mode only

MDP_DTV_ACTIVE_V_END_F2

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	ACTIVE_END_Y_F2	Defines the time period between the start of field2 vsync pulse and the last active line position in dot_clk cycles (a value between `display_start_y' and `display_end_y').

0x051D0040 MDP_DTV_BORDER_CLR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_BORDER_CLR register defines border(inactive) area color for LCD display.

MDP_DTV_BORDER_CLR

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	BORDER_COLOR	Define 24-bit border (background) color value of the inactive region of display. This color value should be packed loose for parallel DTV and should match the output format, pack pattern and packing alignment defined in MDP_DMA_P_CONFIG.

0x051D0044 MDP_DTV_UNDERFLOW_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x8000_0000

MDP_DTV_UNDERFLOW_CTL register defines the displayed color in case of data underflow and enables the auto recovery mechanism.

MDP_DTV_UNDERFLOW_CTL

Bits	Name	Description
31	ERR_RECOVERY_EN	Enable auto recovery during error conditions like underflow etc. 0x0: Disable 0x1: Enable (default)
30:24	RESERVED30_24	This field has no function and should be set to zero for future compatibility
23:0	UNDERFLOW_COLOR	Define the 24 bit color value to be displayed in case of underflow. This color value should be packed loose for parallel DTV and should match the output format, pack pattern and packing alignment defined in MDP_DMA_P_CONFIG. The border color programmed should be packed tight for MDDI based DTV.

0x051D0048 MDP_DTV_HSYNC_SKEW

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_HSYNC_SKEW defines the relative skew between HSYNC and VSYNC active edges.

MDP_DTV_HSYNC_SKEW

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	HSYNC_SKEW	Define the number of dot_clk cycles HSYNC active edge is delayed from VSYNC active edge

0x051D004C MDP_DTV_TEST_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_TEST_CTL controls test pattern generation and defines its parametersh

MDP_DTV_TEST_CTL

Bits	Name	Description
31	TEST_PATTERN_EN	Enable hardware test pattern generation (color rectangles)
30:28	TEST_PATTERN_SEL	Select Test Pattern 0x0: Checkered Pattern (default) 0x1: 16 Grayscale Test Pattern 0x2: 256 Grayscale of Red 0x3: 256 Grayscale of Green 0x4: 256 Grayscale of Blue 0x5: Basic Color Changing pattern 0x6: 100 Pixels of Color Var1 followed by Color Var2 repeating 0x7: Constant 24 bit Color of Color Var1
27:16	RESERVED29_16	This field has no function and should be set to zero for future compatibility
15:8	TPG_VAR1	Color rectangle height (y). Applicable only when TEST_PATTERN_SEL is 0
7:0	TPG_VAR0	Color rectangle width (x) Applicable only when TEST_PATTERN_SEL is 0

0x051D0050 MDP_DTV_CTL_POLARITY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_CTL_POLARITY register defines the polarity of control signals to the LCD panel.

MDP_DTV_CTL_POLARITY

Bits	Name	Description
31:3	RESERVED31_3	This field has no function and should be set to zero for future compatibility.
2	DEN_NEG	Data enable polarity 0x0: enable active high (default) 0x1: enable active low
1	VSYNC_NEG	VSYNC polarity: 0x0: VSYNC active high (default) 0x1: VSYNC active low
0	HSYNC_NEG	HSYNC polarity: 0x0: HSYNC active high (default) 0x1: HSYNC active low

0x051D0058 MDP_DTV_CFG

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_CFG register is used to configure the output mode and to enable the DTV timing generator

NOTE Don't write to these registe bits when DTV_EN bit is set to `1' in MDP_DTV_EN register

MDP_DTV_CFG

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility.
11	DSUB_EN	Select RGB DSUB Interface over HDMI interface 0x0: Disable DSUB interface (default) 0x1: Enable DSUB interface
10	DTV_PACK_ALIGN	Packing alignment (within a 24 bit dtv out data bus). This is valid only in DTV 16 bit, 12 bit & 8 bit modes. For eg: In DTV 16 bit mode if this bit is `0' then the 16 bit out maps to LSB bits of the 24 bit dtv out bus( i.e pixel value in [15:0] maps to [15:0] of the dtv out bus). If this bit is set to `1' then the 16 bit bus is mapped to MSB bits of 24 bit out bus (i.e., pixel vallue [15:0] maps to [23:8] of dtv out bus). This mode isnNot valid for MDDI based LCDC where the output is packed tight. 0x0: LSB (default) 0x1: MSB
9:8	PACK_422	This field allows one to configure the DTV OUT packing for YCbCr4:2:2 format (MSB to LSB byte). For eg: If we are in 16 bit OUT mode and this field is set to 0x2 then we will send Y1Cr1 in first cycle followed by Y2Cb1. The process will then repeat every two cycles 0x0: Y2Cr1Y1Cb1 (default) 0x1: Cr1Y2Cb1Y1 0x2: Y2Cb1Y1Cr1 0x3: Cb1Y2Cr1Y1
7	RESERVED7	This field has no function and should be set to zero for future compatibility
6:4	OUT_MODE	Output Mode. 0x0: YCbCr or RGB 4:4:4 Separate Syncs 24 bit interface (default) 0x1: Reserved 0x2: YCbCr 4:2:2 Separate Syncs 16 bit interface
3:2	RESERVED3_2	This field has no function and should be set to zero for future compatibility.

MDP_DTV_CFG (cont.)

Bits	Name	Description
1	DTV_REPEAT_PIXEL	Repeat the pixel in active area. This mode is intended to be used for 720x480i, 720x576i, 720x240p, 720x288p DTV resolutions. 0x0: Do not Repeat the Pixel (default) 0x1: Repeat the pixel
0	INTRLACE_MODE	Interlace enable 0x0: Progressive Out (default) 0x1: Interlace Out

0x051D005C MDP_DTV_TEST_COL_VAR1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x00ff_ffff

MDP_DTV_TEST_COL_VAR1 defines the color value for Var1 . Only used when test pattern 6 or7 is enabled.

MDP_DTV_TEST_COL_VAR1

Bits	Name	Description
31:24	RESERVED31_12	This field has no function and should be set to zero for future compatibility
23:0	TPG_COLOR1	24 bit color value for Var 1 in test pattern 6 and constant color in test pattern 7

0x051D0060 MDP_DTV_TEST_COL_VAR2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_TEST_COL_VAR2 defines the color value for Var2. Only used when test pattern 6 is enabled.

MDP_DTV_TEST_COL_VAR2

Bits	Name	Description
31:24	RESERVED31_12	This field has no function and should be set to zero for future compatibility
23:0	TPG_COLOR2	24 bit color value for Var 1 in test pattern 6

0x051D0064 MDP_DTV_UNDERFLOW_HIDING_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0006_0FFF

MDP_DTV_UNDERFLOW_HIDING_CTL register defines maximum lost pixel count value for interrupt generation, underflow hiding feature on/off and reset condition for accumalated lost pixel count value. This register is not Double Buffered and SW is requested to set this register before LCDC enabled. If SW wants to change this control register after LCDC enabled, SW should change this value as soon as VYNC interrupt occurs.

MDP_DTV_UNDERFLOW_HIDING_CTL

Bits	Name	Description
31:20	RESERVED31_20	This field has no function and should be set to zero for future compatibility.
19	UNDERFLOW_COLOR_SEL	Select display color during underfow situation 0x0: UNDERFLOW_COLOR (default) 0x1: Last pixel color
18	USE_ACCUM_CNT_FOR_INT	Underflow can be detected by accumulated lost pixel count or current lost pixel count. 0x0: current lost pixel count (internal asynchronous counter value debugging purpose) 0x1: accumulated lost pixel count value (default)
17	ACCUM_LOST_PIXEL_CNT_AUTO_CLR_EN	This bit defines reset condition for internal accumulated lost pixel counter. If it is disabled(set to `0'), the internal counter is not cleared by HW so SW can check how many pixels are lost over multiple frames. Accumulated lost pixel counter is reset to zero at the every vsync when this bit is `1'or at the time SW changing this bit from `0' to `1'. 0x0: disalbe auto clear (debugging purpose) 0x1: enable auto clear at every vsync start time (default)
16	UNDERFLOW_HIDING_EN	Underflow hiding feature on/off, if this is disabled, the underflow interrupt is generated by legacy method. 0x0: Underflow hiding feature off (legacy method, default) 0x1: Underflow hiding feature on
15:12	RESERVED15_12	This field has no function and should be set to zero for future compatibility.
11:0	MAX_LOST_PIXEL_CNT	This value defines the maximum number of lost pixel, if the lost pixel counter(accumulated or current) is greater than this value, underflow interrupt is generated. Since DSI1 internal FIFO is 2 pixel based, this field is also 2-pixel based. For example, if this value is 2, the real pixel count is 4.The default value is 0xFFF.

0x051D0068 MDP_DTV_LOST_PIXEL_CNT_VALUE

Type: Read-Only
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DTV_LOST_PIXEL_CNT gives accumulated lost pixel count value and current lost pixel count value.

MDP_DTV_LOST_PIXEL_CNT_VALUE

Bits	Name	Description
31:28	RESERVED31_28	This field has no function and should be set to zero for future compatibility.
27:16	CUR_LOST_PIXEL_CNT	This counter value indicates the internal asynchronous counter's output value which is the number of pixels losted at the moment. This value is increased in case pixels is not ready and pixel is supposed to be output to display and is decreased in case pixel data is provided by upper pipe and this lost_pixel counter value is not zero. Since DSI1 internal FIFO is 2 pixel based, this field is also 2-pixel based. For example, if this value is 2, the real pixel count is 4.
15:12	RESERVED15_12	This field has no function and should be set to zero for future compatibility.
11:0	ACCUM_LOST_PIXEL_CNT	This counter value indicates the total number of lost pixels. This counter value can be cleared at the every vsync by HW, this is normal mode operation, however it can be programmed to maintain the counter value at the vsync, this mode is mainly debugging purpose so we can check how much pixels are lost in multi-frames. Since DSI1 internal FIFO is 2 pixel based, this field is also 2-pixel based. For example, if this value is 2, the real pixel count is 4.

14.15.18 DSI 1 Video Mode Timing Generator registers

0x051E0000 MDP_DSI_VIDEO_EN

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_EN register is used to enable the LCD controller.

NOTE Before enabling this bit make sure that the DSI_VIDEO interface is selected by appropriately setting the PRIM_INTF_SEL bits in the MDP_DISP_INTF_SEL register.

MDP_DSI_VIDEO_EN

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility.
0	DSI_VIDEO_EN	Enable timing generation and kick start DSI_VIDEO operation. NOTE If DSI_VIDEO is disabled by SW in the middle of a frame period, internally the hardware will disable DSI_VIDEO only at the end of the current frame (just before next Vsync).

0x051E0004 MDP_DSI_VIDEO_HSYNC_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_HSYNC_CTL register defines HSYNC parameters like period and width.

MDP_DSI_VIDEO_HSYNC_CTL

Bits	Name	Description
31:29	RESERVED31_29	This field has no function and should be set to zero for future compatibility.
28:16	HSYNC_PERIOD	HSYNC period in dot_clk cycles. This is the time between start of hsync pulse and the start of next hsync pulse. Note: hsync_period = Width + h_porch where, Width = Output image width h_porch = (h_back_porch + h_front_porch) h_back_porch starts at the beginning of hsync pulse Please refer to the panel data sheet or VESA specs to obtain accurate values for hsync parameters.
15:12	RESERVED15_12	This field has no function and should be set to zero for future compatibility
11:0	HSYNC_PULSE_WIDTH	HSYNC pulse width in dot_clk cycles.

0x051E0008 MDP_DSI_VIDEO_VSYNC_PERIOD

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_VSYNC_PERIOD register defines the VSYNC period.

MDP_DSI_VIDEO_VSYNC_PERIOD

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility.
23:0	VSYNC_PERIOD	VSYNC period in dot_clk cycles. This is the time between start of vsync pulse and the start of next vsync pulse. Note: vsync_period = Height + v_porch where, Height = Output image height v_porch = (v_back_porch + v_front_porch) v_back_porch starts at the beginning of vsync pulse Please refer to the panel data sheet or VESA specs to obtain accurate values for vsync parameters.

0x051E000C MDP_DSI_VIDEO_VSYNC_PULSE_WIDTH

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_VSYNC_PULSE_WIDTH register defines the VSYNC pulse width.

MDP_DSI_VIDEO_VSYNC_PULSE_WIDTH

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility.
23:0	VSYNC_PULSE_WIDTH	VSYNC pulse width in dot_clk cycles.

0x051E0010 MDP_DSI_VIDEO_DISPLAY_HCTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_DISPLAY_HCTL register defines the horizontal display region (active + inactive) which can be obtained from hsync period and horizontal blanking (back and front porch) parameters.

MDP_DSI_VIDEO_DISPLAY_HCTL

Bits	Name	Description
31:29	RESERVED31_29	This field has no function and should be set to zero for future compatibility
28:16	DISPLAY_END_X	Defines the time period between the start of hsync pulse and the last displayed pixel position in dot_clk cycles. Note: display_end_x = hsync_period - h_front_porch - 1 where, h_porch (dot cycles) = hsync_period - Width h_porch = (h_back_porch + h_front_porch)
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility
12:0	DISPLAY_START_X	Defines the time period between the start of hsync pulse and the first displayed pixel position in dot_clk cycles. Note: display_start_x = h_back_porch where, h_porch (dot cycles) = hsync_period - Width h_porch = (h_back_porch + h_front_porch)

0x051E0014 MDP_DSI_VIDEO_DISPLAY_V_START

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_DISPLAY_V_START register defines the vertical display region (active + inactive) which can be obtained from vsync period and vertical blanking (back and front porch) parameters.

MDP_DSI_VIDEO_DISPLAY_V_START

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	DISPLAY_START_Y	Defines the time period between the start of vsync pulse and the first displayed line position in dot_clk cycles. Note: display_start_y = v_back_porch where, v_porch = vsync_period - Height v_porch = (v_back_porch + v_front_porch)

0x051E0018 MDP_DSI_VIDEO_DISPLAY_V_END

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_DISPLAY_V_END register defines the vertical display region (active + inactive) which can be obtained from vsync period and vertical blanking (back and front porch) parameters.

MDP_DSI_VIDEO_DISPLAY_V_END

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	DISPLAY_END_Y	Defines the time period between the start of vsync pulse and the last displayed line position in dot_clk cycles. Note: display_end_y = vsync_period - v_front_porch - 1 where, v_porch = vsync_period - Height v_porch = (v_back_porch + v_front_porch)

0x051E001C MDP_DSI_VIDEO_ACTIVE_HCTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_ACTIVE_HCTL register defines the horizontal parameters of DSI_VIDEO active display area.

MDP_DSI_VIDEO_ACTIVE_HCTL

Bits	Name	Description
31	ACTIVE_H_EN	Horizontal active region enable
30:29	RESERVED30_29	This field has no function and should be set to zero for future compatibility
28:16	ACTIVE_END_X	Defines the time period between the start of hsync pulse and the last active pixel position in dot_clk cycles (a value between `display_start_x' and `display_end_x').
15:13	RESERVED15_13	This field has no function and should be set to zero for future compatibility.
12:0	ACTIVE_START_X	Defines the time period between the start of hsync pulse and the first active pixel position in dot_clk cycles (a value between `display_start_x' and `display_end_x').

0x051E0020 MDP_DSI_VIDEO_ACTIVE_V_START

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_ACTIVE_V_START register defines the vertical parameters of DSI_VIDEO active display area.

MDP_DSI_VIDEO_ACTIVE_V_START

Bits	Name	Description
31	ACTIVE_V_EN	Vertical active region enable
30:24	RESERVED30_24	This field has no function and should be set to zero for future compatibility
23:0	ACTIVE_START_Y	Defines the time period between the start of vsync pulse and the first active line position in dot_clk cycles (a value between `display_start_y' and `display_end_y').

0x051E0024 MDP_DSI_VIDEO_ACTIVE_V_END

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_ACTIVE_V_END register defines the vertical parameters of DSI_VIDEO active display area.

MDP_DSI_VIDEO_ACTIVE_V_END

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	ACTIVE_END_Y	Defines the time period between the start of vsync pulse and the last active line position in dot_clk cycles (a value between `display_start_y' and `display_end_y').

0x051E0028 MDP_DSI_VIDEO_BORDER_CLR

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_BORDER_CLR register defines border (inactive) area color for LCD display.

MDP_DSI_VIDEO_BORDER_CLR

Bits	Name	Description
31:24	RESERVED31_24	This field has no function and should be set to zero for future compatibility
23:0	BORDER_COLOR	Define 24-bit border (background) color value of the inactive region of display. This color value should be packed loose for parallel DSI_VIDEO and should match the output format, pack pattern and packing alignment defined in MDP_DMA_P_CONFIG. The border color programmed should be packed tight for MDDI based DSI_VIDEO.

0x051E002C MDP_DSI_VIDEO_UNDERFLOW_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x8000_0000

MDP_DSI_VIDEO_UNDERFLOW_CTL register defines the displayed color in case of data underflow and enables the auto recovery mechanism.

MDP_DSI_VIDEO_UNDERFLOW_CTL

Bits	Name	Description
31	ERR_RECOVERY_EN	Enable auto recovery during error conditions like underflow etc. 0x0: Disable 0x1: Enable (default)
30:24	RESERVED30_24	This field has no function and should be set to zero for future compatibility
23:0	UNDERFLOW_COLOR	Define the 24 bit color value to be displayed in case of underflow. This color value should be packed loose for parallel DSI_VIDEO and should match the output format, pack pattern and packing alignment defined in MDP_DMA_P_CONFIG. The border color programmed should be packed tight for MDDI based DSI_VIDEO.

0x051E0030 MDP_DSI_VIDEO_HSYNC_SKEW

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_HSYNC_SKEW defines the relative skew between HSYNC and VSYNC active edges.

MDP_DSI_VIDEO_HSYNC_SKEW

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility
11:0	HSYNC_SKEW	Define the number of dot_clk cycles HSYNC active edge is delayed from VSYNC active edge

0x051E0034 MDP_DSI_VIDEO_TEST_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_TEST_CTL controls test pattern generation and defines its parameters.

MDP_DSI_VIDEO_TEST_CTL

Bits	Name	Description
31	TEST_PATTERN_EN	Enable hardware test pattern generation (color rectangles)
30:28	TEST_PATTERN_SEL	Select Test Pattern 0x0: Checkered Pattern (default) 0x1: 16 Grayscale Test Pattern 0x2: 256 Grayscale of Red 0x3: 256 Grayscale of Green 0x4: 256 Grayscale of Blue 0x5: Basic Color Changing pattern 0x6: 100 Pixels of Color Var1 followed by Color Var2 repeating 0x7: Constant 24 bit Color of Color Var1
27:16	RESERVED29_16	This field has no function and should be set to zero for future compatibility
15:8	TPG_VAR1	Color rectangle height (y). Applicable only when TEST_PATTERN_SEL is 0
7:0	TPG_VAR0	Color rectangle width (x) Applicable only when TEST_PATTERN_SEL is 0

0x051E0038 MDP_DSI_VIDEO_CTL_POLARITY

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_CTL_POLARITY register defines the polarity of control signals to the LCD panel.

MDP_DSI_VIDEO_CTL_POLARITY

Bits	Name	Description
31:3	RESERVED31_3	This field has no function and should be set to zero for future compatibility.
2	DEN_NEG	Data enable polarity 0x0: enable active high (default) 0x1: enable active low
1	VSYNC_NEG	VSYNC polarity: 0x0: VSYNC active high (default) 0x1: VSYNC active low
0	HSYNC_NEG	HSYNC polarity: 0x0: HSYNC active high (default) 0x1: HSYNC active low

0x051E003C MDP_DSI_VIDEO_TEST_COL_VAR1

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x00ff_ffff

MDP_DSI_VIDEO_TEST_COL_VAR1 defines the color value for Var1. Only used when test pattern 6 o 7 is enabled.

MDP_DSI_VIDEO_TEST_COL_VAR1

Bits	Name	Description
31:24	RESERVED31_12	This field has no function and should be set to zero for future compatibility
23:0	TPG_COLOR1	24 bit color value for Var 1 in test pattern 6 and constant color in test pattern 7

0x051E0040 MDP_DSI_VIDEO_TEST_COL_VAR2

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_VIDEO_TEST_COL_VAR2 defines the color value for Var2. Only used when test pattern 6.is enabled

MDP_DSI_VIDEO_TEST_COL_VAR2

Bits	Name	Description
31:24	RESERVED31_12	This field has no function and should be set to zero for future compatibility
23:0	TPG_COLOR2	24 bit color value for Var 2 in test pattern 6

0x051E0044 MDP_DSI_VIDEO_UNDERFLOW_HIDING_CTL

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0006_0FFF

MDP_DSI_UNDERFLOW_HIDING_CTL register defines maximum lost pixel count value for interrupt generation, underflow hiding feature on/off and reset condition for accumulated lost pixel count value. This register is not Double Buffered and SW is requested to set this register before LCDC enabled. If SW wants to change this control register after LCDC enabled, SW should change this value as soon as VYNC interrupt occurs.

MDP_DSI_VIDEO_UNDERFLOW_HIDING_CTL

Bits	Name	Description
31:20	RESERVED31_20	This field has no function and should be set to zero for future compatibility.
19	UNDERFLOW_COLOR_SEL	Select display color during underflow situation 0x0: UNDERFLOW_COLOR (default) 0x1: Last pixel color
18	USE_ACCUM_CNT_FOR_INT	Underflow can be detected by accumulated lost pixel count or current lost pixel count. 0x0: current lost pixel count (internal asynchronous counter value debugging purpose) 0x1: accumulated lost pixel count value (default)
17	ACCUM_LOST_PIXEL_CNT_AUTO_CLR_EN	This bit defines reset condition for internal accumulated lost pixel counter. If it is disabled (set to `0'), the internal counter is not cleared by HW so SW can check how many pixels are lost over multiple frames. Accumulated lost pixel counter is reset to zero at the every vsync when this bit is `1'or at the time SW changing this bit from `0' to `1'. 0x0: disable auto clear (debugging purpose) 0x1: enable auto clear at every vsync start time (default)
16	UNDERFLOW_HIDING_EN	Underflow hiding feature on/off, if this is disabled, the underflow interrupt is generated by legacy method. 0x0: Underflow hiding feature off (legacy method, default) 0x1: Underflow hiding feature on

MDP_DSI_VIDEO_UNDERFLOW_HIDING_CTL (cont.)

Bits	Name	Description
15:12	RESERVED15_12	This field has no function and should be set to zero for future compatibility.
11:0	MAX_LOST_PIXEL_CNT	This value defines the maximum number of lost pixel, if the lost pixel counter (accumulated or current) is greater than this value, underflow interrupt is generated. Since DSI1 internal FIFO is 4 pixel based, this field is also 4-pixel based. For example, if this value is 2, the real pixel count is 8.The default value is 0xFFF.

0x051E0048 MDP_DSI_VIDEO_LOST_PIXEL_CNT_VALUE

Type: Read-Only
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

MDP_DSI_LOST_PIXEL_CNT gives accumulated lost pixel count value and current lost pixel count value.

MDP_DSI_VIDEO_LOST_PIXEL_CNT_VALUE

Bits	Name	Description
31:28	RESERVED31_28	This field has no function and should be set to zero for future compatibility.
27:16	CUR_LOST_PIXEL_CNT	This counter value indicates the internal asynchronous counter's output value which is the number of pixels lost at the moment. This value is increased in case pixels is not ready and pixel is supposed to be output to display and is decreased in case pixel data is provided by upper pipe and this lost_pixel counter value is not zero.Since DSI1 internal FIFO is 4 pixel based, this field is also 4-pixel based. For example, if this value is 2, the real pixel count is 8.
15:12	RESERVED15_12	This field has no function and should be set to zero for future compatibility.
11:0	ACCUM_LOST_PIXEL_CNT	This counter value indicates the total number of lost pixels. This counter value can be cleared at the every vsync by HW, this is normal mode operation, however it can be programmed to maintain the counter value at the vsync, this mode is mainly debugging purpose so we can check how much pixels are lost in multi-frames.Since DSI1 internal FIFO is 4 pixel based, this field is also 4-pixel based. For example, if this value is 2, the real pixel count is 8.

14.15.19 Test Bus and MISR registers

0x051F0000 MDP_TEST_MODE_CLK

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_MODE_CLK register is used to select the test points for a specified MDP block.

MDP_TEST_MODE_CLK

Bits	Name	Description
31:12	RESERVED31_12	This field has no function and should be set to zero for future compatibility.

MDP_TEST_MODE_CLK (cont.)

Bits	Name	Description
11:4	BLOCK_ID_CONTD1	0x2B: LMIX1_blend0 0x2C: LMIX1_blend1 0x2D: LMIX1_blend2 0x2E: LMIX1_blend3 0x2F: LMIX1_argclut 0x30: LMIX1_csc 0x31: LMIX1_packer0 0x32: LMIX1_packer1 0x33: LMIX1_top 0x34: DMA_P_top 0x35: DMA_P_fetch 0x36: DMA_P_cursor 0x37: DMA_P_blend 0x38: DMA_P_convert 0x39: DMA_P_lut 0x3A: DMA_P_hist 0x3B: DMA_P_dit 0x3C: DMA_P_packera 0x3D: DMA_P_packerb 0x3E: DMA_S_top 0x3F: DMA_S_dither 0x40: DMA_S_packera 0x41: DMA_S_packerb 0x42: DMA_E_top 0x43: DMA_E_fetch 0x44: DMA_E_cursor 0x45: DMA_E_blend 0x46: DMA_E_deflkr 0x47: DMA_E_packera 0x48: DMA_E_packerb 0x49: gen2axi0 (HALCYON / Reserved PHANTOM/BB) 0x4A: gen2axi1 (HALCYON / Reserved PHANTOM/BB) 0x4B: gen2axi2 (HALCYON / Reserved PHANTOM/BB) 0x4C: gen2axi3 (HALCYON / Reserved PHANTOM/BB) 0x4D: DSI_Video 2 / LCDC 0x4E: DTV 0x4F: ATV 0x50: MDDI0 0x51: MDDI1 0x52: AHBM 0x53: DSI_Video 1 0x54: DSI_CMD 1

MDP_TEST_MODE_CLK (cont.)

Bits	Name	Description
11:4	BLOCK_ID_CONTD2	0x55: mGEN2mAXI Client0 (VG1 read PHANTOM/BB) 0x56: mGEN2mAXI Client1 (VG2 read PHANTOM/BB) 0x57: mGEN2mAXI Client2 (RGB1 read PHANTOM/BB) 0x58: mGEN2mAXI Client3 (RGB2 read PHANTOM/BB) 0x59: mGEN2mAXI Client4 (DMA_P image read PHAN/BB) 0x5A: mGEN2mAXI Client5 (DMA_P cursor read PHAN/BB) 0x5B: mGEN2mAXI Client6 (DMA_S read PHAN/BB) 0x5C: mGEN2mAXI Client7 (DMA_E image read PHAN/BB) 0x5D: mGEN2mAXI Client8 (DMA_E cursor read PHAN/BB) 0x5E: mGEN2mAXI Client9 (Overlay0 write PHANTOM/BB) 0x5F: mGEN2mAXI Client10 (Overlay1 write PHANTOM/BB) 0x60: DSI_CMD 2 0x61: DMA_P_igclut 0x62: DMA_P_pcc 0x63: DMA_P_argclut 0x64: DMA_S_fetch 0x65: DMA_S_lut 0x66: DMA_S_hist 0x67: DMA_S_convert 0x68: DMA_S_igclut 0x69: DMA_S_pcc 0x6A: DMA_S_argclut 0x6B: Fixed pattern of 0x55555555 0x6C: Fixed pattern of 0xAAAAAAAA 0x6D: Fixed ID pattern of 0x68710402 0x6E: LMIX2_blend0 0x6F: LMIX2_blend1 0x70: LMIX2_blend2 0x71: LMIX2_blend3 0x72: LMIX2_argclut 0x73: LMIX2_csc 0x74: LMIX2_packer0 0x75: LMIX2_packer1 0x76: LMIX2_top 0x77: LMIX2_border_color 0x78: VG3_top

MDP_TEST_MODE_CLK (cont.)

Bits	Name	Description
11:4	BLOCK_ID	These bits select the test points for the specified MDP block into the test bus. 0x0: Disabled 0x1: Command 0x2: VG1_top 0x3: VG1_fetch 0x4: VG1_upsample 0x5: VG1_deint 0x6: VG1_hist 0x7: VG1_lut 0x8: VG1_scale 0x9: VG1_convert 0xA: VG1_dither 0xB: VG1_igclut 0xC: VG2_top 0xD: VG2_fetch 0xE: VG2_upsample 0xF: VG2_deint 0x10: VG2_hist 0x11: VG2_lut 0x12: VG2_scale 0x13: VG2_convert 0x14: VG2_dither 0x15: VG2_igclut 0x16: RGB1_top 0x17: RGB1_fetch 0x18: RGB1_scale 0x19: RGB1_igclut 0x1A: RGB2_top 0x1B: RGB2_fetch 0x1C: RGB2_scale 0x1D: RGB2_igclut 0x1E: RGB3_top 0x1F: RGB3_fetch 0x20: RGB3_scale 0x21: RGB3_igclut 0x22: LMIX0_blend0 0x23: LMIX0_blend1 0x24: LMIX0_blend2 0x25: LMIX0_blend3 0x26: LMIX0_argclut 0x27: LMIX0_csc 0x28: LMIX0_packer0 0x29: LMIX0_packer1 0x2A: LMIX0_top
3:0	TEST_PT_SEL	These bits select a set of 32-bit test points within a MDP block.

0x051F0004 MDP_TEST_MISR_RESET_CLK

Type: Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_MISR_RESET_CLK register is used to reset the MISR state.

MDP_TEST_MISR_RESET_CLK

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_SW_RESET	A write of `1' to this address will reset the MISR state. It is a self clearing reset. The reset must be asserted after MDP_TEST_MISR_MODE_CLK is set to a non-zero value. 0x1: MISR reset.

0x051F0008 MDP_TEST_EXPORT_MISR_CLK

Type: Read-Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_EXPORT_MISR_CLK register controls what is sent on the testbus. A value of `0' (reset value) will send the data that is going into the MISR on the testbus. A value of `1' will send the current MISR state onto the testbus. The latter option is typically used for debug purposes. For example, if your final MISR signature failed, you might want to know where it failed (i.e., right in the beginning or somewhere else')

MDP_TEST_EXPORT_MISR_CLK

Bits	Name	Description
31:1	RESERVED31_1	Field has no function and should be set to zero for future compatibility.
0	MISR_EXPORT	When clear(0), testbus is driven by what is sent into the MISR. (i.e., What is the result of the MUXing of all the input data streams with MDP_TEST_ MODE_CLK) When set (1), testbus is driven by the current state of the MISR (debug typically)

0x051F000C MDP_TEST_MISR_CURR_VAL_CLK

Type: Read-Only
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

A read from the address in the MDP_TEST_MISR_CURR_VAL_CLK register will return the current MISR state for this block. Keep in mind that this could change every cycle depending on how it is used.

MDP_TEST_MISR_CURR_VAL_CLK

Bits	Name	Description
31:0	MISR_VAL	It holds the current MISR state.

0x051F0100 MDP_TEST_MODE_HCLK

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_MODE_HCLK register selects the test points for the specified MDP block.

MDP_TEST_MODE_HCLK

Bits	Name	Description
31:7	RESERVED31_7	This field has no function and should be set to zero for future compatibility.
6:4	BLOCK_ID	These bits select the test points for the specified MDP block into the test bus. 0x0: Disabled 0x1: MDDI1 0x2: MDDI2 0x3: AHBM
3:0	TEST_PT_SEL	These bits select a set of 32-bit test points within a MDP block.

0x051F0104 MDP_TEST_MISR_RESET_HCLK

Type: Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_MISR_RESET_HCLK is used to reset the MISR state.

MDP_TEST_MISR_RESET_HCLK

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_SW_RESET	A write of `1' to this address will reset the MISR state. It is a self clearing reset. The reset must be asserted after MDP_TEST_MISR_MODE_HCLK is set to a non-zero value. 0x1: MISR reset.

0x051F0108 MDP_TEST_EXPORT_MISR_HCLK

Type: Read-Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_EXPORT_MISR_HCLK register controls what is sent on the testbus. A value of `0' (reset value) will send the data that is going into the MISR on the testbus. A value of `1' will send the current MISR state onto the testbus. The latter option is typically used for debug purposes. For example, if your final MISR signature failed, you might want to know where it failed (i.e., right in the beginning or somewhere else')

MDP_TEST_EXPORT_MISR_HCLK

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., What is the result of the MUXing of all the input data streams with MDP_TEST_MODE_HCLK) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x051F010C MDP_TEST_MISR_CURR_VAL_HCLK

Type: Read-Only
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

A read of the address in the MDP_TEST_MISR_CURR_VAL_HCLK register will return the current MISR state for this block. Keep in mind that this could change every cycle depending on how it is used.

MDP_TEST_MISR_CURR_VAL_HCLK

Bits	Name	Description
31:0	MISR_VAL	This field holds the current MISR state.

0x051F0200 MDP_TEST_MODE_DCLK

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_MODE_DCLK register selects the test points for the specified MDP block.

MDP_TEST_MODE_DCLK

Bits	Name	Description
31:7	RESERVED31_7	This field has no function and should be set to zero for future compatibility.
6:4	BLOCK_ID	These bits select the test points for the specified MDP block into the test bus. 0x0: Disabled 0x1: LCDC1 0x2: LCDC2 0x3: DSI_CMD
3:0	TEST_PT_SEL	These bits select a set of 32-bit test points within a MDP block.

0x051F0204 MDP_TEST_MISR_RESET_DCLK

Type: Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_MISR_RESET_DCLK is used to reset the MISR state.

MDP_TEST_MISR_RESET_DCLK

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_SW_RESET	A write of `1' to this address will reset the MISR state. It is a self clearing reset. The reset must be asserted after MDP_TEST_MISR_MODE_DCLK is set to a non-zero value. 0x1: MISR reset.

0x051F0208 MDP_TEST_EXPORT_MISR_DCLK

Type: Read-Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_EXPORT_MISR_DCLK register controls what is sent on the testbus. A value of `0' (reset value) will send the data that is going into the MISR on the testbus. A value of `1' will send the current MISR state onto the testbus. The latter option is typically used for debug purposes. For example, if your final MISR signature failed, you might want to know where it failed (i.e., right in the beginning or somewhere else')

MDP_TEST_EXPORT_MISR_DCLK

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., What is the result of the MUXing of all the input data streams with MDP_TEST_MODE_DCLK) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x051F020C MDP_TEST_MISR_CURR_VAL_DCLK

Type: Read-Only
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

A read from this address will return the current MISR state for this block. Keep in mind that this could change every cycle depending on how it is used.

MDP_TEST_MISR_CURR_VAL_DCLK

Bits	Name	Description
31:0	MISR_VAL	This field holds the current MISR state.

0x051F0210 MDP_TEST_CAPTURED_DCLK

Type: Read-Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is set to 1 by hardware when a capture strobe is sent to the MISR. If the micro reads a `1' from this register, it means that it can read the captured MISR value from

MDP_TEST_CAPT_MISR_VAL_DCLK register. The microprocessor can write a `0' or `1' into this register to clear it.

MDP_TEST_CAPTURED_DCLK

Bits	Name	Description
31:10	RESERVED31_3	This field has no function and should be set to zero for future compatibility.
9:2	MAX_FRAME_COUNT	MISR is reset when number of frames generated by video mode engine reaches this number. MISR will be updated in MISR_CAPT_VAL register before reset
1	STOP_EN	Capture every MAX_FRAME_COUNT frames or Stop after MAX_FRAME_COUNT
0	CAPTURED	Value up to MAX_FRAME_COUNT frames are captured

0x051F0214 MDP_TEST_MISR_CAPT_VAL_DCLK

Type: Read-Only
Clock: CC_MDP_CLK
Reset State: Undefined

A read from this address will return the captured MISR state for this block

MDP_TEST_MISR_CAPT_VAL_DCLK

Bits	Name	Description
31:0	MISR_VAL	This field holds the captured MISR state.

0x051F0300 MDP_TEST_MODE_TVCLK

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_MODE_TVCLK register selects the test points for the specified MDP block.

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MDP_TEST_MODE_TVCLK

Bits	Name	Description
31:7	RESERVED31_7	This field has no function and should be set to zero for future compatibility.

MDP_TEST_MODE_TVCLK (cont.)

Bits	Name	Description
6:4	BLOCK_ID	These bits select the test points for the specified MDP block into the test bus. 0x0: Disabled 0x1: ATV 0x2: DTV1 0x3: DTV2
3:0	TEST_PT_SEL	These bits select a set of 32-bit test points within a MDP block.

0x051F0304 MDP_TEST_MISR_RESET_TVCLK

Type: Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_MISR_RESET_TVCLK is used to reset the MISR state.

MDP_TEST_MISR_RESET_TVCLK

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_SW_RESET	A write of `1' to this address will reset the MISR state. It is a self clearing reset. The reset must be asserted after MDP_TEST_MISR_MODE_TVCLK is set to a non-zero value. 0x1: MISR reset.

0x051F0308 MDP_TEST_EXPORT_MISR_TVCLK

Type: Read-Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_EXPORT_MISR_TVCLK register controls what is sent on the testbus. A value of `0' (reset value) will send the data that is going into the MISR on the testbus. A value of `1' will send the current MISR state onto the testbus. The latter option is typically used for debug purposes. For example, if your final MISR signature failed, you might want to know where it failed (i.e., right in the beginning or somewhere else')

MDP_TEST_EXPORT_MISR_TVCLK

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility.

MDP_TEST_EXPORT_MISR_TVCLK (cont.)

Bits	Name	Description
0	MISR_EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., What is the result of the MUXing of all the input data streams with MDP_TEST_MODE_TVCLK) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x051F030C MDP_TEST_MISR_CURR_VAL_TVCLK

Type: Read-Only
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

A read from this address will return the current MISR state for this block. Keep in mind that this could change every cycle depending on how it is used.

MDP_TEST_MISR_CURR_VAL_TVCLK

Bits	Name	Description
31:0	MISR_VAL	This field holds the current MISR state.

0x051F0310 MDP_TEST_CAPTURED_TVCLK

Type: Read-Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is set to 1 by hardware when a capture strobe is sent to the MISR. If the micro reads a `1' from this register, it means that it can read the captured MISR value from MDP_TEST_CAPT_MISR_VAL_TVCLK register. The microprocessor can write a `0' or `1' into this register to clear it.

MDP_TEST_CAPTURED_TVCLK

Bits	Name	Description
31:10	RESERVED31_1	This field has no function and should be set to zero for future compatibility.
9:2	MAX_FRAME_COUNT	MISR is reset when number of frames generated by video mode engine reaches this number. MISR will be updated in MISR_CAPT_VAL register before reset.
1	STOP_EN	Capture every MAX_FRAME_COUNT frames or Stop after MAX_FRAME_COUNT
0	CAPTURED	Value up to MAX_FRAME_COUNT frames are captured

0x051F0314 MDP_TEST_MISR_CAPT_VAL_TVCLK

Type: Read-Only
Clock: CC_MDP_CLK
Reset State: Undefined

A read from this address will return the captured MISR state for this block

MDP_TEST_MISR_CAPT_VAL_TVCLK

Bits	Name	Description
31:0	MISR_VAL	This field holds the captured MISR state.

0x051F0400 MDP_TEST_MODE_DSI_PCLK

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_MODE_DSI_PCLK register selects the test points for the specified MDP block.

MDP_TEST_MODE_DSI_PCLK

Bits	Name	Description
31:7	RESERVED31_7	This field has no function and should be set to zero for future compatibility.
6:4	BLOCK_ID	These bits select the test points for the specified MDP block into the test bus. 0x0: Disabled 0x1: DSI_VIDEO1 0x2: DSI_VIDEO2 0x3: DSI_CMD
3:0	TEST_PT_SEL	These bits select a set of 32-bit test points within a MDP block.

0x051F0404 MDP_TEST_MISR_RESET_DSI_PCLK

Type: Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_MISR_RESET_DSI_PCLK is used to reset the MISR state.

MDP_TEST_MISR_RESET_DSI_PCLK

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_SW_RESET	A write of `1' to this address will reset the MISR state. It is a self clearing reset. The reset must be asserted after MDP_TEST_MISR_MODE_DSI_PCLK is set to a non-zero value. 0x1: MISR reset.

0x051F0408 MDP_TEST_EXPORT_MISR_DSI_PCLK

Type: Read-Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_EXPORT_MISR_DSI_PCLK register controls what is sent on the testbus. A value of `0' (reset value) will send the data that is going into the MISR on the testbus. A value of `1' will send the current MISR state onto the testbus. The latter option is typically used for debug purposes. For example, if your final MISR signature failed, you might want to know where it failed (i.e., right in the beginning or somewhere else')

MDP_TEST_EXPORT_MISR_DSI_PCLK

Bits	Name	Description
31:1	RESERVED31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., What is the result of the MUXing of all the input data streams with MDP_TEST_MODE_DSI_PCLK) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x051F040C MDP_TEST_MISR_CURR_VAL_DSI_PCLK

Type: Read-Only
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

A read from this address will return the current MISR state for this block. Keep in mind that this could change every cycle depending on how it is used.

MDP_TEST_MISR_CURR_VAL_DSI_PCLK

Bits	Name	Description
31:0	MISR_VAL	This field holds the current MISR state.

0x051F0410 MDP_TEST_CAPTURED_DSI_PCLK

Type: Read-Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

This register is set to 1 by hardware when a capture strobe is sent to the MISR. If the micro reads a `1' from this register, it means that it can read the captured MISR value from MDP_TEST_CAPT_MISR_VAL_P1CLK register. The microprocessor can write a `0' or `1' into this register to clear it.

MDP_TEST_CAPTURED_DSI_PCLK

Bits	Name	Description
31:10	RESERVED31_10	This field has no function and should be set to zero for future compatibility.
9:2	MAX_FRAME_COUNT	MISR is reset when number of frames generated by video mode engine reaches this number. MISR will be updated in MISR_CAPT_VAL register before reset
1	STOP_EN	Capture every MAX_FRAME_COUNT frames or Stop after MAX_FRAME_COUNT
0	CAPTURED	Value up to MAX_FRAME_COUNT frames are captured

0x051F0414 MDP_TEST_MISR_CAPT_VAL_DSI_PCLK

Type: Read-Only
Clock: CC_MDP_CLK
Reset State: Undefined

A read from this address will return the captured MISR state for this block

MDP_TEST_MISR_CAPT_VAL_DSI_PCLK

Bits	Name	Description
31:0	MISR_VAL	This field holds the captured MISR state.

0x051F0500 MDP_TEST_MODE_AXI_CLK

Type: Read/Write
Clock: CC_MDP_CLK
Reset State: 0x0000_0000

The MDP_TEST_MODE_AXI_CLK register selects the test points for the specified MDP block.

MDP_TEST_MODE_AXI_CLK

Bits	Name	Description
31:8	RESERVED31_8	This field has no function and should be set to zero for future compatibility.
7:4	BLOCK_ID	These bits select the test points for the specified MDP block into the test bus. 0x0: Disabled 0x1: mGEN2mAXI Client0 (VG1 read) 0x2: mGEN2mAXI Client1 (VG2 read) 0x3: mGEN2mAXI Client2 (RGB1 read) 0x4: mGEN2mAXI Client3 (RGB2 read) 0x5: mGEN2mAXI Client4 (DMA_P image read) 0x6: mGEN2mAXI Client5 (DMA_P cursor read) 0x7: mGEN2mAXI Client6 (DMA_S read) 0x8: mGEN2mAXI Client7 (DMA_E image read) 0x9: mGEN2mAXI Client8 (DMA_E cursor read) 0xA: mGEN2mAXI Client9 (Overlay0 write) 0xB: mGEN2mAXI Client10 (Overlay1 write) 0xC: mGEN2mAXI AXI Arbiter/Master 0 0xD: mGEN2mAXI AXI Arbiter/Master 1
3:0	TEST_PT_SEL	These bits select a set of 32-bit test points within a MDP block.

0x051F0600 MDP_TEST_MISR_TESTBUS_CAPT_VAL

Type: Read-Only
Clock: CC_MDP_CLK
Reset State: Undefined

A read from this address will return the captured testbus state at the output of MDP. The test_mode must be enabled (BLOCK_ID selected) for the respective clock domain. The clock domain is selected using the MDP_SEL_TEST_BUS_CLK_DOMAIN register.

Programming Notes:

This section is reserved for special programming instructions to facilitate the software development teams in programming related to the Mobile Display Processor 4.2

Sleep retention signals.

There exists a cc_lut_mdp_clk which is synchronous and balanced with cc_mdp_clk. The cc_lut_mdp_clk is used exclusively to clock LUT related SRAMs, where the related sleep retention signals are used to power down the memories when required.

It is important to note that when the cc_mdp_clk is shut down (mdp in general is not used or required in the specific use case), but MDP's island is not powered down, the cc_lut_mdp_clk should remain on and not powered down to retain the state of the LUTs.

MDP_TEST_MISR_TESTBUS_CAPT_VAL

Bits	Name	Description
31:0	MISR_VAL	This field holds the captured testbus state.

14.16 VPE Registers (0x05300000 VPE_BASE)

The Video Processing Engine (VPE) registers in this section are accessed by the ARM.

Other than the global registers (0x00000 ’ 0x0FFFF), the individual sub-block/pipe register accesses are further distinctly grouped into:

- PPP ACCESS (0x10000 ’ 0x8FFFF)
- COMMAND ACCESS (0x10000 ’ 0x1FFFF)
- TILE FETCH ACCESS (0x20000 ’ 0x2FFFF)
- DEINT ACCESS (0x30000 ’ 0x3FFFF)
- CONVERT ACCESS (0x40000 ’ 0x4FFFF)
- SCALE ACCESS (0x50000 ’ 0x5FFFF)
- ROTATE ACCESS (0x60000 ’ 0x6FFFF)
- BLEND ACCESS (0x70000 ’ 0x7FFFF)
- DITHER ACCESS (0x80000 ’ 0x8FFFF)
- DMA_P ACCESS (0x90000 ’ 0x9FFFF)
- DMA_S ACCESS (0xA0000 ’ 0xAFFFF)
- DMA_E ACCESS (0xB0000 ’ 0xBFFFF)
- TV OUT ACCESS (0xC0000 ’ 0xCFFFF)
- TEST MISR ACCESS (0xD0000 ’ 0xDFFFF)
- TEST MISR1mgen2maxi ACCESS CLK (0xD0000 ’ 0xD00FF)
- TEST MISR2 ACCESS HCLK (0xD0100 ’ 0xD01FF)
- TEST MISR3 ACCESS DCLK (0xD0200 ’ 0xD02FF)
- LCDC ACCESS (0xE0000 ’ 0xEFFFF)
- mgen2maxi Block Control (0x00400 - 0x0041F)

NOTE The VPE registers are inherited from MDP3.1 registers list. Only the PPP path is active in VPE, so other non-related registers have been removed in the RTL (all vsync, dma, tv out and lcdc are removed). To keep the software programming as similar to MDP 3.1, the registers are still listed in this document, although writes to those registers has no effect, and reads from those register will always be all 0's. Each register contains details on whether or not they are used in VPE.

14.16.1 Synchronization registers

0x05300300 VPE_SYNC_CONFIG_0

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_SYNC_CONFIG_0 register is a primary synchronization configuration register.

VPE_SYNC_CONFIG_0

Bits	Name	Description
31:21	HEIGHT	Display height - 1. It is the vertical total number of lines.
20	VSYNC_IN_EN	Setting (1) this bit will sync with the external frame sync input
19	VSYNC_COUNTER_EN	Setting (1) this bit to enable the internal counter
18:0	VSYNC_COUNT	This scale value to be programmed is the ratio of the VPE VSYNC clock frequency to LCD panel frequency divided by the no. of rows (lines) in the LCD panel. For example, if the VSYNC clock is 133 MHz and the LCD is 176 lines (rows) and 220 pixels (columns) at 60 Hz, then the value to be programmed is 133 * 10^6 / (60 * 176) = 12594 That is, it takes 12594 VPE clocks to complete writing one line in the LCD panel.

0x05300304 VPE_SYNC_CONFIG_1

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_SYNC_CONFIG_1 register is a secondary synchronization configuration register.

VPE_SYNC_CONFIG_1

Bits	Name	Description
31:21	HEIGHT	Display height - 1. It is the vertical total number of lines.
20	VSYNC_IN_EN	Setting (1) this bit will sync with external frame sync input
19	VSYNC_COUNTER_EN	Setting (1) this bit will enable the internal counter

VPE_SYNC_CONFIG_1 (cont.)

Bits	Name	Description
18:0	VSYNC_COUNT	This scale value to be programmed is the ratio of the VPE VSYNC clock frequency to LCD panel frequency divided by the no. of rows (lines) in the LCD panel. For example, if the VSYNC clock is 133 MHz and the LDC is 176 lines (rows) and 220 pixels (columns) at 60 Hz, then the value to be programmed is 133 * 10^6 / (60 * 176) = 12594 That is, it takes 12594 VPE clocks to complete writing one line in the LCD panel.

0x05300308 VPE_SYNC_CONFIG_2

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_SYNC_CONFIG_2 register is an external synchronization configuration register.

VPE_SYNC_CONFIG_2

Bits	Name	Description
31:21	HEIGHT	Display height - 1. It is the vertical total number of lines.
20	VSYNC_IN_EN	Setting (1) this bit will sync with external frame sync input
19	VSYNC_COUNTER_EN	Setting (1) this bit will enable the internal counter
18:0	VSYNC_COUNT	This scale value to be programmed is the ratio of the VPE VSYNC clock frequency to LCD panel frequency divided by the no. of rows (lines) in the LCD panel. For example, if the VSYNC clock is 133 MHz and the LDC is 176 lines (rows) and 220 pixels (columns) at 60 Hz, then the value to be programmed is 133 * 10^6 / (60 * 176) = 12594 That is, it takes 12594 VPE clocks to complete writing one line in the LCD panel.

0x0530030C VPE_SYNC_STATUS_0

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_SYNC_STATUS_0 register is a primary synchronization status register. Writing to this register loads the line counter and is equivalent to providing a software Vsync.

VPE_SYNC_STATUS_0

Bits	Name	Description
31:28	RESERVED_BITS31_28	
27:16	FRAME_COUNT	This is a free running counter that is incremented once per frame (that is, when line count resets). Writing to this register will load the counter according to the written value.
15:11	RESERVED_BITS15_11	
10:0	LINE_COUNT	This is the value of the line counter or the current read pointer of the panel mapped to primary vsync according to VPE_VSYNC_SEL. Writing to this register will load the counter according to the written value.

0x05300310 VPE_SYNC_STATUS_1

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_SYNC_STATUS_1 register is a secondary synchronization status register. Writing to this register loads the line counter and is equivalent to providing a software Vsync.

VPE_SYNC_STATUS_1

Bits	Name	Description
31:28	RESERVED_BITS31_28	
27:16	FRAME_COUNT	This is a free running counter that is incremented once per frame (that is, when line count resets). Writing to this register will load the counter according to the written value.
15:11	RESERVED_BITS15_11	
10:0	LINE_COUNT	This is the value of the line counter or the current read pointer of the panel mapped to secondary vsync according to VPE_VSYNC_SEL. Writing to this register will load the counter according to the written value.

0x05300314 VPE_SYNC_STATUS_2

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_SYNC_STATUS_2 register is an external synchronization status register. Writing to this register loads the line counter and is equivalent to providing a software Vsync.

VPE_SYNC_STATUS_2

Bits	Name	Description
31:28	RESERVED_BITS31_28	
27:16	FRAME_COUNT	This is a free running counter that is incremented once per frame (that is, when line count resets). Writing to this register will load the counter according to the written value.
15:11	RESERVED_BITS15_11	
10:0	LINE_COUNT	This is the value of the line counter or the current read pointer of the panel mapped to external vsync according to VPE_VSYNC_SEL. Writing to this register will load the counter according to the written value.

0x05300318 VPE_PRIMARY_VSYNC_OUT_CTRL

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_PRIMARY_VSYNC_OUT_CTRL register is used to configure the primary vsync output.

VPE_PRIMARY_VSYNC_OUT_CTRL

Bits	Name	Description
31	VSYNC_OUT_EN	Set (1) this bit to enable the vsync pulse Clear (0) this bit to not enable the vsync pulse If vsync pulse is enabled, the enable pin is asserted and sync output is the pulse specified. If vsync pulse is disabled, the enabled ID is de-asserted and sync output is gated to ground.

VPE_PRIMARY_VSYNC_OUT_CTRL (cont.)

Bits	Name	Description
30	VSYNC_OUT_INVERT	Set (1) this bit to invert the vsync pulse Clear (0) this bit to not invert the vsync pulse If vsync is not inverted, pulse will be active high if vsync is inverted, pulse will be active low Note: This register bit is also used to invert the incoming vsync when there is no external outgoing vsync.
29:20	RESERVED_BITS29_20	
19:0	VSYNC_OUT_WIDTH	The cycle count of the pulse width

0x0530031C VPE_SECONDARY_VSYNC_OUT_CTRL

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_SECONDARY_VSYNC_OUT_CTRL register is used to configure the secondary vsync output.

VPE_SECONDARY_VSYNC_OUT_CTRL

Bits	Name	Description
31	VSYNC_OUT_EN	Set (1) this bit to enable the vsync pulse Clear (0) this bit to not enable the vsync pulse If the vsync pulse is enabled, the enable pin is asserted and the sync output is the pulse specified. If the vsync pulse is disabled, the enabled ID is de-asserted and the sync output is gated to ground.
30	VSYNC_OUT_INVERT	Set (1) this bit to invert the vsync pulse Clear (0) this bit to not invert the vsync pulse If vsync is not inverted, the pulse will be active high If vsync is inverted, the pulse will be active low Note: This register bit is also used to invert the incoming Vsync when there is no external outgoing vsync
29:20	RESERVED_BITS29_20	
19:0	VSYNC_OUT_WIDTH	The cycle count of the pulse width

0x05300320 VPE_EXTERNAL_VSYNC_OUT_CTRL

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_EXTERNAL_VSYNC_OUT_CTRL register is used to configure the external vsync output.

VPE_EXTERNAL_VSYNC_OUT_CTRL

Bits	Name	Description
31	VSYNC_OUT_EN	Set (1) this bit to enable the vsync pulse Clear (0) this bit to not enable the vsync pulse If the vsync pulse is enabled, the enable pin is asserted and the sync output is the pulse specified. If the vsync pulse is disabled, the enabled ID is de-asserted and the sync output is gated to ground.
30	VSYNC_OUT_INVERT	Set (1) this bit to invert the vsync pulse Clear (0) this bit to not invert the vsync pulse If vsync is not inverted, the pulse will be active high If vsync is inverted, the pulse will be active low Note: This register bit is also used to invert the incoming vsync when there is no external outgoing vsync.
29:20	RESERVED_BITS29_20	
19:0	VSYNC_OUT_WIDTH	The cycle count of the pulse width

0x05300324 VPE_VSYNC_SEL

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_VSYNC_SEL register is used to select either the vsyncs from GPIOs or from MDDI block to be used internally as primary, secondary and external vsyncs.

VPE_VSYNC_SEL

Bits	Name	Description
31:6	RESERVED_BITS31_6	

VPE_VSYNC_SEL (cont.)

Bits	Name	Description
5:4	EXTERNAL_VSYNC_SEL	External vsync sel 0x0: Vsync0 from GPIO 0x1: Vsync1 from GPIO 0x2: Vsync2 from GPIO (default) 0x3: External vsync from MDDI block
3:2	SECONDARY_VSYNC_SEL	Secondary vsync sel 0x0: Vsync0 from GPIO 0x1: Vsync1 from GPIO (default) 0x2: Vsync2 from GPIO 0x3: Secondary vsync from MDDI block
1:0	PRIMARY_VSYNC_SEL	Primary vsync sel 0x0: Vsync0 from GPIO (default) 0x1: Vsync1 from GPIO 0x2: Vsync2 from GPIO 0x3: Primary vsync from MDDI block

0x05300328 VPE_PRIM_VSYNC_INIT_VAL

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_PRIM_VSYNC_INIT_VAL defines the value with which the read pointer gets loaded at primary vsync edge.

VPE_PRIM_VSYNC_INIT_VAL

Bits	Name	Description
31:11	RESERVED_BITS31_11	This field has no function and should be set to zero for future compatibility
10:0	PRIM_VSYNC_INIT_VAL	Specify the init value to which the read pointer gets loaded at vsync edge.

0x0530032C VPE_SEC_VSYNC_INIT_VAL

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_SEC_VSYNC_INIT_VAL defines the value with which the read pointer gets loaded at secondary vsync edge.

VPE_SEC_VSYNC_INIT_VAL

Bits	Name	Description
31:11	RESERVED_BITS31_11	This field has no function and should be set to zero for future compatibility
10:0	SEC_VSYNC_INIT_VAL	Specify the init value to which the read pointer gets loaded at vsync edge.

0x05300330 VPE_EXT_VSYNC_INIT_VAL

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_EXT_VSYNC_INIT_VAL defines the value with which the read pointer gets loaded at external vsync edge.

VPE_EXT_VSYNC_INIT_VAL

Bits	Name	Description
31:11	RESERVED_BITS31_11	This field has no function and should be set to zero for future compatibility
10:0	EXT_VSYNC_INIT_VAL	Specify the init value to which the read pointer gets loaded at vsync edge.

0x05300334 VPE_PRIM_VSYNC_OUT_VAL

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_PRIM_VSYNC_OUT_VAL defines the value of the internally generated read pointer at which the primary outgoing vsync is generated.

VPE_PRIM_VSYNC_OUT_VAL

Bits	Name	Description
31:11	RESERVED_BITS31_11	This field has no function and should be set to zero for future compatibility
10:0	PRIM_VSYNC_OUT_VAL	Specify the value of the read pointer at which the outgoing primary vsync is generated.

0x05300338 VPE_SEC_VSYNC_OUT_VAL

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_SEC_VSYNC_OUT_VAL defines the value of the internally generated read pointer at which the secondary outgoing vsync is generated.

VPE_SEC_VSYNC_OUT_VAL

Bits	Name	Description
31:11	RESERVED_BITS31_11	This field has no function and should be set to zero for future compatibility
10:0	SEC_VSYNC_OUT_VAL	Specify the value of the read pointer at which the secondary outgoing vsync is generated.

0x0530033C VPE_EXT_VSYNC_OUT_VAL

Type: Read/Write
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_EXT_VSYNC_OUT_VAL defines the value of the internally generated read pointer at which the external outgoing vsync is generated.

VPE_EXT_VSYNC_OUT_VAL

Bits	Name	Description
31:11	RESERVED_BITS31_11	This field has no function and should be set to zero for future compatibility

VPE_EXT_VSYNC_OUT_VAL (cont.)

Bits	Name	Description
10:0	EXT_VSYNC_OUT_VAL	Specify the value of the read pointer at which the external outgoing vsync is generated.

0x05300340 VPE_PRIM_INT_CNT_VAL

Type: Read
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_PRIM_INT_CNT_VAL register shows the internal line and frame counter for primary vsync.

VPE_PRIM_INT_CNT_VAL

Bits	Name	Description
31:28	RESERVED_BITS31_28	
27:16	FRAME_COUNT	Internal frame count value for primary vsync.
15:11	RESERVED_BITS15_11	
10:0	LINE_COUNT	Internal line count value for primary vsync.

0x05300344 VPE_SEC_INT_CNT_VAL

Type: Read
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_SEC_INT_CNT_VAL register shows the internal line and frame counter for secondary vsync.

VPE_SEC_INT_CNT_VAL

Bits	Name	Description
31:28	RESERVED_BITS31_28	
27:16	FRAME_COUNT	Internal frame count value for secondary vsync.
15:11	RESERVED_BITS15_11	

VPE_SEC_INT_CNT_VAL (cont.)

Bits	Name	Description
10:0	LINE_COUNT	Internal line count value for secondary vsync.

0x05300348 VPE_EXT_INT_CNT_VAL

Type: Read
Clock: CC_VPE_VSYNC_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_EXT_INT_CNT_VAL register shows the internal line and frame counter for external vsync.

VPE_EXT_INT_CNT_VAL

Bits	Name	Description
31:28	RESERVED_BITS31_28	
27:16	FRAME_COUNT	Internal frame count value for the external vsync.
15:11	RESERVED_BITS15_11	
10:0	LINE_COUNT	Internal line count value for the external vsync.

0x05300200 VPE_SYNC_THRESH_0

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0010_0000

This register is not used in VPE.

The VPE_SYNC_THRESH_0 register is a primary synchronization threshold register.

VPE_SYNC_THRESH_0

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:16	CONTINUE_THRESHOLD	The minimum number of lines the write pointer needs to be above the read pointer so that it is safe to write to the primary LCD. (This check is not done for the first ROI line write of an update).
15:11	RESERVED_BITS15_11	

VPE_SYNC_THRESH_0 (cont.)

Bits	Name	Description
10:0	START_THRESHOLD	Allows the first ROI line write to an primary LCD update when read pointer is between the range of ROI start line and ROI start line plus this setting.

0x05300204 VPE_SYNC_THRESH_1

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0010_0000

This register is not used in VPE.

The VPE_SYNC_THRESH_1 register is a secondary synchronization threshold register.

VPE_SYNC_THRESH_1

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:16	CONTINUE_THRESHOLD	The minimum number of lines the write pointer needs to be above the read pointer so that it is safe to write to the secondary LCD. (This check is not done for the first ROI line write of an update).
15:11	RESERVED_BITS15_11	
10:0	START_THRESHOLD	Allows the first ROI line write to an secondary LCD update when read pointer is between the range of ROI start line and ROI start line plus this setting.

0x05300208 VPE_SYNC_THRESH_2

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0010_0000

This register is not used in VPE.

The VPE_SYNC_THRESH_2 register is an external synchronization threshold register.

VPE_SYNC_THRESH_2

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:16	CONTINUE_THRESHOLD	The minimum number of lines the write pointer needs to be above the read pointer so that it is safe to write to the external LCD. (This check is not done for the first ROI line write of an update).

VPE_SYNC_THRESH_2 (cont.)

Bits	Name	Description
15:11	RESERVED_BITS15_11	
10:0	START_THRESHOLD	Allows the first ROI line write to an external LCD update when read pointer is between the range of ROI start line and ROI start line plus this setting.

0x0530020C VPE_TEAR_CHECK_EN

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_TEAR_CHECK_EN register is used to enable tearing check on different displays.

VPE_TEAR_CHECK_EN

Bits	Name	Description
2	EXTERNAL_TEAR_CHECK_EN	0x0: Disable (default) 0x1: Enable
1	SECONDARY_TEAR_CHECK_EN	0x0: Disable (default) 0x1: Enable
0	PRIMARY_TEAR_CHECK_EN	0x0: Disable (default) 0x1: Enable

0x05300210 VPE_PRIM_START_POS

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

VPE_PRIM_START_POS defines the y position value at which the kick off condition is evaluated (for the primary display).

VPE_PRIM_START_POS

Bits	Name	Description
10:0	START_POS	Specify the y position from which the start_threshold value is added and write is kicked off if the read pointer falls within that region.

0x05300214 VPE_SEC_START_POS

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

VPE_SEC_START_POS defines the y position value for the kick off condition (for the secondary display).

VPE_SEC_START_POS

Bits	Name	Description
10:0	START_POS	Specify the y position from which the start_threshold value is added and write is kicked off if the read pointer falls within that region.

0x05300218 VPE_EXT_START_POS

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

VPE_EXT_START_POS defines the y position value at which the kick off condition is evaluated (for the external display).

VPE_EXT_START_POS

Bits	Name	Description
10:0	START_POS	Specify the y position from which the start_threshold value is added and write is kicked off if the read pointer falls within that region.

0x0530021C VPE_PRIMARY_RD_PTR_IRQ

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_07FF

This register is not used in VPE.

VPE_PRIMARY_RD_PTR_IRQ defines the read pointer of the primary display at which an interrupt has to be generated.

VPE_PRIMARY_RD_PTR_IRQ

Bits	Name	Description
31:11	RESERVED_BITS31_11	This field has no function and should be set to zero for future compatibility
10:0	IRQ_LINE	Specify the read pointer value at which an interrupt has to be generated.

0x05300220 VPE_SECONDARY_RD_PTR_IRQ

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_07FF

This register is not used in VPE.

VPE_SECONDARY_RD_PTR_IRQ defines the read pointer of the secondary display at which an interrupt has to be generated.

VPE_SECONDARY_RD_PTR_IRQ

Bits	Name	Description
31:11	RESERVED_BITS31_11	This field has no function and should be set to zero for future compatibility
10:0	IRQ_LINE	Specify the read pointer value at which an interrupt has to be generated.

0x05300224 VPE_EXTERNAL_RD_PTR_IRQ

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_07FF

This register is not used in VPE.

VPE_EXTERNAL_RD_PTR_IRQ defines the read pointer of the external display at which an interrupt has to be generated.

VPE_EXTERNAL_RD_PTR_IRQ

Bits	Name	Description
31:11	RESERVED_BITS31_11	This field has no function and should be set to zero for future compatibility
10:0	IRQ_LINE	Specify the read pointer value at which an interrupt has to be generated.

14.16.2 Interrupt registers

0x05300020 VPE_INTR_ENABLE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_INTR_ENABLE register is used to enable the VPE interrupts. For VPE, only bit 0 is active, all other bits should be set to 0.

VPE_INTR_ENABLE

Bits	Name	Description
31:23	RESERVED_BITS31_23	
22:0	INTR_ENABLE	Setting (1) a specific bit will enable the respective interrupt source within the VPE to send a level interrupt out of the VPE. Clearing (0) that bit will disable it from generating the VPE interrupt. Bit0: Display list 0 ROI done Bit1: Display list 1 ROI done Bit 2 : DMA_S transfer done Bit 3 : DMA_E transfer done Bit 4 : Display list 0 PPP terminal frame done Bit 5 : Display list 1 PPP terminal frame done Bit 6 : TV out DMA transfer frame done Bit 7 : TV encoder under run Bit 8 : Sync primary line (rd_ptr) interrupt Bit 9 : Sync secondary line (rd_ptr) interrupt Bit 10 : Sync external line (rd_ptr) interrupt Bit 11 : Display list 0 fetched done Bit 12 : Display list 1 fetched done Bit 13 : TV out frame start Bit 14 : DMA_P transfer done Bit 15 : LCDC vsync (or end of frame) interrupt Bit 16 : LCDC underflow Bit 17 : DMA_P line (wr_ptr) interrupt Bit 18 : DMA_S line (wr_ptr) interrupt Bit 19 : DMA_E line (wr_ptr) interrupt Bit 20 : DMA_P histogram interrupt Bit 21 : AXI bus error Bit 22 : AXI write data timeout

0x05300024 VPE_INTR_STATUS

Type: Read
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_INTR_STATUS register is the VPE interrupt status register. For VPE, only bit 0 is active, all other bits should be ignored.

VPE_INTR_STATUS

Bits	Name	Description
31:23	RESERVED_BITS31_23	
22:0	INTR_STATUS	When an VPE interrupt occurs, then reading this register will indicate what caused the interrupt since that each bit indicates the source of the interrupt that had happened. If multiple interrupt sources had happened, then multiple bits of this register will be. Bit0: Display list 0 ROI done Bit1: Display list 1 ROI done Bit 2 : DMA_S transfer done Bit 3 : DMA_E transfer done Bit 4 : Display list 0 PPP terminal frame done Bit 5 : Display list 1 PPP terminal frame done Bit 6 : TV out DMA transfer frame done Bit 7 : TV encoder under run Bit 8 : Sync primary line (rd_ptr) interrupt Bit 9 : Sync secondary line (rd_ptr) interrupt Bit 10 : Sync external line (rd_ptr) interrupt Bit 11 : Display list 0 fetched done Bit 12 : Display list 1 fetched done Bit 13 : TV out frame start Bit 14 : DMA_P transfer done Bit 15 : LCDC vsync (or end of frame) interrupt Bit 16 : LCDC underflow Bit 17 : DMA_P line (wr_ptr) interrupt Bit 18 : DMA_S line (wr_ptr) interrupt Bit 19 : DMA_E line (wr_ptr) interrupt Bit 20 : DMA_P histogram interrupt Bit 21 : AXI bus error Bit 22 : AXI write data timeout

0x05300028 VPE_INTR_CLEAR

Type: Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_INTR_CLEAR register is used to clear the VPE interrupts. For VPE, only bit 0 is active, all other bits should be set to 0.

VPE_INTR_CLEAR

Bits	Name	Description
31:23	RESERVED_BITS31_23	
22:0	INTR_CLEAR	To clear the interrupt, make sure the interrupt has occurred, and then clear (0) this bit. Setting (1) a specific bit and holding at lest 2 clock cycles will clear the respective interrupt. A read from this register would indicate if the respective interrupt source is cleared (the bit is set (1)). So, at power up, it would read all 1's. Bit0: Display list 0 ROI done Bit1: Display list 1 ROI done Bit 2 : DMA_S transfer done Bit 3 : DMA_E transfer done Bit 4 : Display list 0 PPP terminal frame done Bit 5 : Display list 1 PPP terminal frame done Bit 6 : TV out DMA transfer frame done Bit 7 : TV encoder under run Bit 8 : Sync primary line (rd_ptr) interrupt Bit 9 : Sync secondary line (rd_ptr) interrupt Bit 10 : Sync external line (rd_ptr) interrupt Bit 11 : Display list 0 fetched done Bit 12 : Display list 1 fetched done Bit 13 : TV out frame start Bit 14 : DMA_P transfer done Bit 15 : LCDC vsync (or end of frame) interrupt Bit 16 : LCDC underflow Bit 17 : DMA_P line (wr_ptr) interrupt Bit 18 : DMA_S line (wr_ptr) interrupt Bit 19 : DMA_E line (wr_ptr) interrupt Bit 20 : DMA_P histogram interrupt Bit 21 : AXI bus error Bit 22 : AXI write data timeout

14.16.3 Operation control registers

0x05300030 VPE_PPP_DL0_START

Type: Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

A write to the VPE_PPP_DL0_START address register indicates to the VPE that there is a display list available to start processing at the VPE_PPP_DL0_ADDR pointer in command auto mode

(VPE_PPP_CMD_MODE register). In addition, a write to this register also starts PPP processing in the command direct program mode.

Note that bits 2:0 are always ignored as they are assumed to be 0.

VPE_PPP_DL0_START

Bits	Name	Description
31:0	DONT_CARE_BITS31_0	While a display list is being fetched or the PPP is still processing, any writes to this register are ignored.

0x05300034 VPE_PPP_DL1_START

Type: Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

A write to the VPE_PPP_DL1_START address register indicates to the VPE that there is a display list available to start processing at the VPE_PPP_DL1_ADDR pointer in command auto mode.

Note that bits 2:0 are always ignored as they are assumed to be 0.

VPE_PPP_DL1_START

Bits	Name	Description
31:0	DONT_CARE_BITS31_0	While a display list is being fetched or the PPP is still processing, any writes to this register are ignored.

0x05300038 VPE_DISPLAY_STATUS

Type: Read
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

The VPE_DISPLAY_STATUS register is used to indicate the VPE display status.

VPE_DISPLAY_STATUS

Bits	Name	Description
31:10	RESERVED_BITS31_10	
9	AHBM_ACTIVE	AHBM interface is active..
8	DMA_E_ACTIVE	DMA_E channel is active.

VPE_DISPLAY_STATUS (cont.)

Bits	Name	Description
7	DMA_S_ACTIVE	DMA_S channel is active.
6	DMA_P_ACTIVE	DMA_P channel is active
5	LIST1_FETCHING	Display list 1 is being fetched or pending fetching. When a display list has been fetched, this bit is cleared (0).
4	LIST0_FETCHING	Display list 0 is being fetched or pending fetching. When a display list has been fetched, this bit is cleared (0).
3	TVOUT_ACTIVE	TV out DMA channel is active.
2	RESERVED_BIT2	
1	DISPLAY1_ACTIVE	Display list 1 processing in progress. When a display list is being processed or pending processing, this bit is set (1). When a display list has completed, this bit is cleared (0).
0	DISPLAY0_ACTIVE	Display list 0 processing in progress. When a display list is being processed or pending processing, this bit is set (1). When a display list has completed, this bit is cleared (0).

0x05300044 VPE_DMA_P_START

Type: Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

The VPE_DMA_P_START register is used to start a primary DMA channel transfer.

VPE_DMA_P_START

Bits	Name	Description
31:0	DMA_P_START	A write to this register will start a DMA_P channel transfer if the output interface is not LCDC. If the output is LCDC, DMA transfer is started automatically every vsync and a write to this register has no effect.

0x05300048 VPE_DMA_S_START

Type: Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

The VPE_DMA_S_START register is used to start a secondary DMA channel transfer.

VPE_DMA_S_START

Bits	Name	Description
31:0	DMA_S_START	A write to this register will start a DMA_S channel transfer.

0x0530004C VPE_DMA_E_START

Type: Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

The VPE_DMA_E_START register is used to start a external DMA channel transfer.

VPE_DMA_E_START

Bits	Name	Description
31:0	DMA_E_START	A write to this register will start a DMA_E channel transfer.

0x05300070 VPE_HW_VERSION

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x010A_030A

The VPE_HW_VERSION register contains the major and minor versions and release number of the VPE core (p'q'_x'r', q-value is not contained).

VPE_HW_VERSION

Bits	Name	Description
31:24	MAJOR_VERSION	VPE core major version (x-value). 0x1: RESET_VAL
23:16	MINOR_VERSION	VPE core minor version (r-value). 0xA: RESET_VAL
15:8	RELEASE_PHASE	VPE core release phase (p-value). 0x3: RESET_VAL
7:0	REVISION	VPE core revision number (r-value). 0xA: RESET_VAL

0x05300074 VPE_SW_RESET

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_SW_RESET register is used to reset the individual pipes inside VPE.

VPE_SW_RESET

Bits	Name	Description
31:1	RESERVED_BITS31_1	
4	PPP_SW_RESET	Self cleared when reset sequence is completed. 0x1: PPP reset.
3	DMA_P_SW_RESET	0x1: DMA_P reset. (Only supported when DMA_P is in LCDC mode Self cleared when reset sequence is completed.)
2	DMA_S_SW_RESET	Self cleared when reset sequence is completed. 0x1: DMA_S reset. (Currently not supported)
1	DMA_E_SW_RESET	Self cleared when reset sequence is completed. 0x1: DMA_E reset. (Currently not supported)
0	DMA_TV_SW_RESET	Self cleared when reset sequence is completed. 0x1: DMA_TV reset.

0x05300078 VPE_AXI_RD_ARB_CONFIG

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0011_2924

The VPE_AXI_ARB_CONFIG register is used to change how many consecutive grants are allowed by the arbiter to each of the masters. Note that the only supported value for the weights is 4.

VPE_AXI_RD_ARB_CONFIG

Bits	Name	Description
31:21	RESERVED_BITS31_21	
20:18	MASTER7_WEIGHT	Number of consecutive grants (1 to 4) allowed to Master 7.
17:15	MASTER6_WEIGHT	Number of consecutive grants (1 to 4) allowed to Master 6.
14:12	MASTER5_WEIGHT	Number of consecutive grants (1 to 4) allowed to Master 5.
11:9	MASTER3_WEIGHT	Number of consecutive grants (1 to 4) allowed to Master 3.
8:6	MASTER2_WEIGHT	Number of consecutive grants (1 to 4) allowed to Master 2.

VPE_AXI_RD_ARB_CONFIG (cont.)

Bits	Name	Description
5:3	MASTER1_WEIGHT	Number of consecutive grant (1 to 4) allowed to Master 1.
2:0	MASTER0_WEIGHT	Number of consecutive grant (1 to 4) allowed to Master 0.

0x0530007C VPE_SEL_CLK_OR_HCLK_TEST_BUS

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_SEL_CLK_OR_HCLK_TEST_BUS register is used to select whether the VPE_TEST_BUS output is driven with selected VPE CLK or HCLK or LCDC DOT CLK domain test points.

VPE_SEL_CLK_OR_HCLK_TEST_BUS

Bits	Name	Description
31:2	RESERVED_BITS31_1	
1:0	SEL_CLKTB_OR_HCLKTB	0x0: axi_clk_domain 0x1: hclk_domain 0x2: dclk_domain

14.16.4 EBI2 registers

0x0530003C VPE_EBI2_LCD0

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

The VPE_EBI2_LCD0 register stores the base address of a primary LCD panel connected to EBI2.

VPE_EBI2_LCD0

Bits	Name	Description
31:0	BASE_ADDR	This address is assumed to be at least half-word aligned, so bit [0] is ignored.

0x05300040 VPE_EBI2_LCD1

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

The VPE_EBI2_LCD1 register stores the base address of a secondary LCD panel connected to EBI2.

VPE_EBI2_LCD1

Bits	Name	Description
31:0	BASE_ADDR	This address is assumed to be at least half-word aligned, so bit [0] is ignored.

0x05300050 VPE_EBI2_LCD0_YSTRIDE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

The VPE_EBI2_LCD0_YSTRIDE register provides the y-stride for a primary panel connected to EBI2

VPE_EBI2_LCD0_YSTRIDE

Bits	Name	Description
31:15	RESERVED_BITS31_15	
14	EBI2_YSTRIDE_EN	In memory mapped devices, if this bit is set (1) it indicates that the display size (width) is larger than the ROI width. When set, ebi2_ystride is used to write to a memory-mapped panel at EBI2_LCD0_ADDR. This bit can also be set to write to an external memory device in EBI2 space for TEST PURPOSES.
13:0	EBI2_YSTRIDE	The ystride of the LCD device attached to ebi2 interface in bytes.

0x05300054 VPE_EBI2_LCD1_YSTRIDE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

The VPE_EBI2_LCD1_YSTRIDE register provides the y-stride for a secondary panel connected to EBI2

VPE_EBI2_LCD1_YSTRIDE

Bits	Name	Description
31:15	RESERVED_BITS31_15	
14	EBI2_YSTRIDE_EN	In memory mapped devices, if this bit is set (1) it indicates that the display size (width) is larger than the ROI width. When set, ebi2_ystride is used to write to a memory-mapped panel at EBI2_LCD1_ADDR. This bit can also be set to write to an external memory device in EBI2 space for TEST PURPOSES.
13:0	EBI2_YSTRIDE	The ystride of the LCD device attached to ebi2 interface in bytes.

0x0530005C VPE_EBI2_PORTMAP_MODE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

The VPE_EBI2_PORTMAP_MODE register is the EBI2 LCD portmap mode register.

VPE_EBI2_PORTMAP_MODE

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	LCD1_PORTMAP_MODE	When this bit is set (1), it indicates that the LCD1 on EBI2 requires a portmapped write. Otherwise, the writes to EBI2 use the regular memory map one starting from the base address.
0	LCD0_PORTMAP_MODE	When this bit is set (1), it indicates that the LCD0 on EBI2 requires a portmapped write. Otherwise, the writes to EBI2 use the regular memory map one starting from the base address.

14.16.5 MDDI parameter registers

0x05300090 VPE_MDDI_PARAM_WR_SEL

Type: Write Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

The VPE_MDDI_PARAM_WR_SEL register is used to select a MDDI type for writing display parameters. It also writes CLIENTID to the selected register.

VPE_MDDI_PARAM_WR_SEL

Bits	Name	Description
31:16	MDDI_VID_CLIENTID	MDDI video client id parameter
15:2	RESERVED_BITS15_2	
1:0	MDDI_LD_PARAM_SEL	Parameter register write select: 0x0: Primary MDDI set 0x1: Secondary MDDI set 0x2: External MDDI set

0x05300094 VPE_MDDI_PARAM

Type: Write Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

The VPE_MDDI_PARAM register writes the display parameters to the MDDI type selected by VPE_MDDI_PARAM_WR_SEL

VPE_MDDI_PARAM

Bits	Name	Description
31:16	MDDI_VID_FORMAT_DESC	MDDI video format description parameter
15:0	MDDI_PIX_DATA_ATTR	MDDI pixel data attribute parameter

0x05300098 VPE_MDDI_DATA_XFR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE.

The VPE_MDDI_DATA_XFR register determines if the data would be sent out of MDDI every cycle or every alternate cycle

VPE_MDDI_DATA_XFR

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	MDDI_DATA_XFR_EXT	Note: For External MDDI 0x0: Alternate cycle data transfer (default) 0x1: Every cycle data transfer
0	MDDI_DATA_XFR_PRIM	Note: For Primary MDDI 0x0: Alternate cycle data transfer (default) 0x1: Every cycle data transfer.

14.16.6 Clock control registers

0x05300100 VPE_CGC_EN

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_FFFF

The VPE_CGC_EN register is used to enable the automatic functional clock gating mechanism inside the VPE, where the clocks are gated depending on the operation mode. Each bit is assigned to a gated clock tree. For maximum power saving, leave all bits at 1 during initialization. To force a block to have the clock on always regardless of the operation scenario, set the associated enable bit to 0.

VPE_CGC_EN

Bits	Name	Description
31:16	RESERVED_BITS31_16	
15	MDDI	Enables auto functional gating on MDDI block core clocks.
14	AHB	Enables auto functional gating on AHB_M core clock.
13	AXI	Enables auto functional gating on AXI interface clocks.
12	LCDC	Enables auto functional gating on LCDC block core clock.
11	TV_OUT	Enables auto functional gating on TV_Out clock.
10	DMA_P	Enables auto functional gating on DMA_P clock.
9	DMA_S	Enables auto functional gating on DMA_S clock.
8	DMA_E	Enables auto functional gating on DMA_E clock.
7	DOWNSAMPLE	Enables auto functional gating on PPP Downsample clock.
6	DITHER	Enables auto functional gating on PPP Dither clock.
5	BLEND	Enables auto functional gating on PPP Blend clock.

VPE_CGC_EN (cont.)

Bits	Name	Description
4	ROTATE	Enables auto functional gating on PPP Rotate clock.
3	SCALE	Enables auto functional gating on PPP Scale clock.
2	CONVERT	Enables auto functional gating on PPP Convert clock.
1	UPSAMPLE	Enables auto functional gating on PPP Upsample/Deint clock.
0	PPP	Enables auto functional gating on PPP top clock.

14.16.7 PPP registers

0x05310000 VPE_PPP_DL0_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_DL0_ADDR register points to the beginning of the display list 0.

VPE_PPP_DL0_ADDR

Bits	Name	Description
31:0	BASE_ADDR	This address is assumed to be 64-bit word aligned, so bits [2:0] are ignored.

0x05310004 VPE_PPP_DL1_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_DL1_ADDR register points to the beginning of the display list 1.

VPE_PPP_DL1_ADDR

Bits	Name	Description
31:0	BASE_ADDR	This address is assumed to be 64-bit word aligned, so bits [2:0] are ignored.

0x05310008 VPE_PPP_CMD_STATUS

Type: Read
Clock: CC_VPE_CLK
Reset State: 0x0000_3FFF

The VPE_PPP_CMD_STATUS register indicates the internal status of the VPE PPP Command block.

VPE_PPP_CMD_STATUS

Bits	Name	Description
31:14	RESERVED_BITS31_14	
13	CLKCTL_IDLE	Indicates the clock control is idle in PPP.
12	TFETCH_IDLE	Indicates the tile fetch is idle in PPP.
11	DEINT_IDLE	Indicates the de-interlace is idle in PPP.
10	UPSAMPLE_IDLE	Indicates the upsample is idle in PPP.
9	CONVERT_IDLE	Indicates the convert is idle in PPP.
8	SCALE_IDLE	Indicates the scale is idle in PPP.
7	ROTATE_IDLE	Indicates the rotate is idle in PPP.
6	BLEND_IDLE	Indicates the blend is idle in PPP.
5	DITHER_IDLE	Indicates the dither is idle in PPP.
4	DOWNSAMPLE_IDLE	Indicates the downsample is idle in PPP.
3	PACKER_IDLE	Indicates the packer is idle in PPP.
2	DMA_WR_IDLE	Indicates the dma_wr is idle in PPP.
1	DMA_RD_IDLE	Indicates the dma_rd is idle in PPP.
0	DECODE_READY	When this bit is set (1), the command is done decoding.

0x05310010 VPE_PPP_PROFILE_EN

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_PROFILE_EN

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	EN	Enable the ROI cycle counter for profiling

0x05310014 VPE_PPP_PROFILE_COUNT

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_PROFILE_COUNT

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	TOTAL_CYCLE	Total cycle count in a ROI, from new ROI to last pixel out of Packer (PPP goes back to Idle)

0x05310060 VPE_PPP_CMD_MODE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0001

The VPE_PPP_CMD_MODE register is the VPE command list fetch mode register. When in the direct program mode, the peripheral bus interface is used to program all of the PPP registers directly. Writing to the PPP_DL0_START register in this case after all the control is set, starts the ROI processing.

When in the auto mode, the VPE PPP Command block will fetch the display list from the addresses in VPE_PPP_DLn_ADDR, after a respective VPE_PPP_DLn_START register write.

VPE_PPP_CMD_MODE

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	MODE_BIT	0x0: AUTO 0x1: DIRECT PROGRAM

0x05310064 VPE_PPP_DL0_SIZE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_DL0_SIZE register specifies the number of register writes that Display List 0 image has, which is the size to be fetched.

VPE_PPP_DL0_SIZE

Bits	Name	Description
31:16	RESERVED_BITS31_16	
15:0	REG_COUNT	Total number of register writes in the Display List, coincide with number of 64-bit words in the image.

0x05310068 VPE_PPP_DL1_SIZE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_DL1_SIZE register specifies the number of register writes that Display List 1 image has, which is the size to be fetched.

VPE_PPP_DL1_SIZE

Bits	Name	Description
31:16	RESERVED_BITS31_16	
15:0	REG_COUNT	Total number of register writes in the Display List, coincide with number of 64-bit words in the image.

0x05310108 VPE_PPP_SRC_SIZE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0020_0020

VPE_PPP_SRC_SIZE

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_H	Height of input ROI image that needs to be fetched in pixel, including any amount of over-fetching/under-fetching necessary.
15:13	RESERVED_BITS15_13	
12:0	SRC_W	Width of input ROI image that needs to be fetched in pixel, including any amount of over-fetching/under-fetching necessary.

0x0531010C VPE_PPP_SRCP0_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_SRCP0_ADDR

Bits	Name	Description
31:0	SRCP0_ADDR	Base byte address of the Image's single interleave color plane or the luma component plane in pseudo-planar format.

0x05310110 VPE_PPP_SRCP1_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_SRCP1_ADDR

Bits	Name	Description
31:0	SRCP1_ADDR	Base byte address of the Image's chroma plane in pseudo planar format.

0x05310118 VPE_PPP_SRCP3_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_SRCP3_ADDR

Bits	Name	Description
31:0	SRCP3_ADDR	Base byte address of the Image's component plane 3 (alpha), used in pseudo planar + alpha format.

0x0531011C VPE_PPP_SRC_YSTRIDE1

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0080

VPE_PPP_SRC_YSTRIDE1

Bits	Name	Description
31	RESERVED_BIT31	
30:16	SRCP1_YSTRIDE	Plane 1 y stride in bytes.
15	RESERVED_BIT15	
14:0	SRCP0_YSTRIDE	Plane 0 y stride in bytes.

0x05310120 VPE_PPP_SRC_YSTRIDE2

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_SRC_YSTRIDE2

Bits	Name	Description
31	RESERVED_BIT31	
30:16	SRCP3_YSTRIDE	Plane 3 y stride in bytes.
15:0	RESERVED_BITS15_0	

0x05310124 VPE_PPP_SRC_FORMAT

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0002_67FF

VPE_PPP_SRC_FORMAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21	WMV9_MODE	0x1: WMV9 mode on
20:19	FETCH_PLANES	Determines the number of planes to fetch: 0x0: Interleaved 0x2: pseudo planar
18	UNPACK_ALIGN	0x0: To LSB 0x1: To MSB
17	UNPACK_TIGHT	0x0: Loose 0x1: Tight

VPE_PPP_SRC_FORMAT (cont.)

Bits	Name	Description
16:13	UNPACK_COUNT	Valid unpacking pattern count: 0 = 1 component, 1 = 2 components, ..., 15 = 16 components. Unpacking pattern only applies to the interleaved plane (chroma plane in pseudo-planar).
12:11	RESERVED_BITS12_11	Reserved for backward compatibility.
10:9	SRC_BPP	Effective source byte per pixel: 0 = 1 byte, 1 = 2 bytes, 2 = 3 bytes, 3 = 4 bytes. This is only used when unpacking the interleaved plane.
8	SRCC3_EN	0x1: Source has alpha
7:6	SRCC3_BITS	Number of bits for component 3 (alpha) input, this is not used for dither: 0 = 1 bit, 1 = 4 bits, 2 = 6 bits, 3 = 8 bits.
5:4	SRCC2_BITS	Number of bits for component 2 (R / Cr) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	SRCC1_BITS	Number of bits for component 1 (B / Cb) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	SRCC0_BITS	Number of bits for component 0 (G / luma) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x05310128 VPE_PPP_SRC_UNPACK_PATTERN1

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0302_0001

VPE_PPP_SRC_UNPACK_PATTERN1

Bits	Name	Description
31:0	UNPACK_PATTERN31_0	Unpacking pattern, maximum of 8 pattern elements starting from LSB to MSB. Run length portion of the pattern is not supported, thus most significant 6 bits of each byte unused, and returns 0.

0x0531012C VPE_PPP_SRC_UNPACK_PATTERN2

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_SRC_UNPACK_PATTERN2

Bits	Name	Description
31:0	UNPACK_PATTERN63_32	Unpacking pattern, maximum of 8 pattern elements starting from LSB to MSB. Run length portion of the pattern is not supported, thus most significant 6 bits of each byte unused, and returns 0.

0x05310138 VPE_PPP_OP_MODE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_OP_MODE

Bits	Name	Description
31	RESERVED_BIT31	
30	DST_DATA_FORMAT	0x0: RGB 0x1: YCbCr
29	DEINT_ODD_REF	De-interlace uses Odd field as Reference when set.
28	DEINT_EN	De-interlace enable
27	BG_CHROMA_SITE	Background tile chroma siting. 1= offsite, 0 = cosite.
26:25	BG_CHROMA_SAMP	Background tile chroma sampling: 0x0: 4:4:4/RGB 0x1: H2V1 0x2: H1V2 0x3: 4:2:0.
24	BLEND_TRANSP_EN	Transparency check enable: 0x0: Off (Output is according to blend_alpha_sel/blend_eq_sel combo) 0x1: On (Color keying is done on the foreground layer selected by blend_eq_sel, and blended result specified is passed if non-matching.)
23	DST_CHROMA_SITE	Destination chroma siting. 1 = offsite, 0 = cosite.
22:21	DST_CHROMA_SAMP	Destination chroma sampling: 0x0: 4:4:4/RGB 0x1: H2V1 0x2: H1V2 0x3: 4:2:0.
20	SRC_CHROMA_SITE	Source chroma siting. 1 = offsite, 0 = cosite.
19:18	SRC_CHROMA_SAMP	Source chroma sampling: 0x0: 4:4:4/RGB 0x1: H2V1 0x2: H1V2 0x3: 4:2:0.
17	RESERVED_BIT17	Reserved for backward compatibility
16	DITHER_EN	Dither enable.

VPE_PPP_OP_MODE (cont.)

Bits	Name	Description
15	BLEND_EQ_SEL	Blend equation select: 0x0: normal (same as indicating layer0/fg fetch is the foreground in the blend equation) 0x1: reverse alpha (1-alpha is applied to layer0, same as indicating layer1/bg fetch is the foreground in the blend equation)
14:13	BLEND_ALPHA_SEL	Blending alpha select: 0x0: fg per pixel alpha blend (layer0 alpha) 0x1: bg per pixel alpha blend (layer1 alpha) 0x2: constant alpha blend
12	BLEND_EN	Blending is on. When this bit is set (1), the source tile is fetched first followed by the background tile and subsequently alternating between the two.
11:9	ROT_MODE	Rotation mode: Bit 0: Rotate 90 degrees Bit 1: Left/right flip Bit 2: Up/down flip.
8	ROT_EN	Rotate buffer enable. This must be set (1) when blend is enabled also. When this bit is set (1), the mid-PPP ping-pong tile buffer is always used independent of the rotation mode.
7	LUT_C2_EN	Component 2 LUT enable.
6	LUT_C1_EN	Component 1 LUT enable.
5	LUT_C0_EN	Component 0 LUT enable.
4	CONVERT_MATRIX_SEL	Selects which matrix to use during processing 0x0: Primary matrix 0x1: Secondary matrix.
3	CONVERT_MATRIX_EN	Enable color convert. This enables the matrix conversion in the convert block only.
2	SRC_DATA_FORMAT	0x0: RGB 0x1: YCbCr
1	SCALEY_EN	Y scaling enable
0	SCALEX_EN	X scaling enable

0x0531013C VPE_PPP_SCALE_PHASEX_INIT

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_SCALE_PHASEX_INIT

Bits	Name	Description
31:0	PHASEX_INIT	Initial phase accumulator value for x scale (Q29). This is set to 0 normally, unless performing anamorphic scaling of the same source image or scale down to 1 pixel.

0x05310140 VPE_PPP_SCALE_PHASEY_INIT

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_SCALE_PHASEY_INIT

Bits	Name	Description
31:0	PHASEY_INIT	Initial phase accumulator value for y scale (Q29). This is set to 0 normally, unless performing anamorphic scaling of the same source image or scale down to 1 pixel.

0x05310144 VPE_PPP_SCALE_PHASEX_STEP

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_SCALE_PHASEX_STEP

Bits	Name	Description
31:0	PHASEX_STEP	X phase step which is input width/output width in u3.29, phase step of 8 (1/8 scale) is encoded by setting this value to 0 (representing 0x1_0000_0000). For scaling ratio >1/4 using polyphase scaler, this is ((input size -1) / (output size -1))<<29 and round. For scaling ratio <=1/4, please use M/N scaler and set this to (input size / output size)<<29.

0x05310148 VPE_PPP_SCALE_PHASEY_STEP

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_SCALE_PHASEY_STEP

Bits	Name	Description
31:0	PHASEY_STEP	X phase step which is input width/output width in u3.29, phase step of 8 (1/8 scale) is encoded by setting this value to 0 (representing 0x1_0000_0000). For scaling ratio >1/4 using polyphase scaler, this is ((input size -1) / (output size -1))<<29 and round. For scaling ratio <=1/4, please use M/N scaler and set this to (input size / output size)<<29.

0x0531014C VPE_PPP_BLEND_PARAM

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BLEND_PARAM

Bits	Name	Description
31:24	CONSTANT_ALPHA	Constant alpha value.
23:0	TRANSPARENT_COLOR	Transparent color to be masked if in this mode (C2,C1,C0 each 8 bits from MSB to LSB).

0x05310150 VPE_PPP_OUT_FORMAT

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0003_27FF

VPE_PPP_OUT_FORMAT

Bits	Name	Description
31:23	RESERVED_BITS31_23	
22:21	COMP_MODE	Compression mode. Output is written out in 4x4 compressed tile format when compression is enabled. If lossy compression is done, the pixel size could be further reduced by 3-bit at a cost of picture quality degradation. When doing lossy compression, either rounding or truncation is supported. 0x0: Lossless compression (Default) 0x1: Lossy with rounding 0x2: Lossy with truncation 0x3: Undefined
20	COMP_EN	Compression enable. 0x0: Disable (Default) 0x1: Enable

VPE_PPP_OUT_FORMAT (cont.)

Bits	Name	Description
19:18	WRITE_PLANES	It determines the number of planes to write: 0x0: Interleaved 0x2: pseudo planar
17:16	PPP_DST_BPP	Effective destination byte per pixel: 0 = 1 byte, 1 = 2 bytes, 2 = 3 bytes, 3 = 4 bytes. This is only useful when estimating ROI line width for the interleaved plane (chroma plane in pseudo-planar)
15	RESERVED_BIT15	Processing pipe output device select no longer supported, fixed to AXI.
14	PPP_PACK_ALIGN	0x0: To LSB 0x1: To MSB
13	PPP_PACK_TIGHT	0x0: Loose 0x1: Tight
12:9	PPP_PACK_COUNT	Valid packing elements count: 0 = 1 element, 1 = 2 elements, ..., 15 = 16 elements. Packing pattern only applies to the interleaved planes (chroma plane in pseudo-planar) and going to MDDI or AXI write only.
8	PPP_DSTC3_EN	0x1: Destination has alpha.
7:6	PPP_DSTC3_BITS	Number of bits for component 3 (alpha) output, this is not used for dither: 0 = 1 bit, 1 = 4 bits, 2 = 6 bits, 3 = 8 bits.
5:4	PPP_DSTC2_BITS	Number of bits for component 2 (R / Cr) output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	PPP_DSTC1_BITS	Number of bits for component 1 (B / Cb) output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	PPP_DSTC0_BITS	Number of bits for component 0 (G / luma) output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x05310154 VPE_PPP_OUT_PACK_PATTERN1

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0302_0001

VPE_PPP_OUT_PACK_PATTERN1

Bits	Name	Description
31:0	PPP_PACK_PATTERN31_0	Packing pattern, maximum of 8 pattern elements starting from LSB to MSB. Run length portion of the pattern is not supported, thus most significant 6 bits of each byte unused, and returns 0. The packing pattern should be set to the intermediate frame buffer format when going to it, for example, for LCD display RGB888 and 4:2:2 interleaved cosite for TV out display.

0x05310158 VPE_PPP_OUT_PACK_PATTERN2

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_OUT_PACK_PATTERN2

Bits	Name	Description
31:0	PPP_PACK_PATTERN63_32	Packing pattern, maximum of 8 pattern elements starting from LSB to MSB. Run length portion of the pattern is not supported, thus most significant 6 bits of each byte unused, and returns 0.

0x05310164 VPE_PPP_OUT_SIZE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0020_0020

The output width has to be a multiple of 16. Although the PPP logic supports output sizes that's not multiple of 16 pixels, we've mainly tested for output size that is multiple of 16 bytes. So, the DST_W should be a multiple of 16.

VPE_PPP_OUT_SIZE

Bits	Name	Description
31:28	RESERVED_BITS31_28	
27:16	DST_H	Output ROI height (pixel).
15:12	RESERVED_BITS15_12	
11:0	DST_W	Output ROI width (pixel).

0x05310168 VPE_PPP_OUTP0_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_OUTP0_ADDR

Bits	Name	Description
31:0	DSTP0_ADDR	Base byte address of the output Image's single interleave color plane or luma component plane for pseudo planar format.

0x0531016C VPE_PPP_OUTP1_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_OUTP1_ADDR

Bits	Name	Description
31:0	DSTP1_ADDR	Base byte address of the Image's chroma component plane for pseudo planar format.

0x05310174 VPE_PPP_OUTP3_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_OUTP3_ADDR

Bits	Name	Description
31:0	DSTP3_ADDR	Base byte address of the Image's component plane 3, used only in pseudo planar+alpha format.

0x05310178 VPE_PPP_OUT_YSTRIDE1

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0080

VPE_PPP_OUT_YSTRIDE1

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:16	DSTP1_YSTRIDE	Plane 1 y stride in bytes.
15:14	RESERVED_BITS15_14	
13:0	DSTP0_YSTRIDE	Plane 0 y stride in bytes.

0x0531017C VPE_PPP_OUT_YSTRIDE2

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_OUT_YSTRIDE2

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:16	DSTP3_YSTRIDE	Plane 3 y stride in bytes.
15:0	RESERVED_BITS15_0	

0x0531019C VPE_PPP_OUT_XY

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_OUT_XY

Bits	Name	Description
31:28	RESERVED_BITS31_28	
27:16	DST_Y	Output ROI origin y coordinate (pixel) in the output image.
15:12	RESERVED_BITS15_12	
11:0	DST_X	Output ROI origin x coordinate (pixel) in the output image.

0x053101C0 VPE_PPP_BGP0_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BGP0_ADDR

Bits	Name	Description
31:0	BGP0_ADDR	Base byte address of the BG Image's single interleave color plane or the luma component plane in pseudo-planar format.

0x053101C4 VPE_PPP_BGP1_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BGP1_ADDR

Bits	Name	Description
31:0	BGP1_ADDR	Base byte address of the BG Image's chroma plane in pseudo planar format.

0x053101C8 VPE_PPP_BGP3_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BGP3_ADDR

Bits	Name	Description
31:0	BGP3_ADDR	Base byte address of the BG Image's component plane 3 (alpha), used in pseudo planar + alpha format.

0x053101CC VPE_PPP_BG_YSTRIDE1

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0080

VPE_PPP_BG_YSTRIDE1

Bits	Name	Description
31:30	RESERVED_BITS31_30	
29:16	BGP1_YSTRIDE	Background plane 1 y stride in bytes.
15:14	RESERVED_BITS15_14	
13:0	BGP0_YSTRIDE	Background plane 0 y stride in bytes.

0x053101D0 VPE_PPP_BG_YSTRIDE2

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BG_YSTRIDE2

Bits	Name	Description
31:30	RESERVED_BITS31_30	

VPE_PPP_BG_YSTRIDE2 (cont.)

Bits	Name	Description
29:16	BGP3_YSTRIDE	Background plane 3 y stride in bytes.
15:0	RESERVED_BITS15_0	

0x053101D4 VPE_PPP_BG_FORMAT

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0002_67FF

VPE_PPP_BG_FORMAT

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:24	DECOMP_MODE	Decompression mode. Background is in 4x4 compressed tile format when decompression is enabled. If lossy compression was done, the pixel size was reduced by 3-bit at a cost of picture quality degradation. When doing decompression for a lossy input, either bit promotion or just shifting is supported.) 0x0: Lossless 0x1: Lossy by rounding 0x2: Lossy by truncation 0x3: Undefined
23	DECOMP_EN	Decompression enable. 0x0: Disable (Default) 0x1: Enable
22	BG_NOT_ROTATE	Set (1) this bit to indicate that the background fetch order will remain the same as foreground regardless of the rotate mode at the output of PPP (in ROI2 operations). Normally (when this is 0 by default), as in blending on an intermediate buffer background, the fetching tile order will vary depending on the rot_mode setting in 0x10138.
21	BG_WMV9_MODE	WMV9 mode 0x1: on 0x0: off
20:19	BG_FETCH_PLANES	Determines the number of planes for background fetch: 0x0: Interleaved 0x2: pseudo planar
18	BG_UNPACK_ALIGN	0x0: To LSB 0x1: To MSB
17	BG_UNPACK_TIGHT	0x0: Loose 0x1: Tight

VPE_PPP_BG_FORMAT (cont.)

Bits	Name	Description
16:13	BG_UNPACK_COUNT	Valid unpacking pattern count: 0 = 1 component, 1 = 2 components, ..., 15 = 16 components. Unpacking pattern only applies to the interleaved plane (chroma plane in pseudo planar).
12:11	RESERVED_BITS12_11	
10:9	BG_BPP	Effective background byte per pixel: 0 = 1 byte, 1 = 2 bytes, 2 = 3 bytes, 3 = 4 bytes. This is only used when unpacking the interleaved plane.
8	BGC3_EN	0x1: background has alpha
7:6	BGC3_BITS	Number of bits for component 3 (alpha) input, this is not used for dither: 0 = 1 bit, 1 = 4 bits, 2 = 6 bits, 3 = 8 bits.
5:4	BGC2_BITS	Number of bits for component 2 (R / Cr) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
3:2	BGC1_BITS	Number of bits for component 1 (B / Cb) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.
1:0	BGC0_BITS	Number of bits for component 0 (G / luma) input: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits.

0x053101D8 VPE_PPP_BG_UNPACK_PATTERN1

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0302_0001

VPE_PPP_BG_UNPACK_PATTERN1

Bits	Name	Description
31:0	BG_UNPACK_PATTERN31_0	Unpacking pattern, maximum of 16 pattern elements starting from LSB to MSB. Run length portion of the pattern is not supported, thus most significant 6 bits of each byte unused, and returns 0.

0x053101DC VPE_PPP_BG_UNPACK_PATTERN2

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BG_UNPACK_PATTERN2

Bits	Name	Description
31:0	BG_UNPACK_PATTERN63_32	Unpacking pattern, maximum of 16 pattern elements starting from LSB to MSB. Run length portion of the pattern is not supported, thus most significant 6 bits of each byte unused, and returns 0.

0x05310200 VPE_PPP_SRC_XY

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_SRC_XY

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:16	SRC_Y	Source ROI origin screen Y coordinate (pixel) in the source image (i.e., Y offset of source ROI in the source image).
15:13	RESERVED_BITS15_13	
12:0	SRC_X	Source ROI origin screen X coordinate (pixel) in the source image (i.e., X offset of source ROI in the source image).

0x05310204 VPE_PPP_BG_XY

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BG_XY

Bits	Name	Description
31:28	RESERVED_BITS31_28	
27:16	BG_Y	Background ROI origin screen Y coordinate (pixel) in the background image (i.e., Y offset of background ROI in the background image).
15:12	RESERVED_BITS15_12	
11:0	BG_X	Background ROI origin screen X coordinate (pixel) in the background image (i.e., X offset of background ROI in the background image).

0x05310208 VPE_PPP_SRC_IMAGE_SIZE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0020_0020

VPE_PPP_SRC_IMAGE_SIZE

Bits	Name	Description
31:29	RESERVED_BITS31_29	

VPE_PPP_SRC_IMAGE_SIZE (cont.)

Bits	Name	Description
28:16	SRC_IMG_H	Source image height (to determine if lines should be over-fetched or repeated).
15:13	RESERVED_BITS15_13	
12:0	SRC_IMG_W	Source image width (to determine if pixels should be over-fetched or repeated).

0x0531020C VPE_PPP_BG_IMAGE_SIZE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0020_0020

VPE_PPP_BG_IMAGE_SIZE

Bits	Name	Description
31:28	RESERVED_BITS31_28	
27:16	BG_IMG_H	Background image height (to determine if lines should be over-fetched or repeated).
15:12	RESERVED_BITS15_12	
11:0	BG_IMG_W	Background image width (to determine if pixels should be over-fetched or repeated).

0x05310210 VPE_PPP_BG_HDR_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BG_HDR_ADDR

Bits	Name	Description
31:0	BG_HDR_ADDR	Byte address of the header for the first 4x4 compressed tile in the background image. First 4x4 compressed tile is located at X=0, Y=0 pixel coordinate.

0x05310214 VPE_PPP_BG_HDR_YSTRIDE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BG_HDR_YSTRIDE

Bits	Name	Description
31:14	RESERVED_BITS31_14	
13:0	BG_HDR_YSTRIDE	Ystride in bytes for headers of the 4x4 compressed tiles in the background image.

0x05310220 VPE_PPP_DST_HDR_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_DST_HDR_ADDR

Bits	Name	Description
31:0	DST_HDR_ADDR	Byte address of the header for the first 4x4 compressed tile in the destination image. First 4x4 compressed tile is located at X=0, Y=0 pixel coordinate.

0x05310224 VPE_PPP_DST_HDR_YSTRIDE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_DST_HDR_YSTRIDE

Bits	Name	Description
31:14	RESERVED_BITS31_14	
13:0	DST_HDR_YSTRIDE	Ystride in bytes for headers of the 4x4 compressed tiles in the destination image.

0x05310230 VPE_PPP_SCALE_CONFIG

Type: Read/Write
Clock: VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_SCALE_CONFIG register selects additional scale parameters.

VPE_PPP_SCALE_CONFIG

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8	PIX_REPEAT_MODE	Put scaler in Pixel Repeat scaling mode, make sure both scale unit selects are in polyphase when this is on. 0x0: Off 0x1: On
7	SHARPEN_EN	Sharpening enable in polyphase scaling 0x0: Off 0x1: On
6	SVI_EN	Enable SVI on green/luma channel in polyphase scaling 0x0: Off 0x1: On
5:4	Y_TABLE	Scale Y coefficient set for polyphase scaler: 0x0: D0 Set 0x1: D1 Set 0x2: D2 Set 0x3: U1 Set
3:2	X_TABLE	Scale X coefficient set for polyphase scaler: 0x0: D0 Set 0x1: D1 Set 0x2: D2 Set 0x3: U1 Set
1	SCALEY_UNIT_SEL	Select Polyphase FIR or M/N filter for X scaler. M/N should be used at low-end of down scaling (between 1/8 and 1/4) 0x0: Polyphase 0x1: M/N phase-controlled
0	SCALEX_UNIT_SEL	Select Polyphase FIR or M/N filter for Y scaler. M/N should be used at low-end of down scaling (between 1/8 and 1/4) 0x0: Polyphase 0x1: M/N phase-controlled

0x05310240 VPE_PPP_CSC_CONFIG

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_CSC_CONFIG register defines the color and gamma correct parameters.

VPE_PPP_CSC_CONFIG

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5	LUT_SEL	Selects which LUT to use during processing 0x0: Set1 0x1: Set2
4	POST_LIMIT_SEL	Selects which post-limit (i.e., post-clamp) to use during processing 0x0: Set1 0x1: Set2
3	PRE_LIMIT_SEL	Selects which pre-limit (i.e., pre-clamp) to use during processing 0x0: Set1 0x1: Set2
2	POST_BIAS_SEL	Selects which post-bias to use during processing 0x0: Set1 0x1: Set2
1	PRE_BIAS_SEL	Selects which pre-bias to use during processing 0x0: Set1 0x1: Set2
0	LUT_POSITION	Specifies the position of LUT/Gamma table 0x0: Pre-LUT (before matrix convert) 0x1: Post-LUT (after matrix convert)

0x05310250 VPE_PPP_BLEND_PARAM2

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BLEND_PARAM2

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	TRANSPARENCY_MASK	Transparency check bit mask, setting a bit to 1 means the corresponding bit in the transparent color setting is ignored when doing color keying. (c2 c1 c0 each 8 bits from MSB to LSB)

0x05320004 VPE_PPP_TFETCH_TEST_MODE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_TFETCH_TEST_MODE

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	TFETCH_SOLID_FILL	This takes precedence over tfetch_unpack_bypass. If this bit is set (1), the output color is forced to the value written into register 0x20040.This is useful in filling a ROI with a constant color.
0	TFETCH_UNPACK_BYPASS	Setting (1)this bit enables a bypass in the unpacker. Therefore, each data read would be treated as color0, color1, color2, and color3 from lower byte to upper byte.

0x05320008 VPE_PPP_TFETCH_STATUS

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_00FF

VPE_PPP_TFETCH_STATUS

Bits	Name	Description
31:12	RESERVED_BITS31_12	
11:8	FIFO_ERRORS	TileFetch internal FIFO errors. These error bits are pulse catching, and returned to zero when this register is read: Bit 11 = control FIFO error Bit 10 = burstbuf FIFO error Bit 9= line_gen luma FIFO error Bit 8= line_gen chroma FIFO error
7:5	IDLES2	TileFetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 7= conv idle Bit 6= decomp idle Bit 5= lbufs idle
4:0	IDLES	TileFetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 4= dma_rd idle Bit 3= ctl idle Bit 2= burstbuf idle Bit 1= unpack idle Bit 0= line_gen idle

0x05320010 VPE_PPP_TFETCH_TILE_COUNT

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_TFETCH_TILE_COUNT

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:16	NUM_CHROMA_TILE	Number of chroma tiles in an ROI
15:11	RESERVED_BITS15_11	
10:0	NUM_LUMA_TILE	Number of luma/RGB tiles in an ROI

0x05320014 VPE_PPP_TFETCH_FETCH_COUNT

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_TFETCH_FETCH_COUNT

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	P1_FETCH_COUNT	Plane 1 fetch count in an ROI
15	RESERVED_BIT15	
14:0	P0_FETCH_COUNT	Plane 0 fetch count in an ROI

0x05320040 VPE_PPP_TFETCH_CONSTANT_COLOR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0xFFFF_FFFF

VPE_PPP_TFETCH_CONSTANT_COLOR

Bits	Name	Description
31:24	FORCED_COLOR3	Constant color driven for color3 during color force mode.
23:16	FORCED_COLOR2	Constant color driven for color2 during color force mode.
15:8	FORCED_COLOR1	Constant color driven for color1 during color force mode.
7:0	FORCED_COLOR0	Constant color driven for color0 during color force mode.

0x05328004 VPE_PPP_BGTFETCH_TEST_MODE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BGTFETCH_TEST_MODE

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	TFETCH_SOLID_FILL	This takes precedence over tfetch_unpack_bypass. If this bit is set (1), the output color is forced to the value written into register 0x20040.This is useful in filling a ROI with a constant color.
0	TFETCH_UNPACK_BYPASS	Setting (1)this bit enables a bypass in the unpacker. Therefore, each data read would be treated as color0, color1, color2, and color3 from lower byte to upper byte.

0x05328008 VPE_PPP_BGTFETCH_STATUS

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_00FF

VPE_PPP_BGTFETCH_STATUS

Bits	Name	Description
31:12	RESERVED_BITS31_12	
11:8	FIFO_ERRORS	TileFetch internal FIFO errors. These error bits are pulse catching, and returned to zero when this register is read: Bit 11 = control FIFO error Bit 10 = burstbuf FIFO error Bit 9= line_gen luma FIFO error Bit 8= line_gen chroma FIFO error
7:5	IDLES2	TileFetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 7= conv idle Bit 6= decomp idle Bit 5= lbufs idle
4:0	IDLES	TileFetch internal sub-block idle state. Idle means no internal pending data for processing: Bit 4= dma_rd idle Bit 3= ctl idle Bit 2= burstbuf idle Bit 1= unpack idle Bit 0= line_gen idle

0x05328010 VPE_PPP_BGTFETCH_TILE_COUNT

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BGTFETCH_TILE_COUNT

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:16	NUM_CHROMA_TILE	Number of chroma tiles in an ROI
15:11	RESERVED_BITS15_11	
10:0	NUM_LUMA_TILE	Number of luma/RGB tiles in an ROI

0x05328014 VPE_PPP_BGTFETCH_FETCH_COUNT

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BGTFETCH_FETCH_COUNT

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	P1_FETCH_COUNT	Plane 1 fetch count in an ROI
15	RESERVED_BIT15	
14:0	P0_FETCH_COUNT	Plane 0 fetch count in an ROI

0x05328040 VPE_PPP_BGTFETCH_CONSTANT_COLOR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0xFFFF_FFFF

VPE_PPP_BGTFETCH_CONSTANT_COLOR

Bits	Name	Description
31:24	FORCED_COLOR3	Constant color driven for color3 during color force mode.
23:16	FORCED_COLOR2	Constant color driven for color2 during color force mode.
15:8	FORCED_COLOR1	Constant color driven for color1 during color force mode.
7:0	FORCED_COLOR0	Constant color driven for color0 during color force mode.

0x05330000 VPE_PPP_DEINT_STATUS

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_000F

VPE_PPP_DEINT_STATUS

Bits	Name	Description
31:4	RESERVED_BITS31_4	
3:0	IDLES	Internal idles

0x05330004 VPE_PPP_DEINT_DECISION

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0003_0032

VPE_PPP_DEINT_DECISION

Bits	Name	Description
31:20	RESERVED_BITS31_20	
18:16	ATTENU	Attenuation (the shift value) for less temporal resolution; valid range is 0
15:11	RESERVED_BITS15_11	
10:0	THRESH	Threshold (u11) for De-interlace attenuation decision

0x05330010+ 4*n VPE_PPP_DEINT_COEFFn, n=[0..3]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_DEINT_COEFFn registers contain the set of luma filter coefficients, where w3 is for the center pixel, w2 is for (+1, -1) pixels, w1 is for (+2, -2) pixels, and w0 is for (+3, -3) pixels.

VPE_PPP_DEINT_COEFFn

Bits	Name	Description
31:10	RESERVED_BITS31_10	
9:0	COEFF	Luma filter coefficient w0 to w3 (s10).

0x05340400+ 4*n VPE_PPP_CSC_MV1n, n=[0..8]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_CSC_MV1n register contains the set1 matrix vector.

VPE_PPP_CSC_MV1n

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12:0	MV1	MV1 = Matrix vector set1 (s4.9). Matrices are indexed left to right, top to bottom. That is, row 1, col 0 index = 3 (index range - 0 to 8).

0x05340440+ 4*n VPE_PPP_CSC_MV2n, n=[0..8]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_CSC_MV2n register contains the set2 matrix vector.

VPE_PPP_CSC_MV2n

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12:0	MV2	MV2 = Matrix vector set2 (s4.9). Matrices are indexed left to right, top to bottom. That is, row 1, col 0 index = 3 (index range - 0 to 8).

0x05340500+ 4*n VPE_PPP_CSC_PRE_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_CSC_PRE_BV1n register contains the set1 pre-bias vector.

P_

VPE_PPP_CSC_PRE_BV1n

Bits	Name	Description
31:9	RESERVED_BITS31_9	

VPE_PPP_CSC_PRE_BV1n (cont.)

Bits	Name	Description
8:0	PRE_BV1	PRE_BV1= Pre-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x05340540+4*n VPE_PPP_CSC_PRE_BV2n, n=[0..2]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_CSC_PRE_BV2n register contains the set2 pre-bias vector.

VPE_PPP_CSC_PRE_BV2n

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8:0	PRE_BV2	PRE_BV2 = Pre-bias vector set2 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x05340580+4*n VPE_PPP_CSC_POST_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_CSC_POST_BV1n register contains the set1 post-bias vector.

VPE_PPP_CSC_POST_BV1n

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8:0	POST_BV1	POST_BV1 = Post-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x053405C0+4*n VPE_PPP_CSC_POST_BV2n, n=[0..2]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_CSC_POST_BV2n register contains the set2 post-bias vector.

VPE_PPP_CSC_POST_BV2n

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8:0	POST_BV2	POST_BV2 = Post-bias vector set2 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x05340600+4*n VPE_PPP_CSC_PRE_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_CSC_PRE_LV1n register contains the set1 pre-limit vector.

VPE_PPP_CSC_PRE_LV1n

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	PRE_LV1	PRE_LV1 = Pre-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x05340640+4*n VPE_PPP_CSC_PRE_LV2n, n=[0..5]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_CSC_PRE_LV2n register contains the set2 pre-limit vectors.

VPE_PPP_CSC_PRE_LV2n

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	PRE_LV2	PRE_LV2 = Pre-limit vector set2 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x05340680+ 4*n VPE_PPP_CSC_POST_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_CSC_POST_LV1n register contains the set1 post-limit vector.

VPE_PPP_CSC_POST_LV1n

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	POST_LV1	POST_LV1 = Post-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x053406C0+ 4*n VPE_PPP_CSC_POST_LV2n, n=[0..5]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_CSC_POST_LV2n register contains the set2 post-limit vectors.

VPE_PPP_CSC_POST_LV2n

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	POST_LV2	POST_LV2 = Post-limit vector set2 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x05340800+ 4*n VPE_PPP_CSC_LUT1n, n=[0..255]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0xXXXX_XXXX

The VPE_PPP_CSC_LUT1n registers contains the color lookup values for LUT set1. These are implemented as a ram, so on reset the value is X.

VPE_PPP_CSC_LUT1n

Bits	Name	Description
31:24	RESERVED_BITS31_24	

VPE_PPP_CSC_LUT1n (cont.)

Bits	Name	Description
23:16	LUT_COLOR2	LUT value for color2.
15:8	LUT_COLOR1	LUT value for color1.
7:0	LUT_COLOR0	LUT value for color0.

0x05340C00+4*n VPE_PPP_CSC_LUT2n, n=[0..255]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0xXXXX_XXXX

The VPE_PPP_CSC_LUT2n registers contains the color lookup values for LUT set2.These are implemented as a ram, so on reset the value is X.

VPE_PPP_CSC_LUT2n

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	LUT_COLOR2	LUT value for color2.
15:8	LUT_COLOR1	LUT value for color1.
7:0	LUT_COLOR0	LUT value for color0.

0x05350000 VPE_PPP_SCALE_STATUS

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0FFF

VPE_PPP_SCALE_STATUS

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	IDLES	Internal block idles

0x05350010 VPE_PPP_SCALE_SVI_PARAM

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_7304

The VPE_PPP_SCALE_SVI_PARAM register contains all the parameters for applying the SVI on the polyphase scaler.

VPE_PPP_SCALE_SVI_PARAM

Bits	Name	Description
31:16	RESERVED_BIT31_16	
15:8	SVI_THRESH0	SVI threshold 0 (A0), default 0.45
7:4	RESERVED_BITS7_4	
3:0	SVI_AMP0	SVI gain 0 (k0), default 4

0x05350020 VPE_PPP_SCALE_SHARPEN_CFG

Type: Read/Write
Clock: VPE_CLK
Reset State: 0x0000_0040

The VPE_PPP_SCALE_SHARPEN_STRENGTH register sets the sharpening strength.

VPE_PPP_SCALE_SHARPEN_CFG

Bits	Name	Description
31:17	RESERVED_BITS31_17	
7:0	STRENGTH	Sharpening strength (a), range = [-127, 127], default 64

0x05350400+8*n VPE_PPP_SCALE_COEFF_LSP_n, n=[0..127]

Type: Read/Write
Clock: VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_SCALE_COEFF_LSP_n register contains the Least Significant Portion of the whole coefficient word, i.e., coefficients for k-1 and k samples. Note, each coefficient value is aligned to 16-bit word boundary.

VPE_PPP_SCALE_COEFF_LSP_n

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	COEFF1	10 bit (signed) poly-phase scale coefficient for k sample.
15:10	RESERVED_BITS15_10	
9:0	COEFF0	10 bit (signed) poly-phase scale coefficient for k-1 sample.

0x05350404+8*n VPE_PPP_SCALE_COEFF_MSP_n, n=[0..127]

Type: Read/Write
Clock: VPE_CLK
Reset State: 0x0000_0000

The VPE_PPP_SCALE_COEFF_MSP_n register contains the Most Significant Portion of the whole coefficient word, i.e., coefficients for k+1 and k+2 samples. Note, each coefficient value is aligned to 16-bit word boundary. The FIR coefficient tables should be written to in sequence of LSP write first followed by MSP write, writing from lower address to higher address. Each MSP register write actually triggers the write of whole 40-bit coefficient word into the RAM. The tables are separated into different ranges: set D0 starts at 0x50400; set D1 starts at 0x50500; set D2 starts at 0x50600; and set U1 starts at 0x50700. Each set takes up 0x100 addresses.

VPE_PPP_SCALE_COEFF_MSP_n

Bits	Name	Description
31:26	RESERVED_BITS31_26	
25:16	COEFF3	10 bit (signed) poly-phase scale coefficient for k+2 sample.
15:10	RESERVED_BITS15_10	
9:0	COEFF2	10 bit (signed) poly-phase scale coefficient for k+1 sample.

0x05370000 VPE_PPP_BLEND_STATUS

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0027

VPE_PPP_BLEND_STATUS

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:0	IDLES	Internal idles and valids

0x05370004 VPE_PPP_BLEND_COLOR3_OUT

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BLEND_COLOR3_OUT

Bits	Name	Description
31:1	RESERVED_BITS31_1	

VPE_PPP_BLEND_COLOR3_OUT (cont.)

Bits	Name	Description
0	C3_OUT_SEL	Selects which source to drive on the color3 component output in the blending region: 0x0: Background layer color3 0x1: Foreground color3

0x05370010 VPE_PPP_BLEND_BG_ALPHA_SEL

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_PPP_BLEND_BG_ALPHA_SEL

Bits	Name	Description
31:24	CONSTANT_ALPHA	Constant alpha value.
23:4	RESERVED_BITS23_4	
3	BLEND_EQ_SEL	Blend equation select: 0x0: normal (alpha selected is applied to bg pixel) 0x1: reverse alpha (1-alpha is applied to bg pixel)
2:1	BLEND_ALPHA_SEL	Blending alpha select: 0x0: fg per pixel alpha blend (layer0 alpha) 0x1: bg per pixel alpha blend (layer1 alpha) 0x2: constant alpha blend
0	MODE	Selects whether PPP_OP_MODE register setting chooses the alpha selection for both fg and bg (Normal mode) or bg alpha blending is destinated separately using this register: 0x0: Normal 0x1: Separate BG alpha sel

14.16.8 DMA_P registers

0x05390000 VPE_DMA_P_CONFIG

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_CONFIG

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:25	IBUF_FORMAT	0x0: RGB888 format (Default) 0x1: RGB565 format 0x2: xRGB8888 format (not supported for compressed IBUF) 0x3: Undefined
24	DITHER_EN	Dither enable
23:22	RESERVED_BIT23_22	
21	RESERVED_BIT21	
20:19	OUT_SEL	DMA channel output interface select. 0x0: AHB (EBI2) 0x1: MDDI 0x2: LCDC (parallel RGB interface) 0x3: MDDI based LCDC
18	BIT_MASK_POLARITY	Select the bit mask polarity. 0x0: Masked bits are set to '0' 0x1: Masked bits are set to '1'
17	RESERVED_BIT17	
16	COMP2_BIT_FLIP_EN	When set (1) flips all the bits of component2.
15	COMP1_BIT_FLIP_EN	When set (1) flips all the bits of component1.
14	COMP0_BIT_FLIP_EN	When set (1) flips all the bits of component0.
13:8	PACK_PATTERN	Packing pattern used by the packer. 0x21: Data packed as RGB (default) 0x24: Data packed as RBG 0x12: Data packed as BGR 0x18: Data packed as BRG 0x6: Data packed as GBR 0x9: Data packed as GRB
7	PACK_ALIGN	Packing alignment (within a byte) for each color component. This is valid only in parallel LCDC case where the output is packed loose. Not valid for MDDI based LCDC where the output is packed tight. 0x0: LSB (default) 0x1: MSB
6	EBI2_SPLIT_PIX	Set (1) to split one pixel (in 888 format) in to two 12-bit writes. This bit should be set only if the output interface is AHB.
5:4	COMP2_OUT_BITS	Number of bits for component 2 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).
3:2	COMP1_OUT_BITS	Number of bits for component 1 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).

VPE_DMA_P_CONFIG (cont.)

Bits	Name	Description
1:0	COMP0_OUT_BITS	Number of bits for component 0 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).

0x05390004 VPE_DMA_P_SIZE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_SIZE register defines the primary DMA output ROI width and height in pixels. This register is Double Buffered in LCDC mode and the programmed value is latched in to the second buffer every Vsync.

VPE_DMA_P_SIZE

Bits	Name	Description
31:27	RESERVED_BITS31_27	This field has no function and should be set to zero for future compatibility
26:16	DMA_H	DMA output ROI height (in pixels). For LCDC, this specifies the active region height.
15:11	RESERVED_BITS15_11	This field has no function and should be set to zero for future compatibility
10:0	DMA_W	DMA output ROI width (in pixels). For LCDC, this specifies the active region width. Note: The max. ROI width supported when the IBUF is compressed is 1280 when ROI start is 4x4 grid aligned and is 1277 (worst-case) if not grid aligned. The max. width supported is 2047 when IBUF is uncompressed. These restrictions are because of line buffer size limitations in hardware.

0x05390008 VPE_DMA_P_IBUF_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_IBUF_ADDR register defines the primary DMA IBUF address. This register is Double Buffered in LCDC mode and the programmed value is latched in to the second buffer every Vsync.

VPE_DMA_P_IBUF_ADDR

Bits	Name	Description
31:0	IBUF_ADDR	Intermediate buffer base address (byte-aligned). This defines the start of image. Note: If decompression is enabled, the memory size allocated for IBUF should be a multiple of 4x4 irrespective of whether the image in IBUF is a multiple of 4x4.

0x0539000C VPE_DMA_P_IBUF_Y_STRIDE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_IBUF_Y_STRIDE register defines the line jump value (in bytes) in the intermediate buffer. This register is Double Buffered in LCDC mode and the programmed value is latched in to the second buffer every Vsync.

VPE_DMA_P_IBUF_Y_STRIDE

Bits	Name	Description
31:14	RESERVED_BITS31_14	This field has no function and should be set to zero for future compatibility
13:0	IBUF_Y_STRIDE	Y-stride (or) line jump in bytes in the image IBUF.

0x05390010 VPE_DMA_P_OUT_XY

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_OUT_XY

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:16	DMA_OUT_Y	Display (or) screen y coordinate (pixel) where the first line of a ROI will be written. Program this parameter to zero if the output interface is LCDC since all LCDC updates are full screen.
15:11	RESERVED_BITS15_11	
10:0	DMA_OUT_X	Display (or) screen x coordinate (pixel) where the first pixel of a ROI will be written. Program this parameter to zero if the output interface is LCDC since all LCDC updates are full screen.

0x05390014 VPE_DMA_P_LINE_COUNT

Type: Read
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_LINE_COUNT

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:0	LINE_COUNT	Provides the line count or write pointer value (read pointer if output to LCDC). This value is w.r.t. display height and not ROI height.

0x05390018 VPE_DMA_P_LINE_IRQ

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_LINE_IRQ defines the line count or write_pointer value at which an interrupt has to be generated.

VPE_DMA_P_LINE_IRQ

Bits	Name	Description
31:11	RESERVED_BITS31_11	This field has no function and should be set to zero for future compatibility
10:0	IRQ_LINE	Specify the line count or write pointer value at which an interrupt has to be generated. Specify this value w.r.t. display height and not ROI height.

0x0539001C VPE_DMA_P_MASK_PATTERN

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_MASK_PATTERN register defines the pattern that will be used when bit masking is enabled.

VPE_DMA_P_MASK_PATTERN

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	BIT_MASK_PATTERN	This pattern is used to mask the pixel bits when bit masking is enabled. If a pattern bit is set (1) the corresponding pixel bit is masked. The pattern is specified as {C2, C1, C0} where each color component is loosely packed according to the output format in to 8-bits and LSB aligned.

0x05390020 VPE_DMA_P_PROFILE_EN

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

VPE_DMA_P_PROFILE_EN

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	EN	Enable the ROI cycle counter for profiling

0x05390024 VPE_DMA_P_PROFILE_COUNT

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_PROFILE_COUNT

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	TOTAL_CYCLE	Total cycle count (in AXI cycles) in a ROI, from ROI start to last pixel out of Packer (DMA_P goes back to Idle). This count will be reset automatically at the beginning of each ROI start.

0x05390040 VPE_DMA_P_CURSOR_FORMAT

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_CURSOR_FORMAT

Bits	Name	Description
31:3	RESERVED_BITS31_2	
2:0	CURSOR_FORMAT	0x0: ARGB8888 format (Default)

0x05390044 VPE_DMA_P_CURSOR_SIZE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_CURSOR_SIZE register defines the hardware cursor width and height in pixels. This register is Double Buffered in LCDC mode and the programmed value is latched in to the second buffer every Vsync.

VPE_DMA_P_CURSOR_SIZE

Bits	Name	Description
31:23	RESERVED_BITS31_23	This field has no function and should be set to zero for future compatibility
22:16	CURSOR_H	Cursor height (in lines). Max. supported height = 64 lines.
15:7	RESERVED_BITS15_7	This field has no function and should be set to zero for future compatibility
6:0	CURSOR_W	Cursor width (in pixels). Max. supported width = 64 pixels

0x05390048 VPE_DMA_P_CURSOR_BUF_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_CURSOR_BUF_ADDR register defines the cursor buffer address. This register is Double Buffered in LCDC mode and the programmed value is latched in to the second buffer every Vsync.

VPE_DMA_P_CURSOR_BUF_ADDR

Bits	Name	Description
31:0	CURSOR_BUF_ADDR	Cursor buffer base address (byte-aligned).

0x0539004C VPE_DMA_P_CURSOR_POSITION

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_CURSOR_POSITION register defines the start x and y positions of the cursor relative to ROI start x and y. This register is Double Buffered in LCDC mode and the programmed value is latched in to the second buffer every Vsync.

VPE_DMA_P_CURSOR_POSITION

Bits	Name	Description
31:28	RESERVED_BITS31_28	This field has no function and should be set to zero for future compatibility
27:16	CURSOR_Y_START	Define the start (y) position of the cursor relative to ROI start (y). This is a signed value and has to be programmed in (s12) format.
15:12	RESERVED_BITS15_12	This field has no function and should be set to zero for future compatibility
11:0	CURSOR_X_START	Define the start (x) position of the cursor relative to ROI start (x). This is a signed value and has to be programmed in (s12) format.

0x05390060 VPE_DMA_P_CURSOR_BLEND_CONFIG

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_CURSOR_BLEND_CONFIG register enables cursor blend and defines some blend parameters. This register is Double Buffered in LCDC mode and the programmed value is latched in to the second buffer every Vsync.

VPE_DMA_P_CURSOR_BLEND_CONFIG

Bits	Name	Description
31:4	RESERVED_BITS31_4	
3	BLEND_TRANSP_EN	Transparency check enable: 0x0: Off (Output is according to blend_alpha_sel blend output.) 0x1: On (Color keying is done on the cursor and blended result specified from the 2 layers is passed if non-matching; otherwise, the background image layer is sent.)
2:1	BLEND_ALPHA_SEL	Blending alpha select: 0x1: Cursor per pixel alpha (Default) 0x2: Constant alpha
0	BLEND_EN	Cursor blend enable (when disabled, output pixels would be the same as the background image pixels).

0x05390064 VPE_DMA_P_CURSOR_BLEND_PARAM

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_CURSOR_BLEND_PARAM

Bits	Name	Description
31:24	CONSTANT_ALPHA	Constant alpha value.
23:0	TRANSPARENT_COLOR	Color to be used if transparency (color-keying) is enabled (C2,C1,C0 each 8 bits from MSB to LSB).

0x05390068 VPE_DMA_P_CURSOR_BLEND_TRANS_MASK

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_CURSOR_BLEND_TRANS_MASK

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	TRANSPARENCY_MASK	Mask to be used if transparency is enabled (C2,C1,C0 each 8 bits from MSB to LSB). Setting a bit to (1) means the corresponding bit in the transparent_color is ignored during color-keying.

0x05390070 VPE_DMA_P_COLOR_CORRECT_CONFIG

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_COLOR_CORRECT_CONFIG register defines the color and gamma correct parameters. This register is Double Buffered in LCDC mode and the programmed value is latched in to the second buffer every Vsync.

VPE_DMA_P_COLOR_CORRECT_CONFIG

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12	COLOR_FMT_OUT	Select the output color format after correction/conversion 0x0: RGB (default) 0x1: YCbCr
11	COLOR_FMT_IN	Select the input color format for correction/conversion 0x0: RGB (default) 0x1: YCbCr
10	LUT_SEL	Selects which LUT to use during processing 0x0: Set1 0x1: Set2
9	POST_LIMIT_SEL	Selects which post-limit (i.e., post-clamp) to use during processing 0x0: Set1 0x1: Set2
8	PRE_LIMIT_SEL	Selects which pre-limit (i.e., pre-clamp) to use during processing 0x0: Set1 0x1: Set2
7	POST_BIAS_SEL	Selects which post-bias to use during processing 0x0: Set1 0x1: Set2
6	PRE_BIAS_SEL	Selects which pre-bias to use during processing 0x0: Set1 0x1: Set2
5	CONVERT_MATRIX_SEL	Selects which matrix to use during processing 0x0: Set1 0x1: Set2
4	LUT_POSITION	Specifies the position of LUT/Gamma table 0x0: Pre-LUT (before matrix convert) 0x1: Post-LUT (after matrix convert)
3	CONVERT_MATRIX_EN	Enable color convert. This enables the matrix conversion in the convert block.
2	LUT_C2_EN	Component 2 LUT enable.
1	LUT_C1_EN	Component 1 LUT enable.
0	LUT_C0_EN	Component 0 LUT enable.

0x05390080 VPE_DMA_P_DECOMP_CONFIG

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_DECOMP_CONFIG register enables decompression and selects decompress mode. This register is Double Buffered in LCDC mode and the programmed value is latched in to the second buffer every Vsync.

VPE_DMA_P_DECOMP_CONFIG

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2:1	DECOMP_MODE	Select decompression mode 0x0: Lossless (default) 0x1: Lossy with bit shift 0x2: Lossy with bit promotion 0x3: Undefined
0	DECOMP_EN	Decompression enable 0x0: Disable (default) 0x1: Enable

0x05390084 VPE_DMA_P_DECOMP_HDR_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_DECOMP_HDR_ADDR register defines the header address corresponding to the first 4x4 compressed tile in the image IBUF. This register is Double Buffered in LCDC mode and the programmed value is latched in to the second buffer every Vsync.

VPE_DMA_P_DECOMP_HDR_ADDR

Bits	Name	Description
31:0	DECOMP_HDR_ADDR	Header address (byte-aligned) corresponding to the first 4x4 compressed tile in the image IBUF. First 4x4 compressed tile is located at x=0, y=0 input (pixel) coordinate.

0x05390088 VPE_DMA_P_DECOMP_HDR_Y_STRIDE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_DECOMP_HDR_Y_STRIDE register defines the jump value (in bytes) for header fetch when moving from one stripe to next. This register is Double Buffered in LCDC mode and the programmed value is latched in to the second buffer every Vsync.

VPE_DMA_P_DECOMP_HDR_Y_STRIDE

Bits	Name	Description
31:14	RESERVED_BITS31_14	
13:0	DECOMP_HDR_Y_STRIDE	Y-stride (in bytes) for headers of 4x4 compressed tiles in the image IBUF.

0x0539008C VPE_DMA_P_IBUF_XY

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_IBUF_XY register defines the start location of the ROI within an IBUF. This register is Double Buffered in LCDC mode and the programmed value is latched in to the second buffer every Vsync.

VPE_DMA_P_IBUF_XY

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:16	ROI_Y	Defines the y-offset (in pixels) of the ROI in the image IBUF.
15:11	RESERVED_BITS15_11	
10:0	ROI_X	Defines the x-offset (in pixels) of the ROI in the image IBUF.

0x05390090 VPE_DMA_P_DECOMP_PROFILE_COUNT

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_P_DECOMP_PROFILE_COUNT register provides the total number of header bytes and image bytes read from a compressed IBUF for a particular ROI. The compression ratio can be calculated by dividing the contents of this register by the total number of output bytes (ROI_H * ROI_W * bytes_per_pixel).

VPE_DMA_P_DECOMP_PROFILE_COUNT

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	FETCH_BYTE_CNT	Total no. of bytes (header + compressed image) fetched for the current ROI. This count will be reset automatically at the beginning of each ROI.

0x05393400+ 4*n VPE_DMA_P_CSC_MV1n, n=[0..8]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_CSC_MV1n register contains the set1 matrix vector.

VPE_DMA_P_CSC_MV1n

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12:0	MV1	MV1 = Matrix vector set1 (s4.9). Matrices are indexed left to right, top to bottom. That is, row 1, col 0 index = 3 (index range - 0 to 8).

0x05393440+ 4*n VPE_DMA_P_CSC_MV2n, n=[0..8]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_CSC_MV2n register contains the set2 matrix vector.

VPE_DMA_P_CSC_MV2n

Bits	Name	Description
31:13	RESERVED_BITS31_13	
12:0	MV2	MV2 = Matrix vector set2 (s4.9). Matrices are indexed left to right, top to bottom. That is, row 1, col 0 index = 3 (index range - 0 to 8).

0x05393500+4*n VPE_DMA_P_CSC_PRE_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_CSC_PRE_BV1n register contains the set1 pre-bias vector.

P_

VPE_DMA_P_CSC_PRE_BV1n

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8:0	PRE_BV1	PRE_BV1= Pre-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x05393540+4*n VPE_DMA_P_CSC_PRE_BV2n, n=[0..2]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_CSC_PRE_BV2n register contains the set2 pre-bias vector.

VPE_DMA_P_CSC_PRE_BV2n

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8:0	PRE_BV2	PRE_BV2 = Pre-bias vector set2 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x05393580+4*n VPE_DMA_P_CSC_POST_BV1n, n=[0..2]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_CSC_POST_BV1n register contains the set1 post-bias vector.

VPE_DMA_P_CSC_POST_BV1n

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8:0	POST_BV1	POST_BV1 = Post-bias vector set1 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x053935C0+4*n VPE_DMA_P_CSC_POST_BV2n, n=[0..2]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_CSC_POST_BV2n register contains the set2 post-bias vector.

VPE_DMA_P_CSC_POST_BV2n

Bits	Name	Description
31:9	RESERVED_BITS31_9	
8:0	POST_BV2	POST_BV2 = Post-bias vector set2 (s9). 0=R (or) Ybias, 1=G (or) Cb bias, 2=B (or) Cr bias.

0x05393600+ 4*n VPE_DMA_P_CSC_PRE_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_CSC_PRE_LV1n register contains the set1 pre-limit vector.

VPE_DMA_P_CSC_PRE_LV1n

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	PRE_LV1	PRE_LV1 = Pre-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x05393640+ 4*n VPE_DMA_P_CSC_PRE_LV2n, n=[0..5]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_CSC_PRE_LV2n register contains the set2 pre-limit vectors.

VPE_DMA_P_CSC_PRE_LV2n

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	PRE_LV2	PRE_LV2 = Pre-limit vector set2 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x05393680+ 4*n VPE_DMA_P_CSC_POST_LV1n, n=[0..5]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_CSC_POST_LV1n register contains the set1 post-limit vector.

VPE_DMA_P_CSC_POST_LV1n

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	POST_LV1	POST_LV1 = Post-limit vector set1 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x053936C0+ 4*n VPE_DMA_P_CSC_POST_LV2n, n=[0..5]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_CSC_POST_LV2n register contains the set2 post-limit vectors.

VPE_DMA_P_CSC_POST_LV2n

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	POST_LV2	POST_LV2 = Post-limit vector set2 (u8). For limit vectors, 0 = R (or) Y low, 1 = R (or) Y high, 2= G (or) Cb low, 3= G (or) Cb high, 4 = B (or) Cr low, 5= B (or) Cr high.

0x05393800+ 4*n VPE_DMA_P_CSC_LUT1n, n=[0..255]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_CSC_LUT1n registers contains the color lookup values for LUT set1.

VPE_DMA_P_CSC_LUT1n

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	LUT_COLOR2	LUT value for color2.

VPE_DMA_P_CSC_LUT1n (cont.)

Bits	Name	Description
15:8	LUT_COLOR1	LUT value for color1.
7:0	LUT_COLOR0	LUT value for color0.

0x05393C00+4*n VPE_DMA_P_CSC_LUT2n, n=[0..255]

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_CSC_LUT2n registers contains the color lookup values for LUT set2.

VPE_DMA_P_CSC_LUT2n

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	LUT_COLOR2	LUT value for color2.
15:8	LUT_COLOR1	LUT value for color1.
7:0	LUT_COLOR0	LUT value for color0.

0x05394000 VPE_DMA_P_HIST_START

Type: Write Only
Clock: CC_VPE_CLK
Reset State: N/A

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_HIST_START register kicks off histogram generation.

VPE_DMA_P_HIST_START

Bits	Name	Description
31:0	HIST_START	A write to this register kicks off histogram generation. Actual accumulation begins at the start of next ROI. Histogram accumulation can be started only when histogram reset sequence is not currently active.

0x05394004 VPE_DMA_P_HIST_FRAME_CNT

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_HIST_FRAME_CNT register is used to program the frame count for histogram accumulation.

VPE_DMA_P_HIST_FRAME_CNT

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:0	FRAME_CNT	Program the number of frames over which the histogram data has to be collected. If the frame count programmed is more than what each 24-bit bin can support, the bin count will saturate at the maximum value. Here are some max. frame counts that can be programmed for different image sizes for a 24-bit bin. XGA (1024 x 768) - 21 WSVGA (1024 x 600) - 27 WVGA (800 x 480) - 43 VGA (640 x 480) - 54

0x05394008 VPE_DMA_P_HIST_BIT_MASK

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_HIST_BIT_MASK register specifies which MSBs need to be masked before histogram binning.

VPE_DMA_P_HIST_BIT_MASK

Bits	Name	Description
31	BIT_MASK_POLARITY	If set to (1) masked bits are compared to '1' else compared to '0'
30:2	RESERVED_BITS30_2	

VPE_DMA_P_HIST_BIT_MASK (cont.)

Bits	Name	Description
1:0	BIT_MASK	Select which MSBs of the input color component have to be masked before histogram binning. The five unmasked MSBs will be used for bin address generation if the polarity of all the masked bits matches BIT_MASK_POLARITY. 0x0: No masking (default) 0x1: Mask one MSB 0x2: Mask two MSBs 0x3: Mask three MSBs

0x0539400C VPE_DMA_P_HIST_RESET_SEQ_START

Type: Write Only
Clock: CC_VPE_CLK
Reset State: N/A

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_HIST_RESET_SEQ_START kicks off a reset sequence.

VPE_DMA_P_HIST_RESET_SEQ_START

Bits	Name	Description
31:0	RESET_SEQ_START	Writing to this register kicks off a reset sequence.This reset sequence clears all RAM locations and RAM rd/wr pointers. The reset sequence can be initiated only when histogram generation is not currently active. Note: Functional clock gating will shut off the clock to DMA_P sub-blocks when a ROI is not being processed. So DMA_P clock should be forced ON for the reset sequence to complete.

0x05394010 VPE_DMA_P_HIST_CONTROL

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_HIST_CONTROL register controls histogram operation.

VPE_DMA_P_HIST_CONTROL

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	AUTO_CLEAR_EN	When set (1), the bin from which data has been read is cleared automatically.

0x05394014 VPE_DMA_P_HIST_INTR_STATUS

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_HIST_INTR_STATUS register provides histogram interrupt status.

VPE_DMA_P_HIST_INTR_STATUS

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	HIST_DONE	When set (1) implies histogram generation is complete.
0	RESET_SEQ_DONE	When set (1) implies the reset sequence is complete.

0x05394018 VPE_DMA_P_HIST_INTR_CLEAR

Type: Write Only
Clock: CC_VPE_CLK
Reset State: N/A

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_HIST_INTR_CLEAR is used to clear the interrupts generated by histogram block.

VPE_DMA_P_HIST_INTR_CLEAR

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	HIST_DONE	Write (1) to this bit to clear the status.
0	RESET_SEQ_DONE	Write (1) to this bit to clear the status.

0x0539401C VPE_DMA_P_HIST_INTR_ENABLE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_HIST_INTR_ENABLE is used to enable the interrupt sources within the histogram block.

VPE_DMA_P_HIST_INTR_ENABLE

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	HIST_DONE	Write (1) to this bit to enable the interrupt source.
0	RESET_SEQ_DONE	Write (1) to this bit to enable the interrupt source.

0x05394100+4*n VPE_DMA_P_HIST_R_DATAn, n=[0..31]

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_HIST_R_DATAn register provides the histogram data corresponding to the color component R.

VPE_DMA_P_HIST_R_DATAn

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	HIST_R_DATA	Reading this register provides histogram bin data for component R.

0x05394200+4*n VPE_DMA_P_HIST_G_DATAn, n=[0..31]

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_HIST_G_DATAn register provides the histogram data corresponding to the color component G.

VPE_DMA_P_HIST_G_DATAn

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	HIST_G_DATA	Reading this register provides histogram bin data for component G.

0x05394300+4*n VPE_DMA_P_HIST_B_DATAn, n=[0..31]

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_DMA_P_HIST_B_DATAn register provides the histogram data corresponding to the color component B.

VPE_DMA_P_HIST_B_DATAn

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	HIST_B_DATA	Reading this register provides histogram bin data for component B.

14.16.9 DMA_S registers

0x053A0000 VPE_DMA_S_CONFIG

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_S_CONFIG

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:25	IBUF_FORMAT	0x0: RGB888 format (Default) 0x1: RGB565 format 0x2: xRGB8888 format 0x3: Undefined
24	DITHER_EN	Dither enable.
23:22	RESERVED_BIT23_22	
21	RESERVED_BIT21	
20:19	OUT_SEL	DMA channel output interface select. 0x0: AHB (EBI2 Cannot be selected if DMA_E drives EBI2) 0x1: MDDI 0x2: LCDC (Not supported in DMA_S)
18	BIT_MASK_POLARITY	Select the bit mask polarity. 0x0: Masked bits are set to '0' 0x1: Masked bits are set to '1'
17	RESERVED_BIT17	
16	COMP2_BIT_FLIP_EN	When set (1) flips all the bits of component2.
15	COMP1_BIT_FLIP_EN	When set (1) flips all the bits of component1.
14	COMP0_BIT_FLIP_EN	When set (1) flips all the bits of component0.
13:8	PACK_PATTERN	Packing pattern used by the packer. 0x21: Data packed as RGB (default) 0x24: Data packed as RBG 0x12: Data packed as BGR 0x18: Data packed as BRG 0x6: Data packed as GBR 0x9: Data packed as GRB
7	RESERVED_BIT7	
6	EBI2_SPLIT_PIX	Set (1) to split one pixel (in 888 format) in to two 12-bit writes. This bit should be set only if the output interface is AHB.
5:4	COMP2_OUT_BITS	Number of bits for component 2 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).
3:2	COMP1_OUT_BITS	Number of bits for component 1 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).
1:0	COMP0_OUT_BITS	Number of bits for component 0 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).

0x053A0004 VPE_DMA_S_SIZE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_S_SIZE register defines the secondary DMA output width and height in pixels

VPE_DMA_S_SIZE

Bits	Name	Description
31:27	RESERVED_BITS31_27	This field has no function and should be set to zero for future compatibility
26:16	DMA_H	DMA output image height (in pixels).
15:11	RESERVED_BITS15_11	This field has no function and should be set to zero for future compatibility
10:0	DMA_W	DMA output image width (in pixels).

0x053A0008 VPE_DMA_S_IBUF_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_S_IBUF_ADDR register defines the secondary DMA IBUF address.

VPE_DMA_S_IBUF_ADDR

Bits	Name	Description
31:0	IBUF_ADDR	Intermediate buffer base address (byte-aligned).

0x053A000C VPE_DMA_S_IBUF_Y_STRIDE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_S_IBUF_Y_STRIDE register defines the line jump value (in bytes) in the intermediate buffer

VPE_DMA_S_IBUF_Y_STRIDE

Bits	Name	Description
31:14	RESERVED_BITS31_14	This field has no function and should be set to zero for future compatibility
13:0	IBUF_Y_STRIDE	Y-stride (or) line jump value in bytes in the intermediate buffer. Irrespective of whether the data in IBUF is contiguous or non-contiguous, line jump value has to be provided since all the DMA requests are line requests.

0x053A0010 VPE_DMA_S_OUT_XY

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_S_OUT_XY

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:16	DMA_OUT_Y	Screen y coordinate (pixel) where the first line of a ROI will be written.
15:11	RESERVED_BITS15_11	
10:0	DMA_OUT_X	Screen x coordinate (pixel) where the first pixel of a ROI will be written.

0x053A0014 VPE_DMA_S_LINE_COUNT

Type: Read
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_S_LINE_COUNT

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:0	LINE_COUNT	Provides the line count or write pointer value. This value is w.r.t. display height and not ROI height.

0x053A0018 VPE_DMA_S_LINE_IRQ

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_S_LINE_IRQ defines the line count or write_pointer value at which an interrupt has to be generated..

VPE_DMA_S_LINE_IRQ

Bits	Name	Description
31:11	RESERVED_BITS31_11	This field has no function and should be set to zero for future compatibility
10:0	IRQ_LINE	Specify the line count or write pointer value at which an interrupt has to be generated. Specify this value w.r.t. display height and not ROI height.

0x053A001C VPE_DMA_S_MASK_PATTERN

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_S_MASK_PATTERN register defines the pattern that will be used when bit masking is enabled.

VPE_DMA_S_MASK_PATTERN

Bits	Name	Description
31:24	RESERVED_BITS31_24	

VPE_DMA_S_MASK_PATTERN (cont.)

Bits	Name	Description
23:0	BIT_MASK_PATTERN	This pattern is used to mask the pixel bits when bit masking is enabled. If a pattern bit is set (1) the corresponding pixel bit is masked. The pattern is specified as {C2, C1, C0} where each color component is loosely packed according to the output format in to 8-bits and LSB aligned.

0x053A0020 VPE_DMA_S_PROFILE_EN

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_S_PROFILE_EN

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	EN	Enable the ROI cycle counter for profiling

0x053A0024 VPE_DMA_S_PROFILE_COUNT

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_S_PROFILE_COUNT

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	TOTAL_CYCLE	Total cycle count (in AXI cycles) in a ROI, from ROI start to last pixel out of Packer (DMA_S goes back to Idle). This count will be reset automatically at the beginning of each ROI start.

14.16.10 DMA_E registers

0x053B0000 VPE_DMA_E_CONFIG

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_E_CONFIG

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:25	IBUF_FORMAT	0x0: RGB888 format (Default) 0x1: RGB565 format 0x2: xRGB8888 format 0x3: Undefined
24	DITHER_EN	Dither enable.
23:22	RESERVED_BIT23_22	
21	RESERVED_BIT21	
20:19	OUT_SEL	DMA channel output interface select. Note: DMA_E cannot drive EBI2 when OUT_SEL in VPE_DMA_S_CONFIG holds a value 0x0 (EBI2) 0x0: AHB (EBI2 Cannot be selected if DMA_S drives EBI2) 0x1: MDDI 0x2: LCDC (Not supported in DMA_E)
18	BIT_MASK_POLARITY	Select the bit mask polarity. 0x0: Masked bits are set to '0' 0x1: Masked bits are set to '1'
17	RESERVED_BIT17	
16	COMP2_BIT_FLIP_EN	When set (1) flips all the bits of component2.
15	COMP1_BIT_FLIP_EN	When set (1) flips all the bits of component1.
14	COMP0_BIT_FLIP_EN	When set (1) flips all the bits of component0.
13:8	PACK_PATTERN	Packing pattern used by the packer. 0x21: Data packed as RGB (default) 0x24: Data packed as RBG 0x12: Data packed as BGR 0x18: Data packed as BRG 0x6: Data packed as GBR 0x9: Data packed as GRB
7	RESERVED_BIT7	

VPE_DMA_E_CONFIG (cont.)

Bits	Name	Description
6	EBI2_SPLIT_PIX	Set (1) to split one pixel (in 888 format) in to two 12-bit writes. This bit should be set only if the output interface is AHB.
5:4	COMP2_OUT_BITS	Number of bits for component 2 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).
3:2	COMP1_OUT_BITS	Number of bits for component 1 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).
1:0	COMP0_OUT_BITS	Number of bits for component 0 output: 0 = 4 bits, 1 = 5 bits, 2 = 6 bits, 3 = 8 bits (valid output formats are 444/565/666/888).

0x053B0004 VPE_DMA_E_SIZE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_E_SIZE register defines the external DMA output width and height in pixels

VPE_DMA_E_SIZE

Bits	Name	Description
31:27	RESERVED_BITS31_27	This field has no function and should be set to zero for future compatibility
26:16	DMA_H	DMA output image height (in pixels).
15:11	RESERVED_BITS15_11	This field has no function and should be set to zero for future compatibility
10:0	DMA_W	DMA output image width (in pixels).

0x053B0008 VPE_DMA_E_IBUF_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_E_IBUF_ADDR register defines the external DMA IBUF address.

VPE_DMA_E_IBUF_ADDR

Bits	Name	Description
31:0	IBUF_ADDR	Intermediate buffer base address (byte-aligned).

0x053B000C VPE_DMA_E_IBUF_Y_STRIDE

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_E_IBUF_Y_STRIDE register defines the line jump value (in bytes) in the intermediate buffer

VPE_DMA_E_IBUF_Y_STRIDE

Bits	Name	Description
31:14	RESERVED_BITS31_14	This field has no function and should be set to zero for future compatibility
13:0	IBUF_Y_STRIDE	Y-stride (or) line jump value in bytes in the intermediate buffer. Irrespective of whether the data in IBUF is contiguous or non-contiguous, line jump value has to be provided since all the DMA requests are line requests.

0x053B0010 VPE_DMA_E_OUT_XY

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_E_OUT_XY

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:16	DMA_OUT_Y	Screen y coordinate (pixel) where the first line of a ROI will be written.
15:11	RESERVED_BITS15_11	

VPE_DMA_E_OUT_XY (cont.)

Bits	Name	Description
10:0	DMA_OUT_X	Screen x coordinate (pixel) where the first pixel of a ROI will be written.

0x053B0014 VPE_DMA_E_LINE_COUNT

Type: Read
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_E_LINE_COUNT

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:0	LINE_COUNT	Provides the line count or write pointer value. This value is w.r.t. display height and not ROI height.

0x053B0018 VPE_DMA_E_LINE_IRQ

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_E_LINE_IRQ defines the line count or write_pointer value at which an interrupt has to be generated..

VPE_DMA_E_LINE_IRQ

Bits	Name	Description
31:11	RESERVED_BITS31_11	This field has no function and should be set to zero for future compatibility
10:0	IRQ_LINE	Specify the line count or write pointer value at which an interrupt has to be generated. Specify this value w.r.t. display height and not ROI height.

0x053B001C VPE_DMA_E_MASK_PATTERN

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_E_MASK_PATTERN register defines the pattern that will be used when bit masking is enabled.

VPE_DMA_E_MASK_PATTERN

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	BIT_MASK_PATTERN	This pattern is used to mask the pixel bits when bit masking is enabled. If a pattern bit is set (1) the corresponding pixel bit is masked. The pattern is specified as {C2, C1, C0} where each color component is loosely packed according to the output format in to 8-bits and LSB aligned.

0x053B0020 VPE_DMA_E_PROFILE_EN

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_E_PROFILE_EN

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	EN	Enable the ROI cycle counter for profiling

0x053B0024 VPE_DMA_E_PROFILE_COUNT

Type: Read Only
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_DMA_E_PROFILE_COUNT

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:0	TOTAL_CYCLE	Total cycle count (in AXI cycles) in a ROI, from ROI start to last pixel out of Packer (DMA_E goes back to Idle). This count will be reset automatically at the beginning of each ROI start.

14.16.11 TV Out registers

0x053C0000 VPE_TV_OUT_CTL

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_TV_OUT_CTL register is a control register for the TVOUT.

VPE_TV_OUT_CTL

Bits	Name	Description
31:3	RESERVED_BITS31_3	
2	ALPHA_ON	Alpha processing enable. 0x1: Enable 0x0: Disable
1	SOBEL_EN	Sobel filter enable. 0x1: Enable 0x0: Disable
0	TV_OUT_EN	TV_OUT module enable. 0x1: Enable 0x0: Disable

0x053C0004 VPE_TV_OUT_FIR_COEFF

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_TV_OUT_FIR_COEFF register contains the coefficients for the top, bottom, and center taps of the flicker filter.

VPE_TV_OUT_FIR_COEFF

Bits	Name	Description
31:28	RESERVED_BITS31_28	
27:16	TOP_BOTTOM	Coefficient for the top and bottom taps of the flicker filter. 0x0: Disable filter.
15:12	RESERVED_BITS15_12	
11:0	DC_OFFSET	Coefficient for the center tap of the flicker filter. 0xFFF: Disable filter.

0x053C0008 VPE_TV_OUT_BUF_ADDR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_TV_OUT_BUF_ADDR register contains the starting 29-bit address of the video frame buffer.

VPE_TV_OUT_BUF_ADDR

Bits	Name	Description
31:29	RESERVED_BITS31_29	
28:0	FRAME_POINTER	The pointer for the next video frame buffer should be updated after the start of frame output signal is detected. The new address will take effect on the next start of frame.

0x053C000C VPE_TV_OUT_CC_DATA

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_TV_OUT_CC_DATA register contains the CC data for the TV_OUT.

VPE_TV_OUT_CC_DATA

Bits	Name	Description
31:16	CC_DATA_EVEN	CC data for the even field. Driven to the TV encoder at the next start of frame.
15:0	CC_DATA_ODD	CC data for the odd field. Driven to the TV encoder at the next start of frame.

0x053C0010 VPE_TV_OUT_SOBEL

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_TV_OUT_SOBEL register contains the 8-bit sobel threshold value.

VPE_TV_OUT_SOBEL

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7:0	BUFFER_BYPASS	This field defines the filter threshold for determining if the original or filtered luma values are used.

0x053C0018 VPE_TV_OUT_Y_CLAMP

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_TV_OUT_Y_CLAMP register contains the 16-bit luna clamp value.

VPE_TV_OUT_Y_CLAMP

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	Y_MAX	8-bit upper luma clamp value
15:8	RESERVED_BITS15_8	

VPE_TV_OUT_Y_CLAMP (cont.)

Bits	Name	Description
7:0	Y_MIN	8-bit lower luma clamp value.

0x053C001C VPE_TV_OUT_CB_CLAMP

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_TV_OUT_CB_CLAMP register contains the 16-bit Cb clamp value.

VPE_TV_OUT_CB_CLAMP

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	CB_MAX	8-bit upper Cb clamp value
15:8	RESERVED_BITS15_8	
7:0	CB_MIN	8-bit lower Cb clamp value.

0x053C0020 VPE_TV_OUT_CR_CLAMP

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_TV_OUT_CR_CLAMP register contains the 16-bit Cr clamp value.

VPE_TV_OUT_CR_CLAMP

Bits	Name	Description
31:24	RESERVED_BITS31_24	
23:16	CR_MAX	8-bit upper Cr clamp value
15:8	RESERVED_BITS15_8	
7:0	CR_MIN	8-bit lower Cr clamp value.

0x053C0100 VPE_TV_OUT_STATUS

Type: Read/Write.
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

The VPE_TV_OUT_STATUS register is used to indicate the start and end of a TV OUT frame has happened. The value is cleared only if after a register write.

VPE_TV_OUT_STATUS

Bits	Name	Description
31:2	RESERVED_BITS31_2	
1	TV_EOF	End of frame.
0	TV_SOF	Start of frame.

14.16.12 Test MISR registers

0x053D0000 VPE_TEST_MODE_CLK

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_TEST_MODE_CLK register is used to select the test points for a specified VPE block.

VPE_TEST_MODE_CLK

Bits	Name	Description
31:9	RESERVED_BITS31_10	This field has no function and should be set to zero for future compatibility.

VPE_TEST_MODE_CLK (cont.)

Bits	Name	Description
8:4	BLOCK_ID	These bits select the test points for the specified VPE block into the test bus. 0x0: Disabled 0x1: Tile fetch 0x2: Upsample 0x3: CSC 0x4: Rotate 0x5: Blend 0x6: Scale 0x7: packer1a 0x8: packer1b 0x9: Downsample 0xA: Dither 0xB: Deinterlace 0xC: MDDI1 0xD: MDDI2 0xE: Unused_1 0xF: TVOUT 0x10: Unused_2 0x11: Command 0x12: ahb2ahb_slive 0x13: ahb2ahb_master 0x14: BG Tile fetch 0x15: BG Upsample 0x16: SEE_1234ABCD 0x17: mgen2maxi_xin0 0x18: mgen2maxi_xin1 0x19: mgen2maxi_xin2 0x1A: mgen2maxi_arb
3:0	TEST_PT_SEL	These bits select a set of 32-bit test points within vpe_core and mgen2maxi blocks.

0x053D0004 VPE_TEST_MISR_RESET_CLK

Type: Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_TEST_MISR_RESET_CLK register is used to reset the MISR state.

VPE_TEST_MISR_RESET_CLK

Bits	Name	Description
31:1	RESERVED_BITS31_1	This field has no function and should be set to zero for future compatibility.

VPE_TEST_MISR_RESET_CLK (cont.)

Bits	Name	Description
0	MISR_SW_RESET	A write of '1' to this address will reset the MISR state. It is a self clearing reset. The reset must be asserted after VPE_TEST_MISR_MODE_CLK is set to a non-zero value. 0x1: MISR reset.

0x053D0008 VPE_TEST_EXPORT_MISR_CLK

Type: Read-Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_TEST_EXPORT_MISR_CLK register controls what is sent on the testbus. A value of '0' (reset value) will send the data that is going into the MISR on the testbus. A value of '1' will send the current MISR state onto the testbus. The latter option is typically used for debug purposes. For example, if your final MISR signature failed, you might want to know where it failed (i.e., right in the beginning or somewhere else')

VPE_TEST_EXPORT_MISR_CLK

Bits	Name	Description
31:1	RESERVED_BITS31_1	Field has no function and should be set to zero for future compatibility.
0	MISR_EXPORT	When clear(0), testbus is driven by what is sent into the MISR. (i.e., What is the result of the MUXing of all the input data streams with VPE_TEST_ MODE_CLK) When set (1), testbus is driven by the current state of the MISR (debug typically)

0x053D000C VPE_TEST_MISR_CURR_VAL_CLK

Type: Read-Only
Clock: CC_VPE_CLK
Reset State: Undefined

A read from the address in the VPE_TEST_MISR_CURR_VAL_CLK register will return the current MISR state for this block. Keep in mind that this could change every cycle depending on how it is used.

VPE_TEST_MISR_CURR_VAL_CLK

Bits	Name	Description
31:0	MISR_VAL	It holds the current MISR state.

0x053D0100 VPE_TEST_MODE_HCLK

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_TEST_MODE_HCLK register selects the test points for the specified VPE block.

VPE_TEST_MODE_HCLK

Bits	Name	Description
31:7	RESERVED_BITS31_7	This field has no function and should be set to zero for future compatibility.
6:4	BLOCK_ID	These bits select the test points for the specified VPE block into the test bus. 0x0: Disabled 0x1: MDDI1 0x2: MDDI2 0x3: AHBM
3:0	TEST_PT_SEL	These bits select a set of 32-bit test points within a VPE block.

0x053D0104 VPE_TEST_MISR_RESET_HCLK

Type: Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_TEST_MISR_RESET_HCLK is used to reset the MISR state.

VPE_TEST_MISR_RESET_HCLK

Bits	Name	Description
31:1	RESERVED_BITS31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_SW_RESET	A write of '1' to this address will reset the MISR state. It is a self clearing reset. The reset must be asserted after VPE_TEST_MISR_MODE_HCLK is set to a non-zero value. 0x1: MISR reset.

0x053D0108 VPE_TEST_EXPORT_MISR_HCLK

Type: Read-Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_TEST_EXPORT_MISR_HCLK register controls what is sent on the testbus. A value of '0' (reset value) will send the data that is going into the MISR on the testbus. A value of '1' will send the current MISR state onto the testbus. The latter option is typically used for debug purposes. For example, if your final MISR signature failed, you might want to know where it failed (i.e., right in the beginning or somewhere else).

VPE_TEST_EXPORT_MISR_HCLK

Bits	Name	Description
31:1	RESERVED_BITS31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., What is the result of the MUXing of all the input data streams with VPE_TEST_MODE_HCLK) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x053D010C VPE_TEST_MISR_CURR_VAL_HCLK

Type: Read-Only
Clock: CC_VPE_CLK
Reset State: Undefined

A read of the address in the VPE_TEST_MISR_CURR_VAL_HCLK register will return the current MISR state for this block. Keep in mind that this could change every cycle depending on how it is used.

VPE_TEST_MISR_CURR_VAL_HCLK

Bits	Name	Description
31:0	MISR_VAL	This field holds the current MISR state.

0x053D0200 VPE_TEST_MODE_DCLK

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_TEST_MODE_DCLK register selects the test points for the specified VPE block.

VPE_TEST_MODE_DCLK

Bits	Name	Description
31:7	RESERVED_BITS31_7	This field has no function and should be set to zero for future compatibility.

VPE_TEST_MODE_DCLK (cont.)

Bits	Name	Description
6:4	BLOCK_ID	These bits select the test points for the specified VPE block into the test bus. 0x0: Disabled 0x1: LCDC
3:0	TEST_PT_SEL	These bits select a set of 32-bit test points within a VPE block.

0x053D0204 VPE_TEST_MISR_RESET_DCLK

Type: Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_TEST_MISR_RESET_DCLK is used to reset the MISR state.

VPE_TEST_MISR_RESET_DCLK

Bits	Name	Description
31:1	RESERVED_BITS31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_SW_RESET	A write of '1' to this address will reset the MISR state. It is a self clearing reset. The reset must be asserted after VPE_TEST_MISR_MODE_DCLK is set to a non-zero value. 0x1: MISR reset.

0x053D0208 VPE_TEST_EXPORT_MISR_DCLK

Type: Read-Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

The VPE_TEST_EXPORT_MISR_DCLK register controls what is sent on the testbus. A value of '0' (reset value) will send the data that is going into the MISR on the testbus. A value of '1' will send the current MISR state onto the testbus. The latter option is typically used for debug purposes. For example, if your final MISR signature failed, you might want to know where it failed (i.e., right in the beginning or somewhere else')

VPE_TEST_EXPORT_MISR_DCLK

Bits	Name	Description
31:1	RESERVED_BITS31_1	This field has no function and should be set to zero for future compatibility.

VPE_TEST_EXPORT_MISR_DCLK (cont.)

Bits	Name	Description
0	MISR_EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., What is the result of the MUXing of all the input data streams with VPE_TEST_MODE_DCLK) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x053D020C VPE_TEST_MISR_CURR_VAL_DCLK

Type: Read-Only
Clock: CC_VPE_CLK
Reset State: Undefined

A read from this address will return the current MISR state for this block. Keep in mind that this could change every cycle depending on how it is used.

VPE_TEST_MISR_CURR_VAL_DCLK

Bits	Name	Description
31:0	MISR_VAL	This field holds the current MISR state.

0x053D0210 VPE_TEST_CAPTURED_DCLK

Type: Read-Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is set to 1 by hardware when a capture strobe is sent to the MISR. If the micro reads a '1' from this register, it means that it can read the captured MISR value from VPE_TEST_CAPT_MISR_VAL_DCLK register. The microprocessor can write a '0' into this register to clear it.

VPE_TEST_CAPTURED_DCLK

Bits	Name	Description
31:1	RESERVED_BITS31_1	This field has no function and should be set to zero for future compatibility.
0	MISR_EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., What is the result of the MUXing of all the input data streams with VPE_TEST_MODE_DCLK) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x053D0214 VPE_TEST_MISR_CAPT_VAL_DCLK

Type: Read-Only
Clock: CC_VPE_CLK
Reset State: Undefined

A read from this address will return the captured MISR state for this block

VPE_TEST_MISR_CAPT_VAL_DCLK

Bits	Name	Description
31:0	MISR_VAL	This field holds the captured MISR state.

14.16.13 LCDC registers

0x053E0000 VPE_LCDC_EN

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_EN register is used to enable the LCD controller.

VPE_LCDC_EN

Bits	Name	Description
31:1	RESERVED_BITS31_1	This field has no function and should be set to zero for future compatibility.
0	LCDC_EN	Enable timing generation and kick start LCDC operation. Note: If LCDC is disabled by SW in the middle of a frame period, internally the hardware will disable LCDC only at the end of the current frame (just before next Vsync).

0x053E0004 VPE_LCDC_HSYNC_CTL

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_HSYNC_CTL register defines HSYNC parameters like period and width.

VPE_LCDC_HSYNC_CTL

Bits	Name	Description
31:28	RESERVED_BITS31_28	This field has no function and should be set to zero for future compatibility.
27:16	HSYNC_PERIOD	HSYNC period in dot_clk cycles. This is the time between start of hsync pulse and the start of next hsync pulse. Note: hsync_period = Width + h_porch where, Width = Output image width h_porch = (h_back_porch + h_front_porch) h_back_porch starts at the beginning of hsync pulse Please refer to the panel data sheet or VESA specs to obtain accurate values for hsync parameters.
15:12	RESERVED_BITS15_12	This field has no function and should be set to zero for future compatibility
11:0	HSYNC_PULSE_WIDTH	HSYNC pulse width in dot_clk cycles.

0x053E0008 VPE_LCDC_VSYNC_PERIOD

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_VSYNC_PERIOD register defines the VSYNC period.

VPE_LCDC_VSYNC_PERIOD

Bits	Name	Description
31:24	RESERVED_BITS31_24	This field has no function and should be set to zero for future compatibility.

VPE_LCDC_VSYNC_PERIOD (cont.)

Bits	Name	Description
23:0	VSYNC_PERIOD	VSYNC period in dot_clk cycles. This is the time between start of vsync pulse and the start of next vsync pulse. Note: vsync_period = Height + v_porch where, Height = Output image height v_porch = (v_back_porch + v_front_porch) v_back_porch starts at the beginning of vsync pulse Please refer to the panel data sheet or VESA specs to obtain accurate values for vsync parameters.

0x053E000C VPE_LCDC_VSYNC_PULSE_WIDTH

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_VSYNC_PULSE_WIDTH register defines the VSYNC pulse width.

VPE_LCDC_VSYNC_PULSE_WIDTH

Bits	Name	Description
31:24	RESERVED_BITS31_24	This field has no function and should be set to zero for future compatibility.
23:0	VSYNC_PULSE_WIDTH	VSYNC pulse width in dot_clk cycles.

0x053E0010 VPE_LCDC_DISPLAY_HCTL

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_DISPLAY_HCTL register defines the horizontal display region (active + inactive) which can be obtained from hsync period and horizontal blanking (back and front porch) parameters.

VPE_LCDC_DISPLAY_HCTL

VPE_LCDC_DISPLAY_HCTL

Bits	Name	Description
31:28	RESERVED_BITS31_28	This field has no function and should be set to zero for future compatibility
27:16	DISPLAY_END_X	Defines the time period between the start of hsync pulse and the last displayed pixel position in dot_clk cycles. Note: display_end_x = hsync_period - h_front_porch - 1 where, h_porch (dot cycles) = hsync_period - Width h_porch = (h_back_porch + h_front_porch)
15:12	RESERVED_BITS15_12	This field has no function and should be set to zero for future compatibility
11:0	DISPLAY_START_X	Defines the time period between the start of hsync pulse and the first displayed pixel position in dot_clk cycles. Note: display_start_x = h_back_porch where, h_porch (dot cycles) = hsync_period - Width h_porch = (h_back_porch + h_front_porch)

0x053E0014 VPE_LCDC_DISPLAY_V_START

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_DISPLAY_V_START register defines the vertical display region (active + inactive) which can be obtained from vsync period and vertical blanking (back and front porch) parameters.

VPE_LCDC_DISPLAY_V_START

Bits	Name	Description
31:24	RESERVED_BITS31_24	This field has no function and should be set to zero for future compatibility
23:0	DISPLAY_START_Y	Defines the time period between the start of vsync pulse and the first displayed line position in dot_clk cycles. Note: display_start_y = v_back_porch where, v_porch = vsync_period - Height v_porch = (v_back_porch + v_front_porch)

0x053E0018 VPE_LCDC_DISPLAY_V_END

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_DISPLAY_V_END register defines the vertical display region (active + inactive) which can be obtained from vsync period and vertical blanking (back and front porch) parameters.

VPE_LCDC_DISPLAY_V_END

Bits	Name	Description
31:24	RESERVED_BITS31_24	This field has no function and should be set to zero for future compatibility
23:0	DISPLAY_END_Y	Defines the time period between the start of vsync pulse and the last displayed line position in dot_clk cycles. Note: display_end_y = vsync_period - v_front_porch - 1 where, v_porch = vsync_period - Height v_porch = (v_back_porch + v_front_porch)

0x053E001C VPE_LCDC_ACTIVE_HCTL

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_ACTIVE_HCTL register defines the horizontal parameters of LCDC active display area.

VPE_LCDC_ACTIVE_HCTL

Bits	Name	Description
31	ACTIVE_H_EN	Horizontal active region enable
30:28	RESERVED_BITS30_28	This field has no function and should be set to zero for future compatibility
27:16	ACTIVE_END_X	Defines the time period between the start of hsync pulse and the last active pixel position in dot_clk cycles (a value between 'display_start_x' and 'display_end_x').

VPE_LCDC_ACTIVE_HCTL (cont.)

Bits	Name	Description
15:12	RESERVED_BITS15_12	This field has no function and should be set to zero for future compatibility.
11:0	ACTIVE_START_X	Defines the time period between the start of hsync pulse and the first active pixel position in dot_clk cycles (a value between 'display_start_x' and 'display_end_x').

0x053E0020 VPE_LCDC_ACTIVE_V_START

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_ACTIVE_V_START register defines the vertical parameters of LCDC active display area.

VPE_LCDC_ACTIVE_V_START

Bits	Name	Description
31	ACTIVE_V_EN	Vertical active region enable
30:24	RESERVED_BITS30_24	This field has no function and should be set to zero for future compatibility
23:0	ACTIVE_START_Y	Defines the time period between the start of vsync pulse and the first active line position in dot_clk cycles (a value between 'display_start_y' and 'display_end_y').

0x053E0024 VPE_LCDC_ACTIVE_V_END

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_ACTIVE_V_END register defines the vertical parameters of LCDC active display area.

VPE_LCDC_ACTIVE_V_END

Bits	Name	Description
31:24	RESERVED_BITS31_24	This field has no function and should be set to zero for future compatibility
23:0	ACTIVE_END_Y	Defines the time period between the start of vsync pulse and the last active line position in dot_clk cycles (a value between 'display_start_y' and 'display_end_y').

0x053E0028 VPE_LCDC_BORDER_CLR

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_BORDER_CLR register defines border (inactive) area color for LCD display.

VPE_LCDC_BORDER_CLR

Bits	Name	Description
31:24	RESERVED_BITS31_24	This field has no function and should be set to zero for future compatibility
23:0	BORDER_COLOR	Define 24-bit border (background) color value of the inactive region of display. This color value should be packed loose for parallel LCDC and should match the output format, pack pattern and packing alignment defined in VPE_DMA_P_CONFIG. The border color programmed should be packed tight for MDDI based LCDC.

0x053E002C VPE_LCDC_UNDERFLOW_CTL

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_UNDERFLOW_CTL register defines the displayed color in case of data underflow and enables the auto recovery mechanism.

VPE_LCDC_UNDERFLOW_CTL

Bits	Name	Description
31	ERR_RECOVERY_EN	Enable auto recovery during error conditions like underflow etc. 0x0: Disable 0x1: Enable (default)
30:24	RESERVED_BITS30_24	This field has no function and should be set to zero for future compatibility
23:0	UNDERFLOW_COLOR	Define the 24 bit color value to be displayed in case of underflow. This color value should be packed loose for parallel LCDC and should match the output format, pack pattern and packing alignment defined in VPE_DMA_P_CONFIG. The border color programmed should be packed tight for MDDI based LCDC.

0x053E0030 VPE_LCDC_HSYNC_SKEW

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_HSYNC_SKEW defines the relative skew between HSYNC and VSYNC active edges.

VPE_LCDC_HSYNC_SKEW

Bits	Name	Description
31:12	RESERVED_BITS31_12	This field has no function and should be set to zero for future compatibility
11:0	HSYNC_SKEW	Define the number of dot_clk cycles HSYNC active edge is delayed from VSYNC active edge

0x053E0034 VPE_LCDC_TEST_CTL

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_TEST_CTL controls test pattern generation and defines its parameters.

VPE_LCDC_TEST_CTL

Bits	Name	Description
31	TEST_PATTERN_EN	Enable hardware test pattern generation (color rectangles)
30:16	RESERVED_BITS30_16	This field has no function and should be set to zero for future compatibility
15:8	TPG_VAR1	Color rectangle height (y)
7:0	TPG_VAR0	Color rectangle width (x)

0x053E0038 VPE_LCDC_CTL_POLARITY

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

This register is not used in VPE. Writes to this register has no effect. Reads from this register returns 0.

VPE_LCDC_CTL_POLARITY register defines the polarity of control signals to the LCD panel.

VPE_LCDC_CTL_POLARITY

Bits	Name	Description
31:3	RESERVED_BITS31_3	This field has no function and should be set to zero for future compatibility.
2	DEN_NEG	Data enable polarity 0x0: enable active high (default) 0x1: enable active low
1	VSYNC_NEG	VSYNC polarity: 0x0: VSYNC active high (default) 0x1: VSYNC active low
0	HSYNC_NEG	HSYNC polarity: 0x0: HSYNC active high (default) 0x1: HSYNC active low

14.16.14 mgen2maxi Block Control

0x05300400 VPE_AXI_VERSION

Type: Read
Clock: CC_VPE_CLK
Reset State: 0x0000_001d

mgen2maxi core version.

VPE_AXI_VERSION

Bits	Name	Description
31:8	RESERVED_BITS31_8	Reserved bit(s). Read back zero(s).
7:0	VERSION	Hardware version of the MGEN2MAXI core which is embedded in this core. 0x1D: RESET_VAL

0x05300404 VPE_AXI_XBAR_LIM

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x4210_7070

The maximum number of pending data for each client. The programming of the VPE registers must be done while VPE is idle. I.e after VPE interrupt and before the start of the next frame.

VPE_AXI_XBAR_LIM

Bits	Name	Description
31:31	RESERVED_BITS31_31	Reserved bit(s). Read back zero(s).
30:26	AXI_XBAR_IN_WR_LIM	The maximum number of pending writes. Must be <= the HW parameter that limits the same. Range [0,16]. 0x10: RESET_VAL
25:21	AXI_XBAR_IN_RD_BG_LIM	The maximum number of pending reads from Background Tile Fetch. Must be <= the HW parameter that limits the same. Range [0,16]. 0x10: RESET_VAL
20:16	AXI_XBAR_IN_RD_FG_LIM	The maximum number of pending reads from Frontground Tile Fetch. Must be <= the HW parameter that limits the same. Range [0,16]. 0x10: RESET_VAL
15:15	RESERVED_BITS15_15	Reserved bit(s). Read back zero(s).
14:13	AXI_XBAR_OUT_MAX_WR_BURST	The maximum number of write beats minus 1 allowed on the AXI bus (arbiter outputs). Must be < the HW parameter that limits the same. Range [0,3] 0x3: RESET_VAL
12:8	AXI_XBAR_OUT_WR_LIM	The maximum number of pending writes from each arbiter, 5 bits per arbiter. Must be <= the HW parameter that limits the same. Range [0,16] 0x10: RESET_VAL
7:7	RESERVED_BITS7_7	Reserved bit(s). Read back zero(s).

VPE_AXI_XBAR_LIM (cont.)

Bits	Name	Description
6:5	AXI_XBAR_OUT_MAX_RD_BURST	The maximum number of read beats minus 1 allowed on the AXI bus (arbiter outputs). Must be < the HW parameter that limits the same. Range [0,3] 0x3: RESET_VAL
4:0	AXI_XBAR_OUT_RD_LIM	The maximum number of pending reads from each arbiter, 5 bits per arbiter. Must be <= the HW parameter that limits the same. Range [0,16] 0x10: RESET_VAL

0x05300408 VPE_AXI_ARB_1

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0666

Arbitration control. The programming of the VPE registers must be done while VPE is idle. I.e after VPE interrupt and before the start of the next frame.

VPE_AXI_ARB_1

Bits	Name	Description
31:25	RESERVED_BITS31_25	Reserved bit(s). Read back zero(s).
24:19	AXI_PRIORITY_LIST	A list of client numbers, with the highest priority client number on the left side (MSBs). The total width required is NUM_CLIENTS x clog2(NUM_CLIENTS). For 3 clients, that's 3x2=6 bits. Client Number: 0xA: Background Tile Fetch Read 0x1: Write 0x0: Frontground Tile Fetch Read 0x0: RESET_VAL
18:18	AXI_FIXED_PRIOR_EN	Enables fixed priority arbitration, 1 bit per arbiter. If enabled, the other fields are ignored (non-slave-aware and no consecutive client limit) 0x0: RESET_VAL
17:12	AXI_AREQPRIORITY	Request priority, 2 bits per client. This value is driven onto AXI bus only, not used internally for client arbitration. 0x0: RESET_VAL
11:0	AXI_ATYPE	The value to drive on ATYPE signals, 4 bits per client. For example: 0x48: Normal, Cacheable, Writeback, Write-allocate, Non-shared 0x49: Normal, Cacheable, Writeback, Write-allocate, Shared 0x666: RESET_VAL

0x0530040C VPE_AXI_ARB_2

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

Arbitration control. The programming of the VPE registers must be done while VPE is idle. I.e after VPE interrupt and before the start of the next frame.

VPE_AXI_ARB_2

Bits	Name	Description
31:23	RESERVED_BITS31_23	Reserved bit(s). Read back zero(s).
22:8	AXI_CLIENT_LIM	Client limits, 5 bits per client. For 3 clients, this requires 15 bits. Each client limit is the maximum number of consecutive grants minus 1 to give that client before allowing requests from other clients. This is used for both slave-aware and last-client-granted arbitration, but not fixed priority arbitration. NOTE: A client may receive more consecutive grants if no other clients are making requests to the same arbiter. 0x0: RESET_VAL
7:7	RESERVED_BITS7_7	Reserved bit(s). Read back zero(s).
6:4	AXI_AOOOWR	Out of order enable for writes, 1 bit per client. If zero, the AXI bus and slaves must ensure that all writes from this client are completed in the order they are requested from the client. 0x0: RESET_VAL
3:3	RESERVED_BITS3_3	Reserved bit(s). Read back zero(s).
2:0	AXI_AOOORD	Out of order enable for reads, 1 bit per client. If zero, the AXI bus and slaves must ensure that all reads from that client are completed in the order they are requested from the client. 0x0: RESET_VAL

0x05300410 VPE_AXI_ERROR_CTL

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_f011

AXI error handling control. The programming of the VPE registers must be done while VPE is idle. I.e after VPE interrupt and before the start of the next frame.

VPE_AXI_ERROR_CTL

Bits	Name	Description
31:16	RESERVED_BITS31_16	Reserved bit(s). Read back zero(s).

VPE_AXI_ERROR_CTL (cont.)

Bits	Name	Description
15:12	AXI_WDTIMEOUT_LOG2	This field (shared by all arbiters) contains log2 (write data timeout), i.e., the bit number of the timeout counter which, when 1, will trigger the timeout. For example, 15 here means the timeout is 32768 AXI clock cycles. This field is ignored when AXI_HALT_ON_WDTIMEOUT=0. 0xF: RESET_VAL
11:9	RESERVED_BITS11_9	Reserved bit(s). Read back zero(s).
8:8	AXI_HALT_ON_WDTIMEOUT	1 bit per arb. When set (1), write data timeout is enabled, for AXI safety without write data buffering. If required write data is not provided to AXI within the time limit. 0x0: RESET_VAL
7:5	RESERVED_BITS7_5	Reserved bit(s). Read back zero(s).
4:4	AXI_HALT_ON_WR_ERR	1 bit per arb. When set (1), a write error response from AXI (on bresp) acts like a HALT_REQ and also disables all ARB-XIN interfaces - instead, fake write data to AXI (zero write enables) and discard read data from AXI. SW should wait for HALT_ACK and then reset the core. 0x1: RESET_VAL
3:1	RESERVED_BITS3_1	Reserved bit(s). Read back zero(s).
0:0	AXI_HALT_ON_RD_ERR	1 bit per arb. When set (1), an read error response from AXI (on rresp) acts like a HALT_REQ and also disables all ARB-XIN interfaces - instead, fake write data to AXI (zero write enables) and discard read data from AXI. SW should wait for HALT_ACK and then reset the core. 0x1: RESET_VAL

0x05300414 VPE_AXI_ERROR_INFO

Type: Read
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

AXI error information.

VPE_AXI_ERROR_INFO

Bits	Name	Description
31:17	RESERVED_BITS31_17	Reserved bit(s). Read back zero(s).
16:16	AXI_WDTIMEOUT_HALT	Write data timeout. Remain high until AXI reset. 0x0: RESET_VAL
15:13	RESERVED_BITS15_13	Reserved bit(s). Read back zero(s).

VPE_AXI_ERROR_INFO (cont.)

Bits	Name	Description
12:12	AXI_ERR_TYPE	The type of the last error that occurred. 0x0: axi_rresp 0x1: axi_bresp (has priority over rresp if happen same time) 0x0: RESET_VAL
11:10	RESERVED_BITS11_10	Reserved bit(s). Read back zero(s).
9:8	AXI_ERR_RESP	The value of axi_rresp or axi_bresp when the last error occured. 0x0: RESET_VAL
7:6	RESERVED_BITS7_6	Reserved bit(s). Read back zero(s).
5:4	AXI_ERR_MID	The value on axi_rmid or axi_bmid when the last error occured. 0x0: RESET_VAL
3:0	AXI_ERR_TID	The value on axi_rtid or axi_btid when the last error occured. 0x0: RESET_VAL

0x05300418 VPE_AXI_TEST_CTL

Type: Read/Write
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

AXI test/profiling control. The programming of the VPE registers must be done while VPE is idle. I.e after VPE interrupt and before the start of the next frame.

VPE_AXI_TEST_CTL

Bits	Name	Description
31:29	RESERVED_BITS31_29	Reserved bit(s). Read back zero(s).
28:28	AXI_RD_LAT_REP_EN	1 bit per arb. when enabled, each beat of read data is replaced with the read access latency (of AXI cycles from axi_avalid=1 till read data returned with axi_rvalid=1) 0x0: RESET_VAL
27:25	RESERVED_BITS27_25	Reserved bit(s). Read back zero(s).
24:24	AXI_MISR_RES	1 bit per arb, need to write 1 and then write 0. Make sure it is high for at least 2 clock cycles and then write 0 before frame start. 0x0: RESET_VAL
23:21	RESERVED_BITS23_21	Reserved bit(s). Read back zero(s).
20:20	AXI_MISR_EN	1 bit per arb 0x0: RESET_VAL
19:17	RESERVED_BITS19_17	Reserved bit(s). Read back zero(s).

VPE_AXI_TEST_CTL (cont.)

Bits	Name	Description
16:16	AXI_MISR_WD	1 bit per arb, to select misr input 0x0: read data (coming back from AXI) 0x1: write data (going to AXI) 0x0: RESET_VAL
15:13	RESERVED_BITS15_13	Reserved bit(s). Read back zero(s).
12:12	AXI_CTR_EN	Enable all profiling counters 0x0: RESET_VAL
11:9	RESERVED_BITS11_9	Reserved bit(s). Read back zero(s).
8:8	AXI_CTR_RES	Reset all profiling counters. Make sure it is high for at least 2 clock cycles and then write 0 before frame start. 0x0: RESET_VAL
7:6	RESERVED_BITS7_6	Reserved bit(s). Read back zero(s).
5:4	AXI_TEST_ARB_SEL	Select which arbiter to drive VPE_AXI_TEST_OUT. 0x0: RESET_VAL
3:0	AXI_TEST_OUT_SEL	Select which test data is read via VPE_AXI_TEST_OUT. 0x0: num read bursts (32 bits) 0x1: total read BW (32 bits - up to 68GB) 0x8: max outstanding reads (8 bits) 0x9: avg wait for read accept (10 bits over 128 reads) 0x40: min read latency (16 bits) 0x41: max read latency (16 bits) 0x48: avg read latency (16 bits over 1K read beats) 0x3E8: num write bursts (32 bits) 0x3E9: total write BW (32 bits - up to 68GB) 0x3F2: max outstanding writes (8 bits) 0x3F3: avg wait for write accept (10 bits over 128 writes) 0x44C: MISR signature word 0 0x44D: MISR signature word 1 0x456: MISR signature word 2 0x457: MISR signature word 3 0x0: RESET_VAL

0x0530041C VPE_AXI_TEST_OUT

Type: Read
Clock: CC_VPE_CLK
Reset State: 0x0000_0000

AXI test/profiling data.

VPE_AXI_TEST_OUT

Bits	Name	Description
31:0	AXI_TEST_OUT	The output selected by the *_SEL fields in the VPE_AXI_TEST_CTL reg. This is independent of the test bus, which is not accessible by SW unless other SW registers are created for that purpose. 0x0: RESET_VAL

14.17 MM SS FPB XPU Registers (0x05400000 MMSS_APU_BASE)

This section contains the Multimedia Subsystem FPB XPU registers.

0x05400000+4*n MMSS_FPB_APU_RGn_ACR, n=[0..18]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 00, i.e., a single VMID, full access vs. no access permission type APU. These registers include a single 5 bit "owner" VMID field.

MMSS_FPB_APU_RGn_ACR

Bits	Name	Description
31:26	RESERVED31_26	Reserved.
25	RESERVED25	Reserved
24	RESERVED24	Reserved
23:21	RESERVED23_21	Reserved
20:16	RESERVED20_16	Reserved
15:10	RESERVED15_10	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | APU_APU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a "valid" bit for the RWVMID field
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies "owner" VMID with full read/write access to the registers in the associated resource group.

0x05400F80 MMSS_FPB_APU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

MMSS_FPB_APU_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set APU_ESR. APU_EAR and APU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set APU_ESR. APU_EAR and APU_ESYNR0 updated with address and syndrome of error.
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x05400F84 MMSS_FPB_APU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port.

MMSS_FPB_APU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x05400F88 MMSS_FPB_APU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the APU_ESYNRn registers, which are merely the "syndrome" of an error indicated by APU_ESR.

MMSS_FPB_APU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x05400F8C MMSS_FPB_APU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

MMSS_FPB_APU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x05400F90 MMSS_FPB_APU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

MMSS_FPB_APU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x05400F94 MMSS_FPB_APU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

MMSS_FPB_APU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x05400FF4 MMSS_FPB_APU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

MMSS_FPB_APU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved

MMSS_FPB_APU_REV (cont.)

Bits	Name	Description
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x05400FF8 MMSS_FPB_APU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x00001012

APU ID Register: Read-only register that defines various configuration attributes of the APU instance.

MMSS_FPB_APU_IDR

Bits	Name	Description
31:29	RESERVED31_21	Reserved
28:24	MSB	Indicates most significant address bit number used to select a resource group
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.

MMSS_FPB_APU_IDR (cont.)

Bits	Name	Description
9	RESERVED9	Reserved
8:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

0x05400FFC MMSS_FPB_APU_APU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

APU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the APU (including the APU_APU_ACR itself).

MMSS_FPB_APU_APU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the APU's 4KB address region (including the APU_APU_ACR itself). For single VMID type APUs (APU_IDR[MV] = 0) the APU_APU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

14.18 MM SS System FPB Registers (0x05700000 MMSS_SFPB_CFG_BASE)

This section contains the System FPB registers.

14.18.1 Configuration registers

0x05700000 MMSS_SFPB_CTRL_STATUS

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000

The SFPB_CTRL_STATUS register is a general configuration register.

MMSS_SFPB_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables Power up value is clear (0)
11	RPM_ARM7_IRQ_EN	SW: RW, HW: R ARM7InterruptEnable When set, the ARM7 receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	SC_IRQ_EN	SW: RW, HW: R ScorpionInterruptEnable When set, the Scorpion receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

MMSS_SFPB_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x7: Select the M0 ahb2ahb bridge test bus.

0x05700044 MMSS_SFPB_PORT_EN

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFF

The SFPB_PORT_EN register is a SFPB master port enable register.

MMSS_SFPB_PORT_EN

Bits	Name	Description
31:1	RESERVED_BIT31_1	
0	M0_PORT_EN	SW:RW, HW:R M0PortEnable When cleared (0), M0 bridge is prevented from arbitting on the system_fpb bus. Power up value is set(1)

14.18.2 Bus error registers and additional configure registers

0x05700050 MMSS_SFPB_ERROR_STAT

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000000

The SFPB_ERROR_STAT register is the bus error status register.

MMSS_SFPB_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the channel ID that caused the detected error when CID is valid for the master of the access. If not, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Master0
11:10	RESERVED_BITS11_10	
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit
3:2	RESERVED_BIT3_2	

MMSS_SFPB_ERROR_STAT (cont.)

Bits	Name	Description
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted. Clearing (0) this bit clears any interrupts asserted as well as enables the SFPB_ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x05700054 MMSS_SFPB_ERROR_ADDR

Type: Read
Clock: CC_SFPB_CLK
Reset State: 0x00000000

The SFPB_ERROR_ADDR register contains the bus error address.

MMSS_SFPB_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when SFPB_ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x05700058 MMSS_SFPB_GPREG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000

The SFPB_GPREG register is a configurable general purpose register.

MMSS_SFPB_GPREG

Bits	Name	Description
16:13	MMSS_AHB_ARB_DEF_MASTER	SW:RW, HW:R Default Master configuration to MMSS AHB Arbiter It contains 4bits, Only Master 0 and Master 1 are available for support for now as there are only 2 masters hooked-up. others - Reserved (should be written with 0) This also helps in changing the default master when a master port is disabled and avoiding any un-necessary hgrant assertion to disabled default master. 0x0: Master 0 is default master 0x1: Master 1 is default master
12:11	MMSS_AHB_ARB_MATER_PORT_EN	SW:RW, HW:R SW configured master port enable Bit 0 is dedicated to enable/disable the MMSS AHB Arbiter Master0 request. Bit1 is dedicated to enable/disable the MMSS AHB Arbiter Master1 request. 0x1: Enable 0x0: DisableWhen Disabled, Arbiter will not see the HBUSREQ coming from the master, as it is blocked by this bit.
10	FABRIC_TIMEOUT_EN	SW:RW, HW:R This bit enables the use of the timeout register. 0x0: watchdog timer for ahb2msm bus is disabled. This is the default value after reset. The ahb2msm bus inside mmss_fpb will hang the bus if it is not able to respond to ahb request. 0x1: watchdog timer for ahb2msm bus is enabled. The register defined below will set the counter, after which the bus will issue error response.
9:2	FABRIC_TIMEOUT_VAL	SW:RW, HW:R These 8 bits set the value for the timeout register. This register sets the number of cycles after which the ahb2msm bus will issue a error response if it is not able to respond to the ahb request and it will not hang the bus after the programmed number of clock cycles. The default value of this register is 00001111 after reset. also bits 5:2 are inverted. If you program this register to 00001001, you are setting the timeout_val for msm_bus to be 00000110. 0xF: upon reset
1:0	MMSS_TESTBUS_SELECTION	SW:RW, HW:R This bit selects what value to be driven on the MMSS test bus (sfpb_mmss_test_bus). 0x0: 00000000 0x1: AAAAAAAA 0x2: 55555555 0x3: Drives MMSS Internal test bus onto sfpb_mmss_test_bus

0x0570005C MMSS_SFPB_XPU_ACR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFFFFFF

The SFPB_XPU_ACR register is a SFPB Access Control Register for configure register protection.

MMSS_SFPB_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R SFPB XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the SFPB configure space, including this register itself. Power up value is set (1)

0x05700060 MMSS_SFPB_HW_CLK_GATING_CFG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0000

The SFPB_HW_CLK_GATING_CFG register is for hardware clock gating configuration register.

MMSS_SFPB_HW_CLK_GATING_CFG

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	HYSTERESIS_CNT_SW	SW: RW, HW: R Hysteresis Conter Value The value of this field is for SW to set the hysteresis counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)
3:0	WAKE_CNT_SW	SW: RW, HW: R Wakeup Conter Value The value of this field is for SW to set the wakeup counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)

14.19 VCAP Registers (0x05900000 VCAP_BASE)

This section contains the VCAP registers.

0x05900000 VCAP_VCAP_HW_VERSION

Type: Read
Clock: UNDEFINED
Reset State: 0x10000000

VCAP_SYS block HW Version

VCAP_VCAP_HW_VERSION

Bits	Name	Description
31:28	MAJOR	READ ONLY Major Version 1
27:16	MINOR	READ ONLY Minor Version 0
15:0	STEP	READ ONLY Step Version 0

0x05900004 VCAP_VCAP_INT_STATUS

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Interrupt Status for VCAP_VC interrupt. VCAP module has 3 major interrupts (VC, VP and VBIF). VP(I2P) interrupt has its own interrupt signal, so this register doesn't include it. VCA_VC interrupt signal includes VCAP_VC and VBIF. Interrupt clear/mask are not in this space and they are each sub block’s register space.

VCAP_VCAP_INT_STATUS

Bits	Name	Description
31:5	UNUSED_1	
4	VCAP_VBIF_INTERRUT_STATUS	READ ONLY Indicates VBIF interrupt occurs
3:1	UNUSED_2	
0	VCAP_VC_INTERRUT_STATUS	READ ONLY Indicates VC interrupt occurs

0x05900010 VCAP_VCAP_VC_CLK_CTRL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x03010301

VCAP_VC module's clock control register.

VCAP_VC has upper pipe and lower pipe. Clock for upper pipe should be always on when VCAP_VC is enabled while lower pipe clock can be dynamically controlled.

VC0 is connected to upper pipe and VC1 is connected to lower pipe.

VCAP_VCAP_VC_CLK_CTRL

Bits	Name	Description
31:26	UNUSED_1	
25:24	VC1_STRETCH	This registers defines the number of extra active clock cycles when clock is halted. - 0x0 : 2 clock cycles - 0x1 : 4 clock cycles - 0x2 : 8 clock cycles - 0x3 : 16 clock cycles
23:21	UNUSED_2	
20	VC1_FORCE_OFF	If this register is set, clock is turned off and this register takes precedence over FORCE_ON.
19:17	UNUSED_3	
16	VC1_FORCE_ON	If this register is set, clock is turned on
15:10	UNUSED_4	
9:8	VC0_STRETCH	This registers defines the number of extra active clock cycles when clock is halted. - 0x0 : 2 clock cycles - 0x1 : 4 clock cycles - 0x2 : 8 clock cycles - 0x3 : 16 clock cycles
7:5	UNUSED_5	
4	VC0_FORCE_OFF	If this register is set, clock is turned off and this register takes precedence over FORCE_ON.
3:1	UNUSED_6	
0	VC0_FORCE_ON	If this register is set, clock is turned on

0x05900014 VCAP_VCAP_VP_CLK_CTRL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x03010301

VCAP_VP(I2P) module's clock control register.

VCAP_VP has upper pipe and lower pipe. Clock for upper pipe should be always on when VCAP_VP is enabled while lower pipe clock can be dynamically controlled.

VP0 is connected to upper pipe and VP1 is connected to lower pipe.

VCAP_VCAP_VP_CLK_CTRL

Bits	Name	Description
31:26	UNUSED_1	
25:24	VP1_STRETCH	This registers defines the number of extra active clock cycles when clock is halted. - 0x0 : 2 clock cycles - 0x1 : 4 clock cycles - 0x2 : 8 clock cycles - 0x3 : 16 clock cycles
23:21	UNUSED_2	
20	VP1_FORCE_OFF	If this register is set, clock is turned off and this register takes precedence over FORCE_ON.
19:17	UNUSED_3	
16	VP1_FORCE_ON	If this register is set, clock is turned on
15:10	UNUSED_4	
9:8	VP0_STRETCH	This registers defines the number of extra active clock cycles when clock is halted. - 0x0 : 2 clock cycles - 0x1 : 4 clock cycles - 0x2 : 8 clock cycles - 0x3 : 16 clock cycles
7:5	UNUSED_5	
4	VP0_FORCE_OFF	If this register is set, clock is turned off and this register takes precedence over FORCE_ON.
3:1	UNUSED_6	
0	VP0_FORCE_ON	If this register is set, clock is turned on

0x05900018 VCAP_VCAP_VBIF_CLK_CTRL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x03010301

VCAP VBIF has two client interfaces which are VCAP clock domain. One is driven by VCAP_VC and the other is driven by VCAP_VP. This register controls these two clocks.

VCAP_VCAP_VBIF_CLK_CTRL

Bits	Name	Description
31:26	UNUSED_1	
25:24	VP_VBIF_STRETCH	This registers defines the number of extra active clock cycles when clock is halted. - 0x0 : 2 clock cycles - 0x1 : 4 clock cycles - 0x2 : 8 clock cycles - 0x3 : 16 clock cycles
23:21	UNUSED_2	
20	VP_VBIF_FORCE_OFF	If this register is set, clock is turned off and this register takes precedence over FORCE_ON.
19:17	UNUSED_3	
16	VP_VBIF_FORCE_ON	If this register is set, clock is turned on
15:10	UNUSED_4	
9:8	VC_VBIF_STRETCH	This registers defines the number of extra active clock cycles when clock is halted. - 0x0 : 2 clock cycles - 0x1 : 4 clock cycles - 0x2 : 8 clock cycles - 0x3 : 16 clock cycles
7:5	UNUSED_5	
4	VC_VBIF_FORCE_OFF	If this register is set, clock is turned off and this register takes precedence over FORCE_ON.
3:1	UNUSED_6	
0	VC_VBIF_FORCE_ON	If this register is set, clock is turned on

0x0590001C VCAP_VCAP_CMN_CLK_CTRL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x03010301

VCAP has system clock domain as well as event clock domain. System clock is for register/timestamp logic and event clock is for test/debug bus

VCAP_VCAP_CMN_CLK_CTRL

Bits	Name	Description
31:26	UNUSED_1	
25:24	EVENT_STRETCH	This registers defines the number of extra active clock cycles when clock is halted. - 0x0 : 2 clock cycles - 0x1 : 4 clock cycles - 0x2 : 8 clock cycles - 0x3 : 16 clock cycles
23:21	UNUSED_2	
20	EVENT_FORCE_OFF	If this register is set, clock is turned off and this register takes precedence over FORCE_ON.
19:17	UNUSED_3	
16	EVENT_FORCE_ON	If this register is set, clock is turned on
15:10	UNUSED_4	
9:8	SYS_STRETCH	This registers defines the number of extra active clock cycles when clock is halted. - 0x0 : 2 clock cycles - 0x1 : 4 clock cycles - 0x2 : 8 clock cycles - 0x3 : 16 clock cycles
7:5	UNUSED_5	
4	SYS_FORCE_OFF	If this register is set, clock is turned off and this register takes precedence over FORCE_ON.
3:1	UNUSED_6	
0	SYS_FORCE_ON	If this register is set, clock is turned on

0x05900020 VCAP_VCAP_CLK_STATUS

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

This status register indicates each clock is active or not.

- 0x0 : Clock is idle

- 0x1 : Clock is active

VCAP_VCAP_CLK_STATUS

Bits	Name	Description
31	UNUSED_1	
30	AHB_EVENT_CLK_ACTIVE	READ ONLY AHB_EVENT_CLK status
29	AXI_EVENT_CLK_ACTIVE	READ ONLY AXI_EVENT_CLK status
28	VCAP_EVENT_CLK_ACTIV E	READ ONLY VCAP_EVENT_CLK status
27:25	UNUSED_2	
24	VCAP_SYS_CLK_ACTIVE	READ ONLY VCAP_SYS_CLK status
23:21	UNUSED_3	
20	VP_VBIF_CLK_ACTIVE	READ ONLY VP_VBIF_CLK status
19:17	UNUSED_4	
16	VC_VBIF_CLK_ACTIVE	READ ONLY VC_VBIF_CLK status
15:13	UNUSED_5	
12	VCAP_VP1_CLK_ACTIVE	READ ONLY VCAP_VP1_CLK status
11:9	UNUSED_6	
8	VCAP_VP0_CLK_ACTIVE	READ ONLY VCAP_VP0_CLK status
7:5	UNUSED_7	
4	VCAP_VC1_CLK_ACTIVE	READ ONLY VCAP_VC1_CLK status
3:1	UNUSED_8	
0	VCAP_VC0_CLK_ACTIVE	READ ONLY VCAP_VC0_CLK status

0x05900024 VCAP_VCAP_SW_RESET_REQ

Type: Write
Clock: UNDEFINED
Reset State: 0x00000000

VCAP supports SW reset for VCAP_VC/VCAP_VP modules which are AXI interface client. So, SW reset handshaking mechanism should be implemented to make sure there is no pending AXI transactions in VBIF.

SW reset sequence.

- 1. Set VCAP_SW_RESET_REQ for each module.

- 2. Poll corresponding VCAP_SW_RESET_STATUS bit is 0

- 3. Reprogramming if it is required.

VCAP_VC SW registers are not reset by SW_RESET but

VCAP_VP SW registers are reset by SW_RESET.

VCAP_VCAP_SW_RESET_REQ

Bits	Name	Description
31:5	UNUSED_1	
4	VCAP_VP_SW_RESET_REQ	WRITE ONLY Generate SW reset triggering signal for VCAP_VP module.
3:1	UNUSED_2	
0	VCAP_VC_SW_RESET_REQ	WRITE ONLY Generate SW reset triggering signal for VCAP_VP module.

0x05900028 VCAP_VCAP_SW_RESET_STATUS

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

This register indicates SW reset request status.

- 0x0 : SW reset sequence is completed or idle

- 0x1 : SW reset sequence is in progress

VCAP_VCAP_SW_RESET_STATUS

Bits	Name	Description
31:5	UNUSED_1	
4	VCAP_VP_SW_RESET_STATUS	READ ONLY VCAP_VP SW reset status
3:1	UNUSED_2	
0	VCAP_VC_SW_RESET_STATUS	READ ONLY VCAP_VC SW reset status

0x05900030 VCAP_VCAP_TIMESTAMP_REG1

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP captures timestamp value that is from LPASS for Audio/Video synchronization purpose. This register is first level timestamp value

VCAP_VCAP_TIMESTAMP_REG1

Bits	Name	Description
31:0	TIMESTAMP_VALUE	READ ONLY This register captures LPASS timestamp value when vsync is coming from external HDMI receiver

0x05900034 VCAP_VCAP_TIMESTAMP_REG2

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP captures timestamp value that is from LPASS for Audio/Video synchronization purpose. This register is second level timestamp value

VCAP_VCAP_TIMESTAMP_REG2

Bits	Name	Description
31:0	TIMESTAMP_VALUE	READ ONLY This register captures VCAP_TIMESTAMP_REG1 value when frame done interrupt is coming from VCAP_VC module

0x05900040 VCAP_VCAP_VC_VBIF_CTRL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Control VCAP_VC’s VBIF client interface signals

VCAP_VCAP_VC_VBIF_CTRL

Bits	Name	Description
31:9	UNUSED_1	

VCAP_VCAP_VC_VBIF_CTRL (cont.)

Bits	Name	Description
8	VC_CPRIV	AXI Privileged/User attribute on AXI I/F ports dynamically. Indicates if the transaction is user versus privileged mode access. Used to determine access permissions to the MMU.If the signal is asserted, it indicates a privileged mode access
7:6	UNUSED_2	
5:4	VC_CPRIORITYLVL	Request priority Level signal. In APQ8064 project, this feature has not been implemented in VBIF.
3:2	UNUSED	
1:0	VC_CREQPRIORITY	Request priority signal on AXI I/F ports - 2'b00 : the lowest priority level - 2'b11 : the highest priority level

0x05900044 VCAP_VCAP_VP_VBIF_CTRL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Control VCAP_VP's VBIF client interface signals

VCAP_VCAP_VP_VBIF_CTRL

Bits	Name	Description
31:9	UNUSED_1	
8	VP_CPRIV	AXI Privileged/User attribute on AXI I/F ports dynamically. Indicates if the transaction is user versus privileged mode access. Used to determine access permissions to the MMU. If the signal is asserted, it indicates a privileged mode access
7:6	UNUSED_2	
5:4	VP_CPRIORITYLVL	Request priority Level signal. In APQ8064 project, this feature has not been implemented in VBIF.
3:2	UNUSED	
1:0	VP_CREQPRIORITY	Request priority signal on AXI I/F ports - 2'b00 : the lowest priority level - 2'b11 : the highest priority level

0x05900048 VCAP_VCAP_VBIF_CLIENT_STATUS

Type: Read
Clock: UNDEFINED
Reset State: 0x00001111

VBIF client interface status.

Note: Whenever VCAP_I2P_INTERRUPT_STATUS.PICTURE_DONE occurs, SW should check this register's bit 8 is 1. PICTURE_DONE status means picture processing is done from I2P core perspective, it doesn't mean memory writes are passed out VCAP core. In order to make sure memory write is actually done, SW should check VP_WRITES_DONE status bit. VCAP_VC's interrupt status reflects VBIF write done status so SW does not need to check this status bit but SW should check this status for VCAP_VP's interrupt since I2P design (external IP) cannot be modified.

VCAP_VCAP_VBIF_CLIENT_STATUS

Bits	Name	Description
31:13	UNUSED_1	
12	VP_READS_DONE	READ ONLY VCAP_VP read request status. - 0x0 : Read is still progressing. - 0x1 : There is not any pending read request
11:9	UNUSED_2	
8	VP_WRITES_DONE	READ ONLY VCAP_VP write request status. - 0x0 : Write is still progressing. - 0x1 : There is not any pending write request
7:5	UNUSED_3	
4	VC_READS_DONE	READ ONLY VCAP_VC read request status. VCAP_VC doesn't have read functionality, so it should be always 1. - 0x0 : Read is still progressing. - 0x1 : There is not any pending read request
3:1	UNUSED_4	
0	VC_WRITES_DONE	READ ONLY VCAP_VC write request status. - 0x0 : Write is still progressing. - 0x1 : There is not any pending write request

0x05900100 VCAP_VCAP_DEBUGBUS_CTRL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Debug bus control

VCAP_VCAP_DEBUGBUS_CTRL

Bits	Name	Description
31:28	VBIF_TEST_BUS2_DATA_SEL	vbif_test_bus2_data_sel to determine which data stream to output on debugbus
27	UNUSED_1	
26	VBIF_TEST_BUS2_ARB_EN	vbif_test_bus2_arb_en to enable the arbiter selection
25:24	VBIF_TEST_BUS2_XIN_EN	vbif_test_bus2_xin_en selects one XIN block with signals belonging to AXI clock VBIF_TEST_BUS2_DATA_SEL selects which data to output
23:20	VBIF_TEST_BUS1_DATA_SEL	vbif_test_bus1_data_sel : to select which data stream to output on debugbus
19:18	UNUSED_2	
17:16	VBIF_TEST_BUS1_XIN_EN	vbif_test_bus1_xin_en to select one XIN block with signals which corresponds to VCAP_CLK
15:14	VBIF_AHB_TEST_BUS_EN	vbif_ahb_test_bus_en
13:12	AHB2AHB_TEST_BUS_EN	ahb2ahb_test_bus connection
11:10	UNUSED_3	
9:4	DEBUGBUS_SEL	Debug bus select. 0-29 I2P debug signals, 30-39 - AXI debug signals, 40, 41 - AHB debug signals, 43-63 - VC debug signals, Programming this field to 0x3D will output fixed pattern
3:1	UNUSED_4	
0	DEBUGBUS_EN	Enable DebugBus. 0 = disable, 1=enable

0x05900104 VCAP_VCAP_DEBUGBUS

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Debug bus status

VCAP_VCAP_DEBUGBUS

Bits	Name	Description
31:0	DEBUGBUS	READ ONLY Debug bus read only field. Along with the debug bus going out of vcap, the bus status can be read here as well

14.19.1 VCAP_I2P SWI Register Set

VCAP_I2P Registers

0x05900400 VCAP_VCAP_I2P_OUTPUT_STATUS

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

output status

VCAP_VCAP_I2P_OUTPUT_STATUS

Bits	Name	Description
31	CORE_ACTIVE	READ ONLY - 0: core inactive 1:core active
30:27	UNUSED_1	
26:16	OUTPUT_ROW_MIN1	READ ONLY current row being output
15:11	UNUSED_2	
10:0	OUTPUT_COLUMN_MIN1	READ ONLY current horizontal offset being output

0x05900404 VCAP_VCAP_I2P_INTERRUPT_STATUS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

interrupt status

VCAP_VCAP_I2P_INTERRUPT_STATUS

Bits	Name	Description
31:26	UNUSED_1	

VCAP_VCAP_I2P_INTERRUPT_STATUS (cont.)

Bits	Name	Description
25	REGISTER_READ_ERROR	- 1 if register read from invalid address
24	REGISTER_WRITE_ERROR	- 1 if register write to invalid address
23:21	UNUSED_2	
20	OUTPUT_UNDERFLOW_ERROR	if direct video out is used, if output interface is starved of data due a stall in i2p gc
19	UNUSED_3	
18	INPUT_OVERFLOW_ERROR	if direct video input port attempts to input data which is not accepted due to stall in i2p_gc
17	INPUT_HEIGHT_ERROR	- 1: hardware interface input field picture boundary not aligned
16	INPUT_WIDTH_ERROR	- 1: hardware interface input field row boundary not aligned
15:9	UNUSED_4	
8	FILM_MODE_CHANGE	- 1: film mode state / cadence changed
7:2	UNUSED	
1	LAST_CONFIG	- 1: when start picture occurs and (load_new_config=0 or config_base_add=-16)
0	PICTURE_DONE	- 1: picture done. SW needs to check VCAP_VBIF_CLIENT_STATUS.VP_WRITES_DONE status bit if SW really wants to make sure all memory write is done from VCAP level. PICTURE_DONE interrupt is generated when picture is done from I2P core perspective, in other words, there might be pending request in VBIF side.

0x05900408 VCAP_VCAP_I2P_INTERRUPT_ENABLE

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

interrupt enable

VCAP_VCAP_I2P_INTERRUPT_ENABLE

Bits	Name	Description
31:26	UNUSED_1	
25	ENABLE_REGISTER_READ_ERROR	if set, i2p_irq will pulse high whenever register read error occurs
24	ENABLE_REGISTER_WRITE_ERROR	if set, i2p_irq will pulse high whenever register write error occurs
23:21	UNUSED_2	

VCAP_VCAP_I2P_INTERRUPT_ENABLE (cont.)

Bits	Name	Description
20	ENABLE_OUTPUT_UNDERFLOW_ERROR	if set, i2p_irq will pulse high whenever output underflow occurs
19	UNUSED_3	
18	ENABLE_INPUT_OVERFLOW_ERROR	if set, i2p_irq will pulse high whenever input overflow occurs
17	ENABLE_INPUT_HEIGHT_ERROR	if set, i2p_irq will pulse high whenever input height error occurs
16	ENABLE_INPUT_WIDTH_ERROR	if set, i2p_irq will pulse high whenever input width error occurs
15:9	UNUSED_4	
8	ENABLE_FILM_MODE_CHANGE	if set, i2p_irq will pulse high whenever film state or cadenc change
7:2	UNUSED	
1	ENABLE_LAST_CONFIG	if set, i2p_irq will pulse high whenever last config occurs
0	ENABLE_PICTURE_DONE	if set, i2p_irq will pulse high whenever picture done occurs

0x0590040C VCAP_VCAP_I2P_INTERRUPT_CLEAR

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

interrupt clear

VCAP_VCAP_I2P_INTERRUPT_CLEAR

Bits	Name	Description
31:26	UNUSED_1	
25	CLEAR_REGISTER_READ_ERROR	writing a ’1’ clears the status field
24	CLEAR_REGISTER_WRITE_ERROR	writing a ’1’ clears the status field
23:21	UNUSED_2	
20	CLEAR_OUTPUT_UNDERFLOW_ERROR	writing a ’1’ clears the status field
19	UNUSED_3	
18	CLEAR_INPUT_OVERFLOW_ERROR	writing a ’1’ clears the status field

VCAP_VCAP_I2P_INTERRUPT_CLEAR (cont.)

Bits	Name	Description
17	CLEAR_INPUT_HEIGHT_ERROR	writing a ’1’ clears the status field
16	CLEAR_INPUT_WIDTH_ERROR	writing a ’1’ clears the status field
15:9	UNUSED_4	
8	CLEAR_FILM_MODE_CHANGE	writing a ’1’ clears the status field
7:2	UNUSED	
1	CLEAR_LAST_CONFIG	writing a ’1’ clears the status field
0	CLEAR_PICTURE_DONE	writing a ’1’ clears the status field

0x05900410 VCAP_VCAP_I2P_SOFT_RESET

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

soft reset: This SW reset functionality is removed since it breaks AXI operation. VCAP_SW_RESET_REQ.VCAP_VP_SW_RESET_REQ must be used instead of this register

VCAP_VCAP_I2P_SOFT_RESET

Bits	Name	Description
31:1	UNUSED	
0	SOFT_RESET	writing a ’1’ resets I2P_GC core

0x05900414 VCAP_VCAP_I2P_CLOCK_ENABLE

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

clock enable

VCAP_VCAP_I2P_CLOCK_ENABLE

Bits	Name	Description
31:1	UNUSED	
0	FORCE_CLOCK_ENABLE	- 0: auto clock gating is used, 1: force clock to be permanently enabled

0x05900480 VCAP_VCAP_I2P_INPUT_CONFIGURATION

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

input configuration

VCAP_VCAP_I2P_INPUT_CONFIGURATION

Bits	Name	Description
31:29	UNUSED_1	
28	INPUT_CHROMA_HALF_STRIDE	if set, chroma row stride is half luma row stride
27:20	INPUT_ROW_STRIDE	row stride of t(2) luma frame store
19:14	UNUSED_2	
13	INPUT_CHROMA_SIGNED	internal pipeline works on unsigned chroma. If this bit is set, MSb of chroma input will be inverted
12	INPUT_CHROMA_QUASI_422	if set, i2p_gc will read from 4:2:2 source but chroma output to balance logic is processed as if it was 4:2:0
11	INPUT_CHROMA_FORMAT	- 0: chroma_420 input field. 1: chroma_422 input field
10	INPUT_STORE_INTERVEAVED	- 0: field picture store 1: interleaved frame store
9:8	INPUT_STORE_FORMAT	input field store format 00: YUVPL12Y8 YUV PL12 Y8 ’0x0’ = Normal operation (all four input fields used) 01: YUVPL12Y10 YUV PL12 Y10 (10-bit data chroma interleaved) 10: YUVYV12Y8 YUV YV12 Y8 (8-bit data separate chroma planes) 11: YUVYV12Y10 YV12 Y10 (10-bit data separate chroma planes)
7:6	UNUSED_3	
5:4	INPUT_SEQUENCE	’0x1’ = 1st field : output frame is not generated (analysis blocks disabled). If noise reduction is enabled, input field is written to t(-1) without modification. If noise reduction is disabled, and hardware input interface is used, input field written to t(2). ’0x2’ = 2nd field : output frame generated. Field t(2) used in place of t(0), field t(1) used in place of t(-1). Noise reduction block outputs result unmodified. Film mode and motion estimation blocks initialize stores. ’0x3’ = 3rd field : normal operation, with the exception that field t(1) used in place of t(-1)(8-bit data chroma interleaved)
3:1	UNUSED_4	
0	INPUT_HARDWARE_INTERFACE	- 0: t(2) read from memory. 1: t(2) input via hardware interface

0x05900484 VCAP_VCAP_I2P_NOISE_REDUCTION_CONFIGURATION

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

noise reduction configuration

VCAP_VCAP_I2P_NOISE_REDUCTION_CONFIGURATION

Bits	Name	Description
31:28	UNUSED_1	
27:20	NR_ROW_STRIDE	Row stride of t(1), t(0) and t(-1) luma frame store (in 128-bit words, a value of 0 = 4096 byte row stride), if noise reduction is enabled. If noise reduction is disabled, this field isn't used.
19:11	UNUSED_2	
10	NR_STORE_INTERLEAVED	- 0: field picture store. 1: interleaved frame store.if NR is enabled, this field applies to t(1) t(0) t(-1)
9	UNUSED_3	
8	NR_STORE_FORMAT	- 0: YUVPL12Y8 YUV PL12 Y8 (8-bit data chroma interleaved) 1: YUVPL12Y10 YUV PL12 Y10 (10-bit data chroma interleaved)
7:2	UNUSED_4	
1	CYCLE_BUFFERS	If this bit is ’0’, and auto configuration is used, base addresses for nr_t(2), t(1), t(0), and t(-1) will be loaded as part of the auto-configuration process. If this bit is ’0’, and auto-configuration is not used, software is responsible for setting-up base addresses for nr_t(2), t(1), t(0) and t(-1). If this bit is ’1’, and noise reduction is disabled, at the end of a picture (at the same time that picture done interrupt is generated) base address t(0) copied to t(-1) base address t(1) copied to t(0) base address t(2) copied to t(1) If this bit is ’1’, and noise reduction is enabled, at the end of a picture (at the same time that picture done interrupt is generated) base address t(0) copied to t(-1) base address t(1) copied to t(0) base address nr_t(2) copied to t(1) (where at the end of the picture, nr_t(2) will contain noise reduced version of t(2)). If this bit is ’1’, auto-configuration will not load base addresses for t(-1), t(0) or t(1) In 1 field delay mode, t(1)/nr_t(2) copied to t(0), t(-1) is copied to t(-2). In 0 field delay mode, t(0)/nr_t(2) copied to t(-1), t(-2) is copied to t(-3).
0	NOISE_REDUCTION_ENABLE	- 0: noise reduction disabled 1: noise reduction enabled

0x05900488 VCAP_VCAP_I2P_OUTPUT_CONFIGURATION

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

output configuration

VCAP_VCAP_I2P_OUTPUT_CONFIGURATION

Bits	Name	Description
31:29	UNUSED_1	
28	OUTPUT_CHROMA_HALF_STRIDE	If this bit is '1', chroma row stride is half luma row stride (In which case, luma row stride must be multiple of 32-bytes, so that chroma stride is still a multiple of 16-bytes). If this bit is '0', chroma row stride is same as luma row stride
27:20	OUTPUT_ROW_STRIDE	Row stride of output luma frame store (in 128-bit words, a value of 0 = 4096 byte row stride), if output to memory is enabled. If hardware output is used, this field isn't used
19:15	UNUSED_2	
14	OUTPUT_CHROMA_SPATIAL	- 0: interpolate chroma based on luma, 1: force chroma interpolation to spatial only
13	OUTPUT_CHROMA_SIGNED	if this bit is set, MSb of chroma output will be inverted to convert unsigned offset chroma to signed chroma
12	SWAP_CHROMA	if set, chroma order at input (Cb/Cr) will be swapped at output (Cr/Cb)
11	OUTPUT_CHROMA_FORMAT	Defines chroma format of output (if input and output chroma formats are different, balance and filter logic will do the chroma format conversion) 0: CHROMA_420 Output frame 4:2:0 1: CHROMA_422 Output frame 4:2:2
10	UNUSED_3	
9:8	OUTPUT_STORE_FORMAT	- 00: YUVPL12Y8 YUV PL12 Y8 (8-bit data chroma interleaved) 01: YUVPL12Y10 YUV PL12 Y10 (10-bit data chroma interleaved) 10: YUVYV12Y8 YUV YV12 Y8 (8-bit data separate chroma planes) 11: YUVYV12Y10 YV12 Y10 (10-bit data separate chroma planes
7:6	OUTPUT_FIELD_DELAY	defines output field delay 00: 2_FIELD 2 field delay mode 01: 1_FIELD 1 field delay mode 10: 0_FIELD 0 field delay mode 11: RESERVED
5:4	OUTPUT_MODE	Modifies what data is output 00: DISABLED Disable output 01: PROGRESSIVE Output progressive frame (including data from field t0) 10: INTER_FIELD Output only interpolated data, into a field store 11: INTER_FRAME Output only interpolated data, into a frame store
3:1	UNUSED_4	

VCAP_VCAP_I2P_OUTPUT_CONFIGURATION (cont.)

Bits	Name	Description
0	OUTPUT_HARDWARE_INTERFACE	- 0: output to memory. 1: output via hardware interface

0x0590048C VCAP_VCAP_I2P_FRAME_SIZE

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

frame size

VCAP_VCAP_I2P_FRAME_SIZE

Bits	Name	Description
31:27	UNUSED_1	
26:16	FRAME_HEIGHT_MIN1	- 1 less than height of output frame (e.g. setting 1079 = 1080 rows). If frame height is odd (contents of this field even), the input top field will be expected to contain 1 more row than the input bottom field
15:11	UNUSED_2	
10:0	FRAME_WIDTH_MIN1	- 1 less than width of output frame (e.g. setting 1919 = 1920 pixels wide)

0x05900490 VCAP_VCAP_I2P_TM1_LUMA_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

TM1 LUMA BASE Address

VCAP_VCAP_I2P_TM1_LUMA_BASE_ADDRESS

Bits	Name	Description
31:4	TM1_LUMA_BASE_ADDRESS	Defines base address for luma in field t(-1). If noise reduction is enabled, the noise reduced field is also written to this base address (the hardware will always read pixel data for t(-1) before overwriting data with noise reduced version of t(2))
3:0	UNUSED	

0x05900494 VCAP_VCAP_I2P_TM1_CB_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

TM1_CB_BASE_ADDRESS

VCAP_VCAP_I2P_TM1_CB_BASE_ADDRESS

Bits	Name	Description
31:4	TM1_CB_BASE_ADDRESS	Base address for Cb if planar store is used, or both Cb and Cr if interleaved chroma store used, in field t(-1). If noise reduction is enabled, the noise reduced field is also written to this base address (the hardware will always read pixel data for t(-1) before overwriting data with noise reduced version of t(2))
3:0	UNUSED	

0x05900498 VCAP_VCAP_I2P_TM1_CR_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

TM1_CR_BASE_ADDRESS

VCAP_VCAP_I2P_TM1_CR_BASE_ADDRESS

Bits	Name	Description
31:4	TM1_CR_BASE_ADDRESS	Base address for Cr if planar format is used in field t(-1). If noise reduction is enabled, the noise reduced field is also written to this base address (the hardware will always read pixel data for t(-1) before overwriting data with noise reduced version of t(2))
3:0	UNUSED	

0x0590049C VCAP_VCAP_I2P_T0_LUMA_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

T0_LUMA_BASE_ADDRESS

VCAP_VCAP_I2P_T0_LUMA_BASE_ADDRESS

Bits	Name	Description
31:4	T0_LUMA_BASE_ADDRESS	base address for luma in filed t(0)
3:0	UNUSED	

0x059004A0 VCAP_VCAP_I2P_T0_CB_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

T0_CB_BASE_ADDRESS

VCAP_VCAP_I2P_T0_CB_BASE_ADDRESS

Bits	Name	Description
31:4	T0_CB_BASE_ADDRESS	Base address for Cb if planar store is used, or both Cb and Cr if interleaved chroma store used, in field t(0)
3:0	UNUSED	

0x059004A4 VCAP_VCAP_I2P_T0_CR_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

T0_CR_BASE_ADDRESS

VCAP_VCAP_I2P_T0_CR_BASE_ADDRESS

Bits	Name	Description
31:4	T0_CR_BASE_ADDRESS	base address fro Cr if planar format is used in field t(0)
3:0	UNUSED	

0x059004A8 VCAP_VCAP_I2P_T1_LUMA_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

T1_LUMA_BASE_ADDRESS

VCAP_VCAP_I2P_T1_LUMA_BASE_ADDRESS

Bits	Name	Description
31:4	T1_LUMA_BASE_ADDRESS	Base address for Luma in field t(1). In 0 field delay mode, if noise reduction is enabled, base address for t(-3)
3:0	UNUSED	

0x059004AC VCAP_VCAP_I2P_T1_CB_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

T1_CB_BASE_ADDRESS

VCAP_VCAP_I2P_T1_CB_BASE_ADDRESS

Bits	Name	Description
31:4	T1_CB_BASE_ADDRESS	Base address for Cb if planar store is used, or both Cb and Cr if interleaved chroma store used, in field t(1)
3:0	UNUSED	

0x059004B0 VCAP_VCAP_I2P_T1_CR_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

T1_CR_BASE_ADDRESS

VCAP_VCAP_I2P_T1_CR_BASE_ADDRESS

Bits	Name	Description
31:4	T1_CR_BASE_ADDRESS	base address for Cr if planar format is used in field t(1)
3:0	UNUSED	

0x059004B4 VCAP_VCAP_I2P_NR_T2_LUMA_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

NR_T2_LUMA_BASE_ADDRESS

VCAP_VCAP_I2P_NR_T2_LUMA_BASE_ADDRESS

Bits	Name	Description
31:4	NR_T2_LUMA_BASE_ADDRESS	Base address for luma from noise reduced version of field t(2). Only used if noise reduction is enabled. In 1 field delay mode, this register defines base address for noise reduced t(1), and in 0 field delay mode, this register defines base address for noise reduced t(0)
3:0	UNUSED	

0x059004B8 VCAP_VCAP_I2P_NR_T2_CHROMA_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

NR_T2_CHROMA_BASE_ADDRESS

VCAP_VCAP_I2P_NR_T2_CHROMA_BASE_ADDRESS

Bits	Name	Description
31:4	NR_T2_CHROMA_BASE_ADDRESS	Base address for interleaved Chroma from noise reduced version of field t(2). Only used if noise reduction is enabled. In 1 field delay mode, this register defines base address for noise reduced t(1), and in 0 field delay mode, this register defines base address for noise reduced t(0)
3:0	UNUSED	

0x059004C0 VCAP_VCAP_I2P_T2_LUMA_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

T2_LUMA_BASE_ADDRESS

VCAP_VCAP_I2P_T2_LUMA_BASE_ADDRESS

Bits	Name	Description
31:4	T2_LUMA_BASE_ADDRESS	Base address for Luma in field t(2) (the input field). If input field is read from memory, this base address is used to read input field. If input field is from hardware interface, and noise reduction is disabled, this base address is used to write input field to memory. If input field is from hardware interface, and noise reduction is enabled, this base address is not used. In 0/1 field delay mode, this register defines base address for t(-2) rather than t(2)

VCAP_VCAP_I2P_T2_LUMA_BASE_ADDRESS (cont.)

Bits	Name	Description
3:0	UNUSED	

0x059004C4 VCAP_VCAP_I2P_T2_CB_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

T2_CB_BASE_ADDRESS

VCAP_VCAP_I2P_T2_CB_BASE_ADDRESS

Bits	Name	Description
31:4	T2_CB_BASE_ADDRESS	Base address for Cb if planar store is used, or both Cb and Cr if interleaved chroma store used, in field t(2) (the input field). In 0/1 field delay mode, this register defines base address for t(-2) rather than t(2)
3:0	UNUSED	

0x059004C8 VCAP_VCAP_I2P_T2_CR_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

T2_CR_BASE_ADDRESS

VCAP_VCAP_I2P_T2_CR_BASE_ADDRESS

Bits	Name	Description
31:4	T2_CR_BASE_ADDRESS	Base address for Cr if planar format is used in field t(2) (the input field). In 0/1 field delay mode, this register defines base address for t(-2) rather than t(2)
3:0	UNUSED	

0x059004CC VCAP_VCAP_I2P_OUTPUT_LUMA_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

OUTPUT_LUMA_BASE_ADDRESS

VCAP_VCAP_I2P_OUTPUT_LUMA_BASE_ADDRESS

Bits	Name	Description
31:4	OUTPUT_LUMA_BASE_ADDRESS	base address for output frame
3:0	UNUSED	

0x059004D0 VCAP_VCAP_I2P_OUTPUT_CB_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

OUTPUT_CB_BASE_ADDRESS

VCAP_VCAP_I2P_OUTPUT_CB_BASE_ADDRESS

Bits	Name	Description
31:4	OUTPUT_CB_BASE_ADDRESS	Base address for Cb if planar format is used, or both Cb and Cr if interleaved chroma store used, for output frame
3:0	UNUSED	

0x059004D4 VCAP_VCAP_I2P_OUTPUT_CR_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

OUTPUT_CR_BASE_ADDRESS

VCAP_VCAP_I2P_OUTPUT_CR_BASE_ADDRESS

Bits	Name	Description
31:4	OUTPUT_CR_BASE_ADDRESS	base address fro Cr if planar format is used for output frame
3:0	UNUSED	

0x059004D8 VCAP_VCAP_I2P_CONTROL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

CONTROL

VCAP_VCAP_I2P_CONTROL

Bits	Name	Description
31:19	UNUSED_1	
18	START_SEQUENCE	If this flag is set to 1, starts picture initialization sequence (see INPUT_SEQUENCE field of INPUT_CONFIGURATION register)
17	LOAD_NEW_CONFIG	’0’ = Auto-configuration disabled ’1’ = Auto-configuration enabled : At the end of the picture, if ’CONFIG_BASE_ADDRESS’ is not equal to -16, then : If CYCLE_BUFFERS = ’0’, 5 128-bit words are read from memory and used to load register 0x090 to 0x0DC If CYCLE_BUFFERS = ’1’ and noise reduction disabled, 2 128-bit words are read from memory and used to load register 0x0C0 to 0x0DC. In 1 field delay mode, rather than using the first word to load t(2) base addresses, the first word will load t(1) base address registers. In 0 field delay mode, rather than using the first word to load t(2) base addresses, the first word will load t(0) base address registers If CYCLE_BUFFERS = ’1’ and noise reduction enabled, 3 128-bit words are read from memory and used to load register 0x0B4 to 0x0DC. In 1 field delay mode, rather than using the 2ndt word to load t(2) base addresses, the 2nd word will load t(1) base address registers. In 0 field delay mode, rather than using the 2nd word to load t(2) base addresses, the 2nd word will load t(0) base address registers
16	START_PROCESSING	- 0: No effect - i2p gc remains inactive. 1: i2p_gc initiates read requests to start processing new picture
15:11	UNUSED_2	
10:8	BALANCE_MODE	controls balance logic mode operation 000: AUTO The combined results of all analysis blocks used 001: SPACE_TIME Spatial/temporal/motion analysis used (film mode ignored) 010: SPATIAL Spatial analysis result only used (temporal and film mode ignored) 011: TEMPORAL Temporal analysis result only used (spatial and film mode ignored) 100: FAST_SPATIAL DO NOT USE (use 0 field delay config in output config register) 101: WEAVE_FM Weave based on field selected by film mode 110: WEAVE_T1 Weave t(0) with t(1) (all analysis results ignored) 111: WEAVE_TM1 Weave t(0) with t(-1) (all analysis results ignored)
7:1	UNUSED	
0	INPUT_BOTTOM_FIELD	’0’ = t(2) and t(0) are top fields (t(1) and t(-1) are bottom fields) ’1’ = t(2) and t(0) are bottom fields (t(1) and t(-1) are top fields) N.B. Even in 0/1 field delay mode, INPUT_BOTTOM_FIELD will indicate if t(0) is a top or bottom field

0x059004DC VCAP_VCAP_I2P_CONFIG_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0xFFFFFFF0

CONFIG_BASE_ADDRESS

VCAP_VCAP_I2P_CONFIG_BASE_ADDRESS

Bits	Name	Description
31:4	CONFIG_BASE_ADDRESS	Base address used if auto-configuration is enabled at the end of picture If 'LOAD_NEW_CONFIG' = '1', 'CORE_ACTIVE' = '0', and this register is not = 0xFFFFFFF0, then either two (CYCLE_BUFFERS, NR off), three (CYCLE_BUFFERS, NR on) or five (not CYCLE_BUFFERS) 128-bit words will be read from memory to set-up configuration registers for processing a new picture. If 'CYCLE_BUFFERS' field of NOISE_REDUCTION_CONFIGURATION register = '1', if NOISE_REDUCTION_ENABLE = 1 base addresses for t(2), nr_t(2) and output frame are loaded (base addresses for t(1), t(0) and t(-1) are shifted from previous picture). If 'CYCLE_BUFFERS' field of NOISE_REDUCTION_CONFIGURATION register = '1', if NOISE_REDUCTION_ENABLE = 0 base addresses for t(2) and output frame are loaded. In 1 field delay mode, t(1) base address registers are loaded, and t(0), t(- 1) and t(-2) are shifted. In 0 field delay mode, t(0) base address registers are loaded, and t(-1), t(-2) and t(-3) are shifted. If 'CYCLE_BUFFERS' = '0' base addresses for all four input fields, noise reduced field and the output frame are loaded. This loading process will also load a new value into this register, so that a new configuration can be loaded at the end of the new picture. If the new configuration isn't set-up yet, this register can be loaded with -16, and then loaded at a later stage when configuration is set-up
3:0	UNUSED	

0x059004E0 VCAP_VCAP_I2P_MOTION_ESTIMATION_BASE_ADDRESS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

MOTION_ESTIMATION_BASE_ADDRESS

VCAP_VCAP_I2P_MOTION_ESTIMATION_BASE_ADDRESS

Bits	Name	Description
31:4	MOTION_ESTIMATION_BASE_ADDRESS	Base address used to store parameters associated with motion estimation. The motion estimation block retains history of average motion within a 8x4 tile for the last two pictures

VCAP_VCAP_I2P_MOTION_ESTIMATION_BASE_ADDRESS (cont.)

Bits	Name	Description
3:0	UNUSED	

0x05900500 VCAP_VCAP_I2P_FILM_MODE_STATE

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

FILM_MODE_STATE

VCAP_VCAP_I2P_FILM_MODE_STATE

Bits	Name	Description
31:28	COUNT_MIX_FILM	Count of pictures with cells containing film, count between 0 and 10 (value > 10 clipped to 10)
27:24	COUNT_MIX_VIDEO	Count of pictures with mixed mode cells containing video, count between 0 and 10 (value > 10 clipped to 10)
23:22	UNUSED_1	
21:16	FILM_COUNT	count of fields in which last 8 fields are consistent with film mode
15:12	UNUSED_2	
11:8	LAST_BALANCE_MIX	last balance from mixed mode analysis (signed number from -8 to 7)
7	UNUSED	
6:4	HIGH_COMBING_COUNT	indicates if there has been a high combing count within the last 4 fields
3	HIGH_HOR_FREQ	If high horizontal frequencies are found, this flag is used to penalize large spatial angles and temporal interpolation (even if film mode not used) ’0’ = Not significant high frequencies ’1’ = Significant high frequency content
2	WEAVE_T1	Indicates best guess at which field to weave with t(0), updated even when not in film mode ’0’ = weave with t(-1) ’1’ = weave with t(1)
1:0	FILM_STATE	Film state to use if state machine result to be over-ridden 00: VIDEO Video mode (Spatial/Temporal analysis results used) 01: UNSURE Use spatial/temporal analysis, but use temporal angle 0 10: MIXED Use spatial/temporal analysis, but use temporal angle 0, and penalize motion 11: FILM Ignore spatial/temporal results, weave fields

0x05900504 VCAP_VCAP_I2P_FILM_SEQUENCE_HISTORY

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

FILM_SEQUENCE_HISTORY

VCAP_VCAP_I2P_FILM_SEQUENCE_HISTORY

Bits	Name	Description
31:30	HISTORY_SEQUENCE_15	indicates last picture consistent with film or video 00: VIDEO video 10: FILM_BACKWARD film 11: FILM_FORWARD film
29:28	HISTORY_SEQUENCE_14	sequence history from 2 pictures ago
27:26	HISTORY_SEQUENCE_13	sequence history from 3 pictures ago
25:24	HISTORY_SEQUENCE_12	sequence history from 4 pictures ago
23:22	HISTORY_SEQUENCE_11	sequence history from 5 pictures ago
21:20	HISTORY_SEQUENCE_10	sequence history from 6 pictures ago
19:18	HISTORY_SEQUENCE_9	sequence history from 7 pictures ago
17:16	HISTORY_SEQUENCE_8	sequence history from 8 pictures ago
15:14	HISTORY_SEQUENCE_7	sequence history from 9 pictures ago
13:12	HISTORY_SEQUENCE_6	sequence history from 10 pictures ago
11:10	HISTORY_SEQUENCE_5	sequence history from 11 pictures ago
9:8	HISTORY_SEQUENCE_4	sequence history from 12 pictures ago
7:6	HISTORY_SEQUENCE_3	sequence history from 13 pictures ago
5:4	HISTORY_SEQUENCE_2	sequence history from 14 pictures ago
3:2	HISTORY_SEQUENCE_1	sequence history from 15 pictures ago
1:0	HISTORY_SEQUENCE_0	sequence history from 16 pictures ago

0x05900508 VCAP_VCAP_I2P_FILM_PROJECTION_T2

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

FILM_PROJECTION_T2

VCAP_VCAP_I2P_FILM_PROJECTION_T2

Bits	Name	Description
31	UNUSED	
30:0	LAST_PROJECTION_T2	measure of vertical frequency is t1 woven with t2

0x0590050C VCAP_VCAP_I2P_FILM_PROJECTION_T0

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

FILM_PROJECTION_T0

VCAP_VCAP_I2P_FILM_PROJECTION_T0

Bits	Name	Description
31	UNUSED	
30:0	LAST_PROJECTION_T0	measure of vertical frequency is t0 woven with t1

0x05900510 VCAP_VCAP_I2P_FILM_PAST_MAX_PROJECTION

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

FILM_PAST_MAX_PROJECTION

VCAP_VCAP_I2P_FILM_PAST_MAX_PROJECTION

Bits	Name	Description
31	UNUSED	
30:0	PAST_MAX_PROJECTION	max projection from last time weave forward repeated twice

0x05900514 VCAP_VCAP_I2P_FILM_PAST_MIN_PROJECTION

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

FILM_PAST_MIN_PROJECTION

VCAP_VCAP_I2P_FILM_PAST_MIN_PROJECTION

Bits	Name	Description
31	UNUSED	
30:0	PAST_MIN_PROJECTION	min. projection from last time weave forward repeated twice

0x05900518 VCAP_VCAP_I2P_MIXED_ROW_POINTER

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

MIXED_ROW_POINTER

VCAP_VCAP_I2P_MIXED_ROW_POINTER

Bits	Name	Description
31:5	UNUSED	
4:0	MIXED_ROW_POINTER	For every 128 rows of a frame, there are 32-bits of state information stored. For contact switching this information should be capable of being able to be saved/restored. Rather than mapping all registers into the address space, this register defines which word can be read from MIXED_ROW_DATA register. After every read/write to MIXED_ROW_DATA register, MIXED_ROW_POINTER increments

0x0590051C VCAP_VCAP_I2P_MIXED_ROW_DATA

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

MIXED_ROW_DATA

VCAP_VCAP_I2P_MIXED_ROW_DATA

Bits	Name	Description
31:0	MIXED_ROW_DATA	There are 32-bits of state information stored for every 128 frame rows of a picture. This information needs to be capable of being saved/restored on a context switch. Rather than mapping all registers into address space, indirect addressing is used, where MIXED_ROW_POINTER defines which set of 32-bits of state information are read/written. After each read/write to this register MIXED_ROW_POINTER increments, so that a set of repeated reads/writes to this register can read/restore all the state information

0x05900520 VCAP_VCAP_I2P_FILM_ANALYSIS_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x05047D19

FILM_ANALYSIS_CONFIG

VCAP_VCAP_I2P_FILM_ANALYSIS_CONFIG

Bits	Name	Description
31	SURE_IGNORE_ACTIVITY	if this bit is set, activity threshold is ignored if ratio indicates film
30:27	UNUSED_1	
26:24	MIXED_FILM_RATIO	Ratio of forward to backward projection above which cell considered to be film. 0x0= 16, then 0x1 = 2 up to 0x7 = 14
23:19	UNUSED_2	
18:16	MIXED_VIDEO_RATIO	Ratio of forward to backward projection below which cell considered to be video. 0x0 = 3.0, then 0x1 = 1.25 up to 0x7 = 2.75
15:8	CELL_MIN_THRESHOLD	minimum threshold for projection before cell/picture treated as video/film
7:6	UNUSED	
5:0	COMB_INCREMENT	register value times 32 is added to forward and backward projections if combing detected

0x05900524 VCAP_VCAP_I2P_FILM_STATE_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x11230200

FILM_STATE_CONFIG

VCAP_VCAP_I2P_FILM_STATE_CONFIG

Bits	Name	Description
31:24	STAY_IN_FILM	Ratio of forward to backward projection above which a picture is considered to be film (used when already in film mode) ratio = STAY_IN_FILM/16
23:16	START_FILM	Ratio of forward to backward projection above which a picture is considered to be film (used when not in film mode) Ratio = START_FILM/ 16
15:12	UNUSED_1	

VCAP_VCAP_I2P_FILM_STATE_CONFIG (cont.)

Bits	Name	Description
11:8	LAST_PROJECTION	If the new maximum projection is < (4+SCALE_LAST_PROJECTION)*16*last max projection, then new picture processed as if it was low motion.
7	MATCH_ANY_CADENCE	'0' = Film mode only selected if one of the eight pre-defined cadences are recognized '1' = Film mode selected irrespective of sequence of toggle/no toggle pictures detected
6:4	UNUSED_2	
3:0	FORCE_SEQUENCE	- 0x0 = Film mode detection works as normal 0x1-0xF = Force film mode to repeat between 1 and 15 stages of sequence history

0x05900528 VCAP_VCAP_I2P_HORIZONTAL_FREQ_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x0A090555

HORIZONTAL_FREQ_CONFIG

VCAP_VCAP_I2P_HORIZONTAL_FREQ_CONFIG

Bits	Name	Description
31:28	UNUSED_1	
27:24	HORIZONTAL_TIME_PENALTY	If high_hor_freq is set, this value is added into gap time calculation to penalise temporal interpolation 0x0 = 0 , 0x1 = 2, 0x2 = 4, 0x3 = 8, 0x4 = 16, 0x5 = 32, 0x6 = 64, 0x7 = 128, 0x8 = 256, 0x9 = 512, 0xA = 1024, 0xB = 2048, 0xC = 4096, 0xD = 8192, 0xE = 16384, 0xF = 32768
23:20	UNUSED_2	
19:16	HORIZONTAL_SPACE_PENALTY	If high_hor_freq set, this field controls the contribution to 'happy curve' calculation of spatial analysis 0x0 = 0, 0x1 = 16, 0x2 = 32, 0x3 = 64, 0x4 = 128, 0x5 = 256, 0x6 = 512, 0x7 = 1024, 0x8 = 2048, 0x9 = 4096, 0xA = 8192, 0xB = 16384, 0xC = 32768, 0xD-F = 65536
15:12	UNUSED	
11:8	HORIZONTAL_SCALE	- 0x0 = Don't update 'high_hor_freq' 0x1-0xF = Controls threshold above which 'high_hor_freq' should be set
7:4	COMB_CURRENT_RATIO	define ratio of current projection to pixels processed above which picture drops out of film mode
3:0	COMB_BAD_RATIO	define ratio of bad projection to pixels processed above which picture drops out of film mode

0x0590052C VCAP_VCAP_I2P_FILM_ANALYSIS_2_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x0304320F

FILM_ANALYSIS_2_CONFIG

VCAP_VCAP_I2P_FILM_ANALYSIS_2_CONFIG

Bits	Name	Description
31:30	UNUSED_1	
29:24	FILM_THRESHOLD	no of fields required during which sequence history remains consistent with film before film mode selected
23:19	UNUSED_2	
18:16	PROJECTION_SHIFT	shift applied when calculating projection results
15:8	BAD_MOTION_THRESHOLD	threshold above which bad cut analysis performed
7:0	RES1_THRESHOLD	threshold above which result contributes to combing analysis

0x05900530 VCAP_VCAP_I2P_MIXED_ANALYSIS_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x04DB7A51

VCAP_VCAP_I2P_MIXED_ANALYSIS_CONFIG

Bits	Name	Description
31:29	UNUSED	
28:24	THSH_INTEGRATED_COUNTERS	threshold for ignoring insignificant weave count
23	MIXED_THICKNESS	extended range of detection
22	MIXED_CELL_INC	rate at which activity count ramps up
21:16	MIXED_THSH_MOTION	motion threshold for detecting subtitles
15:12	MIXED_NUM_THSH	activity threshold for detecting subtitles
11:8	MIXED_CELL_THSH	maximum cell motion detect
7:4	MIXED_THSH_ROW	activity threshold in a row
3:0	MIXED_AMOUNT	decay rate of analyses along row

0x05900540 VCAP_VCAP_I2P_FVM_STATE

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_FVM_STATE

Bits	Name	Description
31:28	FVM_FIELD_COUNT	count of number fields containing vertical motion
27:0	COUNT_VERT_MOTION	count of vertical motion detected in last field

0x05900550 VCAP_VCAP_I2P_FVM_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x23A60114

VCAP_VCAP_I2P_FVM_CONFIG

Bits	Name	Description
31:28	FVM_RES2_THRESH	max backward projection for vertical motion detection
27:24	FVM_RES1_THRESH	max forward projection for vertical motion detection
23:20	FVM_MOTION_THRESH	max motion for vertical motion detection
19:16	FVM_LENGTH_THRESH	no of consecutive pixels contributing to vertical motion detection
15	UNUSED_1	
14:12	FVM_GAP	max discontinuity in contributing pixels
11:10	UNUSED_2	
9:8	FVM_VERT_MOTION_OFFSET	offset used to define threshold for vertical motion detection
7	UNUSED	
6:4	FVM_VERT_MOTION_SHIFT	shift used to define threshold for vertical motion detection
3:0	FVM_FIELDS_THRESH	number of fields which contribute to vertical motion detection

0x05900580 VCAP_VCAP_I2P_SPATIAL_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x14224916

VCAP_VCAP_I2P_SPATIAL_CONFIG

Bits	Name	Description
31	SPATIAL_SIMPLE_5_EXT	Use simplified scaling when there are 5 extremes
30:29	UNUSED_1	
28:24	SPATIAL_SCALE_5_EXT	Scale factor applied when there are 5 extremes
23	UNUSED_2	
22:16	SPATIAL_MAX_VALID_STEP	Confidence scale parameter (+16) used with large number of extremes
15:11	SPATIAL_NEIGHBORHOOD	Neighborhood*8(+68) defines threshold below which extremes are cleaned
10:8	SPATIAL_PAR3	Scale parameter applied to cleaned extremes
7	UNUSED	
6:4	SPATIAL_PAR2	Offset (+2) subtracted from number of extremes
3:0	SPATIAL_PAR1	Scale factor(+4) applied to calculate gap centre

0x05900584 VCAP_VCAP_I2P_SPATIAL_2_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x83270418

VCAP_VCAP_I2P_SPATIAL_2_CONFIG

Bits	Name	Description
31:24	SPATIAL_NORM_SAD	Scaling parameter to apply to confidence result
23:22	UNUSED_1	
21:16	SPATIAL_PARAMAX	Spatial parameter (scaled by 128) which effects confidence scaling
15:11	UNUSED_2	
10:0	SPATIAL_SCALE_4_EXT	Scaling parameter to use if 4 extremes

0x05900588 VCAP_VCAP_I2P_SPATIAL_3_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000F92

VCAP_VCAP_I2P_SPATIAL_3_CONFIG

Bits	Name	Description
31:14	UNUSED	
13:8	SPATIAL_MAGIC_SAD2	Min. SAD secondary scaling parameter (setting 0 = 32)
7:0	SPATIAL_MAGIC_SAD1	Min. SAD initial scale

0x059005C0 VCAP_VCAP_I2P_TEMPORAL_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_TEMPORAL_CONFIG

Bits	Name	Description
31:14	UNUSED_1	
13:12	THEMPORAL_MOTION_THRESH	temporal correction
11:9	UNUSED_2	
8	THEMPORAL_VMOTION_ENABLE	temporal correction
7:4	UNUSED	
3:0	HIGH_FREQ_ANGLE_PENALTY	Configures penalty applied to larger angles of interpolation

0x05900600 VCAP_VCAP_I2P_NOISE_REDUCTION_LUMA_CONTROL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x40004000

VCAP_VCAP_I2P_NOISE_REDUCTION_LUMA_CONTROL

Bits	Name	Description
31:24	LUMA_SCALE_DIFF	Controls range of values over which blend ratio changes from 0:100 to 100:0 in response to pixel difference If 'luma_scale_diff' > 0 then luma_blend = clip0to255((abs(luma_t2_y1-luma_t0_y1) - luma_diff_limit) * luma_scale_diff / 4) Else luma_blend = luma_diff_limit + 128
23:16	LUMA_DIFF_LIMIT	If pixel difference is below this threshold, no blending is applied (signed value between -128 and +127)

VCAP_VCAP_I2P_NOISE_REDUCTION_LUMA_CONTROL (cont.)

Bits	Name	Description
15:8	LUMA_SCALE_MOTION	Controls range of values over which blend ratio changes from 0:100 to 100:0 If 'luma_scale_motion' > 0 then Blend = clip0to255((luma_blend_limit - current_motion) * luma_scale_motion / 8) Else Blend = luma_blend_limit
7:0	LUMA_BLEND_LIMIT	Sets threshold for maximum motion above which no blending applied (unsigned number in range 0 to 255)

0x05900604 VCAP_VCAP_I2P_NOISE_REDUCTION_CHROMA_CONTROL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x40004000

VCAP_VCAP_I2P_NOISE_REDUCTION_CHROMA_CONTROL

Bits	Name	Description
31:24	CHROMA_SCALE_DIFF	Controls range of values over which blend ratio changes from 0:100 to 100:0 in response to pixel difference If 'chroma_scale_diff' > 0 then cb_blend = clip0to255((abs(cb_t2_y1-cb_t0_y1) - chroma_diff_limit) * chroma_scale_diff / 4) Else cb_blend = chroma_diff_limit + 128
23:16	CHROMA_DIFF_LIMIT	If pixel difference is below this threshold, no blending is applied (signed value between -128 and +127)
15:8	CHROMA_SCALE_MOTION	Controls range of values over which blend ratio changes from 0:100 to 100:0 If 'chroma_scale_motion' > 0 then Blend = clip0to255((chroma_blend_limit - current_motion) * chroma_scale_motion / 8) Else Blend = chroma_blend_limit
7:0	CHROMA_BLEND_LIMIT	Sets threshold for maximum motion above which no blending applied (unsigned number in range 0 to 255)

0x05900608 VCAP_VCAP_I2P_NOISE_REDUCTION_AVERAGE_LUMA

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x40000000

VCAP_VCAP_I2P_NOISE_REDUCTION_AVERAGE_LUMA

Bits	Name	Description
31:0	NR_AVE_LUMA_BLEND	Average luma_blend <<24, using IIR approach to calculate average (ranges from nr_ave_blend >> 24 = 0 equivalent to all pixels from input field, up to nr_ave_blend >> 24 = 255 equivalent to 255:1 blend from reference

0x0590060C VCAP_VCAP_I2P_NOISE_REDUCTION_AVERAGE_CHROMA

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x40000000

VCAP_VCAP_I2P_NOISE_REDUCTION_AVERAGE_CHROMA

Bits	Name	Description
31:0	NR_AVE_CHROMA_BLEND	Average luma_blend <<24, using IIR approach to calculate average (ranges from nr_ave_blend >> 24 = 0 equivalent to all pixels from input field, up to nr_ave_blend >> 24 = 255 equivalent to 255:1 blend from reference

0x05900610 VCAP_VCAP_I2P_NOISE_REDUCTION_AVERAGE_MOTION

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000010

VCAP_VCAP_I2P_NOISE_REDUCTION_AVERAGE_MOTION

Bits	Name	Description
31:10	UNUSED	
9:0	NR_AVE_MOTION	Minimum of current_motion seen within noise reduction window, averaged over multiple frames using IIR calculation (where ave_motion >> 4 is average minimum motion seen)

0x05900614 VCAP_VCAP_I2P_NOISE_REDUCTION_AVERAGE_MOTION2

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x40000000

VCAP_VCAP_I2P_NOISE_REDUCTION_AVERAGE_MOTION2

Bits	Name	Description
31:0	NR_AVE_MOTION2	Average of current_motion <<24, using IIR approach to calculate average

0x05900620 VCAP_VCAP_I2P_NOISE_REDUCTION_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x0A000000

VCAP_VCAP_I2P_NOISE_REDUCTION_CONFIG

Bits	Name	Description
31:28	UNUSED_1	
27:24	NOISE_REDUCTION_WINDOW	Defines size of region around edge of a frame which is excluded from minimum motion calculation (applies to top, bottom, left and right boundaries). This parameter is multiplied by 8, so can define a window between 0 and 120 pixels from picture boundary
23	UNUSED_2	
22:20	DECAY_RATIO	Controls rate of decay in IIR calculations of average blend, where 2^26 decays to 50% over approx 46,500,000 pixels, whereas 2^19 decays to 50% over approx 363,000 pixels 000: DECAY_26 Decay ratio (2^26-1)/(2^26) 001: DECAY_25 Decay ratio (2^25-1)/(2^25) 010: DECAY_24 Decay ratio (2^24-1)/(2^24) 011: DECAY_23 Decay ratio (2^23-1)/(2^23) 100: DECAY_22 Decay ratio (2^22-1)/(2^22) 101: DECAY_21 Decay ratio (2^21-1)/(2^21) 110: DECAY_20 Decay ratio (2^20-1)/(2^20) 111: DECAY_19 Decay ratio (2^19-1)/(2^19)
19:0	UNUSED	

0x05900624 VCAP_VCAP_I2P_NOISE_REDUCTION_LUMA_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x040F4149

VCAP_VCAP_I2P_NOISE_REDUCTION_LUMA_CONFIG

Bits	Name	Description
31:28	UNUSED_1	
27:24	LUMA_MAX_BLEND_RATIO	Controls the maximum blending ratio which can be applied by noise reduction (0 = 50:50, 15 = 31:1)
23:20	UNUSED_2	
19	UPDATE_LUMA_SCALE_DIFF	When this field is set, at the end of a field, LUMA_SCALE_DIFF can be updated based on average motion
18	UPDATE_LUMA_DIFF_LIMIT	When this bit is set, at the end of a field, LUMA_DIFF_LIMIT can be updated based on average motion
17	UPDATE_LUMA_SCALE_MOTION	When this field is set, at the end of a field, LUMA_SCALE_MOTION can be updated based on average motion
16	UPDATE_LUMA_BLEND_LIMIT	When this bit is set, at the end of a field, LUMA_BLEND_LIMIT can be updated based on average motion

VCAP_VCAP_I2P_NOISE_REDUCTION_LUMA_CONFIG (cont.)

Bits	Name	Description
15:12	LUMA_SCALE_DIFF_RATIO	Defines proportion of average_motion to use to set luma_scale_diff, if update of UPDATE_LUMA_SCALE_DIFF is set. A value between 1 and 15 corresponds ramp from 100:0 to 50:50 over scaled average motion*1/16 up to scaled average motion*15/16. A value of 0 corresponds to scaled average motion*16/16
11:8	LUMA_DIFF_LIMIT_RATIO	Defines proportion of scaled average motion to use to set LUMA_DIFF_LIMIT to, if UPDATE_LUMA_DIFF_LIMIT is set. Defines a value between scaled average motion*-8/16 up to scaled average motion*7/16 (where result is signed and clipped to range -128 to 127)
7:4	LUMA_SCALE_MOTION_RATIO	Defines proportion of average_motion to use to set luma_scale_motion, if update of UPDATE_LUMA_SCALE_MOTION is set. A value between 1 and 15 corresponds ramp from 100:0 to 50:50 over scaled average motion*1/16 up to scaled average motion*15/16. A value of 0 corresponds to scaled average motion*16/16
3:0	LUMA_BLEND_LIMIT_RATIO	Defines proportion of scaled average motion to use to set LUMA_BLEND_LIMIT to, if UPDATE_LUMA_BLEND_LIMIT is set. Defines a value between scaled average motion*0/16 up to scaled average motion*15/16 (where maximum result limited to 255).

0x05900628 VCAP_VCAP_I2P_NOISE_REDUCTION_CHROMA_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x040F4149

VCAP_VCAP_I2P_NOISE_REDUCTION_CHROMA_CONFIG

Bits	Name	Description
31:28	UNUSED_1	
27:24	CHROMA_MAX_BLEND_RATIO	Controls the maximum blending ratio which can be applied by noise reduction (0 = 50:50, 15 = 31:1)
23:20	UNUSED_2	
19	UPDATE_CHROMA_SCALE_DIFF	When this field is set, at the end of a field, CHROMA_SCALE_DIFF can be updated based on average motion
18	UPDATE_CHROMA_DIFF_LIMIT	When this bit is set, at the end of a field, CHROMA_DIFF_LIMIT can be updated based on average motion.
17	UPDATE_CHROMA_SCALE_MOTION	When this field is set, at the end of a field, CHROMA_SCALE_MOTION can be updated based on average motion

VCAP_VCAP_I2P_NOISE_REDUCTION_CHROMA_CONFIG (cont.)

Bits	Name	Description
16	UPDATE_CHROMA_BLEND_LIMIT	When this bit is set, at the end of a field, CHROMA_BLEND_LIMIT can be updated based on average motion.
15:12	CHROMA_SCALE_DIFF_RATIO	Defines proportion of average_motion to use to set chroma_scale_diff, if update of UPDATE_CHROMA_SCALE_DIFF is set. A value between 1 and 15 corresponds ramp from 100:0 to 50:50 over scaled average motion*-8/16 up to scaled average motion times7/16 and clipped
11:8	CHROMA_DIFF_LIMIT_RATIO	Defines proportion of scaled average motion to use to set CHROMA_DIFF_LIMIT to, if UPDATE_CHROMA_DIFF_LIMIT is set. Defines a value between scaled average motion*-8/16 up to scaled average motion*7/16 (where result is signed and clipped to range -128 to 127)
7:4	CHROMA_SCALE_MOTION_RATIO	Defines proportion of average_motion to use to set chroma_scale_motion, if update of UPDATE_CHROMA_SCALE_MOTION is set. A value between 1 and 15 corresponds ramp from 100:0 to 50:50 over scaled average motion*1/16 up to scaled average motion*15/16. A value of 0 corresponds to scaled average motion*16/16
3:0	CHROMA_BLEND_LIMIT_RATIO	Defines proportion of scaled average motion to use to set CHROMA_BLEND_LIMIT to, if UPDATE_CHROMA_BLEND_LIMIT is set. Defines a value between scaled average motion*0/16 up to scaled average motion*15/16 (where maximum result limited to 255).

0x05900680 VCAP_VCAP_I2P_BALANCE_CONFIGURATION

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x43C0FD0C

VCAP_VCAP_I2P_BALANCE_CONFIGURATION

Bits	Name	Description
31:28	BALANCE_SCALE_NON_MIX	Scale parameter in non-mixed mode
27	UNUSED_1	
26:22	BALANCE_SCALE_MIX	Scale factor used in mixed mode
21	UNUSED_2	
20	USE_3TAP_BOB	’0’ = use 1-tap vertical bob calculation ’1’ = use 3-tap vertical bob calculation (taps 1,2,1)
19	UNUSED	

VCAP_VCAP_I2P_BALANCE_CONFIGURATION (cont.)

Bits	Name	Description
18:16	MIN_BOB_RATIO	Minimum amount of bob to blend with I2P_GC result, where bob result is simple vertical filter. This number is added to a variable reflecting the certainty of space_time analysis, to select proportion of 'bob' result to use relative to space/time interpolation where bob ratio of 0 = all space/time, bob ratio of 128 = all bob interpolation. (This register is not used in film mode) 0x0 = 0, 0x1 = 8, 0x2 = 16, 0x3 = 24, 0x4 = 32, 0x5 = 64 0x6 = 96, 0x7 =128
15:6	BALANCE_SCALE_OFFSET	Signed offset (multiplied by 8) to add into time penalty calculation
5:0	BALANCE_SCALE_MOTION_TIME	Scale factor applied to motion when calculating time penalty (setting of 0x0 = 64)

0x05900684 VCAP_VCAP_I2P_BALANCE_MOTION_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000255

VCAP_VCAP_I2P_BALANCE_MOTION_CONFIG

Bits	Name	Description
31:10	UNUSED	
9:8	BALANCE_NOISE_SHIFT	Defines if 0 to 3 LSBits of max_motion are masked
7:0	BALANCE_MOTION_PAR	Scaling factor applied to max_motion

0x05900688 VCAP_VCAP_I2P_BALANCE_LIGHT_COMB

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x24154252

VCAP_VCAP_I2P_BALANCE_LIGHT_COMB

Bits	Name	Description
31:28	SUBTITLE_MOTION_THSH	Motion threshold for subtitle penalty
27:24	LIGHT_GAP_TIME	Offset applied if light combing detected
23:20	LIGHT_MIN_DIFF	Minimum difference considered for light combing
19:16	LIGHT_MAX_DIFF	Maximum difference considered for light combing
15:12	LIGHT_MOTION_MAX_LIM	Maximum motion threshold for light combing
11:8	LIGHT_MOTION_MIN_LIM	Minimum motion threshold for light combing
7:4	LIGHT_MUL_FACT	Scaling factor applied to maximum coefficient if subtitles

VCAP_VCAP_I2P_BALANCE_LIGHT_COMB (cont.)

Bits	Name	Description
3	UNUSED	
2:0	LIGHT_THSH_MAX	Maximum coefficient value to be considered for light combing

0x0590068C VCAP_VCAP_I2P_BALANCE_VMOTION_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00024414

VCAP_VCAP_I2P_BALANCE_VMOTION_CONFIG

Bits	Name	Description
31:19	UNUSED_1	
18:16	VMOTION_ACTIVE_SYM_THRESHOLD	If sym_fact greater than threshold and vmotion_fields >=2, process pixel as spatial
15	UNUSED_2	
14:12	VMOTION_SPATIAL_THRESHOLD	If spatial greater than threshold, consider pixel for vertical motion
11	UNUSED_3	
10:8	VMOTION_TEMP_SYM_THRESHOLD	If temporal_motion*sym_fact greater than threshold, consider pixel for vertical motion
7:5	UNUSED_4	
4	VMOTION_REPEAT_THRESHOLD	Pixel repeat threshold = 3 (when 0) or 7 (when 1)
3	UNUSED	
2:0	VMOTION_PIXELS_FIELD	Threshold for number of pixels/field to trigger vertical motion

0x05900690 VCAP_VCAP_I2P_BALANCE_VMOTION_STATE

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_BALANCE_VMOTION_STATE

Bits	Name	Description
31:30	VMOTION_ACTIVE_FIELDS	This register indicates how many fields vertical motion has been active for (the register state should be saved and restored on switching states)

VCAP_VCAP_I2P_BALANCE_VMOTION_STATE (cont.)

Bits	Name	Description
29:0	VMOTION_PIXELS	READ ONLY This is a read only field which indicates how many pixels in the last field contributed to vertical motion detection (Field is reset to 0 at start of each field)

0x05900694 VCAP_VCAP_I2P_BALANCE_AVERAGE_BLEND

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_BALANCE_AVERAGE_BLEND

Bits	Name	Description
31:0	BALANCE_SPACE_TIME_BLEND	IIR accumulated average of space/time blend (updated only when space/time selection made)

0x059006C0 VCAP_VCAP_I2P_DIFF_TP1Y0_TP2YM1

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DIFF_TP1Y0_TP2YM1

Bits	Name	Description
31:0	DIFF_TP1Y0_TP2YM1	READ ONLY Accumulated pixel differenceA

0x059006C4 VCAP_VCAP_I2P_DIFF_TP1Y0_TP2YP1

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DIFF_TP1Y0_TP2YP1

Bits	Name	Description
31:0	DIFF_TP1Y0_TP2YP1	READ ONLY Accumulated pixel differenceB

0x059006C8 VCAP_VCAP_I2P_DIFF_T0YM1_TP1Y0

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DIFF_T0YM1_TP1Y0

Bits	Name	Description
31:0	DIFF_T0YM1_TP1Y0	READ ONLY Accumulated pixel differenceC

0x059006CC VCAP_VCAP_I2P_DIFF_T0YP1_TP1Y0

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DIFF_T0YP1_TP1Y0

Bits	Name	Description
31:0	DIFF_T0YP1_TP1Y0	READ ONLY Accumulated pixel differenceD

0x059006D0 VCAP_VCAP_I2P_DIFF_T0YM1_TP2YM1

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DIFF_T0YM1_TP2YM1

Bits	Name	Description
31:0	DIFF_T0YM1_TP2YM1	READ ONLY Accumulated pixel differenceE

0x059006D4 VCAP_VCAP_I2P_DIFF_TM1Y0_TP1Y0

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DIFF_TM1Y0_TP1Y0

Bits	Name	Description
31:0	DIFF_TM1Y0_TP1Y0	READ ONLY Accumulated pixel differenceF

0x059006D8 VCAP_VCAP_I2P_DIFF_T0YP1_TP2YP1

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DIFF_T0YP1_TP2YP1

Bits	Name	Description
31:0	DIFF_T0YP1_TP2YP1	READ ONLY Accumulated pixel differenceG

0x059006E0 VCAP_VCAP_I2P_DIFF_UP_2

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DIFF_UP_2

Bits	Name	Description
31:0	DIFF_UP_2	READ ONLY Accumulated pixel differencem2

0x059006E4 VCAP_VCAP_I2P_DIFF_UP_1

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DIFF_UP_1

Bits	Name	Description
31:0	DIFF_UP_1	READ ONLY Accumulated pixel differencem1

0x059006E8 VCAP_VCAP_I2P_DIFF_0_VERT

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DIFF_0_VERT

Bits	Name	Description
31:0	DIFF_0_VERT	READ ONLY Accumulated pixel difference0

0x059006EC VCAP_VCAP_I2P_DIFF_DOWN_1

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DIFF_DOWN_1

Bits	Name	Description
31:0	DIFF_DOWN_1	READ ONLY Accumulated pixel difference1

0x059006F0 VCAP_VCAP_I2P_DIFF_DOWN_2

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DIFF_DOWN_2

Bits	Name	Description
31:0	DIFF_DOWN_2	READ ONLY Accumulated pixel difference2

0x059006F8 VCAP_VCAP_I2P_VMOTION_HISTORY

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_VMOTION_HISTORY

Bits	Name	Description
31:22	UNUSED_1	
21:20	HIST_UP_DOWN	Increments if DIFF_DOWN was smaller then DIFF_UP in picture (else decrements to 0)
19:18	UNUSED_2	
17:16	HIST_DOWN_2	Increments if DIFF_DOWN_2 was smallest difference in picture (else decrements to 0)
15:14	UNUSED_3	
13:12	HIST_DOWN_3	Increments if DIFF_DOWN_1 was smallest difference in picture (else decrements to 0)
11:10	UNUSED_4	
9:8	HIST_0_VERT	Increments if DIFF_0_VERT was smallest difference in picture (else decrements to 0)
7:6	UNUSED_5	
5:4	HIST_UP_1	Increments if DIFF_UP_1 was smallest difference in picture (else decrements to 0)
3:2	UNUSED_6	
1:0	HIST_UP_2	Increments if DIFF_UP_2 was smallest difference in picture (else decrements to 0)

0x059006FC VCAP_VCAP_I2P_PIXEL_DIFF_CONFIG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_PIXEL_DIFF_CONFIG

Bits	Name	Description
31:4	UNUSED	
3:0	PIXEL_DIFF_BORDER	Defines number of frame rows at top and bottom of picture which are not included when calculating pixel differences (PIXEL_DIFF_BORDER is multiplied by 8, so can define between 0 and 120 frame lines excluded from top and bottom of picture)

0x05900700 VCAP_VCAP_I2P_LINE_STORE_LUMA_SIGNATURE

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_LINE_STORE_LUMA_SIGNATURE

Bits	Name	Description
31:0	LS_LUMA_SIGNATURE	READ ONLY CRC calculated from output of 10 luma line stores, updated at end of each picture

0x05900704 VCAP_VCAP_I2P_LINE_STORE_CHROMA_SIGNATURE

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_LINE_STORE_CHROMA_SIGNATURE

Bits	Name	Description
31:0	LS_CHROMA_SIGNATURE	READ ONLY - 32-bit CRC calculated from output of 10 chroma line stores (5 Cr and 5 Cb), updated at end of picture

0x05900708 VCAP_VCAP_I2P_MEM_SIGNATURE_CONTROL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_MEM_SIGNATURE_CONTROL

Bits	Name	Description
31:11	UNUSED_1	
10:8	MEM_WRITE_SIGNATURE_CONTROL	Selects which memory write buffer to calculate write signature from 000: OUT_LUMA Luma output 001: OUT_CB Cb output 010: OUT_CR Cr output 011: NOISE_LUMA Noise reduction luma write 100: NOISE_CHROMA Noise reduction chroma write 101: MOTION Motion estimation writes
7:4	UNUSED_2	

VCAP_VCAP_I2P_MEM_SIGNATURE_CONTROL (cont.)

Bits	Name	Description
3:0	MEM_READ_SIGNATURE_CONTROL	Selects which read buffer to calculate memory read signature from 0000: T2_LUMA t(2) Luma 0001: T2_CB t(2) Cb 0010: T2_CR t(2) Cr 0011: T1_LUMA t(1) Luma 0100: T1_CB t(1] Cb 0101: T1_CR t(1) Cr 0110: T0_LUMA t(0) Luma 0111: T0_CB t(0) Cb 1000: T0_CR t(0) Cr 1001: TM1_LUMA t(-1) Luma 1010: TM1_CB t(-1) Cb 1011: TM1_CR t(-1) Cr 1100: MOTION Motion estimation 1110: CONFIG

0x0590070C VCAP_VCAP_I2P_MEM_READ_SIGNATURE

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_MEM_READ_SIGNATURE

Bits	Name	Description
31:0	MEM_READ_SIGNATURE	READ ONLY - 32-bit CRC calculated from words read from TAG defined by MEM_READ_SIGNATURE_CONTROL. Updates at end of picture

0x05900710 VCAP_VCAP_I2P_FILTER_SIGNATURE

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_FILTER_SIGNATURE

Bits	Name	Description
31:0	FILTER_SIGNATURE	READ ONLY - 32-bit CRC on pixels out of balance logic filter, updated at end of picture

0x05900714 VCAP_VCAP_I2P_MEM_WRITE_SIGNATURE

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_MEM_WRITE_SIGNATURE

Bits	Name	Description
31:0	MEM_WRITE_SIGNATURE	READ ONLY - 32-bit CRC calculated from words read from TAG defined by MEM_WRITE_SIGNATURE_CONTROL. Updates at end of picture

0x05900720 VCAP_VCAP_I2P_LINE_STORE_LUMA_SIGNATURE_RAW

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_LINE_STORE_LUMA_SIGNATURE_RAW

Bits	Name	Description
31:0	LS_LUMA_SIGNATURE_RAW	READ ONLY CRC calculated from output of 10 luma line stores, updates every pixel

0x05900724 VCAP_VCAP_I2P_LINE_STORE_CHROMA_SIGNATURE_RAW

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_LINE_STORE_CHROMA_SIGNATURE_RAW

Bits	Name	Description
31:0	LS_CHROMA_SIGNATURE_RAW	READ ONLY - 32-bit CRC calculated from output of 10 chroma line stores (5 Cr and 5 Cb), updates every pixel

0x0590072C VCAP_VCAP_I2P_MEM_READ_SIGNATURE_RAW

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_MEM_READ_SIGNATURE_RAW

Bits	Name	Description
31:0	MEM_READ_SIGNATURE_RAW	READ ONLY MEM_READ_SIGNATURE_RAW 32-bit CRC calculated from words read from TAG defined by MEM_SIGNATURE_CONTROL, updates every word

0x05900730 VCAP_VCAP_I2P_FILTER_SIGNATURE_RAW

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_FILTER_SIGNATURE_RAW

Bits	Name	Description
31:0	FILTER_SIGNATURE_RAW	READ ONLY - 32-bit CRC on pixels out of balance logic filter, updates every pixel

0x05900734 VCAP_VCAP_I2P_MEM_WRITE_SIGNATURE_RAW

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_MEM_WRITE_SIGNATURE_RAW

Bits	Name	Description
31:0	MEM_WRITE_SIGNATURE_RAW	READ ONLY - 32-bit CRC calculated from words written from TAG defined by MEM_WRITE_SIGNATURE_CONTROL, updates every word

0x05900748 VCAP_VCAP_I2P_CORE_FLOW_STATUS

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_CORE_FLOW_STATUS

Bits	Name	Description
31	CORE_ACTIVE_STATUS	READ ONLY Core is processing a picture

VCAP_VCAP_I2P_CORE_FLOW_STATUS (cont.)

Bits	Name	Description
30	MEM_ACTIVE_STATUS	READ ONLY Memory controller still has read/writes pending
29	MEM_CONFIG_PEND_STATUS	READ ONLY Memory controller has config word to send to registers
28	MEM_READ_ACTIVE_STATUS	READ ONLY Memory controller still has reads to issue for current picture
27:26	PIXEL_STATE_STATUS	READ ONLY Line store output state (0 = Idle, 1=Start, 2=Active, 3=End)
25	LS_NR_ENABLE_STATUS	READ ONLY Pixel from line store to noise reduction accepted
24	LS_MOTION_ENABLE_STATUS	READ ONLY Pixel from line store to motion estimation accepted
23	LS_BALANCE_ENABLE_STATUS	READ ONLY Pixel from line store to balance logic accepted
22	LS_BALANCE_VALID_STATUS	READ ONLY Pixel from line store to balance logic valid
21:18	UNUSED	
17	OF_MEM_ENABLE_STATUS	READ ONLY Word from balance logic to memory controller accepted
16	OF_MEM_VALID_STATUS	READ ONLY Word from balance logic to memory controller valid
15	MOTION_MEM_ENABLE_STATUS	READ ONLY Word from motion estimation to memory controller accepted
14	MOTION_MEM_VALID_STATUS	READ ONLY Word from motion estimation to memory controller valid
13	NR_MEM_ENABLE_STATUS	READ ONLY Word from noise reduction to memory controller accepted
12	NR_MEM_VALID_STATUS	READ ONLY Word from noise reduction to memory controller valid
11	MEM_CONFIG_ENABLE_STATUS	READ ONLY Word from memory controller to config registers accepted
10	MEM_CONFIG_VALID_STATUS	READ ONLY Word from memory controllers to config registers valid
9	MEM_MOTION_ENABLE_STATUS	READ ONLY Word from memory controller to motion estimation accepted
8	MEM_MOTION_VALID_STATUS	READ ONLY Word from memory controller to motion estimation valid

VCAP_VCAP_I2P_CORE_FLOW_STATUS (cont.)

Bits	Name	Description
7	MEM_LS_ENABLE_STATUS	READ ONLY Word from memory controller to line store accepted
6	MEM_LS_VALID_STATUS	READ ONLY Word from memory controller to line store valid
5	MEM_ENABLE_STATUS	READ ONLY Memory command accepted
4	MEM_VALID_STATUS	READ ONLY Memory command valid
3	OUT_PIXEL_ENABLE_STATUS	READ ONLY Output pixel accepted
2	OUT_PIXEL_VALID_STATUS	READ ONLY Output pixel valid
1	INP_PIXEL_ENABLE_STATUS	READ ONLY Input pixel accepted
0	INP_PIXEL_VALID_STATUS	READ ONLY Input pixel available

0x0590074C VCAP_VCAP_I2P_LINE_STORE_STATUS

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_LINE_STORE_STATUS

Bits	Name	Description
31:28	UNUSED	
27:26	LS_PIXEL_STATE	READ ONLY Line store output state (0 = Idle, 1=Start, 2=Active, 3=End)
25	LS_NR_ENABLE_LS	READ ONLY Pixel from line store to noise reduction accepted
24	LS_MOTION_ENABLE_LS	READ ONLY Pixel from line store to motion estimation accepted
23	LS_BALANCE_ENABLE_LS	READ ONLY Pixel from line store to balance logic accepted
22	LS_BALANCE_VALID_LS	READ ONLY Pixel from line store to balance logic valid
21:11	LS_PIXEL_Y_OFFSET	READ ONLY Y offset out of line store block

VCAP_VCAP_I2P_LINE_STORE_STATUS (cont.)

Bits	Name	Description
10:0	LS_PIXEL_X_OFFSET	READ ONLY X offset out of line store block

0x05900750 VCAP_VCAP_I2P_SPLIT_SCREEN_CONTROL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_SPLIT_SCREEN_CONTROL

Bits	Name	Description
31:3	UNUSED	
2	SPLIT_SIMPLE_BOB	If split screen enabled, 0 = simple weave, 1 = simple bob
1	SPLIT_SIMPLE_LEFT	If split screen enabled, 0 = simple bob/weave on left, 1 = simple bob/weave on right
0	SPLIT_SCREEN_ENABLE	’1’ = Split screen display enabled (half screen = simple bob/weave)

0x059007C0 VCAP_VCAP_I2P_CORE_ID_REG

Type: Read
Clock: UNDEFINED
Reset State: 0x1002002E

VCAP_VCAP_I2P_CORE_ID_REG

Bits	Name	Description
31:24	GROUP_ID	READ ONLY I2P family of products
23:16	CORE_ID	READ ONLY I2P_GC allocated ID of 2
15:0	CONFIG	READ ONLY bit 0 = Pixel resolution (0 = 8-bit, 1 = 10-bit) bit 1 = Chroma stores (0 = 1 chroma store, 1 = 4 chroma stores) bits 7:4 = Log of max width supported

0x059007D0 VCAP_VCAP_I2P_CORE_REV_REG

Type: Read
Clock: UNDEFINED
Reset State: 0x00010101

VCAP_VCAP_I2P_CORE_REV_REG

Bits	Name	Description
31:24	DESIGNER	READ ONLY
23:16	MAJOR_REV	READ ONLY
15:8	MINOR_REV	READ ONLY
7:0	MAINTENANCE_REV	READ ONLY

0x059007E0 VCAP_VCAP_I2P_DESIGNER1

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DESIGNER1

Bits	Name	Description
31:0	DESIGNER1	READ ONLY

0x059007F0 VCAP_VCAP_I2P_DESIGNER2

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

VCAP_VCAP_I2P_DESIGNER2

Bits	Name	Description
31:0	DESIGNER2	READ ONLY

14.19.2 VCAP_VC SWI Register Set

VCAP_VC Registers

0x05900800 VCAP_VCAP_VC_CTRL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register has the configuration register for VCAP VC block

VCAP_VCAP_VC_CTRL

Bits	Name	Description
31:11	UNUSED	
10	FIELD_WRITTEN_INTR	- 0= Frame done interrupt will fire every frame for interlace resolutions. 1=Frame done interrupt will fire every field for interlace resolutions.
9	FIELD_VSYNC_INTR	- 0= Vsync interrupt will fire every frame for interlace resolutions. 1=Vsync interrupt will fire every field for interlace resolutions.
8	CAP_VSYNC_ONLY	- 0 = Hsync and Vsync needs to be aligned for capture to start. 1= Capture starts on Vsync. Hsync alignment is not changed
7:4	BUF_EN	Enable the third, fourth and fifth buffer if required. 0 = only 2 buffers used to write to the memory Y_ADDR_1, YADDR_2 for Y and RGB, C_ADDR_1 and C_ADDR_2 for Chroma. 1 = Third Buffer Y_ADDR_3 is used for Y or RGB and C_ADDR_3 is used for Chroma. 2= Fourth Buffer Y_ADDR_4 is used for Y or RGB and C_ADDR_4 is used for Chroma. 3= fifth Buffer Y_ADDR_5 is used for Y or RGB and C_ADDR_5 is used for Chroma. 4= Sixth Buffer Y_ADDR_6 is used for Y or RGB and C_ADDR_6 is used for Chroma.
3	INT_EN	This field will indicate if the capture is progressive or interlace format. 0= progressive, 1= Interlace
2	FRAME_OVERWRITE_EN	Configure if the buffer needs to be overwritten or the frames dropped in case software does not pick up the frames captured by hardware. 0 = Frames will be dropped in case the BUF1_WRITTEN_INT and BUF2_WRITTEN_INT and optionally BUF3_WRITTEN_EN fields in STATUS_1 register are not cleared. 1 = Captured frames will overwrite the buffers in case the BUF1_WRITTEN_INT and BUF2_WRITTEN_INT and optionally BUF3_WRITTEN_EN fields in STATUS register are not cleared.
1	Y_RGB_SEL	Configure the input data type. 0= YCrCb, 1= RGB
0	ENABLE	Enable VCAP_VC block. 0=disable, 1= enable. Before enabling the VCAP VC it is required to apply soft reset

0x05900804 VCAP_VCAP_VC_NPL_CTRL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to control VCAP_NPL

VCAP_VCAP_VC_NPL_CTRL

Bits	Name	Description
31:9	UNUSED_1	
8	SW_RESET	Soft reset the NPL block. 0 = normal operation, 1= Soft reset
7:4	SDL_SEL	Delayed clock for capture. 0 = No_delay, programming this field from 0x1 to 0xF gives delay in steps of approximately 0.59ns.
3	UNUSED_2	
2	CLK_INV	Invert the clock, 0=non-inverted clock used to capture the data, 1= Inverted Clock is used to capture the data
1:0	CLK_SEL	Select the clocks 00=No CLock, 01 = shadow test clock, 10 = Delayed clock (When SDL_SEL is programmed to 0 io_clk will be output without delay), 11= Inverted clock

0x05900808 VCAP_VCAP_VC_IN_CRTL1

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x0A418820

This register has the mux control for DATA0,DATA1,DATA2,DATA3,DATA4 and DATA5

VCAP_VCAP_VC_IN_CRTL1

Bits	Name	Description
31:30	UNUSED	
29:25	SEL_DATA5	Select the Data bit 5 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 5, 0x1 = input data 1 is mapped to data bit 5, 0x2 = input data 2 is mapped to data bit 5 and so on.
24:20	SEL_DATA4	Select the Data bit 4 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 4, 0x1 = input data 1 is mapped to data bit 4, 0x2 = input data 2 is mapped to data bit 4 and so on.

VCAP_VCAP_VC_IN_CRTL1 (cont.)

Bits	Name	Description
19:15	SEL_DATA3	Select the Data bit 3 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 3, 0x1 = input data 1 is mapped to data bit 3, 0x2 = input data 2 is mapped to data bit 3 and so on.
14:10	SEL_DATA2	Select the Data bit 2 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 2, 0x1 = input data 1 is mapped to data bit 2, 0x2 = input data 2 is mapped to data bit 2 and so on.
9:5	SEL_DATA1	Select the Data bit 1 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 1, 0x1 = input data 1 is mapped to data bit 1, 0x2 = input data 2 is mapped to data bit 1 and so on.
4:0	SEL_DATA0	Select the Data bit 0 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 0, 0x1 = input data 1 is mapped to data bit 0, 0x2 = input data 2 is mapped to data bit 0 and so on.

0x0590080C VCAP_VCAP_VC_IN_CRTL2

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x16A4A0E6

This register has the mux control for DATA6,DATA7,DATA8,DATA9,DATA10 and DATA11

VCAP_VCAP_VC_IN_CRTL2

Bits	Name	Description
31:30	UNUSED	
29:25	SEL_DATA11	Select the Data bit 11 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 11, 0x1 = input data 1 is mapped to data bit 11, 0x2 = input data 2 is mapped to data bit 11 and so on.
24:20	SEL_DATA10	Select the Data bit 10 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 10, 0x1 = input data 1 is mapped to data bit 10, 0x2 = input data 2 is mapped to data bit 10 and so on.
19:15	SEL_DATA9	Select the Data bit 9 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 9, 0x1 = input data 1 is mapped to data bit 9, 0x2 = input data 2 is mapped to data bit 9 and so on.
14:10	SEL_DATA8	Select the Data bit 8 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 8, 0x1 = input data 1 is mapped to data bit 8, 0x2 = input data 2 is mapped to data bit 8 and so on.

VCAP_VCAP_VC_IN_CRTL2 (cont.)

Bits	Name	Description
9:5	SEL_DATA7	Select the Data bit 7 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 7, 0x1 = input data 1 is mapped to data bit 7, 0x2 = input data 2 is mapped to data bit 7 and so on.
4:0	SEL_DATA6	Select the Data bit 6 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 6, 0x1 = input data 1 is mapped to data bit 6, 0x2 = input data 2 is mapped to data bit 6 and so on.

0x05900810 VCAP_VCAP_VC_IN_CRTL3

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x2307B9AC

This register has the mux control for DATA12,DATA13,DATA14,DATA15,DATA16 and DATA17

VCAP_VCAP_VC_IN_CRTL3

Bits	Name	Description
31:30	UNUSED	
29:25	SEL_DATA17	Select the Data bit 17 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 17, 0x1 = input data 1 is mapped to data bit 17, 0x2 = input data 2 is mapped to data bit 17 and so on.
24:20	SEL_DATA16	Select the Data bit 16 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 16, 0x1 = input data 1 is mapped to data bit 16, 0x2 = input data 2 is mapped to data bit 16 and so on.
19:15	SEL_DATA15	Select the Data bit 15 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 15, 0x1 = input data 1 is mapped to data bit 15, 0x2 = input data 2 is mapped to data bit 15 and so on.
14:10	SEL_DATA14	Select the Data bit 14 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 14, 0x1 = input data 1 is mapped to data bit 14, 0x2 = input data 2 is mapped to data bit 14 and so on.
9:5	SEL_DATA13	Select the Data bit 13 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 13, 0x1 = input data 1 is mapped to data bit 13, 0x2 = input data 2 is mapped to data bit 13 and so on.

VCAP_VCAP_VC_IN_CRTL3 (cont.)

Bits	Name	Description
4:0	SEL_DATA12	Select the Data bit 12 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 12, 0x1 = input data 1 is mapped to data bit 12, 0x2 = input data 2 is mapped to data bit 12 and so on.

0x05900814 VCAP_VCAP_VC_IN_CRTL4

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x2F6AD272

This register has the mux control for DATA18,DATA19,DATA20,DATA21,DATA22 and DATA23

VCAP_VCAP_VC_IN_CRTL4

Bits	Name	Description
31:30	UNUSED	
29:25	SEL_DATA23	Select the Data bit 23 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 23, 0x1 = input data 1 is mapped to data bit 23, 0x2 = input data 2 is mapped to data bit 23 and so on.
24:20	SEL_DATA22	Select the Data bit 22 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 22, 0x1 = input data 1 is mapped to data bit 22, 0x2 = input data 2 is mapped to data bit 22 and so on.
19:15	SEL_DATA21	Select the Data bit 21 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 21, 0x1 = input data 1 is mapped to data bit 21, 0x2 = input data 2 is mapped to data bit 21 and so on.
14:10	SEL_DATA20	Select the Data bit 20 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 20, 0x1 = input data 1 is mapped to data bit 20, 0x2 = input data 2 is mapped to data bit 20 and so on.
9:5	SEL_DATA19	Select the Data bit 19 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 19, 0x1 = input data 1 is mapped to data bit 19, 0x2 = input data 2 is mapped to data bit 19 and so on.
4:0	SEL_DATA18	Select the Data bit 18 from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to data bit 18, 0x1 = input data 1 is mapped to data bit 18, 0x2 = input data 2 is mapped to data bit 18 and so on.

0x05900818 VCAP_VCAP_VC_IN_CRTL5

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00006B38

This register had the mux control for VSYNC, HSYNC and DE

VCAP_VCAP_VC_IN_CRTL5

Bits	Name	Description
31:15	UNUSED	
14:10	SEL_DATA26	Select the HSYNC from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to HSYNC, 0x1 = input data 1 is mapped to HSYNC, 0x2 = input data 2 is mapped to HSYNC and so on.
9:5	SEL_DATA25	Select the VSYNC from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to VSYNC, 0x1 = input data 1 is mapped to VSYNC, 0x2 = input data 2 is mapped to VSYNC and so on.
4:0	SEL_DATA24	Select the DATA_ENABLE (DE) from incoming 27 bit bus. Entries from 0 - 27 are valid options for this field. 0x0= input data 0 is mapped to DE, 0x1 = input data 1 is mapped to DE, 0x2 = input data 2 is mapped to DE and so on.

0x0590081C VCAP_VCAP_VC_POL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to select the polarity for incoming hsync vsync and DE

VCAP_VCAP_VC_POL

Bits	Name	Description
31:9	UNUSED_1	
8	DE_POL	Data enable polarity, 0 = Active Hi, 1 = active lo
7:5	UNUSED_2	
4	HSYNC_POL	Hsync polarity, 0 = Active Hi, 1= active lo
3:1	UNUSED	
0	VSYNC_POL	Vsync polarity, 0 = Active Hi, 1= active lo

0x05900820 VCAP_VCAP_VC_V_H_TOTAL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to configure the Horizontal and vertical totals for the timing engine in the parser block. THis will be used to detect various errors specified in STATUS registers. These fields are programmed as per the timing spec of input resolution, either spec-ed in CEA or VESA spec

VCAP_VCAP_VC_V_H_TOTAL

Bits	Name	Description
31:28	UNUSED_1	
27:16	HTOTAL	Horizontal total for a given resolution. The unit for this field is in number of pixels for a given resolution
15:12	UNUSED_2	
11:0	VTOTAL	Vertical total for a given resolution. The unit for this field is in number of lines for a given resolution

0x05900824 VCAP_VCAP_VC_H_ACTIVE

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to configure the Horizontal active window in pixels for the timing engine in the parser block. THis will be used to detect various errors specified in STATUS registers. These fields are programmed as per the timing spec of input resolution, either spec-ed in CEA or VESA spec

VCAP_VCAP_VC_H_ACTIVE

Bits	Name	Description
31:28	UNUSED_1	
27:16	END	Horizontal active window end in pixels
15:12	UNUSED_2	
11:0	START	Horizontal active window start in pixels

0x05900828 VCAP_VCAP_VC_V_ACTIVE

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to configure the Vertical active window in lines for the timing engine in the parser block. This will be used to detect various errors specified in STATUS registers. These fields are programmed as per the timing spec of input resolution, either spec-ed in CEA or VESA spec

VCAP_VCAP_VC_V_ACTIVE

Bits	Name	Description
31:28	UNUSED_1	
27:16	END	Vertical active window end in lines
15:12	UNUSED_2	
11:0	START	Vertical active window start in lines

0x05900830 VCAP_VCAP_VC_V_ACTIVE_F2

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to configure the Vertical active window in lines for the timing engine in the parser block for interlace format. This will be used to detect various errors specified in STATUS registers. These fields are programmed as per the timing spec of input resolution, either spec-ed in CEA or VESA spec

VCAP_VCAP_VC_V_ACTIVE_F2

Bits	Name	Description
31:28	UNUSED_1	
27:16	END	Vertical active window end in lines for Field 2 of interlace format.
15:12	UNUSED_2	
11:0	START	Vertical active window start in lines for Field 2 of interlace format.

0x05900834 VCAP_VCAP_VC_VSYNC_VPOS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to configure the Vertical position in lines of vsync. THis will be used by timing engine in the parser block to detect various errors specified in STATUS registers. These fields are programmed as per the timing spec of input resolution, either spec-ed in CEA or VESA spec

VCAP_VCAP_VC_VSYNC_VPOS

Bits	Name	Description
31:28	UNUSED_1	
27:16	END	Vertical end line of VSYNC
15:12	UNUSED_2	
11:0	START	Vertical start line of VSYNC

0x05900840 VCAP_VCAP_VC_HSYNC_HPOS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to configure the horizontal position in pixels of hsync. This will be used by timing engine in the parser block to detect various errors specified in STATUS registers. These fields are programmed as per the timing spec of input resolution, either spec-ed in CEA or VESA spec

VCAP_VCAP_VC_HSYNC_HPOS

Bits	Name	Description
31:28	UNUSED_1	
27:16	END	Horizontal end pixel of HSYNC
15:12	UNUSED_2	
11:0	START	Horizontal start pixel of HSYNC

0x05900838 VCAP_VCAP_VC_VSYNC_F2_VPOS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to configure the Vertical position in lines of vsync for Field 2 of interlace format. THis will be used by timing engine in the parser block to detect various errors specified in STATUS registers. These fields are programmed as per the timing spec of input resolution, either spec-ed in CEA or VESA spec

VCAP_VCAP_VC_VSYNC_F2_VPOS

Bits	Name	Description
31:28	UNUSED_1	
27:16	END	Vertical end line of VSYNC for Field 2 of interlace format.
15:12	UNUSED_2	
11:0	START	Vertical start line of VSYNC for Field 2 of interlace format.

0x0590083C VCAP_VCAP_VC_VSYNC_F2_HPOS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to configure the Horizontal position in pixel of vsync for Field 2 of interlace format. THis will be used by timing engine in the parser block to detect various errors specified in STATUS registers. These fields are programmed as per the timing spec of input resolution, either spec-ed in CEA or VESA spec

VCAP_VCAP_VC_VSYNC_F2_HPOS

Bits	Name	Description
31:28	UNUSED_1	
27:16	END	Horizontal end pixel of VSYNC for Field 2 of interlace format.
15:12	UNUSED_2	
11:0	START	Horizontal start pixel of VSYNC for Field 2 of interlace format.

0x05900848 VCAP_VCAP_VC_BUF_CTRL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00007711

This register is used to program the maximum pending requests for Y and C

VCAP_VCAP_VC_BUF_CTRL

Bits	Name	Description
31:15	UNUSED_1	

VCAP_VCAP_VC_BUF_CTRL (cont.)

Bits	Name	Description
14:12	C_BURST_SIZE	C burst size. Max burst = 0x3. Burst programed to 0x0 is burst of 1. Burst programmed to 0x1 is burst of 2.Burst programed to 0x2 is burst of 3. Burst programed to 0x3 is burst of 4. Burst programmed to 0x7 is burst of 8. Only burst sizes of 1,2,3,4 and 8 are supported.
11	UNUSED_2	
10:8	Y_BURST_SIZE	Y burst size. Max burst = 0x7, Burst programed to 0x0 is burst of 1. Burst programmed to 0x1 is burst of 2.Burst programed to 0x2 is burst of 3. Burst programed to 0x3 is burst of 4. Burst Programmed to 0x7 is burst of 8. Only burst sizes of 1,2,3,4 and 8 are supported.
7:4	C_PENDING_REQ	Maximum Pending requests for C
3:0	Y_PENDING_REQ	Maximum Pending requests for Y

0x0590084C VCAP_VCAP_VC_Y_STRIDE

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the Stride for Y

VCAP_VCAP_VC_Y_STRIDE

Bits	Name	Description
31:15	UNUSED	
14:0	STRIDE	Stride for Y plane. Address calculation will be offset + line*stride.

0x05900850 VCAP_VCAP_VC_C_STRIDE

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the Stride for C

VCAP_VCAP_VC_C_STRIDE

Bits	Name	Description
31:15	UNUSED	
14:0	STRIDE	Stride for C plane. Address calculation will be offset + line*stride.

0x05900854 VCAP_VCAP_VC_Y_ADDR_1

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the start address of the first Y/RGB data buffer to be sent through VBIF to memory. This is 128 bits aligned i.e., last 4 bits will be zero-ed out

VCAP_VCAP_VC_Y_ADDR_1

Bits	Name	Description
31:0	OFFSET	Starting address for first Y/RGB data buffer. This field is double buffered, the changes will be effective after the next vsync.

0x05900858 VCAP_VCAP_VC_C_ADDR_1

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the start address of the first C data buffer to be sent through VBIF to memory. This is 128 bits aligned i.e., last 4 bits will be zero-ed out

VCAP_VCAP_VC_C_ADDR_1

Bits	Name	Description
31:0	OFFSET	Starting address for first C data. This field is double buffered, the changes will be effective after the next vsync.

0x0590085C VCAP_VCAP_VC_Y_ADDR_2

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the start address of the second Y/RGB data buffer to be sent through VBIF to memory. This is 128 bits aligned i.e., last 4 bits will be zero-ed out

VCAP_VCAP_VC_Y_ADDR_2

Bits	Name	Description
31:0	OFFSET	Starting address for second Y/RGB data buffer. This field is double buffered, the changes will be effective after the next vsync.

0x05900860 VCAP_VCAP_VC_C_ADDR_2

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the start address of the second C data buffer to be sent through VBIF to memory. This is 128 bits aligned i.e., last 4 bits will be zero-ed out

VCAP_VCAP_VC_C_ADDR_2

Bits	Name	Description
31:0	OFFSET	Starting address for second C data. This field is double buffered, the changes will be effective after the next vsync.

0x05900864 VCAP_VCAP_VC_Y_ADDR_3

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the start address of the third Y/RGB data buffer to be sent through VBIF to memory. This buffer is only used when BUF_EN bit of CTRL register is programmed to 3. This is 128 bits aligned i.e., last 4 bits will be zero-ed out

VCAP_VCAP_VC_Y_ADDR_3

Bits	Name	Description
31:0	OFFSET	Starting address for third Y/RGB data buffer. This field is double buffered, the changes will be effective after the next vsync.

0x05900868 VCAP_VCAP_VC_C_ADDR_3

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the start address of the third C data buffer to be sent through VBIF to memory. This buffer is only used when BUF_THREE_EN bit of CTRL register is programmed to 3.This is 128 bits aligned i.e., last 4 bits will be zero-ed out

VCAP_VCAP_VC_C_ADDR_3

Bits	Name	Description
31:0	OFFSET	Starting address for third C data. This field is double buffered, the changes will be effective after the next vsync.

0x0590086C VCAP_VCAP_VC_Y_ADDR_4

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the start address of the fourth Y/RGB data buffer to be sent through VBIF to memory. This buffer is only used when BUF_THREE_EN bit of CTRL register is programmed to 4.This is 128 bits aligned i.e., last 4 bits will be zero-ed out

VCAP_VCAP_VC_Y_ADDR_4

Bits	Name	Description
31:0	OFFSET	Starting address for fourth Y/RGB data buffer. This field is double buffered, the changes will be effective after the next vsync.

0x05900870 VCAP_VCAP_VC_C_ADDR_4

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the start address of the fourth C data buffer to be sent through VBIF to memory. This buffer is only used when BUF_THREE_EN bit of CTRL register is programmed to 4.This is 128 bits aligned i.e., last 4 bits will be zero-ed out

VCAP_VCAP_VC_C_ADDR_4

Bits	Name	Description
31:0	OFFSET	Starting address for fourth C data. This field is double buffered, the changes will be effective after the next vsync.

0x05900874 VCAP_VCAP_VC_Y_ADDR_5

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the start address of the fifth Y/RGB data buffer to be sent through VBIF to memory. This buffer is only used when BUF_THREE_EN bit of CTRL register is programmed to 5. This is 128 bits aligned i.e., last 4 bits will be zero-ed out

VCAP_VCAP_VC_Y_ADDR_5

Bits	Name	Description
31:0	OFFSET	Starting address for fifth Y/RGB data buffer. This field is double buffered, the changes will be effective after the next vsync.

0x05900878 VCAP_VCAP_VC_C_ADDR_5

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the start address of the fifth C data buffer to be sent through VBIF to memory. This buffer is only used when BUF_THREE_EN bit of CTRL reigster is programmed to 5.This is 128 bits aligned i.e., last 4 bits will be zero-ed out

VCAP_VCAP_VC_C_ADDR_5

Bits	Name	Description
31:0	OFFSET	Starting address for fifth C data. This field is double buffered, the changes will be effective after the next vsync.

0x0590087C VCAP_VCAP_VC_Y_ADDR_6

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the start address of the sixth Y/RGB data buffer to be sent through VBIF to memory. This buffer is only used when BUF_THREE_EN bit of CTRL reigster is programmed to 6. This is 128 bits aligned i.e., last 4 bits will be zero-ed out

VCAP_VCAP_VC_Y_ADDR_6

Bits	Name	Description
31:0	OFFSET	Starting address for sixth Y/RGB data buffer. This field is double buffered, the changes will be effective after the next vsync.

0x05900880 VCAP_VCAP_VC_C_ADDR_6

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the start address of the sixth C data buffer to be sent through VBIF to memory. This buffer is only used when BUF_THREE_EN bit of CTRL reigster is programmed to 6.This is 128 bits aligned i.e., last 4 bits will be zero-ed out

VCAP_VCAP_VC_C_ADDR_6

Bits	Name	Description
31:0	OFFSET	Starting address for sixth C data. This field is double buffered, the changes will be effective after the next vsync.

0x05900884 VCAP_VCAP_VC_INT_MASK

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Interrupt Control

VCAP_VCAP_VC_INT_MASK

Bits	Name	Description
31:13	UNUSED_1	
12	VSYNC_SEQ_ERR_MASK	This field is used to mask the VSYNC_SEQ_ERR_INT interrupt
11	NPL_OVERFLOW_MASK	This field is used to mask the NPL_OVERFLOW_INT interrupt which reflects the interrupt for NPL fifo overflow
10	LBUF_OVERFLOW_MASK	This field is used to mask the BUF_ERROR_INT in STATUS register
9	PARSER_ERR_MASK	This field is used to mask the parser error interrupt.
8:7	UNUSED_2	
6	BUF6_WRITTEN_MASK	This field is used to mask the buffer 6 written indication interrupt
5	BUF5_WRITTEN_MASK	This field is used to mask the buffer 5 written indication interrupt
4	BUF4_WRITTEN_MASK	This field is used to mask the buffer 4 written indication interrupt
3	BUF3_WRITTEN_MASK	This field is used to mask the buffer 3 written indication interrupt
2	BUF2_WRITTEN_MASK	This field is used to mask the buffer 2 written indication interrupt
1	BUF1_WRITTEN_MASK	This field is used to mask the buffer 1 written indication interrupt
0	VSYNC_INT_MASK	This field is used to mask the VSYNC_INT interrupt

0x05900888 VCAP_VCAP_VC_INT_CLEAR

Type: Write
Clock: UNDEFINED
Reset State: 0x00000000

Interrupt Control

VCAP_VCAP_VC_INT_CLEAR

Bits	Name	Description
31:13	UNUSED_1	
12	VSYNC_SEQ_ERR_ACK	WRITE ONLY This field is used to clear the VSYNC_SEQ_ERR_INT in status register.
11	NPL_OVERLFOW_ACK	WRITE ONLY This field is used to clear the NPL_OVERFLOW_INT in status register.
10	LBUF_OVERFLOW_ACK	WRITE ONLY This field is used to clear the BUF_ERROR_INT status in STATUS register
9	PARSER_ERR_ACK	WRITE ONLY This field is used to clear the PARSER_ERR_INT in status register which reflects error while parsing, AKA, Vsync/Line/Pixel error
8:7	UNUSED_2	
6	BUF6_WRITTEN_ACK	WRITE ONLY This field is used to clear the Buffer 6 written interrupt status. Acknowledging will indicate the SW has picked up the buffer 6
5	BUF5_WRITTEN_ACK	WRITE ONLY This field is used to clear the Buffer 5 written interrupt status. Acknowledging will indicate the SW has picked up the buffer 5
4	BUF4_WRITTEN_ACK	WRITE ONLY This field is used to clear the Buffer 4 written interrupt status. Acknowledging will also indicate the SW has picked up the buffer 4
3	BUF3_WRITTEN_ACK	WRITE ONLY This field is used to clear the Buffer 3 written interrupt status. Acknowledging will indicate the SW has picked up the buffer 3
2	BUF2_WRITTEN_ACK	WRITE ONLY This field is used to clear the Buffer 2 written interrupt status. Acknowledging will indicate the SW has picked up the buffer 2
1	BUF1_WRITTEN_ACK	WRITE ONLY This field is used to clear the Buffer 1 written interrupt status. Acknowledging will also indicate the SW has picked up the buffer 1
0	VSYNC_INT_ACK	WRITE ONLY This field is used to clear the vsync interrupt status

0x0590088C VCAP_VCAP_VC_STATUS

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to read various error conditions and interrupts

VCAP_VCAP_VC_STATUS

Bits	Name	Description
31	PIXEL_ERROR	READ ONLY This is read only field, Value of 1 indicated that the pixel error has occurred meaning the captured active horizontal window is not as per the parameters programmed in VCAP_VC_H_ACTIVE register
30	LINE_ERROR	READ ONLY This is read only field, Value of 1 indicates that the line error has occurred meaning, the captured active vertical window is not as per the parameters programed in VCAP_VC_V_ACTIVE register
29	VSYNC_ERROR	READ ONLY This is read only field, Value of 1 indicates that either VSYNC is not captured in the expected line/time, or it is not captured at all when expected
28:13	UNUSED_1	
12	VSYNC_SEQ_ERR_INT	READ ONLY This interrupt indicates that the Vsync happened before the frame done interrupt
11	NPL_OVERFLOW_INT	READ ONLY This interrupt indicates that fifo in the VCAP_NPL module has overflowed.
10	LBUF_OVERFLOW_INT	READ ONLY This interrupt indicates that the latency buffer is overflowed. In this scenario, The whole engine needs to be soft reset.
9	PARSER_ERR_INT	READ ONLY This interrupt indicates that there is an error encountered by capturing the incoming frame data. Parser error interrupt reflects either, Vsync error i.e., Vsync not capture in expected line/time, Pixel error i.e., active line captured is not as per the active line width programmed, line error i.e., Total number of active lines captured are not as per the number of active lines programmed, Fields VSYNC_ERROR, LINE_ERROR and PIXEL_ERROR of STATUS_1 register will indicate which type of error happened.
8:7	UNUSED_2	

VCAP_VCAP_VC_STATUS (cont.)

Bits	Name	Description
6	BUF6_WRITTEN_INT	READ ONLY This interrupt indicates that Buffer 3 with starting address programmed in Y_ADDR_6/C_ADDR_6 registers has been written in the memory and is ready to be picked up. Software will clear this interrupt by writing 1 to BUF6_WRITTEN_ACK field in INT_CLEAR register. If this interrupt is not cleared hardware will conclude that the buffer is not picked up by software. It will then either overwrite the present buffer or drop the currently captured frame depending on the mode programmed in FRAME_OVERWRITE_EN field on CTRL register.
5	BUF5_WRITTEN_INT	READ ONLY This interrupt indicates that Buffer 2 with starting address programmed in Y_ADDR_5/C_ADDR_5 registers has been written in the memory and is ready to be picked up. Software will clear this interrupt by writing 1 to BUF5_WRITTEN_ACK field in INT_CLEAR register. If this interrupt is not cleared hardware will conclude that the buffer is not picked up by software. It will then either overwrite the present buffer or drop the currently captured frame depending on the mode programmed in FRAME_OVERWRITE_EN field on CTRL register.
4	BUF4_WRITTEN_INT	READ ONLY This interrupt indicates that Buffer 1 with starting address programmed in Y_ADDR_4/C_ADDR_4 registers has been written in the memory and is ready to be picked up. Software will clear this interrupt by writing 1 to BUF4_WRITTEN_ACK field in INT_CLEAR register. If this interrupt is not cleared hardware will conclude that the buffer is not picked up by software. It will then either overwrite the present buffer or drop the currently captured frame depending on the mode programmed in FRAME_OVERWRITE_EN field on CTRL register.
3	BUF3_WRITTEN_INT	READ ONLY This interrupt indicates that Buffer 3 with starting address programmed in Y_ADDR_3/C_ADDR_3 registers has been written in the memory and is ready to be picked up. Software will clear this interrupt by writing 1 to BUF3_WRITTEN_ACK field in INT_CTRL register. If this interrupt is not cleared hardware will conclude that the buffer is not picked up by software. It will then either overwrite the present buffer or drop the currently captured frame depending on the mode programmed in FRAME_OVERWRITE_EN field on CTRL register.
2	BUF2_WRITTEN_INT	READ ONLY This interrupt indicates that Buffer 2 with starting address programmed in Y_ADDR_2/C_ADDR_2 registers has been written in the memory and is ready to be picked up. Software will clear this interrupt by writing 1 to BUF2_WRITTEN_ACK field in INT_CTRL register. If this interrupt is not cleared hardware will conclude that the buffer is not picked up by software. It will then either overwrite the present buffer or drop the currently captured frame depending on the mode programmed in FRAME_OVERWRITE_EN field on CTRL register.

VCAP_VCAP_VC_STATUS (cont.)

Bits	Name	Description
1	BUF1_WRITTEN_INT	READ ONLY This interrupt indicates that Buffer 1 with starting address programmed in Y_ADDR_1/C_ADDR_1 registers has been written in the memory and is ready to be picked up. Software will clear this interrupt by writing 1 to BUF1_WRITTEN_ACK field in INT_CTRL register. If this interrupt is not cleared hardware will conclude that the buffer is not picked up by software. It will then either overwrite the present buffer or drop the currently captured frame depending on the mode programmed in FRAME_OVERWRITE_EN field on CTRL register.
0	VSYNC_INT	READ ONLY This interrupt indicates that the vsync is captured in the incoming stream of data from external HDMI receiver part. This interrupt is frame based, i.e., in case of interlace or progressive inputs it will indicate every frame captured.

0x05900890 VCAP_VCAP_VC_BIST_CTRL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to configure the bist for vcap_vc

VCAP_VCAP_VC_BIST_CTRL

Bits	Name	Description
31:16	UNUSED_1	
15:8	PAT_SEL	Pattern select for bist. 0x0=All Black color, 0x1= pattern from BPAT field of VCAP_VC_BIST_PATTERN register is selected, 0x2= Ramp, 0x3= All White, 0x4 = color bar pattern
7:1	UNUSED_2	
0	BIST_EN	This field enables the bist circuit. 0=disable, 1= enable

0x05900894 VCAP_VCAP_VC_BIST_PATTERN

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the bist pattern

VCAP_VCAP_VC_BIST_PATTERN

Bits	Name	Description
31:24	UNUSED	
23:0	BPAT	This field is used to program the pattern to be sent out when bist is enabled. THis pattern will go out when PAT_SEL field of BIST_CTRL register is programmed to 0x1

0x05900898 VCAP_VCAP_VC_VSYNC_ERROR_WIN

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the VSYNC window error detection for Progressive formats and Field 1 of interlace formats

VCAP_VCAP_VC_VSYNC_ERROR_WIN

Bits	Name	Description
31:28	UNUSED_1	
27:16	VSYNC_ERR_END	End line of the Vsync window error detection
15:12	UNUSED_2	
11:0	VSYNC_ERR_START	Start line of the Vsync window error detection

0x0590089C VCAP_VCAP_VC_VSYNC_F2_ERROR_WIN

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used to program the VSYNC window error detection for field 2 of interlace formats

VCAP_VCAP_VC_VSYNC_F2_ERROR_WIN

Bits	Name	Description
31:28	UNUSED_1	
27:16	VSYNC_ERR_END	End line of the Vsync window error detection
15:12	UNUSED_2	
11:0	VSYNC_ERR_START	Start line of the Vsync window error detection

0x059008A0 VCAP_VCAP_VC_VC_DEBUG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

This register is used for debug purposes

VCAP_VCAP_VC_VC_DEBUG

Bits	Name	Description
31:0	DEBUG	Debug field for VCAP_VC

14.19.3 VBIF core Register Set

VBIF core Control Registers

0x05900C00 VCAP_VCAP_VBIF_VERSION

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Hardware version of the VBIF core which is embedded in this core.

VCAP_VCAP_VBIF_VERSION

Bits	Name	Description
31:16	UNUSED	
15:0	VBIF_VERSION	READ ONLY Hardware version of the VBIF core which is embedded in this core. Read-only field.

0x05900CB0 VCAP_VCAP_VBIF_IN_RD_LIM_CONF0

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00001010

The maximum number of pending reads from each Client is programmable.

VCAP_VCAP_VBIF_IN_RD_LIM_CONF0

Bits	Name	Description
31:16	UNUSED	
15:8	IN_RD_LIM_C1	The maximum number of pending reads from Client 1. Must be <= the HW parameter that XBAR_IN_RD_LIM
7:0	IN_RD_LIM_C0	The maximum number of pending reads from Client 0. Must be <= the HW parameter that XBAR_IN_RD_LIM

0x05900CC0 VCAP_VCAP_VBIF_IN_WR_LIM_CONF0

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00001010

The maximum number of pending writes from each Client is programmable.

VCAP_VCAP_VBIF_IN_WR_LIM_CONF0

Bits	Name	Description
31:16	UNUSED	
15:8	IN_WR_LIM_C1	The maximum number of pending writes from Client 1. Must be <= the HW parameter that XBAR_IN_WR_LIM
7:0	IN_WR_LIM_C0	The maximum number of pending writes from Client 0. Must be <= the HW parameter that XBAR_IN_WR_LIM

0x05900CD0 VCAP_VCAP_VBIF_OUT_RD_LIM_CONF0

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000010

The maximum number of pending reads from each AXI is programmable.

VCAP_VCAP_VBIF_OUT_RD_LIM_CONF0

Bits	Name	Description
31:8	UNUSED	
7:0	OUT_RD_LIM_A0	The maximum number of pending reads from AXI 0. Must be <= the HW parameter that XBAR_OUT_RD_LIM

0x05900CD4 VCAP_VCAP_VBIF_OUT_WR_LIM_CONF0

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000010

The maximum number of pending reads from each AXI is programmable.

VCAP_VCAP_VBIF_OUT_WR_LIM_CONF0

Bits	Name	Description
31:8	UNUSED	
7:0	OUT_WR_LIM_A0	The maximum number of pending writes from AXI 0. Must be <= the HW parameter that XBAR_OUT_WR_LIM

0x05900CD8 VCAP_VCAP_VBIF_DDR_OUT_MAX_BURST

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000707

The maximum burst length from any DDR AXI is programmable.

The client bursts will be broken up according to these limits, although the client will not be aware of it.

VCAP_VCAP_VBIF_DDR_OUT_MAX_BURST

Bits	Name	Description
31:16	UNUSED	
15:8	DDR_OUT_MAX_WR_BURST	The maximum number of write beats minus 1 allowed on the AXI bus (arbiter outputs). Must be < the HW parameter that XBAR_OUT_WR_BURST
7:0	DDR_OUT_MAX_RD_BURST	The maximum number of read beats minus 1 allowed on the AXI bus (arbiter outputs). Must be < the HW parameter that XBAR_OUT_RD_BURST

0x05900CE0 VCAP_VCAP_VBIF_ISO_SYNC

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Enables iso-sync operation between client and arbiter, 1-bit per client. Client & AXI clocks must be iso-sync and have balanced clock trees.

VCAP_VCAP_VBIF_ISO_SYNC

Bits	Name	Description
31:2	UNUSED	
1	ISO_SYNC_C1	Enables for Client 1 0x0: Disable 0x1: Enable
0	ISO_SYNC_C0	Enables for Client 0 0x0: Disable 0x1: Enable

0x05900CF0 VCAP_VCAP_VBIF_ARB_CTL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000001

Each arbiter can be programmed to utilize fixed priority, slave-aware or Round-Robin arbitration

VCAP_VCAP_VBIF_ARB_CTL

Bits	Name	Description
31:5	UNUSED_1	
4	ROUND_ROBIN_ARB_EN_A0	Enables Round-Robin arbitration for AXI port 0. If enabled, Slave-Aware and Longest-Time-Waiting arbitrations are ignored. 0x0: Disable 0x1: Enable
3:1	UNUSED_2	
0	FIXED_ARB_EN_A0	Enables fixed priority arbitration for AXI port 0. If enabled, the other arbitrations are ignored 0x0: Disable 0x1: Enable

0x05900CF4 VCAP_VCAP_VBIF_DDR_ARB_CONF0

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Client limits for DDR AXI, 5 bits per client.

Each client limit is the maximum number of consecutive grants minus 1 to give that client before allowing requests from other clients.

This is used for slave-aware, round-robin and longest-time-waiting arbitration, but not fixed priority arbitration.

VCAP_VCAP_VBIF_DDR_ARB_CONF0

Bits	Name	Description
31:10	UNUSED	
9:5	DDR_CLIENT_LIM_C1	Client limits for Client 1
4:0	DDR_CLIENT_LIM_C0	Client limits for Client 0

0x05900D00 VCAP_VCAP_VBIF_FIXED_ARB_CONF0

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000010

A list of Client number for Fixed arbitration

The highest priority client number on highest number of register name.

For example, If total number of clients is 12, and client2 has highest priority

should be wirte 2 into FIXED_ARB_LIST_11. and ignore LIST_12	15. Bits	
31:8	UNUSED	
7:4	FIXED_ARB_LIST_1	A list of Client number for Fixed arbitration
3:0	FIXED_ARB_LIST_0	A list of Client number for Fixed arbitration

VCAP_VCAP_VBIF_FIXED_ARB_CONF0

Bits	Name	Description

0x05900D60 VCAP_VCAP_VBIF_OUT_AXI_AMEMTYPE_CONF0

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000022

When a request is finally granted, this AXI signal is controlled on a per-client basis.

This is driven to AXI port but does not directly impact VBIF functionality.

VCAP_VCAP_VBIF_OUT_AXI_AMEMTYPE_CONF0

Bits	Name	Description
31:7	UNUSED_1	
6:4	AXI_AMEMTYPE_C1	AMEMTYPE signal for Client 1
3	UNUSED_2	
2:0	AXI_AMEMTYPE_C0	AMEMTYPE signal for Client 0

0x05900D68 VCAP_VCAP_VBIF_OUT_AXI_APROTNS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000003

When a request is finally granted, this AXI signal is controlled on a per-client basis.

This is driven to AXI port but does not directly impact VBIF functionality.

VCAP_VCAP_VBIF_OUT_AXI_APROTNS

Bits	Name	Description
31:2	UNUSED	
1	AXI_APROTNS_C1	APROTNS signal for Client 1
0	AXI_APROTNS_C0	APROTNS signal for Client 0

0x05900D6C VCAP_VCAP_VBIF_OUT_AXI_AINST

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

When a request is finally granted, this AXI signal is controlled on a per-client basis.

This is driven to AXI port but does not directly impact VBIF functionality.

VCAP_VCAP_VBIF_OUT_AXI_AINST

Bits	Name	Description
31:2	UNUSED	
1	AXI_AINST_C1	AINST signal for Client 1

VCAP_VCAP_VBIF_OUT_AXI_AINST (cont.)

Bits	Name	Description
0	AXI_AINST_C0	AINST signal for Client 0

0x05900D70 VCAP_VCAP_VBIF_OUT_AXI_ASHARED

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

When a request is finally granted, this AXI signal is controlled on a per-client basis.

This is driven to AXI port but does not directly impact VBIF functionality.

VCAP_VCAP_VBIF_OUT_AXI_ASHARED

Bits	Name	Description
31:2	UNUSED	
1	AXI_ASHARED_C1	ASHARED signal for Client 1
0	AXI_ASHARED_C0	ASHARED signal for Client 0

0x05900D74 VCAP_VCAP_VBIF_OUT_AXI_AINNERSHARED

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

When a request is finally granted, this AXI signal is controlled on a per-client basis.

This is driven to AXI port but does not directly impact VBIF functionality.

VCAP_VCAP_VBIF_OUT_AXI_AINNERSHARED

Bits	Name	Description
31:2	UNUSED	
1	AXI_AINNERSHARED_C1	AINNERSHARED signal for Client 1
0	AXI_AINNERSHARED_C0	AINNERSHARED signal for Client 0

0x05900D78 VCAP_VCAP_VBIF_OUT_AXI_AOOO_EN

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Enable signal for controlling AOOOWR/AOOORD signals on AXI protocol, this signal is controlled on a per-client basis.

Actually, AOOOWR/RD signals are controlled by parent core (via client I/F port) dynamically.

But, it can be controlled by SW for performance test, debugging, etc

If enable this register, ignore Cooo value of client port and SW value applies to AOOO signal.

VCAP_VCAP_VBIF_OUT_AXI_AOOO_EN

Bits	Name	Description
31:2	UNUSED	
1	AXI_AOOO_EN_C1	SW AOOOAOOO_EN signal for Client 1
0	AXI_AOOO_EN_C0	SW AOOO enable signal for Client 0

0x05900D7C VCAP_VCAP_VBIF_OUT_AXI_AOOO

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

When a request is finally granted and AXI_AOOO_EN is enabled, this AXI signal is controlled on a per-client basis.

If AXI_AOOO_EN is disable, ignore this value.

VCAP_VCAP_VBIF_OUT_AXI_AOOO

Bits	Name	Description
31:18	UNUSED_1	
17	AXI_AOOORD_C1	AOOORD signal for Client 1 if AXI_AOOO_EN_C1
16	AXI_AOOORD_C0	AOOORD signal for Client 0 if AXI_AOOO_EN_C0
15:2	UNUSED_2	
1	AXI_AOOOWR_C1	AOOOWR signal for Client 1 if AXI_AOOO_EN_C1
0	AXI_AOOOWR_C0	AOOOWR signal for Client 0 if AXI_AOOO_EN_C0

0x05900D80 VCAP_VCAP_VBIF_OUT_AXI_ANOALLOCATE

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

When a request is finally granted, this AXI signal is controlled on a per-client basis.

This is driven to AXI port but does not directly impact VBIF functionality.

VCAP_VCAP_VBIF_OUT_AXI_ANOALLOCATE

Bits	Name	Description
31:2	UNUSED	
1	AXI_ANOALLOCATE_C1	ANOALLOCATE signal for Client 1
0	AXI_ANOALLOCATE_C0	ANOALLOCATE signal for Client 0

0x05900D84 VCAP_VCAP_VBIF_WD_TIMEOUT

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Write Data Timeout function. enable bit per Client.

Each Client block generate a interrupt when write data timeout with enabled.

VCAP_VCAP_VBIF_WD_TIMEOUT

Bits	Name	Description
31:20	UNUSED_1	
19:16	WD_TIMEOUT_LOG2	This field (shared by all Clients) contains log2(write data timeout), i.e., the bit number of the timeout counter which, when 1, will trigger the timeout. For example, 15 here means the timeout is 32768 AXI clock cycles. This field is ignored when AXI_WD_TIMEOUT_EN=0
15:2	UNUSED_2	
1	WD_TIMEOUT_EN_C1	Write Data Timeout enable for Client 1
0	WD_TIMEOUT_EN_C0	Write Data Timeout enable for Client 0

0x05900D90 VCAP_VCAP_VBIF_PND_ERR

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Pending error status. per client

When error is happened and not masked, this register is set to 1.

But masked, not appear in this register.

VCAP_VCAP_VBIF_PND_ERR

Bits	Name	Description
31:2	UNUSED	
1	CLIENT_PND_ERR_C1	READ ONLY Indicates than an error in Client 1 occurred since the last reset or ERR_CLR was set.
0	CLIENT_PND_ERR_C0	READ ONLY Indicates than an error in Client 0 occurred since the last reset or ERR_CLR was set.

0x05900D94 VCAP_VCAP_VBIF_SRC_ERR

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Source error status. per client

When error is happened, this register is set to 1 even if masked.

VCAP_VCAP_VBIF_SRC_ERR

Bits	Name	Description
31:2	UNUSED	
1	CLIENT_SRC_ERR_C1	READ ONLY Indicates than an error in Client 1 occurred since the last reset or ERR_CLR was set.
0	CLIENT_SRC_ERR_C0	READ ONLY Indicates than an error in Client 0 occurred since the last reset or ERR_CLR was set.

0x05900D98 VCAP_VCAP_VBIF_ERR_MASK

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Error Mask. per client.

When this mask register is set to 1, error is not propagated to Interrupt signal port.

But, can check the error within SRC_ERR register and ERR_INFO register.

VCAP_VCAP_VBIF_ERR_MASK

Bits	Name	Description
31:2	UNUSED	
1	CLIENT_ERR_MASK_C1	Error mask for Client 1
0	CLIENT_ERR_MASK_C0	Error mask for Client 0

0x05900D9C VCAP_VCAP_VBIF_ERR_CLR

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Error clear (interrupt clear). per client

After Client error has been captured, this field should be written to 1 in order to clear the previous error and enable future errors to be captured.

NOT need to write to 0, This field will be changed to 0 automatically when error is cleared.

VCAP_VCAP_VBIF_ERR_CLR

Bits	Name	Description
31:2	UNUSED	
1	CLIENT_ERR_CLR_C1	Error Clear for Client 1
0	CLIENT_ERR_CLR_C0	Error Clear for Client 0

0x05900DA0 VCAP_VCAP_VBIF_ERR_INFO

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Error informations. only the first error is captured. The error must be cleared to enable future errors to be captured.

VCAP_VCAP_VBIF_ERR_INFO

Bits	Name	Description
31:24	UNUSED	
23:16	CLIENT_TID	READ ONLY The value on Client TID when the last error occurred.
15:8	CLIENT_MID	READ ONLY The value on Client MID when the last error occurred.
7:6	AXI_RESP	READ ONLY The value of AXI_RRSP or AXI_BRSP when the last error occurred.
5:4	ERR_TYPE	READ ONLY The type of the last error. Read only 0x0: axi_rresp 0x1: axi_bresp 0x2: WD_timeout 0x3: MMU_translation
3:0	CLIENT_SEL	select number of Client to can read follow error info. (type, resp, mid and tid) For example, if this field is 3, can read error information about Client 3 error.

0x05900DB0 VCAP_VCAP_VBIF_AXI_TEST_CTL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

AXI test bus control

VCAP_VCAP_VBIF_AXI_TEST_CTL

Bits	Name	Description
31:21	UNUSED_1	
20	AXI_RD_LAT_REP_EN_A0	when enabled, each beat of read data is replaced with the read access latency - number of AXI cycles from axi_avalid=1 till read data returned with axi_rvalid=1
19:17	UNUSED_2	
16	AXI_MISR_RES_A0	Reset MISR for AXI 0. Need to write 1 and then write 0. Make sure it is high for at least one axi clock rising edge.

VCAP_VCAP_VBIF_AXI_TEST_CTL (cont.)

Bits	Name	Description
15:13	UNUSED_3	
12	AXI_MISR_EN_A0	Enable MISR for AXI 0
11:9	UNUSED_4	
8	AXI_MISR_WD_A0	Select MISR input for AXI 0. - 0 - read data, 1 - write data
7	AXI_CTR_EN	Enable all profiling counters
6	AXI_CTR_RES	Reset all profiling counters (they are also reset by AXI_RESET). Make sure it is high for at least one axi_clk rising edge.
5:4	AXI_TEST_ARB_SEL	Select which AXI to drive AXI_TEST_OUT
3:0	AXI_TEST_OUT_SEL	Select which test data is read via AXI_TEST_OUT

0x05900DB4 VCAP_VCAP_VBIF_AXI_TEST_OUT

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Test bus

VCAP_VCAP_VBIF_AXI_TEST_OUT

Bits	Name	Description
31:0	AXI_TEST_OUT_BUS	READ ONLY The output selected by the TEST_OUT_SEL and TEST_ARB_SEL fields in the AXI_TEST_CTL reg. This is independent of the test bus, which is not accessible by SW unless other SW registers are created for that purpose.

14.20 VCAP SMMU Registers (0x07200000 SMMU_VCAP_BASE)

This section contains the VCAP SMMU registers.

14.20.1 SMMU Global Registers

14.20.1.1 SMMU VMID/CBNDX mapping registers

0x072FF000+ 0x4*n VCAP_SMMU_VCAP_M2VCBRn, n=[0..15]

Type: Read/Write
Clock: AXI_CLK
Reset State: Undefined

SMMU_M2VCBRm registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

VCAP_SMMU_VCAP_M2VCBRn

Bits	Name	Description
31:28	RESERVED_2	
27:25	BPMEMTYPE	(bypass memory type) Supplies the AMEMTYPE attributes for client requests which bypass the System MMU when SMMU_M2VCBRn[BPMTCFG] = 1 See reference section for AMEMTYPE encoding definitions
24	BPMTCFG	(bypass memory type configuration) Governs the memory type (AMEMTYPE) attributes of client requests which bypass the System MMU BPMTCFG = 0 - use AMEMTYPE Bypass requests use AMEMTYPE signal supplied by client master BPMTCFG = 1 - use SMMU_M2VCBRn[BPMEMTYPE] Bypass requests use SMMU_M2VCBRn[BPMEMTYPE] Reset state : 0
23:22	NSCFG	(non-secure configuration) Governs the incoming security designation of client requests NSCFG = 0b00 - use APROTNS Use APROTNS signal supplied by client master NSCFG = 0b01 - reserved NSCFG = 0b10 - secure System MMU ignores APROTNS; treats all requests as secure NSCFG = 0b11 - non-secure System MMU ignores APROTNS; treats all requests as non-secure Reset state : 0

VCAP_SMMU_VCAP_M2VCBRn (cont.)

Bits	Name	Description
21:20	BPSHCFG	(bypass shareability configuration) Governs the shareability realm (ASHARED and AINNERSHARED) attributes of client requests which bypass the System MMU BPSHCFG = 0b00 - use ASHARED and AINNERSHARED Bypass requests use ASHARED and AINNERSHARED signals supplied by client master BPSHCFG = 0b01 - outer-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 0 BPSHCFG = 0b10 - inner-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 1 BPSHCFG = 0b11 - non-shareable Bypass requests set ASHARED = 0, AINNERSHARED = 0 Reset state : 0
19	BPRCNSH	(bypass redirect cacheable-non-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache Reset state : 0
18	BPRCISH	(bypass redirect cacheable-inner-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0
17	BPRCOSH	(bypass redirect cacheable-outer-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0

VCAP_SMMU_VCAP_M2VCBRn (cont.)

Bits	Name	Description
16	BYPASSD	Bypass disable for this index Governs whether or not client port accesses using this mapping table entry are actually permitted to "bypass" the System MMU when such bypass is indicated (either due to CBNDX = 255 or due to the master asserting the "SMMU bypass" input) This field is ignored (and operates as if it were 0) if SMMU_CR[CLIENTPD] is 1 BYPASSD = 0 - bypass enabled Bypass requests truly bypass the System MMU and "pass-through" to the fabric (no translation, access control, or attribute generation) No cycle of latency for System MMU context bank access Bypass request not considered an error Bypass request error not recorded in SMMU_ESR[BYPASS] Bypass error not reported to requesting master SMMU_rpuErrIrptReq interrupt output not asserted Client accesses still reference M2VCBMT to get VMID value for presentation to fabric BYPASSD = 1 - bypass disabled System MMU terminates the access as RAZ/WI Bypass request is considered an error Bypass request error is recorded in SMMU_ESR[BYPASS] If SMMU_CR[RPUERE] is 1, then bypass error reported to requesting master according to the client port bus protocol If SMMU_CR[RPUEIE] is 1, then SMMU_rpuErrIrptReq interrupt output asserted
15:8	CBNDX	Context bank index Context bank index associated with the M2VCBMT index CBNDX = 255 indicates no context bank assigned ("bypass")
7:5	RESERVED_1	
4:0	VMID	Virtual machine ID VMID value associated with the M2VCBMT index Must be programmed consistently with the SMMU_CBACRn[CBVMID] field for the context bank designated by SMMU_M2VCBRm[CBNDX]

14.20.1.2 SMMU context bank access control registers

0x072FF800+ 0x4*n VCAP_SMMU_VCAP_CBACRn, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs configuration port access to the associated context bank registers.

VCAP_SMMU_VCAP_CBACRn

Bits	Name	Description
31:24	IRPTNDX	(interrupt index) Interrupt output number used for context faults associated with this context bank (use SMMU_contextFaultIrptReq[IRPTNDX])
23:21	RESERVED	
20:16	CBVMID	(context bank VMID) Specifies the VMID with which the client masters using the context bank are associated Must be programmed consistently with the M2VCBMT entries that are configured to use the associated context bank This field is used by configuration port commands that need the context bank's VMID value in order to access the TLB (e.g., SMMU_CBn_TLBIVMID, SMMU_CBn_V2Pxx)
15:10	RESERVED_2	
9	RWGE	Read/write global enable. Setting this bit allows access to the context bank registers from any VMID
8	RWE	Read/write enable. Indicates that the RWVMID field is valid.
7:5	RESERVED_1	
4:0	RWVMID	Specifies owner VMID with full read/write access to the registers in the associated context bank "n".

14.20.1.3 SMMU TLB software access registers

0x072FFE00 VCAP_SMMU_VCAP_TLBRSW

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Writing to this address requests that the TLB entry at INDEX be read into the SMMU_TLBTRn registers

VCAP_SMMU_VCAP_TLBRSW

Bits	Name	Description
31:10	RESERVED	

VCAP_SMMU_VCAP_TLBRSW (cont.)

Bits	Name	Description
9:8	TLBBFBS	This field selects the TLB, TFBFB, SLBFB 0x0: Selecting TLB 0x1: Not defined 0x2: Selecting FL BFB 0x3: Selecting SL BFB
7:0	INDEX	TLB index to be read.

0x072FFE80 VCAP_SMMU_VCAP_TLBTR0

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

This register holds part of TLB entry read by the last TLBRSW command.

VCAP_SMMU_VCAP_TLBTR0

Bits	Name	Description
31:23	RESERVED_4	
22:20	DPSIZC	3 bit decode page size field from CAM-side of TLB CAM-RAM) Same determination and encoding as for DPSIZR The CAM-side copy of this field is used for hit/miss determination in the TLB CAM array
19	RESERVED_3	
18:16	DPSIZR	(3 bit decode page size field from RAM-side of TLB CAM-RAM) Determined from the size fields of the page table entry Encodes the page size as follows: all other values reserved/unused The RAM-side copy of this field is used for virtual ’ physical address formation 0x0: 4KB page 0x1: 64KB page 0x3: 1MB page 0x7: 16MB page
15:12	RESERVED_2	
11	MT2	(memory type bit 2) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[2] attribute bus on the request output of the System MMU

VCAP_SMMU_VCAP_TLBTR0 (cont.)

Bits	Name	Description
10	MT1	(memory type bit 1) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[1] attribute bus on the request output of the System MMU
9	MT0	(memory type bit 0) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[0] attribute bus on the request output of the System MMU
8	SH	(shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's outer-shareable realm This field becomes the ASHARED attribute on the request output of the System MMU
7	ISH	(inner-shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's inner-shareable realm This field becomes the AINNERSHARED attribute on the request output of the System MMU
6	NSDESC	(non-secure descriptor) This TLB entry field is a modified version of the corresponding bit of the page table entry Qualified by the NS-prot attribute of the incoming request which prompted the allocation of the TLB entry, such that if the incoming NS-prot attribute was 1 (non-secure), then the NS-desc field of the page table entry was ignored, and the NS-desc field of the TLB entry was forced to 1 Indicates whether the associated memory page contains secure (NS-desc=0) or non-secure (NS-desc=1) information This field becomes the NS-prot attribute on the request output of the System MMU
5	RESERVED_1	

VCAP_SMMU_VCAP_TLBTR0 (cont.)

Bits	Name	Description
4	XN	(execute never permission) This TLB entry field comes directly from the corresponding bit of the page table entry
3	UW	(user write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
2	UR	(user read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
1	PW	(privileged write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
0	PR	(privileged read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]

0x072FFE84 VCAP_SMMU_VCAP_TLBTR1

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

VCAP_SMMU_VCAP_TLBTR1

Bits	Name	Description
31:12	PA	Physical address [31:12] field of the TLB entry
11:5	RESERVED	
4:0	VMID	VMID [4:0]field of the TLB entry)

0x072FFE88 VCAP_SMMU_VCAP_TLBTR2

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

VCAP_SMMU_VCAP_TLBTR2

Bits	Name	Description
31:12	VA	virtual address field [31:12] of the TLB entry
11	RESERVED	
10	NG	(not global field from page table entry) Indicates whether the page is private to the specified ASID (NG=1) or global to all ASIDs within the VMID using this context bank (NG=0)
9	NSTID	(non-secure tag ID field of the TLB entry) Indicates whether the TLB entry belongs to the secure world (NSTID=0) or the non-secure world (NSTID=1) This field is comned against the incoming NS-prot attribute of the master request as part of TLB hit/miss determination
8	V	valid field of the TLB entry
7:0	ASID	ASID[7:0] field of the TLB entry

0x072FFE8C VCAP_SMMU_VCAP_TESTBUSCR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

Governs which signals (if any) from the system SMMU core or wrapper design hierarchy are sent out to the system via a testbus for diagnostic, and also to the system profiling and diagnostic monitor (SPDM).

VCAP_SMMU_VCAP_TESTBUSCR

Bits	Name	Description
31:28	SPDM3SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[3]
27:24	SPDM2SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[2]
23:20	SPDM1SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[1]
19:16	SPDM0SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[0]
15:14	TBHSEL	Testbus highselect It governs which set of signals are to testbus[31:16] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL

VCAP_SMMU_VCAP_TESTBUSCR (cont.)

Bits	Name	Description
13:12	TBSLSEL	Testbus low select It governs which set of signals are to testbus[15:0] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL
11:10	RESERVED_2	
9:8	WGSEL	Wrapper group select It selects a particular group of signals from the SMMU wrapper hierarchy WGSEL = 0b00 - wrapper signal group 0 WGSEL = 0b01 - wrapper signal group 1 WGSEL = 0b10 - wrapper signal group 2 WGSEL = 0b11 - reserved
7:2	RESERVED_1	
1	SPDMBE	SPDM test enable Reset state : 0
0	TBE	Testbus enable, which governs whether the testbus is driven with all 0s or with the configured signals Reset state : 0

0x072FFEFC VCAP_SMMU_VCAP_VR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: 32'h0000_0000

Note that the DCPBP/DCPPP bits prevent the pipelining of the next transaction when the current transaction is a bypass/pass-through transaction. That is, they add one more cycle of delay between the current and next transactions.

Also note that when we are in global bypass (SMMU_CR[CLIENTPD]=1), these bits should have NO effect, or at least no effect between client transactions, they can have an effect between config and client transactions is appropriate. We must be able to continue to perform fully pipelined transactions when the client port is disabled altogether.

VCAP_SMMU_VCAP_VR0

Bits	Name	Description
31:3	RESERVED	

VCAP_SMMU_VCAP_VR0 (cont.)

Bits	Name	Description
2	DCPPT	Disable client pipelining for client operations in pass-through mode Reset state : 0
1	DCPBP	Disable client pipelining for client operations in bypass mode Reset state : 0
0	DCP	Disable client pipelining Reset state : 0

0x072FFF00 VCAP_SMMU_VCAP_TLBIALL

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries.

VCAP_SMMU_VCAP_TLBIALL

Bits	Name	Description
31:0	EXEC	Writing any value to this register invalidates all TLB entries, as specified by the contents of SMMU_CR[TLBIALLCFG]

0x072FFF04 VCAP_SMMU_VCAP_TLBIVMID

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries matching the IVMID value. Precise function is governed by SMMU_CR[TLBIALLCFG].

VCAP_SMMU_VCAP_TLBIVMID

Bits	Name	Description
31:5	RESERVED	
4:0	IVMID	Designates VMID[4:0] value of entries to be invalidated.

14.20.1.4 SMMU configuration registers

0x072FFF80 VCAP_SMMU_VCAP_CR

Type: Read/Write
Clock: AXI_BUS_CLOCK

Global configuration register.

VCAP_SMMU_VCAP_CR

Bits	Name	Description
31:10	RESERVED_2	
9	RESERVED_1	Reset state : 0
8	TLBIVMIDCFG	TLBIVMID configuration control. When set to 0,flash-invalidate, SMMU_TLBIVMID commands flash-invalidate the entire TLB, without regard to locking,security and VMID value. When set to 1, selective, SMMU_TLBIVMID invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and VMID field matching the VMID specified by SMMU_TLBIVMID command. Reset state : X
7	TLBIALLCFG	TLBIALL configuration control. When set to 0, flash-invalidate, SMMU_TLBIALL commands flash-invalidate the entire TLB, without regard to locking and/or security. When set to 1, selective, SMMU_TLBIALL invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and are unlocked. Reset state : X
6	TLBLKCRWE	TLBLKCR write enable. When set to 0, writes to SMMU_CBn_TLBLKCR are ignored. When set to 1, allows operating environments to manage the TLB locking mechanism directly. Management among multiple operating environments must be coordinated externally between themselves. Reset state : X
5	STALLD	Global disable for stall mode. When set to 1, context bank stall modes are ignored and operate as terminate mode. Reset state : X
4	CLIENTPD	Client port disable. When set, all client accesses are forced to bypass the system MMU. There is no translation. access control, or attribute generation. This bit overrides individual SMMU_M2VCBRn[BYPASSD] settings; client requests are bypassed, even if SMMU_M2VCBRn[BYPASSD] is set to 1. Bypass request errors are not recorded in SMMU_ESR, nor reported to requesting masters. The SMMU_rpuErrIrptReq interrupt output signal is not asserted. Reset state : 1

VCAP_SMMU_VCAP_CR (cont.)

Bits	Name	Description
3	DCDEE	When set to 0, configuration port decode errors do not set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn are not updated. When set to 1, configuration port decode errors set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn updated with address and syndrome of error. Reset state : X
2	RPUEIE	When set, configuration port errors and client port bypass errors are reported directly to the interrupt controller via the SMMU_rputErrIrptReq interrupt output signal. Interrupt output is asserted if SMMU_CR[RPUIE_EN] is 1 and ANY bit is set in SMMU_ESR register. Reset state : 0
1	RPUERE	When set, SMMU reports configuration port errors and client port bypass errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via AXI port will use decode error, rather than slave error. Regardless of the value of this field both configuration port errors and client port bypass request errors are terminated by the SMMU as RAZ/WI, and are recorded in SMMU_ESR register. Reset state : X
0	RPUE	When set, all configuration port accesses are checked against SMMUX_RPU_ACR and/or the SMMUX_CBACRn registers for access permissions. Reset state : 0

14.20.1.5 SMMU error report registers

0x072FFF84 VCAP_SMMU_VCAP_EAR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: unknown

When there is an error, holds the physical address of the errant transaction.

VCAP_SMMU_VCAP_EAR

Bits	Name	Description
31:0	PA	Physical address[31:0]

0x072FFF88 VCAP_SMMU_VCAP_ESR

Type: Read/Write to clear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This register has read/write clear access. Reads return the value in the register, a write with a 1 set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

VCAP_SMMU_VCAP_ESR

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR, SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x072FFF8C VCAP_SMMU_VCAP_ESRRESTORE

Type: Write
Clock: RPM_BUS_CLK
Reset State: Undefined

This register is an aliased address for SMMU_ESR, but it allows direct write access. In this way, diagnostic software can cause an error to be generated and reported.

VCAP_SMMU_VCAP_ESRRESTORE

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR, SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	

VCAP_SMMU_VCAP_ESRRESTORE (cont.)

Bits	Name	Description
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x072FFF90 VCAP_SMMU_VCAP_ESYNR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

VCAP_SMMU_VCAP_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request
15:0	AMID	AMID[15:0] field of errant request

0x072FFF94 VCAP_SMMU_VCAP_ESYNR1

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

VCAP_SMMU_VCAP_ESYNR1

Bits	Name	Description
31	DCD	(decode) Indicates configuration port error due to invalid/unrecognized address (e.g., a reserved register address) Includes decode errors within both the global address space and the individual context bank address space

VCAP_SMMU_VCAP_ESYNR1 (cont.)

Bits	Name	Description
30	AC	(access control) Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO field of the errant request
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request)
15:12	ALEN	ALEN[3:0] field of the errant request
11	RESERVED_2	
10	ABURST	ABURST[1:0] field of the errant request
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request
7	AINST	AINST field of the errant request
6	APROTNS	APROTNS field of the errant request
5	APRIV	APRIV field of the errant request
4	AINNERSHARED	AINNERSHARED field of the errant request
3	ASHARED	ASHARED field of the errant request
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

14.20.1.6 SMMU revision register

0x072FFFF4 VCAP_SMMU_VCAP_REV

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the revision information for the SMMU core and wrapper.

VCAP_SMMU_VCAP_REV

Bits	Name	Description
31:12	RESERVED	

VCAP_SMMU_VCAP_REV (cont.)

Bits	Name	Description
11:8	WRAPPER	Wrapper version
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

14.20.1.7 SMMU implementation parameter register

0x072FFFF8 VCAP_SMMU_VCAP_IDR

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the parameter information for the SMMU core and wrapper

VCAP_SMMU_VCAP_IDR

Bits	Name	Description
31:24	NIRPT	NIRPT[7:0] Indicates number of context fault interrupt outputs (minus 1) supported by the System MMU Value can range from 0 - 255 (1 - 256 context fault interrupt outputs)
23:16	NCB	NCB[7:0] Indicates number of context banks (minus 1) supported by the System MMU Value can range from 0 - 254 (1 - 255 context banks)
15:12	TLBSIZE	TLBSIZE[3:0] Indicates log2(number of TLB entries) That is, number of TLB entries = 2 ** TLBSIZE
11	RESERVED	
10	HUM	Indicates whether or not TLB hit-under-miss behavior is supported
9	HTW	Indicates whether or not the System MMU supports hardware table walk If hardware table walk not supported (HTW=0), then software cannot set SMMU_CBn_ACTLR[TLBMCFG] to 0b10
8:0	NM2VCBMT	NM2VCBMT[8:0] Indicates number of M2VCBMT entries, with a maximum of 512 The bit width of the M2VCBMTIindex input (maximum value is 9) is equal to log base 2 of NM2VCBMT Allows for up to 7-bit MID field, plus NS-prot or other fields to select mapping [

0x072FFFFC VCAP_SMMU_VCAP_RPU_ACR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Using the incoming HVMID, this register controls access to the global register space.

VCAP_SMMU_VCAP_RPU_ACR

Bits	Name	Description
31:0	RWE	Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the entire block of registers within the SMMU's 4KB global address space, including this register itself. A VMID identified by this register is also permitted global access to all context banks. In practice, this register designates the VMID(s) that can act as SROT.

14.20.2 SMMU Context Bank Registers

There are a configurable number (1 to 9) of context banks in the SMMU. Each context bank consists of a set of registers in a unique 4KB address space.

14.20.2.1 SMMU context bank control registers

0x07200000+0x1000*n VCAP_SMMU_VCAP_CBn_SCTLR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank System Control Register controls various architected SMMU features

VCAP_SMMU_VCAP_CBn_SCTLR

Bits	Name	Description
31:5	RESERVED_2	
4	BE	Governs the order byte order or "endianness" of the page table entries. When set to 0, page table entries are in little endian format, so that their least significant byte is in byte 0 of the 32 bit entry. When set to 1, page table entries are in big endian format, so that their most significant byte is in byte 0 of the 32 bit entry.
3	RESERVED_1	Reserved for HAF, Hardware access flag. This bit governs whether the access flag is managed by hardware or software. The SMMU supports software access flag management only, so this bit is read-only and internally driven to 0.

VCAP_SMMU_VCAP_CBn_SCTLR (cont.)

Bits	Name	Description
2	AFE	Access flag enable. When AFE = 0, the access flag field is not supported and the AP[0] page table entry field acts as a bit of the overall AP[2:0] field to determine access permissions. When AFE = 1, the AP[0] page table entry field becomes the access flag, and the reduced number of access permission combinations is specified by AP2:1], and SMMU hardware will signal an Access Flag fault if a request targets a page for which the access flag is 0.
1	TRE	TEX remap enable. This bit governs the mapping of the page table entry TEX[2:0],C,B and SH fields into an SMMU TLB entry, and thus the translation of the AMEMTYPE[2:0], ASHARED and AINNERSHARED bus attributes. When TRE = 0, the TLB value is determined directly from the page table entry fields.
0	M	MMU enable bit. When set to 1, this context bank is enabled for translating requests. When set to 0, accesses bypass the TLB, and there is no address translation, access permission checking or attribute mapping. Incoming master requests are passed through unchanged.

0x07200004+ 0x1000*n VCAP_SMMU_VCAP_CBn_ACTLR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank auxiliary control register controls various implementation specific features.

VCAP_SMMU_VCAP_CBn_ACTLR

Bits	Name	Description
31:19	RESERVED	
18	RESERVED_2	
17:16	V2PCFG	VA-to-PA configuration. Governs operation of VA-to-PA commands that miss in the TLB 0x0: terminate (Record TLB Miss context fault in SMMU_CBn_PAR) 0x1: software table update (Translate based on values in SMMU_CBn_TLBFLPTER and SMMU_CBn_TLBSLPTER) 0x2: hardware table walk (Translate based on value of PTE read from page table in memory) 0x3: reserved

VCAP_SMMU_VCAP_CBn_ACTLR (cont.)

Bits	Name	Description
15	TIPCF	Governs whether or not all subsequent requests using this context bank should be terminated if a prior context fault has occurred and has not yet been cleared from SMMU_CBn_FSR Accesses to other context banks proceed as normal 0x0: do not terminate (System MMU will attempt to process subsequent requests despite the presence of an existing context fault in SMMU_CBn_FSR. SMMU_CBn_FSR will be set if the subsequent access also encounters a context fault) 0x1: terminate (All subsequent accesses terminated by the System MMU as RAZ/WI, even if SMMU_CBn_ACTLR[TLBMCFG, CFCFG] configured for stall mode. SMMU_CBn_FSR set when access is terminated due to TIPCF = 1. Presence of SMMU_CBn_FSR when SMMU_CBn_ACTLR is 1 implies that the later exceptions must have been simply the forced terminations due to the prior context fault. Error optionally reported to the requesting master, according to the client port bus protocol, f SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus if SMMU_CBn_ACTLR is 1.)
14	CFCFG	(context fault configuration) Governs the behavior of all context faults except TLB miss TLB miss context faults are governed by SMMU_CBn_ACTLR[TLBMCFG] 0x0: terminate (Access terminates at the System MMU as RAZ/WI. Context fault exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x1: stall (Requesting master's access stalled while System MMU waits for managing processor to resolve context fault. Context fault exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode)

VCAP_SMMU_VCAP_CBn_ACTLR (cont.)

Bits	Name	Description
13:12	TLBMCFG	(TLB miss configuration) Governs the behavior of client accesses that miss in the TLB 0x0: pass-through (Access passed through to targeted slave without translation, attribute control, or access permission checking. Effectively, behavior is as if SMMU_CBn_SCTLR = 0 i.e., MMU disabled for this context bank. TLB miss not considered a context fault. TLB miss exception not recorded in SMMU_CBn_FSR. TLB miss exception not reported to requesting master. SMMU_contextFaultIrptReq interrupt output not asserted) 0x1: terminate (Access terminates at the System MMU as RAZ/WI,TLB miss exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x2: stall (Requesting master's access stalled while System MMU waits for managing processor to update TLB. TLB miss exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode) 0x3: HTW (Hardware table walk . Requesting master's access stalled while System MMU accesses page table. The is TLB updated and requesting master's access resumed after obtaining valid entry from page table. If translation fault, then access either terminates or stalls according to setting of SMMU_CBn_ACTLR)
11	DNLV2PA	(disable non-locking VA-to-PA allocation) Governs whether or not TLB misses due to non-locking VA-to-PA commands will allocate a new entry This field is ignored for locking VA-to-PA operations (SMMU_CBn_TLBLKCR[LKE] = 1)
10	DNA	(disable normal allocation) Governs whether or not TLB misses due to client port accesses will allocate a new entry
9:8	PRIVCFG	0x0: apriv (System MMU uses APRIV signal supplied by master as user/supervisor indicator 1 = supervisor) 0x1: reserved 0x2: User (System MMU ignores APRIV; treats all requests using this context bank as user) 0x3: Supervisor (System MMU ignores APRIV; treats all requests using this context bank as supervisor)

VCAP_SMMU_VCAP_CBn_ACTLR (cont.)

Bits	Name	Description
7:5	RESERVED_1	
4	RCNSH	(redirect cacheable-non-shareable) Governs whether or not cacheable accesses that are non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache, even though the locations are not being coherently shared with Scorpion-MP
3	RCISH	(redirect cacheable-inner-shareable) Governs whether or not cacheable accesses that are inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
2	RCOSH	(redirect cacheable-outer-shareable) Governs whether or not cacheable accesses that are outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
1	CFEIE	(context fault error interrupt enable) Governs whether or not client port request context faults are reported directly to the interrupt controller via the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus Interrupt output is asserted if SMMU_CBn_ACTLR[CFEIE] is 1 and any context fault bits are set in SMMU_CBn_FSR Such interrupts would generally be directed to the interrupt controller of whichever processor is currently managing this context bank of the System MMU Reset state : 0
0	CFERE	(context fault error report enable) Governs whether or not client port request context faults that are configured for terminate mode (or that are explicitly terminated after stall mode) are reported to the requesting master, according to the client port bus protocol All error types reported via AXI port will use decode error rather than slave error All context faults are recorded in SMMU_CBn_FSR, regardless of the value of this field.

0x07200008+ 0x1000*n VCAP_SMMU_VCAP_CBn_CONTEXTIDR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context ID register holds the ASID associated with this context bank

VCAP_SMMU_VCAP_CBn_CONTEXTIDR

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Specifies the 8 bit ASID value assigned to this context bank. The ASID can be included in the key comparison of TLB entries. .

0x07200010+ 0x1000*n VCAP_SMMU_VCAP_CBn_TTBR0, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR0 is used for low order virtual addresses, typically private pages for a given process.

VCAP_SMMU_VCAP_CBn_TTBR0

Bits	Name	Description
31:7	PA	BIts 31:7 of the physical address of the base of the page table. The actual LSB of the base address is bit 14-N, where N is set in register TTCR
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07200014+ 0x1000*n VCAP_SMMU_VCAP_CBn_TTBR1, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR1 is used for high order virtual addresses, typically global pages for a given VMID, or kernel mappings.

The context bank auxiliary control register controls various implementation specific features.

VCAP_SMMU_VCAP_CBn_TTBR1

Bits	Name	Description
31:14	PA	BIts 31:14 of the physical address of the base of the page table.
13:7	RESERVED_2	
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED_1	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07200018+ 0x1000*n VCAP_SMMU_VCAP_CBn_TTBCR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table control register, which specifies the size of the virtual address space that uses TTBR0.

VCAP_SMMU_VCAP_CBn_TTBCR

Bits	Name	Description
31:6	RESERVED_2	
5	PD1	Page disable 1; if this bit is set, hardware table walks attempting to use TTBR1will result in a first level descriptor translation fault. If clear, TTBR1 contents are used.
4	PD0	Page disable 0; if this bit is set, hardware table walks attempting to use TTBR0 will result in a first level descriptor translation fault. If clear, TTBR0 contents are used.
3	RESERVED_1	
2:0	N	N[2:0] specifies the number of upper order virtual address bits which must be 0 in order for translations to use the table pointed to by TTBR0. If any of these bits are non-zero, TTBR1 is used for the lookup. If N is 0, only TTBR0 is used.

0x0720001C+ 0x1000*n VCAP_SMMU_VCAP_CBn_PAR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The physical address register captures the physical address value resulting from the execution of a VA-to-PA command

Field definitions vary according to whether or not there is a context fault associated with the requested translation

VCAP_SMMU_VCAP_CBn_PAR

Bits	Name	Description
31:12	PAR_FAULT_INFO_312	
11	RESERVED_2	
10:9	PAR_FAULT_INFO_72	
8	RESERVED_1	
7:1	PAR_FAULT_INFO_71	Encoding varies according to value in FAULT field.
0	FAULT	(fault status) This field will be 1 when a context fault is associated with the requested translation, and 0, when there is no context fault associated with the requested translation.

0x07200020+0x1000*n VCAP_SMMU_VCAP_CBn_FSR, n=[0..2]

Type: Read/WriteClear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The Fault Status Register records status information for client accesses that encounter exceptions within the context bank, e.g. translation faults.This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data

This prevents inadvertent clearing of new faults when writing the register to clear an old fault

The presence of an asserted value on any bit in this register (except the SS bit) is what prompts the assertion (when enabled by SMMU_CBn_ACTLR[CFEIE]) of the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus

Therefore, these bits must be cleared by the interrupt handler

This is contrasted with the fields in the SMMU_CBn_FSYNRn registers, which are merely the "syndrome" of the fault indicated by SMMU_CBn_FSR

VCAP_SMMU_VCAP_CBn_FSR

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry

VCAP_SMMU_VCAP_CBn_FSR (cont.)

Bits	Name	Description
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07200024+ 0x1000*n VCAP_SMMU_VCAP_CBn_FSRRESTORE, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Allows SW to force a value into the SMMU_CBn_FSR register.

VCAP_SMMU_VCAP_CBn_FSRRESTORE

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)

VCAP_SMMU_VCAP_CBn_FSRRESTORE (cont.)

Bits	Name	Description
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07200028+ 0x1000*n VCAP_SMMU_VCAP_CBn_FAR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The Fault Address Register records the virtual address of client accesses that encounter exceptions within the context bank, e.g. translation faults. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

VCAP_SMMU_VCAP_CBn_FAR

Bits	Name	Description
31:0	VA	VA[31:0] of errant client access

0x0720002C+ 0x1000*n VCAP_SMMU_VCAP_CBn_FSYNR0, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

NOTE omission of VMID field from this register, as VMID can only be made visible to SROT, and not to general OS software that manages the context bank registers

VCAP_SMMU_VCAP_CBn_FSYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] (ATID field of errant request)

VCAP_SMMU_VCAP_CBn_FSYNR0 (cont.)

Bits	Name	Description
23:16	RESERVED	
15:13	ABID	ABID[2:0] (ABID field of errant request)
12:8	APID	APID[4:0] (APID field of errant request)
7:0	AMID	AMID[7:0] (AMID field of errant request)

0x07200030+ 0x1000*n VCAP_SMMU_VCAP_CBn_FSYNR1, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

VCAP_SMMU_VCAP_CBn_FSYNR1

Bits	Name	Description
31:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO (AOOO field of the errant request)
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request
15:12	ALEN	ALEN[3:0]field of the errant request
11	RESERVED_2	
10	ABURST	field of the errant request
9	RESERVED_1	
8	AWRITE	field of the errant request
7	AINST	field of the errant request
6	APROTNS	field of the errant request
5	APRIV	field of the errant request
4	AINNERSHARED	(AINNERSHARED field of the errant request)
3	ASHARED	(ASHARED field of the errant request)

VCAP_SMMU_VCAP_CBn_FSYNR1 (cont.)

Bits	Name	Description
2:0	AMEMTYPE	AMEMTYPE[2:0] (AMEMTYPE field of the errant request)

0x07200034+ 0x1000*n VCAP_SMMU_VCAP_CBn_PRRR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs memory type and shareability attributes of requests that are both MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1)

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) and/or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, memory type encoding is as follows:

0b00 = strongly-ordered

0b01 = device

0b10 = normal

0b11 = reserved

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VCAP_SMMU_VCAP_CBn_PRRR

Bits	Name	Description
31	NOS7	not-outer-shareable class 7
30	NOS6	not-outer-shareable class 6
29	NOS5	not-outer-shareable class 5
28	NOS4	not-outer-shareable class 4
27	NOS3	not-outer-shareable class 3
26	NOS2	not-outer-shareable class 2

VCAP_SMMU_VCAP_CBn_PRRR (cont.)

Bits	Name	Description
25	NOS1	not-outer-shareable class 1
24	NOS0	not-outer-shareable class 0
23:20	RESERVED	
19	SHNMSH1	(shareable attribute for normal memory accesses with SH=1) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1
18	SHNMSH0	(shareable attribute for normal memory accesses with SH=0) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0
17	SHDSH1	SHDSH1 (shareable attribute for device accesses with SH=1) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1 [
16	SHDSH0	SHDSH0 (shareable attribute for device accesses with SH=0) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0 [
15:14	MTC7	MTC7[1:0] (memory type class 0)
13:12	MTC6	MTC6[1:0] (memory type class 0)
11:10	MTC5	MTC5[1:0] (memory type class 0)
9:8	MTC4	MTC4[1:0] (memory type class 0)
7:6	MTC3	MTC3[1:0] (memory type class 0)
5:4	MTC2	MTC2[1:0] (memory type class 0)
3:2	MTC1	MTC1[1:0] (memory type class 0)
1:0	MTC0	MTC0[1:0] (memory type class 0)

0x07200038+ 0x1000*n VCAP_SMMU_VCAP_CBn_NMRR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs the cache policy of MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1) requests for which the memory type is mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0) or the memory type is mapped to a type other than normal memory (SMMU_CBn_PRRR[MTCn] != 0b10)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, inner-cache and outer-cache policy encodings are as follows:

0b00 = non-cacheable

0b01 = cacheable, copy-back, write-allocate

0b10 = cacheable, write-through, write-no-allocate

0b11 = cacheable, copy-back, write-no-allocate

VCAP_SMMU_VCAP_CBn_NMRR

Bits	Name	Description
31:30	OCPC7	OCPC7[1:0] (inner-cache policy class 7)
29:28	OCPC6	OCPC6[1:0] (inner-cache policy class 6)
27:26	OCPC5	OCPC5[1:0] (inner-cache policy class 5)
25:24	OCPC4	OCPC4[1:0] (inner-cache policy class 4)
23:22	OCPC3	OCPC3[1:0] (inner-cache policy class 3)
21:20	OCPC2	OCPC2[1:0] (inner-cache policy class 2)
19:18	OCPC1	OCPC1[1:0] (inner-cache policy class 1)
17:16	OCPC0	OCPC0[1:0] (inner-cache policy class 0)
15:14	ICPC7	ICPC7[1:0] (inner-cache policy class 7)
13:12	ICPC6	ICPC6[1:0] (inner-cache policy class 6)
11:10	ICPC5	ICPC5[1:0] (inner-cache policy class 5)
9:8	ICPC4	ICPC4[1:0] (inner-cache policy class 4)
7:6	ICPC3	ICPC3[1:0] (inner-cache policy class 3)
5:4	ICPC2	ICPC2[1:0] (inner-cache policy class 2)
3:2	ICPC1	ICPC1[1:0] (inner-cache policy class 1)
1:0	ICPC0	ICPC0[1:0] (inner-cache policy class 0)

0x0720003C+ 0x1000*n VCAP_SMMU_VCAP_CBn_TLBLKCR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB lock control register governs the TLB locking mechanism and TLB invalidate operations.Write access to this register is governed by SMMU_CR[TLBLKCRWE]

When SMMU_CR[TLBLKCRWE] is 0, writes to SMMU_CBn_TLBLKCR are ignored

Read access is still permitted

SROT can set SMMU_CR[TLBLKCRWE] to 1 to allow operating environment(s) to manage the TLB locking mechanism

Management amongst multiple operating environments must be coordinated via semaphore

VCAP_SMMU_VCAP_CBn_TLBLKCR

Bits	Name	Description
31:24	RESERVED_2	
23:16	VICTIM	VICTIM[7:0] Indicates the TLB index at which the next normal (non-locking) allocation will occur Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context
15:8	FLOOR	FLOOR[7:0] Indicates the TLB index from which round-robin replacement on normal (non-locking) allocations occurs TLB entries at indices below this value are locked Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context banks
7:4	RESERVED_1	

VCAP_SMMU_VCAP_CBn_TLBLKCR (cont.)

Bits	Name	Description
3	TLBIVAACFG	(TLBIVAA configuration) TLBIVAACFG = 0 - flash-invalidate SMMU_CBn_TLBIVAA commands flash-invalidate the entire TLB, without regard to locking, security, address, and/or VMID value TLBIVAACFG = 1 - selective SMMU_CBn_TLBIVAA commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank VA field of TLB entry matches VA designated by SMMU_CBn_TLBIVAA command NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked
2	TLBIASIDCFG	(TLBIASID configuration) TLBIASIDCFG = 0 - flash-invalidate SMMU_CBn_TLBIASID commands flash-invalidate the entire TLB, without regard to locking, security, VMID, and/or ASID values TLBIASIDCFG = 1 - selective SMMU_CBn_TLBIASID commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command TLB entry is not global (NG field is 1) NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
1	TLBIALLCFG	(TLBIALL configuration) TLBIALLCFG = 0 - flash-invalidate SMMU_CBn_TLBIALL commands flash-invalidate the entire TLB, without regard to locking, security, and/or VMID value TLBIALLCFG = 1 - selective SMMU_CBn_TLBIALL commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked

VCAP_SMMU_VCAP_CBn_TLBLKCR (cont.)

Bits	Name	Description
0	LKE	(lock enable) Governs whether or not TLB entries established by VA-to-PA commands upon TLB misses are locked LKE = 0 (normal, non-locking) Allocate VA-to-PA TLB entry (if TLB miss) at the index specified by SMMU_CBn_TLBLKCR[VICTIM] Allocation is disabled if SMMU_CBn_ACTLR[DNLV2PA] is 1 Increment SMMU_CBn_TLBLKCR[VICTIM] by 1 (only if new entry allocated) Wrap back to the value of SMMU_CBn_TLBLKCR[FLOOR] when the last entry is written LKE = 1 (locking) Search TLB for specified VA and invalidate if found Provides atomicity between the invalidate and the new allocation within the locked region Allocate VA-to-PA TLB entry at the index specified by data operand bits 7:0 of the VA-to-PA command This value must be less than SMMU_CBn_TLBLKCR[FLOOR] in order for it to remain locked Allocation occurs even if non-locking allocation is disabled due to SMMU_CBn_ACTLR[DNLV2PA] = 1

0x07200040+ 0x1000*n VCAP_SMMU_VCAP_CBn_V2PSR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The VA-to-PA status register records the hit/miss status and TLB index or V2Pxx and TLB invalidate commands.

VCAP_SMMU_VCAP_CBn_V2PSR

Bits	Name	Description
31:16	RESERVED_2	
15:8	INDEX	INDEX[7:0] Indicates the index of the TLB entry associated with the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command If SMMU_CBn_V2PSR[HIT] is 0, then SMMU_CBn_V2PSR[INDEX] is the index to which the entry was allocated (if allocated at all) If SMMU_CBn_V2PSR[HIT] is 1, then SMMU_CBn_V2PSR[INDEX] is the index of the entry which hit
7:1	RESERVED_1	

VCAP_SMMU_VCAP_CBn_V2PSR (cont.)

Bits	Name	Description
0	HIT	Indicates whether or not there was a TLB hit (prior to allocation, if any) on the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command

0x07200044+ 0x1000*n VCAP_SMMU_VCAP_CBn_TLBFLPTER, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB first level PTE register holds the first level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

This register (together with SMMU_CBn_TLBSLPTER) is used as the source of the translation information for VA-to-PA operations when the MMU is enabled (SMMU_CBn_SCTLR[M] = 1) and the operations are configured for software table update (SMMU_CBn_ACTLR[V2PCFG] = 0b01)

Field definitions vary according to the type of PTE (fault, page, section, or supersection), and come directly from the ARMv7 architecture's PTE formats

VCAP_SMMU_VCAP_CBn_TLBFLPTER

Bits	Name	Description
31:10	FL_PTE_HI	
9:5	RESERVED	
4:2	FL_PTE_LO	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	This field should be set to 0b00 or 0b11 to indicate that the translation should result in a context fault, and the rest of the fields are defined as indicated in this section If this field is not 0b00 or 0b11, then the PTE is of some other type (see other sections for the field definitions for those types)

0x07200048+ 0x1000*n VCAP_SMMU_VCAP_CBn_TLBSLPTER, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB second level PTE register holds the second level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

Field definitions vary according to the type of PTE (fault, 64KB or 4KB), and come directly from the ARMv7 architecture's PTE format

VCAP_SMMU_VCAP_CBn_TLBSLPTER

Bits	Name	Description
31:2	SL_PTE	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	0x0: fault

0x0720004C+ 0x1000*n VCAP_SMMU_VCAP_CBn_BFBCR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The burst fetch buffer configuration register governs the operation of the "burst fill" feature of the SMMU.

VCAP_SMMU_VCAP_CBn_BFBCR

Bits	Name	Description
31:12	STRIDE	(stride amount) 4KB-aligned value to be added to virtual address on demand TLB miss for filling subsequent BFB Stride of minimum 4KB alignment useful for preventing stride burst fetch until final PTE of the demand BFB entry is used
11:8	SLVIC	(second-level victim) Indicates the SLBFB index at which the next round-robin allocation will occur
7:4	FLVIC	(first-level victim) Indicates the FLBFB index at which the next round-robin allocation will occur
3	RESERVED	
2	SFVS	(stride-fetch victim selection) SFVS. = 0 (replace normal round-robin victim-selected entry) Useful when stride is larger than the VA space represented by the four PTEs in the demand BFB entry, but the client access pattern is for more than just the initial PTE in that demand BFB entry SFVS. = 1 (replace same BFB used by demand VA for which the stride burst is being performed) Useful when stride is the same as the VA space represented by an individual PTE in the demand BFB entry (such that the stride won't miss against the BFB until the last PTE of the demand BFB entry is accessed), and/or when the client access pattern only uses the initial PTE in the demand BFB entry

VCAP_SMMU_VCAP_CBn_BFBCR (cont.)

Bits	Name	Description
1	BFBSFE	(burst fetch buffer stride fetch enable) Enables stride burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Stride burst fetch is for the block of four PTEs associated with VA+stride VA is the "demanded" VA from the client (or VA-to-PA command) Stride value is specified by SMMU_CBn_BFBCR[STRIDE] Stride burst fetch only occurs if demand access for VA misses in TLB (could hit in BFB) and address VA+stride misses in both TLB and BFB
0	BFBDFE	(burst fetch buffer demand fetch enable) Enables demand burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Demand burst fetch is for the block of four PTEs associated with the "demanded" VA from the client (or VA-to-PA command) Demand burst fetch only occurs if demand access misses in both TLB and BFB

0x07200800+ 0x1000*n VCAP_SMMU_VCAP_CBn_TLBIALL, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate all command register invalidates all TLB entries matching the VMID associated with this context bank. Data operand is ignored.

VCAP_SMMU_VCAP_CBn_TLBIALL

Bits	Name	Description
31:0	RESERVED	

0x07200804+ 0x1000*n VCAP_SMMU_VCAP_CBn_TLBIASID, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by ASID command register invalidates TLB entries matching the specified ASID and matching the VMID associated with this context bank.Invalidates TLB entries which are associated with the designated ASID and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIASIDCFG] governs whether command flash-invalidates entire TLB array or just the entries matching the VMID, ASID, and security state

TLBIASIDCFG = 0 - flash-invalidate

SMMU_CBn_TLBIASID command flash-invalidates the entire TLB, without regard to locking, security, VMID, and/or ASID values

TLBIASIDCFG = 1 - selective

SMMU_CBn_TLBIASID command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command data operand

TLB entry is not global (NG field is 1)

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command

Locking is not considered (matching entries are invalidated even if locked)

ASID field of command specifies the ASID value of the TLB entries to be invalidated

VCAP_SMMU_VCAP_CBn_TLBIASID

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Actual ASID value

0x07200808+0x1000*n VCAP_SMMU_VCAP_CBn_TLBIVA, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA command invalidates TLB entries matching the designated VA, ASID and the VMID associated with this context bank.

Matching entry determined as follows:

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIVA command data operand (or TLB entry is global - NG field is 0)

VA field of TLB entry matches VA value designated by the SMMU_CBn_TLBIVA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIVA command

Locking is not considered (matching entry is invalidated even if locked)

Data operand specifies the VA and ASID value of the TLB entry to be invalidated

VCAP_SMMU_VCAP_CBn_TLBIVA

Bits	Name	Description
31:12	VA	VA[31:12]
11:8	RESERVED	
7:0	ASID	ASID[7:0] value

0x0720080C+ 0x1000*n VCAP_SMMU_VCAP_CBn_TLBIVAA, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA all ASIDS command invalidates TLB entries matching the designated VA and the VMID associated with this context bank, regardless of ASID.Invalidates TLB entries which are associated with the designated VA, regardless of ASID, and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIVAACFG] governs whether command flash-invalidates entire TLB array or just the non-locked entries matching the VMID, ASID, and security state

TLBIVAACFG = 0 - flash-invalidate

SMMU_CBn_TLBIVAA command flash-invalidates the entire TLB, without regard to locking, security, address, and/or VMID value

TLBIVAACFG = 1 - selective

SMMU_CBn_TLBIVAA command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

VA field of TLB entry matches VA designated by the SMMU_CBn_TLBIVAA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command

Entry is unlocked

VCAP_SMMU_VCAP_CBn_TLBIVAA

Bits	Name	Description
31:12	VA	VA[31:12]
11:0	RESERVED	

0x07200810+ 0x1000*n VCAP_SMMU_VCAP_CBn_V2PRR, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

VCAP_SMMU_VCAP_CBn_V2PRR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07200814+ 0x1000*n VCAP_SMMU_VCAP_CBn_V2PPW, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

VCAP_SMMU_VCAP_CBn_V2PPW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07200818+ 0x1000*n VCAP_SMMU_VCAP_CBn_V2PUR, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

VCAP_SMMU_VCAP_CBn_V2PUR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x0720081C+0x1000*n VCAP_SMMU_VCAP_CBn_V2PUW, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

.Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

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VCAP_SMMU_VCAP_CBn_V2PUW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07200820+ 0x1000*n VCAP_SMMU_VCAP_CBn_RESUME, n=[0..2]

Type: Write/command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB resume command causes the SMMU to resume operation after a stalled access..

VCAP_SMMU_VCAP_CBn_RESUME

Bits	Name	Description
31:1	RESERVED	

VCAP_SMMU_VCAP_CBn_RESUME (cont.)

Bits	Name	Description
0	TNR	Terminate/not retry When TNR is written as 0, indicates that the stalled access should be retried by the system MMU. When written as 1, indicates that this stalled transaction is terminated by the system MMU. The error is optionally reported to the requesting master, using the client port bus protocol, if SMMU_CNn_ACTLR[CFERE] == 1. Interrupt optionally remains asserted via SMMU_M2VCBRn[IRPTINDX] selected SMMU_contextFaultIrptReq bit, only if SMMU_CBn_ACTLR[CFEIE] is 1, and only if SMMU_CBn_FSR has not been cleared by software priori to issuing this command..

14.21 JPEG SMMU Registers (0x07300000 SMMU_JPEGD_BASE)

This section contains the JPEG SMMU registers.

14.21.1 SMMU Global Registers

14.21.1.1 SMMU VMID/CBNDX mapping registers

0x073FF000+ 0x4*n JPEGD_SMMU_JPEGD_M2VCBRn, n=[0..1]

Type: Read/Write
Clock: AXI_CLK
Reset State: Undefined

SMMU_M2VCBRm registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

JPEGD_SMMU_JPEGD_M2VCBRn

Bits	Name	Description
31:28	RESERVED_2	
27:25	BPMEMTYPE	(bypass memory type) Supplies the AMEMTYPE attributes for client requests which bypass the System MMU when SMMU_M2VCBRn[BPMTCFG] = 1 See reference section for AMEMTYPE encoding definitions
24	BPMTCFG	(bypass memory type configuration) Governs the memory type (AMEMTYPE) attributes of client requests which bypass the System MMU BPMTCFG = 0 - use AMEMTYPE Bypass requests use AMEMTYPE signal supplied by client master BPMTCFG = 1 - use SMMU_M2VCBRn[BPMEMTYPE] Bypass requests use SMMU_M2VCBRn[BPMEMTYPE] Reset state : 0
23:22	NSCFG	(non-secure configuration) Governs the incoming security designation of client requests NSCFG = 0b00 - use APROTNS Use APROTNS signal supplied by client master NSCFG = 0b01 - reserved NSCFG = 0b10 - secure System MMU ignores APROTNS; treats all requests as secure NSCFG = 0b11 - non-secure System MMU ignores APROTNS; treats all requests as non-secure Reset state : 0

JPEGD_SMMU_JPEGD_M2VCBRn (cont.)

Bits	Name	Description
21:20	BPSHCFG	(bypass shareability configuration) Governs the shareability realm (ASHARED and AINNERSHARED) attributes of client requests which bypass the System MMU BPSHCFG = 0b00 - use ASHARED and AINNERSHARED Bypass requests use ASHARED and AINNERSHARED signals supplied by client master BPSHCFG = 0b01 - outer-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 0 BPSHCFG = 0b10 - inner-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 1 BPSHCFG = 0b11 - non-shareable Bypass requests set ASHARED = 0, AINNERSHARED = 0 Reset state : 0
19	BPRCNSH	(bypass redirect cacheable-non-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache Reset state : 0
18	BPRCISH	(bypass redirect cacheable-inner-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0
17	BPRCOSH	(bypass redirect cacheable-outer-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0

JPEGD_SMMU_JPEGD_M2VCBRn (cont.)

Bits	Name	Description
16	BYPASSD	Bypass disable for this index Governs whether or not client port accesses using this mapping table entry are actually permitted to "bypass" the System MMU when such bypass is indicated (either due to CBNDX = 255 or due to the master asserting the "SMMU bypass" input) This field is ignored (and operates as if it were 0) if SMMU_CR[CLIENTPD] is 1 BYPASSD = 0 - bypass enabled Bypass requests truly bypass the System MMU and "pass-through" to the fabric (no translation, access control, or attribute generation) No cycle of latency for System MMU context bank access Bypass request not considered an error Bypass request error not recorded in SMMU_ESR[BYPASS] Bypass error not reported to requesting master SMMU_rpuErrIrptReq interrupt output not asserted Client accesses still reference M2VCBMT to get VMID value for presentation to fabric BYPASSD = 1 - bypass disabled System MMU terminates the access as RAZ/WI Bypass request is considered an error Bypass request error is recorded in SMMU_ESR[BYPASS] If SMMU_CR[RPUERE] is 1, then bypass error reported to requesting master according to the client port bus protocol If SMMU_CR[RPUEIE] is 1, then SMMU_rpuErrIrptReq interrupt output asserted
15:8	CBNDX	Context bank index Context bank index associated with the M2VCBMT index CBNDX = 255 indicates no context bank assigned ("bypass")
7:5	RESERVED_1	
4:0	VMID	Virtual machine ID VMID value associated with the M2VCBMT index Must be programmed consistently with the SMMU_CBACRn[CBVMID] field for the context bank designated by SMMU_M2VCBRm[CBNDX]

14.21.1.2 SMMU context bank access control registers

0x073FF800+ 0x4*n JPEGD_SMMU_JPEGD_CBACRn, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs configuration port access to the associated context bank registers.

JPEGD_SMMU_JPEGD_CBACRn

Bits	Name	Description
31:24	IRPTNDX	(interrupt index) Interrupt output number used for context faults associated with this context bank (use SMMU_contextFaultIrptReq[IRPTNDX])
23:21	RESERVED	
20:16	CBVMID	(context bank VMID) Specifies the VMID with which the client masters using the context bank are associated Must be programmed consistently with the M2VCBMT entries that are configured to use the associated context bank This field is used by configuration port commands that need the context bank's VMID value in order to access the TLB (e.g., SMMU_CBn_TLBIVMID, SMMU_CBn_V2Pxx)
15:10	RESERVED_2	
9	RWGE	Read/write global enable. Setting this bit allows access to the context bank registers from any VMID
8	RWE	Read/write enable. Indicates that the RWVMID field is valid.
7:5	RESERVED_1	
4:0	RWVMID	Specifies owner VMID with full read/write access to the registers in the associated context bank "n".

14.21.1.3 SMMU TLB software access registers

0x073FFE00 JPEGD_SMMU_JPEGD_TLBRSW

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Writing to this address requests that the TLB entry at INDEX be read into the SMMU_TLBTRn registers

JPEGD_SMMU_JPEGD_TLBRSW

Bits	Name	Description
31:10	RESERVED	
9:8	TLBBFBS	This field selects the TLB, TFBFB, SLBFB 0x0: Selecting TLB 0x1: Not defined 0x2: Selecting FL BFB 0x3: Selecting SL BFB

JPEGD_SMMU_JPEGD_TLBRSW (cont.)

Bits	Name	Description
7:0	INDEX	TLB index to be read.

0x073FFE80 JPEGD_SMMU_JPEGD_TLBTR0

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

This register holds part of TLB entry read by the last TLBRSW command.

JPEGD_SMMU_JPEGD_TLBTR0

Bits	Name	Description
31:23	RESERVED_4	
22:20	DPSIZC	3 bit decode page size field from CAM-side of TLB CAM-RAM) Same determination and encoding as for DPSIZR The CAM-side copy of this field is used for hit/miss determination in the TLB CAM array
19	RESERVED_3	
18:16	DPSIZR	(3 bit decode page size field from RAM-side of TLB CAM-RAM) Determined from the size fields of the page table entry Encodes the page size as follows: all other values reserved/unused The RAM-side copy of this field is used for virtual ’ physical address formation 0x0: 4KB page 0x1: 64KB page 0x3: 1MB page 0x7: 16MB page
15:12	RESERVED_2	
11	MT2	(memory type bit 2) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[2] attribute bus on the request output of the System MMU

JPEGD_SMMU_JPEGD_TLBTR0 (cont.)

Bits	Name	Description
10	MT1	(memory type bit 1) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[1] attribute bus on the request output of the System MMU
9	MT0	(memory type bit 0) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[0] attribute bus on the request output of the System MMU
8	SH	(shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's outer-shareable realm This field becomes the ASHARED attribute on the request output of the System MMU
7	ISH	(inner-shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's inner-shareable realm This field becomes the AINNERSHARED attribute on the request output of the System MMU
6	NSDESC	(non-secure descriptor) This TLB entry field is a modified version of the corresponding bit of the page table entry Qualified by the NS-prot attribute of the incoming request which prompted the allocation of the TLB entry, such that if the incoming NS-prot attribute was 1 (non-secure), then the NS-desc field of the page table entry was ignored, and the NS-desc field of the TLB entry was forced to 1 Indicates whether the associated memory page contains secure (NS-desc=0) or non-secure (NS-desc=1) information This field becomes the NS-prot attribute on the request output of the System MMU
5	RESERVED_1	

JPEGD_SMMU_JPEGD_TLBTR0 (cont.)

Bits	Name	Description
4	XN	(execute never permission) This TLB entry field comes directly from the corresponding bit of the page table entry
3	UW	(user write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
2	UR	(user read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
1	PW	(privileged write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
0	PR	(privileged read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]

0x073FFE84 JPEGD_SMMU_JPEGD_TLBTR1

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

JPEGD_SMMU_JPEGD_TLBTR1

Bits	Name	Description
31:12	PA	Physical address [31:12] field of the TLB entry
11:5	RESERVED	
4:0	VMID	VMID [4:0]field of the TLB entry)

0x073FFE88 JPEGD_SMMU_JPEGD_TLBTR2

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

JPEGD_SMMU_JPEGD_TLBTR2

Bits	Name	Description
31:12	VA	virtual address field [31:12] of the TLB entry
11	RESERVED	
10	NG	(not global field from page table entry) Indicates whether the page is private to the specified ASID (NG=1) or global to all ASIDs within the VMID using this context bank (NG=0)
9	NSTID	(non-secure tag ID field of the TLB entry) Indicates whether the TLB entry belongs to the secure world (NSTID=0) or the non-secure world (NSTID=1) This field is comned against the incoming NS-prot attribute of the master request as part of TLB hit/miss determination
8	V	valid field of the TLB entry
7:0	ASID	ASID[7:0] field of the TLB entry

0x073FFE8C JPEGD_SMMU_JPEGD_TESTBUSCR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

Governs which signals (if any) from the system SMMU core or wrapper design hierarchy are sent out to the system via a testbus for diagnostic, and also to the system profiling and diagnostic monitor (SPDM).

JPEGD_SMMU_JPEGD_TESTBUSCR

Bits	Name	Description
31:28	SPDM3SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[3]
27:24	SPDM2SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[2]
23:20	SPDM1SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[1]
19:16	SPDM0SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[0]
15:14	TBHSEL	Testbus highselect It governs which set of signals are to testbus[31:16] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL

JPEGD_SMMU_JPEGD_TESTBUSCR (cont.)

Bits	Name	Description
13:12	TBSLSEL	Testbus low select It governs which set of signals are to testbus[15:0] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL
11:10	RESERVED_2	
9:8	WGSEL	Wrapper group select It selects a particular group of signals from the SMMU wrapper hierarchy WGSEL = 0b00 - wrapper signal group 0 WGSEL = 0b01 - wrapper signal group 1 WGSEL = 0b10 - wrapper signal group 2 WGSEL = 0b11 - reserved
7:2	RESERVED_1	
1	SPDMBE	SPDM test enable Reset state : 0
0	TBE	Testbus enable, which governs whether the testbus is driven with all 0s or with the configured signals Reset state : 0

0x073FFEFC JPEGD_SMMU_JPEGD_VR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: 32'h0000_0000

Note that the DCPBP/DCPPP bits prevent the pipelining of the next transaction when the current transaction is a bypass/pass-through transaction. That is, they add one more cycle of delay between the current and next transactions.

Also note that when we are in global bypass (SMMU_CR[CLIENTPD]=1), these bits should have NO effect, or at least no effect between client transactions, they can have an effect between config and client transactions is appropriate. We must be able to continue to perform fully pipelined transactions when the client port is disabled altogether.

JPEGD_SMMU_JPEGD_VR0

Bits	Name	Description
31:3	RESERVED	

JPEGD_SMMU_JPEGD_VR0 (cont.)

Bits	Name	Description
2	DCPPT	Disable client pipelining for client operations in pass-through mode Reset state : 0
1	DCPBP	Disable client pipelining for client operations in bypass mode Reset state : 0
0	DCP	Disable client pipelining Reset state : 0

0x073FFF00 JPEGD_SMMU_JPEGD_TLBIALL

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries.

JPEGD_SMMU_JPEGD_TLBIALL

Bits	Name	Description
31:0	EXEC	Writing any value to this register invalidates all TLB entries, as specified by the contents of SMMU_CR[TLBIALLCFG]

0x073FFF04 JPEGD_SMMU_JPEGD_TLBIVMID

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries matching the IVMID value. Precise function is governed by SMMU_CR[TLBIALLCFG].

JPEGD_SMMU_JPEGD_TLBIVMID

Bits	Name	Description
31:5	RESERVED	
4:0	IVMID	Designates VMID[4:0] value of entries to be invalidated.

14.21.1.4 SMMU configuration registers

0x073FFF80 JPEGD_SMMU_JPEGD_CR

Type: Read/Write
Clock: AXI_BUS_CLOCK

Global configuration register.

JPEGD_SMMU_JPEGD_CR

Bits	Name	Description
31:10	RESERVED_2	
9	RESERVED_1	Reset state : 0
8	TLBIVMIDCFG	TLBIVMID configuration control. When set to 0,flash-invalidate, SMMU_TLBIVMID commands flash-invalidate the entire TLB, without regard to locking ,security and VMID value. When set to 1, selective, SMMU_TLBIVMID invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and VMID field matching the VMID specified by SMMU_TLBIVMID command. Reset state : X
7	TLBIALLCFG	TLBIALL configuration control. When set to 0, flash-invalidate, SMMU_TLBIALL commands flash-invalidate the entire TLB, without regard to locking and/or security. When set to 1, selective, SMMU_TLBIALL invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and are unlocked. Reset state : X
6	TLBLKCRWE	TLBLKCR write enable. When set to 0, writes to SMMU_CBn_TLBLKCR are ignored. When set to 1, allows operating environments to manage the TLB locking mechanism directly. Management among multiple operating environments must be coordinated externally between themselves. Reset state : X
5	STALLD	Global disable for stall mode. When set to 1, context bank stall modes are ignored and operate as terminate mode. Reset state : X
4	CLIENTPD	Client port disable. When set, all client accesses are forced to bypass the system MMU. There is no translation. access control, or attribute generation. This bit overrides individual SMMU_M2VCBRn[BYPASSD] settings; client requests are bypassed, even if SMMU_M2VCBRn[BYPASSD] is set to 1. Bypass request errors are not recorded in SMMU_ESR, nor reported to requesting masters. The SMMU_rpuErrIrptReq interrupt output signal is not asserted. Reset state : 1

JPEGD_SMMU_JPEGD_CR (cont.)

Bits	Name	Description
3	DCDEE	When set to 0, configuration port decode errors do not set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn are not updated. When set to 1, configuration port decode errors set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn updated with address and syndrome of error. Reset state : X
2	RPUEIE	When set, configuration port errors and client port bypass errors are reported directly to the interrupt controller via the SMMU_rputErrIrptReq interrupt output signal. Interrupt output is asserted if SMMU_CR[RPUIE_EN] is 1 and ANY bit is set in SMMU_ESR register. Reset state : 0
1	RPUERE	When set, SMMU reports configuration port errors and client port bypass errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via AXI port will use decode error, rather than slave error. Regardless of the value of this field both configuration port errors and client port bypass request errors are terminated by the SMMU as RAZ/WI, and are recorded in SMMU_ESR register. Reset state : X
0	RPUE	When set, all configuration port accesses are checked against SMMUX_RPU_ACR and/or the SMMUX_CBACRn registers for access permissions. Reset state : 0

14.21.1.5 SMMU error report registers

0x073FFF84 JPEGD_SMMU_JPEGD_EAR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: unknown

When there is an error, holds the physical address of the errant transaction.

JPEGD_SMMU_JPEGD_EAR

Bits	Name	Description
31:0	PA	Physical address[31:0]

0x073FFF88 JPEGD_SMMU_JPEGD_ESR

Type: Read/Write to clear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This register has read/write clear access. Reads return the value in the register, a write with a 1 set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

JPEGD_SMMU_JPEGD_ESR

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR, SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x073FFF8C JPEGD_SMMU_JPEGD_ESRRESTORE

Type: Write
Clock: RPM_BUS_CLK
Reset State: Undefined

This register is an aliased address for SMMU_ESR, but it allows direct write access. In this way, diagnostic software can cause an error to be generated and reported.

JPEGD_SMMU_JPEGD_ESRRESTORE

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR, SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	

JPEGD_SMMU_JPEGD_ESRRESTORE (cont.)

Bits	Name	Description
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x073FFF90 JPEGD_SMMU_JPEGD_ESYNR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

JPEGD_SMMU_JPEGD_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request
15:0	AMID	AMID[15:0] field of errant request

0x073FFF94 JPEGD_SMMU_JPEGD_ESYNR1

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

JPEGD_SMMU_JPEGD_ESYNR1

Bits	Name	Description
31	DCD	(decode) Indicates configuration port error due to invalid/unrecognized address (e.g., a reserved register address) Includes decode errors within both the global address space and the individual context bank address space

JPEGD_SMMU_JPEGD_ESYNR1 (cont.)

Bits	Name	Description
30	AC	(access control) Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO field of the errant request
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request)
15:12	ALEN	ALEN[3:0] field of the errant request
11	RESERVED_2	
10	ABURST	ABURST[1:0] field of the errant request
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request
7	AINST	AINST field of the errant request
6	APROTNS	APROTNS field of the errant request
5	APRIV	APRIV field of the errant request
4	AINNERSHARED	AINNERSHARED field of the errant request
3	ASHARED	ASHARED field of the errant request
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

14.21.1.6 SMMU revision register

0x073FFFF4 JPEGD_SMMU_JPEGD_REV

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the revision information for the SMMU core and wrapper.

JPEGD_SMMU_JPEGD_REV

Bits	Name	Description
31:12	RESERVED	

JPEGD_SMMU_JPEGD_REV (cont.)

Bits	Name	Description
11:8	WRAPPER	Wrapper version
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

14.21.1.7 SMMU implementation parameter register

0x073FFFF8 JPEGD_SMMU_JPEGD_IDR

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the parameter information for the SMMU core and wrapper

JPEGD_SMMU_JPEGD_IDR

Bits	Name	Description
31:24	NIRPT	NIRPT[7:0] Indicates number of context fault interrupt outputs (minus 1) supported by the System MMU Value can range from 0 - 255 (1 - 256 context fault interrupt outputs)
23:16	NCB	NCB[7:0] Indicates number of context banks (minus 1) supported by the System MMU Value can range from 0 - 254 (1 - 255 context banks)
15:12	TLBSIZE	TLBSIZE[3:0] Indicates log2(number of TLB entries) That is, number of TLB entries = 2 ** TLBSIZE
11	RESERVED	
10	HUM	Indicates whether or not TLB hit-under-miss behavior is supported
9	HTW	Indicates whether or not the System MMU supports hardware table walk If hardware table walk not supported (HTW=0), then software cannot set SMMU_CBn_ACTLR[TLBMCFG] to 0b10
8:0	NM2VCBMT	NM2VCBMT[8:0] Indicates number of M2VCBMT entries, with a maximum of 512 The bit width of the M2VCBMTIindex input (maximum value is 9) is equal to log base 2 of NM2VCBMT Allows for up to 7-bit MID field, plus NS-prot or other fields to select mapping [

0x073FFFFC JPEGD_SMMU_JPEGD_RPU_ACR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Using the incoming HVMID, this register controls access to the global register space.

JPEGD_SMMU_JPEGD_RPU_ACR

Bits	Name	Description
31:0	RWE	Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the entire block of registers within the SMMU's 4KB global address space, including this register itself. A VMID identified by this register is also permitted global access to all context banks. In practice, this register designates the VMID(s) that can act as SROT.

14.21.2 SMMU Context Bank Registers

There are a configurable number (1 to 9) of context banks in the SMMU. Each context bank consists of a set of registers in a unique 4KB address space.

14.21.2.1 SMMU context bank control registers

0x07300000+0x1000*n JPEGD_SMMU_JPEGD_CBn_SCTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank System Control Register controls various architected SMMU features

JPEGD_SMMU_JPEGD_CBn_SCTLR

Bits	Name	Description
31:5	RESERVED_2	
4	BE	Governs the order byte order or "endianness" of the page table entries. When set to 0, page table entries are in little endian format, so that their least significant byte is in byte 0 of the 32 bit entry. When set to 1, page table entries are in big endian format, so that their most significant byte is in byte 0 of the 32 bit entry.
3	RESERVED_1	Reserved for HAF, Hardware access flag. This bit governs whether the access flag is managed by hardware or software. The SMMU supports software access flag management only, so this bit is read-only and internally driven to 0.

JPEGD_SMMU_JPEGD_CBn_SCTLR (cont.)

Bits	Name	Description
2	AFE	Access flag enable. When AFE = 0, the access flag field is not supported and the AP[0] page table entry field acts as a bit of the overall AP[2:0] field to determine access permissions. When AFE = 1, the AP[0] page table entry field becomes the access flag, and the reduced number of access permission combinations is specified by AP2:1], and SMMU hardware will signal an Access Flag fault if a request targets a page for which the access flag is 0.
1	TRE	TEX remap enable. This bit governs the mapping of the page table entry TEX[2:0],C,B and SH fields into an SMMU TLB entry, and thus the translation of the AMEMTYPE[2:0], ASHARED and AINNERSHARED bus attributes. When TRE = 0, the TLB value is determined directly from the page table entry fields.
0	M	MMU enable bit. When set to 1, this context bank is enabled for translating requests. When set to 0, accesses bypass the TLB, and there is no address translation, access permission checking or attribute mapping. Incoming master requests are passed through unchanged.

0x07300004+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_ACTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank auxiliary control register controls various implementation specific features.

JPEGD_SMMU_JPEGD_CBn_ACTLR

Bits	Name	Description
31:19	RESERVED	
18	RESERVED_2	
17:16	V2PCFG	VA-to-PA configuration. Governs operation of VA-to-PA commands that miss in the TLB 0x0: terminate (Record TLB Miss context fault in SMMU_CBn_PAR) 0x1: software table update (Translate based on values in SMMU_CBn_TLBFLPTER and SMMU_CBn_TLBSLPTER) 0x2: hardware table walk (Translate based on value of PTE read from page table in memory) 0x3: reserved

JPEGD_SMMU_JPEGD_CBn_ACTLR (cont.)

Bits	Name	Description
15	TIPCF	Governs whether or not all subsequent requests using this context bank should be terminated if a prior context fault has occurred and has not yet been cleared from SMMU_CBn_FSR Accesses to other context banks proceed as normal 0x0: do not terminate (System MMU will attempt to process subsequent requests despite the presence of an existing context fault in SMMU_CBn_FSR. SMMU_CBn_FSR will be set if the subsequent access also encounters a context fault) 0x1: terminate (All subsequent accesses terminated by the System MMU as RAZ/WI, even if SMMU_CBn_ACTLR[TLBMCFG, CFCFG] configured for stall mode. SMMU_CBn_FSR set when access is terminated due to TIPCF = 1. Presence of SMMU_CBn_FSR when SMMU_CBn_ACTLR is 1 implies that the later exceptions must have been simply the forced terminations due to the prior context fault. Error optionally reported to the requesting master, according to the client port bus protocol, f SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus if SMMU_CBn_ACTLR is 1.)
14	CFCFG	(context fault configuration) Governs the behavior of all context faults except TLB miss TLB miss context faults are governed by SMMU_CBn_ACTLR[TLBMCFG] 0x0: terminate (Access terminates at the System MMU as RAZ/WI. Context fault exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x1: stall (Requesting master's access stalled while System MMU waits for managing processor to resolve context fault. Context fault exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode)

JPEGD_SMMU_JPEGD_CBn_ACTLR (cont.)

Bits	Name	Description
13:12	TLBMCFG	(TLB miss configuration) Governs the behavior of client accesses that miss in the TLB 0x0: pass-through (Access passed through to targeted slave without translation, attribute control, or access permission checking. Effectively, behavior is as if SMMU_CBn_SCTLR = 0 i.e., MMU disabled for this context bank. TLB miss not considered a context fault. TLB miss exception not recorded in SMMU_CBn_FSR. TLB miss exception not reported to requesting master. SMMU_contextFaultIrptReq interrupt output not asserted) 0x1: terminate (Access terminates at the System MMU as RAZ/WI,TLB miss exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x2: stall (Requesting master's access stalled while System MMU waits for managing processor to update TLB. TLB miss exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode) 0x3: HTW (Hardware table walk. Requesting master's access stalled while System MMU accesses page table. The is TLB updated and requesting master's access resumed after obtaining valid entry from page table. If translation fault, then access either terminates or stalls according to setting of SMMU_CBn_ACTLR)
11	DNLV2PA	(disable non-locking VA-to-PA allocation) Governs whether or not TLB misses due to non-locking VA-to-PA commands will allocate a new entry This field is ignored for locking VA-to-PA operations (SMMU_CBn_TLBLKCR[LKE] = 1)
10	DNA	(disable normal allocation) Governs whether or not TLB misses due to client port accesses will allocate a new entry
9:8	PRIVCFG	0x0: apriv (System MMU uses APRIV signal supplied by master as user/supervisor indicator 1 = supervisor) 0x1: reserved 0x2: User (System MMU ignores APRIV; treats all requests using this context bank as user) 0x3: Supervisor (System MMU ignores APRIV; treats all requests using this context bank as supervisor)

JPEGD_SMMU_JPEGD_CBn_ACTLR (cont.)

Bits	Name	Description
7:5	RESERVED_1	
4	RCNSH	(redirect cacheable-non-shareable) Governs whether or not cacheable accesses that are non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache, even though the locations are not being coherently shared with Scorpion-MP
3	RCISH	(redirect cacheable-inner-shareable) Governs whether or not cacheable accesses that are inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
2	RCOSH	(redirect cacheable-outer-shareable) Governs whether or not cacheable accesses that are outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
1	CFEIE	(context fault error interrupt enable) Governs whether or not client port request context faults are reported directly to the interrupt controller via the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus Interrupt output is asserted if SMMU_CBn_ACTLR[CFEIE] is 1 and any context fault bits are set in SMMU_CBn_FSR Such interrupts would generally be directed to the interrupt controller of whichever processor is currently managing this context bank of the System MMU Reset state : 0
0	CFERE	(context fault error report enable) Governs whether or not client port request context faults that are configured for terminate mode (or that are explicitly terminated after stall mode) are reported to the requesting master, according to the client port bus protocol All error types reported via AXI port will use decode error rather than slave error All context faults are recorded in SMMU_CBn_FSR, regardless of the value of this field.

0x07300008+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_CONTEXTIDR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context ID register holds the ASID associated with this context bank

JPEGD_SMMU_JPEGD_CBn_CONTEXTIDR

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Specifies the 8 bit ASID value assigned to this context bank. The ASID can be included in the key comparison of TLB entries. .

0x07300010+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_TTBR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR0 is used for low order virtual addresses, typically private pages for a given process.

JPEGD_SMMU_JPEGD_CBn_TTBR0

Bits	Name	Description
31:7	PA	BIts 31:7 of the physical address of the base of the page table. The actual LSB of the base address is bit 14-N, where N is set in register TTCR
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07300014+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_TTBR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR1 is used for high order virtual addresses, typically global pages for a given VMID, or kernel mappings.

The context bank auxiliary control register controls various implementation specific features.

JPEGD_SMMU_JPEGD_CBn_TTBR1

Bits	Name	Description
31:14	PA	BIts 31:14 of the physical address of the base of the page table.
13:7	RESERVED_2	
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED_1	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07300018+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_TTBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table control register, which specifies the size of the virtual address space that uses TTBR0.

JPEGD_SMMU_JPEGD_CBn_TTBCR

Bits	Name	Description
31:6	RESERVED_2	
5	PD1	Page disable 1; if this bit is set, hardware table walks attempting to use TTBR1will result in a first level descriptor translation fault. If clear, TTBR1 contents are used.
4	PD0	Page disable 0; if this bit is set, hardware table walks attempting to use TTBR0 will result in a first level descriptor translation fault. If clear, TTBR0 contents are used.
3	RESERVED_1	
2:0	N	N[2:0] specifies the number of upper order virtual address bits which must be 0 in order for translations to use the table pointed to by TTBR0. If any of these bits are non-zero, TTBR1 is used for the lookup. If N is 0, only TTBR0 is used.

0x0730001C+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_PAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The physical address register captures the physical address value resulting from the execution of a VA-to-PA command

Field definitions vary according to whether or not there is a context fault associated with the requested translation

JPEGD_SMMU_JPEGD_CBn_PAR

Bits	Name	Description
31:12	PAR_FAULT_INFO_312	
11	RESERVED_2	
10:9	PAR_FAULT_INFO_72	
8	RESERVED_1	
7:1	PAR_FAULT_INFO_71	Encoding varies according to value in FAULT field.
0	FAULT	(fault status) This field will be 1 when a context fault is associated with the requested translation, and 0, when there is no context fault associated with the requested translation.

0x07300020+0x1000*n JPEGD_SMMU_JPEGD_CBn_FSR, n=[0..1]

Type: Read/WriteClear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The Fault Status Register records status information for client accesses that encounter exceptions within the context bank, e.g. translation faults.This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data

This prevents inadvertent clearing of new faults when writing the register to clear an old fault

The presence of an asserted value on any bit in this register (except the SS bit) is what prompts the assertion (when enabled by SMMU_CBn_ACTLR[CFEIE]) of the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus

Therefore, these bits must be cleared by the interrupt handler

This is contrasted with the fields in the SMMU_CBn_FSYNRn registers, which are merely the "syndrome" of the fault indicated by SMMU_CBn_FSR

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JPEGD_SMMU_JPEGD_CBn_FSR

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	

JPEGD_SMMU_JPEGD_CBn_FSR (cont.)

Bits	Name	Description
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07300024+0x1000*n JPEGD_SMMU_JPEGD_CBn_FSRRESTORE, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Allows SW to force a value into the SMMU_CBn_FSR register.

JPEGD_SMMU_JPEGD_CBn_FSRRESTORE

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)

JPEGD_SMMU_JPEGD_CBn_FSRRESTORE (cont.)

Bits	Name	Description
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07300028+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_FAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The Fault Address Register records the virtual address of client accesses that encounter exceptions within the context bank, e.g. translation faults. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

JPEGD_SMMU_JPEGD_CBn_FAR

Bits	Name	Description
31:0	VA	VA[31:0] of errant client access

0x0730002C+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_FSYNR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

NOTE omission of VMID field from this register, as VMID can only be made visible to SROT, and not to general OS software that manages the context bank registers

JPEGD_SMMU_JPEGD_CBn_FSYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] (ATID field of errant request)

JPEGD_SMMU_JPEGD_CBn_FSYNR0 (cont.)

Bits	Name	Description
23:16	RESERVED	
15:13	ABID	ABID[2:0] (ABID field of errant request)
12:8	APID	APID[4:0] (APID field of errant request)
7:0	AMID	AMID[7:0] (AMID field of errant request)

0x07300030+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_FSYNR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

JPEGD_SMMU_JPEGD_CBn_FSYNR1

Bits	Name	Description
31:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO (AOOO field of the errant request)
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request
15:12	ALEN	ALEN[3:0]field of the errant request
11	RESERVED_2	
10	ABURST	field of the errant request
9	RESERVED_1	
8	AWRITE	field of the errant request
7	AINST	field of the errant request
6	APROTNS	field of the errant request
5	APRIV	field of the errant request
4	AINNERSHARED	(AINNERSHARED field of the errant request)
3	ASHARED	(ASHARED field of the errant request)

JPEGD_SMMU_JPEGD_CBn_FSYNR1 (cont.)

Bits	Name	Description
2:0	AMEMTYPE	AMEMTYPE[2:0] (AMEMTYPE field of the errant request)

0x07300034+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_PRRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs memory type and shareability attributes of requests that are both MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1)

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) and/or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, memory type encoding is as follows:

0b00 = strongly-ordered

0b01 = device

0b10 = normal

0b11 = reserved

JPEGD_SMMU_JPEGD_CBn_PRRR

Bits	Name	Description
31	NOS7	not-outer-shareable class 7
30	NOS6	not-outer-shareable class 6
29	NOS5	not-outer-shareable class 5
28	NOS4	not-outer-shareable class 4
27	NOS3	not-outer-shareable class 3
26	NOS2	not-outer-shareable class 2
25	NOS1	not-outer-shareable class 1
24	NOS0	not-outer-shareable class 0
23:20	RESERVED	

JPEGD_SMMU_JPEGD_CBn_PRRR (cont.)

Bits	Name	Description
19	SHNMSH1	(shareable attribute for normal memory accesses with SH=1) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1
18	SHNMSH0	(shareable attribute for normal memory accesses with SH=0) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0
17	SHDSH1	SHDSH1 (shareable attribute for device accesses with SH=1) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1 [
16	SHDSH0	SHDSH0 (shareable attribute for device accesses with SH=0) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0 [
15:14	MTC7	MTC7[1:0] (memory type class 0)
13:12	MTC6	MTC6[1:0] (memory type class 0)
11:10	MTC5	MTC5[1:0] (memory type class 0)
9:8	MTC4	MTC4[1:0] (memory type class 0)
7:6	MTC3	MTC3[1:0] (memory type class 0)
5:4	MTC2	MTC2[1:0] (memory type class 0)
3:2	MTC1	MTC1[1:0] (memory type class 0)
1:0	MTC0	MTC0[1:0] (memory type class 0)

0x07300038+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_NMRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs the cache policy of MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1) requests for which the memory type is mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0) or the memory type is mapped to a type other than normal memory (SMMU_CBn_PRRR[MTCn] != 0b10)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, inner-cache and outer-cache policy encodings are as follows:

0b00 = non-cacheable

0b01 = cacheable, copy-back, write-allocate

0b10 = cacheable, write-through, write-no-allocate

0b11 = cacheable, copy-back, write-no-allocate

JPEGD_SMMU_JPEGD_CBn_NMRR

Bits	Name	Description
31:30	OCPC7	OCPC7[1:0] (inner-cache policy class 7)
29:28	OCPC6	OCPC6[1:0] (inner-cache policy class 6)
27:26	OCPC5	OCPC5[1:0] (inner-cache policy class 5)
25:24	OCPC4	OCPC4[1:0] (inner-cache policy class 4)
23:22	OCPC3	OCPC3[1:0] (inner-cache policy class 3)
21:20	OCPC2	OCPC2[1:0] (inner-cache policy class 2)
19:18	OCPC1	OCPC1[1:0] (inner-cache policy class 1)
17:16	OCPC0	OCPC0[1:0] (inner-cache policy class 0)
15:14	ICPC7	ICPC7[1:0] (inner-cache policy class 7)
13:12	ICPC6	ICPC6[1:0] (inner-cache policy class 6)
11:10	ICPC5	ICPC5[1:0] (inner-cache policy class 5)
9:8	ICPC4	ICPC4[1:0] (inner-cache policy class 4)
7:6	ICPC3	ICPC3[1:0] (inner-cache policy class 3)
5:4	ICPC2	ICPC2[1:0] (inner-cache policy class 2)
3:2	ICPC1	ICPC1[1:0] (inner-cache policy class 1)
1:0	ICPC0	ICPC0[1:0] (inner-cache policy class 0)

0x0730003C+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_TLBLKCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB lock control register governs the TLB locking mechanism and TLB invalidate operations.Write access to this register is governed by SMMU_CR[TLBLKCRWE]

When SMMU_CR[TLBLKCRWE] is 0, writes to SMMU_CBn_TLBLKCR are ignored

Read access is still permitted

SROT can set SMMU_CR[TLBLKCRWE] to 1 to allow operating environment(s) to manage the TLB locking mechanism

Management amongst multiple operating environments must be coordinated via semaphore

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JPEGD_SMMU_JPEGD_CBn_TLBLKCR

Bits	Name	Description
31:24	RESERVED_2	
23:16	VICTIM	VICTIM[7:0] Indicates the TLB index at which the next normal (non-locking) allocation will occur Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context
15:8	FLOOR	FLOOR[7:0] Indicates the TLB index from which round-robin replacement on normal (non-locking) allocations occurs TLB entries at indices below this value are locked Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context banks
7:4	RESERVED_1	
3	TLBIVAACFG	(TLBIVAA configuration) TLBIVAACFG = 0 - flash-invalidate SMMU_CBn_TLBIVAA commands flash-invalidate the entire TLB, without regard to locking, security, address, and/or VMID value TLBIVAACFG = 1 - selective SMMU_CBn_TLBIVAA commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank VA field of TLB entry matches VA designated by SMMU_CBn_TLBIVAA command NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked

JPEGD_SMMU_JPEGD_CBn_TLBLKCR (cont.)

Bits	Name	Description
2	TLBIASIDCFG	(TLBIASID configuration) TLBIASIDCFG = 0 - flash-invalidate SMMU_CBn_TLBIASID commands flash-invalidate the entire TLB, without regard to locking, security, VMID, and/or ASID values TLBIASIDCFG = 1 - selective SMMU_CBn_TLBIASID commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command TLB entry is not global (NG field is 1) NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
1	TLBIALLCFG	(TLBIALL configuration) TLBIALLCFG = 0 - flash-invalidate SMMU_CBn_TLBIALL commands flash-invalidate the entire TLB, without regard to locking, security, and/or VMID value TLBIALLCFG = 1 - selective SMMU_CBn_TLBIALL commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked
0	LKE	(lock enable) Governs whether or not TLB entries established by VA-to-PA commands upon TLB misses are locked LKE = 0 (normal, non-locking) Allocate VA-to-PA TLB entry (if TLB miss) at the index specified by SMMU_CBn_TLBLKCR[VICTIM] Allocation is disabled if SMMU_CBn_ACTLR[DNLV2PA] is 1 Increment SMMU_CBn_TLBLKCR[VICTIM] by 1 (only if new entry allocated) Wrap back to the value of SMMU_CBn_TLBLKCR[FLOOR] when the last entry is written LKE = 1 (locking) Search TLB for specified VA and invalidate if found Provides atomicity between the invalidate and the new allocation within the locked region Allocate VA-to-PA TLB entry at the index specified by data operand bits 7:0 of the VA-to-PA command This value must be less than SMMU_CBn_TLBLKCR[FLOOR] in order for it to remain locked Allocation occurs even if non-locking allocation is disabled due to SMMU_CBn_ACTLR[DNLV2PA] = 1

0x07300040+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_V2PSR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The VA-to-PA status register records the hit/miss status and TLB index or V2Pxx and TLB invalidate commands.

JPEGD_SMMU_JPEGD_CBn_V2PSR

Bits	Name	Description
31:16	RESERVED_2	
15:8	INDEX	INDEX[7:0] Indicates the index of the TLB entry associated with the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command If SMMU_CBn_V2PSR[HIT] is 0, then SMMU_CBn_V2PSR[INDEX] is the index to which the entry was allocated (if allocated at all) If SMMU_CBn_V2PSR[HIT] is 1, then SMMU_CBn_V2PSR[INDEX] is the index of the entry which hit
7:1	RESERVED_1	
0	HIT	Indicates whether or not there was a TLB hit (prior to allocation, if any) on the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command

0x07300044+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_TLBFLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB first level PTE register holds the first level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

This register (together with SMMU_CBn_TLBSLPTER) is used as the source of the translation information for VA-to-PA operations when the MMU is enabled (SMMU_CBn_SCTLR[M] = 1) and the operations are configured for software table update (SMMU_CBn_ACTLR[V2PCFG] = 0b01)

Field definitions vary according to the type of PTE (fault, page, section, or supersection), and come directly from the ARMv7 architecture's PTE formats

JPEGD_SMMU_JPEGD_CBn_TLBFLPTER

Bits	Name	Description
31:10	FL_PTE_HI	

JPEGD_SMMU_JPEGD_CBn_TLBFLPTER (cont.)

Bits	Name	Description
9:5	RESERVED	
4:2	FL_PTE_LO	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	This field should be set to 0b00 or 0b11 to indicate that the translation should result in a context fault, and the rest of the fields are defined as indicated in this section If this field is not 0b00 or 0b11, then the PTE is of some other type (see other sections for the field definitions for those types)

0x07300048+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_TLBSLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB second level PTE register holds the second level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

Field definitions vary according to the type of PTE (fault, 64KB or 4KB), and come directly from the ARMv7 architecture's PTE format

JPEGD_SMMU_JPEGD_CBn_TLBSLPTER

Bits	Name	Description
31:2	SL_PTE	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	0x0: fault

0x0730004C+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_BFBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The burst fetch buffer configuration register governs the operation of the "burst fill" feature of the SMMU.

JPEGD_SMMU_JPEGD_CBn_BFBCR

Bits	Name	Description
31:12	STRIDE	(stride amount) 4KB-aligned value to be added to virtual address on demand TLB miss for filling subsequent BFB Stride of minimum 4KB alignment useful for preventing stride burst fetch until final PTE of the demand BFB entry is used
11:8	SLVIC	(second-level victim) Indicates the SLBFB index at which the next round-robin allocation will occur
7:4	FLVIC	(first-level victim) Indicates the FLBFB index at which the next round-robin allocation will occur
3	RESERVED	
2	SFVS	(stride-fetch victim selection) SFVS. = 0 (replace normal round-robin victim-selected entry) Useful when stride is larger than the VA space represented by the four PTEs in the demand BFB entry, but the client access pattern is for more than just the initial PTE in that demand BFB entry SFVS. = 1 (replace same BFB used by demand VA for which the stride burst is being performed) Useful when stride is the same as the VA space represented by an individual PTE in the demand BFB entry (such that the stride won't miss against the BFB until the last PTE of the demand BFB entry is accessed), and/or when the client access pattern only uses the initial PTE in the demand BFB entry
1	BFBSFE	(burst fetch buffer stride fetch enable) Enables stride burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Stride burst fetch is for the block of four PTEs associated with VA+stride VA is the "demanded" VA from the client (or VA-to-PA command) Stride value is specified by SMMU_CBn_BFBCR[STRIDE] Stride burst fetch only occurs if demand access for VA misses in TLB (could hit in BFB) and address VA+stride misses in both TLB and BFB
0	BFBDFE	(burst fetch buffer demand fetch enable) Enables demand burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Demand burst fetch is for the block of four PTEs associated with the "demanded" VA from the client (or VA-to-PA command) Demand burst fetch only occurs if demand access misses in both TLB and BFB

0x07300800+0x1000*n JPEGD_SMMU_JPEGD_CBn_TLBIALL, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate all command register invalidates all TLB entries matching the VMID associated with this context bank. Data operand is ignored.

JPEGD_SMMU_JPEGD_CBn_TLBIALL

Bits	Name	Description
31:0	RESERVED	

0x07300804+0x1000*n JPEGD_SMMU_JPEGD_CBn_TLBIASID, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by ASID command register invalidates TLB entries matching the specified ASID and matching the VMID associated with this context bank.Invalidates TLB entries which are associated with the designated ASID and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIASIDCFG] governs whether command flash-invalidates entire TLB array or just the entries matching the VMID, ASID, and security state

TLBIASIDCFG = 0 - flash-invalidate

SMMU_CBn_TLBIASID command flash-invalidates the entire TLB, without regard to locking, security, VMID, and/or ASID values

TLBIASIDCFG = 1 - selective

SMMU_CBn_TLBIASID command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command data operand

TLB entry is not global (NG field is 1)

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command

Locking is not considered (matching entries are invalidated even if locked)

ASID field of command specifies the ASID value of the TLB entries to be invalidated

JPEGD_SMMU_JPEGD_CBn_TLBIASID

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Actual ASID value

0x07300808+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_TLBIVA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA command invalidates TLB entries matching the designated VA, ASID and the VMID associated with this context bank.

Matching entry determined as follows:

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIVA command data operand (or TLB entry is global - NG field is 0)

VA field of TLB entry matches VA value designated by the SMMU_CBn_TLBIVA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIVA command

Locking is not considered (matching entry is invalidated even if locked)

Data operand specifies the VA and ASID value of the TLB entry to be invalidated

JPEGD_SMMU_JPEGD_CBn_TLBIVA

Bits	Name	Description
31:12	VA	VA[31:12]
11:8	RESERVED	
7:0	ASID	ASID[7:0] value

0x0730080C+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_TLBIVAA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA all ASIDS command invalidates TLB entries matching the designated VA and the VMID associated with this context bank, regardless of ASID.Invalidates TLB entries which are associated with the designated VA, regardless of ASID, and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIVAACFG] governs whether command flash-invalidates entire TLB array or just the non-locked entries matching the VMID, ASID, and security state

TLBIVAACFG = 0 - flash-invalidate

SMMU_CBn_TLBIVAA command flash-invalidates the entire TLB, without regard to locking, security, address, and/or VMID value

TLBIVAACFG = 1 - selective

SMMU_CBn_TLBIVAA command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

VA field of TLB entry matches VA designated by the SMMU_CBn_TLBIVAA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command

Entry is unlocked

JPEGD_SMMU_JPEGD_CBn_TLBIVAA

Bits	Name	Description
31:12	VA	VA[31:12]
11:0	RESERVED	

0x07300810+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_V2PRR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

JPEGD_SMMU_JPEGD_CBn_V2PRR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07300814+0x1000*n JPEGD_SMMU_JPEGD_CBn_V2PPW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

JPEGD_SMMU_JPEGD_CBn_V2PPW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07300818+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_V2PUR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

JPEGD_SMMU_JPEGD_CBn_V2PUR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x0730081C+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_V2PUW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

.Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

JPEGD_SMMU_JPEGD_CBn_V2PUW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	

JPEGD_SMMU_JPEGD_CBn_V2PUW (cont.)

Bits	Name	Description
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07300820+ 0x1000*n JPEGD_SMMU_JPEGD_CBn_RESUME, n=[0..1]

Type: Write/command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB resume command causes the SMMU to resume operation after a stalled access..

JPEGD_SMMU_JPEGD_CBn_RESUME

Bits	Name	Description
31:1	RESERVED	
0	TNR	Terminate/not retry When TNR is written as 0, indicates that the stalled access should be retried by the system MMU. When written as 1, indicates that this stalled transaction is terminated by the system MMU. The error is optionally reported to the requesting master, using the client port bus protocol, if SMMU_CNn_ACTLR[CFERE] == 1. Interrupt optionally remains asserted via SMMU_M2VCBRn[IRPTINDX] selected SMMU_contextFaultIrptReq bit, only if SMMU_CBn_ACTLR[CFEIE] is 1, and only if SMMU_CBn_FSR has not been cleared by software priori to issuing this command..

14.22 VPE SMMU Registers (0x07400000 SMMU_VPE_BASE)

This section contains the VPE SMMU registers.

14.22.1 SMMU Global Registers

14.22.1.1 SMMU VMID/CBNDX mapping registers

0x074FF000+ 0x4*n VPE_SMMU_VPE_M2VCBRn, n=[0..1]

Type: Read/Write
Clock: AXI_CLK
Reset State: Undefined

SMMU_M2VCBRm registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

VPE_SMMU_VPE_M2VCBRn

Bits	Name	Description
31:28	RESERVED_2	
27:25	BPMEMTYPE	(bypass memory type) Supplies the AMEMTYPE attributes for client requests which bypass the System MMU when SMMU_M2VCBRn[BPMTCFG] = 1 See reference section for AMEMTYPE encoding definitions
24	BPMTCFG	(bypass memory type configuration) Governs the memory type (AMEMTYPE) attributes of client requests which bypass the System MMU BPMTCFG = 0 - use AMEMTYPE Bypass requests use AMEMTYPE signal supplied by client master BPMTCFG = 1 - use SMMU_M2VCBRn[BPMEMTYPE] Bypass requests use SMMU_M2VCBRn[BPMEMTYPE] Reset state : 0
23:22	NSCFG	(non-secure configuration) Governs the incoming security designation of client requests NSCFG = 0b00 - use APROTNS Use APROTNS signal supplied by client master NSCFG = 0b01 - reserved NSCFG = 0b10 - secure System MMU ignores APROTNS; treats all requests as secure NSCFG = 0b11 - non-secure System MMU ignores APROTNS; treats all requests as non-secure Reset state : 0

VPE_SMMU_VPE_M2VCBRn (cont.)

Bits	Name	Description
21:20	BPSHCFG	(bypass shareability configuration) Governs the shareability realm (ASHARED and AINNERSHARED) attributes of client requests which bypass the System MMU BPSHCFG = 0b00 - use ASHARED and AINNERSHARED Bypass requests use ASHARED and AINNERSHARED signals supplied by client master BPSHCFG = 0b01 - outer-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 0 BPSHCFG = 0b10 - inner-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 1 BPSHCFG = 0b11 - non-shareable Bypass requests set ASHARED = 0, AINNERSHARED = 0 Reset state : 0
19	BPRCNSH	(bypass redirect cacheable-non-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache Reset state : 0
18	BPRCISH	(bypass redirect cacheable-inner-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0
17	BPRCOSH	(bypass redirect cacheable-outer-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0

VPE_SMMU_VPE_M2VCBRn (cont.)

Bits	Name	Description
16	BYPASSD	Bypass disable for this index Governs whether or not client port accesses using this mapping table entry are actually permitted to "bypass" the System MMU when such bypass is indicated (either due to CBNDX = 255 or due to the master asserting the "SMMU bypass" input) This field is ignored (and operates as if it were 0) if SMMU_CR[CLIENTPD] is 1 BYPASSD = 0 - bypass enabled Bypass requests truly bypass the System MMU and "pass-through" to the fabric (no translation, access control, or attribute generation) No cycle of latency for System MMU context bank access Bypass request not considered an error Bypass request error not recorded in SMMU_ESR[BYPASS] Bypass error not reported to requesting master SMMU_rpuErrIrptReq interrupt output not asserted Client accesses still reference M2VCBMT to get VMID value for presentation to fabric BYPASSD = 1 - bypass disabled System MMU terminates the access as RAZ/WI Bypass request is considered an error Bypass request error is recorded in SMMU_ESR[BYPASS] If SMMU_CR[RPUERE] is 1, then bypass error reported to requesting master according to the client port bus protocol If SMMU_CR[RPUEIE] is 1, then SMMU_rpuErrIrptReq interrupt output asserted
15:8	CBNDX	Context bank index Context bank index associated with the M2VCBMT index CBNDX = 255 indicates no context bank assigned ("bypass")
7:5	RESERVED_1	
4:0	VMID	Virtual machine ID VMID value associated with the M2VCBMT index Must be programmed consistently with the SMMU_CBACRn[CBVMID] field for the context bank designated by SMMU_M2VCBRm[CBNDX]

14.22.1.2 SMMU context bank access control registers

0x074FF800+ 0x4*n VPE_SMMU_VPE_CBACRn, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs configuration port access to the associated context bank registers.

VPE_SMMU_VPE_CBACRn

Bits	Name	Description
31:24	IRPTNDX	(interrupt index) Interrupt output number used for context faults associated with this context bank (use SMMU_contextFaultIrptReq[IRPTNDX])
23:21	RESERVED	
20:16	CBVMID	(context bank VMID) Specifies the VMID with which the client masters using the context bank are associated Must be programmed consistently with the M2VCBMT entries that are configured to use the associated context bank This field is used by configuration port commands that need the context bank's VMID value in order to access the TLB (e.g., SMMU_CBn_TLBIVMID, SMMU_CBn_V2Pxx)
15:10	RESERVED_2	
9	RWGE	Read/write global enable. Setting this bit allows access to the context bank registers from any VMID
8	RWE	Read/write enable. Indicates that the RWVMID field is valid.
7:5	RESERVED_1	
4:0	RWVMID	Specifies owner VMID with full read/write access to the registers in the associated context bank "n".

14.22.1.3 SMMU TLB software access registers

0x074FFE00 VPE_SMMU_VPE_TLBRSW

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Writing to this address requests that the TLB entry at INDEX be read into the SMMU_TLBTRn registers

VPE_SMMU_VPE_TLBRSW

Bits	Name	Description
31:10	RESERVED	
9:8	TLBBFBS	This field selects the TLB, TFBFB, SLBFB 0x0: Selecting TLB 0x1: Not defined 0x2: Selecting FL BFB 0x3: Selecting SL BFB

VPE_SMMU_VPE_TLBRSW (cont.)

Bits	Name	Description
7:0	INDEX	TLB index to be read.

0x074FFE80 VPE_SMMU_VPE_TLBTR0

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

This register holds part of TLB entry read by the last TLBRSW command.

VPE_SMMU_VPE_TLBTR0

Bits	Name	Description
31:23	RESERVED_4	
22:20	DPSIZC	3 bit decode page size field from CAM-side of TLB CAM-RAM) Same determination and encoding as for DPSIZR The CAM-side copy of this field is used for hit/miss determination in the TLB CAM array
19	RESERVED_3	
18:16	DPSIZR	(3 bit decode page size field from RAM-side of TLB CAM-RAM) Determined from the size fields of the page table entry Encodes the page size as follows: all other values reserved/unused The RAM-side copy of this field is used for virtual ’ physical address formation 0x0: 4KB page 0x1: 64KB page 0x3: 1MB page 0x7: 16MB page
15:12	RESERVED_2	
11	MT2	(memory type bit 2) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[2] attribute bus on the request output of the System MMU

VPE_SMMU_VPE_TLBTR0 (cont.)

Bits	Name	Description
10	MT1	(memory type bit 1) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[1] attribute bus on the request output of the System MMU
9	MT0	(memory type bit 0) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[0] attribute bus on the request output of the System MMU
8	SH	(shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's outer-shareable realm This field becomes the ASHARED attribute on the request output of the System MMU
7	ISH	(inner-shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's inner-shareable realm This field becomes the AINNERSHARED attribute on the request output of the System MMU
6	NSDESC	(non-secure descriptor) This TLB entry field is a modified version of the corresponding bit of the page table entry Qualified by the NS-prot attribute of the incoming request which prompted the allocation of the TLB entry, such that if the incoming NS-prot attribute was 1 (non-secure), then the NS-desc field of the page table entry was ignored, and the NS-desc field of the TLB entry was forced to 1 Indicates whether the associated memory page contains secure (NS-desc=0) or non-secure (NS-desc=1) information This field becomes the NS-prot attribute on the request output of the System MMU
5	RESERVED_1	

VPE_SMMU_VPE_TLBTR0 (cont.)

Bits	Name	Description
4	XN	(execute never permission) This TLB entry field comes directly from the corresponding bit of the page table entry
3	UW	(user write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
2	UR	(user read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
1	PW	(privileged write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
0	PR	(privileged read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]

0x074FFE84 VPE_SMMU_VPE_TLBTR1

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

VPE_SMMU_VPE_TLBTR1

Bits	Name	Description
31:12	PA	Physical address [31:12] field of the TLB entry
11:5	RESERVED	
4:0	VMID	VMID [4:0]field of the TLB entry)

0x074FFE88 VPE_SMMU_VPE_TLBTR2

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

VPE_SMMU_VPE_TLBTR2

Bits	Name	Description
31:12	VA	virtual address field [31:12] of the TLB entry
11	RESERVED	
10	NG	(not global field from page table entry) Indicates whether the page is private to the specified ASID (NG=1) or global to all ASIDs within the VMID using this context bank (NG=0)
9	NSTID	(non-secure tag ID field of the TLB entry) Indicates whether the TLB entry belongs to the secure world (NSTID=0) or the non-secure world (NSTID=1) This field is comned against the incoming NS-prot attribute of the master request as part of TLB hit/miss determination
8	V	valid field of the TLB entry
7:0	ASID	ASID[7:0] field of the TLB entry

0x074FFE8C VPE_SMMU_VPE_TESTBUSCR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

Governs which signals (if any) from the system SMMU core or wrapper design hierarchy are sent out to the system via a testbus for diagnostic, and also to the system profiling and diagnostic monitor (SPDM).

VPE_SMMU_VPE_TESTBUSCR

Bits	Name	Description
31:28	SPDM3SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[3]
27:24	SPDM2SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[2]
23:20	SPDM1SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[1]
19:16	SPDM0SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[0]
15:14	TBHSEL	Testbus highselect It governs which set of signals are to testbus[31:16] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL

VPE_SMMU_VPE_TESTBUSCR (cont.)

Bits	Name	Description
13:12	TBSLSEL	Testbus low select It governs which set of signals are to testbus[15:0] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL
11:10	RESERVED_2	
9:8	WGSEL	Wrapper group select It selects a particular group of signals from the SMMU wrapper hierarchy WGSEL = 0b00 - wrapper signal group 0 WGSEL = 0b01 - wrapper signal group 1 WGSEL = 0b10 - wrapper signal group 2 WGSEL = 0b11 - reserved
7:2	RESERVED_1	
1	SPDMBE	SPDM test enable Reset state : 0
0	TBE	Testbus enable, which governs whether the testbus is driven with all 0s or with the configured signals Reset state : 0

0x074FFEFC VPE_SMMU_VPE_VR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: 32'h0000_0000

Note that the DCPBP/DCPPP bits prevent the pipelining of the next transaction when the current transaction is a bypass/pass-through transaction. That is, they add one more cycle of delay between the current and next transactions.

Also note that when we are in global bypass (SMMU_CR[CLIENTPD]=1), these bits should have NO effect, or at least no effect between client transactions, they can have an effect between config and client transactions is appropriate. We must be able to continue to perform fully pipelined transactions when the client port is disabled altogether.

VPE_SMMU_VPE_VR0

Bits	Name	Description
31:3	RESERVED	

VPE_SMMU_VPE_VR0 (cont.)

Bits	Name	Description
2	DCPPT	Disable client pipelining for client operations in pass-through mode Reset state : 0
1	DCPBP	Disable client pipelining for client operations in bypass mode Reset state : 0
0	DCP	Disable client pipelining Reset state : 0

0x074FFF00 VPE_SMMU_VPE_TLBIALL

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries.

VPE_SMMU_VPE_TLBIALL

Bits	Name	Description
31:0	EXEC	Writing any value to this register invalidates all TLB entries, as specified by the contents of SMMU_CR[TLBIALLCFG]

0x074FFF04 VPE_SMMU_VPE_TLBIVMID

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries matching the IVMID value. Precise function is governed by SMMU_CR[TLBIALLCFG].

VPE_SMMU_VPE_TLBIVMID

Bits	Name	Description
31:5	RESERVED	
4:0	IVMID	Designates VMID[4:0] value of entries to be invalidated.

14.22.1.4 SMMU configuration registers

0x074FFF80 VPE_SMMU_VPE_CR

Type: Read/Write
Clock: AXI_BUS_CLOCK

Global configuration register.

VPE_SMMU_VPE_CR

Bits	Name	Description
31:10	RESERVED_2	
9	RESERVED_1	Reset state : 0
8	TLBIVMIDCFG	TLBIVMID configuration control. When set to 0,flash-invalidate, SMMU_TLBIVMID commands flash-invalidate the entire TLB, without regard to locking ,security and VMID value. When set to 1, selective, SMMU_TLBIVMID invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and VMID field matching the VMID specified by SMMU_TLBIVMID command. Reset state : X
7	TLBIALLCFG	TLBIALL configuration control. When set to 0, flash-invalidate, SMMU_TLBIALL commands flash-invalidate the entire TLB, without regard to locking and/or security. When set to 1, selective, SMMU_TLBIALL invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and are unlocked. Reset state : X
6	TLBLKCRWE	TLBLKCR write enable. When set to 0, writes to SMMU_CBn_TLBLKCR are ignored. When set to 1, allows operating environments to manage the TLB locking mechanism directly. Management amounst multiple operating environments must be coordinated externally between themselves. Reset state : X
5	STALLD	Global disable for stall mode. When set to 1, context bank stall modes are ignored and operate as terminate mode. Reset state : X
4	CLIENTPD	Client port disable. When set, all client accesses are forced to bypass the system MMU. There is no translation. access control, or attribute generation. This bit overrides individual SMMU_M2VCBRn[BYPASSD] settings; client requests are bypassed, even if SMMU_M2VCBRn[BYPASSD] is set to 1. Bypass request errors are not recorded in SMMU_ESR, nor reported to requesting masters. The SMMU_rpuErrIrptReq interrupt output signal is not asserted. Reset state : 1

VPE_SMMU_VPE_CR (cont.)

Bits	Name	Description
3	DCDEE	When set to 0, configuration port decode errors do not set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn are not updated. When set to 1, configuration port decode errors set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn updated with address and syndrome of error. Reset state : X
2	RPUEIE	When set, configuration port errors and client port bypass errors are reported directly to the interrupt controller via the SMMU_rputErrIrptReq interrupt output signal. Interrupt output is asserted if SMMU_CR[RPUIE_EN] is 1 and ANY bit is set in SMMU_ESR register. Reset state : 0
1	RPUERE	When set, SMMU reports configuration port errors and client port bypass errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via AXI port will use decode error, rather than slave error. Regardless of the value of this field both configuration port errors and client port bypass request errors are terminated by the SMMU as RAZ/WI, and are recorded in SMMU_ESR register. Reset state : X
0	RPUE	When set, all configuration port accesses are checked against SMMUX_RPU_ACR and/or the SMMUX_CBACRn registers for access permissions. Reset state : 0

14.22.1.5 SMMU error report registers

0x074FFF84 VPE_SMMU_VPE_EAR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: unknown

When there is an error, holds the physical address of the errant transaction.

VPE_SMMU_VPE_EAR

Bits	Name	Description
31:0	PA	Physical address[31:0]

0x074FFF88 VPE_SMMU_VPE_ESR

Type: Read/Write to clear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This register has read/write clear access. Reads return the value in the register, a write with a 1 set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

VPE_SMMU_VPE_ESR

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x074FFF8C VPE_SMMU_VPE_ESRRESTORE

Type: Write
Clock: RPM_BUS_CLK
Reset State: Undefined

This register is an aliased address for SMMU_ESR, but it allows direct write access. In this way, diagnostic software can cause an error to be generated and reported.

VPE_SMMU_VPE_ESRRESTORE

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR, SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	

VPE_SMMU_VPE_ESRRESTORE (cont.)

Bits	Name	Description
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x074FFF90 VPE_SMMU_VPE_ESYNR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

VPE_SMMU_VPE_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request
15:0	AMID	AMID[15:0] field of errant request

0x074FFF94 VPE_SMMU_VPE_ESYNR1

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

VPE_SMMU_VPE_ESYNR1

Bits	Name	Description
31	DCD	(decode) Indicates configuration port error due to invalid/unrecognized address (e.g., a reserved register address) Includes decode errors within both the global address space and the individual context bank address space

VPE_SMMU_VPE_ESYNR1 (cont.)

Bits	Name	Description
30	AC	(access control) Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO field of the errant request
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request)
15:12	ALEN	ALEN[3:0] field of the errant request
11	RESERVED_2	
10	ABURST	ABURST[1:0] field of the errant request
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request
7	AINST	AINST field of the errant request
6	APROTNS	APROTNS field of the errant request
5	APRIV	APRIV field of the errant request
4	AINNERSHARED	AINNERSHARED field of the errant request
3	ASHARED	ASHARED field of the errant request
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

14.22.1.6 SMMU revision register

0x074FFFF4 VPE_SMMU_VPE_REV

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the revision information for the SMMU core and wrapper.

VPE_SMMU_VPE_REV

Bits	Name	Description
31:12	RESERVED	

VPE_SMMU_VPE_REV (cont.)

Bits	Name	Description
11:8	WRAPPER	Wrapper version
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

14.22.1.7 SMMU implementation parameter register

0x074FFFF8 VPE_SMMU_VPE_IDR

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the parameter information for the SMMU core and wrapper

VPE_SMMU_VPE_IDR

Bits	Name	Description
31:24	NIRPT	NIRPT[7:0] Indicates number of context fault interrupt outputs (minus 1) supported by the System MMU Value can range from 0 - 255 (1 - 256 context fault interrupt outputs)
23:16	NCB	NCB[7:0] Indicates number of context banks (minus 1) supported by the System MMU Value can range from 0 - 254 (1 - 255 context banks)
15:12	TLBSIZE	TLBSIZE[3:0] Indicates log2(number of TLB entries) That is, number of TLB entries = 2 ** TLBSIZE
11	RESERVED	
10	HUM	Indicates whether or not TLB hit-under-miss behavior is supported
9	HTW	Indicates whether or not the System MMU supports hardware table walk If hardware table walk not supported (HTW=0), then software cannot set SMMU_CBn_ACTLR[TLBMCFG] to 0b10
8:0	NM2VCBMT	NM2VCBMT[8:0] Indicates number of M2VCBMT entries, with a maximum of 512 The bit width of the M2VCBMTIindex input (maximum value is 9) is equal to log base 2 of NM2VCBMT Allows for up to 7-bit MID field, plus NS-prot or other fields to select mapping [

0x074FFFFC VPE_SMMU_VPE_RPU_ACR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Using the incoming HVMID, this register controls access to the global register space.

VPE_SMMU_VPE_RPU_ACR

Bits	Name	Description
31:0	RWE	Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the entire block of registers within the SMMU's 4KB global address space, including this register itself. A VMID identified by this register is also permitted global access to all context banks. In practice, this register designates the VMID(s) that can act as SROT.

14.22.2 SMMU Context Bank Registers

There are a configurable number (1 to 9) of context banks in the SMMU. Each context bank consists of a set of registers in a unique 4KB address space.

14.22.2.1 SMMU context bank control registers

0x07400000+0x1000*n VPE_SMMU_VPE_CBn_SCTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank System Control Register controls various architected SMMU features

VPE_SMMU_VPE_CBn_SCTLR

Bits	Name	Description
31:5	RESERVED_2	
4	BE	Governs the order byte order or "endianness" of the page table entries. When set to 0, page table entries are in little endian format, so that their least significant byte is in byte 0 of the 32 bit entry. When set to 1, page table entries are in big endian format, so that their most significant byte is in byte 0 of the 32 bit entry.
3	RESERVED_1	Reserved for HAF, Hardware access flag. This bit governs whether the access flag is managed by hardware or software. The SMMU supports software access flag management only, so this bit is read-only and internally driven to 0.

VPE_SMMU_VPE_CBn_SCTLR (cont.)

Bits	Name	Description
2	AFE	Access flag enable. When AFE = 0, the access flag field is not supported and the AP[0] page table entry field acts as a bit of the overall AP[2:0] field to determining access permissions. When AFE = 1, the AP[0] page table entry field becomes the access flag, and the reduced number of access permission combinations is specified by AP2:1], and SMMU hardware will signal an Access Flag fault if a request targets a page for which the access flag is 0.
1	TRE	TEX remap enable. This bit governs the mapping of the page table entry TEX[2:0],C,B and SH fields into an SMMU TLB entry, and thus the translation of the AMEMTYPE[2:0], ASHARED and AINNERSHARED bus attributes. When TRE = 0, the TLB value is determined directly from the page table entry fields.
0	M	MMU enable bit. When set to 1, this context bank is enabled for translating requests. When set to 0, accesses bypass the TLB, and there is no address translation, access permission checking or attribute mapping. Incoming master requests are passed through unchanged.

0x07400004+ 0x1000*n VPE_SMMU_VPE_CBn_ACTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank auxiliary control register controls various implementation specific features.

VPE_SMMU_VPE_CBn_ACTLR

Bits	Name	Description
31:19	RESERVED	
18	RESERVED_2	
17:16	V2PCFG	VA-to-PA configuration. Governs operation of VA-to-PA commands that miss in the TLB 0x0: terminate (Record TLB Miss context fault in SMMU_CBn_PAR) 0x1: software table update (Translate based on values in SMMU_CBn_TLBFLPTER and SMMU_CBn_TLBSLPTER) 0x2: hardware table walk (Translate based on value of PTE read from page table in memory) 0x3: reserved

VPE_SMMU_VPE_CBn_ACTLR (cont.)

Bits	Name	Description
15	TIPCF	Governs whether or not all subsequent requests using this context bank should be terminated if a prior context fault has occurred and has not yet been cleared from SMMU_CBn_FSR Accesses to other context banks proceed as normal 0x0: do not terminate (System MMU will attempt to process subsequent requests despite the presence of an existing context fault in SMMU_CBn_FSR. SMMU_CBn_FSR will be set if the subsequent access also encounters a context fault) 0x1: terminate (All subsequent accesses terminated by the System MMU as RAZ/WI, even if SMMU_CBn_ACTLR[TLBMCFG, CFCFG] configured for stall mode. SMMU_CBn_FSR set when access is terminated due to TIPCF = 1. Presence of SMMU_CBn_FSR when SMMU_CBn_ACTLR is 1 implies that the later exceptions must have been simply the forced terminations due to the prior context fault. Error optionally reported to the requesting master, according to the client port bus protocol, f SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus if SMMU_CBn_ACTLR is 1.)
14	CFCFG	(context fault configuration) Governs the behavior of all context faults except TLB miss TLB miss context faults are governed by SMMU_CBn_ACTLR[TLBMCFG] 0x0: terminate (Access terminates at the System MMU as RAZ/WI. Context fault exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x1: stall (Requesting master's access stalled while System MMU waits for managing processor to resolve context fault. Context fault exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode)

VPE_SMMU_VPE_CBn_ACTLR (cont.)

Bits	Name	Description
13:12	TLBMCFG	(TLB miss configuration) Governs the behavior of client accesses that miss in the TLB 0x0: pass-through (Access passed through to targeted slave without translation, attribute control, or access permission checking. Effectively, behavior is as if SMMU_CBn_SCTLR = 0 i.e., MMU disabled for this context bank. TLB miss not considered a context fault. TLB miss exception not recorded in SMMU_CBn_FSR. TLB miss exception not reported to requesting master. SMMU_contextFaultIrptReq interrupt output not asserted) 0x1: terminate (Access terminates at the System MMU as RAZ/WI,TLB miss exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x2: stall (Requesting master's access stalled while System MMU waits for managing processor to update TLB. TLB miss exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode) 0x3: HTW (Hardware table walk . Requesting master's access stalled while System MMU accesses page table. The is TLB updated and requesting master's access resumed after obtaining valid entry from page table. If translation fault, then access either terminates or stalls according to setting of SMMU_CBn_ACTLR)
11	DNLV2PA	(disable non-locking VA-to-PA allocation) Governs whether or not TLB misses due to non-locking VA-to-PA commands will allocate a new entry This field is ignored for locking VA-to-PA operations (SMMU_CBn_TLBLKCR[LKE] = 1)
10	DNA	(disable normal allocation) Governs whether or not TLB misses due to client port accesses will allocate a new entry
9:8	PRIVCFG	0x0: apriv (System MMU uses APRIV signal supplied by master as user/supervisor indicator 1 = supervisor) 0x1: reserved 0x2: User (System MMU ignores APRIV; treats all requests using this context bank as user) 0x3: Supervisor (System MMU ignores APRIV; treats all requests using this context bank as supervisor)

VPE_SMMU_VPE_CBn_ACTLR (cont.)

Bits	Name	Description
7:5	RESERVED_1	
4	RCNSH	(redirect cacheable-non-shareable) Governs whether or not cacheable accesses that are non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache, even though the locations are not being coherently shared with Scorpion-MP
3	RCISH	(redirect cacheable-inner-shareable) Governs whether or not cacheable accesses that are inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
2	RCOSH	(redirect cacheable-outer-shareable) Governs whether or not cacheable accesses that are outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
1	CFEIE	(context fault error interrupt enable) Governs whether or not client port request context faults are reported directly to the interrupt controller via the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus Interrupt output is asserted if SMMU_CBn_ACTLR[CFEIE] is 1 and any context fault bits are set in SMMU_CBn_FSR Such interrupts would generally be directed to the interrupt controller of whichever processor is currently managing this context bank of the System MMU Reset state : 0
0	CFERE	(context fault error report enable) Governs whether or not client port request context faults that are configured for terminate mode (or that are explicitly terminated after stall mode) are reported to the requesting master, according to the client port bus protocol All error types reported via AXI port will use decode error rather than slave error All context faults are recorded in SMMU_CBn_FSR, regardless of the value of this field.

0x07400008+ 0x1000*n VPE_SMMU_VPE_CBn_CONTEXTIDR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context ID register holds the ASID associated with this context bank

VPE_SMMU_VPE_CBn_CONTEXTIDR

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Specifies the 8 bit ASID value assigned to this context bank. The ASID can be included in the key comparison of TLB entries. .

0x07400010+ 0x1000*n VPE_SMMU_VPE_CBn_TTBR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR0 is used for low order virtual addresses, typically private pages for a given process.

VPE_SMMU_VPE_CBn_TTBR0

Bits	Name	Description
31:7	PA	BIts 31:7 of the physical address of the base of the page table. The actual LSB of the base address is bit 14-N, where N is set in register TTCR
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07400014+ 0x1000*n VPE_SMMU_VPE_CBn_TTBR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR1 is used for high order virtual addresses, typically global pages for a given VMID, or kernal mappings.

The context bank auxiliary control register controls various implementation specific features.

VPE_SMMU_VPE_CBn_TTBR1

Bits	Name	Description
31:14	PA	BIts 31:14 of the physical address of the base of the page table.
13:7	RESERVED_2	
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED_1	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07400018+ 0x1000*n VPE_SMMU_VPE_CBn_TTBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table control register, which specifies the size of the virtual address space that uses TTBR0.

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VPE_SMMU_VPE_CBn_TTBCR

Bits	Name	Description
31:6	RESERVED_2	
5	PD1	Page disable 1; if this bit is set, hardware table walks attempting to use TTBR1will result in a first level descriptor translation fault. If clear, TTBR1 contents are used.
4	PD0	Page disable 0; if this bit is set, hardware table walks attempting to use TTBR0 will result in a first level descriptor translation fault. If clear, TTBR0 contents are used.
3	RESERVED_1	
2:0	N	N[2:0] specifies the number of upper order virtual address bits which must be 0 in order for translations to use the table pointed to by TTBR0. If any of these bits are non-zero, TTBR1 is used for the lookup. If N is 0, only TTBR0 is used.

0x0740001C+ 0x1000*n VPE_SMMU_VPE_CBn_PAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The physical address register captures the physical address value resulting from the execution of a VA-to-PA command

Field definitions vary according to whether or not there is a context fault associated with the requested translation

VPE_SMMU_VPE_CBn_PAR

Bits	Name	Description
31:12	PAR_FAULT_INFO_312	
11	RESERVED_2	
10:9	PAR_FAULT_INFO_72	
8	RESERVED_1	
7:1	PAR_FAULT_INFO_71	Encoding varies according to value in FAULT field.
0	FAULT	(fault status) This field will be 1 when a context fault is associated with the requested translation, and 0, when there is no context fault associated with the requested translation.

0x07400020+0x1000*n VPE_SMMU_VPE_CBn_FSR, n=[0..1]

Type: Read/WriteClear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The Fault Status Register records status information for client accesses that encounter exceptions within the context bank, e.g. translation faults.This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data

This prevents inadvertent clearing of new faults when writing the register to clear an old fault

The presence of an asserted value on any bit in this register (except the SS bit) is what prompts the assertion (when enabled by SMMU_CBn_ACTLR[CFEIE]) of the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus

Therefore, these bits must be cleared by the interrupt handler

This is contrasted with the fields in the SMMU_CBn_FSYNRn registers, which are merely the "syndrome" of the fault indicated by SMMU_CBn_FSR

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VPE_SMMU_VPE_CBn_FSR

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	

VPE_SMMU_VPE_CBn_FSR (cont.)

Bits	Name	Description
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07400024+ 0x1000*n VPE_SMMU_VPE_CBn_FSRRESTORE, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Allows SW to force a value into the SMMU_CBn_FSR register.

VPE_SMMU_VPE_CBn_FSRRESTORE

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)

VPE_SMMU_VPE_CBn_FSRRESTORE (cont.)

Bits	Name	Description
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07400028+ 0x1000*n VPE_SMMU_VPE_CBn_FAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The Fault Address Register records the virtual address of client accesses that encounter exceptions within the context bank, e.g. translation faults. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

VPE_SMMU_VPE_CBn_FAR

Bits	Name	Description
31:0	VA	VA[31:0] of errant client access

0x0740002C+ 0x1000*n VPE_SMMU_VPE_CBn_FSYNR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

NOTE omission of VMID field from this register, as VMID can only be made visible to SROT, and not to general OS software that manages the context bank registers

VPE_SMMU_VPE_CBn_FSYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] (ATID field of errant request)

VPE_SMMU_VPE_CBn_FSYNR0 (cont.)

Bits	Name	Description
23:16	RESERVED	
15:13	ABID	ABID[2:0] (ABID field of errant request)
12:8	APID	APID[4:0] (APID field of errant request)
7:0	AMID	AMID[7:0] (AMID field of errant request)

0x07400030+ 0x1000*n VPE_SMMU_VPE_CBn_FSYNR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

VPE_SMMU_VPE_CBn_FSYNR1

Bits	Name	Description
31:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO (AOOO field of the errant request)
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request
15:12	ALEN	ALEN[3:0]field of the errant request
11	RESERVED_2	
10	ABURST	field of the errant request
9	RESERVED_1	
8	AWRITE	field of the errant request
7	AINST	field of the errant request
6	APROTNS	field of the errant request
5	APRIV	field of the errant request
4	AINNERSHARED	(AINNERSHARED field of the errant request)
3	ASHARED	(ASHARED field of the errant request)

VPE_SMMU_VPE_CBn_FSYNR1 (cont.)

Bits	Name	Description
2:0	AMEMTYPE	AMEMTYPE[2:0] (AMEMTYPE field of the errant request)

0x07400034+ 0x1000*n VPE_SMMU_VPE_CBn_PRRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs memory type and shareability attributes of requests that are both MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1)

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) and/or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, memory type encoding is as follows:

0b00 = strongly-ordered

0b01 = device

0b10 = normal

0b11 = reserved

VPE_SMMU_VPE_CBn_PRRR

Bits	Name	Description
31	NOS7	not-outer-shareable class 7
30	NOS6	not-outer-shareable class 6
29	NOS5	not-outer-shareable class 5
28	NOS4	not-outer-shareable class 4
27	NOS3	not-outer-shareable class 3
26	NOS2	not-outer-shareable class 2
25	NOS1	not-outer-shareable class 1
24	NOS0	not-outer-shareable class 0
23:20	RESERVED	

VPE_SMMU_VPE_CBn_PRRR (cont.)

Bits	Name	Description
19	SHNMSH1	(shareable attribute for normal memory accesses with SH=1) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1
18	SHNMSH0	(shareable attribute for normal memory accesses with SH=0) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0
17	SHDSH1	SHDSH1 (shareable attribute for device accesses with SH=1) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1 [
16	SHDSH0	SHDSH0 (shareable attribute for device accesses with SH=0) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0 [
15:14	MTC7	MTC7[1:0] (memory type class 0)
13:12	MTC6	MTC6[1:0] (memory type class 0)
11:10	MTC5	MTC5[1:0] (memory type class 0)
9:8	MTC4	MTC4[1:0] (memory type class 0)
7:6	MTC3	MTC3[1:0] (memory type class 0)
5:4	MTC2	MTC2[1:0] (memory type class 0)
3:2	MTC1	MTC1[1:0] (memory type class 0)
1:0	MTC0	MTC0[1:0] (memory type class 0)

0x07400038+ 0x1000*n VPE_SMMU_VPE_CBn_NMRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs the cache policy of MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1) requests for which the memory type is mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0) or the memory type is mapped to a type other than normal memory (SMMU_CBn_PRRR[MTCn] != 0b10)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, inner-cache and outer-cache policy encodings are as follows:

0b00 = non-cacheable

0b01 = cacheable, copy-back, write-allocate

0b10 = cacheable, write-through, write-no-allocate

0b11 = cacheable, copy-back, write-no-allocate

VPE_SMMU_VPE_CBn_NMRR

Bits	Name	Description
31:30	OCPC7	OCPC7[1:0] (inner-cache policy class 7)
29:28	OCPC6	OCPC6[1:0] (inner-cache policy class 6)
27:26	OCPC5	OCPC5[1:0] (inner-cache policy class 5)
25:24	OCPC4	OCPC4[1:0] (inner-cache policy class 4)
23:22	OCPC3	OCPC3[1:0] (inner-cache policy class 3)
21:20	OCPC2	OCPC2[1:0] (inner-cache policy class 2)
19:18	OCPC1	OCPC1[1:0] (inner-cache policy class 1)
17:16	OCPC0	OCPC0[1:0] (inner-cache policy class 0)
15:14	ICPC7	ICPC7[1:0] (inner-cache policy class 7)
13:12	ICPC6	ICPC6[1:0] (inner-cache policy class 6)
11:10	ICPC5	ICPC5[1:0] (inner-cache policy class 5)
9:8	ICPC4	ICPC4[1:0] (inner-cache policy class 4)
7:6	ICPC3	ICPC3[1:0] (inner-cache policy class 3)
5:4	ICPC2	ICPC2[1:0] (inner-cache policy class 2)
3:2	ICPC1	ICPC1[1:0] (inner-cache policy class 1)
1:0	ICPC0	ICPC0[1:0] (inner-cache policy class 0)

0x0740003C+0x1000*n VPE_SMMU_VPE_CBn_TLBLKCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB lock control register governs the TLB locking mechanism and TLB invalidate operations.Write access to this register is governed by SMMU_CR[TLBLKCRWE]

When SMMU_CR[TLBLKCRWE] is 0, writes to SMMU_CBn_TLBLKCR are ignored

Read access is still permitted

SROT can set SMMU_CR[TLBLKCRWE] to 1 to allow operating environment(s) to manage the TLB locking mechanism

Management amongst multiple operating environments must be coordinated via semaphore

VPE_SMMU_VPE_CBn_TLBLKCR

Bits	Name	Description
31:24	RESERVED_2	
23:16	VICTIM	VICTIM[7:0] Indicates the TLB index at which the next normal (non-locking) allocation will occur Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context
15:8	FLOOR	FLOOR[7:0] Indicates the TLB index from which round-robin replacement on normal (non-locking) allocations occurs TLB entries at indices below this value are locked Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context banks
7:4	RESERVED_1	
3	TLBIVAACFG	(TLBIVAA configuration) TLBIVAACFG = 0 - flash-invalidate SMMU_CBn_TLBIVAA commands flash-invalidate the entire TLB, without regard to locking, security, address, and/or VMID value TLBIVAACFG = 1 - selective SMMU_CBn_TLBIVAA commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank VA field of TLB entry matches VA designated by SMMU_CBn_TLBIVAA command NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked

VPE_SMMU_VPE_CBn_TLBLKCR (cont.)

Bits	Name	Description
2	TLBIASIDCFG	(TLBIASID configuration) TLBIASIDCFG = 0 - flash-invalidate SMMU_CBn_TLBIASID commands flash-invalidate the entire TLB, without regard to locking, security, VMID, and/or ASID values TLBIASIDCFG = 1 - selective SMMU_CBn_TLBIASID commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command TLB entry is not global (NG field is 1) NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
1	TLBIALLCFG	(TLBIALL configuration) TLBIALLCFG = 0 - flash-invalidate SMMU_CBn_TLBIALL commands flash-invalidate the entire TLB, without regard to locking, security, and/or VMID value TLBIALLCFG = 1 - selective SMMU_CBn_TLBIALL commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked
0	LKE	(lock enable) Governs whether or not TLB entries established by VA-to-PA commands upon TLB misses are locked LKE = 0 (normal, non-locking) Allocate VA-to-PA TLB entry (if TLB miss) at the index specified by SMMU_CBn_TLBLKCR[VICTIM] Allocation is disabled if SMMU_CBn_ACTLR[DNLV2PA] is 1 Increment SMMU_CBn_TLBLKCR[VICTIM] by 1 (only if new entry allocated) Wrap back to the value of SMMU_CBn_TLBLKCR[FLOOR] when the last entry is written LKE = 1 (locking) Search TLB for specified VA and invalidate if found Provides atomicity between the invalidate and the new allocation within the locked region Allocate VA-to-PA TLB entry at the index specified by data operand bits 7:0 of the VA-to-PA command This value must be less than SMMU_CBn_TLBLKCR[FLOOR] in order for it to remain locked Allocation occurs even if non-locking allocation is disabled due to SMMU_CBn_ACTLR[DNLV2PA] = 1

0x07400040+ 0x1000*n VPE_SMMU_VPE_CBn_V2PSR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The VA-to-PA status register records the hit/miss status and TLB index or V2Pxx and TLB invalidate commands.

VPE_SMMU_VPE_CBn_V2PSR

Bits	Name	Description
31:16	RESERVED_2	
15:8	INDEX	INDEX[7:0] Indicates the index of the TLB entry associated with the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command If SMMU_CBn_V2PSR[HIT] is 0, then SMMU_CBn_V2PSR[INDEX] is the index to which the entry was allocated (if allocated at all) If SMMU_CBn_V2PSR[HIT] is 1, then SMMU_CBn_V2PSR[INDEX] is the index of the entry which hit
7:1	RESERVED_1	
0	HIT	Indicates whether or not there was a TLB hit (prior to allocation, if any) on the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command

0x07400044+ 0x1000*n VPE_SMMU_VPE_CBn_TLBFLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB first level PTE register holds the first level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

This register (together with SMMU_CBn_TLBSLPTER) is used as the source of the translation information for VA-to-PA operations when the MMU is enabled (SMMU_CBn_SCTLR[M] = 1) and the operations are configured for software table update (SMMU_CBn_ACTLR[V2PCFG] = 0b01)

Field definitions vary according to the type of PTE (fault, page, section, or supersection), and come directly from the ARMv7 architecture's PTE formats

VPE_SMMU_VPE_CBn_TLBFLPTER

Bits	Name	Description
31:10	FL_PTE_HI	

VPE_SMMU_VPE_CBn_TLBFLPTER (cont.)

Bits	Name	Description
9:5	RESERVED	
4:2	FL_PTE_LO	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	This field should be set to 0b00 or 0b11 to indicate that the translation should result in a context fault, and the rest of the fields are defined as indicated in this section If this field is not 0b00 or 0b11, then the PTE is of some other type (see other sections for the field definitions for those types)

0x07400048+ 0x1000*n VPE_SMMU_VPE_CBn_TLBSLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB second level PTE register holds the second level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

Field definitions vary according to the type of PTE (fault, 64KB or 4KB), and come directly from the ARMv7 architecture's PTE format

VPE_SMMU_VPE_CBn_TLBSLPTER

Bits	Name	Description
31:2	SL_PTE	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	0x0: fault

0x0740004C+ 0x1000*n VPE_SMMU_VPE_CBn_BFBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The burst fetch buffer configuration register governs the operation of the "burst fill" feature of the SMMU.

VPE_SMMU_VPE_CBn_BFBCR

Bits	Name	Description
31:12	STRIDE	(stride amount) 4KB-aligned value to be added to virtual address on demand TLB miss for filling subsequent BFB Stride of minimum 4KB alignment useful for preventing stride burst fetch until final PTE of the demand BFB entry is used
11:8	SLVIC	(second-level victim) Indicates the SLBFB index at which the next round-robin allocation will occur
7:4	FLVIC	(first-level victim) Indicates the FLBFB index at which the next round-robin allocation will occur
3	RESERVED	
2	SFVS	(stride-fetch victim selection) SFVS. = 0 (replace normal round-robin victim-selected entry) Useful when stride is larger than the VA space represented by the four PTEs in the demand BFB entry, but the client access pattern is for more than just the initial PTE in that demand BFB entry SFVS. = 1 (replace same BFB used by demand VA for which the stride burst is being performed) Useful when stride is the same as the VA space represented by an individual PTE in the demand BFB entry (such that the stride won't miss against the BFB until the last PTE of the demand BFB entry is accessed), and/or when the client access pattern only uses the initial PTE in the demand BFB entry
1	BFBSFE	(burst fetch buffer stride fetch enable) Enables stride burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Stride burst fetch is for the block of four PTEs associated with VA+stride VA is the "demanded" VA from the client (or VA-to-PA command) Stride value is specified by SMMU_CBn_BFBCR[STRIDE] Stride burst fetch only occurs if demand access for VA misses in TLB (could hit in BFB) and address VA+stride misses in both TLB and BFB
0	BFBDFE	(burst fetch buffer demand fetch enable) Enables demand burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Demand burst fetch is for the block of four PTEs associated with the "demanded" VA from the client (or VA-to-PA command) Demand burst fetch only occurs if demand access misses in both TLB and BFB

0x07400800+ 0x1000*n VPE_SMMU_VPE_CBn_TLBIALL, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate all command register invalidates all TLB entries matching the VMID associated with this context bank. Data operand is ignored.

VPE_SMMU_VPE_CBn_TLBIALL

Bits	Name	Description
31:0	RESERVED	

0x07400804+ 0x1000*n VPE_SMMU_VPE_CBn_TLBIASID, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by ASID command register invalidates TLB entries matching the specified ASID and matching the VMID associated with this context bank.Invalidates TLB entries which are associated with the designated ASID and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIASIDCFG] governs whether command flash-invalidates entire TLB array or just the entries matching the VMID, ASID, and security state

TLBIASIDCFG = 0 - flash-invalidate

SMMU_CBn_TLBIASID command flash-invalidates the entire TLB, without regard to locking, security, VMID, and/or ASID values

TLBIASIDCFG = 1 - selective

SMMU_CBn_TLBIASID command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command data operand

TLB entry is not global (NG field is 1)

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command

Locking is not considered (matching entries are invalidated even if locked)

ASID field of command specifies the ASID value of the TLB entries to be invalidated

VPE_SMMU_VPE_CBn_TLBIASID

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Actual ASID value

0x07400808+ 0x1000*n VPE_SMMU_VPE_CBn_TLBIVA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA command invalidates TLB entries matching the designated VA, ASID and the VMID associated with this context bank.

Matching entry determined as follows:

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIVA command data operand (or TLB entry is global - NG field is 0)

VA field of TLB entry matches VA value designated by the SMMU_CBn_TLBIVA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIVA command

Locking is not considered (matching entry is invalidated even if locked)

Data operand specifies the VA and ASID value of the TLB entry to be invalidated

VPE_SMMU_VPE_CBn_TLBIVA

Bits	Name	Description
31:12	VA	VA[31:12]
11:8	RESERVED	
7:0	ASID	ASID[7:0] value

0x0740080C+ 0x1000*n VPE_SMMU_VPE_CBn_TLBIVAA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA all ASIDS command invalidates TLB entries matching the designated VA and the VMID associated with this context bank, regardless of ASID.Invalidates TLB entries which are associated with the designated VA, regardless of ASID, and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIVAACFG] governs whether command flash-invalidates entire TLB array or just the non-locked entries matching the VMID, ASID, and security state

TLBIVAACFG = 0 - flash-invalidate

SMMU_CBn_TLBIVAA command flash-invalidates the entire TLB, without regard to locking, security, address, and/or VMID value

TLBIVAACFG = 1 - selective

SMMU_CBn_TLBIVAA command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

VA field of TLB entry matches VA designated by the SMMU_CBn_TLBIVAA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command

Entry is unlocked

VPE_SMMU_VPE_CBn_TLBIVAA

Bits	Name	Description
31:12	VA	VA[31:12]
11:0	RESERVED	

0x07400810+ 0x1000*n VPE_SMMU_VPE_CBn_V2PRR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

VPE_SMMU_VPE_CBn_V2PRR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07400814+0x1000*n VPE_SMMU_VPE_CBn_V2PPW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

VPE_SMMU_VPE_CBn_V2PPW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07400818+ 0x1000*n VPE_SMMU_VPE_CBn_V2PUR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

VPE_SMMU_VPE_CBn_V2PUR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x0740081C+ 0x1000*n VPE_SMMU_VPE_CBn_V2PUW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

.Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

VPE_SMMU_VPE_CBn_V2PUW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	

VPE_SMMU_VPE_CBn_V2PUW (cont.)

Bits	Name	Description
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07400820+ 0x1000*n VPE_SMMU_VPE_CBn_RESUME, n=[0..1]

Type: Write/command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB resume command causes the SMMU to resume operation after a stalled access..

VPE_SMMU_VPE_CBn_RESUME

Bits	Name	Description
31:1	RESERVED	
0	TNR	Terminate/not retry When TNR is written as 0, indicates that the stalled access should be retried by the system MMU. When written as 1, indicates that this stalled transaction is terminated by the system MMU. The error is optionally reported to the requesting master, using the client port bus protocol, if SMMU_CNn_ACTLR[CFERE] == 1. Interrupt optionally remains asserted via SMMU_M2VCBRn[IRPTINDX] selected SMMU_contextFaultIrptReq bit, only if SMMU_CBn_ACTLR[CFEIE] is 1, and only if SMMU_CBn_FSR has not been cleared by software priori to issuing this command..

14.23 MDP4 0 SMMU Registers (0x07500000 SMMU_MDP4_0_BASE)

This section contains the MDP4 0 SMMU registers.

14.23.1 SMMU Global Registers

14.23.1.1 SMMU VMID/CBNDX mapping registers

0x075FF000+ 0x4*n MDP4_0_SMMU_MDP0_M2VCBRn, n=[0..15]

Type: Read/Write
Clock: AXI_CLK
Reset State: Undefined

SMMU_M2VCBRm registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

MDP4_0_SMMU_MDP0_M2VCBRn

Bits	Name	Description
31:28	RESERVED_2	
27:25	BPMEMTYPE	(bypass memory type) Supplies the AMEMTYPE attributes for client requests which bypass the System MMU when SMMU_M2VCBRn[BPMTCFG] = 1 See reference section for AMEMTYPE encoding definitions
24	BPMTCFG	(bypass memory type configuration) Governs the memory type (AMEMTYPE) attributes of client requests which bypass the System MMU BPMTCFG = 0 - use AMEMTYPE Bypass requests use AMEMTYPE signal supplied by client master BPMTCFG = 1 - use SMMU_M2VCBRn[BPMEMTYPE] Bypass requests use SMMU_M2VCBRn[BPMEMTYPE] Reset state : 0
23:22	NSCFG	(non-secure configuration) Governs the incoming security designation of client requests NSCFG = 0b00 - use APROTNS Use APROTNS signal supplied by client master NSCFG = 0b01 - reserved NSCFG = 0b10 - secure System MMU ignores APROTNS; treats all requests as secure NSCFG = 0b11 - non-secure System MMU ignores APROTNS; treats all requests as non-secure Reset state : 0

MDP4_0_SMMU_MDP0_M2VCBRn (cont.)

Bits	Name	Description
21:20	BPSHCFG	(bypass shareability configuration) Governs the shareability realm (ASHARED and AINNERSHARED) attributes of client requests which bypass the System MMU BPSHCFG = 0b00 - use ASHARED and AINNERSHARED Bypass requests use ASHARED and AINNERSHARED signals supplied by client master BPSHCFG = 0b01 - outer-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 0 BPSHCFG = 0b10 - inner-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 1 BPSHCFG = 0b11 - non-shareable Bypass requests set ASHARED = 0, AINNERSHARED = 0 Reset state : 0
19	BPRCNSH	(bypass redirect cacheable-non-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache Reset state : 0
18	BPRCISH	(bypass redirect cacheable-inner-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0
17	BPRCOSH	(bypass redirect cacheable-outer-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0

MDP4_0_SMMU_MDP0_M2VCBRn (cont.)

Bits	Name	Description
16	BYPASSD	Bypass disable for this index Governs whether or not client port accesses using this mapping table entry are actually permitted to "bypass" the System MMU when such bypass is indicated (either due to CBNDX = 255 or due to the master asserting the "SMMU bypass" input) This field is ignored (and operates as if it were 0) if SMMU_CR[CLIENTPD] is 1 BYPASSD = 0 - bypass enabled Bypass requests truly bypass the System MMU and "pass-through" to the fabric (no translation, access control, or attribute generation) No cycle of latency for System MMU context bank access Bypass request not considered an error Bypass request error not recorded in SMMU_ESR[BYPASS] Bypass error not reported to requesting master SMMU_rpuErrIrptReq interrupt output not asserted Client accesses still reference M2VCBMT to get VMID value for presentation to fabric BYPASSD = 1 - bypass disabled System MMU terminates the access as RAZ/WI Bypass request is considered an error Bypass request error is recorded in SMMU_ESR[BYPASS] If SMMU_CR[RPUERE] is 1, then bypass error reported to requesting master according to the client port bus protocol If SMMU_CR[RPUEIE] is 1, then SMMU_rpuErrIrptReq interrupt output asserted
15:8	CBNDX	Context bank index Context bank index associated with the M2VCBMT index CBNDX = 255 indicates no context bank assigned ("bypass")
7:5	RESERVED_1	
4:0	VMID	Virtual machine ID VMID value associated with the M2VCBMT index Must be programmed consistently with the SMMU_CBACRn[CBVMID] field for the context bank designated by SMMU_M2VCBRm[CBNDX]

14.23.1.2 SMMU context bank access control registers

0x075FF800+ 0x4*n MDP4_0_SMMU_MDP0_CBACRn, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs configuration port access to the associated context bank registers.

MDP4_0_SMMU_MDP0_CBACRn

Bits	Name	Description
31:24	IRPTNDX	(interrupt index) Interrupt output number used for context faults associated with this context bank (use SMMU_contextFaultIrptReq[IRPTNDX])
23:21	RESERVED	
20:16	CBVMID	(context bank VMID) Specifies the VMID with which the client masters using the context bank are associated Must be programmed consistently with the M2VCBMT entries that are configured to use the associated context bank This field is used by configuration port commands that need the context bank's VMID value in order to access the TLB (e.g., SMMU_CBn_TLBIVMID, SMMU_CBn_V2Pxx)
15:10	RESERVED_2	
9	RWGE	Read/write global enable. Setting this bit allows access to the context bank registers from any VMID
8	RWE	Read/write enable. Indicates that the RWVMID field is valid.
7:5	RESERVED_1	
4:0	RWVMID	Specifies owner VMID with full read/write access to the registers in the associated context bank "n".

14.23.1.3 SMMU TLB software access registers

0x075FFE00 MDP4_0_SMMU_MDP0_TLBRSW

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Writing to this address requests that the TLB entry at INDEX be read into the SMMU_TLBTRn registers

MDP4_0_SMMU_MDP0_TLBRSW

Bits	Name	Description
31:10	RESERVED	
9:8	TLBBFBS	This field selects the TLB, TFBFB, SLBFB 0x0: Selecting TLB 0x1: Not defined 0x2: Selecting FL BFB 0x3: Selecting SL BFB

MDP4_0_SMMU_MDP0_TLBRSW (cont.)

Bits	Name	Description
7:0	INDEX	TLB index to be read.

0x075FFE80 MDP4_0_SMMU_MDP0_TLBTR0

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

This register holds part of TLB entry read by the last TLBRSW command.

MDP4_0_SMMU_MDP0_TLBTR0

Bits	Name	Description
31:23	RESERVED_4	
22:20	DPSIZC	3 bit decode page size field from CAM-side of TLB CAM-RAM) Same determination and encoding as for DPSIZR The CAM-side copy of this field is used for hit/miss determination in the TLB CAM array
19	RESERVED_3	
18:16	DPSIZR	(3 bit decode page size field from RAM-side of TLB CAM-RAM) Determined from the size fields of the page table entry Encodes the page size as follows: all other values reserved/unused The RAM-side copy of this field is used for virtual ’ physical address formation 0x0: 4KB page 0x1: 64KB page 0x3: 1MB page 0x7: 16MB page
15:12	RESERVED_2	
11	MT2	(memory type bit 2) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[2] attribute bus on the request output of the System MMU

MDP4_0_SMMU_MDP0_TLBTR0 (cont.)

Bits	Name	Description
10	MT1	(memory type bit 1) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[1] attribute bus on the request output of the System MMU
9	MT0	(memory type bit 0) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[0] attribute bus on the request output of the System MMU
8	SH	(shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's outer-shareable realm This field becomes the ASHARED attribute on the request output of the System MMU
7	ISH	(inner-shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's inner-shareable realm This field becomes the AINNERSHARED attribute on the request output of the System MMU
6	NSDESC	(non-secure descriptor) This TLB entry field is a modified version of the corresponding bit of the page table entry Qualified by the NS-prot attribute of the incoming request which prompted the allocation of the TLB entry, such that if the incoming NS-prot attribute was 1 (non-secure), then the NS-desc field of the page table entry was ignored, and the NS-desc field of the TLB entry was forced to 1 Indicates whether the associated memory page contains secure (NS-desc=0) or non-secure (NS-desc=1) information This field becomes the NS-prot attribute on the request output of the System MMU
5	RESERVED_1	

MDP4_0_SMMU_MDP0_TLBTR0 (cont.)

Bits	Name	Description
4	XN	(execute never permission) This TLB entry field comes directly from the corresponding bit of the page table entry
3	UW	(user write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
2	UR	(user read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
1	PW	(privileged write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
0	PR	(privileged read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]

0x075FFE84 MDP4_0_SMMU_MDP0_TLBTR1

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

MDP4_0_SMMU_MDP0_TLBTR1

Bits	Name	Description
31:12	PA	Physical address [31:12] field of the TLB entry
11:5	RESERVED	
4:0	VMID	VMID [4:0]field of the TLB entry)

0x075FFE88 MDP4_0_SMMU_MDP0_TLBTR2

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

MDP4_0_SMMU_MDP0_TLBTR2

Bits	Name	Description
31:12	VA	virtual address field [31:12] of the TLB entry
11	RESERVED	
10	NG	(not global field from page table entry) Indicates whether the page is private to the specified ASID (NG=1) or global to all ASIDs within the VMID using this context bank (NG=0)
9	NSTID	(non-secure tag ID field of the TLB entry) Indicates whether the TLB entry belongs to the secure world (NSTID=0) or the non-secure world (NSTID=1) This field is comned against the incoming NS-prot attribute of the master request as part of TLB hit/miss determination
8	V	valid field of the TLB entry
7:0	ASID	ASID[7:0] field of the TLB entry

0x075FFE8C MDP4_0_SMMU_MDP0_TESTBUSCR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

Governs which signals (if any) from the system SMMU core or wrapper design hierarchy are sent out to the system via a testbus for diagnostic, and also to the system profiling and diagnostic monitor(SPDM).

MDP4_0_SMMU_MDP0_TESTBUSCR

Bits	Name	Description
31:28	SPDM3SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[3]
27:24	SPDM2SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[2]
23:20	SPDM1SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[1]
19:16	SPDM0SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[0]
15:14	TBHSEL	Testbus highselect It governs which set of signals are to testbus[31:16] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL

MDP4_0_SMMU_MDP0_TESTBUSCR (cont.)

Bits	Name	Description
13:12	TBSLSEL	Testbus low select It governs which set of signals are to testbus[15:0] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL
11:10	RESERVED_2	
9:8	WGSEL	Wrapper group select It selects a particular group of signals from the SMMU wrapper hierarchy WGSEL = 0b00 - wrapper signal group 0 WGSEL = 0b01 - wrapper signal group 1 WGSEL = 0b10 - wrapper signal group 2 WGSEL = 0b11 - reserved
7:2	RESERVED_1	
1	SPDMBE	SPDM test enable Reset state : 0
0	TBE	Testbus enable, which governs whether the testbus is driven with all 0s or with the configured signals Reset state : 0

0x075FFEFC MDP4_0_SMMU_MDP0_VR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: 32'h0000_0000

Note that the DCPBP/DCPPP bits prevent the pipelining of the next transaction when the current transaction is a bypass/pass-through transaction. That is, they add one more cycle of delay between the current and next transactions.

Also note that when we are in global bypass (SMMU_CR[CLIENTPD]=1), these bits should have NO effect, or at least no effect between client transactions, they can have an effect between config and client transactions is appropriate. We must be able to continue to perform fully pipelined transactions when the client port is disabled altogether.

MDP4_0_SMMU_MDP0_VR0

Bits	Name	Description
31:3	RESERVED	

MDP4_0_SMMU_MDP0_VR0 (cont.)

Bits	Name	Description
2	DCPPT	Disable client pipelining for client operations in pass-through mode Reset state : 0
1	DCPBP	Disable client pipelining for client operations in bypass mode Reset state : 0
0	DCP	Disable client pipelining Reset state : 0

0x075FFF00 MDP4_0_SMMU_MDP0_TLBIALL

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries.

MDP4_0_SMMU_MDP0_TLBIALL

Bits	Name	Description
31:0	EXEC	Writing any value to this register invalidates all TLB entries, as specified by the contents of SMMU_CR[TLBIALLCFG]

0x075FFF04 MDP4_0_SMMU_MDP0_TLBIVMID

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries matching the IVMID value. Precise function is governed by SMMU_CR[TLBIALLCFG].

MDP4_0_SMMU_MDP0_TLBIVMID

Bits	Name	Description
31:5	RESERVED	
4:0	IVMID	Designates VMID[4:0] value of entries to be invalidated.

14.23.1.4 SMMU configuration registers

0x075FFF80 MDP4_0_SMMU_MDP0_CR

Type: Read/Write
Clock: AXI_BUS_CLOCK

Global configuration register.

MDP4_0_SMMU_MDP0_CR

Bits	Name	Description
31:10	RESERVED_2	
9	RESERVED_1	Reset state : 0
8	TLBIVMIDCFG	TLBIVMID configuration control. When set to 0,flash-invalidate, SMMU_TLBIVMID commands flash-invalidate the entire TLB, without regard to locking ,security and VMID value. When set to 1, selective, SMMU_TLBIVMID invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and VMID field matching the VMID specified by SMMU_TLBIVMID command. Reset state : X
7	TLBIALLCFG	TLBIALL configuration control. When set to 0, flash-invalidate, SMMU_TLBIALL commands flash-invalidate the entire TLB, without regard to locking and/or security. When set to 1, selective, SMMU_TLBIALL invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and are unlocked. Reset state : X
6	TLBLKCRWE	TLBLKCR write enable. When set to 0, writes to SMMU_CBn_TLBLKCR are ignored. When set to 1, allows operating environments to manage the TLB locking mechanism directly. Management amounst multiple operating environments must be coordinated externally between themselves. Reset state : X
5	STALLD	Global disable for stall mode. When set to 1, context bank stall modes are ignored and operate as terminate mode. Reset state : X
4	CLIENTPD	Client port disable. When set, all client accesses are forced to bypass the system MMU. There is no translation. access control, or attribute generation. This bit overrides individual SMMU_M2VCBRn[BYPASSD] settings; client requests are bypassed, even if SMMU_M2VCBRn[BYPASSD] is set to 1. Bypass request errors are not recorded in SMMU_ESR, nor reported to requesting masters. The SMMU_rpuErrIrptReq interrupt output signal is not asserted. Reset state : 1

MDP4_0_SMMU_MDP0_CR (cont.)

Bits	Name	Description
3	DCDEE	When set to 0, configuration port decode errors do not set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn are not updated. When set to 1, configuration port decode errors set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn updated with address and syndrome of error. Reset state : X
2	RPUEIE	When set, configuration port errors and client port bypass errors are reported directly to the interrupt controller via the SMMU_rputErrIrptReq interrupt output signal. Interrupt output is asserted if SMMU_CR[RPUIE_EN] is 1 and ANY bit is set in SMMU_ESR register. Reset state : 0
1	RPUERE	When set, SMMU reports configuration port errors and client port bypass errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via AXI port will use decode error, rather than slave error. Regardless of the value of this field both configuration port errors and client port bypass request errors are terminated by the SMMU as RAZ/WI, and are recorded in SMMU_ESR register. Reset state : X
0	RPUE	When set, all configuration port accesses are checked against SMMUX_RPU_ACR and/or the SMMUX_CBACRn registers for access permissions. Reset state : 0

14.23.1.5 SMMU error report registers

0x075FFF84 MDP4_0_SMMU_MDP0_EAR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: unknown

When there is an error, holds the physical address of the errant transaction.

MDP4_0_SMMU_MDP0_EAR

Bits	Name	Description
31:0	PA	Physical address[31:0]

0x075FFF88 MDP4_0_SMMU_MDP0_ESR

Type: Read/Write to clear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This register has read/write clear access. Reads return the value in the register, a write with a 1 set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

MDP4_0_SMMU_MDP0_ESR

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x075FFF8C MDP4_0_SMMU_MDP0_ESRRESTORE

Type: Write
Clock: RPM_BUS_CLK
Reset State: Undefined

This register is an aliased address for SMMU_ESR, but it allows direct write access. In this way, diagnostic software can cause an error to be generated and reported.

MDP4_0_SMMU_MDP0_ESRRESTORE

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	

MDP4_0_SMMU_MDP0_ESRRESTORE (cont.)

Bits	Name	Description
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x075FFF90 MDP4_0_SMMU_MDP0_ESYNR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

MDP4_0_SMMU_MDP0_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request
15:0	AMID	AMID[15:0] field of errant request

0x075FFF94 MDP4_0_SMMU_MDP0_ESYNR1

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

MDP4_0_SMMU_MDP0_ESYNR1

Bits	Name	Description
31	DCD	(decode) Indicates configuration port error due to invalid/unrecognized address (e.g., a reserved register address) Includes decode errors within both the global address space and the individual context bank address space

MDP4_0_SMMU_MDP0_ESYNR1 (cont.)

Bits	Name	Description
30	AC	(access control) Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO field of the errant request
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request)
15:12	ALEN	ALEN[3:0] field of the errant request
11	RESERVED_2	
10	ABURST	ABURST[1:0] field of the errant request
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request
7	AINST	AINST field of the errant request
6	APROTNS	APROTNS field of the errant request
5	APRIV	APRIV field of the errant request
4	AINNERSHARED	AINNERSHARED field of the errant request
3	ASHARED	ASHARED field of the errant request
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

14.23.1.6 SMMU revision register

0x075FFFF4 MDP4_0_SMMU_MDP0_REV

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the revision information for the SMMU core and wrapper.

MDP4_0_SMMU_MDP0_REV

Bits	Name	Description
31:12	RESERVED	

MDP4_0_SMMU_MDP0_REV (cont.)

Bits	Name	Description
11:8	WRAPPER	Wrapper version
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

14.23.1.7 SMMU implementation parameter register

0x075FFFF8 MDP4_0_SMMU_MDP0_IDR

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the parameter information for the SMMU core and wrapper

MDP4_0_SMMU_MDP0_IDR

Bits	Name	Description
31:24	NIRPT	NIRPT[7:0] Indicates number of context fault interrupt outputs (minus 1) supported by the System MMU Value can range from 0 - 255 (1 - 256 context fault interrupt outputs)
23:16	NCB	NCB[7:0] Indicates number of context banks (minus 1) supported by the System MMU Value can range from 0 - 254 (1 - 255 context banks)
15:12	TLBSIZE	TLBSIZE[3:0] Indicates log2(number of TLB entries) That is, number of TLB entries = 2 ** TLBSIZE
11	RESERVED	
10	HUM	Indicates whether or not TLB hit-under-miss behavior is supported
9	HTW	Indicates whether or not the System MMU supports hardware table walk If hardware table walk not supported (HTW=0), then software cannot set SMMU_CBn_ACTLR[TLBMCFG] to 0b10
8:0	NM2VCBMT	NM2VCBMT[8:0] Indicates number of M2VCBMT entries, with a maximum of 512 The bit width of the M2VCBMTIindex input (maximum value is 9) is equal to log base 2 of NM2VCBMT Allows for up to 7-bit MID field, plus NS-prot or other fields to select mapping [

0x075FFFFC MDP4_0_SMMU_MDP0_RPU_ACR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Using the incoming HVMID, this register controls access to the global register space.

MDP4_0_SMMU_MDP0_RPU_ACR

Bits	Name	Description
31:0	RWE	Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the entire block of registers within the SMMU's 4KB global address space, including this register itself. A VMID identified by this register is also permitted global access to all context banks. In practice, this register designates the VMID(s) that can act as SROT.

14.23.2 SMMU Context Bank Registers

There are a configurable number (1 to 9) of context banks in the SMMU. Each context bank consists of a set of registers in a unique 4KB address space.

14.23.2.1 SMMU context bank control registers

0x07500000+0x1000*n MDP4_0_SMMU_MDP0_CBn_SCTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank System Control Register controls various architected SMMU features

MDP4_0_SMMU_MDP0_CBn_SCTLR

Bits	Name	Description
31:5	RESERVED_2	
4	BE	Governs the order byte order or "endianness" of the page table entries. When set to 0, page table entries are in little endian format, so that their least significant byte is in byte 0 of the 32 bit entry. When set to 1, page table entries are in big endian format, so that their most significant byte is in byte 0 of the 32 bit entry.
3	RESERVED_1	Reserved for HAF, Hardware access flag. This bit governs whether the access flag is managed by hardware or software. The SMMU supports software access flag management only, so this bit is read-only and internally driven to 0.

MDP4_0_SMMU_MDP0_CBn_SCTLR (cont.)

Bits	Name	Description
2	AFE	Access flag enable. When AFE = 0, the access flag field is not supported and the AP[0] page table entry field acts as a bit of the overall AP[2:0] field to determining access permissions. When AFE = 1, the AP[0] page table entry field becomes the access flag, and the reduced number of access permission combinations is specified by AP2:1], and SMMU hardware will signal an Access Flag fault if a request targets a page for which the access flag is 0.
1	TRE	TEX remap enable. This bit governs the mapping of the page table entry TEX[2:0],C,B and SH fields into an SMMU TLB entry, and thus the translation of the AMEMTYPE[2:0], ASHARED and AINNERSHARED bus attributes. When TRE = 0, the TLB value is determined directly from the page table entry fields.
0	M	MMU enable bit. When set to 1, this context bank is enabled for translating requests. When set to 0, accesses bypass the TLB, and there is no address translation, access permission checking or attribute mapping. Incoming master requests are passed through unchanged.

0x07500004+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_ACTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank auxiliary control register controls various implementation specific features.

MDP4_0_SMMU_MDP0_CBn_ACTLR

Bits	Name	Description
31:19	RESERVED	
18	RESERVED_2	
17:16	V2PCFG	VA-to-PA configuration. Governs operation of VA-to-PA commands that miss in the TLB 0x0: terminate (Record TLB Miss context fault in SMMU_CBn_PAR) 0x1: software table update (Translate based on values in SMMU_CBn_TLBFLPTER and SMMU_CBn_TLBSLPTER) 0x2: hardware table walk (Translate based on value of PTE read from page table in memory) 0x3: reserved

MDP4_0_SMMU_MDP0_CBn_ACTLR (cont.)

Bits	Name	Description
15	TIPCF	Governs whether or not all subsequent requests using this context bank should be terminated if a prior context fault has occurred and has not yet been cleared from SMMU_CBn_FSR Accesses to other context banks proceed as normal 0x0: do not terminate (System MMU will attempt to process subsequent requests despite the presence of an existing context fault in SMMU_CBn_FSR. SMMU_CBn_FSR will be set if the subsequent access also encounters a context fault) 0x1: terminate (All subsequent accesses terminated by the System MMU as RAZ/WI, even if SMMU_CBn_ACTLR[TLBMCFG, CFCFG] configured for stall mode. SMMU_CBn_FSR set when access is terminated due to TIPCF = 1. Presence of SMMU_CBn_FSR when SMMU_CBn_ACTLR is 1 implies that the later exceptions must have been simply the forced terminations due to the prior context fault. Error optionally reported to the requesting master, according to the client port bus protocol, f SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus if SMMU_CBn_ACTLR is 1.)
14	CFCFG	(context fault configuration) Governs the behavior of all context faults except TLB miss TLB miss context faults are governed by SMMU_CBn_ACTLR[TLBMCFG] 0x0: terminate (Access terminates at the System MMU as RAZ/WI. Context fault exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x1: stall (Requesting master's access stalled while System MMU waits for managing processor to resolve context fault. Context fault exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode)

MDP4_0_SMMU_MDP0_CBn_ACTLR (cont.)

Bits	Name	Description
13:12	TLBMCFG	(TLB miss configuration) Governs the behavior of client accesses that miss in the TLB 0x0: pass-through (Access passed through to targeted slave without translation, attribute control, or access permission checking. Effectively, behavior is as if SMMU_CBn_SCTLR = 0 i.e., MMU disabled for this context bank. TLB miss not considered a context fault. TLB miss exception not recorded in SMMU_CBn_FSR. TLB miss exception not reported to requesting master. SMMU_contextFaultIrptReq interrupt output not asserted) 0x1: terminate (Access terminates at the System MMU as RAZ/WI,TLB miss exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x2: stall (Requesting master's access stalled while System MMU waits for managing processor to update TLB. TLB miss exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode) 0x3: HTW (Hardware table walk . Requesting master's access stalled while System MMU accesses page table. The is TLB updated and requesting master's access resumed after obtaining valid entry from page table. If translation fault, then access either terminates or stalls according to setting of SMMU_CBn_ACTLR)
11	DNLV2PA	(disable non-locking VA-to-PA allocation) Governs whether or not TLB misses due to non-locking VA-to-PA commands will allocate a new entry This field is ignored for locking VA-to-PA operations (SMMU_CBn_TLBLKCR[LKE] = 1)
10	DNA	(disable normal allocation) Governs whether or not TLB misses due to client port accesses will allocate a new entry
9:8	PRIVCFG	0x0: apriv (System MMU uses APRIV signal supplied by master as user/supervisor indicator 1 = supervisor) 0x1: reserved 0x2: User (System MMU ignores APRIV; treats all requests using this context bank as user) 0x3: Supervisor (System MMU ignores APRIV; treats all requests using this context bank as supervisor)

MDP4_0_SMMU_MDP0_CBn_ACTLR (cont.)

Bits	Name	Description
7:5	RESERVED_1	
4	RCNSH	(redirect cacheable-non-shareable) Governs whether or not cacheable accesses that are non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache, even though the locations are not being coherently shared with Scorpion-MP
3	RCISH	(redirect cacheable-inner-shareable) Governs whether or not cacheable accesses that are inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
2	RCOSH	(redirect cacheable-outer-shareable) Governs whether or not cacheable accesses that are outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
1	CFEIE	(context fault error interrupt enable) Governs whether or not client port request context faults are reported directly to the interrupt controller via the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus Interrupt output is asserted if SMMU_CBn_ACTLR[CFEIE] is 1 and any context fault bits are set in SMMU_CBn_FSR Such interrupts would generally be directed to the interrupt controller of whichever processor is currently managing this context bank of the System MMU Reset state : 0
0	CFERE	(context fault error report enable) Governs whether or not client port request context faults that are configured for terminate mode (or that are explicitly terminated after stall mode) are reported to the requesting master, according to the client port bus protocol All error types reported via AXI port will use decode error rather than slave error All context faults are recorded in SMMU_CBn_FSR, regardless of the value of this field.

0x07500008+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_CONTEXTIDR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context ID register holds the ASID associated with this context bank

MDP4_0_SMMU_MDP0_CBn_CONTEXTIDR

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Specifies the 8 bit ASID value assigned to this context bank. The ASID can be included in the key comparison of TLB entries. .

0x07500010+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_TTBR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR0 is used for low order virtual addresses, typically private pages for a given process.

MDP4_0_SMMU_MDP0_CBn_TTBR0

Bits	Name	Description
31:7	PA	BIts 31:7 of the physical address of the base of the page table. The actual LSB of the base address is bit 14-N, where N is set in register TTCR
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07500014+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_TTBR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR1 is used for high order virtual addresses, typically global pages for a given VMID, or kernal mappings.

The context bank auxiliary control register controls various implementation specific features.

MDP4_0_SMMU_MDP0_CBn_TTBR1

Bits	Name	Description
31:14	PA	BIts 31:14 of the physical address of the base of the page table.
13:7	RESERVED_2	
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED_1	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07500018+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_TTBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table control register, which specifies the size of the virtual address space that uses TTBR0.

MDP4_0_SMMU_MDP0_CBn_TTBCR

Bits	Name	Description
31:6	RESERVED_2	
5	PD1	Page disable 1; if this bit is set, hardware table walks attempting to use TTBR1will result in a first level descriptor translation fault. If clear, TTBR1 contents are used.
4	PD0	Page disable 0; if this bit is set, hardware table walks attempting to use TTBR0 will result in a first level descriptor translation fault. If clear, TTBR0 contents are used.
3	RESERVED_1	
2:0	N	N[2:0] specifies the number of upper order virtual address bits which must be 0 in order for translations to use the table pointed to by TTBR0. If any of these bits are non-zero, TTBR1 is used for the lookup. If N is 0, only TTBR0 is used.

0x0750001C+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_PAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The physical address register captures the physical address value resulting from the execution of a VA-to-PA command

Field definitions vary according to whether or not there is a context fault associated with the requested translation

MDP4_0_SMMU_MDP0_CBn_PAR

Bits	Name	Description
31:12	PAR_FAULT_INFO_312	
11	RESERVED_2	
10:9	PAR_FAULT_INFO_72	
8	RESERVED_1	
7:1	PAR_FAULT_INFO_71	Encoding varies according to value in FAULT field.
0	FAULT	(fault status) This field will be 1 when a context fault is associated with the requested translation, and 0, when there is no context fault associated with the requested translation.

0x07500020+0x1000*n MDP4_0_SMMU_MDP0_CBn_FSR, n=[0..1]

Type: Read/WriteClear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The Fault Status Register records status information for client accesses that encounter exceptions within the context bank, e.g. translation faults.This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data

This prevents inadvertent clearing of new faults when writing the register to clear an old fault

The presence of an asserted value on any bit in this register (except the SS bit) is what prompts the assertion (when enabled by SMMU_CBn_ACTLR[CFEIE]) of the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus

Therefore, these bits must be cleared by the interrupt handler

This is contrasted with the fields in the SMMU_CBn_FSYNRn registers, which are merely the "syndrome" of the fault indicated by SMMU_CBn_FSR

MDP4_0_SMMU_MDP0_CBn_FSR

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry

MDP4_0_SMMU_MDP0_CBn_FSR (cont.)

Bits	Name	Description
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07500024+0x1000*n MDP4_0_SMMU_MDP0_CBn_FSRRESTORE, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Allows SW to force a value into the SMMU_CBn_FSR register.

MDP4_0_SMMU_MDP0_CBn_FSRRESTORE

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)

MDP4_0_SMMU_MDP0_CBn_FSRRESTORE (cont.)

Bits	Name	Description
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07500028+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_FAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The Fault Address Register records the virtual address of client accesses that encounter exceptions within the context bank, e.g. translation faults. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

MDP4_0_SMMU_MDP0_CBn_FAR

Bits	Name	Description
31:0	VA	VA[31:0] of errant client access

0x0750002C+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_FSYNR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

NOTE omission of VMID field from this register, as VMID can only be made visible to SROT, and not to general OS software that manages the context bank registers

MDP4_0_SMMU_MDP0_CBn_FSYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] (ATID field of errant request)

MDP4_0_SMMU_MDP0_CBn_FSYNR0 (cont.)

Bits	Name	Description
23:16	RESERVED	
15:13	ABID	ABID[2:0] (ABID field of errant request)
12:8	APID	APID[4:0] (APID field of errant request)
7:0	AMID	AMID[7:0] (AMID field of errant request)

0x07500030+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_FSYNR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

MDP4_0_SMMU_MDP0_CBn_FSYNR1

Bits	Name	Description
31:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO (AOOO field of the errant request)
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request
15:12	ALEN	ALEN[3:0]field of the errant request
11	RESERVED_2	
10	ABURST	field of the errant request
9	RESERVED_1	
8	AWRITE	field of the errant request
7	AINST	field of the errant request
6	APROTNS	field of the errant request
5	APRIV	field of the errant request
4	AINNERSHARED	(AINNERSHARED field of the errant request)
3	ASHARED	(ASHARED field of the errant request)

MDP4_0_SMMU_MDP0_CBn_FSYNR1 (cont.)

Bits	Name	Description
2:0	AMEMTYPE	AMEMTYPE[2:0] (AMEMTYPE field of the errant request)

0x07500034+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_PRRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs memory type and shareability attributes of requests that are both MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1)

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) and/or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, memory type encoding is as follows:

0b00 = strongly-ordered

0b01 = device

0b10 = normal

0b11 = reserved

MDP4_0_SMMU_MDP0_CBn_PRRR

Bits	Name	Description
31	NOS7	not-outer-shareable class 7
30	NOS6	not-outer-shareable class 6
29	NOS5	not-outer-shareable class 5
28	NOS4	not-outer-shareable class 4
27	NOS3	not-outer-shareable class 3
26	NOS2	not-outer-shareable class 2
25	NOS1	not-outer-shareable class 1
24	NOS0	not-outer-shareable class 0
23:20	RESERVED	

MDP4_0_SMMU_MDP0_CBn_PRRR (cont.)

Bits	Name	Description
19	SHNMSH1	(shareable attribute for normal memory accesses with SH=1) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1
18	SHNMSH0	(shareable attribute for normal memory accesses with SH=0) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0
17	SHDSH1	SHDSH1 (shareable attribute for device accesses with SH=1) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1 [
16	SHDSH0	SHDSH0 (shareable attribute for device accesses with SH=0) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0 [
15:14	MTC7	MTC7[1:0] (memory type class 0)
13:12	MTC6	MTC6[1:0] (memory type class 0)
11:10	MTC5	MTC5[1:0] (memory type class 0)
9:8	MTC4	MTC4[1:0] (memory type class 0)
7:6	MTC3	MTC3[1:0] (memory type class 0)
5:4	MTC2	MTC2[1:0] (memory type class 0)
3:2	MTC1	MTC1[1:0] (memory type class 0)
1:0	MTC0	MTC0[1:0] (memory type class 0)

0x07500038+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_NMRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs the cache policy of MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1) requests for which the memory type is mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0) or the memory type is mapped to a type other than normal memory (SMMU_CBn_PRRR[MTCn] != 0b10)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, inner-cache and outer-cache policy encodings are as follows:

0b00 = non-cacheable

0b01 = cacheable, copy-back, write-allocate

0b10 = cacheable, write-through, write-no-allocate

0b11 = cacheable, copy-back, write-no-allocate

MDP4_0_SMMU_MDP0_CBn_NMRR

Bits	Name	Description
31:30	OCPC7	OCPC7[1:0] (inner-cache policy class 7)
29:28	OCPC6	OCPC6[1:0] (inner-cache policy class 6)
27:26	OCPC5	OCPC5[1:0] (inner-cache policy class 5)
25:24	OCPC4	OCPC4[1:0] (inner-cache policy class 4)
23:22	OCPC3	OCPC3[1:0] (inner-cache policy class 3)
21:20	OCPC2	OCPC2[1:0] (inner-cache policy class 2)
19:18	OCPC1	OCPC1[1:0] (inner-cache policy class 1)
17:16	OCPC0	OCPC0[1:0] (inner-cache policy class 0)
15:14	ICPC7	ICPC7[1:0] (inner-cache policy class 7)
13:12	ICPC6	ICPC6[1:0] (inner-cache policy class 6)
11:10	ICPC5	ICPC5[1:0] (inner-cache policy class 5)
9:8	ICPC4	ICPC4[1:0] (inner-cache policy class 4)
7:6	ICPC3	ICPC3[1:0] (inner-cache policy class 3)
5:4	ICPC2	ICPC2[1:0] (inner-cache policy class 2)
3:2	ICPC1	ICPC1[1:0] (inner-cache policy class 1)
1:0	ICPC0	ICPC0[1:0] (inner-cache policy class 0)

0x0750003C+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_TLBLKCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB lock control register governs the TLB locking mechanism and TLB invalidate operations.Write access to this register is governed by SMMU_CR[TLBLKCRWE]

When SMMU_CR[TLBLKCRWE] is 0, writes to SMMU_CBn_TLBLKCR are ignored

Read access is still permitted

SROT can set SMMU_CR[TLBLKCRWE] to 1 to allow operating environment(s) to manage the TLB locking mechanism

Management amongst multiple operating environments must be coordinated via semaphore

MDP4_0_SMMU_MDP0_CBn_TLBLKCR

Bits	Name	Description
31:24	RESERVED_2	
23:16	VICTIM	VICTIM[7:0] Indicates the TLB index at which the next normal (non-locking) allocation will occur Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context
15:8	FLOOR	FLOOR[7:0] Indicates the TLB index from which round-robin replacement on normal (non-locking) allocations occurs TLB entries at indices below this value are locked Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context banks
7:4	RESERVED_1	
3	TLBIVAACFG	(TLBIVAA configuration) TLBIVAACFG = 0 - flash-invalidate SMMU_CBn_TLBIVAA commands flash-invalidate the entire TLB, without regard to locking, security, address, and/or VMID value TLBIVAACFG = 1 - selective SMMU_CBn_TLBIVAA commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank VA field of TLB entry matches VA designated by SMMU_CBn_TLBIVAA command NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked

MDP4_0_SMMU_MDP0_CBn_TLBLKCR (cont.)

Bits	Name	Description
2	TLBIASIDCFG	(TLBIASID configuration) TLBIASIDCFG = 0 - flash-invalidate SMMU_CBn_TLBIASID commands flash-invalidate the entire TLB, without regard to locking, security, VMID, and/or ASID values TLBIASIDCFG = 1 - selective SMMU_CBn_TLBIASID commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command TLB entry is not global (NG field is 1) NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
1	TLBIALLCFG	(TLBIALL configuration) TLBIALLCFG = 0 - flash-invalidate SMMU_CBn_TLBIALL commands flash-invalidate the entire TLB, without regard to locking, security, and/or VMID value TLBIALLCFG = 1 - selective SMMU_CBn_TLBIALL commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked
0	LKE	(lock enable) Governs whether or not TLB entries established by VA-to-PA commands upon TLB misses are locked LKE = 0 (normal, non-locking) Allocate VA-to-PA TLB entry (if TLB miss) at the index specified by SMMU_CBn_TLBLKCR[VICTIM] Allocation is disabled if SMMU_CBn_ACTLR[DNLV2PA] is 1 Increment SMMU_CBn_TLBLKCR[VICTIM] by 1 (only if new entry allocated) Wrap back to the value of SMMU_CBn_TLBLKCR[FLOOR] when the last entry is written LKE = 1 (locking) Search TLB for specified VA and invalidate if found Provides atomicity between the invalidate and the new allocation within the locked region Allocate VA-to-PA TLB entry at the index specified by data operand bits 7:0 of the VA-to-PA command This value must be less than SMMU_CBn_TLBLKCR[FLOOR] in order for it to remain locked Allocation occurs even if non-locking allocation is disabled due to SMMU_CBn_ACTLR[DNLV2PA] = 1

0x07500040+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_V2PSR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The VA-to-PA status register records the hit/miss status and TLB index or V2Pxx and TLB invalidate commands.

MDP4_0_SMMU_MDP0_CBn_V2PSR

Bits	Name	Description
31:16	RESERVED_2	
15:8	INDEX	INDEX[7:0] Indicates the index of the TLB entry associated with the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command If SMMU_CBn_V2PSR[HIT] is 0, then SMMU_CBn_V2PSR[INDEX] is the index to which the entry was allocated (if allocated at all) If SMMU_CBn_V2PSR[HIT] is 1, then SMMU_CBn_V2PSR[INDEX] is the index of the entry which hit
7:1	RESERVED_1	
0	HIT	Indicates whether or not there was a TLB hit (prior to allocation, if any) on the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command

0x07500044+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_TLBFLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB first level PTE register holds the first level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

This register (together with SMMU_CBn_TLBSLPTER) is used as the source of the translation information for VA-to-PA operations when the MMU is enabled (SMMU_CBn_SCTLR[M] = 1) and the operations are configured for software table update (SMMU_CBn_ACTLR[V2PCFG] = 0b01)

Field definitions vary according to the type of PTE (fault, page, section, or supersection), and come directly from the ARMv7 architecture's PTE formats

MDP4_0_SMMU_MDP0_CBn_TLBFLPTER

Bits	Name	Description
31:10	FL_PTE_HI	

MDP4_0_SMMU_MDP0_CBn_TLBFLPTER (cont.)

Bits	Name	Description
9:5	RESERVED	
4:2	FL_PTE_LO	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	This field should be set to 0b00 or 0b11 to indicate that the translation should result in a context fault, and the rest of the fields are defined as indicated in this section If this field is not 0b00 or 0b11, then the PTE is of some other type (see other sections for the field definitions for those types)

0x07500048+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_TLBSLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB second level PTE register holds the second level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

Field definitions vary according to the type of PTE (fault, 64KB or 4KB), and come directly from the ARMv7 architecture's PTE format

MDP4_0_SMMU_MDP0_CBn_TLBSLPTER

Bits	Name	Description
31:2	SL_PTE	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	0x0: fault

0x0750004C+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_BFBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The burst fetch buffer configuration register governs the operation of the "burst fill" feature of the SMMU.

MDP4_0_SMMU_MDP0_CBn_BFBCR

Bits	Name	Description
31:12	STRIDE	(stride amount) 4KB-aligned value to be added to virtual address on demand TLB miss for filling subsequent BFB Stride of minimum 4KB alignment useful for preventing stride burst fetch until final PTE of the demand BFB entry is used
11:8	SLVIC	(second-level victim) Indicates the SLBFB index at which the next round-robin allocation will occur
7:4	FLVIC	(first-level victim) Indicates the FLBFB index at which the next round-robin allocation will occur
3	RESERVED	
2	SFVS	(stride-fetch victim selection) SFVS. = 0 (replace normal round-robin victim-selected entry) Useful when stride is larger than the VA space represented by the four PTEs in the demand BFB entry, but the client access pattern is for more than just the initial PTE in that demand BFB entry SFVS. = 1 (replace same BFB used by demand VA for which the stride burst is being performed) Useful when stride is the same as the VA space represented by an individual PTE in the demand BFB entry (such that the stride won't miss against the BFB until the last PTE of the demand BFB entry is accessed), and/or when the client access pattern only uses the initial PTE in the demand BFB entry
1	BFBSFE	(burst fetch buffer stride fetch enable) Enables stride burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Stride burst fetch is for the block of four PTEs associated with VA+stride VA is the "demanded" VA from the client (or VA-to-PA command) Stride value is specified by SMMU_CBn_BFBCR[STRIDE] Stride burst fetch only occurs if demand access for VA misses in TLB (could hit in BFB) and address VA+stride misses in both TLB and BFB
0	BFBDFE	(burst fetch buffer demand fetch enable) Enables demand burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Demand burst fetch is for the block of four PTEs associated with the "demanded" VA from the client (or VA-to-PA command) Demand burst fetch only occurs if demand access misses in both TLB and BFB

0x07500800+0x1000*n MDP4_0_SMMU_MDP0_CBn_TLBIALL, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate all command register invalidates all TLB entries matching the VMID associated with this context bank. Data operand is ignored.

MDP4_0_SMMU_MDP0_CBn_TLBIALL

Bits	Name	Description
31:0	RESERVED	

0x07500804+0x1000*n MDP4_0_SMMU_MDP0_CBn_TLBIASID, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by ASID command register invalidates TLB entries matching the specified ASID and matching the VMID associated with this context bank.Invalidates TLB entries which are associated with the designated ASID and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIASIDCFG] governs whether command flash-invalidates entire TLB array or just the entries matching the VMID, ASID, and security state

TLBIASIDCFG = 0 - flash-invalidate

SMMU_CBn_TLBIASID command flash-invalidates the entire TLB, without regard to locking, security, VMID, and/or ASID values

TLBIASIDCFG = 1 - selective

SMMU_CBn_TLBIASID command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command data operand

TLB entry is not global (NG field is 1)

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command

Locking is not considered (matching entries are invalidated even if locked)

ASID field of command specifies the ASID value of the TLB entries to be invalidated

MDP4_0_SMMU_MDP0_CBn_TLBIASID

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Actual ASID value

0x07500808+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_TLBIVA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA command invalidates TLB entries matching the designated VA, ASID and the VMID associated with this context bank.

Matching entry determined as follows:

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIVA command data operand (or TLB entry is global - NG field is 0)

VA field of TLB entry matches VA value designated by the SMMU_CBn_TLBIVA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIVA command

Locking is not considered (matching entry is invalidated even if locked)

Data operand specifies the VA and ASID value of the TLB entry to be invalidated

MDP4_0_SMMU_MDP0_CBn_TLBIVA

Bits	Name	Description
31:12	VA	VA[31:12]
11:8	RESERVED	
7:0	ASID	ASID[7:0] value

0x0750080C+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_TLBIVAA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA all ASIDS command invalidates TLB entries matching the designated VA and the VMID associated with this context bank, regardless of ASID.Invalidates TLB entries which are associated with the designated VA, regardless of ASID, and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIVAACFG] governs whether command flash-invalidates entire TLB array or just the non-locked entries matching the VMID, ASID, and security state

TLBIVAACFG = 0 - flash-invalidate

SMMU_CBn_TLBIVAA command flash-invalidates the entire TLB, without regard to locking, security, address, and/or VMID value

TLBIVAACFG = 1 - selective

SMMU_CBn_TLBIVAA command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

VA field of TLB entry matches VA designated by the SMMU_CBn_TLBIVAA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command

Entry is unlocked

MDP4_0_SMMU_MDP0_CBn_TLBIVAA

Bits	Name	Description
31:12	VA	VA[31:12]
11:0	RESERVED	

0x07500810+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_V2PRR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

MDP4_0_SMMU_MDP0_CBn_V2PRR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07500814+0x1000*n MDP4_0_SMMU_MDP0_CBn_V2PPW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

MDP4_0_SMMU_MDP0_CBn_V2PPW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07500818+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_V2PUR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

MDP4_0_SMMU_MDP0_CBn_V2PUR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x0750081C+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_V2PUW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

.Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

MDP4_0_SMMU_MDP0_CBn_V2PUW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	

MDP4_0_SMMU_MDP0_CBn_V2PUW (cont.)

Bits	Name	Description
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07500820+ 0x1000*n MDP4_0_SMMU_MDP0_CBn_RESUME, n=[0..1]

Type: Write/command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB resume command causes the SMMU to resume operation after a stalled access..

MDP4_0_SMMU_MDP0_CBn_RESUME

Bits	Name	Description
31:1	RESERVED	
0	TNR	Terminate/not retry When TNR is written as 0, indicates that the stalled access should be retried by the system MMU. When written as 1, indicates that this stalled transaction is terminated by the system MMU. The error is optionally reported to the requesting master, using the client port bus protocol, if SMMU_CNn_ACTLR[CFERE] == 1. Interrupt optionally remains asserted via SMMU_M2VCBRn[IRPTINDX] selected SMMU_contextFaultIrptReq bit, only if SMMU_CBn_ACTLR[CFEIE] is 1, and only if SMMU_CBn_FSR has not been cleared by software priori to issuing this command..

14.24 MDP4 1 SMMU Registers (0x07600000 SMMU_MDP4_1_BASE)

This section contains the MDPF4 1 SMMU registers.

14.24.1 SMMU Global Registers

14.24.1.1 SMMU VMID/CBNDX mapping registers

0x076FF000+ 0x4*n MDP4_1_SMMU_MDP1_M2VCBRn, n=[0..15]

Type: Read/Write
Clock: AXI_CLK
Reset State: Undefined

SMMU_M2VCBRm registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

MDP4_1_SMMU_MDP1_M2VCBRn

Bits	Name	Description
31:28	RESERVED_2	
27:25	BPMEMTYPE	(bypass memory type) Supplies the AMEMTYPE attributes for client requests which bypass the System MMU when SMMU_M2VCBRn[BPMTCFG] = 1 See reference section for AMEMTYPE encoding definitions
24	BPMTCFG	(bypass memory type configuration) Governs the memory type (AMEMTYPE) attributes of client requests which bypass the System MMU BPMTCFG = 0 - use AMEMTYPE Bypass requests use AMEMTYPE signal supplied by client master BPMTCFG = 1 - use SMMU_M2VCBRn[BPMEMTYPE] Bypass requests use SMMU_M2VCBRn[BPMEMTYPE] Reset state : 0
23:22	NSCFG	(non-secure configuration) Governs the incoming security designation of client requests NSCFG = 0b00 - use APROTNS Use APROTNS signal supplied by client master NSCFG = 0b01 - reserved NSCFG = 0b10 - secure System MMU ignores APROTNS; treats all requests as secure NSCFG = 0b11 - non-secure System MMU ignores APROTNS; treats all requests as non-secure Reset state : 0

MDP4_1_SMMU_MDP1_M2VCBRn (cont.)

Bits	Name	Description
21:20	BPSHCFG	(bypass shareability configuration) Governs the shareability realm (ASHARED and AINNERSHARED) attributes of client requests which bypass the System MMU BPSHCFG = 0b00 - use ASHARED and AINNERSHARED Bypass requests use ASHARED and AINNERSHARED signals supplied by client master BPSHCFG = 0b01 - outer-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 0 BPSHCFG = 0b10 - inner-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 1 BPSHCFG = 0b11 - non-shareable Bypass requests set ASHARED = 0, AINNERSHARED = 0 Reset state : 0
19	BPRCNSH	(bypass redirect cacheable-non-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache Reset state : 0
18	BPRCISH	(bypass redirect cacheable-inner-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0
17	BPRCOSH	(bypass redirect cacheable-outer-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0

MDP4_1_SMMU_MDP1_M2VCBRn (cont.)

Bits	Name	Description
16	BYPASSD	Bypass disable for this index Governs whether or not client port accesses using this mapping table entry are actually permitted to "bypass" the System MMU when such bypass is indicated (either due to CBNDX = 255 or due to the master asserting the "SMMU bypass" input) This field is ignored (and operates as if it were 0) if SMMU_CR[CLIENTPD] is 1 BYPASSD = 0 - bypass enabled Bypass requests truly bypass the System MMU and "pass-through" to the fabric (no translation, access control, or attribute generation) No cycle of latency for System MMU context bank access Bypass request not considered an error Bypass request error not recorded in SMMU_ESR[BYPASS] Bypass error not reported to requesting master SMMU_rpuErrIrptReq interrupt output not asserted Client accesses still reference M2VCBMT to get VMID value for presentation to fabric BYPASSD = 1 - bypass disabled System MMU terminates the access as RAZ/WI Bypass request is considered an error Bypass request error is recorded in SMMU_ESR[BYPASS] If SMMU_CR[RPUERE] is 1, then bypass error reported to requesting master according to the client port bus protocol If SMMU_CR[RPUEIE] is 1, then SMMU_rpuErrIrptReq interrupt output asserted
15:8	CBNDX	Context bank index Context bank index associated with the M2VCBMT index CBNDX = 255 indicates no context bank assigned ("bypass")
7:5	RESERVED_1	
4:0	VMID	Virtual machine ID VMID value associated with the M2VCBMT index Must be programmed consistently with the SMMU_CBACRn[CBVMID] field for the context bank designated by SMMU_M2VCBRm[CBNDX]

14.24.1.2 SMMU context bank access control registers

0x076FF800+ 0x4*n MDP4_1_SMMU_MDP1_CBACRn, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs configuration port access to the associated context bank registers.

MDP4_1_SMMU_MDP1_CBACRn

Bits	Name	Description
31:24	IRPTNDX	(interrupt index) Interrupt output number used for context faults associated with this context bank (use SMMU_contextFaultIrptReq[IRPTNDX])
23:21	RESERVED	
20:16	CBVMID	(context bank VMID) Specifies the VMID with which the client masters using the context bank are associated Must be programmed consistently with the M2VCBMT entries that are configured to use the associated context bank This field is used by configuration port commands that need the context bank's VMID value in order to access the TLB (e.g., SMMU_CBn_TLBIVMID, SMMU_CBn_V2Pxx)
15:10	RESERVED_2	
9	RWGE	Read/write global enable. Setting this bit allows access to the context bank registers from any VMID
8	RWE	Read/write enable. Indicates that the RWVMID field is valid.
7:5	RESERVED_1	
4:0	RWVMID	Specifies owner VMID with full read/write access to the registers in the associated context bank "n".

14.24.1.3 SMMU TLB software access registers

0x076FFE00 MDP4_1_SMMU_MDP1_TLBRSW

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Writing to this address requests that the TLB entry at INDEX be read into the SMMU_TLBTRn registers

MDP4_1_SMMU_MDP1_TLBRSW

Bits	Name	Description
31:10	RESERVED	
9:8	TLBBFBS	This field selects the TLB, TFBFB, SLBFB 0x0: Selecting TLB 0x1: Not defined 0x2: Selecting FL BFB 0x3: Selecting SL BFB

MDP4_1_SMMU_MDP1_TLBRSW (cont.)

Bits	Name	Description
7:0	INDEX	TLB index to be read.

0x076FFE80 MDP4_1_SMMU_MDP1_TLBTR0

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

This register holds part of TLB entry read by the last TLBRSW command.

MDP4_1_SMMU_MDP1_TLBTR0

Bits	Name	Description
31:23	RESERVED_4	
22:20	DPSIZC	3 bit decode page size field from CAM-side of TLB CAM-RAM) Same determination and encoding as for DPSIZR The CAM-side copy of this field is used for hit/miss determination in the TLB CAM array
19	RESERVED_3	
18:16	DPSIZR	(3 bit decode page size field from RAM-side of TLB CAM-RAM) Determined from the size fields of the page table entry Encodes the page size as follows: all other values reserved/unused The RAM-side copy of this field is used for virtual ’ physical address formation 0x0: 4KB page 0x1: 64KB page 0x3: 1MB page 0x7: 16MB page
15:12	RESERVED_2	
11	MT2	(memory type bit 2) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[2] attribute bus on the request output of the System MMU

MDP4_1_SMMU_MDP1_TLBTR0 (cont.)

Bits	Name	Description
10	MT1	(memory type bit 1) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[1] attribute bus on the request output of the System MMU
9	MT0	(memory type bit 0) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[0] attribute bus on the request output of the System MMU
8	SH	(shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's outer-shareable realm This field becomes the ASHARED attribute on the request output of the System MMU
7	ISH	(inner-shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's inner-shareable realm This field becomes the AINNERSHARED attribute on the request output of the System MMU
6	NSDESC	(non-secure descriptor) This TLB entry field is a modified version of the corresponding bit of the page table entry Qualified by the NS-prot attribute of the incoming request which prompted the allocation of the TLB entry, such that if the incoming NS-prot attribute was 1 (non-secure), then the NS-desc field of the page table entry was ignored, and the NS-desc field of the TLB entry was forced to 1 Indicates whether the associated memory page contains secure (NS-desc=0) or non-secure (NS-desc=1) information This field becomes the NS-prot attribute on the request output of the System MMU
5	RESERVED_1	

MDP4_1_SMMU_MDP1_TLBTR0 (cont.)

Bits	Name	Description
4	XN	(execute never permission) This TLB entry field comes directly from the corresponding bit of the page table entry
3	UW	(user write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
2	UR	(user read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
1	PW	(privileged write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
0	PR	(privileged read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]

0x076FFE84 MDP4_1_SMMU_MDP1_TLBTR1

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

MDP4_1_SMMU_MDP1_TLBTR1

Bits	Name	Description
31:12	PA	Physical address [31:12] field of the TLB entry
11:5	RESERVED	
4:0	VMID	VMID [4:0]field of the TLB entry)

0x076FFE88 MDP4_1_SMMU_MDP1_TLBTR2

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

MDP4_1_SMMU_MDP1_TLBTR2

Bits	Name	Description
31:12	VA	virtual address field [31:12] of the TLB entry
11	RESERVED	
10	NG	(not global field from page table entry) Indicates whether the page is private to the specified ASID (NG=1) or global to all ASIDs within the VMID using this context bank (NG=0)
9	NSTID	(non-secure tag ID field of the TLB entry) Indicates whether the TLB entry belongs to the secure world (NSTID=0) or the non-secure world (NSTID=1) This field is comned against the incoming NS-prot attribute of the master request as part of TLB hit/miss determination
8	V	valid field of the TLB entry
7:0	ASID	ASID[7:0] field of the TLB entry

0x076FFE8C MDP4_1_SMMU_MDP1_TESTBUSCR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

Governs which signals (if any) from the system SMMU core or wrapper design hierarchy are sent out to the system via a testbus for diagnostic, and also to the system profiling and diagnostic monitor(SPDM).

MDP4_1_SMMU_MDP1_TESTBUSCR

Bits	Name	Description
31:28	SPDM3SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[3]
27:24	SPDM2SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[2]
23:20	SPDM1SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[1]
19:16	SPDM0SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[0]
15:14	TBHSEL	Testbus highselect It governs which set of signals are to testbus[31:16] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL

MDP4_1_SMMU_MDP1_TESTBUSCR (cont.)

Bits	Name	Description
13:12	TBSLSEL	Testbus low select It governs which set of signals are to testbus[15:0] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL
11:10	RESERVED_2	
9:8	WGSEL	Wrapper group select It selects a particular group of signals from the SMMU wrapper hierarchy WGSEL = 0b00 - wrapper signal group 0 WGSEL = 0b01 - wrapper signal group 1 WGSEL = 0b10 - wrapper signal group 2 WGSEL = 0b11 - reserved
7:2	RESERVED_1	
1	SPDMBE	SPDM test enable Reset state : 0
0	TBE	Testbus enable, which governs whether the testbus is driven with all 0s or with the configured signals Reset state : 0

0x076FFEFC MDP4_1_SMMU_MDP1_VR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: 32'h0000_0000

Note that the DCPBP/DCPPP bits prevent the pipelining of the next transaction when the current transaction is a bypass/pass-through transaction. That is, they add one more cycle of delay between the current and next transactions.

Also note that when we are in global bypass (SMMU_CR[CLIENTPD]=1), these bits should have NO effect, or at least no effect between client transactions, they can have an effect between config and client transactions is appropriate. We must be able to continue to perform fully pipelined transactions when the client port is disabled altogether.

MDP4_1_SMMU_MDP1_VR0

Bits	Name	Description
31:3	RESERVED	

MDP4_1_SMMU_MDP1_VR0 (cont.)

Bits	Name	Description
2	DCPPT	Disable client pipelining for client operations in pass-through mode Reset state : 0
1	DCPBP	Disable client pipelining for client operations in bypass mode Reset state : 0
0	DCP	Disable client pipelining Reset state : 0

0x076FFF00 MDP4_1_SMMU_MDP1_TLBIALL

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries.

MDP4_1_SMMU_MDP1_TLBIALL

Bits	Name	Description
31:0	EXEC	Writing any value to this register invalidates all TLB entries, as specified by the contents of SMMU_CR[TLBIALLCFG]

0x076FFF04 MDP4_1_SMMU_MDP1_TLBIVMID

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries matching the IVMID value. Precise function is governed by SMMU_CR[TLBIALLCFG].

MDP4_1_SMMU_MDP1_TLBIVMID

Bits	Name	Description
31:5	RESERVED	
4:0	IVMID	Designates VMID[4:0] value of entries to be invalidated.

14.24.1.4 SMMU configuration registers

0x076FFF80 MDP4_1_SMMU_MDP1_CR

Type: Read/Write
Clock: AXI_BUS_CLOCK

Global configuration register.

MDP4_1_SMMU_MDP1_CR

Bits	Name	Description
31:10	RESERVED_2	
9	RESERVED_1	Reset state : 0
8	TLBIVMIDCFG	TLBIVMID configuration control. When set to 0,flash-invalidate, SMMU_TLBIVMID commands flash-invalidate the entire TLB, without regard to locking ,security and VMID value. When set to 1, selective, SMMU_TLBIVMID invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and VMID field matching the VMID specified by SMMU_TLBIVMID command. Reset state : X
7	TLBIALLCFG	TLBIALL configuration control. When set to 0, flash-invalidate, SMMU_TLBIALL commands flash-invalidate the entire TLB, without regard to locking and/or security. When set to 1, selective, SMMU_TLBIALL invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and are unlocked. Reset state : X
6	TLBLKCRWE	TLBLKCR write enable. When set to 0, writes to SMMU_CBn_TLBLKCR are ignored. When set to 1, allows operating environments to manage the TLB locking mechanism directly. Management amounst multiple operating environments must be coordinated externally between themselves. Reset state : X
5	STALLD	Global disable for stall mode. When set to 1, context bank stall modes are ignored and operate as terminate mode. Reset state : X
4	CLIENTPD	Client port disable. When set, all client accesses are forced to bypass the system MMU. There is no translation. access control, or attribute generation. This bit overrides individual SMMU_M2VCBRn[BYPASSD] settings; client requests are bypassed, even if SMMU_M2VCBRn[BYPASSD] is set to 1. Bypass request errors are not recorded in SMMU_ESR, nor reported to requesting masters. The SMMU_rpuErrIrptReq interrupt output signal is not asserted. Reset state : 1

MDP4_1_SMMU_MDP1_CR (cont.)

Bits	Name	Description
3	DCDEE	When set to 0, configuration port decode errors do not set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn are not updated. When set to 1, configuration port decode errors set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn updated with address and syndrome of error. Reset state : X
2	RPUEIE	When set, configuration port errors and client port bypass errors are reported directly to the interrupt controller via the SMMU_rputErrIrptReq interrupt output signal. Interrupt output is asserted if SMMU_CR[RPUIE_EN] is 1 and ANY bit is set in SMMU_ESR register. Reset state : 0
1	RPUERE	When set, SMMU reports configuration port errors and client port bypass errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via AXI port will use decode error, rather than slave error. Regardless of the value of this field both configuration port errors and client port bypass request errors are terminated by the SMMU as RAZ/WI, and are recorded in SMMU_ESR register. Reset state : X
0	RPUE	When set, all configuration port accesses are checked against SMMUX_RPU_ACR and/or the SMMUX_CBACRn registers for access permissions. Reset state : 0

14.24.1.5 SMMU error report registers

0x076FFF84 MDP4_1_SMMU_MDP1_EAR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: unknown

When there is an error, holds the physical address of the errant transaction.

MDP4_1_SMMU_MDP1_EAR

Bits	Name	Description
31:0	PA	Physical address[31:0]

0x076FFF88 MDP4_1_SMMU_MDP1_ESR

Type: Read/Write to clear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This register has read/write clear access. Reads return the value in the register, a write with a 1 set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

MDP4_1_SMMU_MDP1_ESR

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x076FFF8C MDP4_1_SMMU_MDP1_ESRRESTORE

Type: Write
Clock: RPM_BUS_CLK
Reset State: Undefined

This register is an aliased address for SMMU_ESR, but it allows direct write access. In this way, diagnostic software can cause an error to be generated and reported.

MDP4_1_SMMU_MDP1_ESRRESTORE

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	

MDP4_1_SMMU_MDP1_ESRRESTORE (cont.)

Bits	Name	Description
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x076FFF90 MDP4_1_SMMU_MDP1_ESYNR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

MDP4_1_SMMU_MDP1_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request
15:0	AMID	AMID[15:0] field of errant request

0x076FFF94 MDP4_1_SMMU_MDP1_ESYNR1

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

MDP4_1_SMMU_MDP1_ESYNR1

Bits	Name	Description
31	DCD	(decode) Indicates configuration port error due to invalid/unrecognized address (e.g., a reserved register address) Includes decode errors within both the global address space and the individual context bank address space

MDP4_1_SMMU_MDP1_ESYNR1 (cont.)

Bits	Name	Description
30	AC	(access control) Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO field of the errant request
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request)
15:12	ALEN	ALEN[3:0] field of the errant request
11	RESERVED_2	
10	ABURST	ABURST[1:0] field of the errant request
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request
7	AINST	AINST field of the errant request
6	APROTNS	APROTNS field of the errant request
5	APRIV	APRIV field of the errant request
4	AINNERSHARED	AINNERSHARED field of the errant request
3	ASHARED	ASHARED field of the errant request
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

14.24.1.6 SMMU revision register

0x076FFFF4 MDP4_1_SMMU_MDP1_REV

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the revision information for the SMMU core and wrapper.

MDP4_1_SMMU_MDP1_REV

Bits	Name	Description
31:12	RESERVED	

MDP4_1_SMMU_MDP1_REV (cont.)

Bits	Name	Description
11:8	WRAPPER	Wrapper version
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

14.24.1.7 SMMU implementation parameter register

0x076FFFF8 MDP4_1_SMMU_MDP1_IDR

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the parameter information for the SMMU core and wrapper

MDP4_1_SMMU_MDP1_IDR

Bits	Name	Description
31:24	NIRPT	NIRPT[7:0] Indicates number of context fault interrupt outputs (minus 1) supported by the System MMU Value can range from 0 - 255 (1 - 256 context fault interrupt outputs)
23:16	NCB	NCB[7:0] Indicates number of context banks (minus 1) supported by the System MMU Value can range from 0 - 254 (1 - 255 context banks)
15:12	TLBSIZE	TLBSIZE[3:0] Indicates log2(number of TLB entries) That is, number of TLB entries = 2 ** TLBSIZE
11	RESERVED	
10	HUM	Indicates whether or not TLB hit-under-miss behavior is supported
9	HTW	Indicates whether or not the System MMU supports hardware table walk If hardware table walk not supported (HTW=0), then software cannot set SMMU_CBn_ACTLR[TLBMCFG] to 0b10
8:0	NM2VCBMT	NM2VCBMT[8:0] Indicates number of M2VCBMT entries, with a maximum of 512 The bit width of the M2VCBMTIindex input (maximum value is 9) is equal to log base 2 of NM2VCBMT Allows for up to 7-bit MID field, plus NS-prot or other fields to select mapping [

0x076FFFFC MDP4_1_SMMU_MDP1_RPU_ACR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Using the incoming HVMID, this register controls access to the global register space.

MDP4_1_SMMU_MDP1_RPU_ACR

Bits	Name	Description
31:0	RWE	Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the entire block of registers within the SMMU's 4KB global address space, including this register itself. A VMID identified by this register is also permitted global access to all context banks. In practice, this register designates the VMID(s) that can act as SROT.

14.24.2 SMMU Context Bank Registers

There are a configurable number (1 to 9) of context banks in the SMMU. Each context bank consists of a set of registers in a unique 4KB address space.

14.24.2.1 SMMU context bank control registers

0x07600000+0x1000*n MDP4_1_SMMU_MDP1_CBn_SCTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank System Control Register controls various architected SMMU features

MDP4_1_SMMU_MDP1_CBn_SCTLR

Bits	Name	Description
31:5	RESERVED_2	
4	BE	Governs the order byte order or "endianness" of the page table entries. When set to 0, page table entries are in little endian format, so that their least significant byte is in byte 0 of the 32 bit entry. When set to 1, page table entries are in big endian format, so that their most significant byte is in byte 0 of the 32 bit entry.
3	RESERVED_1	Reserved for HAF, Hardware access flag. This bit governs whether the access flag is managed by hardware or software. The SMMU supports software access flag management only, so this bit is read-only and internally driven to 0.

MDP4_1_SMMU_MDP1_CBn_SCTLR (cont.)

Bits	Name	Description
2	AFE	Access flag enable. When AFE = 0, the access flag field is not supported and the AP[0] page table entry field acts as a bit of the overall AP[2:0] field to determining access permissions. When AFE = 1, the AP[0] page table entry field becomes the access flag, and the reduced number of access permission combinations is specified by AP2:1], and SMMU hardware will signal an Access Flag fault if a request targets a page for which the access flag is 0.
1	TRE	TEX remap enable. This bit governs the mapping of the page table entry TEX[2:0],C,B and SH fields into an SMMU TLB entry, and thus the translation of the AMEMTYPE[2:0], ASHARED and AINNERSHARED bus attributes. When TRE = 0, the TLB value is determined directly from the page table entry fields.
0	M	MMU enable bit. When set to 1, this context bank is enabled for translating requests. When set to 0, accesses bypass the TLB, and there is no address translation, access permission checking or attribute mapping. Incoming master requests are passed through unchanged.

0x07600004+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_ACTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank auxiliary control register controls various implementation specific features.

MDP4_1_SMMU_MDP1_CBn_ACTLR

Bits	Name	Description
31:19	RESERVED	
18	RESERVED_2	
17:16	V2PCFG	VA-to-PA configuration. Governs operation of VA-to-PA commands that miss in the TLB 0x0: terminate (Record TLB Miss context fault in SMMU_CBn_PAR) 0x1: software table update (Translate based on values in SMMU_CBn_TLBFLPTER and SMMU_CBn_TLBSLPTER) 0x2: hardware table walk (Translate based on value of PTE read from page table in memory) 0x3: reserved

MDP4_1_SMMU_MDP1_CBn_ACTLR (cont.)

Bits	Name	Description
15	TIPCF	Governs whether or not all subsequent requests using this context bank should be terminated if a prior context fault has occurred and has not yet been cleared from SMMU_CBn_FSR Accesses to other context banks proceed as normal 0x0: do not terminate (System MMU will attempt to process subsequent requests despite the presence of an existing context fault in SMMU_CBn_FSR. SMMU_CBn_FSR will be set if the subsequent access also encounters a context fault) 0x1: terminate (All subsequent accesses terminated by the System MMU as RAZ/WI, even if SMMU_CBn_ACTLR[TLBMCFG, CFCFG] configured for stall mode. SMMU_CBn_FSR set when access is terminated due to TIPCF = 1. Presence of SMMU_CBn_FSR when SMMU_CBn_ACTLR is 1 implies that the later exceptions must have been simply the forced terminations due to the prior context fault. Error optionally reported to the requesting master, according to the client port bus protocol, f SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus if SMMU_CBn_ACTLR is 1.)
14	CFCFG	(context fault configuration) Governs the behavior of all context faults except TLB miss TLB miss context faults are governed by SMMU_CBn_ACTLR[TLBMCFG] 0x0: terminate (Access terminates at the System MMU as RAZ/WI. Context fault exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x1: stall (Requesting master's access stalled while System MMU waits for managing processor to resolve context fault. Context fault exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode)

MDP4_1_SMMU_MDP1_CBn_ACTLR (cont.)

Bits	Name	Description
13:12	TLBMCFG	(TLB miss configuration) Governs the behavior of client accesses that miss in the TLB 0x0: pass-through (Access passed through to targeted slave without translation, attribute control, or access permission checking. Effectively, behavior is as if SMMU_CBn_SCTLR = 0 i.e., MMU disabled for this context bank. TLB miss not considered a context fault. TLB miss exception not recorded in SMMU_CBn_FSR. TLB miss exception not reported to requesting master. SMMU_contextFaultIrptReq interrupt output not asserted) 0x1: terminate (Access terminates at the System MMU as RAZ/WI,TLB miss exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x2: stall (Requesting master's access stalled while System MMU waits for managing processor to update TLB. TLB miss exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode) 0x3: HTW (Hardware table walk . Requesting master's access stalled while System MMU accesses page table. The is TLB updated and requesting master's access resumed after obtaining valid entry from page table. If translation fault, then access either terminates or stalls according to setting of SMMU_CBn_ACTLR)
11	DNLV2PA	(disable non-locking VA-to-PA allocation) Governs whether or not TLB misses due to non-locking VA-to-PA commands will allocate a new entry This field is ignored for locking VA-to-PA operations (SMMU_CBn_TLBLKCR[LKE] = 1)
10	DNA	(disable normal allocation) Governs whether or not TLB misses due to client port accesses will allocate a new entry
9:8	PRIVCFG	0x0: apriv (System MMU uses APRIV signal supplied by master as user/supervisor indicator 1 = supervisor) 0x1: reserved 0x2: User (System MMU ignores APRIV; treats all requests using this context bank as user) 0x3: Supervisor (System MMU ignores APRIV; treats all requests using this context bank as supervisor)

MDP4_1_SMMU_MDP1_CBn_ACTLR (cont.)

Bits	Name	Description
7:5	RESERVED_1	
4	RCNSH	(redirect cacheable-non-shareable) Governs whether or not cacheable accesses that are non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache, even though the locations are not being coherently shared with Scorpion-MP
3	RCISH	(redirect cacheable-inner-shareable) Governs whether or not cacheable accesses that are inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
2	RCOSH	(redirect cacheable-outer-shareable) Governs whether or not cacheable accesses that are outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
1	CFEIE	(context fault error interrupt enable) Governs whether or not client port request context faults are reported directly to the interrupt controller via the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus Interrupt output is asserted if SMMU_CBn_ACTLR[CFEIE] is 1 and any context fault bits are set in SMMU_CBn_FSR Such interrupts would generally be directed to the interrupt controller of whichever processor is currently managing this context bank of the System MMU Reset state : 0
0	CFERE	(context fault error report enable) Governs whether or not client port request context faults that are configured for terminate mode (or that are explicitly terminated after stall mode) are reported to the requesting master, according to the client port bus protocol All error types reported via AXI port will use decode error rather than slave error All context faults are recorded in SMMU_CBn_FSR, regardless of the value of this field.

0x07600008+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_CONTEXTIDR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context ID register holds the ASID associated with this context bank

MDP4_1_SMMU_MDP1_CBn_CONTEXTIDR

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Specifies the 8 bit ASID value assigned to this context bank. The ASID can be included in the key comparison of TLB entries. .

0x07600010+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_TTBR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR0 is used for low order virtual addresses, typically private pages for a given process.

MDP4_1_SMMU_MDP1_CBn_TTBR0

Bits	Name	Description
31:7	PA	BIts 31:7 of the physical address of the base of the page table. The actual LSB of the base address is bit 14-N, where N is set in register TTCR
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07600014+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_TTBR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR1 is used for high order virtual addresses, typically global pages for a given VMID, or kernal mappings.

The context bank auxiliary control register controls various implementation specific features.

MDP4_1_SMMU_MDP1_CBn_TTBR1

Bits	Name	Description
31:14	PA	BIts 31:14 of the physical address of the base of the page table.
13:7	RESERVED_2	
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED_1	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07600018+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_TTBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table control register, which specifies the size of the virtual address space that uses TTBR0.

MDP4_1_SMMU_MDP1_CBn_TTBCR

Bits	Name	Description
31:6	RESERVED_2	
5	PD1	Page disable 1; if this bit is set, hardware table walks attempting to use TTBR1will result in a first level descriptor translation fault. If clear, TTBR1 contents are used.
4	PD0	Page disable 0; if this bit is set, hardware table walks attempting to use TTBR0 will result in a first level descriptor translation fault. If clear, TTBR0 contents are used.
3	RESERVED_1	
2:0	N	N[2:0] specifies the number of upper order virtual address bits which must be 0 in order for translations to use the table pointed to by TTBR0. If any of these bits are non-zero, TTBR1 is used for the lookup. If N is 0, only TTBR0 is used.

0x0760001C+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_PAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The physical address register captures the physical address value resulting from the execution of a VA-to-PA command

Field definitions vary according to whether or not there is a context fault associated with the requested translation

MDP4_1_SMMU_MDP1_CBn_PAR

Bits	Name	Description
31:12	PAR_FAULT_INFO_312	
11	RESERVED_2	
10:9	PAR_FAULT_INFO_72	
8	RESERVED_1	
7:1	PAR_FAULT_INFO_71	Encoding varies according to value in FAULT field.
0	FAULT	(fault status) This field will be 1 when a context fault is associated with the requested translation, and 0, when there is no context fault associated with the requested translation.

0x07600020+0x1000*n MDP4_1_SMMU_MDP1_CBn_FSR, n=[0..1]

Type: Read/WriteClear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The Fault Status Register records status information for client accesses that encounter exceptions within the context bank, e.g. translation faults.This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data

This prevents inadvertent clearing of new faults when writing the register to clear an old fault

The presence of an asserted value on any bit in this register (except the SS bit) is what prompts the assertion (when enabled by SMMU_CBn_ACTLR[CFEIE]) of the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus

Therefore, these bits must be cleared by the interrupt handler

This is contrasted with the fields in the SMMU_CBn_FSYNRn registers, which are merely the "syndrome" of the fault indicated by SMMU_CBn_FSR

MDP4_1_SMMU_MDP1_CBn_FSR

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry

MDP4_1_SMMU_MDP1_CBn_FSR (cont.)

Bits	Name	Description
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07600024+0x1000*n MDP4_1_SMMU_MDP1_CBn_FSRRESTORE, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Allows SW to force a value into the SMMU_CBn_FSR register.

MDP4_1_SMMU_MDP1_CBn_FSRRESTORE

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)

MDP4_1_SMMU_MDP1_CBn_FSRRESTORE (cont.)

Bits	Name	Description
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07600028+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_FAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The Fault Address Register records the virtual address of client accesses that encounter exceptions within the context bank, e.g. translation faults. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

MDP4_1_SMMU_MDP1_CBn_FAR

Bits	Name	Description
31:0	VA	VA[31:0] of errant client access

0x0760002C+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_FSYNR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

NOTE omission of VMID field from this register, as VMID can only be made visible to SROT, and not to general OS software that manages the context bank registers

MDP4_1_SMMU_MDP1_CBn_FSYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] (ATID field of errant request)

MDP4_1_SMMU_MDP1_CBn_FSYNR0 (cont.)

Bits	Name	Description
23:16	RESERVED	
15:13	ABID	ABID[2:0] (ABID field of errant request)
12:8	APID	APID[4:0] (APID field of errant request)
7:0	AMID	AMID[7:0] (AMID field of errant request)

0x07600030+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_FSYNR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

MDP4_1_SMMU_MDP1_CBn_FSYNR1

Bits	Name	Description
31:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO (AOOO field of the errant request)
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request
15:12	ALEN	ALEN[3:0]field of the errant request
11	RESERVED_2	
10	ABURST	field of the errant request
9	RESERVED_1	
8	AWRITE	field of the errant request
7	AINST	field of the errant request
6	APROTNS	field of the errant request
5	APRIV	field of the errant request
4	AINNERSHARED	(AINNERSHARED field of the errant request)
3	ASHARED	(ASHARED field of the errant request)

MDP4_1_SMMU_MDP1_CBn_FSYNR1 (cont.)

Bits	Name	Description
2:0	AMEMTYPE	AMEMTYPE[2:0] (AMEMTYPE field of the errant request)

0x07600034+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_PRRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs memory type and shareability attributes of requests that are both MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1)

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) and/or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, memory type encoding is as follows:

0b00 = strongly-ordered

0b01 = device

0b10 = normal

0b11 = reserved

MDP4_1_SMMU_MDP1_CBn_PRRR

Bits	Name	Description
31	NOS7	not-outer-shareable class 7
30	NOS6	not-outer-shareable class 6
29	NOS5	not-outer-shareable class 5
28	NOS4	not-outer-shareable class 4
27	NOS3	not-outer-shareable class 3
26	NOS2	not-outer-shareable class 2
25	NOS1	not-outer-shareable class 1
24	NOS0	not-outer-shareable class 0
23:20	RESERVED	

MDP4_1_SMMU_MDP1_CBn_PRRR (cont.)

Bits	Name	Description
19	SHNMSH1	(shareable attribute for normal memory accesses with SH=1) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1
18	SHNMSH0	(shareable attribute for normal memory accesses with SH=0) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0
17	SHDSH1	SHDSH1 (shareable attribute for device accesses with SH=1) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1 [
16	SHDSH0	SHDSH0 (shareable attribute for device accesses with SH=0) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0 [
15:14	MTC7	MTC7[1:0] (memory type class 0)
13:12	MTC6	MTC6[1:0] (memory type class 0)
11:10	MTC5	MTC5[1:0] (memory type class 0)
9:8	MTC4	MTC4[1:0] (memory type class 0)
7:6	MTC3	MTC3[1:0] (memory type class 0)
5:4	MTC2	MTC2[1:0] (memory type class 0)
3:2	MTC1	MTC1[1:0] (memory type class 0)
1:0	MTC0	MTC0[1:0] (memory type class 0)

0x07600038+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_NMRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs the cache policy of MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1) requests for which the memory type is mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0) or the memory type is mapped to a type other than normal memory (SMMU_CBn_PRRR[MTCn] != 0b10)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, inner-cache and outer-cache policy encodings are as follows:

0b00 = non-cacheable

0b01 = cacheable, copy-back, write-allocate

0b10 = cacheable, write-through, write-no-allocate

0b11 = cacheable, copy-back, write-no-allocate

MDP4_1_SMMU_MDP1_CBn_NMRR

Bits	Name	Description
31:30	OCPC7	OCPC7[1:0] (inner-cache policy class 7)
29:28	OCPC6	OCPC6[1:0] (inner-cache policy class 6)
27:26	OCPC5	OCPC5[1:0] (inner-cache policy class 5)
25:24	OCPC4	OCPC4[1:0] (inner-cache policy class 4)
23:22	OCPC3	OCPC3[1:0] (inner-cache policy class 3)
21:20	OCPC2	OCPC2[1:0] (inner-cache policy class 2)
19:18	OCPC1	OCPC1[1:0] (inner-cache policy class 1)
17:16	OCPC0	OCPC0[1:0] (inner-cache policy class 0)
15:14	ICPC7	ICPC7[1:0] (inner-cache policy class 7)
13:12	ICPC6	ICPC6[1:0] (inner-cache policy class 6)
11:10	ICPC5	ICPC5[1:0] (inner-cache policy class 5)
9:8	ICPC4	ICPC4[1:0] (inner-cache policy class 4)
7:6	ICPC3	ICPC3[1:0] (inner-cache policy class 3)
5:4	ICPC2	ICPC2[1:0] (inner-cache policy class 2)
3:2	ICPC1	ICPC1[1:0] (inner-cache policy class 1)
1:0	ICPC0	ICPC0[1:0] (inner-cache policy class 0)

0x0760003C+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_TLBLKCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB lock control register governs the TLB locking mechanism and TLB invalidate operations.Write access to this register is governed by SMMU_CR[TLBLKCRWE]

When SMMU_CR[TLBLKCRWE] is 0, writes to SMMU_CBn_TLBLKCR are ignored

Read access is still permitted

SROT can set SMMU_CR[TLBLKCRWE] to 1 to allow operating environment(s) to manage the TLB locking mechanism

Management amongst multiple operating environments must be coordinated via semaphore

MDP4_1_SMMU_MDP1_CBn_TLBLKCR

Bits	Name	Description
31:24	RESERVED_2	
23:16	VICTIM	VICTIM[7:0] Indicates the TLB index at which the next normal (non-locking) allocation will occur Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context
15:8	FLOOR	FLOOR[7:0] Indicates the TLB index from which round-robin replacement on normal (non-locking) allocations occurs TLB entries at indices below this value are locked Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context banks
7:4	RESERVED_1	
3	TLBIVAACFG	(TLBIVAA configuration) TLBIVAACFG = 0 - flash-invalidate SMMU_CBn_TLBIVAA commands flash-invalidate the entire TLB, without regard to locking, security, address, and/or VMID value TLBIVAACFG = 1 - selective SMMU_CBn_TLBIVAA commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank VA field of TLB entry matches VA designated by SMMU_CBn_TLBIVAA command NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked

MDP4_1_SMMU_MDP1_CBn_TLBLKCR (cont.)

Bits	Name	Description
2	TLBIASIDCFG	(TLBIASID configuration) TLBIASIDCFG = 0 - flash-invalidate SMMU_CBn_TLBIASID commands flash-invalidate the entire TLB, without regard to locking, security, VMID, and/or ASID values TLBIASIDCFG = 1 - selective SMMU_CBn_TLBIASID commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command TLB entry is not global (NG field is 1) NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
1	TLBIALLCFG	(TLBIALL configuration) TLBIALLCFG = 0 - flash-invalidate SMMU_CBn_TLBIALL commands flash-invalidate the entire TLB, without regard to locking, security, and/or VMID value TLBIALLCFG = 1 - selective SMMU_CBn_TLBIALL commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked
0	LKE	(lock enable) Governs whether or not TLB entries established by VA-to-PA commands upon TLB misses are locked LKE = 0 (normal, non-locking) Allocate VA-to-PA TLB entry (if TLB miss) at the index specified by SMMU_CBn_TLBLKCR[VICTIM] Allocation is disabled if SMMU_CBn_ACTLR[DNLV2PA] is 1 Increment SMMU_CBn_TLBLKCR[VICTIM] by 1 (only if new entry allocated) Wrap back to the value of SMMU_CBn_TLBLKCR[FLOOR] when the last entry is written LKE = 1 (locking) Search TLB for specified VA and invalidate if found Provides atomicity between the invalidate and the new allocation within the locked region Allocate VA-to-PA TLB entry at the index specified by data operand bits 7:0 of the VA-to-PA command This value must be less than SMMU_CBn_TLBLKCR[FLOOR] in order for it to remain locked Allocation occurs even if non-locking allocation is disabled due to SMMU_CBn_ACTLR[DNLV2PA] = 1

0x07600040+0x1000*n MDP4_1_SMMU_MDP1_CBn_V2PSR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The VA-to-PA status register records the hit/miss status and TLB index or V2Pxx and TLB invalidate commands.

MDP4_1_SMMU_MDP1_CBn_V2PSR

Bits	Name	Description
31:16	RESERVED_2	
15:8	INDEX	INDEX[7:0] Indicates the index of the TLB entry associated with the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command If SMMU_CBn_V2PSR[HIT] is 0, then SMMU_CBn_V2PSR[INDEX] is the index to which the entry was allocated (if allocated at all) If SMMU_CBn_V2PSR[HIT] is 1, then SMMU_CBn_V2PSR[INDEX] is the index of the entry which hit
7:1	RESERVED_1	
0	HIT	Indicates whether or not there was a TLB hit (prior to allocation, if any) on the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command

0x07600044+0x1000*n MDP4_1_SMMU_MDP1_CBn_TLBFLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB first level PTE register holds the first level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

This register (together with SMMU_CBn_TLBSLPTER) is used as the source of the translation information for VA-to-PA operations when the MMU is enabled (SMMU_CBn_SCTLR[M] = 1) and the operations are configured for software table update (SMMU_CBn_ACTLR[V2PCFG] = 0b01)

Field definitions vary according to the type of PTE (fault, page, section, or supersection), and come directly from the ARMv7 architecture's PTE formats

MDP4_1_SMMU_MDP1_CBn_TLBFLPTER

Bits	Name	Description
31:10	FL_PTE_HI	

MDP4_1_SMMU_MDP1_CBn_TLBFLPTER (cont.)

Bits	Name	Description
9:5	RESERVED	
4:2	FL_PTE_LO	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	This field should be set to 0b00 or 0b11 to indicate that the translation should result in a context fault, and the rest of the fields are defined as indicated in this section If this field is not 0b00 or 0b11, then the PTE is of some other type (see other sections for the field definitions for those types)

0x07600048+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_TLBSLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB second level PTE register holds the second level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

Field definitions vary according to the type of PTE (fault, 64KB or 4KB), and come directly from the ARMv7 architecture's PTE format

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MDP4_1_SMMU_MDP1_CBn_TLBSLPTER

Bits	Name	Description
31:2	SL_PTE	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	0x0: fault

0x0760004C+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_BFBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The burst fetch buffer configuration register governs the operation of the "burst fill" feature of the SMMU.

MDP4_1_SMMU_MDP1_CBn_BFBCR

Bits	Name	Description
31:12	STRIDE	(stride amount) 4KB-aligned value to be added to virtual address on demand TLB miss for filling subsequent BFB Stride of minimum 4KB alignment useful for preventing stride burst fetch until final PTE of the demand BFB entry is used
11:8	SLVIC	(second-level victim) Indicates the SLBFB index at which the next round-robin allocation will occur
7:4	FLVIC	(first-level victim) Indicates the FLBFB index at which the next round-robin allocation will occur
3	RESERVED	
2	SFVS	(stride-fetch victim selection) SFVS. = 0 (replace normal round-robin victim-selected entry) Useful when stride is larger than the VA space represented by the four PTEs in the demand BFB entry, but the client access pattern is for more than just the initial PTE in that demand BFB entry SFVS. = 1 (replace same BFB used by demand VA for which the stride burst is being performed) Useful when stride is the same as the VA space represented by an individual PTE in the demand BFB entry (such that the stride won't miss against the BFB until the last PTE of the demand BFB entry is accessed), and/or when the client access pattern only uses the initial PTE in the demand BFB entry
1	BFBSFE	(burst fetch buffer stride fetch enable) Enables stride burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Stride burst fetch is for the block of four PTEs associated with VA+stride VA is the "demanded" VA from the client (or VA-to-PA command) Stride value is specified by SMMU_CBn_BFBCR[STRIDE] Stride burst fetch only occurs if demand access for VA misses in TLB (could hit in BFB) and address VA+stride misses in both TLB and BFB
0	BFBDFE	(burst fetch buffer demand fetch enable) Enables demand burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Demand burst fetch is for the block of four PTEs associated with the "demanded" VA from the client (or VA-to-PA command) Demand burst fetch only occurs if demand access misses in both TLB and BFB

0x07600800+0x1000*n MDP4_1_SMMU_MDP1_CBn_TLBIALL, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate all command register invalidates all TLB entries matching the VMID associated with this context bank. Data operand is ignored.

MDP4_1_SMMU_MDP1_CBn_TLBIALL

Bits	Name	Description
31:0	RESERVED	

0x07600804+0x1000*n MDP4_1_SMMU_MDP1_CBn_TLBIASID, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by ASID command register invalidates TLB entries matching the specified ASID and matching the VMID associated with this context bank.Invalidates TLB entries which are associated with the designated ASID and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIASIDCFG] governs whether command flash-invalidates entire TLB array or just the entries matching the VMID, ASID, and security state

TLBIASIDCFG = 0 - flash-invalidate

SMMU_CBn_TLBIASID command flash-invalidates the entire TLB, without regard to locking, security, VMID, and/or ASID values

TLBIASIDCFG = 1 - selective

SMMU_CBn_TLBIASID command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command data operand

TLB entry is not global (NG field is 1)

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command

Locking is not considered (matching entries are invalidated even if locked)

ASID field of command specifies the ASID value of the TLB entries to be invalidated

MDP4_1_SMMU_MDP1_CBn_TLBIASID

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Actual ASID value

0x07600808+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_TLBIVA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA command invalidates TLB entries matching the designated VA, ASID and the VMID associated with this context bank.

Matching entry determined as follows:

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIVA command data operand (or TLB entry is global - NG field is 0)

VA field of TLB entry matches VA value designated by the SMMU_CBn_TLBIVA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIVA command

Locking is not considered (matching entry is invalidated even if locked)

Data operand specifies the VA and ASID value of the TLB entry to be invalidated

MDP4_1_SMMU_MDP1_CBn_TLBIVA

Bits	Name	Description
31:12	VA	VA[31:12]
11:8	RESERVED	
7:0	ASID	ASID[7:0] value

0x0760080C+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_TLBIVAA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA all ASIDS command invalidates TLB entries matching the designated VA and the VMID associated with this context bank, regardless of ASID.Invalidates TLB entries which are associated with the designated VA, regardless of ASID, and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIVAACFG] governs whether command flash-invalidates entire TLB array or just the non-locked entries matching the VMID, ASID, and security state

TLBIVAACFG = 0 - flash-invalidate

SMMU_CBn_TLBIVAA command flash-invalidates the entire TLB, without regard to locking, security, address, and/or VMID value

TLBIVAACFG = 1 - selective

SMMU_CBn_TLBIVAA command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

VA field of TLB entry matches VA designated by the SMMU_CBn_TLBIVAA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command

Entry is unlocked

MDP4_1_SMMU_MDP1_CBn_TLBIVAA

Bits	Name	Description
31:12	VA	VA[31:12]
11:0	RESERVED	

0x07600810+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_V2PRR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

MDP4_1_SMMU_MDP1_CBn_V2PRR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07600814+0x1000*n MDP4_1_SMMU_MDP1_CBn_V2PPW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

MDP4_1_SMMU_MDP1_CBn_V2PPW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07600818+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_V2PUR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

MDP4_1_SMMU_MDP1_CBn_V2PUR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x0760081C+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_V2PUW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

.Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

MDP4_1_SMMU_MDP1_CBn_V2PUW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	

MDP4_1_SMMU_MDP1_CBn_V2PUW (cont.)

Bits	Name	Description
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07600820+ 0x1000*n MDP4_1_SMMU_MDP1_CBn_RESUME, n=[0..1]

Type: Write/command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB resume command causes the SMMU to resume operation after a stalled access..

MDP4_1_SMMU_MDP1_CBn_RESUME

Bits	Name	Description
31:1	RESERVED	
0	TNR	Terminate/not retry When TNR is written as 0, indicates that the stalled access should be retried by the system MMU. When written as 1, indicates that this stalled transaction is terminated by the system MMU. The error is optionally reported to the requesting master, using the client port bus protocol, if SMMU_CNn_ACTLR[CFERE] == 1. Interrupt optionally remains asserted via SMMU_M2VCBRn[IRPTINDX] selected SMMU_contextFaultIrptReq bit, only if SMMU_CBn_ACTLR[CFEIE] is 1, and only if SMMU_CBn_FSR has not been cleared by software priori to issuing this command..

14.25 Rotator SMMU Registers (0x07700000 SMMU_ROTATOR_BASE)

This section contains the Rotator SMMU registers.

14.25.1 SMMU Global Registers

14.25.1.1 SMMU VMID/CBNDX mapping registers

0x077FF000+ 0x4*n ROT_SMMU_ROT_M2VCBRn, n=[0..1]

Type: Read/Write
Clock: AXI_CLK
Reset State: Undefined

SMMU_M2VCBRm registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

ROT_SMMU_ROT_M2VCBRn

Bits	Name	Description
31:28	RESERVED_2	
27:25	BPMEMTYPE	(bypass memory type) Supplies the AMEMTYPE attributes for client requests which bypass the System MMU when SMMU_M2VCBRn[BPMTCFG] = 1 See reference section for AMEMTYPE encoding definitions
24	BPMTCFG	(bypass memory type configuration) Governs the memory type (AMEMTYPE) attributes of client requests which bypass the System MMU BPMTCFG = 0 - use AMEMTYPE Bypass requests use AMEMTYPE signal supplied by client master BPMTCFG = 1 - use SMMU_M2VCBRn[BPMEMTYPE] Bypass requests use SMMU_M2VCBRn[BPMEMTYPE] Reset state : 0
23:22	NSCFG	(non-secure configuration) Governs the incoming security designation of client requests NSCFG = 0b00 - use APROTNS Use APROTNS signal supplied by client master NSCFG = 0b01 - reserved NSCFG = 0b10 - secure System MMU ignores APROTNS; treats all requests as secure NSCFG = 0b11 - non-secure System MMU ignores APROTNS; treats all requests as non-secure Reset state : 0

ROT_SMMU_ROT_M2VCBRn (cont.)

Bits	Name	Description
21:20	BPSHCFG	(bypass shareability configuration) Governs the shareability realm (ASHARED and AINNERSHARED) attributes of client requests which bypass the System MMU BPSHCFG = 0b00 - use ASHARED and AINNERSHARED Bypass requests use ASHARED and AINNERSHARED signals supplied by client master BPSHCFG = 0b01 - outer-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 0 BPSHCFG = 0b10 - inner-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 1 BPSHCFG = 0b11 - non-shareable Bypass requests set ASHARED = 0, AINNERSHARED = 0 Reset state : 0
19	BPRCNSH	(bypass redirect cacheable-non-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache Reset state : 0
18	BPRCISH	(bypass redirect cacheable-inner-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0
17	BPRCOSH	(bypass redirect cacheable-outer-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0

ROT_SMMU_ROT_M2VCBRn (cont.)

Bits	Name	Description
16	BYPASSD	Bypass disable for this index Governs whether or not client port accesses using this mapping table entry are actually permitted to "bypass" the System MMU when such bypass is indicated (either due to CBNDX = 255 or due to the master asserting the "SMMU bypass" input) This field is ignored (and operates as if it were 0) if SMMU_CR[CLIENTPD] is 1 BYPASSD = 0 - bypass enabled Bypass requests truly bypass the System MMU and "pass-through" to the fabric (no translation, access control, or attribute generation) No cycle of latency for System MMU context bank access Bypass request not considered an error Bypass request error not recorded in SMMU_ESR[BYPASS] Bypass error not reported to requesting master SMMU_rpuErrIrptReq interrupt output not asserted Client accesses still reference M2VCBMT to get VMID value for presentation to fabric BYPASSD = 1 - bypass disabled System MMU terminates the access as RAZ/WI Bypass request is considered an error Bypass request error is recorded in SMMU_ESR[BYPASS] If SMMU_CR[RPUERE] is 1, then bypass error reported to requesting master according to the client port bus protocol If SMMU_CR[RPUEIE] is 1, then SMMU_rpuErrIrptReq interrupt output asserted
15:8	CBNDX	Context bank index Context bank index associated with the M2VCBMT index CBNDX = 255 indicates no context bank assigned ("bypass")
7:5	RESERVED_1	
4:0	VMID	Virtual machine ID VMID value associated with the M2VCBMT index Must be programmed consistently with the SMMU_CBACRn[CBVMID] field for the context bank designated by SMMU_M2VCBRm[CBNDX]

14.25.1.2 SMMU context bank access control registers

0x077FF800+ 0x4*n ROT_SMMU_ROT_CBACRn, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs configuration port access to the associated context bank registers.

ROT_SMMU_ROT_CBACRn

Bits	Name	Description
31:24	IRPTNDX	(interrupt index) Interrupt output number used for context faults associated with this context bank (use SMMU_contextFaultIrptReq[IRPTNDX])
23:21	RESERVED	
20:16	CBVMID	(context bank VMID) Specifies the VMID with which the client masters using the context bank are associated Must be programmed consistently with the M2VCBMT entries that are configured to use the associated context bank This field is used by configuration port commands that need the context bank's VMID value in order to access the TLB (e.g., SMMU_CBn_TLBIVMID, SMMU_CBn_V2Pxx)
15:10	RESERVED_2	
9	RWGE	Read/write global enable. Setting this bit allows access to the context bank registers from any VMID
8	RWE	Read/write enable. Indicates that the RWVMID field is valid.
7:5	RESERVED_1	
4:0	RWVMID	Specifies owner VMID with full read/write access to the registers in the associated context bank "n".

14.25.1.3 SMMU TLB software access registers

0x077FFE00 ROT_SMMU_ROT_TLBRSW

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Writing to this address requests that the TLB entry at INDEX be read into the SMMU_TLBTRn registers

ROT_SMMU_ROT_TLBRSW

Bits	Name	Description
31:10	RESERVED	
9:8	TLBBFBS	This field selects the TLB, TFBFB, SLBFB 0x0: Selecting TLB 0x1: Not defined 0x2: Selecting FL BFB 0x3: Selecting SL BFB

ROT_SMMU_ROT_TLBRSW (cont.)

Bits	Name	Description
7:0	INDEX	TLB index to be read.

0x077FFE80 ROT_SMMU_ROT_TLBTR0

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

This register holds part of TLB entry read by the last TLBRSW command.

ROT_SMMU_ROT_TLBTR0

Bits	Name	Description
31:23	RESERVED_4	
22:20	DPSIZC	3 bit decode page size field from CAM-side of TLB CAM-RAM) Same determination and encoding as for DPSIZR The CAM-side copy of this field is used for hit/miss determination in the TLB CAM array
19	RESERVED_3	
18:16	DPSIZR	(3 bit decode page size field from RAM-side of TLB CAM-RAM) Determined from the size fields of the page table entry Encodes the page size as follows: all other values reserved/unused The RAM-side copy of this field is used for virtual ’ physical address formation 0x0: 4KB page 0x1: 64KB page 0x3: 1MB page 0x7: 16MB page
15:12	RESERVED_2	
11	MT2	(memory type bit 2) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[2] attribute bus on the request output of the System MMU

ROT_SMMU_ROT_TLBTR0 (cont.)

Bits	Name	Description
10	MT1	(memory type bit 1) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[1] attribute bus on the request output of the System MMU
9	MT0	(memory type bit 0) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[0] attribute bus on the request output of the System MMU
8	SH	(shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's outer-shareable realm This field becomes the ASHARED attribute on the request output of the System MMU
7	ISH	(inner-shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's inner-shareable realm This field becomes the AINNERSHARED attribute on the request output of the System MMU
6	NSDESC	(non-secure descriptor) This TLB entry field is a modified version of the corresponding bit of the page table entry Qualified by the NS-prot attribute of the incoming request which prompted the allocation of the TLB entry, such that if the incoming NS-prot attribute was 1 (non-secure), then the NS-desc field of the page table entry was ignored, and the NS-desc field of the TLB entry was forced to 1 Indicates whether the associated memory page contains secure (NS-desc=0) or non-secure (NS-desc=1) information This field becomes the NS-prot attribute on the request output of the System MMU
5	RESERVED_1	

ROT_SMMU_ROT_TLBTR0 (cont.)

Bits	Name	Description
4	XN	(execute never permission) This TLB entry field comes directly from the corresponding bit of the page table entry
3	UW	(user write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
2	UR	(user read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
1	PW	(privileged write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
0	PR	(privileged read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]

0x077FFE84 ROT_SMMU_ROT_TLBTR1

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

ROT_SMMU_ROT_TLBTR1

Bits	Name	Description
31:12	PA	Physical address [31:12] field of the TLB entry
11:5	RESERVED	
4:0	VMID	VMID [4:0]field of the TLB entry)

0x077FFE88 ROT_SMMU_ROT_TLBTR2

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

ROT_SMMU_ROT_TLBTR2

Bits	Name	Description
31:12	VA	virtual address field [31:12] of the TLB entry
11	RESERVED	
10	NG	(not global field from page table entry) Indicates whether the page is private to the specified ASID (NG=1) or global to all ASIDs within the VMID using this context bank (NG=0)
9	NSTID	(non-secure tag ID field of the TLB entry) Indicates whether the TLB entry belongs to the secure world (NSTID=0) or the non-secure world (NSTID=1) This field is comned against the incoming NS-prot attribute of the master request as part of TLB hit/miss determination
8	V	valid field of the TLB entry
7:0	ASID	ASID[7:0] field of the TLB entry

0x077FFE8C ROT_SMMU_ROT_TESTBUSCR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

Governs which signals (if any) from the system SMMU core or wrapper design hierarchy are sent out to the system via a testbus for diagnostic, and also to the system profiling and diagnostic monitor(SPDM).

ROT_SMMU_ROT_TESTBUSCR

Bits	Name	Description
31:28	SPDM3SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[3]
27:24	SPDM2SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[2]
23:20	SPDM1SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[1]
19:16	SPDM0SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[0]
15:14	TBHSEL	Testbus highselect It governs which set of signals are to testbus[31:16] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL

ROT_SMMU_ROT_TESTBUSCR (cont.)

Bits	Name	Description
13:12	TBSLSEL	Testbus low select It governs which set of signals are to testbus[15:0] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL
11:10	RESERVED_2	
9:8	WGSEL	Wrapper group select It selects a particular group of signals from the SMMU wrapper hierarchy WGSEL = 0b00 - wrapper signal group 0 WGSEL = 0b01 - wrapper signal group 1 WGSEL = 0b10 - wrapper signal group 2 WGSEL = 0b11 - reserved
7:2	RESERVED_1	
1	SPDMBE	SPDM test enable Reset state : 0
0	TBE	Testbus enable, which governs whether the testbus is driven with all 0s or with the configured signals Reset state : 0

0x077FFEFC ROT_SMMU_ROT_VR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: 32'h0000_0000

Note that the DCPBP/DCPPP bits prevent the pipelining of the next transaction when the current transaction is a bypass/pass-through transaction. That is, they add one more cycle of delay between the current and next transactions.

Also note that when we are in global bypass (SMMU_CR[CLIENTPD]=1), these bits should have NO effect, or at least no effect between client transactions, they can have an effect between config and client transactions is appropriate. We must be able to continue to perform fully pipelined transactions when the client port is disabled altogether.

ROT_SMMU_ROT_VR0

Bits	Name	Description
31:3	RESERVED	

ROT_SMMU_ROT_VR0 (cont.)

Bits	Name	Description
2	DCPPT	Disable client pipelining for client operations in pass-through mode Reset state : 0
1	DCPBP	Disable client pipelining for client operations in bypass mode Reset state : 0
0	DCP	Disable client pipelining Reset state : 0

0x077FFF00 ROT_SMMU_ROT_TLBIALL

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries.

ROT_SMMU_ROT_TLBIALL

Bits	Name	Description
31:0	EXEC	Writing any value to this register invalidates all TLB entries, as specified by the contents of SMMU_CR[TLBIALLCFG]

0x077FFF04 ROT_SMMU_ROT_TLBIVMID

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries matching the IVMID value. Precise function is governed by SMMU_CR[TLBIALLCFG].

ROT_SMMU_ROT_TLBIVMID

Bits	Name	Description
31:5	RESERVED	
4:0	IVMID	Designates VMID[4:0] value of entries to be invalidated.

14.25.1.4 SMMU configuration registers

0x077FFF80 ROT_SMMU_ROT_CR

Type: Read/Write
Clock: AXI_BUS_CLOCK

Global configuration register.

ROT_SMMU_ROT_CR

Bits	Name	Description
31:10	RESERVED_2	
9	RESERVED_1	Reset state : 0
8	TLBIVMIDCFG	TLBIVMID configuration control. When set to 0,flash-invalidate, SMMU_TLBIVMID commands flash-invalidate the entire TLB, without regard to locking ,security and VMID value. When set to 1, selective, SMMU_TLBIVMID invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and VMID field matching the VMID specified by SMMU_TLBIVMID command. Reset state : X
7	TLBIALLCFG	TLBIALL configuration control. When set to 0, flash-invalidate, SMMU_TLBIALL commands flash-invalidate the entire TLB, without regard to locking and/or security. When set to 1, selective, SMMU_TLBIALL invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and are unlocked. Reset state : X
6	TLBLKCRWE	TLBLKCR write enable. When set to 0, writes to SMMU_CBn_TLBLKCR are ignored. When set to 1, allows operating environments to manage the TLB locking mechanism directly. Management amounst multiple operating environments must be coordinated externally between themselves. Reset state : X
5	STALLD	Global disable for stall mode. When set to 1, context bank stall modes are ignored and operate as terminate mode. Reset state : X
4	CLIENTPD	Client port disable. When set, all client accesses are forced to bypass the system MMU. There is no translation. access control, or attribute generation. This bit overrides individual SMMU_M2VCBRn[BYPASSD] settings; client requests are bypassed, even if SMMU_M2VCBRn[BYPASSD] is set to 1. Bypass request errors are not recorded in SMMU_ESR, nor reported to requesting masters. The SMMU_rpuErrIrptReq interrupt output signal is not asserted. Reset state : 1

ROT_SMMU_ROT_CR (cont.)

Bits	Name	Description
3	DCDEE	When set to 0, configuration port decode errors do not set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn are not updated. When set to 1, configuration port decode errors set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn updated with address and syndrome of error. Reset state : X
2	RPUEIE	When set, configuration port errors and client port bypass errors are reported directly to the interrupt controller via the SMMU_rputErrIrptReq interrupt output signal. Interrupt output is asserted if SMMU_CR[RPUIE_EN] is 1 and ANY bit is set in SMMU_ESR register. Reset state : 0
1	RPUERE	When set, SMMU reports configuration port errors and client port bypass errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via AXI port will use decode error, rather than slave error. Regardless of the value of this field both configuration port errors and client port bypass request errors are terminated by the SMMU as RAZ/WI, and are recorded in SMMU_ESR register. Reset state : X
0	RPUE	When set, all configuration port accesses are checked against SMMUX_RPU_ACR and/or the SMMUX_CBACRn registers for access permissions. Reset state : 0

14.25.1.5 SMMU error report registers

0x077FFF84 ROT_SMMU_ROT_EAR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: unknown

When there is an error, holds the physical address of the errant transaction.

ROT_SMMU_ROT_EAR

Bits	Name	Description
31:0	PA	Physical address[31:0]

0x077FFF88 ROT_SMMU_ROT_ESR

Type: Read/Write to clear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This register has read/write clear access. Reads return the value in the register, a write with a 1 set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

ROT_SMMU_ROT_ESR

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x077FFF8C ROT_SMMU_ROT_ESRRESTORE

Type: Write
Clock: RPM_BUS_CLK
Reset State: Undefined

This register is an aliased address for SMMU_ESR, but it allows direct write access. In this way, diagnostic software can cause an error to be generated and reported.

ROT_SMMU_ROT_ESRRESTORE

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	

ROT_SMMU_ROT_ESRRESTORE (cont.)

Bits	Name	Description
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x077FFF90 ROT_SMMU_ROT_ESYNR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

ROT_SMMU_ROT_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request
15:0	AMID	AMID[15:0] field of errant request

0x077FFF94 ROT_SMMU_ROT_ESYNR1

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

ROT_SMMU_ROT_ESYNR1

Bits	Name	Description
31	DCD	(decode) Indicates configuration port error due to invalid/unrecognized address (e.g., a reserved register address) Includes decode errors within both the global address space and the individual context bank address space

ROT_SMMU_ROT_ESYNR1 (cont.)

Bits	Name	Description
30	AC	(access control) Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO field of the errant request
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request)
15:12	ALEN	ALEN[3:0] field of the errant request
11	RESERVED_2	
10	ABURST	ABURST[1:0] field of the errant request
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request
7	AINST	AINST field of the errant request
6	APROTNS	APROTNS field of the errant request
5	APRIV	APRIV field of the errant request
4	AINNERSHARED	AINNERSHARED field of the errant request
3	ASHARED	ASHARED field of the errant request
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

14.25.1.6 SMMU revision register

0x077FFFF4 ROT_SMMU_ROT_REV

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the revision information for the SMMU core and wrapper.

ROT_SMMU_ROT_REV

Bits	Name	Description
31:12	RESERVED	

ROT_SMMU_ROT_REV (cont.)

Bits	Name	Description
11:8	WRAPPER	Wrapper version
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

14.25.1.7 SMMU implementation parameter register

0x077FFFF8 ROT_SMMU_ROT_IDR

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the parameter information for the SMMU core and wrapper

ROT_SMMU_ROT_IDR

Bits	Name	Description
31:24	NIRPT	NIRPT[7:0] Indicates number of context fault interrupt outputs (minus 1) supported by the System MMU Value can range from 0 - 255 (1 - 256 context fault interrupt outputs)
23:16	NCB	NCB[7:0] Indicates number of context banks (minus 1) supported by the System MMU Value can range from 0 - 254 (1 - 255 context banks)
15:12	TLBSIZE	TLBSIZE[3:0] Indicates log2(number of TLB entries) That is, number of TLB entries = 2 ** TLBSIZE
11	RESERVED	
10	HUM	Indicates whether or not TLB hit-under-miss behavior is supported
9	HTW	Indicates whether or not the System MMU supports hardware table walk If hardware table walk not supported (HTW=0), then software cannot set SMMU_CBn_ACTLR[TLBMCFG] to 0b10
8:0	NM2VCBMT	NM2VCBMT[8:0] Indicates number of M2VCBMT entries, with a maximum of 512 The bit width of the M2VCBMTIindex input (maximum value is 9) is equal to log base 2 of NM2VCBMT Allows for up to 7-bit MID field, plus NS-prot or other fields to select mapping [

0x077FFFFC ROT_SMMU_ROT_RPU_ACR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Using the incoming HVMID, this register controls access to the global register space.

ROT_SMMU_ROT_RPU_ACR

Bits	Name	Description
31:0	RWE	Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the entire block of registers within the SMMU's 4KB global address space, including this register itself. A VMID identified by this register is also permitted global access to all context banks. In practice, this register designates the VMID(s) that can act as SROT.

14.25.2 SMMU Context Bank Registers

There are a configurable number (1 to 9) of context banks in the SMMU. Each context bank consists of a set of registers in a unique 4KB address space.

14.25.2.1 SMMU context bank control registers

0x07700000+0x1000*n ROT_SMMU_ROT_CBn_SCTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank System Control Register controls various architected SMMU features

ROT_SMMU_ROT_CBn_SCTLR

Bits	Name	Description
31:5	RESERVED_2	
4	BE	Governs the order byte order or "endianness" of the page table entries. When set to 0, page table entries are in little endian format, so that their least significant byte is in byte 0 of the 32 bit entry. When set to 1, page table entries are in big endian format, so that their most significant byte is in byte 0 of the 32 bit entry.
3	RESERVED_1	Reserved for HAF, Hardware access flag. This bit governs whether the access flag is managed by hardware or software. The SMMU supports software access flag management only, so this bit is read-only and internally driven to 0.

ROT_SMMU_ROT_CBn_SCTLR (cont.)

Bits	Name	Description
2	AFE	Access flag enable. When AFE = 0, the access flag field is not supported and the AP[0] page table entry field acts as a bit of the overall AP[2:0] field to determining access permissions. When AFE = 1, the AP[0] page table entry field becomes the access flag, and the reduced number of access permission combinations is specified by AP2:1], and SMMU hardware will signal an Access Flag fault if a request targets a page for which the access flag is 0.
1	TRE	TEX remap enable. This bit governs the mapping of the page table entry TEX[2:0],C,B and SH fields into an SMMU TLB entry, and thus the translation of the AMEMTYPE[2:0], ASHARED and AINNERSHARED bus attributes. When TRE = 0, the TLB value is determined directly from the page table entry fields.
0	M	MMU enable bit. When set to 1, this context bank is enabled for translating requests. When set to 0, accesses bypass the TLB, and there is no address translation, access permission checking or attribute mapping. Incoming master requests are passed through unchanged.

0x07700004+ 0x1000*n ROT_SMMU_ROT_CBn_ACTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank auxiliary control register controls various implementation specific features.

ROT_SMMU_ROT_CBn_ACTLR

Bits	Name	Description
31:19	RESERVED	
18	RESERVED_2	
17:16	V2PCFG	VA-to-PA configuration. Governs operation of VA-to-PA commands that miss in the TLB 0x0: terminate (Record TLB Miss context fault in SMMU_CBn_PAR) 0x1: software table update (Translate based on values in SMMU_CBn_TLBFLPTER and SMMU_CBn_TLBSLPTER) 0x2: hardware table walk (Translate based on value of PTE read from page table in memory) 0x3: reserved

ROT_SMMU_ROT_CBn_ACTLR (cont.)

Bits	Name	Description
15	TIPCF	Governs whether or not all subsequent requests using this context bank should be terminated if a prior context fault has occurred and has not yet been cleared from SMMU_CBn_FSR Accesses to other context banks proceed as normal 0x0: do not terminate (System MMU will attempt to process subsequent requests despite the presence of an existing context fault in SMMU_CBn_FSR. SMMU_CBn_FSR will be set if the subsequent access also encounters a context fault) 0x1: terminate (All subsequent accesses terminated by the System MMU as RAZ/WI, even if SMMU_CBn_ACTLR[TLBMCFG, CFCFG] configured for stall mode. SMMU_CBn_FSR set when access is terminated due to TIPCF = 1. Presence of SMMU_CBn_FSR when SMMU_CBn_ACTLR is 1 implies that the later exceptions must have been simply the forced terminations due to the prior context fault. Error optionally reported to the requesting master, according to the client port bus protocol, f SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus if SMMU_CBn_ACTLR is 1.)
14	CFCFG	(context fault configuration) Governs the behavior of all context faults except TLB miss TLB miss context faults are governed by SMMU_CBn_ACTLR[TLBMCFG] 0x0: terminate (Access terminates at the System MMU as RAZ/WI. Context fault exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x1: stall (Requesting master's access stalled while System MMU waits for managing processor to resolve context fault. Context fault exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode)

ROT_SMMU_ROT_CBn_ACTLR (cont.)

Bits	Name	Description
13:12	TLBMCFG	(TLB miss configuration) Governs the behavior of client accesses that miss in the TLB 0x0: pass-through (Access passed through to targeted slave without translation, attribute control, or access permission checking. Effectively, behavior is as if SMMU_CBn_SCTLR = 0 i.e., MMU disabled for this context bank. TLB miss not considered a context fault. TLB miss exception not recorded in SMMU_CBn_FSR. TLB miss exception not reported to requesting master. SMMU_contextFaultIrptReq interrupt output not asserted) 0x1: terminate (Access terminates at the System MMU as RAZ/WI,TLB miss exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x2: stall (Requesting master's access stalled while System MMU waits for managing processor to update TLB. TLB miss exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode) 0x3: HTW (Hardware table walk . Requesting master's access stalled while System MMU accesses page table. The is TLB updated and requesting master's access resumed after obtaining valid entry from page table. If translation fault, then access either terminates or stalls according to setting of SMMU_CBn_ACTLR)
11	DNLV2PA	(disable non-locking VA-to-PA allocation) Governs whether or not TLB misses due to non-locking VA-to-PA commands will allocate a new entry This field is ignored for locking VA-to-PA operations (SMMU_CBn_TLBLKCR[LKE] = 1)
10	DNA	(disable normal allocation) Governs whether or not TLB misses due to client port accesses will allocate a new entry
9:8	PRIVCFG	0x0: apriv (System MMU uses APRIV signal supplied by master as user/supervisor indicator 1 = supervisor) 0x1: reserved 0x2: User (System MMU ignores APRIV; treats all requests using this context bank as user) 0x3: Supervisor (System MMU ignores APRIV; treats all requests using this context bank as supervisor)

ROT_SMMU_ROT_CBn_ACTLR (cont.)

Bits	Name	Description
7:5	RESERVED_1	
4	RCNSH	(redirect cacheable-non-shareable) Governs whether or not cacheable accesses that are non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache, even though the locations are not being coherently shared with Scorpion-MP
3	RCISH	(redirect cacheable-inner-shareable) Governs whether or not cacheable accesses that are inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
2	RCOSH	(redirect cacheable-outer-shareable) Governs whether or not cacheable accesses that are outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
1	CFEIE	(context fault error interrupt enable) Governs whether or not client port request context faults are reported directly to the interrupt controller via the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus Interrupt output is asserted if SMMU_CBn_ACTLR[CFEIE] is 1 and any context fault bits are set in SMMU_CBn_FSR Such interrupts would generally be directed to the interrupt controller of whichever processor is currently managing this context bank of the System MMU Reset state : 0
0	CFERE	(context fault error report enable) Governs whether or not client port request context faults that are configured for terminate mode (or that are explicitly terminated after stall mode) are reported to the requesting master, according to the client port bus protocol All error types reported via AXI port will use decode error rather than slave error All context faults are recorded in SMMU_CBn_FSR, regardless of the value of this field.

0x07700008+ 0x1000*n ROT_SMMU_ROT_CBn_CONTEXTIDR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context ID register holds the ASID associated with this context bank

ROT_SMMU_ROT_CBn_CONTEXTIDR

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Specifies the 8 bit ASID value assigned to this context bank. The ASID can be included in the key comparison of TLB entries. .

0x07700010+ 0x1000*n ROT_SMMU_ROT_CBn_TTBR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR0 is used for low order virtual addresses, typically private pages for a given process.

ROT_SMMU_ROT_CBn_TTBR0

Bits	Name	Description
31:7	PA	BIts 31:7 of the physical address of the base of the page table. The actual LSB of the base address is bit 14-N, where N is set in register TTCR
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07700014+0x1000*n ROT_SMMU_ROT_CBn_TTBR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR1 is used for high order virtual addresses, typically global pages for a given VMID, or kernal mappings.

The context bank auxiliary control register controls various implementation specific features.

ROT_SMMU_ROT_CBn_TTBR1

Bits	Name	Description
31:14	PA	BIts 31:14 of the physical address of the base of the page table.
13:7	RESERVED_2	
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED_1	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07700018+0x1000*n ROT_SMMU_ROT_CBn_TTBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table control register, which specifies the size of the virtual address space that uses TTBR0.

ROT_SMMU_ROT_CBn_TTBCR

Bits	Name	Description
31:6	RESERVED_2	
5	PD1	Page disable 1; if this bit is set, hardware table walks attempting to use TTBR1will result in a first level descriptor translation fault. If clear, TTBR1 contents are used.
4	PD0	Page disable 0; if this bit is set, hardware table walks attempting to use TTBR0 will result in a first level descriptor translation fault. If clear, TTBR0 contents are used.
3	RESERVED_1	
2:0	N	N[2:0] specifies the number of upper order virtual address bits which must be 0 in order for translations to use the table pointed to by TTBR0. If any of these bits are non-zero, TTBR1 is used for the lookup. If N is 0, only TTBR0 is used.

0x0770001C+ 0x1000*n ROT_SMMU_ROT_CBn_PAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The physical address register captures the physical address value resulting from the execution of a VA-to-PA command

Field definitions vary according to whether or not there is a context fault associated with the requested translation

ROT_SMMU_ROT_CBn_PAR

Bits	Name	Description
31:12	PAR_FAULT_INFO_312	
11	RESERVED_2	
10:9	PAR_FAULT_INFO_72	
8	RESERVED_1	
7:1	PAR_FAULT_INFO_71	Encoding varies according to value in FAULT field.
0	FAULT	(fault status) This field will be 1 when a context fault is associated with the requested translation, and 0, when there is no context fault associated with the requested translation.

0x07700020+0x1000*n ROT_SMMU_ROT_CBn_FSR, n=[0..1]

Type: Read/WriteClear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The Fault Status Register records status information for client accesses that encounter exceptions within the context bank, e.g. translation faults.This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data

This prevents inadvertent clearing of new faults when writing the register to clear an old fault

The presence of an asserted value on any bit in this register (except the SS bit) is what prompts the assertion (when enabled by SMMU_CBn_ACTLR[CFEIE]) of the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus

Therefore, these bits must be cleared by the interrupt handler

This is contrasted with the fields in the SMMU_CBn_FSYNRn registers, which are merely the "syndrome" of the fault indicated by SMMU_CBn_FSR

ROT_SMMU_ROT_CBn_FSR

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry

ROT_SMMU_ROT_CBn_FSR (cont.)

Bits	Name	Description
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07700024+ 0x1000*n ROT_SMMU_ROT_CBn_FSRRESTORE, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Allows SW to force a value into the SMMU_CBn_FSR register.

ROT_SMMU_ROT_CBn_FSRRESTORE

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)

ROT_SMMU_ROT_CBn_FSRRESTORE (cont.)

Bits	Name	Description
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07700028+ 0x1000*n ROT_SMMU_ROT_CBn_FAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The Fault Address Register records the virtual address of client accesses that encounter exceptions within the context bank, e.g. translation faults. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

ROT_SMMU_ROT_CBn_FAR

Bits	Name	Description
31:0	VA	VA[31:0] of errant client access

0x0770002C+ 0x1000*n ROT_SMMU_ROT_CBn_FSYNR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

NOTE omission of VMID field from this register, as VMID can only be made visible to SROT, and not to general OS software that manages the context bank registers

ROT_SMMU_ROT_CBn_FSYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] (ATID field of errant request)

ROT_SMMU_ROT_CBn_FSYNR0 (cont.)

Bits	Name	Description
23:16	RESERVED	
15:13	ABID	ABID[2:0] (ABID field of errant request)
12:8	APID	APID[4:0] (APID field of errant request)
7:0	AMID	AMID[7:0] (AMID field of errant request)

0x07700030+ 0x1000*n ROT_SMMU_ROT_CBn_FSYNR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

ROT_SMMU_ROT_CBn_FSYNR1

Bits	Name	Description
31:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO (AOOO field of the errant request)
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request
15:12	ALEN	ALEN[3:0]field of the errant request
11	RESERVED_2	
10	ABURST	field of the errant request
9	RESERVED_1	
8	AWRITE	field of the errant request
7	AINST	field of the errant request
6	APROTNS	field of the errant request
5	APRIV	field of the errant request
4	AINNERSHARED	(AINNERSHARED field of the errant request)
3	ASHARED	(ASHARED field of the errant request)

ROT_SMMU_ROT_CBn_FSYNR1 (cont.)

Bits	Name	Description
2:0	AMEMTYPE	AMEMTYPE[2:0] (AMEMTYPE field of the errant request)

0x07700034+0x1000*n ROT_SMMU_ROT_CBn_PRRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs memory type and shareability attributes of requests that are both MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1)

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) and/or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, memory type encoding is as follows:

0b00 = strongly-ordered

0b01 = device

0b10 = normal

0b11 = reserved

ROT_SMMU_ROT_CBn_PRRR

Bits	Name	Description
31	NOS7	not-outer-shareable class 7
30	NOS6	not-outer-shareable class 6
29	NOS5	not-outer-shareable class 5
28	NOS4	not-outer-shareable class 4
27	NOS3	not-outer-shareable class 3
26	NOS2	not-outer-shareable class 2
25	NOS1	not-outer-shareable class 1
24	NOS0	not-outer-shareable class 0
23:20	RESERVED	

ROT_SMMU_ROT_CBn_PRRR (cont.)

Bits	Name	Description
19	SHNMSH1	(shareable attribute for normal memory accesses with SH=1) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1
18	SHNMSH0	(shareable attribute for normal memory accesses with SH=0) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0
17	SHDSH1	SHDSH1 (shareable attribute for device accesses with SH=1) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1 [
16	SHDSH0	SHDSH0 (shareable attribute for device accesses with SH=0) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0 [
15:14	MTC7	MTC7[1:0] (memory type class 0)
13:12	MTC6	MTC6[1:0] (memory type class 0)
11:10	MTC5	MTC5[1:0] (memory type class 0)
9:8	MTC4	MTC4[1:0] (memory type class 0)
7:6	MTC3	MTC3[1:0] (memory type class 0)
5:4	MTC2	MTC2[1:0] (memory type class 0)
3:2	MTC1	MTC1[1:0] (memory type class 0)
1:0	MTC0	MTC0[1:0] (memory type class 0)

0x07700038+0x1000*n ROT_SMMU_ROT_CBn_NMRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs the cache policy of MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1) requests for which the memory type is mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0) or the memory type is mapped to a type other than normal memory (SMMU_CBn_PRRR[MTCn] != 0b10)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, inner-cache and outer-cache policy encodings are as follows:

0b00 = non-cacheable

0b01 = cacheable, copy-back, write-allocate

0b10 = cacheable, write-through, write-no-allocate

0b11 = cacheable, copy-back, write-no-allocate

ROT_SMMU_ROT_CBn_NMRR

Bits	Name	Description
31:30	OCPC7	OCPC7[1:0] (inner-cache policy class 7)
29:28	OCPC6	OCPC6[1:0] (inner-cache policy class 6)
27:26	OCPC5	OCPC5[1:0] (inner-cache policy class 5)
25:24	OCPC4	OCPC4[1:0] (inner-cache policy class 4)
23:22	OCPC3	OCPC3[1:0] (inner-cache policy class 3)
21:20	OCPC2	OCPC2[1:0] (inner-cache policy class 2)
19:18	OCPC1	OCPC1[1:0] (inner-cache policy class 1)
17:16	OCPC0	OCPC0[1:0] (inner-cache policy class 0)
15:14	ICPC7	ICPC7[1:0] (inner-cache policy class 7)
13:12	ICPC6	ICPC6[1:0] (inner-cache policy class 6)
11:10	ICPC5	ICPC5[1:0] (inner-cache policy class 5)
9:8	ICPC4	ICPC4[1:0] (inner-cache policy class 4)
7:6	ICPC3	ICPC3[1:0] (inner-cache policy class 3)
5:4	ICPC2	ICPC2[1:0] (inner-cache policy class 2)
3:2	ICPC1	ICPC1[1:0] (inner-cache policy class 1)
1:0	ICPC0	ICPC0[1:0] (inner-cache policy class 0)

0x0770003C+0x1000*n ROT_SMMU_ROT_CBn_TLBLKCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB lock control register governs the TLB locking mechanism and TLB invalidate operations.Write access to this register is governed by SMMU_CR[TLBLKCRWE]

When SMMU_CR[TLBLKCRWE] is 0, writes to SMMU_CBn_TLBLKCR are ignored

Read access is still permitted

SROT can set SMMU_CR[TLBLKCRWE] to 1 to allow operating environment(s) to manage the TLB locking mechanism

Management amongst multiple operating environments must be coordinated via semaphore

ROT_SMMU_ROT_CBn_TLBLKCR

Bits	Name	Description
31:24	RESERVED_2	
23:16	VICTIM	VICTIM[7:0] Indicates the TLB index at which the next normal (non-locking) allocation will occur Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context
15:8	FLOOR	FLOOR[7:0] Indicates the TLB index from which round-robin replacement on normal (non-locking) allocations occurs TLB entries at indices below this value are locked Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context banks
7:4	RESERVED_1	
3	TLBIVAACFG	(TLBIVAA configuration) TLBIVAACFG = 0 - flash-invalidate SMMU_CBn_TLBIVAA commands flash-invalidate the entire TLB, without regard to locking, security, address, and/or VMID value TLBIVAACFG = 1 - selective SMMU_CBn_TLBIVAA commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank VA field of TLB entry matches VA designated by SMMU_CBn_TLBIVAA command NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked

ROT_SMMU_ROT_CBn_TLBLKCR (cont.)

Bits	Name	Description
2	TLBIASIDCFG	(TLBIASID configuration) TLBIASIDCFG = 0 - flash-invalidate SMMU_CBn_TLBIASID commands flash-invalidate the entire TLB, without regard to locking, security, VMID, and/or ASID values TLBIASIDCFG = 1 - selective SMMU_CBn_TLBIASID commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command TLB entry is not global (NG field is 1) NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
1	TLBIALLCFG	(TLBIALL configuration) TLBIALLCFG = 0 - flash-invalidate SMMU_CBn_TLBIALL commands flash-invalidate the entire TLB, without regard to locking, security, and/or VMID value TLBIALLCFG = 1 - selective SMMU_CBn_TLBIALL commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked
0	LKE	(lock enable) Governs whether or not TLB entries established by VA-to-PA commands upon TLB misses are locked LKE = 0 (normal, non-locking) Allocate VA-to-PA TLB entry (if TLB miss) at the index specified by SMMU_CBn_TLBLKCR[VICTIM] Allocation is disabled if SMMU_CBn_ACTLR[DNLV2PA] is 1 Increment SMMU_CBn_TLBLKCR[VICTIM] by 1 (only if new entry allocated) Wrap back to the value of SMMU_CBn_TLBLKCR[FLOOR] when the last entry is written LKE = 1 (locking) Search TLB for specified VA and invalidate if found Provides atomicity between the invalidate and the new allocation within the locked region Allocate VA-to-PA TLB entry at the index specified by data operand bits 7:0 of the VA-to-PA command This value must be less than SMMU_CBn_TLBLKCR[FLOOR] in order for it to remain locked Allocation occurs even if non-locking allocation is disabled due to SMMU_CBn_ACTLR[DNLV2PA] = 1

0x07700040+0x1000*n ROT_SMMU_ROT_CBn_V2PSR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The VA-to-PA status register records the hit/miss status and TLB index or V2Pxx and TLB invalidate commands.

ROT_SMMU_ROT_CBn_V2PSR

Bits	Name	Description
31:16	RESERVED_2	
15:8	INDEX	INDEX[7:0] Indicates the index of the TLB entry associated with the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command If SMMU_CBn_V2PSR[HIT] is 0, then SMMU_CBn_V2PSR[INDEX] is the index to which the entry was allocated (if allocated at all) If SMMU_CBn_V2PSR[HIT] is 1, then SMMU_CBn_V2PSR[INDEX] is the index of the entry which hit
7:1	RESERVED_1	
0	HIT	Indicates whether or not there was a TLB hit (prior to allocation, if any) on the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command

0x07700044+0x1000*n ROT_SMMU_ROT_CBn_TLBFLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB first level PTE register holds the first level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

This register (together with SMMU_CBn_TLBSLPTER) is used as the source of the translation information for VA-to-PA operations when the MMU is enabled (SMMU_CBn_SCTLR[M] = 1) and the operations are configured for software table update (SMMU_CBn_ACTLR[V2PCFG] = 0b01)

Field definitions vary according to the type of PTE (fault, page, section, or supersection), and come directly from the ARMv7 architecture's PTE formats

ROT_SMMU_ROT_CBn_TLBFLPTER

Bits	Name	Description
31:10	FL_PTE_HI	

ROT_SMMU_ROT_CBn_TLBFLPTER (cont.)

Bits	Name	Description
9:5	RESERVED	
4:2	FL_PTE_LO	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	This field should be set to 0b00 or 0b11 to indicate that the translation should result in a context fault, and the rest of the fields are defined as indicated in this section If this field is not 0b00 or 0b11, then the PTE is of some other type (see other sections for the field definitions for those types)

0x07700048+ 0x1000*n ROT_SMMU_ROT_CBn_TLBSLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB second level PTE register holds the second level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

Field definitions vary according to the type of PTE (fault, 64KB or 4KB), and come directly from the ARMv7 architecture's PTE format

ROT_SMMU_ROT_CBn_TLBSLPTER

Bits	Name	Description
31:2	SL_PTE	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	0x0: fault

0x0770004C+ 0x1000*n ROT_SMMU_ROT_CBn_BFBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The burst fetch buffer configuration register governs the operation of the "burst fill" feature of the SMMU.

ROT_SMMU_ROT_CBn_BFBCR

Bits	Name	Description
31:12	STRIDE	(stride amount) 4KB-aligned value to be added to virtual address on demand TLB miss for filling subsequent BFB Stride of minimum 4KB alignment useful for preventing stride burst fetch until final PTE of the demand BFB entry is used
11:8	SLVIC	(second-level victim) Indicates the SLBFB index at which the next round-robin allocation will occur
7:4	FLVIC	(first-level victim) Indicates the FLBFB index at which the next round-robin allocation will occur
3	RESERVED	
2	SFVS	(stride-fetch victim selection) SFVS. = 0 (replace normal round-robin victim-selected entry) Useful when stride is larger than the VA space represented by the four PTEs in the demand BFB entry, but the client access pattern is for more than just the initial PTE in that demand BFB entry SFVS. = 1 (replace same BFB used by demand VA for which the stride burst is being performed) Useful when stride is the same as the VA space represented by an individual PTE in the demand BFB entry (such that the stride won't miss against the BFB until the last PTE of the demand BFB entry is accessed), and/or when the client access pattern only uses the initial PTE in the demand BFB entry
1	BFBSFE	(burst fetch buffer stride fetch enable) Enables stride burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Stride burst fetch is for the block of four PTEs associated with VA+stride VA is the "demanded" VA from the client (or VA-to-PA command) Stride value is specified by SMMU_CBn_BFBCR[STRIDE] Stride burst fetch only occurs if demand access for VA misses in TLB (could hit in BFB) and address VA+stride misses in both TLB and BFB
0	BFBDFE	(burst fetch buffer demand fetch enable) Enables demand burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Demand burst fetch is for the block of four PTEs associated with the "demanded" VA from the client (or VA-to-PA command) Demand burst fetch only occurs if demand access misses in both TLB and BFB

0x07700800+ 0x1000*n ROT_SMMU_ROT_CBn_TLBIALL, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate all command register invalidates all TLB entries matching the VMID associated with this context bank. Data operand is ignored.

ROT_SMMU_ROT_CBn_TLBIALL

Bits	Name	Description
31:0	RESERVED	

0x07700804+ 0x1000*n ROT_SMMU_ROT_CBn_TLBIASID, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by ASID command register invalidates TLB entries matching the specified ASID and matching the VMID associated with this context bank.Invalidates TLB entries which are associated with the designated ASID and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIASIDCFG] governs whether command flash-invalidates entire TLB array or just the entries matching the VMID, ASID, and security state

TLBIASIDCFG = 0 - flash-invalidate

SMMU_CBn_TLBIASID command flash-invalidates the entire TLB, without regard to locking, security, VMID, and/or ASID values

TLBIASIDCFG = 1 - selective

SMMU_CBn_TLBIASID command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command data operand

TLB entry is not global (NG field is 1)

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command

Locking is not considered (matching entries are invalidated even if locked)

ASID field of command specifies the ASID value of the TLB entries to be invalidated

ROT_SMMU_ROT_CBn_TLBIASID

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Actual ASID value

0x07700808+0x1000*n ROT_SMMU_ROT_CBn_TLBIVA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA command invalidates TLB entries matching the designated VA, ASID and the VMID associated with this context bank.

Matching entry determined as follows:

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIVA command data operand (or TLB entry is global - NG field is 0)

VA field of TLB entry matches VA value designated by the SMMU_CBn_TLBIVA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIVA command

Locking is not considered (matching entry is invalidated even if locked)

Data operand specifies the VA and ASID value of the TLB entry to be invalidated

ROT_SMMU_ROT_CBn_TLBIVA

Bits	Name	Description
31:12	VA	VA[31:12]
11:8	RESERVED	
7:0	ASID	ASID[7:0] value

0x0770080C+0x1000*n ROT_SMMU_ROT_CBn_TLBIVAA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA all ASIDS command invalidates TLB entries matching the designated VA and the VMID associated with this context bank, regardless of ASID.Invalidates TLB entries which are associated with the designated VA, regardless of ASID, and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIVAACFG] governs whether command flash-invalidates entire TLB array or just the non-locked entries matching the VMID, ASID, and security state

TLBIVAACFG = 0 - flash-invalidate

SMMU_CBn_TLBIVAA command flash-invalidates the entire TLB, without regard to locking, security, address, and/or VMID value

TLBIVAACFG = 1 - selective

SMMU_CBn_TLBIVAA command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

VA field of TLB entry matches VA designated by the SMMU_CBn_TLBIVAA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command

Entry is unlocked

ROT_SMMU_ROT_CBn_TLBIVAA

Bits	Name	Description
31:12	VA	VA[31:12]
11:0	RESERVED	

0x07700810+ 0x1000*n ROT_SMMU_ROT_CBn_V2PRR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

ROT_SMMU_ROT_CBn_V2PRR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07700814+0x1000*n ROT_SMMU_ROT_CBn_V2PPW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

ROT_SMMU_ROT_CBn_V2PPW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07700818+ 0x1000*n ROT_SMMU_ROT_CBn_V2PUR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

ROT_SMMU_ROT_CBn_V2PUR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x0770081C+ 0x1000*n ROT_SMMU_ROT_CBn_V2PUW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

.Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

ROT_SMMU_ROT_CBn_V2PUW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	

ROT_SMMU_ROT_CBn_V2PUW (cont.)

Bits	Name	Description
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07700820+ 0x1000*n ROT_SMMU_ROT_CBn_RESUME, n=[0..1]

Type: Write/command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB resume command causes the SMMU to resume operation after a stalled access..

ROT_SMMU_ROT_CBn_RESUME

Bits	Name	Description
31:1	RESERVED	
0	TNR	Terminate/not retry When TNR is written as 0, indicates that the stalled access should be retried by the system MMU. When written as 1, indicates that this stalled transaction is terminated by the system MMU. The error is optionally reported to the requesting master, using the client port bus protocol, if SMMU_CNn_ACTLR[CFERE] == 1. Interrupt optionally remains asserted via SMMU_M2VCBRn[IRPTINDX] selected SMMU_contextFaultIrptReq bit, only if SMMU_CBn_ACTLR[CFEIE] is 1, and only if SMMU_CBn_FSR has not been cleared by software priori to issuing this command..

14.26 IJPEG SMMU Registers (0x07800000 SMMU_JPEG_BASE)

This section contains IJPEG SMMU registers.

14.26.1 SMMU Global Registers

14.26.1.1 SMMU VMID/CBNDX mapping registers

0x078FF000+ 0x4*n IJPEG_SMMU_IJPEG_M2VCBRn, n=[0..1]

Type: Read/Write
Clock: AXI_CLK
Reset State: Undefined

SMMU_M2VCBRm registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

IJPEG_SMMU_IJPEG_M2VCBRn

Bits	Name	Description
31:28	RESERVED_2	
27:25	BPMEMTYPE	(bypass memory type) Supplies the AMEMTYPE attributes for client requests which bypass the System MMU when SMMU_M2VCBRn[BPMTCFG] = 1 See reference section for AMEMTYPE encoding definitions
24	BPMTCFG	(bypass memory type configuration) Governs the memory type (AMEMTYPE) attributes of client requests which bypass the System MMU BPMTCFG = 0 - use AMEMTYPE Bypass requests use AMEMTYPE signal supplied by client master BPMTCFG = 1 - use SMMU_M2VCBRn[BPMEMTYPE] Bypass requests use SMMU_M2VCBRn[BPMEMTYPE] Reset state : 0
23:22	NSCFG	(non-secure configuration) Governs the incoming security designation of client requests NSCFG = 0b00 - use APROTNS Use APROTNS signal supplied by client master NSCFG = 0b01 - reserved NSCFG = 0b10 - secure System MMU ignores APROTNS; treats all requests as secure NSCFG = 0b11 - non-secure System MMU ignores APROTNS; treats all requests as non-secure Reset state : 0

IJPEG_SMMU_IJPEG_M2VCBRn (cont.)

Bits	Name	Description
21:20	BPSHCFG	(bypass shareability configuration) Governs the shareability realm (ASHARED and AINNERSHARED) attributes of client requests which bypass the System MMU BPSHCFG = 0b00 - use ASHARED and AINNERSHARED Bypass requests use ASHARED and AINNERSHARED signals supplied by client master BPSHCFG = 0b01 - outer-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 0 BPSHCFG = 0b10 - inner-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 1 BPSHCFG = 0b11 - non-shareable Bypass requests set ASHARED = 0, AINNERSHARED = 0 Reset state : 0
19	BPRCNSH	(bypass redirect cacheable-non-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache Reset state : 0
18	BPRCISH	(bypass redirect cacheable-inner-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0
17	BPRCOSH	(bypass redirect cacheable-outer-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0

IJPEG_SMMU_IJPEG_M2VCBRn (cont.)

Bits	Name	Description
16	BYPASSD	Bypass disable for this index Governs whether or not client port accesses using this mapping table entry are actually permitted to "bypass" the System MMU when such bypass is indicated (either due to CBNDX = 255 or due to the master asserting the "SMMU bypass" input) This field is ignored (and operates as if it were 0) if SMMU_CR[CLIENTPD] is 1 BYPASSD = 0 - bypass enabled Bypass requests truly bypass the System MMU and "pass-through" to the fabric (no translation, access control, or attribute generation) No cycle of latency for System MMU context bank access Bypass request not considered an error Bypass request error not recorded in SMMU_ESR[BYPASS] Bypass error not reported to requesting master SMMU_rpuErrIrptReq interrupt output not asserted Client accesses still reference M2VCBMT to get VMID value for presentation to fabric BYPASSD = 1 - bypass disabled System MMU terminates the access as RAZ/WI Bypass request is considered an error Bypass request error is recorded in SMMU_ESR[BYPASS] If SMMU_CR[RPUERE] is 1, then bypass error reported to requesting master according to the client port bus protocol If SMMU_CR[RPUEIE] is 1, then SMMU_rpuErrIrptReq interrupt output asserted
15:8	CBNDX	Context bank index Context bank index associated with the M2VCBMT index CBNDX = 255 indicates no context bank assigned ("bypass")
7:5	RESERVED_1	
4:0	VMID	Virtual machine ID VMID value associated with the M2VCBMT index Must be programmed consistently with the SMMU_CBACRn[CBVMID] field for the context bank designated by SMMU_M2VCBRm[CBNDX]

14.26.1.2 SMMU context bank access control registers

0x078FF800+ 0x4*n IJPEG_SMMU_IJPEG_CBACRn, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs configuration port access to the associated context bank registers.

IJPEG_SMMU_IJPEG_CBACRn

Bits	Name	Description
31:24	IRPTNDX	(interrupt index) Interrupt output number used for context faults associated with this context bank (use SMMU_contextFaultIrptReq[IRPTNDX])
23:21	RESERVED	
20:16	CBVMID	(context bank VMID) Specifies the VMID with which the client masters using the context bank are associated Must be programmed consistently with the M2VCBMT entries that are configured to use the associated context bank This field is used by configuration port commands that need the context bank's VMID value in order to access the TLB (e.g., SMMU_CBn_TLBIVMID, SMMU_CBn_V2Pxx)
15:10	RESERVED_2	
9	RWGE	Read/write global enable. Setting this bit allows access to the context bank registers from any VMID
8	RWE	Read/write enable. Indicates that the RWVMID field is valid.
7:5	RESERVED_1	
4:0	RWVMID	Specifies owner VMID with full read/write access to the registers in the associated context bank "n".

14.26.1.3 SMMU TLB software access registers

0x078FFE00 IJPEG_SMMU_IJPEG_TLBRSW

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Writing to this address requests that the TLB entry at INDEX be read into the SMMU_TLBTRn registers

IJPEG_SMMU_IJPEG_TLBRSW

Bits	Name	Description
31:10	RESERVED	

IJPEG_SMMU_IJPEG_TLBRSW (cont.)

Bits	Name	Description
9:8	TLBBFBS	This field selects the TLB, TFBFB, SLBFB 0x0: Selecting TLB 0x1: Not defined 0x2: Selecting FL BFB 0x3: Selecting SL BFB
7:0	INDEX	TLB index to be read.

0x078FFE80 IJPEG_SMMU_IJPEG_TLBTR0

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

This register holds part of TLB entry read by the last TLBRSW command.

IJPEG_SMMU_IJPEG_TLBTR0

Bits	Name	Description
31:23	RESERVED_4	
22:20	DPSIZC	3 bit decode page size field from CAM-side of TLB CAM-RAM) Same determination and encoding as for DPSIZR The CAM-side copy of this field is used for hit/miss determination in the TLB CAM array
19	RESERVED_3	
18:16	DPSIZR	(3 bit decode page size field from RAM-side of TLB CAM-RAM) Determined from the size fields of the page table entry Encodes the page size as follows: all other values reserved/unused The RAM-side copy of this field is used for virtual ’ physical address formation 0x0: 4KB page 0x1: 64KB page 0x3: 1MB page 0x7: 16MB page
15:12	RESERVED_2	
11	MT2	(memory type bit 2) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[2] attribute bus on the request output of the System MMU

IJPEG_SMMU_IJPEG_TLBTR0 (cont.)

Bits	Name	Description
10	MT1	(memory type bit 1) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[1] attribute bus on the request output of the System MMU
9	MT0	(memory type bit 0) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[0] attribute bus on the request output of the System MMU
8	SH	(shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's outer-shareable realm This field becomes the ASHARED attribute on the request output of the System MMU
7	ISH	(inner-shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's inner-shareable realm This field becomes the AINNERSHARED attribute on the request output of the System MMU
6	NSDESC	(non-secure descriptor) This TLB entry field is a modified version of the corresponding bit of the page table entry Qualified by the NS-prot attribute of the incoming request which prompted the allocation of the TLB entry, such that if the incoming NS-prot attribute was 1 (non-secure), then the NS-desc field of the page table entry was ignored, and the NS-desc field of the TLB entry was forced to 1 Indicates whether the associated memory page contains secure (NS-desc=0) or non-secure (NS-desc=1) information This field becomes the NS-prot attribute on the request output of the System MMU
5	RESERVED_1	

IJPEG_SMMU_IJPEG_TLBTR0 (cont.)

Bits	Name	Description
4	XN	(execute never permission) This TLB entry field comes directly from the corresponding bit of the page table entry
3	UW	(user write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
2	UR	(user read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
1	PW	(privileged write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
0	PR	(privileged read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]

0x078FFE84 IJPEG_SMMU_IJPEG_TLBTR1

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

IJPEG_SMMU_IJPEG_TLBTR1

Bits	Name	Description
31:12	PA	Physical address [31:12] field of the TLB entry
11:5	RESERVED	
4:0	VMID	VMID [4:0]field of the TLB entry)

0x078FFE88 IJPEG_SMMU_IJPEG_TLBTR2

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

IJPEG_SMMU_IJPEG_TLBTR2

Bits	Name	Description
31:12	VA	virtual address field [31:12] of the TLB entry
11	RESERVED	
10	NG	(not global field from page table entry) Indicates whether the page is private to the specified ASID (NG=1) or global to all ASIDs within the VMID using this context bank (NG=0)
9	NSTID	(non-secure tag ID field of the TLB entry) Indicates whether the TLB entry belongs to the secure world (NSTID=0) or the non-secure world (NSTID=1) This field is comned against the incoming NS-prot attribute of the master request as part of TLB hit/miss determination
8	V	valid field of the TLB entry
7:0	ASID	ASID[7:0] field of the TLB entry

0x078FFE8C IJPEG_SMMU_IJPEG_TESTBUSCR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

Governs which signals (if any) from the system SMMU core or wrapper design hierarchy are sent out to the system via a testbus for diagnostic, and also to the system profiling and diagnostic monitor(SPDM).

IJPEG_SMMU_IJPEG_TESTBUSCR

Bits	Name	Description
31:28	SPDM3SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[3]
27:24	SPDM2SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[2]
23:20	SPDM1SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[1]
19:16	SPDM0SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[0]
15:14	TBHSEL	Testbus highselect It governs which set of signals are to testbus[31:16] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL

IJPEG_SMMU_IJPEG_TESTBUSCR (cont.)

Bits	Name	Description
13:12	TBSLSEL	Testbus low select It governs which set of signals are to testbus[15:0] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL
11:10	RESERVED_2	
9:8	WGSEL	Wrapper group select It selects a particular group of signals from the SMMU wrapper hierarchy WGSEL = 0b00 - wrapper signal group 0 WGSEL = 0b01 - wrapper signal group 1 WGSEL = 0b10 - wrapper signal group 2 WGSEL = 0b11 - reserved
7:2	RESERVED_1	
1	SPDMBE	SPDM test enable Reset state : 0
0	TBE	Testbus enable, which governs whether the testbus is driven with all 0s or with the configured signals Reset state : 0

0x078FFEFC IJPEG_SMMU_IJPEG_VR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: 32'h0000_0000

Note that the DCPBP/DCPPP bits prevent the pipelining of the next transaction when the current transaction is a bypass/pass-through transaction. That is, they add one more cycle of delay between the current and next transactions.

Also note that when we are in global bypass (SMMU_CR[CLIENTPD]=1), these bits should have NO effect, or at least no effect between client transactions, they can have an effect between config and client transactions is appropriate. We must be able to continue to perform fully pipelined transactions when the client port is disabled altogether.

IJPEG_SMMU_IJPEG_VR0

Bits	Name	Description
31:3	RESERVED	

IJPEG_SMMU_IJPEG_VR0 (cont.)

Bits	Name	Description
2	DCPPT	Disable client pipelining for client operations in pass-through mode Reset state : 0
1	DCPBP	Disable client pipelining for client operations in bypass mode Reset state : 0
0	DCP	Disable client pipelining Reset state : 0

0x078FFF00 IJPEG_SMMU_IJPEG_TLBIALL

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries.

IJPEG_SMMU_IJPEG_TLBIALL

Bits	Name	Description
31:0	EXEC	Writing any value to this register invalidates all TLB entries, as specified by the contents of SMMU_CR[TLBIALLCFG]

0x078FFF04 IJPEG_SMMU_IJPEG_TLBIVMID

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries matching the IVMID value. Precise function is governed by SMMU_CR[TLBIALLCFG].

IJPEG_SMMU_IJPEG_TLBIVMID

Bits	Name	Description
31:5	RESERVED	
4:0	IVMID	Designates VMID[4:0] value of entries to be invalidated.

14.26.1.4 SMMU configuration registers

0x078FFF80 IJPEG_SMMU_IJPEG_CR

Type: Read/Write
Clock: AXI_BUS_CLOCK

Global configuration register.

IJPEG_SMMU_IJPEG_CR

Bits	Name	Description
31:10	RESERVED_2	
9	RESERVED_1	Reset state : 0
8	TLBIVMIDCFG	TLBIVMID configuration control. When set to 0,flash-invalidate, SMMU_TLBIVMID commands flash-invalidate the entire TLB, without regard to locking ,security and VMID value. When set to 1, selective, SMMU_TLBIVMID invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and VMID field matching the VMID specified by SMMU_TLBIVMID command. Reset state : X
7	TLBIALLCFG	TLBIALL configuration control. When set to 0, flash-invalidate, SMMU_TLBIALL commands flash-invalidate the entire TLB, without regard to locking and/or security. When set to 1, selective, SMMU_TLBIALL invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and are unlocked. Reset state : X
6	TLBLKCRWE	TLBLKCR write enable. When set to 0, writes to SMMU_CBn_TLBLKCR are ignored. When set to 1, allows operating environments to manage the TLB locking mechanism directly. Management amounst multiple operating environments must be coordinated externally between themselves. Reset state : X
5	STALLD	Global disable for stall mode. When set to 1, context bank stall modes are ignored and operate as terminate mode. Reset state : X
4	CLIENTPD	Client port disable. When set, all client accesses are forced to bypass the system MMU. There is no translation. access control, or attribute generation. This bit overrides individual SMMU_M2VCBRn[BYPASSD] settings; client requests are bypassed, even if SMMU_M2VCBRn[BYPASSD] is set to 1. Bypass request errors are not recorded in SMMU_ESR, nor reported to requesting masters. The SMMU_rpuErrIrptReq interrupt output signal is not asserted. Reset state : 1

IJPEG_SMMU_IJPEG_CR (cont.)

Bits	Name	Description
3	DCDEE	When set to 0, configuration port decode errors do not set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn are not updated. When set to 1, configuration port decode errors set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn updated with address and syndrome of error. Reset state : X
2	RPUEIE	When set, configuration port errors and client port bypass errors are reported directly to the interrupt controller via the SMMU_rputErrIrptReq interrupt output signal. Interrupt output is asserted if SMMU_CR[RPUIE_EN] is 1 and ANY bit is set in SMMU_ESR register. Reset state : 0
1	RPUERE	When set, SMMU reports configuration port errors and client port bypass errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via AXI port will use decode error, rather than slave error. Regardless of the value of this field both configuration port errors and client port bypass request errors are terminated by the SMMU as RAZ/WI, and are recorded in SMMU_ESR register. Reset state : X
0	RPUE	When set, all configuration port accesses are checked against SMMUX_RPU_ACR and/or the SMMUX_CBACRn registers for access permissions. Reset state : 0

14.26.1.5 SMMU error report registers

0x078FFF84 IJPEG_SMMU_IJPEG_EAR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: unknown

When there is an error, holds the physical address of the errant transaction.

IJPEG_SMMU_IJPEG_EAR

Bits	Name	Description
31:0	PA	Physical address[31:0]

0x078FFF88 IJPEG_SMMU_IJPEG_ESR

Type: Read/Write to clear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This register has read/write clear access. Reads return the value in the register, a write with a 1 set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

IJPEG_SMMU_IJPEG_ESR

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x078FFF8C IJPEG_SMMU_IJPEG_ESRRESTORE

Type: Write
Clock: RPM_BUS_CLK
Reset State: Undefined

This register is an aliased address for SMMU_ESR, but it allows direct write access. In this way, diagnostic software can cause an error to be generated and reported.

IJPEG_SMMU_IJPEG_ESRRESTORE

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	

IJPEG_SMMU_IJPEG_ESRRESTORE (cont.)

Bits	Name	Description
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x078FFF90 IJPEG_SMMU_IJPEG_ESYNR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

IJPEG_SMMU_IJPEG_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request
15:0	AMID	AMID[15:0] field of errant request

0x078FFF94 IJPEG_SMMU_IJPEG_ESYNR1

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

IJPEG_SMMU_IJPEG_ESYNR1

Bits	Name	Description
31	DCD	(decode) Indicates configuration port error due to invalid/unrecognized address (e.g., a reserved register address) Includes decode errors within both the global address space and the individual context bank address space

IJPEG_SMMU_IJPEG_ESYNR1 (cont.)

Bits	Name	Description
30	AC	(access control) Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO field of the errant request
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request)
15:12	ALEN	ALEN[3:0] field of the errant request
11	RESERVED_2	
10	ABURST	ABURST[1:0] field of the errant request
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request
7	AINST	AINST field of the errant request
6	APROTNS	APROTNS field of the errant request
5	APRIV	APRIV field of the errant request
4	AINNERSHARED	AINNERSHARED field of the errant request
3	ASHARED	ASHARED field of the errant request
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

14.26.1.6 SMMU revision register

0x078FFFF4 IJPEG_SMMU_IJPEG_REV

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the revision information for the SMMU core and wrapper.

IJPEG_SMMU_IJPEG_REV

Bits	Name	Description
31:12	RESERVED	

IJPEG_SMMU_IJPEG_REV (cont.)

Bits	Name	Description
11:8	WRAPPER	Wrapper version
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

14.26.1.7 SMMU implementation parameter register

0x078FFFF8 IJPEG_SMMU_IJPEG_IDR

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the parameter information for the SMMU core and wrapper

IJPEG_SMMU_IJPEG_IDR

Bits	Name	Description
31:24	NIRPT	NIRPT[7:0] Indicates number of context fault interrupt outputs (minus 1) supported by the System MMU Value can range from 0 - 255 (1 - 256 context fault interrupt outputs)
23:16	NCB	NCB[7:0] Indicates number of context banks (minus 1) supported by the System MMU Value can range from 0 - 254 (1 - 255 context banks)
15:12	TLBSIZE	TLBSIZE[3:0] Indicates log2(number of TLB entries) That is, number of TLB entries = 2 ** TLBSIZE
11	RESERVED	
10	HUM	Indicates whether or not TLB hit-under-miss behavior is supported
9	HTW	Indicates whether or not the System MMU supports hardware table walk If hardware table walk not supported (HTW=0), then software cannot set SMMU_CBn_ACTLR[TLBMCFG] to 0b10
8:0	NM2VCBMT	NM2VCBMT[8:0] Indicates number of M2VCBMT entries, with a maximum of 512 The bit width of the M2VCBMTIindex input (maximum value is 9) is equal to log base 2 of NM2VCBMT Allows for up to 7-bit MID field, plus NS-prot or other fields to select mapping [

0x078FFFFC IJPEG_SMMU_IJPEG_RPU_ACR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Using the incoming HVMID, this register controls access to the global register space.

IJPEG_SMMU_IJPEG_RPU_ACR

Bits	Name	Description
31:0	RWE	Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the entire block of registers within the SMMU's 4KB global address space, including this register itself. A VMID identified by this register is also permitted global access to all context banks. In practice, this register designates the VMID(s) that can act as SROT.

14.26.2 SMMU Context Bank Registers

There are a configurable number (1 to 9) of context banks in the SMMU. Each context bank consists of a set of registers in a unique 4KB address space.

14.26.2.1 SMMU context bank control registers

0x07800000+0x1000*n IJPEG_SMMU_IJPEG_CBn_SCTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank System Control Register controls various architected SMMU features

IJPEG_SMMU_IJPEG_CBn_SCTLR

Bits	Name	Description
31:5	RESERVED_2	
4	BE	Governs the order byte order or "endianness" of the page table entries. When set to 0, page table entries are in little endian format, so that their least significant byte is in byte 0 of the 32 bit entry. When set to 1, page table entries are in big endian format, so that their most significant byte is in byte 0 of the 32 bit entry.
3	RESERVED_1	Reserved for HAF, Hardware access flag. This bit governs whether the access flag is managed by hardware or software. The SMMU supports software access flag management only, so this bit is read-only and internally driven to 0.

IJPEG_SMMU_IJPEG_CBn_SCTLR (cont.)

Bits	Name	Description
2	AFE	Access flag enable. When AFE = 0, the access flag field is not supported and the AP[0] page table entry field acts as a bit of the overall AP[2:0] field to determining access permissions. When AFE = 1, the AP[0] page table entry field becomes the access flag, and the reduced number of access permission combinations is specified by AP2:1], and SMMU hardware will signal an Access Flag fault if a request targets a page for which the access flag is 0.
1	TRE	TEX remap enable. This bit governs the mapping of the page table entry TEX[2:0],C,B and SH fields into an SMMU TLB entry, and thus the translation of the AMEMTYPE[2:0], ASHARED and AINNERSHARED bus attributes. When TRE = 0, the TLB value is determined directly from the page table entry fields.
0	M	MMU enable bit. When set to 1, this context bank is enabled for translating requests. When set to 0, accesses bypass the TLB, and there is no address translation, access permission checking or attribute mapping. Incoming master requests are passed through unchanged.

0x07800004+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_ACTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank auxiliary control register controls various implementation specific features.

IJPEG_SMMU_IJPEG_CBn_ACTLR

Bits	Name	Description
31:19	RESERVED	
18	RESERVED_2	
17:16	V2PCFG	VA-to-PA configuration. Governs operation of VA-to-PA commands that miss in the TLB 0x0: terminate (Record TLB Miss context fault in SMMU_CBn_PAR) 0x1: software table update (Translate based on values in SMMU_CBn_TLBFLPTER and SMMU_CBn_TLBSLPTER) 0x2: hardware table walk (Translate based on value of PTE read from page table in memory) 0x3: reserved

IJPEG_SMMU_IJPEG_CBn_ACTLR (cont.)

Bits	Name	Description
15	TIPCF	Governs whether or not all subsequent requests using this context bank should be terminated if a prior context fault has occurred and has not yet been cleared from SMMU_CBn_FSR Accesses to other context banks proceed as normal 0x0: do not terminate (System MMU will attempt to process subsequent requests despite the presence of an existing context fault in SMMU_CBn_FSR. SMMU_CBn_FSR will be set if the subsequent access also encounters a context fault) 0x1: terminate (All subsequent accesses terminated by the System MMU as RAZ/WI, even if SMMU_CBn_ACTLR[TLBMCFG, CFCFG] configured for stall mode. SMMU_CBn_FSR set when access is terminated due to TIPCF = 1. Presence of SMMU_CBn_FSR when SMMU_CBn_ACTLR is 1 implies that the later exceptions must have been simply the forced terminations due to the prior context fault. Error optionally reported to the requesting master, according to the client port bus protocol, f SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus if SMMU_CBn_ACTLR is 1.)
14	CFCFG	(context fault configuration) Governs the behavior of all context faults except TLB miss TLB miss context faults are governed by SMMU_CBn_ACTLR[TLBMCFG] 0x0: terminate (Access terminates at the System MMU as RAZ/WI. Context fault exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x1: stall (Requesting master's access stalled while System MMU waits for managing processor to resolve context fault. Context fault exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode)

IJPEG_SMMU_IJPEG_CBn_ACTLR (cont.)

Bits	Name	Description
13:12	TLBMCFG	(TLB miss configuration) Governs the behavior of client accesses that miss in the TLB 0x0: pass-through (Access passed through to targeted slave without translation, attribute control, or access permission checking. Effectively, behavior is as if SMMU_CBn_SCTLR = 0 i.e., MMU disabled for this context bank. TLB miss not considered a context fault. TLB miss exception not recorded in SMMU_CBn_FSR. TLB miss exception not reported to requesting master. SMMU_contextFaultIrptReq interrupt output not asserted) 0x1: terminate (Access terminates at the System MMU as RAZ/WI,TLB miss exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x2: stall (Requesting master's access stalled while System MMU waits for managing processor to update TLB. TLB miss exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode) 0x3: HTW (Hardware table walk . Requesting master's access stalled while System MMU accesses page table. The is TLB updated and requesting master's access resumed after obtaining valid entry from page table. If translation fault, then access either terminates or stalls according to setting of SMMU_CBn_ACTLR)
11	DNLV2PA	(disable non-locking VA-to-PA allocation) Governs whether or not TLB misses due to non-locking VA-to-PA commands will allocate a new entry This field is ignored for locking VA-to-PA operations (SMMU_CBn_TLBLKCR[LKE] = 1)
10	DNA	(disable normal allocation) Governs whether or not TLB misses due to client port accesses will allocate a new entry
9:8	PRIVCFG	0x0: apriv (System MMU uses APRIV signal supplied by master as user/supervisor indicator 1 = supervisor) 0x1: reserved 0x2: User (System MMU ignores APRIV; treats all requests using this context bank as user) 0x3: Supervisor (System MMU ignores APRIV; treats all requests using this context bank as supervisor)

IJPEG_SMMU_IJPEG_CBn_ACTLR (cont.)

Bits	Name	Description
7:5	RESERVED_1	
4	RCNSH	(redirect cacheable-non-shareable) Governs whether or not cacheable accesses that are non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache, even though the locations are not being coherently shared with Scorpion-MP
3	RCISH	(redirect cacheable-inner-shareable) Governs whether or not cacheable accesses that are inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
2	RCOSH	(redirect cacheable-outer-shareable) Governs whether or not cacheable accesses that are outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
1	CFEIE	(context fault error interrupt enable) Governs whether or not client port request context faults are reported directly to the interrupt controller via the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus Interrupt output is asserted if SMMU_CBn_ACTLR[CFEIE] is 1 and any context fault bits are set in SMMU_CBn_FSR Such interrupts would generally be directed to the interrupt controller of whichever processor is currently managing this context bank of the System MMU Reset state : 0
0	CFERE	(context fault error report enable) Governs whether or not client port request context faults that are configured for terminate mode (or that are explicitly terminated after stall mode) are reported to the requesting master, according to the client port bus protocol All error types reported via AXI port will use decode error rather than slave error All context faults are recorded in SMMU_CBn_FSR, regardless of the value of this field.

0x07800008+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_CONTEXTIDR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context ID register holds the ASID associated with this context bank

IJPEG_SMMU_IJPEG_CBn_CONTEXTIDR

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Specifies the 8 bit ASID value assigned to this context bank. The ASID can be included in the key comparison of TLB entries. .

0x07800010+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_TTBR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR0 is used for low order virtual addresses, typically private pages for a given process.

IJPEG_SMMU_IJPEG_CBn_TTBR0

Bits	Name	Description
31:7	PA	BIts 31:7 of the physical address of the base of the page table. The actual LSB of the base address is bit 14-N, where N is set in register TTCR
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07800014+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_TTBR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR1 is used for high order virtual addresses, typically global pages for a given VMID, or kernal mappings.

The context bank auxiliary control register controls various implementation specific features.

IJPEG_SMMU_IJPEG_CBn_TTBR1

Bits	Name	Description
31:14	PA	BIts 31:14 of the physical address of the base of the page table.
13:7	RESERVED_2	
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED_1	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07800018+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_TTBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table control register, which specifies the size of the virtual address space that uses TTBR0.

IJPEG_SMMU_IJPEG_CBn_TTBCR

Bits	Name	Description
31:6	RESERVED_2	
5	PD1	Page disable 1; if this bit is set, hardware table walks attempting to use TTBR1will result in a first level descriptor translation fault. If clear, TTBR1 contents are used.
4	PD0	Page disable 0; if this bit is set, hardware table walks attempting to use TTBR0 will result in a first level descriptor translation fault. If clear, TTBR0 contents are used.
3	RESERVED_1	
2:0	N	N[2:0] specifies the number of upper order virtual address bits which must be 0 in order for translations to use the table pointed to by TTBR0. If any of these bits are non-zero, TTBR1 is used for the lookup. If N is 0, only TTBR0 is used.

0x0780001C+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_PAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The physical address register captures the physical address value resulting from the execution of a VA-to-PA command

Field definitions vary according to whether or not there is a context fault associated with the requested translation

IJPEG_SMMU_IJPEG_CBn_PAR

Bits	Name	Description
31:12	PAR_FAULT_INFO_312	
11	RESERVED_2	
10:9	PAR_FAULT_INFO_72	
8	RESERVED_1	
7:1	PAR_FAULT_INFO_71	Encoding varies according to value in FAULT field.
0	FAULT	(fault status) This field will be 1 when a context fault is associated with the requested translation, and 0, when there is no context fault associated with the requested translation.

0x07800020+0x1000*n IJPEG_SMMU_IJPEG_CBn_FSR, n=[0..1]

Type: Read/WriteClear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The Fault Status Register records status information for client accesses that encounter exceptions within the context bank, e.g. translation faults.This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data

This prevents inadvertent clearing of new faults when writing the register to clear an old fault

The presence of an asserted value on any bit in this register (except the SS bit) is what prompts the assertion (when enabled by SMMU_CBn_ACTLR[CFEIE]) of the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus

Therefore, these bits must be cleared by the interrupt handler

This is contrasted with the fields in the SMMU_CBn_FSYNRn registers, which are merely the "syndrome" of the fault indicated by SMMU_CBn_FSR

IJPEG_SMMU_IJPEG_CBn_FSR

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry

IJPEG_SMMU_IJPEG_CBn_FSR (cont.)

Bits	Name	Description
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07800024+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_FSRRESTORE, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Allows SW to force a value into the SMMU_CBn_FSR register.

IJPEG_SMMU_IJPEG_CBn_FSRRESTORE

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)

IJPEG_SMMU_IJPEG_CBn_FSRRESTORE (cont.)

Bits	Name	Description
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07800028+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_FAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The Fault Address Register records the virtual address of client accesses that encounter exceptions within the context bank, e.g. translation faults. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

IJPEG_SMMU_IJPEG_CBn_FAR

Bits	Name	Description
31:0	VA	VA[31:0] of errant client access

0x0780002C+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_FSYNR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

NOTE omission of VMID field from this register, as VMID can only be made visible to SROT, and not to general OS software that manages the context bank registers

IJPEG_SMMU_IJPEG_CBn_FSYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] (ATID field of errant request)

IJPEG_SMMU_IJPEG_CBn_FSYNR0 (cont.)

Bits	Name	Description
23:16	RESERVED	
15:13	ABID	ABID[2:0] (ABID field of errant request)
12:8	APID	APID[4:0] (APID field of errant request)
7:0	AMID	AMID[7:0] (AMID field of errant request)

0x07800030+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_FSYNR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

IJPEG_SMMU_IJPEG_CBn_FSYNR1

Bits	Name	Description
31:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO (AOOO field of the errant request)
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request
15:12	ALEN	ALEN[3:0]field of the errant request
11	RESERVED_2	
10	ABURST	field of the errant request
9	RESERVED_1	
8	AWRITE	field of the errant request
7	AINST	field of the errant request
6	APROTNS	field of the errant request
5	APRIV	field of the errant request
4	AINNERSHARED	(AINNERSHARED field of the errant request)
3	ASHARED	(ASHARED field of the errant request)

IJPEG_SMMU_IJPEG_CBn_FSYNR1 (cont.)

Bits	Name	Description
2:0	AMEMTYPE	AMEMTYPE[2:0] (AMEMTYPE field of the errant request)

0x07800034+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_PRRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs memory type and shareability attributes of requests that are both MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1)

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) and/or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, memory type encoding is as follows:

0b00 = strongly-ordered

0b01 = device

0b10 = normal

0b11 = reserved

IJPEG_SMMU_IJPEG_CBn_PRRR

Bits	Name	Description
31	NOS7	not-outer-shareable class 7
30	NOS6	not-outer-shareable class 6
29	NOS5	not-outer-shareable class 5
28	NOS4	not-outer-shareable class 4
27	NOS3	not-outer-shareable class 3
26	NOS2	not-outer-shareable class 2
25	NOS1	not-outer-shareable class 1
24	NOS0	not-outer-shareable class 0
23:20	RESERVED	

IJPEG_SMMU_IJPEG_CBn_PRRR (cont.)

Bits	Name	Description
19	SHNMSH1	(shareable attribute for normal memory accesses with SH=1) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1
18	SHNMSH0	(shareable attribute for normal memory accesses with SH=0) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0
17	SHDSH1	SHDSH1 (shareable attribute for device accesses with SH=1) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1 [
16	SHDSH0	SHDSH0 (shareable attribute for device accesses with SH=0) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0 [
15:14	MTC7	MTC7[1:0] (memory type class 0)
13:12	MTC6	MTC6[1:0] (memory type class 0)
11:10	MTC5	MTC5[1:0] (memory type class 0)
9:8	MTC4	MTC4[1:0] (memory type class 0)
7:6	MTC3	MTC3[1:0] (memory type class 0)
5:4	MTC2	MTC2[1:0] (memory type class 0)
3:2	MTC1	MTC1[1:0] (memory type class 0)
1:0	MTC0	MTC0[1:0] (memory type class 0)

0x07800038+0x1000*n IJPEG_SMMU_IJPEG_CBn_NMRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs the cache policy of MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1) requests for which the memory type is mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0) or the memory type is mapped to a type other than normal memory (SMMU_CBn_PRRR[MTCn] != 0b10)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, inner-cache and outer-cache policy encodings are as follows:

0b00 = non-cacheable

0b01 = cacheable, copy-back, write-allocate

0b10 = cacheable, write-through, write-no-allocate

0b11 = cacheable, copy-back, write-no-allocate

IJPEG_SMMU_IJPEG_CBn_NMRR

Bits	Name	Description
31:30	OCPC7	OCPC7[1:0] (inner-cache policy class 7)
29:28	OCPC6	OCPC6[1:0] (inner-cache policy class 6)
27:26	OCPC5	OCPC5[1:0] (inner-cache policy class 5)
25:24	OCPC4	OCPC4[1:0] (inner-cache policy class 4)
23:22	OCPC3	OCPC3[1:0] (inner-cache policy class 3)
21:20	OCPC2	OCPC2[1:0] (inner-cache policy class 2)
19:18	OCPC1	OCPC1[1:0] (inner-cache policy class 1)
17:16	OCPC0	OCPC0[1:0] (inner-cache policy class 0)
15:14	ICPC7	ICPC7[1:0] (inner-cache policy class 7)
13:12	ICPC6	ICPC6[1:0] (inner-cache policy class 6)
11:10	ICPC5	ICPC5[1:0] (inner-cache policy class 5)
9:8	ICPC4	ICPC4[1:0] (inner-cache policy class 4)
7:6	ICPC3	ICPC3[1:0] (inner-cache policy class 3)
5:4	ICPC2	ICPC2[1:0] (inner-cache policy class 2)
3:2	ICPC1	ICPC1[1:0] (inner-cache policy class 1)
1:0	ICPC0	ICPC0[1:0] (inner-cache policy class 0)

0x0780003C+0x1000*n IJPEG_SMMU_IJPEG_CBn_TLBLKCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB lock control register governs the TLB locking mechanism and TLB invalidate operations.Write access to this register is governed by SMMU_CR[TLBLKCRWE]

When SMMU_CR[TLBLKCRWE] is 0, writes to SMMU_CBn_TLBLKCR are ignored

Read access is still permitted

SROT can set SMMU_CR[TLBLKCRWE] to 1 to allow operating environment(s) to manage the TLB locking mechanism

Management amongst multiple operating environments must be coordinated via semaphore

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IJPEG_SMMU_IJPEG_CBn_TLBLKCR

Bits	Name	Description
31:24	RESERVED_2	
23:16	VICTIM	VICTIM[7:0] Indicates the TLB index at which the next normal (non-locking) allocation will occur Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context
15:8	FLOOR	FLOOR[7:0] Indicates the TLB index from which round-robin replacement on normal (non-locking) allocations occurs TLB entries at indices below this value are locked Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context banks
7:4	RESERVED_1	
3	TLBIVAACFG	(TLBIVAA configuration) TLBIVAACFG = 0 - flash-invalidate SMMU_CBn_TLBIVAA commands flash-invalidate the entire TLB, without regard to locking, security, address, and/or VMID value TLBIVAACFG = 1 - selective SMMU_CBn_TLBIVAA commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank VA field of TLB entry matches VA designated by SMMU_CBn_TLBIVAA command NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked

IJPEG_SMMU_IJPEG_CBn_TLBLKCR (cont.)

Bits	Name	Description
2	TLBIASIDCFG	(TLBIASID configuration) TLBIASIDCFG = 0 - flash-invalidate SMMU_CBn_TLBIASID commands flash-invalidate the entire TLB, without regard to locking, security, VMID, and/or ASID values TLBIASIDCFG = 1 - selective SMMU_CBn_TLBIASID commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command TLB entry is not global (NG field is 1) NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
1	TLBIALLCFG	(TLBIALL configuration) TLBIALLCFG = 0 - flash-invalidate SMMU_CBn_TLBIALL commands flash-invalidate the entire TLB, without regard to locking, security, and/or VMID value TLBIALLCFG = 1 - selective SMMU_CBn_TLBIALL commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked
0	LKE	(lock enable) Governs whether or not TLB entries established by VA-to-PA commands upon TLB misses are locked LKE = 0 (normal, non-locking) Allocate VA-to-PA TLB entry (if TLB miss) at the index specified by SMMU_CBn_TLBLKCR[VICTIM] Allocation is disabled if SMMU_CBn_ACTLR[DNLV2PA] is 1 Increment SMMU_CBn_TLBLKCR[VICTIM] by 1 (only if new entry allocated) Wrap back to the value of SMMU_CBn_TLBLKCR[FLOOR] when the last entry is written LKE = 1 (locking) Search TLB for specified VA and invalidate if found Provides atomicity between the invalidate and the new allocation within the locked region Allocate VA-to-PA TLB entry at the index specified by data operand bits 7:0 of the VA-to-PA command This value must be less than SMMU_CBn_TLBLKCR[FLOOR] in order for it to remain locked Allocation occurs even if non-locking allocation is disabled due to SMMU_CBn_ACTLR[DNLV2PA] = 1

0x07800040+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_V2PSR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The VA-to-PA status register records the hit/miss status and TLB index or V2Pxx and TLB invalidate commands.

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IJPEG_SMMU_IJPEG_CBn_V2PSR

Bits	Name	Description
31:16	RESERVED_2	
15:8	INDEX	INDEX[7:0] Indicates the index of the TLB entry associated with the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command If SMMU_CBn_V2PSR[HIT] is 0, then SMMU_CBn_V2PSR[INDEX] is the index to which the entry was allocated (if allocated at all) If SMMU_CBn_V2PSR[HIT] is 1, then SMMU_CBn_V2PSR[INDEX] is the index of the entry which hit
7:1	RESERVED_1	
0	HIT	Indicates whether or not there was a TLB hit (prior to allocation, if any) on the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command

0x07800044+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_TLBFLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB first level PTE register holds the first level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

This register (together with SMMU_CBn_TLBSLPTER) is used as the source of the translation information for VA-to-PA operations when the MMU is enabled (SMMU_CBn_SCTLR[M] = 1) and the operations are configured for software table update (SMMU_CBn_ACTLR[V2PCFG] = 0b01)

Field definitions vary according to the type of PTE (fault, page, section, or supersection), and come directly from the ARMv7 architecture's PTE formats

IJPEG_SMMU_IJPEG_CBn_TLBFLPTER

Bits	Name	Description
31:10	FL_PTE_HI	
9:5	RESERVED	
4:2	FL_PTE_LO	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	This field should be set to 0b00 or 0b11 to indicate that the translation should result in a context fault, and the rest of the fields are defined as indicated in this section If this field is not 0b00 or 0b11, then the PTE is of some other type (see other sections for the field definitions for those types)

0x07800048+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_TLBSLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB second level PTE register holds the second level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

Field definitions vary according to the type of PTE (fault, 64KB or 4KB), and come directly from the ARMv7 architecture's PTE format

IJPEG_SMMU_IJPEG_CBn_TLBSLPTER

Bits	Name	Description
31:2	SL_PTE	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	0x0: fault

0x0780004C+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_BFBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The burst fetch buffer configuration register governs the operation of the "burst fill" feature of the SMMU.

IJPEG_SMMU_IJPEG_CBn_BFBCR

Bits	Name	Description
31:12	STRIDE	(stride amount) 4KB-aligned value to be added to virtual address on demand TLB miss for filling subsequent BFB Stride of minimum 4KB alignment useful for preventing stride burst fetch until final PTE of the demand BFB entry is used
11:8	SLVIC	(second-level victim) Indicates the SLBFB index at which the next round-robin allocation will occur
7:4	FLVIC	(first-level victim) Indicates the FLBFB index at which the next round-robin allocation will occur
3	RESERVED	
2	SFVS	(stride-fetch victim selection) SFVS. = 0 (replace normal round-robin victim-selected entry) Useful when stride is larger than the VA space represented by the four PTEs in the demand BFB entry, but the client access pattern is for more than just the initial PTE in that demand BFB entry SFVS. = 1 (replace same BFB used by demand VA for which the stride burst is being performed) Useful when stride is the same as the VA space represented by an individual PTE in the demand BFB entry (such that the stride won't miss against the BFB until the last PTE of the demand BFB entry is accessed), and/or when the client access pattern only uses the initial PTE in the demand BFB entry
1	BFBSFE	(burst fetch buffer stride fetch enable) Enables stride burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Stride burst fetch is for the block of four PTEs associated with VA+stride VA is the "demanded" VA from the client (or VA-to-PA command) Stride value is specified by SMMU_CBn_BFBCR[STRIDE] Stride burst fetch only occurs if demand access for VA misses in TLB (could hit in BFB) and address VA+stride misses in both TLB and BFB
0	BFBDFE	(burst fetch buffer demand fetch enable) Enables demand burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Demand burst fetch is for the block of four PTEs associated with the "demanded" VA from the client (or VA-to-PA command) Demand burst fetch only occurs if demand access misses in both TLB and BFB

0x07800800+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_TLBIALL, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate all command register invalidates all TLB entries matching the VMID associated with this context bank. Data operand is ignored.

IJPEG_SMMU_IJPEG_CBn_TLBIALL

Bits	Name	Description
31:0	RESERVED	

0x07800804+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_TLBIASID, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by ASID command register invalidates TLB entries matching the specified ASID and matching the VMID associated with this context bank.Invalidates TLB entries which are associated with the designated ASID and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIASIDCFG] governs whether command flash-invalidates entire TLB array or just the entries matching the VMID, ASID, and security state

TLBIASIDCFG = 0 - flash-invalidate

SMMU_CBn_TLBIASID command flash-invalidates the entire TLB, without regard to locking, security, VMID, and/or ASID values

TLBIASIDCFG = 1 - selective

SMMU_CBn_TLBIASID command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command data operand

TLB entry is not global (NG field is 1)

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command

Locking is not considered (matching entries are invalidated even if locked)

ASID field of command specifies the ASID value of the TLB entries to be invalidated

IJPEG_SMMU_IJPEG_CBn_TLBIASID

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Actual ASID value

0x07800808+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_TLBIVA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA command invalidates TLB entries matching the designated VA, ASID and the VMID associated with this context bank.

Matching entry determined as follows:

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIVA command data operand (or TLB entry is global - NG field is 0)

VA field of TLB entry matches VA value designated by the SMMU_CBn_TLBIVA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIVA command

Locking is not considered (matching entry is invalidated even if locked)

Data operand specifies the VA and ASID value of the TLB entry to be invalidated

IJPEG_SMMU_IJPEG_CBn_TLBIVA

Bits	Name	Description
31:12	VA	VA[31:12]
11:8	RESERVED	
7:0	ASID	ASID[7:0] value

0x0780080C+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_TLBIVAA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA all ASIDS command invalidates TLB entries matching the designated VA and the VMID associated with this context bank, regardless of ASID.Invalidates TLB entries which are associated with the designated VA, regardless of ASID, and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIVAACFG] governs whether command flash-invalidates entire TLB array or just the non-locked entries matching the VMID, ASID, and security state

TLBIVAACFG = 0 - flash-invalidate

SMMU_CBn_TLBIVAA command flash-invalidates the entire TLB, without regard to locking, security, address, and/or VMID value

TLBIVAACFG = 1 - selective

SMMU_CBn_TLBIVAA command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

VA field of TLB entry matches VA designated by the SMMU_CBn_TLBIVAA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command

Entry is unlocked

IJPEG_SMMU_IJPEG_CBn_TLBIVAA

Bits	Name	Description
31:12	VA	VA[31:12]
11:0	RESERVED	

0x07800810+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_V2PRR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

IJPEG_SMMU_IJPEG_CBn_V2PRR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07800814+0x1000*n IJPEG_SMMU_IJPEG_CBn_V2PPW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

IJPEG_SMMU_IJPEG_CBn_V2PPW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07800818+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_V2PUR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

IJPEG_SMMU_IJPEG_CBn_V2PUR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x0780081C+0x1000*n IJPEG_SMMU_IJPEG_CBn_V2PUW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

.Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

IJPEG_SMMU_IJPEG_CBn_V2PUW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	

IJPEG_SMMU_IJPEG_CBn_V2PUW (cont.)

Bits	Name	Description
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07800820+ 0x1000*n IJPEG_SMMU_IJPEG_CBn_RESUME, n=[0..1]

Type: Write/command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB resume command causes the SMMU to resume operation after a stalled access..

IJPEG_SMMU_IJPEG_CBn_RESUME

Bits	Name	Description
31:1	RESERVED	
0	TNR	Terminate/not retry When TNR is written as 0, indicates that the stalled access should be retried by the system MMU. When written as 1, indicates that this stalled transaction is terminated by the system MMU. The error is optionally reported to the requesting master, using the client port bus protocol, if SMMU_CNn_ACTLR[CFERE] == 1. Interrupt optionally remains asserted via SMMU_M2VCBRn[IRPTINDX] selected SMMU_contextFaultIrptReq bit, only if SMMU_CBn_ACTLR[CFEIE] is 1, and only if SMMU_CBn_FSR has not been cleared by software priori to issuing this command..

14.27 VFE SMMU Registers (0x07900000 SMMU_VFE_BASE)

This section contains VFE SMMU registers.

14.27.1 SMMU Global Registers

14.27.1.1 SMMU VMID/CBNDX mapping registers

0x079FF000+ 0x4*n VFE_SMMU_VFE_M2VCBRn, n=[0..15]

Type: Read/Write
Clock: AXI_CLK
Reset State: Undefined

SMMU_M2VCBRm registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

VFE_SMMU_VFE_M2VCBRn

Bits	Name	Description
31:28	RESERVED_2	
27:25	BPMEMTYPE	(bypass memory type) Supplies the AMEMTYPE attributes for client requests which bypass the System MMU when SMMU_M2VCBRn[BPMTCFG] = 1 See reference section for AMEMTYPE encoding definitions
24	BPMTCFG	(bypass memory type configuration) Governs the memory type (AMEMTYPE) attributes of client requests which bypass the System MMU BPMTCFG = 0 - use AMEMTYPE Bypass requests use AMEMTYPE signal supplied by client master BPMTCFG = 1 - use SMMU_M2VCBRn[BPMEMTYPE] Bypass requests use SMMU_M2VCBRn[BPMEMTYPE] Reset state : 0
23:22	NSCFG	(non-secure configuration) Governs the incoming security designation of client requests NSCFG = 0b00 - use APROTNS Use APROTNS signal supplied by client master NSCFG = 0b01 - reserved NSCFG = 0b10 - secure System MMU ignores APROTNS; treats all requests as secure NSCFG = 0b11 - non-secure System MMU ignores APROTNS; treats all requests as non-secure Reset state : 0

VFE_SMMU_VFE_M2VCBRn (cont.)

Bits	Name	Description
21:20	BPSHCFG	(bypass shareability configuration) Governs the shareability realm (ASHARED and AINNERSHARED) attributes of client requests which bypass the System MMU BPSHCFG = 0b00 - use ASHARED and AINNERSHARED Bypass requests use ASHARED and AINNERSHARED signals supplied by client master BPSHCFG = 0b01 - outer-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 0 BPSHCFG = 0b10 - inner-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 1 BPSHCFG = 0b11 - non-shareable Bypass requests set ASHARED = 0, AINNERSHARED = 0 Reset state : 0
19	BPRCNSH	(bypass redirect cacheable-non-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache Reset state : 0
18	BPRCISH	(bypass redirect cacheable-inner-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0
17	BPRCOSH	(bypass redirect cacheable-outer-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0

VFE_SMMU_VFE_M2VCBRn (cont.)

Bits	Name	Description
16	BYPASSD	Bypass disable for this index Governs whether or not client port accesses using this mapping table entry are actually permitted to "bypass" the System MMU when such bypass is indicated (either due to CBNDX = 255 or due to the master asserting the "SMMU bypass" input) This field is ignored (and operates as if it were 0) if SMMU_CR[CLIENTPD] is 1 BYPASSD = 0 - bypass enabled Bypass requests truly bypass the System MMU and "pass-through" to the fabric (no translation, access control, or attribute generation) No cycle of latency for System MMU context bank access Bypass request not considered an error Bypass request error not recorded in SMMU_ESR[BYPASS] Bypass error not reported to requesting master SMMU_rpuErrIrptReq interrupt output not asserted Client accesses still reference M2VCBMT to get VMID value for presentation to fabric BYPASSD = 1 - bypass disabled System MMU terminates the access as RAZ/WI Bypass request is considered an error Bypass request error is recorded in SMMU_ESR[BYPASS] If SMMU_CR[RPUERE] is 1, then bypass error reported to requesting master according to the client port bus protocol If SMMU_CR[RPUEIE] is 1, then SMMU_rpuErrIrptReq interrupt output asserted
15:8	CBNDX	Context bank index Context bank index associated with the M2VCBMT index CBNDX = 255 indicates no context bank assigned ("bypass")
7:5	RESERVED_1	
4:0	VMID	Virtual machine ID VMID value associated with the M2VCBMT index Must be programmed consistently with the SMMU_CBACRn[CBVMID] field for the context bank designated by SMMU_M2VCBRm[CBNDX]

14.27.1.2 SMMU context bank access control registers

0x079FF800+ 0x4*n VFE_SMMU_VFE_CBACRn, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs configuration port access to the associated context bank registers.

VFE_SMMU_VFE_CBACRn

Bits	Name	Description
31:24	IRPTNDX	(interrupt index) Interrupt output number used for context faults associated with this context bank (use SMMU_contextFaultIrptReq[IRPTNDX])
23:21	RESERVED	
20:16	CBVMID	(context bank VMID) Specifies the VMID with which the client masters using the context bank are associated Must be programmed consistently with the M2VCBMT entries that are configured to use the associated context bank This field is used by configuration port commands that need the context bank's VMID value in order to access the TLB (e.g., SMMU_CBn_TLBIVMID, SMMU_CBn_V2Pxx)
15:10	RESERVED_2	
9	RWGE	Read/write global enable. Setting this bit allows access to the context bank registers from any VMID
8	RWE	Read/write enable. Indicates that the RWVMID field is valid.
7:5	RESERVED_1	
4:0	RWVMID	Specifies owner VMID with full read/write access to the registers in the associated context bank "n".

14.27.1.3 SMMU TLB software access registers

0x079FFE00 VFE_SMMU_VFE_TLBRSW

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Writing to this address requests that the TLB entry at INDEX be read into the SMMU_TLBTRn registers

VFE_SMMU_VFE_TLBRSW

Bits	Name	Description
31:10	RESERVED	

VFE_SMMU_VFE_TLBRSW (cont.)

Bits	Name	Description
9:8	TLBBFBS	This field selects the TLB, TFBFB, SLBFB 0x0: Selecting TLB 0x1: Not defined 0x2: Selecting FL BFB 0x3: Selecting SL BFB
7:0	INDEX	TLB index to be read.

0x079FFE80 VFE_SMMU_VFE_TLBTR0

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

This register holds part of TLB entry read by the last TLBRSW command.

VFE_SMMU_VFE_TLBTR0

Bits	Name	Description
31:23	RESERVED_4	
22:20	DPSIZC	3 bit decode page size field from CAM-side of TLB CAM-RAM) Same determination and encoding as for DPSIZR The CAM-side copy of this field is used for hit/miss determination in the TLB CAM array
19	RESERVED_3	
18:16	DPSIZR	(3 bit decode page size field from RAM-side of TLB CAM-RAM) Determined from the size fields of the page table entry Encodes the page size as follows: all other values reserved/unused The RAM-side copy of this field is used for virtual ’ physical address formation 0x0: 4KB page 0x1: 64KB page 0x3: 1MB page 0x7: 16MB page
15:12	RESERVED_2	
11	MT2	(memory type bit 2) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[2] attribute bus on the request output of the System MMU

VFE_SMMU_VFE_TLBTR0 (cont.)

Bits	Name	Description
10	MT1	(memory type bit 1) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[1] attribute bus on the request output of the System MMU
9	MT0	(memory type bit 0) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[0] attribute bus on the request output of the System MMU
8	SH	(shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's outer-shareable realm This field becomes the ASHARED attribute on the request output of the System MMU
7	ISH	(inner-shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's inner-shareable realm This field becomes the AINNERSHARED attribute on the request output of the System MMU
6	NSDESC	(non-secure descriptor) This TLB entry field is a modified version of the corresponding bit of the page table entry Qualified by the NS-prot attribute of the incoming request which prompted the allocation of the TLB entry, such that if the incoming NS-prot attribute was 1 (non-secure), then the NS-desc field of the page table entry was ignored, and the NS-desc field of the TLB entry was forced to 1 Indicates whether the associated memory page contains secure (NS-desc=0) or non-secure (NS-desc=1) information This field becomes the NS-prot attribute on the request output of the System MMU
5	RESERVED_1	

VFE_SMMU_VFE_TLBTR0 (cont.)

Bits	Name	Description
4	XN	(execute never permission) This TLB entry field comes directly from the corresponding bit of the page table entry
3	UW	(user write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
2	UR	(user read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
1	PW	(privileged write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
0	PR	(privileged read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]

0x079FFE84 VFE_SMMU_VFE_TLBTR1

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

VFE_SMMU_VFE_TLBTR1

Bits	Name	Description
31:12	PA	Physical address [31:12] field of the TLB entry
11:5	RESERVED	
4:0	VMID	VMID [4:0]field of the TLB entry)

0x079FFE88 VFE_SMMU_VFE_TLBTR2

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

VFE_SMMU_VFE_TLBTR2

Bits	Name	Description
31:12	VA	virtual address field [31:12] of the TLB entry
11	RESERVED	
10	NG	(not global field from page table entry) Indicates whether the page is private to the specified ASID (NG=1) or global to all ASIDs within the VMID using this context bank (NG=0)
9	NSTID	(non-secure tag ID field of the TLB entry) Indicates whether the TLB entry belongs to the secure world (NSTID=0) or the non-secure world (NSTID=1) This field is comned against the incoming NS-prot attribute of the master request as part of TLB hit/miss determination
8	V	valid field of the TLB entry
7:0	ASID	ASID[7:0] field of the TLB entry

0x079FFE8C VFE_SMMU_VFE_TESTBUSCR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

Governs which signals (if any) from the system SMMU core or wrapper design hierarchy are sent out to the system via a testbus for diagnostic, and also to the system profiling and diagnostic monitor(SPDM).

VFE_SMMU_VFE_TESTBUSCR

Bits	Name	Description
31:28	SPDM3SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[3]
27:24	SPDM2SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[2]
23:20	SPDM1SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[1]
19:16	SPDM0SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[0]
15:14	TBHSEL	Testbus highselect It governs which set of signals are to testbus[31:16] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL

VFE_SMMU_VFE_TESTBUSCR (cont.)

Bits	Name	Description
13:12	TBSLSEL	Testbus low select It governs which set of signals are to testbus[15:0] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL
11:10	RESERVED_2	
9:8	WGSEL	Wrapper group select It selects a particular group of signals from the SMMU wrapper hierarchy WGSEL = 0b00 - wrapper signal group 0 WGSEL = 0b01 - wrapper signal group 1 WGSEL = 0b10 - wrapper signal group 2 WGSEL = 0b11 - reserved
7:2	RESERVED_1	
1	SPDMBE	SPDM test enable Reset state : 0
0	TBE	Testbus enable, which governs whether the testbus is driven with all 0s or with the configured signals Reset state : 0

0x079FFEFC VFE_SMMU_VFE_VR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: 32'h0000_0000

Note that the DCPBP/DCPPP bits prevent the pipelining of the next transaction when the current transaction is a bypass/pass-through transaction. That is, they add one more cycle of delay between the current and next transactions.

Also note that when we are in global bypass (SMMU_CR[CLIENTPD]=1), these bits should have NO effect, or at least no effect between client transactions, they can have an effect between config and client transactions is appropriate. We must be able to continue to perform fully pipelined transactions when the client port is disabled altogether.

VFE_SMMU_VFE_VR0

Bits	Name	Description
31:3	RESERVED	

VFE_SMMU_VFE_VR0 (cont.)

Bits	Name	Description
2	DCPPT	Disable client pipelining for client operations in pass-through mode Reset state : 0
1	DCPBP	Disable client pipelining for client operations in bypass mode Reset state : 0
0	DCP	Disable client pipelining Reset state : 0

0x079FFF00 VFE_SMMU_VFE_TLBIALL

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries.

VFE_SMMU_VFE_TLBIALL

Bits	Name	Description
31:0	EXEC	Writing any value to this register invalidates all TLB entries, as specified by the contents of SMMU_CR[TLBIALLCFG]

0x079FFF04 VFE_SMMU_VFE_TLBIVMID

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries matching the IVMID value. Precise function is governed by SMMU_CR[TLBIALLCFG].

VFE_SMMU_VFE_TLBIVMID

Bits	Name	Description
31:5	RESERVED	
4:0	IVMID	Designates VMID[4:0] value of entries to be invalidated.

14.27.1.4 SMMU configuration registers

0x079FFF80 VFE_SMMU_VFE_CR

Type: Read/Write
Clock: AXI_BUS_CLOCK

Global configuration register.

VFE_SMMU_VFE_CR

Bits	Name	Description
31:10	RESERVED_2	
9	RESERVED_1	Reset state : 0
8	TLBIVMIDCFG	TLBIVMID configuration control. When set to 0,flash-invalidate, SMMU_TLBIVMID commands flash-invalidate the entire TLB, without regard to locking ,security and VMID value. When set to 1, selective, SMMU_TLBIVMID invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and VMID field matching the VMID specified by SMMU_TLBIVMID command. Reset state : X
7	TLBIALLCFG	TLBIALL configuration control. When set to 0, flash-invalidate, SMMU_TLBIALL commands flash-invalidate the entire TLB, without regard to locking and/or security. When set to 1, selective, SMMU_TLBIALL invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and are unlocked. Reset state : X
6	TLBLKCRWE	TLBLKCR write enable. When set to 0, writes to SMMU_CBn_TLBLKCR are ignored. When set to 1, allows operating environments to manage the TLB locking mechanism directly. Management amounst multiple operating environments must be coordinated externally between themselves. Reset state : X
5	STALLD	Global disable for stall mode. When set to 1, context bank stall modes are ignored and operate as terminate mode. Reset state : X
4	CLIENTPD	Client port disable. When set, all client accesses are forced to bypass the system MMU. There is no translation. access control, or attribute generation. This bit overrides individual SMMU_M2VCBRn[BYPASSD] settings; client requests are bypassed, even if SMMU_M2VCBRn[BYPASSD] is set to 1. Bypass request errors are not recorded in SMMU_ESR, nor reported to requesting masters. The SMMU_rpuErrIrptReq interrupt output signal is not asserted. Reset state : 1

VFE_SMMU_VFE_CR (cont.)

Bits	Name	Description
3	DCDEE	When set to 0, configuration port decode errors do not set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn are not updated. When set to 1, configuration port decode errors set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn updated with address and syndrome of error. Reset state : X
2	RPUEIE	When set, configuration port errors and client port bypass errors are reported directly to the interrupt controller via the SMMU_rputErrIrptReq interrupt output signal. Interrupt output is asserted if SMMU_CR[RPUIE_EN] is 1 and ANY bit is set in SMMU_ESR register. Reset state : 0
1	RPUERE	When set, SMMU reports configuration port errors and client port bypass errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via AXI port will use decode error, rather than slave error. Regardless of the value of this field both configuration port errors and client port bypass request errors are terminated by the SMMU as RAZ/WI, and are recorded in SMMU_ESR register. Reset state : X
0	RPUE	When set, all configuration port accesses are checked against SMMUX_RPU_ACR and/or the SMMUX_CBACRn registers for access permissions. Reset state : 0

14.27.1.5 SMMU error report registers

0x079FFF84 VFE_SMMU_VFE_EAR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: unknown

When there is an error, holds the physical address of the errant transaction.

VFE_SMMU_VFE_EAR

Bits	Name	Description
31:0	PA	Physical address[31:0]

0x079FFF88 VFE_SMMU_VFE_ESR

Type: Read/Write to clear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This register has read/write clear access. Reads return the value in the register, a write with a 1 set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

VFE_SMMU_VFE_ESR

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x079FFF8C VFE_SMMU_VFE_ESRRESTORE

Type: Write
Clock: RPM_BUS_CLK
Reset State: Undefined

This register is an aliased address for SMMU_ESR, but it allows direct write access. In this way, diagnostic software can cause an error to be generated and reported.

VFE_SMMU_VFE_ESRRESTORE

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	

VFE_SMMU_VFE_ESRRESTORE (cont.)

Bits	Name	Description
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x079FFF90 VFE_SMMU_VFE_ESYNR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

VFE_SMMU_VFE_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request
15:0	AMID	AMID[15:0] field of errant request

0x079FFF94 VFE_SMMU_VFE_ESYNR1

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

VFE_SMMU_VFE_ESYNR1

Bits	Name	Description
31	DCD	(decode) Indicates configuration port error due to invalid/unrecognized address (e.g., a reserved register address) Includes decode errors within both the global address space and the individual context bank address space

VFE_SMMU_VFE_ESYNR1 (cont.)

Bits	Name	Description
30	AC	(access control) Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO field of the errant request
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request)
15:12	ALEN	ALEN[3:0] field of the errant request
11	RESERVED_2	
10	ABURST	ABURST[1:0] field of the errant request
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request
7	AINST	AINST field of the errant request
6	APROTNS	APROTNS field of the errant request
5	APRIV	APRIV field of the errant request
4	AINNERSHARED	AINNERSHARED field of the errant request
3	ASHARED	ASHARED field of the errant request
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

14.27.1.6 SMMU revision register

0x079FFFF4 VFE_SMMU_VFE_REV

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the revision information for the SMMU core and wrapper.

VFE_SMMU_VFE_REV

Bits	Name	Description
31:12	RESERVED	
11:8	WRAPPER	Wrapper version
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

14.27.1.7 SMMU implementation parameter register

0x079FFFF8 VFE_SMMU_VFE_IDR

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the parameter information for the SMMU core and wrapper

VFE_SMMU_VFE_IDR

Bits	Name	Description
31:24	NIRPT	NIRPT[7:0] Indicates number of context fault interrupt outputs (minus 1) supported by the System MMU Value can range from 0 - 255 (1 - 256 context fault interrupt outputs)
23:16	NCB	NCB[7:0] Indicates number of context banks (minus 1) supported by the System MMU Value can range from 0 - 254 (1 - 255 context banks)
15:12	TLBSIZE	TLBSIZE[3:0] Indicates log2(number of TLB entries) That is, number of TLB entries = 2 ** TLBSIZE
11	RESERVED	
10	HUM	Indicates whether or not TLB hit-under-miss behavior is supported
9	HTW	Indicates whether or not the System MMU supports hardware table walk If hardware table walk not supported (HTW=0), then software cannot set SMMU_CBn_ACTLR[TLBMCFG] to 0b10
8:0	NM2VCBMT	NM2VCBMT[8:0] Indicates number of M2VCBMT entries, with a maximum of 512 The bit width of the M2VCBMTIindex input (maximum value is 9) is equal to log base 2 of NM2VCBMT Allows for up to 7-bit MID field, plus NS-prot or other fields to select mapping [

0x079FFFFC VFE_SMMU_VFE_RPU_ACR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Using the incoming HVMID, this register controls access to the global register space.

VFE_SMMU_VFE_RPU_ACR

Bits	Name	Description
31:0	RWE	Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the entire block of registers within the SMMU's 4KB global address space, including this register itself. A VMID identified by this register is also permitted global access to all context banks. In practice, this register designates the VMID(s) that can act as SROT.

14.27.2 SMMU Context Bank Registers

There are a configurable number (1 to 9) of context banks in the SMMU. Each context bank consists of a set of registers in a unique 4KB address space.

14.27.2.1 SMMU context bank control registers

0x07900000+0x1000*n VFE_SMMU_VFE_CBn_SCTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank System Control Register controls various architected SMMU features

VFE_SMMU_VFE_CBn_SCTLR

Bits	Name	Description
31:5	RESERVED_2	
4	BE	Governs the order byte order or "endianness" of the page table entries. When set to 0, page table entries are in little endian format, so that their least significant byte is in byte 0 of the 32 bit entry. When set to 1, page table entries are in big endian format, so that their most significant byte is in byte 0 of the 32 bit entry.
3	RESERVED_1	Reserved for HAF, Hardware access flag. This bit governs whether the access flag is managed by hardware or software. The SMMU supports software access flag management only, so this bit is read-only and internally driven to 0.

VFE_SMMU_VFE_CBn_SCTLR (cont.)

Bits	Name	Description
2	AFE	Access flag enable. When AFE = 0, the access flag field is not supported and the AP[0] page table entry field acts as a bit of the overall AP[2:0] field to determining access permissions. When AFE = 1, the AP[0] page table entry field becomes the access flag, and the reduced number of access permission combinations is specified by AP2:1], and SMMU hardware will signal an Access Flag fault if a request targets a page for which the access flag is 0.
1	TRE	TEX remap enable. This bit governs the mapping of the page table entry TEX[2:0],C,B and SH fields into an SMMU TLB entry, and thus the translation of the AMEMTYPE[2:0], ASHARED and AINNERSHARED bus attributes. When TRE = 0, the TLB value is determined directly from the page table entry fields.
0	M	MMU enable bit. When set to 1, this context bank is enabled for translating requests. When set to 0, accesses bypass the TLB, and there is no address translation, access permission checking or attribute mapping. Incoming master requests are passed through unchanged.

0x07900004+ 0x1000*n VFE_SMMU_VFE_CBn_ACTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank auxiliary control register controls various implementation specific features.

VFE_SMMU_VFE_CBn_ACTLR

Bits	Name	Description
31:19	RESERVED	
18	RESERVED_2	
17:16	V2PCFG	VA-to-PA configuration. Governs operation of VA-to-PA commands that miss in the TLB 0x0: terminate (Record TLB Miss context fault in SMMU_CBn_PAR) 0x1: software table update (Translate based on values in SMMU_CBn_TLBFLPTER and SMMU_CBn_TLBSLPTER) 0x2: hardware table walk (Translate based on value of PTE read from page table in memory) 0x3: reserved

VFE_SMMU_VFE_CBn_ACTLR (cont.)

Bits	Name	Description
15	TIPCF	Governs whether or not all subsequent requests using this context bank should be terminated if a prior context fault has occurred and has not yet been cleared from SMMU_CBn_FSR Accesses to other context banks proceed as normal 0x0: do not terminate (System MMU will attempt to process subsequent requests despite the presence of an existing context fault in SMMU_CBn_FSR. SMMU_CBn_FSR will be set if the subsequent access also encounters a context fault) 0x1: terminate (All subsequent accesses terminated by the System MMU as RAZ/WI, even if SMMU_CBn_ACTLR[TLBMCFG, CFCFG] configured for stall mode. SMMU_CBn_FSR set when access is terminated due to TIPCF = 1. Presence of SMMU_CBn_FSR when SMMU_CBn_ACTLR is 1 implies that the later exceptions must have been simply the forced terminations due to the prior context fault. Error optionally reported to the requesting master, according to the client port bus protocol, f SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus if SMMU_CBn_ACTLR is 1.)
14	CFCFG	(context fault configuration) Governs the behavior of all context faults except TLB miss TLB miss context faults are governed by SMMU_CBn_ACTLR[TLBMCFG] 0x0: terminate (Access terminates at the System MMU as RAZ/WI. Context fault exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x1: stall (Requesting master's access stalled while System MMU waits for managing processor to resolve context fault. Context fault exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode)

VFE_SMMU_VFE_CBn_ACTLR (cont.)

Bits	Name	Description
13:12	TLBMCFG	(TLB miss configuration) Governs the behavior of client accesses that miss in the TLB 0x0: pass-through (Access passed through to targeted slave without translation, attribute control, or access permission checking. Effectively, behavior is as if SMMU_CBn_SCTLR = 0 i.e., MMU disabled for this context bank. TLB miss not considered a context fault. TLB miss exception not recorded in SMMU_CBn_FSR. TLB miss exception not reported to requesting master. SMMU_contextFaultIrptReq interrupt output not asserted) 0x1: terminate (Access terminates at the System MMU as RAZ/WI,TLB miss exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x2: stall (Requesting master's access stalled while System MMU waits for managing processor to update TLB. TLB miss exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode) 0x3: HTW (Hardware table walk . Requesting master's access stalled while System MMU accesses page table. The is TLB updated and requesting master's access resumed after obtaining valid entry from page table. If translation fault, then access either terminates or stalls according to setting of SMMU_CBn_ACTLR)
11	DNLV2PA	(disable non-locking VA-to-PA allocation) Governs whether or not TLB misses due to non-locking VA-to-PA commands will allocate a new entry This field is ignored for locking VA-to-PA operations (SMMU_CBn_TLBLKCR[LKE] = 1)
10	DNA	(disable normal allocation) Governs whether or not TLB misses due to client port accesses will allocate a new entry
9:8	PRIVCFG	0x0: apriv (System MMU uses APRIV signal supplied by master as user/supervisor indicator 1 = supervisor) 0x1: reserved 0x2: User (System MMU ignores APRIV; treats all requests using this context bank as user) 0x3: Supervisor (System MMU ignores APRIV; treats all requests using this context bank as supervisor)

VFE_SMMU_VFE_CBn_ACTLR (cont.)

Bits	Name	Description
7:5	RESERVED_1	
4	RCNSH	(redirect cacheable-non-shareable) Governs whether or not cacheable accesses that are non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache, even though the locations are not being coherently shared with Scorpion-MP
3	RCISH	(redirect cacheable-inner-shareable) Governs whether or not cacheable accesses that are inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
2	RCOSH	(redirect cacheable-outer-shareable) Governs whether or not cacheable accesses that are outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
1	CFEIE	(context fault error interrupt enable) Governs whether or not client port request context faults are reported directly to the interrupt controller via the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus Interrupt output is asserted if SMMU_CBn_ACTLR[CFEIE] is 1 and any context fault bits are set in SMMU_CBn_FSR Such interrupts would generally be directed to the interrupt controller of whichever processor is currently managing this context bank of the System MMU Reset state : 0
0	CFERE	(context fault error report enable) Governs whether or not client port request context faults that are configured for terminate mode (or that are explicitly terminated after stall mode) are reported to the requesting master, according to the client port bus protocol All error types reported via AXI port will use decode error rather than slave error All context faults are recorded in SMMU_CBn_FSR, regardless of the value of this field.

0x07900008+ 0x1000*n VFE_SMMU_VFE_CBn_CONTEXTIDR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context ID register holds the ASID associated with this context bank

VFE_SMMU_VFE_CBn_CONTEXTIDR

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Specifies the 8 bit ASID value assigned to this context bank. The ASID can be included in the key comparison of TLB entries. .

0x07900010+ 0x1000*n VFE_SMMU_VFE_CBn_TTBR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR0 is used for low order virtual addresses, typically private pages for a given process.

VFE_SMMU_VFE_CBn_TTBR0

Bits	Name	Description
31:7	PA	BIts 31:7 of the physical address of the base of the page table. The actual LSB of the base address is bit 14-N, where N is set in register TTCR
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07900014+ 0x1000*n VFE_SMMU_VFE_CBn_TTBR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR1 is used for high order virtual addresses, typically global pages for a given VMID, or kernal mappings.

The context bank auxiliary control register controls various implementation specific features.

VFE_SMMU_VFE_CBn_TTBR1

Bits	Name	Description
31:14	PA	BIts 31:14 of the physical address of the base of the page table.
13:7	RESERVED_2	
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED_1	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07900018+ 0x1000*n VFE_SMMU_VFE_CBn_TTBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table control register, which specifies the size of the virtual address space that uses TTBR0.

VFE_SMMU_VFE_CBn_TTBCR

Bits	Name	Description
31:6	RESERVED_2	
5	PD1	Page disable 1; if this bit is set, hardware table walks attempting to use TTBR1will result in a first level descriptor translation fault. If clear, TTBR1 contents are used.
4	PD0	Page disable 0; if this bit is set, hardware table walks attempting to use TTBR0 will result in a first level descriptor translation fault. If clear, TTBR0 contents are used.
3	RESERVED_1	
2:0	N	N[2:0] specifies the number of upper order virtual address bits which must be 0 in order for translations to use the table pointed to by TTBR0. If any of these bits are non-zero, TTBR1 is used for the lookup. If N is 0, only TTBR0 is used.

0x0790001C+ 0x1000*n VFE_SMMU_VFE_CBn_PAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The physical address register captures the physical address value resulting from the execution of a VA-to-PA command

Field definitions vary according to whether or not there is a context fault associated with the requested translation

VFE_SMMU_VFE_CBn_PAR

Bits	Name	Description
31:12	PAR_FAULT_INFO_312	
11	RESERVED_2	
10:9	PAR_FAULT_INFO_72	
8	RESERVED_1	
7:1	PAR_FAULT_INFO_71	Encoding varies according to value in FAULT field.
0	FAULT	(fault status) This field will be 1 when a context fault is associated with the requested translation, and 0, when there is no context fault associated with the requested translation.

0x07900020+0x1000*n VFE_SMMU_VFE_CBn_FSR, n=[0..1]

Type: Read/WriteClear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The Fault Status Register records status information for client accesses that encounter exceptions within the context bank, e.g. translation faults.This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data

This prevents inadvertent clearing of new faults when writing the register to clear an old fault

The presence of an asserted value on any bit in this register (except the SS bit) is what prompts the assertion (when enabled by SMMU_CBn_ACTLR[CFEIE]) of the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus

Therefore, these bits must be cleared by the interrupt handler

This is contrasted with the fields in the SMMU_CBn_FSYNRn registers, which are merely the "syndrome" of the fault indicated by SMMU_CBn_FSR

VFE_SMMU_VFE_CBn_FSR

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry

VFE_SMMU_VFE_CBn_FSR (cont.)

Bits	Name	Description
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07900024+ 0x1000*n VFE_SMMU_VFE_CBn_FSRRESTORE, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Allows SW to force a value into the SMMU_CBn_FSR register.

VFE_SMMU_VFE_CBn_FSRRESTORE

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)

VFE_SMMU_VFE_CBn_FSRRESTORE (cont.)

Bits	Name	Description
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07900028+ 0x1000*n VFE_SMMU_VFE_CBn_FAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The Fault Address Register records the virtual address of client accesses that encounter exceptions within the context bank, e.g. translation faults. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

VFE_SMMU_VFE_CBn_FAR

Bits	Name	Description
31:0	VA	VA[31:0] of errant client access

0x0790002C+ 0x1000*n VFE_SMMU_VFE_CBn_FSYNR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

NOTE omission of VMID field from this register, as VMID can only be made visible to SROT, and not to general OS software that manages the context bank registers

VFE_SMMU_VFE_CBn_FSYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] (ATID field of errant request)

VFE_SMMU_VFE_CBn_FSYNR0 (cont.)

Bits	Name	Description
23:16	RESERVED	
15:13	ABID	ABID[2:0] (ABID field of errant request)
12:8	APID	APID[4:0] (APID field of errant request)
7:0	AMID	AMID[7:0] (AMID field of errant request)

0x07900030+ 0x1000*n VFE_SMMU_VFE_CBn_FSYNR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

VFE_SMMU_VFE_CBn_FSYNR1

Bits	Name	Description
31:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO (AOOO field of the errant request)
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request
15:12	ALEN	ALEN[3:0]field of the errant request
11	RESERVED_2	
10	ABURST	field of the errant request
9	RESERVED_1	
8	AWRITE	field of the errant request
7	AINST	field of the errant request
6	APROTNS	field of the errant request
5	APRIV	field of the errant request
4	AINNERSHARED	(AINNERSHARED field of the errant request)
3	ASHARED	(ASHARED field of the errant request)

VFE_SMMU_VFE_CBn_FSYNR1 (cont.)

Bits	Name	Description
2:0	AMEMTYPE	AMEMTYPE[2:0] (AMEMTYPE field of the errant request)

0x07900034+ 0x1000*n VFE_SMMU_VFE_CBn_PRRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs memory type and shareability attributes of requests that are both MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1)

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) and/or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, memory type encoding is as follows:

0b00 = strongly-ordered

0b01 = device

0b10 = normal

0b11 = reserved

VFE_SMMU_VFE_CBn_PRRR

Bits	Name	Description
31	NOS7	not-outer-shareable class 7
30	NOS6	not-outer-shareable class 6
29	NOS5	not-outer-shareable class 5
28	NOS4	not-outer-shareable class 4
27	NOS3	not-outer-shareable class 3
26	NOS2	not-outer-shareable class 2
25	NOS1	not-outer-shareable class 1
24	NOS0	not-outer-shareable class 0
23:20	RESERVED	

VFE_SMMU_VFE_CBn_PRRR (cont.)

Bits	Name	Description
19	SHNMSH1	(shareable attribute for normal memory accesses with SH=1) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1
18	SHNMSH0	(shareable attribute for normal memory accesses with SH=0) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0
17	SHDSH1	SHDSH1 (shareable attribute for device accesses with SH=1) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1 [
16	SHDSH0	SHDSH0 (shareable attribute for device accesses with SH=0) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0 [
15:14	MTC7	MTC7[1:0] (memory type class 0)
13:12	MTC6	MTC6[1:0] (memory type class 0)
11:10	MTC5	MTC5[1:0] (memory type class 0)
9:8	MTC4	MTC4[1:0] (memory type class 0)
7:6	MTC3	MTC3[1:0] (memory type class 0)
5:4	MTC2	MTC2[1:0] (memory type class 0)
3:2	MTC1	MTC1[1:0] (memory type class 0)
1:0	MTC0	MTC0[1:0] (memory type class 0)

0x07900038+0x1000*n VFE_SMMU_VFE_CBn_NMRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs the cache policy of MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1) requests for which the memory type is mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0) or the memory type is mapped to a type other than normal memory (SMMU_CBn_PRRR[MTCn] != 0b10)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, inner-cache and outer-cache policy encodings are as follows:

0b00 = non-cacheable

0b01 = cacheable, copy-back, write-allocate

0b10 = cacheable, write-through, write-no-allocate

0b11 = cacheable, copy-back, write-no-allocate

VFE_SMMU_VFE_CBn_NMRR

Bits	Name	Description
31:30	OCPC7	OCPC7[1:0] (inner-cache policy class 7)
29:28	OCPC6	OCPC6[1:0] (inner-cache policy class 6)
27:26	OCPC5	OCPC5[1:0] (inner-cache policy class 5)
25:24	OCPC4	OCPC4[1:0] (inner-cache policy class 4)
23:22	OCPC3	OCPC3[1:0] (inner-cache policy class 3)
21:20	OCPC2	OCPC2[1:0] (inner-cache policy class 2)
19:18	OCPC1	OCPC1[1:0] (inner-cache policy class 1)
17:16	OCPC0	OCPC0[1:0] (inner-cache policy class 0)
15:14	ICPC7	ICPC7[1:0] (inner-cache policy class 7)
13:12	ICPC6	ICPC6[1:0] (inner-cache policy class 6)
11:10	ICPC5	ICPC5[1:0] (inner-cache policy class 5)
9:8	ICPC4	ICPC4[1:0] (inner-cache policy class 4)
7:6	ICPC3	ICPC3[1:0] (inner-cache policy class 3)
5:4	ICPC2	ICPC2[1:0] (inner-cache policy class 2)
3:2	ICPC1	ICPC1[1:0] (inner-cache policy class 1)
1:0	ICPC0	ICPC0[1:0] (inner-cache policy class 0)

0x0790003C+0x1000*n VFE_SMMU_VFE_CBn_TLBLKCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB lock control register governs the TLB locking mechanism and TLB invalidate operations.Write access to this register is governed by SMMU_CR[TLBLKCRWE]

When SMMU_CR[TLBLKCRWE] is 0, writes to SMMU_CBn_TLBLKCR are ignored

Read access is still permitted

SROT can set SMMU_CR[TLBLKCRWE] to 1 to allow operating environment(s) to manage the TLB locking mechanism

Management amongst multiple operating environments must be coordinated via semaphore

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VFE_SMMU_VFE_CBn_TLBLKCR

Bits	Name	Description
31:24	RESERVED_2	
23:16	VICTIM	VICTIM[7:0] Indicates the TLB index at which the next normal (non-locking) allocation will occur Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context
15:8	FLOOR	FLOOR[7:0] Indicates the TLB index from which round-robin replacement on normal (non-locking) allocations occurs TLB entries at indices below this value are locked Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context banks
7:4	RESERVED_1	
3	TLBIVAACFG	(TLBIVAA configuration) TLBIVAACFG = 0 - flash-invalidate SMMU_CBn_TLBIVAA commands flash-invalidate the entire TLB, without regard to locking, security, address, and/or VMID value TLBIVAACFG = 1 - selective SMMU_CBn_TLBIVAA commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank VA field of TLB entry matches VA designated by SMMU_CBn_TLBIVAA command NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked

VFE_SMMU_VFE_CBn_TLBLKCR (cont.)

Bits	Name	Description
2	TLBIASIDCFG	(TLBIASID configuration) TLBIASIDCFG = 0 - flash-invalidate SMMU_CBn_TLBIASID commands flash-invalidate the entire TLB, without regard to locking, security, VMID, and/or ASID values TLBIASIDCFG = 1 - selective SMMU_CBn_TLBIASID commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command TLB entry is not global (NG field is 1) NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
1	TLBIALLCFG	(TLBIALL configuration) TLBIALLCFG = 0 - flash-invalidate SMMU_CBn_TLBIALL commands flash-invalidate the entire TLB, without regard to locking, security, and/or VMID value TLBIALLCFG = 1 - selective SMMU_CBn_TLBIALL commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked
0	LKE	(lock enable) Governs whether or not TLB entries established by VA-to-PA commands upon TLB misses are locked LKE = 0 (normal, non-locking) Allocate VA-to-PA TLB entry (if TLB miss) at the index specified by SMMU_CBn_TLBLKCR[VICTIM] Allocation is disabled if SMMU_CBn_ACTLR[DNLV2PA] is 1 Increment SMMU_CBn_TLBLKCR[VICTIM] by 1 (only if new entry allocated) Wrap back to the value of SMMU_CBn_TLBLKCR[FLOOR] when the last entry is written LKE = 1 (locking) Search TLB for specified VA and invalidate if found Provides atomicity between the invalidate and the new allocation within the locked region Allocate VA-to-PA TLB entry at the index specified by data operand bits 7:0 of the VA-to-PA command This value must be less than SMMU_CBn_TLBLKCR[FLOOR] in order for it to remain locked Allocation occurs even if non-locking allocation is disabled due to SMMU_CBn_ACTLR[DNLV2PA] = 1

0x07900040+0x1000*n VFE_SMMU_VFE_CBn_V2PSR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The VA-to-PA status register records the hit/miss status and TLB index or V2Pxx and TLB invalidate commands.

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VFE_SMMU_VFE_CBn_V2PSR

Bits	Name	Description
31:16	RESERVED_2	
15:8	INDEX	INDEX[7:0] Indicates the index of the TLB entry associated with the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command If SMMU_CBn_V2PSR[HIT] is 0, then SMMU_CBn_V2PSR[INDEX] is the index to which the entry was allocated (if allocated at all) If SMMU_CBn_V2PSR[HIT] is 1, then SMMU_CBn_V2PSR[INDEX] is the index of the entry which hit
7:1	RESERVED_1	
0	HIT	Indicates whether or not there was a TLB hit (prior to allocation, if any) on the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command

0x07900044+0x1000*n VFE_SMMU_VFE_CBn_TLBFLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB first level PTE register holds the first level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

This register (together with SMMU_CBn_TLBSLPTER) is used as the source of the translation information for VA-to-PA operations when the MMU is enabled (SMMU_CBn_SCTLR[M] = 1) and the operations are configured for software table update (SMMU_CBn_ACTLR[V2PCFG] = 0b01)

Field definitions vary according to the type of PTE (fault, page, section, or supersection), and come directly from the ARMv7 architecture's PTE formats

VFE_SMMU_VFE_CBn_TLBFLPTER

Bits	Name	Description
31:10	FL_PTE_HI	
9:5	RESERVED	
4:2	FL_PTE_LO	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	This field should be set to 0b00 or 0b11 to indicate that the translation should result in a context fault, and the rest of the fields are defined as indicated in this section If this field is not 0b00 or 0b11, then the PTE is of some other type (see other sections for the field definitions for those types)

0x07900048+ 0x1000*n VFE_SMMU_VFE_CBn_TLBSLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB second level PTE register holds the second level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

Field definitions vary according to the type of PTE (fault, 64KB or 4KB), and come directly from the ARMv7 architecture's PTE format

VFE_SMMU_VFE_CBn_TLBSLPTER

Bits	Name	Description
31:2	SL_PTE	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	0x0: fault

0x0790004C+ 0x1000*n VFE_SMMU_VFE_CBn_BFBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The burst fetch buffer configuration register governs the operation of the "burst fill" feature of the SMMU.

VFE_SMMU_VFE_CBn_BFBCR

Bits	Name	Description
31:12	STRIDE	(stride amount) 4KB-aligned value to be added to virtual address on demand TLB miss for filling subsequent BFB Stride of minimum 4KB alignment useful for preventing stride burst fetch until final PTE of the demand BFB entry is used
11:8	SLVIC	(second-level victim) Indicates the SLBFB index at which the next round-robin allocation will occur
7:4	FLVIC	(first-level victim) Indicates the FLBFB index at which the next round-robin allocation will occur
3	RESERVED	
2	SFVS	(stride-fetch victim selection) SFVS. = 0 (replace normal round-robin victim-selected entry) Useful when stride is larger than the VA space represented by the four PTEs in the demand BFB entry, but the client access pattern is for more than just the initial PTE in that demand BFB entry SFVS. = 1 (replace same BFB used by demand VA for which the stride burst is being performed) Useful when stride is the same as the VA space represented by an individual PTE in the demand BFB entry (such that the stride won't miss against the BFB until the last PTE of the demand BFB entry is accessed), and/or when the client access pattern only uses the initial PTE in the demand BFB entry
1	BFBSFE	(burst fetch buffer stride fetch enable) Enables stride burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Stride burst fetch is for the block of four PTEs associated with VA+stride VA is the "demanded" VA from the client (or VA-to-PA command) Stride value is specified by SMMU_CBn_BFBCR[STRIDE] Stride burst fetch only occurs if demand access for VA misses in TLB (could hit in BFB) and address VA+stride misses in both TLB and BFB
0	BFBDFE	(burst fetch buffer demand fetch enable) Enables demand burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Demand burst fetch is for the block of four PTEs associated with the "demanded" VA from the client (or VA-to-PA command) Demand burst fetch only occurs if demand access misses in both TLB and BFB

0x07900800+ 0x1000*n VFE_SMMU_VFE_CBn_TLBIALL, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate all command register invalidates all TLB entries matching the VMID associated with this context bank. Data operand is ignored.

VFE_SMMU_VFE_CBn_TLBIALL

Bits	Name	Description
31:0	RESERVED	

0x07900804+ 0x1000*n VFE_SMMU_VFE_CBn_TLBIASID, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by ASID command register invalidates TLB entries matching the specified ASID and matching the VMID associated with this context bank.Invalidates TLB entries which are associated with the designated ASID and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIASIDCFG] governs whether command flash-invalidates entire TLB array or just the entries matching the VMID, ASID, and security state

TLBIASIDCFG = 0 - flash-invalidate

SMMU_CBn_TLBIASID command flash-invalidates the entire TLB, without regard to locking, security, VMID, and/or ASID values

TLBIASIDCFG = 1 - selective

SMMU_CBn_TLBIASID command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command data operand

TLB entry is not global (NG field is 1)

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command

Locking is not considered (matching entries are invalidated even if locked)

ASID field of command specifies the ASID value of the TLB entries to be invalidated

VFE_SMMU_VFE_CBn_TLBIASID

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Actual ASID value

0x07900808+ 0x1000*n VFE_SMMU_VFE_CBn_TLBIVA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA command invalidates TLB entries matching the designated VA, ASID and the VMID associated with this context bank.

Matching entry determined as follows:

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIVA command data operand (or TLB entry is global - NG field is 0)

VA field of TLB entry matches VA value designated by the SMMU_CBn_TLBIVA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIVA command

Locking is not considered (matching entry is invalidated even if locked)

Data operand specifies the VA and ASID value of the TLB entry to be invalidated

VFE_SMMU_VFE_CBn_TLBIVA

Bits	Name	Description
31:12	VA	VA[31:12]
11:8	RESERVED	
7:0	ASID	ASID[7:0] value

0x0790080C+ 0x1000*n VFE_SMMU_VFE_CBn_TLBIVAA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA all ASIDS command invalidates TLB entries matching the designated VA and the VMID associated with this context bank, regardless of ASID.Invalidates TLB entries which are associated with the designated VA, regardless of ASID, and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIVAACFG] governs whether command flash-invalidates entire TLB array or just the non-locked entries matching the VMID, ASID, and security state

TLBIVAACFG = 0 - flash-invalidate

SMMU_CBn_TLBIVAA command flash-invalidates the entire TLB, without regard to locking, security, address, and/or VMID value

TLBIVAACFG = 1 - selective

SMMU_CBn_TLBIVAA command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

VA field of TLB entry matches VA designated by the SMMU_CBn_TLBIVAA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command

Entry is unlocked

VFE_SMMU_VFE_CBn_TLBIVAA

Bits	Name	Description
31:12	VA	VA[31:12]
11:0	RESERVED	

0x07900810+ 0x1000*n VFE_SMMU_VFE_CBn_V2PRR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

VFE_SMMU_VFE_CBn_V2PRR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07900814+0x1000*n VFE_SMMU_VFE_CBn_V2PPW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

VFE_SMMU_VFE_CBn_V2PPW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07900818+ 0x1000*n VFE_SMMU_VFE_CBn_V2PUR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

VFE_SMMU_VFE_CBn_V2PUR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x0790081C+ 0x1000*n VFE_SMMU_VFE_CBn_V2PUW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

.Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

VFE_SMMU_VFE_CBn_V2PUW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	

VFE_SMMU_VFE_CBn_V2PUW (cont.)

Bits	Name	Description
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07900820+ 0x1000*n VFE_SMMU_VFE_CBn_RESUME, n=[0..1]

Type: Write/command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB resume command causes the SMMU to resume operation after a stalled access..

VFE_SMMU_VFE_CBn_RESUME

Bits	Name	Description
31:1	RESERVED	
0	TNR	Terminate/not retry When TNR is written as 0, indicates that the stalled access should be retried by the system MMU. When written as 1, indicates that this stalled transaction is terminated by the system MMU. The error is optionally reported to the requesting master, using the client port bus protocol, if SMMU_CNn_ACTLR[CFERE] == 1. Interrupt optionally remains asserted via SMMU_M2VCBRn[IRPTINDX] selected SMMU_contextFaultIrptReq bit, only if SMMU_CBn_ACTLR[CFEIE] is 1, and only if SMMU_CBn_FSR has not been cleared by software priori to issuing this command..

14.28 VCODEC A SS1080P 0 SMMU Registers (0x07A00000 SMMU_SS1080P_0_BASE)

This section contains VCODEC A SS1080P 0 SMMU registers.

14.28.1 SMMU Global Registers

14.28.1.1 SMMU VMID/CBNDX mapping registers

0x07AFF000+0x4*n SS1080P_0_SMMU_VCODEC_A_M2VCBRn, n=[0..15]

Type: Read/Write
Clock: AXI_CLK
Reset State: Undefined

SMMU_M2VCBRm registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

SS1080P_0_SMMU_VCODEC_A_M2VCBRn

Bits	Name	Description
31:28	RESERVED_2	
27:25	BPMEMTYPE	(bypass memory type) Supplies the AMEMTYPE attributes for client requests which bypass the System MMU when SMMU_M2VCBRn[BPMTCFG] = 1 See reference section for AMEMTYPE encoding definitions
24	BPMTCFG	(bypass memory type configuration) Governs the memory type (AMEMTYPE) attributes of client requests which bypass the System MMU BPMTCFG = 0 - use AMEMTYPE Bypass requests use AMEMTYPE signal supplied by client master BPMTCFG = 1 - use SMMU_M2VCBRn[BPMEMTYPE] Bypass requests use SMMU_M2VCBRn[BPMEMTYPE] Reset state : 0
23:22	NSCFG	(non-secure configuration) Governs the incoming security designation of client requests NSCFG = 0b00 - use APROTNS Use APROTNS signal supplied by client master NSCFG = 0b01 - reserved NSCFG = 0b10 - secure System MMU ignores APROTNS; treats all requests as secure NSCFG = 0b11 - non-secure System MMU ignores APROTNS; treats all requests as non-secure Reset state : 0

SS1080P_0_SMMU_VCODEC_A_M2VCBRn (cont.)

Bits	Name	Description
21:20	BPSHCFG	(bypass shareability configuration) Governs the shareability realm (ASHARED and AINNERSHARED) attributes of client requests which bypass the System MMU BPSHCFG = 0b00 - use ASHARED and AINNERSHARED Bypass requests use ASHARED and AINNERSHARED signals supplied by client master BPSHCFG = 0b01 - outer-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 0 BPSHCFG = 0b10 - inner-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 1 BPSHCFG = 0b11 - non-shareable Bypass requests set ASHARED = 0, AINNERSHARED = 0 Reset state : 0
19	BPRCNSH	(bypass redirect cacheable-non-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache Reset state : 0
18	BPRCISH	(bypass redirect cacheable-inner-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0
17	BPRCOSH	(bypass redirect cacheable-outer-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0

SS1080P_0_SMMU_VCODEC_A_M2VCBRn (cont.)

Bits	Name	Description
16	BYPASSD	Bypass disable for this index Governs whether or not client port accesses using this mapping table entry are actually permitted to "bypass" the System MMU when such bypass is indicated (either due to CBNDX = 255 or due to the master asserting the "SMMU bypass" input) This field is ignored (and operates as if it were 0) if SMMU_CR[CLIENTPD] is 1 BYPASSD = 0 - bypass enabled Bypass requests truly bypass the System MMU and "pass-through" to the fabric (no translation, access control, or attribute generation) No cycle of latency for System MMU context bank access Bypass request not considered an error Bypass request error not recorded in SMMU_ESR[BYPASS] Bypass error not reported to requesting master SMMU_rpuErrIrptReq interrupt output not asserted Client accesses still reference M2VCBMT to get VMID value for presentation to fabric BYPASSD = 1 - bypass disabled System MMU terminates the access as RAZ/WI Bypass request is considered an error Bypass request error is recorded in SMMU_ESR[BYPASS] If SMMU_CR[RPUERE] is 1, then bypass error reported to requesting master according to the client port bus protocol If SMMU_CR[RPUEIE] is 1, then SMMU_rpuErrIrptReq interrupt output asserted
15:8	CBNDX	Context bank index Context bank index associated with the M2VCBMT index CBNDX = 255 indicates no context bank assigned ("bypass")
7:5	RESERVED_1	
4:0	VMID	Virtual machine ID VMID value associated with the M2VCBMT index Must be programmed consistently with the SMMU_CBACRn[CBVMID] field for the context bank designated by SMMU_M2VCBRm[CBNDX]

14.28.1.2 SMMU context bank access control registers

0x07AFF800+0x4*n SS1080P_0_SMMU_VCODEC_A_CBACRn, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs configuration port access to the associated context bank registers.

SS1080P_0_SMMU_VCODEC_A_CBACRn

Bits	Name	Description
31:24	IRPTNDX	(interrupt index) Interrupt output number used for context faults associated with this context bank (use SMMU_contextFaultIrptReq[IRPTNDX])
23:21	RESERVED	
20:16	CBVMID	(context bank VMID) Specifies the VMID with which the client masters using the context bank are associated Must be programmed consistently with the M2VCBMT entries that are configured to use the associated context bank This field is used by configuration port commands that need the context bank's VMID value in order to access the TLB (e.g., SMMU_CBn_TLBIVMID, SMMU_CBn_V2Pxx)
15:10	RESERVED_2	
9	RWGE	Read/write global enable. Setting this bit allows access to the context bank registers from any VMID
8	RWE	Read/write enable. Indicates that the RWVMID field is valid.
7:5	RESERVED_1	
4:0	RWVMID	Specifies owner VMID with full read/write access to the registers in the associated context bank "n".

14.28.1.3 SMMU TLB software access registers

0x07AFFE00 SS1080P_0_SMMU_VCODEC_A_TLBRSW

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Writing to this address requests that the TLB entry at INDEX be read into the SMMU_TLBTRn registers

SS1080P_0_SMMU_VCODEC_A_TLBRSW

Bits	Name	Description
31:10	RESERVED	

SS1080P_0_SMMU_VCODEC_A_TLBRSW (cont.)

Bits	Name	Description
9:8	TLBBFBS	This field selects the TLB, TFBFB, SLBFB 0x0: Selecting TLB 0x1: Not defined 0x2: Selecting FL BFB 0x3: Selecting SL BFB
7:0	INDEX	TLB index to be read.

0x07AFFE80 SS1080P_0_SMMU_VCODEC_A_TLBTR0

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

This register holds part of TLB entry read by the last TLBRSW command.

SS1080P_0_SMMU_VCODEC_A_TLBTR0

Bits	Name	Description
31:23	RESERVED_4	
22:20	DPSIZC	3 bit decode page size field from CAM-side of TLB CAM-RAM) Same determination and encoding as for DPSIZR The CAM-side copy of this field is used for hit/miss determination in the TLB CAM array
19	RESERVED_3	
18:16	DPSIZR	(3 bit decode page size field from RAM-side of TLB CAM-RAM) Determined from the size fields of the page table entry Encodes the page size as follows: all other values reserved/unused The RAM-side copy of this field is used for virtual ’ physical address formation 0x0: 4KB page 0x1: 64KB page 0x3: 1MB page 0x7: 16MB page
15:12	RESERVED_2	
11	MT2	(memory type bit 2) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[2] attribute bus on the request output of the System MMU

SS1080P_0_SMMU_VCODEC_A_TLBTR0 (cont.)

Bits	Name	Description
10	MT1	(memory type bit 1) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[1] attribute bus on the request output of the System MMU
9	MT0	(memory type bit 0) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[0] attribute bus on the request output of the System MMU
8	SH	(shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's outer-shareable realm This field becomes the ASHARED attribute on the request output of the System MMU
7	ISH	(inner-shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's inner-shareable realm This field becomes the AINNERSHARED attribute on the request output of the System MMU
6	NSDESC	(non-secure descriptor) This TLB entry field is a modified version of the corresponding bit of the page table entry Qualified by the NS-prot attribute of the incoming request which prompted the allocation of the TLB entry, such that if the incoming NS-prot attribute was 1 (non-secure), then the NS-desc field of the page table entry was ignored, and the NS-desc field of the TLB entry was forced to 1 Indicates whether the associated memory page contains secure (NS-desc=0) or non-secure (NS-desc=1) information This field becomes the NS-prot attribute on the request output of the System MMU
5	RESERVED_1	

SS1080P_0_SMMU_VCODEC_A_TLBTR0 (cont.)

Bits	Name	Description
4	XN	(execute never permission) This TLB entry field comes directly from the corresponding bit of the page table entry
3	UW	(user write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
2	UR	(user read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
1	PW	(privileged write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
0	PR	(privileged read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]

0x07AFFE84 SS1080P_0_SMMU_VCODEC_A_TLBTR1

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

SS1080P_0_SMMU_VCODEC_A_TLBTR1

Bits	Name	Description
31:12	PA	Physical address [31:12] field of the TLB entry
11:5	RESERVED	
4:0	VMID	VMID [4:0]field of the TLB entry)

0x07AFFE88 SS1080P_0_SMMU_VCODEC_A_TLBTR2

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

SS1080P_0_SMMU_VCODEC_A_TLBTR2

Bits	Name	Description
31:12	VA	virtual address field [31:12] of the TLB entry
11	RESERVED	
10	NG	(not global field from page table entry) Indicates whether the page is private to the specified ASID (NG=1) or global to all ASIDs within the VMID using this context bank (NG=0)
9	NSTID	(non-secure tag ID field of the TLB entry) Indicates whether the TLB entry belongs to the secure world (NSTID=0) or the non-secure world (NSTID=1) This field is comned against the incoming NS-prot attribute of the master request as part of TLB hit/miss determination
8	V	valid field of the TLB entry
7:0	ASID	ASID[7:0] field of the TLB entry

0x07AFFE8C SS1080P_0_SMMU_VCODEC_A_TESTBUSCR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

Governs which signals (if any) from the system SMMU core or wrapper design hierarchy are sent out to the system via a testbus for diagnostic, and also to the system profiling and diagnostic monitor(SPDM).

SS1080P_0_SMMU_VCODEC_A_TESTBUSCR

Bits	Name	Description
31:28	SPDM3SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[3]
27:24	SPDM2SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[2]
23:20	SPDM1SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[1]
19:16	SPDM0SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[0]
15:14	TBHSEL	Testbus highselect It governs which set of signals are to testbus[31:16] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL

SS1080P_0_SMMU_VCODEC_A_TESTBUSCR (cont.)

Bits	Name	Description
13:12	TBSLSEL	Testbus low select It governs which set of signals are to testbus[15:0] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL
11:10	RESERVED_2	
9:8	WGSEL	Wrapper group select It selects a particular group of signals from the SMMU wrapper hierarchy WGSEL = 0b00 - wrapper signal group 0 WGSEL = 0b01 - wrapper signal group 1 WGSEL = 0b10 - wrapper signal group 2 WGSEL = 0b11 - reserved
7:2	RESERVED_1	
1	SPDMBE	SPDM test enable Reset state : 0
0	TBE	Testbus enable, which governs whether the testbus is driven with all 0s or with the configured signals Reset state : 0

0x07AFFEFC SS1080P_0_SMMU_VCODEC_A_VR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: 32'h0000_0000

Note that the DCPBP/DCPPP bits prevent the pipelining of the next transaction when the current transaction is a bypass/pass-through transaction. That is, they add one more cycle of delay between the current and next transactions.

Also note that when we are in global bypass (SMMU_CR[CLIENTPD]=1), these bits should have NO effect, or at least no effect between client transactions, they can have an effect between config and client transactions is appropriate. We must be able to continue to perform fully pipelined transactions when the client port is disabled altogether.

SS1080P_0_SMMU_VCODEC_A_VR0

Bits	Name	Description
31:3	RESERVED	

SS1080P_0_SMMU_VCODEC_A_VR0 (cont.)

Bits	Name	Description
2	DCPPT	Disable client pipelining for client operations in pass-through mode Reset state : 0
1	DCPBP	Disable client pipelining for client operations in bypass mode Reset state : 0
0	DCP	Disable client pipelining Reset state : 0

0x07AFFF00 SS1080P_0_SMMU_VCODEC_A_TLBIALL

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries.

SS1080P_0_SMMU_VCODEC_A_TLBIALL

Bits	Name	Description
31:0	EXEC	Writing any value to this register invalidates all TLB entries, as specified by the contents of SMMU_CR[TLBIALLCFG]

0x07AFFF04 SS1080P_0_SMMU_VCODEC_A_TLBIVMID

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries matching the IVMID value. Precise function is governed by SMMU_CR[TLBIALLCFG].

SS1080P_0_SMMU_VCODEC_A_TLBIVMID

Bits	Name	Description
31:5	RESERVED	
4:0	IVMID	Designates VMID[4:0] value of entries to be invalidated.

14.28.1.4 SMMU configuration registers

0x07AFFF80 SS1080P_0_SMMU_VCODEC_A_CR

Type: Read/Write
Clock: AXI_BUS_CLOCK

Global configuration register.

SS1080P_0_SMMU_VCODEC_A_CR

Bits	Name	Description
31:10	RESERVED_2	
9	RESERVED_1	Reset state : 0
8	TLBIVMIDCFG	TLBIVMID configuration control. When set to 0,flash-invalidate, SMMU_TLBIVMID commands flash-invalidate the entire TLB, without regard to locking ,security and VMID value. When set to 1, selective, SMMU_TLBIVMID invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and VMID field matching the VMID specified by SMMU_TLBIVMID command. Reset state : X
7	TLBIALLCFG	TLBIALL configuration control. When set to 0, flash-invalidate, SMMU_TLBIALL commands flash-invalidate the entire TLB, without regard to locking and/or security. When set to 1, selective, SMMU_TLBIALL invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and are unlocked. Reset state : X
6	TLBLKCRWE	TLBLKCR write enable. When set to 0, writes to SMMU_CBn_TLBLKCR are ignored. When set to 1, allows operating environments to manage the TLB locking mechanism directly. Management amounst multiple operating environments must be coordinated externally between themselves. Reset state : X
5	STALLD	Global disable for stall mode. When set to 1, context bank stall modes are ignored and operate as terminate mode. Reset state : X
4	CLIENTPD	Client port disable. When set, all client accesses are forced to bypass the system MMU. There is no translation. access control, or attribute generation. This bit overrides individual SMMU_M2VCBRn[BYPASSD] settings; client requests are bypassed, even if SMMU_M2VCBRn[BYPASSD] is set to 1. Bypass request errors are not recorded in SMMU_ESR, nor reported to requesting masters. The SMMU_rpuErrIrptReq interrupt output signal is not asserted. Reset state : 1

SS1080P_0_SMMU_VCODEC_A_CR (cont.)

Bits	Name	Description
3	DCDEE	When set to 0, configuration port decode errors do not set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn are not updated. When set to 1, configuration port decode errors set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn updated with address and syndrome of error. Reset state : X
2	RPUEIE	When set, configuration port errors and client port bypass errors are reported directly to the interrupt controller via the SMMU_rputErrIrptReq interrupt output signal. Interrupt output is asserted if SMMU_CR[RPUIE_EN] is 1 and ANY bit is set in SMMU_ESR register. Reset state : 0
1	RPUERE	When set, SMMU reports configuration port errors and client port bypass errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via AXI port will use decode error, rather than slave error. Regardless of the value of this field both configuration port errors and client port bypass request errors are terminated by the SMMU as RAZ/WI, and are recorded in SMMU_ESR register. Reset state : X
0	RPUE	When set, all configuration port accesses are checked against SMMUX_RPU_ACR and/or the SMMUX_CBACRn registers for access permissions. Reset state : 0

14.28.1.5 SMMU error report registers

0x07AFFF84 SS1080P_0_SMMU_VCODEC_A_EAR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: unknown

When there is an error, holds the physical address of the errant transaction.

SS1080P_0_SMMU_VCODEC_A_EAR

Bits	Name	Description
31:0	PA	Physical address[31:0]

0x07AFFF88 SS1080P_0_SMMU_VCODEC_A_ESR

Type: Read/Write to clear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This register has read/write clear access. Reads return the value in the register, a write with a 1 set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

SS1080P_0_SMMU_VCODEC_A_ESR

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x07AFFF8C SS1080P_0_SMMU_VCODEC_A_ESRRESTORE

Type: Write
Clock: RPM_BUS_CLK
Reset State: Undefined

This register is an aliased address for SMMU_ESR, but it allows direct write access. In this way, diagnostic software can cause an error to be generated and reported.

SS1080P_0_SMMU_VCODEC_A_ESRRESTORE

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	

SS1080P_0_SMMU_VCODEC_A_ESRRESTORE (cont.)

Bits	Name	Description
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x07AFFF90 SS1080P_0_SMMU_VCODEC_A_ESYNR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

SS1080P_0_SMMU_VCODEC_A_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request
15:0	AMID	AMID[15:0] field of errant request

0x07AFFF94 SS1080P_0_SMMU_VCODEC_A_ESYNR1

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

SS1080P_0_SMMU_VCODEC_A_ESYNR1

Bits	Name	Description
31	DCD	(decode) Indicates configuration port error due to invalid/unrecognized address (e.g., a reserved register address) Includes decode errors within both the global address space and the individual context bank address space

SS1080P_0_SMMU_VCODEC_A_ESYNR1 (cont.)

Bits	Name	Description
30	AC	(access control) Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO field of the errant request
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request)
15:12	ALEN	ALEN[3:0] field of the errant request
11	RESERVED_2	
10	ABURST	ABURST[1:0] field of the errant request
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request
7	AINST	AINST field of the errant request
6	APROTNS	APROTNS field of the errant request
5	APRIV	APRIV field of the errant request
4	AINNERSHARED	AINNERSHARED field of the errant request
3	ASHARED	ASHARED field of the errant request
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

14.28.1.6 SMMU revision register

0x07AFFFF4 SS1080P_0_SMMU_VCODEC_A_REV

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the revision information for the SMMU core and wrapper.

SS1080P_0_SMMU_VCODEC_A_REV

Bits	Name	Description
31:12	RESERVED	
11:8	WRAPPER	Wrapper version
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

14.28.1.7 SMMU implementation parameter register

0x07AFFFF8 SS1080P_0_SMMU_VCODEC_A_IDR

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the parameter information for the SMMU core and wrapper

SS1080P_0_SMMU_VCODEC_A_IDR

Bits	Name	Description
31:24	NIRPT	NIRPT[7:0] Indicates number of context fault interrupt outputs (minus 1) supported by the System MMU Value can range from 0 - 255 (1 - 256 context fault interrupt outputs)
23:16	NCB	NCB[7:0] Indicates number of context banks (minus 1) supported by the System MMU Value can range from 0 - 254 (1 - 255 context banks)
15:12	TLBSIZE	TLBSIZE[3:0] Indicates log2(number of TLB entries) That is, number of TLB entries = 2 ** TLBSIZE
11	RESERVED	
10	HUM	Indicates whether or not TLB hit-under-miss behavior is supported
9	HTW	Indicates whether or not the System MMU supports hardware table walk If hardware table walk not supported (HTW=0), then software cannot set SMMU_CBn_ACTLR[TLBMCFG] to 0b10

SS1080P_0_SMMU_VCODEC_A_IDR (cont.)

Bits	Name	Description
8:0	NM2VCBMT	NM2VCBMT[8:0] Indicates number of M2VCBMT entries, with a maximum of 512 The bit width of the M2VCBMTIindex input (maximum value is 9) is equal to log base 2 of NM2VCBMT Allows for up to 7-bit MID field, plus NS-prot or other fields to select mapping [

0x07AFFFFC SS1080P_0_SMMU_VCODEC_A_RPU_ACR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Using the incoming HVMID, this register controls access to the global register space.

SS1080P_0_SMMU_VCODEC_A_RPU_ACR

Bits	Name	Description
31:0	RWE	Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the entire block of registers within the SMMU's 4KB global address space, including this register itself. A VMID identified by this register is also permitted global access to all context banks. In practice, this register designates the VMID(s) that can act as SROT.

14.28.2 SMMU Context Bank Registers

There are a configurable number (1 to 9) of context banks in the SMMU. Each context bank consists of a set of registers in a unique 4KB address space.

14.28.2.1 SMMU context bank control registers

0x07A00000+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_SCTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank System Control Register controls various architected SMMU features

SS1080P_0_SMMU_VCODEC_A_CBn_SCTLR

Bits	Name	Description
31:5	RESERVED_2	
4	BE	Governs the order byte order or "endianness" of the page table entries. When set to 0, page table entries are in little endian format, so that their least significant byte is in byte 0 of the 32 bit entry. When set to 1, page table entries are in big endian format, so that their most significant byte is in byte 0 of the 32 bit entry.
3	RESERVED_1	Reserved for HAF, Hardware access flag. This bit governs whether the access flag is managed by hardware or software. The SMMU supports software access flag management only, so this bit is read-only and internally driven to 0.
2	AFE	Access flag enable. When AFE = 0, the access flag field is not supported and the AP[0] page table entry field acts as a bit of the overall AP[2:0] field to determining access permissions. When AFE = 1, the AP[0] page table entry field becomes the access flag, and the reduced number of access permission combinations is specified by AP2:1], and SMMU hardware will signal an Access Flag fault if a request targets a page for which the access flag is 0.
1	TRE	TEX remap enable. This bit governs the mapping of the page table entry TEX[2:0],C,B and SH fields into an SMMU TLB entry, and thus the translation of the AMEMTYPE[2:0], ASHARED and AINNERSHARED bus attributes. When TRE = 0, the TLB value is determined directly from the page table entry fields.
0	M	MMU enable bit. When set to 1, this context bank is enabled for translating requests. When set to 0, accesses bypass the TLB, and there is no address translation, access permission checking or attribute mapping. Incoming master requests are passed through unchanged.

0x07A00004+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_ACTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank auxiliary control register controls various implementation specific features.

SS1080P_0_SMMU_VCODEC_A_CBn_ACTLR

Bits	Name	Description
31:19	RESERVED	
18	RESERVED_2	

SS1080P_0_SMMU_VCODEC_A_CBn_ACTLR (cont.)

Bits	Name	Description
17:16	V2PCFG	VA-to-PA configuration. Governs operation of VA-to-PA commands that miss in the TLB 0x0: terminate (Record TLB Miss context fault in SMMU_CBn_PAR) 0x1: software table update (Translate based on values in SMMU_CBn_TLBFLPTER and SMMU_CBn_TLBSLPTER) 0x2: hardware table walk (Translate based on value of PTE read from page table in memory) 0x3: reserved
15	TIPCF	Governs whether or not all subsequent requests using this context bank should be terminated if a prior context fault has occurred and has not yet been cleared from SMMU_CBn_FSR Accesses to other context banks proceed as normal 0x0: do not terminate (System MMU will attempt to process subsequent requests despite the presence of an existing context fault in SMMU_CBn_FSR. SMMU_CBn_FSR will be set if the subsequent access also encounters a context fault) 0x1: terminate (All subsequent accesses terminated by the System MMU as RAZ/WI, even if SMMU_CBn_ACTLR[TLBMCFG, CFCFG] configured for stall mode. SMMU_CBn_FSR set when access is terminated due to TIPCF = 1. Presence of SMMU_CBn_FSR when SMMU_CBn_ACTLR is 1 implies that the later exceptions must have been simply the forced terminations due to the prior context fault. Error optionally reported to the requesting master, according to the client port bus protocol, f SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus if SMMU_CBn_ACTLR is 1.)

SS1080P_0_SMMU_VCODEC_A_CBn_ACTLR (cont.)

Bits	Name	Description
14	CFCFG	(context fault configuration) Governs the behavior of all context faults except TLB miss TLB miss context faults are governed by SMMU_CBn_ACTLR[TLBMCFG] 0x0: terminate (Access terminates at the System MMU as RAZ/WI. Context fault exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x1: stall (Requesting master's access stalled while System MMU waits for managing processor to resolve context fault. Context fault exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode)

SS1080P_0_SMMU_VCODEC_A_CBn_ACTLR (cont.)

Bits	Name	Description
13:12	TLBMCFG	(TLB miss configuration) Governs the behavior of client accesses that miss in the TLB 0x0: pass-through (Access passed through to targeted slave without translation, attribute control, or access permission checking. Effectively, behavior is as if SMMU_CBn_SCTLR = 0 i.e., MMU disabled for this context bank. TLB miss not considered a context fault. TLB miss exception not recorded in SMMU_CBn_FSR. TLB miss exception not reported to requesting master. SMMU_contextFaultIrptReq interrupt output not asserted) 0x1: terminate (Access terminates at the System MMU as RAZ/WI,TLB miss exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x2: stall (Requesting master's access stalled while System MMU waits for managing processor to update TLB. TLB miss exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode) 0x3: HTW (Hardware table walk . Requesting master's access stalled while System MMU accesses page table. The is TLB updated and requesting master's access resumed after obtaining valid entry from page table. If translation fault, then access either terminates or stalls according to setting of SMMU_CBn_ACTLR)
11	DNLV2PA	(disable non-locking VA-to-PA allocation) Governs whether or not TLB misses due to non-locking VA-to-PA commands will allocate a new entry This field is ignored for locking VA-to-PA operations (SMMU_CBn_TLBLKCR[LKE] = 1)
10	DNA	(disable normal allocation) Governs whether or not TLB misses due to client port accesses will allocate a new entry
9:8	PRIVCFG	0x0: apriv (System MMU uses APRIV signal supplied by master as user/supervisor indicator 1 = supervisor) 0x1: reserved 0x2: User (System MMU ignores APRIV; treats all requests using this context bank as user) 0x3: Supervisor (System MMU ignores APRIV; treats all requests using this context bank as supervisor)

SS1080P_0_SMMU_VCODEC_A_CBn_ACTLR (cont.)

Bits	Name	Description
7:5	RESERVED_1	
4	RCNSH	(redirect cacheable-non-shareable) Governs whether or not cacheable accesses that are non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache, even though the locations are not being coherently shared with Scorpion-MP
3	RCISH	(redirect cacheable-inner-shareable) Governs whether or not cacheable accesses that are inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
2	RCOSH	(redirect cacheable-outer-shareable) Governs whether or not cacheable accesses that are outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
1	CFEIE	(context fault error interrupt enable) Governs whether or not client port request context faults are reported directly to the interrupt controller via the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus Interrupt output is asserted if SMMU_CBn_ACTLR[CFEIE] is 1 and any context fault bits are set in SMMU_CBn_FSR Such interrupts would generally be directed to the interrupt controller of whichever processor is currently managing this context bank of the System MMU Reset state : 0
0	CFERE	(context fault error report enable) Governs whether or not client port request context faults that are configured for terminate mode (or that are explicitly terminated after stall mode) are reported to the requesting master, according to the client port bus protocol All error types reported via AXI port will use decode error rather than slave error All context faults are recorded in SMMU_CBn_FSR, regardless of the value of this field.

0x07A00008+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_CONTEXTIDR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context ID register holds the ASID associated with this context bank

SS1080P_0_SMMU_VCODEC_A_CBn_CONTEXTIDR

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Specifies the 8 bit ASID value assigned to this context bank. The ASID can be included in the key comparison of TLB entries. .

0x07A00010+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_TTBR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR0 is used for low order virtual addresses, typically private pages for a given process.

SS1080P_0_SMMU_VCODEC_A_CBn_TTBR0

Bits	Name	Description
31:7	PA	BIts 31:7 of the physical address of the base of the page table. The actual LSB of the base address is bit 14-N, where N is set in register TTCR
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07A00014+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_TTBR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR1 is used for high order virtual addresses, typically global pages for a given VMID, or kernal mappings.

The context bank auxiliary control register controls various implementation specific features.

SS1080P_0_SMMU_VCODEC_A_CBn_TTBR1

Bits	Name	Description
31:14	PA	BIts 31:14 of the physical address of the base of the page table.
13:7	RESERVED_2	
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED_1	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07A00018+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_TTBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table control register, which specifies the size of the virtual address space that uses TTBR0.

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SS1080P_0_SMMU_VCODEC_A_CBn_TTBCR

Bits	Name	Description
31:6	RESERVED_2	
5	PD1	Page disable 1; if this bit is set, hardware table walks attempting to use TTBR1will result in a first level descriptor translation fault. If clear, TTBR1 contents are used.
4	PD0	Page disable 0; if this bit is set, hardware table walks attempting to use TTBR0 will result in a first level descriptor translation fault. If clear, TTBR0 contents are used.
3	RESERVED_1	
2:0	N	N[2:0] specifies the number of upper order virtual address bits which must be 0 in order for translations to use the table pointed to by TTBR0. If any of these bits are non-zero, TTBR1 is used for the lookup. If N is 0, only TTBR0 is used.

0x07A0001C+0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_PAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The physical address register captures the physical address value resulting from the execution of a VA-to-PA command

Field definitions vary according to whether or not there is a context fault associated with the requested translation

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SS1080P_0_SMMU_VCODEC_A_CBn_PAR

Bits	Name	Description
31:12	PAR_FAULT_INFO_312	
11	RESERVED_2	
10:9	PAR_FAULT_INFO_72	
8	RESERVED_1	
7:1	PAR_FAULT_INFO_71	Encoding varies according to value in FAULT field.

SS1080P_0_SMMU_VCODEC_A_CBn_PAR (cont.)

Bits	Name	Description
0	FAULT	(fault status) This field will be 1 when a context fault is associated with the requested translation, and 0, when there is no context fault associated with the requested translation.

0x07A00020+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_FSR, n=[0..1]

Type: Read/WriteClear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The Fault Status Register records status information for client accesses that encounter exceptions within the context bank, e.g. translation faults.This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data

This prevents inadvertent clearing of new faults when writing the register to clear an old fault

The presence of an asserted value on any bit in this register (except the SS bit) is what prompts the assertion (when enabled by SMMU_CBn_ACTLR[CFEIE]) of the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus

Therefore, these bits must be cleared by the interrupt handler

This is contrasted with the fields in the SMMU_CBn_FSYNRn registers, which are merely the "syndrome" of the fault indicated by SMMU_CBn_FSR

SS1080P_0_SMMU_VCODEC_A_CBn_FSR

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"

SS1080P_0_SMMU_VCODEC_A_CBn_FSR (cont.)

Bits	Name	Description
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07A00024+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_FSRRESTORE, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Allows SW to force a value into the SMMU_CBn_FSR register.

SS1080P_0_SMMU_VCODEC_A_CBn_FSRRESTORE

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode

SS1080P_0_SMMU_VCODEC_A_CBn_FSRRESTORE (cont.)

Bits	Name	Description
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07A00028+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_FAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The Fault Address Register records the virtual address of client accesses that encounter exceptions within the context bank, e.g. translation faults. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

SS1080P_0_SMMU_VCODEC_A_CBn_FAR

Bits	Name	Description
31:0	VA	VA[31:0] of errant client access

0x07A0002C+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_FSYNR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

NOTE omission of VMID field from this register, as VMID can only be made visible to SROT, and not to general OS software that manages the context bank registers

SS1080P_0_SMMU_VCODEC_A_CBn_FSYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] (ATID field of errant request)
23:16	RESERVED	
15:13	ABID	ABID[2:0] (ABID field of errant request)
12:8	APID	APID[4:0] (APID field of errant request)
7:0	AMID	AMID[7:0] (AMID field of errant request)

0x07A00030+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_FSYNR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

SS1080P_0_SMMU_VCODEC_A_CBn_FSYNR1

Bits	Name	Description
31:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO (AOOO field of the errant request)
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request
15:12	ALEN	ALEN[3:0]field of the errant request
11	RESERVED_2	
10	ABURST	field of the errant request
9	RESERVED_1	
8	AWRITE	field of the errant request
7	AINST	field of the errant request
6	APROTNS	field of the errant request
5	APRIV	field of the errant request
4	AINNERSHARED	(AINNERSHARED field of the errant request)

SS1080P_0_SMMU_VCODEC_A_CBn_FSYNR1 (cont.)

Bits	Name	Description
3	ASHARED	(ASHARED field of the errant request)
2:0	AMEMTYPE	AMEMTYPE[2:0] (AMEMTYPE field of the errant request)

0x07A00034+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_PRRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs memory type and shareability attributes of requests that are both MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1)

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) and/or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, memory type encoding is as follows:

0b00 = strongly-ordered

0b01 = device

0b10 = normal

0b11 = reserved

SS1080P_0_SMMU_VCODEC_A_CBn_PRRR

Bits	Name	Description
31	NOS7	not-outer-shareable class 7
30	NOS6	not-outer-shareable class 6
29	NOS5	not-outer-shareable class 5
28	NOS4	not-outer-shareable class 4
27	NOS3	not-outer-shareable class 3
26	NOS2	not-outer-shareable class 2
25	NOS1	not-outer-shareable class 1
24	NOS0	not-outer-shareable class 0

SS1080P_0_SMMU_VCODEC_A_CBn_PRRR (cont.)

Bits	Name	Description
23:20	RESERVED	
19	SHNMSH1	(shareable attribute for normal memory accesses with SH=1) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1
18	SHNMSH0	(shareable attribute for normal memory accesses with SH=0) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0
17	SHDSH1	SHDSH1 (shareable attribute for device accesses with SH=1) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1 [
16	SHDSH0	SHDSH0 (shareable attribute for device accesses with SH=0) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0 [
15:14	MTC7	MTC7[1:0] (memory type class 0)
13:12	MTC6	MTC6[1:0] (memory type class 0)
11:10	MTC5	MTC5[1:0] (memory type class 0)
9:8	MTC4	MTC4[1:0] (memory type class 0)
7:6	MTC3	MTC3[1:0] (memory type class 0)
5:4	MTC2	MTC2[1:0] (memory type class 0)
3:2	MTC1	MTC1[1:0] (memory type class 0)
1:0	MTC0	MTC0[1:0] (memory type class 0)

0x07A00038+0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_NMRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs the cache policy of MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1) requests for which the memory type is mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0) or the memory type is mapped to a type other than normal memory (SMMU_CBn_PRRR[MTCn] != 0b10)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, inner-cache and outer-cache policy encodings are as follows:

0b00 = non-cacheable

0b01 = cacheable, copy-back, write-allocate

0b10 = cacheable, write-through, write-no-allocate

0b11 = cacheable, copy-back, write-no-allocate

SS1080P_0_SMMU_VCODEC_A_CBn_NMRR

Bits	Name	Description
31:30	OCPC7	OCPC7[1:0] (inner-cache policy class 7)
29:28	OCPC6	OCPC6[1:0] (inner-cache policy class 6)
27:26	OCPC5	OCPC5[1:0] (inner-cache policy class 5)
25:24	OCPC4	OCPC4[1:0] (inner-cache policy class 4)
23:22	OCPC3	OCPC3[1:0] (inner-cache policy class 3)
21:20	OCPC2	OCPC2[1:0] (inner-cache policy class 2)
19:18	OCPC1	OCPC1[1:0] (inner-cache policy class 1)
17:16	OCPC0	OCPC0[1:0] (inner-cache policy class 0)
15:14	ICPC7	ICPC7[1:0] (inner-cache policy class 7)
13:12	ICPC6	ICPC6[1:0] (inner-cache policy class 6)
11:10	ICPC5	ICPC5[1:0] (inner-cache policy class 5)
9:8	ICPC4	ICPC4[1:0] (inner-cache policy class 4)
7:6	ICPC3	ICPC3[1:0] (inner-cache policy class 3)
5:4	ICPC2	ICPC2[1:0] (inner-cache policy class 2)
3:2	ICPC1	ICPC1[1:0] (inner-cache policy class 1)
1:0	ICPC0	ICPC0[1:0] (inner-cache policy class 0)

0x07A0003C+0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_TLBLKCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB lock control register governs the TLB locking mechanism and TLB invalidate operations.Write access to this register is governed by SMMU_CR[TLBLKCRWE]

When SMMU_CR[TLBLKCRWE] is 0, writes to SMMU_CBn_TLBLKCR are ignored

Read access is still permitted

SROT can set SMMU_CR[TLBLKCRWE] to 1 to allow operating environment(s) to manage the TLB locking mechanism

Management amongst multiple operating environments must be coordinated via semaphore

SS1080P_0_SMMU_VCODEC_A_CBn_TLBLKCR

Bits	Name	Description
31:24	RESERVED_2	
23:16	VICTIM	VICTIM[7:0] Indicates the TLB index at which the next normal (non-locking) allocation will occur Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context
15:8	FLOOR	FLOOR[7:0] Indicates the TLB index from which round-robin replacement on normal (non-locking) allocations occurs TLB entries at indices below this value are locked Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context banks
7:4	RESERVED_1	

SS1080P_0_SMMU_VCODEC_A_CBn_TLBLKCR (cont.)

Bits	Name	Description
3	TLBIVAACFG	(TLBIVAA configuration) TLBIVAACFG = 0 - flash-invalidate SMMU_CBn_TLBIVAA commands flash-invalidate the entire TLB, without regard to locking, security, address, and/or VMID value TLBIVAACFG = 1 - selective SMMU_CBn_TLBIVAA commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank VA field of TLB entry matches VA designated by SMMU_CBn_TLBIVAA command NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked
2	TLBIASIDCFG	(TLBIASID configuration) TLBIASIDCFG = 0 - flash-invalidate SMMU_CBn_TLBIASID commands flash-invalidate the entire TLB, without regard to locking, security, VMID, and/or ASID values TLBIASIDCFG = 1 - selective SMMU_CBn_TLBIASID commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command TLB entry is not global (NG field is 1) NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
1	TLBIALLCFG	(TLBIALL configuration) TLBIALLCFG = 0 - flash-invalidate SMMU_CBn_TLBIALL commands flash-invalidate the entire TLB, without regard to locking, security, and/or VMID value TLBIALLCFG = 1 - selective SMMU_CBn_TLBIALL commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked

SS1080P_0_SMMU_VCODEC_A_CBn_TLBLKCR (cont.)

Bits	Name	Description
0	LKE	(lock enable) Governs whether or not TLB entries established by VA-to-PA commands upon TLB misses are locked LKE = 0 (normal, non-locking) Allocate VA-to-PA TLB entry (if TLB miss) at the index specified by SMMU_CBn_TLBLKCR[VICTIM] Allocation is disabled if SMMU_CBn_ACTLR[DNLV2PA] is 1 Increment SMMU_CBn_TLBLKCR[VICTIM] by 1 (only if new entry allocated) Wrap back to the value of SMMU_CBn_TLBLKCR[FLOOR] when the last entry is written LKE = 1 (locking) Search TLB for specified VA and invalidate if found Provides atomicity between the invalidate and the new allocation within the locked region Allocate VA-to-PA TLB entry at the index specified by data operand bits 7:0 of the VA-to-PA command This value must be less than SMMU_CBn_TLBLKCR[FLOOR] in order for it to remain locked Allocation occurs even if non-locking allocation is disabled due to SMMU_CBn_ACTLR[DNLV2PA] = 1

0x07A00040+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_V2PSR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The VA-to-PA status register records the hit/miss status and TLB index or V2Pxx and TLB invalidate commands.

SS1080P_0_SMMU_VCODEC_A_CBn_V2PSR

Bits	Name	Description
31:16	RESERVED_2	
15:8	INDEX	INDEX[7:0] Indicates the index of the TLB entry associated with the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command If SMMU_CBn_V2PSR[HIT] is 0, then SMMU_CBn_V2PSR[INDEX] is the index to which the entry was allocated (if allocated at all) If SMMU_CBn_V2PSR[HIT] is 1, then SMMU_CBn_V2PSR[INDEX] is the index of the entry which hit
7:1	RESERVED_1	

SS1080P_0_SMMU_VCODEC_A_CBn_V2PSR (cont.)

Bits	Name	Description
0	HIT	Indicates whether or not there was a TLB hit (prior to allocation, if any) on the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command

0x07A00044+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_TLBFLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB first level PTE register holds the first level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

This register (together with SMMU_CBn_TLBSLPTER) is used as the source of the translation information for VA-to-PA operations when the MMU is enabled (SMMU_CBn_SCTLR[M] = 1) and the operations are configured for software table update (SMMU_CBn_ACTLR[V2PCFG] = 0b01)

Field definitions vary according to the type of PTE (fault, page, section, or supersection), and come directly from the ARMv7 architecture's PTE formats

SS1080P_0_SMMU_VCODEC_A_CBn_TLBFLPTER

Bits	Name	Description
31:10	FL_PTE_HI	
9:5	RESERVED	
4:2	FL_PTE_LO	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	This field should be set to 0b00 or 0b11 to indicate that the translation should result in a context fault, and the rest of the fields are defined as indicated in this section If this field is not 0b00 or 0b11, then the PTE is of some other type (see other sections for the field definitions for those types)

0x07A00048+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_TLBSLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB second level PTE register holds the second level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

Field definitions vary according to the type of PTE (fault, 64KB or 4KB), and come directly from the ARMv7 architecture's PTE format

SS1080P_0_SMMU_VCODEC_A_CBn_TLBSLPTER

Bits	Name	Description
31:2	SL_PTE	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	0x0: fault

0x07A0004C+0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_BFBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The burst fetch buffer configuration register governs the operation of the "burst fill" feature of the SMMU.

SS1080P_0_SMMU_VCODEC_A_CBn_BFBCR

Bits	Name	Description
31:12	STRIDE	(stride amount) 4KB-aligned value to be added to virtual address on demand TLB miss for filling subsequent BFB Stride of minimum 4KB alignment useful for preventing stride burst fetch until final PTE of the demand BFB entry is used
11:8	SLVIC	(second-level victim) Indicates the SLBFB index at which the next round-robin allocation will occur
7:4	FLVIC	(first-level victim) Indicates the FLBFB index at which the next round-robin allocation will occur
3	RESERVED	
2	SFVS	(stride-fetch victim selection) SFVS. = 0 (replace normal round-robin victim-selected entry) Useful when stride is larger than the VA space represented by the four PTEs in the demand BFB entry, but the client access pattern is for more than just the initial PTE in that demand BFB entry SFVS. = 1 (replace same BFB used by demand VA for which the stride burst is being performed) Useful when stride is the same as the VA space represented by an individual PTE in the demand BFB entry (such that the stride won't miss against the BFB until the last PTE of the demand BFB entry is accessed), and/or when the client access pattern only uses the initial PTE in the demand BFB entry

SS1080P_0_SMMU_VCODEC_A_CBn_BFBCR (cont.)

Bits	Name	Description
1	BFBSFE	(burst fetch buffer stride fetch enable) Enables stride burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Stride burst fetch is for the block of four PTEs associated with VA+stride VA is the "demanded" VA from the client (or VA-to-PA command) Stride value is specified by SMMU_CBn_BFBCR[STRIDE] Stride burst fetch only occurs if demand access for VA misses in TLB (could hit in BFB) and address VA+stride misses in both TLB and BFB
0	BFBDFE	(burst fetch buffer demand fetch enable) Enables demand burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Demand burst fetch is for the block of four PTEs associated with the "demanded" VA from the client (or VA-to-PA command) Demand burst fetch only occurs if demand access misses in both TLB and BFB

0x07A00800+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_TLBIALL, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate all command register invalidates all TLB entries matching the VMID associated with this context bank. Data operand is ignored.

SS1080P_0_SMMU_VCODEC_A_CBn_TLBIALL

Bits	Name	Description
31:0	RESERVED	

0x07A00804+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_TLBIASID, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by ASID command register invalidates TLB entries matching the specified ASID and matching the VMID associated with this context bank.Invalidates TLB entries which are associated with the designated ASID and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIASIDCFG] governs whether command flash-invalidates entire TLB array or just the entries matching the VMID, ASID, and security state

TLBIASIDCFG = 0 - flash-invalidate

SMMU_CBn_TLBIASID command flash-invalidates the entire TLB, without regard to locking, security, VMID, and/or ASID values

TLBIASIDCFG = 1 - selective

SMMU_CBn_TLBIASID command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command data operand

TLB entry is not global (NG field is 1)

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command

Locking is not considered (matching entries are invalidated even if locked)

ASID field of command specifies the ASID value of the TLB entries to be invalidated

SS1080P_0_SMMU_VCODEC_A_CBn_TLBIASID

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Actual ASID value

0x07A00808+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_TLBIVA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA command invalidates TLB entries matching the designated VA, ASID and the VMID associated with this context bank.

Matching entry determined as follows:

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIVA command data operand (or TLB entry is global - NG field is 0)

VA field of TLB entry matches VA value designated by the SMMU_CBn_TLBIVA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIVA command

Locking is not considered (matching entry is invalidated even if locked)

Data operand specifies the VA and ASID value of the TLB entry to be invalidated

SS1080P_0_SMMU_VCODEC_A_CBn_TLBIVA

Bits	Name	Description
31:12	VA	VA[31:12]
11:8	RESERVED	
7:0	ASID	ASID[7:0] value

0x07A0080C+0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_TLBIVAA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA all ASIDS command invalidates TLB entries matching the designated VA and the VMID associated with this context bank, regardless of ASID.Invalidates TLB entries which are associated with the designated VA, regardless of ASID, and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIVAACFG] governs whether command flash-invalidates entire TLB array or just the non-locked entries matching the VMID, ASID, and security state

TLBIVAACFG = 0 - flash-invalidate

SMMU_CBn_TLBIVAA command flash-invalidates the entire TLB, without regard to locking, security, address, and/or VMID value

TLBIVAACFG = 1 - selective

SMMU_CBn_TLBIVAA command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

VA field of TLB entry matches VA designated by the SMMU_CBn_TLBIVAA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command

Entry is unlocked

SS1080P_0_SMMU_VCODEC_A_CBn_TLBIVAA

Bits	Name	Description
31:12	VA	VA[31:12]
11:0	RESERVED	

0x07A00810+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_V2PRR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

SS1080P_0_SMMU_VCODEC_A_CBn_V2PRR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07A00814+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_V2PPW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

SS1080P_0_SMMU_VCODEC_A_CBn_V2PPW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07A00818+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_V2PUR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

SS1080P_0_SMMU_VCODEC_A_CBn_V2PUR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07A0081C+0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_V2PUW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

.Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

SS1080P_0_SMMU_VCODEC_A_CBn_V2PUW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07A00820+ 0x1000*n SS1080P_0_SMMU_VCODEC_A_CBn_RESUME, n=[0..1]

Type: Write/command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB resume command causes the SMMU to resume operation after a stalled access..

SS1080P_0_SMMU_VCODEC_A_CBn_RESUME

Bits	Name	Description
31:1	RESERVED	

SS1080P_0_SMMU_VCODEC_A_CBn_RESUME (cont.)

Bits	Name	Description
0	TNR	Terminate/not retry When TNR is written as 0, indicates that the stalled access should be retried by the system MMU. When written as 1, indicates that this stalled transaction is terminated by the system MMU. The error is optionally reported to the requesting master, using the client port bus protocol, if SMMU_CNn_ACTLR[CFERE] == 1. Interrupt optionally remains asserted via SMMU_M2VCBRn[IRPTINDX] selected SMMU_contextFaultIrptReq bit, only if SMMU_CBn_ACTLR[CFEIE] is 1, and only if SMMU_CBn_FSR has not been cleared by software priori to issuing this command..

14.29 VCODEC B SS1080P 1 SMMU Registers (0x07B00000 SMMU_SS1080P_1_BASE)

This section contains VCODEC B SS1080P 1 SMMU registers.

14.29.1 SMMU Global Registers

14.29.1.1 SMMU VMID/CBNDX mapping registers

0x07BFF000+0x4*n SS1080P_1_SMMU_VCODEC_B_M2VCBRn, n=[0..15]

Type: Read/Write
Clock: AXI_CLK
Reset State: Undefined

SMMU_M2VCBRm registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

SS1080P_1_SMMU_VCODEC_B_M2VCBRn

Bits	Name	Description
31:28	RESERVED_2	
27:25	BPMEMTYPE	(bypass memory type) Supplies the AMEMTYPE attributes for client requests which bypass the System MMU when SMMU_M2VCBRn[BPMTCFG] = 1 See reference section for AMEMTYPE encoding definitions
24	BPMTCFG	(bypass memory type configuration) Governs the memory type (AMEMTYPE) attributes of client requests which bypass the System MMU BPMTCFG = 0 - use AMEMTYPE Bypass requests use AMEMTYPE signal supplied by client master BPMTCFG = 1 - use SMMU_M2VCBRn[BPMEMTYPE] Bypass requests use SMMU_M2VCBRn[BPMEMTYPE] Reset state : 0
23:22	NSCFG	(non-secure configuration) Governs the incoming security designation of client requests NSCFG = 0b00 - use APROTNS Use APROTNS signal supplied by client master NSCFG = 0b01 - reserved NSCFG = 0b10 - secure System MMU ignores APROTNS; treats all requests as secure NSCFG = 0b11 - non-secure System MMU ignores APROTNS; treats all requests as non-secure Reset state : 0

SS1080P_1_SMMU_VCODEC_B_M2VCBRn (cont.)

Bits	Name	Description
21:20	BPSHCFG	(bypass shareability configuration) Governs the shareability realm (ASHARED and AINNERSHARED) attributes of client requests which bypass the System MMU BPSHCFG = 0b00 - use ASHARED and AINNERSHARED Bypass requests use ASHARED and AINNERSHARED signals supplied by client master BPSHCFG = 0b01 - outer-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 0 BPSHCFG = 0b10 - inner-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 1 BPSHCFG = 0b11 - non-shareable Bypass requests set ASHARED = 0, AINNERSHARED = 0 Reset state : 0
19	BPRCNSH	(bypass redirect cacheable-non-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache Reset state : 0
18	BPRCISH	(bypass redirect cacheable-inner-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0
17	BPRCOSH	(bypass redirect cacheable-outer-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0

SS1080P_1_SMMU_VCODEC_B_M2VCBRn (cont.)

Bits	Name	Description
16	BYPASSD	Bypass disable for this index Governs whether or not client port accesses using this mapping table entry are actually permitted to "bypass" the System MMU when such bypass is indicated (either due to CBNDX = 255 or due to the master asserting the "SMMU bypass" input) This field is ignored (and operates as if it were 0) if SMMU_CR[CLIENTPD] is 1 BYPASSD = 0 - bypass enabled Bypass requests truly bypass the System MMU and "pass-through" to the fabric (no translation, access control, or attribute generation) No cycle of latency for System MMU context bank access Bypass request not considered an error Bypass request error not recorded in SMMU_ESR[BYPASS] Bypass error not reported to requesting master SMMU_rpuErrIrptReq interrupt output not asserted Client accesses still reference M2VCBMT to get VMID value for presentation to fabric BYPASSD = 1 - bypass disabled System MMU terminates the access as RAZ/WI Bypass request is considered an error Bypass request error is recorded in SMMU_ESR[BYPASS] If SMMU_CR[RPUERE] is 1, then bypass error reported to requesting master according to the client port bus protocol If SMMU_CR[RPUEIE] is 1, then SMMU_rpuErrIrptReq interrupt output asserted
15:8	CBNDX	Context bank index Context bank index associated with the M2VCBMT index CBNDX = 255 indicates no context bank assigned ("bypass")
7:5	RESERVED_1	
4:0	VMID	Virtual machine ID VMID value associated with the M2VCBMT index Must be programmed consistently with the SMMU_CBACRn[CBVMID] field for the context bank designated by SMMU_M2VCBRm[CBNDX]

14.29.1.2 SMMU context bank access control registers

0x07BFF800+0x4*n SS1080P_1_SMMU_VCODEC_B_CBACRn, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs configuration port access to the associated context bank registers.

SS1080P_1_SMMU_VCODEC_B_CBACRn

Bits	Name	Description
31:24	IRPTNDX	(interrupt index) Interrupt output number used for context faults associated with this context bank (use SMMU_contextFaultIrptReq[IRPTNDX])
23:21	RESERVED	
20:16	CBVMID	(context bank VMID) Specifies the VMID with which the client masters using the context bank are associated Must be programmed consistently with the M2VCBMT entries that are configured to use the associated context bank This field is used by configuration port commands that need the context bank's VMID value in order to access the TLB (e.g., SMMU_CBn_TLBIVMID, SMMU_CBn_V2Pxx)
15:10	RESERVED_2	
9	RWGE	Read/write global enable. Setting this bit allows access to the context bank registers from any VMID
8	RWE	Read/write enable. Indicates that the RWVMID field is valid.
7:5	RESERVED_1	
4:0	RWVMID	Specifies owner VMID with full read/write access to the registers in the associated context bank "n".

14.29.1.3 SMMU TLB software access registers

0x07BFFE00 SS1080P_1_SMMU_VCODEC_B_TLBRSW

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Writing to this address requests that the TLB entry at INDEX be read into the SMMU_TLBTRn registers

SS1080P_1_SMMU_VCODEC_B_TLBRSW

Bits	Name	Description
31:10	RESERVED	

SS1080P_1_SMMU_VCODEC_B_TLBRSW (cont.)

Bits	Name	Description
9:8	TLBBFBS	This field selects the TLB, TFBFB, SLBFB 0x0: Selecting TLB 0x1: Not defined 0x2: Selecting FL BFB 0x3: Selecting SL BFB
7:0	INDEX	TLB index to be read.

0x07BFFE80 SS1080P_1_SMMU_VCODEC_B_TLBTR0

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

This register holds part of TLB entry read by the last TLBRSW command.

SS1080P_1_SMMU_VCODEC_B_TLBTR0

Bits	Name	Description
31:23	RESERVED_4	
22:20	DPSIZC	3 bit decode page size field from CAM-side of TLB CAM-RAM) Same determination and encoding as for DPSIZR The CAM-side copy of this field is used for hit/miss determination in the TLB CAM array
19	RESERVED_3	
18:16	DPSIZR	(3 bit decode page size field from RAM-side of TLB CAM-RAM) Determined from the size fields of the page table entry Encodes the page size as follows: all other values reserved/unused The RAM-side copy of this field is used for virtual ’ physical address formation 0x0: 4KB page 0x1: 64KB page 0x3: 1MB page 0x7: 16MB page
15:12	RESERVED_2	
11	MT2	(memory type bit 2) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[2] attribute bus on the request output of the System MMU

SS1080P_1_SMMU_VCODEC_B_TLBTR0 (cont.)

Bits	Name	Description
10	MT1	(memory type bit 1) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[1] attribute bus on the request output of the System MMU
9	MT0	(memory type bit 0) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[0] attribute bus on the request output of the System MMU
8	SH	(shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's outer-shareable realm This field becomes the ASHARED attribute on the request output of the System MMU
7	ISH	(inner-shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's inner-shareable realm This field becomes the AINNERSHARED attribute on the request output of the System MMU
6	NSDESC	(non-secure descriptor) This TLB entry field is a modified version of the corresponding bit of the page table entry Qualified by the NS-prot attribute of the incoming request which prompted the allocation of the TLB entry, such that if the incoming NS-prot attribute was 1 (non-secure), then the NS-desc field of the page table entry was ignored, and the NS-desc field of the TLB entry was forced to 1 Indicates whether the associated memory page contains secure (NS-desc=0) or non-secure (NS-desc=1) information This field becomes the NS-prot attribute on the request output of the System MMU
5	RESERVED_1	

SS1080P_1_SMMU_VCODEC_B_TLBTR0 (cont.)

Bits	Name	Description
4	XN	(execute never permission) This TLB entry field comes directly from the corresponding bit of the page table entry
3	UW	(user write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
2	UR	(user read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
1	PW	(privileged write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
0	PR	(privileged read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]

0x07BFFE84 SS1080P_1_SMMU_VCODEC_B_TLBTR1

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

SS1080P_1_SMMU_VCODEC_B_TLBTR1

Bits	Name	Description
31:12	PA	Physical address [31:12] field of the TLB entry
11:5	RESERVED	
4:0	VMID	VMID [4:0]field of the TLB entry)

0x07BFFE88 SS1080P_1_SMMU_VCODEC_B_TLBTR2

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

SS1080P_1_SMMU_VCODEC_B_TLBTR2

Bits	Name	Description
31:12	VA	virtual address field [31:12] of the TLB entry
11	RESERVED	
10	NG	(not global field from page table entry) Indicates whether the page is private to the specified ASID (NG=1) or global to all ASIDs within the VMID using this context bank (NG=0)
9	NSTID	(non-secure tag ID field of the TLB entry) Indicates whether the TLB entry belongs to the secure world (NSTID=0) or the non-secure world (NSTID=1) This field is comned against the incoming NS-prot attribute of the master request as part of TLB hit/miss determination
8	V	valid field of the TLB entry
7:0	ASID	ASID[7:0] field of the TLB entry

0x07BFFE8C SS1080P_1_SMMU_VCODEC_B_TESTBUSCR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

Governs which signals (if any) from the system SMMU core or wrapper design hierarchy are sent out to the system via a testbus for diagnostic, and also to the system profiling and diagnostic monitor(SPDM).

SS1080P_1_SMMU_VCODEC_B_TESTBUSCR

Bits	Name	Description
31:28	SPDM3SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[3]
27:24	SPDM2SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[2]
23:20	SPDM1SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[1]
19:16	SPDM0SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[0]
15:14	TBHSEL	Testbus highselect It governs which set of signals are to testbus[31:16] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL

SS1080P_1_SMMU_VCODEC_B_TESTBUSCR (cont.)

Bits	Name	Description
13:12	TBSLSEL	Testbus low select It governs which set of signals are to testbus[15:0] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL
11:10	RESERVED_2	
9:8	WGSEL	Wrapper group select It selects a particular group of signals from the SMMU wrapper hierarchy WGSEL = 0b00 - wrapper signal group 0 WGSEL = 0b01 - wrapper signal group 1 WGSEL = 0b10 - wrapper signal group 2 WGSEL = 0b11 - reserved
7:2	RESERVED_1	
1	SPDMBE	SPDM test enable Reset state : 0
0	TBE	Testbus enable, which governs whether the testbus is driven with all 0s or with the configured signals Reset state : 0

0x07BFFEFC SS1080P_1_SMMU_VCODEC_B_VR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: 32'h0000_0000

Note that the DCPBP/DCPPP bits prevent the pipelining of the next transaction when the current transaction is a bypass/pass-through transaction. That is, they add one more cycle of delay between the current and next transactions.

Also note that when we are in global bypass (SMMU_CR[CLIENTPD]=1), these bits should have NO effect, or at least no effect between client transactions, they can have an effect between config and client transactions is appropriate. We must be able to continue to perform fully pipelined transactions when the client port is disabled altogether.

SS1080P_1_SMMU_VCODEC_B_VR0

Bits	Name	Description
31:3	RESERVED	

SS1080P_1_SMMU_VCODEC_B_VR0 (cont.)

Bits	Name	Description
2	DCPPT	Disable client pipelining for client operations in pass-through mode Reset state : 0
1	DCPBP	Disable client pipelining for client operations in bypass mode Reset state : 0
0	DCP	Disable client pipelining Reset state : 0

0x07BFFF00 SS1080P_1_SMMU_VCODEC_B_TLBIALL

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries.

SS1080P_1_SMMU_VCODEC_B_TLBIALL

Bits	Name	Description
31:0	EXEC	Writing any value to this register invalidates all TLB entries, as specified by the contents of SMMU_CR[TLBIALLCFG]

0x07BFFF04 SS1080P_1_SMMU_VCODEC_B_TLBIVMID

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries matching the IVMID value. Precise function is governed by SMMU_CR[TLBIALLCFG].

SS1080P_1_SMMU_VCODEC_B_TLBIVMID

Bits	Name	Description
31:5	RESERVED	
4:0	IVMID	Designates VMID[4:0] value of entries to be invalidated.

14.29.1.4 SMMU configuration registers

0x07BFFF80 SS1080P_1_SMMU_VCODEC_B_CR

Type: Read/Write
Clock: AXI_BUS_CLOCK

Global configuration register.

SS1080P_1_SMMU_VCODEC_B_CR

Bits	Name	Description
31:10	RESERVED_2	
9	RESERVED_1	Reset state : 0
8	TLBIVMIDCFG	TLBIVMID configuration control. When set to 0,flash-invalidate, SMMU_TLBIVMID commands flash-invalidate the entire TLB, without regard to locking ,security and VMID value. When set to 1, selective, SMMU_TLBIVMID invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and VMID field matching the VMID specified by SMMU_TLBIVMID command. Reset state : X
7	TLBIALLCFG	TLBIALL configuration control. When set to 0, flash-invalidate, SMMU_TLBIALL commands flash-invalidate the entire TLB, without regard to locking and/or security. When set to 1, selective, SMMU_TLBIALL invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and are unlocked. Reset state : X
6	TLBLKCRWE	TLBLKCR write enable. When set to 0, writes to SMMU_CBn_TLBLKCR are ignored. When set to 1, allows operating environments to manage the TLB locking mechanism directly. Management amounst multiple operating environments must be coordinated externally between themselves. Reset state : X
5	STALLD	Global disable for stall mode. When set to 1, context bank stall modes are ignored and operate as terminate mode. Reset state : X

SS1080P_1_SMMU_VCODEC_B_CR (cont.)

Bits	Name	Description
4	CLIENTPD	Client port disable. When set, all client accesses are forced to bypass the system MMU. There is no translation. access control, or attribute generation. This bit overrides individual SMMU_M2VCBRn[BYPASSD] settings; client requests are bypassed, even if SMMU_M2VCBRn[BYPASSD] is set to 1. Bypass request errors are not recorded in SMMU_ESR, nor reported to requesting masters. The SMMU_rpuErrIrptReq interrupt output signal is not asserted. Reset state : 1
3	DCDEE	When set to 0, configuration port decode errors do not set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn are not updated. When set to 1, configuration port decode errors set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn updated with address and syndrome of error. Reset state : X
2	RPUEIE	When set, configuration port errors and client port bypass errors are reported directly to the interrupt controller via the SMMU_rputErrIrptReq interrupt output signal. Interrupt output is asserted if SMMU_CR[RPUIE_EN] is 1 and ANY bit is set in SMMU_ESR register. Reset state : 0
1	RPUERE	When set, SMMU reports configuration port errors and client port bypass errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via AXI port will use decode error, rather than slave error. Regardless of the value of this field both configuration port errors and client port bypass request errors are terminated by the SMMU as RAZ/WI, and are recorded in SMMU_ESR register. Reset state : X
0	RPUE	When set, all configuration port accesses are checked against SMMUX_RPU_ACR and/or the SMMUX_CBACRn registers for access permissions. Reset state : 0

14.29.1.5 SMMU error report registers

0x07BFFF84 SS1080P_1_SMMU_VCODEC_B_EAR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: unknown

When there is an error, holds the physical address of the errant transaction.

SS1080P_1_SMMU_VCODEC_B_EAR

Bits	Name	Description
31:0	PA	Physical address[31:0]

0x07BFFF88 SS1080P_1_SMMU_VCODEC_B_ESR

Type: Read/Write to clear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This register has read/write clear access. Reads return the value in the register, a write with a 1 set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

SS1080P_1_SMMU_VCODEC_B_ESR

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x07BFFF8C SS1080P_1_SMMU_VCODEC_B_ESRRESTORE

Type: Write
Clock: RPM_BUS_CLK
Reset State: Undefined

This register is an aliased address for SMMU_ESR, but it allows direct write access. In this way, diagnostic software can cause an error to be generated and reported.

SS1080P_1_SMMU_VCODEC_B_ESRRESTORE

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x07BFFF90 SS1080P_1_SMMU_VCODEC_B_ESYNR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

SS1080P_1_SMMU_VCODEC_B_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request
15:0	AMID	AMID[15:0] field of errant request

0x07BFFF94 SS1080P_1_SMMU_VCODEC_B_ESYNR1

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

SS1080P_1_SMMU_VCODEC_B_ESYNR1

Bits	Name	Description
31	DCD	(decode) Indicates configuration port error due to invalid/unrecognized address (e.g., a reserved register address) Includes decode errors within both the global address space and the individual context bank address space
30	AC	(access control) Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO field of the errant request
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request)
15:12	ALEN	ALEN[3:0] field of the errant request
11	RESERVED_2	
10	ABURST	ABURST[1:0] field of the errant request
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request
7	AINST	AINST field of the errant request
6	APROTNS	APROTNS field of the errant request
5	APRIV	APRIV field of the errant request
4	AINNERSHARED	AINNERSHARED field of the errant request
3	ASHARED	ASHARED field of the errant request
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

14.29.1.6 SMMU revision register

0x07BFFFF4 SS1080P_1_SMMU_VCODEC_B_REV

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the revision information for the SMMU core and wrapper.

SS1080P_1_SMMU_VCODEC_B_REV

Bits	Name	Description
31:12	RESERVED	
11:8	WRAPPER	Wrapper version
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

14.29.1.7 SMMU implementation parameter register

0x07BFFFF8 SS1080P_1_SMMU_VCODEC_B_IDR

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the parameter information for the SMMU core and wrapper.

SS1080P_1_SMMU_VCODEC_B_IDR

Bits	Name	Description
31:24	NIRPT	NIRPT[7:0] Indicates number of context fault interrupt outputs (minus 1) supported by the System MMU Value can range from 0 - 255 (1 - 256 context fault interrupt outputs)
23:16	NCB	NCB[7:0] Indicates number of context banks (minus 1) supported by the System MMU Value can range from 0 - 254 (1 - 255 context banks)
15:12	TLBSIZE	TLBSIZE[3:0] Indicates log2(number of TLB entries) That is, number of TLB entries = 2 ** TLBSIZE
11	RESERVED	
10	HUM	Indicates whether or not TLB hit-under-miss behavior is supported

SS1080P_1_SMMU_VCODEC_B_IDR (cont.)

Bits	Name	Description
9	HTW	Indicates whether or not the System MMU supports hardware table walk If hardware table walk not supported (HTW=0), then software cannot set SMMU_CBn_ACTLR[TLBMCFG] to 0b10
8:0	NM2VCBMT	NM2VCBMT[8:0] Indicates number of M2VCBMT entries, with a maximum of 512 The bit width of the M2VCBMTIindex input (maximum value is 9) is equal to log base 2 of NM2VCBMT Allows for up to 7-bit MID field, plus NS-prot or other fields to select mapping [

0x07BFFFFC SS1080P_1_SMMU_VCODEC_B_RPU_ACR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Using the incoming HVMID, this register controls access to the global register space.

SS1080P_1_SMMU_VCODEC_B_RPU_ACR

Bits	Name	Description
31:0	RWE	Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the entire block of registers within the SMMU's 4KB global address space, including this register itself. A VMID identified by this register is also permitted global access to all context banks. In practice, this register designates the VMID(s) that can act as SROT.

14.29.2 SMMU Context Bank Registers

There are a configurable number (1 to 9) of context banks in the SMMU. Each context bank consists of a set of registers in a unique 4KB address space.

14.29.2.1 SMMU context bank control registers

0x07B00000+0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_SCTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank System Control Register controls various architected SMMU features

SS1080P_1_SMMU_VCODEC_B_CBn_SCTLR

Bits	Name	Description
31:5	RESERVED_2	
4	BE	Governs the order byte order or "endianness" of the page table entries. When set to 0, page table entries are in little endian format, so that their least significant byte is in byte 0 of the 32 bit entry. When set to 1, page table entries are in big endian format, so that their most significant byte is in byte 0 of the 32 bit entry.
3	RESERVED_1	Reserved for HAF, Hardware access flag. This bit governs whether the access flag is managed by hardware or software. The SMMU supports software access flag management only, so this bit is read-only and internally driven to 0.
2	AFE	Access flag enable. When AFE = 0, the access flag field is not supported and the AP[0] page table entry field acts as a bit of the overall AP[2:0] field to determining access permissions. When AFE = 1, the AP[0] page table entry field becomes the access flag, and the reduced number of access permission combinations is specified by AP2:1], and SMMU hardware will signal an Access Flag fault if a request targets a page for which the access flag is 0.
1	TRE	TEX remap enable. This bit governs the mapping of the page table entry TEX[2:0],C,B and SH fields into an SMMU TLB entry, and thus the translation of the AMEMTYPE[2:0], ASHARED and AINNERSHARED bus attributes. When TRE = 0, the TLB value is determined directly from the page table entry fields.
0	M	MMU enable bit. When set to 1, this context bank is enabled for translating requests. When set to 0, accesses bypass the TLB, and there is no address translation, access permission checking or attribute mapping. Incoming master requests are passed through unchanged.

0x07B00004+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_ACTLR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank auxiliary control register controls various implementation specific features.

SS1080P_1_SMMU_VCODEC_B_CBn_ACTLR

Bits	Name	Description
31:19	RESERVED	
18	RESERVED_2	

SS1080P_1_SMMU_VCODEC_B_CBn_ACTLR (cont.)

Bits	Name	Description
17:16	V2PCFG	VA-to-PA configuration. Governs operation of VA-to-PA commands that miss in the TLB 0x0: terminate (Record TLB Miss context fault in SMMU_CBn_PAR) 0x1: software table update (Translate based on values in SMMU_CBn_TLBFLPTER and SMMU_CBn_TLBSLPTER) 0x2: hardware table walk (Translate based on value of PTE read from page table in memory) 0x3: reserved
15	TIPCF	Governs whether or not all subsequent requests using this context bank should be terminated if a prior context fault has occurred and has not yet been cleared from SMMU_CBn_FSR Accesses to other context banks proceed as normal 0x0: do not terminate (System MMU will attempt to process subsequent requests despite the presence of an existing context fault in SMMU_CBn_FSR. SMMU_CBn_FSR will be set if the subsequent access also encounters a context fault) 0x1: terminate (All subsequent accesses terminated by the System MMU as RAZ/WI, even if SMMU_CBn_ACTLR[TLBMCFG, CFCFG] configured for stall mode. SMMU_CBn_FSR set when access is terminated due to TIPCF = 1. Presence of SMMU_CBn_FSR when SMMU_CBn_ACTLR is 1 implies that the later exceptions must have been simply the forced terminations due to the prior context fault. Error optionally reported to the requesting master, according to the client port bus protocol, f SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus if SMMU_CBn_ACTLR is 1.)

SS1080P_1_SMMU_VCODEC_B_CBn_ACTLR (cont.)

Bits	Name	Description
14	CFCFG	(context fault configuration) Governs the behavior of all context faults except TLB miss TLB miss context faults are governed by SMMU_CBn_ACTLR[TLBMCFG] 0x0: terminate (Access terminates at the System MMU as RAZ/WI. Context fault exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x1: stall (Requesting master's access stalled while System MMU waits for managing processor to resolve context fault. Context fault exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode)

SS1080P_1_SMMU_VCODEC_B_CBn_ACTLR (cont.)

Bits	Name	Description
13:12	TLBMCFG	(TLB miss configuration) Governs the behavior of client accesses that miss in the TLB 0x0: pass-through (Access passed through to targeted slave without translation, attribute control, or access permission checking. Effectively, behavior is as if SMMU_CBn_SCTLR = 0 i.e., MMU disabled for this context bank. TLB miss not considered a context fault. TLB miss exception not recorded in SMMU_CBn_FSR. TLB miss exception not reported to requesting master. SMMU_contextFaultIrptReq interrupt output not asserted) 0x1: terminate (Access terminates at the System MMU as RAZ/WI,TLB miss exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x2: stall (Requesting master's access stalled while System MMU waits for managing processor to update TLB. TLB miss exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode) 0x3: HTW (Hardware table walk . Requesting master's access stalled while System MMU accesses page table. The is TLB updated and requesting master's access resumed after obtaining valid entry from page table. If translation fault, then access either terminates or stalls according to setting of SMMU_CBn_ACTLR)
11	DNLV2PA	(disable non-locking VA-to-PA allocation) Governs whether or not TLB misses due to non-locking VA-to-PA commands will allocate a new entry This field is ignored for locking VA-to-PA operations (SMMU_CBn_TLBLKCR[LKE] = 1)
10	DNA	(disable normal allocation) Governs whether or not TLB misses due to client port accesses will allocate a new entry
9:8	PRIVCFG	0x0: apriv (System MMU uses APRIV signal supplied by master as user/supervisor indicator 1 = supervisor) 0x1: reserved 0x2: User (System MMU ignores APRIV; treats all requests using this context bank as user) 0x3: Supervisor (System MMU ignores APRIV; treats all requests using this context bank as supervisor)

SS1080P_1_SMMU_VCODEC_B_CBn_ACTLR (cont.)

Bits	Name	Description
7:5	RESERVED_1	
4	RCNSH	(redirect cacheable-non-shareable) Governs whether or not cacheable accesses that are non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache, even though the locations are not being coherently shared with Scorpion-MP
3	RCISH	(redirect cacheable-inner-shareable) Governs whether or not cacheable accesses that are inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
2	RCOSH	(redirect cacheable-outer-shareable) Governs whether or not cacheable accesses that are outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
1	CFEIE	(context fault error interrupt enable) Governs whether or not client port request context faults are reported directly to the interrupt controller via the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus Interrupt output is asserted if SMMU_CBn_ACTLR[CFEIE] is 1 and any context fault bits are set in SMMU_CBn_FSR Such interrupts would generally be directed to the interrupt controller of whichever processor is currently managing this context bank of the System MMU Reset state : 0
0	CFERE	(context fault error report enable) Governs whether or not client port request context faults that are configured for terminate mode (or that are explicitly terminated after stall mode) are reported to the requesting master, according to the client port bus protocol All error types reported via AXI port will use decode error rather than slave error All context faults are recorded in SMMU_CBn_FSR, regardless of the value of this field.

0x07B00008+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_CONTEXTIDR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context ID register holds the ASID associated with this context bank

SS1080P_1_SMMU_VCODEC_B_CBn_CONTEXTIDR

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Specifies the 8 bit ASID value assigned to this context bank. The ASID can be included in the key comparison of TLB entries. .

0x07B00010+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_TTBR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR0 is used for low order virtual addresses, typically private pages for a given process.

SS1080P_1_SMMU_VCODEC_B_CBn_TTBR0

Bits	Name	Description
31:7	PA	BIts 31:7 of the physical address of the base of the page table. The actual LSB of the base address is bit 14-N, where N is set in register TTCR
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07B00014+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_TTBR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR1 is used for high order virtual addresses, typically global pages for a given VMID, or kernal mappings.

The context bank auxiliary control register controls various implementation specific features.

SS1080P_1_SMMU_VCODEC_B_CBn_TTBR1

Bits	Name	Description
31:14	PA	BIts 31:14 of the physical address of the base of the page table.
13:7	RESERVED_2	
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED_1	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07B00018+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_TTBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table control register, which specifies the size of the virtual address space that uses TTBR0.

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SS1080P_1_SMMU_VCODEC_B_CBn_TTBCR

Bits	Name	Description
31:6	RESERVED_2	
5	PD1	Page disable 1; if this bit is set, hardware table walks attempting to use TTBR1will result in a first level descriptor translation fault. If clear, TTBR1 contents are used.
4	PD0	Page disable 0; if this bit is set, hardware table walks attempting to use TTBR0 will result in a first level descriptor translation fault. If clear, TTBR0 contents are used.
3	RESERVED_1	
2:0	N	N[2:0] specifies the number of upper order virtual address bits which must be 0 in order for translations to use the table pointed to by TTBR0. If any of these bits are non-zero, TTBR1 is used for the lookup. If N is 0, only TTBR0 is used.

0x07B0001C+0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_PAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The physical address register captures the physical address value resulting from the execution of a VA-to-PA command

Field definitions vary according to whether or not there is a context fault associated with the requested translation

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SS1080P_1_SMMU_VCODEC_B_CBn_PAR

Bits	Name	Description
31:12	PAR_FAULT_INFO_312	
11	RESERVED_2	
10:9	PAR_FAULT_INFO_72	
8	RESERVED_1	
7:1	PAR_FAULT_INFO_71	Encoding varies according to value in FAULT field.

SS1080P_1_SMMU_VCODEC_B_CBn_PAR (cont.)

Bits	Name	Description
0	FAULT	(fault status) This field will be 1 when a context fault is associated with the requested translation, and 0, when there is no context fault associated with the requested translation.

0x07B00020+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_FSR, n=[0..1]

Type: Read/WriteClear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The Fault Status Register records status information for client accesses that encounter exceptions within the context bank, e.g., translation faults.This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data.

This prevents inadvertent clearing of new faults when writing the register to clear an old fault.

The presence of an asserted value on any bit in this register (except the SS bit) is what prompts the assertion (when enabled by SMMU_CBn_ACTLR[CFEIE]) of the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus.

Therefore, these bits must be cleared by the interrupt handler

This is contrasted with the fields in the SMMU_CBn_FSYNRn registers, which are merely the "syndrome" of the fault indicated by SMMU_CBn_FSR.

SS1080P_1_SMMU_VCODEC_B_CBn_FSR

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"

SS1080P_1_SMMU_VCODEC_B_CBn_FSR (cont.)

Bits	Name	Description
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07B00024+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_FSRRESTORE, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Allows SW to force a value into the SMMU_CBn_FSR register.

SS1080P_1_SMMU_VCODEC_B_CBn_FSRRESTORE

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode

SS1080P_1_SMMU_VCODEC_B_CBn_FSRRESTORE (cont.)

Bits	Name	Description
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07B00028+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_FAR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The Fault Address Register records the virtual address of client accesses that encounter exceptions within the context bank, e.g. translation faults. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

SS1080P_1_SMMU_VCODEC_B_CBn_FAR

Bits	Name	Description
31:0	VA	VA[31:0] of errant client access

0x07B0002C+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_FSYNR0, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

NOTE Omission of VMID field from this register, as VMID can only be made visible to SROT, and not to general OS software that manages the context bank registers.

SS1080P_1_SMMU_VCODEC_B_CBn_FSYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] (ATID field of errant request)
23:16	RESERVED	
15:13	ABID	ABID[2:0] (ABID field of errant request)
12:8	APID	APID[4:0] (APID field of errant request)
7:0	AMID	AMID[7:0] (AMID field of errant request)

0x07B00030+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_FSYNR1, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

SS1080P_1_SMMU_VCODEC_B_CBn_FSYNR1

Bits	Name	Description
31:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO (AOOO field of the errant request)
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request
15:12	ALEN	ALEN[3:0]field of the errant request
11	RESERVED_2	
10	ABURST	field of the errant request
9	RESERVED_1	
8	AWRITE	field of the errant request
7	AINST	field of the errant request
6	APROTNS	field of the errant request
5	APRIV	field of the errant request
4	AINNERSHARED	(AINNERSHARED field of the errant request)

SS1080P_1_SMMU_VCODEC_B_CBn_FSYNR1 (cont.)

Bits	Name	Description
3	ASHARED	(ASHARED field of the errant request)
2:0	AMEMTYPE	AMEMTYPE[2:0] (AMEMTYPE field of the errant request)

0x07B00034+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_PRRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs memory type and shareability attributes of requests that are both MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1)

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) and/or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, memory type encoding is as follows:

- 0b00 = strongly-ordered
- 0b01 = device
- 0b10 = normal
- 0b11 = reserved

SS1080P_1_SMMU_VCODEC_B_CBn_PRRR

Bits	Name	Description
31	NOS7	not-outer-shareable class 7
30	NOS6	not-outer-shareable class 6
29	NOS5	not-outer-shareable class 5
28	NOS4	not-outer-shareable class 4
27	NOS3	not-outer-shareable class 3
26	NOS2	not-outer-shareable class 2
25	NOS1	not-outer-shareable class 1
24	NOS0	not-outer-shareable class 0

SS1080P_1_SMMU_VCODEC_B_CBn_PRRR (cont.)

Bits	Name	Description
23:20	RESERVED	
19	SHNMSH1	(shareable attribute for normal memory accesses with SH=1) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1
18	SHNMSH0	(shareable attribute for normal memory accesses with SH=0) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0
17	SHDSH1	SHDSH1 (shareable attribute for device accesses with SH=1) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1 [
16	SHDSH0	SHDSH0 (shareable attribute for device accesses with SH=0) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0 [
15:14	MTC7	MTC7[1:0] (memory type class 0)
13:12	MTC6	MTC6[1:0] (memory type class 0)
11:10	MTC5	MTC5[1:0] (memory type class 0)
9:8	MTC4	MTC4[1:0] (memory type class 0)
7:6	MTC3	MTC3[1:0] (memory type class 0)
5:4	MTC2	MTC2[1:0] (memory type class 0)
3:2	MTC1	MTC1[1:0] (memory type class 0)
1:0	MTC0	MTC0[1:0] (memory type class 0)

0x07B00038+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_NMRR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs the cache policy of MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1) requests for which the memory type is mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0) or the memory type is mapped to a type other than normal memory (SMMU_CBn_PRRR[MTCn] != 0b10)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, inner-cache and outer-cache policy encodings are as follows:

- 0b00 = non-cacheable
- 0b01 = cacheable, copy-back, write-allocate
- 0b10 = cacheable, write-through, write-no-allocate
- 0b11 = cacheable, copy-back, write-no-allocate

SS1080P_1_SMMU_VCODEC_B_CBn_NMRR

Bits	Name	Description
31:30	OCPC7	OCPC7[1:0] (inner-cache policy class 7)
29:28	OCPC6	OCPC6[1:0] (inner-cache policy class 6)
27:26	OCPC5	OCPC5[1:0] (inner-cache policy class 5)
25:24	OCPC4	OCPC4[1:0] (inner-cache policy class 4)
23:22	OCPC3	OCPC3[1:0] (inner-cache policy class 3)
21:20	OCPC2	OCPC2[1:0] (inner-cache policy class 2)
19:18	OCPC1	OCPC1[1:0] (inner-cache policy class 1)
17:16	OCPC0	OCPC0[1:0] (inner-cache policy class 0)
15:14	ICPC7	ICPC7[1:0] (inner-cache policy class 7)
13:12	ICPC6	ICPC6[1:0] (inner-cache policy class 6)
11:10	ICPC5	ICPC5[1:0] (inner-cache policy class 5)
9:8	ICPC4	ICPC4[1:0] (inner-cache policy class 4)
7:6	ICPC3	ICPC3[1:0] (inner-cache policy class 3)
5:4	ICPC2	ICPC2[1:0] (inner-cache policy class 2)
3:2	ICPC1	ICPC1[1:0] (inner-cache policy class 1)
1:0	ICPC0	ICPC0[1:0] (inner-cache policy class 0)

0x07B0003C+0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_TLBLKCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB lock control register governs the TLB locking mechanism and TLB invalidate operations.Write access to this register is governed by SMMU_CR[TLBLKCRWE]

When SMMU_CR[TLBLKCRWE] is 0, writes to SMMU_CBn_TLBLKCR are ignored

Read access is still permitted

SROT can set SMMU_CR[TLBLKCRWE] to 1 to allow operating environment(s) to manage the TLB locking mechanism

Management amongst multiple operating environments must be coordinated via semaphore

SS1080P_1_SMMU_VCODEC_B_CBn_TLBLKCR

Bits	Name	Description
31:24	RESERVED_2	
23:16	VICTIM	VICTIM[7:0] Indicates the TLB index at which the next normal (non-locking) allocation will occur Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context
15:8	FLOOR	FLOOR[7:0] Indicates the TLB index from which round-robin replacement on normal (non-locking) allocations occurs TLB entries at indices below this value are locked Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context banks
7:4	RESERVED_1	

SS1080P_1_SMMU_VCODEC_B_CBn_TLBLKCR (cont.)

Bits	Name	Description
3	TLBIVAACFG	(TLBIVAA configuration) TLBIVAACFG = 0 - flash-invalidate SMMU_CBn_TLBIVAA commands flash-invalidate the entire TLB, without regard to locking, security, address, and/or VMID value TLBIVAACFG = 1 - selective SMMU_CBn_TLBIVAA commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank VA field of TLB entry matches VA designated by SMMU_CBn_TLBIVAA command NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked
2	TLBIASIDCFG	(TLBIASID configuration) TLBIASIDCFG = 0 - flash-invalidate SMMU_CBn_TLBIASID commands flash-invalidate the entire TLB, without regard to locking, security, VMID, and/or ASID values TLBIASIDCFG = 1 - selective SMMU_CBn_TLBIASID commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command TLB entry is not global (NG field is 1) NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
1	TLBIALLCFG	(TLBIALL configuration) TLBIALLCFG = 0 - flash-invalidate SMMU_CBn_TLBIALL commands flash-invalidate the entire TLB, without regard to locking, security, and/or VMID value TLBIALLCFG = 1 - selective SMMU_CBn_TLBIALL commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked

SS1080P_1_SMMU_VCODEC_B_CBn_TLBLKCR (cont.)

Bits	Name	Description
0	LKE	(lock enable) Governs whether or not TLB entries established by VA-to-PA commands upon TLB misses are locked LKE = 0 (normal, non-locking) Allocate VA-to-PA TLB entry (if TLB miss) at the index specified by SMMU_CBn_TLBLKCR[VICTIM] Allocation is disabled if SMMU_CBn_ACTLR[DNLV2PA] is 1 Increment SMMU_CBn_TLBLKCR[VICTIM] by 1 (only if new entry allocated) Wrap back to the value of SMMU_CBn_TLBLKCR[FLOOR] when the last entry is written LKE = 1 (locking) Search TLB for specified VA and invalidate if found Provides atomicity between the invalidate and the new allocation within the locked region Allocate VA-to-PA TLB entry at the index specified by data operand bits 7:0 of the VA-to-PA command This value must be less than SMMU_CBn_TLBLKCR[FLOOR] in order for it to remain locked Allocation occurs even if non-locking allocation is disabled due to SMMU_CBn_ACTLR[DNLV2PA] = 1

0x07B00040+0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_V2PSR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The VA-to-PA status register records the hit/miss status and TLB index or V2Pxx and TLB invalidate commands.

SS1080P_1_SMMU_VCODEC_B_CBn_V2PSR

Bits	Name	Description
31:16	RESERVED_2	
15:8	INDEX	INDEX[7:0] Indicates the index of the TLB entry associated with the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command If SMMU_CBn_V2PSR[HIT] is 0, then SMMU_CBn_V2PSR[INDEX] is the index to which the entry was allocated (if allocated at all) If SMMU_CBn_V2PSR[HIT] is 1, then SMMU_CBn_V2PSR[INDEX] is the index of the entry which hit
7:1	RESERVED_1	

SS1080P_1_SMMU_VCODEC_B_CBn_V2PSR (cont.)

Bits	Name	Description
0	HIT	Indicates whether or not there was a TLB hit (prior to allocation, if any) on the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command

0x07B00044+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_TLBFLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB first level PTE register holds the first level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

This register (together with SMMU_CBn_TLBSLPTER) is used as the source of the translation information for VA-to-PA operations when the MMU is enabled (SMMU_CBn_SCTLR[M] = 1) and the operations are configured for software table update (SMMU_CBn_ACTLR[V2PCFG] = 0b01)

Field definitions vary according to the type of PTE (fault, page, section, or supersection), and come directly from the ARMv7 architecture's PTE formats

SS1080P_1_SMMU_VCODEC_B_CBn_TLBFLPTER

Bits	Name	Description
31:10	FL_PTE_HI	
9:5	RESERVED	
4:2	FL_PTE_LO	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	This field should be set to 0b00 or 0b11 to indicate that the translation should result in a context fault, and the rest of the fields are defined as indicated in this section If this field is not 0b00 or 0b11, then the PTE is of some other type (see other sections for the field definitions for those types)

0x07B00048+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_TLBSLPTER, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB second level PTE register holds the second level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

Field definitions vary according to the type of PTE (fault, 64KB or 4KB), and come directly from the ARMv7 architecture's PTE format

SS1080P_1_SMMU_VCODEC_B_CBn_TLBSLPTER

Bits	Name	Description
31:2	SL_PTE	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	0x0: fault

0x07B0004C+0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_BFBCR, n=[0..1]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The burst fetch buffer configuration register governs the operation of the "burst fill" feature of the SMMU.

SS1080P_1_SMMU_VCODEC_B_CBn_BFBCR

Bits	Name	Description
31:12	STRIDE	(stride amount) 4KB-aligned value to be added to virtual address on demand TLB miss for filling subsequent BFB Stride of minimum 4KB alignment useful for preventing stride burst fetch until final PTE of the demand BFB entry is used
11:8	SLVIC	(second-level victim) Indicates the SLBFB index at which the next round-robin allocation will occur
7:4	FLVIC	(first-level victim) Indicates the FLBFB index at which the next round-robin allocation will occur
3	RESERVED	
2	SFVS	(stride-fetch victim selection) SFVS. = 0 (replace normal round-robin victim-selected entry) Useful when stride is larger than the VA space represented by the four PTEs in the demand BFB entry, but the client access pattern is for more than just the initial PTE in that demand BFB entry SFVS. = 1 (replace same BFB used by demand VA for which the stride burst is being performed) Useful when stride is the same as the VA space represented by an individual PTE in the demand BFB entry (such that the stride won't miss against the BFB until the last PTE of the demand BFB entry is accessed), and/or when the client access pattern only uses the initial PTE in the demand BFB entry

SS1080P_1_SMMU_VCODEC_B_CBn_BFBCR (cont.)

Bits	Name	Description
1	BFBSFE	(burst fetch buffer stride fetch enable) Enables stride burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Stride burst fetch is for the block of four PTEs associated with VA+stride VA is the "demanded" VA from the client (or VA-to-PA command) Stride value is specified by SMMU_CBn_BFBCR[STRIDE] Stride burst fetch only occurs if demand access for VA misses in TLB (could hit in BFB) and address VA+stride misses in both TLB and BFB
0	BFBDFE	(burst fetch buffer demand fetch enable) Enables demand burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Demand burst fetch is for the block of four PTEs associated with the "demanded" VA from the client (or VA-to-PA command) Demand burst fetch only occurs if demand access misses in both TLB and BFB

0x07B00800+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_TLBIALL, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate all command register invalidates all TLB entries matching the VMID associated with this context bank. Data operand is ignored.

SS1080P_1_SMMU_VCODEC_B_CBn_TLBIALL

Bits	Name	Description
31:0	RESERVED	

0x07B00804+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_TLBIASID, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by ASID command register invalidates TLB entries matching the specified ASID and matching the VMID associated with this context bank.Invalidates TLB entries which are associated with the designated ASID and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIASIDCFG] governs whether command flash-invalidates entire TLB array or just the entries matching the VMID, ASID, and security state

TLBIASIDCFG = 0 - flash-invalidate

SMMU_CBn_TLBIASID command flash-invalidates the entire TLB, without regard to locking, security, VMID, and/or ASID values

TLBIASIDCFG = 1 - selective

SMMU_CBn_TLBIASID command invalidates only entries that match all of the following conditions:

- VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]
- ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command data operand
- TLB entry is not global (NG field is 1)
- NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
- Locking is not considered (matching entries are invalidated even if locked)
- ASID field of command specifies the ASID value of the TLB entries to be invalidated

SS1080P_1_SMMU_VCODEC_B_CBn_TLBIASID

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Actual ASID value

0x07B00808+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_TLBIVA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA command invalidates TLB entries matching the designated VA, ASID and the VMID associated with this context bank.

Matching entry determined as follows:

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIVA command data operand (or TLB entry is global - NG field is 0)

VA field of TLB entry matches VA value designated by the SMMU_CBn_TLBIVA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIVA command

Locking is not considered (matching entry is invalidated even if locked)

Data operand specifies the VA and ASID value of the TLB entry to be invalidated

SS1080P_1_SMMU_VCODEC_B_CBn_TLBIVA

Bits	Name	Description
31:12	VA	VA[31:12]
11:8	RESERVED	
7:0	ASID	ASID[7:0] value

0x07B0080C+0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_TLBIVAA, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA all ASIDS command invalidates TLB entries matching the designated VA and the VMID associated with this context bank, regardless of ASID.Invalidates TLB entries which are associated with the designated VA, regardless of ASID, and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIVAACFG] governs whether command flash-invalidates entire TLB array or just the non-locked entries matching the VMID, ASID, and security state

TLBIVAACFG = 0 - flash-invalidate

SMMU_CBn_TLBIVAA command flash-invalidates the entire TLB, without regard to locking, security, address, and/or VMID value

TLBIVAACFG = 1 - selective

SMMU_CBn_TLBIVAA command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

VA field of TLB entry matches VA designated by the SMMU_CBn_TLBIVAA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command

Entry is unlocked

SS1080P_1_SMMU_VCODEC_B_CBn_TLBIVAA

Bits	Name	Description
31:12	VA	VA[31:12]
11:0	RESERVED	

0x07B00810+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_V2PRR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

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SS1080P_1_SMMU_VCODEC_B_CBn_V2PRR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	

SS1080P_1_SMMU_VCODEC_B_CBn_V2PRR (cont.)

Bits	Name	Description
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07B00814+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_V2PPW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

SS1080P_1_SMMU_VCODEC_B_CBn_V2PPW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07B00818+ 0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_V2PUR, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR.

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB.

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB.

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

SS1080P_1_SMMU_VCODEC_B_CBn_V2PUR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07B0081C+0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_V2PUW, n=[0..1]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID] ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

.Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE.

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry.

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking).

SS1080P_1_SMMU_VCODEC_B_CBn_V2PUW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07B00820+0x1000*n SS1080P_1_SMMU_VCODEC_B_CBn_RESUME, n=[0..1]

Type: Write/command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB resume command causes the SMMU to resume operation after a stalled access.

SS1080P_1_SMMU_VCODEC_B_CBn_RESUME

Bits	Name	Description
31:1	RESERVED	
0	TNR	Terminate/not retry When TNR is written as 0, indicates that the stalled access should be retried by the system MMU. When written as 1, indicates that this stalled transaction is terminated by the system MMU. The error is optionally reported to the requesting master, using the client port bus protocol, if SMMU_CNn_ACTLR[CFERE] == 1. Interrupt optionally remains asserted via SMMU_M2VCBRn[IRPTINDX] selected SMMU_contextFaultIrptReq bit, only if SMMU_CBn_ACTLR[CFEIE] is 1, and only if SMMU_CBn_FSR has not been cleared by software priori to issuing this command..

14.30 3D Graphics SMMU Registers (0x07C00000 SMMU_GFX3D_BASE)

This section contains 3D Graphics SMMU registers.

14.30.1 SMMU Global Registers

14.30.1.1 SMMU VMID/CBNDX mapping registers

0x07CFF000+0x4*n GFX3D_SMMU_GFX3D_M2VCBRn, n=[0..31]

Type: Read/Write
Clock: AXI_CLK
Reset State: Undefined

SMMU_M2VCBRm registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

GFX3D_SMMU_GFX3D_M2VCBRn

Bits	Name	Description
31:28	RESERVED_2	
27:25	BPMEMTYPE	(bypass memory type) Supplies the AMEMTYPE attributes for client requests which bypass the System MMU when SMMU_M2VCBRn[BPMTCFG] = 1 See reference section for AMEMTYPE encoding definitions
24	BPMTCFG	(bypass memory type configuration) Governs the memory type (AMEMTYPE) attributes of client requests which bypass the System MMU BPMTCFG = 0 - use AMEMTYPE Bypass requests use AMEMTYPE signal supplied by client master BPMTCFG = 1 - use SMMU_M2VCBRn[BPMEMTYPE] Bypass requests use SMMU_M2VCBRn[BPMEMTYPE] Reset state : 0
23:22	NSCFG	(non-secure configuration) Governs the incoming security designation of client requests NSCFG = 0b00 - use APROTNS Use APROTNS signal supplied by client master NSCFG = 0b01 - reserved NSCFG = 0b10 - secure System MMU ignores APROTNS; treats all requests as secure NSCFG = 0b11 - non-secure System MMU ignores APROTNS; treats all requests as non-secure Reset state : 0

GFX3D_SMMU_GFX3D_M2VCBRn (cont.)

Bits	Name	Description
21:20	BPSHCFG	(bypass shareability configuration) Governs the shareability realm (ASHARED and AINNERSHARED) attributes of client requests which bypass the System MMU BPSHCFG = 0b00 - use ASHARED and AINNERSHARED Bypass requests use ASHARED and AINNERSHARED signals supplied by client master BPSHCFG = 0b01 - outer-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 0 BPSHCFG = 0b10 - inner-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 1 BPSHCFG = 0b11 - non-shareable Bypass requests set ASHARED = 0, AINNERSHARED = 0 Reset state : 0
19	BPRCNSH	(bypass redirect cacheable-non-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache Reset state : 0
18	BPRCISH	(bypass redirect cacheable-inner-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0
17	BPRCOSH	(bypass redirect cacheable-outer-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0

GFX3D_SMMU_GFX3D_M2VCBRn (cont.)

Bits	Name	Description
16	BYPASSD	Bypass disable for this index Governs whether or not client port accesses using this mapping table entry are actually permitted to "bypass" the System MMU when such bypass is indicated (either due to CBNDX = 255 or due to the master asserting the "SMMU bypass" input) This field is ignored (and operates as if it were 0) if SMMU_CR[CLIENTPD] is 1 BYPASSD = 0 - bypass enabled Bypass requests truly bypass the System MMU and "pass-through" to the fabric (no translation, access control, or attribute generation) No cycle of latency for System MMU context bank access Bypass request not considered an error Bypass request error not recorded in SMMU_ESR[BYPASS] Bypass error not reported to requesting master SMMU_rpuErrIrptReq interrupt output not asserted Client accesses still reference M2VCBMT to get VMID value for presentation to fabric BYPASSD = 1 - bypass disabled System MMU terminates the access as RAZ/WI Bypass request is considered an error Bypass request error is recorded in SMMU_ESR[BYPASS] If SMMU_CR[RPUERE] is 1, then bypass error reported to requesting master according to the client port bus protocol If SMMU_CR[RPUEIE] is 1, then SMMU_rpuErrIrptReq interrupt output asserted
15:8	CBNDX	Context bank index Context bank index associated with the M2VCBMT index CBNDX = 255 indicates no context bank assigned ("bypass")
7:5	RESERVED_1	
4:0	VMID	Virtual machine ID VMID value associated with the M2VCBMT index Must be programmed consistently with the SMMU_CBACRn[CBVMID] field for the context bank designated by SMMU_M2VCBRm[CBNDX]

14.30.1.2 SMMU context bank access control registers

0x07CFF800+0x4*n GFX3D_SMMU_GFX3D_CBACRn, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs configuration port access to the associated context bank registers.

GFX3D_SMMU_GFX3D_CBACRn

Bits	Name	Description
31:24	IRPTNDX	(interrupt index) Interrupt output number used for context faults associated with this context bank (use SMMU_contextFaultIrptReq[IRPTNDX])
23:21	RESERVED	
20:16	CBVMID	(context bank VMID) Specifies the VMID with which the client masters using the context bank are associated Must be programmed consistently with the M2VCBMT entries that are configured to use the associated context bank This field is used by configuration port commands that need the context bank's VMID value in order to access the TLB (e.g., SMMU_CBn_TLBIVMID, SMMU_CBn_V2Pxx)
15:10	RESERVED_2	
9	RWGE	Read/write global enable. Setting this bit allows access to the context bank registers from any VMID
8	RWE	Read/write enable. Indicates that the RWVMID field is valid.
7:5	RESERVED_1	
4:0	RWVMID	Specifies owner VMID with full read/write access to the registers in the associated context bank "n".

14.30.1.3 SMMU TLB software access registers

0x07CFFE00 GFX3D_SMMU_GFX3D_TLBRSW

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Writing to this address requests that the TLB entry at INDEX be read into the SMMU_TLBTRn registers

GFX3D_SMMU_GFX3D_TLBRSW

Bits	Name	Description
31:10	RESERVED	

GFX3D_SMMU_GFX3D_TLBRSW (cont.)

Bits	Name	Description
9:8	TLBBFBS	This field selects the TLB, TFBFB, SLBFB 0x0: Selecting TLB 0x1: Not defined 0x2: Selecting FL BFB 0x3: Selecting SL BFB
7:0	INDEX	TLB index to be read.

0x07CFFE80 GFX3D_SMMU_GFX3D_TLBTR0

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

This register holds part of TLB entry read by the last TLBRSW command.

GFX3D_SMMU_GFX3D_TLBTR0

Bits	Name	Description
31:23	RESERVED_4	
22:20	DPSIZC	3 bit decode page size field from CAM-side of TLB CAM-RAM) Same determination and encoding as for DPSIZR The CAM-side copy of this field is used for hit/miss determination in the TLB CAM array
19	RESERVED_3	
18:16	DPSIZR	(3 bit decode page size field from RAM-side of TLB CAM-RAM) Determined from the size fields of the page table entry Encodes the page size as follows: all other values reserved/unused The RAM-side copy of this field is used for virtual ’ physical address formation 0x0: 4KB page 0x1: 64KB page 0x3: 1MB page 0x7: 16MB page
15:12	RESERVED_2	
11	MT2	(memory type bit 2) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[2] attribute bus on the request output of the System MMU

GFX3D_SMMU_GFX3D_TLBTR0 (cont.)

Bits	Name	Description
10	MT1	(memory type bit 1) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[1] attribute bus on the request output of the System MMU
9	MT0	(memory type bit 0) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[0] attribute bus on the request output of the System MMU
8	SH	(shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's outer-shareable realm This field becomes the ASHARED attribute on the request output of the System MMU
7	ISH	(inner-shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's inner-shareable realm This field becomes the AINNERSHARED attribute on the request output of the System MMU
6	NSDESC	(non-secure descriptor) This TLB entry field is a modified version of the corresponding bit of the page table entry Qualified by the NS-prot attribute of the incoming request which prompted the allocation of the TLB entry, such that if the incoming NS-prot attribute was 1 (non-secure), then the NS-desc field of the page table entry was ignored, and the NS-desc field of the TLB entry was forced to 1 Indicates whether the associated memory page contains secure (NS-desc=0) or non-secure (NS-desc=1) information This field becomes the NS-prot attribute on the request output of the System MMU
5	RESERVED_1	

GFX3D_SMMU_GFX3D_TLBTR0 (cont.)

Bits	Name	Description
4	XN	(execute never permission) This TLB entry field comes directly from the corresponding bit of the page table entry
3	UW	(user write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
2	UR	(user read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
1	PW	(privileged write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
0	PR	(privileged read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]

0x07CFFE84 GFX3D_SMMU_GFX3D_TLBTR1

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

GFX3D_SMMU_GFX3D_TLBTR1

Bits	Name	Description
31:12	PA	Physical address [31:12] field of the TLB entry
11:5	RESERVED	
4:0	VMID	VMID [4:0]field of the TLB entry)

0x07CFFE88 GFX3D_SMMU_GFX3D_TLBTR2

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

GFX3D_SMMU_GFX3D_TLBTR2

Bits	Name	Description
31:12	VA	virtual address field [31:12] of the TLB entry
11	RESERVED	
10	NG	(not global field from page table entry) Indicates whether the page is private to the specified ASID (NG=1) or global to all ASIDs within the VMID using this context bank (NG=0)
9	NSTID	(non-secure tag ID field of the TLB entry) Indicates whether the TLB entry belongs to the secure world (NSTID=0) or the non-secure world (NSTID=1) This field is comned against the incoming NS-prot attribute of the master request as part of TLB hit/miss determination
8	V	valid field of the TLB entry
7:0	ASID	ASID[7:0] field of the TLB entry

0x07CFFE8C GFX3D_SMMU_GFX3D_TESTBUSCR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

Governs which signals (if any) from the system SMMU core or wrapper design hierarchy are sent out to the system via a testbus for diagnostic, and also to the system profiling and diagnostic monitor(SPDM).

GFX3D_SMMU_GFX3D_TESTBUSCR

Bits	Name	Description
31:28	SPDM3SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[3]
27:24	SPDM2SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[2]
23:20	SPDM1SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[1]
19:16	SPDM0SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[0]
15:14	TBHSEL	Testbus highselect It governs which set of signals are to testbus[31:16] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL

GFX3D_SMMU_GFX3D_TESTBUSCR (cont.)

Bits	Name	Description
13:12	TBSLSEL	Testbus low select It governs which set of signals are to testbus[15:0] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL
11:10	RESERVED_2	
9:8	WGSEL	Wrapper group select It selects a particular group of signals from the SMMU wrapper hierarchy WGSEL = 0b00 - wrapper signal group 0 WGSEL = 0b01 - wrapper signal group 1 WGSEL = 0b10 - wrapper signal group 2 WGSEL = 0b11 - reserved
7:2	RESERVED_1	
1	SPDMBE	SPDM test enable Reset state : 0
0	TBE	Testbus enable, which governs whether the testbus is driven with all 0s or with the configured signals Reset state : 0

0x07CFFEFC GFX3D_SMMU_GFX3D_VR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: 32'h0000_0000

Note that the DCPBP/DCPPP bits prevent the pipelining of the next transaction when the current transaction is a bypass/pass-through transaction. That is, they add one more cycle of delay between the current and next transactions.

Also note that when we are in global bypass (SMMU_CR[CLIENTPD]=1), these bits should have NO effect, or at least no effect between client transactions, they can have an effect between config and client transactions is appropriate. We must be able to continue to perform fully pipelined transactions when the client port is disabled altogether.

GFX3D_SMMU_GFX3D_VR0

Bits	Name	Description
31:3	RESERVED	

GFX3D_SMMU_GFX3D_VR0 (cont.)

Bits	Name	Description
2	DCPPT	Disable client pipelining for client operations in pass-through mode Reset state : 0
1	DCPBP	Disable client pipelining for client operations in bypass mode Reset state : 0
0	DCP	Disable client pipelining Reset state : 0

0x07CFFF00 GFX3D_SMMU_GFX3D_TLBIALL

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries.

GFX3D_SMMU_GFX3D_TLBIALL

Bits	Name	Description
31:0	EXEC	Writing any value to this register invalidates all TLB entries, as specified by the contents of SMMU_CR[TLBIALLCFG]

0x07CFFF04 GFX3D_SMMU_GFX3D_TLBIVMID

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries matching the IVMID value. Precise function is governed by SMMU_CR[TLBIALLCFG].

GFX3D_SMMU_GFX3D_TLBIVMID

Bits	Name	Description
31:5	RESERVED	
4:0	IVMID	Designates VMID[4:0] value of entries to be invalidated.

14.30.1.4 SMMU configuration registers

0x07CFFF80 GFX3D_SMMU_GFX3D_CR

Type: Read/Write
Clock: AXI_BUS_CLOCK

Global configuration register.

GFX3D_SMMU_GFX3D_CR

Bits	Name	Description
31:10	RESERVED_2	
9	RESERVED_1	Reset state : 0
8	TLBIVMIDCFG	TLBIVMID configuration control. When set to 0,flash-invalidate, SMMU_TLBIVMID commands flash-invalidate the entire TLB, without regard to locking ,security and VMID value. When set to 1, selective, SMMU_TLBIVMID invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and VMID field matching the VMID specified by SMMU_TLBIVMID command. Reset state : X
7	TLBIALLCFG	TLBIALL configuration control. When set to 0, flash-invalidate, SMMU_TLBIALL commands flash-invalidate the entire TLB, without regard to locking and/or security. When set to 1, selective, SMMU_TLBIALL invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and are unlocked. Reset state : X
6	TLBLKCRWE	TLBLKCR write enable. When set to 0, writes to SMMU_CBn_TLBLKCR are ignored. When set to 1, allows operating environments to manage the TLB locking mechanism directly. Management amounst multiple operating environments must be coordinated externally between themselves. Reset state : X
5	STALLD	Global disable for stall mode. When set to 1, context bank stall modes are ignored and operate as terminate mode. Reset state : X
4	CLIENTPD	Client port disable. When set, all client accesses are forced to bypass the system MMU. There is no translation. access control, or attribute generation. This bit overrides individual SMMU_M2VCBRn[BYPASSD] settings; client requests are bypassed, even if SMMU_M2VCBRn[BYPASSD] is set to 1. Bypass request errors are not recorded in SMMU_ESR, nor reported to requesting masters. The SMMU_rpuErrIrptReq interrupt output signal is not asserted. Reset state : 1

GFX3D_SMMU_GFX3D_CR (cont.)

Bits	Name	Description
3	DCDEE	When set to 0, configuration port decode errors do not set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn are not updated. When set to 1, configuration port decode errors set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn updated with address and syndrome of error. Reset state : X
2	RPUEIE	When set, configuration port errors and client port bypass errors are reported directly to the interrupt controller via the SMMU_rputErrIrptReq interrupt output signal. Interrupt output is asserted if SMMU_CR[RPUIE_EN] is 1 and ANY bit is set in SMMU_ESR register. Reset state : 0
1	RPUERE	When set, SMMU reports configuration port errors and client port bypass errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via AXI port will use decode error, rather than slave error. Regardless of the value of this field both configuration port errors and client port bypass request errors are terminated by the SMMU as RAZ/WI, and are recorded in SMMU_ESR register. Reset state : X
0	RPUE	When set, all configuration port accesses are checked against SMMUX_RPU_ACR and/or the SMMUX_CBACRn registers for access permissions. Reset state : 0

14.30.1.5 SMMU error report registers

0x07CFFF84 GFX3D_SMMU_GFX3D_EAR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: unknown

When there is an error, holds the physical address of the errant transaction.

GFX3D_SMMU_GFX3D_EAR

Bits	Name	Description
31:0	PA	Physical address[31:0]

0x07CFFF88 GFX3D_SMMU_GFX3D_ESR

Type: Read/Write to clear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This register has read/write clear access. Reads return the value in the register, a write with a 1 set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

GFX3D_SMMU_GFX3D_ESR

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x07CFFF8C GFX3D_SMMU_GFX3D_ESRRESTORE

Type: Write
Clock: RPM_BUS_CLK
Reset State: Undefined

This register is an aliased address for SMMU_ESR, but it allows direct write access. In this way, diagnostic software can cause an error to be generated and reported.

GFX3D_SMMU_GFX3D_ESRRESTORE

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	

GFX3D_SMMU_GFX3D_ESRRESTORE (cont.)

Bits	Name	Description
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x07CFFF90 GFX3D_SMMU_GFX3D_ESYNR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

GFX3D_SMMU_GFX3D_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request
15:0	AMID	AMID[15:0] field of errant request

0x07CFFF94 GFX3D_SMMU_GFX3D_ESYNR1

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

GFX3D_SMMU_GFX3D_ESYNR1

Bits	Name	Description
31	DCD	(decode) Indicates configuration port error due to invalid/unrecognized address (e.g., a reserved register address) Includes decode errors within both the global address space and the individual context bank address space

GFX3D_SMMU_GFX3D_ESYNR1 (cont.)

Bits	Name	Description
30	AC	(access control) Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO field of the errant request
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request)
15:12	ALEN	ALEN[3:0] field of the errant request
11	RESERVED_2	
10	ABURST	ABURST[1:0] field of the errant request
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request
7	AINST	AINST field of the errant request
6	APROTNS	APROTNS field of the errant request
5	APRIV	APRIV field of the errant request
4	AINNERSHARED	AINNERSHARED field of the errant request
3	ASHARED	ASHARED field of the errant request
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

14.30.1.6 SMMU revision register

0x07CFFFF4 GFX3D_SMMU_GFX3D_REV

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the revision information for the SMMU core and wrapper.

GFX3D_SMMU_GFX3D_REV

Bits	Name	Description
31:12	RESERVED	
11:8	WRAPPER	Wrapper version
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

14.30.1.7 SMMU implementation parameter register

0x07CFFFF8 GFX3D_SMMU_GFX3D_IDR

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the parameter information for the SMMU core and wrapper

GFX3D_SMMU_GFX3D_IDR

Bits	Name	Description
31:24	NIRPT	NIRPT[7:0] Indicates number of context fault interrupt outputs (minus 1) supported by the System MMU Value can range from 0 - 255 (1 - 256 context fault interrupt outputs)
23:16	NCB	NCB[7:0] Indicates number of context banks (minus 1) supported by the System MMU Value can range from 0 - 254 (1 - 255 context banks)
15:12	TLBSIZE	TLBSIZE[3:0] Indicates log2(number of TLB entries) That is, number of TLB entries = 2 ** TLBSIZE
11	RESERVED	
10	HUM	Indicates whether or not TLB hit-under-miss behavior is supported
9	HTW	Indicates whether or not the System MMU supports hardware table walk If hardware table walk not supported (HTW=0), then software cannot set SMMU_CBn_ACTLR[TLBMCFG] to 0b10

GFX3D_SMMU_GFX3D_IDR (cont.)

Bits	Name	Description
8:0	NM2VCBMT	NM2VCBMT[8:0] Indicates number of M2VCBMT entries, with a maximum of 512 The bit width of the M2VCBMTIindex input (maximum value is 9) is equal to log base 2 of NM2VCBMT Allows for up to 7-bit MID field, plus NS-prot or other fields to select mapping [

0x07CFFFFC GFX3D_SMMU_GFX3D_RPU_ACR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Using the incoming HVMID, this register controls access to the global register space.

GFX3D_SMMU_GFX3D_RPU_ACR

Bits	Name	Description
31:0	RWE	Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the entire block of registers within the SMMU's 4KB global address space, including this register itself. A VMID identified by this register is also permitted global access to all context banks. In practice, this register designates the VMID(s) that can act as SROT.

14.30.2 SMMU Context Bank Registers

There are a configurable number (1 to 9) of context banks in the SMMU. Each context bank consists of a set of registers in a unique 4KB address space.

14.30.2.1 SMMU context bank control registers

0x07C00000+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_SCTLR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank System Control Register controls various architected SMMU features

GFX3D_SMMU_GFX3D_CBn_SCTLR

Bits	Name	Description
31:5	RESERVED_2	
4	BE	Governs the order byte order or "endianness" of the page table entries. When set to 0, page table entries are in little endian format, so that their least significant byte is in byte 0 of the 32 bit entry. When set to 1, page table entries are in big endian format, so that their most significant byte is in byte 0 of the 32 bit entry.
3	RESERVED_1	Reserved for HAF, Hardware access flag. This bit governs whether the access flag is managed by hardware or software. The SMMU supports software access flag management only, so this bit is read-only and internally driven to 0.
2	AFE	Access flag enable. When AFE = 0, the access flag field is not supported and the AP[0] page table entry field acts as a bit of the overall AP[2:0] field to determining access permissions. When AFE = 1, the AP[0] page table entry field becomes the access flag, and the reduced number of access permission combinations is specified by AP2:1], and SMMU hardware will signal an Access Flag fault if a request targets a page for which the access flag is 0.
1	TRE	TEX remap enable. This bit governs the mapping of the page table entry TEX[2:0],C,B and SH fields into an SMMU TLB entry, and thus the translation of the AMEMTYPE[2:0], ASHARED and AINNERSHARED bus attributes. When TRE = 0, the TLB value is determined directly from the page table entry fields.
0	M	MMU enable bit. When set to 1, this context bank is enabled for translating requests. When set to 0, accesses bypass the TLB, and there is no address translation, access permission checking or attribute mapping. Incoming master requests are passed through unchanged.

0x07C00004+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_ACTLR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank auxiliary control register controls various implementation specific features.

GFX3D_SMMU_GFX3D_CBn_ACTLR

Bits	Name	Description
31:19	RESERVED	
18	RESERVED_2	

GFX3D_SMMU_GFX3D_CBn_ACTLR (cont.)

Bits	Name	Description
17:16	V2PCFG	VA-to-PA configuration. Governs operation of VA-to-PA commands that miss in the TLB 0x0: terminate (Record TLB Miss context fault in SMMU_CBn_PAR) 0x1: software table update (Translate based on values in SMMU_CBn_TLBFLPTER and SMMU_CBn_TLBSLPTER) 0x2: hardware table walk (Translate based on value of PTE read from page table in memory) 0x3: reserved
15	TIPCF	Governs whether or not all subsequent requests using this context bank should be terminated if a prior context fault has occurred and has not yet been cleared from SMMU_CBn_FSR Accesses to other context banks proceed as normal 0x0: do not terminate (System MMU will attempt to process subsequent requests despite the presence of an existing context fault in SMMU_CBn_FSR. SMMU_CBn_FSR will be set if the subsequent access also encounters a context fault) 0x1: terminate (All subsequent accesses terminated by the System MMU as RAZ/WI, even if SMMU_CBn_ACTLR[TLBMCFG, CFCFG] configured for stall mode. SMMU_CBn_FSR set when access is terminated due to TIPCF = 1. Presence of SMMU_CBn_FSR when SMMU_CBn_ACTLR is 1 implies that the later exceptions must have been simply the forced terminations due to the prior context fault. Error optionally reported to the requesting master, according to the client port bus protocol, f SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus if SMMU_CBn_ACTLR is 1.)

GFX3D_SMMU_GFX3D_CBn_ACTLR (cont.)

Bits	Name	Description
14	CFCFG	(context fault configuration) Governs the behavior of all context faults except TLB miss TLB miss context faults are governed by SMMU_CBn_ACTLR[TLBMCFG] 0x0: terminate (Access terminates at the System MMU as RAZ/WI. Context fault exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x1: stall (Requesting master's access stalled while System MMU waits for managing processor to resolve context fault. Context fault exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode)

GFX3D_SMMU_GFX3D_CBn_ACTLR (cont.)

Bits	Name	Description
13:12	TLBMCFG	(TLB miss configuration) Governs the behavior of client accesses that miss in the TLB 0x0: pass-through (Access passed through to targeted slave without translation, attribute control, or access permission checking. Effectively, behavior is as if SMMU_CBn_SCTLR = 0 i.e., MMU disabled for this context bank. TLB miss not considered a context fault. TLB miss exception not recorded in SMMU_CBn_FSR. TLB miss exception not reported to requesting master. SMMU_contextFaultIrptReq interrupt output not asserted) 0x1: terminate (Access terminates at the System MMU as RAZ/WI,TLB miss exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x2: stall (Requesting master's access stalled while System MMU waits for managing processor to update TLB. TLB miss exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode) 0x3: HTW (Hardware table walk . Requesting master's access stalled while System MMU accesses page table. The is TLB updated and requesting master's access resumed after obtaining valid entry from page table. If translation fault, then access either terminates or stalls according to setting of SMMU_CBn_ACTLR)
11	DNLV2PA	(disable non-locking VA-to-PA allocation) Governs whether or not TLB misses due to non-locking VA-to-PA commands will allocate a new entry This field is ignored for locking VA-to-PA operations (SMMU_CBn_TLBLKCR[LKE] = 1)
10	DNA	(disable normal allocation) Governs whether or not TLB misses due to client port accesses will allocate a new entry
9:8	PRIVCFG	0x0: apriv (System MMU uses APRIV signal supplied by master as user/supervisor indicator 1 = supervisor) 0x1: reserved 0x2: User (System MMU ignores APRIV; treats all requests using this context bank as user) 0x3: Supervisor (System MMU ignores APRIV; treats all requests using this context bank as supervisor)

GFX3D_SMMU_GFX3D_CBn_ACTLR (cont.)

Bits	Name	Description
7:5	RESERVED_1	
4	RCNSH	(redirect cacheable-non-shareable) Governs whether or not cacheable accesses that are non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache, even though the locations are not being coherently shared with Scorpion-MP
3	RCISH	(redirect cacheable-inner-shareable) Governs whether or not cacheable accesses that are inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
2	RCOSH	(redirect cacheable-outer-shareable) Governs whether or not cacheable accesses that are outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
1	CFEIE	(context fault error interrupt enable) Governs whether or not client port request context faults are reported directly to the interrupt controller via the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus Interrupt output is asserted if SMMU_CBn_ACTLR[CFEIE] is 1 and any context fault bits are set in SMMU_CBn_FSR Such interrupts would generally be directed to the interrupt controller of whichever processor is currently managing this context bank of the System MMU Reset state : 0
0	CFERE	(context fault error report enable) Governs whether or not client port request context faults that are configured for terminate mode (or that are explicitly terminated after stall mode) are reported to the requesting master, according to the client port bus protocol All error types reported via AXI port will use decode error rather than slave error All context faults are recorded in SMMU_CBn_FSR, regardless of the value of this field.

0x07C00008+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_CONTEXTIDR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context ID register holds the ASID associated with this context bank

GFX3D_SMMU_GFX3D_CBn_CONTEXTIDR

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Specifies the 8 bit ASID value assigned to this context bank. The ASID can be included in the key comparison of TLB entries. .

0x07C00010+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_TTBR0, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR0 is used for low order virtual addresses, typically private pages for a given process.

GFX3D_SMMU_GFX3D_CBn_TTBR0

Bits	Name	Description
31:7	PA	BIts 31:7 of the physical address of the base of the page table. The actual LSB of the base address is bit 14-N, where N is set in register TTCR
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07C00014+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_TTBR1, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR1 is used for high order virtual addresses, typically global pages for a given VMID, or kernal mappings.

The context bank auxiliary control register controls various implementation specific features.

GFX3D_SMMU_GFX3D_CBn_TTBR1

Bits	Name	Description
31:14	PA	BIts 31:14 of the physical address of the base of the page table.
13:7	RESERVED_2	
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED_1	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07C00018+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_TTBCR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table control register, which specifies the size of the virtual address space that uses TTBR0.

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GFX3D_SMMU_GFX3D_CBn_TTBCR

Bits	Name	Description
31:6	RESERVED_2	
5	PD1	Page disable 1; if this bit is set, hardware table walks attempting to use TTBR1will result in a first level descriptor translation fault. If clear, TTBR1 contents are used.
4	PD0	Page disable 0; if this bit is set, hardware table walks attempting to use TTBR0 will result in a first level descriptor translation fault. If clear, TTBR0 contents are used.
3	RESERVED_1	
2:0	N	N[2:0] specifies the number of upper order virtual address bits which must be 0 in order for translations to use the table pointed to by TTBR0. If any of these bits are non-zero, TTBR1 is used for the lookup. If N is 0, only TTBR0 is used.

0x07C0001C+0x1000*n GFX3D_SMMU_GFX3D_CBn_PAR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The physical address register captures the physical address value resulting from the execution of a VA-to-PA command

Field definitions vary according to whether or not there is a context fault associated with the requested translation

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GFX3D_SMMU_GFX3D_CBn_PAR

Bits	Name	Description
31:12	PAR_FAULT_INFO_312	
11	RESERVED_2	
10:9	PAR_FAULT_INFO_72	
8	RESERVED_1	
7:1	PAR_FAULT_INFO_71	Encoding varies according to value in FAULT field.

GFX3D_SMMU_GFX3D_CBn_PAR (cont.)

Bits	Name	Description
0	FAULT	(fault status) This field will be 1 when a context fault is associated with the requested translation, and 0, when there is no context fault associated with the requested translation.

0x07C00020+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_FSR, n=[0..2]

Type: Read/WriteClear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The Fault Status Register records status information for client accesses that encounter exceptions within the context bank, e.g. translation faults.This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data

This prevents inadvertent clearing of new faults when writing the register to clear an old fault

The presence of an asserted value on any bit in this register (except the SS bit) is what prompts the assertion (when enabled by SMMU_CBn_ACTLR[CFEIE]) of the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus

Therefore, these bits must be cleared by the interrupt handler

This is contrasted with the fields in the SMMU_CBn_FSYNRn registers, which are merely the "syndrome" of the fault indicated by SMMU_CBn_FSR

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GFX3D_SMMU_GFX3D_CBn_FSR

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"

GFX3D_SMMU_GFX3D_CBn_FSR (cont.)

Bits	Name	Description
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07C00024+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_FSRRESTORE, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Allows SW to force a value into the SMMU_CBn_FSR register.

GFX3D_SMMU_GFX3D_CBn_FSRRESTORE

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode

GFX3D_SMMU_GFX3D_CBn_FSRRESTORE (cont.)

Bits	Name	Description
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07C00028+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_FAR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The Fault Address Register records the virtual address of client accesses that encounter exceptions within the context bank, e.g. translation faults. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

GFX3D_SMMU_GFX3D_CBn_FAR

Bits	Name	Description
31:0	VA	VA[31:0] of errant client access

0x07C0002C+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_FSYNR0, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

NOTE omission of VMID field from this register, as VMID can only be made visible to SROT, and not to general OS software that manages the context bank registers

GFX3D_SMMU_GFX3D_CBn_FSYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] (ATID field of errant request)
23:16	RESERVED	
15:13	ABID	ABID[2:0] (ABID field of errant request)
12:8	APID	APID[4:0] (APID field of errant request)
7:0	AMID	AMID[7:0] (AMID field of errant request)

0x07C00030+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_FSYNR1, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

GFX3D_SMMU_GFX3D_CBn_FSYNR1

Bits	Name	Description
31:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO (AOOO field of the errant request)
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request
15:12	ALEN	ALEN[3:0]field of the errant request
11	RESERVED_2	
10	ABURST	field of the errant request
9	RESERVED_1	
8	AWRITE	field of the errant request
7	AINST	field of the errant request
6	APROTNS	field of the errant request
5	APRIV	field of the errant request
4	AINNERSHARED	(AINNERSHARED field of the errant request)

GFX3D_SMMU_GFX3D_CBn_FSYNR1 (cont.)

Bits	Name	Description
3	ASHARED	(ASHARED field of the errant request)
2:0	AMEMTYPE	AMEMTYPE[2:0] (AMEMTYPE field of the errant request)

0x07C00034+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_PRRR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs memory type and shareability attributes of requests that are both MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1)

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) and/or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, memory type encoding is as follows:

0b00 = strongly-ordered

0b01 = device

0b10 = normal

0b11 = reserved

GFX3D_SMMU_GFX3D_CBn_PRRR

Bits	Name	Description
31	NOS7	not-outer-shareable class 7
30	NOS6	not-outer-shareable class 6
29	NOS5	not-outer-shareable class 5
28	NOS4	not-outer-shareable class 4
27	NOS3	not-outer-shareable class 3
26	NOS2	not-outer-shareable class 2
25	NOS1	not-outer-shareable class 1
24	NOS0	not-outer-shareable class 0

GFX3D_SMMU_GFX3D_CBn_PRRR (cont.)

Bits	Name	Description
23:20	RESERVED	
19	SHNMSH1	(shareable attribute for normal memory accesses with SH=1) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1
18	SHNMSH0	(shareable attribute for normal memory accesses with SH=0) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0
17	SHDSH1	SHDSH1 (shareable attribute for device accesses with SH=1) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1 [
16	SHDSH0	SHDSH0 (shareable attribute for device accesses with SH=0) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0 [
15:14	MTC7	MTC7[1:0] (memory type class 0)
13:12	MTC6	MTC6[1:0] (memory type class 0)
11:10	MTC5	MTC5[1:0] (memory type class 0)
9:8	MTC4	MTC4[1:0] (memory type class 0)
7:6	MTC3	MTC3[1:0] (memory type class 0)
5:4	MTC2	MTC2[1:0] (memory type class 0)
3:2	MTC1	MTC1[1:0] (memory type class 0)
1:0	MTC0	MTC0[1:0] (memory type class 0)

0x07C00038+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_NMRR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs the cache policy of MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1) requests for which the memory type is mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0) or the memory type is mapped to a type other than normal memory (SMMU_CBn_PRRR[MTCn] != 0b10)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, inner-cache and outer-cache policy encodings are as follows:

0b00 = non-cacheable

0b01 = cacheable, copy-back, write-allocate

0b10 = cacheable, write-through, write-no-allocate

0b11 = cacheable, copy-back, write-no-allocate

GFX3D_SMMU_GFX3D_CBn_NMRR

Bits	Name	Description
31:30	OCPC7	OCPC7[1:0] (inner-cache policy class 7)
29:28	OCPC6	OCPC6[1:0] (inner-cache policy class 6)
27:26	OCPC5	OCPC5[1:0] (inner-cache policy class 5)
25:24	OCPC4	OCPC4[1:0] (inner-cache policy class 4)
23:22	OCPC3	OCPC3[1:0] (inner-cache policy class 3)
21:20	OCPC2	OCPC2[1:0] (inner-cache policy class 2)
19:18	OCPC1	OCPC1[1:0] (inner-cache policy class 1)
17:16	OCPC0	OCPC0[1:0] (inner-cache policy class 0)
15:14	ICPC7	ICPC7[1:0] (inner-cache policy class 7)
13:12	ICPC6	ICPC6[1:0] (inner-cache policy class 6)
11:10	ICPC5	ICPC5[1:0] (inner-cache policy class 5)
9:8	ICPC4	ICPC4[1:0] (inner-cache policy class 4)
7:6	ICPC3	ICPC3[1:0] (inner-cache policy class 3)
5:4	ICPC2	ICPC2[1:0] (inner-cache policy class 2)
3:2	ICPC1	ICPC1[1:0] (inner-cache policy class 1)
1:0	ICPC0	ICPC0[1:0] (inner-cache policy class 0)

0x07C0003C+0x1000*n GFX3D_SMMU_GFX3D_CBn_TLBLKCR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB lock control register governs the TLB locking mechanism and TLB invalidate operations.Write access to this register is governed by SMMU_CR[TLBLKCRWE]

When SMMU_CR[TLBLKCRWE] is 0, writes to SMMU_CBn_TLBLKCR are ignored

Read access is still permitted

SROT can set SMMU_CR[TLBLKCRWE] to 1 to allow operating environment(s) to manage the TLB locking mechanism

Management amongst multiple operating environments must be coordinated via semaphore

GFX3D_SMMU_GFX3D_CBn_TLBLKCR

Bits	Name	Description
31:24	RESERVED_2	
23:16	VICTIM	VICTIM[7:0] Indicates the TLB index at which the next normal (non-locking) allocation will occur Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context
15:8	FLOOR	FLOOR[7:0] Indicates the TLB index from which round-robin replacement on normal (non-locking) allocations occurs TLB entries at indices below this value are locked Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context banks
7:4	RESERVED_1	

GFX3D_SMMU_GFX3D_CBn_TLBLKCR (cont.)

Bits	Name	Description
3	TLBIVAACFG	(TLBIVAA configuration) TLBIVAACFG = 0 - flash-invalidate SMMU_CBn_TLBIVAA commands flash-invalidate the entire TLB, without regard to locking, security, address, and/or VMID value TLBIVAACFG = 1 - selective SMMU_CBn_TLBIVAA commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank VA field of TLB entry matches VA designated by SMMU_CBn_TLBIVAA command NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked
2	TLBIASIDCFG	(TLBIASID configuration) TLBIASIDCFG = 0 - flash-invalidate SMMU_CBn_TLBIASID commands flash-invalidate the entire TLB, without regard to locking, security, VMID, and/or ASID values TLBIASIDCFG = 1 - selective SMMU_CBn_TLBIASID commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command TLB entry is not global (NG field is 1) NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
1	TLBIALLCFG	(TLBIALL configuration) TLBIALLCFG = 0 - flash-invalidate SMMU_CBn_TLBIALL commands flash-invalidate the entire TLB, without regard to locking, security, and/or VMID value TLBIALLCFG = 1 - selective SMMU_CBn_TLBIALL commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked

GFX3D_SMMU_GFX3D_CBn_TLBLKCR (cont.)

Bits	Name	Description
0	LKE	(lock enable) Governs whether or not TLB entries established by VA-to-PA commands upon TLB misses are locked LKE = 0 (normal, non-locking) Allocate VA-to-PA TLB entry (if TLB miss) at the index specified by SMMU_CBn_TLBLKCR[VICTIM] Allocation is disabled if SMMU_CBn_ACTLR[DNLV2PA] is 1 Increment SMMU_CBn_TLBLKCR[VICTIM] by 1 (only if new entry allocated) Wrap back to the value of SMMU_CBn_TLBLKCR[FLOOR] when the last entry is written LKE = 1 (locking) Search TLB for specified VA and invalidate if found Provides atomicity between the invalidate and the new allocation within the locked region Allocate VA-to-PA TLB entry at the index specified by data operand bits 7:0 of the VA-to-PA command This value must be less than SMMU_CBn_TLBLKCR[FLOOR] in order for it to remain locked Allocation occurs even if non-locking allocation is disabled due to SMMU_CBn_ACTLR[DNLV2PA] = 1

0x07C00040+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_V2PSR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The VA-to-PA status register records the hit/miss status and TLB index or V2Pxx and TLB invalidate commands.

GFX3D_SMMU_GFX3D_CBn_V2PSR

Bits	Name	Description
31:16	RESERVED_2	
15:8	INDEX	INDEX[7:0] Indicates the index of the TLB entry associated with the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command If SMMU_CBn_V2PSR[HIT] is 0, then SMMU_CBn_V2PSR[INDEX] is the index to which the entry was allocated (if allocated at all) If SMMU_CBn_V2PSR[HIT] is 1, then SMMU_CBn_V2PSR[INDEX] is the index of the entry which hit
7:1	RESERVED_1	

GFX3D_SMMU_GFX3D_CBn_V2PSR (cont.)

Bits	Name	Description
0	HIT	Indicates whether or not there was a TLB hit (prior to allocation, if any) on the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command

0x07C00044+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_TLBFLPTER, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB first level PTE register holds the first level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

This register (together with SMMU_CBn_TLBSLPTER) is used as the source of the translation information for VA-to-PA operations when the MMU is enabled (SMMU_CBn_SCTLR[M] = 1) and the operations are configured for software table update (SMMU_CBn_ACTLR[V2PCFG] = 0b01)

Field definitions vary according to the type of PTE (fault, page, section, or supersection), and come directly from the ARMv7 architecture's PTE formats

GFX3D_SMMU_GFX3D_CBn_TLBFLPTER

Bits	Name	Description
31:10	FL_PTE_HI	
9:5	RESERVED	
4:2	FL_PTE_LO	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	This field should be set to 0b00 or 0b11 to indicate that the translation should result in a context fault, and the rest of the fields are defined as indicated in this section If this field is not 0b00 or 0b11, then the PTE is of some other type (see other sections for the field definitions for those types)

0x07C00048+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_TLBSLPTER, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB second level PTE register holds the second level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

Field definitions vary according to the type of PTE (fault, 64KB or 4KB), and come directly from the ARMv7 architecture's PTE format

GFX3D_SMMU_GFX3D_CBn_TLBSLPTER

Bits	Name	Description
31:2	SL_PTE	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	0x0: fault

0x07C0004C+0x1000*n GFX3D_SMMU_GFX3D_CBn_BFBCR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The burst fetch buffer configuration register governs the operation of the "burst fill" feature of the SMMU.

GFX3D_SMMU_GFX3D_CBn_BFBCR

Bits	Name	Description
31:12	STRIDE	(stride amount) 4KB-aligned value to be added to virtual address on demand TLB miss for filling subsequent BFB Stride of minimum 4KB alignment useful for preventing stride burst fetch until final PTE of the demand BFB entry is used
11:8	SLVIC	(second-level victim) Indicates the SLBFB index at which the next round-robin allocation will occur
7:4	FLVIC	(first-level victim) Indicates the FLBFB index at which the next round-robin allocation will occur
3	RESERVED	
2	SFVS	(stride-fetch victim selection) SFVS. = 0 (replace normal round-robin victim-selected entry) Useful when stride is larger than the VA space represented by the four PTEs in the demand BFB entry, but the client access pattern is for more than just the initial PTE in that demand BFB entry SFVS. = 1 (replace same BFB used by demand VA for which the stride burst is being performed) Useful when stride is the same as the VA space represented by an individual PTE in the demand BFB entry (such that the stride won't miss against the BFB until the last PTE of the demand BFB entry is accessed), and/or when the client access pattern only uses the initial PTE in the demand BFB entry

GFX3D_SMMU_GFX3D_CBn_BFBCR (cont.)

Bits	Name	Description
1	BFBSFE	(burst fetch buffer stride fetch enable) Enables stride burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Stride burst fetch is for the block of four PTEs associated with VA+stride VA is the "demanded" VA from the client (or VA-to-PA command) Stride value is specified by SMMU_CBn_BFBCR[STRIDE] Stride burst fetch only occurs if demand access for VA misses in TLB (could hit in BFB) and address VA+stride misses in both TLB and BFB
0	BFBDFE	(burst fetch buffer demand fetch enable) Enables demand burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Demand burst fetch is for the block of four PTEs associated with the "demanded" VA from the client (or VA-to-PA command) Demand burst fetch only occurs if demand access misses in both TLB and BFB

0x07C00800+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_TLBIALL, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate all command register invalidates all TLB entries matching the VMID associated with this context bank. Data operand is ignored.

GFX3D_SMMU_GFX3D_CBn_TLBIALL

Bits	Name	Description
31:0	RESERVED	

0x07C00804+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_TLBIASID, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by ASID command register invalidates TLB entries matching the specified ASID and matching the VMID associated with this context bank.Invalidates TLB entries which are associated with the designated ASID and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIASIDCFG] governs whether command flash-invalidates entire TLB array or just the entries matching the VMID, ASID, and security state

TLBIASIDCFG = 0 - flash-invalidate

SMMU_CBn_TLBIASID command flash-invalidates the entire TLB, without regard to locking, security, VMID, and/or ASID values

TLBIASIDCFG = 1 - selective

SMMU_CBn_TLBIASID command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command data operand

TLB entry is not global (NG field is 1)

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command

Locking is not considered (matching entries are invalidated even if locked)

ASID field of command specifies the ASID value of the TLB entries to be invalidated

GFX3D_SMMU_GFX3D_CBn_TLBIASID

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Actual ASID value

0x07C00808+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_TLBIVA, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA command invalidates TLB entries matching the designated VA, ASID and the VMID associated with this context bank.

Matching entry determined as follows:

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIVA command data operand (or TLB entry is global - NG field is 0)

VA field of TLB entry matches VA value designated by the SMMU_CBn_TLBIVA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIVA command

Locking is not considered (matching entry is invalidated even if locked)

Data operand specifies the VA and ASID value of the TLB entry to be invalidated

GFX3D_SMMU_GFX3D_CBn_TLBIVA

Bits	Name	Description
31:12	VA	VA[31:12]
11:8	RESERVED	
7:0	ASID	ASID[7:0] value

0x07C0080C+0x1000*n GFX3D_SMMU_GFX3D_CBn_TLBIVAA, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA all ASIDS command invalidates TLB entries matching the designated VA and the VMID associated with this context bank, regardless of ASID.Invalidates TLB entries which are associated with the designated VA, regardless of ASID, and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIVAACFG] governs whether command flash-invalidates entire TLB array or just the non-locked entries matching the VMID, ASID, and security state

TLBIVAACFG = 0 - flash-invalidate

SMMU_CBn_TLBIVAA command flash-invalidates the entire TLB, without regard to locking, security, address, and/or VMID value

TLBIVAACFG = 1 - selective

SMMU_CBn_TLBIVAA command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

VA field of TLB entry matches VA designated by the SMMU_CBn_TLBIVAA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command

Entry is unlocked

GFX3D_SMMU_GFX3D_CBn_TLBIVAA

Bits	Name	Description
31:12	VA	VA[31:12]
11:0	RESERVED	

0x07C00810+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_V2PRR, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

GFX3D_SMMU_GFX3D_CBn_V2PRR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07C00814+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_V2PPW, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

GFX3D_SMMU_GFX3D_CBn_V2PPW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07C00818+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_V2PUR, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

GFX3D_SMMU_GFX3D_CBn_V2PUR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07C0081C+0x1000*n GFX3D_SMMU_GFX3D_CBn_V2PUW, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

.Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

GFX3D_SMMU_GFX3D_CBn_V2PUW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07C00820+ 0x1000*n GFX3D_SMMU_GFX3D_CBn_RESUME, n=[0..2]

Type: Write/command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB resume command causes the SMMU to resume operation after a stalled access..

GFX3D_SMMU_GFX3D_CBn_RESUME

Bits	Name	Description
31:1	RESERVED	

GFX3D_SMMU_GFX3D_CBn_RESUME (cont.)

Bits	Name	Description
0	TNR	Terminate/not retry When TNR is written as 0, indicates that the stalled access should be retried by the system MMU. When written as 1, indicates that this stalled transaction is terminated by the system MMU. The error is optionally reported to the requesting master, using the client port bus protocol, if SMMU_CNn_ACTLR[CFERE] == 1. Interrupt optionally remains asserted via SMMU_M2VCBRn[IRPTINDX] selected SMMU_contextFaultIrptReq bit, only if SMMU_CBn_ACTLR[CFEIE] is 1, and only if SMMU_CBn_FSR has not been cleared by software priori to issuing this command..

14.31 3D Graphics 1 SMMU Registers (0x07D00000 SMMU_GFX3D1_BASE)

This section contains 3D Graphics 1 SMMU registers.

14.31.1 SMMU Global Registers

14.31.1.1 SMMU VMID/CBNDX mapping registers

0x07DFF000+0x4*n GFX3D1_SMMU_GFX3D1_M2VCBRn, n=[0..31]

Type: Read/Write
Clock: AXI_CLK
Reset State: Undefined

SMMU_M2VCBRm registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

GFX3D1_SMMU_GFX3D1_M2VCBRn

Bits	Name	Description
31:28	RESERVED_2	
27:25	BPMEMTYPE	(bypass memory type) Supplies the AMEMTYPE attributes for client requests which bypass the System MMU when SMMU_M2VCBRn[BPMTCFG] = 1 See reference section for AMEMTYPE encoding definitions
24	BPMTCFG	(bypass memory type configuration) Governs the memory type (AMEMTYPE) attributes of client requests which bypass the System MMU BPMTCFG = 0 - use AMEMTYPE Bypass requests use AMEMTYPE signal supplied by client master BPMTCFG = 1 - use SMMU_M2VCBRn[BPMEMTYPE] Bypass requests use SMMU_M2VCBRn[BPMEMTYPE] Reset state : 0
23:22	NSCFG	(non-secure configuration) Governs the incoming security designation of client requests NSCFG = 0b00 - use APROTNS Use APROTNS signal supplied by client master NSCFG = 0b01 - reserved NSCFG = 0b10 - secure System MMU ignores APROTNS; treats all requests as secure NSCFG = 0b11 - non-secure System MMU ignores APROTNS; treats all requests as non-secure Reset state : 0

GFX3D1_SMMU_GFX3D1_M2VCBRn (cont.)

Bits	Name	Description
21:20	BPSHCFG	(bypass shareability configuration) Governs the shareability realm (ASHARED and AINNERSHARED) attributes of client requests which bypass the System MMU BPSHCFG = 0b00 - use ASHARED and AINNERSHARED Bypass requests use ASHARED and AINNERSHARED signals supplied by client master BPSHCFG = 0b01 - outer-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 0 BPSHCFG = 0b10 - inner-shareable Bypass requests set ASHARED = 1, AINNERSHARED = 1 BPSHCFG = 0b11 - non-shareable Bypass requests set ASHARED = 0, AINNERSHARED = 0 Reset state : 0
19	BPRCNSH	(bypass redirect cacheable-non-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache Reset state : 0
18	BPRCISH	(bypass redirect cacheable-inner-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0
17	BPRCOSH	(bypass redirect cacheable-outer-shareable) Governs whether or not client accesses that bypass the System MMU and which are cacheable and outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache Reset state : 0

GFX3D1_SMMU_GFX3D1_M2VCBRn (cont.)

Bits	Name	Description
16	BYPASSD	Bypass disable for this index Governs whether or not client port accesses using this mapping table entry are actually permitted to "bypass" the System MMU when such bypass is indicated (either due to CBNDX = 255 or due to the master asserting the "SMMU bypass" input) This field is ignored (and operates as if it were 0) if SMMU_CR[CLIENTPD] is 1 BYPASSD = 0 - bypass enabled Bypass requests truly bypass the System MMU and "pass-through" to the fabric (no translation, access control, or attribute generation) No cycle of latency for System MMU context bank access Bypass request not considered an error Bypass request error not recorded in SMMU_ESR[BYPASS] Bypass error not reported to requesting master SMMU_rpuErrIrptReq interrupt output not asserted Client accesses still reference M2VCBMT to get VMID value for presentation to fabric BYPASSD = 1 - bypass disabled System MMU terminates the access as RAZ/WI Bypass request is considered an error Bypass request error is recorded in SMMU_ESR[BYPASS] If SMMU_CR[RPUERE] is 1, then bypass error reported to requesting master according to the client port bus protocol If SMMU_CR[RPUEIE] is 1, then SMMU_rpuErrIrptReq interrupt output asserted
15:8	CBNDX	Context bank index Context bank index associated with the M2VCBMT index CBNDX = 255 indicates no context bank assigned ("bypass")
7:5	RESERVED_1	
4:0	VMID	Virtual machine ID VMID value associated with the M2VCBMT index Must be programmed consistently with the SMMU_CBACRn[CBVMID] field for the context bank designated by SMMU_M2VCBRm[CBNDX]

14.31.1.2 SMMU context bank access control registers

0x07DFF800+0x4*n GFX3D1_SMMU_GFX3D1_CBACRn, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs configuration port access to the associated context bank registers.

GFX3D1_SMMU_GFX3D1_CBACRn

Bits	Name	Description
31:24	IRPTNDX	(interrupt index) Interrupt output number used for context faults associated with this context bank (use SMMU_contextFaultIrptReq[IRPTNDX])
23:21	RESERVED	
20:16	CBVMID	(context bank VMID) Specifies the VMID with which the client masters using the context bank are associated Must be programmed consistently with the M2VCBMT entries that are configured to use the associated context bank This field is used by configuration port commands that need the context bank's VMID value in order to access the TLB (e.g., SMMU_CBn_TLBIVMID, SMMU_CBn_V2Pxx)
15:10	RESERVED_2	
9	RWGE	Read/write global enable. Setting this bit allows access to the context bank registers from any VMID
8	RWE	Read/write enable. Indicates that the RWVMID field is valid.
7:5	RESERVED_1	
4:0	RWVMID	Specifies owner VMID with full read/write access to the registers in the associated context bank "n".

14.31.1.3 SMMU TLB software access registers

0x07DFFE00 GFX3D1_SMMU_GFX3D1_TLBRSW

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Writing to this address requests that the TLB entry at INDEX be read into the SMMU_TLBTRn registers

GFX3D1_SMMU_GFX3D1_TLBRSW

Bits	Name	Description
31:10	RESERVED	

GFX3D1_SMMU_GFX3D1_TLBRSW (cont.)

Bits	Name	Description
9:8	TLBBFBS	This field selects the TLB, TFBFB, SLBFB 0x0: Selecting TLB 0x1: Not defined 0x2: Selecting FL BFB 0x3: Selecting SL BFB
7:0	INDEX	TLB index to be read.

0x07DFFE80 GFX3D1_SMMU_GFX3D1_TLBTR0

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

This register holds part of TLB entry read by the last TLBRSW command.

GFX3D1_SMMU_GFX3D1_TLBTR0

Bits	Name	Description
31:23	RESERVED_4	
22:20	DPSIZC	3 bit decode page size field from CAM-side of TLB CAM-RAM) Same determination and encoding as for DPSIZR The CAM-side copy of this field is used for hit/miss determination in the TLB CAM array
19	RESERVED_3	
18:16	DPSIZR	(3 bit decode page size field from RAM-side of TLB CAM-RAM) Determined from the size fields of the page table entry Encodes the page size as follows: all other values reserved/unused The RAM-side copy of this field is used for virtual ’ physical address formation 0x0: 4KB page 0x1: 64KB page 0x3: 1MB page 0x7: 16MB page
15:12	RESERVED_2	
11	MT2	(memory type bit 2) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[2] attribute bus on the request output of the System MMU

GFX3D1_SMMU_GFX3D1_TLBTR0 (cont.)

Bits	Name	Description
10	MT1	(memory type bit 1) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[1] attribute bus on the request output of the System MMU
9	MT0	(memory type bit 0) Determined from SMMU_CBn_PRRR, SMMU_CBn_NMRR, SMMU_CBn_SCTLR[TRE], and the TEX[0], C and B fields of the page table entry Indicates the memory type and cache policy of the page This field becomes the AMEMTYPE[0] attribute bus on the request output of the System MMU
8	SH	(shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's outer-shareable realm This field becomes the ASHARED attribute on the request output of the System MMU
7	ISH	(inner-shareable) Determined from SMMU_CBn_PRRR, together with SMMU_CBn_SCTLR[TRE] and the TEX[0], C, B, and SH fields of the page table entry Indicates whether or not hardware must enforce cache coherency for the page, with respect to agents that are members of the requesting master's inner-shareable realm This field becomes the AINNERSHARED attribute on the request output of the System MMU
6	NSDESC	(non-secure descriptor) This TLB entry field is a modified version of the corresponding bit of the page table entry Qualified by the NS-prot attribute of the incoming request which prompted the allocation of the TLB entry, such that if the incoming NS-prot attribute was 1 (non-secure), then the NS-desc field of the page table entry was ignored, and the NS-desc field of the TLB entry was forced to 1 Indicates whether the associated memory page contains secure (NS-desc=0) or non-secure (NS-desc=1) information This field becomes the NS-prot attribute on the request output of the System MMU
5	RESERVED_1	

GFX3D1_SMMU_GFX3D1_TLBTR0 (cont.)

Bits	Name	Description
4	XN	(execute never permission) This TLB entry field comes directly from the corresponding bit of the page table entry
3	UW	(user write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
2	UR	(user read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
1	PW	(privileged write permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]
0	PR	(privileged read permission) Determined from AP[2:0] fields of page table entry, together with SMMU_CBn_SCTLR[AFE]

0x07DFFE84 GFX3D1_SMMU_GFX3D1_TLBTR1

Type: Read /Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

GFX3D1_SMMU_GFX3D1_TLBTR1

Bits	Name	Description
31:12	PA	Physical address [31:12] field of the TLB entry
11:5	RESERVED	
4:0	VMID	VMID [4:0]field of the TLB entry)

0x07DFFE88 GFX3D1_SMMU_GFX3D1_TLBTR2

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

These registers hold the result of a TLBRSW command.

GFX3D1_SMMU_GFX3D1_TLBTR2

Bits	Name	Description
31:12	VA	virtual address field [31:12] of the TLB entry
11	RESERVED	
10	NG	(not global field from page table entry) Indicates whether the page is private to the specified ASID (NG=1) or global to all ASIDs within the VMID using this context bank (NG=0)
9	NSTID	(non-secure tag ID field of the TLB entry) Indicates whether the TLB entry belongs to the secure world (NSTID=0) or the non-secure world (NSTID=1) This field is comned against the incoming NS-prot attribute of the master request as part of TLB hit/miss determination
8	V	valid field of the TLB entry
7:0	ASID	ASID[7:0] field of the TLB entry

0x07DFFE8C GFX3D1_SMMU_GFX3D1_TESTBUSCR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

Governs which signals (if any) from the system SMMU core or wrapper design hierarchy are sent out to the system via a testbus for diagnostic, and also to the system profiling and diagnostic monitor(SPDM).

GFX3D1_SMMU_GFX3D1_TESTBUSCR

Bits	Name	Description
31:28	SPDM3SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[3]
27:24	SPDM2SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[2]
23:20	SPDM1SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[1]
19:16	SPDM0SEL	It selects one of 16 signals to be sent to SPDM on spdmbus[0]
15:14	TBHSEL	Testbus highselect It governs which set of signals are to testbus[31:16] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL

GFX3D1_SMMU_GFX3D1_TESTBUSCR (cont.)

Bits	Name	Description
13:12	TBSLSEL	Testbus low select It governs which set of signals are to testbus[15:0] TBSLSEL = 0b00 - Bits 15:0 from nuleus bus TBSLSEL = 0b01 - Bits 31:16 from nuleus bus TBSLSEL = 0b10 - Bits 15:0 from wrapper group selected by SMMU_TESTBUSCR[WGSEL] TBSLSEL = 0b11 - Bits 31:16 from wrapper group selected by SMMU_TESTBUSCR[WGSEL
11:10	RESERVED_2	
9:8	WGSEL	Wrapper group select It selects a particular group of signals from the SMMU wrapper hierarchy WGSEL = 0b00 - wrapper signal group 0 WGSEL = 0b01 - wrapper signal group 1 WGSEL = 0b10 - wrapper signal group 2 WGSEL = 0b11 - reserved
7:2	RESERVED_1	
1	SPDMBE	SPDM test enable Reset state : 0
0	TBE	Testbus enable, which governs whether the testbus is driven with all 0s or with the configured signals Reset state : 0

0x07DFFEFC GFX3D1_SMMU_GFX3D1_VR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: 32'h0000_0000

Note that the DCPBP/DCPPP bits prevent the pipelining of the next transaction when the current transaction is a bypass/pass-through transaction. That is, they add one more cycle of delay between the current and next transactions.

Also note that when we are in global bypass (SMMU_CR[CLIENTPD]=1), these bits should have NO effect, or at least no effect between client transactions, they can have an effect between config and client transactions is appropriate. We must be able to continue to perform fully pipelined transactions when the client port is disabled altogether.

GFX3D1_SMMU_GFX3D1_VR0

Bits	Name	Description
31:3	RESERVED	

GFX3D1_SMMU_GFX3D1_VR0 (cont.)

Bits	Name	Description
2	DCPPT	Disable client pipelining for client operations in pass-through mode Reset state : 0
1	DCPBP	Disable client pipelining for client operations in bypass mode Reset state : 0
0	DCP	Disable client pipelining Reset state : 0

0x07DFFF00 GFX3D1_SMMU_GFX3D1_TLBIALL

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries.

GFX3D1_SMMU_GFX3D1_TLBIALL

Bits	Name	Description
31:0	EXEC	Writing any value to this register invalidates all TLB entries, as specified by the contents of SMMU_CR[TLBIALLCFG]

0x07DFFF04 GFX3D1_SMMU_GFX3D1_TLBIVMID

Type: Write/Command
Clock: AXI_BUS_CLOCK
Reset State: undefined

Invalidates all TLB entries matching the IVMID value. Precise function is governed by SMMU_CR[TLBIALLCFG].

GFX3D1_SMMU_GFX3D1_TLBIVMID

Bits	Name	Description
31:5	RESERVED	
4:0	IVMID	Designates VMID[4:0] value of entries to be invalidated.

14.31.1.4 SMMU configuration registers

0x07DFFF80 GFX3D1_SMMU_GFX3D1_CR

Type: Read/Write
Clock: AXI_BUS_CLOCK

Global configuration register.

GFX3D1_SMMU_GFX3D1_CR

Bits	Name	Description
31:10	RESERVED_2	
9	RESERVED_1	Reset state : 0
8	TLBIVMIDCFG	TLBIVMID configuration control. When set to 0,flash-invalidate, SMMU_TLBIVMID commands flash-invalidate the entire TLB, without regard to locking ,security and VMID value. When set to 1, selective, SMMU_TLBIVMID invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and VMID field matching the VMID specified by SMMU_TLBIVMID command. Reset state : X
7	TLBIALLCFG	TLBIALL configuration control. When set to 0, flash-invalidate, SMMU_TLBIALL commands flash-invalidate the entire TLB, without regard to locking and/or security. When set to 1, selective, SMMU_TLBIALL invalidates only entries that have NSTID field matching HPROTNS of SMMU_TLBIALL command, and are unlocked. Reset state : X
6	TLBLKCRWE	TLBLKCR write enable. When set to 0, writes to SMMU_CBn_TLBLKCR are ignored. When set to 1, allows operating environments to manage the TLB locking mechanism directly. Management amounst multiple operating environments must be coordinated externally between themselves. Reset state : X
5	STALLD	Global disable for stall mode. When set to 1, context bank stall modes are ignored and operate as terminate mode. Reset state : X
4	CLIENTPD	Client port disable. When set, all client accesses are forced to bypass the system MMU. There is no translation. access control, or attribute generation. This bit overrides individual SMMU_M2VCBRn[BYPASSD] settings; client requests are bypassed, even if SMMU_M2VCBRn[BYPASSD] is set to 1. Bypass request errors are not recorded in SMMU_ESR, nor reported to requesting masters. The SMMU_rpuErrIrptReq interrupt output signal is not asserted. Reset state : 1

GFX3D1_SMMU_GFX3D1_CR (cont.)

Bits	Name	Description
3	DCDEE	When set to 0, configuration port decode errors do not set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn are not updated. When set to 1, configuration port decode errors set SMMU_ESR[CFG], SMMU_EAR and SMMU_ESYNRn updated with address and syndrome of error. Reset state : X
2	RPUEIE	When set, configuration port errors and client port bypass errors are reported directly to the interrupt controller via the SMMU_rputErrIrptReq interrupt output signal. Interrupt output is asserted if SMMU_CR[RPUIE_EN] is 1 and ANY bit is set in SMMU_ESR register. Reset state : 0
1	RPUERE	When set, SMMU reports configuration port errors and client port bypass errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via AXI port will use decode error, rather than slave error. Regardless of the value of this field both configuration port errors and client port bypass request errors are terminated by the SMMU as RAZ/WI, and are recorded in SMMU_ESR register. Reset state : X
0	RPUE	When set, all configuration port accesses are checked against SMMUX_RPU_ACR and/or the SMMUX_CBACRn registers for access permissions. Reset state : 0

14.31.1.5 SMMU error report registers

0x07DFFF84 GFX3D1_SMMU_GFX3D1_EAR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: unknown

When there is an error, holds the physical address of the errant transaction.

GFX3D1_SMMU_GFX3D1_EAR

Bits	Name	Description
31:0	PA	Physical address[31:0]

0x07DFFF88 GFX3D1_SMMU_GFX3D1_ESR

Type: Read/Write to clear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This register has read/write clear access. Reads return the value in the register, a write with a 1 set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

GFX3D1_SMMU_GFX3D1_ESR

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x07DFFF8C GFX3D1_SMMU_GFX3D1_ESRRESTORE

Type: Write
Clock: RPM_BUS_CLK
Reset State: Undefined

This register is an aliased address for SMMU_ESR, but it allows direct write access. In this way, diagnostic software can cause an error to be generated and reported.

GFX3D1_SMMU_GFX3D1_ESRRESTORE

Bits	Name	Description
31	MULTI	When set to 1, indicates that an additional error occurred while SMMU_ESR was non-zero. The SMMU_EAR ,SMMU_ESYNRn and SMMU_ESR registers (with the exception of this bit) lock upon the first error, and must be cleared to unlock.
30:2	RESERVED	

GFX3D1_SMMU_GFX3D1_ESRRESTORE (cont.)

Bits	Name	Description
1	BYPASS	When set, indicates an error due to a client port bypass request (CBNDX = 255 or "SMMU_Bypass" input asserted. This is only considered an error when SMMU_CR[CLIENTPD] == 0 and SMMU_M2VCBRn[BYPASSD] == 1. Bypass request errors are the only client port errors that are recorded in SMMU_ESR. All other faults associated with client port accesses using a particular M2VCBMT entry and associated context bank are recorded within that context bank's SMMU_CBn_FSR and reported directly to that context's managing processor, using the bit of SMMU_contextFaultIrptReq interrupt output bus selected by SMMU_M2VCBRn[IRPTNDX].
0	CFG	When set, indicates an error associated with a configuration port request.

0x07DFFF90 GFX3D1_SMMU_GFX3D1_ESYNR0

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

GFX3D1_SMMU_GFX3D1_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request
15:0	AMID	AMID[15:0] field of errant request

0x07DFFF94 GFX3D1_SMMU_GFX3D1_ESYNR1

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

GFX3D1_SMMU_GFX3D1_ESYNR1

Bits	Name	Description
31	DCD	(decode) Indicates configuration port error due to invalid/unrecognized address (e.g., a reserved register address) Includes decode errors within both the global address space and the individual context bank address space

GFX3D1_SMMU_GFX3D1_ESYNR1 (cont.)

Bits	Name	Description
30	AC	(access control) Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO field of the errant request
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request)
15:12	ALEN	ALEN[3:0] field of the errant request
11	RESERVED_2	
10	ABURST	ABURST[1:0] field of the errant request
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request
7	AINST	AINST field of the errant request
6	APROTNS	APROTNS field of the errant request
5	APRIV	APRIV field of the errant request
4	AINNERSHARED	AINNERSHARED field of the errant request
3	ASHARED	ASHARED field of the errant request
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

14.31.1.6 SMMU revision register

0x07DFFFF4 GFX3D1_SMMU_GFX3D1_REV

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the revision information for the SMMU core and wrapper.

GFX3D1_SMMU_GFX3D1_REV

Bits	Name	Description
31:12	RESERVED	
11:8	WRAPPER	Wrapper version
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

14.31.1.7 SMMU implementation parameter register

0x07DFFFF8 GFX3D1_SMMU_GFX3D1_IDR

Type: Read
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Reports the parameter information for the SMMU core and wrapper

GFX3D1_SMMU_GFX3D1_IDR

Bits	Name	Description
31:24	NIRPT	NIRPT[7:0] Indicates number of context fault interrupt outputs (minus 1) supported by the System MMU Value can range from 0 - 255 (1 - 256 context fault interrupt outputs)
23:16	NCB	NCB[7:0] Indicates number of context banks (minus 1) supported by the System MMU Value can range from 0 - 254 (1 - 255 context banks)
15:12	TLBSIZE	TLBSIZE[3:0] Indicates log2(number of TLB entries) That is, number of TLB entries = 2 ** TLBSIZE
11	RESERVED	
10	HUM	Indicates whether or not TLB hit-under-miss behavior is supported
9	HTW	Indicates whether or not the System MMU supports hardware table walk If hardware table walk not supported (HTW=0), then software cannot set SMMU_CBn_ACTLR[TLBMCFG] to 0b10

GFX3D1_SMMU_GFX3D1_IDR (cont.)

Bits	Name	Description
8:0	NM2VCBMT	NM2VCBMT[8:0] Indicates number of M2VCBMT entries, with a maximum of 512 The bit width of the M2VCBMTIindex input (maximum value is 9) is equal to log base 2 of NM2VCBMT Allows for up to 7-bit MID field, plus NS-prot or other fields to select mapping [

0x07DFFFFC GFX3D1_SMMU_GFX3D1_RPU_ACR

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Using the incoming HVMID, this register controls access to the global register space.

GFX3D1_SMMU_GFX3D1_RPU_ACR

Bits	Name	Description
31:0	RWE	Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the entire block of registers within the SMMU's 4KB global address space, including this register itself. A VMID identified by this register is also permitted global access to all context banks. In practice, this register designates the VMID(s) that can act as SROT.

14.31.2 SMMU Context Bank Registers

There are a configurable number (1 to 9) of context banks in the SMMU. Each context bank consists of a set of registers in a unique 4KB address space.

14.31.2.1 SMMU context bank control registers

0x07D00000+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_SCTLR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank System Control Register controls various architected SMMU features

GFX3D1_SMMU_GFX3D1_CBn_SCTLR

Bits	Name	Description
31:5	RESERVED_2	
4	BE	Governs the order byte order or "endianness" of the page table entries. When set to 0, page table entries are in little endian format, so that their least significant byte is in byte 0 of the 32 bit entry. When set to 1, page table entries are in big endian format, so that their most significant byte is in byte 0 of the 32 bit entry.
3	RESERVED_1	Reserved for HAF, Hardware access flag. This bit governs whether the access flag is managed by hardware or software. The SMMU supports software access flag management only, so this bit is read-only and internally driven to 0.
2	AFE	Access flag enable. When AFE = 0, the access flag field is not supported and the AP[0] page table entry field acts as a bit of the overall AP[2:0] field to determining access permissions. When AFE = 1, the AP[0] page table entry field becomes the access flag, and the reduced number of access permission combinations is specified by AP2:1], and SMMU hardware will signal an Access Flag fault if a request targets a page for which the access flag is 0.
1	TRE	TEX remap enable. This bit governs the mapping of the page table entry TEX[2:0],C,B and SH fields into an SMMU TLB entry, and thus the translation of the AMEMTYPE[2:0], ASHARED and AINNERSHARED bus attributes. When TRE = 0, the TLB value is determined directly from the page table entry fields.
0	M	MMU enable bit. When set to 1, this context bank is enabled for translating requests. When set to 0, accesses bypass the TLB, and there is no address translation, access permission checking or attribute mapping. Incoming master requests are passed through unchanged.

0x07D00004+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_ACTLR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context bank auxiliary control register controls various implementation specific features.

GFX3D1_SMMU_GFX3D1_CBn_ACTLR

Bits	Name	Description
31:19	RESERVED	
18	RESERVED_2	

GFX3D1_SMMU_GFX3D1_CBn_ACTLR (cont.)

Bits	Name	Description
17:16	V2PCFG	VA-to-PA configuration. Governs operation of VA-to-PA commands that miss in the TLB 0x0: terminate (Record TLB Miss context fault in SMMU_CBn_PAR) 0x1: software table update (Translate based on values in SMMU_CBn_TLBFLPTER and SMMU_CBn_TLBSLPTER) 0x2: hardware table walk (Translate based on value of PTE read from page table in memory) 0x3: reserved
15	TIPCF	Governs whether or not all subsequent requests using this context bank should be terminated if a prior context fault has occurred and has not yet been cleared from SMMU_CBn_FSR Accesses to other context banks proceed as normal 0x0: do not terminate (System MMU will attempt to process subsequent requests despite the presence of an existing context fault in SMMU_CBn_FSR. SMMU_CBn_FSR will be set if the subsequent access also encounters a context fault) 0x1: terminate (All subsequent accesses terminated by the System MMU as RAZ/WI, even if SMMU_CBn_ACTLR[TLBMCFG, CFCFG] configured for stall mode. SMMU_CBn_FSR set when access is terminated due to TIPCF = 1. Presence of SMMU_CBn_FSR when SMMU_CBn_ACTLR is 1 implies that the later exceptions must have been simply the forced terminations due to the prior context fault. Error optionally reported to the requesting master, according to the client port bus protocol, f SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus if SMMU_CBn_ACTLR is 1.)

GFX3D1_SMMU_GFX3D1_CBn_ACTLR (cont.)

Bits	Name	Description
14	CFCFG	(context fault configuration) Governs the behavior of all context faults except TLB miss TLB miss context faults are governed by SMMU_CBn_ACTLR[TLBMCFG] 0x0: terminate (Access terminates at the System MMU as RAZ/WI. Context fault exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x1: stall (Requesting master's access stalled while System MMU waits for managing processor to resolve context fault. Context fault exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode)

GFX3D1_SMMU_GFX3D1_CBn_ACTLR (cont.)

Bits	Name	Description
13:12	TLBMCFG	(TLB miss configuration) Governs the behavior of client accesses that miss in the TLB 0x0: pass-through (Access passed through to targeted slave without translation, attribute control, or access permission checking. Effectively, behavior is as if SMMU_CBn_SCTLR = 0 i.e., MMU disabled for this context bank. TLB miss not considered a context fault. TLB miss exception not recorded in SMMU_CBn_FSR. TLB miss exception not reported to requesting master. SMMU_contextFaultIrptReq interrupt output not asserted) 0x1: terminate (Access terminates at the System MMU as RAZ/WI,TLB miss exception recorded in SMMU_CBn_FSR. Error optionally reported to the requesting master, according to the client port bus protocol, if SMMU_CBn_ACTLR is 1. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1) 0x2: stall (Requesting master's access stalled while System MMU waits for managing processor to update TLB. TLB miss exception recorded in SMMU_CBn_FSR. Error not reported to requesting master regardless of value of SMMU_CBn_ACTLR. Interrupt optionally asserted via SMMU_M2VCBRn-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus, if SMMU_CBn_ACTLR is 1. In practice, software should set SMMU_CBn_ACTLR to 1 whenever using stall mode, as the interrupt is the means of notifying the managing processor to resolve the stall and resume. To resume, the managing processor must write to SMMU_CBn_RESUME upon resolving the TLB miss, in order for System MMU to retry or terminate the stalled operation and proceed. If SMMU_CR is 1 stall mode disabled, then setting this field to 0b10 causes the System MMU to operate as if this field were 0b01, i.e., terminate mode) 0x3: HTW (Hardware table walk . Requesting master's access stalled while System MMU accesses page table. The is TLB updated and requesting master's access resumed after obtaining valid entry from page table. If translation fault, then access either terminates or stalls according to setting of SMMU_CBn_ACTLR)
11	DNLV2PA	(disable non-locking VA-to-PA allocation) Governs whether or not TLB misses due to non-locking VA-to-PA commands will allocate a new entry This field is ignored for locking VA-to-PA operations (SMMU_CBn_TLBLKCR[LKE] = 1)
10	DNA	(disable normal allocation) Governs whether or not TLB misses due to client port accesses will allocate a new entry
9:8	PRIVCFG	0x0: apriv (System MMU uses APRIV signal supplied by master as user/supervisor indicator 1 = supervisor) 0x1: reserved 0x2: User (System MMU ignores APRIV; treats all requests using this context bank as user) 0x3: Supervisor (System MMU ignores APRIV; treats all requests using this context bank as supervisor)

GFX3D1_SMMU_GFX3D1_CBn_ACTLR (cont.)

Bits	Name	Description
7:5	RESERVED_1	
4	RCNSH	(redirect cacheable-non-shareable) Governs whether or not cacheable accesses that are non-shareable are redirected to the Scorpion-MP L2 slave port, in order that they may use the Scorpion-MP L2 cache, even though the locations are not being coherently shared with Scorpion-MP
3	RCISH	(redirect cacheable-inner-shareable) Governs whether or not cacheable accesses that are inner-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
2	RCOSH	(redirect cacheable-outer-shareable) Governs whether or not cacheable accesses that are outer-shareable are redirected to the Scorpion-MP L2 slave port, in order to access the Scorpion-MP coherent L2 cache
1	CFEIE	(context fault error interrupt enable) Governs whether or not client port request context faults are reported directly to the interrupt controller via the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus Interrupt output is asserted if SMMU_CBn_ACTLR[CFEIE] is 1 and any context fault bits are set in SMMU_CBn_FSR Such interrupts would generally be directed to the interrupt controller of whichever processor is currently managing this context bank of the System MMU Reset state : 0
0	CFERE	(context fault error report enable) Governs whether or not client port request context faults that are configured for terminate mode (or that are explicitly terminated after stall mode) are reported to the requesting master, according to the client port bus protocol All error types reported via AXI port will use decode error rather than slave error All context faults are recorded in SMMU_CBn_FSR, regardless of the value of this field.

0x07D00008+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_CONTEXTIDR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The context ID register holds the ASID associated with this context bank

GFX3D1_SMMU_GFX3D1_CBn_CONTEXTIDR

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Specifies the 8 bit ASID value assigned to this context bank. The ASID can be included in the key comparison of TLB entries. .

0x07D00010+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_TTBR0, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR0 is used for low order virtual addresses, typically private pages for a given process.

GFX3D1_SMMU_GFX3D1_CBn_TTBR0

Bits	Name	Description
31:7	PA	BIts 31:7 of the physical address of the base of the page table. The actual LSB of the base address is bit 14-N, where N is set in register TTCR
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07D00014+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_TTBR1, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table base register, specifies the physical base address and attributes of this context bank's page table. TTBR1 is used for high order virtual addresses, typically global pages for a given VMID, or kernal mappings.

The context bank auxiliary control register controls various implementation specific features.

GFX3D1_SMMU_GFX3D1_CBn_TTBR1

Bits	Name	Description
31:14	PA	BIts 31:14 of the physical address of the base of the page table.
13:7	RESERVED_2	
6	IRGN0	LSB of IRGN[1:0]. See description of IRGN above
5	NOS	Not outer shareable Governs the AINNERSHARED attribute for HTW access
4:3	ORGN	ORGN[1:0] outer cache policy for HTW accesses Encoding is as for IRGN
2	RESERVED_1	
1	SH	shareable Governs the ASHARED attribute of the HTW access.
0	IRGN1	Together with IRGN0 defines the inner cache policy for the accesses to this page table. AMEMTYPE[2:0] for HTW accesses is derived from the IRGN and ORGN fields. IRGN1 IRGN0 0 0 - non-cacheable 0 1 - copy back, write allocate 1 0 - write through, write no allocate 1 1 - copy back, write no allocate

0x07D00018+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_TTBCR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Translation table control register, which specifies the size of the virtual address space that uses TTBR0.

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GFX3D1_SMMU_GFX3D1_CBn_TTBCR

Bits	Name	Description
31:6	RESERVED_2	
5	PD1	Page disable 1; if this bit is set, hardware table walks attempting to use TTBR1will result in a first level descriptor translation fault. If clear, TTBR1 contents are used.
4	PD0	Page disable 0; if this bit is set, hardware table walks attempting to use TTBR0 will result in a first level descriptor translation fault. If clear, TTBR0 contents are used.
3	RESERVED_1	
2:0	N	N[2:0] specifies the number of upper order virtual address bits which must be 0 in order for translations to use the table pointed to by TTBR0. If any of these bits are non-zero, TTBR1 is used for the lookup. If N is 0, only TTBR0 is used.

0x07D0001C+0x1000*n GFX3D1_SMMU_GFX3D1_CBn_PAR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The physical address register captures the physical address value resulting from the execution of a VA-to-PA command

Field definitions vary according to whether or not there is a context fault associated with the requested translation

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GFX3D1_SMMU_GFX3D1_CBn_PAR

Bits	Name	Description
31:12	PAR_FAULT_INFO_312	
11	RESERVED_2	
10:9	PAR_FAULT_INFO_72	
8	RESERVED_1	
7:1	PAR_FAULT_INFO_71	Encoding varies according to value in FAULT field.

GFX3D1_SMMU_GFX3D1_CBn_PAR (cont.)

Bits	Name	Description
0	FAULT	(fault status) This field will be 1 when a context fault is associated with the requested translation, and 0, when there is no context fault associated with the requested translation.

0x07D00020+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_FSR, n=[0..2]

Type: Read/WriteClear
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The Fault Status Register records status information for client accesses that encounter exceptions within the context bank, e.g. translation faults.This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data

This prevents inadvertent clearing of new faults when writing the register to clear an old fault

The presence of an asserted value on any bit in this register (except the SS bit) is what prompts the assertion (when enabled by SMMU_CBn_ACTLR[CFEIE]) of the SMMU_M2VCBRn[IRPTNDX]-selected bit of the SMMU_contextFaultIrptReq[n-1:0] interrupt output bus

Therefore, these bits must be cleared by the interrupt handler

This is contrasted with the fields in the SMMU_CBn_FSYNRn registers, which are merely the "syndrome" of the fault indicated by SMMU_CBn_FSR

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GFX3D1_SMMU_GFX3D1_CBn_FSR

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"

GFX3D1_SMMU_GFX3D1_CBn_FSR (cont.)

Bits	Name	Description
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07D00024+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_FSRRESTORE, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Allows SW to force a value into the SMMU_CBn_FSR register.

GFX3D1_SMMU_GFX3D1_CBn_FSRRESTORE

Bits	Name	Description
31	MULTI	(multiple faults) Indicates additional context fault occurred while SMMU_CBn_FSR still non-zero SMMU_CBn_FAR and SMMU_CBn_FSYNRn registers (and SMMU_CBn_FSR itself, except for the SS and MULTI bits) "lock" upon first context fault; SMMU_CBn_FSR must be cleared to unlock Status, address, and syndrome of errors that occur while SMMU_CBn_FSR is non-zero are "lost"
30	SS	(stalled status) Indicates whether or not the System MMU is currently stalled due to an exception within this context bank SMMU_CBn_FSR[SS] does not get updated by direct writes to SMMU_CBn_FSR If stalled, software must execute an SMMU_CBn_RESUME command to either retry or terminate the stalled access SMMU_CBn_FSR[SS] will be cleared as a result Reset state : 0
29:17	RESERVED	
16	SL	(second-level) Indicates whether or not the context fault is associated with the second-level page table entry
15:8	RESERVED_2	
7	MHF	(multi-hit fault) Context fault due to multi-hit in TLB (programming error or soft hardware error)
6	HTWSEEF	(hardware table walk slave error external fault) Context fault due to slave error external fault (bus slave error) reported on hardware table walk request
5	HTWDEEF	(hardware table walk decode error external fault) Context fault due to decode error external fault (bus decode error) reported on hardware table walk request
4	TLBMF	(TLB miss fault) Context fault due to TLB miss when SMMU_CBn_ACTLR[TLBMCFG] set to "terminate" or "stall" mode

GFX3D1_SMMU_GFX3D1_CBn_FSRRESTORE (cont.)

Bits	Name	Description
3	APF	(access permission fault) Context fault due to lack of access permission (read, write, execute)
2	AFF	(access flag fault) Context fault due to page table entry AF (AP[0]) field = 0 when SMMU_CBn_SCTLR[AFE, AFFD] = 0b10 AP[0] field acts as the AF field when SMMU_CBn_SCTLR[AFE] is 1, and SMMU_CBn_SCTLR[AFFD] in turn governs whether AF=0 is actually considered a fault or simply ignored
1	TF	(translation fault) Context fault due to invalid page table entry
0	RESERVED_1	Keep aligned with SMMU_CBn_PAR fields

0x07D00028+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_FAR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: undefined

The Fault Address Register records the virtual address of client accesses that encounter exceptions within the context bank, e.g. translation faults. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

GFX3D1_SMMU_GFX3D1_CBn_FAR

Bits	Name	Description
31:0	VA	VA[31:0] of errant client access

0x07D0002C+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_FSYNR0, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

NOTE omission of VMID field from this register, as VMID can only be made visible to SROT, and not to general OS software that manages the context bank registers

GFX3D1_SMMU_GFX3D1_CBn_FSYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] (ATID field of errant request)
23:16	RESERVED	
15:13	ABID	ABID[2:0] (ABID field of errant request)
12:8	APID	APID[4:0] (APID field of errant request)
7:0	AMID	AMID[7:0] (AMID field of errant request)

0x07D00030+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_FSYNR1, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Records partial syndrome of client access that encountered an exception within the context bank. This register's contents are valid only after SMMU hardware has set a bit in SMMU_CBn_FSR[5:0]

GFX3D1_SMMU_GFX3D1_CBn_FSYNR1

Bits	Name	Description
31:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	RESERVED_4	
22	AOOO	AOOO (AOOO field of the errant request)
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request)
19	RESERVED_3	
18:16	ASIZE	ASIZE[2:0] field of the errant request
15:12	ALEN	ALEN[3:0]field of the errant request
11	RESERVED_2	
10	ABURST	field of the errant request
9	RESERVED_1	
8	AWRITE	field of the errant request
7	AINST	field of the errant request
6	APROTNS	field of the errant request
5	APRIV	field of the errant request
4	AINNERSHARED	(AINNERSHARED field of the errant request)

GFX3D1_SMMU_GFX3D1_CBn_FSYNR1 (cont.)

Bits	Name	Description
3	ASHARED	(ASHARED field of the errant request)
2:0	AMEMTYPE	AMEMTYPE[2:0] (AMEMTYPE field of the errant request)

0x07D00034+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_PRRR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs memory type and shareability attributes of requests that are both MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1)

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) and/or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, memory type encoding is as follows:

0b00 = strongly-ordered

0b01 = device

0b10 = normal

0b11 = reserved

GFX3D1_SMMU_GFX3D1_CBn_PRRR

Bits	Name	Description
31	NOS7	not-outer-shareable class 7
30	NOS6	not-outer-shareable class 6
29	NOS5	not-outer-shareable class 5
28	NOS4	not-outer-shareable class 4
27	NOS3	not-outer-shareable class 3
26	NOS2	not-outer-shareable class 2
25	NOS1	not-outer-shareable class 1
24	NOS0	not-outer-shareable class 0

GFX3D1_SMMU_GFX3D1_CBn_PRRR (cont.)

Bits	Name	Description
23:20	RESERVED	
19	SHNMSH1	(shareable attribute for normal memory accesses with SH=1) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1
18	SHNMSH0	(shareable attribute for normal memory accesses with SH=0) Governs the shareable attribute for classes mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0
17	SHDSH1	SHDSH1 (shareable attribute for device accesses with SH=1) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 1 [
16	SHDSH0	SHDSH0 (shareable attribute for device accesses with SH=0) Governs the shareable attribute for classes mapped as device memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B, and for which the page table entry's SH field is 0 [
15:14	MTC7	MTC7[1:0] (memory type class 0)
13:12	MTC6	MTC6[1:0] (memory type class 0)
11:10	MTC5	MTC5[1:0] (memory type class 0)
9:8	MTC4	MTC4[1:0] (memory type class 0)
7:6	MTC3	MTC3[1:0] (memory type class 0)
5:4	MTC2	MTC2[1:0] (memory type class 0)
3:2	MTC1	MTC1[1:0] (memory type class 0)
1:0	MTC0	MTC0[1:0] (memory type class 0)

0x07D00038+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_NMRR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

Governs the cache policy of MMU-enabled (SMMU_CBn_SCTLR[M] = 1) and TEX-remap enabled (SMMU_CBn_SCTLR[TRE] = 1) requests for which the memory type is mapped as normal memory by the SMMU_CBn_PRRR field selected by TEX[0], C, B

This register is ignored when MMU is disabled (SMMU_CBn_SCTLR[M] = 0) or TEX-remap is disabled (SMMU_CBn_SCTLR[TRE] = 0) or the memory type is mapped to a type other than normal memory (SMMU_CBn_PRRR[MTCn] != 0b10)

Access "class" is determined by the associated page table entry's TEX[0], C, B fields

TEX[0], C, B = 0b000 means class 0

TEX[0], C, B] = 0b001 means class 1

etc.

For each access class, inner-cache and outer-cache policy encodings are as follows:

0b00 = non-cacheable

0b01 = cacheable, copy-back, write-allocate

0b10 = cacheable, write-through, write-no-allocate

0b11 = cacheable, copy-back, write-no-allocate

GFX3D1_SMMU_GFX3D1_CBn_NMRR

Bits	Name	Description
31:30	OCPC7	OCPC7[1:0] (inner-cache policy class 7)
29:28	OCPC6	OCPC6[1:0] (inner-cache policy class 6)
27:26	OCPC5	OCPC5[1:0] (inner-cache policy class 5)
25:24	OCPC4	OCPC4[1:0] (inner-cache policy class 4)
23:22	OCPC3	OCPC3[1:0] (inner-cache policy class 3)
21:20	OCPC2	OCPC2[1:0] (inner-cache policy class 2)
19:18	OCPC1	OCPC1[1:0] (inner-cache policy class 1)
17:16	OCPC0	OCPC0[1:0] (inner-cache policy class 0)
15:14	ICPC7	ICPC7[1:0] (inner-cache policy class 7)
13:12	ICPC6	ICPC6[1:0] (inner-cache policy class 6)
11:10	ICPC5	ICPC5[1:0] (inner-cache policy class 5)
9:8	ICPC4	ICPC4[1:0] (inner-cache policy class 4)
7:6	ICPC3	ICPC3[1:0] (inner-cache policy class 3)
5:4	ICPC2	ICPC2[1:0] (inner-cache policy class 2)
3:2	ICPC1	ICPC1[1:0] (inner-cache policy class 1)
1:0	ICPC0	ICPC0[1:0] (inner-cache policy class 0)

0x07D0003C+0x1000*n GFX3D1_SMMU_GFX3D1_CBn_TLBLKCR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB lock control register governs the TLB locking mechanism and TLB invalidate operations.Write access to this register is governed by SMMU_CR[TLBLKCRWE]

When SMMU_CR[TLBLKCRWE] is 0, writes to SMMU_CBn_TLBLKCR are ignored

Read access is still permitted

SROT can set SMMU_CR[TLBLKCRWE] to 1 to allow operating environment(s) to manage the TLB locking mechanism

Management amongst multiple operating environments must be coordinated via semaphore

GFX3D1_SMMU_GFX3D1_CBn_TLBLKCR

Bits	Name	Description
31:24	RESERVED_2	
23:16	VICTIM	VICTIM[7:0] Indicates the TLB index at which the next normal (non-locking) allocation will occur Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context
15:8	FLOOR	FLOOR[7:0] Indicates the TLB index from which round-robin replacement on normal (non-locking) allocations occurs TLB entries at indices below this value are locked Note that this is a "global" field Updating this field using the SMMU_CBn_TLBLKCR of any particular context bank affects the value of this field for all context banks
7:4	RESERVED_1	

GFX3D1_SMMU_GFX3D1_CBn_TLBLKCR (cont.)

Bits	Name	Description
3	TLBIVAACFG	(TLBIVAA configuration) TLBIVAACFG = 0 - flash-invalidate SMMU_CBn_TLBIVAA commands flash-invalidate the entire TLB, without regard to locking, security, address, and/or VMID value TLBIVAACFG = 1 - selective SMMU_CBn_TLBIVAA commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank VA field of TLB entry matches VA designated by SMMU_CBn_TLBIVAA command NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked
2	TLBIASIDCFG	(TLBIASID configuration) TLBIASIDCFG = 0 - flash-invalidate SMMU_CBn_TLBIASID commands flash-invalidate the entire TLB, without regard to locking, security, VMID, and/or ASID values TLBIASIDCFG = 1 - selective SMMU_CBn_TLBIASID commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command TLB entry is not global (NG field is 1) NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command
1	TLBIALLCFG	(TLBIALL configuration) TLBIALLCFG = 0 - flash-invalidate SMMU_CBn_TLBIALL commands flash-invalidate the entire TLB, without regard to locking, security, and/or VMID value TLBIALLCFG = 1 - selective SMMU_CBn_TLBIALL commands invalidate only entries that match all of the following conditions VMID field of TLB entry matches VMID value associated with the context bank NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command Entry is unlocked

GFX3D1_SMMU_GFX3D1_CBn_TLBLKCR (cont.)

Bits	Name	Description
0	LKE	(lock enable) Governs whether or not TLB entries established by VA-to-PA commands upon TLB misses are locked LKE = 0 (normal, non-locking) Allocate VA-to-PA TLB entry (if TLB miss) at the index specified by SMMU_CBn_TLBLKCR[VICTIM] Allocation is disabled if SMMU_CBn_ACTLR[DNLV2PA] is 1 Increment SMMU_CBn_TLBLKCR[VICTIM] by 1 (only if new entry allocated) Wrap back to the value of SMMU_CBn_TLBLKCR[FLOOR] when the last entry is written LKE = 1 (locking) Search TLB for specified VA and invalidate if found Provides atomicity between the invalidate and the new allocation within the locked region Allocate VA-to-PA TLB entry at the index specified by data operand bits 7:0 of the VA-to-PA command This value must be less than SMMU_CBn_TLBLKCR[FLOOR] in order for it to remain locked Allocation occurs even if non-locking allocation is disabled due to SMMU_CBn_ACTLR[DNLV2PA] = 1

0x07D00040+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_V2PSR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The VA-to-PA status register records the hit/miss status and TLB index or V2Pxx and TLB invalidate commands.

GFX3D1_SMMU_GFX3D1_CBn_V2PSR

Bits	Name	Description
31:16	RESERVED_2	
15:8	INDEX	INDEX[7:0] Indicates the index of the TLB entry associated with the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command If SMMU_CBn_V2PSR[HIT] is 0, then SMMU_CBn_V2PSR[INDEX] is the index to which the entry was allocated (if allocated at all) If SMMU_CBn_V2PSR[HIT] is 1, then SMMU_CBn_V2PSR[INDEX] is the index of the entry which hit
7:1	RESERVED_1	

GFX3D1_SMMU_GFX3D1_CBn_V2PSR (cont.)

Bits	Name	Description
0	HIT	Indicates whether or not there was a TLB hit (prior to allocation, if any) on the last SMMU_CBn_V2Pxx or SMMU_CBn_TLBIVA command

0x07D00044+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_TLBFLPTER, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB first level PTE register holds the first level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

This register (together with SMMU_CBn_TLBSLPTER) is used as the source of the translation information for VA-to-PA operations when the MMU is enabled (SMMU_CBn_SCTLR[M] = 1) and the operations are configured for software table update (SMMU_CBn_ACTLR[V2PCFG] = 0b01)

Field definitions vary according to the type of PTE (fault, page, section, or supersection), and come directly from the ARMv7 architecture's PTE formats

GFX3D1_SMMU_GFX3D1_CBn_TLBFLPTER

Bits	Name	Description
31:10	FL_PTE_HI	
9:5	RESERVED	
4:2	FL_PTE_LO	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	This field should be set to 0b00 or 0b11 to indicate that the translation should result in a context fault, and the rest of the fields are defined as indicated in this section If this field is not 0b00 or 0b11, then the PTE is of some other type (see other sections for the field definitions for those types)

0x07D00048+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_TLBSLPTER, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB second level PTE register holds the second level page table entry value for subsequent use when TLB entry is written by software via SMMU_CBn_TLBWSW.

Field definitions vary according to the type of PTE (fault, 64KB or 4KB), and come directly from the ARMv7 architecture's PTE format

GFX3D1_SMMU_GFX3D1_CBn_TLBSLPTER

Bits	Name	Description
31:2	SL_PTE	The actual contents of the PTE vary depending on the TYPE
1:0	TYPE	0x0: fault

0x07D0004C+0x1000*n GFX3D1_SMMU_GFX3D1_CBn_BFBCR, n=[0..2]

Type: Read/Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The burst fetch buffer configuration register governs the operation of the "burst fill" feature of the SMMU.

GFX3D1_SMMU_GFX3D1_CBn_BFBCR

Bits	Name	Description
31:12	STRIDE	(stride amount) 4KB-aligned value to be added to virtual address on demand TLB miss for filling subsequent BFB Stride of minimum 4KB alignment useful for preventing stride burst fetch until final PTE of the demand BFB entry is used
11:8	SLVIC	(second-level victim) Indicates the SLBFB index at which the next round-robin allocation will occur
7:4	FLVIC	(first-level victim) Indicates the FLBFB index at which the next round-robin allocation will occur
3	RESERVED	
2	SFVS	(stride-fetch victim selection) SFVS. = 0 (replace normal round-robin victim-selected entry) Useful when stride is larger than the VA space represented by the four PTEs in the demand BFB entry, but the client access pattern is for more than just the initial PTE in that demand BFB entry SFVS. = 1 (replace same BFB used by demand VA for which the stride burst is being performed) Useful when stride is the same as the VA space represented by an individual PTE in the demand BFB entry (such that the stride won't miss against the BFB until the last PTE of the demand BFB entry is accessed), and/or when the client access pattern only uses the initial PTE in the demand BFB entry

GFX3D1_SMMU_GFX3D1_CBn_BFBCR (cont.)

Bits	Name	Description
1	BFBSFE	(burst fetch buffer stride fetch enable) Enables stride burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Stride burst fetch is for the block of four PTEs associated with VA+stride VA is the "demanded" VA from the client (or VA-to-PA command) Stride value is specified by SMMU_CBn_BFBCR[STRIDE] Stride burst fetch only occurs if demand access for VA misses in TLB (could hit in BFB) and address VA+stride misses in both TLB and BFB
0	BFBDFE	(burst fetch buffer demand fetch enable) Enables demand burst fetch of four aligned-contiguous PTEs into BFB due to TLB miss Demand burst fetch is for the block of four PTEs associated with the "demanded" VA from the client (or VA-to-PA command) Demand burst fetch only occurs if demand access misses in both TLB and BFB

0x07D00800+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_TLBIALL, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate all command register invalidates all TLB entries matching the VMID associated with this context bank. Data operand is ignored.

GFX3D1_SMMU_GFX3D1_CBn_TLBIALL

Bits	Name	Description
31:0	RESERVED	

0x07D00804+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_TLBIASID, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by ASID command register invalidates TLB entries matching the specified ASID and matching the VMID associated with this context bank.Invalidates TLB entries which are associated with the designated ASID and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIASIDCFG] governs whether command flash-invalidates entire TLB array or just the entries matching the VMID, ASID, and security state

TLBIASIDCFG = 0 - flash-invalidate

SMMU_CBn_TLBIASID command flash-invalidates the entire TLB, without regard to locking, security, VMID, and/or ASID values

TLBIASIDCFG = 1 - selective

SMMU_CBn_TLBIASID command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIASID command data operand

TLB entry is not global (NG field is 1)

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIASID command

Locking is not considered (matching entries are invalidated even if locked)

ASID field of command specifies the ASID value of the TLB entries to be invalidated

GFX3D1_SMMU_GFX3D1_CBn_TLBIASID

Bits	Name	Description
31:8	RESERVED	
7:0	ASID	Actual ASID value

0x07D00808+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_TLBIVA, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA command invalidates TLB entries matching the designated VA, ASID and the VMID associated with this context bank.

Matching entry determined as follows:

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

ASID field of TLB entry matches ASID value designated by the SMMU_CBn_TLBIVA command data operand (or TLB entry is global - NG field is 0)

VA field of TLB entry matches VA value designated by the SMMU_CBn_TLBIVA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIVA command

Locking is not considered (matching entry is invalidated even if locked)

Data operand specifies the VA and ASID value of the TLB entry to be invalidated

GFX3D1_SMMU_GFX3D1_CBn_TLBIVA

Bits	Name	Description
31:12	VA	VA[31:12]
11:8	RESERVED	
7:0	ASID	ASID[7:0] value

0x07D0080C+0x1000*n GFX3D1_SMMU_GFX3D1_CBn_TLBIVAA, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB invalidate by VA all ASIDS command invalidates TLB entries matching the designated VA and the VMID associated with this context bank, regardless of ASID.Invalidates TLB entries which are associated with the designated VA, regardless of ASID, and which are associated with the VMID associated with the specified context bank

SMMU_CBn_TLBLKCR[TLBIVAACFG] governs whether command flash-invalidates entire TLB array or just the non-locked entries matching the VMID, ASID, and security state

TLBIVAACFG = 0 - flash-invalidate

SMMU_CBn_TLBIVAA command flash-invalidates the entire TLB, without regard to locking, security, address, and/or VMID value

TLBIVAACFG = 1 - selective

SMMU_CBn_TLBIVAA command invalidates only entries that match all of the following conditions

VMID field of TLB entry matches VMID value associated with the context bank from SMMU_CBACRn[CBVMID]

VA field of TLB entry matches VA designated by the SMMU_CBn_TLBIVAA command data operand

NSTID field of TLB entry matches APROTNS of SMMU_CBn_TLBIALL command

Entry is unlocked

GFX3D1_SMMU_GFX3D1_CBn_TLBIVAA

Bits	Name	Description
31:12	VA	VA[31:12]
11:0	RESERVED	

0x07D00810+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_V2PRR, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

GFX3D1_SMMU_GFX3D1_CBn_V2PRR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07D00814+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_V2PPW, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "privileged write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR. Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

GFX3D1_SMMU_GFX3D1_CBn_V2PPW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07D00818+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_V2PUR, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user read". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

GFX3D1_SMMU_GFX3D1_CBn_V2PUR

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07D0081C+0x1000*n GFX3D1_SMMU_GFX3D1_CBn_V2PUW, n=[0..2]

Type: Write
Clock: AXI_BUS_CLOCK
Reset State: Undefined

This VA-to-PA command translates the given virtual address value to the corresponding physical address, using the access permission type "user write". If the translation is successful, the resulting physical address is placed in the SMMU_CBn_PAR.

Searches TLB (and optionally the page table) for the translation of the specified VA

VMID is as configured for the context bank via SMMU_CBACRn[CBVMID]

ASID is as specified in SMMU_CBn_CONTEXTIDR[ASID]

Result recorded in SMMU_CBn_PAR

SMMU_CBn_TLBLKCR[LKE] governs whether or not TLB entries allocated by SMMU_CBn_V2Pxx commands are locked in the TLB

SMMU_CBn_ACTLR[V2PCFG] governs the operation of SMMU_CBn_V2Pxx commands that miss in the TLB

.Either pass-through as if MMU were disabled, or signal TLB Miss context fault, or use SMMU_CBn_TLBFLPTER/TLBSLPTER as PTE, or perform hardware table walk to access PTE

SMMU_CBn_ACTLR[DNLV2PA] governs whether non-locking SMMU_CBn_V2Pxx commands that miss in the TLB will allocate a new entry

Data operand specifies the VA to be translated (and optionally the TLB index at which to allocate the entry, if locking)

GFX3D1_SMMU_GFX3D1_CBn_V2PUW

Bits	Name	Description
31:12	VA	VA[31:12] to be translated
11:8	RESERVED	
7:0	INDEX	INDEX[7:0] (index) TLB index at which the new entry should be allocated when locking is enabled (SMMU_CBn_TLBLKCR[LKE] is 1)

0x07D00820+ 0x1000*n GFX3D1_SMMU_GFX3D1_CBn_RESUME, n=[0..2]

Type: Write/command
Clock: AXI_BUS_CLOCK
Reset State: Undefined

The TLB resume command causes the SMMU to resume operation after a stalled access..

GFX3D1_SMMU_GFX3D1_CBn_RESUME

Bits	Name	Description
31:1	RESERVED	

GFX3D1_SMMU_GFX3D1_CBn_RESUME (cont.)

Bits	Name	Description
0	TNR	Terminate/not retry When TNR is written as 0, indicates that the stalled access should be retried by the system MMU. When written as 1, indicates that this stalled transaction is terminated by the system MMU. The error is optionally reported to the requesting master, using the client port bus protocol, if SMMU_CNn_ACTLR[CFERE] == 1. Interrupt optionally remains asserted via SMMU_M2VCBRn[IRPTINDX] selected SMMU_contextFaultIrptReq bit, only if SMMU_CBn_ACTLR[CFEIE] is 1, and only if SMMU_CBn_FSR has not been cleared by software priori to issuing this command..

14.32 System FPB SMMU Registers (0x07F00000 SMMU_SFPB_CFG_DUMMY_BASE)

This section contains System FPB SMMU registers.

14.32.1 System FPB Registers

14.32.1.1 Configuration registers

0x07F00000 SMMU_SFPB_CFG_SFPB_CTRL_STATUS

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000

The SFPB_CTRL_STATUS register is a general configuration register.

SMMU_SFPB_CFG_SFPB_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables Power up value is clear (0)
11	RPM_ARM7_IRQ_EN	SW: RW, HW: R ARM7InterruptEnable When set, the ARM7 receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	SC_IRQ_EN	SW: RW, HW: R ScorpionInterruptEnable When set, the Scorpion receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

SMMU_SFPB_CFG_SFPB_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x7: Select the M0 ahb2ahb bridge test bus.

0x07F00004+0x4*a SMMU_SFPB_CFG_SFPB_AHB2AHB_CFG_Ma, a=[0..0]

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x09

The SFPB_AHB2AHB_CFG_Ma register is to configure the AHB2AHB bridge of master Ma. The AHB2AHB bridge is instantiated if the AHB interface is async (Generic: MASTER_ASYNC_IF(a) = ’1’). Otherwise this register is reserved.

SMMU_SFPB_CFG_SFPB_AHB2AHB_CFG_Ma

Bits	Name	Description
30:6	RESERVED_BITS30_6	
5:4	M_AHB2AHB_TEST_EN	SW: RW, HW: R Test enable for the Sa lite_bridge. Power up value is 00 0x0: DISABLED 0x1: Select slave side test signals 0x2: Select master side test signals 0x3: RESERVED_PROGRAMMING
3	M_WPOST_EN	SW: RW, HW: R MaWritePostEnable When set (1), the ahb2ahb bridge will support posting of write data. When cleared (0), each write request must complete across the bus before the next is accepted. Power up value is set (1)
2	M_HALT_ACK	SW:R, HW:W Indicates the Ma acknowledgement of halt_req asserted by software. Power up value is clear (0).

SMMU_SFPB_CFG_SFPB_AHB2AHB_CFG_Ma (cont.)

Bits	Name	Description
1	M_HALT_REQ	SW:RW, HW:R Software should write to this register to request the Ma lite_bridge master to cleanly halt. Power up value is clear (0).
0	M_IDLE	SW:R, HW:W Indicates that the Ma lite bridge master FSM is in IDLE state. Power up value is set (1).

0x07F00044 SMMU_SFPB_CFG_SFPB_PORT_EN

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFF

The SFPB_PORT_EN register is a SFPB master port enable register.

SMMU_SFPB_CFG_SFPB_PORT_EN

Bits	Name	Description
31:1	RESERVED_BIT31_1	
0	M0_PORT_EN	SW:RW, HW:R M0PortEnable When cleared (0), M0 bridge is prevented from arbitting on the system_fpb bus. Power up value is set(1)

14.32.1.2 Bus error registers and additional configure registers

0x07F00050 SMMU_SFPB_CFG_SFPB_ERROR_STAT

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000000

The SFPB_ERROR_STAT register is the bus error status register.

SMMU_SFPB_CFG_SFPB_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	

SMMU_SFPB_CFG_SFPB_ERROR_STAT (cont.)

Bits	Name	Description
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the channel ID that caused the detected error when CID is valid for the master of the access. If not, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Master0
11:10	RESERVED_BITS11_10	
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit
3:2	RESERVED_BIT3_2	
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

SMMU_SFPB_CFG_SFPB_ERROR_STAT (cont.)

Bits	Name	Description
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted. Clearing (0) this bit clears any interrupts asserted as well as enables the SFPB_ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x07F00054 SMMU_SFPB_CFG_SFPB_ERROR_ADDR

Type: Read
Clock: CC_SFPB_CLK
Reset State: 0x00000000

The SFPB_ERROR_ADDR register contains the bus error address.

SMMU_SFPB_CFG_SFPB_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when SFPB_ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x07F00058 SMMU_SFPB_CFG_SFPB_GPREG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0

The SFPB_GPREG register is a configurable general purpose register.

SMMU_SFPB_CFG_SFPB_GPREG

Bits	Name	Description
0	GPREG_RESERVED	SW: RW, HW: R Reserved. Power up value is 0.

0x07F0005C SMMU_SFPB_CFG_SFPB_XPU_ACR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFFFFFF

The SFPB_XPU_ACR register is a SFPB Access Control Register for configure register protection.

SMMU_SFPB_CFG_SFPB_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R SFPB XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the SFPB configure space, including this register itself. Power up value is set (1)

0x07F00060 SMMU_SFPB_CFG_SFPB_HW_CLK_GATING_CFG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0000

The SFPB_HW_CLK_GATING_CFG register is for hardward clock gating configuration register.

SMMU_SFPB_CFG_SFPB_HW_CLK_GATING_CFG

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	HYSTERESIS_CNT_SW	SW: RW, HW: R Hysteresis Conter Value The value of this field is for SW to set the hysteresis counter for hardward clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)
3:0	WAKE_CNT_SW	SW: RW, HW: R Wakeup Conter Value The value of this field is for SW to set the wakeup counter for hardward clock gating scheme. This field is used when ENABLE_HW_CLK_GATING is set to 1. Power up value is clear (0)

15 PCIE20 Registers

15.1 Overview

Table 15-1 PCIE20 Bases

Base Name	Parent	Address
PCIE20_DEVICE_VENDORID	PCIE20_BASE	0x1B500000
PCIE20_ELBI_VERSION	PCIE20_ELBI_BASE	0x1B502000
PCIE20_PARF_SYS_CTRL	PCIE20_PARF_BASE	0x1B600000

15.2 PCIE20 Registers (0x1B500000 PCIE20_BASE)

This section contains PCIe20 registers.

0x1B500000 PCIE20_DEVICE_VENDORID

Type: Read
Clock: UNDEFINED
Reset State: 0x010117CB

Device and Vendor ID

PCIE20_DEVICE_VENDORID

Bits	Name	Description
31:16	DEVICEID	READ ONLY Device ID
15:0	VENDORID	READ ONLY Vendor ID

0x1B500004 PCIE20_STATUS_COMMAND_REGISTER

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00100000

Status and Command registers

PCIE20_STATUS_COMMAND_REGISTER

Bits	Name	Description
31	DETECT_PARERR	Detected Parity Error
30	SIGNAL_SYSERR	Signaled System Error
29	RCVD_MASTERABORT	Received Master Abort
28	RCVD_TRGTABORT	Received Target Abort
27	SIGNAL_TRGTABORT	Signaled Target Abort
26:25	DEVSEL_TIME	READ ONLY DevSel Timing, Hardwired to 0 for PCIExpress
24	MASTERDATA_PARERR	Master Data Parity Error
23	FAST_B2B	READ ONLY Back to Back Capable, Hardwired to 0 for PCIExpress

PCIE20_STATUS_COMMAND_REGISTER (cont.)

Bits	Name	Description
22	RESERV3	READ ONLY Reserved
21	C66MHZ_CAP	READ ONLY - 66MHz Capable, Hardwired to 0 for PCIExpress
20	CAP_LIST	READ ONLY Capabilities List Hardwired to 1
19	INTX_STATUS	READ ONLY INTx Status
18:16	RESERV2	READ ONLY Reserved
15:11	RESERV1	READ ONLY Reserved
10	INTX_ASSER_DIS	INTx Assertion Disable
9	FAST_BBEN	READ ONLY Bit hardwired to 0 for PCIExpress
8	SERR_EN	SERR Enable
7	IDSEL_CTRL	READ ONLY Bit hardwired to 0 for PCIExpress
6	PARITYERRRESP	Parity Error Response
5	VGA_SNOOP	READ ONLY Not Applicable for PCI Express. Bit hardwired to 0 for PCIExpress
4	MEMWR_INVA	READ ONLY Not Applicable for PCI Express. Bit hardwired to 0 for PCIExpress
3	SPEC_CYCLE_EN	READ ONLY Not Applicable for PCI Express. Bit hardwired to 0 for PCIExpress
2	BUSMASTER_EN	Bus Master Enable
1	MEM_SPACE_EN	Memory Space Enable
0	IO_SPACE_EN	IO Space Enable

0x1B500008 PCIE20_CLASSCODE_REVISIONID

Type: Read
Clock: UNDEFINED
Reset State: 0xFF000000

Class code and Revision ID

PCIE20_CLASSCODE_REVISIONID

Bits	Name	Description
31:24	BASE_CLS_CD	READ ONLY Sub Class Code
23:16	SUBCLS_CD	READ ONLY Sub Class Code
15:8	PROG_IF_CODE	READ ONLY Programming Interface Code
7:0	REVID	READ ONLY Revision ID

0x1B50000C PCIE20_BIST_HEAD_LAT_CACH

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00010000

BIST, Header Type, Latency Timer, Cache Line Size

PCIE20_BIST_HEAD_LAT_CACH

Bits	Name	Description
31:24	BIST	READ ONLY BIST
23	MFD	READ ONLY MultiFunction Device
22:16	HEAD_TYP	READ ONLY Header Type
15:8	MSTR_LAT_TIM	READ ONLY Master Latency Timer, Not Applicable for PCIe hence hardwired to 0
7:0	CACH_LN_SZE	Cache Line Size, No impact on write, write is allowed only for legacy purpose

0x1B500010 PCIE20_BAR_ADR_0

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Base Address Register 0

PCIE20_BAR_ADR_0

Bits	Name	Description
31:4	BAR0_BASE_ADDR	BAR0 base address bits (for a 64-bit BAR, the remaining upper address bits are in BAR1). The BAR0 Mask value determines which address bits are masked/RO.
3	BAR0_PREFETCHABLE	READ ONLY If BAR0 is a memory BAR, bit 3 indicates if the memory region is prefetchable: . 0 = Non-prefetchable 1 = Prefetchable If BAR0 is an I/O BAR, bit 3 is the second least significant bit of the base address.
2:1	BAR0_TYPE	READ ONLY If BAR0 is a memory BAR, bits [2:1] determine the BAR type: . 00 = 32-bit BAR . 10 = 64-bit BAR If BAR0 is an I/O BAR, bit 2 the least significant bit of the base address and bit 1 is 0.
0	BAR0_MEM_INDICATOR	READ ONLY - 0 = BAR0 is a memory BAR . 1 = BAR0 is an I/O BAR

0x1B500014 PCIE20_BAR_ADR_1

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Base Address Register 1

PCIE20_BAR_ADR_1

Bits	Name	Description
31:4	BAR1_BASE_ADDR	BAR1 base address bits (for a 64-bit BAR, the remaining upper address bits are in BAR1, lower 32 bits in BAR0 Register). If BAR0 is only 32 bit then BAR1 can be programmed separately as 32 bit BAR Register
3	BAR1_PREFETCHABLE	READ ONLY If BAR1 is a memory BAR, bit 3 indicates if the memory region is prefetchable: . 0 = Non-prefetchable . 1 = Prefetchable If BAR1 is an I/O BAR, bit 3 is the second least significant bit of the base address.
2:1	BAR1_TYPE	READ ONLY If BAR1 is a memory BAR, bits [2:1] determine the BAR type: . 00 = 32-bit BAR . 10 = 64-bit BAR If BAR1 is an I/O BAR, bit 2 the least significant bit of the base address and bit 1 is 0.
0	BAR1_MEM_INDICATOR	READ ONLY - 0 = BAR1 is a memory BAR. 1 = BAR1 is an I/O BAR

0x1B500018 PCIE20_BUS_NUM_REG

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Bus Number Registers

PCIE20_BUS_NUM_REG

Bits	Name	Description
31:24	SEC_LAT_TIMER	READ ONLY Secondary Latency Timer, Not Applicable for PCI Express hence hardwired to 0
23:16	SUBORD_BUS_NUM	Subordinate Bus Number
15:8	SEC_BUS_NUM	Secondary Bus Number
7:0	PRIM_BUS_NUM	Primary Bus Number

0x1B50001C PCIE20_IOBASE_LIMIT_SEC_STATUS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

IO Base,Limit and Secondary Status Register

PCIE20_IOBASE_LIMIT_SEC_STATUS

Bits	Name	Description
31	DET_PAR_ERR	Detected Parity Error
30	RCVD_SYS_ERR	Received System Error
29	RCVD_MSTR_ABORT	Received Master Abort
28	RCVD_TRGT_ABORT	Received Target Error
27	SGNLD_TRGT_ABORT	Signaled Target Error
26:25	DEVSEL_TIMING	READ ONLY DEVSEL Timing, Not Applicable for PCI Express hence hardwired to 0
24	MSTR_DATA_PRTY_ERR	Mastered Data Parity Error
23	FAST_B2B_CAP	READ ONLY Fast Back to Back Capable, Not Applicable for PCI Express hence hardwired to 0

PCIE20_IOBASE_LIMIT_SEC_STATUS (cont.)

Bits	Name	Description
22	RSVD1	READ ONLY Reserved
21	C66MHZ_CAPA	READ ONLY - 66MHz Capable, Not Applicable for PCI Express hence hardwired to 0
20:16	RSVD2	READ ONLY Reserved
15:12	IO_SPACE_LIMIT	IO_Space_Limit
11:9	RSVD3	READ ONLY Reserved
8	IODECODE_32	READ ONLY - 32 or 16 Bit IO Space
7:4	IO_SPACE_BASE	IO_Space_Limit
3:1	RSVD4	READ ONLY Reserved
0	IODECODE_32_0	READ ONLY - 32 or 16 Bit IO Space

0x1B500020 PCIE20_MEM_BASE_LIMIT

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Memory Base and Limit Register

PCIE20_MEM_BASE_LIMIT

Bits	Name	Description
31:20	MEM_LIMIT_ADDR	Memory Limit Address
19:16	RSVD1	READ ONLY Reserved
15:4	MEM_BASE_ADDR	Memory Base Address
3:0	RSVD2	READ ONLY Reserved

0x1B500024 PCIE20_PREF_MEM_BASE_LIMIT

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00010001

Prefetchable Memory Base and Limit Register

PCIE20_PREF_MEM_BASE_LIMIT

Bits	Name	Description
31:20	PREF_MEM_ADDR	Upper 12 bits of 32-bit Prefetchable Memory End Address
19:17	RSVD1	READ ONLY Reserved
16	MEMDECODE_64	READ ONLY - 64-Bit Memory Addressing
15:4	UPPPREF_MEM_ADDR	Upper 12 bits of 32-bit Prefetchable Memory start Address
3:1	RSVD2	READ ONLY Reserved
0	MEMDECODE_64_0	READ ONLY - 64-Bit Memory Addressing

0x1B500028 PCIE20_UPPER_32BIT_PREF_BASEADDR

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Upper 32 Bit Prefetchable Base Address Register

PCIE20_UPPER_32BIT_PREF_BASEADDR

Bits	Name	Description
31:0	ADDRUPP	Upper 32 Bits of Base Address of Prefetchable Memory Space, Used only if 64 Bit Prefetchable Addressing is enabled

0x1B50002C PCIE20_UPPER_32BIT_PREF_LIMITADDR

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Upper 32 Bit Prefetchable Limit Address Register

PCIE20_UPPER_32BIT_PREF_LIMITADDR

Bits	Name	Description
31:0	ADDRUPP_LIMIT	Upper 32 Bits of Limit Address of Prefetchable Memory Space, Used only if 64 Bit Prefetchable Addressing is enabled

0x1B500030 PCIE20_IO_BASE_LIMIT

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

IO Base and Limit Register

PCIE20_IO_BASE_LIMIT

Bits	Name	Description
31:16	UPP16_IOLIMIT	Upper 16 IO Limit Address
15:0	UPP16_IOBASE	Upper 16 IO Base Address

0x1B500034 PCIE20_CAPPTR

Type: Read
Clock: UNDEFINED
Reset State: 0x00000040

CapPtr

PCIE20_CAPPTR

Bits	Name	Description
31:8	RESERVE1	READ ONLY Reserved
7:0	CAPTR	READ ONLY First Capability Pointer

0x1B500038 PCIE20_EXP_ROM_ADDR

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Expansion ROM Base Address

PCIE20_EXP_ROM_ADDR

Bits	Name	Description
31:11	ADDR	Expansion ROM Address
10:1	RSVD	READ ONLY Reserved Bits
0	EXP_ROM_EN	Expansion ROM Enable

0x1B50003C PCIE20_BRIDGE_INT

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x000001FF

Bridge Control and Int Pin and line

PCIE20_BRIDGE_INT

Bits	Name	Description
31:28	RSVD1	READ ONLY Reserved
27	DT_SERR_EN	READ ONLY Discard Timer SERR Enable Status
26	DT_STS	READ ONLY Discard Timer Status
25	SEC_DT	READ ONLY Secondary Discard Timer
24	PRI_DT	READ ONLY Primary Discard Timer
23	FAST_B2B_EN	READ ONLY Fast Back-to-Back Transactions Enable
22	SEC_BUS_RST	Secondary Bus Reset
21	MST_ABT_MOD	READ ONLY Master Abort Mode
20	VGA_16B_DEC	VGA 16-Bit Decode
19	VGA_EN	VGA Enable
18	ISA_EN	ISA Enable
17	SERR_EN	SERR Enable
16	PERR_RESP_EN	Parity Error Response Enable

PCIE20_BRIDGE_INT (cont.)

Bits	Name	Description
15:8	INT_PIN	READ ONLY Interrupt Pin
7:0	INT_LIN	Interrupt Line

0x1B500040 PCIE20_CFG_PWR_CAP

Type: Read
Clock: UNDEFINED
Reset State: 0xDBC35001

Power, ID

PCIE20_CFG_PWR_CAP

Bits	Name	Description
31:27	PME_SP	READ ONLY PME Support, writable through the DBI.
26	D2_SP	READ ONLY D2 Support, writable through the DBI.
25	D1_SP	READ ONLY D1 Support, writable through the DBI.
24:22	AUX_CUR	READ ONLY AUX Current, writable through the DBI.
21	DSI	READ ONLY Device Specific Initialization (DSI), writable through the DBI.
20	RSVD1	READ ONLY Reserved
19	PME_CLK	READ ONLY PME Clock, hardwired to 0
18:16	PMC_VER	READ ONLY Power Management specification version, writable through the DBI
15:8	PM_NX_PTR	READ ONLY Next Capability Pointer
7:0	CAP_ID	READ ONLY Capability ID

0x1B500044 PCIE20_PWR_CSR

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

PM Control Status

PCIE20_PWR_CSR

Bits	Name	Description
31:24	DATA1	READ ONLY Data register for additional information (not supported)
23	BP_CCE	READ ONLY Bus Power/Clock Control Enable, hardwired to 0
22	B2B3_SP	READ ONLY B2/B3 Support, hardwired to 0
21:16	RSVD1	READ ONLY Reserved
15	PME_STATUS	PME Status
14:13	DATA_SCALE	READ ONLY Data Scale (not supported)
12:9	DATA_SEL	READ ONLY Data Select (not supported)
8	PME_EN	PME Enable (sticky bit)
7:4	RSVD2	READ ONLY Reserved
3	NSR	READ ONLY No Soft Reset, writable through the DBI
2	RSVD3	READ ONLY Reserved
1:0	PW_STATE	Power State

0x1B500050 PCIE20_MSG_CTR

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00807005

MSI cap structure

PCIE20_MSG_CTR

Bits	Name	Description
31:25	RSVD1	READ ONLY Reserved
24	PVM_EN	READ ONLY MSI Per Vector Masking (PVM) supported
23	MSI_64_EN	READ ONLY - 64-bit Address Capable, writable through the DBI
22:20	MME	Multiple Message Enable
19:17	MMC	READ ONLY Multiple Message Capable, writable through the DBI
16	MSI_EN	MSI Enabled
15:8	MSI_NX_PTR	READ ONLY Next Capability Pointer
7:0	CAP_ID	READ ONLY MSI Capability ID

0x1B500054 PCIE20_MSI_L32

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

MSI Lower 32-bit address register

PCIE20_MSI_L32

Bits	Name	Description
31:2	ADDR	Lower 32 Bit Address
1:0	RSVD	READ ONLY Reserved

0x1B500058 PCIE20_MSI_U32

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

MSI Upper 32-bit address register

PCIE20_MSI_U32

Bits	Name	Description
31:0	ADDR	Upper 32 Bit Address, Optional, used only if 'MSI_64_EN = 1

0x1B50005C PCIE20_MSI_DATA

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

MSI Data Register

PCIE20_MSI_DATA

Bits	Name	Description
31:16	RSVD	READ ONLY Reserved
15:0	MSI_DATA_F	MSI Data

0x1B500060 PCIE20_MSI_MASK

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

MSI Mask Bit Register

PCIE20_MSI_MASK

Bits	Name	Description
31:0	MSI_MASKBITS	MSI Mask Bit Register

0x1B500064 PCIE20_MSI_PEND

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

MSI Pending Bit Register

PCIE20_MSI_PEND

Bits	Name	Description
31:0	MSI_PENDBITS	READ ONLY MSI Pending Bit Register

0x1B500070 PCIE20_PCIE_CAP

Type: Read
Clock: UNDEFINED
Reset State: 0x00420010

PCIE cap structure

PCIE20_PCIE_CAP

Bits	Name	Description
31:30	RSVD1	READ ONLY Reserved
29:25	IM_NUM	READ ONLY Interrupt Message Number
24	SLOT	READ ONLY Slot Implemented
23:20	DEV_TYPE	READ ONLY Device/Port Type
19:16	PCIE_VER	READ ONLY PCI Express Capability Version
15:8	PCIE_NX_PTR	READ ONLY Next Capability Pointer
7:0	CAP_ID	READ ONLY Capability ID

0x1B500074 PCIE20_DEV_CAP

Type: Read
Clock: UNDEFINED
Reset State: 0x00008000

PCIE Device Capabilities

PCIE20_DEV_CAP

Bits	Name	Description
31:29	RSVD2	READ ONLY Reserved
28	FLR_EN	READ ONLY Function Level Reset Capability
27:26	CAPT_SLOW_PWRLIMIT_SCALE	READ ONLY Captured Slow Power Scale Value, for Upstream Port Only
25:18	CAPT_SLOW_PWRLIMIT_VALUE	READ ONLY Captured Slow Power Limit Value, for Upstream Port Only
17:16	RSVD1	READ ONLY Reserved
15	ROLEBASED_ERRRPT	READ ONLY Role Based Error Reporting
14:12	UNDEFINED	READ ONLY Undefined from PCIe 1.1 onwards
11:9	DEFAULT_EP_L1_ACCPT_LATENCY	READ ONLY Endpoint L1 Acceptable Latency
8:6	DEFAULT_EP_L0S_ACCPT_LATENCY	READ ONLY Endpoint L0s Acceptable Latency
5	EXTTAGFIELD_SUPPORT	READ ONLY Value derived from DEFAULT_EXT_TAG_FIELD_SUPPORTED
4:3	PHANTOMFUNC	READ ONLY Phantom Function Support, NOT SUPPORTED PRESENTLY
2:0	MAX_PAYLOAD_SIZE	READ ONLY Automatically derived from CX_MAX_MTU

0x1B500078 PCIE20_DEV_CAS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00002010

PCIE Device Control and Status

PCIE20_DEV_CAS

Bits	Name	Description
31:22	RSVD	READ ONLY Reserved

PCIE20_DEV_CAS (cont.)

Bits	Name	Description
21	TRANS_PEND	READ ONLY Transaction Pending
20	AUXP_DET	READ ONLY Aux Power Detected
19	UR_DET	Unsupported Request Detected
18	FT_DET	Fatal Error Detected
17	NFT_DET	Non-Fatal Error Detected
16	COR_DET	Correctable Error Detected
15	INIT_FLR	READ ONLY Reserved
14:12	MRRS	Max_Read_Request_Size
11	NOSNP_EN	Enable No Snoop
10	AUXPM_EN	AUX Power PM Enable
9	PHFUN_EN	Phantom Function Enable
8	EXTAG_EN	Extended Tag Field Enable
7:5	MPS	Max_Payload_Size
4	EN_RO	Enable Relaxed Ordering
3	UR_RE	Unsupported Request Reporting Enable
2	FT_RE	Fatal Error Reporting Enable
1	NFT_RE	Non-Fatal Error Reporting Enable
0	COR_RE	Correctable Error Reporting Enable

0x1B50007C PCIE20_LNK_CAP

Type: Read
Clock: UNDEFINED
Reset State: 0x00764C42

PCIE Link Capabilities

PCIE20_LNK_CAP

Bits	Name	Description
31:24	PORT_NUM	READ ONLY Port Number

PCIE20_LNK_CAP (cont.)

Bits	Name	Description
23	RSVD	READ ONLY Reserved
22	ASPM_OPT_COMP	READ ONLY ASPM Optionally Compliance
21	LNK_BW_NOT_CAP	READ ONLY Link Bandwidth Notification Capability
20	DLL_ACTRPT_CAP	READ ONLY Data Link Layer Active Reporting Capable
19	UNSUP	READ ONLY Unsupported, Surprise Down Error Reporting Capable, Hardwired to 0
18	CLK_PWR_MGMT	READ ONLY Clock Power Management
17:15	L1_EXIT_LAT	READ ONLY L1 Exit Latency
14:12	L0S_EXIT_LAT	READ ONLY L0s Exit Latency
11:10	AS_LINK_PM_SUPPORT	READ ONLY Active State Link PM Support
9:4	MAX_LINK_WIDTH	READ ONLY Max Link Width
3:0	MAX_LINK_SPEEDS	READ ONLY Supported Max Link Speed

0x1B500080 PCIE20_LNK_CAS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x10110000

PCIE Link Control and Status

PCIE20_LNK_CAS

Bits	Name	Description
31	LAB_STATUS	Link Autonomous Bandwidth Status
30	LBW_STATUS	Link Bandwidth Management Status
29	DLL_ACT	READ ONLY Data Link Layer Active

PCIE20_LNK_CAS (cont.)

Bits	Name	Description
28	SLOT_CLK_CONFIG	READ ONLY SLOT_CLK_CONFIGined
27	LINK_TRAIN	READ ONLY LINK_TRAINined
26	UNDEF	READ ONLY Undefined
25:20	NEG_LW	READ ONLY Negotiated Link Width
19:16	LINK_SPEED	READ ONLY Link Speed
15:12	RSVD2	READ ONLY Reserved
11	LABIE	READ ONLY Link Autonomous Bandwidth Interrupt Enable. Reserved for upstream port
10	LBMIE	READ ONLY Link Bandwidth Management Interrupt Enable. Reserved for upstream port
9	HAWD	READ ONLY Hardware Autonomous Width Disable
8	EN_CPM	Enable Clock Power Management
7	EXT_SYN	Extended Synch
6	COM_CLK_CFG	Common Clock Configuration
5	RETRAIN_LINK	Retrain Link
4	LINK_DIS	Link Disable
3	RCB	READ ONLY Read Completion Boundary
2	RSVD	READ ONLY Reserved
1:0	ASPM_CTRL	Active State Link PM Control

0x1B500084 PCIE20_SLOT_CAP

Type: Read
Clock: UNDEFINED
Reset State: 0x0002007F

Slot Capabilities Register

PCIE20_SLOT_CAP

Bits	Name	Description
31:19	PSN	READ ONLY Physical Slot Number
18	NCCS	READ ONLY No Command Complete Support
17	EIP	READ ONLY Electromechanical Interlock Present
16:15	SPLS	READ ONLY Slot Power Limit Scale
14:7	SPLV	READ ONLY Slot Power Limit Value
6	HPC	READ ONLY Hot-Plug Capable
5	HPS	READ ONLY Hot-Plug Surprise
4	PIP	READ ONLY Power Indicator Present
3	AIP	READ ONLY Attention Indicator Present
2	MRLSP	READ ONLY MRL Sensor Present
1	PCP	READ ONLY Power Controller Present
0	ABP	READ ONLY Attention Button Present

0x1B500088 PCIE20_SLOT_CAS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x000003C0

Slot Control and Status Register

PCIE20_SLOT_CAS

Bits	Name	Description
31:25	RSVD2	READ ONLY Reserved

PCIE20_SLOT_CAS (cont.)

Bits	Name	Description
24	DSC	Data Link Layer State Changed
23	EIS	READ ONLY Electromechanical Interlock Status
22	PDS	READ ONLY Presence Detect State
21	MRLSS	READ ONLY MRL Sensor State
20	CC	Command Completed
19	PDC	Presence Detect Changed
18	MRCSC	MRL Sensor Changed
17	PFD	Power Fault Detected
16	ABP	Attention Button Pressed
15:13	RSVD1	READ ONLY Reserved
12	DSC_EN	Data Link Layer State Changed Enable
11	EIC	Electromechanical Interlock Control
10	PCC	Power Controller Control
9:8	PIC	Power Indicator Control
7:6	AIC	Attention Indicator Control
5	HPI_EN	Hot-Plug Interrupt Enable
4	CCI_EN	Command Completed Interrupt Enable
3	PDC_EN	Presence Detect Changed Enable
2	MRLSC_EN	MRL Sensor Changed Enable
1	PFD_EN	Power Fault Detected Enable
0	ABP_EN	Attention Button Pressed Enable

0x1B50008C PCIE20_ROOT_CAC

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Root Control and Capability Register

PCIE20_ROOT_CAC

Bits	Name	Description
31:17	RSVD2	READ ONLY Reserved
16	CRSSV	READ ONLY CRS Software Visibility
15:5	RSVD1	READ ONLY Reserved
4	CRSSV_EN	READ ONLY CRS Software Visibility Enable
3	PMEI_EN	PME Interrupt Enable
2	SEFE_EN	System Error on Fatal Error Enable
1	SENE_EN	System Error on Non-fatal Error Enable
0	SECE_EN	System Error on Correctable Error Enable

0x1B500090 PCIE20_ROOT_STS

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Root Status Register

PCIE20_ROOT_STS

Bits	Name	Description
31:18	RSVD	READ ONLY Reserved
17	PME_PND	READ ONLY PME Pending
16	PME_STS	PME Status
15:0	PME_RID	READ ONLY PME Requester ID

0x1B500094 PCIE20_DEV_CAP_2

Type: Read
Clock: UNDEFINED
Reset State: 0x00000010

Device Capabilities 2 Register

PCIE20_DEV_CAP_2

Bits	Name	Description
31:14	RSVD2	READ ONLY Reserved
13:12	TPHC_SP	READ ONLY TPH Completer Supported
11	RSVD1	READ ONLY Reserved
10	NOROPR	READ ONLY No RO-enabled PR-PR Passing
9	CASC128_SP	READ ONLY - 128-bit CAS Completer Supported
8	AOC64_SP	READ ONLY - 64-bit AtomicOp Completer Supported
7	AOC32_SP	READ ONLY - 32-bit AtomicOp Completer Supported
6	AOR_SP	READ ONLY AtomicOp Routing Supported
5	ARI_FWD_SP	READ ONLY ARI Forwarding Supported
4	CPL_TIMEOUT_DIS_SUPPORTED	READ ONLY Completion Timeout Disable Supported
3:0	CPL_TIMEOUT_RNG_SUPPORTED	READ ONLY Completion Timeout Ranges Supported

0x1B500098 PCIE20_DEV_CAS_2

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Device Control 2 Register

PCIE20_DEV_CAS_2

Bits	Name	Description
31:10	RSVD	READ ONLY Reserved
9	IDO_CPL_EN	IDO Completion Enable

PCIE20_DEV_CAS_2 (cont.)

Bits	Name	Description
8	IDO_REQ_EN	IDO Request Enable
7	AOP_EG_BLK	AtomicOp Egress Blocking
6	AOP_REQ_EN	AtomicOp Requester Enable
5	ARI_FWD_SP	ARI Forwarding Supported
4	CPL_TIMEOUT_DIS	Completion Timeout Disable
3:0	CPL_TIMEOUT_VALUE	Completion Timeout Values

0x1B50009C PCIE20_LNK_CAP_2

Type: Read
Clock: UNDEFINED
Reset State: 0x00000006

PCIE Link Capabilities 2 Register

PCIE20_LNK_CAP_2

Bits	Name	Description
31:9	RSVD2	READ ONLY Reserved
8	CROSSLINK_SP	READ ONLY Crosslink Supported
7:1	SP_LS_VEC	READ ONLY Supported Link Speeds Vector
0	RSVD1	READ ONLY Reserved

0x1B5000A0 PCIE20_LNK_CAS_2

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000002

Link Control and Status 2 Register

PCIE20_LNK_CAS_2

Bits	Name	Description
31:22	RSVD	READ ONLY Reserved
21	LINK_EQ_REQ	Link Equalization Request
20	EQ_PH3	READ ONLY Equalization Ph3 Success, Gen3 Only
19	EQ_PH2	READ ONLY Equalization Ph2 Success, Gen3 Only
18	EQ_PH1	READ ONLY Equalization Ph1 Success, Gen3 Only
17	EQ_COMPLETE	READ ONLY Equalization Complete, Gen3 Only
16	DEEMPH_LEVEL	READ ONLY Current De-emphasis Level
15:12	COMPL_PRST_DEEPH	Compliance Pre-set/ De-emphasis
11	COMPL_SOS	Compliance SOS
10	ENT_MOD_COMPL	Enter Modified Compliance
9:7	TX_MARGIN	Transmit Margin
6	SEL_DEEMP	READ ONLY Selectable De-emphasize
5	HW_AUTO_SP_DIS	Hardware Autonomous Speed Disable
4	ENTR_COMPL	Enter Compliance
3:0	TRGT_LINK_SPEED	Target Link Speed

0x1B500100 PCIE20_PCIE_EN_CAP

Type: Read
Clock: UNDEFINED
Reset State: 0x00010001

PCIE Express enhanced Cap Header

PCIE20_PCIE_EN_CAP

Bits	Name	Description
31:20	NXT_CAPABILITY_OFFSET	READ ONLY Next Capability Offset

PCIE20_PCIE_EN_CAP (cont.)

Bits	Name	Description
19:16	CAPABILITY_VER	READ ONLY Capability Version
15:0	PCIE_EXTD_CAPID	READ ONLY PCI Express Extended Capability ID, Default value is 0x1 for Advanced Error Reporting

0x1B500104 PCIE20_UN_ERR_ST_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Uncorrectable Error Status Register

PCIE20_UN_ERR_ST_R

Bits	Name	Description
31:25	RESERV4	READ ONLY Reserved
24	AOP_EG_BLK_STATUS	AtomicOp Egress Blocked Status
23:21	RESERV3	READ ONLY Reserved
20	UNS_REQ_ERR_STATUS	Unsupported Req Err Status
19	ECRC_ERR_STATUS	ECRC_Err_Status
18	MALFORMED_TLP_STATUS	Malformed TLP Status
17	RCVR_OVERFLOW_STATUS	Receiver Overflow Status
16	UNX_CPL_STATUS	Unexpected Completion Status
15	CPL_ABORT_STATUS	Cpl_Abort_Status
14	CPL_TIMEOUT_STATUS	Cpl_Timeout_Status
13	FC_PROT_ERR_STATUS	Flow Control Protocol Error Status
12	POISONEDTLP_STATUS	Poisoned TLP Status
11:6	RESERV2	READ ONLY Reserved
5	UNSUPPORTED	READ ONLY Surprise Down Err Status, Not Supported

PCIE20_UN_ERR_ST_R (cont.)

Bits	Name	Description
4	DATALINKPRO_ERR_STATUS	DataLink Protocol Error Status
3:1	RESERV1	READ ONLY Reserved
0	UNDEFINED	READ ONLY Undefined

0x1B500108 PCIE20_UN_ERR_MS_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Uncorrectable Error Mask Register

PCIE20_UN_ERR_MS_R

Bits	Name	Description
31:25	RESERV4	READ ONLY Reserved
24	AOP_EG_BLK_MASK	AtomicOp Egress Blocked Mask
23:21	RESERV3	READ ONLY Reserved
20	UNS_REQ_ERR_MASK	Unsupported Req Err Mask
19	ECRC_ERR_MASK	ECRC_Err_Mask
18	MALFORMED_TLP_MASK	Malformed TLP Mask
17	RCVR_OVERFLOW_MASK	Receiver Overflow Mask
16	UNX_CPL_MASK	Unexpected Completion Mask
15	CPL_ABORT_MASK	Cpl_Abort_Mask
14	CPL_TIMEOUT_MASK	Cpl_Timeout_Mask
13	FC_PROT_ERR_MASK	Flow Control Protocol Error Mask
12	POISONEDTLP_MASK	Poisoned TLP Mask
11:6	RESERV2	READ ONLY Reserved
5	UNSUPPORTED	READ ONLY Surprise Down Err Mask, Not Supported
4	DATALINKPRO_ERR_MASK	DataLink Protocol Error Mask

PCIE20_UN_ERR_MS_R (cont.)

Bits	Name	Description
3:1	RESERV1	READ ONLY Reserved
0	UNDEFIND	READ ONLY Undefined

0x1B50010C PCIE20_UN_ERR_SV_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00462031

Uncorrectable Error Severity Register

PCIE20_UN_ERR_SV_R

Bits	Name	Description
31:25	RESERV4	READ ONLY Reserved
24	AO_EG_ERR_SVT	AtomicOp Egress Blocked Severity
23:21	RESERV3	READ ONLY Reserved
20	UNS_REQ_ERR_SVT	Unsupported Req Err Svt
19	ECRC_ERR_SVT	ECRC_Err_Svt
18	MALFORMED_TLP_SVT	Malformed TLP Severity
17	RCVR_OVERFLOW_SVT	Receiver Overflow Severity
16	UNX_CPL_SVT	Unexpected Completion Severity
15	CPL_ABORT_SVT	Cpl_Abort_Svt
14	CPL_TIMEOUT_SVT	Cpl_Timeout_Svt
13	FC_PROT_ERR_SVT	Flow Control Protocol Error Severity
12	POISONEDTLP_SVT	Poisoned TLP Severity
11:6	RESERV2	READ ONLY Reserved
5	UNSUPPORTED	READ ONLY Surprise Down Err Severity, Not Supported
4	DATALINKPRO_ERR_SVT	DataLink Protocol Error Severity
3:1	RESERV1	READ ONLY Reserved

PCIE20_UN_ERR_SV_R (cont.)

Bits	Name	Description
0	UNDEFIND	READ ONLY Undefined

0x1B500110 PCIE20_CO_ERR_ST_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Correctable Error Status Register

PCIE20_CO_ERR_ST_R

Bits	Name	Description
31:14	RESERV3	READ ONLY Reserved
13	ADV_NONFAT_ERR_STATUS	Advisory Non Fatal Error Status
12	REPLAYTIMER_TIMEOUTSTATUS	Replay Timer Timeout Status
11:9	RESERV2	READ ONLY Reserved
8	REPLAY_NUM_ROLLOVER_STATUS	REPLAY_NUM_ROLLOVER_Status
7	BAD_DLLP_STATUS	Bad DLLP Status
6	BAD_TLP_STATUS	Bad TLP Status
5:1	RESERV1	READ ONLY Reserved
0	RCVR_ERR_STATUS	Receiver Error Status

0x1B500114 PCIE20_CO_ERR_MS_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00002000

Correctable Error Mask Register

PCIE20_CO_ERR_MS_R

Bits	Name	Description
31:14	RESERV3	READ ONLY Reserved
13	ADV_NONFAT_ERR_MASK	Advisory Non Fatal Error MAsk
12	REPLAYTIMER_TIMEOUTMASK	Replay Timer Timeout Mask
11:9	RESERV2	READ ONLY Reserved
8	REPLAY_NUM_ROLLOVER_MASK	REPLAY_NUM_ROLLOVER_MASK
7	BAD_DLLP_MASK	Bad DLLP Mask
6	BAD_TLP_MASK	Bad TLP Mask
5:1	RESERV1	READ ONLY Reserved
0	RCVR_ERR_MASK	Receiver Error Mask

0x1B500118 PCIE20_ADERR_CAP_CR

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x000000A0

Advanced Error Capabilities and Control Register

PCIE20_ADERR_CAP_CR

Bits	Name	Description
31:9	RSVD	READ ONLY Reserved
8	ECRC_CHK_EN	ECRC Check Enable
7	ECRC_CHK_CAP	READ ONLY ECRC Check Capability
6	ECRC_GEN_EN	ECRC Generation Enable
5	ECRC_GEN_CAP	READ ONLY ECRC Generation Capability
4:0	FIRST_ERR_PTR	READ ONLY First Error Pointer

0x1B50011C PCIE20_HD_L_R0

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Header Log Registers 0

PCIE20_HD_L_R0

Bits	Name	Description
31:0	HDR0	READ ONLY Header Log Register 0

0x1B500120 PCIE20_HD_L_R1

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Header Log Registers 1

PCIE20_HD_L_R1

Bits	Name	Description
31:0	HDR1	READ ONLY Header Log Register 1

0x1B500124 PCIE20_HD_L_R2

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Header Log Registers 2

PCIE20_HD_L_R2

Bits	Name	Description
31:0	HDR2	READ ONLY Header Log Register 2

0x1B500128 PCIE20_HD_L_R3

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Header Log Registers 3

PCIE20_HD_L_R3

Bits	Name	Description
31:0	HDR3	READ ONLY Header Log Register 3

0x1B50012C PCIE20_RT_ERR_CMD_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Root Error Command Register

PCIE20_RT_ERR_CMD_R

Bits	Name	Description
31:3	RSVD1	READ ONLY Reserved
2	FT_ERR_RPT_EN	Fatal Error Reporting Enable
1	NFT_ERR_RPT_EN	Non-Fatal Error Reporting Enable
0	COR_ERR_RPT_EN	Correctable Error Reporting Enable

0x1B500130 PCIE20_RT_ERR_STS_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Root Error Status Register

PCIE20_RT_ERR_STS_R

Bits	Name	Description
31:27	ADE_INT_MSG_NUM	READ ONLY Advanced Error Interrupt Message Number

PCIE20_RT_ERR_STS_R (cont.)

Bits	Name	Description
26:7	RSVD1	READ ONLY Reserved
6	FT_MSG_RCVD	Fatal Error Messages Received
5	NFT_MSG_RCVD	Non-Fatal Error Messages Received
4	FST_UNCOR_FT	First Uncorrectable Fatal
3	MULTI_FT_NFT_RCVD	Multiple ERR_FATAL/NONFATAL Received
2	FT_NFT_RCVD	ERR_FATAL/NONFATAL Received
1	MULTI_COR_RCVD	Multiple ERR_COR Received
0	COR_RCVD	ERR_COR Received

0x1B500134 PCIE20_ERR_SRC_ID_R

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Error Source Identification Register

PCIE20_ERR_SRC_ID_R

Bits	Name	Description
31:16	FT_NFT_SRC_ID	READ ONLY ERR_FATAL/NONFATAL Source Identification
15:0	COR_SRC_ID	READ ONLY ERR_COR Source Identification

0x1B500700 PCIE20_LAT_REL_TIM

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x006D0024

Ack Latency and Replay Timer Register

PCIE20_LAT_REL_TIM

Bits	Name	Description
31:16	REPLAY_TIME_LIMIT	The replay timer expires when it reaches this limit. The core initiates a replay upon reception of a Nak or when the replay timer expires. The default value depends on number of bytes (NB) per cycle, which depends on which version of the core you are using (1 = 250 MHz, 2 = 125 MHz). The default is then updated based on the Negotiated Link Width and Max_Payload_Size. Note: If operating at 5 Gb/s, then an additional 153/'CX_NB is added. This is for additional internal processing for received TLPs and transmitted DLLPs.
15:0	LATENCY_TIME_LIMIT	The Ack/Nak latency timer expires when it reaches this limit. The default value depends on number of bytes (NB) per cycle, which depends on which version of the core you are using (1 = 250 MHz, 2 = 125 MHz). The default is then updated based on the Negotiated Link Width and Max_Payload_Size. Note: If operating at 5 Gb/s, then an additional 51/'CX_NB is added. This is for additional internal processing for received TLPs and transmitted DLLPs.

0x1B500704 PCIE20_VENDOR_SPECIFIC_DLLP

Type: Read/Write
Clock: UNDEFINED
Reset State: 0xFFFFFFFF

Vendor Specific DLLP Register

PCIE20_VENDOR_SPECIFIC_DLLP

Bits	Name	Description
31:0	VEN_DLLP_REG	Used to send a specific PCI Express DLLP. The application writes the 8-bit DLLP Type and 24-bits of Payload data into this register, then sets bit 0 of the Port Link Control Register on page 765 to send the DLLP.

0x1B500708 PCIE20_PT_LNK_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x070000DE

Port Force Link Register

PCIE20_PT_LNK_R

Bits	Name	Description
31:24	LOW_POWER_ENTR_CNT	The Power Management state will wait for this many clock cycles for the associated completion of a CfgWr to D-state register to go low-power. This register is intended for applications that do not let the core handle a completion for configuration request to the PMCSCR register. Note: Only used in the DM core (in EP mode), EP core, and the Upstream Port of a Switch.
23:22	RSVD1	READ ONLY Reserved
21:16	LINK_STATE	The Link state that the core will be forced to when bit 15 (Force Link) is set. State encoding is defined in xmlh_ltssm.v.
15	FORCE_LINK	Forces the Link to the state specified by the Link State field. The Force Link pulse will trigger Link re-negotiation. * Reading from this self-clearing register field always returns a 0.
14:8	RSVD0	READ ONLY Reserved
7:0	LINK_NUM	Link Number. Not used for Endpoint

0x1B50070C PCIE20_ACK_FREQ_ASPM

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x1B2C2C00

Ack Frequency and L0-L1 ASPM Control Register

PCIE20_ACK_FREQ_ASPM

Bits	Name	Description
31	RSVD	READ ONLY Reserved
30	L1_ENTR_WO_L0S	Enter ASPM L1 without receive in L0s. Allow core to enter ASPM L1 even when link partner did not go to L0s (receive is not in L0s). When not set, core goes to ASPM L1 only after idle period during which both receive and transmit are in L0s.
29:27	L1_ENTR_LAT	L1 Entrance Latency. Values correspond to: 000: 1 us 001: 2 us 010: 4 us 011: 8 us 100: 16 us 101: 32 us 110 or 111: 64 us
26:24	L0S_ENTR_LAT	L0s Entrance Latency. Values correspond to: 000: 1 us 001: 2 us 010: 3 us - 011: 4 us 100: 5 us 101: 6 us 110 or 111: 7 us

PCIE20_ACK_FREQ_ASPM (cont.)

Bits	Name	Description
23:16	COMMOM_CLK_N_FTS	This is the N_FTS when common clock is used. The number of Fast Training Sequence ordered sets to be transmitted when transitioning from L0s to L0. The maximum number of FTS ordered-sets that a component can request is 255.
15:8	N_FTS	The number of Fast Training Sequence ordered sets to be transmitted when transitioning from L0s to L0. The maximum number of FTS ordered-sets that a component can request is 255. Note: The core does not support a value of zero; a value of zero can cause the LTSSM to go into the recovery state when exiting from L0s.
7:0	ACK_FREQ	Ack Frequency. The core accumulates the number of pending Acks specified here (up to 255) before sending an Ack DLLP See Effect of Link Layer Flow Control and ACK/NAK DLLPs on page 1274 for more details.

0x1B500710 PCIE20_PT_LNK_CTRL_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00070020

Port Link Control Register

PCIE20_PT_LNK_CTRL_R

Bits	Name	Description
31:24	RSVD4	READ ONLY Reserved
23	CROSSLINK_ACT	READ ONLY Crosslink Active
22	CROSSLINK_EN	Crosslink Enable
21:16	LINK_MODE	Link Mode Enable
15:8	RSVD3	READ ONLY Reserved
7	FAST_LINK	Fast Link Mode
6	RSVD2	READ ONLY Reserved
5	DL_EN	DLL Link Enable
4	RSVD1	READ ONLY Reserved
3	RESET_ASSERT	Reset Assert

PCIE20_PT_LNK_CTRL_R (cont.)

Bits	Name	Description
2	LB_EN	Loopback Enable
1	SCRAMBLE_DIS	Scramble Disable
0	VEN_DLLP_REQ	Vendor Specific DLLP Request

0x1B500714 PCIE20_LN_SKW_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Lane Skew Register

PCIE20_LN_SKW_R

Bits	Name	Description
31	DIS_L2L_SKEW	Disable Lane-to-Lane De-skew
30:26	RSVD	READ ONLY Reserved
25	ACKNAK_DIS	Ack/Nak Disable
24	FC_DIS	Flow Control Disable
23:0	LANE_SKEW	Insert Lane Skew for Transmit

0x1B500718 PCIE20_SYMB_N_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00008001

Symbol Number Register

PCIE20_SYMB_N_R

Bits	Name	Description
31:29	RSVD2	READ ONLY Reserved
28:24	FCTIM_INC	Timer Modifier for Flow Control Watchdog Timer
23:19	LATENCY_INC	Timer Modifier for Ack/Nak Latency Timer
18:14	REPLAY_ADJ	Timer Modifier for Replay Timer

PCIE20_SYMB_N_R (cont.)

Bits	Name	Description
13:8	RSVD1	READ ONLY Reserved
7:0	MAX_FUNC	Configuration Requests targeted at function numbers above this value will be returned with UR (unsupported request).

0x1B50071C PCIE20_SYMB_T_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000280

Symbol Timer and Filter Mask Register 1

PCIE20_SYMB_T_R

Bits	Name	Description
31:16	FLT_MSK_1	Mask RADM Filtering and Error Handling Rules: Mask 1
15	DIS_FC_TIM	Disable FC Watchdog Timer
14:11	RSVD	READ ONLY Reserved
10:0	SKP_INT	SKP Interval Value

0x1B500720 PCIE20_FL_MSK_R2

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

Filter Mask Register 2

PCIE20_FL_MSK_R2

Bits	Name	Description
31:0	FLT_MSK_2	Mask RADM Filtering and Error Handling Rules: Mask 2

0x1B500724 PCIE20_OBNP_SUBREQ_CTRL

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000001

AMBA Multiple Outbound Decomposed NP Sub-Requests Control Register

PCIE20_OBNP_SUBREQ_CTRL

Bits	Name	Description
31:1	RSVD	READ ONLY Reserved
0	EN_OBNP_SUBREQ	Enable AMBA Multiple Outbound Decomposed NP Sub-Requests.

0x1B500728 PCIE20_DB_R0

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Debug Register 0

PCIE20_DB_R0

Bits	Name	Description
31:0	DBG_R0	READ ONLY The value on cxpl_debug_info

0x1B50072C PCIE20_DB_R1

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Debug Register 1

PCIE20_DB_R1

Bits	Name	Description
31:0	DBG_R1	READ ONLY The value on cxpl_debug_info[63:32].

0x1B500730 PCIE20_TR_P_STS_R

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Transmit Posted FC Credit Status Register

PCIE20_TR_P_STS_R

Bits	Name	Description
31:20	RSVD	READ ONLY Reserved
19:12	PH_CRDT	READ ONLY Transmit Posted Header FC Credits
11:0	PD_CRDT	READ ONLY Transmit Posted Data FC Credits

0x1B500734 PCIE20_TR_NP_STS_R

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Transmit Non-Posted FC Credit Status Register

PCIE20_TR_NP_STS_R

Bits	Name	Description
31:20	RSVD	READ ONLY Reserved
19:12	NPH_CRDT	READ ONLY Transmit Non-Posted Header FC Credits
11:0	NPD_CRDT	READ ONLY Transmit Non-Posted Data FC Credits

0x1B500738 PCIE20_TR_C_STS_R

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Transmit Completion FC Credit Status Register

PCIE20_TR_C_STS_R

Bits	Name	Description
31:20	RSVD	READ ONLY Reserved
19:12	CPLH_CRDT	READ ONLY Transmit Completion Header FC Credits
11:0	CPLD_CRDT	READ ONLY Transmit Completion Data FC Credits

0x1B50073C PCIE20_Q_STS_R

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

Queue Status Register

PCIE20_Q_STS_R

Bits	Name	Description
31:3	RSVD	READ ONLY Reserved
2	RCVQ_NOT_EMPTY	READ ONLY Received Queue Not Empty
1	RTYB_NOT_EMPTY	READ ONLY Transmit Retry Buffer Not Empty
0	CRDT_NOT_RTRN	READ ONLY Received TLP FC Credits Not Returned

0x1B500740 PCIE20_VC_TR_A_R1

Type: Read
Clock: UNDEFINED
Reset State: 0x0000000F

VC Transmit Arbitration Register 1

PCIE20_VC_TR_A_R1

Bits	Name	Description
31:24	WRR_VC3	READ ONLY WRR Weight for VC3
23:16	WRR_VC2	READ ONLY WRR Weight for VC2
15:8	WRR_VC1	READ ONLY WRR Weight for VC1
7:0	WRR_VC0	READ ONLY WRR Weight for VC0

0x1B500744 PCIE20_VC_TR_A_R2

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

No description provided for this register.

PCIE20_VC_TR_A_R2

Bits	Name	Description
31:24	WRR_VC7	READ ONLY WRR Weight for VC7
23:16	WRR_VC6	READ ONLY WRR Weight for VC6
15:8	WRR_VC5	READ ONLY WRR Weight for VC5
7:0	WRR_VC4	READ ONLY WRR Weight for VC4

0x1B500748 PCIE20_VC0_PR_Q_C

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x0021001E

VC0 Posted Receive Queue Control

PCIE20_VC0_PR_Q_C

Bits	Name	Description
31	CFG_RADM_STRICT_VC_PRIOR	VC Ordering for Receive Queues
30	CFG_RADM_ORDER_RULE	TLP Type Ordering for VC0
29:24	RSVD0	READ ONLY Reserved
23:21	CFG_RADM_PQ_MODE	VC0 Posted TLP Queue Mode
20	RSVD1	READ ONLY Reserved
19:12	CFG_FC_CREDIT_PH	READ ONLY VC0 Posted Header Credits
11:0	CFG_FC_CREDIT_PD	READ ONLY VC0 Posted Data Credits

0x1B50074C PCIE20_VC0_NPR_Q_C

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00210007

VC0 Non-Posted Receive Queue Control

PCIE20_VC0_NPR_Q_C

Bits	Name	Description
31:24	RSVD0	READ ONLY Reserved
23:21	CFG_RADM_NPQ_MODE	VC0 Non-Posted TLP Queue Mode
20	RSVD1	READ ONLY Reserved
19:12	CFG_FC_CREDIT_NPH	READ ONLY VC0 Non-Posted Header Credits
11:0	CFG_FC_CREDIT_NPD	READ ONLY VC0 Non-Posted Data Credits

0x1B500750 PCIE20_VC0_CR_Q_C

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00800000

VC0 Completion Receive Queue Control

PCIE20_VC0_CR_Q_C

Bits	Name	Description
31:24	RSVD0	READ ONLY Reserved
23:21	CFG_RADM_CPLQ_MODE	VC0 Completion TLP Queue Mode
20	RSVD1	READ ONLY Reserved
19:12	CFG_FC_CREDIT_CPLH	READ ONLY VC0 Completion Header Credits
11:0	CFG_FC_CREDIT_CPLD	READ ONLY VC0 Completion Data Credits

0x1B5007A8 PCIE20_VC0_PB_D

Type: Read
Clock: UNDEFINED
Reset State: 0x0011003D

VC0 Posted Buffer Depth

PCIE20_VC0_PB_D

Bits	Name	Description
31:26	RSVD0	READ ONLY Reserved
25:16	CFG_PHQ_DEPTHS	READ ONLY VC0 Posted Header Queue Depth
15:14	RSVD1	READ ONLY Reserved
13:0	CFG_PDQ_DEPTHS	READ ONLY VC0 Posted Data Queue Depth

0x1B5007AC PCIE20_VC0_NPB_D

Type: Read
Clock: UNDEFINED
Reset State: 0x0011000F

VC0 Non-Posted Buffer Depth

PCIE20_VC0_NPB_D

Bits	Name	Description
31:26	RSVD0	READ ONLY Reserved
25:16	CFG_NPHQ_DEPTHS	READ ONLY VC0 Non-Posted Header Queue Depth
15:14	RSVD1	READ ONLY Reserved
13:0	CFG_NPDQ_DEPTHS	READ ONLY VC0 Non-Posted Data Queue Depth

0x1B5007B0 PCIE20_VC0_CB_D

Type: Read
Clock: UNDEFINED
Reset State: 0x00030003

VC0 Completion Buffer Depth

PCIE20_VC0_CB_D

Bits	Name	Description
31:26	RSVD0	READ ONLY Reserved
25:16	CFG_CPLHQ_DEPTHS	READ ONLY VC0 Completion Header Queue Depth
15:14	RSVD1	READ ONLY Reserved
13:0	CFG_CPLDQ_DEPTHS	READ ONLY VC0 Completion Data Queue Depth

0x1B50080C PCIE20_GEN2

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x0002042C

Gen2 Related

PCIE20_GEN2

Bits	Name	Description
31:21	RSVD	READ ONLY Reserved
20	CFG_UP_SEL_DEEMPH	Used to set the de-emphasis level for Upstream Ports
19	CFG_TX_COMPLIANCE_RCV	Config Tx Compliance Receive Bit
18	CFG_PHY_TXSWING	Config PHY Tx Swing
17	CFG_DIRECTED_SPEED_CHANGE	Directed Speed Change
16:8	CFG_LANE_EN	Predetermined Number of Lanes
7:0	CFG_GEN2_N_FTS	Number of Fast Training Sequences

0x1B500810 PCIE20_PHY_STS_R

Type: Read
Clock: UNDEFINED
Reset State: 0x00000000

PHY Status Register

PCIE20_PHY_STS_R

Bits	Name	Description
31:0	PHY_STS	READ ONLY PHY Status

0x1B500814 PCIE20_PHY_CTRL_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

PHY Control Register

PCIE20_PHY_CTRL_R

Bits	Name	Description
31:0	PHY_CTRL	PHY Control

0x1B500818 PCIE20_AXI_MSTR_RESP_COMP_CTRL0

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000105

AXI Master Response Composer Control Register 0

PCIE20_AXI_MSTR_RESP_COMP_CTRL0

Bits	Name	Description
31:16	RSVD	READ ONLY Reserved
15:8	CFG_REMOTE_MAX_BRIDGE_TAG	READ ONLY Remote Max Bridge Tag
7:3	RSVD0	READ ONLY Reserved
2:0	CFG_REMOTE_RD_REQ_BRIDGE_SIZE	Remote Max Bridge Tag

0x1B50081C PCIE20_AXI_MSTR_RESP_COMP_CTRL1

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

AXI Master Response Composer Control Register 1

PCIE20_AXI_MSTR_RESP_COMP_CTRL1

Bits	Name	Description
31:1	RSVD	READ ONLY Reserved
0	CFG_BRIDGE_SB_INIT	Resize Master Response Composer

0x1B500900 PCIE20_IATU_VIEWPORT_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

iATU Viewport Register

PCIE20_IATU_VIEWPORT_R

Bits	Name	Description
31	ATU_REG_N_IS_IN	Region Direction
30:4	RSVD1	READ ONLY Reserved
3:0	ATU_REG_N	Region Index

0x1B500904 PCIE20_IATU_CTRL1_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

iATU Region Control 1 Register

PCIE20_IATU_CTRL1_R

Bits	Name	Description
31:23	RSVD1	READ ONLY Reserved
22:20	ATU_REG_FUNC_NUM	Function Number
19:16	RSVD2	READ ONLY Reserved
15:11	RSVD3	READ ONLY Reserved
10:9	ATU_REG_ATTR	ATTR
8	ATU_REG_TD	TD
7:5	ATU_REG_TC	TC
4:0	ATU_REG_TYPE	TYPE

0x1B500908 PCIE20_IATU_CTRL2_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

iATU Region Control 2 Register

PCIE20_IATU_CTRL2_R

Bits	Name	Description
31	ATU_REG_EN	Region Enable
30	ATU_REG_BAR_MATCH	Match Mode
29	ATU_REG_INVERT	Invert Mode
28	ATU_REG_SHIFT	CFG Shift Mode
27	ATU_REG_FUZZY	Fuzzy Type Match Mode
26	RSVD1	READ ONLY Reserved
25:24	ATU_REG_RSP_CODE	Response Code
23:22	RSVD2	READ ONLY Reserved
21	ATU_REG_MSGCODE_MATCH_EN	Message Code Match Enable
20	RSVD3	READ ONLY Reserved
19	ATU_REG_FUNC_MATCH_EN	Function Number Match Enable
18:17	RSVD4	READ ONLY Reserved
16	ATU_REG_ATTR_MATCH_EN	ATTR Match Enable
15	ATU_REG_TD_MATCH_EN	TD Match Enable
14	ATU_REG_TC_MATCH_EN	TC Match Enable
13:11	RSVD5	READ ONLY Reserved
10:8	ATU_REG_BAR_NUM	BAR Number
7:0	ATU_REG_MSG_CODE	Message Code

0x1B50090C PCIE20_IATU_LBA_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

iATU Region Lower Base Address Register

PCIE20_IATU_LBA_R

Bits	Name	Description
31:12	ATU_REG_LWR_BASE_PART1	iATU Lower Base Address to be translated
11:0	ATU_REG_LWR_BASE_PART2	READ ONLY iATU Lower Base Address to be translated and hard wired to all 0

0x1B500910 PCIE20_IATU_UBA_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

iATU Region Upper Base Address Register

PCIE20_IATU_UBA_R

Bits	Name	Description
31:0	ATU_REG_UPR_BASE	iATU Upper Base Address

0x1B500914 PCIE20_IATU_LA_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000FFF

iATU Region Limited Address Register

PCIE20_IATU_LA_R

Bits	Name	Description
31:12	ATU_REG_LIMIT_PART1	iATU Limited Address to be translated
11:0	ATU_REG_LIMIT_PART2	READ ONLY iATU Limited Address to be translated and hard wired to all 1

0x1B500918 PCIE20_IATU_LTA_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

iATU Region Lower Target Address Register

PCIE20_IATU_LTA_R

Bits	Name	Description
31:12	ATU_REG_LWR_TRGT_PART1	iATU Lower Target Address
11:0	ATU_REG_LWR_TRGT_PART2	READ ONLY iATU Lower Target Address and hard wired to all 0

0x1B50091C PCIE20_IATU_UTA_R

Type: Read/Write
Clock: UNDEFINED
Reset State: 0x00000000

iATU Region Upper Target Address Register

PCIE20_IATU_UTA_R

Bits	Name	Description
31:0	ATU_REG_UPR_TRGT	iATU Upper Target Address

15.3 PCIE20 ELBI Registers (0x1B502000 PCIE20_ELBI_BASE)

This section contains the description for the External Local Bus Interface (ELBI) Registers added to the Synopsys PCIe2.0 Controller.

The Registers are accessed through a dedicated Configuration AXI Slave port called DBI. It is the same port used to access the Synopsys Controller PCIe registers too.

ELBI Registers support only DWord (4 byte) aligned writes and reads on the Configuration Bus interface.

15.3.1 PCIE20 control registers

PCIE20 ELBI Control registers configure the operational state, SW reset, interrupts and others.

The ELBI register file is clock by core_clock but the accesses to it are made through dbi_clk.

0x1B502000 PCIE20_ELBI_VERSION

Type: Read
Clock: DBI_CLK
Reset State: 0X01002107

PCIe 2.0 version register reflects the core version and hardware development stages (P/Q/R).

The APQ8064 1.0 release is using the pcie20_avenger_p3q1r9 tag, which shows up as p2q1r7 in this register.

PCIE20_ELBI_VERSION

Bits	Name	Description
31:24	MAJOR_VER	Major Version 0x1: APQ8064
23:16	MINOR_VER	Minor Version
15:12	P_INDEX	Hardware development P index
11:8	Q_INDEX	Hardware development Q index
7:0	R_INDEX	Hardware development R index

0x1B502004 PCIE20_ELBI_SYS_CTRL

Type: Read/Write
Clock: DBI_CLK
Reset State: 0X00000000

PCIE20 System Control register.

PCIE20_ELBI_SYS_CTRL

Bits	Name	Description
31:7	RESERVED_31_7	Reserved
6	INIT_RST	Write '1' to pulse ‘app_init_rst’ to the controller, causing a Hot Reset of the downstream device. Writing '0' has no effect. Reading returns '0'.
5	UNLOCK_MSG	Write '1' to pulse ‘app_unlock_msg’ to the controller, causing an unlock message on the PCIe link Writing '0' has no effect. Reading returns '0'.
4	PME_TURNOFF_MSG	Write '1' to pulse ‘apps_pm_xmt_turnoff’ to the controller, causing a PME_Turnoff message on the PCIe link. Writing '0' has no effect. Reading returns '0'.
3:1	RESERVED_3_1	Reserved
0	LTSSM_EN	Enable/Disable the Link Training State Machine (LTSSM) in the controller core. See ‘app_ltssm_enable’ in the controller data book. This bit is important to be enabled to start the controller and is part of the power up sequence. 0x0: LTSSM disabled 0x1: LTSSM enabled

0x1B502008 PCIE20_ELBI_SYS_STTS

Type: Read
Clock: DBI_CLK
Reset State: 0X00000000

PCIE20 Status register.

PCIE20_ELBI_SYS_STTS

Bits	Name	Description
31:21	RESERVED_31_21	Reserved
20:18	PM_CURNT_STATE	Reflects the ‘pm_curnt_state’ signal.
17:12	XMLH_LTSSM_STATE	Reflects the ‘xmlh_ltssm_state’ signal.
11	XMLH_IN_RL0S	Reflects the ‘xmlh_in_rl0s’ signal.
10	XMLH_LINK_UP	Reflects the ‘xmlh_link_up’ signal.
9	CFG_HW_AUTO_SP_DIS	Reflects the ‘cfg_hw_auto_sp_dis’ signal.
8	CPL_TIMEOUT	Indication of a PCIe completion timeout, (by ‘radm_cpl_timeout’ signal). Note: registered bit. Has to be cleared using PCIE20_ELBI_SYS_CLR register.

PCIE20_ELBI_SYS_STTS (cont.)

Bits	Name	Description
7:6	RESERVED_7_6	Reserved
5	GM_RSP_CMPSR_ERR	Error indicated by ;gm_cmposer_lookup_err' signal. This error is considered fatal and should never happen. Note: registered bit. Has to be cleared using PCIE20_ELBI_SYS_CLR register.
4	RADMX_RSP_CMPSR_ERR	Error indicated by ;radmx_cmposer_lookup_err' signal. This error is considered fatal and should never happen. Note: registered bit. Has to be cleared using PCIE20_ELBI_SYS_CLR register
3	RESERVED_3	Reserved
2	BLK_TLP	Power Management Indication to the Application to stop scheduling new TLPs (transactions). See 'pm_xtlh_block_tlp' signal in Synopsys databook for more info.
1	PME_TO_ACK	This bit indicates that a PME_TO_Ack Message received by the core. See 'radm_pm_to_ack' signal in the Synopsys databook. Note: registered bit. Has to be cleared using PCIE20_ELBI_SYS_CLR register
0	LINK_REQ_RST_NOT	This indicates the core is requesting a reset due to link down. See 'link_req_rst_not' signal in controller data book. 0x1: Active 0x0: Core Requesting Reset

0x1B50200C PCIE20_ELBI_SYS_CLR

Type: Write
Clock: DBI_CLK
Reset State: 0X00000000

PCIE20 Clear register. This is Write only register, thus reads always return a zero

PCIE20_ELBI_SYS_CLR

Bits	Name	Description
31:9	RESERVED_31_9	Reserved
8	CPL_TIMEOUT	Write '1' to clears CPL_TIMEOUT status bit Writing '0' has no effect. Reading returns '0'.
7:6	RESERVED_7_6	Reserved
5	GM_RSP_CMPSR_ERR	Write '1' to clears GM_RSP_CMPSR_ERR status bit Writing '0' has no effect. Reading returns '0'.

PCIE20_ELBI_SYS_CLR (cont.)

Bits	Name	Description
4	RADMX_RSP_CMPSR_ERR	Write '1' to clears RADMX_RSP_CMPSR_ERR status bit Writing '0' has no effect. Reading returns '0'.
3:2	RESERVED_3_2	Reserved
1	PME_TO_ACK	Writing 0x1 to this bit clears the PME_TO_Ack Message received indication in the PCIE20_ELBI_SYS_CLR register.
0	RESERVED_0	Reserved

0x1B502020 PCIE20_ELBI_TESTBUS_CTRL

Type: Read/Write
Clock: DBI_CLK
Reset State: 0X00000000

PCIE20 Testbus control register.

PCIE20_ELBI_TESTBUS_CTRL

Bits	Name	Description
31:3	RESERVED_31_3	Reserved
2:0	DIAG_CTRL_BUS	Bits driving the ‘diag_ctrl_bus[2:0]’ signal to the controller. See Data Book for details

0x1B502030+4*n PCIE20_ELBI_DEBUG_INFO_n, n=[0..1]

Type: Read
Clock: DBI_CLK
Reset State: 0X00000000

PCIE20 debug bus status register (cxpl_debug_info).

PCIE20_ELBI_DEBUG_INFO_n

Bits	Name	Description
31:0	BUS	bits [32*n+31:32*n] of the ‘cxpl_debug_info’ signal.

0x1B502040+4*n PCIE20_ELBI_TB_DIAG_n, n=[0..17]

Type: Read
Clock: DBI_CLK
Reset State: 0X00000000

PCIE20 diagnostics bus status register (diag_status_bus).

PCIE20_ELBI_TB_DIAG_n

Bits	Name	Description
31:0	BUS	bits [32*(n+1)-1:32*n] of the ‘diag_status_bus’ signal.

15.4 PCIE20 PARF Registers (0x1B600000 PCIE20_PARF_BASE)

This section contains the description for the PCIe Auxiliary Register File (PARF) Registers added to the Synopsys PCIe2.0 Controller.

The Registers are accessed through a dedicated Configuration AHB Slave port.

PARF Registers support only DWord (4 byte) aligned writes and reads on the PARF Bus interface.

PCIE20 Auxiliary Register File (PARF) registers configure the PHY, PCS and Controller parameter values.

The PARF is clocked separately from the PCIe 2.0 core and is available even when core_clk is turned off or not available, thus allowing configuration of the various parameters while holding the PHY and/or Controller in reset.

0x1B600000 PCIE20_PARF_SYS_CTRL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0X00000000

PCIE20 System Control register.

PCIE20_PARF_SYS_CTRL

Bits	Name	Description
31:24	RESERVED_31_24	Reserved

PCIE20_PARF_SYS_CTRL (cont.)

Bits	Name	Description
23:16	TESTBUS_SELECTOR	Test bus selector chooses different chunks of the two testbuses provided by the Synopsys core, check the Controller databook for description of cxpl_debug_info' & diag_status_bus. x14 : {20'h0 , diag_status_bus[32*(17+1)-21: 32*17]} 0x0: None (Zero) 0x1: cxpl_debug_info[31:0] 0x2: cxpl_debug_info[63:32] 0x3: diag_status_bus[32*_1 (0+1-1 : 32* 0]) 0x4: diag_status_bus[32*_2 (1+1-1 : 32* 1]) 0x5: diag_status_bus[32*_3 (2+1-1 : 32* 2]) 0x6: diag_status_bus[32*_4 (3+1-1 : 32* 3]) 0x7: diag_status_bus[32*_5 (4+1-1 : 32* 4]) 0x0: diag_status_bus[32*_6 (5+1-1 : 32* 5]) 0x0: diag_status_bus[32*_7 (6+1-1 : 32* 6]) 0x0: diag_status_bus[32*_8 (7+1-1 : 32* 7]) 0x0: diag_status_bus[32*_9 (8+1-1 : 32* 8]) 0x0: diag_status_bus[32*_10 (9+1-1 : 32* 9]) 0x0: diag_status_bus[32*_11 (10+1-1 : 32*10]) 0x0: diag_status_bus[32*_12 (11+1-1 : 32*11]) 0x0: diag_status_bus[32*_13 (12+1-1 : 32*12]) 0x8: diag_status_bus[32*_14 (13+1-1 : 32*13]) 0x9: diag_status_bus[32*_15 (14+1-1 : 32*14]) 0xA: diag_status_bus[32*_16 (15+1-1 : 32*15]) 0xB: diag_status_bus[32*_17 (16+1-1 : 32*16])
15	RESERVED_15	Reserved
14	PHY_P2_IN_L1_DIS	Do not Enter P2 when in L1 state. Enabling this bit shortens L1 exit latency but consumes more power in L1 state. This is only relevant when using the CLK_RST module. This bit may be changed only when the controller is in reset. 0x1: Disable P2 when in L1 0x0: Enable P2 when in L1
13	MST_WAKEUP_EN	Enable Master Access avoiding the core from L1. This is required to be Enabled when using L1 Clock Removal or placing PHY in P2 while in L1. Leaving this disabled while power conserving functions enabled, may result in incorrect behavior. When Enabled, the core will not enter L1 state if a Master access is attempted. This is only relevant when using the CLK_RST module. This bit may be changed only when the controller is in reset. 0x1: Enable Master Wakeup 0x0: Disable Master Wakeup

PCIE20_PARF_SYS_CTRL (cont.)

Bits	Name	Description
12	SLV_WAKEUP_EN	Enable Slave Access waking the core out of L1. This is required to be Enabled when using L1 Clock Removal or placing PHY in P2 while in L1. Leaving this disabled during power conserving functions enabled, may result in a stuck access to the Core. When Enabled, the core will exit L1 state if a Slave access is attempted. This is only relevant when using the CLK_RST module. This bit may be changed only when the controller is in reset. 0x1: Enable SLV Wakeup 0x0: Disable SLV Wakeup
11	DBI_WAKEUP_EN	Enable DBI Config Access waking the core out of L1. This is required to be Enabled when using L1 Clock Removal or placing PHY in P2 while in L1. Leaving this disabled during power conserving functions enabled, may result in a stuck config access to the Core. When Enabled, the core will exit L1 state if a DBI Config access is attempted. This is only relevant when using the CLK_RST module. This bit may be changed only when the controller is in reset. 0x1: Enable DBI Wakeup 0x0: Disable DBI Wakeup
10:9	RESERVED_10_9	Reserved
8	ACLK_REQ_OVERRIDE	Override the HW generated ACLK Request value by the SW generated ACLK_REQ value in this register. This feature was removed in APQ8064. 0x1: Override HW value 0x0: Use HW value
7	ACLK_REQ	SW generated ACLK Request value. May be used to override the HW value. This feature was removed in APQ8064. 0x1: ACLK Requested 0x0: ACLK Not Requested
6	CORE_CLK_CGC_DIS	Disable the Core clock CGC that gates Pipe clock from propagating to Core clock. This is only relevant when using the CLK_RST module. This bit may be changed only when the controller is in reset. 0x1: Disable CGC 0x0: CGC Enabled
5	AUX_CLK_MUX_DIS	Disable the AUX Clock Mux that chooses Chip Sleep clock instead of Pipe Clock. This is only relevant when using the CLK_RST module. This bit may be changed only when the controller is in reset. 0x1: Disable Mux 0x0: Mux Enabled

PCIE20_PARF_SYS_CTRL (cont.)

Bits	Name	Description
4	AUX_PWR_DET	Controls the 'sys_aux_pwr_det' signal to the controller core. See 'sys_aux_pwr_det' in Synopsys data book. This bit may be changed only when the controller is in reset. 0x0: Auxiliary power is off 0x1: Auxiliary power is on
3	AUX_CLK_DIS	Disable Aux Clock usage. Enabling this bit will prevent using Aux (Sleep) clock when in L0s, L1, L2 states. This is only relevant when using the CLK_RST module. This bit may be changed only when the controller is in reset. 0x1: Disable Aux Clock 0x0: Use Aux Clock
2	L23_CLK_RMV_DIS	Do not Gate off the Pipe clock and replace it with Aux (Sleep) Clock. Enabling this bit leaves the Pipe clock always active and thus consumes more power in L23 states. This is only relevant when using the CLK_RST module. This bit may be changed only when the controller is in reset. 0x1: Disable Clock Removal 0x0: Enable Clock Removal
1	L1_CLK_RMV_DIS	Do not Gate off the Pipe clock and replace it with Aux (Sleep) Clock. Enabling this bit leaves the Pipe clock always active and thus consumes more power in L0s & L1 states. This is only relevant when using the CLK_RST module. This bit may be changed only when the controller is in reset. 0x1: Disable Clock Removal 0x0: Enable Clock Removal
0	CLK_RST_MDL_EN	Enable Clock Reset Module. Enabling this causes Pcie 2.0 to use Clocks and Resets (CLK_RST) module. When not using the Clocks and Resets module, the SW is responsible to provide PHY Reset indications from the Chip Clock Controller. Otherwise it will be provided by the Pcie 2.0 controller to the PHY. When not using the Clocks and Resets module, the Pcie 2.0 module does not use the Aux (Sleep) clock from the chip, does not gate the Pipe clock during L0s, L1, L2 states and does not put the PHY in P2 while in L1. If Clocks and Resets module is used, other bits in this register may be of additional interest. Changing this bit is only allowed while PCIe PHY, PCIe Core and PCIe Power Resets are asserted by the Chip Clock Controller module. 0x1: Enable Clocks Resets 0x0: Disable Clocks Resets

0x1B600004 PCIE20_PARF_PHY_LATENCY

Type: Read/Write
Clock: AHB_CLK
Reset State: 0X00000006

PCIE20 PHY Latency for transmitting ELECIDLE prior to resetting the core by the clk_rst module. This is used by the CLK_RST module after a link down event.

This register may be set only when the controller is in reset.

PCIE20_PARF_PHY_LATENCY

Bits	Name	Description
31:8	RESERVED_31_8	Reserved
7:0	PHY_LATENCY	PHY Latency Value

0x1B600008 PCIE20_PARF_BRIDGE_ERR_MAP

Type: Read/Write
Clock: AHB_CLK
Reset State: 0X00000000

PCIE20 AXI Error mapping configuration.

This register may be set only when the controller is in reset.

PCIE20_PARF_BRIDGE_ERR_MAP

Bits	Name	Description
31:18	RESERVED_31_18	Reserved
17:16	AXI_MSTR_ERR_MAP	AXI master error mapping (AXI error responses to PCIe error completions). See 'mstr_resp_err_map' description in controller data book.
15:6	RESERVED_15_6	Reserved
5:0	AXI_SLV_ERR_MAP	AXI slave error mapping (PCIe error completions to AXI error responses). See 'slv_resp_err_map' description in controller data book.

0x1B600010 PCIE20_PARF_DB_CTRL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0X00000000

PCIe 2.0 presence detect debouncer control register. This register also controls the hysteresis counters for the Master, Slave and DBI access wakeup from L1 mechanism.

PCIE20_PARF_DB_CTRL

Bits	Name	Description
31:7	RESERVED_31_7	Reserved
6	MST_WKP_BLOCK	Enable/Disable debouncing on Master wakeup de-assertion. Blocking eventually ignores the debouncer delay and allows immediate removal detection. This bit may be changed only when the controller is in reset. 0x1: blocked 0x0: passed
5	SLV_WKP_BLOCK	Enable/Disable debouncing on Slave wakeup de-assertion. Blocking eventually ignores the debouncer delay and allows immediate removal detection. This bit may be changed only when the controller is in reset. 0x1: blocked 0x0: passed
4	DBI_WKP_BLOCK	Enable/Disable debouncing on DBI wakeup de-assertion. Blocking eventually ignores the debouncer delay and allows immediate removal detection. This bit may be changed only when the controller is in reset. 0x1: blocked 0x0: passed
3:2	RESERVED_3_2	Reserved
1	RMVL_DBNCR_BLOCK	Enable/Disable debouncing on card removal. Blocking eventually ignores the debouncer delay and allows immediate removal detection. 0x1: blocked 0x0: passed
0	INSR_DBNCR_BLOCK	Enable/Disable debouncing on card insertion. Blocking eventually ignores the debouncer delay and allows immediate insertion detection. 0x1: blocked 0x0: passed

0x1B600014 PCIE20_PARF_PREDET_DB_INSR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0X00010000

PCIe 2.0 presence detect debouncer counter for card-insertion events.

This register may be set only when the controller is in reset.

PCIE20_PARF_PREDET_DB_INSR

Bits	Name	Description
31:0	INSR_DBNCR_VAL	Debouncing value for card insertion: presence detect assertion is passed to controller only after this number clock cycles

0x1B600018 PCIE20_PARF_PREDET_DB_RMVL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0X00010000

PCIe 2.0 presence detect debouncer counter for card-removal events.

This register may be set only when the controller is in reset.

PCIE20_PARF_PREDET_DB_RMVL

Bits	Name	Description
31:0	RMVL_DBNCR_VAL	Debouncing value for card removal: presence detect de-assertion is passed to controller only after this number clock cycles

0x1B60001C PCIE20_PARF_WKP_DB_RMVL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0X00101010

PCIe 2.0 Hysteresis counter values for de-assertion of Exit L1 Requests as a result of a bus access taking place.

This register may be set only when the controller is in reset.

PCIE20_PARF_WKP_DB_RMVL

Bits	Name	Description
31:24	RESERVED_31_24	Reserved
23:16	MST_DBNCR_VAL	Hysteresis counter value for Exit L1 Request de-assertion after a Master access
15:8	SLV_DBNCR_VAL	Hysteresis counter value for Exit L1 Request de-assertion after a Slave access
7:0	DBI_DBNCR_VAL	Hysteresis counter value for Exit L1 Request de-assertion after a DBI access

0x1B600020 PCIE20_PARF_PM_CTRL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0X00000000

PCIE20 Power Management Control register.

PCIE20_PARF_PM_CTRL

Bits	Name	Description
31:3	RESERVED_31_3	Reserved
2	READY_ENTR_L23	Application indication that system is ready to enter L2/L3 power states. Check 'app_ready_entr_l23' signal in the controller databook. 0x0: not ready 0x1: ready
1	REQ_EXIT_L1	Application request to the controller to exit L1 power state. Check 'app_req_exit_l1' signal in the controller databook. 0x0: De-assert Exit Request 0x1: Assert Exit Request
0	REQ_ENTR_L1	Application request to the controller to enter L1 power state. Check 'app_req_entr_l1' signal in the controller databook. 0x0: De-assert Enter Request 0x1: Assert Enter Request

0x1B600024 PCIE20_PARF_PM_STTS

Type: Read
Clock: AHB_CLK
Reset State: 0X00000000

PCIE20 Power Management Status register.

PCIE20_PARF_PM_STTS

Bits	Name	Description
31:8	RESERVED_31_8	Reserved
7	PM_LINKST_L2_EXIT	Reflects 'pm_linkst_l2_exit' indication from the Power Management controller. See controller databook for more info
6	PM_LINKST_IN_L2	Reflects 'pm_linkst_in_l2' indication from the Power Management controller. See controller databook for more info

PCIE20_PARF_PM_STTS (cont.)

Bits	Name	Description
5	PM_LINKST_IN_L1	Reflects 'pm_linkst_in_l1' indication from the Power Management controller. See controller databook for more info
4	PM_PME_EN	Reflects 'pm_pme_en' indication from the Power Management controller. See controller databook for more info
3	PM_STATUS	Reflects 'pm_status' indication from the Power Management controller. See controller databook for more info
2:0	PM_DSTATE	Reflects 'pm_dstate' indication from the Power Management controller. See controller databook for more info.

0x1B600030 PCIE20_PARF_PCS_CTRL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x00000000

PCIE20 PCS Control register.

PCIE20_PARF_PCS_CTRL

Bits	Name	Description
31:2	RESERVED_31_2	Reserved
1	TX2RX_LOOPBACK_EN	Force the PHY into TX2RX loopback state. Data from the transmit pre-driver is looped back to the receive slicers. This bit may be changed only when the controller & PHY are in reset. 0x0: Normal mode 0x1: TX2RX loopback
0	COMMON_CLOCKS	When asserted, indicates that the controller requires the reference clock to remain active. see 'pcs_common_clocks' in the phy databook. This bit may be changed only when the controller and PHY are in reset.

0x1B600034 PCIE20_PARF_PCS_DEEMPH

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x00151520

PCIE20 PCS De-emphasis control register.

This register may be set only when the controller and PHY are in reset.

PCIE20_PARF_PCS_DEEMPH

Bits	Name	Description
31:22	RESERVED_31_22	Reserved
21:16	TX_DEEMPH_GEN1	Sets the Tx driver de-emphasis value in the case where 'pipe0_tx_deemph' is set to 0x1, and the PHY is running at Gen1 rate. See PHY data book.
15:14	RESERVED_15_14	Reserved
13:8	TX_DEEMPH_GEN2_3_5DB	Sets the Tx driver de-emphasis value in the case where 'pipe0_tx_deemph' is set to 0x1, and the PHY is running at Gen2 rate. See PHY data book.
7:6	RESERVED_7_6	Reserved
5:0	TX_DEEMPH_GEN2_6DB	Sets the Tx driver de-emphasis value in the case where 'pipe0_tx_deemph' is set to 0x0, and the PHY is running at Gen2 rate. See PHY data book.

0x1B600038 PCIE20_PARF_PCS_SWING

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x00007979

PCIE20 PCS voltage swing control register.

This register may be set only when the controller and PHY are in reset.

PCIE20_PARF_PCS_SWING

Bits	Name	Description
31:15	RESERVED_31_15	Reserved
14:8	TX_SWING_FULL	Sets the TX launch amplitude when 'pipe0_tx_swing' is set to 0x0 (default state). See PHY data book.
7	RESERVED_7	Reserved
6:0	TX_SWING_LOW	Sets the TX launch amplitude when 'pipe0_tx_swing' is set to 0x1 (low-swing state). See PHY data book.

0x1B600040 PCIE20_PARF_PHY_CTRL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0X00000900

PCIE20 PHY control register.

his register may be set only when the controller and PHY are in reset.

PCIE20_PARF_PHY_CTRL

Bits	Name	Description
31:21	RESERVED_31_21	Reserved
20:16	PHY_TX0_TERM_OFFST	Transmitter Termination Offset See 'phy_tx0_term_offset' in PHY data book.
15:13	RESERVED_15_13	Reserved
12:8	PHY_LOS_LEVEL	Loss-of-Signal Detector Sensitivity Level Control. See 'phy_los_level' PHY data book.
7:5	RESERVED_7_5	Reserved
4	PHY_RTUNE_REQ	Write 0x1 to trigger a resistor tune request. See 'phy_rtune_req' in PHY data book.
3	RESERVED_3	Reserved
2	PHY_TEST_BURNIN	Drives PHY reserved pin 'phy_test_burnin'
1	PHY_TEST_BYPASS	Drives PHY reserved pin 'phy_test_bypass'
0	PHY_TEST_PWR_DOWN	Force the entire PHY into its lowest power state by turning everything completely off. This is used to conserve power. See 'phy_test_powerdown' in PHY data book. 0x0: PHY power on 0x1: PHY power-down

0x1B600044 PCIE20_PARF_PHY_STTS

Type: Read
Clock: AHB_CLK
Reset State: 0X00000000

PCIE20 PHY control register.

PCIE20_PARF_PHY_STTS

Bits	Name	Description
31:5	RESERVED_31_5	RESERVED

PCIE20_PARF_PHY_STTS (cont.)

Bits	Name	Description
4	PHY_RTUNE_ACK	While asserted high, Resistor calibration is in process. See 'phy_rtune_ack' in PHY data book. SW is responsible to read this bit twice for detecting the correct value, since this bit is a level signal which is not synchronized to AHB clock domain. The reason there is no sychronization is that there's no AHB clock available most of the time.
3:0	RESERVED_3_0	RESERVED

0x1B60004C PCIE20_PARF_PHY_REFCLK

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0001019

PCIE20 PHY reference clock control register.

his register may be set only when the controller and PHY are in reset.

PCIE20_PARF_PHY_REFCLK

Bits	Name	Description
31:17	RESERVED_31_17	Reserved
16	REF_SSP_EN	Indicates to PHY that external reference clock is stable and ready for use. This bit must be enabled in order to use the controller and is described in the power up sequence. See 'phy_ref_ssp_en' in PHY data book. 0x1: Refclk stable 0x0: No Refclk
15:13	RESERVED_15_13	Reserved
12	REF_USE_PAD	Chooses the source for the reference clock for the PHY. See 'phy_ref_use_pad' in PHY databook. 0x1: Refclk from pad 0x0: Refclk from alt
11:9	RESERVED_11_9	Reserved
8	REFCLK_DIV2	Divides the reference clock frequency by 2, when higher than 100 MHz. See 'phy_ref_clkdiv2' in PHY data book. 0x1: divide refclk 0x0: don't divide
7	RESERVED_7	Reserved

PCIE20_PARF_PHY_REFCLK (cont.)

Bits	Name	Description
6:0	MPLL_MULTIPLIER	Multiplies the reference clock to a frequency suitable for intended operating speed. See 'phy_mpll_multiplier' in PHY data book.

0x1B600050 PCIE20_PARF_CONFIG_BITS

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x00000000

PCIE20 Config Bits.

PCIE20_PARF_CONFIG_BITS

Bits	Name	Description
31:27	BITS31_27	Reserved For Configuration Bits
26:24	PHY_RX0_EQ	This field controls the value of PHY_RX0_EQ to the PHY
23:0	BITS23_0	Reserved For Configuration Bits

16 RIVA Registers

16.1 Overview

Table 16-1 RIVA Bases

Base Name	Parent	Address
RIVA_BASE2	RIVA_BASE	0x03000000

16.2 RIVA Registers (0x03100000 RIVA_BASE)

This section contains RIVA registers.

16.2.1 A2XB Registers

0x3000000 A2XB_A2XB_CFG

Type: read-write
Reset State: 0x00000020

This register's value configures general A2XB features.

A2XB_A2XB_CFG

Bits	Name	Description
21:16	MSTR_SPLIT_TIMEOUT	Shows the split timeout status of each of the CDAHB masters (one bit per master). When set signifies that the master has been split for longer than the timeout limit and therefore has seen a split timeout. The bits are sticky so that if more than one timeout happen the new timed out masters get OR-ed in with the previous value.
15:10	MSTR_SPLIT_STAT	Shows the split status of each of the CDAHB masters (one bit per master). When set signifies that the master has been split by A2XB. There are four reasons for a master being split: 1. Command Queue is full so request could not be accepted 2. Write data Queue is full so write data could not be accepted 3. Read request is pending and A2XB is waiting on AXI read completion 4. A write by another master is pending due to <2> so a new write command cannot be accepted
9:2	SPLIT_LIMIT	Configures the split timeout limit in the AHB slave in thousands of cycles. If a master is split for more than the configured limit a split timeout error interrupt will be generated. Reset State: 0x00000008
1	BUSY_OFF	Purely a debug feature. A bug in the busy generation logic has the potential to hang every master in Riva. Should this type of bug be encountered, setting this bit to 1 will ensure that busy is always low, thereby preventing masters from getting hung waiting for completion of writes. Please note that this will likely cause data coherency issues between masters. Reset State: 0x00000000

A2XB_A2XB_CFG (cont.)

Bits	Name	Description
0	ENABLE	Set to enable the A2XB bridge functionality. This register is actually on the PMU and this read only bit just reflects the status of the corresponding PMU register. requests not destined to internal A2XB registers will generate an AHB error response. Reset State: 0x00000000

0x3000004 A2XB_INT_MSK

Type: read-write
Reset State: 0x0000000F

The value of this register is used to mask interrupt sources.

A2XB_INT_MSK

Bits	Name	Description
3	A2XB_AXI_HALT_REQ_SET_INT_MSK	When clear it masks off the a2xb_axi_halt_req_set interrupt request. Reset State: 0x00000001
2	A2XB_SPLIT_TIMEOUT_ERR_INT_MSK	When clear it masks off the a2xb_split_timeout_err interrupt request. Reset State: 0x00000001
1	A2XB_RD_ERR_INT_MSK	When clear it masks off the a2xb_rd_err interrupt request. Reset State: 0x00000001
0	A2XB_WR_ERR_INT_MSK	When clear it masks off the a2xb_wr_err interrupt request. Reset State: 0x00000001

0x3000008 A2XB_INT_SRC_MSKD

Type: read-only
Reset State: 0x00000000

The value of this register is the masked interrupt source. It is the logical AND of the INT_SRC with INT_MSK

A2XB_INT_SRC_MSKD

Bits	Name	Description
3	A2XB_AXI_HALT_REQ_SET_INT_MSKD	This field is the masked a2xb_axi_halt_req_set_int Reset State: 0x00000000

A2XB_INT_SRC_MSKD (cont.)

Bits	Name	Description
2	A2XB_SPLIT_TIMEOUT_ERR_INT_MSKD	This field is the masked a2xb_split_timeout_err_int Reset State: 0x00000000
1	A2XB_RD_ERR_INT_MSKD	This field is the masked a2xb_rd_err_int Reset State: 0x00000000
0	A2XB_WR_ERR_INT_MSKD	This field is the masked a2xb_wr_err_int Reset State: 0x00000000

0x300000C A2XB_INT_SRC

Type: read-only
Reset State: 0x00000000

The value of this register is the interrupt source.

A2XB_INT_SRC

Bits	Name	Description
3	A2XB_AXI_HALT_REQ_SET_INT	This field is set when A2XB receives a halt request from the AXI fabric. This is a fatal error that will require a full A2XB reset to recover. Upon receiving the halt request, the A2XB will immediately unsplit any split masters, will flush all its buffers, will discard any data incoming on its AXI port side and will from then on return error responses to any AHB transaction destined to the fabric. Local access to A2XB CSRs will still work normally. Reset State: 0x00000000
2	A2XB_SPLIT_TIMEOUT_ERR_INT	This field is set when the A2XB GAS detects that a master has been split for longer than the timeout limit. This is a fatal error that will require at least a full A2XB reset to recover. On occurrence, A2XB will immediately unsplit any split masters, will flush all its buffers, will discard any data incoming on its AXI port side and will from then on return error responses to any AHB transaction destined to the fabric. Local access to A2XB CSRs will still work normally. Reset State: 0x00000000
1	A2XB_RD_ERR_INT	This field is set when A2XB receives an error response from the AXI fabric on any data beat of a read transaction. Data following the first beat with an error and belonging to the same transfer will be discarded and when the AHB master returns to complete its read it will be able to complete only as many beats as completed without an AXI error (if any) and will then receive an AHB error response on the beat that incurred the AXI error. Reset State: 0x00000000

A2XB_INT_SRC (cont.)

Bits	Name	Description
0	A2XB_WR_ERR_INT	This field is set when A2XB receives an error response from the AXI fabric for a write transaction. Since the AHB protocol provides no way to notify the originating master of errors incurred on posted writes, this interrupt will be the only indication that a write error occurred. Reset State: 0x00000000

0x3000010 A2XB_INT_CLR

Type: write-only
Reset State: 0x00000000

The value of this register is used to clear interrupt sources.

A2XB_INT_CLR

Bits	Name	Description
3	A2XB_AXI_HALT_REQ_SET_INT_CLR	This field when set will clear the halt request set interrupt indication. This only clears the interrupt request, A2XB reset will be required to return to normal operation. Reset State: 0x00000000
2	A2XB_SPLIT_TIMEOUT_ERR_INT_CLR	This field when set will clear the split timeout error interrupt. This only clears the interrupt request, A2XB reset will be required to return to normal operation. Reset State: 0x00000000
1	AXI_RD_ERR_INT_CLR	This field when set will clear the AXI read error interrupt. Reset State: 0x00000000
0	AXI_WR_ERR_INT_CLR	This field when set will clear the AXI write error interrupt. Reset State: 0x00000000

0x3000014 A2XB_TSTBUS_CTRL

Type: read-write
Reset State: 0x00000001

The value of this register is used to control a mux that selects which set of internal A2XB signals gets put on the chip-wide test bus.

A2XB_TSTBUS_CTRL

Bits	Name	Description
29:28	CTRL_SEL	Controls the different testbus configurations on the a2xb main control module. 3 different testbus configs are available 0x0: CFG_0 0x1: CFG_1 0x2: CFG_2 Reset State: 0x00000000
24	CSR_SEL	Controls the different testbus configurations on the a2xb_csr module. 2 different testbus configs are available 0x0: CFG_0 0x1: CFG_1 Reset State: 0x00000000
10:8	AXIM_SEL	Controls the different testbus configurations on the a2xb_axim module. 7 different testbus configs are available 0x0: CFG_0 0x1: CFG_1 0x2: CFG_2 0x3: CFG_3 0x4: CFG_4 0x5: CFG_5 0x6: CFG_6 Reset State: 0x00000000
5:4	AHB_SEL	Controls the different testbus configurations on the a2xb_ahb module. 3 different configs are available 0x0: CFG_0 0x1: CFG_1 0x2: CFG_2 Reset State: 0x00000000
3:1	SEL	Controls which of the internal a2xb local testbusses gets put out on the actual A2XB testbus output 0x0: MIX 0x1: AHB 0x2: AXIM 0x3: CMDFIFO 0x4: WRFIFO 0x5: RDFIFO 0x6: CSR 0x6: CTRL Reset State: 0x00000000
0	EN	Enable. When enabled the flop that drives the A2XB testbus will update its value every cycle, otherwise the flop outputs will remain constant. Reset State: 0x00000001

0x3000018 A2XB_TSTBUS

Type: read-only

This register provides bits [31:0] of the A2XB testbus.

A2XB_TSTBUS

Bits	Name	Description
31:0	VALUE	

0x300001C A2XB_ERR_INFO

Type: read-only

Records which AHB master IDs have received AXI write or read error responses for any of their transfers. Once set, the bit can only be cleared by resetting the A2XB.

A2XB_ERR_INFO

Bits	Name	Description
11	MID_6_RD_ERR	Set if AHB MID 6 got an AXI read error response in any of its transfers.
10	MID_5_RD_ERR	Set if AHB MID 5 got an AXI read error response in any of its transfers.
9	MID_4_RD_ERR	Set if AHB MID 4 got an AXI read error response in any of its transfers.
8	MID_3_RD_ERR	Set if AHB MID 3 got an AXI read error response in any of its transfers.
7	MID_2_RD_ERR	Set if AHB MID 2 got an AXI read error response in any of its transfers.
6	MID_1_RD_ERR	Set if AHB MID 1 got an AXI read error response in any of its transfers.
5	MID_6_WR_ERR	Set if AHB MID 6 got an AXI write error response in any of its transfers.
4	MID_5_WR_ERR	Set if AHB MID 5 got an AXI write error response in any of its transfers.
3	MID_4_WR_ERR	Set if AHB MID 4 got an AXI write error response in any of its transfers.
2	MID_3_WR_ERR	Set if AHB MID 3 got an AXI write error response in any of its transfers.
1	MID_2_WR_ERR	Set if AHB MID 2 got an AXI write error response in any of its transfers.
0	MID_1_WR_ERR	Set if AHB MID 1 got an AXI write error response in any of its transfers.

0x3000020 A2XB_REVISION

Type: read-only
Reset State: 0x00000045

This register's value represents the A2XB RTL revision present in the hardware.

A2XB_REVISION

Bits	Name	Description
31:0	REVID	Revision ID. Corresponds to the label number of A2XB (revision of .info file) Reset State: 0x00000045

0x3000024 A2XB_SPARE

Type: read-write
Reset State: 0x00000000

This register defines a few control spare bits to be used for bug fixing

A2XB_SPARE

Bits	Name	Description
7:0	SPARE	Spare bits to be used for bug fixing. Reset State: 0x00000000

16.2.2 ccahb

0x3000000 CCAHB_CCAHB_BT_PL

Type: read-write
Reset State: 0x00000005

ccahb Arbiter arbitration priority level for bt master. In the ccahb arbitration scheme, the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CCAHB_CCAHB_BT_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for bt master.The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the ccahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x3000004 CCAHB_CCAHB_FM_PL

Type: read-write
Reset State: 0x00000005

ccahb Arbiter arbitration priority level for fm master. In the ccahb arbitration scheme, the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CCAHB_CCAHB_FM_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for fm master.The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the ccahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x3000008 CCAHB_CCAHB_RRI_PL

Type: read-write
Reset State: 0x00000001

ccahb Arbiter arbitration priority level for rri master. In the ccahb arbitration scheme, the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CCAHB_CCAHB_RRI_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for rri master.The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the ccahb arbiter will prevent a master from disabling itself. Reset State: 0x00000001

0x300000C CCAHB_CCAHB_DXE_PL

Type: read-write
Reset State: 0x00000001

ccahb Arbiter arbitration priority level for dxe master. In the ccahb arbitration scheme, the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CCAHB_CCAHB_DXE_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for dxe master.The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the ccahb arbiter will prevent a master from disabling itself. Reset State: 0x00000001

0x3000010 CCAHB_CCAHB_CCPU_PL

Type: read-write
Reset State: 0x00000004

ccahb Arbiter arbitration priority level for ccpu master. In the ccahb arbitration scheme, the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CCAHB_CCAHB_CCPU_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for ccpu master.The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the ccahb arbiter will prevent a master from disabling itself. Reset State: 0x00000004

0x3000014 CCAHB_CCAHB_A2AB_PL

Type: read-write
Reset State: 0x00000001

ccahb Arbiter arbitration priority level for a2ab master. In the ccahb arbitration scheme, the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CCAHB_CCAHB_A2AB_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for a2ab master.The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the ccahb arbiter will prevent a master from disabling itself. Reset State: 0x00000001

0x3000018 CCAHB_CCAHB_TIC_PL

Type: read-write
Reset State: 0x00000005

ccahb Arbiter arbitration priority level for tic master. In the ccahb arbitration scheme, the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CCAHB_CCAHB_TIC_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for tic master.The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the ccahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x300001C CCAHB_CCAHB_CBR_PL

Type: read-write
Reset State: 0x00000005

ccahb Arbiter arbitration priority level for cbr master. In the ccahb arbitration scheme, the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CCAHB_CCAHB_CBR_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for cbr master.The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the ccahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x3000048 CCAHB_CCAHB_DFLT_MST

Type: read-write
Reset State: 0x00000000

This register identifies the default master for the ccahb

CCAHB_CCAHB_DFLT_MST

Bits	Name	Description
3:0	DFT_MST	Default Master ID number register. The default master is the master that is granted by the bus when no master has requested ownership. NOTE: Writing anything beyond the 4 R/W bits will cause the entire write to be discarded. 0x0: DMY 0x1: BT 0x2: FM 0x3: RRI 0x4: DXE 0x5: CCPU 0x6: A2AB 0x7: TIC 0x8: CBR Reset State: 0x00000000

0x3000090 CCAHB_CCAHB_VERSION

Type: read-only
Reset State: 0x3230382A

ASCII value for each number in the version, followed by '*'. For example 32_30_31_2A represents the version 2.01*.

CCAHB_CCAHB_VERSION

Bits	Name	Description
31:24	CCAHB_COMP_VERSION_BYTE0	Reset State: 0x00000032
23:16	CCAHB_COMP_VERSION_BYTE1	Reset State: 0x00000030
15:8	CCAHB_COMP_VERSION_BYTE2	Reset State: 0x00000038
7:0	CCAHB_COMP_VERSION_BYTE3	Reset State: 0x0000002A

16.2.3 ccu_qgic_ci

0x3000000 CCU_QGIC_CI_GICC_CTLR

Type: read-write
Reset State: 0x00000000

The GICC_CTLR configures the generic interrupt controller CPU interface.

CCU_QGIC_CI_GICC_CTLR

Bits	Name	Description
4	SBPR	Controls which binary point register is used to calculate pre-emption.0: BANKED (secure interrupts use the secure Binary Point Register, non-secure interrupts use the non-secure Binary Point Register)1: RESTRICTED (all interrupts use the secure Binary Point Register) Reset State: 0x00000000
3	S_DEST	Controls destination of secure interrupts.0: IRQ1: FIQ Reset State: 0x00000000
2	S_ACK	Controls the side effect behavior of a secure read request to the Interrupt Acknowledge Register in the case where the highest priority pending interrupt is non-secure.0: DISABLE ACK OF NS PENDING1: ENABLE ACK OF NS PENDING Reset State: 0x00000000
1	ENABLE_NS	For secure software, a read/writable alias of non secure software enable bit (bit 0 of this same register in non secure space).0: CLR1: SET Reset State: 0x00000000
0	ENABLE	For non-secure software, this bit enables/disables non secure interrupts. For secure software, this bit enables/disables secure interrupts.0: CLR1: SET Reset State: 0x00000000

0x3000004 CCU_QGIC_CI_GICC_PMR

Type: read-write
Reset State: 0x00000000

The GICC_PMR register configures the generic interrupt controller CPU interface Priority Mask. The Priority Mask can be used to limit the interrupts that can cause an interrupt request to the CPU based on priority levels.

CCU_QGIC_CI_GICC_PMR

Bits	Name	Description
7:0	LEVEL	Set the Priority Mask Level. The CPU interface asserts an interrupt request to CPU if the priority of the highest Pending interrupt sent by the interrupt Distributor is strictly higher than at least the mask set in Priority Mask Register. Reset State: 0x00000000

0x3000008 CCU_QGIC_CI_GICC_BPR

Type: read-write
Reset State: 0x00000000

The GICC_BPR register configures the generic interrupt controller CPU interface Binary Point. The Binary Point is used to limit interrupts that can cause an interrupt request to the CPU based on the interrupts priority and the interrupt priority that currently being serviced by the CPU (if there is one). If the CPU is not servicing an interrupt, the Binary Point register is not used.

CCU_QGIC_CI_GICC_BPR

Bits	Name	Description
2:0	VAL	The VAL setting is used to determine the priority bits used for preemption according to Table 11-9 Interpretation of Binary Point Register value. Reset State: 0x00000000

0x300000C CCU_QGIC_CI_GICC_IAR

Type: read-write
Reset State: 0x00000000

The GICC_IAR register is used by the CPU to obtain the ID of the interrupt which caused the assertion if IRQn or FIQn. Performing this read has the side effect of causing the Distributor to change the interrupt from the Pending state to the Active or Active and Pending state.

CCU_QGIC_CI_GICC_IAR

Bits	Name	Description
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. Reset State: 0x00000000

CCU_QGIC_CI_GICC_IAR (cont.)

Bits	Name	Description
9:0	INT_ID	Interrupt Identifier. The value returned in this field is dependent on the security state of the access to the register, and the security state of any outstanding interrupts, as described in Table 11-9 Interpretation of Binary Point Register value. Reset State: 0x00000000

0x3000010 CCU_QGIC_CI_GICC_EOIR

Type: read-write
Reset State: 0x00000000

The GICC_EOIR (End Of Interrupt) register is written to indicate when software has finished handling an interrupt. Writing to this register will set the interrupt to Inactive or Pending (if prior to writing to this register, the interrupt was both Active and Pending) in the Distributor. The value written must be the interrupt ID, and the CPU Source ID for sgis, of the interrupt that is being completed. The security status of the write to this register (NS-prot) must match the security status (NS-int) of the interrupt ID, according to Table 17-9 (GICC_EIOR security (and source CPU) match definition), in order for the interrupt to be successfully cleared.

CCU_QGIC_CI_GICC_EOIR

Bits	Name	Description
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it must match the ID of the CPU which requested the Interrupt. As described in Table 17-9, the CPU Source ID must match an active interrupt in order for the GICC_EOIR to take effect. The CPU_ID is written must match that delivered to software when GICC_IAR is read. Reset State: 0x00000000
9:0	INT_ID	Interrupt Identifier. The value must match the interrupt ID that software received when reading the GICC_IAR register. If the security settings match the Active state in the Distributor for the corresponding interrupt will be cleared. Reset State: 0x00000000

0x3000014 CCU_QGIC_CI_GICC_RPR

Type: read-write
Reset State: 0x00000000

The GICC_RPR (Running Priority) register provides access to the highest priority of all the Active interrupts on this CPU. The priority value returned is sensitive to the security status (NS-int) of the interrupt currently running and the NS-prot.

CCU_QGIC_CI_GICC_RPR

Bits	Name	Description
7:0	VAL	Running Priority Reset State: 0x00000000

0x3000018 CCU_QGIC_CI_GICC_HPPIR

Type: read-write
Reset State: 0x00000000

The GICC_HPPIR register provides access to the highest priority pending interrupt to the CPU Interface.

CCU_QGIC_CI_GICC_HPPIR

Bits	Name	Description
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. Reset State: 0x00000000
9:0	INT_ID	Interrupt Identifier. The value returned in this field is dependent on the security state of the access to the register, and the security state of any outstanding interrupts, as described in Table 11-9 Interpretation of Binary Point Register value. Reset State: 0x00000000

0x300001C CCU_QGIC_CI_GICC_ABPR

Type: read-write
Reset State: 0x00000000

The GICC_ABPR register provides a copy of the non-secure binary point register for use by secure software. See the definition of the GICC_BPR register for details on the use of this register.

CCU_QGIC_CI_GICC_ABPR

Bits	Name	Description
2:0	VAL	Same as the GICC_BPR register - affects only non-secure interrupts. Reset State: 0x00000000

0x30000FC CCU_QGIC_CI_GICC_IIDR

Type: read-write
Reset State: 0x00000000

The GICC_IIDR register provides information about the generic interrupt controller CPU Interface version and device implementer information.

CCU_QGIC_CI_GICC_IIDR

Bits	Name	Description
31:20	PART_NUM	Part Number: 0x390 Reset State: 0x00000000
19:16	ARCH_VERSION	Architecture Version : 0x1 Reset State: 0x00000000
15:12	REVISION	Revision number: 0x0 Reset State: 0x00000000
11:0	IMPLEMENTOR	Bits[11:8] contain the implementers JEP106 continuation code, 0x0 Bit[7] is always 0 Bits[6:0] contain bits [6:0] of the implementers JEP106 code, Reset State: 0x00000000

16.2.4 ccu_qgic_di

0x3000000 CCU_QGIC_DI_GICD_CTLR

Type: read-write
Reset State: 0x00000000

The GICD_CTLR register controls if the Distributor responds to external interrupt stimulus changes.

CCU_QGIC_DI_GICD_CTLR

Bits	Name	Description
1	ENABLE_NS	This bit is an alias of the enable_ns bit.0: CLR1: SET Reset State: 0x00000000
0	ENABLE	This bit is the enable bit for both Secure and Non-secure software. Secure software accesses enable_s at this location. Non-secure software accesses enable_ns.0: CLR1: SET Reset State: 0x00000000

0x3000004 CCU_QGIC_DI_GICD_TYPER

Type: read-write
Reset State: 0x00000000

The GICD_TYPER register provides information about the configuration of the GIC.

CCU_QGIC_DI_GICD_TYPER

Bits	Name	Description
15:11	LSPI	Returns the number of Lockable Shared Peripheral Interrupts (LSPIs) that the generic interrupt controller contains. Reset State: 0x00000000
10	TZ	TrustZone support. Generic interrupt controller supports TrustZone, always reads back 0x1. Reset State: 0x00000000
9:8	RESERVED_BITS9_TO_8	Reserved Reset State: 0x00000000
7:5	CPU_NUM	Returns the number of CPU interfaces that the generic interrupt controller provides. Reset State: 0x00000000
4:0	IT_LINES	Returns the number of INTIDs, to the nearest 32, that the Distributor provides. Reset State: 0x00000000

0x3000008 CCU_QGIC_DI_GICD_IIDR

Type: read-write
Reset State: 0x00000070

The GICD_IIDR register provides information the implementor of the Distributor and the revision of the Distributor.

CCU_QGIC_DI_GICD_IIDR

Bits	Name	Description
15:12	REVISION	Returns the revision number of the Distributor, 0x0 Reset State: 0x00000000
11:0	IMPLEMENTOR	Returns JEP106 ID number, 0b 01110000 Reset State: 0x00000070

0x3000020 CCU_QGIC_DI_GICD_ANSACR

Type: read-write
Reset State: 0x00000000

The auxiliary non-secure access control register (GICD_ANSACR) is used to control non-secure access to GICD_CGCR.

CCU_QGIC_DI_GICD_ANSACR

Bits	Name	Description
0	GICD_CGCR	0x0: SEC (Dis-allows non-secure access.1: NS Allows non-secure access.) Reset State: 0x00000000

0x3000024 CCU_QGIC_DI_GICD_CGCR

Type: read-write
Reset State: 0x00000000

The clock gate control register (GICD_CGCR) is used to control localized clock gating over-ride logic. Setting bits in GICD_CGCR disables the corresponding local clock gating logic. The local clock gating logic normally turns off a local (small subset) clock tree automatically if there is no need for the clock. If any error is found in the gating logic, these bits can be used to over-ride it.

CCU_QGIC_DI_GICD_CGCR

Bits	Name	Description
16	TOP	0x1: DISABLE0: ENABLE Controls the top level clock gate (which gates entire GIC.) Reset State: 0x00000000
15:4	RESERVED_15_TO_4	Reserved Reset State: 0x00000000
3	DI_SGI_STATE	0x1: DISABLE0: ENABLE Controls the clock gate for Distributor interrupt state data base registers for SGI interrupts. Reset State: 0x00000000
2	DI_PPI_SPI_STATE	0x1: DISABLE0: ENABLE Controls the clock gate for Distributor interrupt state data base registers for PPI and SPI interrupts. Reset State: 0x00000000
1	DI_DEMET	0x1: DISABLE0: ENABLE Controls the clock gate for Distributor interrupt input demet registers. Reset State: 0x00000000
0	DI_RD	0x1: DISABLE0: ENABLE Controls the clock gate for Distributor CRIF Read Data. Reset State: 0x00000000

0x3000080+0x4*n CCU_QGIC_DI_GICD_ISRn, n=[0..8]

Type: read-write
Reset State: 0x00000000

Each bit in an GICD_ISR register controls the security state of an interrupt, to be either secure or non-secure. You can only access these registers with secure read or secure write accesses. NOTE: The GICD_ISR register at address offset 0x0080 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

CCU_QGIC_DI_GICD_ISRn

Bits	Name	Description
31:0	INT_NS	0x0: SEC (Assigns INTID N to the Secure state.1: NS Assigns INTID N to the Non-secure state.) Reset State: 0x00000000

0x3000100+0x4*n CCU_QGIC_DI_GICD_ISENABLERn, n=[0..8]

Type: read-write
Reset State: 0x00000000

Each bit in an GICD_ISENABLER register controls the enabling of an interrupt. Reading this register returns the currently enabled interrupts subject to NS-int dependent access rules. NOTE The GICD_ISENABLER register at address offset 0x0100 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

CCU_QGIC_DI_GICD_ISENABLERn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ICENABLER register.1: SET Enables INTID N.) Reset State: 0x00000000

0x3000180+0x4*n CCU_QGIC_DI_GICD_ICENABLERn, n=[0..8]

Type: read-write
Reset State: 0x00000000

Each bit in an GICD_ICENABLER register controls the disabling of an interrupt. Reading this register returns the currently enabled interrupts subject to NS-int dependent access rules. NOTE The GICD_ICENABLER register at address offset 0x0180 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

CCU_QGIC_DI_GICD_ICENABLERn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ISENABLER register.1: CLR Enables INTID N.) Reset State: 0x00000000

0x3000200+0x4*n CCU_QGIC_DI_GICD_ISPENDRn, n=[0..8]

Type: read-write
Reset State: 0x00000000

Each bit in an GICD_ISPENDR register controls the enabling of an interrupt. Reading this register returns the currently pending interrupts subject to NS-int dependent access rules. NOTE The GICD_ISPENDR register at address offset 0x0200 is repeated once per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI interrupts. SGI interrupt bits are read-only, however the distributor updates these using the GICD_SGIR register. The remaining registers control the SPI interrupts.

CCU_QGIC_DI_GICD_ISPENDRn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ICPENDR register.1: SET Sets INTID N to the Pending state.) Reset State: 0x00000000

0x3000280+0x4*n CCU_QGIC_DI_GICD_ICPENDRn, n=[0..8]

Type: read-write
Reset State: 0x00000000

Each bit in an GICD_ICPENDR register controls the disabling of an interrupt. Reading this register returns the currently pending interrupts subject to NS-int dependent access rules. NOTE The GICD_ICPENDR register at address offset 0x0280 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI interrupts. SGI interrupt bits are read-only, however the distributor updates these using the GICD_SGIR register. The remaining registers control the SPI interrupts.

CCU_QGIC_DI_GICD_ICPENDRn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ISPENDR register.1: CLR Clears INTID N. from the pending state.) Reset State: 0x00000000

0x3000300+0x4*n CCU_QGIC_DI_GICD_IACTIVERn, n=[0..8]

Type: read-write
Reset State: 0x00000000

Each bit in the GICD_IACTIVER register provides the active status of an interrupt. NOTE The GICD_IACTIVER register at address offset 0x0300 is repeated once per CPU Interface. It is only accessible from the designated CPU and provides information for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

CCU_QGIC_DI_GICD_IACTIVERn

Bits	Name	Description
31:0	INT	0x0: CLR1: SET Reset State: 0x00000000

0x3000400+0x4*n CCU_QGIC_DI_GICD_IPRIORITYRn, n=[0..71]

Type: read-write
Reset State: 0x00000000

Each field in the GICD_IPRIORITYR registers controls the priority level of an interrupt. NOTE The GICD_IPRIORITYR registers at address offsets 0x0400 to 0x41C are repeated once per CPU Interface. These are only accessible from the designated CPU and control the priority levels for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupt priority levels.

CCU_QGIC_DI_GICD_IPRIORITYRn

Bits	Name	Description
31:24	INT3	see below Reset State: 0x00000000
23:16	INT2	see below Reset State: 0x00000000
15:8	INT1	see below Reset State: 0x00000000
7:0	INT0	All bits cleared (0x0) is the highest priorty. All bits set (0xFF) is the lowest priority. For non-secure write access, the MSB is always set (0x1). For non-secure read access, the MSB is always clear (0x0). Non-secure entities cant use the highest priorities without secure software setting such a priority. The highest priorities are typically reserved for secure software. Reset State: 0x00000000

0x3000800+0x4*n CCU_QGIC_DI_GICD_ITARGETSRn, n=[0..71]

Type: read-write
Reset State: 0x00000000

Each field in the GICD_ITARGETSR registers controls the destination CPU(s) of an interrupt.

NOTE The GICD_ITARGETSR registers at address offsets 0x0800 to 0x81C are not actually implemented. These are place holders PPI and SGI interrupts. PPI interrupts, being private, only have one destination CPU. SGI interrupts are generated by the QGIC_DI_SOFT_INT register only. The remaining registers control the SPI interrupt destinations.

CCU_QGIC_DI_GICD_ITARGETSRn

Bits	Name	Description
31:24	INT3	see below Reset State: 0x00000000
23:16	INT2	see below Reset State: 0x00000000
15:8	INT1	see below Reset State: 0x00000000
7:0	INT0	Each bit represents one of 8 CPUs. Bit 0 represents the zeroth CPU, bit 7 represents the seventh CPU. Setting this field to 0 will disable the interrupt as no CPU will see it set. Reset State: 0x00000000

0x3000C00+0x4*n CCU_QGIC_DI_GICD_ICFGRn, n=[0..17]

Type: read-write
Reset State: 0x00000000

Each field in the GICD_ICFGR registers allows: control of type of an SPI: level-sensitive / edge-sensitive reading the type of PPIs and sgis.

NOTE The GICD_ICFGR registers at address offsets 0x0C00 to 0xC04 are repeated once per CPU Interface. These are only accessible from the designated CPU and allow read access for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

CCU_QGIC_DI_GICD_ICFGRn

Bits	Name	Description
31:30	INT15	see below Reset State: 0x00000000
29:28	INT14	see below Reset State: 0x00000000
27:26	INT13	see below Reset State: 0x00000000
25:24	INT12	see below Reset State: 0x00000000
23:22	INT11	see below Reset State: 0x00000000
21:20	INT10	see below Reset State: 0x00000000
19:18	INT9	see below Reset State: 0x00000000
17:16	INT8	see below Reset State: 0x00000000
15:14	INT7	see below Reset State: 0x00000000
13:12	INT6	see below Reset State: 0x00000000
11:10	INT5	see below Reset State: 0x00000000
9:8	INT4	see below Reset State: 0x00000000
7:6	INT3	see below Reset State: 0x00000000
5:4	INT2	see below Reset State: 0x00000000
3:2	INT1	see below Reset State: 0x00000000
1:0	INT0	0x0: LVL N to N 01 : LVL 1 to N 10 : EDGE N to N 11 : EDGE 1 to N These bits behave differently for each of the three interrupt types as follows: For SGI, read back as 0b10 - SGI interrupts are edge-sensitive and use the N-N model. For PPI/SPI, read/writable as 0b01 or 0b11 - PPI/SPI interrupts can be edge or level sensitive and use the 1-N model. Reset State: 0x00000000

0x3000F00 CCU_QGIC_DI_GICD_SGIR

Type: read-write
Reset State: 0x00000000

The GICD_SGIR register provides the method by which software may cause interrupts to become pending for designated target CPU(s). The generic interrupt controller maintains an internal database of all outstanding software interrupt requests pended to each CPU Interface and rotates through them in Round Robin fashion. Signaling the same interrupt a second time before it is serviced will result in only one interrupt from the source CPU to the target CPU(s).

CCU_QGIC_DI_GICD_SGIR

Bits	Name	Description
25:24	T_FILTER	Target Filter 00 : LIST (Use the T_LIST as is) 01 : OTHERS (Send to all CPUs except the CPU MID making the request, ignoring T_LIST) 10 : MID (Send to only the CPU MID making the request, ignoring T_LIST) 11 : NA (Reserved) Reset State: 0x00000000
23:16	T_LIST	Target List. Each bit set represents a CPU target for the INT_ID, subject to the T_FILTER field. Reset State: 0x00000000
15	SATT	Security ATTribute. This bit is only programmable by secure Software. See0: SECURE (Secure interrupt is issued)1: NONSECURE (Non-secure interrupt is issued). Reset State: 0x00000000
14:4	RESERVED_BITS14_TO_4	Reserved Reset State: 0x00000000
3:0	INT_ID	The INT ID number (0-15) of the SGI to be set as pending. See the SGI pending truth table for security status Table 11-4 (SATT vs. NS-prot) for information on the conditions that allow an SGI to be set pending. Reset State: 0x00000000

0x3000FD0 CCU_QGIC_DI_GICD_PIDR0

Type: read-write
Reset State: 0x00000090

The GICD_PIDR0 provides access to generic interrupt controller peripheral identification.

CCU_QGIC_DI_GICD_PIDR0

Bits	Name	Description
7:0	PART_NUM	Returns lower byte of the generic interrupt controller part number 0xB390, 0x90 Reset State: 0x00000090

0x3000FF0 CCU_QGIC_DI_GICD_CIDR0

Type: read-write
Reset State: 0x0000000D

The GICD_CIDR0 provides access to generic interrupt controller component identification.

CCU_QGIC_DI_GICD_CIDR0

Bits	Name	Description
7:0	COMP_ID_0	Reads back as 0x0D. Reset State: 0x0000000D

0x3000FF4 CCU_QGIC_DI_GICD_CIDR1

Type: read-write
Reset State: 0x000000F0

The GICD_CIDR0 provides access to generic interrupt controller component identification.

CCU_QGIC_DI_GICD_CIDR1

Bits	Name	Description
7:0	COMP_ID_0	Reads back as 0xF0. Reset State: 0x000000F0

0x3000FF8 CCU_QGIC_DI_GICD_CIDR2

Type: read-write
Reset State: 0x00000005

The GICD_CIDR0 provides access to generic interrupt controller component identification.

CCU_QGIC_DI_GICD_CIDR2

Bits	Name	Description
7:0	COMP_ID_0	Reads back as 0x05. Reset State: 0x00000005

0x3000FFC CCU_QGIC_DI_GICD_CIDR3

Type: read-write
Reset State: 0x000000B1

The GICD_CIDR0 provides access to generic interrupt controller component identification.

CCU_QGIC_DI_GICD_CIDR3

Bits	Name	Description
7:0	COMP_ID_0	Reads back as 0xB1. Reset State: 0x000000B1

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0x3000000 CCU_CCU_TMR1

Type: read-write
Reset State: 0x00000000

The CCU_TMR1 runs on 32 KHz clock. This is a free-running timer once enabled by writing to the CCU_TIMERS_CTL register. An interrupt is generated when the timer reaches the CCU_TMRMTH1 registers match count.

CCU_CCU_TMR1

Bits	Name	Description
31:0	TMR1_COUNT	Count for ticks of 32 KHz clock Reset State: 0x00000000

0x3000004 CCU_CCU_TMR2

Type: read-write
Reset State: 0x00000000

The CCU_TMR2 runs on 32 KHz clock. This is a free-running timer once enabled by writing to the CCU_TIMERS_CTL register. An interrupt is generated when the timer reaches the CCU_TMRMTH2 registers match count.

CCU_CCU_TMR2

Bits	Name	Description
31:0	TMR2_COUNT	Count for ticks of 32 KHz clock Reset State: 0x00000000

0x3000008 CCU_CCU_TMRMTH1

Type: read-write
Reset State: 0xFFFFFFFF

The CCU_TMRMTH1 is programmed with match count for CCU_TMR1 reg. Match between the count and timer will result in interrupt generation to GIC.

CCU_CCU_TMRMTH1

Bits	Name	Description
31:0	TMR1_MATCH	Count to match with 32 KHz timer Reset State: 0xFFFFFFFF

0x300000C CCU_CCU_TMRMTH2

Type: read-write
Reset State: 0xFFFFFFFF

The CCU_TMRMTH2 is programmed with match count for CCU_TMR2 reg. Match between the count and timer will result in interrupt generation to GIC.

CCU_CCU_TMRMTH2

Bits	Name	Description
31:0	TMR2_MATCH	Count to match with 32 KHz timer Reset State: 0xFFFFFFFF

0x3000010 CCU_CCU_SYSTMR

Type: read-write
Reset State: 0x00000000

The CCU_SYSTMR runs on chip XO clock. This timer can be enabled by writing to the CCU_TIMERS_CTL reg. This is mainly for software system debug purposes.

CCU_CCU_SYSTMR

Bits	Name	Description
31:0	SYSTMR_COUNT	Count for clock ticks Reset State: 0x00000000

0x3000014 CCU_CCU_WDGTMR

Type: read-write
Reset State: 0x00000000

The CCU_WDGTMR runs on AHB_CLK. Basically, when the watch dog timer is enabled, this timer keeps ++ at every millisecond. Once it reaches watch dog THR0, an interrupt is generated when it reaches THR1 another interrupt is generated (higher priority). On reaching THR3, another higher priority interrupt is generated. Typically this is used to reset the chip.

CCU_CCU_WDGTMR

Bits	Name	Description
31:30	ENABLE_DISABLE	Watch dog timer and the corresponding interrupts are enabled only when these bits are 10, 01 is disable. Any other combination will not be accepted and if software writes 00 or 11, the status is maintained. Reset State: 0x00000000
29:24	PROTECTION_VECTOR	This is write only register. When it is read ZEROs are returned. Writes to the watch dog register can happen (including the enable/disable) only when this field matches the CCU_WDGTHR 0[25:24],THR1[25:24],THR2[25:24] Reset State: 0x00000000
23:0	TIMER_COUNT	When enabled, it keeps ++ at every millisecond. Software can write to it only when the protection vector matches the concat of the 2 bit protection bits from the watch dog threshold register. The protection vector can't be 00 or 3f Reset State: 0x00000000

0x3000018 CCU_CCU_WDGTHR0

Type: read-write
Reset State: 0x00000000

The CCU_WDGTHR0 runs on AHB_CLK. This register contains THR0 for watch dog timer (CCU_WDGTMR).

CCU_CCU_WDGTHR0

Bits	Name	Description
27:26	PROTECTION_FIELD	This register is writable only when this field is 11 Reset State: 0x00000000
25:24	PROTECTION_VECTOR	2 bits of the protection_vector0 of watch dog timer. Reset State: 0x00000000
23:0	THRESHOLD	Contains the watch dog THR0. It is writable by software only when its protection field =11 Reset State: 0x00000000

0x300001C CCU_CCU_WDGTHR1

Type: read-write
Reset State: 0x00000000

The CCU_WDGTHR1 runs on AHB_CLK. This register contains THR1 for watch dog timer (CCU_WDGTMR).

CCU_CCU_WDGTHR1

Bits	Name	Description
27:26	PROTECTION_FIELD	This register is writable only when this field is 10 Reset State: 0x00000000
25:24	PROTECTION_VECTOR	2 bits of the protection_vector1 of watch dog timer. Reset State: 0x00000000
23:0	THRESHOLD	Contains the watch dog THR1. It is writable by software only when its protection field =10 Reset State: 0x00000000

0x3000020 CCU_CCU_WDGTHR2

Type: read-write
Reset State: 0x00000000

The CCU_WDGTHR2 runs on AHB_CLK. This register contains THR2 for watch dog timer (CCU_WDGTMR).

CCU_CCU_WDGTHR2

Bits	Name	Description
27:26	PROTECTION_FIELD	This register is writable only when this field is 01 Reset State: 0x00000000

CCU_CCU_WDGTHR2 (cont.)

Bits	Name	Description
25:24	PROTECTION_VECTOR	2 bits of the protection_vector2 of watch dog timer. Reset State: 0x00000000
23:0	THRESHOLD	Contains the watch dog THR2. It is writable by software only when its protection field =01 Reset State: 0x00000000

0x3000024 CCU_CCU_WDG_CFG

Type: read-write
Reset State: 0x00000000

This register controls the number of AHB clock ticks per micro-second used by CCU_WDGTMR.

CCU_CCU_WDG_CFG

Bits	Name	Description
7:0	CCU_WDGTMR_ONE_USEC_LIMIT	Count for ticks of 32 KHz clock Reset State: 0x00000000

0x3000028 CCU_CCU_TIMERS_CTL

Type: read-write
Reset State: 0x00000000

This register controls the enables for TMR1, TMR2 and SYSTMR.

CCU_CCU_TIMERS_CTL

Bits	Name	Description
2	SYSTMR_ENABLE	0x0: Disable Timer (Default 1: Enable Timer) Reset State: 0x00000000
1	TMR2_ENABLE	0x0: Disable Timer 1: Enable Timer (Default) Reset State: 0x00000000
0	TMR1_ENABLE	0x0: Disable Timer 1: Enable Timer (Default) Reset State: 0x00000000

0x300002C CCU_CCU_SPARE_TEST_CTL

Type: read-write
Reset State: 0x00000000

Spare test control register.

CCU_CCU_SPARE_TEST_CTL

Bits	Name	Description
31:12	SPARE	[31:16] ccu_a2ab_timeout_value; A2AB transaction timeout time in units of 0x1FF clock cycles; 0x0 means the timeout timer is disabled [15:12] Spare Bits Reset State: 0x00000000
11	CCU_TESTMUX_SW_TRIGGER_EN	when set, enables software overwrite of a testbus signal Reset State: 0x00000000
10	CCU_TESTMUX_SW_TRIGGER_SEL	0x1: overwrite will happen for testbus bit 0, 1b1: overwrite will happen for testbus bit 28 Reset State: 0x00000000
9	CCU_TESTMUX_SW_TRIGGER_VALUE	The value that will be put out on the selected testbus signal Reset State: 0x00000000
8	ECAHB_VITALS_TESTBUS_ENABLE	ecahb_vitals_testbus_enable Reset State: 0x00000000
7	ECAHB_TESTBUS_ENABLE	ecahb_testbus_enable Reset State: 0x00000000
6:4	A2AB_TESTBUS_SEL	a2ab_testbus_sel Reset State: 0x00000000
3	CDAHB_VITALS_TESTBUS_ENABLE	cdahb_vitals_testbus_enable Reset State: 0x00000000
2	CDAHB_TESTBUS_ENABLE	cdahb_testbus_enable Reset State: 0x00000000
1	CCAHB_VITALS_TESTBUS_ENABLE	ccahb_vitals_testbus_enable Reset State: 0x00000000
0	CCAHB_TESTBUS_ENABLE	ccahb_testbus_enable Reset State: 0x00000000

0x3000030 CCU_CCU_SPARE_INT_CTL

Type: read-write
Reset State: 0x00000000

Spare Int control register.

CCU_CCU_SPARE_INT_CTL

Bits	Name	Description
31:5	SPARE	Spare Bits Reset State: 0x00000000

CCU_CCU_SPARE_INT_CTL (cont.)

Bits	Name	Description
4:2	TRC_MAIN_CTRL_STE	Tracer main control state machine state Reset State: 0x00000000
1:0	TRC_CMEM_WRCTL_STE	Tracer cmem interface write control state machine state Reset State: 0x00000000

0x3000034 CCU_CCU_ROM_BASE_ADDR1

Type: read-write
Reset State: 0x00000000

Base Address for ROM in Dwords; Left-Shift by 2-bits to get the byte address

CCU_CCU_ROM_BASE_ADDR1

Bits	Name	Description
27:21	BA3	patch3_base_addr Reset State: 0x00000000
20:14	BA2	patch2_base_addr Reset State: 0x00000000
13:7	BA1	patch1_base_addr Reset State: 0x00000000
6:0	BA0	patch0_base_addr Reset State: 0x00000000

0x3000038 CCU_CCU_ROM_BASE_ADDR2

Type: read-write
Reset State: 0x00000000

Base Address for ROM in Dwords; Left-Shift by 2-bits to get the byte address

CCU_CCU_ROM_BASE_ADDR2

Bits	Name	Description
27:21	BA7	patch7_base_addr Reset State: 0x00000000
20:14	BA6	patch6_base_addr Reset State: 0x00000000
13:7	BA5	patch5_base_addr Reset State: 0x00000000

CCU_CCU_ROM_BASE_ADDR2 (cont.)

Bits	Name	Description
6:0	BA4	patch4_base_addr Reset State: 0x00000000

0x300003C CCU_CCU_ROM_START_ADDR1

Type: read-write
Reset State: 0x00000000

Start Address for ROM in Dwords; Left-Shift by 2-bits to get the byte address

CCU_CCU_ROM_START_ADDR1

Bits	Name	Description
31:16	SA1	patch1_start_addr Reset State: 0x00000000
15:0	SA0	patch0_start_addr Reset State: 0x00000000

0x3000040 CCU_CCU_ROM_START_ADDR2

Type: read-write
Reset State: 0x00000000

Start Address for ROM in Dwords; Left-Shift by 2-bits to get the byte address

CCU_CCU_ROM_START_ADDR2

Bits	Name	Description
31:16	SA3	patch3_start_addr Reset State: 0x00000000
15:0	SA2	patch2_start_addr Reset State: 0x00000000

0x3000044 CCU_CCU_ROM_START_ADDR3

Type: read-write
Reset State: 0x00000000

Start Address for ROM in Dwords; Left-Shift by 2-bits to get the byte address

CCU_CCU_ROM_START_ADDR3

Bits	Name	Description
31:16	SA5	patch5_start_addr Reset State: 0x00000000
15:0	SA4	patch4_start_addr Reset State: 0x00000000

0x3000048 CCU_CCU_ROM_START_ADDR4

Type: read-write
Reset State: 0x00000000

Start Address for ROM in Dwords; Left-Shift by 2-bits to get the byte address

CCU_CCU_ROM_START_ADDR4

Bits	Name	Description
31:16	SA7	patch7_start_addr Reset State: 0x00000000
15:0	SA6	patch6_start_addr Reset State: 0x00000000

0x300004C CCU_CCU_ROM_END_ADDR1

Type: read-write
Reset State: 0x00000000

End Address for ROM in Dwords; Left-Shift by 2-bits to get the byte address

CCU_CCU_ROM_END_ADDR1

Bits	Name	Description
31:16	EA1	patch1_end_addr Reset State: 0x00000000
15:0	EA0	patch0_end_addr Reset State: 0x00000000

0x3000050 CCU_CCU_ROM_END_ADDR2

Type: read-write
Reset State: 0x00000000

End Address for ROM in Dwords; Left-Shift by 2-bits to get the byte address

CCU_CCU_ROM_END_ADDR2

Bits	Name	Description
31:16	EA3	patch3_end_addr Reset State: 0x00000000
15:0	EA2	patch2_end_addr Reset State: 0x00000000

0x3000054 CCU_CCU_ROM_END_ADDR3

Type: read-write
Reset State: 0x00000000

End Address for ROM in Dwords; Left-Shift by 2-bits to get the byte address

CCU_CCU_ROM_END_ADDR3

Bits	Name	Description
31:16	EA5	patch5_end_addr Reset State: 0x00000000
15:0	EA4	patch4_end_addr Reset State: 0x00000000

0x3000058 CCU_CCU_ROM_END_ADDR4

Type: read-write
Reset State: 0x00000000

End Address for ROM in Dwords; Left-Shift by 2-bits to get the byte address

CCU_CCU_ROM_END_ADDR4

Bits	Name	Description
31:16	EA7	patch7_end_addr Reset State: 0x00000000
15:0	EA6	patch6_end_addr Reset State: 0x00000000

0x300005C CCU_CCU_VERSION

Type: read-write
Reset State: 0x00020002

This register indicates the version number of the Common SS for FPGA builds.

CCU_CCU_VERSION

Bits	Name	Description
19:16	CHIP_VERSION	Chip Version Number. Reset State: 0x00000002
15:0	VERSION_NUM	Version Number reference to the build. Reset State: 0x00000002

0x3000060 CCU_CCU_SOFT_RESET

Type: read-write
Reset State: 0x00000000

This register controls Soft Reset control of Common SS modules. Set high to reset.

CCU_CCU_SOFT_RESET

Bits	Name	Description
17	TESTMUX_SOFT_RESET	Soft Reset for Testmux. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
16	PMU_SLP_SOFT_RESET	Soft Reset for PMU. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
15	PMU_TCXO_SOFT_RESET	Soft Reset for PMU. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
14	PMU_AHB_SOFT_RESET	Soft Reset for PMU. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
13	LTE_SOFT_RESET	Soft Reset for LTE. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
12	FM_SOFT_RESET	Soft Reset for FM. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000

CCU_CCU_SOFT_RESET (cont.)

Bits	Name	Description
11	BT_SOFT_RESET	Soft Reset for FM. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
10	TIC_SOFT_RESET	Soft Reset for TIC. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
9	ROM_SOFT_RESET	Soft Reset for ROM. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
8	SPDM_SOFT_RESET	Soft Reset for SPDM. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
7	CDAHB_SOFT_RESET	Soft Reset for CDAHB. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
6	CCAHB_SOFT_RESET	Soft Reset for CCHB. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
5	A2XB_SOFT_RESET	Soft Reset for A2XB. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
4	A2AB_SOFT_RESET	Soft Reset for A2AB. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
3	RRI_SOFT_RESET	Soft Reset for RRI. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
2	DXE_SOFT_RESET	Soft Reset for DXE. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
1	CMEM_SOFT_RESET	Soft Reset for CMEM. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000
0	CCPU_SOFT_RESET	Soft Reset for CCPU. Asserts the reset when set. Needs to be cleared by SW. Reset State: 0x00000000

0x3000064 CCU_CCU_ENABLE_CLK

Type: read-write
Reset State: 0x00007FFF

This register enables the clock to Common SS modules. If set, the clock is enabled.

CCU_CCU_ENABLE_CLK

Bits	Name	Description
15	TESTMUX_ROOT_CLK_ENABLE	Enable clock for testmux Reset State: 0x00000000
14	PMU_TCXO_ENABLE_CLK	Enable clock for pmu_tcxo Reset State: 0x00000001
13	LTE_ENABLE_CLK	Enable clock for lte Reset State: 0x00000001
12	FM_ENABLE_CLK	Enable clock for fm Reset State: 0x00000001
11	BT_ENABLE_CLK	Enable clock for bt Reset State: 0x00000001
10	TIC_ENABLE_CLK	Enable clock for tic Reset State: 0x00000001
9	ROM_ENABLE_CLK	Enable clock for rom Reset State: 0x00000001
8	SPDM_ENABLE_CLK	Enable clock for spdm Reset State: 0x00000001
7	CDAHB_ENABLE_CLK	Enable clock for cdahb Reset State: 0x00000001
6	CCAHB_ENABLE_CLK	Enable clock for ccahb Reset State: 0x00000001
5	A2XB_ENABLE_CLK	Enable clock for a2xb Reset State: 0x00000001
4	A2AB_ENABLE_CLK	Enable clock for a2ab Reset State: 0x00000001
3	RRI_ENABLE_CLK	Enable clock for rri Reset State: 0x00000001
2	DXE_ENABLE_CLK	Enable clock for dxe Reset State: 0x00000001
1	CMEM_ENABLE_CLK	Enable clock for cmem Reset State: 0x00000001
0	CCPU_ENABLE_CLK	Enable clock for ccpu Reset State: 0x00000001

0x3000068 CCU_CCU_DISABLE_CLK_GATING

Type: read-write
Reset State: 0x0000C5F0

Controls clock gating in the module. If set, clock gating to the module and in the module is disabled.

CCU_CCU_DISABLE_CLK_GATING

Bits	Name	Description
16	TESTMUX_CLKGATE_DISABLE	Disable clock gating for testmux Reset State: 0x00000000
15	PMU_TCXO_DISABLE_CLK_GATING	Disable clk gating for pmu tcxo Reset State: 0x00000001
14	PMU_DISABLE_CLK_GATING	Disable clk gating for pmu Reset State: 0x00000001
13	LTE_DISABLE_CLK_GATING	Disable clk gating for lte Reset State: 0x00000000
12	FM_DISABLE_CLK_GATING	Disable clk gating for fm Reset State: 0x00000000
11	BT_DISABLE_CLK_GATING	Disable clk gating for bt Reset State: 0x00000000
10	TIC_DISABLE_CLK_GATING	Disable clk gating for tic Reset State: 0x00000001
9	AXI_FABRIC_DISABLE_CLK_GATING	Disable clk gating for AXI Fabric clock Reset State: 0x00000000
8	SPDM_DISABLE_CLK_GATING	Disable clk gating for spdm Reset State: 0x00000001
7	CDAHB_DISABLE_CLK_GATING	Disable clk gating for cdahb Reset State: 0x00000001
6	CCAHB_DISABLE_CLK_GATING	Disable clk gating for ccahb Reset State: 0x00000001
5	A2XB_DISABLE_CLK_GATING	Disable clk gating for a2xb Reset State: 0x00000001
4	A2AB_DISABLE_CLK_GATING	Disable clk gating for a2ab Reset State: 0x00000001
3	RRI_DISABLE_CLK_GATING	Disable clk gating for rri Reset State: 0x00000000
2	DXE_DISABLE_CLK_GATING	Disable clk gating for dxe Reset State: 0x00000000

CCU_CCU_DISABLE_CLK_GATING (cont.)

Bits	Name	Description
1	CMEM_DISABLE_CLK_GATING	Disable clk gating for cmem Reset State: 0x00000000
0	CCPU_DISABLE_CLK_GATING	Disable clk gating for ccpu Reset State: 0x00000000

0x300006C CCU_CCU_GCU_DISABLE_CLK_GATING

Type: read-write
Reset State: 0x000000F0

Controls clock gating in the module. If set, clock gating to the module and in the module is disabled.

CCU_CCU_GCU_DISABLE_CLK_GATING

Bits	Name	Description
13	LTE_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for lte Reset State: 0x00000000
12	FM_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for fm Reset State: 0x00000000
11	BT_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for bt Reset State: 0x00000000
10	TIC_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for tic Reset State: 0x00000000
9	ROM_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for rom Reset State: 0x00000000
8	SPDM_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for spdm Reset State: 0x00000000
7	CDAHB_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for cdahb Reset State: 0x00000001
6	CCAHB_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for ccahb Reset State: 0x00000001
5	A2XB_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for a2xb Reset State: 0x00000001
4	A2AB_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for a2ab Reset State: 0x00000001
3	RRI_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for rri Reset State: 0x00000000

CCU_CCU_GCU_DISABLE_CLK_GATING (cont.)

Bits	Name	Description
2	DXE_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for dxe Reset State: 0x00000000
1	CMEM_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for cmem Reset State: 0x00000000
0	CCPU_GCU_DISABLE_CLK_GATING	Disable GCU clk gating for ccpu Reset State: 0x00000000

0x3000070 CCU_CCU_CRCM_CONTROL

Type: read-write
Reset State: 0x00000000

This register represents CRCM control signals

CCU_CCU_CRCM_CONTROL

Bits	Name	Description
2	WMAC_SYNC_RST_CLK_EN_OVERRIDE	wmac_sync_rst_clk_en_override to CRCM Reset State: 0x00000000
1	CMEM_MEM_CLK_ENABLED	cmem_mem_clk_enabled to CMEM Reset State: 0x00000000
0	CMEM_TEST_CLK_GATE_DISABLE	cmem_test_clk_gate_disable to CRCM Reset State: 0x00000000

0x3000074 CCU_CCU_TESTBUS_CONTROL

Type: read-write
Reset State: 0x00000000

This register represents testbus control

CCU_CCU_TESTBUS_CONTROL

Bits	Name	Description
7:4	CCU_TESTBUS_SEL	Select signals for CCU testbus Reset State: 0x00000000
3:0	MODULE_SEL	Select module for testbus: 4'd0: CCU 4'd1: CMEM 4'd2: DXE 4'd3: RRI 4'd4: A2AB 4'd5: A2XB 4'd6: CCAHB 4'd7: CDAHB 4'd8: SPDM 4'd9: ROM 4'd9-15: unused Reset State: 0x00000000

0x3000078 CCU_CCU_TESTBUS_LOWER

Type: read-only
Reset State: 0x00000000

Holds the lower 32 bits of the Common SS testbus.

CCU_CCU_TESTBUS_LOWER

Bits	Name	Description
31:0	TESTBUS_LOWER	lower 32 bits of the testbus. Reset State: 0x00000000

0x300007C CCU_CCU_TESTBUS_UPPER

Type: read-only
Reset State: 0x00000000

Holds the upper 13 bits of the Common SS testbus

CCU_CCU_TESTBUS_UPPER

Bits	Name	Description
12:0	TESTBUS_UPPER	upper 13 bits of the testbus Reset State: 0x00000000

0x3000080 CCU_CCU_RRI_SW_REG_REINIT

Type: command
Reset State: 0x00000000

CCU_RRI_SW_REG_REINIT

CCU_CCU_RRI_SW_REG_REINIT

Bits	Name	Description
0	RRI_SW_REG_REINIT_P	Write a one to initiate the reg-reinit process. Write only Reset State: 0x00000000

0x3000084 CCU_CCU_RRI_SW_REG_REINIT_ADDR

Type: read-write
Reset State: 0x00000000

CCU_RRI_SW_REG_REINIT_ADDR

CCU_CCU_RRI_SW_REG_REINIT_ADDR

Bits	Name	Description
31:2	RRI_SW_REG_REINIT_ADDR	The starting (word) address of the software triggered register re-configuration table. Reset State: 0x00000000

0x3000088 CCU_CCU_RRI_POLL_CMD_ERR_ADDR

Type: read-only
Reset State: 0x00000000

CCU_RRI_POLL_CMD_ERR_ADDR

CCU_CCU_RRI_POLL_CMD_ERR_ADDR

Bits	Name	Description
31:2	RRI_POLL_CMD_ERR_ADDR	the poll cmd address when it reaches retry timeout error. Read Only Reset State: 0x00000000

0x300008C CCU_CCU_RRI_MISC_CFG

Type: read-write
Reset State: 0x00000000

CCU_RRI_MISC_CFG

CCU_CCU_RRI_MISC_CFG

Bits	Name	Description
19:15	RRI_CCU_ENCODED_FSM	rri_ccu_encoded_fsm, Read Only Reset State: 0x00000000
14:11	CCU_RRI_TESTBUS_SEL	Testbus select for RRI Reset State: 0x00000000
10	CCU_RRI_GOTO_IDLE	When set, force RRI FSM to go back to idle. Default to 0 Reset State: 0x00000000
9	CCU_RRI_ERR_STATE_CFG	When set, RRI FSM will continue to finish the process when error occurs. When cleared, RRI FSM will go to error state and software has to write to the ccu_rri_err_exit bit to clear the error. Default to 0. Reset State: 0x00000000

CCU_CCU_RRI_MISC_CFG (cont.)

Bits	Name	Description
8	CCU_RRI_ERR_EXIT	Write 1 for RRI FSM to go back to IDLE from error state. Always read 0. Reset State: 0x00000000
7:0	CCU_RRI_ONE_USEC_LIMIT	Value in number of clock cycles to generate the 1microseconds pulse. Reset State: 0x00000000

0x3000090 CCU_CCU_TIC_CTL

Type: read-write
Reset State: 0x00000000

TIC related control.

CCU_CCU_TIC_CTL

Bits	Name	Description
0	CCU_TIC_BUS_SELECT	0x0: Riva TIC is hooked up to the CCAHB 1: Riva TIC is hooked up to the CDAHB Reset State: 0x00000000

0x3000094 CCU_CCU_MISC_CTL

Type: read-write
Reset State: 0x00000000

CCU Controller related misc control.

CCU_CCU_MISC_CTL

Bits	Name	Description
6	CCU_CCPU_WRAP8_DISABLE	When set it disables the wrap8 logic implemented in CCPU for Riva 2.0 Reset State: 0x00000000
5	CCPU_CMEM_TIMEOUT_CHK_EN	CCPU CMEM Timeout check enable Reset State: 0x00000000
4	CCPU_STATUS_COUNT_RESET	Signal to reset CCPU Status count Reset State: 0x00000000
3	CCPU_STATUS_COUNT_EN	Signal to enable CCPU Status count Reset State: 0x00000000

CCU_CCU_MISC_CTL (cont.)

Bits	Name	Description
2	ITCM_ENABLE	0x0: ITCM interface on ARM9 disabled 1: ITCM interface on ARM9 enabled Reset State: 0x00000000
1	GAS2CRIF_WR_CLK_GATE_DISABLE	0x0: GICs CRIF wr_clk gating not disabled 1: GICs CRIF wr_clk gating disabled Reset State: 0x00000000
0	GAS2CRIF_NS_SELECT	0x0: GICs CRIF accesses are Secure 1: GICs CRIF accesses are Non-Secure Reset State: 0x00000000

0x3000098 CCU_CCU_CCPU_STALL_COUNT

Type: read-only
Reset State: 0x00000000

CCPU Stall counter value

CCU_CCU_CCPU_STALL_COUNT

Bits	Name	Description
31:0	CCPU_STALL_COUNT	CCPU Stall Counter value Reset State: 0x00000000

0x300009C CCU_CCU_CCPU_ACTIVE_COUNT

Type: read-only
Reset State: 0x00000000

CCPU Active counter value.

CCU_CCU_CCPU_ACTIVE_COUNT

Bits	Name	Description
31:0	CCPU_ACTIVE_COUNT	CCPU Active Counter value Reset State: 0x00000000

0x3000100 CCU_CCU_CCPU_INVALID_ADDR

Type: read-only
Reset State: 0x00000000

CCPU Last Invalid Addr.

CCU_CCU_CCPU_INVALID_ADDR

Bits	Name	Description
31:0	CCPU_INVALID_ADDR	CCPU Last Invalid Addr Reset State: 0x00000000

0x3000104 CCU_CCU_CCPU_LAST_ADDR0

Type: read-only
Reset State: 0x00000000

CCPU Last Address 0. The last 3 addresses the ARM9 has requested over the memory bus

CCU_CCU_CCPU_LAST_ADDR0

Bits	Name	Description
31:0	CCPU_LAST_ADDR0	CCPU Last Address 0 Reset State: 0x00000000

0x3000108 CCU_CCU_CCPU_LAST_ADDR1

Type: read-only
Reset State: 0x00000000

CCPU Last Address 1. The last 3 addresses the ARM9 has requested over the memory bus

CCU_CCU_CCPU_LAST_ADDR1

Bits	Name	Description
31:0	CCPU_LAST_ADDR1	CCPU Last Address 1 Reset State: 0x00000000

0x300010C CCU_CCU_CCPU_LAST_ADDR2

Type: read-only
Reset State: 0x00000000

CCPU Last Address 2. The last 3 addresses the ARM9 has requested over the memory bus.

CCU_CCU_CCPU_LAST_ADDR2

Bits	Name	Description
31:0	CCPU_LAST_ADDR2	CCPU Last Address 2 Reset State: 0x00000000

0x3000110 CCU_CCU_A2AB_ERR_ADDR

Type: read-only
Reset State: 0x00000000

A2AB error address register.

CCU_CCU_A2AB_ERR_ADDR

Bits	Name	Description
31:0	A2AB_CCU_AHB_ERR_ADDR	a2ab_ccu_ahb_err_addr, can be cleared by writing to A2AB_CTL register Reset State: 0x00000000

0x3000114 CCU_CCU_A2AB_CTL

Type: read-write
Reset State: 0x00000000

A2AB control register.

CCU_CCU_A2AB_CTL

Bits	Name	Description
0	A2AB_AHB_ERR_CLEAR	Write 1 to clear CCU_A2AB_ERR_ADDR register and generate ccu_a2ab_ahb_err_clear signal. software needs to clear this bit to de-assert the clear signal. Reset State: 0x00000000

0x3000118 CCU_CCU_A2AB_CFG

Type: read-write
Reset State: 0x00000000

A2AB config register.

CCU_CCU_A2AB_CFG

Bits	Name	Description
3:0	CCU_A2AB_CFG_HREADY_LIMIT	A2AB input config signal Reset State: 0x00000000

0x30001F0 CCU_CCU_CCPU_DBG_STATUS

Type: read-only
Reset State: 0x00000003

CCPU irq_n & fiq_n status

CCU_CCU_CCPU_DBG_STATUS

Bits	Name	Description
7:5	FIQ_COUNT	Count negedges of fiq_n Reset State: 0x00000000
4:2	IRQ_COUNT	Count negedges of irq_n Reset State: 0x00000000
1	FIQ_N	fiq_n raw status Reset State: 0x00000001
0	IRQ_N	irq_n raw status Reset State: 0x00000001

0x3000200 CCU_CCU_CCPU_TO_MSM_MB_INT_STAT

Type: read-only
Reset State: 0x00000000

Register indicating for which mailboxes an interrupt to the APQ is pending.

CCU_CCU_CCPU_TO_MSM_MB_INT_STAT

Bits	Name	Description
11:0	MBX_INT_STATUS	Each bit stands for the corresponding mailbox. When set, an interrupt from that Mailbox is pending Reset State: 0x00000000

0x3000204 CCU_CCU_MSM_TO_CCPU_MB_INT_STAT

Type: read-only
Reset State: 0x00000000

Register indicating for which mailboxes an interrupt to the cCPU is pending

CCU_CCU_MSM_TO_CCPU_MB_INT_STAT

Bits	Name	Description
3:0	MBX_INT_STATUS	Each bit stands for the corresponding mailbox. When set, an interrupt from that Mailbox is pending Reset State: 0x00000000

0x3000208 CCU_CCU_MB0_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB0_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to Zero: ReadOnly Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x300020C CCU_CCU_MB0_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB0_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb0_control register. This value gets cleared on a mb0 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset. Reset State: 0x00000000

0x3000210 CCU_CCU_MB1_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB1_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to Zero: ReadOnly Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x3000214 CCU_CCU_MB1_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB1_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb1_control register. This value gets cleared on a mb1 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000218 CCU_CCU_MB2_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB2_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to Zero: ReadOnly Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x300021C CCU_CCU_MB2_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB2_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb2_control register. This value gets cleared on a mb2 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000220 CCU_CCU_MB3_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB3_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to Zero: ReadOnly Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x3000224 CCU_CCU_MB3_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB3_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb3_control register. This value gets cleared on a mb3 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000228 CCU_CCU_MB4_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB4_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ When set to one: APQ to cCPU Hard Coded to Zero: ReadOnly Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x300022C CCU_CCU_MB4_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB4_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb4_control register. This value gets cleared on a mb4 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000230 CCU_CCU_MB5_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB5_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to Zero: ReadOnly Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x3000234 CCU_CCU_MB5_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB5_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb5_control register. This value gets cleared on a mb5 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000238 CCU_CCU_MB6_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB6_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to Zero: ReadOnly Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x300023C CCU_CCU_MB6_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB6_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb6_control register. This value gets cleared on a mb6 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000240 CCU_CCU_MB7_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB7_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to Zero: ReadOnly Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x3000244 CCU_CCU_MB7_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB7_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb7_control register. This value gets cleared on a mb7 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000248 CCU_CCU_MB8_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB8_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to Zero: ReadOnly Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x300024C CCU_CCU_MB8_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB8_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb8_control register. This value gets cleared on a mb8 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000250 CCU_CCU_MB9_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB9_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to Zero: ReadOnly Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x3000254 CCU_CCU_MB9_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB9_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb9_control register. This value gets cleared on a mb9 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000258 CCU_CCU_MB10_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB10_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to zero: ReadOnly Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x300025C CCU_CCU_MB10_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB10_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb10_control register. This value gets cleared on a mb10 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000260 CCU_CCU_MB11_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB11_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to zero: ReadOnly Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x3000264 CCU_CCU_MB11_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB11_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb11_control register. This value gets cleared on a mb11 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000268 CCU_CCU_MB12_CONTROL

Type: read-write
Reset State: 0x00000002

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB12_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to one: ReadOnly Reset State: 0x00000001
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x300026C CCU_CCU_MB12_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB12_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb12_control register. This value gets cleared on a mb12 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000270 CCU_CCU_MB13_CONTROL

Type: read-write
Reset State: 0x00000002

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB13_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to one: ReadOnly Reset State: 0x00000001
0	MB_RESET	When set, all to this MB -elated parameters, including the counters, are cleared. Reset State: 0x00000000

0x3000274 CCU_CCU_MB13_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB13_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb13_control register. This value gets cleared on a mb13 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000278 CCU_CCU_MB14_CONTROL

Type: read-write
Reset State: 0x00000002

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB14_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to one: ReadOnly Reset State: 0x00000001
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x300027C CCU_CCU_MB14_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB14_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb14_control register. This value gets cleared on a mb14 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000280 CCU_CCU_MB15_CONTROL

Type: read-write
Reset State: 0x00000002

General purpose Mailbox register, which can be used to generate interrupts to the ccpu or to the APQ.

CCU_CCU_MB15_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: cCPU to APQ. When set to one: APQ to cCPU Hard Coded to one: ReadOnly Reset State: 0x00000001
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x3000284 CCU_CCU_MB15_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

CCU_CCU_MB15_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb15_control register. This value gets cleared on a mb15 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset Reset State: 0x00000000

0x3000288 CCU_CCU_MUTEX0

Type: read-write
Reset State: 0x00000101

General purpose semaphore and/or mutex register

CCU_CCU_MUTEX0

Bits	Name	Description
31	RESET	When set, both CURRENTCOUNT and MAXCOUNT fields get initialized with the value written to the MAXCOUNT field. This bit will not get set on a write operation. Reset State: 0x00000000
15:8	MAXCOUNT	THe Max count of semaphores available. Can only be set when the Reset bit is written with value 1. Reset State: 0x00000001
7:0	CURRENTCOUNT	Current count of the semaphore. On a read, the current value of the Semaphore is returned and if the CurrentCount > 0, the CurrentCount value is decreased by one. On a write, the current value of the Semaphore is increased by one if the CurrentCount < MaxCount Reset State: 0x00000001

0x300028C CCU_CCU_MUTEX1

Type: read-write
Reset State: 0x00000101

General purpose semaphore and/or mutex register

CCU_CCU_MUTEX1

Bits	Name	Description
31	RESET	When set, both CURRENTCOUNT and MAXCOUNT fields get initialized with the value written to the MAXCOUNT field. This bit will not get set on a write operation. Reset State: 0x00000000
15:8	MAXCOUNT	The Max count of semaphores available. Can only be set when the Reset bit is written with value 1. Reset State: 0x00000001
7:0	CURRENTCOUNT	Current count of the semaphore. On a read, the current value of the Semaphore is returned and if the CurrentCount > 0, the CurrentCount value is decreased by one. On a write, the current value of the Semaphore is increased by one if the CurrentCount < MaxCount Reset State: 0x00000001

0x3000290 CCU_CCU_MUTEX2

Type: read-write
Reset State: 0x00000101

General purpose semaphore and/or mutex register

CCU_CCU_MUTEX2

Bits	Name	Description
31	RESET	When set, both CURRENTCOUNT and MAXCOUNT fields get initialized with the value written to the MAXCOUNT field. This bit will not get set on a write operation. Reset State: 0x00000000
15:8	MAXCOUNT	THe Max count of semaphores available. Can only be set when the Reset bit is written with value 1. Reset State: 0x00000001
7:0	CURRENTCOUNT	Current count of the semaphore. On a read, the current value of the Semaphore is returned and if the CurrentCount > 0, the CurrentCount value is decreased by one. On a write, the current value of the Semaphore is increased by one if the CurrentCount < MaxCount Reset State: 0x00000001

0x3000294 CCU_CCU_MUTEX3

Type: read-write
Reset State: 0x00000101

General purpose semaphore and/or mutex register

CCU_CCU_MUTEX3

Bits	Name	Description
31	RESET	When set, both CURRENTCOUNT and MAXCOUNT fields get initialized with the value written to the MAXCOUNT field. This bit will not get set on a write operation. Reset State: 0x00000000
15:8	MAXCOUNT	THe Max count of semaphores available. Can only be set when the Reset bit is written with value 1. Reset State: 0x00000001
7:0	CURRENTCOUNT	Current count of the semaphore. On a read, the current value of the Semaphore is returned and if the CurrentCount > 0, the CurrentCount value is decreased by one. On a write, the current value of the Semaphore is increased by one if the CurrentCount < MaxCount Reset State: 0x00000001

0x3000298 CCU_CCU_MUTEX4

Type: read-write
Reset State: 0x00000101

General purpose semaphore and/or mutex register

CCU_CCU_MUTEX4

Bits	Name	Description
31	RESET	When set, both CURRENTCOUNT and MAXCOUNT fields get initialized with the value written to the MAXCOUNT field. This bit will not get set on a write operation. Reset State: 0x00000000
15:8	MAXCOUNT	THe Max count of semaphores available. Can only be set when the Reset bit is written with value 1. Reset State: 0x00000001
7:0	CURRENTCOUNT	Current count of the semaphore. On a read, the current value of the Semaphore is returned and if the CurrentCount > 0, the CurrentCount value is decreased by one. On a write, the current value of the Semaphore is increased by one if the CurrentCount < MaxCount Reset State: 0x00000001

0x300029C CCU_CCU_MUTEX5

Type: read-write
Reset State: 0x00000101

General purpose semaphore and/or mutex register

CCU_CCU_MUTEX5

Bits	Name	Description
31	RESET	When set, both CURRENTCOUNT and MAXCOUNT fields get initialized with the value written to the MAXCOUNT field. This bit will not get set on a write operation. Reset State: 0x00000000
15:8	MAXCOUNT	THe Max count of semaphores available. Can only be set when the Reset bit is written with value 1. Reset State: 0x00000001
7:0	CURRENTCOUNT	Current count of the semaphore. On a read, the current value of the Semaphore is returned and if the CurrentCount > 0, the CurrentCount value is decreased by one. On a write, the current value of the Semaphore is increased by one if the CurrentCount < MaxCount Reset State: 0x00000001

0x30002A0 CCU_CCU_MUTEX6

Type: read-write
Reset State: 0x00000101

General purpose semaphore and/or mutex register

CCU_CCU_MUTEX6

Bits	Name	Description
31	RESET	When set, both CURRENTCOUNT and MAXCOUNT fields get initialized with the value written to the MAXCOUNT field. This bit will not get set on a write operation. Reset State: 0x00000000
15:8	MAXCOUNT	THe Max count of semaphores available. Can only be set when the Reset bit is written with value 1. Reset State: 0x00000001
7:0	CURRENTCOUNT	Current count of the semaphore. On a read, the current value of the Semaphore is returned and if the CurrentCount > 0, the CurrentCount value is decreased by one. On a write, the current value of the Semaphore is increased by one if the CurrentCount < MaxCount Reset State: 0x00000001

0x30002A4 CCU_CCU_MUTEX7

Type: read-write
Reset State: 0x00000101

General purpose semaphore and/or mutex register

CCU_CCU_MUTEX7

Bits	Name	Description
31	RESET	When set, both CURRENTCOUNT and MAXCOUNT fields get initialized with the value written to the MAXCOUNT field. This bit will not get set on a write operation. Reset State: 0x00000000
15:8	MAXCOUNT	THe Max count of semaphores available. Can only be set when the Reset bit is written with value 1. Reset State: 0x00000001
7:0	CURRENTCOUNT	Current count of the semaphore. On a read, the current value of the Semaphore is returned and if the CurrentCount > 0, the CurrentCount value is decreased by one. On a write, the current value of the Semaphore is increased by one if the CurrentCount < MaxCount Reset State: 0x00000001

0x30002A8 CCU_CCU_TRACE_CONTROL1

Type: read-write
Reset State: 0x00000000

Trace function enable/disable control

CCU_CCU_TRACE_CONTROL1

Bits	Name	Description
1	CCU_TRC_BUF_CFG	0x0: captured samples write is blocked when buffer is full, 1 = overwrite mode enabled Reset State: 0x00000000
0	CCU_TRC_ENABLE	When set, the trace function is enabled Reset State: 0x00000000

0x30002AC CCU_CCU_TRACE_CONTROL2

Type: read-write
Reset State: 0x3FFF0000

Trace function sample storage location in cMEM control

CCU_CCU_TRACE_CONTROL2

Bits	Name	Description
29:16	CCU_TRC_END_ADDR	trace buffer cMEM ending address Reset State: 0x00003FFF
13:0	CCU_TRC_START_ADDR	trace buffer cMEM starting address Reset State: 0x00000000

0x30002B0 CCU_CCU_TRC_WFT_CAPTURE_CTRL

Type: read-write
Reset State: 0x00000000

Wait for Trigger capture control

CCU_CCU_TRC_WFT_CAPTURE_CTRL

Bits	Name	Description
31:30	CCU_WFT_CAPTURE_MODE	0x0: no capture of samples, 01 = capture samples every clock, 10 = capture only when signals selected by capture mask have changed states, 11 = reserved Reset State: 0x00000000
29:0	CCU_WFT_CAPTURE_MASK	Wait For trigger capture mask Reset State: 0x00000000

0x30002B4 CCU_CCU_TRC_WFT_STATE_CTRL

Type: read-write
Reset State: 0x00000000

Wait for Trigger state control

CCU_CCU_TRC_WFT_STATE_CTRL

Bits	Name	Description
31:16	CCU_MAX_CAPTURE_COUNT	Maximum number of samples to be captured after entering this state. A value of 0 indicates unlimited samples Reset State: 0x00000000
15:5	CCU_SPARE2	Reserved Reset State: 0x00000000

CCU_CCU_TRC_WFT_STATE_CTRL (cont.)

Bits	Name	Description
4:0	CCU_TS_TRANSITION_ENABLE	These enables indicate to which other TSs the trigger state machine is allowed to jump when the corresponding trigger is seen. When multiple enabled triggers come in at the same time, the lowest TS gets priority Bit 0: When set, transition to TS1 enabled when TS1 trigger is seen Bit 1: When set, transition to TS2 enabled when TS2 trigger is seen Bit 2: When set, transition to TS3 enabled when TS3 trigger is seen Bit 3: When set, transition to TS4 enabled when TS4 trigger is seen Bit 4: When set, transition to TS5 enabled when TS5 trigger is seen Reset State: 0x00000000

0x30002B8 CCU_CCU_TRC_TS1_CAPTURE_CTRL

Type: read-write
Reset State: 0x00000000

Trigger State 1 capture control

CCU_CCU_TRC_TS1_CAPTURE_CTRL

Bits	Name	Description
31:30	CCU_TS1_CAPTURE_MODE	0x0: no capture of samples, 01 = capture samples every clock, 10 = capture only when signals selected by capture mask have changed states, 11 = reserved Reset State: 0x00000000
29:0	CCU_TS1_CAPTURE_MASK	TS1 capture mask Reset State: 0x00000000

0x30002BC CCU_CCU_TRC_TS1_STATE_CTRL

Type: read-write
Reset State: 0x00000000

Trigger State 1 state control

CCU_CCU_TRC_TS1_STATE_CTRL

Bits	Name	Description
31:16	CCU_MAX_CAPTURE_COUNT	Maximum number of samples to be captured after entering this state. A value of 0 indicates unlimited samples Reset State: 0x00000000
15:5	CCU_SPARE2	Reserved Reset State: 0x00000000

CCU_CCU_TRC_TS1_STATE_CTRL (cont.)

Bits	Name	Description
4:0	CCU_TS_TRANSITION_ENABLE	These enables indicate to which other TSs the trigger state machine is allowed to jump when the corresponding trigger is seen. When multiple enabled triggers come in at the same time, the lowest TS gets priority Bit 0: When set, transition to TS1 enabled when TS1 trigger is seen Bit 1: When set, transition to TS2 enabled when TS2 trigger is seen Bit 2: When set, transition to TS3 enabled when TS3 trigger is seen Bit 3: When set, transition to TS4 enabled when TS4 trigger is seen Bit 4: When set, transition to TS5 enabled when TS5 trigger is seen Reset State: 0x00000000

0x30002C0 CCU_CCU_TRC_TS1_TRIGGER_MASK

Type: read-write
Reset State: 0x00000000

TS1 Trigger Mask control

CCU_CCU_TRC_TS1_TRIGGER_MASK

Bits	Name	Description
29:0	CCU_TRIGGER_MASK	All bits set to 1 in this mask, selects the signals in the test bus for which a trigger value is defined. All bits set to 0 indicate testbus signals that are don't cares, and will not be used for this trigger. Reset State: 0x00000000

0x30002C4 CCU_CCU_TRC_TS1_TRIGGER_VALUE

Type: read-write
Reset State: 0x00000000

TS1 Trigger value control

CCU_CCU_TRC_TS1_TRIGGER_VALUE

Bits	Name	Description
29:0	CCU_TRIGGER_VALUE	For each bit that is a 1 in the ts1 trigger mask, the value in of the corresponding bit in this register indicates the trigger value of the testbus signal. Reset State: 0x00000000

0x30002C8 CCU_CCU_TRC_TS2_CAPTURE_CTRL

Type: read-write
Reset State: 0x00000000

Trigger State 2 capture control

CCU_CCU_TRC_TS2_CAPTURE_CTRL

Bits	Name	Description
31:30	CCU_TS2_CAPTURE_MODE	0x0: no capture of samples, 01 = capture samples every clock, 10 = capture only when signals selected by capture mask have changed states, 11 = reserved Reset State: 0x00000000
29:0	CCU_TS2_CAPTURE_MASK	TS1 capture mask Reset State: 0x00000000

0x30002CC CCU_CCU_TRC_TS2_STATE_CTRL

Type: read-write
Reset State: 0x00000000

Trigger State 2 state control

CCU_CCU_TRC_TS2_STATE_CTRL

Bits	Name	Description
31:16	CCU_MAX_CAPTURE_COUNT	Maximum number of samples to be captured after entering this state. A value of 0 indicates unlimited samples Reset State: 0x00000000
15:5	CCU_SPARE2	Reserved Reset State: 0x00000000
4:0	CCU_TS_TRANSITION_ENABLE	These enables indicate to which other TSs the trigger state machine is allowed to jump when the corresponding trigger is seen. When multiple enabled triggers come in at the same time, the lowest TS gets priority Bit 0: When set, transition to TS1 enabled when TS1 trigger is seen Bit 1: When set, transition to TS2 enabled when TS2 trigger is seen Bit 2: When set, transition to TS3 enabled when TS3 trigger is seen Bit 3: When set, transition to TS4 enabled when TS4 trigger is seen Bit 4: When set, transition to TS5 enabled when TS5 trigger is seen Reset State: 0x00000000

0x30002D0 CCU_CCU_TRC_TS2_TRIGGER_MASK

Type: read-write
Reset State: 0x00000000

TS2 Trigger Mask control

CCU_CCU_TRC_TS2_TRIGGER_MASK

Bits	Name	Description
29:0	CCU_TRIGGER_MASK	All bits set to 1 in this mask, selects the signals in the test bus for which a trigger value is defined. All bits set to 0 indicate testbus signals that are don't cares, and will not be used for this trigger. Reset State: 0x00000000

0x30002D4 CCU_CCU_TRC_TS2_TRIGGER_VALUE

Type: read-write
Reset State: 0x00000000

TS2 Trigger value control

CCU_CCU_TRC_TS2_TRIGGER_VALUE

Bits	Name	Description
29:0	CCU_TRIGGER_VALUE	For each bit that is a 1 in the ts2 trigger mask, the value in of the corresponding bit in this register indicates the trigger value of the testbus signal. Reset State: 0x00000000

0x30002D8 CCU_CCU_TRC_TS3_CAPTURE_CTRL

Type: read-write
Reset State: 0x00000000

Trigger State 3 capture control

CCU_CCU_TRC_TS3_CAPTURE_CTRL

Bits	Name	Description
31:30	CCU_TS3_CAPTURE_MODE	0x0: no capture of samples, 01 = capture samples every clock, 10 = capture only when signals selected by capture mask have changed states, 11 = reserved Reset State: 0x00000000

CCU_CCU_TRC_TS3_CAPTURE_CTRL (cont.)

Bits	Name	Description
29:0	CCU_TS3_CAPTURE_MASK	TS1 capture mask Reset State: 0x00000000

0x30002DC CCU_CCU_TRC_TS3_STATE_CTRL

Type: read-write
Reset State: 0x00000000

Trigger State 3 state control

CCU_CCU_TRC_TS3_STATE_CTRL

Bits	Name	Description
31:16	CCU_MAX_CAPTURE_COUNT	Maximum number of samples to be captured after entering this state. A value of 0 indicates unlimited samples Reset State: 0x00000000
15:5	CCU_SPARE2	Reserved Reset State: 0x00000000
4:0	CCU_TS_TRANSITION_ENABLE	These enables indicate to which other TSs the trigger state machine is allowed to jump when the corresponding trigger is seen. When multiple enabled triggers come in at the same time, the lowest TS gets priority Bit 1: When set, transition to TS1 enabled when TS1 trigger is seen Bit 2: When set, transition to TS2 enabled when TS2 trigger is seen Bit 3: When set, transition to TS3 enabled when TS3 trigger is seen Bit 4: When set, transition to TS4 enabled when TS4 trigger is seen Bit 5: When set, transition to TS5 enabled when TS5 trigger is seen Reset State: 0x00000000

0x30002E0 CCU_CCU_TRC_TS3_TRIGGER_MASK

Type: read-write
Reset State: 0x00000000

TS3 Trigger Mask control

CCU_CCU_TRC_TS3_TRIGGER_MASK

Bits	Name	Description
29:0	CCU_TRIGGER_MASK	All bits set to 1 in this mask, selects the signals in the test bus for which a trigger value is defined. All bits set to 0 indicate testbus signals that are don't cares, and will not be used for this trigger. Reset State: 0x00000000

0x30002E4 CCU_CCU_TRC_TS3_TRIGGER_VALUE

Type: read-write
Reset State: 0x00000000

TS3 Trigger value control

CCU_CCU_TRC_TS3_TRIGGER_VALUE

Bits	Name	Description
29:0	CCU_TRIGGER_VALUE	For each bit that is a 1 in the ts3 trigger mask, the value in of the corresponding bit in this register indicates the trigger value of the testbus signal. Reset State: 0x00000000

0x30002E8 CCU_CCU_TRC_TS4_CAPTURE_CTRL

Type: read-write
Reset State: 0x00000000

Trigger State 4 capture control

CCU_CCU_TRC_TS4_CAPTURE_CTRL

Bits	Name	Description
31:30	CCU_TS4_CAPTURE_MODE	0x0: no capture of samples, 01 = capture samples every clock, 10 = capture only when signals selected by capture mask have changed states, 11 = reserved Reset State: 0x00000000
29:0	CCU_TS4_CAPTURE_MASK	TS1 capture mask Reset State: 0x00000000

0x30002EC CCU_CCU_TRC_TS4_STATE_CTRL

Type: read-write
Reset State: 0x00000000

Trigger State 4 state control

CCU_CCU_TRC_TS4_STATE_CTRL

Bits	Name	Description
31:16	CCU_MAX_CAPTURE_COUNT	Maximum number of samples to be captured after entering this state. A value of 0 indicates unlimited samples Reset State: 0x00000000

CCU_CCU_TRC_TS4_STATE_CTRL (cont.)

Bits	Name	Description
15:5	CCU_SPARE2	Reserved Reset State: 0x00000000
4:0	CCU_TS_TRANSITION_ENABLE	These enables indicate to which other TSs the trigger state machine is allowed to jump when the corresponding trigger is seen. When multiple enabled triggers come in at the same time, the lowest TS gets priority Bit 1: When set, transition to TS1 enabled when TS1 trigger is seen Bit 2: When set, transition to TS2 enabled when TS2 trigger is seen Bit 3: When set, transition to TS3 enabled when TS3 trigger is seen Bit 4: When set, transition to TS4 enabled when TS4 trigger is seen Bit 5: When set, transition to TS5 enabled when TS5 trigger is seen Reset State: 0x00000000

0x30002F0 CCU_CCU_TRC_TS4_TRIGGER_MASK

Type: read-write
Reset State: 0x00000000

TS4 Trigger Mask control

CCU_CCU_TRC_TS4_TRIGGER_MASK

Bits	Name	Description
29:0	CCU_TRIGGER_MASK	All bits set to 1 in this mask, selects the signals in the test bus for which a trigger value is defined. All bits set to 0 indicate testbus signals that are don't cares, and will not be used for this trigger. Reset State: 0x00000000

0x30002F4 CCU_CCU_TRC_TS4_TRIGGER_VALUE

Type: read-write
Reset State: 0x00000000

TS4 Trigger value control

CCU_CCU_TRC_TS4_TRIGGER_VALUE

Bits	Name	Description
29:0	CCU_TRIGGER_VALUE	For each bit that is a 1 in the ts4 trigger mask, the value in of the corresponding bit in this register indicates the trigger value of the testbus signal. Reset State: 0x00000000

0x30002F8 CCU_CCU_TRC_TS5_CAPTURE_CTRL

Type: read-write
Reset State: 0x00000000

Trigger State 5 capture control

CCU_CCU_TRC_TS5_CAPTURE_CTRL

Bits	Name	Description
31:30	CCU_TS5_CAPTURE_MODE	0x0: no capture of samples, 01 = capture samples every clock, 10 = capture only when signals selected by capture mask have changed states, 11 = reserved Reset State: 0x00000000
29:0	CCU_TS5_CAPTURE_MASK	TS1 capture mask Reset State: 0x00000000

0x30002FC CCU_CCU_TRC_TS5_STATE_CTRL

Type: read-write
Reset State: 0x00000000

Trigger State 5 state control

CCU_CCU_TRC_TS5_STATE_CTRL

Bits	Name	Description
31:16	CCU_MAX_CAPTURE_COUNT	Maximum number of samples to be captured after entering this state. A value of 0 indicates unlimited samples Reset State: 0x00000000
15:5	CCU_SPARE2	Reserved Reset State: 0x00000000
4:0	CCU_TS_TRANSITION_ENABLE	These enables indicate to which other TSs the trigger state machine is allowed to jump when the corresponding trigger is seen. When multiple enabled triggers come in at the same time, the lowest TS gets priority Bit 0: When set, transition to TS1 enabled when TS1 trigger is seen Bit 1: When set, transition to TS2 enabled when TS2 trigger is seen Bit 2: When set, transition to TS3 enabled when TS3 trigger is seen Bit 3: When set, transition to TS4 enabled when TS4 trigger is seen Bit 4: When set, transition to TS5 enabled when TS5 trigger is seen Reset State: 0x00000000

0x3000300 CCU_CCU_TRC_TS5_TRIGGER_MASK

Type: read-write
Reset State: 0x00000000

TS5 Trigger Mask control

CCU_CCU_TRC_TS5_TRIGGER_MASK

Bits	Name	Description
29:0	CCU_TRIGGER_MASK	All bits set to 1 in this mask, selects the signals in the test bus for which a trigger value is defined. All bits set to 0 indicate testbus signals that are don't cares, and will not be used for this trigger. Reset State: 0x00000000

0x3000304 CCU_CCU_TRC_TS5_TRIGGER_VALUE

Type: read-write
Reset State: 0x00000000

TS5 Trigger value control

CCU_CCU_TRC_TS5_TRIGGER_VALUE

Bits	Name	Description
29:0	CCU_TRIGGER_VALUE	For each bit that is a 1 in the ts5 trigger mask, the value in of the corresponding bit in this register indicates the trigger value of the testbus signal. Reset State: 0x00000000

0x3000310 CCU_CCU_DXE_INT_SELECT

Type: read-write
Reset State: 0x00000000

Select the DXE interrupts to generate the xfer done and rx data avail apss interrupts

CCU_CCU_DXE_INT_SELECT

Bits	Name	Description
22:16	RX_DATA_AVAIL_DXE_CHANNEL_SELECT	Bit 16: when set, dxe channel 0 interrupt is ORed into riva_apps_wlan_rx_data_avail interrupt. Bit 17: when set, dxe channel 1 interrupt is ORed into riva_apps_wlan_rx_data_avail interrupt. Bit 18: when set, dxe channel 2 interrupt is ORed into riva_apps_wlan_rx_data_avail interrupt. Bit 19: when set, dxe channel 3 interrupt is ORed into riva_apps_wlan_rx_data_avail interrupt. Bit 20: when set, dxe channel 4 interrupt is ORed into riva_apps_wlan_rx_data_avail interrupt. Bit 21: when set, dxe channel 5 interrupt is ORed into riva_apps_wlan_rx_data_avail interrupt. Bit 22: when set, dxe channel 6 interrupt is ORed into riva_apps_wlan_rx_data_avail interrupt. Reset State: 0x00000000
6:0	XFER_DONE_DXE_CHANNEL_SELECT	Bit 0: when set, dxe channel 0 interrupt is ORed into riva_apps_wlan_data_xfer_done interrupt. Bit 1: when set, dxe channel 1 interrupt is ORed into riva_apps_wlan_data_xfer_done interrupt. Bit 2: when set, dxe channel 2 interrupt is ORed into riva_apps_wlan_data_xfer_done interrupt. Bit 3: when set, dxe channel 3 interrupt is ORed into riva_apps_wlan_data_xfer_done interrupt. Bit 4: when set, dxe channel 4 interrupt is ORed into riva_apps_wlan_data_xfer_done interrupt. Bit 5: when set, dxe channel 5 interrupt is ORed into riva_apps_wlan_data_xfer_done interrupt. Bit 6: when set, dxe channel 6 interrupt is ORed into riva_apps_wlan_data_xfer_done interrupt. Reset State: 0x00000000

0x3000314 CCU_CCU_DXE_INT_SELECT_STATUS

Type: read-only
Reset State: 0x00000000

The pending DXE interrupts that generate the xfer done and rx data avail apss interrupts

CCU_CCU_DXE_INT_SELECT_STATUS

Bits	Name	Description
22:16	RX_DATA_AVAIL_DXE_CHANNEL_STATUS	Bit 16: when set, dxe channel 0 interrupt is setting riva_apps_wlan_rx_data_avail interrupt. Bit 17: when set, dxe channel 1 interrupt is setting riva_apps_wlan_rx_data_avail interrupt. Bit 18: when set, dxe channel 2 interrupt is setting riva_apps_wlan_rx_data_avail interrupt. Bit 19: when set, dxe channel 3 interrupt is setting riva_apps_wlan_rx_data_avail interrupt. Bit 20: when set, dxe channel 4 interrupt is setting riva_apps_wlan_rx_data_avail interrupt. Bit 21: when set, dxe channel 5 interrupt is setting riva_apps_wlan_rx_data_avail interrupt. Bit 22: when set, dxe channel 6 interrupt is setting riva_apps_wlan_rx_data_avail interrupt. Reset State: 0x00000000

CCU_CCU_DXE_INT_SELECT_STATUS (cont.)

Bits	Name	Description
6:0	XFER_DONE_DXE_CHANNEL_STATUS	Bit 0: when set, dxe channel 0 interrupt is setting riva_apps_wlan_data_xfer_done interrupt. Bit 1: when set, dxe channel 1 interrupt is setting riva_apps_wlan_data_xfer_done interrupt. Bit 2: when set, dxe channel 2 interrupt is setting riva_apps_wlan_data_xfer_done interrupt. Bit 3: when set, dxe channel 3 interrupt is setting riva_apps_wlan_data_xfer_done interrupt. Bit 4: when set, dxe channel 4 interrupt is setting riva_apps_wlan_data_xfer_done interrupt. Bit 5: when set, dxe channel 5 interrupt is setting riva_apps_wlan_data_xfer_done interrupt. Bit 6: when set, dxe channel 6 interrupt is setting riva_apps_wlan_data_xfer_done interrupt. Reset State: 0x00000000

0x3000318 CCU_CCU_ASIC_INT_ENABLE

Type: read-write
Reset State: 0x00000000

The interrupt enables for generating apss interrupt: riva_apss_asic_interrupt

CCU_CCU_ASIC_INT_ENABLE

Bits	Name	Description
22	DXE_CHANNEL6_ENABLE	When set, dxe channel 6 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000
21	DXE_CHANNEL5_ENABLE	When set, dxe channel 5 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000
20	DXE_CHANNEL4_ENABLE	When set, dxe channel 4 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000
19	DXE_CHANNEL3_ENABLE	When set, dxe channel 3 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000
18	DXE_CHANNEL2_ENABLE	When set, dxe channel 2 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000
17	DXE_CHANNEL1_ENABLE	When set, dxe channel 1 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000
16	DXE_CHANNEL0_ENABLE	When set, dxe channel 0 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000

CCU_CCU_ASIC_INT_ENABLE (cont.)

Bits	Name	Description
15:12	CCU_SPARE	Reserved Reset State: 0x00000000
11	MAC_HOST_INTR_EN	When set, it enables the MAC-HOST interrupt (generated from MCU register: MAC_HOST_INT_(MASKED)_STATUS) Reset State: 0x00000000
10	ADU_ERR_WQ10_WQ13_DAVAIL_INTR_EN	When set, it enables the ADU error WQ10 or WQ13 data available interrupt. Reset State: 0x00000000
9	DPU_ERR_WQ8_WQ9_DAVAIL_INTR_EN	When set, it enables the DPU error WQ8 or WQ9 data available interrupt. Reset State: 0x00000000
8	MTU_TIMER_3_INTR_EN	When set, it enables the MTU timer 3 timeout interrupt. Reset State: 0x00000000
7	MTU_TIMER_2_INTR_EN	When set, it enables the MTU timer 2 timeout interrupt. Reset State: 0x00000000
6:3	SYS_MB_INTR_EN	When each bit is set, it enables the corresponding SYS MB interrupt. Bit3: MCU MB0 Bit4: MCU MB1, etc Reset State: 0x00000000
2	DPU_MIC_ERR_INTR_EN	When set, it enables the DPU MIC error interrupt. Reset State: 0x00000000
1	WATCHDOG_INTR_2_EN	When set, it enables the watchdog timer 2 event interrupt. Reset State: 0x00000000
0	CCU_SPARE2	Reserved Reset State: 0x00000000

0x300031C CCU_CCU_ASIC_INT_STATUS

Type: read-only
Reset State: 0x00000000

The (enable masked) status of all inputs generating apss interrupt: riva_apss_asic_interrupt

CCU_CCU_ASIC_INT_STATUS

Bits	Name	Description
22	DXE_CHANNEL6_STATUS	When set, dxe channel 6 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000
21	DXE_CHANNEL5_STATUS	When set, dxe channel 5 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000

CCU_CCU_ASIC_INT_STATUS (cont.)

Bits	Name	Description
20	DXE_CHANNEL4_STATUS	When set, dxe channel 4 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000
19	DXE_CHANNEL3_STATUS	When set, dxe channel 3 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000
18	DXE_CHANNEL2_STATUS	When set, dxe channel 2 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000
17	DXE_CHANNEL1_STATUS	When set, dxe channel 1 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000
16	DXE_CHANNEL0_STATUS	When set, dxe channel 0 interrupt will set riva_apss_asic_intr interrupt. Reset State: 0x00000000
11	MAC_HOST_INTR	When set, the MAC-HOST interrupt (generated from MCU register: MAC_HOST_INT_(MASKED)_STATUS is pending Reset State: 0x00000000
10	ADU_ERR_WQ10_WQ13_DAVAIL_INTR	When set, it indicates that the ADU error WQ10 or WQ13 data available interrupt occurs. Reset State: 0x00000000
9	DPU_ERR_WQ8_WQ9_DAVAIL_INTR	When set, it indicates that the DPU error WQ8 or WQ9 data available interrupt occurs. Reset State: 0x00000000
8	MTU_TIMER_3_INTR	When set, it indicates that the MTU timer 3 timeout interrupt occurs. Reset State: 0x00000000
7	MTU_TIMER_2_INTR	When set, it indicates that the MTU timer 2 timeout interrupt occurs. Reset State: 0x00000000
6:3	SYS_MB_INTR	When each bit is set, it indicates that the corresponding SYS MB interrupt occurs. Reset State: 0x00000000
2	DPU_MIC_ERR_INTR	When set, it indicates that a DPU MIC error interrupt occurs. Reset State: 0x00000000
1	WATCHDOG_2_EVENT_INTR	When set, it indicates that the watchdog timer 2 event interrupt occurs. Reset State: 0x00000000

0x3000320 CCU_TESTMUX_CONTROL1

Type: read-write
Reset State: 0x00000000

The register contains several controls for the testmux module. The output of the testmux module feeds into two testbusses: one going to the trace module, the other one going to the riva testbus (leaving Riva)

CCU_TESTMUX_CONTROL1

Bits	Name	Description
20:16	RIVA_TRACE_TESTBUS_SEL	This controls the selection of the testbus going to the trace module 5'h00: No testbus selected: output is zero 5'h01: Width reduced AHB clock domain testbus 5'h02: Width reduced phydbg clock domain testbus 5'h03: Width reduced 19.2 clock domain testbus 5'h04: Width reduced mac phy clock domain testbus 5'h04: Width reduced 32m clock domain testbus 5'h05 - 5'h1e: Reserved 5'h1f: Value: 29'h01234567 Reset State: 0x00000000
12:8	RIVA_TESTBUS_SEL	This control the testbus selection of the signals on the riva testbus, leaving riva 5'h00: No testbus selected: output is zero 5'h01: Width reduced AHB clock domain testbus 5'h02: Width reduced phydbg clock domain testbus 5'h03: Width reduced 19.2 clock domain testbus 5'h04: Width reduced mac phy clock domain testbus 5'h04: Width reduced 32m clock domain testbus 5'h05 - 5'h1e: Reserved 5'h1f: Value: 32'h76543210 Reset State: 0x00000000
0	TESTMUX_TRC_ENABLE	When set, the test muxing logic generating testbus inputs into the trace module is enabled Reset State: 0x00000000

0x3000324 CCU_TESTMUX_CONTROL2

Type: read-write
Reset State: 0x00000000

The register contains several controls for the testmux module. The output of the testmux module feeds into two testbusses: one going to the trace module, the other one going to the riva testbus (leaving Riva)

CCU_TESTMUX_CONTROL2

Bits	Name	Description
29:28	A32MCLK_TESTBUS_BUSRED_SEL	Selects the bus width reduction bit shifting option for the 32m testbus Reset State: 0x00000000

CCU_TESTMUX_CONTROL2 (cont.)

Bits	Name	Description
25:24	MAC160CLK_TESTBUS_BUSRED_SEL	Selects the bus width reduction bit shifting option for the mac phy clock domain testbus Reset State: 0x00000000
21:20	A19P2CLK_TESTBUS_BUSRED_SEL	Selects the bus width reduction bit shifting option for the 19.2 clock domain testbus Reset State: 0x00000000
17:16	A19P2CLK_TESTBUS_SEL	Selects the 19.2 clock domain testbus Reset State: 0x00000000
13:12	PHYDBGCLK_TESTBUS_BUSRED_SEL	phydbgclk_testbus_busred_sel Reset State: 0x00000000
9:8	PHYDBGCLK_TESTBUS_SEL	phydbgclk_testbus_sel Reset State: 0x00000000
5:4	AHBCLK_TESTBUS_BUSRED_SEL	ahbclk_testbus_busred_sel Reset State: 0x00000000
3:0	AHBCLK_TESTBUS_SEL	ahbclk_testbus_sel Reset State: 0x00000000

16.2.6 ccu_uart

0x3000000 CCU_UART_UART_RBR

Type: read-only
Reset State: 0x00000000

Receive Buffer Register

CCU_UART_UART_RBR

Bits	Name	Description
7:0	VALUE	Reset State: 0x00000000

0x3000004 CCU_UART_UART_DLH

Type: read-write
Reset State: 0x00000000

Divisor Latch High Register

CCU_UART_UART_DLH

Bits	Name	Description
7:0	VALUE	Reset State: 0x00000000

0x3000008 CCU_UART_UART_IIR

Type: read-only
Reset State: 0x00000000

Interrupt Identify Register

CCU_UART_UART_IIR

Bits	Name	Description
7:6	FEN	Reset State: 0x00000000
3:0	ID	Reset State: 0x00000000

0x300000C CCU_UART_UART_LCR

Type: read-write
Reset State: 0x00000000

Line Control Register

CCU_UART_UART_LCR

Bits	Name	Description
7	DLAB	Reset State: 0x00000000
6	BREAK	Reset State: 0x00000000
4	EPS	Reset State: 0x00000000
3	PEN	Reset State: 0x00000000
2	STOP	Reset State: 0x00000000
1:0	DLS	Reset State: 0x00000000

0x3000010 CCU_UART_UART_MCR

Type: read-write
Reset State: 0x00000000

Modem Control Register

CCU_UART_UART_MCR

Bits	Name	Description
5	AFCE	Reset State: 0x00000000
4	LOOPBACK	Reset State: 0x00000000
3	OUT2	Reset State: 0x00000000
2	OUT1	Reset State: 0x00000000
1	RTS	Reset State: 0x00000000
0	DTR	Reset State: 0x00000000

0x3000014 CCU_UART_UART_LSR

Type: read-only
Reset State: 0x00000060

Line Status Register

CCU_UART_UART_LSR

Bits	Name	Description
7	RFE	Reset State: 0x00000000
6	TEMPT	Reset State: 0x00000001
5	THRE	Reset State: 0x00000001
4	BI	Reset State: 0x00000000
3	FE	Reset State: 0x00000000
2	PE	Reset State: 0x00000000
1	OE	Reset State: 0x00000000
0	DR	Reset State: 0x00000000

0x3000018 CCU_UART_UART_MSR

Type: read-only
Reset State: 0x00000011

Modem Status Register

CCU_UART_UART_MSR

Bits	Name	Description
7	DCD	Reset State: 0x00000000
6	RI	Reset State: 0x00000000
5	DSR	Reset State: 0x00000000
4	CTS	Reset State: 0x00000001
3	DDCD	Reset State: 0x00000000
2	TERI	Reset State: 0x00000000
1	DDSR	Reset State: 0x00000000
0	DCTS	Reset State: 0x00000001

0x300001C CCU_UART_UART_SCRATCH

Type: read-write
Reset State: 0x00000000

Scratch Pad Register

CCU_UART_UART_SCRATCH

Bits	Name	Description
7:0	SCRATCH	Reset State: 0x00000000

0x3000070 CCU_UART_UART_FAR

Type: read-only
Reset State: 0x00000000

FIFO Access Register

CCU_UART_UART_FAR

Bits	Name	Description
0	FAR	Reset State: 0x00000000

0x300007C CCU_UART_UART_USR

Type: read-only
Reset State: 0x00000000

UART Status Register

CCU_UART_UART_USR

Bits	Name	Description
0	BUSY	Reset State: 0x00000000

0x30000A4 CCU_UART_UART_HTX

Type: read-write
Reset State: 0x00000000

Halt TX Register

CCU_UART_UART_HTX

Bits	Name	Description
0	HALT	Reset State: 0x00000000

0x30000A8 CCU_UART_UART_DMASA

Type: read-only
Reset State: 0x00000000

DMA Software Acknowledge Register

CCU_UART_UART_DMASA

Bits	Name	Description
0	ACK	Reset State: 0x00000000

16.2.7 cdahb

0x3000000 CDAHB_CDAHB_RRI_PL

Type: read-write
Reset State: 0x00000001

cdahb Arbiter arbitration priority level for rri master. In the cdahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CDAHB_CDAHB_RRI_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for rri master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cdahb arbiter will prevent a master from disabling itself. Reset State: 0x00000001

0x3000004 CDAHB_CDAHB_FDBR_PL

Type: read-write
Reset State: 0x00000005

cdahb Arbiter arbitration priority level for fdbr master. In the cdahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CDAHB_CDAHB_FDBR_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for fdbr master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cdahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x3000008 CDAHB_CDAHB_CCPU_PL

Type: read-write
Reset State: 0x00000005

cdahb Arbiter arbitration priority level for ccpu master. In the cdahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CDAHB_CDAHB_CCPU_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for ccpu master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cdahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x300000C CDAHB_CDAHB_DBR_PL

Type: read-write
Reset State: 0x00000001

cdahb Arbiter arbitration priority level for dbr master. In the cdahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CDAHB_CDAHB_DBR_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for dbr master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cdahb arbiter will prevent a master from disabling itself. Reset State: 0x00000001

0x3000010 CDAHB_CDAHB_TIC_PL

Type: read-write
Reset State: 0x00000005

cdahb Arbiter arbitration priority level for tic master. In the cdahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CDAHB_CDAHB_TIC_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for tic master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cdahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x3000014 CDAHB_CDAHB_DXE_PL

Type: read-write
Reset State: 0x00000001

cdahb Arbiter arbitration priority level for dxe master. In the cdahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CDAHB_CDAHB_DXE_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for dxe master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cdahb arbiter will prevent a master from disabling itself. Reset State: 0x00000001

0x3000048 CDAHB_CDAHB_DFLT_MST

Type: read-write
Reset State: 0x00000000

This register identifies the default master for the cdahb

CDAHB_CDAHB_DFLT_MST

Bits	Name	Description
3:0	DFT_MST	Default Master ID number register. The default master is the master that is granted by the bus when no master has requested ownership. NOTE: Writing anything beyond the 4 R/W bits will cause the entire write to be discarded. 0x0: DMY 0x1: RRI 0x2: FDBR 0x3: CCPU 0x4: DBR 0x5: TIC 0x6: DXE Reset State: 0x00000000

0x3000090 CDAHB_CDAHB_VERSION

Type: read-only
Reset State: 0x3230382A

ASCII value for each number in the version, followed by '*'. For example 32_30_31_2A represents the version 2.01*.

CDAHB_CDAHB_VERSION

Bits	Name	Description
31:24	CDAHB_COMP_VERSION_BYTE3	Reset State: 0x00000032

CDAHB_CDAHB_VERSION (cont.)

Bits	Name	Description
23:16	CDAHB_COMP_VERSION_BYTE2	Reset State: 0x00000030
15:8	CDAHB_COMP_VERSION_BYTE1	Reset State: 0x00000038
7:0	CDAHB_COMP_VERSION_BYTE0	Reset State: 0x0000002A

16.2.8 cmem

0x3000000 CMEM_CMEM_INT

Type: read-only
Reset State: 0x00000000

Interrupts in CMEM.

CMEM_CMEM_INT

Bits	Name	Description
23:20	INVALID_MASTER_ID_DAHB	AHB master ID that has caused invalid address access in DAHB Reset State: 0x00000000
19:16	INVALID_MASTER_ID_CAHB	AHB master ID that has caused invalid address access in CAHB Reset State: 0x00000000
3	CMEM_ACPU_INVALID_RADDR_INT	Invalid read address access from CPU port interrupt. Reset State: 0x00000000
2	CMEM_ACPU_INVALID_WADDR_INT	Invalid write address access from CPU port interrupt. Reset State: 0x00000000
1	CMEM_DAHB_INVALID_ADDR_INT	Invalid address access from DAHB port interrupt. Reset State: 0x00000000
0	CMEM_CAHB_INVALID_ADDR_INT	Invalid address access from CAHB port interrupt. Reset State: 0x00000000

0x3000004 CMEM_CMEM_INT_EN

Type: read-write
Reset State: 0x00000000

Enable assertion of interrupt

CMEM_CMEM_INT_EN

Bits	Name	Description
3	CMEM_ACPU_INVALID_RADDR_INT_EN	Enable invalid read address access from CPU interrupt. Reset State: 0x00000000
2	CMEM_ACPU_INVALID_WADDR_INT_EN	Enable invalid write address access from CPU interrupt. Reset State: 0x00000000
1	CMEM_DAHB_INVALID_ADDR_INT_EN	Enable invalid address access from DAHB interrupt. Reset State: 0x00000000
0	CMEM_CAHB_INVALID_ADDR_INT_EN	Enable invalid address access from CAHB interrupt. Reset State: 0x00000000

0x3000008 CMEM_CMEM_INT_CLR

Type: read-write
Reset State: 0x00000000

Clear the interrupts status bit.

CMEM_CMEM_INT_CLR

Bits	Name	Description
3	CMEM_ACPU_INVALID_RADDR_INT_CLR	Clear invalid read address access from CPU interrupt. Reset State: 0x00000000
2	CMEM_ACPU_INVALID_WADDR_INT_CLR	Clear invalid write address access from CPU interrupt. Reset State: 0x00000000
1	CMEM_DAHB_INVALID_ADDR_INT_CLR	Clear invalid address access from DAHB interrupt. Reset State: 0x00000000
0	CMEM_CAHB_INVALID_ADDR_INT_CLR	Clear invalid address access from CAHB interrupt. Reset State: 0x00000000

0x300000C CMEM_CMEM_MEM_CFG

Type: read-write
Reset State: 0x00280000

Memory rdOnly

CMEM_CMEM_MEM_CFG

Bits	Name	Description
31:16	CMEM_LRAM_KBYTES	Memory configuration Reset State: 0x00000028
3:0	MEM_CFG	Reset State: 0x00000000

0x3000010 CMEM_CMEM_TRANSBLK_CODE

Type: read-write
Reset State: 0x00000000

Unlock the access to transblk_start_addr, transblk_end_addr and transblk_port_en registers by writing 32'hA1A602E7

CMEM_CMEM_TRANSBLK_CODE

Bits	Name	Description
31:0	CMEM_TRANSBLK_CODE	Transaction blocking write-access code. Reset State: 0x00000000

0x3000014 CMEM_CMEM_TRANSBLK_START_ADDR

Type: read-write
Reset State: 0x00000000

Starting address of transfer block region in memory.

CMEM_CMEM_TRANSBLK_START_ADDR

Bits	Name	Description
31:10	CMEM_TRANSBLK_START_ADDR	starting address of transfer block region in kbytes Reset State: 0x00000000

0x3000018 CMEM_CMEM_TRANSBLK_END_ADDR

Type: read-write
Reset State: 0x00000000

Ending address of transfer block region in memory.

CMEM_CMEM_TRANSBLK_END_ADDR

Bits	Name	Description
31:10	CMEM_TRANSBLK_END_ADDR	ending address of transfer block region in kbytes Reset State: 0x00000000

0x300001C CMEM_CMEM_TRANSBLK_PORT_EN

Type: read-write
Reset State: 0x00000000

transfer block enable for each port.

CMEM_CMEM_TRANSBLK_PORT_EN

Bits	Name	Description
23:20	CMEM_TRANSBLK_MSTID1	second AHB master ID blocked from accessing blocked region. valid only when cmem_transblk_mstid1_vld is set to 1. Reset State: 0x00000000
19:16	CMEM_TRANSBLK_MSTID0	first AHB master ID blocked from accessing blocked region. valid only when cmem_transblk_mstid0_vld is set to 1. Reset State: 0x00000000
3	CMEM_TRANSBLK_MSTID1_VLD	cmem_transblk_mstid1 is valid Reset State: 0x00000000
2	CMEM_TRANSBLK_MSTID0_VLD	cmem_transblk_mstid0 is valid Reset State: 0x00000000
1:0	CMEM_TRANSBLK_PORT_EN	transfer block enable for each port Reset State: 0x00000000

0x3000020 CMEM_CMEM_ARB_POLICY

Type: read-write
Reset State: 0x00000000

Arbitration policy when two AHB ports are active

CMEM_CMEM_ARB_POLICY

Bits	Name	Description
28:24	CMEM_ACPU_PRTY	CPU port priority for each 5 SRAM block.Bit 1 corresponds to SRAM_1. Reset State: 0x00000000

CMEM_CMEM_ARB_POLICY (cont.)

Bits	Name	Description
20:16	CMEM_DAHB_PRTY	DAHB port priority for each 5 SRAM block.Bit 1 corresponds to SRAM_1. Reset State: 0x00000000
12:8	CMEM_CAHB_PRTY	CAHB port priority for each 5 SRAM block.Bit 1 corresponds to SRAM_1. Reset State: 0x00000000
5:1	CMEM_LRAM_ARB_POLICY	Arbitration for each 5 SRAM block.Bit 1 corresponds to SRAM_1(128KB).Obsolete. Reset State: 0x00000000
0	CMEM_AHB_ARB_POLICY	Arbitration policy. 0x0: PRR 0x1: SRR Reset State: 0x00000000

0x3000024 CMEM_CMEM_TEST_OUT_SEL

Type: read-write
Reset State: 0x00000000

testbus output selection.

CMEM_CMEM_TEST_OUT_SEL

Bits	Name	Description
31:0	TEST_OUT_SEL	testbus output selection. bit[2:0] - cmem_test_sel. 0 - sel aap0 (CAHB) 1 - sel aap1 (DAHB) 2 - sel mmx 3 - sel lram bit[6:4] - aap_test_sel bit[10:8] - mmx_test_sel bit[14:12] - lram_test_sel bit[18:16] - ahb_dec_test_sel bit[22:20] - regs_test_sel bit[26:24] - cpu_dec_test_sel bit[28] - cmem_test_en Reset State: 0x00000000

0x3000028 CMEM_CMEM_ACC

Type: read-write
Reset State: 0x00000000

acc[7:0] control to 1mbit RAMs

CMEM_CMEM_ACC

Bits	Name	Description
7:0	ACC	acc[7:0] control to 1mbit RAMs. Obsolete. Reset State: 0x00000000

0x300002C CMEM_CMEM_CAHB_INVALID_ADDR

Type: read-only
Reset State: 0x00000000

The last invalid address CAHB port accessed

CMEM_CMEM_CAHB_INVALID_ADDR

Bits	Name	Description
31:0	CMEM_CAHB_INVALID_ADDR	Stored invalid address that CAHB port access recently. Reset State: 0x00000000

0x3000030 CMEM_CMEM_DAHB_INVALID_ADDR

Type: read-only
Reset State: 0x00000000

The last invalid address DAHB port accessed

CMEM_CMEM_DAHB_INVALID_ADDR

Bits	Name	Description
31:0	CMEM_DAHB_INVALID_ADDR	Stored invalid address that DAHB port access recently. Reset State: 0x00000000

0x3000034 CMEM_CMEM_ACPU_INVALID_ADDR

Type: read-only
Reset State: 0x00000000

The last invalid address CPU port accessed

CMEM_CMEM_ACPU_INVALID_ADDR

Bits	Name	Description
31:0	CMEM_ACPU_INVALID_ADDR	Stored invalid address that CPU port access recently. Reset State: 0x00000000

0x3000038 CMEM_CMEM_CNT_CTRL

Type: read-write
Reset State: 0x00000000

This register controls the cmem counters

CMEM_CMEM_CNT_CTRL

Bits	Name	Description
1	CMEM_CNT_CLR	Clear the cmem counters to 0. Reset State: 0x00000000
0	CMEM_CNT_EN	Enable the cmem counters to increment. Reset State: 0x00000000

0x300003C CMEM_CMEM_CAHB_BUSY_CNT

Type: read-only
Reset State: 0x00000000

32-bit of cmem_cahb_busy_cnt

CMEM_CMEM_CAHB_BUSY_CNT

Bits	Name	Description
31:0	CMEM_CAHB_BUSY_CNT	Number of AHB clock cycle while CAHB port is busy. Reset State: 0x00000000

0x3000040 CMEM_CMEM_CAHB_IDLE_CNT

Type: read-only
Reset State: 0x00000000

32-bit of cmem_cahb_idle_cnt

CMEM_CMEM_CAHB_IDLE_CNT

Bits	Name	Description
31:0	CMEM_CAHB_IDLE_CNT	Number of AHB clock cycle while CAHB port is idle. Reset State: 0x00000000

0x3000044 CMEM_CMEM_CAHB_ACTIVE_CNT

Type: read-only
Reset State: 0x00000000

32-bit of cmem_cahb_active_cnt

CMEM_CMEM_CAHB_ACTIVE_CNT

Bits	Name	Description
31:0	CMEM_CAHB_ACTIVE_CNT	Number of AHB clock cycle while CAHB port is busy and active. Reset State: 0x00000000

0x3000048 CMEM_CMEM_DAHB_BUSY_CNT

Type: read-only
Reset State: 0x00000000

32-bit of cmem_dahb_busy_cnt

CMEM_CMEM_DAHB_BUSY_CNT

Bits	Name	Description
31:0	CMEM_DAHB_BUSY_CNT	Number of AHB clock cycle while DAHB port is busy. Reset State: 0x00000000

0x300004C CMEM_CMEM_DAHB_IDLE_CNT

Type: read-only
Reset State: 0x00000000

32-bit of cmem_dahb_idle_cnt

CMEM_CMEM_DAHB_IDLE_CNT

Bits	Name	Description
31:0	CMEM_DAHB_IDLE_CNT	Number of AHB clock cycle while DAHB port is idle. Reset State: 0x00000000

0x3000050 CMEM_CMEM_DAHB_ACTIVE_CNT

Type: read-only
Reset State: 0x00000000

32-bit of cmem_dahb_active_cnt

CMEM_CMEM_DAHB_ACTIVE_CNT

Bits	Name	Description
31:0	CMEM_DAHB_ACTIVE_CNT	Number of AHB clock cycle while DAHB port is busy and active. Reset State: 0x00000000

0x3000054 CMEM_CMEM_ACPU_BUSY_CNT

Type: read-only
Reset State: 0x00000000

32-bit of cmem_acpu_busy_cnt

CMEM_CMEM_ACPU_BUSY_CNT

Bits	Name	Description
31:0	CMEM_ACPU_BUSY_CNT	Number of ACPU clock cycle while CPU memory port is busy. Reset State: 0x00000000

0x3000058 CMEM_CMEM_ACPU_IDLE_CNT

Type: read-only
Reset State: 0x00000000

32-bit of cmem_acpu_idle_cnt

CMEM_CMEM_ACPU_IDLE_CNT

Bits	Name	Description
31:0	CMEM_ACPU_IDLE_CNT	Number of ACPU clock cycle while CPU memory port is busy. Reset State: 0x00000000

0x300005C CMEM_CMEM_ACPU_ACTIVE_CNT

Type: read-only
Reset State: 0x00000000

32-bit of cmem_acpu_active_cnt

CMEM_CMEM_ACPU_ACTIVE_CNT

Bits	Name	Description
31:0	CMEM_ACPU_ACTIVE_CNT	Number of ACPU clock cycle while CPU memory port is busy and active. Reset State: 0x00000000

0x3000060 CMEM_CMEM_TESTBUS_HI

Type: read-only
Reset State: 0x00000000

The upper 13-bit of cmem_testbus

CMEM_CMEM_TESTBUS_HI

Bits	Name	Description
12:0	CMEM_TESTBUS_HI	Upper 13-bit of cmem_testbus. cmem_testbus[44:32]. Reset State: 0x00000000

0x3000064 CMEM_CMEM_TESTBUS_LO

Type: read-only
Reset State: 0x00000000

The lower 32-bit of cmem_testbus

CMEM_CMEM_TESTBUS_LO

Bits	Name	Description
31:0	CMEM_TESTBUS_LO	Lower 32-bit of cmem_testbus. cmem_testbus[31:0]. Reset State: 0x00000000

0x3000068 CMEM_CMEM_CLK_GATE

Type: read-write
Reset State: 0x00010104

disable control for top cmem clock gates

CMEM_CMEM_CLK_GATE

Bits	Name	Description
23:16	GAS_BUSY_MSK	number of cycles that gas_busy enables the clock after it is de-asserted. Reset State: 0x00000001
15:8	AHB_BUSY_MSK	number of cycles that ahb_busy enables the clock after it is de-asserted. Reset State: 0x00000001
7	DAHB_ABORT_HAPPENED	indication of abort happened. Reset State: 0x00000000
6	DAHB_ABORT_CLR	clear abort_happened Reset State: 0x00000000
5	CAHB_ABORT_HAPPENED	indication of abort happened. Reset State: 0x00000000
4	CAHB_ABORT_CLR	clear abort_happened Reset State: 0x00000000
3	CMEM_RD_CLK_GATE_DISABLE	Disable read path clock gate. Reset State: 0x00000000
2	CMEM_MEM_CLK_GATE_DISABLE	Disable top clock gate for memory clock. Reset State: 0x00000001
1	CMEM_ACPU_CLK_GATE_DISABLE	Disable top clock gate for 40/80MHz ACPU clock. Reset State: 0x00000000
0	CMEM_AHB_CLK_GATE_DISABLE	Disable top clock gate for 40MHz AHB clock. Reset State: 0x00000000

0x300006C CMEM_CMEM_CAHB_RX_CTL

Type: read-write
Reset State: 0x00000000

various control for CAHB rx fifo and data path

CMEM_CMEM_CAHB_RX_CTL

Bits	Name	Description
2	CMEM_RX_CLR_ON_CMD_EN	when the bit is set, rx path is cleared when new transaction starts. Reset State: 0x00000000
1	CMEM_RX_CLR	clear the RX FIFO and the read data path Reset State: 0x00000000
0	CMEM_RX_FIFO_CLR	clear the RX FIFO Reset State: 0x00000000

0x3000070 CMEM_CMEM_DAHB_RX_CTL

Type: read-write
Reset State: 0x00000000

various control for DAHB rx fifo and data path

CMEM_CMEM_DAHB_RX_CTL

Bits	Name	Description
2	CMEM_RX_CLR_ON_CMD_EN	when the bit is set, rx path is cleared when new transaction starts. Reset State: 0x00000000
1	CMEM_RX_CLR	clear the RX FIFO and the read data path Reset State: 0x00000000
0	CMEM_RX_FIFO_CLR	clear the RX FIFO Reset State: 0x00000000

16.2.9 DXE_0

0x3000000 DXE_0_DMA_CSR

Type: read-write
Reset State: 0x00004E50

The DMA Control and status Register (DMA_CSR) is used for configuration settings that, in general, apply to all the DMA channels.

DXE_0_DMA_CSR

Bits	Name	Description
31:18	RESERVED	Reserved. Writes ignored, reads will return 0.
16	H2H_SYNC_EN	When set, DXE will wait for confirmation from MIF that H2H written data has made it all the way out to memory before continuing with the transfers. This will slow things down but guarantee that the data is always consistent no matter what MIF port is used to write it or read it back. When clear, as long as the data is read from the same MIF port from which it was written, MIF will guarantee that data coherency without the need to wait. Reset State: 0x00000000
15	PAUSED	This status bit will be set when as a result of setting the pause request bit (PAUSE), the state machine has completed any ongoing chunk transfer, released the AHB interfaces, and entered the pause state. This will bit be cleared when as a result of clearing the pause request bit (PAUSE), the state machine has gone back to processing any outstanding transfers or else it has gone back to the IDLE state to wait for new transfer requests.
14	ECTR_EN	Event Counter Enable. When set the event counters will be enabled. Reset State: 0x00000001
13:9	B2H_TSTMP_OFF	Timestamp Offset. This bit field specifies the offset (multiple of 4 bytes) to be used for writing the start and end timestamps in the BD for B2H type transfers Reset State: 0x00000007
8:4	H2B_TSTMP_OFF	Timestamp Offset. This bit field specifies the offset (multiple of 4 bytes) to be used for writing the start and end timestamps in the BD for H2B transfers. Reset State: 0x00000005
3	TSTMP_EN	Timestamp Enable. When set, this bit enables the writing of start and end timestamps for H2B and B2H transfers. The timestamps will be written in the BD at the offset specified by the setting of the TMSTMP_OFF bit field as two consecutive 32-bit starting with the start timestamp. When this bit is cleared no timestamps will be written to the BD. Reset State: 0x00000000
2	RESET	Soft reset for DMA engine
1	PAUSE	Pause the DMA engine. The engine will stop as soon as the next chunk transfer is complete so no data will be lost. It will also release the AHB interfaces. No progress will be made until software clears this bit. Reset State: 0x00000000
0	EN	Enables the DMA engine Reset State: 0x00000000

0x3000004 DXE_0_DMA_ENCH

Type: write-only

This register is write-only and provides a convenient way for software to enable one or more channels with a single register write. When writing to this register, each data bit set HIGH causes the corresponding CH_CSR[EN] bit in the channel to be set thereby enabling the channel. Data bits that are low have no effect in their corresponding channel CSR[EN] bits.

DXE_0_DMA_ENCH

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_EN	Enable channel 6.
5	CH5_EN	Enable channel 5.
4	CH4_EN	Enable channel 4.
3	CH3_EN	Enable channel 3.
2	CH2_EN	Enable channel 2.
1	CH1_EN	Enable channel 1.
0	CH0_EN	Enable channel 0.

0x3000008 DXE_0_DMA_CH_EN

Type: read-only

This register is read-only and indicates which DMA channels are enabled. Each bit in this register reflects the status of the corresponding EN bit in each of the channels' CHn_CSRs. As such, used in combination with DMA_DONE, it provides a convenient way for software to determine which channels are available for a new DMA operation.

DXE_0_DMA_CH_EN

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_EN	Enable (EN) bit status for DMA Channel 6 in CH6_CSR.
5	CH5_EN	Enable (EN) bit status for DMA Channel 5 in CH5_CSR.
4	CH4_EN	Enable (EN) bit status for DMA Channel 4 in CH4_CSR.
3	CH3_EN	Enable (EN) bit status for DMA Channel 3 in CH3_CSR.
2	CH2_EN	Enable (EN) bit status for DMA Channel 2 in CH2_CSR.
1	CH1_EN	Enable (EN) bit status for DMA Channel 1 in CH1_CSR.
0	CH0_EN	Enable (EN) bit status for DMA Channel 0 in CH0_CSR.

0x300000C DXE_0_DMA_CH_DONE

Type: read-only

This register is read-only and indicates which DMA channels are done with their programmed transfer, each bit in this register reflects the status of the corresponding DONE bit in each of the channels' CHn_CSRs. As such, it provides a convenient way for software to determine which channels have finished their programmed DMA operation.

DXE_0_DMA_CH_DONE

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_DONE	Done (DONE) bit for DMA Channel 6 in CH6_CSR.
5	CH5_DONE	Done (DONE) bit for DMA Channel 5 in CH5_CSR.
4	CH4_DONE	Done (DONE) bit for DMA Channel 4 in CH4_CSR.
3	CH3_DONE	Done (DONE) bit for DMA Channel 3 in CH3_CSR.
2	CH2_DONE	Done (DONE) bit for DMA Channel 2 in CH2_CSR.
1	CH1_DONE	Done (DONE) bit for DMA Channel 1 in CH1_CSR.
0	CH0_DONE	Done (DONE) bit for DMA Channel 0 in CH0_CSR.

0x3000010 DXE_0_DMA_CH_ERR

Type: read-only

This register is read-only and indicates which DMA channels have errors, each bit in this register reflects the status of the corresponding ERR bit in each of the channels' CHn_CSRs. As such, it provides a convenient way for software to determine which channels have incurred errors during operation.

DXE_0_DMA_CH_ERR

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_ERR	Error (ERR) bit for DMA Channel 6 in CH6_CSR.
5	CH5_ERR	Error (ERR) bit for DMA Channel 5 in CH5_CSR.
4	CH4_ERR	Error (ERR) bit for DMA Channel 4 in CH4_CSR.
3	CH3_ERR	Error (ERR) bit for DMA Channel 3 in CH3_CSR.
2	CH2_ERR	Error (ERR) bit for DMA Channel 2 in CH2_CSR.
1	CH1_ERR	Error (ERR) bit for DMA Channel 1 in CH1_CSR.
0	CH0_ERR	Error (ERR) bit for DMA Channel 0 in CH0_CSR.

0x3000014 DXE_0_DMA_CH_STOP

Type: read-only

This register is read-only and indicates which DMA channels have been stopped by software request, each bit in this register reflects the status of the corresponding STOP bit in each of the channels' CHn_CSRs. As such, it provides a convenient way for software to determine which channels have incurred stops during operation.

DXE_0_DMA_CH_STOP

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_STOP	Stop (STOP) bit for DMA Channel 6 in CH6_CSR.
5	CH5_STOP	Stop (STOP) bit for DMA Channel 5 in CH5_CSR.
4	CH4_STOP	Stop (STOP) bit for DMA Channel 4 in CH4_CSR.
3	CH3_STOP	Stop (STOP) bit for DMA Channel 3 in CH3_CSR.
2	CH2_STOP	Stop (STOP) bit for DMA Channel 2 in CH2_CSR.
1	CH1_STOP	Stop (STOP) bit for DMA Channel 1 in CH1_CSR.
0	CH0_STOP	Stop (STOP) bit for DMA Channel 0 in CH0_CSR.

0x3000018 DXE_0_INT_MSK

Type: read-write
Reset State: 0x00000000

The Interrupt Mask register defines the functionality of DXE's all-channel combined interrupt output. A bit set to one in the mask enables the generation of the interrupt for that source channel, a zero disables the generation of an interrupt.

DXE_0_INT_MSK

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_INTEN	Interrupt Enable. Enable DMA Channel 6 Interrupts. Reset State: 0x00000000
5	CH5_INTEN	Interrupt Enable. Enable DMA Channel 5 Interrupts. Reset State: 0x00000000
4	CH4_INTEN	Interrupt Enable. Enable DMA Channel 4 Interrupts. Reset State: 0x00000000
3	CH3_INTEN	Interrupt Enable. Enable DMA Channel 3 Interrupts. Reset State: 0x00000000

DXE_0_INT_MSK (cont.)

Bits	Name	Description
2	CH2_INTEN	Interrupt Enable. Enable DMA Channel 2 Interrupts. Reset State: 0x00000000
1	CH1_INTEN	Interrupt Enable. Enable DMA Channel 1 Interrupts. Reset State: 0x00000000
0	CH0_INTEN	Interrupt Enable. Enable DMA Channel 0 Interrupts. Reset State: 0x00000000

0x300001C DXE_0_INT_SRC_MSKD

Type: read-only

This read-only register is the bitwise AND of INT_SRC_RAW with INT_MSK. If any of its bits is a one, the DXE will generate an interrupt request to the interrupt controller.

DXE_0_INT_SRC_MSKD

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_INT	ED, Done or Error interrupt request by CH6 after masking with INT_MSK[6].
5	CH5_INT	ED, Done or Error interrupt request by CH5 after masking with INT_MSK[5].
4	CH4_INT	ED, Done or Error interrupt request by CH4 after masking with INT_MSK[4].
3	CH3_INT	ED, Done or Error interrupt request by CH3 after masking with INT_MSK[3].
2	CH2_INT	ED, Done or Error interrupt request by CH2 after masking with INT_MSK[2].
1	CH1_INT	ED, Done or Error interrupt request by CH1 after masking with INT_MSK[1].
0	CH0_INT	ED, Done or Error interrupt request by CH0 after masking with INT_MSK[0].

0x3000020 DXE_0_INT_SRC_RAW

Type: read-only

This read-only register combines the sources of all types of error interrupt requests: descriptor, done and error types. It is basically the bitwise OR of INT_ED_SRC, INT_DONE_SRC and INT_ERR_SRC

DXE_0_INT_SRC_RAW

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_INT	ED, Done or Error interrupt requested by CH6.
5	CH5_INT	ED, Done or Error interrupt requested by CH5.
4	CH4_INT	ED, Done or Error interrupt requested by CH4.
3	CH3_INT	ED, Done or Error interrupt requested by CH3.
2	CH2_INT	ED, Done or Error interrupt requested by CH2.
1	CH1_INT	ED, Done or Error interrupt requested by CH1.
0	CH0_INT	ED, Done or Error interrupt requested by CH0.

0x3000024 DXE_0_INT_ED_SRC

Type: read-only

This read-only register combines the sources of all external descriptor requested interrupts. It is the "raw" unmasked value from the channel registers.

DXE_0_INT_ED_SRC

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_ED_INT	External descriptor interrupt requested by CH6.
5	CH5_ED_INT	External descriptor interrupt requested by CH5.
4	CH4_ED_INT	External descriptor interrupt requested by CH4.
3	CH3_ED_INT	External descriptor interrupt requested by CH3.
2	CH2_ED_INT	External descriptor interrupt requested by CH2.
1	CH1_ED_INT	External descriptor interrupt requested by CH1.
0	CH0_ED_INT	External descriptor interrupt requested by CH0.

0x3000028 DXE_0_INT_DONE_SRC

Type: read-only

This read-only register combines the sources of all done interrupt requests. It is the "raw" unmasked value from the channel registers.

DXE_0_INT_DONE_SRC

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_DONE_INT	Done interrupt requested by CH6.
5	CH5_DONE_INT	Done interrupt requested by CH5.
4	CH4_DONE_INT	Done interrupt requested by CH4.
3	CH3_DONE_INT	Done interrupt requested by CH3.
2	CH2_DONE_INT	Done interrupt requested by CH2.
1	CH1_DONE_INT	Done interrupt requested by CH1.
0	CH0_DONE_INT	Done interrupt requested by CH0.

0x300002C DXE_0_INT_ERR_SRC

Type: read-only

This read-only register combines the sources of all error interrupt requests. It is the "raw" unmasked value from the channel registers.

DXE_0_INT_ERR_SRC

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_ERR_INT	Error interrupt requested by CH6.
5	CH5_ERR_INT	Error interrupt requested by CH5.
4	CH4_ERR_INT	Error interrupt requested by CH4.
3	CH3_ERR_INT	Error interrupt requested by CH3.
2	CH2_ERR_INT	Error interrupt requested by CH2.
1	CH1_ERR_INT	Error interrupt requested by CH1.
0	CH0_ERR_INT	Error interrupt requested by CH0.

0x3000030 DXE_0_INT_CLR

Type: write-only

This register is write-only and is used to clear interrupt request form either all or specific individual channels. When writing to this register, each data bit set HIGH causes the corresponding bits in the channel CSR to be cleared. All ED, DONE and ERROR source will be cleared at once. Data bits that are low have no effect on the corresponding bit in the channel CSR register.

DXE_0_INT_CLR

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_INT_CLR	Clear all interrupt sources in CH6.
5	CH5_INT_CLR	Clear all interrupt sources in CH5.
4	CH4_INT_CLR	Clear all interrupt sources in CH4.
3	CH3_INT_CLR	Clear all interrupt sources in CH3.
2	CH2_INT_CLR	Clear all interrupt sources in CH2.
1	CH1_INT_CLR	Clear all interrupt sources in CH1.
0	CH0_INT_CLR	Clear all interrupt sources in CH0.

0x3000034 DXE_0_INT_ED_CLR

Type: write-only

This register is write-only and is used to clear external descriptor interrupt requests simultaneously from either all or specific individual channels. When writing to this register, each data bit set HIGH causes the corresponding bits in the channel CSR to be cleared. Data bits that are low have no effect on the corresponding bit in the channel CSR register.

DXE_0_INT_ED_CLR

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_INT_ED_CLR	Clear ED interrupt source in CH6.
5	CH5_INT_ED_CLR	Clear ED interrupt source in CH5.
4	CH4_INT_ED_CLR	Clear ED interrupt source in CH4.
3	CH3_INT_ED_CLR	Clear ED interrupt source in CH3.
2	CH2_INT_ED_CLR	Clear ED interrupt source in CH2.
1	CH1_INT_ED_CLR	Clear ED interrupt source in CH1.
0	CH0_INT_ED_CLR	Clear ED interrupt source in CH0.

0x3000038 DXE_0_INT_DONE_CLR

Type: write-only

This register is write-only and is used to clear DONE interrupt requests simultaneously from either all or specific individual channels. When writing to this register, each data bit set HIGH causes the

corresponding bits in the channel CSR to be cleared. Data bits that are low have no effect on the corresponding bit in the channel CSR register.

DXE_0_INT_DONE_CLR

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_INT_DONE_CLR	Clear DONE interrupt source in CH6.
5	CH5_INT_DONE_CLR	Clear DONE interrupt source in CH5.
4	CH4_INT_DONE_CLR	Clear DONE interrupt source in CH4.
3	CH3_INT_DONE_CLR	Clear DONE interrupt source in CH3.
2	CH2_INT_DONE_CLR	Clear DONE interrupt source in CH2.
1	CH1_INT_DONE_CLR	Clear DONE interrupt source in CH1.
0	CH0_INT_DONE_CLR	Clear DONE interrupt source in CH0.

0x300003C DXE_0_INT_ERR_CLR

Type: write-only

This register is write-only and is used to clear ERROR interrupt requests simultaneously from either all or specific individual channels. When writing to this register, each data bit set HIGH causes the corresponding bits in the channel CSR to be cleared. Data bits that are low have no effect on the corresponding bit in the channel CSR register.

DXE_0_INT_ERR_CLR

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CH6_INT_ERR_CLR	Clear ERROR interrupt source in CH6.
5	CH5_INT_ERR_CLR	Clear ERROR interrupt source in CH5.
4	CH4_INT_ERR_CLR	Clear ERROR interrupt source in CH4.
3	CH3_INT_ERR_CLR	Clear ERROR interrupt source in CH3.
2	CH2_INT_ERR_CLR	Clear ERROR interrupt source in CH2.
1	CH1_INT_ERR_CLR	Clear ERROR interrupt source in CH1.
0	CH0_INT_ERR_CLR	Clear ERROR interrupt source in CH0.

0x3000040 DXE_0_DMA_CH_PRES

Type: read-only
Reset State: 0x0000007F

This register is read-only and indicates which DMA channels exist in the hardware.

DXE_0_DMA_CH_PRES

Bits	Name	Description
31	CH31_PRES	Channel 31 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
30	CH30_PRES	Channel 30 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
29	CH29_PRES	Channel 29 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
28	CH28_PRES	Channel 28 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
27	CH27_PRES	Channel 27 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
26	CH26_PRES	Channel 26 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
25	CH25_PRES	Channel 25 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
24	CH24_PRES	Channel 24 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
23	CH23_PRES	Channel 23 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
22	CH22_PRES	Channel 22 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
21	CH21_PRES	Channel 21 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000

DXE_0_DMA_CH_PRES (cont.)

Bits	Name	Description
20	CH20_PRES	Channel 20 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
19	CH19_PRES	Channel 19 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
18	CH18_PRES	Channel 18 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
17	CH17_PRES	Channel 17 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
16	CH16_PRES	Channel 16 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
15	CH15_PRES	Channel 15 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
14	CH14_PRES	Channel 14 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
13	CH13_PRES	Channel 13 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
12	CH12_PRES	Channel 12 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
11	CH11_PRES	Channel 11 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
10	CH10_PRES	Channel 10 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
9	CH9_PRES	Channel 9 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
8	CH8_PRES	Channel 8 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000
7	CH7_PRES	Channel 7 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000000

DXE_0_DMA_CH_PRES (cont.)

Bits	Name	Description
6	CH6_PRES	Channel 6 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000001
5	CH5_PRES	Channel 5 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000001
4	CH4_PRES	Channel 4 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000001
3	CH3_PRES	Channel 3 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000001
2	CH2_PRES	Channel 2 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000001
1	CH1_PRES	Channel 1 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000001
0	CH0_PRES	Channel 0 Present. When high signifies that the channel exists in this implementation of the HW. Reset State: 0x00000001

0x3000044 DXE_0_TSTBUS_CTRL

Type: read-write
Reset State: 0x0000000B

The Value of this register is used to control a mux that selects which set of internal DXE signals gets put on the chip-wide test bus.

DXE_0_TSTBUS_CTRL

Bits	Name	Description
31:5	RESERVED	Reserved. Writes ignored, reads will return 0.

DXE_0_TSTBUS_CTRL (cont.)

Bits	Name	Description
4:1	SEL	Controls which of the following sets gets put into the DXE testbus: 0x0: MIX 0x1: DE 0x2: ARB 0x3: GAM 0x4: GBI 0x5: GAS 0x6: FIFO_CTRL 0x7: FIFO_IN 0x8: FIFO_OUT Reset State: 0x00000005
0	EN	Enable. When enabled the flop that drives the DXE testbus will update its value every cycle, otherwise the flop outputs will remain constant. Reset State: 0x00000001

0x3000048 DXE_0_TSTBUS_LOW

Type: read-only

This register provides bits [31:0] of the DXE testbus.

DXE_0_TSTBUS_LOW

Bits	Name	Description
31:0	VALUE	

0x300004C DXE_0_TSTBUS_HIGH

Type: read-only

This register provides bits [44:32] of the DXE testbus.

DXE_0_TSTBUS_HIGH

Bits	Name	Description
31:0	VALUE	

0x3000050 DXE_0_PF_BD

Type: read-only
Reset State: 0x00000000

This read-only register contains the index of any prefetched BD index. The index is only meaningful if the accompanying valid bit is set.

DXE_0_PF_BD

Bits	Name	Description
31:17	RESERVED	Reserved. Writes ignored, reads will return 0. Reset State: 0x00000000
16	VALID	Valid. When set indicates that the INDEX bit field contains a valid BD index pointer. Reset State: 0x00000000
15:0	INDEX	BD Index.

0x3000054 DXE_0_PF_PDU

Type: read-only
Reset State: 0x00000000

This read-only register contains the index of any prefetched PDU index. The index is only meaningful if the accompanying valid bit is set.

DXE_0_PF_PDU

Bits	Name	Description
31:17	RESERVED	Reserved. Reads will return 0. Reset State: 0x00000000
16	VALID	Valid. When set indicates that the INDEX bit field contains a valid PDU index pointer. Reset State: 0x00000000
15:0	INDEX	PDU Index.

0x3000058 DXE_0_REVISION

Type: read-only
Reset State: 0x0000001D

This register's value represents the DXE RTL revision present in the hardware.

DXE_0_REVISION

Bits	Name	Description
31:0	REVID	Revision ID. Corresponds to the label number of DXE (revision of.info file) Reset State: 0x0000001D

0x300005C DXE_0_BMU_SB_QDAT_AVAIL

Type: read-only

This read-only register provides the status of BMU WQ data available sideband signals as seen by DXE.

DXE_0_BMU_SB_QDAT_AVAIL

Bits	Name	Description
31:24	RSVD	Reserved.
23:0	QDAT_AV	BMU WQ Data Aavailable.

0x3000060 DXE_0_BMU_SB_PDU_AVAIL

Type: read-only

This read-only register provides the status of BMU PDU available sideband signals as seen by DXE.

DXE_0_BMU_SB_PDU_AVAIL

Bits	Name	Description
31:10	RSVD	Reserved.
9:0	PDU_AV	BMU BD/PDU Aavailable.

0x3000064 DXE_0_STATE

Type: read-only

This read-only register provides key DXE state machine status to help debug.

DXE_0_STATE

Bits	Name	Description
31	RX_SPAVAIL	Space is available in one or more of the UIF RX endpoints
30	TX_MGMT_DAVAIL	Data is available in the UIF TX management endpoint
29	TX_DAT_DAVAIL	Data is available in the UIF TX data endpoint
28	WQ_DAVAIL	Data is available in selected BMU WQ
27	PDU_AVAIL	PDUs are available for current threshold
26:25	XFER_IDX	Id of the transfer size source that turned out to be the minimum and therefore picked as size of current transfer

DXE_0_STATE (cont.)

Bits	Name	Description
24:17	XFER_SZ	Calculated max transfer size from minimum of chunk size and space or data available in either source PDU, destination PDU, or UIF endpoint.
16:12	SEL_CH	Currently Selected Channel.
11:10	PFSM	State of prefetch engine state machine
9:8	DFSM	State of DPDMA state machine
7:6	SFSM	State of SPDMA state machine

DXE_0_STATE (cont.)

Bits	Name	Description
5:0	MFSM	State of main state machine 0x0: IDLE 0x1: H2H_START 0x2: H2H_RD 0x3: H2H_WR 0x4: H2H_UPDATE 0x5: LD_DESC 0x6: CKEDVAL 0x7: CLREDVAL 0x8: WB_CTRL 0x9: WB_SZ 0xA: WB_SADR 0xB: WB_DADR 0xC: WB_DESC 0xD: PAUSE 0xE: B2H_START 0xF: B2H_POPWQ 0x10: B2H_GET_BD_INFO 0x11: B2H_RD_BD 0x12: B2H_WR_BD 0x13: B2H_RD_PDU 0x14: B2H_WR_PDU 0x15: B2H_NXT_PDU 0x16: B2H_UPNCK_PDU 0x17: B2H_WR_TSTMP 0x18: B2H_REL_PKT 0x19: H2B_START 0x1A: H2B_GET_PDU 0x1B: H2B_RD_PDU 0x1C: H2B_WR_PDU 0x1D: H2B_LNK_PDU 0x1E: H2B_UPDT_BD1 0x1F: H2B_UPDT_BD2 0x20: H2B_PUSHWQ 0x21: ABORT 0x22: ERROR 0x23: H2B_WR_TSTMP 0x24: WR_TOT_XFER_LEN 0x25: H2B_BD_TMPLT_RD 0x26: H2B_BD_TMPLT_WR

0x3000068 DXE_0_ARB_CH_MSK

Type: read-only

This register is read-only and indicates which enabled DMA channels have been masked from active arbitration by some blocking condition

DXE_0_ARB_CH_MSK

Bits	Name	Description
31:7	RSVD	Reserved. Reads return 0
6	CH6_MSKD	When set indicates that CH6 is masked by the arbiter and is therefore currently not actively participating in the arbitration because of some blocking condition that would prevent it from making progress..
5	CH5_MSKD	When set indicates that CH5 is masked by the arbiter and is therefore currently not actively participating in the arbitration because of some blocking condition that would prevent it from making progress..
4	CH4_MSKD	When set indicates that CH4 is masked by the arbiter and is therefore currently not actively participating in the arbitration because of some blocking condition that would prevent it from making progress..
3	CH3_MSKD	When set indicates that CH3 is masked by the arbiter and is therefore currently not actively participating in the arbitration because of some blocking condition that would prevent it from making progress..
2	CH2_MSKD	When set indicates that CH2 is masked by the arbiter and is therefore currently not actively participating in the arbitration because of some blocking condition that would prevent it from making progress..
1	CH1_MSKD	When set indicates that CH1 is masked by the arbiter and is therefore currently not actively participating in the arbitration because of some blocking condition that would prevent it from making progress..
0	CH0_MSKD	When set indicates that CH0 is masked by the arbiter and is therefore currently not actively participating in the arbitration because of some blocking condition that would prevent it from making progress..

0x300006C DXE_0_UIF_SB

Type: read-only

This read-only register provides the status of important UIF sideband signals

DXE_0_UIF_SB

Bits	Name	Description
31:22	RSVD	Reserved. Writes ignored, reads will return 0.

DXE_0_UIF_SB (cont.)

Bits	Name	Description
21:14	RX_SPACE_REM_DAT_REM	Provides the number of dwords that can be written to the active Rx endpoint
13	RX4_SPAVAIL	When high means that there is space available in the Rx1 endpoint
12	RX3_SPAVAIL	When high means that there is space available in the Rx1 endpoint
11	RX2_SPAVAIL	When high means that there is space available in the Rx1 endpoint
10	RX1_SPAVAIL	When high means that there is space available in the Rx1 endpoint
9:2	TX_DAT_REM	Provides the number of dwords available in the active Tx endpoint
1	TX_MGMT_DAVAIL	When high means that there is data available in the Tx management endpoint
0	TX_DAT_DAVAIL	When high means that there is data available in the Tx data endpoint

0x3000070 DXE_0_TIMESTAMP

Type: read-only
Reset State: 0x00000046

This read-only register provides the current value of the MTU timestamp

DXE_0_TIMESTAMP

Bits	Name	Description
31:0	TSTMP	Reset State: 0x00000046

0x3000074 DXE_0_ARB_CH_MSK_CLR

Type: write-only

This write-only register provides for a way to forcibly unmask currently masked channels and return them to active participation in the arbitration

DXE_0_ARB_CH_MSK_CLR

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored. Reads return 0
6	CH6_MSK_CLR	Writing a one clears the arbiter mask for channel 6 thereby returning the channel to active arbitration. Reads always return 0.
5	CH5_MSK_CLR	Writing a one clears the arbiter mask for channel 5 thereby returning the channel to active arbitration. Reads always return 0.

DXE_0_ARB_CH_MSK_CLR (cont.)

Bits	Name	Description
4	CH4_MSK_CLR	Writing a one clears the arbiter mask for channel 4 thereby returning the channel to active arbitration. Reads always return 0.
3	CH3_MSK_CLR	Writing a one clears the arbiter mask for channel 3 thereby returning the channel to active arbitration. Reads always return 0.
2	CH2_MSK_CLR	Writing a one clears the arbiter mask for channel 2 thereby returning the channel to active arbitration. Reads always return 0.
1	CH1_MSK_CLR	Writing a one clears the arbiter mask for channel 1 thereby returning the channel to active arbitration. Reads always return 0.
0	CH0_MSK_CLR	Writing a one clears the arbiter mask for channel 0 thereby returning the channel to active arbitration. Reads always return 0.

0x3000078 DXE_0_CTR_PRES

Type: read-only
Reset State: 0x0000007F

This register is read-only and indicates how many counters actually exist in this implementation of the hardware.

DXE_0_CTR_PRES

Bits	Name	Description
31	CTR31_PRES	Counter 31 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
30	CTR30_PRES	Counter 30 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
29	CTR29_PRES	Counter 29 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
28	CTR28_PRES	Counter 28 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
27	CTR27_PRES	Counter 27 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
26	CTR26_PRES	Counter 26 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000

DXE_0_CTR_PRES (cont.)

Bits	Name	Description
25	CTR25_PRES	Counter 25 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
24	CTR24_PRES	Counter 24 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
23	CTR23_PRES	Counter 23 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
22	CTR22_PRES	Counter 22 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
21	CTR21_PRES	Counter 21 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
20	CTR20_PRES	Counter 20 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
19	CTR19_PRES	Counter 19 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
18	CTR18_PRES	Counter 18 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
17	CTR17_PRES	Counter 17 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
16	CTR16_PRES	Counter 16 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
15	CTR15_PRES	Counter 15 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
14	CTR14_PRES	Counter 14 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
13	CTR13_PRES	Counter 13 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
12	CTR12_PRES	Counter 12 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000

DXE_0_CTR_PRES (cont.)

Bits	Name	Description
11	CTR11_PRES	Counter 11 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
10	CTR10_PRES	Counter 10 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
9	CTR9_PRES	Counter 9 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
8	CTR8_PRES	Counter 8 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
7	CTR7_PRES	Counter 7 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000000
6	CTR6_PRES	Counter 6 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000001
5	CTR5_PRES	Counter 5 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000001
4	CTR4_PRES	Counter 4 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000001
3	CTR3_PRES	Counter 3 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000001
2	CTR2_PRES	Counter 2 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000001
1	CTR1_PRES	Counter 1 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000001
0	CTR0_PRES	Counter 0 Present. When high signifies that the counter exists in this implementation of the HW. Reset State: 0x00000001

0x300007C DXE_0_CTR_CLR

Type: write-only

This register is write-only and is used to reset the count from one or more specific event counters. When writing to this register, each data bit set HIGH causes the count value in the corresponding counter to be cleared. Data bits that are low have no effect on the corresponding counter.

DXE_0_CTR_CLR

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored, reads return 0
6	CTR6_CLR	Zero the count value in CTR6.
5	CTR5_CLR	Zero the count value in CTR5.
4	CTR4_CLR	Zero the count value in CTR4.
3	CTR3_CLR	Zero the count value in CTR3.
2	CTR2_CLR	Zero the count value in CTR2.
1	CTR1_CLR	Zero the count value in CTR1.
0	CTR0_CLR	Zero the count value in CTR0.

0x3000080 DXE_0_BD_TMPLTL

Type: read-write

The BD template base address high register holds the low bits of the base address for the BD templates store. DXE supports up to 4 templates and automatically calculates the address of the selected template based on the base address and the values programmed in CHn_CTRL[BDT_IDX] as follows: BD_TMPLT_ADDR = BD_TMPLT_BASE + (128 * CHn_CTRL[BDT_IDX])

DXE_0_BD_TMPLTL

Bits	Name	Description
31:0	BASEL	BD Template Base Low Address.

0x3000084 DXE_0_BD_TMPLTH

Type: read-write

The BD template base address high register holds the high bits of the base address for the BD templates store. Please see the description of CH_SADRL for more info.

DXE_0_BD_TMPLTH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.

DXE_0_BD_TMPLTH (cont.)

Bits	Name	Description
1:0	BASEH	Base Address High. BD template base address. With the current address mapping in Virgo these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in BD_TMPLTL) go untranslated through the target interface or if they use the interface's address translation windows. This applies only to PCI and PCIe interfaces. Since the BD templates should in almost all cases be stored in internal chip memory (MIF) this bit field should almost always be set to zero. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x3000088 DXE_0_BDT_DAT_START

Type: read-write
Reset State: 0x00000040

The BD template data start offset register holds the offset used to start writing payload data when the DXE is in H2B mode and the BD template feature has been enabled. In this mode, at the start of every new packet transfer, DXE will copy only enough bytes from the BD template to fill the space between byte 0 of the BD and the data start offset. Once this much of the BD template has been transferred, DXE will start reading data from the programmed source address and writing it into the BD starting at the programmed offset. Due to limitations of other modules in the chip, it's imperative that the value in this register allow for any header data to fit completely within the BD of the packet. That is, the total of adding the value contained in the BD template field "MPDU Header length" to the value in this register needs to be less than or equal to 127 in order to avoid problems. Further, it is necessary that the value of this register match the "MPDU Header Offset" field programmed in the BD template. DXE makes no attempt to check this is really the case.

DXE_0_BDT_DAT_START

Bits	Name	Description
31:7	RSVD	Reserved. Writes ignored. Reads always return zeroes.
6:0	OFFSET	Data start offset. Reset State: 0x00000040

0x3000200 DXE_0_COUNTER0

Type: read-write
Reset State: 0x00000000

This register can be configured to count whole packets in the H2B or B2H direction or to count the number of transfers (descriptors) for H2H transactions. For now this counter is hardwired to always count all transfers completing on channel 0, but will eventually be able to count events happening on any channel and also only count transfers with the INC bit set in the CH_CSR (Not implemented yet).

The value gets cleared at reset and the counter can also be cleared or preset to any starting value by directly writing to it. As a convenience to the programmer the CTR_CLR register has been provided to quickly clear the value in one or more of the event counters.

DXE_0_COUNTER0

Bits	Name	Description
31:16	RSVD	Reset State: 0x00000000
15:0	CNT	Reset State: 0x00000000

0x3000204 DXE_0_COUNTER1

Type: read-write
Reset State: 0x00000000

This register can be configured to count whole packets in the H2B or B2H direction or to count the number of transfers (descriptors) for H2H transactions. For now this counter is hardwired to always count all transfers completing on channel 1, but will eventually be able to count events happening on any channel and also only count transfers with the INC bit set in the CH_CSR (Not implemented yet).

The value gets cleared at reset and the counter can also be cleared or preset to any starting value by directly writing to it. As a convenience to the programmer the CTR_CLR register has been provided to quickly clear the value in one or more of the event counters.

DXE_0_COUNTER1

Bits	Name	Description
31:16	RSVD	Reset State: 0x00000000
15:0	CNT	Reset State: 0x00000000

0x3000208 DXE_0_COUNTER2

Type: read-write
Reset State: 0x00000000

This register can be configured to count whole packets in the H2B or B2H direction or to count the number of transfers (descriptors) for H2H transactions. For now this counter is hardwired to always count all transfers completing on channel 2, but will eventually be able to count events

happening on any channel and also only count transfers with the INC bit set in the CH_CSR (Not implemented yet)

The value gets cleared at reset and the counter can also be cleared or preset to any starting value by directly writing to it. As a convenience to the programmer the CTR_CLR register has been provided to quickly clear the value in one or more of the event counters.

DXE_0_COUNTER2

Bits	Name	Description
31:16	RSVD	Reset State: 0x00000000
15:0	CNT	Reset State: 0x00000000

0x300020C DXE_0_COUNTER3

Type: read-write
Reset State: 0x00000000

This register can be configured to count whole packets in the H2B or B2H direction or to count the number of transfers (descriptors) for H2H transactions. For now this counter is hardwired to always count all transfers completing on channel 3, but will eventually be able to count events happening on any channel and also only count transfers with the INC bit set in the CH_CSR (Not implemented yet).

The value gets cleared at reset and the counter can also be cleared or preset to any starting value by directly writing to it. As a convenience to the programmer the CTR_CLR register has been provided to quickly clear the value in one or more of the event counters.

DXE_0_COUNTER3

Bits	Name	Description
31:16	RSVD	Reset State: 0x00000000
15:0	CNT	Reset State: 0x00000000

0x3000210 DXE_0_COUNTER4

Type: read-write
Reset State: 0x00000000

This register can be configured to count whole packets in the H2B or B2H direction or to count the number of transfers (descriptors) for H2H transactions. For now this counter is hardwired to always count all transfers completing on channel 4, but will eventually be able to count events happening on any channel and also only count transfers with the INC bit set in the CH_CSR (Not implemented yet).

The value gets cleared at reset and the counter can also be cleared or preset to any starting value by directly writing to it. As a convenience to the programmer the CTR_CLR register has been provided to quickly clear the value in one or more of the event counters.

DXE_0_COUNTER4

Bits	Name	Description
31:16	RSVD	Reset State: 0x00000000
15:0	CNT	Reset State: 0x00000000

0x3000214 DXE_0_COUNTER5

Type: read-write
Reset State: 0x00000000

This register can be configured to count whole packets in the H2B or B2H direction or to count the number of transfers (descriptors) for H2H transactions. For now this counter is hardwired to always count all transfers completing on channel 5, but will eventually be able to count events happening on any channel and also only count transfers with the INC bit set in the CH_CSR (Not implemented yet)
to any starting value by directly writing to it. As a convenience to the programmer the CTR_CLR register has been provided to quickly clear the value in one or more of the event counters.

DXE_0_COUNTER5

Bits	Name	Description
31:16	RSVD	Reset State: 0x00000000
15:0	CNT	Reset State: 0x00000000

0x3000218 DXE_0_COUNTER6

Type: read-write
Reset State: 0x00000000

This register can be configured to count whole packets in the H2B or B2H direction or to count the number of transfers (descriptors) for H2H transactions. For now this counter is hardwired to always count all transfers completing on channel 6, but will eventually be able to count events happening on any channel and also only count transfers with the INC bit set in the CH_CSR (Not implemented yet)
to any starting value by directly writing to it. As a convenience to the programmer the CTR_CLR register has been provided to quickly clear the value in one or more of the event counters.

DXE_0_COUNTER6

Bits	Name	Description
31:16	RSVD	Reset State: 0x00000000
15:0	CNT	Reset State: 0x00000000

0x3000400 DXE_0_CH0_CTRL

Type: read-write
Reset State: 0x10000708

Serves to configure channel 0 operation

DXE_0_CH0_CTRL

Bits	Name	Description
31	SWAP	Endian Byte Swap Enable. When high instructs DXE to perform an endian swap of the incoming byte stream. The corresponding bit field in the DXE descriptor control word is located at DXE_DESC_CTRL[20]
30:29	BDT_IDX	BD Template Index. When XTYPE=H2B and BDH=1, DXE supports creating a BD by using template data from one of up to 4 different BD templates. The BD template base store is pointed at by the DXE BD_TMPLT(H/L) registers and the address used to read the template data is calculated as follows: BD_TMPLT_ADRR = BD_TMPLT_BASE + (128 * CH_CTRL[BDT_IDX]) The corresponding bit field in the control word of the external descriptor is mapped to bits[19:18]
28	DFMT	Descriptor Format. This bit field is used to select between long and short descriptor formats. When using the short descriptor format, the high part of the source, destination and descriptor addresses will be taken from the SADRH_DFLT, DADRH_DFLT or DESCH_DFLT registers respectively. Default is to use the long descriptor format 0x0: SHORT 0x1: LONG Reset State: 0x00000001

DXE_0_CH0_CTRL (cont.)

Bits	Name	Description
27	ABORT	Writing a one to this bit will cause the channel to stop its current transfer and set the ERR bit and ERR_CODE fields in CH_STATUS. Note that if the channel is currently disabled or if it is about to be disabled because it has just finished its programmed transfer, then the abort request will be ignored and the error bit and error codes won't be set. If the channel is currently masked by the arbiter then setting this bit will forcibly unmask it so that the transfer can be aborted the next time the channel is selected by the internal arbiter. The abort request is automatically cleared by hardware once the channel has aborted the transfer. Also note that since the DXE will not attempt to do any cleanup when a transfer is aborted, software might need to do so. For example, for H2B transfers, software should manually release the BD and any PDUs currently in use by the partial transfer or else a BD/PDU leak will result. Reset State: 0x00000000
26	ENDIANNESS	Specifies the endianness of the master generating the data. Affects alignment of valid bytes for non-dword aligned reads/writes. The corresponding field in the DXE descriptor control word is located in DXE_DESC_CTRL[21] 0x0: BIGEND 0x1: LTLEND Reset State: 0x00000000
25:22	CTR_SEL	Counter Select. If the event counters are enabled (DMA_CSR[ECTR_EN]=1) then this bit field selects the counter that will be incremented at the end of the transfer. By default the value in this bit field is the same as the channel number so that after reset channel 0 increments counter 0, channel 1 increments counter 1 and so on. Reset State: 0x00000000
21	EDVEN	When set, the DMA engine will clear the VAL bit in the DESC_CSR word of the current descriptor once it has completed processing it. This is useful for implementing a descriptor "ring" (see the description of the VALID bit in Table 3.1) Reset State: 0x00000000
20	EDEN	External Descriptor Enable. Use External Descriptor Linked List Reset State: 0x00000000
19	INE_DONE	Enable Channel Interrupt when Channel is Done. The corresponding interrupt source bit is INT_DONE Reset State: 0x00000000
18	INE_ERR	Enable Channel Interrupt on Errors. The corresponding interrupt source bit is INT_ERR Reset State: 0x00000000

DXE_0_CH0_CTRL (cont.)

Bits	Name	Description
17	INE_ED	Enable External Descriptor Interrupt. When this bit is set, an interrupt will be generated after processing a descriptor item that has the INT bit set in its DESC_CTRL word (see Table 3.1). The corresponding interrupt source bit is INT_ED Reset State: 0x00000000
16	STOP	Channel processing stopped due to a request in the last processed linked list descriptor (see the STOP bit in the definition of the DESC_CSR word in Table 3.1). This bit will be automatically cleared when the channel is restarted. Reset State: 0x00000000
15:13	PRIO	This field sets the channel priority.
12:9	BTHLD_SEL	BMU Threshold Select. This value tells DXE which of the BMU BD/PDU thresholds to check before issuing BMU commands that reserve, or get BDs or PDUs. It also specifies the module index value that will be used to issue any required BMU commands (see BMU spec for details). that involve the BMU and therefore its value will be ignored for H2H transfers. 0x0: RSVD0 0x1: RSVD1 0x2: THLD2 0x3: THLD3 0x4: THLD4 0x5: THLD5 0x6: THLD6 0x7: THLD7 0x8: THLD8 0x9: THLD9 0xA: THLD10 0xB: RSVD11 0xC: RSVD12 0xD: RSVD13 0xE: RSVD14 0xF: RSVD15 Reset State: 0x00000003

DXE_0_CH0_CTRL (cont.)

Bits	Name	Description
8	PDU_REL	0x0: Don't release BD and PDUs when done. 0x0: KEEP 0x1: RELEASE Reset State: 0x00000001
7	PIQ	next descriptor Pointer address Is Queue. When set the source of the descriptor address is interpreted as a queue ID instead of just the address of a flat memory location. The only valid source queues for descriptors are the UIF Tx data and Tx management endpoints. Any other IDs will result the channel aborting the transfer with an invalid source queue error. Therefore, when this bit is set, software must ensure that the CH_DESCL[QID] bit field is set to a valid queue ID and that the CH_DESCL[BASE] bit field is set to the base address of the source UIF endpoint. This base address is formed by taking the base address for the UIF block in the SAHB bus which can be found in the Nova address map document and then adding the internal UIF offset for the correct source endpoint. This offsets can be obtained from the UIF specification document. For convenience, the current internal UIF offsets are provided in the description of the QID bit field in the CH_DESCL register description. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
6	DIQ	Destination Is Queue. When set the destination address is interpreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF RX endpoints or and EIF outbound FIFO. When this bit is set, software must ensure that the DADR[QID] bit field is set to a valid queue ID and that the DADR[BASE] bit field is set to the base address of the destination queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
5	SIQ	Source Is Queue. When set the source address is interpreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF TX endpoints or and EIF inbound FIFO. When this bit is set, software must ensure that the SADR[QID] bit field is set to a valid queue ID and that the SADR[BASE] bit field is set to the base address of the source queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000

DXE_0_CH0_CTRL (cont.)

Bits	Name	Description
4	BDH	BD Handling bit. The behavior depends on the setting of XTYPE. desc for BDT_IDX). ignored. Reset State: 0x00000000
3	EOP	End of Packet bit. For H2B transfers marks the end of a packet cannot support the gather functionality and therefore the EOP bit must be set. For XTYPE values of H2H, B2B and B2H the value of this bit is ignored. Reset State: 0x00000001
2:1	XTYPE	Transfer Type. Specifies the type of transfer to perform: will also perform the required data format translation. The format translation behavior can be modified by the setting of the BDH and PAD bits. 0x0: H2H 0x1: B2B 0x2: H2B 0x3: B2H
0	EN	Channel Enable or Restart. Writing this bit with a one either starts a new DMA transfer according to the parameters programmed in the channel's configuration registers and clears the DONE bit or, if the channel is already enabled but the STOP bit is set, then it restarts channel processing and also clears the STOP bit. This bit is automatically cleared when a single transfer completes or, if the channel is configured to use linked list descriptors, when the last transfer in the descriptor linked list completes (DESC_NXT is NULL or/and DESC_CSR[VALID]=0). The channel is also disabled and this bit cleared if a channel error is encountered. Reading this bit indicates whether a channel is currently enabled or disabled:. the DMA_ENCH register which aggregates the EN bits of all channels. Note: Software must take care to not disable the channel while it is busy or data could be lost. Reset State: 0x00000000

0x3000404 DXE_0_CH0_STATUS

Type: read-write
Reset State: 0x00000000

Serves to report the status of the programmed channel operation.

DXE_0_CH0_STATUS

Bits	Name	Description
31:16	RSVD	Reserved. Reads always return 0. Writes are ignored.
15	INT_DONE	Interrupt Source: Asserted when the channel has finished all processing.
14	INT_ERR	Interrupt Source: Asserted when a channel error has occurred. Masked by the INE_ERR
13	INT_ED	Interrupt Source. Descriptor Done and INT requested
12	ABORT_REQ	Abort Request. Software has requested that the current operation be aborted. However, if CH_STATUS[EN] is still set then the channel has registered the request but is not yet in a position to abort the transfer "safely". Once the channel finishes its current operation it will abort the transfer and set the error flag and error code bit fields accordingly.
11	STOP_REQ	Stop Request. Software has requested that the channel stop it operation after the current descriptor has been processed. Once this happens the STOPD bit field will be set to one and the channel will be disabled.

DXE_0_CH0_STATUS (cont.)

Bits	Name	Description
10:6	ERR_CODE	Used to identify the source or cause of an error. 0x0: NONE 0x1: SAHB_ERR 0x2: H2H_RD_BUS_ERR 0x3: H2H_WR_BUS_ERR 0x4: PRG_INV_XTYPE 0x5: BERR_POPWQ 0x6: BERR_PUSHWQ 0x7: BERR_RLSS 0x8: BERR_GETPDU 0x9: PRG_INV_WQ 0xA: PRG_INV_H2H_SRC_QID 0xB: PRG_INV_H2H_DST_QID 0xC: PRG_INV_B2H_SRC_QID 0xD: PRG_INV_B2H_DST_QID 0xE: PRG_INV_B2H_SRC_IDX 0xF: PRG_INV_H2B_SRC_QID 0x10: PRG_INV_H2B_DST_QID 0x11: PRG_INV_H2B_DST_IDX 0x12: PRG_INV_H2B_SZ 0x13: PRG_INV_SADR 0x14: PRG_INV_DADR 0x15: PRG_INV_EDADR 0x16: PRG_INV_SRC_WQID 0x17: PRG_INV_DST_WQID 0x18: PRG_XTYPE_MSMTCH 0x19: PKT_ERR 0x1A: ABORT 0x1B: PDU_CNT_OVFL Reset State: 0x00000000
5	ERR	DMA channel stopped due to error. To clear the error status it is necessary to write a 1 into this bit position.
4	STOPD	Channel Stopped. The channel has stopped further processing and disabled itself due to a stop request in the last processed descriptor. Reset State: 0x00000000
3	MSKD	Channel Masked. The channel has been automatically masked out from arbitration due to a blocking condition. Reset State: 0x00000000
2	DONE	DMA channel Done. This bit will be automatically cleared the next time the channel is enabled. Reset State: 0x00000000
1	BUSY	Channel busy. HIgh when the channel is enabled and currently active (won internal arbitration) Reset State: 0x00000000

DXE_0_CH0_STATUS (cont.)

Bits	Name	Description
0	EN	Channel Enabled. Copy of CH_CTRL[EN]. Reset State: 0x00000000

0x3000408 DXE_0_CH0_SZ

Type: read-write

The transfer size register specifies the total, remaining, and burst or 'chunk' transfer sizes for each channel. The maximum total transfer size is 16K-1 bytes. The chunk size control can be useful to control the relative bandwidth used by each channel as the dma engine will change channels, release the AHB bus, and rearbitrate for access after transferring chunk size bytes.

DXE_0_CH0_SZ

Bits	Name	Description
31:28	CHK_SZ	Chunk transfer size. Specifies the number of bytes (in multiples of 8) to be transferred at one given time (not implying they are buffered but that they will be transferred for each start event in one bus request cycle). If chunk size is zero the DMA engine will always perform maximum chunk size transfers. Maximum chunk size is 128 bytes.
27:14	REM_SZ	Remaining transfer size. Specifies the number of bytes that remain to be transferred to complete the current operation.
13:0	TOT_SZ	Total Transfer Size. Specifies the number of bytes to be transferred. Maximum total transfer size is (4K-1) bytes. Note: This field is unnecessary and will be ignored for B2H or B2B transfers, when the source of the transfer is in BMU space (either BMU queue or direct pointer to BD). This is because the size of the transfer will be the packet length encoded in the BD at offset 0x0c bits [11:0].

0x300040C DXE_0_CH0_SADRL

Type: read-write

The channel source address register specifies either the source address in flat internal or external memory, or else the BMU queue ID, UIF TX endpoint ID, or EIF inbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the source, addresses can have arbitrary byte-alignment When using a BMU queue, UIF endpoint or EIF fifo as a source, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[SIQ] bit. When CH_CSR[SIQ] is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when it is set this register has two bit fields: The SQID bit field

used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF source endpoint/FIFO

SWQID matches BMU), the DXE will issue a BMU POPWQ command to pop the specified queue and obtain the BD index of the source packet. Else, when the source is an address (CH_CSR[SIQ] = 0), the DXE will interpret the address as the index of the packet BD and will add it to the BMU_BASE to obtain the physical address to use to fetch it directly from memory.

and SQID matches UIF/EIF), software should program the SAHB base address of the UIF source endpoint in the BASE bit field and the queue ID to match in the SWQID bit field, then the DXE will use the base address given to generate the physical address and read the data over the SAHB bus and also use the appropriate sideband signals as specified by the SQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and SQID fields are consistent and refer to the same endpoint or else hangs or unpredictable behavior might occur. Else, when the source is just a location in flat memory space, (CH_CSR[SIQ] = 0), the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the physical address to use to fetch the data. For this case, software should make sure that the provided address maps to the intended source interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus.

   ADDR[31:7] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document) of SQID field

DXE_0_CH0_SADRL

Bits	Name	Description
31:7	BASE	Base Address. This bit field provides the base address of the source UIF TX endpoint or EIF inbound FIFO. The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH0_SADRL (cont.)

Bits	Name	Description
6:0	SQID	Source Queue ID. This bit field provides the ID for the source BMU, UIF or EIF queue to be used for the transfer. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: RSVD_25 0x1A: RSVD_26 0x1B: RSVD_27 0x1C: RSVD_28 0x1D: RSVD_29 0x1E: RSVD_30 0x1F: RSVD_31

0x3000410 DXE_0_CH0_SADRH

Type: read-write

The channel source address high register holds the high bits of the source address for a transfer. Please see the description of CH_SADRL for more info.

DXE_0_CH0_SADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_SADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x3000414 DXE_0_CH0_DADRL

Type: read-write

The channel destination address register specifies either the destination address in flat internal or external memory, or else the BMU queue ID, UIF RX endpoint ID, or EIF outbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the destination, addresses can have arbitrary byte-alignment. When using a BMU queue, UIF endpoint or EIF fifo as a destination, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[DIQ] bit. When this bit is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when the bit is set this register has two bit fields: The DQID bit field used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF destination endpoint/FIFO.

and DQID matches BMU), the DXE will push the index of the BD of the packet into the specified queue at the end of the packet transfer. Therefore, software is responsible for programming a valid BMU Queue ID.

address obtained by adding the provided index to the BMU_BASE, again, the software must ensure that said address is legal and known to BMU. That is, software must preallocate the BD (get the BD from BMU via GET BD/PDU cmd) for the BD before starting the transfer. For B2H or H2H transfers, if the destination is a UIF endpoint or EIF FIFO (CH_CSR[DIQ] = 1 and DQID matches UIF/EIF), software should program the SAHB base address of the UIF destination endpoint in the BASE bit field and the queue ID to match in the DQID bit field, then the DXE will use the base address given to generate the physical address and write the data over the SAHB bus and also use the appropriate sideband signals as specified by the DQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and DQID fields are

consistent and refer to the same endpoint else hangs or unpredictable behavior might occur. On the other hand, when the destination is just a location in flat memory space, (CH_CSR[DIQ] = 0), be it internal or external, the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the address to write the data. For this case, software should make sure that the address maps to the intended destination interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus. To summarize, for H2B and B2B transfers the address must conform to the following format:

BMU_BASE + BD_INDEX[15:0]

   ADDR[4:0] = Any BMU Queue ID as specified in description of QID field

   ADDR[31:0] = address mapping to destination interface address map + Interface uarch document) of DQID field

DXE_0_CH0_DADRL

Bits	Name	Description
31:7	BASE	Base Address. This bit field provides the base address of the destination UIF RX endpoint or EIF outbound FIFO (for BMU software may use any value can be used but zero is suggested). The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH0_DADRL (cont.)

Bits	Name	Description
6:0	DQID	Destination Queue ID. This bit field provides the ID for the destination BMU WQ, UIF RX endpoint or EIF outbound queue to be used for the transfer. meaning and is interpreted only as part of the full 32-bit source address. 0x0: RSVD_0 0x1: RSVD_1 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: BMU_25 0x1A: BMU_26 0x1B: BMU_SINK_WQ 0x1C: UIF_RX_1_EP 0x1D: UIF_RX_2_EP 0x1E: UIF_RX_3_EP 0x1F: UIF_RX_4_EP

0x3000418 DXE_0_CH0_DADRH

Type: read-write

The channel destination address high register holds the high bits of the destination address for a transfer. Please see the description of CH_DADRL for more info.

DXE_0_CH0_DADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	This register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x300041C DXE_0_CH0_DESCL

Type: read-write

The Channel 0 Linked List Descriptor Pointer register contains the 32 lower bits of the address of the next descriptor to be loaded in the linked list. This address must be dword (32-bit) aligned (addr[1:0]=0 if CH_CTRL[PIQ]=0). Each complete transfer descriptor consists of 7 32-bit values arranged contiguously in memory. The value of this register will be overwritten with the address of the start of the next descriptor set in the list after the current descriptor has been fetched. The meaning of the value in this register depends on the value of the CH_CTRL[PIQ] bit field similar to the way in which SADRL and DADRL are depending in SIQ and DIQ respectively. For CH_CTRL[PIQ]=0 then this register has no bit fields and the value is just interpreted as an address in flat memory space. When CH_CTRL[PIQ] is set then the descriptor will be read from FIFO type memory in UIF and the register has 2 bit fields: BASE, and SQID. BASE specifies the base address of the UIF Tx queue (derived from the start of the UIF address space in SAHB plus the internal UIF offset).

DXE_0_CH0_DESCL

Bits	Name	Description
31:7	BASE	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify the base address of the UIF endpoint to use as the source of the descriptor. Please refer to the Nova address map document and to the UIF architecture document for guaranteed correct values to use here. For convenience but without a guarantee of accuracy, the base value to use for both the Tx data and management endpoints is the following: x100 = 0x0E02_5100>>7 = 0x1C_04A2

DXE_0_CH0_DESCL (cont.)

Bits	Name	Description
6:0	SQID	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify which of the two UIF TX queues to use. Note that in this case software also needs to program the correct base address of the source UIF endpoint in the BASE bit field. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x3000420 DXE_0_CH0_DESCH

Type: read-write

The channel destination address high register holds the high bits of the the address of the next descriptor to be loaded in the linked list.

DXE_0_CH0_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. Please note that if the source of the descriptor is either of the UIF endpoints (CH_CTRL[PIQ]=1) then the value in ADDRH has to be 0 or else the descriptor read could end up mapping to the XIF or PIF. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x3000424 DXE_0_CH0_LST_DESCL

Type: read-only

The read-only Channel 0 Current/last Linked List Descriptor Pointer register contains the low 32-bits of the address of the descriptor currently being processed or of the last descriptor processed if the channel is disabled.

explained for the CH_DESCL register.

DXE_0_CH0_LST_DESCL

Bits	Name	Description
31:7	BASE	See description of CH_DESCL[BASE].
6:0	SQID	See description of CH_DESCL[SQID]. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x3000428 DXE_0_CH0_LST_DESCH

Type: read-only

The channel destination address high register holds the high bits of the the address of the next descriptor to be loaded in the linked list. Note that The meaning of the value and bit fields is the same as was explained for the CH_DESCL register.

DXE_0_CH0_LST_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address.

0x300042C DXE_0_CH0_BD

Type: read-only

DXE_0_CH0_BD

Bits	Name	Description
31:24	RSVD	Reserved. Always returns 0 when read.
23	VAL	Valid. BD has been loaded and is valid.
22:16	PDU_CNT	PDU count of packet.
15:0	IDX	Index of BD. To get actual physical address must be added to BD/PDU base.

0x3000430 DXE_0_CH0_HEAD

Type: read-only
Reset State: 0x00000000

Address of head of packet.

DXE_0_CH0_HEAD

Bits	Name	Description
31:27	RSVD	Reserved. Reset State: 0x00000000
26	DESCVAL	Descriptor valid. Signifies descriptor has already been loaded. Used to prevent reloading of a descriptor. Reset State: 0x00000000
25:21	DWQID	Destination WQ ID. Original BMU, UIF or EIF destination queue. Valid only when CH_CSR[DIQ]=1 Reset State: 0x00000000
20:16	SWQID	Source WQ ID. Original BMU, UIF or EIF source queue. Valid only when CH_CSR[SIQ]=1 Reset State: 0x00000000
15:0	IDX	Index of Head. Must be added to BD/PDU base for actual physical address.

0x3000434 DXE_0_CH0_TAIL

Type: read-only
Reset State: 0x00000000

Address of tail of packet.

DXE_0_CH0_TAIL

Bits	Name	Description
31:16	RSVD	Reserved. Reset State: 0x00000000
15:0	IDX	Index of Tail. Must be added to BD/PDU base for actual physical address

0x3000438 DXE_0_CH0_PDU

Type: read-only
Reset State: 0x00000000

PDU info register.

DXE_0_CH0_PDU

Bits	Name	Description
31	RSVD	Reserved. Always returns 0 when read. Reset State: 0x00000000
30:24	PDU_CNT	Current PDU count.
23:8	IDX	Index of current PDU. Must be added to BD/PDU base for actual physical address
7:0	FST_OFF	First PDU offset.

0x300043C DXE_0_CH0_TSTMP

Type: read-only
Reset State: 0x00000000

Contains last sampled value of the system timestamp

DXE_0_CH0_TSTMP

Bits	Name	Description
31:0	VALUE	Reset State: 0x00000000

0x3000440 DXE_0_CH1_CTRL

Type: read-write
Reset State: 0x10400708

Serves to configure channel 1 operation

DXE_0_CH1_CTRL

Bits	Name	Description
31	SWAP	Endian Byte Swap Enable. When high instructs DXE to perform an endian swap of the incoming byte stream. The corresponding bit field in the DXE descriptor control word is located at DXE_DESC_CTRL[20]

DXE_0_CH1_CTRL (cont.)

Bits	Name	Description
30:29	BDT_IDX	BD Template Index. by using template data from one of up to 4 different BD templates. The BD template base store is pointed at by the DXE BD_TMPLT(H/L) registers and the address used to read the template data is calculated as follows: CH_CTRL[BDT_IDX]) The corresponding bit field in the control word of the external descriptor is mapped to bits[19:18]
28	DFMT	Descriptor Format. descriptor formats. When using the short descriptor format, the high part of the source, destination and descriptor addresses will be taken from the SADRH_DFLT, DADRH_DFLT or DESCH_DFLT registers respectively. Default is to use the long descriptor format 0x0: SHORT 0x1: LONG Reset State: 0x00000001
27	ABORT	Writing a one to this bit will cause the channel to stop its current transfer and set the ERR bit and ERR_CODE fields in CH_STATUS. Note that if the channel is currently disabled or if it is about to be disabled because it has just finished its programmed transfer, then the abort request will be ignored and the error bit and error codes won't be set. If the channel is currently masked by the arbiter then setting this bit will forcibly unmask it so that the transfer can be aborted the next time the channel is selected by the internal arbiter. The abort request is automatically cleared by hardware once the channel has aborted the transfer. Also note that since the DXE will not attempt to do any cleanup when a transfer is aborted, software might need to do so. For example, for H2B transfers, software should manually release the BD and any PDUs currently in use by the partial transfer or else a BD/PDU leak will result. Reset State: 0x00000000
26	ENDIANNESS	Specifies the endianness of the master generating the data. Affects alignment of valid bytes for non-dword aligned reads/writes. The corresponding field in the DXE descriptor control word is located in DXE_DESC_CTRL[21] 0x0: BIGEND 0x1: LTLEND Reset State: 0x00000000
25:22	CTR_SEL	Counter Select. If the event counters are enabled (DMA_CSR[ECTR_EN]=1) then this bit field selects the counter that will be incremented at the end of the transfer. By default the value in this bit field is the same as the channel number so that after reset channel 0 increments counter 0, channel 1 increments counter 1 and so on. Reset State: 0x00000001

DXE_0_CH1_CTRL (cont.)

Bits	Name	Description
21	EDVEN	When set, the DMA engine will clear the VAL bit in the DESC_CSR word of the current descriptor once it has completed processing it. This is useful for implementing a descriptor "ring" (see the description of the VALID bit in Table 3.1) Reset State: 0x00000000
20	EDEN	External Descriptor Enable. Use External Descriptor Linked List Reset State: 0x00000000
19	INE_DONE	Enable Channel Interrupt when Channel is Done. The corresponding interrupt source bit is INT_DONE Reset State: 0x00000000
18	INE_ERR	Enable Channel Interrupt on Errors. The corresponding interrupt source bit is INT_ERR Reset State: 0x00000000
17	INE_ED	Enable External Descriptor Interrupt. When this bit is set, an interrupt will be generated after processing a descriptor item that has the INT bit set in its DESC_CTRL word (see Table 3.1). The corresponding interrupt source bit is INT_ED Reset State: 0x00000000
16	STOP	Channel processing stopped due to a request in the last processed linked list descriptor (see the STOP bit in the definition of the DESC_CSR word in Table 3.1). This bit will be automatically cleared when the channel is restarted. Reset State: 0x00000000
15:13	PRIO	This field sets the channel priority. 0: Lowest Priority.

DXE_0_CH1_CTRL (cont.)

Bits	Name	Description
12:9	BTHLD_SEL	BMU Threshold Select. This value tells DXE which of the BMU BD/PDU thresholds to check before issuing BMU commands that reserve, or get BDs or PDUs. It also specifies the module index value that will be used to issue any required BMU commands (see BMU spec for details). The value of this bit field is only meaningful for transfer types that involve the BMU and therefore its value will be ignored for H2H transfers. 0x0: RSVD0 0x1: RSVD1 0x2: THLD2 0x3: THLD3 0x4: THLD4 0x5: THLD5 0x6: THLD6 0x7: THLD7 0x8: THLD8 0x9: THLD9 0xA: THLD10 0xB: RSVD11 0xC: RSVD12 0xD: RSVD13 0xE: RSVD14 0xF: RSVD15 Reset State: 0x00000003
8	PDU_REL	0x0: Don't release BD and PDUs when done. 1: Release BD and PDUs when done. 0x0: KEEP 0x1: RELEASE Reset State: 0x00000001

DXE_0_CH1_CTRL (cont.)

Bits	Name	Description
7	PIQ	next descriptor Pointer address Is Queue. When set the source of the descriptor address is interepreted as a queue ID instead of just the address of a flat memory location. The only valid source queues for descriptors are the UIF Tx data and Tx management endpoints. Any other IDs will result the channel aborting the transfer with an invalid source queue error. Therefore, when this bit is set, software must ensure that the CH_DESCL[QID] bit field is set to a valid queue ID and that the CH_DESCL[BASE] bit field is set to the base address of the source UIF endpoint. This base address is formed by taking the base address for the UIF block in the SAHB bus which can be found in the Nova address map document and then adding the internal UIF offset for the correct source endpoint. This offsets can be obtained from the UIF specification document. For convenience, the current internal UIF offsets are provided in the descripiton of the QID bit field in the CH_DESCL register description. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
6	DIQ	Destination Is Queue. When set the destination address is interepreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF RX endpoints or and EIF outbound FIFO. When this bit is set, software must ensure that the DADR[QID] bit field is set to a valid queue ID and that the DADR[BASE] bit field is set to the base address of the destination queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
5	SIQ	Source Is Queue. When set the source address is interepreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF TX endpoints or and EIF inbound FIFO. When this bit is set, software must ensure that the SADR[QID] bit field is set to a valid queue ID and that the SADR[BASE] bit field is set to the base address of the source queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000

DXE_0_CH1_CTRL (cont.)

Bits	Name	Description
4	BDH	BD Handling bit. The behavior depends on the setting of XTYPE. If XTYPE is: H2B: Then if BDH is: 0: Use first 128 bytes of packet as BD. 1: Create BD from BD template (Up to 4 supported. Also see desc for BDT_IDX). B2H: Then if BDH is: 0: Insert BD in front of payload. 1: Discard BD. For XTYPE values of H2H and B2B the value of this bit is ignored. Reset State: 0x00000000
3	EOP	End of Packet bit. For H2B transfers marks the end of a packet Please note that when not using external descriptors DXE cannot support the gather functionality and therefore the EOP bit must be set. For XTYPE values of H2H, B2B and B2H the value of this bit is ignored. Reset State: 0x00000001
2:1	XTYPE	Transfer Type. Specifies the type of transfer to perform: 00: H2H. Host space to Host space transfer. 01: B2B. BMU space to BMU space transfer. 10: H2B. Host space to BMU translation. 11: B2H. BMU space to Host space translation. For cross-space transfers (H2B and B2H) the DMA engine will also perform the required data format translation. The format translation behavior can be modified by the setting of the BDH and PAD bits. 0x0: H2H 0x1: B2B 0x2: H2B 0x3: B2H
0	EN	Channel Enable or Restart. Writing this bit with a one either starts a new DMA transfer according to the parameters programmed in the channel's configuration registers and clears the DONE bit or, if the channel is already enabled but the STOP bit is set, then it restarts channel processing and also clears the STOP bit. This bit is automatically cleared when a single transfer completes or, if the channel is configured to use linked list descriptors, when the last transfer in the descriptor linked list completes (DESC_NXT is NULL or/and DESC_CSR[VALID]=0). The channel is also disabled and this bit cleared if a channel error is encountered. Reading this bit indicates whether a channel is currently enabled or disabled:. 0: Channel Disabled. 1: Channel Enabled. The Channel Enable bit status can also be found by reading the DMA_ENCH register which aggregates the EN bits of all channels. Note: Software must take care to not disable the channel while it is busy or data could be lost. Reset State: 0x00000000

0x3000444 DXE_0_CH1_STATUS

Type: read-write
Reset State: 0x00000000

Serves to report the status of the programmed channel operation.

DXE_0_CH1_STATUS

Bits	Name	Description
31:16	RSVD	Reserved. Reads always return 0. Writes are ignored.
15	INT_DONE	Interrupt Source: Asserted when the channel has finished all processing.
14	INT_ERR	Interrupt Source: Asserted when a channel error has occurred. Masked by the INE_ERR
13	INT_ED	Interrupt Source. Descriptor Done and INT requested
12	ABORT_REQ	Abort Request. Software has requested that the current operation be aborted. However, if CH_STATUS[EN] is still set then the channel has registered the request but is not yet in a position to abort the transfer "safely". Once the channel finishes its current operation it will abort the transfer and set the error flag and error code bit fields accordingly.
11	STOP_REQ	Stop Request. Software has requested that the channel stop it operation after the current descriptor has been processed. Once this happens the STOPD bit field will be set to one and the channel will be disabled.

DXE_0_CH1_STATUS (cont.)

Bits	Name	Description
10:6	ERR_CODE	Used to identify the source or cause of an error. 0x0: NONE 0x1: SAHB_ERR 0x2: H2H_RD_BUS_ERR 0x3: H2H_WR_BUS_ERR 0x4: PRG_INV_XTYPE 0x5: BERR_POPWQ 0x6: BERR_PUSHWQ 0x7: BERR_RLSS 0x8: BERR_GETPDU 0x9: PRG_INV_WQ 0xA: PRG_INV_H2H_SRC_QID 0xB: PRG_INV_H2H_DST_QID 0xC: PRG_INV_B2H_SRC_QID 0xD: PRG_INV_B2H_DST_QID 0xE: PRG_INV_B2H_SRC_IDX 0xF: PRG_INV_H2B_SRC_QID 0x10: PRG_INV_H2B_DST_QID 0x11: PRG_INV_H2B_DST_IDX 0x12: PRG_INV_H2B_SZ 0x13: PRG_INV_SADR 0x14: PRG_INV_DADR 0x15: PRG_INV_EDADR 0x16: PRG_INV_SRC_WQID 0x17: PRG_INV_DST_WQID 0x18: PRG_XTYPE_MSMTCH 0x19: PKT_ERR 0x1A: ABORT 0x1B: PDU_CNT_OVFL Reset State: 0x00000000
5	ERR	DMA channel stopped due to error. To clear the error status it is necessary to write a 1 into this bit position.
4	STOPD	Channel Stopped. The channel has stopped further processing and disabled itself due to a stop request in the last processed descriptor. Reset State: 0x00000000
3	MSKD	Channel Masked. The channel has been automatically masked out from arbitration due to a blocking condition. Reset State: 0x00000000
2	DONE	DMA channel Done. This bit will be automatically cleared the next time the channel is enabled. Reset State: 0x00000000
1	BUSY	Channel busy. HIgh when the channel is enabled and currently active (won internal arbitration) Reset State: 0x00000000

DXE_0_CH1_STATUS (cont.)

Bits	Name	Description
0	EN	Channel Enabled. Copy of CH_CTRL[EN]. Reset State: 0x00000000

0x3000448 DXE_0_CH1_SZ

Type: read-write

The transfer size register specifies the total, remaining, and burst or 'chunk' transfer sizes for each channel. The maximum total transfer size is 16K-1 bytes. The chunk size control can be useful to control the relative bandwidth used by each channel as the dma engine will change channels, release the AHB bus, and rearbitrate for access after transferring chunk size bytes.

DXE_0_CH1_SZ

Bits	Name	Description
31:28	CHK_SZ	Chunk transfer size. Specifies the number of bytes (in multiples of 8) to be transferred at one given time (not implying they are buffered but that they will be transferred for each start event in one bus request cycle). If chunk size is zero the DMA engine will always perform maximum chunk size transfers. Maximum chunk size is 128 bytes.
27:14	REM_SZ	Remaining transfer size. Specifies the number of bytes that remain to be transferred to complete the current operation.
13:0	TOT_SZ	Total Transfer Size. Specifies the number of bytes to be transferred. Maximum total transfer size is (4K-1) bytes. Note: This field is unnecessary and will be ignored for B2H or B2B transfers, when the source of the transfer is in BMU space (either BMU queue or direct pointer to BD). This is because the size of the transfer will be the packet length encoded in the BD at offset 0x0c bits [11:0].

0x300044C DXE_0_CH1_SADRL

Type: read-write

The channel source address register specifies either the source address in flat internal or external memory, or else the BMU queue ID, UIF TX endpoint ID, or EIF inbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the source, addresses can have arbitrary byte-alignment When using a BMU queue, UIF endpoint or EIF fifo as a source, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[SIQ] bit. When CH_CSR[SIQ] is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when it is set this register has two bit fields: The SQID bit field

used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF source endpoint/FIFO.

For B2H or B2B transfers, when the source is a BMU Queue ID (CH_CSR[SIQ] = 1 and SWQID matches BMU), the DXE will issue a BMU POPWQ command to pop the specified queue and obtain the BD index of the source packet. Else, when the source is an address (CH_CSR[SIQ] = 0), the DXE will interpret the address as the index of the packet BD and will add it to the BMU_BASE to obtain the physical addresss to use to fetch it directly from memory.

For H2B or H2H transfers, if the source is a UIF endpoint or EIF FIFO (CH_CSR[SIQ] = 1 and SQID matches UIF/EIF), software should program the SAHB base address of the UIF source endpoint in the BASE bit field and the queue ID to match in the SWQID bit field, then the DXE will use the base address given to generate the physical address and read the data over the SAHB bus and also use the appropriate sideband signals as specified by the SQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and SQID fields are consistend and refer to the same endpoint or else hangs or unpredictable behavior might occur. Else, when the source is just a location in flat memory space, (CH_CSR[SIQ] = 0), the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the physical address to use to fetch the data. For this case, software should make sure that the provided address maps to the intended source interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus.

To summarize, for B2H and B2B transfers the address must conform to the following format:

For index of BD mode (CH_CSR[SIQ] = 0):

   ADDR[31:7] = BMU_BASE + BD_INDEX[15:0]

   ADDR[6:0] = 7'd0

For BMU Queue ID mode (CH_CSR[SIQ] = 1 & SQID matching one of the BMU queues):

   ADDR[31:7] = Any value will do but zero preferred

   ADDR[6:0] = Any BMU Queue ID as specified in description of SQID field

For H2B and H2H transfers the address must conform to the following format:

For sources in flat memory space (CH_CSR[SIQ] = 0):   ADDR[31:0] = address mapping to source interface

For UIF RX endpoints or EIF FIFOs (CH_CSR[SIQ] = 1 & QID matching UIF or EIF):

   ADDR[31:7] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document)

   ADDR[6:0] = Queue ID matching UIF or EIF as specified in description of SQID field

DXE_0_CH1_SADRL

Bits	Name	Description
31:7	BASE	Base Address. For this case, this bit field provides the base address of the source UIF TX endpoint or EIF inbound FIFO. The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd Please consult the appropriate interface uarch for the offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH1_SADRL (cont.)

Bits	Name	Description
6:0	SQID	Source Queue ID. Valid only when the CH_CSR[SIQ] bit is set. For this case, this bit field provides the ID for the source BMU, UIF or EIF queue to be used for the transfer. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: RSVD_25 0x1A: RSVD_26 0x1B: RSVD_27 0x1C: RSVD_28 0x1D: RSVD_29 0x1E: RSVD_30 0x1F: RSVD_31

0x3000450 DXE_0_CH1_SADRH

Type: read-write

The channel source address high register holds the high bits of the source address for a transfer. Please see the description of CH_SADRL for more info.

DXE_0_CH1_SADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_SADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x3000454 DXE_0_CH1_DADRL

Type: read-write

The channel destination address register specifies either the destination address in flat internal or external memory, or else the BMU queue ID, UIF RX endpoint ID, or EIF outbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the destination, addresses can have arbitrary byte-alignment. When using a BMU queue, UIF endpoint or EIF fifo as a destination, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[DIQ] bit. When this bit is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when the bit is set this register has two bit fields: The DQID bit field used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF destination endpoint/FIFO.

For H2B or B2B transfers, when using a BMU queue as the destination (CH_CSR[DIQ] = 1 and DQID matches BMU), the DXE will push the index of the BD of the packet into the specified queue at the end of the packet transfer. Therefore, software is responsible for programming a valid BMU Queue ID.

Else, when the destination is an index (CH_CSR[DIQ] = 0), the BD will be written to the address obtained by adding the provided index to the BMU_BASE, again, the software must ensure that said address is legal and known to BMU. That is, software must preallocate the BD (get the BD from BMU via GET BD/PDU cmd) for the BD before starting the transfer. For B2H or H2H transfers, if the destination is a UIF endpoint or EIF FIFO (CH_CSR[DIQ] = 1 and DQID matches UIF/EIF), software should program the SAHB base address of the UIF destination endpoint in the BASE bit field and the queue ID to match in the DQID bit field, then the DXE will use the base address given to generate the physical address and write the data over the SAHB bus and also use the appropriate sideband signals as specified by the DQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and DQID fields are consistent and refer

to the same endpoint else hangs or unpredictable behavior might occur. On the other hand, when the destination is just a location in flat memory space, (CH_CSR[DIQ] = 0), be it internal or external, the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the address to write the data. For this case, software should make sure that the address maps to the intended destination interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus. To summarize, for H2B and B2B transfers the address must conform to the following format:

For index of BD mode (CH_CSR[DIQ] = 0):   ADDR[31:7] = BMU_BASE + BD_INDEX[15:0]

   ADDR[6:0] = 7'd0

For BMU Queue ID mode (CH_CSR[DIQ] = 1 & DQID matching one of the BMU queues):

   ADDR[31:5] = Any value will do but zero preferred

   ADDR[4:0] = Any BMU Queue ID as specified in description of QID field

For B2H and H2H transfers the address must conform to the following format:

For destinations in flat memory space (CH_CSR[DIQ] = 0):   ADDR[31:0] = address mapping to destination interface

For UIF RX endpoints or EIF FIFOs (CH_CSR[DIQ] = 1 & DQID matching UIF or EIF):

   ADDR[31:5] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document)

   ADDR[4:0] = Queue ID matching UIF or EIF as specified in description of DQID field

DXE_0_CH1_DADRL

Bits	Name	Description
31:7	BASE	Base Address. Valid only when the CH_CSR[DIQ] bit is set. For this case, this bit field provides the base address of the destination UIF RX endpoint or EIF outbound FIFO (for BMU software may use any value can be used but zero is suggested). The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd Please consult the appropriate interface uarch for the offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH1_DADRL (cont.)

Bits	Name	Description
6:0	DQID	Destination Queue ID. is set. For this case, this bit field provides the ID for the destination BMU WQ, UIF RX endpoint or EIF outbound queue to be used for the transfer. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: RSVD_0 0x1: RSVD_1 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: BMU_25 0x1A: BMU_26 0x1B: BMU_SINK_WQ 0x1C: UIF_RX_1_EP 0x1D: UIF_RX_2_EP 0x1E: UIF_RX_3_EP 0x1F: UIF_RX_4_EP

0x3000458 DXE_0_CH1_DADRH

Type: read-write

The channel destination address high register holds the high bits of the destination address for a transfer. Please see the description of CH_DADRL for more info.

DXE_0_CH1_DADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	This register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x300045C DXE_0_CH1_DESCL

Type: read-write

The Channel 1 Linked List Descriptor Pointer register contains the 32 lower bits of the address of the next descriptor to be loaded in the linked list. This address must be dword (32-bit) aligned (addr[1:0]=0 if CH_CTRL[PIQ]=0). Each complete transfer descriptor consists of 7 32-bit values arranged contiguously in memory. The value of this register will be overwritten with the address of the start of the next descriptor set in the list after the current descriptor has been fetched. The meaning of the value in this register depends on the value of the CH_CTRL[PIQ] bit field similar to the way in which SADRL and DADRL are depending in SIQ and DIQ respectively. For CH_CTRL[PIQ]=0 then this register has no bit fields and the value is just intrepreted as an address in flat memory space. When CH_CTRL[PIQ] is set then the descriptor will be read from FIFO type memory in UIF and the register has 2 bit fields: BASE, and SQID. BASE specifies the base address of the UIF Tx queue (derived from the start of the UIF address space in SAHB plus the internal UIF offset).

DXE_0_CH1_DESCL

Bits	Name	Description
31:7	BASE	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify the base address of the UIF endpoint to use as the source of the descriptor. Please refer to the Nova address map document and to the UIF architecture document for guaranteed correct values to use here. For convenience but without a guarantee of accuracy, the base value to use for both the Tx data and management endpoints is the following: base = UIF base + TD_and_TM_offset = 0x0E02_5000 + x100 = 0x0E02_5100>>7 = 0x1C_04A2

DXE_0_CH1_DESCL (cont.)

Bits	Name	Description
6:0	SQID	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify which of the two UIF TX queues to use. Note that in this case software also needs to program the correct base address of the source UIF endpoint in the BASE bit field. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x3000460 DXE_0_CH1_DESCH

Type: read-write

The channel destination address high register holds the high bits of the the address of the next descriptor to be loaded in the linked list.

DXE_0_CH1_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. Please note that if the source of the descriptor is either of the UIF endpoints (CH_CTRL[PIQ]=1) then the value in ADDRH has to be 0 or else the descriptor read could end up mapping to the XIF or PIF. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x3000464 DXE_0_CH1_LST_DESCL

Type: read-only

The read-only Channel 1 Current/last Linked List Descriptor Pointer register contains the low 32-bits of the address of the descriptor currently being processed or of the last descriptor processed if the channel is disabled.

The meaning of the value and bit fields with regards to CH_CTRL[PIQ] is the same as was explained for the CH_DESCL register.

DXE_0_CH1_LST_DESCL

Bits	Name	Description
31:7	BASE	See description of CH_DESCL[BASE].
6:0	SQID	See description of CH_DESCL[SQID]. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x3000468 DXE_0_CH1_LST_DESCH

Type: read-only

The channel destination address high register holds the high bits of the the address of the next descriptor to be loaded in the linked list. Note that The meaning of the value and bit fields is the same as was explained for the CH_DESCL register.

DXE_0_CH1_LST_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address.

0x300046C DXE_0_CH1_BD

Type: read-only

DXE_0_CH1_BD

Bits	Name	Description
31:24	RSVD	Reserved. Always returns 0 when read.
23	VAL	Valid. BD has been loaded and is valid.
22:16	PDU_CNT	PDU count of packet.
15:0	IDX	Index of BD. To get actual physical address must be added to BD/PDU base.

0x3000470 DXE_0_CH1_HEAD

Type: read-only
Reset State: 0x00000000

Address of head of packet.

DXE_0_CH1_HEAD

Bits	Name	Description
31:27	RSVD	Reserved. Reset State: 0x00000000
26	DESCVAL	Descriptor valid. Signifies descriptor has already been loaded. Used to prevent reloading of a descriptor. Reset State: 0x00000000
25:21	DWQID	Destination WQ ID. Original BMU, UIF or EIF destination queue. Valid only when CH_CSR[DIQ]=1 Reset State: 0x00000000
20:16	SWQID	Source WQ ID. Original BMU, UIF or EIF source queue. Valid only when CH_CSR[SIQ]=1 Reset State: 0x00000000
15:0	IDX	Index of Head. Must be added to BD/PDU base for actual physical address.

0x3000474 DXE_0_CH1_TAIL

Type: read-only
Reset State: 0x00000000

Address of tail of packet.

DXE_0_CH1_TAIL

Bits	Name	Description
31:16	RSVD	Reserved. Reset State: 0x00000000
15:0	IDX	Index of Tail. Must be added to BD/PDU base for actual physical address

0x3000478 DXE_0_CH1_PDU

Type: read-only
Reset State: 0x00000000

PDU info register.

All its fields are working fields that get modified as the programmed operation progresses.

DXE_0_CH1_PDU

Bits	Name	Description
31	RSVD	Reserved. Always returns 0 when read. Reset State: 0x00000000
30:24	PDU_CNT	Current PDU count.
23:8	IDX	Index of current PDU. Must be added to BD/PDU base for actual physical address
7:0	FST_OFF	First PDU offset.

0x300047C DXE_0_CH1_TSTMP

Type: read-only
Reset State: 0x00000000

Contains last sampled value of the system timestamp

DXE_0_CH1_TSTMP

Bits	Name	Description
31:0	VALUE	Reset State: 0x00000000

0x3000480 DXE_0_CH2_CTRL

Type: read-write
Reset State: 0x10800708

Serves to configure channel 2 operation

DXE_0_CH2_CTRL

Bits	Name	Description
31	SWAP	Endian Byte Swap Enable. When high instructs DXE to perform an endian swap of the incoming byte stream. The corresponding bit field in the DXE descriptor control word is located at DXE_DESC_CTRL[20]

DXE_0_CH2_CTRL (cont.)

Bits	Name	Description
30:29	BDT_IDX	BD Template Index. When XTYPE=H2B and BDH=1, DXE supports creating a BD by using template data from one of up to 4 different BD templates. The BD template base store is pointed at by the DXE BD_TMPLT(H/L) registers and the address used to read the template data is calculated as follows: BD_TMPLT_ADRR = BD_TMPLT_BASE + (128 * CH_CTRL[BDT_IDX]) The corresponding bit field in the control word of the external descriptor is mapped to bits[19:18]
28	DFMT	Descriptor Format. This bit field is used to select between long and short descriptor formats. When using the short descriptor format, the high part of the source, destination and descriptor addresses will be taken from the SADRH_DFLT, DADRH_DFLT or DESCH_DFLT registers respectively. Default is to use the long descriptor format 0x0: SHORT 0x1: LONG Reset State: 0x00000001
27	ABORT	Writing a one to this bit will cause the channel to stop its current transfer and set the ERR bit and ERR_CODE fields in CH_STATUS. Note that if the channel is currently disabled or if it is about to be disabled because it has just finished its programmed transfer, then the abort request will be ignored and the error bit and error codes won't be set. If the channel is currently masked by the arbiter then setting this bit will forcibly unmask it so that the transfer can be aborted the next time the channel is selected by the internal arbiter. The abort request is automatically cleared by hardware once the channel has aborted the transfer. Also note that since the DXE will not attempt to do any cleanup when a transfer is aborted, software might need to do so. For example, for H2B transfers, software should manually release the BD and any PDUs currently in use by the partial transfer or else a BD/PDU leak will result. Reset State: 0x00000000
26	ENDIANNESS	Specifies the endianness of the master generating the data. Affects alignment of valid bytes for non-dword aligned reads/writes. The corresponding field in the DXE descriptor control word is located in DXE_DESC_CTRL[21] 0x0: BIGEND 0x1: LTLEND Reset State: 0x00000000
25:22	CTR_SEL	Counter Select. If the event counters are enabled (DMA_CSR[ECTR_EN]=1) then this bit field selects the counter that will be incremented at the end of the transfer. By default the value in this bit field is the same as the channel number so that after reset channel 0 increments counter 0, channel 1 increments counter 1 and so on. Reset State: 0x00000002

DXE_0_CH2_CTRL (cont.)

Bits	Name	Description
21	EDVEN	When set, the DMA engine will clear the VAL bit in the DESC_CSR word of the current descriptor once it has completed processing it. This is useful for implementing a descriptor "ring" (see the description of the VALID bit in Table 3.1) Reset State: 0x00000000
20	EDEN	External Descriptor Enable. Use External Descriptor Linked List Reset State: 0x00000000
19	INE_DONE	Enable Channel Interrupt when Channel is Done. The corresponding interrupt source bit is INT_DONE Reset State: 0x00000000
18	INE_ERR	Enable Channel Interrupt on Errors. The corresponding interrupt source bit is INT_ERR Reset State: 0x00000000
17	INE_ED	Enable External Descriptor Interrupt. When this bit is set, an interrupt will be generated after processing a descriptor item that has the INT bit set in its DESC_CTRL word (see Table 3.1). The corresponding interrupt source bit is INT_ED Reset State: 0x00000000
16	STOP	Channel processing stopped due to a request in the last processed linked list descriptor (see the STOP bit in the definition of the DESC_CSR word in Table 3.1). This bit will be automatically cleared when the channel is restarted. Reset State: 0x00000000
15:13	PRIO	This field sets the channel priority. 7: Highest Priority. 0: Lowest Priority.

DXE_0_CH2_CTRL (cont.)

Bits	Name	Description
12:9	BTHLD_SEL	BMU Threshold Select. This value tells DXE which of the BMU BD/PDU thresholds to check before issuing BMU commands that reserve, or get BDs or PDUs. It also specifies the module index value that will be used to issue any required BMU commands (see BMU spec for details). The value of this bit field is only meaningful for transfer types that involve the BMU and therefore its value will be ignored for H2H transfers. 0x0: RSVD0 0x1: RSVD1 0x2: THLD2 0x3: THLD3 0x4: THLD4 0x5: THLD5 0x6: THLD6 0x7: THLD7 0x8: THLD8 0x9: THLD9 0xA: THLD10 0xB: RSVD11 0xC: RSVD12 0xD: RSVD13 0xE: RSVD14 0xF: RSVD15 Reset State: 0x00000003
8	PDU_REL	0x0: Don't release BD and PDUs when done. 1: Release BD and PDUs when done. 0x0: KEEP 0x1: RELEASE Reset State: 0x00000001

DXE_0_CH2_CTRL (cont.)

Bits	Name	Description
7	PIQ	next descriptor Pointer address Is Queue. When set the source of the descriptor address is interepreted as a queue ID instead of just the address of a flat memory location. The only valid source queues for descriptors are the UIF Tx data and Tx management endpoints. Any other IDs will result the channel aborting the transfer with an invalid source queue error. Therefore, when this bit is set, software must ensure that the CH_DESCL[QID] bit field is set to a valid queue ID and that the CH_DESCL[BASE] bit field is set to the base address of the source UIF endpoint. This base address is formed by taking the base address for the UIF block in the SAHB bus which can be found in the Nova address map document and then adding the internal UIF offset for the correct source endpoint. This offsets can be obtained from the UIF specification document. For convenience, the current internal UIF offsets are provided in the descripiton of the QID bit field in the CH_DESCL register description. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
6	DIQ	Destination Is Queue. When set the destination address is interepreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF RX endpoints or and EIF outbound FIFO. When this bit is set, software must ensure that the DADR[QID] bit field is set to a valid queue ID and that the DADR[BASE] bit field is set to the base address of the destination queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
5	SIQ	Source Is Queue. When set the source address is interepreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF TX endpoints or and EIF inbound FIFO. When this bit is set, software must ensure that the SADR[QID] bit field is set to a valid queue ID and that the SADR[BASE] bit field is set to the base address of the source queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000

DXE_0_CH2_CTRL (cont.)

Bits	Name	Description
4	BDH	BD Handling bit. The behavior depends on the setting of XTYPE. If XTYPE is: H2B: Then if BDH is: 0: Use first 128 bytes of packet as BD. 1: Create BD from BD template (Up to 4 supported. Also see desc for BDT_IDX). B2H: Then if BDH is: 0: Insert BD in front of payload. 1: Discard BD. For XTYPE values of H2H and B2B the value of this bit is ignored. Reset State: 0x00000000
3	EOP	End of Packet bit. For H2B transfers marks the end of a packet Please note that when not using external descriptors DXE cannot support the gather functionality and therefore the EOP bit must be set. For XTYPE values of H2H, B2B and B2H the value of this bit is ignored. Reset State: 0x00000001
2:1	XTYPE	Transfer Type. Specifies the type of transfer to perform: 00: H2H. Host space to Host space transfer. 01: B2B. BMU space to BMU space transfer. 10: H2B. Host space to BMU translation. 11: B2H. BMU space to Host space translation. For cross-space transfers (H2B and B2H) the DMA engine will also perform the required data format translation. The format translation behavior can be modified by the setting of the BDH and PAD bits. 0x0: H2H 0x1: B2B 0x2: H2B 0x3: B2H
0	EN	Channel Enable or Restart. Writing this bit with a one either starts a new DMA transfer according to the parameters programmed in the channel's configuration registers and clears the DONE bit or, if the channel is already enabled but the STOP bit is set, then it restarts channel processing and also clears the STOP bit. This bit is automatically cleared when a single transfer completes or, if the channel is configured to use linked list descriptors, when the last transfer in the descriptor linked list completes (DESC_NXT is NULL or/and DESC_CSR[VALID]=0). The channel is also disabled and this bit cleared if a channel error is encountered. Reading this bit indicates whether a channel is currently enabled or disabled:. 0: Channel Disabled. 1: Channel Enabled. The Channel Enable bit status can also be found by reading the DMA_ENCH register which aggregates the EN bits of all channels. Note: Software must take care to not disable the channel while it is busy or data could be lost. Reset State: 0x00000000

0x3000484 DXE_0_CH2_STATUS

Type: read-write
Reset State: 0x00000000

Serves to report the status of the programmed channel operation.

DXE_0_CH2_STATUS

Bits	Name	Description
31:16	RSVD	Reserved. Reads always return 0. Writes are ignored.
15	INT_DONE	Interrupt Source: Asserted when the channel has finished all processing.
14	INT_ERR	Interrupt Source: Asserted when a channel error has occurred. Masked by the INE_ERR
13	INT_ED	Interrupt Source. Descriptor Done and INT requested
12	ABORT_REQ	Abort Request. Software has requested that the current operation be aborted. However, if CH_STATUS[EN] is still set then the channel has registered the request but is not yet in a position to abort the transfer "safely". Once the channel finishes its current operation it will abort the transfer and set the error flag and error code bit fields accordingly.
11	STOP_REQ	Stop Request. Software has requested that the channel stop it operation after the current descriptor has been processed. Once this happens the STOPD bit field will be set to one and the channel will be disabled.

DXE_0_CH2_STATUS (cont.)

Bits	Name	Description
10:6	ERR_CODE	Used to identify the source or cause of an error. 0x0: NONE 0x1: SAHB_ERR 0x2: H2H_RD_BUS_ERR 0x3: H2H_WR_BUS_ERR 0x4: PRG_INV_XTYPE 0x5: BERR_POPWQ 0x6: BERR_PUSHWQ 0x7: BERR_RLSS 0x8: BERR_GETPDU 0x9: PRG_INV_WQ 0xA: PRG_INV_H2H_SRC_QID 0xB: PRG_INV_H2H_DST_QID 0xC: PRG_INV_B2H_SRC_QID 0xD: PRG_INV_B2H_DST_QID 0xE: PRG_INV_B2H_SRC_IDX 0xF: PRG_INV_H2B_SRC_QID 0x10: PRG_INV_H2B_DST_QID 0x11: PRG_INV_H2B_DST_IDX 0x12: PRG_INV_H2B_SZ 0x13: PRG_INV_SADR 0x14: PRG_INV_DADR 0x15: PRG_INV_EDADR 0x16: PRG_INV_SRC_WQID 0x17: PRG_INV_DST_WQID 0x18: PRG_XTYPE_MSMTCH 0x19: PKT_ERR 0x1A: ABORT 0x1B: PDU_CNT_OVFL Reset State: 0x00000000
5	ERR	DMA channel stopped due to error. To clear the error status it is necessary to write a 1 into this bit position.
4	STOPD	Channel Stopped. The channel has stopped further processing and disabled itself due to a stop request in the last processed descriptor. Reset State: 0x00000000
3	MSKD	Channel Masked. The channel has been automatically masked out from arbitration due to a blocking condition. Reset State: 0x00000000
2	DONE	DMA channel Done. This bit will be automatically cleared the next time the channel is enabled. Reset State: 0x00000000
1	BUSY	Channel busy. HIgh when the channel is enabled and currently active (won internal arbitration) Reset State: 0x00000000

DXE_0_CH2_STATUS (cont.)

Bits	Name	Description
0	EN	Channel Enabled. Copy of CH_CTRL[EN]. Reset State: 0x00000000

0x3000488 DXE_0_CH2_SZ

Type: read-write

The transfer size register specifies the total, remaining, and burst or 'chunk' transfer sizes for each channel. The maximum total transfer size is 16K-1 bytes. The chunk size control can be useful to control the relative bandwidth used by each channel as the dma engine will change channels, release the AHB bus, and rearbitrate for access after transferring chunk size bytes.

DXE_0_CH2_SZ

Bits	Name	Description
31:28	CHK_SZ	Chunk transfer size. Specifies the number of bytes (in multiples of 8) to be transferred at one given time (not implying they are buffered but that they will be transferred for each start event in one bus request cycle). If chunk size is zero the DMA engine will always perform maximum chunk size transfers. Maximum chunk size is 128 bytes.
27:14	REM_SZ	Remaining transfer size. Specifies the number of bytes that remain to be transferred to complete the current operation.
13:0	TOT_SZ	Total Transfer Size. Specifies the number of bytes to be transferred. Maximum total transfer size is (4K-1) bytes. Note: This field is unnecessary and will be ignored for B2H or B2B transfers, when the source of the transfer is in BMU space (either BMU queue or direct pointer to BD). This is because the size of the transfer will be the packet length encoded in the BD at offset 0x0c bits [11:0].

0x300048C DXE_0_CH2_SADRL

Type: read-write

The channel source address register specifies either the source address in flat internal or external memory, or else the BMU queue ID, UIF TX endpoint ID, or EIF inbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the source, addresses can have arbitrary byte-alignment When using a BMU queue, UIF endpoint or EIF fifo as a source, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[SIQ] bit. When CH_CSR[SIQ] is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when it is set this register has two bit fields: The SQID bit field

used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF source endpoint/FIFO.

For B2H or B2B transfers, when the source is a BMU Queue ID (CH_CSR[SIQ] = 1 and SWQID matches BMU), the DXE will issue a BMU POPWQ command to pop the specified queue and obtain the BD index of the source packet. Else, when the source is an address (CH_CSR[SIQ] = 0), the DXE will interpret the address as the index of the packet BD and will add it to the BMU_BASE to obtain the physical addresss to use to fetch it directly from memory.

For H2B or H2H transfers, if the source is a UIF endpoint or EIF FIFO (CH_CSR[SIQ] = 1 and SQID matches UIF/EIF), software should program the SAHB base address of the UIF source endpoint in the BASE bit field and the queue ID to match in the SWQID bit field, then the DXE will use the base address given to generate the physical address and read the data over the SAHB bus and also use the appropriate sideband signals as specified by the SQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and SQID fields are consistend and refer to the same endpoint or else hangs or unpredictable behavior might occur. Else, when the source is just a location in flat memory space, (CH_CSR[SIQ] = 0), the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the physical address to use to fetch the data. For this case, software should make sure that the provided address maps to the intended source interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus.

To summarize, for B2H and B2B transfers the address must conform to the following format:

For index of BD mode (CH_CSR[SIQ] = 0):

   ADDR[31:7] = BMU_BASE + BD_INDEX[15:0]

   ADDR[6:0] = 7'd0

For BMU Queue ID mode (CH_CSR[SIQ] = 1 & SQID matching one of the BMU queues):

   ADDR[31:7] = Any value will do but zero preferred

   ADDR[6:0] = Any BMU Queue ID as specified in description of SQID field

For H2B and H2H transfers the address must conform to the following format:

For sources in flat memory space (CH_CSR[SIQ] = 0):   ADDR[31:0] = address mapping to source interface

For UIF RX endpoints or EIF FIFOs (CH_CSR[SIQ] = 1 & QID matching UIF or EIF):

   ADDR[31:7] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document)

   ADDR[6:0] = Queue ID matching UIF or EIF as specified in description of SQID field

DXE_0_CH2_SADRL

Bits	Name	Description
31:7	BASE	Base Address. For this case, this bit field provides the base address of the source UIF TX endpoint or EIF inbound FIFO. The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd Please consult the appropriate interface uarch for the offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH2_SADRL (cont.)

Bits	Name	Description
6:0	SQID	Source Queue ID. Valid only when the CH_CSR[SIQ] bit is set. For this case, this bit field provides the ID for the source BMU, UIF or EIF queue to be used for the transfer. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: RSVD_25 0x1A: RSVD_26 0x1B: RSVD_27 0x1C: RSVD_28 0x1D: RSVD_29 0x1E: RSVD_30 0x1F: RSVD_31

0x3000490 DXE_0_CH2_SADRH

Type: read-write

The channel source address high register holds the high bits of the source address for a transfer. Please see the description of CH_SADRL for more info.

DXE_0_CH2_SADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_SADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x3000494 DXE_0_CH2_DADRL

Type: read-write

The channel destination address register specifies either the destination address in flat internal or external memory, or else the BMU queue ID, UIF RX endpoint ID, or EIF outbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the destination, addresses can have arbitrary byte-alignment. When using a BMU queue, UIF endpoint or EIF fifo as a destination, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[DIQ] bit. When this bit is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when the bit is set this register has two bit fields: The DQID bit field used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF destination endpoint/FIFO.

For H2B or B2B transfers, when using a BMU queue as the destination (CH_CSR[DIQ] = 1 and DQID matches BMU), the DXE will push the index of the BD of the packet into the specified queue at the end of the packet transfer. Therefore, software is responsible for programming a valid BMU Queue ID.

Else, when the destination is an index (CH_CSR[DIQ] = 0), the BD will be written to the address obtained by adding the provided index to the BMU_BASE, again, the software must ensure that said address is legal and known to BMU. That is, software must preallocate the BD (get the BD from BMU via GET BD/PDU cmd) for the BD before starting the transfer. For B2H or H2H transfers, if the destination is a UIF endpoint or EIF FIFO (CH_CSR[DIQ] = 1 and DQID matches UIF/EIF), software should program the SAHB base address of the UIF destination endpoint in the BASE bit field and the queue ID to match in the DQID bit field, then the DXE will use the base address given to generate the physical address and write the data over the SAHB bus and also use the appropriate sideband signals as specified by the DQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and DQID fields are consistent and refer

to the same endpoint else hangs or unpredictable behavior might occur. On the other hand, when the destination is just a location in flat memory space, (CH_CSR[DIQ] = 0), be it internal or external, the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the address to write the data. For this case, software should make sure that the address maps to the intended destination interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus. To summarize, for H2B and B2B transfers the address must conform to the following format:

For index of BD mode (CH_CSR[DIQ] = 0):   ADDR[31:7] = BMU_BASE + BD_INDEX[15:0]

   ADDR[6:0] = 7'd0

For BMU Queue ID mode (CH_CSR[DIQ] = 1 & DQID matching one of the BMU queues):

   ADDR[31:5] = Any value will do but zero preferred

   ADDR[4:0] = Any BMU Queue ID as specified in description of QID field

For B2H and H2H transfers the address must conform to the following format:

For destinations in flat memory space (CH_CSR[DIQ] = 0):   ADDR[31:0] = address mapping to destination interface

For UIF RX endpoints or EIF FIFOs (CH_CSR[DIQ] = 1 & DQID matching UIF or EIF):

   ADDR[31:5] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document)

   ADDR[4:0] = Queue ID matching UIF or EIF as specified in description of DQID field

DXE_0_CH2_DADRL

Bits	Name	Description
31:7	BASE	Base Address. Valid only when the CH_CSR[DIQ] bit is set. For this case, this bit field provides the base address of the destination UIF RX endpoint or EIF outbound FIFO (for BMU software may use any value can be used but zero is suggested). The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd Please consult the appropriate interface uarch for the offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH2_DADRL (cont.)

Bits	Name	Description
6:0	DQID	Destination Queue ID. is set. For this case, this bit field provides the ID for the destination BMU WQ, UIF RX endpoint or EIF outbound queue to be used for the transfer. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: RSVD_0 0x1: RSVD_1 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: BMU_25 0x1A: BMU_26 0x1B: BMU_SINK_WQ 0x1C: UIF_RX_1_EP 0x1D: UIF_RX_2_EP 0x1E: UIF_RX_3_EP 0x1F: UIF_RX_4_EP

0x3000498 DXE_0_CH2_DADRH

Type: read-write

The channel destination address high register holds the high bits of the destination address for a transfer. Please see the description of CH_DADRL for more info.

DXE_0_CH2_DADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	This register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x300049C DXE_0_CH2_DESCL

Type: read-write

The Channel 2 Linked List Descriptor Pointer register contains the 32 lower bits of the address of the next descriptor to be loaded in the linked list. This address must be dword (32-bit) aligned (addr[1:0]=0 if CH_CTRL[PIQ]=0). Each complete transfer descriptor consists of 7 32-bit values arranged contiguously in memory. The value of this register will be overwritten with the address of the start of the next descriptor set in the list after the current descriptor has been fetched. The meaning of the value in this register depends on the value of the CH_CTRL[PIQ] bit field similar to the way in which SADRL and DADRL are depending in SIQ and DIQ respectively. For CH_CTRL[PIQ]=0 then this register has no bit fields and the value is just intrepreted as an address in flat memory space. When CH_CTRL[PIQ] is set then the descriptor will be read from FIFO type memory in UIF and the register has 2 bit fields: BASE, and SQID. BASE specifies the base address of the UIF Tx queue (derived from the start of the UIF address space in SAHB plus the internal UIF offset).

DXE_0_CH2_DESCL

Bits	Name	Description
31:7	BASE	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify the base address of the UIF endpoint to use as the source of the descriptor. Please refer to the Nova address map document and to the UIF architecture document for guaranteed correct values to use here. For convenience but without a guarantee of accuracy, the base value to use for both the Tx data and management endpoints is the following: base = UIF base + TD_and_TM_offset = 0x0E02_5000 + x100 = 0x0E02_5100>>7 = 0x1C_04A2

DXE_0_CH2_DESCL (cont.)

Bits	Name	Description
6:0	SQID	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify which of the two UIF TX queues to use. Note that in this case software also needs to program the correct base address of the source UIF endpoint in the BASE bit field. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x30004A0 DXE_0_CH2_DESCH

Type: read-write

The channel destination address high register holds the high bits of the the address of the next descriptor to be loaded in the linked list.

DXE_0_CH2_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. Please note that if the source of the descriptor is either of the UIF endpoints (CH_CTRL[PIQ]=1) then the value in ADDRH has to be 0 or else the descriptor read could end up mapping to the XIF or PIF. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x30004A4 DXE_0_CH2_LST_DESCL

Type: read-only

The read-only Channel 2 Current/last Linked List Descriptor Pointer register contains the low 32-bits of the address of the descriptor currently being processed or of the last descriptor processed if the channel is disabled.

The meaning of the value and bit fields with regards to CH_CTRL[PIQ] is the same as was explained for the CH_DESCL register.

DXE_0_CH2_LST_DESCL

Bits	Name	Description
31:7	BASE	See description of CH_DESCL[BASE].
6:0	SQID	See description of CH_DESCL[SQID]. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x30004A8 DXE_0_CH2_LST_DESCH

Type: read-only

The channel destination address high register holds the high bits of the the address of the next descriptor to be loaded in the linked list. Note that The meaning of the value and bit fields is the same as was explained for the CH_DESCL register.

DXE_0_CH2_LST_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address.

0x30004AC DXE_0_CH2_BD

Type: read-only

DXE_0_CH2_BD

Bits	Name	Description
31:24	RSVD	Reserved. Always returns 0 when read.
23	VAL	Valid. BD has been loaded and is valid.
22:16	PDU_CNT	PDU count of packet.
15:0	IDX	Index of BD. To get actual physical address must be added to BD/PDU base.

0x30004B0 DXE_0_CH2_HEAD

Type: read-only
Reset State: 0x00000000

Address of head of packet.

DXE_0_CH2_HEAD

Bits	Name	Description
31:27	RSVD	Reserved. Reset State: 0x00000000
26	DESCVAL	Descriptor valid. Signifies descriptor has already been loaded. Used to prevent reloading of a descriptor. Reset State: 0x00000000
25:21	DWQID	Destination WQ ID. Original BMU, UIF or EIF destination queue. Valid only when CH_CSR[DIQ]=1 Reset State: 0x00000000
20:16	SWQID	Source WQ ID. Original BMU, UIF or EIF source queue. Valid only when CH_CSR[SIQ]=1 Reset State: 0x00000000
15:0	IDX	Index of Head. Must be added to BD/PDU base for actual physical address.

0x30004B4 DXE_0_CH2_TAIL

Type: read-only
Reset State: 0x00000000

Address of tail of packet.

DXE_0_CH2_TAIL

Bits	Name	Description
31:16	RSVD	Reserved. Reset State: 0x00000000
15:0	IDX	Index of Tail. Must be added to BD/PDU base for actual physical address

0x30004B8 DXE_0_CH2_PDU

Type: read-only
Reset State: 0x00000000

PDU info register.

All its fields are working fields that get modified as the programmed operation progresses.

DXE_0_CH2_PDU

Bits	Name	Description
31	RSVD	Reserved. Always returns 0 when read. Reset State: 0x00000000
30:24	PDU_CNT	Current PDU count.
23:8	IDX	Index of current PDU. Must be added to BD/PDU base for actual physical address
7:0	FST_OFF	First PDU offset.

0x30004BC DXE_0_CH2_TSTMP

Type: read-only
Reset State: 0x00000000

Contains last sampled value of the system timestamp

DXE_0_CH2_TSTMP

Bits	Name	Description
31:0	VALUE	Reset State: 0x00000000

0x30004C0 DXE_0_CH3_CTRL

Type: read-write
Reset State: 0x10C00708

Serves to configure channel 3 operation

DXE_0_CH3_CTRL

Bits	Name	Description
31	SWAP	Endian Byte Swap Enable. When high instructs DXE to perform an endian swap of the incoming byte stream. The corresponding bit field in the DXE descriptor control word is located at DXE_DESC_CTRL[20]

DXE_0_CH3_CTRL (cont.)

Bits	Name	Description
30:29	BDT_IDX	BD Template Index. When XTYPE=H2B and BDH=1, DXE supports creating a BD by using template data from one of up to 4 different BD templates. The BD template base store is pointed at by the DXE BD_TMPLT(H/L) registers and the address used to read the template data is calculated as follows: BD_TMPLT_ADRR = BD_TMPLT_BASE + (128 * CH_CTRL[BDT_IDX]) The corresponding bit field in the control word of the external descriptor is mapped to bits[19:18]
28	DFMT	Descriptor Format. This bit field is used to select between long and short descriptor formats. When using the short descriptor format, the high part of the source, destination and descriptor addresses will be taken from the SADRH_DFLT, DADRH_DFLT or DESCH_DFLT registers respectively. Default is to use the long descriptor format 0x0: SHORT 0x1: LONG Reset State: 0x00000001
27	ABORT	Writing a one to this bit will cause the channel to stop its current transfer and set the ERR bit and ERR_CODE fields in CH_STATUS. Note that if the channel is currently disabled or if it is about to be disabled because it has just finished its programmed transfer, then the abort request will be ignored and the error bit and error codes won't be set. If the channel is currently masked by the arbiter then setting this bit will forcibly unmask it so that the transfer can be aborted the next time the channel is selected by the internal arbiter. The abort request is automatically cleared by hardware once the channel has aborted the transfer. Also note that since the DXE will not attempt to do any cleanup when a transfer is aborted, software might need to do so. For example, for H2B transfers, software should manually release the BD and any PDUs currently in use by the partial transfer or else a BD/PDU leak will result. Reset State: 0x00000000
26	ENDIANNESS	Specifies the endianness of the master generating the data. Affects alignment of valid bytes for non-dword aligned reads/writes. The corresponding field in the DXE descriptor control word is located in DXE_DESC_CTRL[21] 0x0: BIGEND 0x1: LTLEND Reset State: 0x00000000
25:22	CTR_SEL	Counter Select. If the event counters are enabled (DMA_CSR[ECTR_EN]=1) then this bit field selects the counter that will be incremented at the end of the transfer. By default the value in this bit field is the same as the channel number so that after reset channel 0 increments counter 0, channel 1 increments counter 1 and so on. Reset State: 0x00000003

DXE_0_CH3_CTRL (cont.)

Bits	Name	Description
21	EDVEN	When set, the DMA engine will clear the VAL bit in the DESC_CSR word of the current descriptor once it has completed processing it. This is useful for implementing a descriptor "ring" (see the description of the VALID bit in Table 3.1) Reset State: 0x00000000
20	EDEN	External Descriptor Enable. Use External Descriptor Linked List Reset State: 0x00000000
19	INE_DONE	Enable Channel Interrupt when Channel is Done. The corresponding interrupt source bit is INT_DONE Reset State: 0x00000000
18	INE_ERR	Enable Channel Interrupt on Errors. The corresponding interrupt source bit is INT_ERR Reset State: 0x00000000
17	INE_ED	Enable External Descriptor Interrupt. When this bit is set, an interrupt will be generated after processing a descriptor item that has the INT bit set in its DESC_CTRL word (see Table 3.1). The corresponding interrupt source bit is INT_ED Reset State: 0x00000000
16	STOP	Channel processing stopped due to a request in the last processed linked list descriptor (see the STOP bit in the definition of the DESC_CSR word in Table 3.1). This bit will be automatically cleared when the channel is restarted. Reset State: 0x00000000
15:13	PRIO	This field sets the channel priority. 7: Highest Priority. 0: Lowest Priority.

DXE_0_CH3_CTRL (cont.)

Bits	Name	Description
12:9	BTHLD_SEL	BMU Threshold Select. This value tells DXE which of the BMU BD/PDU thresholds to check before issuing BMU commands that reserve, or get BDs or PDUs. It also specifies the module index value that will be used to issue any required BMU commands (see BMU spec for details). The value of this bit field is only meaningful for transfer types that involve the BMU and therefore its value will be ignored for H2H transfers. 0x0: RSVD0 0x1: RSVD1 0x2: THLD2 0x3: THLD3 0x4: THLD4 0x5: THLD5 0x6: THLD6 0x7: THLD7 0x8: THLD8 0x9: THLD9 0xA: THLD10 0xB: RSVD11 0xC: RSVD12 0xD: RSVD13 0xE: RSVD14 0xF: RSVD15 Reset State: 0x00000003
8	PDU_REL	0x0: Don't release BD and PDUs when done. 1: Release BD and PDUs when done. 0x0: KEEP 0x1: RELEASE Reset State: 0x00000001

DXE_0_CH3_CTRL (cont.)

Bits	Name	Description
7	PIQ	next descriptor Pointer address Is Queue. When set the source of the descriptor address is interepreted as a queue ID instead of just the address of a flat memory location. The only valid source queues for descriptors are the UIF Tx data and Tx management endpoints. Any other IDs will result the channel aborting the transfer with an invalid source queue error. Therefore, when this bit is set, software must ensure that the CH_DESCL[QID] bit field is set to a valid queue ID and that the CH_DESCL[BASE] bit field is set to the base address of the source UIF endpoint. This base address is formed by taking the base address for the UIF block in the SAHB bus which can be found in the Nova address map document and then adding the internal UIF offset for the correct source endpoint. This offsets can be obtained from the UIF specification document. For convenience, the current internal UIF offsets are provided in the descripiton of the QID bit field in the CH_DESCL register description. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
6	DIQ	Destination Is Queue. When set the destination address is interepreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF RX endpoints or and EIF outbound FIFO. When this bit is set, software must ensure that the DADR[QID] bit field is set to a valid queue ID and that the DADR[BASE] bit field is set to the base address of the destination queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
5	SIQ	Source Is Queue. When set the source address is interepreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF TX endpoints or and EIF inbound FIFO. When this bit is set, software must ensure that the SADR[QID] bit field is set to a valid queue ID and that the SADR[BASE] bit field is set to the base address of the source queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000

DXE_0_CH3_CTRL (cont.)

Bits	Name	Description
4	BDH	BD Handling bit. The behavior depends on the setting of XTYPE. If XTYPE is: H2B: Then if BDH is: 0: Use first 128 bytes of packet as BD. 1: Create BD from BD template (Up to 4 supported. Also see desc for BDT_IDX). B2H: Then if BDH is: 0: Insert BD in front of payload. 1: Discard BD. For XTYPE values of H2H and B2B the value of this bit is ignored. Reset State: 0x00000000
3	EOP	End of Packet bit. For H2B transfers marks the end of a packet Please note that when not using external descriptors DXE cannot support the gather functionality and therefore the EOP bit must be set. For XTYPE values of H2H, B2B and B2H the value of this bit is ignored. Reset State: 0x00000001
2:1	XTYPE	Transfer Type. Specifies the type of transfer to perform: 00: H2H. Host space to Host space transfer. 01: B2B. BMU space to BMU space transfer. 10: H2B. Host space to BMU translation. 11: B2H. BMU space to Host space translation. For cross-space transfers (H2B and B2H) the DMA engine will also perform the required data format translation. The format translation behavior can be modified by the setting of the BDH and PAD bits. 0x0: H2H 0x1: B2B 0x2: H2B 0x3: B2H
0	EN	Channel Enable or Restart. Writing this bit with a one either starts a new DMA transfer according to the parameters programmed in the channel's configuration registers and clears the DONE bit or, if the channel is already enabled but the STOP bit is set, then it restarts channel processing and also clears the STOP bit. This bit is automatically cleared when a single transfer completes or, if the channel is configured to use linked list descriptors, when the last transfer in the descriptor linked list completes (DESC_NXT is NULL or/and DESC_CSR[VALID]=0). The channel is also disabled and this bit cleared if a channel error is encountered. Reading this bit indicates whether a channel is currently enabled or disabled:. 0: Channel Disabled. 1: Channel Enabled. The Channel Enable bit status can also be found by reading the DMA_ENCH register which aggregates the EN bits of all channels. Note: Software must take care to not disable the channel while it is busy or data could be lost. Reset State: 0x00000000

0x30004C4 DXE_0_CH3_STATUS

Type: read-write
Reset State: 0x00000000

Serves to report the status of the programmed channel operation.

DXE_0_CH3_STATUS

Bits	Name	Description
31:16	RSVD	Reserved. Reads always return 0. Writes are ignored.
15	INT_DONE	Interrupt Source: Asserted when the channel has finished all processing.
14	INT_ERR	Interrupt Source: Asserted when a channel error has occurred. Masked by the INE_ERR
13	INT_ED	Interrupt Source. Descriptor Done and INT requested
12	ABORT_REQ	Abort Request. Software has requested that the current operation be aborted. However, if CH_STATUS[EN] is still set then the channel has registered the request but is not yet in a position to abort the transfer "safely". Once the channel finishes its current operation it will abort the transfer and set the error flag and error code bit fields accordingly.
11	STOP_REQ	Stop Request. Software has requested that the channel stop it operation after the current descriptor has been processed. Once this happens the STOPD bit field will be set to one and the channel will be disabled.

DXE_0_CH3_STATUS (cont.)

Bits	Name	Description
10:6	ERR_CODE	Used to identify the source or cause of an error. 0x0: NONE 0x1: SAHB_ERR 0x2: H2H_RD_BUS_ERR 0x3: H2H_WR_BUS_ERR 0x4: PRG_INV_XTYPE 0x5: BERR_POPWQ 0x6: BERR_PUSHWQ 0x7: BERR_RLSS 0x8: BERR_GETPDU 0x9: PRG_INV_WQ 0xA: PRG_INV_H2H_SRC_QID 0xB: PRG_INV_H2H_DST_QID 0xC: PRG_INV_B2H_SRC_QID 0xD: PRG_INV_B2H_DST_QID 0xE: PRG_INV_B2H_SRC_IDX 0xF: PRG_INV_H2B_SRC_QID 0x10: PRG_INV_H2B_DST_QID 0x11: PRG_INV_H2B_DST_IDX 0x12: PRG_INV_H2B_SZ 0x13: PRG_INV_SADR 0x14: PRG_INV_DADR 0x15: PRG_INV_EDADR 0x16: PRG_INV_SRC_WQID 0x17: PRG_INV_DST_WQID 0x18: PRG_XTYPE_MSMTCH 0x19: PKT_ERR 0x1A: ABORT 0x1B: PDU_CNT_OVFL Reset State: 0x00000000
5	ERR	DMA channel stopped due to error. To clear the error status it is necessary to write a 1 into this bit position.
4	STOPD	Channel Stopped. The channel has stopped further processing and disabled itself due to a stop request in the last processed descriptor. Reset State: 0x00000000
3	MSKD	Channel Masked. The channel has been automatically masked out from arbitration due to a blocking condition. Reset State: 0x00000000
2	DONE	DMA channel Done. This bit will be automatically cleared the next time the channel is enabled. Reset State: 0x00000000
1	BUSY	Channel busy. HIgh when the channel is enabled and currently active (won internal arbitration) Reset State: 0x00000000

DXE_0_CH3_STATUS (cont.)

Bits	Name	Description
0	EN	Channel Enabled. Copy of CH_CTRL[EN]. Reset State: 0x00000000

0x30004C8 DXE_0_CH3_SZ

Type: read-write

The transfer size register specifies the total, remaining, and burst or 'chunk' transfer sizes for each channel. The maximum total transfer size is 16K-1 bytes. The chunk size control can be useful to control the relative bandwidth used by each channel as the dma engine will change channels, release the AHB bus, and rearbitrate for access after transferring chunk size bytes.

DXE_0_CH3_SZ

Bits	Name	Description
31:28	CHK_SZ	Chunk transfer size. Specifies the number of bytes (in multiples of 8) to be transferred at one given time (not implying they are buffered but that they will be transferred for each start event in one bus request cycle). If chunk size is zero the DMA engine will always perform maximum chunk size transfers. Maximum chunk size is 128 bytes.
27:14	REM_SZ	Remaining transfer size. Specifies the number of bytes that remain to be transferred to complete the current operation.
13:0	TOT_SZ	Total Transfer Size. Specifies the number of bytes to be transferred. Maximum total transfer size is (4K-1) bytes. Note: This field is unnecessary and will be ignored for B2H or B2B transfers, when the source of the transfer is in BMU space (either BMU queue or direct pointer to BD). This is because the size of the transfer will be the packet length encoded in the BD at offset 0x0c bits [11:0].

0x30004CC DXE_0_CH3_SADRL

Type: read-write

The channel source address register specifies either the source address in flat internal or external memory, or else the BMU queue ID, UIF TX endpoint ID, or EIF inbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the source, addresses can have arbitrary byte-alignment When using a BMU queue, UIF endpoint or EIF fifo as a source, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[SIQ] bit. When CH_CSR[SIQ] is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when it is set this register has two bit fields: The SQID bit field

used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF source endpoint/FIFO.

For B2H or B2B transfers, when the source is a BMU Queue ID (CH_CSR[SIQ] = 1 and SWQID matches BMU), the DXE will issue a BMU POPWQ command to pop the specified queue and obtain the BD index of the source packet. Else, when the source is an address (CH_CSR[SIQ] = 0), the DXE will interpret the address as the index of the packet BD and will add it to the BMU_BASE to obtain the physical addresss to use to fetch it directly from memory.

For H2B or H2H transfers, if the source is a UIF endpoint or EIF FIFO (CH_CSR[SIQ] = 1 and SQID matches UIF/EIF), software should program the SAHB base address of the UIF source endpoint in the BASE bit field and the queue ID to match in the SWQID bit field, then the DXE will use the base address given to generate the physical address and read the data over the SAHB bus and also use the appropriate sideband signals as specified by the SQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and SQID fields are consistend and refer to the same endpoint or else hangs or unpredictable behavior might occur. Else, when the source is just a location in flat memory space, (CH_CSR[SIQ] = 0), the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the physical address to use to fetch the data. For this case, software should make sure that the provided address maps to the intended source interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus.

To summarize, for B2H and B2B transfers the address must conform to the following format:

For index of BD mode (CH_CSR[SIQ] = 0):

   ADDR[31:7] = BMU_BASE + BD_INDEX[15:0]

   ADDR[6:0] = 7'd0

For BMU Queue ID mode (CH_CSR[SIQ] = 1 & SQID matching one of the BMU queues):

   ADDR[31:7] = Any value will do but zero preferred

   ADDR[6:0] = Any BMU Queue ID as specified in description of SQID field

For H2B and H2H transfers the address must conform to the following format:

For sources in flat memory space (CH_CSR[SIQ] = 0):   ADDR[31:0] = address mapping to source interface

For UIF RX endpoints or EIF FIFOs (CH_CSR[SIQ] = 1 & QID matching UIF or EIF):

   ADDR[31:7] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document)

   ADDR[6:0] = Queue ID matching UIF or EIF as specified in description of SQID field

DXE_0_CH3_SADRL

Bits	Name	Description
31:7	BASE	Base Address. For this case, this bit field provides the base address of the source UIF TX endpoint or EIF inbound FIFO. The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd Please consult the appropriate interface uarch for the offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH3_SADRL (cont.)

Bits	Name	Description
6:0	SQID	Source Queue ID. Valid only when the CH_CSR[SIQ] bit is set. For this case, this bit field provides the ID for the source BMU, UIF or EIF queue to be used for the transfer. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: RSVD_25 0x1A: RSVD_26 0x1B: RSVD_27 0x1C: RSVD_28 0x1D: RSVD_29 0x1E: RSVD_30 0x1F: RSVD_31

0x30004D0 DXE_0_CH3_SADRH

Type: read-write

The channel source address high register holds the high bits of the source address for a transfer. Please see the description of CH_SADRL for more info.

DXE_0_CH3_SADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_SADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x30004D4 DXE_0_CH3_DADRL

Type: read-write

The channel destination address register specifies either the destination address in flat internal or external memory, or else the BMU queue ID, UIF RX endpoint ID, or EIF outbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the destination, addresses can have arbitrary byte-alignment. When using a BMU queue, UIF endpoint or EIF fifo as a destination, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[DIQ] bit. When this bit is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when the bit is set this register has two bit fields: The DQID bit field used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF destination endpoint/FIFO.

For H2B or B2B transfers, when using a BMU queue as the destination (CH_CSR[DIQ] = 1 and DQID matches BMU), the DXE will push the index of the BD of the packet into the specified queue at the end of the packet transfer. Therefore, software is responsible for programming a valid BMU Queue ID.

Else, when the destination is an index (CH_CSR[DIQ] = 0), the BD will be written to the address obtained by adding the provided index to the BMU_BASE, again, the software must ensure that said address is legal and known to BMU. That is, software must preallocate the BD (get the BD from BMU via GET BD/PDU cmd) for the BD before starting the transfer. For B2H or H2H transfers, if the destination is a UIF endpoint or EIF FIFO (CH_CSR[DIQ] = 1 and DQID matches UIF/EIF), software should program the SAHB base address of the UIF destination endpoint in the BASE bit field and the queue ID to match in the DQID bit field, then the DXE will use the base address given to generate the physical address and write the data over the SAHB bus and also use the appropriate sideband signals as specified by the DQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and DQID fields are consistent and refer

to the same endpoint else hangs or unpredictable behavior might occur. On the other hand, when the destination is just a location in flat memory space, (CH_CSR[DIQ] = 0), be it internal or external, the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the address to write the data. For this case, software should make sure that the address maps to the intended destination interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus. To summarize, for H2B and B2B transfers the address must conform to the following format:

For index of BD mode (CH_CSR[DIQ] = 0):   ADDR[31:7] = BMU_BASE + BD_INDEX[15:0]

   ADDR[6:0] = 7'd0

For BMU Queue ID mode (CH_CSR[DIQ] = 1 & DQID matching one of the BMU queues):

   ADDR[31:5] = Any value will do but zero preferred

   ADDR[4:0] = Any BMU Queue ID as specified in description of QID field

For B2H and H2H transfers the address must conform to the following format:

For destinations in flat memory space (CH_CSR[DIQ] = 0):   ADDR[31:0] = address mapping to destination interface

For UIF RX endpoints or EIF FIFOs (CH_CSR[DIQ] = 1 & DQID matching UIF or EIF):

   ADDR[31:5] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document)

   ADDR[4:0] = Queue ID matching UIF or EIF as specified in description of DQID field

DXE_0_CH3_DADRL

Bits	Name	Description
31:7	BASE	Base Address. Valid only when the CH_CSR[DIQ] bit is set. For this case, this bit field provides the base address of the destination UIF RX endpoint or EIF outbound FIFO (for BMU software may use any value can be used but zero is suggested). The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd Please consult the appropriate interface uarch for the offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH3_DADRL (cont.)

Bits	Name	Description
6:0	DQID	Destination Queue ID. Valid only when the CH_CSR[SIQ] bit is set. For this case, this bit field provides the ID for the destination BMU WQ, UIF RX endpoint or EIF outbound queue to be used for the transfer. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: RSVD_0 0x1: RSVD_1 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: BMU_25 0x1A: BMU_26 0x1B: BMU_SINK_WQ 0x1C: UIF_RX_1_EP 0x1D: UIF_RX_2_EP 0x1E: UIF_RX_3_EP 0x1F: UIF_RX_4_EP

0x30004D8 DXE_0_CH3_DADRH

Type: read-write

The channel destination address high register holds the high bits of the destination address for a transfer. Please see the description of CH_DADRL for more info.

DXE_0_CH3_DADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	This register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x30004DC DXE_0_CH3_DESCL

Type: read-write

The Channel 3 Linked List Descriptor Pointer register contains the 32 lower bits of the address of the next descriptor to be loaded in the linked list. This address must be dword (32-bit) aligned (addr[1:0]=0 if CH_CTRL[PIQ]=0). Each complete transfer descriptor consists of 7 32-bit values arranged contiguously in memory. The value of this register will be overwritten with the address of the start of the next descriptor set in the list after the current descriptor has been fetched. The meaning of the value in this register depends on the value of the CH_CTRL[PIQ] bit field similar to the way in which SADRL and DADRL are depending in SIQ and DIQ respectively. For CH_CTRL[PIQ]=0 then this register has no bit fields and the value is just intrepreted as an address in flat memory space. When CH_CTRL[PIQ] is set then the descriptor will be read from FIFO type memory in UIF and the register has 2 bit fields: BASE, and SQID. BASE specifies the base address of the UIF Tx queue (derived from the start of the UIF address space in SAHB plus the internal UIF offset).

DXE_0_CH3_DESCL

Bits	Name	Description
31:7	BASE	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify the base address of the UIF endpoint to use as the source of the descriptor. Please refer to the Nova address map document and to the UIF architecture document for guaranteed correct values to use here. For convenience but without a guarantee of accuracy, the base value to use for both the Tx data and management endpoints is the following: base = UIF base + TD_and_TM_offset = 0x0E02_5000 + x100 = 0x0E02_5100>>7 = 0x1C_04A2

DXE_0_CH3_DESCL (cont.)

Bits	Name	Description
6:0	SQID	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify which of the two UIF TX queues to use. Note that in this case software also needs to program the correct base address of the source UIF endpoint in the BASE bit field. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x30004E0 DXE_0_CH3_DESCH

Type: read-write

The channel destination address high register holds the high bits of the the address of the next descriptor to be loaded in the linked list.

DXE_0_CH3_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. Please note that if the source of the descriptor is either of the UIF endpoints (CH_CTRL[PIQ]=1) then the value in ADDRH has to be 0 or else the descriptor read could end up mapping to the XIF or PIF. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x30004E4 DXE_0_CH3_LST_DESCL

Type: read-only

The read-only Channel 3 Current/last Linked List Descriptor Pointer register contains the low 32-bits of the address of the descriptor currently being processed or of the last descriptor processed if the channel is disabled.

The meaning of the value and bit fields with regards to CH_CTRL[PIQ] is the same as was explained for the CH_DESCL register.

DXE_0_CH3_LST_DESCL

Bits	Name	Description
31:7	BASE	See description of CH_DESCL[BASE].
6:0	SQID	See description of CH_DESCL[SQID]. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x30004E8 DXE_0_CH3_LST_DESCH

Type: read-only

The channel destination address high register holds the high bits of the the address of the next descriptor to be loaded in the linked list. Note that The meaning of the value and bit fields is the same as was explained for the CH_DESCL register.

DXE_0_CH3_LST_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address.

0x30004EC DXE_0_CH3_BD

Type: read-only

DXE_0_CH3_BD

Bits	Name	Description
31:24	RSVD	Reserved. Always returns 0 when read.
23	VAL	Valid. BD has been loaded and is valid.
22:16	PDU_CNT	PDU count of packet.
15:0	IDX	Index of BD. To get actual physical address must be added to BD/PDU base.

0x30004F0 DXE_0_CH3_HEAD

Type: read-only
Reset State: 0x00000000

Address of head of packet.

DXE_0_CH3_HEAD

Bits	Name	Description
31:27	RSVD	Reserved. Reset State: 0x00000000
26	DESCVAL	Descriptor valid. Signifies descriptor has already been loaded. Used to prevent reloading of a descriptor. Reset State: 0x00000000
25:21	DWQID	Destination WQ ID. Original BMU, UIF or EIF destination queue. Valid only when CH_CSR[DIQ]=1 Reset State: 0x00000000
20:16	SWQID	Source WQ ID. Original BMU, UIF or EIF source queue. Valid only when CH_CSR[SIQ]=1 Reset State: 0x00000000
15:0	IDX	Index of Head. Must be added to BD/PDU base for actual physical address.

0x30004F4 DXE_0_CH3_TAIL

Type: read-only
Reset State: 0x00000000

Address of tail of packet.

DXE_0_CH3_TAIL

Bits	Name	Description
31:16	RSVD	Reserved. Reset State: 0x00000000
15:0	IDX	Index of Tail. Must be added to BD/PDU base for actual physical address

0x30004F8 DXE_0_CH3_PDU

Type: read-only
Reset State: 0x00000000

PDU info register.

All its fields are working fields that get modified as the programmed operation progresses.

DXE_0_CH3_PDU

Bits	Name	Description
31	RSVD	Reserved. Always returns 0 when read. Reset State: 0x00000000
30:24	PDU_CNT	Current PDU count.
23:8	IDX	Index of current PDU. Must be added to BD/PDU base for actual physical address
7:0	FST_OFF	First PDU offset.

0x30004FC DXE_0_CH3_TSTMP

Type: read-only
Reset State: 0x00000000

Contains last sampled value of the system timestamp

DXE_0_CH3_TSTMP

Bits	Name	Description
31:0	VALUE	Reset State: 0x00000000

0x3000500 DXE_0_CH4_CTRL

Type: read-write
Reset State: 0x11000708

Serves to configure channel 4 operation

DXE_0_CH4_CTRL

Bits	Name	Description
31	SWAP	Endian Byte Swap Enable. When high instructs DXE to perform an endian swap of the incoming byte stream. The corresponding bit field in the DXE descriptor control word is located at DXE_DESC_CTRL[20]

DXE_0_CH4_CTRL (cont.)

Bits	Name	Description
30:29	BDT_IDX	BD Template Index. When XTYPE=H2B and BDH=1, DXE supports creating a BD by using template data from one of up to 4 different BD templates. The BD template base store is pointed at by the DXE BD_TMPLT(H/L) registers and the address used to read the template data is calculated as follows: BD_TMPLT_ADRR = BD_TMPLT_BASE + (128 * CH_CTRL[BDT_IDX]) The corresponding bit field in the control word of the external descriptor is mapped to bits[19:18]
28	DFMT	Descriptor Format. This bit field is used to select between long and short descriptor formats. When using the short descriptor format, the high part of the source, destination and descriptor addresses will be taken from the SADRH_DFLT, DADRH_DFLT or DESCH_DFLT registers respectively. Default is to use the long descriptor format 0x0: SHORT 0x1: LONG Reset State: 0x00000001
27	ABORT	Writing a one to this bit will cause the channel to stop its current transfer and set the ERR bit and ERR_CODE fields in CH_STATUS. Note that if the channel is currently disabled or if it is about to be disabled because it has just finished its programmed transfer, then the abort request will be ignored and the error bit and error codes won't be set. If the channel is currently masked by the arbiter then setting this bit will forcibly unmask it so that the transfer can be aborted the next time the channel is selected by the internal arbiter. The abort request is automatically cleared by hardware once the channel has aborted the transfer. Also note that since the DXE will not attempt to do any cleanup when a transfer is aborted, software might need to do so. For example, for H2B transfers, software should manually release the BD and any PDUs currently in use by the partial transfer or else a BD/PDU leak will result. Reset State: 0x00000000
26	ENDIANNESS	Specifies the endianness of the master generating the data. Affects alignment of valid bytes for non-dword aligned reads/writes. The corresponding field in the DXE descriptor control word is located in DXE_DESC_CTRL[21] 0x0: BIGEND 0x1: LTLEND Reset State: 0x00000000
25:22	CTR_SEL	Counter Select. If the event counters are enabled (DMA_CSR[ECTR_EN]=1) then this bit field selects the counter that will be incremented at the end of the transfer. By default the value in this bit field is the same as the channel number so that after reset channel 0 increments counter 0, channel 1 increments counter 1 and so on. Reset State: 0x00000004

DXE_0_CH4_CTRL (cont.)

Bits	Name	Description
21	EDVEN	When set, the DMA engine will clear the VAL bit in the DESC_CSR word of the current descriptor once it has completed processing it. This is useful for implementing a descriptor "ring" (see the description of the VALID bit in Table 3.1) Reset State: 0x00000000
20	EDEN	External Descriptor Enable. Use External Descriptor Linked List Reset State: 0x00000000
19	INE_DONE	Enable Channel Interrupt when Channel is Done. The corresponding interrupt source bit is INT_DONE Reset State: 0x00000000
18	INE_ERR	Enable Channel Interrupt on Errors. The corresponding interrupt source bit is INT_ERR Reset State: 0x00000000
17	INE_ED	Enable External Descriptor Interrupt. When this bit is set, an interrupt will be generated after processing a descriptor item that has the INT bit set in its DESC_CTRL word (see Table 3.1). The corresponding interrupt source bit is INT_ED Reset State: 0x00000000
16	STOP	Channel processing stopped due to a request in the last processed linked list descriptor (see the STOP bit in the definition of the DESC_CSR word in Table 3.1). This bit will be automatically cleared when the channel is restarted. Reset State: 0x00000000
15:13	PRIO	This field sets the channel priority. 7: Highest Priority. 0: Lowest Priority.

DXE_0_CH4_CTRL (cont.)

Bits	Name	Description
12:9	BTHLD_SEL	BMU Threshold Select. This value tells DXE which of the BMU BD/PDU thresholds to check before issuing BMU commands that reserve, or get BDs or PDUs. It also specifies the module index value that will be used to issue any required BMU commands (see BMU spec for details). The value of this bit field is only meaningful for transfer types that involve the BMU and therefore its value will be ignored for H2H transfers. 0x0: RSVD0 0x1: RSVD1 0x2: THLD2 0x3: THLD3 0x4: THLD4 0x5: THLD5 0x6: THLD6 0x7: THLD7 0x8: THLD8 0x9: THLD9 0xA: THLD10 0xB: RSVD11 0xC: RSVD12 0xD: RSVD13 0xE: RSVD14 0xF: RSVD15 Reset State: 0x00000003
8	PDU_REL	0x0: Don't release BD and PDUs when done. 1: Release BD and PDUs when done. 0x0: KEEP 0x1: RELEASE Reset State: 0x00000001

DXE_0_CH4_CTRL (cont.)

Bits	Name	Description
7	PIQ	next descriptor Pointer address Is Queue. When set the source of the descriptor address is interepreted as a queue ID instead of just the address of a flat memory location. The only valid source queues for descriptors are the UIF Tx data and Tx management endpoints. Any other IDs will result the channel aborting the transfer with an invalid source queue error. Therefore, when this bit is set, software must ensure that the CH_DESCL[QID] bit field is set to a valid queue ID and that the CH_DESCL[BASE] bit field is set to the base address of the source UIF endpoint. This base address is formed by taking the base address for the UIF block in the SAHB bus which can be found in the Nova address map document and then adding the internal UIF offset for the correct source endpoint. This offsets can be obtained from the UIF specification document. For convenience, the current internal UIF offsets are provided in the descripiton of the QID bit field in the CH_DESCL register description. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
6	DIQ	Destination Is Queue. When set the destination address is interepreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF RX endpoints or and EIF outbound FIFO. When this bit is set, software must ensure that the DADR[QID] bit field is set to a valid queue ID and that the DADR[BASE] bit field is set to the base address of the destination queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
5	SIQ	Source Is Queue. When set the source address is interepreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF TX endpoints or and EIF inbound FIFO. When this bit is set, software must ensure that the SADR[QID] bit field is set to a valid queue ID and that the SADR[BASE] bit field is set to the base address of the source queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000

DXE_0_CH4_CTRL (cont.)

Bits	Name	Description
4	BDH	BD Handling bit. The behavior depends on the setting of XTYPE. If XTYPE is: H2B: Then if BDH is: 0: Use first 128 bytes of packet as BD. 1: Create BD from BD template (Up to 4 supported. Also see desc for BDT_IDX). B2H: Then if BDH is: 0: Insert BD in front of payload. 1: Discard BD. For XTYPE values of H2H and B2B the value of this bit is ignored. Reset State: 0x00000000
3	EOP	End of Packet bit. For H2B transfers marks the end of a packet Please note that when not using external descriptors DXE cannot support the gather functionality and therefore the EOP bit must be set. For XTYPE values of H2H, B2B and B2H the value of this bit is ignored. Reset State: 0x00000001
2:1	XTYPE	Transfer Type. Specifies the type of transfer to perform: 00: H2H. Host space to Host space transfer. 01: B2B. BMU space to BMU space transfer. 10: H2B. Host space to BMU translation. 11: B2H. BMU space to Host space translation. For cross-space transfers (H2B and B2H) the DMA engine will also perform the required data format translation. The format translation behavior can be modified by the setting of the BDH and PAD bits. 0x0: H2H 0x1: B2B 0x2: H2B 0x3: B2H
0	EN	Channel Enable or Restart. Writing this bit with a one either starts a new DMA transfer according to the parameters programmed in the channel's configuration registers and clears the DONE bit or, if the channel is already enabled but the STOP bit is set, then it restarts channel processing and also clears the STOP bit. This bit is automatically cleared when a single transfer completes or, if the channel is configured to use linked list descriptors, when the last transfer in the descriptor linked list completes (DESC_NXT is NULL or/and DESC_CSR[VALID]=0). The channel is also disabled and this bit cleared if a channel error is encountered. Reading this bit indicates whether a channel is currently enabled or disabled:. 0: Channel Disabled. 1: Channel Enabled. The Channel Enable bit status can also be found by reading the DMA_ENCH register which aggregates the EN bits of all channels. Note: Software must take care to not disable the channel while it is busy or data could be lost. Reset State: 0x00000000

0x3000504 DXE_0_CH4_STATUS

Type: read-write
Reset State: 0x00000000

Serves to report the status of the programmed channel operation.

DXE_0_CH4_STATUS

Bits	Name	Description
31:16	RSVD	Reserved. Reads always return 0. Writes are ignored.
15	INT_DONE	Interrupt Source: Asserted when the channel has finished all processing.
14	INT_ERR	Interrupt Source: Asserted when a channel error has occurred. Masked by the INE_ERR
13	INT_ED	Interrupt Source. Descriptor Done and INT requested
12	ABORT_REQ	Abort Request. Software has requested that the current operation be aborted. However, if CH_STATUS[EN] is still set then the channel has registered the request but is not yet in a position to abort the transfer "safely". Once the channel finishes its current operation it will abort the transfer and set the error flag and error code bit fields accordingly.
11	STOP_REQ	Stop Request. Software has requested that the channel stop it operation after the current descriptor has been processed. Once this happens the STOPD bit field will be set to one and the channel will be disabled.

DXE_0_CH4_STATUS (cont.)

Bits	Name	Description
10:6	ERR_CODE	Used to identify the source or cause of an error. 0x0: NONE 0x1: SAHB_ERR 0x2: H2H_RD_BUS_ERR 0x3: H2H_WR_BUS_ERR 0x4: PRG_INV_XTYPE 0x5: BERR_POPWQ 0x6: BERR_PUSHWQ 0x7: BERR_RLSS 0x8: BERR_GETPDU 0x9: PRG_INV_WQ 0xA: PRG_INV_H2H_SRC_QID 0xB: PRG_INV_H2H_DST_QID 0xC: PRG_INV_B2H_SRC_QID 0xD: PRG_INV_B2H_DST_QID 0xE: PRG_INV_B2H_SRC_IDX 0xF: PRG_INV_H2B_SRC_QID 0x10: PRG_INV_H2B_DST_QID 0x11: PRG_INV_H2B_DST_IDX 0x12: PRG_INV_H2B_SZ 0x13: PRG_INV_SADR 0x14: PRG_INV_DADR 0x15: PRG_INV_EDADR 0x16: PRG_INV_SRC_WQID 0x17: PRG_INV_DST_WQID 0x18: PRG_XTYPE_MSMTCH 0x19: PKT_ERR 0x1A: ABORT 0x1B: PDU_CNT_OVFL Reset State: 0x00000000
5	ERR	DMA channel stopped due to error. To clear the error status it is necessary to write a 1 into this bit position.
4	STOPD	Channel Stopped. The channel has stopped further processing and disabled itself due to a stop request in the last processed descriptor. Reset State: 0x00000000
3	MSKD	Channel Masked. The channel has been automatically masked out from arbitration due to a blocking condition. Reset State: 0x00000000
2	DONE	DMA channel Done. This bit will be automatically cleared the next time the channel is enabled. Reset State: 0x00000000
1	BUSY	Channel busy. HIgh when the channel is enabled and currently active (won internal arbitration) Reset State: 0x00000000

DXE_0_CH4_STATUS (cont.)

Bits	Name	Description
0	EN	Channel Enabled. Copy of CH_CTRL[EN]. Reset State: 0x00000000

0x3000508 DXE_0_CH4_SZ

Type: read-write

The transfer size register specifies the total, remaining, and burst or 'chunk' transfer sizes for each channel. The maximum total transfer size is 16K-1 bytes. The chunk size control can be useful to control the relative bandwidth used by each channel as the dma engine will change channels, release the AHB bus, and rearbitrate for access after transferring chunk size bytes.

DXE_0_CH4_SZ

Bits	Name	Description
31:28	CHK_SZ	Chunk transfer size. Specifies the number of bytes (in multiples of 8) to be transferred at one given time (not implying they are buffered but that they will be transferred for each start event in one bus request cycle). If chunk size is zero the DMA engine will always perform maximum chunk size transfers. Maximum chunk size is 128 bytes.
27:14	REM_SZ	Remaining transfer size. Specifies the number of bytes that remain to be transferred to complete the current operation.
13:0	TOT_SZ	Total Transfer Size. Specifies the number of bytes to be transferred. Maximum total transfer size is (4K-1) bytes. Note: This field is unnecessary and will be ignored for B2H or B2B transfers, when the source of the transfer is in BMU space (either BMU queue or direct pointer to BD). This is because the size of the transfer will be the packet length encoded in the BD at offset 0x0c bits [11:0].

0x300050C DXE_0_CH4_SADRL

Type: read-write

The channel source address register specifies either the source address in flat internal or external memory, or else the BMU queue ID, UIF TX endpoint ID, or EIF inbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the source, addresses can have arbitrary byte-alignment When using a BMU queue, UIF endpoint or EIF fifo as a source, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[SIQ] bit. When CH_CSR[SIQ] is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when it is set this register has two bit fields: The SQID bit field

used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF source endpoint/FIFO.

For B2H or B2B transfers, when the source is a BMU Queue ID (CH_CSR[SIQ] = 1 and SWQID matches BMU), the DXE will issue a BMU POPWQ command to pop the specified queue and obtain the BD index of the source packet. Else, when the source is an address (CH_CSR[SIQ] = 0), the DXE will interpret the address as the index of the packet BD and will add it to the BMU_BASE to obtain the physical addresss to use to fetch it directly from memory.

For H2B or H2H transfers, if the source is a UIF endpoint or EIF FIFO (CH_CSR[SIQ] = 1 and SQID matches UIF/EIF), software should program the SAHB base address of the UIF source endpoint in the BASE bit field and the queue ID to match in the SWQID bit field, then the DXE will use the base address given to generate the physical address and read the data over the SAHB bus and also use the appropriate sideband signals as specified by the SQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and SQID fields are consistend and refer to the same endpoint or else hangs or unpredictable behavior might occur. Else, when the source is just a location in flat memory space, (CH_CSR[SIQ] = 0), the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the physical address to use to fetch the data. For this case, software should make sure that the provided address maps to the intended source interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus.

To summarize, for B2H and B2B transfers the address must conform to the following format:

For index of BD mode (CH_CSR[SIQ] = 0):

   ADDR[31:7] = BMU_BASE + BD_INDEX[15:0]

   ADDR[6:0] = 7'd0

For BMU Queue ID mode (CH_CSR[SIQ] = 1 & SQID matching one of the BMU queues):

   ADDR[31:7] = Any value will do but zero preferred

   ADDR[6:0] = Any BMU Queue ID as specified in description of SQID field

For H2B and H2H transfers the address must conform to the following format:

For sources in flat memory space (CH_CSR[SIQ] = 0):   ADDR[31:0] = address mapping to source interface

For UIF RX endpoints or EIF FIFOs (CH_CSR[SIQ] = 1 & QID matching UIF or EIF):

   ADDR[31:7] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document)

   ADDR[6:0] = Queue ID matching UIF or EIF as specified in description of SQID field

DXE_0_CH4_SADRL

Bits	Name	Description
31:7	BASE	Base Address. For this case, this bit field provides the base address of the source UIF TX endpoint or EIF inbound FIFO. The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd Please consult the appropriate interface uarch for the offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH4_SADRL (cont.)

Bits	Name	Description
6:0	SQID	Source Queue ID. Valid only when the CH_CSR[SIQ] bit is set. For this case, this bit field provides the ID for the source BMU, UIF or EIF queue to be used for the transfer. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: RSVD_25 0x1A: RSVD_26 0x1B: RSVD_27 0x1C: RSVD_28 0x1D: RSVD_29 0x1E: RSVD_30 0x1F: RSVD_31

0x3000510 DXE_0_CH4_SADRH

Type: read-write

The channel source address high register holds the high bits of the source address for a transfer. Please see the description of CH_SADRL for more info.

DXE_0_CH4_SADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_SADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x3000514 DXE_0_CH4_DADRL

Type: read-write

The channel destination address register specifies either the destination address in flat internal or external memory, or else the BMU queue ID, UIF RX endpoint ID, or EIF outbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the destination, addresses can have arbitrary byte-alignment. When using a BMU queue, UIF endpoint or EIF fifo as a destination, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[DIQ] bit. When this bit is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when the bit is set this register has two bit fields: The DQID bit field used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF destination endpoint/FIFO.

For H2B or B2B transfers, when using a BMU queue as the destination (CH_CSR[DIQ] = 1 and DQID matches BMU), the DXE will push the index of the BD of the packet into the specified queue at the end of the packet transfer. Therefore, software is responsible for programming a valid BMU Queue ID.

Else, when the destination is an index (CH_CSR[DIQ] = 0), the BD will be written to the address obtained by adding the provided index to the BMU_BASE, again, the software must ensure that said address is legal and known to BMU. That is, software must preallocate the BD (get the BD from BMU via GET BD/PDU cmd) for the BD before starting the transfer. For B2H or H2H transfers, if the destination is a UIF endpoint or EIF FIFO (CH_CSR[DIQ] = 1 and DQID matches UIF/EIF), software should program the SAHB base address of the UIF destination endpoint in the BASE bit field and the queue ID to match in the DQID bit field, then the DXE will use the base address given to generate the physical address and write the data over the SAHB bus and also use the appropriate sideband signals as specified by the DQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and DQID fields are consistent and refer

to the same endpoint else hangs or unpredictable behavior might occur. On the other hand, when the destination is just a location in flat memory space, (CH_CSR[DIQ] = 0), be it internal or external, the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the address to write the data. For this case, software should make sure that the address maps to the intended destination interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus. To summarize, for H2B and B2B transfers the address must conform to the following format:

For index of BD mode (CH_CSR[DIQ] = 0):   ADDR[31:7] = BMU_BASE + BD_INDEX[15:0]

   ADDR[6:0] = 7'd0

For BMU Queue ID mode (CH_CSR[DIQ] = 1 & DQID matching one of the BMU queues):

   ADDR[31:5] = Any value will do but zero preferred

   ADDR[4:0] = Any BMU Queue ID as specified in description of QID field

For B2H and H2H transfers the address must conform to the following format:

For destinations in flat memory space (CH_CSR[DIQ] = 0):   ADDR[31:0] = address mapping to destination interface

For UIF RX endpoints or EIF FIFOs (CH_CSR[DIQ] = 1 & DQID matching UIF or EIF):

   ADDR[31:5] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document)

   ADDR[4:0] = Queue ID matching UIF or EIF as specified in description of DQID field

DXE_0_CH4_DADRL

Bits	Name	Description
31:7	BASE	Base Address. Valid only when the CH_CSR[DIQ] bit is set. For this case, this bit field provides the base address of the destination UIF RX endpoint or EIF outbound FIFO (for BMU software may use any value can be used but zero is suggested). The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd Please consult the appropriate interface uarch for the offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH4_DADRL (cont.)

Bits	Name	Description
6:0	DQID	Destination Queue ID. Valid only when the CH_CSR[SIQ] bit is set. For this case, this bit field provides the ID for the destination BMU WQ, UIF RX endpoint or EIF outbound queue to be used for the transfer. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: RSVD_0 0x1: RSVD_1 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: BMU_25 0x1A: BMU_26 0x1B: BMU_SINK_WQ 0x1C: UIF_RX_1_EP 0x1D: UIF_RX_2_EP 0x1E: UIF_RX_3_EP 0x1F: UIF_RX_4_EP

0x3000518 DXE_0_CH4_DADRH

Type: read-write

The channel destination address high register holds the high bits of the destination address for a transfer. Please see the description of CH_DADRL for more info.

DXE_0_CH4_DADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	This register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x300051C DXE_0_CH4_DESCL

Type: read-write

The Channel 4 Linked List Descriptor Pointer register contains the 32 lower bits of the address of the next descriptor to be loaded in the linked list. This address must be dword (32-bit) aligned (addr[1:0]=0 if CH_CTRL[PIQ]=0). Each complete transfer descriptor consists of 7 32-bit values arranged contiguously in memory. The value of this register will be overwritten with the address of the start of the next descriptor set in the list after the current descriptor has been fetched. The meaning of the value in this register depends on the value of the CH_CTRL[PIQ] bit field similar to the way in which SADRL and DADRL are depending in SIQ and DIQ respectively. For CH_CTRL[PIQ]=0 then this register has no bit fields and the value is just intrepreted as an address in flat memory space. When CH_CTRL[PIQ] is set then the descriptor will be read from FIFO type memory in UIF and the register has 2 bit fields: BASE, and SQID. BASE specifies the base address of the UIF Tx queue (derived from the start of the UIF address space in SAHB plus the internal UIF offset).

DXE_0_CH4_DESCL

Bits	Name	Description
31:7	BASE	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify the base address of the UIF endpoint to use as the source of the descriptor. Please refer to the Nova address map document and to the UIF architecture document for guaranteed correct values to use here. For convenience but without a guarantee of accuracy, the base value to use for both the Tx data and management endpoints is the following: base = UIF base + TD_and_TM_offset = 0x0E02_5000 + x100 = 0x0E02_5100>>7 = 0x1C_04A2

DXE_0_CH4_DESCL (cont.)

Bits	Name	Description
6:0	SQID	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify which of the two UIF TX queues to use. Note that in this case software also needs to program the correct base address of the source UIF endpoint in the BASE bit field. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x3000520 DXE_0_CH4_DESCH

Type: read-write

The channel destination address high register holds the high bits of the the address of the next descriptor to be loaded in the linked list.

DXE_0_CH4_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. Please note that if the source of the descriptor is either of the UIF endpoints (CH_CTRL[PIQ]=1) then the value in ADDRH has to be 0 or else the descriptor read could end up mapping to the XIF or PIF. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x3000524 DXE_0_CH4_LST_DESCL

Type: read-only

The read-only Channel 4 Current/last Linked List Descriptor Pointer register contains the low 32-bits of the address of the descriptor currently being processed or of the last descriptor processed if the channel is disabled.

The meaning of the value and bit fields with regards to CH_CTRL[PIQ] is the same as was explained for the CH_DESCL register.

DXE_0_CH4_LST_DESCL

Bits	Name	Description
31:7	BASE	See description of CH_DESCL[BASE].
6:0	SQID	See description of CH_DESCL[SQID]. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x3000528 DXE_0_CH4_LST_DESCH

Type: read-only

The channel destination address high register holds the high bits of the the address of the next descriptor to be loaded in the linked list. Note that The meaning of the value and bit fields is the same as was explained for the CH_DESCL register.

DXE_0_CH4_LST_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address.

0x300052C DXE_0_CH4_BD

Type: read-only

DXE_0_CH4_BD

Bits	Name	Description
31:24	RSVD	Reserved. Always returns 0 when read.
23	VAL	Valid. BD has been loaded and is valid.
22:16	PDU_CNT	PDU count of packet.
15:0	IDX	Index of BD. To get actual physical address must be added to BD/PDU base.

0x3000530 DXE_0_CH4_HEAD

Type: read-only
Reset State: 0x00000000

Address of head of packet.

DXE_0_CH4_HEAD

Bits	Name	Description
31:27	RSVD	Reserved. Reset State: 0x00000000
26	DESCVAL	Descriptor valid. Signifies descriptor has already been loaded. Used to prevent reloading of a descriptor. Reset State: 0x00000000
25:21	DWQID	Destination WQ ID. Original BMU, UIF or EIF destination queue. Valid only when CH_CSR[DIQ]=1 Reset State: 0x00000000
20:16	SWQID	Source WQ ID. Original BMU, UIF or EIF source queue. Valid only when CH_CSR[SIQ]=1 Reset State: 0x00000000
15:0	IDX	Index of Head. Must be added to BD/PDU base for actual physical address.

0x3000534 DXE_0_CH4_TAIL

Type: read-only
Reset State: 0x00000000

Address of tail of packet.

DXE_0_CH4_TAIL

Bits	Name	Description
31:16	RSVD	Reserved. Reset State: 0x00000000
15:0	IDX	Index of Tail. Must be added to BD/PDU base for actual physical address

0x3000538 DXE_0_CH4_PDU

Type: read-only
Reset State: 0x00000000

PDU info register.

All its fields are working fields that get modified as the programmed operation progresses.

DXE_0_CH4_PDU

Bits	Name	Description
31	RSVD	Reserved. Always returns 0 when read. Reset State: 0x00000000
30:24	PDU_CNT	Current PDU count.
23:8	IDX	Index of current PDU. Must be added to BD/PDU base for actual physical address
7:0	FST_OFF	First PDU offset.

0x300053C DXE_0_CH4_TSTMP

Type: read-only
Reset State: 0x00000000

Contains last sampled value of the system timestamp

DXE_0_CH4_TSTMP

Bits	Name	Description
31:0	VALUE	Reset State: 0x00000000

0x3000540 DXE_0_CH5_CTRL

Type: read-write
Reset State: 0x11400708

Serves to configure channel 5 operation

DXE_0_CH5_CTRL

Bits	Name	Description
31	SWAP	Endian Byte Swap Enable. When high instructs DXE to perform an endian swap of the incoming byte stream. The corresponding bit field in the DXE descriptor control word is located at DXE_DESC_CTRL[20]

DXE_0_CH5_CTRL (cont.)

Bits	Name	Description
30:29	BDT_IDX	BD Template Index. When XTYPE=H2B and BDH=1, DXE supports creating a BD by using template data from one of up to 4 different BD templates. The BD template base store is pointed at by the DXE BD_TMPLT(H/L) registers and the address used to read the template data is calculated as follows: BD_TMPLT_ADRR = BD_TMPLT_BASE + (128 * CH_CTRL[BDT_IDX]) The corresponding bit field in the control word of the external descriptor is mapped to bits[19:18]
28	DFMT	Descriptor Format. This bit field is used to select between long and short descriptor formats. When using the short descriptor format, the high part of the source, destination and descriptor addresses will be taken from the SADRH_DFLT, DADRH_DFLT or DESCH_DFLT registers respectively. Default is to use the long descriptor format 0x0: SHORT 0x1: LONG Reset State: 0x00000001
27	ABORT	Writing a one to this bit will cause the channel to stop its current transfer and set the ERR bit and ERR_CODE fields in CH_STATUS. Note that if the channel is currently disabled or if it is about to be disabled because it has just finished its programmed transfer, then the abort request will be ignored and the error bit and error codes won't be set. If the channel is currently masked by the arbiter then setting this bit will forcibly unmask it so that the transfer can be aborted the next time the channel is selected by the internal arbiter. The abort request is automatically cleared by hardware once the channel has aborted the transfer. Also note that since the DXE will not attempt to do any cleanup when a transfer is aborted, software might need to do so. For example, for H2B transfers, software should manually release the BD and any PDUs currently in use by the partial transfer or else a BD/PDU leak will result. Reset State: 0x00000000
26	ENDIANNESS	Specifies the endianness of the master generating the data. Affects alignment of valid bytes for non-dword aligned reads/writes. The corresponding field in the DXE descriptor control word is located in DXE_DESC_CTRL[21] 0x0: BIGEND 0x1: LTLEND Reset State: 0x00000000
25:22	CTR_SEL	Counter Select. If the event counters are enabled (DMA_CSR[ECTR_EN]=1) then this bit field selects the counter that will be incremented at the end of the transfer. By default the value in this bit field is the same as the channel number so that after reset channel 0 increments counter 0, channel 1 increments counter 1 and so on. Reset State: 0x00000005

DXE_0_CH5_CTRL (cont.)

Bits	Name	Description
21	EDVEN	When set, the DMA engine will clear the VAL bit in the DESC_CSR word of the current descriptor once it has completed processing it. This is useful for implementing a descriptor "ring" (see the description of the VALID bit in Table 3.1) Reset State: 0x00000000
20	EDEN	External Descriptor Enable. Use External Descriptor Linked List Reset State: 0x00000000
19	INE_DONE	Enable Channel Interrupt when Channel is Done. The corresponding interrupt source bit is INT_DONE Reset State: 0x00000000
18	INE_ERR	Enable Channel Interrupt on Errors. The corresponding interrupt source bit is INT_ERR Reset State: 0x00000000
17	INE_ED	Enable External Descriptor Interrupt. When this bit is set, an interrupt will be generated after processing a descriptor item that has the INT bit set in its DESC_CTRL word (see Table 3.1). The corresponding interrupt source bit is INT_ED Reset State: 0x00000000
16	STOP	Channel processing stopped due to a request in the last processed linked list descriptor (see the STOP bit in the definition of the DESC_CSR word in Table 3.1). This bit will be automatically cleared when the channel is restarted. Reset State: 0x00000000
15:13	PRIO	This field sets the channel priority. 7: Highest Priority. 0: Lowest Priority.

DXE_0_CH5_CTRL (cont.)

Bits	Name	Description
12:9	BTHLD_SEL	BMU Threshold Select. This value tells DXE which of the BMU BD/PDU thresholds to check before issuing BMU commands that reserve, or get BDs or PDUs. It also specifies the module index value that will be used to issue any required BMU commands (see BMU spec for details). The value of this bit field is only meaningful for transfer types that involve the BMU and therefore its value will be ignored for H2H transfers. 0x0: RSVD0 0x1: RSVD1 0x2: THLD2 0x3: THLD3 0x4: THLD4 0x5: THLD5 0x6: THLD6 0x7: THLD7 0x8: THLD8 0x9: THLD9 0xA: THLD10 0xB: RSVD11 0xC: RSVD12 0xD: RSVD13 0xE: RSVD14 0xF: RSVD15 Reset State: 0x00000003
8	PDU_REL	0x0: Don't release BD and PDUs when done. 1: Release BD and PDUs when done. 0x0: KEEP 0x1: RELEASE Reset State: 0x00000001

DXE_0_CH5_CTRL (cont.)

Bits	Name	Description
7	PIQ	next descriptor Pointer address Is Queue. When set the source of the descriptor address is interepreted as a queue ID instead of just the address of a flat memory location. The only valid source queues for descriptors are the UIF Tx data and Tx management endpoints. Any other IDs will result the channel aborting the transfer with an invalid source queue error. Therefore, when this bit is set, software must ensure that the CH_DESCL[QID] bit field is set to a valid queue ID and that the CH_DESCL[BASE] bit field is set to the base address of the source UIF endpoint. This base address is formed by taking the base address for the UIF block in the SAHB bus which can be found in the Nova address map document and then adding the internal UIF offset for the correct source endpoint. This offsets can be obtained from the UIF specification document. For convenience, the current internal UIF offsets are provided in the descripiton of the QID bit field in the CH_DESCL register description. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
6	DIQ	Destination Is Queue. When set the destination address is interepreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF RX endpoints or and EIF outbound FIFO. When this bit is set, software must ensure that the DADR[QID] bit field is set to a valid queue ID and that the DADR[BASE] bit field is set to the base address of the destination queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
5	SIQ	Source Is Queue. When set the source address is interepreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF TX endpoints or and EIF inbound FIFO. When this bit is set, software must ensure that the SADR[QID] bit field is set to a valid queue ID and that the SADR[BASE] bit field is set to the base address of the source queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000

DXE_0_CH5_CTRL (cont.)

Bits	Name	Description
4	BDH	BD Handling bit. The behavior depends on the setting of XTYPE. If XTYPE is: H2B: Then if BDH is: 0: Use first 128 bytes of packet as BD. 1: Create BD from BD template (Up to 4 supported. Also see desc for BDT_IDX). B2H: Then if BDH is: 0: Insert BD in front of payload. 1: Discard BD. For XTYPE values of H2H and B2B the value of this bit is ignored. Reset State: 0x00000000
3	EOP	End of Packet bit. For H2B transfers marks the end of a packet Please note that when not using external descriptors DXE cannot support the gather functionality and therefore the EOP bit must be set. For XTYPE values of H2H, B2B and B2H the value of this bit is ignored. Reset State: 0x00000001
2:1	XTYPE	Transfer Type. Specifies the type of transfer to perform: 00: H2H. Host space to Host space transfer. 01: B2B. BMU space to BMU space transfer. 10: H2B. Host space to BMU translation. 11: B2H. BMU space to Host space translation. For cross-space transfers (H2B and B2H) the DMA engine will also perform the required data format translation. The format translation behavior can be modified by the setting of the BDH and PAD bits. 0x0: H2H 0x1: B2B 0x2: H2B 0x3: B2H
0	EN	Channel Enable or Restart. Writing this bit with a one either starts a new DMA transfer according to the parameters programmed in the channel's configuration registers and clears the DONE bit or, if the channel is already enabled but the STOP bit is set, then it restarts channel processing and also clears the STOP bit. This bit is automatically cleared when a single transfer completes or, if the channel is configured to use linked list descriptors, when the last transfer in the descriptor linked list completes (DESC_NXT is NULL or/and DESC_CSR[VALID]=0). The channel is also disabled and this bit cleared if a channel error is encountered. Reading this bit indicates whether a channel is currently enabled or disabled:. 0: Channel Disabled. 1: Channel Enabled. The Channel Enable bit status can also be found by reading the DMA_ENCH register which aggregates the EN bits of all channels. Note: Software must take care to not disable the channel while it is busy or data could be lost. Reset State: 0x00000000

0x3000544 DXE_0_CH5_STATUS

Type: read-write
Reset State: 0x00000000

Serves to report the status of the programmed channel operation.

DXE_0_CH5_STATUS

Bits	Name	Description
31:16	RSVD	Reserved. Reads always return 0. Writes are ignored.
15	INT_DONE	Interrupt Source: Asserted when the channel has finished all processing.
14	INT_ERR	Interrupt Source: Asserted when a channel error has occurred. Masked by the INE_ERR
13	INT_ED	Interrupt Source. Descriptor Done and INT requested
12	ABORT_REQ	Abort Request. Software has requested that the current operation be aborted. However, if CH_STATUS[EN] is still set then the channel has registered the request but is not yet in a position to abort the transfer "safely". Once the channel finishes its current operation it will abort the transfer and set the error flag and error code bit fields accordingly.
11	STOP_REQ	Stop Request. Software has requested that the channel stop it operation after the current descriptor has been processed. Once this happens the STOPD bit field will be set to one and the channel will be disabled.

DXE_0_CH5_STATUS (cont.)

Bits	Name	Description
10:6	ERR_CODE	Used to identify the source or cause of an error. 0x0: NONE 0x1: SAHB_ERR 0x2: H2H_RD_BUS_ERR 0x3: H2H_WR_BUS_ERR 0x4: PRG_INV_XTYPE 0x5: BERR_POPWQ 0x6: BERR_PUSHWQ 0x7: BERR_RLSS 0x8: BERR_GETPDU 0x9: PRG_INV_WQ 0xA: PRG_INV_H2H_SRC_QID 0xB: PRG_INV_H2H_DST_QID 0xC: PRG_INV_B2H_SRC_QID 0xD: PRG_INV_B2H_DST_QID 0xE: PRG_INV_B2H_SRC_IDX 0xF: PRG_INV_H2B_SRC_QID 0x10: PRG_INV_H2B_DST_QID 0x11: PRG_INV_H2B_DST_IDX 0x12: PRG_INV_H2B_SZ 0x13: PRG_INV_SADR 0x14: PRG_INV_DADR 0x15: PRG_INV_EDADR 0x16: PRG_INV_SRC_WQID 0x17: PRG_INV_DST_WQID 0x18: PRG_XTYPE_MSMTCH 0x19: PKT_ERR 0x1A: ABORT 0x1B: PDU_CNT_OVFL Reset State: 0x00000000
5	ERR	DMA channel stopped due to error. To clear the error status it is necessary to write a 1 into this bit position.
4	STOPD	Channel Stopped. The channel has stopped further processing and disabled itself due to a stop request in the last processed descriptor. Reset State: 0x00000000
3	MSKD	Channel Masked. The channel has been automatically masked out from arbitration due to a blocking condition. Reset State: 0x00000000
2	DONE	DMA channel Done. This bit will be automatically cleared the next time the channel is enabled. Reset State: 0x00000000
1	BUSY	Channel busy. HIgh when the channel is enabled and currently active (won internal arbitration) Reset State: 0x00000000

DXE_0_CH5_STATUS (cont.)

Bits	Name	Description
0	EN	Channel Enabled. Copy of CH_CTRL[EN]. Reset State: 0x00000000

0x3000548 DXE_0_CH5_SZ

Type: read-write

The transfer size register specifies the total, remaining, and burst or 'chunk' transfer sizes for each channel. The maximum total transfer size is 16K-1 bytes. The chunk size control can be useful to control the relative bandwidth used by each channel as the dma engine will change channels, release the AHB bus, and rearbitrate for access after transferring chunk size bytes.

DXE_0_CH5_SZ

Bits	Name	Description
31:28	CHK_SZ	Chunk transfer size. Specifies the number of bytes (in multiples of 8) to be transferred at one given time (not implying they are buffered but that they will be transferred for each start event in one bus request cycle). If chunk size is zero the DMA engine will always perform maximum chunk size transfers. Maximum chunk size is 128 bytes.
27:14	REM_SZ	Remaining transfer size. Specifies the number of bytes that remain to be transferred to complete the current operation.
13:0	TOT_SZ	Total Transfer Size. Specifies the number of bytes to be transferred. Maximum total transfer size is (4K-1) bytes. Note: This field is unnecessary and will be ignored for B2H or B2B transfers, when the source of the transfer is in BMU space (either BMU queue or direct pointer to BD). This is because the size of the transfer will be the packet length encoded in the BD at offset 0x0c bits [11:0].

0x300054C DXE_0_CH5_SADRL

Type: read-write

The channel source address register specifies either the source address in flat internal or external memory, or else the BMU queue ID, UIF TX endpoint ID, or EIF inbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the source, addresses can have arbitrary byte-alignment When using a BMU queue, UIF endpoint or EIF fifo as a source, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[SIQ] bit. When CH_CSR[SIQ] is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when it is set this register has two bit fields: The SQID bit field

used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF source endpoint/FIFO.

For B2H or B2B transfers, when the source is a BMU Queue ID (CH_CSR[SIQ] = 1 and SWQID matches BMU), the DXE will issue a BMU POPWQ command to pop the specified queue and obtain the BD index of the source packet. Else, when the source is an address (CH_CSR[SIQ] = 0), the DXE will interpret the address as the index of the packet BD and will add it to the BMU_BASE to obtain the physical addresss to use to fetch it directly from memory.

For H2B or H2H transfers, if the source is a UIF endpoint or EIF FIFO (CH_CSR[SIQ] = 1 and SQID matches UIF/EIF), software should program the SAHB base address of the UIF source endpoint in the BASE bit field and the queue ID to match in the SWQID bit field, then the DXE will use the base address given to generate the physical address and read the data over the SAHB bus and also use the appropriate sideband signals as specified by the SQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and SQID fields are consistend and refer to the same endpoint or else hangs or unpredictable behavior might occur. Else, when the source is just a location in flat memory space, (CH_CSR[SIQ] = 0), the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the physical address to use to fetch the data. For this case, software should make sure that the provided address maps to the intended source interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus.

To summarize, for B2H and B2B transfers the address must conform to the following format:

For index of BD mode (CH_CSR[SIQ] = 0):

   ADDR[31:7] = BMU_BASE + BD_INDEX[15:0]

   ADDR[6:0] = 7'd0

For BMU Queue ID mode (CH_CSR[SIQ] = 1 & SQID matching one of the BMU queues):

   ADDR[31:7] = Any value will do but zero preferred

   ADDR[6:0] = Any BMU Queue ID as specified in description of SQID field

For H2B and H2H transfers the address must conform to the following format:

For sources in flat memory space (CH_CSR[SIQ] = 0):   ADDR[31:0] = address mapping to source interface

For UIF RX endpoints or EIF FIFOs (CH_CSR[SIQ] = 1 & QID matching UIF or EIF):

   ADDR[31:7] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document)

   ADDR[6:0] = Queue ID matching UIF or EIF as specified in description of SQID field

DXE_0_CH5_SADRL

Bits	Name	Description
31:7	BASE	Base Address. For this case, this bit field provides the base address of the source UIF TX endpoint or EIF inbound FIFO. The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd Please consult the appropriate interface uarch for the offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH5_SADRL (cont.)

Bits	Name	Description
6:0	SQID	Source Queue ID. set. For this case, this bit field provides the ID for the source BMU, UIF or EIF queue to be used for the transfer. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: RSVD_25 0x1A: RSVD_26 0x1B: RSVD_27 0x1C: RSVD_28 0x1D: RSVD_29 0x1E: RSVD_30 0x1F: RSVD_31

0x3000550 DXE_0_CH5_SADRH

Type: read-write

The channel source address high register holds the high bits of the source address for a transfer. Please see the description of CH_SADRL for more info.

DXE_0_CH5_SADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_SADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x3000554 DXE_0_CH5_DADRL

Type: read-write

The channel destination address register specifies either the destination address in flat internal or external memory, or else the BMU queue ID, UIF RX endpoint ID, or EIF outbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the destination, addresses can have arbitrary byte-alignment. When using a BMU queue, UIF endpoint or EIF fifo as a destination, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[DIQ] bit. When this bit is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when the bit is set this register has two bit fields: The DQID bit field used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF destination endpoint/FIFO.

For H2B or B2B transfers, when using a BMU queue as the destination (CH_CSR[DIQ] = 1 and DQID matches BMU), the DXE will push the index of the BD of the packet into the specified queue at the end of the packet transfer. Therefore, software is responsible for programming a valid BMU Queue ID.

Else, when the destination is an index (CH_CSR[DIQ] = 0), the BD will be written to the address obtained by adding the provided index to the BMU_BASE, again, the software must ensure that said address is legal and known to BMU. That is, software must preallocate the BD (get the BD from BMU via GET BD/PDU cmd) for the BD before starting the transfer. For B2H or H2H transfers, if the destination is a UIF endpoint or EIF FIFO (CH_CSR[DIQ] = 1 and DQID matches UIF/EIF), software should program the SAHB base address of the UIF destination endpoint in the BASE bit field and the queue ID to match in the DQID bit field, then the DXE will use the base address given to generate the physical address and write the data over the SAHB bus and also use the appropriate sideband signals as specified by the DQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and DQID fields are consistent and refer

to the same endpoint else hangs or unpredictable behavior might occur. On the other hand, when the destination is just a location in flat memory space, (CH_CSR[DIQ] = 0), be it internal or external, the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the address to write the data. For this case, software should make sure that the address maps to the intended destination interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus. To summarize, for H2B and B2B transfers the address must conform to the following format:

For index of BD mode (CH_CSR[DIQ] = 0):   ADDR[31:7] = BMU_BASE + BD_INDEX[15:0]

   ADDR[6:0] = 7'd0

For BMU Queue ID mode (CH_CSR[DIQ] = 1 & DQID matching one of the BMU queues):

   ADDR[31:5] = Any value will do but zero preferred

   ADDR[4:0] = Any BMU Queue ID as specified in description of QID field

For B2H and H2H transfers the address must conform to the following format:

For destinations in flat memory space (CH_CSR[DIQ] = 0):   ADDR[31:0] = address mapping to destination interface

For UIF RX endpoints or EIF FIFOs (CH_CSR[DIQ] = 1 & DQID matching UIF or EIF):

   ADDR[31:5] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document)

   ADDR[4:0] = Queue ID matching UIF or EIF as specified in description of DQID field

DXE_0_CH5_DADRL

Bits	Name	Description
31:7	BASE	Base Address. Valid only when the CH_CSR[DIQ] bit is set. For this case, this bit field provides the base address of the destination UIF RX endpoint or EIF outbound FIFO (for BMU software may use any value can be used but zero is suggested). The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd Please consult the appropriate interface uarch for the offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH5_DADRL (cont.)

Bits	Name	Description
6:0	DQID	Destination Queue ID. Valid only when the CH_CSR[SIQ] bit is set. For this case, this bit field provides the ID for the destination BMU WQ, UIF RX endpoint or EIF outbound queue to be used for the transfer. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: RSVD_0 0x1: RSVD_1 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: BMU_25 0x1A: BMU_26 0x1B: BMU_SINK_WQ 0x1C: UIF_RX_1_EP 0x1D: UIF_RX_2_EP 0x1E: UIF_RX_3_EP 0x1F: UIF_RX_4_EP

0x3000558 DXE_0_CH5_DADRH

Type: read-write

The channel destination address high register holds the high bits of the destination address for a transfer. Please see the description of CH_DADRL for more info.

DXE_0_CH5_DADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	This register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x300055C DXE_0_CH5_DESCL

Type: read-write

The Channel 5 Linked List Descriptor Pointer register contains the 32 lower bits of the address of the next descriptor to be loaded in the linked list. This address must be dword (32-bit) aligned (addr[1:0]=0 if CH_CTRL[PIQ]=0). Each complete transfer descriptor consists of 7 32-bit values arranged contiguously in memory. The value of this register will be overwritten with the address of the start of the next descriptor set in the list after the current descriptor has been fetched. The meaning of the value in this register depends on the value of the CH_CTRL[PIQ] bit field similar to the way in which SADRL and DADRL are depending in SIQ and DIQ respectively. For CH_CTRL[PIQ]=0 then this register has no bit fields and the value is just intrepreted as an address in flat memory space. When CH_CTRL[PIQ] is set then the descriptor will be read from FIFO type memory in UIF and the register has 2 bit fields: BASE, and SQID. BASE specifies the base address of the UIF Tx queue (derived from the start of the UIF address space in SAHB plus the internal UIF offset).

DXE_0_CH5_DESCL

Bits	Name	Description
31:7	BASE	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify the base address of the UIF endpoint to use as the source of the descriptor. Please refer to the Nova address map document and to the UIF architecture document for guaranteed correct values to use here. For convenience but without a guarantee of accuracy, the base value to use for both the Tx data and management endpoints is the following: base = UIF base + TD_and_TM_offset = 0x0E02_5000 + x100 = 0x0E02_5100>>7 = 0x1C_04A2

DXE_0_CH5_DESCL (cont.)

Bits	Name	Description
6:0	SQID	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify which of the two UIF TX queues to use. Note that in this case software also needs to program the correct base address of the source UIF endpoint in the BASE bit field. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x3000560 DXE_0_CH5_DESCH

Type: read-write

The channel destination address high register holds the high bits of the the address of the next descriptor to be loaded in the linked list.

DXE_0_CH5_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. Please note that if the source of the descriptor is either of the UIF endpoints (CH_CTRL[PIQ]=1) then the value in ADDRH has to be 0 or else the descriptor read could end up mapping to the XIF or PIF. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x3000564 DXE_0_CH5_LST_DESCL

Type: read-only

The read-only Channel 5 Current/last Linked List Descriptor Pointer register contains the low 32-bits of the address of the descriptor currently being processed or of the last descriptor processed if the channel is disabled.

The meaning of the value and bit fields with regards to CH_CTRL[PIQ] is the same as was explained for the CH_DESCL register.

DXE_0_CH5_LST_DESCL

Bits	Name	Description
31:7	BASE	See description of CH_DESCL[BASE].
6:0	SQID	See description of CH_DESCL[SQID]. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x3000568 DXE_0_CH5_LST_DESCH

Type: read-only

The channel destination address high register holds the high bits of the the address of the next descriptor to be loaded in the linked list. Note that The meaning of the value and bit fields is the same as was explained for the CH_DESCL register.

DXE_0_CH5_LST_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address.

0x300056C DXE_0_CH5_BD

Type: read-only

DXE_0_CH5_BD

Bits	Name	Description
31:24	RSVD	Reserved. Always returns 0 when read.
23	VAL	Valid. BD has been loaded and is valid.
22:16	PDU_CNT	PDU count of packet.
15:0	IDX	Index of BD. To get actual physical address must be added to BD/PDU base.

0x3000570 DXE_0_CH5_HEAD

Type: read-only
Reset State: 0x00000000

Address of head of packet.

DXE_0_CH5_HEAD

Bits	Name	Description
31:27	RSVD	Reserved. Reset State: 0x00000000
26	DESCVAL	Descriptor valid. Signifies descriptor has already been loaded. Used to prevent reloading of a descriptor. Reset State: 0x00000000
25:21	DWQID	Destination WQ ID. Original BMU, UIF or EIF destination queue. Valid only when CH_CSR[DIQ]=1 Reset State: 0x00000000
20:16	SWQID	Source WQ ID. Original BMU, UIF or EIF source queue. Valid only when CH_CSR[SIQ]=1 Reset State: 0x00000000
15:0	IDX	Index of Head. Must be added to BD/PDU base for actual physical address.

0x3000574 DXE_0_CH5_TAIL

Type: read-only
Reset State: 0x00000000

Address of tail of packet.

DXE_0_CH5_TAIL

Bits	Name	Description
31:16	RSVD	Reserved. Reset State: 0x00000000
15:0	IDX	Index of Tail. Must be added to BD/PDU base for actual physical address

0x3000578 DXE_0_CH5_PDU

Type: read-only
Reset State: 0x00000000

PDU info register.

All its fields are working fields that get modified as the programmed operation progresses.

DXE_0_CH5_PDU

Bits	Name	Description
31	RSVD	Reserved. Always returns 0 when read. Reset State: 0x00000000
30:24	PDU_CNT	Current PDU count.
23:8	IDX	Index of current PDU. Must be added to BD/PDU base for actual physical address
7:0	FST_OFF	First PDU offset.

0x300057C DXE_0_CH5_TSTMP

Type: read-only
Reset State: 0x00000000

Contains last sampled value of the system timestamp

DXE_0_CH5_TSTMP

Bits	Name	Description
31:0	VALUE	Reset State: 0x00000000

0x3000580 DXE_0_CH6_CTRL

Type: read-write
Reset State: 0x11800708

Serves to configure channel 6 operation

DXE_0_CH6_CTRL

Bits	Name	Description
31	SWAP	Endian Byte Swap Enable. When high instructs DXE to perform an endian swap of the incoming byte stream. The corresponding bit field in the DXE descriptor control word is located at DXE_DESC_CTRL[20]

DXE_0_CH6_CTRL (cont.)

Bits	Name	Description
30:29	BDT_IDX	BD Template Index. When XTYPE=H2B and BDH=1, DXE supports creating a BD by using template data from one of up to 4 different BD templates. The BD template base store is pointed at by the DXE BD_TMPLT(H/L) registers and the address used to read the template data is calculated as follows: BD_TMPLT_ADRR = BD_TMPLT_BASE + (128 * CH_CTRL[BDT_IDX]) The corresponding bit field in the control word of the external descriptor is mapped to bits[19:18]
28	DFMT	Descriptor Format. This bit field is used to select between long and short descriptor formats. When using the short descriptor format, the high part of the source, destination and descriptor addresses will be taken from the SADRH_DFLT, DADRH_DFLT or DESCH_DFLT registers respectively. Default is to use the long descriptor format 0x0: SHORT 0x1: LONG Reset State: 0x00000001
27	ABORT	Writing a one to this bit will cause the channel to stop its current transfer and set the ERR bit and ERR_CODE fields in CH_STATUS. Note that if the channel is currently disabled or if it is about to be disabled because it has just finished its programmed transfer, then the abort request will be ignored and the error bit and error codes won't be set. If the channel is currently masked by the arbiter then setting this bit will forcibly unmask it so that the transfer can be aborted the next time the channel is selected by the internal arbiter. The abort request is automatically cleared by hardware once the channel has aborted the transfer. Also note that since the DXE will not attempt to do any cleanup when a transfer is aborted, software might need to do so. For example, for H2B transfers, software should manually release the BD and any PDUs currently in use by the partial transfer or else a BD/PDU leak will result. Reset State: 0x00000000
26	ENDIANNESS	Specifies the endianness of the master generating the data. Affects alignment of valid bytes for non-dword aligned reads/writes. The corresponding field in the DXE descriptor control word is located in DXE_DESC_CTRL[21] 0x0: BIGEND 0x1: LTLEND Reset State: 0x00000000
25:22	CTR_SEL	Counter Select. If the event counters are enabled (DMA_CSR[ECTR_EN]=1) then this bit field selects the counter that will be incremented at the end of the transfer. By default the value in this bit field is the same as the channel number so that after reset channel 0 increments counter 0, channel 1 increments counter 1 and so on. Reset State: 0x00000006

DXE_0_CH6_CTRL (cont.)

Bits	Name	Description
21	EDVEN	When set, the DMA engine will clear the VAL bit in the DESC_CSR word of the current descriptor once it has completed processing it. This is useful for implementing a descriptor "ring" (see the description of the VALID bit in Table 3.1) Reset State: 0x00000000
20	EDEN	External Descriptor Enable. Use External Descriptor Linked List Reset State: 0x00000000
19	INE_DONE	Enable Channel Interrupt when Channel is Done. The corresponding interrupt source bit is INT_DONE Reset State: 0x00000000
18	INE_ERR	Enable Channel Interrupt on Errors. The corresponding interrupt source bit is INT_ERR Reset State: 0x00000000
17	INE_ED	Enable External Descriptor Interrupt. When this bit is set, an interrupt will be generated after processing a descriptor item that has the INT bit set in its DESC_CTRL word (see Table 3.1). The corresponding interrupt source bit is INT_ED Reset State: 0x00000000
16	STOP	Channel processing stopped due to a request in the last processed linked list descriptor (see the STOP bit in the definition of the DESC_CSR word in Table 3.1). This bit will be automatically cleared when the channel is restarted. Reset State: 0x00000000
15:13	PRIO	This field sets the channel priority. 7: Highest Priority. 0: Lowest Priority.

DXE_0_CH6_CTRL (cont.)

Bits	Name	Description
12:9	BTHLD_SEL	BMU Threshold Select. This value tells DXE which of the BMU BD/PDU thresholds to check before issuing BMU commands that reserve, or get BDs or PDUs. It also specifies the module index value that will be used to issue any required BMU commands (see BMU spec for details). The value of this bit field is only meaningful for transfer types that involve the BMU and therefore its value will be ignored for H2H transfers. 0x0: RSVD0 0x1: RSVD1 0x2: THLD2 0x3: THLD3 0x4: THLD4 0x5: THLD5 0x6: THLD6 0x7: THLD7 0x8: THLD8 0x9: THLD9 0xA: THLD10 0xB: RSVD11 0xC: RSVD12 0xD: RSVD13 0xE: RSVD14 0xF: RSVD15 Reset State: 0x00000003
8	PDU_REL	0x0: Don't release BD and PDUs when done. 1: Release BD and PDUs when done. 0x0: KEEP 0x1: RELEASE Reset State: 0x00000001

DXE_0_CH6_CTRL (cont.)

Bits	Name	Description
7	PIQ	next descriptor Pointer address Is Queue. When set the source of the descriptor address is interepreted as a queue ID instead of just the address of a flat memory location. The only valid source queues for descriptors are the UIF Tx data and Tx management endpoints. Any other IDs will result the channel aborting the transfer with an invalid source queue error. Therefore, when this bit is set, software must ensure that the CH_DESCL[QID] bit field is set to a valid queue ID and that the CH_DESCL[BASE] bit field is set to the base address of the source UIF endpoint. This base address is formed by taking the base address for the UIF block in the SAHB bus which can be found in the Nova address map document and then adding the internal UIF offset for the correct source endpoint. This offsets can be obtained from the UIF specification document. For convenience, the current internal UIF offsets are provided in the descripiton of the QID bit field in the CH_DESCL register description. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
6	DIQ	Destination Is Queue. When set the destination address is interepreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF RX endpoints or and EIF outbound FIFO. When this bit is set, software must ensure that the DADR[QID] bit field is set to a valid queue ID and that the DADR[BASE] bit field is set to the base address of the destination queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000
5	SIQ	Source Is Queue. When set the source address is interepreted as a queue ID instead of just the address of a flat memory location. The queue could be either a BMU queue, one of the UIF TX endpoints or and EIF inbound FIFO. When this bit is set, software must ensure that the SADR[QID] bit field is set to a valid queue ID and that the SADR[BASE] bit field is set to the base address of the source queue for UIF or EIF, or to zero for a BMU queue. endpoint. 0x0: FLAT 0x1: QUEUE Reset State: 0x00000000

DXE_0_CH6_CTRL (cont.)

Bits	Name	Description
4	BDH	BD Handling bit. The behavior depends on the setting of XTYPE. If XTYPE is: H2B: Then if BDH is: 0: Use first 128 bytes of packet as BD. 1: Create BD from BD template (Up to 4 supported. Also see desc for BDT_IDX). B2H: Then if BDH is: 0: Insert BD in front of payload. 1: Discard BD. For XTYPE values of H2H and B2B the value of this bit is ignored. Reset State: 0x00000000
3	EOP	End of Packet bit. For H2B transfers marks the end of a packet Please note that when not using external descriptors DXE cannot support the gather functionality and therefore the EOP bit must be set. For XTYPE values of H2H, B2B and B2H the value of this bit is ignored. Reset State: 0x00000001
2:1	XTYPE	Transfer Type. Specifies the type of transfer to perform: 00: H2H. Host space to Host space transfer. space to BMU space transfer. translation. translation. DMA engine will also perform the required data format translation. The format translation behavior can be modified by the setting of the BDH and PAD bits. 0x0: H2H 0x1: B2B 0x2: H2B 0x3: B2H
0	EN	Channel Enable or Restart. Writing this bit with a one either starts a new DMA transfer according to the parameters programmed in the channel's configuration registers and clears the DONE bit or, if the channel is already enabled but the STOP bit is set, then it restarts channel processing and also clears the STOP bit. This bit is automatically cleared when a single transfer completes or, if the channel is configured to use linked list descriptors, when the last transfer in the descriptor linked list completes (DESC_NXT is NULL or/and DESC_CSR[VALID]=0). The channel is also disabled and this bit cleared if a channel error is encountered. Reading this bit indicates whether a channel is currently enabled or disabled:. The Channel Enable bit status can also be found by reading the DMA_ENCH register which aggregates the EN bits of all channels. Note: Software must take care to not disable the channel while it is busy or data could be lost. Reset State: 0x00000000

0x3000584 DXE_0_CH6_STATUS

Type: read-write
Reset State: 0x00000000

Serves to report the status of the programmed channel operation.

DXE_0_CH6_STATUS

Bits	Name	Description
31:16	RSVD	Reserved. Reads always return 0. Writes are ignored.
15	INT_DONE	Interrupt Source: Asserted when the channel has finished all processing.
14	INT_ERR	Interrupt Source: Asserted when a channel error has occurred. Masked by the INE_ERR
13	INT_ED	Interrupt Source. Descriptor Done and INT requested
12	ABORT_REQ	Abort Request. Software has requested that the current operation be aborted. However, if CH_STATUS[EN] is still set then the channel has registered the request but is not yet in a position to abort the transfer "safely". Once the channel finishes its current operation it will abort the transfer and set the error flag and error code bit fields accordingly.
11	STOP_REQ	Stop Request. Software has requested that the channel stop it operation after the current descriptor has been processed. Once this happens the STOPD bit field will be set to one and the channel will be disabled.

DXE_0_CH6_STATUS (cont.)

Bits	Name	Description
10:6	ERR_CODE	Used to identify the source or cause of an error. 0x0: NONE 0x1: SAHB_ERR 0x2: H2H_RD_BUS_ERR 0x3: H2H_WR_BUS_ERR 0x4: PRG_INV_XTYPE 0x5: BERR_POPWQ 0x6: BERR_PUSHWQ 0x7: BERR_RLSS 0x8: BERR_GETPDU 0x9: PRG_INV_WQ 0xA: PRG_INV_H2H_SRC_QID 0xB: PRG_INV_H2H_DST_QID 0xC: PRG_INV_B2H_SRC_QID 0xD: PRG_INV_B2H_DST_QID 0xE: PRG_INV_B2H_SRC_IDX 0xF: PRG_INV_H2B_SRC_QID 0x10: PRG_INV_H2B_DST_QID 0x11: PRG_INV_H2B_DST_IDX 0x12: PRG_INV_H2B_SZ 0x13: PRG_INV_SADR 0x14: PRG_INV_DADR 0x15: PRG_INV_EDADR 0x16: PRG_INV_SRC_WQID 0x17: PRG_INV_DST_WQID 0x18: PRG_XTYPE_MSMTCH 0x19: PKT_ERR 0x1A: ABORT 0x1B: PDU_CNT_OVFL Reset State: 0x00000000
5	ERR	DMA channel stopped due to error. To clear the error status it is necessary to write a 1 into this bit position.
4	STOPD	Channel Stopped. The channel has stopped further processing and disabled itself due to a stop request in the last processed descriptor. Reset State: 0x00000000
3	MSKD	Channel Masked. The channel has been automatically masked out from arbitration due to a blocking condition. Reset State: 0x00000000
2	DONE	DMA channel Done. This bit will be automatically cleared the next time the channel is enabled. Reset State: 0x00000000
1	BUSY	Channel busy. HIgh when the channel is enabled and currently active (won internal arbitration) Reset State: 0x00000000

DXE_0_CH6_STATUS (cont.)

Bits	Name	Description
0	EN	Channel Enabled. Copy of CH_CTRL[EN]. Reset State: 0x00000000

0x3000588 DXE_0_CH6_SZ

Type: read-write

The transfer size register specifies the total, remaining, and burst or 'chunk' transfer sizes for each channel. The maximum total transfer size is 16K-1 bytes. The chunk size control can be useful to control the relative bandwidth used by each channel as the dma engine will change channels, release the AHB bus, and rearbitrate for access after transferring chunk size bytes.

DXE_0_CH6_SZ

Bits	Name	Description
31:28	CHK_SZ	Chunk transfer size. Specifies the number of bytes (in multiples of 8) to be transferred at one given time (not implying they are buffered but that they will be transferred for each start event in one bus request cycle). If chunk size is zero the DMA engine will always perform maximum chunk size transfers. Maximum chunk size is 128 bytes.
27:14	REM_SZ	Remaining transfer size. Specifies the number of bytes that remain to be transferred to complete the current operation.
13:0	TOT_SZ	Total Transfer Size. Specifies the number of bytes to be transferred. Maximum total transfer size is (4K-1) bytes. Note: This field is unnecessary and will be ignored for B2H or B2B transfers, when the source of the transfer is in BMU space (either BMU queue or direct pointer to BD). This is because the size of the transfer will be the packet length encoded in the BD at offset 0x0c bits [11:0].

0x300058C DXE_0_CH6_SADRL

Type: read-write

The channel source address register specifies either the source address in flat internal or external memory, or else the BMU queue ID, UIF TX endpoint ID, or EIF inbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the source, addresses can have arbitrary byte-alignment When using a BMU queue, UIF endpoint or EIF fifo as a source, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[SIQ] bit. When CH_CSR[SIQ] is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when it is set this register has two bit fields: The SQID bit field

used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF source endpoint/FIFO.
ID (CH_CSR[SIQ] = 1 and SWQID matches BMU), the DXE will issue a BMU POPWQ command to pop the specified queue and obtain the BD index of the source packet. Else, when the source is an address (CH_CSR[SIQ] = 0), the DXE will interpret the address as the index of the packet BD and will add it to the BMU_BASE to obtain the physical addresss to use to fetch it directly from memory.
(CH_CSR[SIQ] = 1 and SQID matches UIF/EIF), software should program the SAHB base address of the UIF source endpoint in the BASE bit field and the queue ID to match in the SWQID bit field, then the DXE will use the base address given to generate the physical address and read the data over the SAHB bus and also use the appropriate sideband signals as specified by the SQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and SQID fields are consistend and refer to the same endpoint or else hangs or unpredictable behavior might occur. Else, when the source is just a location in flat memory space, (CH_CSR[SIQ] = 0), the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the register as the physical address to use to fetch the data. For this case, software should make sure that the provided address maps to the intended source interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus.
transfers the address must conform to the following format:
(CH_CSR[SIQ] = 0):
BD_INDEX[15:0]
(CH_CSR[SIQ] = 1 & SQID matching one of the BMU queues):
   ADDR[31:7] = Any value will do but zero preferred
   ADDR[6:0] = Any BMU Queue ID as specified in description of SQID field format:
   ADDR[31:0] = address mapping to source interface
endpoints or EIF FIFOs (CH_CSR[SIQ] = 1 & QID matching UIF or EIF):
   ADDR[31:7] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document)
or EIF as specified in description of SQID field

DXE_0_CH6_SADRL

Bits	Name	Description
31:7	BASE	Base Address. For this case, this bit field provides the base address of the source UIF TX endpoint or EIF inbound FIFO. The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd interface uarch for the offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH6_SADRL (cont.)

Bits	Name	Description
6:0	SQID	Source Queue ID. set. For this case, this bit field provides the ID for the source BMU, UIF or EIF queue to be used for the transfer. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: RSVD_25 0x1A: RSVD_26 0x1B: RSVD_27 0x1C: RSVD_28 0x1D: RSVD_29 0x1E: RSVD_30 0x1F: RSVD_31

0x3000590 DXE_0_CH6_SADRH

Type: read-write

The channel source address high register holds the high bits of the source address for a transfer. Please see the description of CH_SADRL for more info.

DXE_0_CH6_SADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_SADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x3000594 DXE_0_CH6_DADRL

Type: read-write

The channel destination address register specifies either the destination address in flat internal or external memory, or else the BMU queue ID, UIF RX endpoint ID, or EIF outbound FIFO ID for the transfer. The register must be programmed directly by software before the channel is enabled, then, once the DMA channel is enabled, the register is updated after each atomic chunk transfer (read+write) with the number of bytes transferred. (except when using a UIF/EIF queue) and also after loading a new descriptor When using flat memory as the destination, addresses can have arbitrary byte-alignment. When using a BMU queue, UIF endpoint or EIF fifo as a destination, the software is responsible for programming a valid queue ID and correct base address for the queue. The layout of bit fields in this register depends on the setting of the CH_CSR[DIQ] bit. When this bit is clear then the register has no bit fields and the full 32-bits are interpreted as the physical address of a location in flat memory, and when the bit is set this register has two bit fields: The DQID bit field used to specify the queue ID, and the BASE bit field used to provide the base address for the UIF or EIF destination endpoint/FIFO.
a BMU queue as the destination (CH_CSR[DIQ] = 1 and DQID matches BMU), the DXE will push the index of the BD of the packet into the specified queue at the end of the packet transfer. Therefore, software is responsible for programming a valid BMU Queue ID.
destination is an index (CH_CSR[DIQ] = 0), the BD will be written to the address obtained by adding the provided index to the BMU_BASE, again, the software must ensure that said address is legal and known to BMU. That is, software must preallocate the BD (get the BD from BMU via GET BD/PDU cmd) for the BD before starting the transfer. For B2H or H2H transfers, if the destination is a UIF endpoint or EIF FIFO (CH_CSR[DIQ] = 1 and DQID matches UIF/EIF), software should program the SAHB base address of the UIF destination endpoint in the BASE bit field and the queue ID to match in the DQID bit field, then the DXE will use the base address given to generate the physical address and write the data over the SAHB bus and also use the appropriate sideband signals as specified by the DQID field to communicate with the selected UIF endpoint. software should make sure that the BASE and DQID fields are consistent and refer to the same endpoint else hangs or unpredictable behavior might occur. On the other hand, when the destination is just a location in flat memory space, (CH_CSR[DIQ] = 0), be it internal or external, the bit fields lose their special meaning and DXE will just use the full 32-bits programmed into the

register as the address to write the data. For this case, software should make sure that the address maps to the intended destination interface (Internal memory, USB, PCI, PCIe) by conforming to the address map specified for the SAHB bus. To summarize, for H2B and B2B transfers the address must conform to the following format:
   ADDR[31:7] = BMU_BASE + BD_INDEX[15:0]
   ADDR[6:0] = 7'd0
DQID matching one of the BMU queues):
do but zero preferred
description of QID field
following format:
   ADDR[31:0] = address mapping to destination interface
endpoints or EIF FIFOs (CH_CSR[DIQ] = 1 & DQID matching UIF or EIF):
   ADDR[31:5] = UIF RX endpoint base or EIF inboud FIFO base (see address map + Interface uarch document)
or EIF as specified in description of DQID field

DXE_0_CH6_DADRL

Bits	Name	Description
31:7	BASE	Base Address. For this case, this bit field provides the base address of the destination UIF RX endpoint or EIF outbound FIFO (for BMU software may use any value can be used but zero is suggested). The correct base address (with 1Kb granularity) for the source interface can be found in the address map document located here (sys control tab): //depot/hardware/ip/internal/nova/docs/arch/Address Map Drawing.vsd interface uarch for the offset within the interface's address space. When CH_CSR[SIQ] bit is not set this field loses its special meaning and is interpreted only as part of the full 32-bit source address.

DXE_0_CH6_DADRL (cont.)

Bits	Name	Description
6:0	DQID	Destination Queue ID. is set. For this case, this bit field provides the ID for the destination BMU WQ, UIF RX endpoint or EIF outbound queue to be used for the transfer. its special meaning and is interpreted only as part of the full 32-bit source address. 0x0: RSVD_0 0x1: RSVD_1 0x2: BMU_2 0x3: BMU_3 0x4: BMU_4 0x5: BMU_5 0x6: BMU_6 0x7: BMU_7 0x8: BMU_8 0x9: BMU_9 0xA: BMU_10 0xB: BMU_11 0xC: BMU_12 0xD: BMU_13 0xE: BMU_14 0xF: BMU_15 0x10: BMU_16 0x11: BMU_17 0x12: BMU_18 0x13: BMU_19 0x14: BMU_20 0x15: BMU_21 0x16: BMU_22 0x17: BMU_23 0x18: BMU_24 0x19: BMU_25 0x1A: BMU_26 0x1B: BMU_SINK_WQ 0x1C: UIF_RX_1_EP 0x1D: UIF_RX_2_EP 0x1E: UIF_RX_3_EP 0x1F: UIF_RX_4_EP

0x3000598 DXE_0_CH6_DADRH

Type: read-write

The channel destination address high register holds the high bits of the destination address for a transfer. Please see the description of CH_DADRL for more info.

DXE_0_CH6_DADRH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	This register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x300059C DXE_0_CH6_DESCL

Type: read-write

The Channel 6 Linked List Descriptor Pointer register contains the 32 lower bits of the address of the next descriptor to be loaded in the linked list. This address must be dword (32-bit) aligned (addr[1:0]=0 if CH_CTRL[PIQ]=0). Each complete transfer descriptor consists of 7 32-bit values arranged contiguously in memory. The value of this register will be overwritten with the address of the start of the next descriptor set in the list after the current descriptor has been fetched. The meaning of the value in this register depends on the value of the CH_CTRL[PIQ] bit field similar to the way in which SADRL and DADRL are depending in SIQ and DIQ respectively. For CH_CTRL[PIQ]=0 then this register has no bit fields and the value is just interpreted as an address in flat memory space. When CH_CTRL[PIQ] is set then the descriptor will be read from FIFO type memory in UIF and the register has 2 bit fields: BASE, and SQID. BASE specifies the base address of the UIF Tx queue (derived from the start of the UIF address space in SAHB plus the internal UIF offset).

DXE_0_CH6_DESCL

Bits	Name	Description
31:7	BASE	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify the base address of the UIF endpoint to use as the source of the descriptor. Please refer to the Nova address map document and to the UIF architecture document for guaranteed correct values to use here. For convenience but without a guarantee of accuracy, the base value to use for both the Tx data and management endpoints is the following: 0x0E02_5000 + x100 = 0x0E02_5100>>7 = 0x1C_04A2

DXE_0_CH6_DESCL (cont.)

Bits	Name	Description
6:0	SQID	This bit field only exists and has meaning when the descriptor needs to be read from a UIF TX queue (and therefore CH_CTRL[PIQ]=1), then it serves to specify which of the two UIF TX queues to use. Note that in this case software also needs to program the correct base address of the source UIF endpoint in the BASE bit field. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x30005A0 DXE_0_CH6_DESCH

Type: read-write

The channel destination address high register holds the high bits of the address of the next descriptor to be loaded in the linked list.

DXE_0_CH6_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address. With the current address mapping these high order bits determine where the transfer is routed and whether the lower 32 bits of the address (the ones held in CH_DADRL) go untranslated through PIF or XIF or if they use the PIF and XIF address translation windows. See the bit field encoding descriptions for an explanation. Please note that if the source of the descriptor is either of the UIF endpoints (CH_CTRL[PIQ]=1) then the value in ADDRH has to be 0 or else the descriptor read could end up mapping to the XIF or PIF. 0x0: ADDR_XTLN 0x1: PIF_NO_XTLN 0x2: XIF_NO_XTLN 0x3: RSVD

0x30005A4 DXE_0_CH6_LST_DESCL

Type: read-only

The read-only Channel 6 Current/last Linked List Descriptor Pointer register contains the low 32-bits of the address of the descriptor currently being processed or of the last descriptor processed if the channel is disabled.
CH_CTRL[PIQ] is the same as was explained for the CH_DESCL register.

DXE_0_CH6_LST_DESCL

Bits	Name	Description
31:7	BASE	See description of CH_DESCL[BASE].
6:0	SQID	See description of CH_DESCL[SQID]. 0x0: UIF_TX_DATA_EP 0x1: UIF_TX_MGMT_EP

0x30005A8 DXE_0_CH6_LST_DESCH

Type: read-only

The channel destination address high register holds the high bits of the address of the next descriptor to be loaded in the linked list. Note that The meaning of the value and bit fields is the same as was explained for the CH_DESCL register.

DXE_0_CH6_LST_DESCH

Bits	Name	Description
31:2	RSVD	Reserved. Writes ignored. Reads always return zeroes.
1:0	ADDRH	For taurus, this register holds bits 33 and 32 of the address.

0x30005AC DXE_0_CH6_BD

Type: read-only

DXE_0_CH6_BD

Bits	Name	Description
31:24	RSVD	Reserved. Always returns 0 when read.
23	VAL	Valid. BD has been loaded and is valid.
22:16	PDU_CNT	PDU count of packet.
15:0	IDX	Index of BD. To get actual physical address must be added to BD/PDU base.

0x30005B0 DXE_0_CH6_HEAD

Type: read-only
Reset State: 0x00000000

Address of head of packet.

DXE_0_CH6_HEAD

Bits	Name	Description
31:27	RSVD	Reserved. Reset State: 0x00000000
26	DESCVAL	Descriptor valid. Signifies descriptor has already been loaded. Used to prevent reloading of a descriptor. Reset State: 0x00000000
25:21	DWQID	Destination WQ ID. Original BMU, UIF or EIF destination queue. Valid only when CH_CSR[DIQ]=1 Reset State: 0x00000000
20:16	SWQID	Source WQ ID. Original BMU, UIF or EIF source queue. Valid only when CH_CSR[SIQ]=1 Reset State: 0x00000000
15:0	IDX	Index of Head. Must be added to BD/PDU base for actual physical address.

0x30005B4 DXE_0_CH6_TAIL

Type: read-only
Reset State: 0x00000000

Address of tail of packet.

DXE_0_CH6_TAIL

Bits	Name	Description
31:16	RSVD	Reserved. Reset State: 0x00000000
15:0	IDX	Index of Tail. Must be added to BD/PDU base for actual physical address

0x30005B8 DXE_0_CH6_PDU

Type: read-only
Reset State: 0x00000000

PDU info register.
operation progresses.

DXE_0_CH6_PDU

Bits	Name	Description
31	RSVD	Reserved. Always returns 0 when read. Reset State: 0x00000000
30:24	PDU_CNT	Current PDU count.
23:8	IDX	Index of current PDU. Must be added to BD/PDU base for actual physical address
7:0	FST_OFF	First PDU offset.

0x30005BC DXE_0_CH6_TSTMP

Type: read-only
Reset State: 0x00000000

Contains last sampled value of the system timestamp

DXE_0_CH6_TSTMP

Bits	Name	Description
31:0	VALUE	Reset State: 0x00000000

16.2.10 lte_cxm

0x3000008 LTE_CXM_CXM_WLAN_TX_GRANT_SEL

Type: read-write
Reset State: 0x00000000

CxM_WLAN_TX_Grant_sel

LTE_CXM_CXM_WLAN_TX_GRANT_SEL

Bits	Name	Description
0	CXM_WLAN_TX_GRANT_SEL	TX Grant Select for Wlan. 1: Select CxM Wlan Tx Grant, 0: Select QTA tx grant. Reset State: 0x00000000

0x3000010 LTE_CXM_CXM_WLAN_RX_GRANT_SEL

Type: read-write
Reset State: 0x00000000

CxM_WLAN_RX_Grant_sel

LTE_CXM_CXM_WLAN_RX_GRANT_SEL

Bits	Name	Description
0	CXM_WLAN_RX_GRANT_SEL	RX Grant Select for Wlan. 1: Select CxM Wlan Rx Grant, 0: Select QTA rx grant. Reset State: 0x00000000

0x3000014 LTE_CXM_CXM_WLAN_TX_RX_GRANT_EN

Type: read-write
Reset State: 0x0000000F

CxM_TX_RX_Grant_Enable

LTE_CXM_CXM_WLAN_TX_RX_GRANT_EN

Bits	Name	Description
3	CXM_WLAN_RX_GRANT_BM_OVERWRITE_VALUE	Override Value of WLAN RX Grant. Reset State: 0x00000001
2	CXM_WLAN_RX_GRANT_BM_OVERWRITE_ENABLE	Enable override of WLAN RX Grant. Reset State: 0x00000001
1	CXM_WLAN_TX_GRANT_BM_OVERWRITE_VALUE	Override Value of WLAN TX Grant. Reset State: 0x00000001
0	CXM_WLAN_TX_GRANT_BM_OVERWRITE_ENABLE	Enable override of WLAN TX Grant. Reset State: 0x00000001

0x3000018 LTE_CXM_CXM_TIMER_COUNTER

Type: read-only
Reset State: 0x00000000

CxM_Timer_Counter

LTE_CXM_CXM_TIMER_COUNTER

Bits	Name	Description
31:0	TIMER_COUNTER	Counter running at 19.2 MHz Reset State: 0x00000000

0x300001C LTE_CXM_LTE_CXM_COUNTER_LOAD_CMD

Type: read-write
Reset State: 0x00000000

CxM_Counter_Load_CMD

LTE_CXM_LTE_CXM_COUNTER_LOAD_CMD

Bits	Name	Description
0	CXM_COUNTER_LOAD_CMD	0 -> 1 change in value triggers loading of new value. Setting is done by software and reset by hardware once load command is performed Reset State: 0x00000000

0x3000020 LTE_CXM_LTE_CXM_COUNTER_LOAD_CTRL

Type: read-write
Reset State: 0x00000000

CxM_Counter_Load_Ctrl

LTE_CXM_LTE_CXM_COUNTER_LOAD_CTRL

Bits	Name	Description
0	CXM_COUNTER_LOAD_CTRL	0x0: CxM Timer counter shall be loaded with CxM_Counter_Load_Value when CxM_Counter_Load_CMD changes from 0 to 1; this load is one shot by self-clear CxM_Counter_Load_CMD to zero. 1: CxM Timer counter shall be loaded with CxM_Counter_Load_Value when CxM_Timer_Counter is equal to CxM_Counter_Load_Timer_Stamp; this loading is also triggered by CxM_Counter_Load_CMD changes from 0 to 1 and this load is one shot by self-clear CxM_Counter_Load_CMD to zero when the condition (CxM_Timer_Counter is equal to CxM_Counter_Load_Timer_Stamp happens.) Reset State: 0x00000000

0x3000024 LTE_CXM_CXM_COUNTERLOAD_VALUE

Type: read-write
Reset State: 0x00000000

CxM_Counter_Load_Value

LTE_CXM_CXM_COUNTERLOAD_VALUE

Bits	Name	Description
31:0	CXM_COUNTER_LOAD_VALUE	The value to be loaded to CxM_Timer_Counter controlled by CxM_Counter_Load_Ctrl. Reset State: 0x00000000

0x3000028 LTE_CXM_CXM_COUNTER_LOAD_TIME_STAMP

Type: read-write
Reset State: 0x00000000

CxM_Counter_Time_Stamp

LTE_CXM_CXM_COUNTER_LOAD_TIME_STAMP

Bits	Name	Description
31:0	CXM_COUNTER_TIME_STAMP	The value to be loaded to CxM_Timer_Counter controlled by CxM_Counter_Load_Ctrl. Reset State: 0x00000000

0x300002C LTE_CXM_CXM_CLOCK_SEL

Type: read-write
Reset State: 0x00000000

CxM_CLK_Sel

LTE_CXM_CXM_CLOCK_SEL

Bits	Name	Description
0	CXM_CLK_SEL	0x0: Select PMIC 19.2MHz clock for CxM logic. 1: Select IRIS generated 19.2MHz clock for CxM logic. Reset State: 0x00000000

0x3000030 LTE_CXM_CXM_SW_CAPTURE_CLK

Type: read-write
Reset State: 0x00000000

CXM_SW_Capture_CLK

LTE_CXM_CXM_SW_CAPTURE_CLK

Bits	Name	Description
0	CXM_SW_CAPTURE_CLK	0->1 triggers sync timing. Reset State: 0x00000000

0x3000034 LTE_CXM_CXM_SW_CAPTURE_SEL

Type: read-write
Reset State: 0x00000000

CXM_SW_Capture_SEL

LTE_CXM_CXM_SW_CAPTURE_SEL

Bits	Name	Description
0	CXM_SW_CAPTURE_SEL	0x0: Select SW_Capture_CLK to trigger timing sync 1: Select LET_Frame_Sync_Test_In to trigger timing sync. Reset State: 0x00000000

0x3000038 LTE_CXM_LTE_CXM_COUNTER_CAPTURED

Type: read-only
Reset State: 0x00000000

CxM_Counter_Captured

LTE_CXM_LTE_CXM_COUNTER_CAPTURED

Bits	Name	Description
31:0	CXM_COUNTER_CAPTURED	Value captured from CxM_Timer_Counter when timing sync is triggered. Reset State: 0x00000000

0x300003C LTE_CXM_CXM_CP_INTERRUPT_CTRL

Type: read-write
Reset State: 0x00000000

CxM_Interrupt_Ctrl

LTE_CXM_CXM_CP_INTERRUPT_CTRL

Bits	Name	Description
3:0	CXM_INTERRUPT_CTRL	Bit_i controls the mode of strobe i, i= 0,1,2,3. 0: indicates the strobe is one-shot, 1: indicates the strobe is periodic. Reset State: 0x00000000

0x3000040 LTE_CXM_CXM_CP_INTERRUPT_MASK_N

Type: read-write
Reset State: 0x00000000

CxM_Interrupt_Mask_n

LTE_CXM_CXM_CP_INTERRUPT_MASK_N

Bits	Name	Description
3:0	CXM_INTERRUPT_MASK_N	Bit_i controls the mode of strobe i, i= 0,1,2,3. 0: strobe is disabled 1: strobe is enabled Reset State: 0x00000000

0x3000044 LTE_CXM_CXM_CP_INTERRUPT_RESET_N

Type: read-write
Reset State: 0x00000000

CxM_Interrupt_Reset_n

LTE_CXM_CXM_CP_INTERRUPT_RESET_N

Bits	Name	Description
3:0	CXM_INTERRUPT_RESET_N	Bit_i resets strobe i, i= 0,1,2,3. 0 indicates reset, i.e., no further strobes are generated after reset. For one-shot interrupt, it is self cleared to zero. For periodic interrupt, it is not self-cleared (CxM-SW can reset it). Reset State: 0x00000000

0x3000050 LTE_CXM_CXM_CP_INTERRUPT_STATUS

Type: read-only
Reset State: 0x00000000

CxM_Interrupt_Status

LTE_CXM_CXM_CP_INTERRUPT_STATUS

Bits	Name	Description
3:0	CXM_INTERRUPT_STATUS	0x1: indicates the CxM_Interrupt is generated by strobe 0 0x2: indicates the CxM_Interrupt is generated by strobe 1 0x4: indicates the CxM_Interrupt is generated by strobe 2 0x8: indicates the CxM_Interrupt is generated by strobe 3 This register is readable by CxM-SW. This register is self-cleared. Reset State: 0x00000000

0x3000054 LTE_CXM_CXM_WLAN_TX_GRANT_ENABLE1

Type: read-write
Reset State: 0x00000000

CxM_WLAN_TX_Grant_Enable1

LTE_CXM_CXM_WLAN_TX_GRANT_ENABLE1

Bits	Name	Description
0	CXM_WLAN_TX_GRANT_ENABLE1	This register is used together with CxM_Timer_Counter CxM_WLAN_TX_Grant_Threshold1, and CxM_WLAN_TX_Grant_Value1 Reset State: 0x00000000

0x3000058 LTE_CXM_CXM_WLAN_TX_GRANT_THRESHOLD1

Type: read-write
Reset State: 0x00000000

CxM_WLAN_TX_Grant_Threshold1

LTE_CXM_CXM_WLAN_TX_GRANT_THRESHOLD1

Bits	Name	Description
31:0	CXM_WLAN_TX_GRANT_THRESHOLD1	This register is used together with CxM_Timer_Counter, CxM_WLAN_TX_Grant_Enable1, and CxM_WLAN_TX_Grant_Value1. Reset State: 0x00000000

0x300005C LTE_CXM_CXM_WLAN_TX_GRANT_VALUE1

Type: read-write
Reset State: 0x00000000

CxM_WLAN_TX_Grant_Value1

LTE_CXM_CXM_WLAN_TX_GRANT_VALUE1

Bits	Name	Description
0	CXM_WLAN_TX_GRANT_VALUE1	This register is used together with CxM_Timer_Counter, CxM_WLAN_TX_Grant_Enable1, and CxM_WLAN_TX_Grant_Threshold1. Reset State: 0x00000000

0x3000060 LTE_CXM_CXM_WLAN_TX_GRANT_ENABLE2

Type: read-write
Reset State: 0x00000000

CxM_WLAN_TX_Grant_Enable2

LTE_CXM_CXM_WLAN_TX_GRANT_ENABLE2

Bits	Name	Description
0	CXM_WLAN_TX_GRANT_VALUE2	This register is used together with CxM_Timer_Counter, CxM_WLAN_TX_Grant_Enable2, and CxM_WLAN_TX_Grant_Threshold2. Reset State: 0x00000000

0x3000064 LTE_CXM_CXM_WLAN_TX_GRANT_THRESHOLD2

Type: read-write
Reset State: 0x00000000

CxM_WLAN_TX_Grant_Threshold2

LTE_CXM_CXM_WLAN_TX_GRANT_THRESHOLD2

Bits	Name	Description
31:0	CXM_WLAN_TX_GRANT_THRESHOLD2	This register is used together with CxM_Timer_Counter, CxM_WLAN_TX_Grant_Enable2, and CxM_WLAN_TX_Grant_Value2. Reset State: 0x00000000

0x3000068 LTE_CXM_CXM_WLAN_TX_GRANT_VALUE2

Type: read-write
Reset State: 0x00000000

CxM_WLAN_TX_Grant_Value2

LTE_CXM_CXM_WLAN_TX_GRANT_VALUE2

Bits	Name	Description
0	CXM_WLAN_TX_GRANT_VALUE2	This register is used together with CxM_Timer_Counter, CxM_WLAN_TX_Grant_Enable1, and CxM_WLAN_TX_Grant_Threshold2. Reset State: 0x00000000

0x300006C LTE_CXM_CXM_WLAN_RX_GRANT_ENABLE1

Type: read-write
Reset State: 0x00000000

CxM_WLAN_RX_Grant_Enable1

LTE_CXM_CXM_WLAN_RX_GRANT_ENABLE1

Bits	Name	Description
0	CXM_WLAN_RX_GRANT_ENABLE1	This register is used together with CxM_Timer_Counter CxM_WLAN_RX_Grant_Threshold1, and CxM_WLAN_RX_Grant_Value1 Reset State: 0x00000000

0x3000070 LTE_CXM_CXM_WLAN_RX_GRANT_THRESHOLD1

Type: read-write
Reset State: 0x00000000

CxM_WLAN_RX_Grant_Threshold1

LTE_CXM_CXM_WLAN_RX_GRANT_THRESHOLD1

Bits	Name	Description
31:0	CXM_WLAN_RX_GRANT_THRESHOLD1	This register is used together with CxM_Timer_Counter, CxM_WLAN_RX_Grant_Enable1, and CxM_WLAN_RX_Grant_Value1. Reset State: 0x00000000

0x3000074 LTE_CXM_CXM_WLAN_RX_GRANT_VALUE1

Type: read-write
Reset State: 0x00000000

CxM_WLAN_RX_Grant_Value1

LTE_CXM_CXM_WLAN_RX_GRANT_VALUE1

Bits	Name	Description
0	CXM_WLAN_RX_GRANT_VALUE1	This register is used together with CxM_Timer_Counter, CxM_WLAN_RX_Grant_Enable1, and CxM_WLAN_RX_Grant_Threshold1. Reset State: 0x00000000

0x3000078 LTE_CXM_CXM_WLAN_RX_GRANT_ENABLE2

Type: read-write
Reset State: 0x00000000

CxM_WLAN_RX_Grant_Enable2

LTE_CXM_CXM_WLAN_RX_GRANT_ENABLE2

Bits	Name	Description
0	CXM_WLAN_RX_GRANT_ENABLE2	This register is used together with CxM_Timer_Counter CxM_WLAN_RX_Grant_Threshold2, and CxM_WLAN_RX_Grant_Value2 Reset State: 0x00000000

0x300007C LTE_CXM_CXM_WLAN_RX_GRANT_THRESHOLD2

Type: read-write
Reset State: 0x00000000

CxM_WLAN_RX_Grant_Threshold2

LTE_CXM_CXM_WLAN_RX_GRANT_THRESHOLD2

Bits	Name	Description
31:0	CXM_WLAN_RX_GRANT_THRESHOLD2	This register is used together with CxM_Timer_Counter, CxM_WLAN_RX_Grant_Enable2, and CxM_WLAN_RX_Grant_Value2. Reset State: 0x00000000

0x3000080 LTE_CXM_CXM_WLAN_RX_GRANT_VALUE2

Type: read-write
Reset State: 0x00000000

CxM_WLAN_RX_Grant_Value2

LTE_CXM_CXM_WLAN_RX_GRANT_VALUE2

Bits	Name	Description
0	CXM_WLAN_RX_GRANT_VALUE2	This register is used together with CxM_Timer_Counter, CxM_WLAN_RX_Grant_Enable2, and CxM_WLAN_RX_Grant_Threshold2. Reset State: 0x00000000

0x3000084 LTE_CXM_CXM_BT_TX_GRANT_ENABLE1

Type: read-write
Reset State: 0x00000000

CxM_BT_TX_Grant_Enable1

LTE_CXM_CXM_BT_TX_GRANT_ENABLE1

Bits	Name	Description
0	CXM_BT_TX_GRANT_ENABLE1	This register is used together with CxM_Timer_Counter CxM_BT_TX_Grant_Threshold1, and CxM_BT_TX_Grant_Value1 Reset State: 0x00000000

0x3000088 LTE_CXM_CXM_BT_TX_GRANT_THRESHOLD1

Type: read-write
Reset State: 0x00000000

CxM_BT_TX_Grant_Threshold1

LTE_CXM_CXM_BT_TX_GRANT_THRESHOLD1

Bits	Name	Description
31:0	CXM_BT_TX_GRANT_THRESHOLD1	This register is used together with CxM_Timer_Counter, CxM_BT_TX_Grant_Enable1, and CxM_BT_TX_Grant_Value1. Reset State: 0x00000000

0x300008C LTE_CXM_CXM_BT_TX_GRANT_VALUE1

Type: read-write
Reset State: 0x00000000

CxM_BT_TX_Grant_Value1

LTE_CXM_CXM_BT_TX_GRANT_VALUE1

Bits	Name	Description
0	CXM_BT_TX_GRANT_VALUE1	This register is used together with CxM_Timer_Counter, CxM_BT_TX_Grant_Enable1, and CxM_BT_TX_Grant_Threshold1. Reset State: 0x00000000

0x3000090 LTE_CXM_CXM_BT_TX_GRANT_ENABLE2

Type: read-write
Reset State: 0x00000000

CxM_BT_TX_Grant_Enable2

LTE_CXM_CXM_BT_TX_GRANT_ENABLE2

Bits	Name	Description
0	CXM_BT_TX_GRANT_VALUE2	This register is used together with CxM_Timer_Counter, CxM_BT_TX_Grant_Enable2, and CxM_BT_TX_Grant_Threshold2. Reset State: 0x00000000

0x3000094 LTE_CXM_CXM_BT_TX_GRANT_THRESHOLD2

Type: read-write
Reset State: 0x00000000

CxM_BT_TX_Grant_Threshold2

LTE_CXM_CXM_BT_TX_GRANT_THRESHOLD2

Bits	Name	Description
31:0	CXM_BT_TX_GRANT_THRESHOLD2	This register is used together with CxM_Timer_Counter, CxM_BT_TX_Grant_Enable2, and CxM_BT_TX_Grant_Value2. Reset State: 0x00000000

0x3000098 LTE_CXM_CXM_BT_TX_GRANT_VALUE2

Type: read-write
Reset State: 0x00000000

CxM_BT_TX_Grant_Value2

LTE_CXM_CXM_BT_TX_GRANT_VALUE2

Bits	Name	Description
0	CXM_BT_TX_GRANT_VALUE2	This register is used together with CxM_Timer_Counter, CxM_BT_TX_Grant_Enable1, and CxM_BT_TX_Grant_Threshold2. Reset State: 0x00000000

0x300009C LTE_CXM_CXM_BT_RX_GRANT_ENABLE1

Type: read-write
Reset State: 0x00000000

CxM_BT_RX_Grant_Enable1

LTE_CXM_CXM_BT_RX_GRANT_ENABLE1

Bits	Name	Description
0	CXM_BT_RX_GRANT_ENABLE1	This register is used together with CxM_Timer_Counter CxM_BT_RX_Grant_Threshold1, and CxM_BT_RX_Grant_Value1 Reset State: 0x00000000

0x30000A0 LTE_CXM_CXM_BT_RX_GRANT_THRESHOLD1

Type: read-write
Reset State: 0x00000000

CxM_BT_RX_Grant_Threshold1

LTE_CXM_CXM_BT_RX_GRANT_THRESHOLD1

Bits	Name	Description
31:0	CXM_BT_RX_GRANT_THRESHOLD1	This register is used together with CxM_Timer_Counter, CxM_BT_RX_Grant_Enable1, and CxM_BT_RX_Grant_Value1. Reset State: 0x00000000

0x30000A4 LTE_CXM_CXM_BT_RX_GRANT_VALUE1

Type: read-write
Reset State: 0x00000000

CxM_BT_RX_Grant_Value1

LTE_CXM_CXM_BT_RX_GRANT_VALUE1

Bits	Name	Description
0	CXM_BT_RX_GRANT_VALUE1	This register is used together with CxM_Timer_Counter, CxM_BT_RX_Grant_Enable1, and CxM_BT_RX_Grant_Threshold1. Reset State: 0x00000000

0x30000A8 LTE_CXM_CXM_BT_RX_GRANT_ENABLE2

Type: read-write
Reset State: 0x00000000

CxM_BT_RX_Grant_Enable2

LTE_CXM_CXM_BT_RX_GRANT_ENABLE2

Bits	Name	Description
0	CXM_BT_RX_GRANT_ENABLE2	This register is used together with CxM_Timer_Counter CxM_BT_RX_Grant_Threshold2, and CxM_BT_RX_Grant_Value2 Reset State: 0x00000000

0x30000AC LTE_CXM_CXM_BT_RX_GRANT_THRESHOLD2

Type: read-write
Reset State: 0x00000000

CxM_BT_RX_Grant_Threshold2

LTE_CXM_CXM_BT_RX_GRANT_THRESHOLD2

Bits	Name	Description
31:0	CXM_BT_RX_GRANT_THRESHOLD2	This register is used together with CxM_Timer_Counter, CxM_BT_RX_Grant_Enable2, and CxM_BT_RX_Grant_Value2. Reset State: 0x00000000

0x30000B0 LTE_CXM_CXM_BT_RX_GRANT_VALUE2

Type: read-write
Reset State: 0x00000000

CxM_BT_RX_Grant_Value2

LTE_CXM_CXM_BT_RX_GRANT_VALUE2

Bits	Name	Description
0	CXM_BT_RX_GRANT_VALUE2	This register is used together with CxM_Timer_Counter, CxM_BT_RX_Grant_Enable2, and CxM_BT_RX_Grant_Threshold2. Reset State: 0x00000000

0x30000B4 LTE_CXM_CXM_BT_RX_TX_GRANT_SEL

Type: read-write
Reset State: 0x00000001

CxM_BT_RX_Grant_sel

LTE_CXM_CXM_BT_RX_TX_GRANT_SEL

Bits	Name	Description
2	CXM_BT_TX_GRANT_SEL	0x0: Cxm_BT_TX_Grant goes to the mux output; 1: WLAN_ACTIVE goes to the mux output S/R by CxM-SW. Reset State: 0x00000000
1:0	CXM_BT_RX_GRANT_SEL	0x0: CxM_BT_RX_Grant_bm OR'ed with wlan_tx_en reaches the mux output. 01: CxM_BT_RX_Grant_bm ORed with mtu_mcu_tx_rx_busy reaches the mux output. 02: CxM_BT_RX_Grant_bm reaches the mux output. 03: not allowed S/R by CxM-SW. Reset State: 0x00000001

0x30000B8 LTE_CXM_CXM_BT_TX_RX_GRANT_EN

Type: read-write
Reset State: 0x00000005

CxM_BT_TX_RX_Grant_en

LTE_CXM_CXM_BT_TX_RX_GRANT_EN

Bits	Name	Description
3	CXM_BT_RX_GRANT_BM_OVERWRITE_VALUE	Override Value for BT RX Grant. Reset State: 0x00000000
2	CXM_BT_RX_GRANT_BM_OVERWRITE_ENABLE	Enable grant override for BT RX Grant. Reset State: 0x00000001
1	CXM_BT_TX_GRANT_BM_OVERWRITE_VALUE	Override Value for BT TX Grant. Reset State: 0x00000000
0	CXM_BT_TX_GRANT_BM_OVERWRITE_ENABLE	Enable grant override for BT TX Grant. Reset State: 0x00000001

0x30000BC LTE_CXM_CXM_CP_INTERRUPT_STROBE_0_START_COUNT

Type: read-write
Reset State: 0x00000000

CxM_Interrupt_Stobe_0_Start_Count

LTE_CXM_CXM_CP_INTERRUPT_STROBE_0_START_COUNT

Bits	Name	Description
31:0	CXM_INTERRUPT_STOBE_0_START_COUNT	When Strobe i is in one-shot mode, stobe i shall generate a one-shot pulse when the CxM_Timer_Counter is equal to CxM_Interrupt_Stobe_i_Start_Count . When Strobe i is in periodic mode, stobe i shall generate a periodic pulse that starts when the CxM_Timer_Counter is equal to CxM_Interrupt_Stobe_i_Start_Count, which the periodicity defined by the following register. S/R by CxM-SW. Reset State: 0x00000000

0x30000C0 LTE_CXM_CXM_CP_INTERRUPT_STROBE_1_START_COUNT

Type: read-write
Reset State: 0x00000000

CxM_Interrupt_Stobe_1_Start_Count

LTE_CXM_CXM_CP_INTERRUPT_STROBE_1_START_COUNT

Bits	Name	Description
31:0	CXM_INTERRUPT_STOBE_1_START_COUNT	When Strobe i is in one-shot mode, stobe i shall generate a one-shot pulse when the CxM_Timer_Counter is equal to CxM_Interrupt_Stobe_i_Start_Count. When Strobe i is in periodic mode, stobe i shall generate a periodic pulse that starts when the CxM_Timer_Counter is equal to CxM_Interrupt_Stobe_i_Start_Count, which the periodicity defined by the following register. S/R by CxM-SW. Reset State: 0x00000000

0x30000C4 LTE_CXM_CXM_CP_INTERRUPT_STROBE_2_START_COUNT

Type: read-write
Reset State: 0x00000000

CxM_Interrupt_Stobe_2_Start_Count

LTE_CXM_CXM_CP_INTERRUPT_STROBE_2_START_COUNT

Bits	Name	Description
31:0	CXM_INTERRUPT_STOBE_2_START_COUNT	When Strobe i is in one-shot mode, stobe i shall generate a one-shot pulse when the CxM_Timer_Counter is equal to CxM_Interrupt_Stobe_i_Start_Count. When Strobe i is in periodic mode, stobe i shall generate a periodic pulse that starts when the CxM_Timer_Counter is equal to CxM_Interrupt_Stobe_i_Start_Count, which the periodicity defined by the following register. S/R by CxM-SW. Reset State: 0x00000000

0x30000C8 LTE_CXM_CXM_CP_INTERRUPT_STROBE_3_START_COUNT

Type: read-write
Reset State: 0x00000000

CxM_Interrupt_Stobe_3_Start_Count

LTE_CXM_CXM_CP_INTERRUPT_STROBE_3_START_COUNT

Bits	Name	Description
31:0	CXM_INTERRUPT_STOBE_3_START_COUNT	When Strobe i is in one-shot mode, stobe i shall generate a one-shot pulse when the CxM_Timer_Counter is equal to CxM_Interrupt_Stobe_i_Start_Count. When Strobe i is in periodic mode, stobe i shall generate a periodic pulse that starts when the CxM_Timer_Counter is equal to CxM_Interrupt_Stobe_i_Start_Count, which the periodicity defined by the following register. S/R by CxM-SW. Reset State: 0x00000000

0x30000DC LTE_CXM_CXM_CP_INTERRUPT_STROBE_0_PERIODICITY

Type: read-write
Reset State: 0x00000000

CxM_Interrupt_Stobe_0_Periodicity

LTE_CXM_CXM_CP_INTERRUPT_STROBE_0_PERIODICITY

Bits	Name	Description
23:0	CXM_INTERRUPT_STOBE_0_PERIODICITY	When Strobe i is in periodic mode, stobe i should generate a strobe with periodicity defined by CxM_Interrupt_Stobe_i_Periodicity. The same clock as the CxM-Timer is used here. S/R by CxM-SW. Reset State: 0x00000000

0x30000E0 LTE_CXM_CXM_CP_INTERRUPT_STROBE_1_PERIODICITY

Type: read-write
Reset State: 0x00000000

CxM_Interrupt_Stobe_1_Periodicity

LTE_CXM_CXM_CP_INTERRUPT_STROBE_1_PERIODICITY

Bits	Name	Description
23:0	CXM_INTERRUPT_STOBE_1_PERIODICITY	When Strobe i is in periodic mode, stobe i should generate a strobe with periodicity defined by CxM_Interrupt_Stobe_i_Periodicity. The same clock as the CxM-Timer is used here. S/R by CxM-SW. Reset State: 0x00000000

0x30000E4 LTE_CXM_CXM_CP_INTERRUPT_STROBE_2_PERIODICITY

Type: read-write
Reset State: 0x00000000

CxM_Interrupt_Stobe_2_Periodicity

LTE_CXM_CXM_CP_INTERRUPT_STROBE_2_PERIODICITY

Bits	Name	Description
23:0	CXM_INTERRUPT_STOBE_2_PERIODICITY	When Strobe i is in periodic mode, stobe i should generate a strobe with periodicity defined by CxM_Interrupt_Stobe_i_Periodicity. The same clock as the CxM-Timer is used here. S/R by CxM-SW. Reset State: 0x00000000

0x30000E8 LTE_CXM_CXM_CP_INTERRUPT_STROBE_3_PERIODICITY

Type: read-write
Reset State: 0x00000000

CxM_Interrupt_Stobe_3_Periodicity. to WCN_PRIORITY

LTE_CXM_CXM_CP_INTERRUPT_STROBE_3_PERIODICITY

Bits	Name	Description
23:0	CXM_INTERRUPT_STOBE_3_PERIODICITY	When Strobe i is in periodic mode, stobe i should generate a strobe with periodicity defined by CxM_Interrupt_Stobe_i_Periodicity. The same clock as the CxM-Timer is used here. S/R by CxM-SW. Reset State: 0x00000000

0x30000EC LTE_CXM_CXM_WCN_PRIORITY_ENABLES

Type: read-write
Reset State: 0x00000010

Following registers are related to WCN_PRIORITY

LTE_CXM_CXM_WCN_PRIORITY_ENABLES

Bits	Name	Description
6	CXM_FRAME_SYNC_SEL	CxM_frame_sync_sel Reset State: 0x00000000

LTE_CXM_CXM_WCN_PRIORITY_ENABLES (cont.)

Bits	Name	Description
5	CXM_WCN_PRIORITY_OVERWRITE_VALUE	CxM_WCN_Priority_overwrite_value Reset State: 0x00000000
4	CXM_WCN_PRIORITY_OVERWRITE_ENABLE	CxM_WCN_Priority_overwrite_enable Reset State: 0x00000001
3	CXM_WCN_PRIORITY_VALUE2	CxM_WCN_Priority_Value2 Reset State: 0x00000000
2	CXM_WCN_PRIORITY_ENABLE2	CxM_WCN_Priority_Enable2 Reset State: 0x00000000
1	CXM_WCN_PRIORITY_VALUE1	CxM_WCN_Priority_Value1 Reset State: 0x00000000
0	CXM_WCN_PRIORITY_ENABLE1	CxM_WCN_Priority_Enable1 Reset State: 0x00000000

0x30000F0 LTE_CXM_CXM_WCN_PRIORITY_THRESHOLD1

Type: read-write
Reset State: 0x00000000

CXM_WCN_Priority_Threshold1

LTE_CXM_CXM_WCN_PRIORITY_THRESHOLD1

Bits	Name	Description
31:0	CXM_WCN_PRIORITY_THRESHOLD1	This register is used together with CxM_WCN_Priority_Enable1, CxM_WCN_Priority_Enable2, CxM_WCN_Priority_Value1, CxM_WCN_Priority_Value2, etc. Reset State: 0x00000000

0x30000F4 LTE_CXM_CXM_WCN_PRIORITY_THRESHOLD2

Type: read-write
Reset State: 0x00000000

CXM_WCN_Priority_Threshold2

LTE_CXM_CXM_WCN_PRIORITY_THRESHOLD2

Bits	Name	Description
31:0	CXM_WCN_PRIORITY_THRESHOLD2	This register is used together with CxM_WCN_Priority_Enable1, CxM_WCN_Priority_Enable2, CxM_WCN_Priority_Value1, CxM_WCN_Priority_Value2, etc. Reset State: 0x00000000

0x30000F8 LTE_CXM_CXM_LTE_ACTIVE_FRAME_SYNC_VALUE

Type: read-only
Reset State: 0x00000000

This register "polls" the frame_sync input and LTE_active input values.

LTE_CXM_CXM_LTE_ACTIVE_FRAME_SYNC_VALUE

Bits	Name	Description
1	I_RIVA_LTE_ACTIVE	This register captures the i_riva_lte_active input signal value. Reset State: 0x00000000
0	I_RIVA_LTE_FRAME_SYNC	This register captures the i_riva_lte_frame_sync input signal value. Reset State: 0x00000000

16.2.11 AGC

0x3000000 AGC_AGC_RESET

Type: read-write
Reset State: 0x0001

Soft reset of the AGC state machine.

AGC_AGC_RESET

Bits	Name	Description
0	RESET	Reset bit. 0x0: NORMAL 0x1: RESET Reset State: 0x0001

0x3000004 AGC_DIS_MODE

Type: read-write
Reset State: 0x0000

Disables detection of OFDM (11a,11g)/OFDM-MIMO, Barker/CCK (11b) packets or double bandwidth 11a/MIMO packets. Useful to reduce misdetect probability in a pure 11a or 11b environment.

AGC_DIS_MODE

Bits	Name	Description
3	DISABLE_11AC80	Disable quadruple bandwidth bit for 11ac80 MHz packets. 0x0: ENABLE 0x1: DISABLE Reset State: 0x0000
2	DISABLE_11N40	Disable double bandwidth bit for 11n40 MHz packets. 0x0: ENABLE 0x1: DISABLE Reset State: 0x0000
1	DISABLE_11B	Disable 11b bit. 0x0: ENABLE 0x1: DISABLE Reset State: 0x0000
0	DISABLE_11AG	Disable 11a/g bit. 0x0: ENABLE 0x1: DISABLE Reset State: 0x0000

0x3000008 AGC_RX_OVERRIDE

Type: read-write
Reset State: 0x0000

This register allows the EN_RX (Receive Enable) outputs of the BBIC, the standby input and the powerdown inputs of the built-in ADC to be software- controlled. These outputs are used to enable the AD converters and RF ASICs for debugging and calibration purposes. The power down bits are used to put all of the ADCs in power down mode (for instance in beacon power save mode) or part of its ADCs to be powered down (for instance a product not using all of the antenna).

AGC_RX_OVERRIDE

Bits	Name	Description
4:4	ENRX_VAL	Enable values for receive chain 0 to 0. For these values to take effect, the corresponding override bits should be set. Reset State: 0x0000

AGC_RX_OVERRIDE (cont.)

Bits	Name	Description
0:0	STBY_VAL	ADC standby values for receive chain 0 to 0. Note that the standby values are asserted low, and de-asserted high. For these values to take effect, the corresponding override bits should be set. Reset State: 0x0000

0x300000C AGC_PHY_LOOPBACK

Type: read-write
Reset State: 0x0008

Configures support for PHY loopback.

AGC_PHY_LOOPBACK

Bits	Name	Description
3	DIG_LOOPBACK	Enables the loopback digitally. Reset State: 0x0001
2	PMI_EN	Enables loop backed data to go out the PMI to the MAC. Reset State: 0x0000
1:0	MODE	Sets the PHY loopback mode. PHY loopback can be enabled statically, where it is always in loopback mode, or dynamically where it only enters loopback mode when we're transmitting. 0x0: DISABLED 0x1: STATIC_EN 0x2: DYN_EN Reset State: 0x0000

0x3000010 AGC_CONFIG_XBAR

Type: read-write
Reset State: 0x0000

Sets the configuration for the digital / analog crossbar. This will configure how a particular analog receive chain is mapped to a particular digital RX processing chain. In addition, it will also configure how a particular digital TX processing chain is connected to a particular analog transmit chain. An analog chain includes the baseband analog + the corresponding RF chain. Although there are separate controls for txxbar and rxxbar, for normal mode of operation, they should be set the same. Please refer to the System Engineering Specification on the edge portal for the configuration and connectivity of xbar. Note that no analog chain other than analog chain 2 can feed the digital chain 2 and hence there is no xbar functionality on digital chain 2

AGC_CONFIG_XBAR

Bits	Name	Description
15	PHYDBG_SEL	PHYDBG input select. Used for playing PHYDBG data into RX ADC path. Reset State: 0x0000
14	IQSWAP_EN	Enables swapping of the I and Q rails of the ADC. Reset State: 0x0000

0x3000014 AGC_CW_DETECT

Type: read-write
Reset State: 0x000B

At packet detection, the PHY detects narrowband interference to avoid false alarms caused by narrowband interference. This type of interference could arise as the result of LO leakage, LO interference of other IEEE802.11 devices in the vicinity of the receiver and other, intentional radiators, such as Bluetooth devices. of factors the explanation of which is beyond the scope of this guide. When CW is found the packet detection is ignored since it is most likely that the packet detectors triggered on the CW interference. The CW frequency is used to set a CW notch filter inside the RXFIR to cancel out that interference in the future, until a different CW interferer is found or until a timer expires.

AGC_CW_DETECT

Bits	Name	Description
6	CW_EN_RXB_DATA	Enables CW notch processing when the AGC is in states 9 or 11. 0x0: DISABLE 0x1: ENABLE Reset State: 0x0000
5	CW_EN_RXB	Enables CW notch processing when the AGC is in states 2,3 or 7. 0x0: DISABLE 0x1: ENABLE Reset State: 0x0000
4	CW_EN_RXA_DATA	Enables CW notch processing when the AGC is in states 8 or 10. 0x0: DISABLE 0x1: ENABLE Reset State: 0x0000
3	CW_EN_RXA	Enables CW notch processing when the AGC is in states 2,3 or 6. 0x0: DISABLE 0x1: ENABLE Reset State: 0x0001

AGC_CW_DETECT (cont.)

Bits	Name	Description
2	DC_DIS	Disables the use of the Rxfir with a DC notch. Note that this bit field should be set in conjunction with the RACTL's rxfir_scaling_coeff register. 0x0: ENABLE 0x1: DISABLE Reset State: 0x0000
1	RADAR_DETECT_DIS	0x1: DISABLE 0x0: ENABLE Reset State: 0x0001
0	PKT_DETECT_DIS	0x1: DISABLE 0x0: ENABLE Reset State: 0x0001

0x3000018 AGC_CW_NOTCH_TIMEOUT

Type: read-write
Reset State: 0x0064

The CW notch filter applies a notch to the receiver input signal at a frequency as measured by the CW detector. The notch is applied until the CW detector passes a different value to the notch filter, or until the notch filter's built-in timer expires. When this timer expires the input signal bypasses the notch filter altogether. The timeout value of the timer is defined in this register.

AGC_CW_NOTCH_TIMEOUT

Bits	Name	Description
8	DIS	Setting this field to 1 is equivalent to setting an infinite timeout value. When set, the cw notch index will remain the same until is set to a different value. Reset State: 0x0000
7:0	VAL	Timeout value. This value is multiplied by 2^19 to get the number of 80 MHz clock cycles that make up the timeout time. 0x1: MINIMUM 0x64: DEFAULT 0xFF: MAXIMUM Reset State: 0x0064

0x300001C AGC_GAIN_MODE

Type: read-write
Reset State: 0x0000

AGC_GAIN_MODE

Bits	Name	Description
1	MULT_STEP	This bit defines if only a single COARSE_STEP or SAT_STEP is made or if multiple steps are possible. 0x0: SING 0x1: MULT Reset State: 0x0000
0	USE_RXFIR_PWR	Setting this field to 1 will cause the gain computation to come from the power measured in the RXFIR power detector instead of the ADC power detector. Reset State: 0x0000

0x3000020 AGC_TESTBUS

Type: read-write
Reset State: 0x0000

Selects the inputs to the test bus.

AGC_TESTBUS

Bits	Name	Description
5:0	AGC_RXTMUX_TMUXSEL	RX test multiplexer select lines. 0x0: AGC_40_0 0x1: AGC_40_1 0x2: AGC_40_2 0x3: AGC_40_3 0x8: AGC_80_0 0x9: AGC_80_1 0xA: AGC_80_2 0xB: AGC_80_3 0xC: AGC_80_4 0xD: AGC_80_5 0xE: AGC_80_6 0x18: AGC_80_40_0 0x19: AGC_80_40_1 0x1A: AGC_80_40_2 0x1B: AGC_80_40_3 0x1C: AGC_80_40_4 0x1D: AGC_80_40_5 0x20: RXB_40_0 0x21: RXB_40_1 0x22: RXB_40_2 0x23: RXB_40_3 0x24: RXB_40_4 0x25: RXB_40_5 0x26: RXB_40_6 0x27: RXB_40_7 Reset State: 0x0000

0x3000024 AGC_GAINSET0

Type: read-write
Reset State: 0x0000

Allows to break AGC gain setting loop and manually override AGC setting of chain 0. For debugging purposes.

AGC_GAINSET0

Bits	Name	Description
7	OVERRIDE	Override bit. 0x0: NORMAL 0x1: OVERRIDE Reset State: 0x0000

AGC_GAINSET0 (cont.)

Bits	Name	Description
6:0	GAIN	Gain setting. Reset State: 0x0000

0x3000028 AGC_GAINSET_WRITE

Type: command
Reset State: 0x0000

When a 1 is written to this register, the gain registers of the RFIC(s) are loaded with the values stored in bit [3:0] of registers GAINSET0.. 0, provided that the override bit [4] these registers is set. At the moment that these registers are written, the gain that is programmed in the RFIC receivers will remain at its previously programmed value. Writing to this register enforces a write of the gain values to the RFIC gain registers, which would otherwise happen only when the AGC decides to change gain when a packet is received or a strong signal clips the RF front end, or when the AGC is reset (through RX_RESET signal, SLEEP signal, packet transmission or by writing to AGC_RESET register. On the chains on which the override bit is not set, the current gain remains unchanged. This register is provided for debugging purposes. This register cannot be read back

AGC_GAINSET_WRITE

Bits	Name	Description
0	OVERRIDE	Gain write pulse bit. 0x0: NORMAL 0x1: OVERRIDE Reset State: 0x0000

0x300002C AGC_STAT_CTRL

Type: read-write
Reset State: 0x0001

Control for AGC specific stat info

AGC_STAT_CTRL

Bits	Name	Description
0	RSSI_TYPE	0x0: ADC 0x1: RXFIR Reset State: 0x0001

0x3000030 AGC_SUBBAND_CONFIG

Type: read-write
Reset State: 0x0000

Sets subband configuration.

AGC_SUBBAND_CONFIG

Bits	Name	Description
3:2	STG3_SUBBAND	Selects the subband location for the stage 3 RxFIR filter. 0x0: LOWER 0x1: UPPER 0x2: CENTER 0x3: RESERVED Reset State: 0x0000
1:0	STG2_SUBBAND	Selects the subband location for the stage 2 RxFIR filter. 0x0: LOWER 0x1: UPPER 0x2: CENTER 0x3: RESERVED Reset State: 0x0000

0x3000034 AGC_CHANNEL_FREQ

Type: read-write
Reset State: 0x096C

This stores the channel frequency in MHz is stored used to calculate re-sampler offset for 11b operation. This register needs to be reprogrammed every time the MAC switches to a different RF channel. Width is 13 bits, so 11b mode can also operate in 5 GHz band, if the need arises.

AGC_CHANNEL_FREQ

Bits	Name	Description
12:0	FREQ	Channel frequency 0x96C: CH1 0x971: CH2 0x976: CH3 0x97B: CH4 0x980: CH5 0x985: CH6 0x98A: CH7 0x98F: CH8 0x994: CH9 0x999: CH10 0x99E: CH11 0x9A3: CH12 0x9A8: CH13 0x9B4: CH14 Reset State: 0x096C

0x3000038 AGC_N_ACTIVE

Type: read-write
Reset State: 0x0001

Specifies number of receive chains used to receive a packet.

AGC_N_ACTIVE

Bits	Name	Description
0:0	NUMBER	Receive chains. Reset State: 0x0001

0x300003C AGC_N_LISTEN

Type: read-write
Reset State: 0x0011

Specifies number of receive chains used to listen for a packet.

AGC_N_LISTEN

Bits	Name	Description
4:4	RF_ANT_EN	If number of listen chains is 0, then this specifies which RF antennas to enable during listen mode. Reset State: 0x0001
0:0	NUMBER	Listen chains. Reset State: 0x0001

0x3000040 AGC_N_MEASURE

Type: read-write
Reset State: 0x0001

Specifies number of receive chains that is switched on to measure power on.

AGC_N_MEASURE

Bits	Name	Description
0:0	NUMBER	Measure chains. Reset State: 0x0001

0x3000044 AGC_N_CAPTURE

Type: read-write
Reset State: 0x0011

Specifies number of receive chains used to capture a packet.

AGC_N_CAPTURE

Bits	Name	Description
4:4	RF_ANT_EN	If number of capture chains is 0, then this specifies which RF antennas to enable during capture mode. Reset State: 0x0001
0:0	NUMBER	Receive chains. Reset State: 0x0001

0x3000048 AGC_CCA_MODE

Type: read-write
Reset State: 0x0B6D

Determines how the CCA signal from the PHY to the MAC is generated.

AGC_CCA_MODE

Bits	Name	Description
11:9	SB3	Clear Channel Assessment Mode for channel subband 3 0x0: CLEAR 0x1: BUSY 0x2: GI 0x3: ED_OR_GI 0x4: GI_OR_CS_AND_CD 0x5: ED_OR_GI_AND_CS_AND_CD Reset State: 0x0005
8:6	SB2	Clear Channel Assessment Mode for channel subband 2 0x0: CLEAR 0x1: BUSY 0x2: GI 0x3: ED_OR_GI 0x4: GI_OR_CS_AND_CD 0x5: ED_OR_GI_AND_CS_AND_CD Reset State: 0x0005
5:3	SB1	Clear Channel Assessment Mode for channel subband 1 0x0: CLEAR 0x1: BUSY 0x2: GI 0x3: ED_OR_GI 0x4: GI_OR_CS_AND_CD 0x5: ED_OR_GI_AND_CS_AND_CD Reset State: 0x0005
2:0	SB0	Clear Channel Assessment Mode for channel subband 0 0x0: CLEAR 0x1: BUSY 0x2: GI 0x3: ED_OR_GI 0x4: GI_OR_CS_AND_CD 0x5: ED_OR_GI_AND_CS_AND_CD Reset State: 0x0005

0x300004C AGC_CCA_GI_DET_CFG

Type: read-write
Reset State: 0x5FBF

AGC_CCA_GI_DET_CFG

Bits	Name	Description
14:8	TH_SGI	Reset State: 0x005F
7:1	TH_LGI	Reset State: 0x005F
0	DIS	Reset State: 0x0001

0x3000050 AGC_TH_CD20

Type: read-write
Reset State: 0x0000

If the 11a or 11b packet correlator detects a packet and the RSSI on receive Chain 0 exceeds this threshold, then the carrier detect flag is set. Depending on the value of the CCA mode register this determines the behavior of the CCA signal from the PHY to the MAC. Value 8'hff is used to disable this check.

AGC_TH_CD20

Bits	Name	Description
6:0	TH	CD Threshold. Default value (0 = -?? dB below max level). Reset State: 0x0000

0x3000054 AGC_TH_CD40

Type: read-write
Reset State: 0x0000

If the 11a or 11b packet correlator detects a packet and the RSSI on receive Chain 0 exceeds this threshold, then the carrier detect flag is set. Depending on the value of the CCA mode register this determines the behavior of the CCA signal from the PHY to the MAC. Value 8'hff is used to disable this check.

AGC_TH_CD40

Bits	Name	Description
6:0	TH	CD Threshold. Default value (0 = -?? dB below max level). Reset State: 0x0000

0x3000058 AGC_TH_CD80

Type: read-write
Reset State: 0x0000

If the 11a or 11b packet correlator detects a packet and the RSSI on receive Chain 0 exceeds this threshold, then the carrier detect flag is set. Depending on the value of the CCA mode register this determines the behavior of the CCA signal from the PHY to the MAC. Value 8'hff is used to disable this check.

AGC_TH_CD80

Bits	Name	Description
6:0	TH	CD Threshold. Default value (0 = -?? dB below max level). Reset State: 0x0000

0x300005C AGC_TH_CS20

Type: read-write
Reset State: 0x0012

If the 11a or 11b packet correlator detects a packet and the RSSI on receive Chain 0 exceeds the carrier detect threshold, and the received energy also exceeds the carrier sense threshold, then the carrier sense flag is set. Depending on the value of the CCA mode register this determines the behavior of the CCA signal from the PHY to the MAC. Value 8'hff is used to disable this check.

AGC_TH_CS20

Bits	Name	Description
6:0	TH	CS Threshold Default value (-82 dBm) Reset State: 0x0012

0x3000060 AGC_TH_CS40

Type: read-write
Reset State: 0x0012

If the 11a or 11b packet correlator detects a packet and the RSSI on receive Chain 0 exceeds the carrier detect threshold, and the received energy also exceeds the carrier sense threshold, then the carrier sense flag is set. Depending on the value of the CCA mode register this determines the behavior of the CCA signal from the PHY to the MAC. Value 8'hff is used to disable this check.

AGC_TH_CS40

Bits	Name	Description
6:0	TH	CS Threshold Default value (-82 dBm) Reset State: 0x0012

0x3000064 AGC_TH_CS80

Type: read-write
Reset State: 0x0012

If the 11a or 11b packet correlator detects a packet and the RSSI on receive Chain 0 exceeds the carrier detect threshold, and the received energy also exceeds the carrier sense threshold, then the carrier sense flag is set. Depending on the value of the CCA mode register this determines the behavior of the CCA signal from the PHY to the MAC. Value 8'hff is used to disable this check.

AGC_TH_CS80

Bits	Name	Description
6:0	TH	CS Threshold Default value (-82 dBm) Reset State: 0x0012

0x3000068 AGC_TH_EDET

Type: read-write
Reset State: 0x2626

If the RSSI on receive chain 0 exceeds this threshold then the energy detect flag is set. Depending on the value of the CCA mode register this determines the behavior of the CCA signal from the PHY to the MAC. Value 8'hff is used to disable this check.

AGC_TH_EDET

Bits	Name	Description
14:8	TH20	ED Threshold. Default value (-62 dBm) Reset State: 0x0026
6:0	TH40	ED Threshold. Default value (-62 dBm) Reset State: 0x0026

0x300006C AGC_D_AGC_A

Type: read-write
Reset State: 0x000A

This latency is the sum of three components. The ADC latency, the latency through the FIR and CAL module and the latency for AGC 11a processing, which is determined by interference locator processing latency. Ranges from 0 to 1.575 micro seconds.

AGC_D_AGC_A

Bits	Name	Description
5:0	DELAY	Propagation time in 80/40MHz dynamic clocks. Reset State: 0x000A

0x3000070 AGC_D_AGC_B

Type: read-write
Reset State: 0x0006

This latency is the sum of two components. The ADC latency, and the latency through the FIR and CAL module. Ranges from 0 to 1.575 micro seconds.

AGC_D_AGC_B

Bits	Name	Description
5:0	DELAY	Propagation time in 50ns units. Default value is 6, corresponding to 300ns. Reset State: 0x0006

0x3000074 AGC_RSSI_OFFSET0

Type: read-write
Reset State: 0x003A

This register holds an offset value (determined at manufacturing time) that is used to translate rssi values to dBm values as measured at the antenna input. The same offset is used to correct both the ADC and FIR RSSI.

AGC_RSSI_OFFSET0

Bits	Name	Description
7:0	OFFSET	Offset is a 2cc encoded number that is added to the rssi computed by the power module. Reset State: 0x003A

0x3000078 AGC_RSSI_BT_OFFSET0

Type: read-write
Reset State: 0x0000

When a Bluetooth transmission takes place the RSSI on one of the receive antennae is reduced. This register is used to compensate for that attenuation change so that the reported RSSI is the true dBm number at the antenna.

AGC_RSSI_BT_OFFSET0

Bits	Name	Description
7:0	OFFSET	Offset is a 2cc encoded number that is added to the rssi computed by the power module. Reset State: 0x0000

0x300007C AGC_CLIP_COUNT

Type: write-only

Debug Counter. Counts transitions between CORR state and GAIN_SETTLE state due to ADC clip events.

AGC_CLIP_COUNT

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x3000080 AGC_SAT_COUNT

Type: write-only

Debug Counter. Counts transitions between CORR state and GAIN_SETTLE state due to RF sat events.

AGC_SAT_COUNT

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x3000084 AGC_PIP_COUNT

Type: write-only

Debug Counter. Counts the number of packet in packet detection (power_jum_det during some of the states)

AGC_PIP_COUNT

Bits	Name	Description
7:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x3000088 AGC_NOT_AVALID_20M_COUNT

Type: write-only

BTCF not_avalid signal

AGC_NOT_AVALID_20M_COUNT

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x300008C AGC_NOT_AVALID_40M_COUNT

Type: write-only

BTCF not_avalid signal

AGC_NOT_AVALID_40M_COUNT

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x3000090 AGC_RXA_HDR_INVALID_20M_COUNT

Type: write-only

BTCF not_avalid signal

AGC_RXA_HDR_INVALID_20M_COUNT

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x3000094 AGC_RXA_HDR_INVALID_40M_COUNT

Type: write-only

BTCF not_avalid signal

AGC_RXA_HDR_INVALID_40M_COUNT

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x3000098 AGC_RXB_NO_B_PKT_DET_COUNT

Type: write-only

AGC_RXB_NO_B_PKT_DET_COUNT

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x300009C AGC_RXB_INV_HDR_COUNT

Type: write-only

AGC_RXB_INV_HDR_COUNT

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30000A0 AGC_RXB_ILL_HDR_COUNT

Type: write-only

AGC_RXB_ILL_HDR_COUNT

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30000A4 AGC_COARSE_DCO_UPDATE_COUNTER

Type: write-only

AGC_COARSE_DCO_UPDATE_COUNTER

Bits	Name	Description
7:0	VALUE	Coarse DCO measurement update counter.

0x30000A8 AGC_FALSE_AC_ABORT_COUNT

Type: write-only

Counts number of aborts of legacy packets that occur due to clip events in potential VHT-STS.

AGC_FALSE_AC_ABORT_COUNT

Bits	Name	Description
7:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30000AC AGC_LATE_AC_DET_COUNT

Type: write-only

Counts number of late 11AC detects that cause missed VHT-STS gain commands.

AGC_LATE_AC_DET_COUNT

Bits	Name	Description
7:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30000B0 AGC_CCA_PKTDET_STATUS

Type: read-only

Samples the current value of the CCA and pktdet flags

AGC_CCA_PKTDET_STATUS

Bits	Name	Description
6	LSIG_TXOP	
5	EARLY_PKTDET_N	
4	PKTDET_N	
3:0	CCA	

0x30000B4 AGC_SAMPLE_ADC_I0

Type: read-only

AGC_SAMPLE_ADC_I0

Bits	Name	Description
11	OVFL	Overflow bit. 0x0: NO_OVFL 0x1: OVFL
10:0	ADC	ADC output, offset binary encoded ADC Chain 0 i output.

0x30000B8 AGC_SAMPLE_ADC_Q0

Type: read-only

AGC_SAMPLE_ADC_Q0

Bits	Name	Description
11	OVFL	Overflow bit. 0x0: NO_OVFL 0x1: OVFL
10:0	ADC	ADC output, offset binary encoded ADC Chain 0 q output.

0x30000BC AGC_ADC_RSSI0

Type: read-only

Read out RSSI measured right after ADC0 while not receiving a packet. Invalid bit indicates that RSSI is not current, since a packet is being received. The value is the RSSI stored just before the AGC detected the packet.

AGC_ADC_RSSI0

Bits	Name	Description
8	NAV_BUSY	NAV status which helps software to allow/ignore the sampled rssi value for 11k measurements. 0x0: IDLE 0x1: BUSY
7	INVALID	RSSI0 not current 0x0: VALID 0x1: INVALID
6:0	RSSI	RSSI measurement on Chain 0 ranging from 0 (lowest RSSI) to 113 (highest RSSI), measured in dB.

0x30000C0 AGC_FIR_RSSI0

Type: read-only

Read out RSSI measured after FIR while not receiving a packet. Invalid bit indicates that RSSI is not current, since a packet is being received. The value is the RSSI stored just before the AGC detected the packet.

AGC_FIR_RSSI0

Bits	Name	Description
8	NAV_BUSY	NAV status which helps software to allow/ignore the sampled rssi value for 11k measurements. 0x0: IDLE 0x1: BUSY
7	INVALID	RSSI0 not current 0x0: VALID 0x1: INVALID
6:0	RSSI	RSSI measurement on Chain 0 ranging from 0 (lowest RSSI) to 113 (highest RSSI), measured in dB.

0x30000C4 AGC_COARSE_DCO_CHAIN0_REAL

Type: read-only
Reset State: 0x0000

This register stores the measured DC offset value from the AGC_POWER module if the value exceeds the th_dco_cal parameter during CORR state and (rx_gain == INIT_GAIN)

AGC_COARSE_DCO_CHAIN0_REAL

Bits	Name	Description
9:0	VALUE	Value of DC offset on the real component of chain 0 measured by the AGC_POWER module Reset State: 0x0000

0x30000C8 AGC_COARSE_DCO_CHAIN0_IMAG

Type: read-only
Reset State: 0x0000

This register stores the measured DC offset value from the AGC_POWER module if the value exceeds the th_dco_cal parameter during CORR state and (rx_gain == INIT_GAIN)

AGC_COARSE_DCO_CHAIN0_IMAG

Bits	Name	Description
9:0	VALUE	Value of DC offset on the imag component of chain 0 measured by the AGC_POWER module Reset State: 0x0000

0x30000CC AGC_INIT_GAIN

Type: read-write
Reset State: 0x0046

Initial gain setting in 1dB steps.

AGC_INIT_GAIN

Bits	Name	Description
6:0	GAIN	Gain setting in 1dB steps. Reset State: 0x0046

0x30000D0 AGC_MAX_GAIN

Type: read-write
Reset State: 0x0046

maximum gain that can be commanded to RF ASIC.

AGC_MAX_GAIN

Bits	Name	Description
6:0	GAIN	For RFIC operation the 7 bits denote 1 dB steps. Reset State: 0x0046

0x30000D4 AGC_GAIN_OFFSET0

Type: read-write
Reset State: 0x0000

receiver gain offset in 1dB steps per chain

AGC_GAIN_OFFSET0

Bits	Name	Description
4:0	VAL	Reset State: 0x0000

0x30000D8 AGC_TR_SW_GAIN_THRESH0

Type: read-write
Reset State: 0x0000

The T/R switch is driven to transmit mode whenever the commanded gain index is below this threshold. Setting this to 0 effectively disables this.

AGC_TR_SW_GAIN_THRESH0

Bits	Name	Description
6:0	GAIN	Reset State: 0x0000

0x30000DC AGC_SAT_STEP

Type: read-write
Reset State: 0x0070

The sat_step field is used to specify the step used to gain the RF Front end down if the RF is saturated. The same value is used to step up the gain if the signal energy is below TH_NO_SIGNAL. This gain step is specified in multiples of 2dB from 0 dB to 128 dB. The enable field is used to switch this functionality on or off.

AGC_SAT_STEP

Bits	Name	Description
7	IGNORE_ADC_CLIP	Normally, a sat step is only taken if a digital (or ADC) clip is also seen at the same time, but if you set this bit to 1, then only the RF sat flag is used. Reset State: 0x0000
6	SAT_STEP_EN	Allow AGC to make gain step when in Vega mode RF front end is in saturation. 0x0: DISABLE 0x1: ENABLE Reset State: 0x0001
5:0	SAT_STEP	Coarse gain step. Default value is 25, or 50dB step for Vega mode Reset State: 0x0030

0x30000E0 AGC_COARSE_STEP_HT

Type: read-write
Reset State: 0x0514

Coarse gain step. Used to step gain down if one chain's ADCs clip. Used to step up if the signal energy is below TH_NO_SIGNAL. Specified in multiples of 4dB steps, from 0 dB to 60 dB.

AGC_COARSE_STEP_HT

Bits	Name	Description
14	VHT_STS_FINE_GAIN_SET_DIS	Enable VHT-STS fine gain setting 0x1: DISABLE 0x0: ENABLE Reset State: 0x0000
13	VHT_STS_COARSE_GAIN_SET_DIS	Enable VHT-STS coarse gain setting 0x1: DISABLE 0x0: ENABLE Reset State: 0x0000
12	HT_STS_GAIN_SET_DIS	Enable HT-STS gain setting 0x1: DISABLE 0x0: ENABLE Reset State: 0x0000
11:6	VHTSTS_STEP	Coarse gain step for 2nd STF in mixed mode packets. Reset State: 0x0014
5:0	HTSTS_STEP	Coarse gain step. Reset State: 0x0014

0x30000E4 AGC_COARSE_STEP

Type: read-write
Reset State: 0x0056

Coarse gain step. Used to step gain down if one chain's ADCs clip. Used to step up if the signal energy is below TH_NO_SIGNAL. Specified in multiples of 4dB steps, from 0 dB to 60 dB.

AGC_COARSE_STEP

Bits	Name	Description
6	COARSE_STEP_EN	Allow AGC to make coarse gain step when digital clip is detected. 0x0: DISABLE 0x1: ENABLE Reset State: 0x0001
5:0	COARSE_STEP	Coarse gain step. Reset State: 0x0016

0x30000E8 AGC_MAX_POWER_DIFF

Type: read-write
Reset State: 0x0004

The value in this register specifies maximum power difference. If the received power on all any antenna is this much less than the power on the strongest antenna, then the AGC limits the gain for the chain with the less power to that corresponding with a power of the strongest power minus the value in this register. This threshold avoids gaining up receive chains with weak signal and thereby blowing up noise. antenna.

AGC_MAX_POWER_DIFF

Bits	Name	Description
3:0	DIFFERENCE	Maximum power difference in 4 dB steps. From 0.. 14*4=56 dB Reset State: 0x0004

0x30000EC AGC_TARGET_BO_ACTIVE

Type: read-write
Reset State: 0x0020

Target Backoff for Listen chains. The gain is set this amount of dBs below the gain that would fully saturate the receiver. The backoff is specified in 0.5 dB steps.

AGC_TARGET_BO_ACTIVE

Bits	Name	Description
5:0	BACK_OFF	Backoff value. Default backoff is 32, or 16 dB. Reset State: 0x0020

0x30000F0 AGC_TARGET_BO_INACTIVE

Type: read-write
Reset State: 0x0024

Target Backoff for Receive chains, that are not listen chains. The gain is set this amount of dBs below the gain that would fully saturate the receiver. This backoff is typically higher than that of listen antennas to accommodate the unknown up-fading on the inactive receive chains. The backoff is specified in 0.5 dB steps.

AGC_TARGET_BO_INACTIVE

Bits	Name	Description
5:0	BACK_OFF	Backoff value. Default backoff is 36, i.e., 18 dB. Reset State: 0x0024

0x30000F4 AGC_TH_CLIP_HIGH

Type: read-write
Reset State: 0x0734

If the output of any of the ADCs is greater than this value the clip flag of the corresponding ADC is asserted.

AGC_TH_CLIP_HIGH

Bits	Name	Description
10:0	THRESHOLD	Clip threshold in offset binary. Example: if the 2's complement threshold is 400(0x190), then the 11-bit offset binary code is 400 + 1024 = 1424, +800 corresponds to 1824 Reset State: 0x0734

0x30000F8 AGC_TH_CLIP_LOW

Type: read-write
Reset State: 0x00CC

If the output of any of the ADCs is less than this value the clip flag of the corresponding ADC is asserted.

AGC_TH_CLIP_LOW

Bits	Name	Description
10:0	THRESHOLD	Clip threshold in offset binary. Example: if the 2's complement threshold is -400, then the 11-bit offset binary code is -400 + 1024 = 624. -800 corresponds to 224 Reset State: 0x00CC

0x30000FC AGC_TH_SIGNAL_HIGH

Type: read-write
Reset State: 0x00B4

AGC compares power with this threshold. If power is higher, a coarse gain reduction is done. In steps of 16384 (2^14).

AGC_TH_SIGNAL_HIGH

Bits	Name	Description
7:0	THRESHOLD	Power threshold. Default value 110 (1802240). Reset State: 0x00B4

0x3000100 AGC_TH_SIGNAL_LOW

Type: read-write
Reset State: 0x0050

AGC compares power with this threshold. If power is lower, a coarse gain reduction is done if the ADCs clip. Specified in steps of 1024 (2^10).

AGC_TH_SIGNAL_LOW

Bits	Name	Description
7:0	THRESHOLD	Power threshold. Default value 60 (61440). Reset State: 0x0050

0x3000104 AGC_TH_HTSTS_CLIP

Type: read-write
Reset State: 0x006E

Minimum ADC power during HT-STS needed for clip detection.

AGC_TH_HTSTS_CLIP

Bits	Name	Description
7:0	THRESHOLD	Power threshold. Default value 110 (1802240). Reset State: 0x006E

0x3000108 AGC_TH_VHTSTS_CLIP

Type: read-write
Reset State: 0x006E

Minimum ADC power during VHT-STS needed for clip detection.

AGC_TH_VHTSTS_CLIP

Bits	Name	Description
7:0	THRESHOLD	Power threshold. Default value 110 (1802240). Reset State: 0x006E

0x300010C AGC_TH_POWER_CLIP

Type: read-write
Reset State: 0x003F

Used to do extra gain reduction if an antenna is clipping, but there is no time to do a coarse step.

AGC_TH_POWER_CLIP

Bits	Name	Description
5:0	THLD	Power clip threshold. Reset State: 0x003F

0x3000110 AGC_SAT_DELAY

Type: read-write
Reset State: 0x000A

AGC_SAT_DELAY

Bits	Name	Description
5:0	TIME	Reset State: 0x000A

0x3000114 AGC_CLIP_WINDOW

Type: read-write
Reset State: 0x0000

AGC_CLIP_WINDOW

Bits	Name	Description
11:6	THRESHOLD	Threshold for the minimum number of clips needed in the window for a true clip to be detected. Reset State: 0x0000
5:0	TIME	Window size in 80MHz clocks that clips are monitored. Reset State: 0x0000

0x3000118 AGC_TH_NO_SIGNAL

Type: read-write
Reset State: 0x0001

Decision Threshold for absence of signal energy, which will result in the AGC stepping up the gain, if it is not already at its maximum setting.

AGC_TH_NO_SIGNAL

Bits	Name	Description
7:0	THRESHOLD	Detection threshold. Default value 1. Reset State: 0x0001

0x300011C AGC_TH_DCO_CAL

Type: read-write
Reset State: 0x000A

This register holds the RSSI threshold to trigger capture of the DCO value measured by AGC_POWER during CORR state

AGC_TH_DCO_CAL

Bits	Name	Description
6:0	THLD	Coarse DCO measurement threshold. Reset State: 0x000A

0x3000120 AGC_DET_DATA_SHIFT

Type: read-write
Reset State: 0x0005

Right shift the data by this amount

AGC_DET_DATA_SHIFT

Bits	Name	Description
3:2	DET11A	Right shift the det11a detector input by this amount Reset State: 0x0001
1:0	DET11B	Right shift the det11b detector input by this amount Reset State: 0x0001

0x3000124 AGC_TH_RXB_PWR_HIGH

Type: read-write
Reset State: 0x0005

This threshold is used to by the AGC to set the digital AGC shift value for det11b and RXB.

AGC_TH_RXB_PWR_HIGH

Bits	Name	Description
5:0	THLD	11B Digital AGC power setting threshold. Reset State: 0x0005

0x3000128 AGC_TH_CW_LOW

Type: read-write
Reset State: 0x0020

The CW detect threshold is set to this value if non of the RSSI values exceeds the th_cw_rssi threshold.

AGC_TH_CW_LOW

Bits	Name	Description
7:0	THRESHOLD	CW detect threshold. Reset State: 0x0020

0x300012C AGC_TH_CW_HIGH

Type: read-write
Reset State: 0x00C8

The CW interference detect threshold is set to this value if one or more of the RSSI values exceeds the th_cw_rssi threshold.

AGC_TH_CW_HIGH

Bits	Name	Description
7:0	THRESHOLD	CW detect threshold. Reset State: 0x00C8

0x3000130 AGC_TH_CW_RSSI

Type: read-write
Reset State: 0x000E

If one of the RSSI values exceeds this threshold, the cd detect threshold is set to th_cw_high. Otherwise the CW detect threshold is set to the_cw_low. The CW detect threshold is updated when an RXA packet or an RXB packet is received.

AGC_TH_CW_RSSI

Bits	Name	Description
6:0	THRESHOLD	RSSI threshold. Reset State: 0x000E

0x3000134 AGC_CW_MODE_DELAY

Type: read-write
Reset State: 0x7D00

Specifies various delays for several operating modes of the CW detector

AGC_CW_MODE_DELAY

Bits	Name	Description
15:8	RADAR_DET_DELAY	Delay before starting cs_det after a pulse detect Reset State: 0x007D

0x3000138 AGC_TH_D0_A

Type: read-write
Reset State: 0x0087

This registers sets the correlation threshold above which the AGC decides an 802.11a packet is being received.

AGC_TH_D0_A

Bits	Name	Description
7:0	THRESHOLD	Reset State: 0x0087

0x300013C AGC_TH_D0_A_LOW

Type: read-write
Reset State: 0x0078

This registers sets the correlation threshold above which the AGC decides an 802.11a packet with high SNR is being received. The purpose of this register is to have a more sensitive and hence faster packet detection, since high SNR signals require two coarse gain steps, which are time consuming.

AGC_TH_D0_A_LOW

Bits	Name	Description
7:0	THRESHOLD	Reset State: 0x0078

0x3000140 AGC_TH_D0_B

Type: read-write
Reset State: 0x008C

This registers sets the correlation threshold above which the AGC decides an 802.11b packet is being received. It can be set lower than the threshold for 11a packets since there is a longer time interval to correlate over.

AGC_TH_D0_B

Bits	Name	Description
7:0	THRESHOLD	Reset State: 0x008C

0x3000144 AGC_TH_D0_B_TF_EST

Type: read-write
Reset State: 0x0050

This registers sets the correlation threshold above which the AGC decides an 802.11b packet is being received during the timing and frequency estimation state. This is a reconfirmation test which reduces the false alarm rate of the AGC for 11b packets. It is generally set lower than the initial threshold for 11b packets since the correlator is to allow margin for a low correlation value which can occur at the moment the correlator output is sampled (at the end of the 10 us tf (time and frequency)-estimation interval).

AGC_TH_D0_B_TF_EST

Bits	Name	Description
7:0	THLD	Reset State: 0x0050

0x3000148 AGC_TH_D0_11N

Type: read-write
Reset State: 0x005A

This registers sets the correlation threshold above which the AGC decides an 802.11n packet is being received

AGC_TH_D0_11N

Bits	Name	Description
7:0	VAL	Reset State: 0x005A

0x300014C AGC_TH_D0_11N_LOW

Type: read-write
Reset State: 0x0078

This registers sets the correlation threshold above which the AGC decides an 802.11n packet is being received

AGC_TH_D0_11N_LOW

Bits	Name	Description
7:0	VAL	Reset State: 0x0078

0x3000150 AGC_TH_D0_11AC

Type: read-write
Reset State: 0x0078

This registers sets the correlation threshold above which the AGC decides an 802.11ac packet is being received

AGC_TH_D0_11AC

Bits	Name	Description
7:0	VAL	Reset State: 0x0078

0x3000154 AGC_TH_D0_11AC_LOW

Type: read-write
Reset State: 0x0078

This registers sets the correlation threshold above which the AGC decides an 802.11ac packet is being received

AGC_TH_D0_11AC_LOW

Bits	Name	Description
7:0	VAL	Reset State: 0x0078

0x3000158 AGC_TH_MAXCORBA

Type: read-write
Reset State: 0x0000

This registers sets the cross check correlation threshold above which the AGC decides between 802.11b vs. 802.11a packet is being received

AGC_TH_MAXCORBA

Bits	Name	Description
7:0	VAL	Reset State: 0x0000

0x300015C AGC_TH_MAXCOR40

Type: read-write
Reset State: 0x00C8

This registers sets the cross check correlation threshold above which the AGC decides between 802.11n40 vs. 802.11a packet is being received

AGC_TH_MAXCOR40

Bits	Name	Description
7:0	VAL	Reset State: 0x00C8

0x3000160 AGC_TH_MAXCORA40

Type: read-write
Reset State: 0x0032

This registers sets the cross check correlation threshold above which the AGC decides between 802.11a and a 802.11n packet is being received

AGC_TH_MAXCORA40

Bits	Name	Description
7:0	VAL	Reset State: 0x0032

0x3000164 AGC_TH_MAXCOR20

Type: read-write
Reset State: 0x00C8

This registers sets the cross check correlation threshold above which the AGC decides between 802.11ac vs. 802.11a packet is being received

AGC_TH_MAXCOR20

Bits	Name	Description
10	DIS	Reset State: 0x0000
9:0	VAL	Reset State: 0x00C8

0x3000168 AGC_TH_MAXCORA80

Type: read-write
Reset State: 0x0032

This registers sets the cross check correlation threshold above which the AGC decides between 802.11a and a 802.11n packet is being received

AGC_TH_MAXCORA80

Bits	Name	Description
7:0	VAL	Reset State: 0x0032

0x300016C AGC_TH_MAXCORAB

Type: read-write
Reset State: 0x0005

For a positive 802.11b packet detection, not only should the auto-correlation value divided by the signal power exceed TH_D0_A (or TH_D0_A_LOW in high SNR), it should also exceed that of the 802.11b bandwidth packet detector multiplied by the value in this register, divided by 256. The default fraction of the double bandwidth detector output that the 802.11b detector should exceed is 0.5 (128/256).

AGC_TH_MAXCORAB

Bits	Name	Description
7:0	THRESHOLD	Reset State: 0x0005

0x3000170 AGC_C11B

Type: read-write
Reset State: 0x00E2

Averaging Parameter for correlation metric of 11b detector. Allowed values are 200-255

AGC_C11B

Bits	Name	Description
7:0	VAL	Reset State: 0x00E2

0x3000174 AGC_C11BP

Type: read-write
Reset State: 0x00FD

Averaging Parameter for power metric of 11b detector. Allowed values are 200-255

AGC_C11BP

Bits	Name	Description
7:0	VAL	Reset State: 0x00FD

0x3000178 AGC_TH_CAP_A

Type: read-write
Reset State: 0x0032

Detection threshold for capture event when reception of current 11a packet has been aborted. Value 0 is disables this check.

AGC_TH_CAP_A

Bits	Name	Description
7:0	LEVEL_JUMP	Delta signal level. Default value 50 (7dB). Reset State: 0x0032

0x300017C AGC_TH_CAP_B

Type: read-write
Reset State: 0x0032

Detection threshold for capture event when reception of current 11b packet has been aborted. Value 0 is disables this check.

AGC_TH_CAP_B

Bits	Name	Description
7:0	LEVEL_JUMP	Delta signal level. Default value 50 (7dB). Reset State: 0x0032

0x3000180 AGC_TH_CAP_RXA

Type: read-write
Reset State: 0x0032

Detection threshold for capture event when 11a packet is being received. Value 0 is disables this check.

AGC_TH_CAP_RXA

Bits	Name	Description
7:0	LEVEL_JUMP	Delta signal level. Default value 50 (7dB). Reset State: 0x0032

0x3000184 AGC_TH_CAP_RXB

Type: read-write
Reset State: 0x0032

Detection threshold for capture event when 11b packet is being received. Value 0 is disables this check.

AGC_TH_CAP_RXB

Bits	Name	Description
7:0	LEVEL_JUMP	Delta signal level. Default value 50 (7dB). Reset State: 0x0032

0x3000188 AGC_TH_PIP_PWR_JUMP

Type: read-write
Reset State: 0x0000

Threshold for power jump to detect for a packet-in-packet case

AGC_TH_PIP_PWR_JUMP

Bits	Name	Description
7:0	VAL	Reset State: 0x0000

0x300018C AGC_TH_EOP_LVL_DROP

Type: read-write
Reset State: 0x0010

Threshold for signal level drop to detect end of packet in the case of a corrupted length field.

AGC_TH_EOP_LVL_DROP

Bits	Name	Description
7:0	EOP_LVL_DROP	Delta signal level Default value 16 (12dB). Reset State: 0x0010

0x3000190 AGC_TH_CORR_DROP

Type: read-write
Reset State: 0x0000

AGC compares power with this threshold. If power is lower, in correlation state then an 802.11a trigger is ignored.

AGC_TH_CORR_DROP

Bits	Name	Description
7:0	THRESHOLD	Power drop threshold. Default value 0 (i.e., disabled). Reset State: 0x0000

0x3000194 AGC_CORR_TIME

Type: read-write
Reset State: 0x0190

This register specifies the time, in increments of 25ns, which the AGC can spend correlating if an energy jump has been detected in the AGC state.

AGC_CORR_TIME

Bits	Name	Description
11:0	TIME	Correlation Time. Default value is 400, i.e., 10 microseconds. Reset State: 0x0190

0x3000198 AGC_ALL_RX_ON_TIME

Type: read-write
Reset State: 0x0019

Time to leave all antennas on after a set_all_rx command. Units are in 0.8us steps.

AGC_ALL_RX_ON_TIME

Bits	Name	Description
5:0	DELAY	Reset State: 0x0019

0x300019C AGC_TRIGGER_DELAY

Type: read-write
Reset State: 0x0014

Detector triggers are ignored for a time specified by this register after a set_all_rx command. This enables the detectors to build up a reliable power estimate.

AGC_TRIGGER_DELAY

Bits	Name	Description
4:0	TIME	Delay in 100ns increments. Reset State: 0x0014

0x30001A0 AGC_PWR_NOTCH_ALPHA1

Type: read-write
Reset State: 0x012C

AGC_PWR_NOTCH_ALPHA1

Bits	Name	Description
8:0	ALPHA	Reset State: 0x012C

0x30001A4 AGC_PWR_NOTCH_ALPHA2

Type: read-write
Reset State: 0x01FF

AGC_PWR_NOTCH_ALPHA2

Bits	Name	Description
8:0	ALPHA	Reset State: 0x01FF

0x30001A8 AGC_PWR_NOTCH_T_ALPHA

Type: read-write
Reset State: 0x0008

AGC_PWR_NOTCH_T_ALPHA

Bits	Name	Description
9	BYPASS	0x0: ENABLE 0x1: BYPASS Reset State: 0x0000
8:0	TIME	Reset State: 0x0008

0x30001AC AGC_D_TX_SETTLE

Type: read-write
Reset State: 0x0028

Ranges from 0 to 12.775 micro seconds.

AGC_D_TX_SETTLE

Bits	Name	Description
8:0	DELAY	Propagation time in 25ns units. Reset State: 0x0028

0x30001B0 AGC_D_UNSATURATED

Type: read-write
Reset State: 0x0010

Gain settling delay for RF RX non-saturated RX FE. Settling time in increments of 25 ns (40 MHz samples) Ranges from 0 to 1.575 micro seconds.

AGC_D_UNSATURATED

Bits	Name	Description
5:0	DELAY	Settling time in 25ns units. Reset State: 0x0010

0x30001B4 AGC_D_SATURATED

Type: read-write
Reset State: 0x0010

Gain settling delay for RF RX saturated RX FE. Settling time in increments of 25 ns (40 MHz samples) Ranges from 0 to 1.575 micro seconds.

AGC_D_SATURATED

Bits	Name	Description
5:0	DELAY	Settling time in 25ns units. Reset State: 0x0010

0x30001B8 AGC_D_FIRANDCAL

Type: read-write
Reset State: 0x0010

RXFIR and CAL propagation delay. Ranges from 0 to 1.575 micro seconds.

AGC_D_FIRANDCAL

Bits	Name	Description
5:0	DELAY	Propagation time in 25ns units. Default value is 14, corresponding to 350 ns. Reset State: 0x0010

0x30001BC AGC_D_HT_STS_COARSE_MEAS

Type: read-write
Reset State: 0x0028

AGC_D_HT_STS_COARSE_MEAS

Bits	Name	Description
7:0	TIME	Settling time in 25ns units. Reset State: 0x0028

0x30001C0 AGC_D_HT_STS_FINE_MEAS

Type: read-write
Reset State: 0x0064

AGC_D_HT_STS_FINE_MEAS

Bits	Name	Description
7:0	TIME	Settling time in 25ns units. Reset State: 0x0064

0x30001C4 AGC_D_VHT_STS_COARSE_MEAS

Type: read-write
Reset State: 0x0028

AGC_D_VHT_STS_COARSE_MEAS

Bits	Name	Description
7:0	TIME	Settling time in 25ns units. Reset State: 0x0028

0x30001C8 AGC_D_VHT_STS_FINE_MEAS

Type: read-write
Reset State: 0x0066

AGC_D_VHT_STS_FINE_MEAS

Bits	Name	Description
7:0	TIME	Settling time in 25ns units. Reset State: 0x0066

0x30001CC AGC_D_VHT_DET_TIME

Type: read-write
Reset State: 0x008E

AGC_D_VHT_DET_TIME

Bits	Name	Description
7:0	TIME	Max time in 25ns units that VHT detection is allowed from the start of the VHT-STS. Reset State: 0x008E

0x30001D0 AGC_SIFS_TIME_A

Type: read-write
Reset State: 0x0028

This register specifies the time in 25 ns increments, that the receiver is insensitive after the reception of an IEEE802.11a packet. This value may be set to zero which increases false detection probability of ACK packets, but which allows receptions of packets with a non-standard interframe spacing.

AGC_SIFS_TIME_A

Bits	Name	Description
9:0	SIFS_A	SIFS time. Default value is 40, or 1 micro seconds (16 us as per 11a standard - 4us CCA hangover time). 0x0: MIN 0x1: STEP 0x3FF: MAX Reset State: 0x0028

0x30001D4 AGC_SIFS_TIME_B

Type: read-write
Reset State: 0x0028

This register specifies the time in 25 ns increments, that the receiver is insensitive after the reception of an IEEE802.11b packet. This value may be set to zero which increases false detection probability of ACK packet, but which allows receptions of packets with a non-standard interframe spacing.

AGC_SIFS_TIME_B

Bits	Name	Description
9:0	SIFS_B	SIFS time. Default value is 40, or 1 micro seconds. 0x0: MIN 0x1: STEP 0x3FF: MAX Reset State: 0x0028

0x30001D8 AGC_MAX_RX_TIME_A

Type: read-write
Reset State: 0x01AD

Max receive time of an 11a packet in 12.8 us increments. Used to prevent lockup of the AGC state machine when it is unable to determine end of packet in the case of a corrupted length field when no end of packet level drop is detected.

AGC_MAX_RX_TIME_A

Bits	Name	Description
11:0	MAX_RX_TIME	Max RX time. Default value 20+4096*8/6=5482 (6 Mbit/s packet of 4096 bytes plus OFDM preamble) and 429*12.8=5491.2) Reset State: 0x01AD

0x30001DC AGC_MAX_RX_TIME_B

Type: read-write
Reset State: 0x0A10

Max receive time of an 11b packet in 25.6 us increments. Used to prevent lockup of the AGC state machine when it is unable to determine end of packet in the case of a corrupted length field when no end of packet level drop is detected.

AGC_MAX_RX_TIME_B

Bits	Name	Description
11:0	MAX_RX_TIME	Max RX time. Default value 192+4096*8=32960 (1 Mbit/s packet of 4096 bytes plus long preamble) and 2576*12.8=32973) Reset State: 0x0A10

0x30001E0 AGC_WLAN_POS_EN

Type: read-write
Reset State: 0x0000

Enable for WLAN positioning feature

AGC_WLAN_POS_EN

Bits	Name	Description
0	ENABLE	Reset State: 0x0000

0x30001E4 AGC_WLAN_POS_OFFSET_11B

Type: read-write
Reset State: 0x0040

Offset applied to SIFS time measured for 11b packets.

AGC_WLAN_POS_OFFSET_11B

Bits	Name	Description
6:0	OFFSET	In 25ns steps. Reset State: 0x0040

0x30001E8 AGC_WLAN_POS_OFFSET_11A

Type: read-write
Reset State: 0x0040

Offset applied to SIFS time measured for 11a/n 20MHz packets.

AGC_WLAN_POS_OFFSET_11A

Bits	Name	Description
6:0	OFFSET	In 25ns steps. Reset State: 0x0040

0x30001EC AGC_WLAN_POS_OFFSET_11N

Type: read-write
Reset State: 0x0040

Offset applied to SIFS time measured for 11n 40MHz packets.

AGC_WLAN_POS_OFFSET_11N

Bits	Name	Description
6:0	OFFSET	In 25ns steps. Reset State: 0x0040

0x30001F0 AGC_WLAN_POS_OFFSET_11AC

Type: read-write
Reset State: 0x0040

Offset applied to SIFS time measured for 11ac 80MHz packets.

AGC_WLAN_POS_OFFSET_11AC

Bits	Name	Description
6:0	OFFSET	In 25ns steps. Reset State: 0x0040

0x30001F4 AGC_WLAN_POS_STATUS

Type: read-only

AGC_WLAN_POS_STATUS

Bits	Name	Description
9:0	SIFS_TIME	Measured SIFS time in 25ns steps. To clear this value, set the wlan_pos_en register to 0.

0x30001F8 AGC_RDET_RSSI_THRESHOLD

Type: read-write
Reset State: 0x007F

If the maximum of the N_LISTEN RSSI inputs as calculated by the power block in the AGC exceeds the value in the up threshold field of this register, a start of pulse is flagged to the pulse train detector. When the max RSSI sinks below the value of the down threshold field, the end of pulse is flagged. If both thresholds are set to 0, the analog pulse detector (in the Mars RF ASIC) is used instead. The start of the pulse is detected on the rising edge of this signal. The end of the pulse is detected on the falling edge.

AGC_RDET_RSSI_THRESHOLD

Bits	Name	Description
13:7	DET_THLD_DN	Pulse detection threshold. Reset State: 0x0000
6:0	DET_THLD_UP	Pulse detection threshold. Reset State: 0x007F

0x30001FC AGC_RDET_MIN_IAT_WRITE

Type: read-write
Reset State: 0x6F7C

This register defines the maximum inter-arrival time between radar pulses, measured in multiples of 128 samples. Pulse that arrive after the previous pulse within a time less than the value in this register are ignored by the radar pulse train detector. If set equal to max_iat, then this register has no effect on the operation of the radar detector. This value gets written to the appropriate train detector selected by det_sel, with the write itself enabled using det_write (see register rdet_reset).

AGC_RDET_MIN_IAT_WRITE

Bits	Name	Description
15:0	MIN_IAT	Minimum Inter-arrival time. default is 0.499 ms (radar type 3). 0x1: STEP_SIZE Reset State: 0x6F7C

0x3000200 AGC_RDET_MAX_IAT_WRITE

Type: read-write
Reset State: 0x01BF

This register defines the maximum inter-arrival time between radar pulses, measured in multiples of 128 samples. If this time is exceeded, then the radar detector assumes the pulse train has ended and checks whether more than min_pulse_train_count1 pulses have been counted. This value gets written to the appropriate train detector selected by det_sel, with the write itself enabled using det_write (see register rdet_reset).

AGC_RDET_MAX_IAT_WRITE

Bits	Name	Description
15:0	MAX_IAT	Maximum Inter-arrival time. Default is 3.072 (ms radar type 1). 0x1: STEP_SIZE Reset State: 0x01BF

0x3000204 AGC_RDET_PULSE_WIDTH_MARGIN_WRITE

Type: read-write
Reset State: 0x0005

When the first pulse of a train arrives, its duration is stored. Subsequent pulses' durations are compared to this first one. If a pulse of a different length is encountered, the pulse train ends. The comparison uses a margin as defined by this register. The check performed is if abs (current_pulse_duration - first_pulse_duration) <= this register then the current pulse does not break the train, and the pulse counter is increased. This value gets written to the appropriate train detector selected by det_sel, with the write itself enabled using det_write (see register rdet_reset).

AGC_RDET_PULSE_WIDTH_MARGIN_WRITE

Bits	Name	Description
7:0	PW_MRGN	Pulse width margin. Reset State: 0x0005

0x3000208 AGC_RDET_MIN_PULSE_TRAIN_COUNT1_WRITE

Type: read-write
Reset State: 0x0004

If a radar pulse train ends because the maximum inter-arrival time has expired, the current number of pulses counted is compared with this register. If the number of pulses is greater than or equal to this register's contents, then the radar detection flag is raised. This value gets written to the appropriate train detector selected by det_sel, with the write itself enabled using det_write (see register rdet_reset).

AGC_RDET_MIN_PULSE_TRAIN_COUNT1_WRITE

Bits	Name	Description
15:0	CNT_THLD	Pulse count threshold. Reset State: 0x0004

0x300020C AGC_RDET_MIN_PULSE_TRAIN_COUNT2_WRITE

Type: read-write
Reset State: 0x0004

If a radar pulse train ends because a pulse of different duration as the first pulse in the train is detected, the current number of pulses counted is compared with this register. If the number of pulses is greater than or equal to this register's contents, then the radar detection flag is raised. This value gets written to the appropriate train detector selected by det_sel, with the write itself enabled using det_write (see register rdet_reset).

AGC_RDET_MIN_PULSE_TRAIN_COUNT2_WRITE

Bits	Name	Description
15:0	CNT_THLD	Pulse count threshold. Reset State: 0x0004

0x3000210 AGC_RDET_MIN_PULSE_TRAIN_COUNT3_WRITE

Type: read-write
Reset State: 0x0004

If a radar a pulse is detected the number of pulses counted is increased. If the number of pulses counted is greater than or equal to this register's contents, then the radar detection flag is raised. This value gets written to the appropriate train detector selected by det_sel, with the write itself enabled using det_write (see register rdet_reset).

AGC_RDET_MIN_PULSE_TRAIN_COUNT3_WRITE

Bits	Name	Description
15:0	CNT_THLD	Pulse count threshold. Reset State: 0x0004

0x3000214 AGC_RDET_MIN_PULSE_TRAIN_COUNT4_WRITE

Type: read-write
Reset State: 0x0000

If a pulse arrives before the minimum inter-arrival time has expired the current number of pulses counted is compared with this register. If the number of pulses is greater than or equal to this register's contents, then the radar detection flag is raised. Special values are provided to simply ignore radar pulses which arrive within the minimum arrival time or to reset the pulse counter without comparing the current pulse count with this register. This value gets written to the appropriate train detector selected by det_sel, with the write itself enabled using det_write (see register rdet_reset).

AGC_RDET_MIN_PULSE_TRAIN_COUNT4_WRITE

Bits	Name	Description
15:0	CNT_THLD	Pulse count threshold. Default is 0 0x0: NO_RESET 0xFFFF: NO_CHECK Reset State: 0x0000

0x3000218 AGC_RDET_MIN_RADAR_PULSE_WIDTH_WRITE

Type: read-write
Reset State: 0x0012

Minimum radar pulse width, specified in samples. When the end of a pulse is detected, its duration is compared to the contents of this registers. When the pulse duration is less than or equal to the this register's content, the pulse is ignored. This mechanism is to ensure that short glitches (for instance ripple on a pulse which is just on the rssi_threshold level) or a rapidly switching clip detect signal are ignored. This value gets written to the appropriate train detector selected by det_sel, with the write itself enabled using det_write (see register rdet_reset).

AGC_RDET_MIN_RADAR_PULSE_WIDTH_WRITE

Bits	Name	Description
15:0	MIN_PW	Minimum pulse width. Reset State: 0x0012

0x300021C AGC_RDET_MAX_RADAR_PULSE_WIDTH_WRITE

Type: read-write
Reset State: 0x0016

Maximum radar pulse width, specified in samples. When the end of a pulse is detected, its duration is compared to the contents of this registers. When the pulse duration is greater than or equal to the this register's content, the pulse is ignored. This mechanism is to ensure that packet transmissions (typically of much longer duration as radar pulses) are not counted as radar pulses. Setting this register to 0 will disable the radar detector. This value gets written to the appropriate train detector selected by det_sel, with the write itself enabled using det_write (see register rdet_reset).

AGC_RDET_MAX_RADAR_PULSE_WIDTH_WRITE

Bits	Name	Description
15:0	MAX_PW	Maximum pulse width. Reset State: 0x0016

0x3000220 AGC_RDET_MIN_IAT_READ

Type: read-only

This register defines the maximum inter-arrival time between radar pulses, measured in multiples of 128 samples. Pulse that arrive after the previous pulse within a time less than the value in this register are ignored by the radar pulse train detector. If set equal to max_iat, then this value has no effect on the operation of the radar detector. This value is read from the appropriate train detector selected by det_sel (see register rdet_reset).

AGC_RDET_MIN_IAT_READ

Bits	Name	Description
15:0	MIN_IAT	Minimum Inter-arrival time. default is 0.499 ms (radar type 3). 0x1: STEP_SIZE

0x3000224 AGC_RDET_MAX_IAT_READ

Type: read-only

This register defines the maximum inter-arrival time between radar pulses, measured in multiples of 128 samples. If this time is exceeded, then the radar detector assumes the pulse train has ended and checks whether more than min_pulse_train_count1 pulses have been counted. This value is read from the appropriate train detector selected by det_sel (see register rdet_reset).

AGC_RDET_MAX_IAT_READ

Bits	Name	Description
15:0	MAX_IAT	Maximum Inter-arrival time. Default is 3.072 (ms radar type 1). 0x1: STEP_SIZE

0x3000228 AGC_RDET_PULSE_WIDTH_MARGIN_READ

Type: read-only

When the first pulse of a train arrives, its duration is stored. Subsequent pulses' durations are compared to this first one. If a pulse of a different length is encountered, the pulse train ends. The comparison uses a margin as defined by this register. The check performed is if abs (current_pulse_duration - first_pulse_duration) <= this register then the current pulse does not break the train, and the pulse counter is increased. This value is read from the appropriate train detector selected by det_sel (see register rdet_reset).

AGC_RDET_PULSE_WIDTH_MARGIN_READ

Bits	Name	Description
7:0	PW_MRGN	Pulse width margin.

0x300022C AGC_RDET_MIN_PULSE_TRAIN_COUNT1_READ

Type: read-only

If a radar pulse train ends because the maximum inter-arrival time has expired, the current number of pulses counted is compared with this register. If the number of pulses is greater than or equal to this register's contents, then the radar detection flag is raised. This value is read from the appropriate train detector selected by det_sel (see register rdet_reset).

AGC_RDET_MIN_PULSE_TRAIN_COUNT1_READ

Bits	Name	Description
15:0	CNT_THLD	Pulse count threshold.

0x3000230 AGC_RDET_MIN_PULSE_TRAIN_COUNT2_READ

Type: read-only

If a radar pulse train ends because a pulse of different duration as the first pulse in the train is detected, the current number of pulses counted is compared with this register. If the number of pulses is greater than or equal to this register's contents, then the radar detection flag is raised. This value is read from the appropriate train detector selected by det_sel (see register rdet_reset).

AGC_RDET_MIN_PULSE_TRAIN_COUNT2_READ

Bits	Name	Description
15:0	CNT_THLD	Pulse count threshold.

0x3000234 AGC_RDET_MIN_PULSE_TRAIN_COUNT3_READ

Type: read-only

If a radar a pulse is detected the number of pulses counted is increased. If the number of pulses counted is greater than or equal to this register's contents, then the radar detection flag is raised. This value is read from the appropriate train detector selected by det_sel (see register rdet_reset).

AGC_RDET_MIN_PULSE_TRAIN_COUNT3_READ

Bits	Name	Description
15:0	CNT_THLD	Pulse count threshold.

0x3000238 AGC_RDET_MIN_PULSE_TRAIN_COUNT4_READ

Type: read-only

If a pulse arrives before the minimum inter-arrival time has expired the current number of pulses counted is compared with this register. If the number of pulses is greater than or equal to this register's contents, then the radar detection flag is raised. Special values are provided to simply ignore radar pulses which arrive within the minimum arrival time or to reset the pulse counter without comparing the current pulse count with this register. This value is read from the appropriate train detector selected by det_sel (see register rdet_reset).

AGC_RDET_MIN_PULSE_TRAIN_COUNT4_READ

Bits	Name	Description
15:0	CNT_THLD	Pulse count threshold. Default is 0 0x0: NO_RESET 0xFFFF: NO_CHECK

0x300023C AGC_RDET_MIN_RADAR_PULSE_WIDTH_READ

Type: read-only

Minimum radar pulse width, specified in samples. When the end of a pulse is detected, its duration is compared to the contents of this registers. When the pulse duration is less than or equal to the this register's content, the pulse is ignored. This mechanism is to ensure that short glitches (for instance ripple on a pulse which is just on the rssi_threshold level) or a rapidly switching clip detect signal are ignored. This value is read from the appropriate train detector selected by det_sel (see register rdet_reset).

AGC_RDET_MIN_RADAR_PULSE_WIDTH_READ

Bits	Name	Description
15:0	MIN_PW	Minimum pulse width.

0x3000240 AGC_RDET_MAX_RADAR_PULSE_WIDTH_READ

Type: read-only

Maximum radar pulse width, specified in samples. When the end of a pulse is detected, its duration is compared to the contents of this registers. When the pulse duration is greater than or equal to the this register's content, the pulse is ignored. This mechanism is to ensure that packet transmissions (typically of much longer duration as radar pulses) are not counted as radar pulses. Setting this register to 0 will disable the radar detector. This value is read from the appropriate train detector selected by det_sel (see register rdet_reset).

AGC_RDET_MAX_RADAR_PULSE_WIDTH_READ

Bits	Name	Description
15:0	MAX_PW	Maximum pulse width.

0x3000244 AGC_RDET_RESET

Type: read-write
Reset State: 0x08FF

Reset the radar detector to its initial state by writing a 1 followed by a zero to bit 0 in this register. Writing a 1 will disable the radar detector. The radar detector is disabled by default.

AGC_RDET_RESET

Bits	Name	Description
14	DET_WRITE	Train detector APB write bit. 0x0: DIS 0x1: EN Reset State: 0x0000
13:11	RSSI_MODE	Configure RSSI combination mode. 0x0: RSSI0 0x1: MAX_RSSI 0x2: MIN_RSSI Reset State: 0x0001
10:8	DET_SEL	Select train detector to program. 0x7: SEL7 0x6: SEL6 0x5: SEL5 0x4: SEL4 0x3: SEL3 0x2: SEL2 0x1: SEL1 0x0: SEL0 Reset State: 0x0000
7:0	DET_RST	8'b0xxxxxxx -> enable7 (Enable train detector 7) 8'b1xxxxxxx -> disable7 (Disable train detector 7) 8'bx0xxxxxx -> enable6 (Enable train detector 6) 8'bx1xxxxxx -> disable6 (Disable train detector 6) 8'bxx0xxxxx -> enable5 (Enable train detector 5) 8'bxx1xxxxx -> disable5 (Disable train detector 5) 8'bxxx0xxxx -> enable4 (Enable train detector 4) 8'bxxx1xxxx -> disable4 (Disable train detector 4) 8'bxxxx0xxx -> enable3 (Enable train detector 3) 8'bxxxx1xxx -> disable3 (Disable train detector 3) 8'bxxxxx0xx -> enable2 (Enable train detector 2) 8'bxxxxx1xx -> disable2 (Disable train detector 2) 8'bxxxxxx0x -> enable1 (Enable train detector 1) 8'bxxxxxx1x -> disable1 (Disable train detector 1) 8'bxxxxxxx0 -> enable0 (Enable train detector and rest of radar detector) 8'bxxxxxxx1 -> disable0 (Disable train detector and rest of radar detector) Enable/Disable of radar detector and train detector instantiations. Reset State: 0x00FF

0x3000248 AGC_RDET_RADAR_DETECTED

Type: read-only

When this bit is set a radar pulse train has been detected. This bit must be reset by the radar detection (interrupt) services routine by writing a '1' into the dflag_rst register.

AGC_RDET_RADAR_DETECTED

Bits	Name	Description
5:3	TRIGGER_DET	Number of detector instance that triggered the radar detector.
2:1	TRIGGER_SRC	Trigger source. For debugging purposes this field display the reason why the radar detector triggered. 0x1: C1 0x2: C2 0x3: C3 0x0: C4
0	PULSE_DET	Detection bit. 0x0: IDEL 0x1: PDET

0x300024C AGC_RDET_PULSEWIDTH

Type: read-only

This register specifies the width of the first pulse in the detected pulse train. All other pulses in the train have an equal with, to within the pulse_width_margin.

AGC_RDET_PULSEWIDTH

Bits	Name	Description
15:0	PULSE_WIDTH	Pulse width.

0x3000250 AGC_RDET_NUM_DETECTED

Type: read-only

This register reports the number of pulses counted by the radar detection algorithm.

AGC_RDET_NUM_DETECTED

Bits	Name	Description
15:0	NUM_DET	Number of pulses counted.

0x3000254 AGC_RDET_MEASUREMENT_DELAY

Type: read-write
Reset State: 0x0020

This register configures the time interval (measured in rssi samples) after which the radar detector measures rssi level after it returns to the CORR state after a gain set due to a clip event. It can not

evaluate RSSI immediately since the RSSI circuit comes out of reset when the CORR state is entered. Therefore it takes time for the RSSI to ramp up (about 32 samples). The time programmed in this register should be larger than the RSSI ramp up time.

AGC_RDET_MEASUREMENT_DELAY

Bits	Name	Description
8	CORR_FLAG_BYPASS	Correlation flag function bypass. If asserted, the correlation flag function in the RDET pulse detector (used to delay transition of the main state machine from IDLE to CLIP_S1) will be bypassed. Default setting = 1'b0. Reset State: 0x0000
7:0	TIME	Measurement delay. Reset State: 0x0020

0x3000258 AGC_RDET_FLAG_RESET

Type: command
Reset State: 0x0000

This register contains 2 bits that control the operation of the radar detector.

AGC_RDET_FLAG_RESET

Bits	Name	Description
0	DFLAG_RST	Reset detector flag. While the detector flag is set further radar detects are ignored and the num_detected and pulse width registers are not updated. By writing a 1 to this register, the detector flag is reset and will be set when the next radar burst is detected. 0x0: NORMAL 0x1: RESET Reset State: 0x0000

0x300025C AGC_RSSI_THRESHOLD_CLIPPED

Type: read-write
Reset State: 0x0000

RSSI threshold for clipped pulses

AGC_RSSI_THRESHOLD_CLIPPED

Bits	Name	Description
13:7	DET_THLD_DN	Pulse detection threshold. Reset State: 0x0000

AGC_RSSI_THRESHOLD_CLIPPED (cont.)

Bits	Name	Description
6:0	DET_THLD_UP	Pulse detection threshold. Reset State: 0x0000

0x3000260 AGC_CW_PULSE_WIDTH

Type: read-write
Reset State: 0x0019

When the radar detector's pulse detector detects a radar pulse it monitors the CW detect flag. When this flag is set the pulse detector sets a local flag called cw_detected. When at the end of the radar pulse, the cw_detected flag is still not set, the in the pulse is discounted as a radar pulse (which should be narrow-band) and the pulse_cancel output is asserted. Some pulses are too short to perform a cw detection on. The cw detection time is the sum of the sample data gathering time (which is programmed in CSR cw_radar_delay) and the fft and cw detect calculation time. If the pulse duration is less than the number in this register, then the radar detector'S pulse detector assumes that the detected pulse is a radar pulse. The radar detector's train detectors may still reject is because it is not in between the minimum and maximum radar pulse width.

AGC_CW_PULSE_WIDTH

Bits	Name	Description
7:0	VAL	Duration of data gathering and calculation time for cw detection, specified in multiples of 0.8 us (16 20 Mhz sample). Reset State: 0x0019

0x3000264 AGC_CW_RADAR

Type: read-write
Reset State: 0x007D

This register configures if and with what delay the radar detector can start the CW detector.

AGC_CW_RADAR

Bits	Name	Description
9	DET_DIS	Disables control of the CW detector by the radar detector. Reset State: 0x0000
8:0	DELAY	Amount of delay in 40 MHz samples between start pulse of the radar detector and the time that the CW detector starts calculating. Reset State: 0x007D

0x3000268 AGC_ACI_DETECT_TH

Type: read-write
Reset State: 0x0148

When detecting a radar pulse, the radar detector's pulse detector calculates the difference between the total (pre FIR) RSSI and the in-band (post FIR) RSSI. If this difference exceeds the threshold programmed in this register, the aci_detect flag is asserted. If, during a radar pulse, the ratio of the total time that this flag is asserted and the pulse's duration exceeds the second threshold specified in this register, then the radar detector decides that this pulse was in the adjacent channel. The rain detector will then ignored this pulse. This mechanism help to avoid false triggers on packet traffic, interference and radar pulses in the adjacent channel. This type of false triggers would have the adverse effect that the radar detector would vacate a clean channel because a noisy neighbor.

AGC_ACI_DETECT_TH

Bits	Name	Description
12	DETECT_DIS	0x1: DISABLE 0x0: ENABLE Reset State: 0x0000
11:4	TH_RSSI_ACI	This register field specifies the RSSI delta which the pre and post FIR RSSI should differ by, to be considered adjacent channel power. Reset State: 0x0014
3:0	ACI_FRACTION	This register field specifies the fractional threshold that the pre and post FIR RSSI difference should exceed to be counted as ACI (Adjacent Channel Interference). This threshold is specified in integer multiples of 1/16-this. For example, a value of 8 means that the RSSI should differ by more than th_rss_aci for more than 50% of the duration of the detected radar pulse for it to ruled ACI. Reset State: 0x0008

0x300026C AGC_TRANSITION_COUNT_GLOBAL_EN

Type: read-write
Reset State: 0x0001

This is a global enable/disable for all transition counters. This is useful for freezing the counters at the same time instant before reading or writing to them.

AGC_TRANSITION_COUNT_GLOBAL_EN

Bits	Name	Description
0	ENABLE	Reset State: 0x0001

0x3000270 AGC_TRANSITION_COUNT0_EN

Type: read-write
Reset State: 0x0000

Control word for state transition counter 0. This counter can be triggered on any transition between any 2 AGC states.

AGC_TRANSITION_COUNT0_EN

Bits	Name	Description
10	ENABLE	Enables counter. Reset State: 0x0000
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x3000274 AGC_TRANSITION_COUNT1_EN

Type: read-write
Reset State: 0x0000

Control word for state transition counter 1. This counter can be triggered on any transition between any 2 AGC states.

AGC_TRANSITION_COUNT1_EN

Bits	Name	Description
10	ENABLE	Enables counter. Reset State: 0x0000
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x3000278 AGC_TRANSITION_COUNT2_EN

Type: read-write
Reset State: 0x0000

Control word for state transition counter 2. This counter can be triggered on any transition between any 2 AGC states.

AGC_TRANSITION_COUNT2_EN

Bits	Name	Description
10	ENABLE	Enables counter. Reset State: 0x0000
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x300027C AGC_TRANSITION_COUNT3_EN

Type: read-write
Reset State: 0x0000

Control word for state transition counter 3. This counter can be triggered on any transition between any 2 AGC states.

AGC_TRANSITION_COUNT3_EN

Bits	Name	Description
10	ENABLE	Enables counter. Reset State: 0x0000
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x3000280 AGC_TRANSITION_COUNT4_EN

Type: read-write
Reset State: 0x0000

Control word for state transition counter 4. This counter can be triggered on any transition between any 2 AGC states.

AGC_TRANSITION_COUNT4_EN

Bits	Name	Description
10	ENABLE	Enables counter. Reset State: 0x0000

AGC_TRANSITION_COUNT4_EN (cont.)

Bits	Name	Description
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x3000284 AGC_TRANSITION_COUNT5_EN

Type: read-write
Reset State: 0x0000

Control word for state transition counter 5. This counter can be triggered on any transition between any 2 AGC states.

AGC_TRANSITION_COUNT5_EN

Bits	Name	Description
10	ENABLE	Enables counter. Reset State: 0x0000
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x3000288 AGC_TRANSITION_COUNT6_EN

Type: read-write
Reset State: 0x0000

Control word for state transition counter 6. This counter can be triggered on any transition between any 2 AGC states.

AGC_TRANSITION_COUNT6_EN

Bits	Name	Description
10	ENABLE	Enables counter. Reset State: 0x0000
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x300028C AGC_TRANSITION_COUNT7_EN

Type: read-write
Reset State: 0x0000

Control word for state transition counter 7. This counter can be triggered on any transition between any 2 AGC states.

AGC_TRANSITION_COUNT7_EN

Bits	Name	Description
10	ENABLE	Enables counter. Reset State: 0x0000
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x3000290 AGC_TRANSITION_COUNT8_EN

Type: read-write
Reset State: 0x0000

Control word for state transition counter 8. This counter can be triggered on any transition between any 2 AGC states.

AGC_TRANSITION_COUNT8_EN

Bits	Name	Description
10	ENABLE	Enables counter. Reset State: 0x0000
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x3000294 AGC_TRANSITION_COUNT9_EN

Type: read-write
Reset State: 0x0000

Control word for state transition counter 9. This counter can be triggered on any transition between any 2 AGC states.

AGC_TRANSITION_COUNT9_EN

Bits	Name	Description
10	ENABLE	Enables counter. Reset State: 0x0000
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x3000298 AGC_TRANSITION_COUNT10_EN

Type: read-write
Reset State: 0x0000

Control word for state transition counter 10. This counter can be triggered on any transition between any 2 AGC states.

AGC_TRANSITION_COUNT10_EN

Bits	Name	Description
10	ENABLE	Enables counter. Reset State: 0x0000
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x300029C AGC_TRANSITION_COUNT11_EN

Type: read-write
Reset State: 0x0000

Control word for state transition counter 11. This counter can be triggered on any transition between any 2 AGC states.

AGC_TRANSITION_COUNT11_EN

Bits	Name	Description
10	ENABLE	Enables counter. Reset State: 0x0000

AGC_TRANSITION_COUNT11_EN (cont.)

Bits	Name	Description
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x30002A0 AGC_TRANSITION_COUNT0

Type: write-only

Debug Counter. Counts transitions between arbitrary states of the AGC state machine.

AGC_TRANSITION_COUNT0

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30002A4 AGC_TRANSITION_COUNT1

Type: write-only

Debug Counter. Counts transitions between arbitrary states of the AGC state machine.

AGC_TRANSITION_COUNT1

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30002A8 AGC_TRANSITION_COUNT2

Type: write-only

Debug Counter. Counts transitions between arbitrary states of the AGC state machine.

AGC_TRANSITION_COUNT2

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30002AC AGC_TRANSITION_COUNT3

Type: write-only

Debug Counter. Counts transitions between arbitrary states of the AGC state machine.

AGC_TRANSITION_COUNT3

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30002B0 AGC_TRANSITION_COUNT4

Type: write-only

Debug Counter. Counts transitions between arbitrary states of the AGC state machine.

AGC_TRANSITION_COUNT4

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30002B4 AGC_TRANSITION_COUNT5

Type: write-only

Debug Counter. Counts transitions between arbitrary states of the AGC state machine.

AGC_TRANSITION_COUNT5

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30002B8 AGC_TRANSITION_COUNT6

Type: write-only

Debug Counter. Counts transitions between arbitrary states of the AGC state machine.

AGC_TRANSITION_COUNT6

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30002BC AGC_TRANSITION_COUNT7

Type: write-only

Debug Counter. Counts transitions between arbitrary states of the AGC state machine.

AGC_TRANSITION_COUNT7

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30002C0 AGC_TRANSITION_COUNT8

Type: write-only

Debug Counter. Counts transitions between arbitrary states of the AGC state machine.

AGC_TRANSITION_COUNT8

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30002C4 AGC_TRANSITION_COUNT9

Type: write-only

Debug Counter. Counts transitions between arbitrary states of the AGC state machine.

AGC_TRANSITION_COUNT9

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30002C8 AGC_TRANSITION_COUNT10

Type: write-only

Debug Counter. Counts transitions between arbitrary states of the AGC state machine.

AGC_TRANSITION_COUNT10

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30002CC AGC_TRANSITION_COUNT11

Type: write-only

Debug Counter. Counts transitions between arbitrary states of the AGC state machine.

AGC_TRANSITION_COUNT11

Bits	Name	Description
15:0	COUNT	Counter output. This counter is reset by writing a 0 to it.

0x30002D0 AGC_NOISE_HIST_CTRL

Type: read-write
Reset State: 0x0001

Controls various modes of operation of the noise histogram module. It can be reset and stopped, it can be read out and reset, it can read out without being reset, and it can be read out, reset and stopped.

AGC_NOISE_HIST_CTRL

Bits	Name	Description
2	READ_AND_CLEAR	When this bit is set and the read_pulse bit is written to, the current noise histogram bin counter values are latched into the rssi status registers, the noise histogram counters are reset and noise histogram collection continues. Reset State: 0x0000
1	READOUT	When this bit is set and the read_pulse bit is written to, the current noise histogram bin counter values are latched into to the rssi status registers. Noise histogram collection continues. Reset State: 0x0000
0	RESET	When this bit is set the current noise histogram bin counter values are written to the rssi status registers, the noise histogram collection is halted and the counters are reset. Reset State: 0x0001

0x30002D4 AGC_NOISE_HIST_BIN0_MSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 0. Most significant 10 bits.

AGC_NOISE_HIST_BIN0_MSW

Bits	Name	Description
9:0	IPI_COUNT	IPI level counter value.

0x30002D8 AGC_NOISE_HIST_BIN0_LSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 0. Least significant 16 bits.

AGC_NOISE_HIST_BIN0_LSW

Bits	Name	Description
15:0	IPI_COUNT	IPI level counter value.

0x30002DC AGC_NOISE_HIST_BIN1_MSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 1. Most significant 10 bits.

AGC_NOISE_HIST_BIN1_MSW

Bits	Name	Description
9:0	IPI_COUNT	IPI level counter value.

0x30002E0 AGC_NOISE_HIST_BIN1_LSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 1. Least significant 16 bits.

AGC_NOISE_HIST_BIN1_LSW

Bits	Name	Description
15:0	IPI_COUNT	IPI level counter value.

0x30002E4 AGC_NOISE_HIST_BIN2_MSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 2. Most significant 10 bits.

AGC_NOISE_HIST_BIN2_MSW

Bits	Name	Description
9:0	IPI_COUNT	IPI level counter value.

0x30002E8 AGC_NOISE_HIST_BIN2_LSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 2. Least significant 16 bits.

AGC_NOISE_HIST_BIN2_LSW

Bits	Name	Description
15:0	IPI_COUNT	IPI level counter value.

0x30002EC AGC_NOISE_HIST_BIN3_MSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 3. Most significant 10 bits.

AGC_NOISE_HIST_BIN3_MSW

Bits	Name	Description
9:0	IPI_COUNT	IPI level counter value.

0x30002F0 AGC_NOISE_HIST_BIN3_LSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 3. Least significant 16 bits.

AGC_NOISE_HIST_BIN3_LSW

Bits	Name	Description
15:0	IPI_COUNT	IPI level counter value.

0x30002F4 AGC_NOISE_HIST_BIN4_MSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 4. Most significant 10 bits.

AGC_NOISE_HIST_BIN4_MSW

Bits	Name	Description
9:0	IPI_COUNT	IPI level counter value.

0x30002F8 AGC_NOISE_HIST_BIN4_LSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 4. Least significant 16 bits.

AGC_NOISE_HIST_BIN4_LSW

Bits	Name	Description
15:0	IPI_COUNT	IPI level counter value.

0x30002FC AGC_NOISE_HIST_BIN5_MSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 5. Most significant 10 bits.

AGC_NOISE_HIST_BIN5_MSW

Bits	Name	Description
9:0	IPI_COUNT	IPI level counter value.

0x3000300 AGC_NOISE_HIST_BIN5_LSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 5. Least significant 16 bits.

AGC_NOISE_HIST_BIN5_LSW

Bits	Name	Description
15:0	IPI_COUNT	IPI level counter value.

0x3000304 AGC_NOISE_HIST_BIN6_MSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 6. Most significant 10 bits.

AGC_NOISE_HIST_BIN6_MSW

Bits	Name	Description
9:0	IPI_COUNT	IPI level counter value.

0x3000308 AGC_NOISE_HIST_BIN6_LSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 6. Least significant 16 bits.

AGC_NOISE_HIST_BIN6_LSW

Bits	Name	Description
15:0	IPI_COUNT	IPI level counter value.

0x300030C AGC_NOISE_HIST_BIN7_MSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 7. Most significant 10 bits.

AGC_NOISE_HIST_BIN7_MSW

Bits	Name	Description
9:0	IPI_COUNT	IPI level counter value.

0x3000310 AGC_NOISE_HIST_BIN7_LSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 7. Least significant 16 bits.

AGC_NOISE_HIST_BIN7_LSW

Bits	Name	Description
15:0	IPI_COUNT	IPI level counter value.

0x3000314 AGC_NOISE_HIST_BIN8_MSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 8. Most significant 10 bits.

AGC_NOISE_HIST_BIN8_MSW

Bits	Name	Description
9:0	IPI_COUNT	IPI level counter value.

0x3000318 AGC_NOISE_HIST_BIN8_LSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 8. Least significant 16 bits.

AGC_NOISE_HIST_BIN8_LSW

Bits	Name	Description
15:0	IPI_COUNT	IPI level counter value.

0x300031C AGC_NOISE_HIST_BIN9_MSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 9. Most significant 10 bits.

AGC_NOISE_HIST_BIN9_MSW

Bits	Name	Description
9:0	IPI_COUNT	IPI level counter value.

0x3000320 AGC_NOISE_HIST_BIN9_LSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 9. Least significant 16 bits.

AGC_NOISE_HIST_BIN9_LSW

Bits	Name	Description
15:0	IPI_COUNT	IPI level counter value.

0x3000324 AGC_NOISE_HIST_BIN10_MSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 10. Most significant 10 bits.

AGC_NOISE_HIST_BIN10_MSW

Bits	Name	Description
9:0	IPI_COUNT	IPI level counter value.

0x3000328 AGC_NOISE_HIST_BIN10_LSW

Type: read-only

Counts RSSI samples within IPI (idle power indicator) level 10. Least significant 16 bits.

AGC_NOISE_HIST_BIN10_LSW

Bits	Name	Description
15:0	IPI_COUNT	IPI level counter value.

0x300032C AGC_NOISE_HIST_BUSY_MSW

Type: read-only

Counts microseconds during noise histogram collection during which no noise is measured because a packet is transmitted, received or NAV is busy. Most significant 10 bits.

AGC_NOISE_HIST_BUSY_MSW

Bits	Name	Description
9:0	COUNT	IPI level counter value.

0x3000330 AGC_NOISE_HIST_BUSY_LSW

Type: read-only

Counts microseconds during noise histogram collection during which no noise is measured because a packet is transmitted, received or NAV is busy. Least significant 16 bits.

AGC_NOISE_HIST_BUSY_LSW

Bits	Name	Description
15:0	COUNT	IPI level counter value.

0x3000334 AGC_WATCHDOG_MASK

Type: read-write
Reset State: 0x0001

This register is used to mask the watchdog-driven reset of the AGC state machine. When the reset is not masked, an expiry of the AGC watchdog timer will set the timeout state register, generate an interrupt and reset the AGC state machine. When the reset is masked, an expiry of the AGC watchdog timer will set the timeout state register, generate an interrupt, but will not reset the AGC state machine. This functionality is intended for debugging purposes when the AGC state machine

needs to remain in the hanging state so the various conditions that may have lead to the hangup can be studied before they are automatically reset by the watchdog timer.

AGC_WATCHDOG_MASK

Bits	Name	Description
0	MASK	0x0: UNMASKED 0x1: MASKED Reset State: 0x0001

0x3000338 AGC_TIMEOUT_STATE

Type: read-only

AGC state in which watchdog timer expired.

AGC_TIMEOUT_STATE

Bits	Name	Description
4:0	STATE	AGC State.

0x300033C AGC_AGC_WATCHDOG_TIMEOUT_WAIT_DCO_A20

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the WAIT_DCO_A state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_WAIT_DCO_A20

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 2 to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2 * 12.5 ns = 6.375 us. Reset State: 0x0000

0x3000340 AGC_AGC_WATCHDOG_TIMEOUT_WAIT_DCO_A40

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the WAIT_DCO_A40 state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_WAIT_DCO_A40

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 2 to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2 * 12.5 ns = 6.375 us. Reset State: 0x0000

0x3000344 AGC_AGC_WATCHDOG_TIMEOUT_WAIT_DCO_A80

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the WAIT_DCO_A80 state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_WAIT_DCO_A80

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 2 to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2 * 12.5 ns = 6.375 us. Reset State: 0x0000

0x3000348 AGC_AGC_WATCHDOG_TIMEOUT_WAIT_DCO_B

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the WAIT_DCO_B state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_WAIT_DCO_B

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 2 to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2 * 12.5 ns = 6.375 us. Reset State: 0x0000

0x300034C AGC_AGC_WATCHDOG_TIMEOUT_WAIT_A

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the WAIT_A state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_WAIT_A

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 8 (2^3) to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2^3 * 25 ns = 51 us. Reset State: 0x0000

0x3000350 AGC_AGC_WATCHDOG_TIMEOUT_RXA_HDR

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the RXA_HDR state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_RXA_HDR

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 8 (2^3) to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2^3 * 25 ns = 51 us. Reset State: 0x0000

0x3000354 AGC_AGC_WATCHDOG_TIMEOUT_HT_STS_COARSE

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the HT_STS_COARSE state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_HT_STS_COARSE

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 2 to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2 * 12.5 ns = 6.375 us. Reset State: 0x0000

0x3000358 AGC_AGC_WATCHDOG_TIMEOUT_HT_STS_FINE

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the HT_STS_FINE state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_HT_STS_FINE

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 2 to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2 * 12.5 ns = 6.375 us. Reset State: 0x0000

0x300035C AGC_AGC_WATCHDOG_TIMEOUT_VHT_STS_COARSE

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the VHT_STS_COARSE state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state

machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_VHT_STS_COARSE

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 2 to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2 * 12.5 ns = 6.375 us. Reset State: 0x0000

0x3000360 AGC_AGC_WATCHDOG_TIMEOUT_VHT_STS_FINE

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the VHT_STS_FINE state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_VHT_STS_FINE

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 2 to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2 * 12.5 ns = 6.375 us. Reset State: 0x0000

0x3000364 AGC_AGC_WATCHDOG_TIMEOUT_RXA_DATA

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the RXA_DATA state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_RXA_DATA

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 16384 (2^14) to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2^14 * 25 ns = 104 ms. Reset State: 0x0000

0x3000368 AGC_AGC_WATCHDOG_TIMEOUT_CAP_A

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the CAP_A state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_CAP_A

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 16384 (2^14) to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2^14 * 25 ns = 104 ms. Reset State: 0x0000

0x300036C AGC_AGC_WATCHDOG_TIMEOUT_TF_EST

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the TF_EST state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_TF_EST

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 4 (2^2) to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2^2 * 25 ns = 25.5 us. Reset State: 0x0000

0x3000370 AGC_AGC_WATCHDOG_TIMEOUT_WAIT_B

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the WAIT_B state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_WAIT_B

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 64 (2^6) to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2^6 * 25 ns = 408 us. Reset State: 0x0000

0x3000374 AGC_AGC_WATCHDOG_TIMEOUT_RXB_HDR

Type: read-write
Reset State: 0x007D

This register configures the watchdog timer for the RXB_HDR state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_RXB_HDR

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 64 (2^6) to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2^6 * 25 ns = 408 us. Reset State: 0x007D

0x3000378 AGC_AGC_WATCHDOG_TIMEOUT_RXB_DATA

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the RXB_DATA state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_RXB_DATA

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 16384 (2^14) to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2^14 * 25 ns = 104 ms. Reset State: 0x0000

0x300037C AGC_AGC_WATCHDOG_TIMEOUT_CAP_B

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the CAP_B state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_CAP_B

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 16384 (2^14) to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2^14 * 25 ns = 104 ms. Reset State: 0x0000

0x3000380 AGC_AGC_WATCHDOG_TIMEOUT_WAIT_SIFS

Type: read-write
Reset State: 0x0000

This register configures the watchdog timer for the WAIT_SIFS state of the AGC state machine. The watchdog timer is reset when the AGC state machine transitions from one state to another. When its value exceeds the threshold programmed in this register it resets the AGC state machine as well as the RXA and RXB modules. A value of zero disables the watchdog timer in this state.

AGC_AGC_WATCHDOG_TIMEOUT_WAIT_SIFS

Bits	Name	Description
7:0	TIME	Timeout delay. This value is multiplied by 8 (2^3) to arrive at the number of 40 MHz clock cycles after which the watchdog timer expires. This results in a maximum delay of 255 * 2^3 * 25 ns = 51 us. Reset State: 0x0000

0x3000384 AGC_RXFIR_CONFIG

Type: read-write
Reset State: 0x0000

Contains RxFIR configuration settings.

AGC_RXFIR_CONFIG

Bits	Name	Description
0	DEC_BY_4	Enables decimation-by-4 in the stage 1 RxFIR instead of decimation-by-3 in the normal functional mode. Reset State: 0x0000

0x3000388 AGC_VHTSIGA1_CONTENTS_1

Type: read-write
Reset State: 0x00C0

Contains programming for bit fields for VHTSIGA1"

AGC_VHTSIGA1_CONTENTS_1

Bits	Name	Description
9:5	START_BWCFG	Start of bwcfg field in VHTSIGA1 Reset State: 0x0006
4:0	START_RESERVED	Start of reserved field in VHTSIGA1 Reset State: 0x0000

0x300038C AGC_VHTSIGA1_CONTENTS_2

Type: read-write
Reset State: 0x000A

Contains programming for bit fields for VHTSIGA1"

AGC_VHTSIGA1_CONTENTS_2

Bits	Name	Description
4:0	START_MUMIMO	Start of MUMIMO field in VHTSIGA1 Reset State: 0x000A

0x3000390 AGC_VHTSIGA2_CONTENTS_1

Type: read-write
Reset State: 0x0020

Contains programming for bit fields for VHTSIGA2"

AGC_VHTSIGA2_CONTENTS_1

Bits	Name	Description
13:10	RESERVED	Reserved bits Reset State: 0x0000
9:5	START_NOTSOUNDING	Start for VHTSIGA2 notsounding bit Reset State: 0x0001
4:0	START_SMOOTHING	Start for VHTSIGA2 smoothing bit Reset State: 0x0000

0x3000394 AGC_VHTSIGA2_CONTENTS_2

Type: read-write
Reset State: 0x0062

Contains programming for bit fields for VHTSIGA2"

AGC_VHTSIGA2_CONTENTS_2

Bits	Name	Description
9:5	START_SHORTGI	Start for VHTSIGA2 shortgi bit Reset State: 0x0003
4:0	START_STBC	Start for VHTSIGA2 stbc bit Reset State: 0x0002

0x3000398 AGC_VHTSIGA2_CONTENTS_3

Type: read-write
Reset State: 0x0004

Contains programming for bit fields for VHTSIGA2"

AGC_VHTSIGA2_CONTENTS_3

Bits	Name	Description
4:0	START_RESERVED	Start of reserved field in VHTSIGA2 Reset State: 0x0004

0x300039C AGC_VHTSIGA2_CONTENTS_4

Type: read-write
Reset State: 0x024A

Contains programming for bit fields for VHTSIGA2"

AGC_VHTSIGA2_CONTENTS_4

Bits	Name	Description
9:5	START_TAIL	Start of tail field in VHTSIGA2. Width is constant 6 bits Reset State: 0x0012
4:0	START_CRC	Start of crc field in VHTSIGA2. Width is constant 8 bits Reset State: 0x000A

0x30003A0 AGC_VHTSIGB_CONTENTS_1

Type: read-write
Reset State: 0x0120

Contains programming for bit fields for VHTSIGB"

AGC_VHTSIGB_CONTENTS_1

Bits	Name	Description
9:5	START_CODING	Start for VHTSIGB shortgi bit Reset State: 0x0009
4:0	START_MCS	Start for VHTSIGB mcs bits Reset State: 0x0000

0x30003A4 AGC_VHTSIGB_CONTENTS_2

Type: read-write
Reset State: 0x024A

Contains programming for bit fields for VHTSIGB"

AGC_VHTSIGB_CONTENTS_2

Bits	Name	Description
9:5	START_TAIL	Start of tail field in VHTSIGB. Width is constant 6 bits Reset State: 0x0012
4:0	START_CRC	Start of crc field in VHTSIGB. Width is constant 8 bits Reset State: 0x000A

0x30003A8 AGC_VHTSIGA_BWENCODING

Type: read-write
Reset State: 0x01AC

Contains programming for bandwidth

AGC_VHTSIGA_BWENCODING

Bits	Name	Description
8:6	BW80	Fully specified field to indicate 20M mode, 40M mode and 80M mode. Reset State: 0x0006
5:3	BW40	Reset State: 0x0005
2:0	BW20	Reset State: 0x0004

0x30003AC AGC_VHTSIGA_GID1

Type: read-write
Reset State: 0x003F

Contains programming for group-id

AGC_VHTSIGA_GID1

Bits	Name	Description
11:6	GID2	The receiver will use this GID as the reference GID, i.e., the receiver will compare the received GID with this GID and if they do not match, will abort the packet defer for the duration of lsig. Reset State: 0x0000
5:0	GID1	The transmitter and receiver will use this GID as the reference GID, i.e., the Tx will fill this group-id in GID field to signal SU. The receiver will compare the received GID with this GID and if they do not match, will abort the packet defer for the duration of lsig. Reset State: 0x003F

0x30003B0 AGC_VHTSIGA_GID2

Type: read-write
Reset State: 0x0000

Contains programming for group-id

AGC_VHTSIGA_GID2

Bits	Name	Description
5:0	GID3	The transmitter and receiver will use this GID as the reference GID, i.e., the Tx will fill this group-id in GID field. The receiver will compare the received GID with this GID and if they do not match, will abort the packet defer for the duration of lsig. Reset State: 0x0000

0x30003B4 AGC_CCA_GI_DET_CFG_LGI

Type: read-write
Reset State: 0xA59B

AGC_CCA_GI_DET_CFG_LGI

Bits	Name	Description
15:8	TIMER_MAX_END	This register holds the upper limit on the timer (running off 40MHz clock) by when the subsequent ccadet-threshold crossing is expected. Ideally this value is 160 implying 4 microseconds. Reset State: 0x00A5
7:0	TIMER_MIN_END	This register holds the lower limit on the timer (running off 40MHz clock) by when the subsequent ccadet-threshold crossing is expected. Ideally this value is 160 implying 4 microseconds. Reset State: 0x009B

0x30003B8 AGC_CCA_GI_DET_CFG_SGI

Type: read-write
Reset State: 0x958B

AGC_CCA_GI_DET_CFG_SGI

Bits	Name	Description
15:8	TIMER_MAX_END	This register holds the upper limit on the timer (running off 40MHz clock) by when the subsequent ccadet-threshold crossing is expected. Ideally this value is 144 implying 3.6 microseconds. Reset State: 0x0095
7:0	TIMER_MIN_END	This register holds the lower limit on the timer (running off 40MHz clock) by when the subsequent ccadet-threshold crossing is expected. Ideally this value is 144 implying 3.6 microseconds. Reset State: 0x008B

16.2.12 btcf

0x3000000 BTCF_BTCF_CONFIG

Type: read-write
Reset State: 0x0EDD

Programs the offsets that will be added to the computed values

BTCF_BTCF_CONFIG

Bits	Name	Description
11:8	FFT_TOFFSET256	signed 2's complement number which is used to adjust the timing offset for the 256-point FFT start time Reset State: 0x000E
7:4	FFT_TOFFSET128	signed 2's complement number which is used to adjust the timing offset for the 128-point FFT start time Reset State: 0x000D
3:0	FFT_TOFFSET64	signed 2's complement number which is used to adjust the timing offset for the 64-point FFT start time Reset State: 0x000D

0x3000004 BTCF_BTCF_DET_RATIO

Type: read-write
Reset State: 0x0005

Detection thresholds for OFDM packets.

BTCF_BTCF_DET_RATIO

Bits	Name	Description
2:0	VALUE	The alpha value used to compute the pkt_valid flag. unsigned number. A combination of pkt_det_ratio and pkt_det_dshift determine the 11a detection threshold. Reset State: 0x0005

0x3000008 BTCF_BTCF_DET_DSHIFT

Type: read-write
Reset State: 0x0001

Detection shift values for OFDM packets.

BTCF_BTCF_DET_DSHIFT

Bits	Name	Description
2:0	VALUE	The shift value used to compute the pkt_valid flag. unsigned number Reset State: 0x0001

0x300000C BTCF_BTCFMIN

Type: read-only

Stores the last computed btcf_min value

BTCF_BTCFMIN

Bits	Name	Description
14:0	BTCF	The last latched btcf value when newmin was asserted. This is denoted as Bmin(t) in the uarch.

0x3000010 BTCF_PWRMIN

Type: read-only

Stores the last computed pow(t) value corresponding to btcf_min

BTCF_PWRMIN

Bits	Name	Description
15:0	POW	The last latched pow(t) value when newmin was asserted

0x3000014 BTCF_OFFSETMIN

Type: read-only

Stores the last computed offset counter value corresponding to btcf_min

BTCF_OFFSETMIN

Bits	Name	Description
7:0	COUNT	The last latched offset count when newmin was asserted. This provides the count value from when the first valid btcf value was computed. This value added with fft_toffset gives the delta to the TDC module

16.2.13 cal

0x3000000 CAL_CALMODE

Type: read-write

Determines the calibration mode and generates calibration enable ring these modes The Enable_Measure bit in the MSB of the register is used to enable the measurement of the value. For instance, in DC offset initial calibration mode, the CPU writes to the DC offset DAC n the RF ASIC through the SPI interface. The CPU then has to command the DC offset calibration module in the PHY to measure the DC offset (at the ADC output) after the new DAC output (in the RF ASIC) can be observed at the ADC output (typically after 0.5 us after the DAC is written to in the RF ASIC). Hence, once the CPU writes to the SPI interface, it then waits for a specific period of time (1 us) after the SPI write completes, and then asserts this bit to command the DC offset module to start the measurement. Once the measurement is done (as indicated by the CAL_STATUS) register, this bit has to be disabled so as to set up for the next measurement.

CAL_CALMODE

Bits	Name	Description
2:0	MODE	Sets the calibration mode mode value 3'b101 to 3'b111 are unused 0x0: NORMAL 0x1: INITDCCAL 0x2: RESDCCAL 0x3: IQCAL 0x4: TXLOCAL

0x3000004 CAL_MEASURE

Type: command
Reset State: 0x0000

By writing to this register, in calibration modes other than normal mode, a measure pulse is pulsed to the calibration module. Originally, this was a level signal called Enable_Measure. With the wr_Pulse register type being supported, it was decided to add this, so that software does not have to disable and then enable for the cal module to detect a pulse

CAL_MEASURE

Bits	Name	Description
0	CMD	Measure write pulse bit which enables the measurement for the specified calibration mode in the cal_mode register 0x0: NORMAL 0x1: MEASURE Reset State: 0x0000

0x3000008 CAL_CHAIN_SEL

Type: read-write

Determines which transmit/receive channel is being calibrated. If Bit 2 is 0, then the I channel of the transmit/receive chain is selected. If Bit 2 is 1, then the Q chain of the transmit/receive chain is selected. CS1 and CS0 determine which of the receive chains 0,1,2 or the transmit chains 0,1 are being calibrated as shown in table below.

CAL_CHAIN_SEL

Bits	Name	Description
2	IQSEL	Selects I/Q inputs for the inputs specified in chain 0x0: ISEL 0x1: QSEL
1:0	CHAIN	Selects receive chain output 0x0: CHAIN0 0x1: CHAIN1 0x2: CHAIN2 0x3: CHAIN3

0x300000C CAL_LENGTH_INIT

Type: read-write
Reset State: 0x03FF

The CAL_LENGTH registers are used to determine what length should the calibration module average over. If it is desirable to average over N samples, the CPU should write N-1 to this register where N is always an integer number that represents some power of 2.

CAL_LENGTH_INIT

Bits	Name	Description
11:0	LENGTH	Reset State: 0x03FF

0x3000010 CAL_LENGTH_RSA

Type: read-write
Reset State: 0x0001

The CAL_LENGTH registers are used to determine what length should the calibration module average over. If it is desirable to average over N samples, the CPU should write N-1 to this register where N is always an integer number that represents some power of 2.

CAL_LENGTH_RSA

Bits	Name	Description
11:0	LENGTH	Reset State: 0x0001

0x3000014 CAL_LENGTH_RSB

Type: read-write
Reset State: 0x00FF

The CAL_LENGTH registers are used to determine what length should the calibration module average over. If it is desirable to average over N samples, the CPU should write N-1 to this register where N is always an integer number that represents some power of 2.

CAL_LENGTH_RSB

Bits	Name	Description
11:0	LENGTH	Reset State: 0x00FF

0x3000018 CAL_DCO_THRESHOLD

Type: read-write
Reset State: 0x004C

Threshold value for the digital DC offset measured on a per-packet basis. If the measured digital DC offset is more than this threshold, the DC offset module sets the CAL_ATTENTION register to request CPU to recalibrate. Default is 150 mV (= 76 LSBs of a 10-bit ADC with a -1V to +1V swing) =0x4C

CAL_DCO_THRESHOLD

Bits	Name	Description
10:0	VALUE	Reset State: 0x004C

0x300001C CAL_DCTIMER1

Type: read-write
Reset State: 0x2C24

When the DC offset module is commanded to measure the digital DC offset either by the CPU or the AGC module (the AGC module does so on every packet), the DC offset module terminates all the RFICs inputs and waits for the time (number for 80MHz clocks) specified in the CAL_DC_TIMER1 register. This allows for the terminated input to be observed at the ADC outputs. This time is typically in the order if 0.5 us = 20 40MHz clocks = = 40 80 MHz clocks =

0x28 - 1 POR. Note that this number should always be an odd number (to be a multiple of 40 MHz clocks)

CAL_DCTIMER1

Bits	Name	Description
15:8	VALUE_RSB	Reset State: 0x002C
7:0	VALUE_RSA	Reset State: 0x0024

0x3000020 CAL_DCTIMER2

Type: read-write
Reset State: 0x2000

When the DC offset module is commanded to measure the digital DC offset either by the CPU or the AGC module (the AGC module does so on every packet), the DC offset module terminates all the RFICs inputs and waits for the time (number for 80MHz clocks) specified in the CAL_DC_TIMER1 register. This allows for the terminated input to be observed at the ADC outputs. This time is typically in the order if 0.5 us = 20 40MHz = 40 80 MHz clocks = 0x28-1. Now when the DC offset measurement is done, the DC offset module switches the RF front end back in. After switching the RF FE in, the DC offset module waits for CAL_DC_TIMER2 time before it can assert a data valid signal to the rest of the blocks. The reason there are two different timer registers for turning on and turning off the RF FE is so as to support any asymmetry in turning on/turning off the RF FE. If this saves clocks, then it allows data to be sampled earlier which may be particularly useful in per-packet calibration. Presently, the default value is 0.5us.

CAL_DCTIMER2

Bits	Name	Description
15:8	VALUE_RSB	Reset State: 0x0020
7:0	VALUE_RSA	Reset State: 0x0000

0x3000024 CAL_DCOFFSET

Type: read-only
Reset State: 0x0000

Measured DC offset, lower order bits. This register gives the measured DC offset (the output of the ADC of the selected chain) when the calibration mode is in DC Offset Initial Calibration and/or Digital DC offset calibration mode. This is a 11-bit 2's complement value. The CPU reads this value when it reads the CAL_STATUS to be done. The value read corresponds to the value in CHAIN_SEL.

CAL_DCOFFSET

Bits	Name	Description
10:0	DCOFFSET	Reset State: 0x0000

0x3000028 CAL_PWRDCOFFSET

Type: read-only
Reset State: 0x0000

Measured power of DC offset, lower order bits. This register gives the measured power of the input signal (the output of the ADC of the selected chain) when the calibration mode is in DC Offset Initial Calibration and/or Digital DC offset calibration mode. This is a 11-bit 2's complement value. The CPU reads this value when it reads the CAL_STATUS to be done. The value read corresponds to the value in CHAIN_SEL.

CAL_PWRDCOFFSET

Bits	Name	Description
15:0	POWER	Reset State: 0x0000

0x300002C CAL_CLR_DCOFFSET

Type: command
Reset State: 0x0000

Usually the last measured DC offset is held for the next packet as well until a new dco measurement is commanded by the AGC. Since, DC offset can change with time, when the AGC comes out of reset (like after beacon power save modes), software may decide to clear the DC offset register.

CAL_CLR_DCOFFSET

Bits	Name	Description
0	CMD	Clear write pulse bit which clears the latched DC offset values 0x0: NORMAL 0x1: MEASURE Reset State: 0x0000

0x3000030 CAL_CHN0_DCO_OVR

Type: read-write
Reset State: 0x0000

Used to override the measured DC offset for chain 0

CAL_CHN0_DCO_OVR

Bits	Name	Description
15:8	Q0	Reset State: 0x0000
7:0	I0	Reset State: 0x0000

0x3000034 CAL_STATUS

Type: read-only
Reset State: 0x0000

Indicates the calibration status for the current mode

CAL_STATUS

Bits	Name	Description
15:14	STATUS	Only busy, idle and done are implemented 0x0: IDLE 0x1: DONE 0x2: BUSY 0x3: ERR Reset State: 0x0000

0x3000038 CAL_OVERRIDE

Type: read-write
Reset State: 0x0000

Sets the test mode for calibration

CAL_OVERRIDE

Bits	Name	Description
0	CHN0_DC	DCO bypass bit 0x0: NORMAL 0x1: BYPASS Reset State: 0x0000

0x300003C CAL_CORR_ENABLE

Type: read-write
Reset State: 0x0002

This register provides packet-type specific enables for DCO correction

CAL_CORR_ENABLE

Bits	Name	Description
1	EN_11B	Reset State: 0x0001
0	EN_OFDM	Reset State: 0x0000

0x3000040 CAL_AIEST

Type: read-only
Reset State: 0x0000

When CAL_MODE is set to I/Q amplitude imbalance, this register gives the amplitude imbalance for that tone (CAL_IQ_TONENUM reg) for the current gain setting in AGC_GAIN_SET register. This is a 10-bit value. The CPU reads this value when it reads the CAL_STATUS to be done.The value read corresponds to the value in CHAIN_SEL.

CAL_AIEST

Bits	Name	Description
8:0	AIEST	Reset State: 0x0000

0x3000044 CAL_IQ_CORR_MODE

Type: read-write
Reset State: 0x0005

This register is used for controlling the corrector modes.

CAL_IQ_CORR_MODE

Bits	Name	Description
3:1	C0_THROUGH_TAP_SEL	Allows for selecting the specific tap location as the through tap component for the I/Q correctors. Default selection is the centre tap location. Non-listed encodings default to centre tap selection. 0x0: C0_IN_DATA_TAP 0x1: C0_IN_DATA_DLY1 0x2: C0_IN_DATA_DLY2 0x3: C0_IN_DATA_DLY3 0x4: C0_IN_DATA_DLY4 Reset State: 0x0002
0	BYPASS	When set(1), the iq corr coefficients are set to 0. When 0, iq corr coefficients are read from IQ_CORR_COEFF memory. This register was added to purely save test time and sim issues so the memories don't have to be slammed at the start of the sim Reset State: 0x0001

0x3000048 CAL_DEBUG_OUTPUT_EN_MASK

Type: read-write
Reset State: 0x0008

The bit fields in this register mask the cal_txfir_txlomode and dc_bsr_dcest output wires. This is to be used for cal debugging and system bring-up. When the *_en bits are zero the associated signals will not be asserted outside of the CAL module. The default is to have all bits in the *_en asserted for normal operation. The DC estimation enables have now been split into three categories - coarse (periodic) cal, OFDM packet residual CAL and 11b residual CAL.

CAL_DEBUG_OUTPUT_EN_MASK

Bits	Name	Description
3	TXLO_EN	Reset State: 0x0001
2	DC_EST_EN_11B	Reset State: 0x0000
1	DC_EST_EN_OFDM	Reset State: 0x0000
0	DC_EST_EN_COARSE	Reset State: 0x0000

0x300004C CAL_FORCE_TR_SWITCH

Type: read-write
Reset State: 0x0000

Using this register, the T/R switches may be set to TX mode during DCO calibration. The register provides this function to be enabled in any of the three following categories - coarse (periodic) cal, OFDM packet residual CAL and 11b residual CAL.

CAL_FORCE_TR_SWITCH

Bits	Name	Description
2	EN_11B	Reset State: 0x0000
1	EN_OFDM	Reset State: 0x0000
0	EN_COARSE	Reset State: 0x0000

0x3000050 CAL_AIEST_DISABLE

Type: read-write
Reset State: 0x0000

Using this register, the IQ amplitude imbalance estimate may be suppressed during IQ phase imbalance calculation.

CAL_AIEST_DISABLE

Bits	Name	Description
0	FLAG	Reset State: 0x0000

0x3000054 CAL_BARAM_ACCESS

Type: read-write
Reset State: 0x0000

This register controls which data stream has access to the BARAM memory. When set, the BARAM is only accessible by the host, not by internal logic.

CAL_BARAM_ACCESS

Bits	Name	Description
0	APB	Reset State: 0x0000

0x3000200+0x8*n CAL_BARAMn_0, n=[0..63]

Type: read-write
Reset State: 0x0000

Read write interface to the burst average RAM in the PIE module

CAL_BARAMn_0

Bits	Name	Description
15:0	IAVG	Reset State: 0x0000

0x3000204+0x8*n CAL_BARAMn_1, n=[0..63]

Type: read-write
Reset State: 0x0000

Read write interface to the burst average RAM in the PIE module

CAL_BARAMn_1

Bits	Name	Description
15:0	QAVG	Reset State: 0x0000

0x3000800+0x20*n CAL_IQ_CORR_COEFF_MEMn_0, n=[0..39]

Type: read-write
Reset State: 0x0000

Contains RX IQ imbalance correction coefficients for each RF gain setting

CAL_IQ_CORR_COEFF_MEMn_0

Bits	Name	Description
15:9	C0_I1_0	2's complement IQ imbalance correction coefficient for I-rail tap1 on chain 0 Reset State: 0x0000
8:0	C0_I0	2's complement IQ imbalance correction coefficient for I-rail tap0 on chain 0 Reset State: 0x0000

0x3000804+0x20*n CAL_IQ_CORR_COEFF_MEMn_1, n=[0..39]

Type: read-write
Reset State: 0x0000

Contains RX IQ imbalance correction coefficients for each RF gain setting

CAL_IQ_CORR_COEFF_MEMn_1

Bits	Name	Description
15:11	C0_I3_0	2's complement IQ imbalance correction coefficient for I-rail tap3 on chain 0 Reset State: 0x0000
10:2	C0_I2	2's complement IQ imbalance correction coefficient for I-rail tap2 on chain 0 Reset State: 0x0000
1:0	C0_I1_1	2's complement IQ imbalance correction coefficient for I-rail tap1 on chain 0 Reset State: 0x0000

0x3000808+0x20*n CAL_IQ_CORR_COEFF_MEMn_2, n=[0..39]

Type: read-write
Reset State: 0x0000

Contains RX IQ imbalance correction coefficients for each RF gain setting

CAL_IQ_CORR_COEFF_MEMn_2

Bits	Name	Description
15:13	C0_Q0_0	2's complement IQ imbalance correction coefficient for Q-rail tap0 on chain 0 Reset State: 0x0000
12:4	C0_I4	2's complement IQ imbalance correction coefficient for I-rail tap4 on chain 0 Reset State: 0x0000
3:0	C0_I3_1	2's complement IQ imbalance correction coefficient for I-rail tap3 on chain 0 Reset State: 0x0000

0x300080C+0x20*n CAL_IQ_CORR_COEFF_MEMn_3, n=[0..39]

Type: read-write
Reset State: 0x0000

Contains RX IQ imbalance correction coefficients for each RF gain setting

CAL_IQ_CORR_COEFF_MEMn_3

Bits	Name	Description
15	C0_Q2_0	2's complement IQ imbalance correction coefficient for Q-rail tap2 on chain 0 Reset State: 0x0000
14:6	C0_Q1	2's complement IQ imbalance correction coefficient for Q-rail tap1 on chain 0 Reset State: 0x0000
5:0	C0_Q0_1	2's complement IQ imbalance correction coefficient for Q-rail tap0 on chain 0 Reset State: 0x0000

0x3000810+0x20*n CAL_IQ_CORR_COEFF_MEMn_4, n=[0..39]

Type: read-write
Reset State: 0x0000

Contains RX IQ imbalance correction coefficients for each RF gain setting

CAL_IQ_CORR_COEFF_MEMn_4

Bits	Name	Description
15:8	C0_Q3_0	2's complement IQ imbalance correction coefficient for Q-rail tap3 on chain 0 Reset State: 0x0000
7:0	C0_Q2_1	2's complement IQ imbalance correction coefficient for Q-rail tap2 on chain 0 Reset State: 0x0000

0x3000814+0x20*n CAL_IQ_CORR_COEFF_MEMn_5, n=[0..39]

Type: read-write
Reset State: 0x0000

Contains RX IQ imbalance correction coefficients for each RF gain setting

CAL_IQ_CORR_COEFF_MEMn_5

Bits	Name	Description
9:1	C0_Q4	2's complement IQ imbalance correction coefficient for Q-rail tap4 on chain 0 Reset State: 0x0000

CAL_IQ_CORR_COEFF_MEMn_5 (cont.)

Bits	Name	Description
0	C0_Q3_1	2's complement IQ imbalance correction coefficient for Q-rail tap3 on chain 0 Reset State: 0x0000

16.2.14 fft

0x3000000+0x8*n FFT_FFT_RAM_0n_0, n=[0..255]

Type: read-write
Reset State: 0x0000

Ping-Pong FFT Reorder RAM shared by all receive chains.

FFT_FFT_RAM_0n_0

Bits	Name	Description
15:12	IMAG_DATA0_0	12-bit image data for Rx antenna 0 Reset State: 0x0000
11:0	REAL_DATA0	12-bit real data for Rx antenna 0 Reset State: 0x0000

0x3000004+0x8*n FFT_FFT_RAM_0n_1, n=[0..255]

Type: read-write
Reset State: 0x0000

Ping-Pong FFT Reorder RAM shared by all receive chains.

FFT_FFT_RAM_0n_1

Bits	Name	Description
7:0	IMAG_DATA0_1	12-bit image data for Rx antenna 0 Reset State: 0x0000

0x3000800+0x8*n FFT_FFT_RAM_1n_0, n=[0..255]

Type: read-write
Reset State: 0x0000

Ping-Pong FFT Reorder RAM shared by all receive chains.

FFT_FFT_RAM_1n_0

Bits	Name	Description
15:12	IMAG_DATA0_0	12-bit image data for Rx antenna 0 Reset State: 0x0000
11:0	REAL_DATA0	12-bit real data for Rx antenna 0 Reset State: 0x0000

0x3000804+0x8*n FFT_FFT_RAM_1n_1, n=[0..255]

Type: read-write
Reset State: 0x0000

Ping-Pong FFT Reorder RAM shared by all receive chains.

FFT_FFT_RAM_1n_1

Bits	Name	Description
7:0	IMAG_DATA0_1	12-bit image data for Rx antenna 0 Reset State: 0x0000

0x3001000 FFT_APB_ACCESS

Type: read-write
Reset State: 0x0000

This register controls APB access of the FFT Reorder RAM.

FFT_APB_ACCESS

Bits	Name	Description
0	APB_MODE	APB access enable bit - internal memory may be accessed only when this bit is asserted Reset State: 0x0000

0x3001004 FFT_FFT_TOGGLE

Type: read-only

This register is a 1-bit counter that is updated at the end of each FFT block.

FFT_FFT_TOGGLE

Bits	Name	Description
0	COUNT	FFT block count

16.2.15 mpi

0x3000000 MPI_WATCHDOG_MAX_COMMAND1

Type: read-write
Reset State: 0x0000

Allowed time for state machine to remain in COMMAND1 state

MPI_WATCHDOG_MAX_COMMAND1

Bits	Name	Description
15:0	CYCLES	Allowed period of time in this state = (Register value * 128 * 12.5)ns. The state machine automatically adjusts for 20/40/80MHz bandwidth settings. Setting a value of 0 disables the watchdog. Reset State: 0x0000

0x3000004 MPI_WATCHDOG_MAX_COMMAND2

Type: read-write
Reset State: 0x0000

Allowed time for state machine to remain in COMMAND2 state

MPI_WATCHDOG_MAX_COMMAND2

Bits	Name	Description
15:0	CYCLES	Allowed period of time in this state = (Register value * 128 * 12.5)ns. The state machine automatically adjusts for 20/40/80MHz bandwidth settings. Setting a value of 0 disables the watchdog. Reset State: 0x0000

0x3000008 MPI_WATCHDOG_MAX_WAIT

Type: read-write
Reset State: 0x0000

Allowed time for state machine to remain in WAIT state

MPI_WATCHDOG_MAX_WAIT

Bits	Name	Description
15:0	CYCLES	Allowed period of time in this state = (Register value * 128 * 12.5)ns. The state machine automatically adjusts for 20/40/80MHz bandwidth settings. Setting a value of 0 disables the watchdog. Reset State: 0x0000

0x300000C MPI_WATCHDOG_MAX_TRANSFER

Type: read-write
Reset State: 0x0000

Allowed time for state machine to remain in TRANSFER state

MPI_WATCHDOG_MAX_TRANSFER

Bits	Name	Description
15:0	CYCLES	Allowed period of time in this state = (Register value * 128 * 12.5)ns. The state machine automatically adjusts for 20/40/80MHz bandwidth settings. Setting a value of 0 disables the watchdog. Reset State: 0x0000

0x3000010 MPI_MAX_REQAORB

Type: read-write
Reset State: 0x0000

Holds the maximum number of txa or txb requests per packet that should be allowed during transmit. Default value of 0 disables the reporting of max_request_exceeded violation

MPI_MAX_REQAORB

Bits	Name	Description
15:0	VALUE	Reset State: 0x0000

0x3000014 MPI_COMMAND2_DELAY

Type: read-write
Reset State: 0x026C

Delay between end of first 4 bytes of COMMAND and start of rest of COMMAND. The state machine automatically adjusts for 20/40/80MHz bandwidth settings.

MPI_COMMAND2_DELAY

Bits	Name	Description
15:0	VALUE	Reset State: 0x026C

0x3000018 MPI_MPI_ENABLE

Type: read-write
Reset State: 0x0000

This register must be set to 0x1 for the MPI to respond to TXP signals. This register is used to disable the MPI during MAC loopback tests.

MPI_MPI_ENABLE

Bits	Name	Description
0	VALUE	Reset State: 0x0000

0x300001C MPI_TXP_MPI_START

Type: write-only

Counts number of TXP_MPI_START events received by TX Mac-PHY Interface module.

MPI_TXP_MPI_START

Bits	Name	Description
15:0	COUNT	TXP_MPI_START event counter.

0x3000020 MPI_MPI_TXP_REQ

Type: write-only

Counts number of MPI_TXP_REQ generated by TX MAC-PHY Interface module.

MPI_MPI_TXP_REQ

Bits	Name	Description
15:0	COUNT	MPI_TXP_REQ event counter.

0x3000024 MPI_TXA_MPI_DATA_REQ

Type: write-only

Counts number of TXA_MPI_DATA_REQ events received by TX Mac-PHY Interface module.

MPI_TXA_MPI_DATA_REQ

Bits	Name	Description
15:0	COUNT	TXA_MPI_DATA_REQ event counter.

0x3000028 MPI_TXB_MPI_DATA_REQ

Type: write-only

Counts number of TXB_MPI_DATA_REQ events received by TX Mac-PHY Interface module.

MPI_TXB_MPI_DATA_REQ

Bits	Name	Description
15:0	COUNT	TXB_MPI_DATA_REQ event counter.

0x300002C MPI_TXP_MPI_DATA_VAL

Type: write-only

Counts number of TXP_MPI_DATA_VAL pulses received.

MPI_TXP_MPI_DATA_VAL

Bits	Name	Description
15:0	COUNT	TXP_MPI_DATA_VAL event counter.

0x3000030 MPI_MPI_TXA_DATA_VAL

Type: write-only

Counts number of MPI_TXA_DATA_VAL generated by TX MAC-PHY Interface module.

MPI_MPI_TXA_DATA_VAL

Bits	Name	Description
15:0	COUNT	MPI_TXA_DATA_VAL event counter.

0x3000034 MPI_MPI_TXB_DATA_VAL

Type: write-only

Counts number of MPI_TXB_DATA_VAL generated by TX MAC-PHY Interface module.

MPI_MPI_TXB_DATA_VAL

Bits	Name	Description
15:0	COUNT	MPI_TXB_DATA_VAL event counter.

0x3000038 MPI_MPI_TXA_LASTBYTE

Type: write-only

Counts number of MPI_TXA_LASTBYTE generated by TX MAC-PHY Interface module.

MPI_MPI_TXA_LASTBYTE

Bits	Name	Description
15:0	COUNT	MPI_TXA_LASTBYTE event counter.

0x300003C MPI_MPI_TXA_CW_LASTBYTE

Type: write-only

Counts number of MPI_TXA_CW_LASTBYTE generated by TX MAC-PHY Interface module.

MPI_MPI_TXA_CW_LASTBYTE

Bits	Name	Description
15:0	COUNT	MPI_TXA_CW_LASTBYTE event counter.

0x3000040 MPI_MPI_TXA_CW_MAX_PARITY

Type: write-only

Counts number of MPI_TXA_CW_MAX_PARITY generated by TX MAC-PHY Interface module.

MPI_MPI_TXA_CW_MAX_PARITY

Bits	Name	Description
15:0	COUNT	MPI_TXA_CW_MAX_PARITY event counter.

0x3000044 MPI_MPI_STATE

Type: read-only

Stores the last 4 MPI states.

MPI_MPI_STATE

Bits	Name	Description
15:0	VALUE	Bit[15:12] = Previous MPI state (N-3) Bit[11:8] = Previous MPI state (N-2) Bit[7:4] = Previous MPI state (N-1) Bit[3:0] = Current MPI state

0x3000048 MPI_IDLE_FLAG

Type: read-only

Indicates current state of the IDLE flag.

MPI_IDLE_FLAG

Bits	Name	Description
0	VALUE	

0x300004C MPI_REQ_ALARM

Type: write-only

Counts number of REQ_ALARM abort pulses generated by TX MAC-PHY Interface module (when too many MPI requests were issued or if contiguous request pulses received).

MPI_REQ_ALARM

Bits	Name	Description
15:0	COUNT	

0x3000050 MPI_WATCHDOG_ALARM

Type: write-only

Counts number of WATCHDOG_ALARM abort pulses generated by TX MAC-PHY Interface module.

MPI_WATCHDOG_ALARM

Bits	Name	Description
15:0	COUNT	

0x3000054 MPI_COMMAND_ALARM

Type: write-only

Counts number of times that a command word was received when data was expected by the TX MAC-PHY Interface module and vice versa.

MPI_COMMAND_ALARM

Bits	Name	Description
15:0	COUNT	

0x3000058 MPI_TXP_ABORT

Type: write-only

Counts number of times that an abort was received from the TXP.

MPI_TXP_ABORT

Bits	Name	Description
15:0	COUNT	

0x300005C MPI_TXCTL_ABORT

Type: write-only

Counts number of times that an abort was received from the TXCTL.

MPI_TXCTL_ABORT

Bits	Name	Description
15:0	COUNT	

16.2.16 phydbg

0x3000000 PHYDBG_CFGMODE

Type: read-write
Reset State: 0x0000

This register configures basic modes of the capture and playback controllers in phydbg module. In all registers, fields with a suffix of 0 affect the capture controller and fields with a suffix of 1 affect the playback controller.

PHYDBG_CFGMODE

Bits	Name	Description
15	ENB_TESTBUS_OUTPUT	When high the testbus is output. This uses the phydbg mif write fifo, so no capture of data to the mif is possible while this is set. Reset State: 0x0000
13	DBGMEM_SEL1	High use debug SRAM for playback; Low use packet SRAM for playback. If dbgmem_sel0 and dbgmem_sel1 are both high then playback will use the lower half of debug SRAM. Reset State: 0x0000
12	STOP1	High to terminate playback after current packet. Reset State: 0x0000
8	CONT1	High for continuous playback; Low for single-shot playback. Reset State: 0x0000
7	TESTBUS_VITSEL0	High to select combo mux vital signals to testbus; Low to select combo mux data to testbus. Reset State: 0x0000
6	DBGMEM_SEL0	High use debug SRAM for capture; Low use packet SRAM for capture. If dbgmem_sel0 and dbgmem_sel1 are both high then capture will use the upper half of debug SRAM. Reset State: 0x0000
5	CRCCAPTURE0	High to select CRC based capture; Low normal capture mode. Reset State: 0x0000
4	STOP0	This field is used only if cont0 is high and seltrig[stop] configuration is set. High to terminate continuous capture. Reset State: 0x0000
3	SC0	High to select start trigger as the start condition for capture; Low to capture as soon as 'start' is set. Reset State: 0x0000
2	EC0	High to select end trigger as the stop condition for capture; Low to select max address or full length of RAM as the stop condition. Reset State: 0x0000
1	CONT0	High for continuous capture; Low for single-shot capture. Reset State: 0x0000

0x3000004 PHYDBG_SELTRIG

Type: read-write
Reset State: 0x0000

Selects which of the triggers will be used as triggers for start, end and stop condition.

PHYDBG_SELTRIG

Bits	Name	Description
12	AMPDU_CRC	If set, then crc trigger conditions are related to AMPDU packets otherwise, they relate to MPDU packets. Reset State: 0x0000
10:8	STOP0	Selects between various events to terminate continuous capture. AGC and CRC stop conditions are intended for use with CRC capture mode. 0x0: REG 0x1: AGC 0x2: GPIO 0x4: NOAGC 0x5: CRCPASS 0x6: CRCFAIL Reset State: 0x0000
6:4	ETRIG0	Selects between various sources of end trigger for the capture controller 0x0: TBUS 0x1: AGC 0x2: GPIO 0x4: CRCDONE 0x5: CRCPASS 0x6: CRCFAIL Reset State: 0x0000
2:0	STRIG0	Selects between various sources of start trigger for the capture controller 0x0: TBUS 0x1: AGC 0x2: GPIO 0x4: CRCDONE 0x5: CRCPASS 0x6: CRCFAIL 0x7: DISABLED Reset State: 0x0000

0x3000008 PHYDBG_RST0

Type: command
Reset State: 0x0000

Resets capture controller

PHYDBG_RST0

Bits	Name	Description
0	RST	When this register is written, a pulse of width same as clock period is generated Reset State: 0x0000

0x300000C PHYDBG_RST1

Type: command
Reset State: 0x0000

Resets playback controller

PHYDBG_RST1

Bits	Name	Description
0	RST	When this register is written, a pulse of width same as clock period is generated Reset State: 0x0000

0x3000010 PHYDBG_START0

Type: command
Reset State: 0x0000

Reference pulse for starting capture controller

PHYDBG_START0

Bits	Name	Description
0	START	When this register is written, a pulse of width same as clock period is generated that starts the capture controller state machine. Reset State: 0x0000

0x3000014 PHYDBG_START1

Type: command
Reset State: 0x0000

Reference pulse for starting the playback controller

PHYDBG_START1

Bits	Name	Description
0	START	When this register is written, a pulse of width same as clock period is generated that starts the playback controller. Reset State: 0x0000

0x3000018 PHYDBG_STATUS

Type: read-only

Status Register of the capture and playback controllers.

PHYDBG_STATUS

Bits	Name	Description
13	RDBUSY	Status of playback controller (gen_raddr) during read. High for busy.
12:8	TXSTATE	Current state of packet generator (gen_txdata) FSM 0x0: IDLE 0x1: INFD0 0x2: INFD1 0x3: WARMUP 0x4: CLKSTART0 0x5: CLKSTART1 0x6: CLKSTART2 0x7: CLKSTART3 0x8: CMD_START 0x9: CMD 0xA: CMD_WAIT 0xB: PYLDF 0xC: PYLDF_WAIT 0xD: PYLDR 0xE: PYLDR_WAIT 0xF: CRC 0x10: CRC_WAIT 0x11: FLUSH 0x12: TXDONEWAIT 0x13: TIFWAIT
4:0	WRSTATE	Current state of capture controller (gen_waddr) FSM. 0x1: IDLE 0x2: START 0x4: WRWAIT 0x8: WRACTIVE 0x10: WRPOST

0x300001C PHYDBG_DELAY0

Type: read-write
Reset State: 0x0000

Delay capture from the start trigger.

PHYDBG_DELAY0

Bits	Name	Description
15:0	DLY	Number of clocks to wait after the start condition (Ref CFGMODE[sc0]) before starting capture. Reset State: 0x0000

0x3000020 PHYDBG_TRIGPTR0

Type: read-only

Indicates the RAM address to which the phydbg data was being written to when the end trigger came

PHYDBG_TRIGPTR0

Bits	Name	Description
13:0	TRIGPTR	In capture modes involving end trigger, the memory address wraps around the full length of memory. This refers to the last address of the memory to which the data was written to, when the end trigger came. With the length of memory of L, if the value of this register is sampled as T, the previous data is stored contiguously from locations T+1 ... L-1, 0, 1 ... T.

0x3000024 PHYDBG_TMUX_STRBQUAL

Type: read-write
Reset State: 0x0000

Data qualifier for the tmux input data

PHYDBG_TMUX_STRBQUAL

Bits	Name	Description
13:11	STRBDIV0	Captures very n+1 strobed pieces of data. Reset State: 0x0000

PHYDBG_TMUX_STRBQUAL (cont.)

Bits	Name	Description
10:8	STRBSEL0	Strobe source select and generator 0x0: STRB_NORMAL 0x1: STRB_TMUX 0x2: STRB_VIT 0x3: STRB_ALL Reset State: 0x0000
6:0	STRBPOS0	Bit position of capture strobe from testmux data or vital signals Reset State: 0x0000

0x3000028 PHYDBG_CAPT_CFG

Type: read-write
Reset State: 0x0000

Selects which of the input data will be captured in the associated memories. Note that the selection for capture to memory is done for up to 128 bits of data, depending on [MEM_CFG] setting. Only 54 bits can be output on the testbus. See also register CAPT_CFG2.

PHYDBG_CAPT_CFG

Bits	Name	Description
13:8	XBARSEL	Multiplexer select for 80MHz domain signals (i.e.. ADC, RXFIR and DAC data). The available modes depend on the number of TX and RX chains in the device. 0x0: C32_ADC_CH0 0x4: C32_RXF20_CH0 0x8: C32_RXF40_CH0 0xC: C32_RXF80_CH0 0x20: C32_DAC_CH0 Reset State: 0x0000
7	RFSAT_GAIN_SEL	High to capture rxgainN[0] in place of rfsatN bits. Reset State: 0x0000
6:4	VITSEL	Multiplexer select lines for vital bus mux for memory capture or testbus or trigger selection logic. 0x0: VITSEL_RXA 0x1: VITSEL_RXB 0x2: VITSEL_RXSM 0x3: VITSEL_TX 0x4: VITSEL_AGC 0x5: VITSEL_PMI Reset State: 0x0000

PHYDBG_CAPT_CFG (cont.)

Bits	Name	Description
3:0	DATASEL	Multiplexer select lines for data mux for memory capture or testbus. 0x0: SEL_XBAR 0x1: SEL_AGC 0x2: SEL_RXA 0x3: SEL_TX 0x4: SEL_RAVIT 0x5: SEL_RBVIT 0x6: SEL_RXFSM 0x7: SEL_TXVIT 0x8: SEL_PMI 0x9: SEL_AGCVIT Reset State: 0x0000

0x300002C PHYDBG_CAPT_CFG2

Type: read-write
Reset State: 0x0000

Selects which of the input data will be captured in the associated memories. Note that the selection for capture to memory is done for up to 128 bits of data, depending on [MEM_CFG] setting. Only 54 bits can be output on the testbus. See also register CAPT_CFG.

PHYDBG_CAPT_CFG2

Bits	Name	Description
0	XBAR_PIC_DATASEL	Multiplexer select line for selecting between xbar data iq values and post IQ Corrected data. This applies for all capture modes. 0x0: LO 0x1: HI Reset State: 0x0000

0x3000030 PHYDBG_START_TRIGWD0

Type: read-write
Reset State: 0x0000

This register specifies the current state and new state of AGC main state machine, the transition between which will cause a pulse to be generated. That can be used as a trigger to capture the required data selected by SELECT register.

PHYDBG_START_TRIGWD0

Bits	Name	Description
10	ENB	High to enable trigger. Reset State: 0x0000
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x3000034 PHYDBG_END_TRIGWD0

Type: read-write
Reset State: 0x0000

This register specifies the current state and new state of AGC main state machine, the transition between which will cause a pulse to be generated. That can be used as a trigger to capture the required data selected by SELECT register.

PHYDBG_END_TRIGWD0

Bits	Name	Description
10	ENB	High to enable trigger. Reset State: 0x0000
9:5	NEXT_STATE	State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	State from which transition originates. Reset State: 0x0000

0x3000038 PHYDBG_STOP_TRIGWD0

Type: read-write
Reset State: 0x0000

This register specifies the state of AGC main state machine that is detected to terminate crc-based capture.

PHYDBG_STOP_TRIGWD0

Bits	Name	Description
4:0	STATE	State to detect. Reset State: 0x0000

0x300003C PHYDBG_START_ADDR0

Type: read-write
Reset State: 0x0000

Specifies the start address of memory to be used for capture. The controller generates addresses from START_ADDR to MAX_ADDR. If MAX_ADDR is less than START_ADDR then capture will wrap-around at the top of memory.

PHYDBG_START_ADDR0

Bits	Name	Description
13:0	ADDR	Reset State: 0x0000

0x3000040 PHYDBG_MAX_ADDR0

Type: read-write
Reset State: 0x0000

Specifies the max address of memory to be used for capture. The controller generates addresses from 0 to MAXADDR.

PHYDBG_MAX_ADDR0

Bits	Name	Description
13:0	ADDR	Reset State: 0x0000

0x3000044 PHYDBG_START_ADDR1

Type: read-write
Reset State: 0x0000

Specifies the start address of memory to be used for playback. The controller generates addresses from START_ADDR to MAX_ADDR. If MAX_ADDR is less than START_ADDR then playback will wrap-around at the top of memory.

PHYDBG_START_ADDR1

Bits	Name	Description
13:0	ADDR	Reset State: 0x0000

0x3000048 PHYDBG_MAX_ADDR1

Type: read-write
Reset State: 0x0000

Specifies the max address of memory to be used for playback. The controller generates addresses from STARTADDR to MAXADDR.

PHYDBG_MAX_ADDR1

Bits	Name	Description
13:0	ADDR	Reset State: 0x0000

0x300004C PHYDBG_AGCRST

Type: read-write
Reset State: 0x0000

Enable register for AGC reset during playback mode

PHYDBG_AGCRST

Bits	Name	Description
0	EN	When high, will enable reset generated by playback controller Reset State: 0x0000

0x3000050 PHYDBG_TMUX_STRIG

Type: read-write
Reset State: 0x0000

Bit position of start trigger when generated from testmux data or vital signals

PHYDBG_TMUX_STRIG

Bits	Name	Description
8	INVERT0	Invert trigger bit. When 0, trigger on active high signal. When 1, trigger on active low signal. Reset State: 0x0000
7	SELFMVIT0	High to select TMUX_STRIG[pos0] and TMUX_STRIG[pos0] from muxed vital signals bus rather than muxed databus. Reset State: 0x0000

PHYDBG_TMUX_STRIG (cont.)

Bits	Name	Description
6:0	POS0	The signal in bit position indicated by this value will be used as a start trigger source for the capture controller (refer to the SELTRIG register description). Reset State: 0x0000

0x3000054 PHYDBG_TMUX_ETRIG

Type: read-write
Reset State: 0x0000

Bit position of end trigger when generated from testmux data or vital signals

PHYDBG_TMUX_ETRIG

Bits	Name	Description
8	INVERT0	Invert trigger bit. When 0, trigger on active high signal. When 1, trigger on active low signal. Reset State: 0x0000
6:0	POS0	The signal in bit position indicated by this value will be used as a end trigger source for the capture controller (refer to the SELTRIG register description). Reset State: 0x0000

0x3000058 PHYDBG_PLYBCK_CFG

Type: read-write
Reset State: 0x0000

Configures the phydbg playback modes

PHYDBG_PLYBCK_CFG

Bits	Name	Description
15:13	PLYBK_RATE	Set sample playback rate. 0x0: PLYBK_240M 0x1: PLYBK_160M 0x2: PLYBK_120M 0x3: PLYBK_80M 0x4: PLYBK_40M 0x5: PLYBK_20M Reset State: 0x0000

PHYDBG_PLYBCK_CFG (cont.)

Bits	Name	Description
12:8	TXPB_MODE	These bits control playback of TX sample data. 0x0: TXPB32_DISABLE 0x1: TXPB32_TXF80_CH0 0x5: TXPB32_DAC80_CH0 Reset State: 0x0000
7:3	RXPB_MODE	These bits control playback of RX sample data. 0x0: RXPB32_DISABLE 0xA: RXPB32_ADC80_CH0 Reset State: 0x0000
2	TXAIF_DBGSEL	When high, tx_aif will select phydbg data. Reset State: 0x0000
1	TXFIR_DBGSEL	When high, tx_fir will select phydbg data. Reset State: 0x0000
0	MPI_TXTEST	When high, the data from phydbg is used in tx-mpi in place of tfp inputs Reset State: 0x0000

0x300005C PHYDBG_PLYBCK_CFG2

Type: read-write
Reset State: 0x0000

Controls playback data from memory.

PHYDBG_PLYBCK_CFG2

Bits	Name	Description
6:5	TX_ATTENUATION	specifies the attenuation for tx playback. From 0 to 18db in 6db increments. Reset State: 0x0000
4:0	ADDR_INC	specifies the address increment value for playback from memory. Increment will be (addr_inc + 1), giving a range of 1 to 32. Reset State: 0x0000

0x3000060 PHYDBG_PRBS

Type: read-write
Reset State: 0x00FF

Initializes PRBS generator for MPI packet generator.

PHYDBG_PRBS

Bits	Name	Description
15	AUTO_RELOAD	Reload the prbs for every packet transmitted. Reset State: 0x0000
7:0	SEED_LSB	LSB of the prbs seed Reset State: 0x00FF

0x3000064 PHYDBG_PRBS_MS

Type: read-write
Reset State: 0xFFFF

Most significant word of the prbs seed

PHYDBG_PRBS_MS

Bits	Name	Description
15:0	SEED_MSW	MSW of the prbs seed Reset State: 0xFFFF

0x3000068 PHYDBG_PRBS_LOAD

Type: command
Reset State: 0x0000

Loads PRBS generator with seed specified in {PRBS_MS, PRBS[7:0]} registers

PHYDBG_PRBS_LOAD

Bits	Name	Description
0	LOAD	When this register is written, a pulse of width same as clock period is generated Reset State: 0x0000

0x300006C PHYDBG_TXPKT_CNT

Type: read-write
Reset State: 0x0001

Max number of packets that will be driven to mpi interface from memory. This field is ignored when CFGMODE[cpm1] is high.

PHYDBG_TXPKT_CNT

Bits	Name	Description
15:0	CNT	Reset State: 0x0001

0x3000070 PHYDBG_RXPKT_CNT

Type: write-only

Incremented for each packet received that matches the pattern specified in RXPKT_FLTRn and with correct CRC.

PHYDBG_RXPKT_CNT

Bits	Name	Description
15:0	CNT	Write zero to clear.

0x3000074 PHYDBG_CAPTCNT

Type: write-only

Incremented for each word written to SRAM.

PHYDBG_CAPTCNT

Bits	Name	Description
15:0	CNT	Write zero to clear.

0x3000078 PHYDBG_POSTTRIGCNT

Type: read-write
Reset State: 0x0000

Number of words of data captured after the end-trigger condition in the post-trigger capture mode (used with CRC capture mode). Must be less than size of available capture memory.

PHYDBG_POSTTRIGCNT

Bits	Name	Description
13:0	CNT	Reset State: 0x0000

0x300007C PHYDBG_WARMUP_DLY

Type: read-write
Reset State: 0x0000

Sets the duration of RF warmup as a multiple of the Phy clock period. Setting to zero will keep the warmup signal continuously asserted.

PHYDBG_WARMUP_DLY

Bits	Name	Description
15:0	DLY	Reset State: 0x0000

0x3000080 PHYDBG_RXPKT_FILTER_10

Type: read-write
Reset State: 0x0000

2 bytes of the RX packet filter pattern for CRC check. All-zeros pattern disables filtering.

PHYDBG_RXPKT_FILTER_10

Bits	Name	Description
15:0	DATA	Reset State: 0x0000

0x3000084 PHYDBG_RXPKT_FILTER_32

Type: read-write
Reset State: 0x0000

2 bytes of the RX packet filter pattern for CRC check. All-zeros pattern disables filtering.

PHYDBG_RXPKT_FILTER_32

Bits	Name	Description
15:0	DATA	Reset State: 0x0000

0x3000088 PHYDBG_PLYBKCNT

Type: write-only

Increment for each packet transmitted when mpi_txtest is high. Not used when mpi_txtest is low.

PHYDBG_PLYBKCNT

Bits	Name	Description
15:0	CNT	Write zero to clear.

0x300008C PHYDBG_AMPDU_RXPKT_CNT

Type: write-only

Incremented for each AMPDU packet received with correct CRC.

PHYDBG_AMPDU_RXPKT_CNT

Bits	Name	Description
15:0	CNT	Write zero to clear.

0x3000090 PHYDBG_AUTO_TRIG_PLAYBACK1

Type: read-write
Reset State: 0x0000

This register controls the automatic data playback trigger. The trigger can be either the AGC state machine transitioning from one state to another, or the gpio trigger

PHYDBG_AUTO_TRIG_PLAYBACK1

Bits	Name	Description
11	GPIO_ENB	High to enable gpio auto playback trigger, overrides the "enb" for agc. Reset State: 0x0000
10	ENB	High to enable agc auto playback trigger. Reset State: 0x0000
9:5	NEXT_STATE	Agc State in which transition ends. Reset State: 0x0000
4:0	CURRENT_STATE	AGC State from which transition originates. Reset State: 0x0000

0x3000094 PHYDBG_AUTO_TRIG_PLAYBACK_DELAY1

Type: read-write
Reset State: 0x0000

Indicates the number of clk160 clocks to count before triggering the start of the transmit packet after detecting the agc state transition. In volans the clk160 is running at 80MHz, so the range is 0 to 819us in 12.5ns increments.

PHYDBG_AUTO_TRIG_PLAYBACK_DELAY1

Bits	Name	Description
15:0	DELAY	Reset State: 0x0000

0x3000098 PHYDBG_AUTO_TRIG_PLAYBACK_TIMEOUT_DELAY1

Type: read-write
Reset State: 0x0000

Indicates the number of clk160 clocks to count before initiating a transmit packet. This is to deal with the possibility that the AGC will not detect the incoming packet, and as a result no more packets being transmitted. The delay is will be "delay x 4096" clocks. In volans the clk160 is running at 80MHz, so the range is 0 to 209ms in 51.2us increments.

PHYDBG_AUTO_TRIG_PLAYBACK_TIMEOUT_DELAY1

Bits	Name	Description
11:0	DELAY	Reset State: 0x0000

0x300009C PHYDBG_GPIO_OUT_TRIG

Type: read-write
Reset State: 0x0000

Select the source to be used for gpio output trigger.

PHYDBG_GPIO_OUT_TRIG

Bits	Name	Description
2:0	SELECT	Multiplexer select which source to use for the gpio output trigger. 0x0: GPIO_DISABLE 0x1: GPIO_START 0x2: GPIO_END 0x3: GPIO_STOP 0x4: GPIO_AUTO Reset State: 0x0000

0x3002000+0x8*n PHYDBG_DBGMEMn_0, n=[0..1023]

Type: read-write
Reset State: 0x0000

Read/write access to phydbg internal memory.

PHYDBG_DBGMEMn_0

Bits	Name	Description
15:0	DATA_0	Reset State: 0x0000

0x3002004+0x8*n PHYDBG_DBGMEMn_1, n=[0..1023]

Type: read-write
Reset State: 0x0000

Read/write access to phydbg internal memory.

PHYDBG_DBGMEMn_1

Bits	Name	Description
15:0	DATA_1	Reset State: 0x0000

16.2.17 phyint

0x3000000 PHYINT_STATUS

Type: read-write
Reset State: 0x0000

This register consolidates all the interrupt requests on Phy. All interrupt requests are active high. Interrupt bit fields ending in "_P" can be cleared by writing a "1" to the corresponding bit in this register. Interrupt bit fields not ending in "_P" must be cleared at source.

PHYINT_STATUS

Bits	Name	Description
14	AGC_WATCHDOG_EXP	AGC FSM watchdog timer expired Reset State: 0x0000
13	TAHDR_INVLD_RATE	Txa header processor found a bad rate field from mpi data *** This interrupt does not exist in Gen5/6 *** Reset State: 0x0000

PHYINT_STATUS (cont.)

Bits	Name	Description
12	PMI_ALARM_P	The alarm condition in PMI Reset State: 0x0000
11	RACTL_ALARM_P	The alarm condition in RACTL Reset State: 0x0000
10	RBHPC_SOFEOFATN_P	The sof/eof interrupt from the RXB Reset State: 0x0000
9	TXCTL_ALARM_P	The interrupt from overall Tx Controller indicating error condition inside Phy TX Reset State: 0x0000
8	TACTL_ALARM_P	The interrupt from TACTL indicating error condition inside Phy Txa Reset State: 0x0000
7	MPI_MAXREQATN_P	The interrupt from MAC-Phy Interface (MPI) block indicating too many requests from txa or txb controller engines The threshold is configurable in mpi.reg Reset State: 0x0000
6	MPI_WATCHDOG_P	The interrupt from MAC-Phy Interface (MPI) block indicating expiry of watchdog timer Reset State: 0x0000
5	MPI_TXPABORT_P	The interrupt from MAC-Phy Interface (MPI) block indicating Txp abort Reset State: 0x0000
4	TPC_ATN_P	The interrupt from Transmit Power Control (TPC) block signifying error in tpc loop convergence. Reset State: 0x0000
3	CAL_ATN_P	The interrupt from the Calibration (CAL) block signifying calibration failure. Reset State: 0x0000
2	AGC_RADARDET_P	Set whenever the AGC detects radar. *** This interrupt does not exist in Libra *** Reset State: 0x0000
1	AGC_CLRCHAN_P	Set whenever the channel is clear, i.e., CCA is high. Reset State: 0x0000
0	RFIF_CALIB_DONE_P	Interrupt from Iris on calibration completion. ** NOTE ** this bit is used for agc_pktdet_n interrupt in Virgo ** ** NOTE ** this bit was used for indicating vswr overload in Libra and Volans ** Reset State: 0x0000

0x3000004 PHYINT_FAST_MASK

Type: read-write
Reset State: 0x0000

This register masks the Status register before the bits are combined to generate the fast interrupt to the embedded CPU. Setting a bit to "1" enables the interrupt, "0" masks the interrupt.

PHYINT_FAST_MASK

Bits	Name	Description
14	AGC_WATCHDOG_EXP	Fast mask bit for bit[14] in STATUS register. Reset State: 0x0000
13	TAHDR_INVLD_RATE	Fast mask bit for bit[13] in STATUS register. Reset State: 0x0000
12	PMI_ALARM_P	Fast mask bit for bit[12] in STATUS register. Reset State: 0x0000
11	RACTL_ALARM_P	Fast mask bit for bit[11] in STATUS register. Reset State: 0x0000
10	RBHPC_SOFEOFATN_P	Fast mask bit for bit[10] in STATUS register. Reset State: 0x0000
9	TXCTL_ALARM_P	Fast mask bit for bit[9] in STATUS register. Reset State: 0x0000
8	TACTL_ALARM_P	Fast mask bit for bit[8] in STATUS register. Reset State: 0x0000
7	MPI_MAXREQATN_P	Fast mask bit for bit[7] in STATUS register. Reset State: 0x0000
6	MPI_WATCHDOG_P	Fast mask bit for bit[6] in STATUS register. Reset State: 0x0000
5	MPI_TXPABORT_P	Fast mask bit for bit[5] in STATUS register. Reset State: 0x0000
4	TPC_ATN_P	Fast mask bit for bit[4] in STATUS register. Reset State: 0x0000
3	CAL_ATN_P	Fast mask bit for bit[3] in STATUS register. Reset State: 0x0000
2	AGC_RADARDET_P	Fast mask bit for bit[2] in STATUS register. Reset State: 0x0000
1	AGC_CLRCHAN_P	Fast mask bit for bit[1] in STATUS register. Reset State: 0x0000
0	RFIF_CALIB_DONE_P	Fast mask bit for bit[0] in STATUS register. Reset State: 0x0000

0x3000008 PHYINT_SLOW_MASK

Type: read-write
Reset State: 0x0000

This register masks the Status register before the bits are combined to generate the slow interrupt to the embedded CPU. Setting a bit to "1" enables the interrupt, "0" masks the interrupt.

PHYINT_SLOW_MASK

Bits	Name	Description
14	AGC_WATCHDOG_EXP	Slow mask bit for bit[14] in STATUS register. Reset State: 0x0000
13	TAHDR_INVLD_RATE	Slow mask bit for bit[13] in STATUS register. Reset State: 0x0000
12	PMI_ALARM_P	Slow mask bit for bit[12] in STATUS register. Reset State: 0x0000
11	RACTL_ALARM_P	Slow mask bit for bit[11] in STATUS register. Reset State: 0x0000
10	RBHPC_SOFEOFATN_P	Slow mask bit for bit[10] in STATUS register. Reset State: 0x0000
9	TXCTL_ALARM_P	Slow mask bit for bit[9] in STATUS register. Reset State: 0x0000
8	TACTL_ALARM_P	Slow mask bit for bit[8] in STATUS register. Reset State: 0x0000
7	MPI_MAXREQATN_P	Slow mask bit for bit[7] in STATUS register. Reset State: 0x0000
6	MPI_WATCHDOG_P	Slow mask bit for bit[6] in STATUS register. Reset State: 0x0000
5	MPI_TXPABORT_P	Slow mask bit for bit[5] in STATUS register. Reset State: 0x0000
4	TPC_ATN_P	Slow mask bit for bit[4] in STATUS register. Reset State: 0x0000
3	CAL_ATN_P	Slow mask bit for bit[3] in STATUS register. Reset State: 0x0000
2	AGC_RADARDET_P	Slow mask bit for bit[2] in STATUS register. Reset State: 0x0000
1	AGC_CLRCHAN_P	Slow mask bit for bit[1] in STATUS register. Reset State: 0x0000
0	RFIF_CALIB_DONE_P	Slow mask bit for bit[0] in STATUS register. Reset State: 0x0000

0x300000C PHYINT_HOST_MASK

Type: read-write
Reset State: 0x0000

This register masks the Status register before the bits are combined to generate the PCI/USB interrupt to the Host processor. Setting a bit to "1" enables the interrupt, "0" masks the interrupt.

PHYINT_HOST_MASK

Bits	Name	Description
14	AGC_WATCHDOG_EXP	Host mask bit for bit[14] in STATUS register. Reset State: 0x0000
13	TAHDR_INVLD_RATE	Host mask bit for bit[13] in STATUS register. Reset State: 0x0000
12	PMI_ALARM_P	Host mask bit for bit[12] in STATUS register. Reset State: 0x0000
11	RACTL_ALARM_P	Host mask bit for bit[11] in STATUS register. Reset State: 0x0000
10	RBHPC_SOFEOFATN_P	Host interrupt mask bit for bit[10] in STATUS register. Reset State: 0x0000
9	TXCTL_ALARM_P	Host interrupt mask bit for bit[9] in STATUS register. Reset State: 0x0000
8	TACTL_ALARM_P	Host interrupt mask bit for bit[8] in STATUS register. Reset State: 0x0000
7	MPI_MAXREQATN_P	Host interrupt mask bit for bit[7] in STATUS register. Reset State: 0x0000
6	MPI_WATCHDOG_P	Host interrupt mask bit for bit[6] in STATUS register. Reset State: 0x0000
5	MPI_TXPABORT_P	Host interrupt mask bit for bit[5] in STATUS register. Reset State: 0x0000
4	TPC_ATN_P	Host interrupt mask bit for bit[4] in STATUS register. Reset State: 0x0000
3	CAL_ATN_P	Host interrupt mask bit for bit[3] in STATUS register. Reset State: 0x0000
2	AGC_RADARDET_P	Host interrupt mask bit for bit[2] in STATUS register. Reset State: 0x0000
1	AGC_CLRCHAN_P	Host interrupt mask bit for bit[1] in STATUS register. Reset State: 0x0000
0	RFIF_CALIB_DONE_P	Host interrupt mask bit for bit[0] in STATUS register. Reset State: 0x0000

16.2.18 pmi

0x3000000 PMI_PMI_STATE

Type: read-only

Reflects the current value of the state machine.

PMI_PMI_STATE

Bits	Name	Description
2:0	VALUE	PMI state.

0x3000004 PMI_RXA_PKTS

Type: write-only

Counts number of single packets only.

PMI_RXA_PKTS

Bits	Name	Description
15:0	COUNT	RXA single packet event counter.

0x300000C PMI_RXB_PACKETS

Type: write-only

Counts number of RXB packets.

PMI_RXB_PACKETS

Bits	Name	Description
15:0	COUNT	RXB packet start event counter.

0x3000010 PMI_RXA_DATA_VALID

Type: write-only

Counts number of RXA data valid pulses.

PMI_RXA_DATA_VALID

Bits	Name	Description
15:0	COUNT	RXA data valid pulse counter.

0x3000014 PMI_RXB_DATA_VALID

Type: write-only

Counts number of RXB data valid pulses.

PMI_RXB_DATA_VALID

Bits	Name	Description
15:0	COUNT	RXB data valid pulse counter.

0x3000018 PMI_RXP_SHUTOFF

Type: write-only

Counts number of RXP shutoff pulses.

PMI_RXP_SHUTOFF

Bits	Name	Description
15:0	COUNT	RXP shutoff pulse counter.

0x300001C PMI_PHY_STARTS

Type: write-only

Counts number of RXP start pulses issued.

PMI_PHY_STARTS

Bits	Name	Description
15:0	COUNT	RXP start pulses counter.

0x3000020 PMI_PHY_DATA_VAL

Type: write-only

Counts number of RXP data valid pulses.

PMI_PHY_DATA_VAL

Bits	Name	Description
15:0	COUNT	RXP data valid pulses counter.

0x3000024 PMI_PHY_ABORT

Type: write-only

Counts number of RXP abort pulses.

PMI_PHY_ABORT

Bits	Name	Description
15:0	COUNT	RXP abort pulses counter.

0x3000028 PMI_PHY_INT

Type: write-only

Counts number of interrupt pulses.

PMI_PHY_INT

Bits	Name	Description
15:0	COUNT	PHYINT interrupt pulses counter.

0x300002C PMI_WATCHDOG_TIMEOUT_GENERAL

Type: read-write
Reset State: 0x0000

Max duration of non-idle time for PMI state machine before abort generated. Duration defined as (x*128 + 128) clocks, where x is the value in this register.

PMI_WATCHDOG_TIMEOUT_GENERAL

Bits	Name	Description
15:0	VALUE	PMI state machine general timeout value (disabled by default). Reset State: 0x0000

0x3000030 PMI_WATCHDOG_TIMEOUT_11A

Type: read-write
Reset State: 0x0015

Max duration of time between 11a data valids before abort generated. Duration defined as (x*128 + 128) clocks, where x is the value in this register.

PMI_WATCHDOG_TIMEOUT_11A

Bits	Name	Description
15:0	VALUE	PMI state machine 11a-dval timeout value (default value 21). Reset State: 0x0015

0x3000034 PMI_WATCHDOG_TIMEOUT_11B

Type: read-write
Reset State: 0x002A

Max duration of time between 11b data valids before abort generated. Duration defined as (x*128 + 128) clocks, where x is the value in this register.

PMI_WATCHDOG_TIMEOUT_11B

Bits	Name	Description
15:0	VALUE	PMI state machine 11b-dval timeout value (default value 42). Reset State: 0x002A

0x3000038 PMI_DISABLE_FLAGS

Type: read-write
Reset State: 0x0000

Various functionality enables.

PMI_DISABLE_FLAGS

Bits	Name	Description
2	STATS_UPDATE_DISABLE_FLAG	When asserted, this switch disables updating of the stats APB registers in the PMI. Reset State: 0x0000
1	CRC_DISABLE_FLAG	When asserted, this switch disables CRC checking in the PMI. Reset State: 0x0000
0	RXP_DISABLE_FLAG	When asserted, this switch disables all output to the RXP. Reset State: 0x0000

0x300003C PMI_CRC_FSM_RESET

Type: command
Reset State: 0x0000

Accessing this register will generate a pulse that resets the CRC FSM

PMI_CRC_FSM_RESET

Bits	Name	Description
0	PULSE	Reset State: 0x0000

0x3000040 PMI_RXPKT_FILTER_LSW

Type: read-write
Reset State: 0x0000

LS 2 bytes of the RX packet filter pattern for CRC check. All-zeros pattern disables filtering.

PMI_RXPKT_FILTER_LSW

Bits	Name	Description
15:0	DATA	Reset State: 0x0000

0x3000044 PMI_RXPKT_FILTER_MSW

Type: read-write
Reset State: 0x0000

MS 2 bytes of the RX packet filter pattern for CRC check. All-zeros pattern disables filtering.

PMI_RXPKT_FILTER_MSW

Bits	Name	Description
15:0	DATA	Reset State: 0x0000

0x3000048 PMI_CRC_DONE

Type: write-only

Number of packets that completed the CRC check.

PMI_CRC_DONE

Bits	Name	Description
15:0	COUNT	

0x300004C PMI_CRC_PASS

Type: write-only

Number of packets that passed the CRC check.

PMI_CRC_PASS

Bits	Name	Description
15:0	COUNT	

0x3000050 PMI_AMPDU_BAD

Type: write-only

Number of packets that failed the AMPDU CRC check.

PMI_AMPDU_BAD

Bits	Name	Description
15:0	COUNT	

0x3000054 PMI_AMPDU_GOOD

Type: write-only

Number of packets that passed the AMPDU CRC check.

PMI_AMPDU_GOOD

Bits	Name	Description
15:0	COUNT	

0x3000058 PMI_AMPDU_DONE

Type: write-only

Number of packets that completed the AMPDU CRC check.

PMI_AMPDU_DONE

Bits	Name	Description
15:0	COUNT	

0x300005C PMI_LAST_STATS0

Type: read-only

Last statistics data transferred to RXP, bits[15:0].

PMI_LAST_STATS0

Bits	Name	Description
15:0	DATA	

0x3000060 PMI_LAST_STATS1

Type: read-only

Last statistics data transferred to RXP, bits[31:16].

PMI_LAST_STATS1

Bits	Name	Description
15:0	DATA	

0x3000064 PMI_LAST_STATS2

Type: read-only

Last statistics data transferred to RXP, bits[47:32].

PMI_LAST_STATS2

Bits	Name	Description
15:0	DATA	

0x3000068 PMI_LAST_STATS3

Type: read-only

Last statistics data transferred to RXP, bits[63:48].

PMI_LAST_STATS3

Bits	Name	Description
15:0	DATA	

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0x3000000 RACTL_PTC_LOOP_EN

Type: read-write
Reset State: 0x003F

This registers provides the enable signals for the amplitude, frequency and channel tracking functions within the RXA PTC module. When each bit is asserted, the corresponding tracking loop is enabled.

RACTL_PTC_LOOP_EN

Bits	Name	Description
5	TIME_ADJ_EN	TDC timing adjustment enable. Reset State: 0x0001
4	PH_ADJ_EN	TDC phase adjustment enable. Reset State: 0x0001
3	CHAN_EN	Channel tracking enable. If asserted, PTC channel tracking loop will detect channel phase changes and modify the channel estimate samples received from the channel estimator module. Reset State: 0x0001
2	FREQ_EN	Frequency tracking enable. If asserted, PTC frequency tracking loop will track reference oscillator frequency drift and modify the phase of the incoming samples received from the phase imbalance corrector module. Reset State: 0x0001
1	AMP_EN_MIMO	Amplitude tracking enable for mimo symbols. If asserted, PTC amplitude tracking loop will track and modify the amplitude of the incoming samples received from the phase imbalance corrector module (mimo symbols only) Reset State: 0x0001
0	AMP_EN_SIMO	Amplitude tracking enable for simo symbols. If asserted, PTC amplitude tracking loop will track and modify the amplitude of the incoming samples received from the phase imbalance corrector module (simo symbols only) Reset State: 0x0001

0x3000004 RACTL_PTC_LOOP_GAIN

Type: read-write
Reset State: 0x002A

This registers provides the gain factors for the amplitude, frequency and channel tracking functions within the RXA PTC module.

RACTL_PTC_LOOP_GAIN

Bits	Name	Description
7:4	CHAN_GAIN	Channel tracking loop gain. 0x0: CGAIN_2 0x1: CGAIN_3 0x2: CGAIN_4 0x3: CGAIN_4TOO Reset State: 0x0002
3:2	FREQ_GAIN	Frequency tracking loop gain. 0x0: FGNO_AVG 0x1: FGAIN_2 0x2: FGAIN_3 0x3: FGAIN_4 Reset State: 0x0002
1:0	AMP_GAIN	Amplitude tracking loop gain. 0x0: AGNO_AVG 0x1: AGAIN_3 0x2: AGAIN_4 0x3: AGAIN_5 Reset State: 0x0002

0x3000008 RACTL_PTC_CHAN_FREQ

Type: read-write
Reset State: 0x087E

This value represents the ratio of sampling frequency to RF channel frequency using 10-bit quantisation

RACTL_PTC_CHAN_FREQ

Bits	Name	Description
11:0	PTC_CHAN_FREQ	Default setting = 12'd2174 Reset State: 0x087E

0x300000C RACTL_RACTL_TEST

Type: read-write
Reset State: 0x07B0

This register contains all the test mode flags for the RX-A controller

RACTL_RACTL_TEST

Bits	Name	Description
10	NDP_EN_11N	This bit enables the checking of NDP(ZLF) packets Reset State: 0x0001
9	FCM_EN_11N	This bit enables declaration of 256 QAM as supported rate in 11AC Reset State: 0x0001
8	RATE_EN_11N	This bit enables service-field-overloading for bw-capability exchange in legacy rts/cts frames. Default enabled, pmi byte5[6:4] gets data from de-scrambler input. Reset State: 0x0001
7	SSF_RESERVED_CHK_EN	This bit enables the SSF RESERVED field check mode. If not set, ESF packet reception is disabled. Ref register hexD4. NOTE - for Taurus, this bit is not used Reset State: 0x0001
6	DEBUG_MODE_EN	This bit controls if ractl should use watchdog mechanism to generate end-of-input-pkt. Reset State: 0x0000
5	RATE_CHK_EN	This bit enables the RATE field content check mode and enables assertion of the SHDR_INVALID or EHDR_INVALID flag to the AGC module if the RATE field does not contain a legal value. Reset State: 0x0001
4	SERVICE_EN	This bit enables the SERVICE field content check mode and enables assertion of the SERVICE_INVALID flag to the AGC module. Reset State: 0x0001
3	SOUNDING_BIT_CHK_EN	This bit (previously called parity_check_en) enables checking of sounding bit for unsupported htsig purpose (applies only to non-ndp packets) Reset State: 0x0000

0x3000010 RACTL_RXA_ABORT

Type: command
Reset State: 0x0000

Writing any value to this register instructs the RX-A controller to abort the current packet and return the RXA module to idle mode.

RACTL_RXA_ABORT

Bits	Name	Description
0	RXA_ABORT	Writing any value to this bit will trigger an abort of the RX-A module. Reading this register will return a 0 value. Reset State: 0x0000

0x3000014 RACTL_RACTL_TOFFSET

Type: read-write
Reset State: 0x0000

This register contains a timing offset value that is added to the timing correction value provided by the BTCF module. This addition takes place in the TDC module.

RACTL_RACTL_TOFFSET

Bits	Name	Description
7:0	RACTL_TOFFSET	Timing offset value fed to the TDC module. Default setting = 8'h0. Reset State: 0x0000

0x3000018 RACTL_RACTL_DELTAT_IN

Type: read-write
Reset State: 0x0000

This register contains a test value that overrides the timing correction value provided by the BTCF module.

RACTL_RACTL_DELTAT_IN

Bits	Name	Description
15	APB_DT_OVERRIDE	If asserted, the RACTL module passes the APB timing offset value to the TDC module instead of that received from BTCF. Reset State: 0x0000
8:0	APB_DT	Test BTCF timing correction value that overrides the internally-calculated value. Default setting = 8'h0. Reset State: 0x0000

0x300001C RACTL_RACTL_DELTAT_OUT

Type: read-only

This register allows the host to observe timing value that is fed to the TDC module

RACTL_RACTL_DELTAT_OUT

Bits	Name	Description
8:0	TDC_DT	Current timing correction value being used by TDC module provided by PTC Note the current timing adjust value is in PTC_DELTAAMP_TIMINGOFFSET_OUT register

0x3000020 RACTL_RACTL_DELTAF_IN

Type: read-write
Reset State: 0x0000

Test frequency correction value that overrides the value provided by the BTCF module.

RACTL_RACTL_DELTAF_IN

Bits	Name	Description
15	APB_DFUPDT_OVERRIDE	Use this to indicate PTC to use the initially received value rather than updating it. Reset State: 0x0000
14	APB_DFINIT_OVERRIDE	If asserted, the RACTL module passes the APB frequency error value to the TDC module instead of that received from BTCF. Reset State: 0x0000
9:0	APB_DF	Test frequency correction value that overrides the internally-calculated value. Default setting = 10'h0. Reset State: 0x0000

0x3000024 RACTL_RACTL_DELTAF_OUT

Type: read-only

Current frequency correction value being used by TDC module

RACTL_RACTL_DELTAF_OUT

Bits	Name	Description
11:0	PTC_DF	Current frequency correction value being used by TDC module

0x3000028 RACTL_PTC_DELTAAMP_TIMINGOFFSET_OUT

Type: read-only

Current frequency correction value being used by PTC module

RACTL_PTC_DELTAAMP_TIMINGOFFSET_OUT

Bits	Name	Description
9:8	PTC_DT	Current timing offset correction value being provided PTC to TDC
7:0	PTC_DA	Current amplitude correction value being used by PTC module

0x300002C RACTL_RACTL_TEST_SIG_LEN

Type: read-write
Reset State: 0xFFFF

Test SIGNAL field length value that overrides the internally-demodulated value.

RACTL_RACTL_TEST_SIG_LEN

Bits	Name	Description
15:0	RACTL_LENGTH	Test LENGTH field value that overrides the internally-demodulated value. Default setting = 16'hffff. Reset State: 0xFFFF

0x3000030 RACTL_RACTL_TEST_CFG

Type: read-write
Reset State: 0x0000

Contains test SIGNAL field rate values

RACTL_RACTL_TEST_CFG

Bits	Name	Description
5:2	RACTL_RATE	Test RATE field value that overrides the internally-demodulated value. Default setting = 4'h0. Reset State: 0x0000
1	LENGTH_OVRD_EN	This bit enables the use of APB LENGTH value rather than the LENGTH field decoded by RAHDR. Reset State: 0x0000
0	RATE_OVRD_EN	This bit enables the use of APB RATE value rather than the RATE field decoded by RAHDR. Reset State: 0x0000

0x3000034 RACTL_TESTMUX_SEL

Type: read-write
Reset State: 0x0014

Selector signals for the test busses from the RX-A module

RACTL_TESTMUX_SEL

Bits	Name	Description
15:13	RESERVED	RESERVED FOR FUTURE USE Reset State: 0x0000
12:11	RACTLTEST_HDRSELECT	0x0: Selects existing testbus in pktparams 1: Selects lsig and htsig (tail and crc on the msbs-see the 3 lsbs to determine the pkt-type 2: Selects lsig and vhtsiga tail and crc on the msbs-see the 3 lsbs to determine the pkt-type) Reset State: 0x0000
10:9	RACTLTEST_SELECT160	Selector signal for the RACTL testbus at 160 0 test0 1 160 domain signals involved in clock-domain-crossing 2, 3 - tdcintf and other 160M ractl-interface signals Reset State: 0x0000
8:7	RACTLTEST_SELECT8040	Selector signal for the RACTL vital testbus at 8040 0 vital0 1 vital1 2 - 8040 domain signals involved in clock-domain-crossing 3 - Ractl main state machine essential signals Reset State: 0x0000
6:0	TESTBUS_SELECT	Selector signal for the RX-A test bus Bit 6 will select between the vital signals at rxa_top (0) or vital signals from only ractl (1) Bit 5 will select between the signals in 80M (0) and 160M (1) domain Bit 4:0 will select the modules for which signals will be monitored in both 80M domain and 160M domains 4:0 80 / 8040 160 ---------- ---------- 0 fscale tdc,fft 1 btcf tdc1 2 tdc tdc2 3 ractl1 fft1 4 ractl2 fft2 5 ractl3 fft3 7 che 8 ptc1 9 ptc2 10 lmap 11 dint 12 vit 13 radscr 14 che-ptc 15 che-lmap 16 che-lmap 17 lmap snr 18 ractl 19 che new set in riva 20 che new set in riva 21-24 phycsxi che and lmap interface data Reset State: 0x0014

0x3000038 RACTL_RACTL_PKTCOUNT

Type: write-only

Number of packet burst start signals received by the RACTL module

RACTL_RACTL_PKTCOUNT

Bits	Name	Description
11:0	RACTL_SPKTCOUNT	Number of packet burst start signals received by the RACTL module from AGC

0x300003C RACTL_RACTL_SYMCOUNT

Type: write-only

Number of OFDM symbol start signals generated by the RACTL module

RACTL_RACTL_SYMCOUNT

Bits	Name	Description
15:0	RACTL_SYMCOUNT	Number of OFDM symbol start signals generated by the RACTL module

0x3000048 RACTL_PTC_PKTCOUNT

Type: write-only

Number of packet burst start signals received by the PTC module

RACTL_PTC_PKTCOUNT

Bits	Name	Description
11:0	PTC_SPKTCOUNT	Number of packet burst start signals received by the PTC module (all packet types)

0x300004C RACTL_PTC_SYMCOUNT

Type: write-only

Number of OFDM symbol start signals received by the PTC module

RACTL_PTC_SYMCOUNT

Bits	Name	Description
15:0	PTC_SYMCOUNT	Number of OFDM symbol start signals received by the PTC module

0x300005C RACTL_PTC_PKTCOUNT_20M

Type: write-only

Number of packet burst start signals received by the PTC module in 20MHz modes

RACTL_PTC_PKTCOUNT_20M

Bits	Name	Description
11:0	PTC_SPKTCOUNT_20M	Number of packet burst start signals received by the PTC module in 20MHz modes (all packet types) This includes the 20M 11n packets falsely detected as 40M packets

0x3000060 RACTL_PTC_PKTCOUNT_40M

Type: write-only

Number of packet burst start signals received by the PTC module in 40MHz modes

RACTL_PTC_PKTCOUNT_40M

Bits	Name	Description
11:0	PTC_SPKTCOUNT_40M	Number of packet burst start signals received by the PTC module in 40MHz and 80MHz modes (all packet types) This includes the 40M 11n packets falsely detected as 80M packets

0x3000064 RACTL_PTC_PKTCOUNT_SIMO

Type: write-only

Number of packet burst start signals received by the PTC module in simo mode

RACTL_PTC_PKTCOUNT_SIMO

Bits	Name	Description
11:0	PTC_SPKTCOUNT_SIMO	Number of packet burst start signals received by the PTC module in simo modes. This includes the 20M and 40M 11n and legacy mode packets but does not include stbc mode packets

0x3000074 RACTL_PTC_PKTCOUNT_STBC

Type: write-only

Number of packet burst start signals received by the PTC module in stbc modes

RACTL_PTC_PKTCOUNT_STBC

Bits	Name	Description
11:0	PTC_SPKTCOUNT_STBC	Number of packet burst start signals received by the PTC module in stbc modes. This includes the 20M and 40M 11n mode packets.

0x3000078 RACTL_FFT_OPSCALE

Type: read-write
Reset State: 0x0000

Amount of output attenuation to be applied by the FFT module

RACTL_FFT_OPSCALE

Bits	Name	Description
1:0	FFT_OPSCALE	Amount of output attenuation to be applied by the FFT module 0x0: GAIN_1 0x1: GAIN_1_2 0x2: GAIN_1_4 0x3: GAIN_1_8 Reset State: 0x0000

0x300007C RACTL_RACTL_STATE

Type: read-only

Current state of RACTL state machine

RACTL_RACTL_STATE

Bits	Name	Description
14:10	PREV1_STATE	Previous-but-1 state of RACTL state machine
9:5	PREV0_STATE	Previous state of RACTL state machine
4:0	CURRENT_STATE	Current state of RACTL state machine

0x3000080 RACTL_AGC_ABORT_COUNT

Type: write-only

Number of abort signals received from the AGC module

RACTL_AGC_ABORT_COUNT

Bits	Name	Description
15:0	AGC_ABORTCOUNT	Number of abort signals received from the AGC module

0x3000084 RACTL_SIGNAL_INVALID_COUNT_LSIG

Type: write-only

Number of packets received with invalid LEGACY SIGNAL field values

RACTL_SIGNAL_INVALID_COUNT_LSIG

Bits	Name	Description
15:0	INVALID_SFCOUNT	Number of packets received with invalid SIGNAL field values

0x3000088 RACTL_SERV_INVALID_COUNT

Type: write-only

Number of packets received with invalid SERVICE field values

RACTL_SERV_INVALID_COUNT

Bits	Name	Description
15:0	INVALID_SERVCOUNT	Number of packets received with invalid SERVICE field values

0x300008C RACTL_INTERRUPT_COUNT

Type: write-only

Combined number of interrupts received by RAHDR and RACTL

RACTL_INTERRUPT_COUNT

Bits	Name	Description
15:0	INTERRUPT_COUNT	Total number of interrupts. For Volans: Does not include the NDP packets that qualify for CSI transfer. Does not include the "Unsupported configuration" (Note that for Volans, 1rx 4ss configuration is allowed.)

0x3000090 RACTL_LAST_LS_SIGNAL

Type: read-only
Reset State: 0x0000

This register holds the LS 16 bits of the last decoded standard SIGNAL field value. On reset, the register is set to 0

RACTL_LAST_LS_SIGNAL

Bits	Name	Description
15:0	VALUE	LS 16 bits of the last decoded standard SIGNAL field Reset State: 0x0000

0x3000094 RACTL_LAST_MS_SIGNAL

Type: read-only
Reset State: 0x0000

This register holds the MS 16 bits of the last decoded standard SIGNAL field value. On reset, the register is set to 0

RACTL_LAST_MS_SIGNAL

Bits	Name	Description
7:0	VALUE	MS 8 bits of the last decoded standard SIGNAL field Reset State: 0x0000

0x3000098 RACTL_STATISTICS_SELECT

Type: read-write
Reset State: 0x0000

This register selects the format of the 8-byte stats field appended to the end of a received packet

RACTL_STATISTICS_SELECT

Bits	Name	Description
2:0	VALUE	Stats format selector 0x0: AGC_CONSOLIDATED1 0x1: AGC_CONSOLIDATED2 0x2: TDC_CONSOLIDATED 0x3: CAL_ONLY 0x4: KNOWN_PATTERN 0x5: FSCALE_CONSOLIDATED Reset State: 0x0000

0x300009C RACTL_AC_CHK

Type: read-write
Reset State: 0x0001

Supplies the configuration parameters to RAHDR

RACTL_AC_CHK

Bits	Name	Description
0	BW_MSB_CHECK	Asserted to indicate the vhtsiga bits [2:0] will be checked against agc bw [2:0] settings. 0 => vhtsiga bits [1:0] will be checked against agc bw [1:0] settings. Reset State: 0x0001

0x30000A0 RACTL_DAGC_TGTBO

Type: read-write
Reset State: 0x001E

Fscale Target Backoff for Digital Gain computation. The gain is set this amount of dBs below the gain that would fully saturate the receiver. The backoff is specified in 0.5 dB steps.

RACTL_DAGC_TGTBO

Bits	Name	Description
5:0	BACK_OFF	Backoff value. Default backoff is 30. Reset State: 0x001E

0x30000A4 RACTL_CMDWDFILL

Type: read-write
Reset State: 0x0003

Sets the options for software to get sig,htsig,service field in the command word

RACTL_CMDWDFILL

Bits	Name	Description
1	SERVICE_EN	Asserted to enable transmission of sig,htsig from RAHDR to PMI. Default is enable. Reset State: 0x0001
0	HDR_EN	Asserted to enable transmission of sig,htsig rom RAHDR to PMI. Default is enable. Reset State: 0x0001

0x30000A8 RACTL_LAST_HTSIGNAL0

Type: read-only
Reset State: 0x0000

This register holds the LS 16 bits of the last decoded 'unsupported' HTSIG SIGNAL field value. On reset, the register is set to 0

RACTL_LAST_HTSIGNAL0

Bits	Name	Description
15:0	VALUE	LS 16 bits of the last decoded 'unsupported' HTSIG SIGNAL field Reset State: 0x0000

0x30000AC RACTL_LAST_HTSIGNAL1

Type: read-only
Reset State: 0x0000

This register holds bits[31:16] of the last decoded 'unsupported' HTSIG SIGNAL field value. On reset, the register is set to 0

RACTL_LAST_HTSIGNAL1

Bits	Name	Description
15:0	VALUE	bits [31:16] of the last decoded 'unsupported' HTSIG SIGNAL field Reset State: 0x0000

0x30000B0 RACTL_LAST_HTSIGNAL2

Type: read-only
Reset State: 0x0000

This register holds bits [47:32] of the last decoded 'unsupported' HTSIG SIGNAL field value. On reset, the register is set to 0

RACTL_LAST_HTSIGNAL2

Bits	Name	Description
15:0	VALUE	MS 16 bits of the last decoded 'unsupported' HTSIG SIGNAL field Reset State: 0x0000

0x30000B4 RACTL_PTC_TH

Type: read-write
Reset State: 0x0008

RACTL_PTC_TH

Bits	Name	Description
3:0	QBPSK	Reset State: 0x0008

0x30000B8 RACTL_RACTL_STATUS

Type: read-write
Reset State: 0x0000

RACTL_RACTL_STATUS

Bits	Name	Description
13	PKTABORTSCOPE_CLR	Clear for bits [9:1] Reset State: 0x0000
12	PKT_PENDING_CLR	Clear for bit 0. Reset State: 0x0000
9:1	PKTABORTSCOPE	When sampled, shows the reason for ractl packet abort 0 - ssf_invalid 1 - htsig_invalid 2 - not_avalid 3 - serv_invalid 4 - state machine watchdog expired 5 - unsupported mode with given antenna configuration (NOTE that for Volans, 1rx all streams are supported for CSI transfer. However, the definition of this bit has been retained) 6 - unsupported htsig (NOTE that for Volans, NDP packets are supported for CSI transfer. However, the definition of this bit has been retained) 7 - spare 8 - spare
0	PKT_PENDING	When sampled, shows if a packet is pending for processing by RACTL

0x30000BC RACTL_STROBE_UNSUPPHTSIG

Type: command

Initiates write of the 1st occurrence of unsupported htsig

RACTL_STROBE_UNSUPPHTSIG

Bits	Name	Description
0	INITIATE	Write to this register to do only one write to registers 9C to A0 above.

0x30000C0 RACTL_NES2_MCSBOUND0

Type: read-write
Reset State: 0x1715

Programmable lower and upper bounds of mcs fields to detect Nes of 2

RACTL_NES2_MCSBOUND0

Bits	Name	Description
14:8	MCSUB0	Upper bound0. This value will be used with 11n40 flag to declare Nes of 2 Reset State: 0x0017

RACTL_NES2_MCSBOUND0 (cont.)

Bits	Name	Description
6:0	MCSLB0	Lower bound0. This value will be used with 11n40 flag to declare Nes of 2 Reset State: 0x0015

0x30000C4 RACTL_NES2_MCSBOUND1

Type: read-write
Reset State: 0x1F1C

Programmable lower and upper bounds of mcs fields to detect Nes of 2

RACTL_NES2_MCSBOUND1

Bits	Name	Description
14:8	MCSUB1	Upper bound1. This value will be used with 11n40 flag to declare Nes of 2 Reset State: 0x001F
6:0	MCSLB1	Lower bound1. This value will be used with 11n40 flag to declare Nes of 2 Reset State: 0x001C

0x30000C8 RACTL_NES2_MCSBOUND2

Type: read-write
Reset State: 0x3434

Programmable lower and upper bounds of mcs fields to detect Nes of 2

RACTL_NES2_MCSBOUND2

Bits	Name	Description
14:8	MCSUB2	Upper bound2. This value will be used with 11n40 flag to declare Nes of 2 Reset State: 0x0034
6:0	MCSLB2	Lower bound2. This value will be used with 11n40 flag to declare Nes of 2 Reset State: 0x0034

0x30000CC RACTL_NES2_MCSBOUND3

Type: read-write
Reset State: 0x4C46

Programmable lower and upper bounds of mcs fields to detect Nes of 2

RACTL_NES2_MCSBOUND3

Bits	Name	Description
14:8	MCSUB3	Upper bound3. This value will be used with 11n40 flag to declare Nes of 2 Reset State: 0x004C
6:0	MCSLB3	Lower bound3. This value will be used with 11n40 flag to declare Nes of 2 Reset State: 0x0046

0x30000D0 RACTL_LSIGLEN_LOWERBOUND

Type: read-write
Reset State: 0x0149

Programmable lower bound of length field in LSIG to detect htsig in a MM packet

RACTL_LSIGLEN_LOWERBOUND

Bits	Name	Description
9:5	LSIGLENLB_AC	The length field in the lsig is required to be equal to or more than this value to look for an vhtsiga in the next symbol Reset State: 0x000A
4:0	LSIGLENLB_N	The length field in the lsig is required to be equal to or more than this value to look for an htsig in the next symbol Reset State: 0x0009

0x30000D4 RACTL_RACTL_INTR_EN

Type: read-write
Reset State: 0x0060

The enables to report the interrupts to Phyint. Bit 0 is for enabling interrupt from rahdr and the other ones are in sequence corresponding to register RACTL_STATUS By default, only watchdog-expiry and unsupported configuration-related interrupts are enabled

RACTL_RACTL_INTR_EN

Bits	Name	Description
7	UNSUPHTSIG_INTRMASKEN	Reset State: 0x0000
6	UNSUPCFG_INTRMASKEN	Reset State: 0x0001
5	WATCHDOGEXP_INTRMASKEN	Reset State: 0x0001
4	SERVINVALID_INTRMASKEN	Reset State: 0x0000
3	NOTAVALID_INTRMASKEN	Reset State: 0x0000
2	HTSIG_INVALID_INTRMASKEN	Reset State: 0x0000
1	SSF_INVALID_INTRMASKEN	Reset State: 0x0000
0	RAHDR_INTRMASKEN	Reset State: 0x0000

0x30000D8 RACTL_RACTL_SUPP_BWMISMCOUNT

Type: read-write
Reset State: 0x0000

RACTL counter to count the number of times rxa demodulated a packet at a lower bandwidth compared to that specified by agc. Note that counter is in hardware and the slave is only a readonly.

RACTL_RACTL_SUPP_BWMISMCOUNT

Bits	Name	Description
15	RST	Resets the above counters Reset State: 0x0000
14:10	BW80FOUND20MISM	The dynamic bandwidth setting is 80Mhz but 20M packet detected
9:5	BW80FOUND40MISM	The dynamic bandwidth setting is 80Mhz but 40M packet detected
4:0	BW40FOUND20MISM	The dynamic bandwidth setting is 40Mhz but 20M packet detected

0x30000DC RACTL_PTC_TH1

Type: read-write
Reset State: 0x0006

RACTL_PTC_TH1

Bits	Name	Description
3:0	IBPSK	Reset State: 0x0006

0x30000F0 RACTL_LMAP

Type: read-write
Reset State: 0x0000

This register holds 2 bits - one (bit 1) is applicable till the header is demodulated and the other (bit 0) for the data symbols in general. The value in bit 0 of this bit register specifies whether duplicate tones need to be combined in the RXA before simo slicer function in the data portions of the symbol Note that the contents of this register is modified by ractl's mode detection logic such that HT-duplicate packets should always do MRC over duplicate tones irrespective of this setting. Stated otherwise, this register only affects legacy duplicate mode packets.

RACTL_LMAP

Bits	Name	Description
1	DUPTONE_COMB_EN_SF	Off by default. When high, duplicate tones combining will take place only for signal fields (legacy or htsig) duplicate symbols. Note that due to hardware processing latencies, the settings of this bit will affect the duplicate combining of the service-data symbol of the legacy duplicate packet. Reset State: 0x0000
0	DUPTONE_COMB_EN	Off by default. When high, duplicate tones combining will take place only for legacy duplicate symbols. Note that due to hardware processing latencies, the settings of this bit will _not_ affect the duplicate combining of the service-data symbol of the legacy duplicate packet. Reset State: 0x0000

0x30000F4 RACTL_RACTL_SPL

Type: read-write
Reset State: 0x0006

This register holds some configuration bits to handle ractl-agc signalling of txop signal (only for MM packets and when LSIG and HTSIG both pass) and ractl-rahdr signalling to steer transfer of data to pmi.

RACTL_RACTL_SPL

Bits	Name	Description
15	RESET_TXOP	Off by default. When high, the txop signal from ractl will be cleared. This clearing mechanism is devised since the txop signal is not cleared with regular clearing mechanism in ractl like agc_start and agc_abort Reset State: 0x0000
2	NDP_PMI_XFER	ON by default. When high, the command-word and statistics bytes go to pmi. When low, nothing goes. Reset State: 0x0001
1	TXOP_SIG_NDP	On by default. When low, specifies that txop signal need not be toggled at all for ndp (zlf) packets Reset State: 0x0001
0	TXOP_SIG_SUPPHTSIG	Off by default. When high, specifies that txop calculation to be done for supported htsig Note that txop calculation is always done on unsupported htsig. Reset State: 0x0000

0x30000F8 RACTL_WATCHDOG1

Type: read-write
Reset State: 0x0000

Watchdog timer max values in header detection states Watchdog timer max values in microseconds.

RACTL_WATCHDOG1

Bits	Name	Description
15:12	WD_HTSIG	Watchdog timer maxvalue in HTSIG state; Minimum value 5. Value of 0 disables this timer. Reset State: 0x0000
11:8	WD_SF3	Watchdog timer maxvalue in SF3 state; Minimum value 5. Value of 0 disables this timer. Reset State: 0x0000
7:4	WD_SF2	Watchdog timer maxvalue in SF2 state; Minimum value 5. Value of 0 disables this timer. Reset State: 0x0000
3:0	WD_SF1	Watchdog timer maxvalue in SF1 state; Minimum value 5. Value of 0 disables this timer. Reset State: 0x0000

0x30000FC RACTL_WATCHDOG2

Type: read-write
Reset State: 0x0000

Watchdog timer max values in extra short and long training, servdata and recovery states Watchdog timer maxvalues in microseconds.

RACTL_WATCHDOG2

Bits	Name	Description
15:12	WD_WF	Watchdog timer maxvalue in WAITFINISH state; Minimum value 11. Value of 0 disables this timer. Reset State: 0x0000
11:8	WD_SERV	Watchdog timer maxvalue in SERV state; Minimum value 5. Value of 0 disables this timer. Reset State: 0x0000
7:4	WD_EXTRALTF	Watchdog timer maxvalue in extra LTF states; Minimum value 5. Value of 0 disables this timer. Reset State: 0x0000
3:0	WD_STS	Watchdog timer maxvalue in STS state; Minimum value 7. Value of 0 disables this timer. Reset State: 0x0000

0x3000100 RACTL_WATCHDOG3

Type: read-write
Reset State: 0x0000

Watchdog timer max values in data state and eopcount state Watchdog timer maxvalues in microseconds.

RACTL_WATCHDOG3

Bits	Name	Description
15	WDEXP_ABORT_EN	Enable for generating internal ractl abort based on expiry of watchdog timers listed in the registers WATCHDOG1, WATCHDOG2 and WATCHDOG3 Reset State: 0x0000
12:0	WD_DAT	Watchdog timer maxvalue in DATA and EOPCNT state. Value of 0 disables this timer. Reset State: 0x0000

0x3000104 RACTL_PTC_PKTCOUNT_GF

Type: write-only

Number of packet burst start signals received by the PTC module in all Greenfield modes

RACTL_PTC_PKTCOUNT_GF

Bits	Name	Description
11:0	PTC_SPKTCOUNT_GF	Number of packet burst start signals received by the PTC module in all Greenfield modes.

0x3000108 RACTL_PTC_PKTCOUNT_MM

Type: write-only

Number of packet burst start signals received by the PTC module in all Mixed-mode packets

RACTL_PTC_PKTCOUNT_MM

Bits	Name	Description
11:0	PTC_SPKTCOUNT_MM	Number of packet burst start signals received by the PTC module in all Mixed-mode modes.

0x300010C RACTL_LMAP_CONTROL

Type: read-write
Reset State: 0x0005

This registers provides the channel tracking controls

RACTL_LMAP_CONTROL

Bits	Name	Description
2:1	LMAP_TRACK_GAIN	Programmable tracking loop gain. Default setting = 2'h2. 0x0: LOOPGAIN_8 0x1: LOOPGAIN_16 0x2: LOOPGAIN_32 0x3: INVALID Reset State: 0x0002
0	LMAP_TRACK_EN	Channel tracking enable. If de-asserted, the channel tracking loop will not modify channel estimate samples received from the channel estimator module. Default setting = 1'b1. Reset State: 0x0001

0x3000110 RACTL_RACTL_UNSUPP_BWMISMCOUNT

Type: read-write
Reset State: 0x0000

RACTL counter to count the number of times rxa encountered packet at a higher bandwidth compared to that specified by agc. Note that counter is in hardware and the slave is only a readonly.

RACTL_RACTL_UNSUPP_BWMISMCOUNT

Bits	Name	Description
15	RST	Resets the above counters Reset State: 0x0000
14:10	BW20FOUND80MISM	The dynamic bandwidth setting is 20Mhz but 80M packet detected
9:5	BW40FOUND80MISM	The dynamic bandwidth setting is 40Mhz but 80M packet detected
4:0	BW20FOUND40MISM	The dynamic bandwidth setting is 20Mhz but 40M packet detected

0x3000114 RACTL_RACTL_LAST_BW

Type: read-only

RACTL_RACTL_LAST_BW

Bits	Name	Description
15:8	DYN	Most recent rightmost {prev4_dyn, prev3_dyn, prev2_dyn, prev1_dyn}
7:0	STATIC	Most recent rightmost {prev4_static, prev3_static, prev2_static, prev1_static}

0x300012C RACTL_RACTL_CLK160_DYNSEL1

Type: read-write
Reset State: 0x0099

RACTL_RACTL_CLK160_DYNSEL1

Bits	Name	Description
7	ENABLE_GF	If set, selects the following clock-ratios for the data section of the clk160 processing in rxa. Default setting-dynamic selection disabled for gf packets Reset State: 0x0001

RACTL_RACTL_CLK160_DYNSEL1 (cont.)

Bits	Name	Description
5:4	GF_CLKRATIOSEL	0x0: switched-clk is 1:1 of original clock1: switched-clk is 2:3 of original clock 2 : switched-clk is 4:5 of original clock 3 : switched-clk is 8:9 of original clock Default is 1:1 Reset State: 0x0001
3	ENABLE_LEGACY	If set, selects the following clock-ratios for the data section of the clk160 processing in rxa. Default setting-dynamic selection enabled for legacy packets Reset State: 0x0001
1:0	LGCY_CLKRATIOSEL	0x0: switched-clk is 1:1 of original clock1: switched-clk is 2:3 of original clock 2 : switched-clk is 4:5 of original clock 3 : switched-clk is 8:9 of original clock Default is 2:3 Reset State: 0x0001

0x3000130 RACTL_RACTL_CLK160_DYNSEL2

Type: read-write
Reset State: 0x0A89

RACTL_RACTL_CLK160_DYNSEL2

Bits	Name	Description
15	ENABLE_MM_SGISTBC	If set, selects the following clock-ratios for the data section of the clk160 processing in rxa. Default setting-dynamic selection enabled for mm stbc short-gi packets Reset State: 0x0000
13:12	MM_SGISTBC_CLKRATIOSEL	0x0: switched-clk is 1:1 of original clock1: switched-clk is 2:3 of original clock 2 : switched-clk is 4:5 of original clock 3 : switched-clk is 8:9 of original clock Default is 8:9 Reset State: 0x0000
11	ENABLE_MM_SGI	If set, selects the following clock-ratios for the data section of the clk160 processing in rxa. Default setting-dynamic selection enabled for mm short-gi packets Reset State: 0x0001
9:8	MM_SGI_CLKRATIOSEL	0x0: switched-clk is 1:1 of original clock1: switched-clk is 2:3 of original clock 2 : switched-clk is 4:5 of original clock 3 : switched-clk is 8:9 of original clock Default is 4:5 Reset State: 0x0002
7	ENABLE_MM_LGISTBC	If set, selects the following clock-ratios for the data section of the clk160 processing in rxa. Default setting-dynamic selection enabled for mm stbc packets Reset State: 0x0001

RACTL_RACTL_CLK160_DYNSEL2 (cont.)

Bits	Name	Description
5:4	MM_LGISTBC_CLKRATIOSEL	0x0: switched-clk is 1:1 of original clock1: switched-clk is 2:3 of original clock 2 : switched-clk is 4:5 of original clock 3 : switched-clk is 8:9 of original clock Default is 4:5 Reset State: 0x0000
3	ENABLE_MM_LGI	If set, selects the following clock-ratios for the data section of the clk160 processing in rxa. Default setting-dynamic selection enabled for mm long-gi packets Reset State: 0x0001
1:0	MM_LGI_CLKRATIOSEL	0x0: switched-clk is 1:1 of original clock1: switched-clk is 2:3 of original clock 2 : switched-clk is 4:5 of original clock 3 : switched-clk is 8:9 of original clock Default is 2:3 Reset State: 0x0001

0x3000134 RACTL_RACTL_SNRSTATS

Type: read-only

RACTL_RACTL_SNRSTATS

Bits	Name	Description
15:0	STATS	Note that this is a running sum or minimum of the per symbol snr based on the register below. This is cleared with the clear bit below.

0x3000138 RACTL_RACTL_SNRSTATS_SYMCNT

Type: read-only

RACTL_RACTL_SNRSTATS_SYMCNT

Bits	Name	Description
7:0	STATS_SYMCNT	Note that this is a running symbol count that is cleared with the clear bit below.

0x300013C RACTL_RACTL_SNRSTATSCLR

Type: command
Reset State: 0x0000

RACTL_RACTL_SNRSTATSCLR

Bits	Name	Description
0	CLR	Reset State: 0x0000

0x3000140 RACTL_RACTL_SNRSTATSCFG

Type: read-write
Reset State: 0x0000

RACTL_RACTL_SNRSTATSCFG

Bits	Name	Description
1	COLLECT_ALWAYS	When high, the statistics is collected irrespective of txbusy is high or not. Reset State: 0x0000
0	LOCK	As long as the lock is asserted, the data (RACTL_SNRSTATS and RACTL_SNRSTATS_SYMCNT) do not get updated. Reset State: 0x0000

0x3000144 RACTL_LMAP_SNR_SEL

Type: read-write
Reset State: 0x0001

RACTL_LMAP_SNR_SEL

Bits	Name	Description
0	ENABLE_SNRCOMP	When asserted, selects the LMAP SNR computation function. This is used in CSI report as well as per-symbol snr metric Reset State: 0x0001

0x3000148 RACTL_CSI_CONFIG

Type: read-write
Reset State: 0x0183

RACTL_CSI_CONFIG

Bits	Name	Description
9	CSI_ABORT_CLR	When set to 1, CSI abort counter is cleared Reset State: 0x0000
8	CSI_XFER_EN	When set to 1, CSI-transfer is enabled. This influences CHE and PHYCSXI functionality for CSI transfer Reset State: 0x0001
7	CSI_WATCHDOG_EN	When set to 1, the watchdog timer in PHYCSXI is on and expires after 10 microseconds (max possible CSI xfer time) Note - has power impact. Switch this off if power-saving is desired. Reset State: 0x0001

RACTL_CSI_CONFIG (cont.)

Bits	Name	Description
6	NOTSOUNDINGPPDU_GENERATE_CSI	When set to 1, generate CSI report for nonsounding valid PPDU (MCS <8 length > 0, not_sounding is 1) See PHYCSXI documentation Reset State: 0x0000
5	INVALID_NDP2_GENERATE_CSI	When set to 1, generate CSI report for invalid NDP2 (8 <= MCS < 32, length is 0, not_sounding is 1) Reset State: 0x0000
4	INVALID_NDP1_GENERATE_CSI	When set to 1, generate CSI report for invalid NDP1 (MCS < 8, length is 0, not_sounding is 0 or 1) Reset State: 0x0000
3:2	NG	0x0: NG_56 0x1: NG_30 0x2: NG_16 0x3: NG_RESVD Reset State: 0x0000
1:0	NB	0x0: NB_4 0x1: NB_5 0x2: NB_6 0x3: NB_8 Reset State: 0x0003

0x300014C RACTL_SIGNAL_INVALID_COUNT_HTSIG

Type: write-only

Number of packets received with invalid HT SIGNAL field values

RACTL_SIGNAL_INVALID_COUNT_HTSIG

Bits	Name	Description
15:0	INVALID_SFCOUNT	Number of packets received with invalid SIGNAL field values

0x3000150 RACTL_LST_MCS

Type: read-only

The last MCS received by the controller

RACTL_LST_MCS

Bits	Name	Description
6:0	VALUE	

0x3000154 RACTL_RXFIR_SCALING_COEFF

Type: read-write
Reset State: 0x0001

RACTL_RXFIR_SCALING_COEFF

Bits	Name	Description
0	DC_NOTCH_EN	When high, selects rxfir scaling coefficients (to be used by FFT) appropriate with rxfir operation WITH dc notch. Note to use this register bit with appropriate AGC bit settings Reset State: 0x0001

0x3000158 RACTL_CSI_STATS1

Type: write-only

Number of CSI transfers initiated by RACTL in various cases

RACTL_CSI_STATS1

Bits	Name	Description
7:0	MACREQ_NONNDP_SOUNDING	Counts the number of MAC-requested CSI transfers for non-NDP sounding PPDU packets. These packets will have MCS less than 8 and may be STBC packets. [Case1 - (mcs_lt_8 & length_ge0 & not_sounding_0 & nonndp_sounding_cfg_modf)]

0x300015C RACTL_CSI_STATS2

Type: write-only

Number of CSI transfers initiated by RACTL in various cases

RACTL_CSI_STATS2

Bits	Name	Description
7:0	MACREQ_NDP_SOUNDING	Counts the number of MAC-requested CSI transfers for NDP sounding packets. These packets will have MCS between 8 and 31 and non-STBC packets. The HTSIG is 'unsupported' type [Case2 - (mcs_ge8_n_lt32 & length_0 & not_sounding_0 & stbc_0 & ndp_sounding_cfg_modf)]

0x3000160 RACTL_CSI_STATS3

Type: write-only

Number of CSI transfers initiated by RACTL in various cases

RACTL_CSI_STATS3

Bits	Name	Description
7:0	INTREQ_NDP	Counts the number of RACTL-requested CSI transfers for NDP packets. These packets will have MCS less than 8. Note that GF SISO NDP packets, CSI transfer is not supported. [Case3 - mcs_lt_8 & length_0 & ractlreg_ractlpp_invalid_ndp1_generate_csi & ((

0x3000164 RACTL_CSI_STATS4

Type: write-only

Number of CSI transfers initiated by RACTL in various cases

RACTL_CSI_STATS4

Bits	Name	Description
7:0	INTREQ_NDP_NONSOUNDING	Counts the number of RACTL-requested CSI transfers for NDP non-sounding packets. These packets will have MCS between 8 and 31. The HTSIG is 'unsupported' type [Case4 - mcs_ge8_n_lt32 & length_0 & not_sounding & ractlreg_ractlpp_invalid_ndp2_generate_csi]

0x3000168 RACTL_CSI_STATS5

Type: read-only

Number of CSI aborts initiated by RACTL in various cases

RACTL_CSI_STATS5

Bits	Name	Description
7:0	ABORTCNT	

0x300016C RACTL_RACTL_CRCCHKCFG

Type: read-write
Reset State: 0x0004

RACTL_RACTL_CRCCHKCFG

Bits	Name	Description
2:1	CRCCHK_EN_VHTSIGB	Do CRC-field check in VHTSIGB over VHTSIGB only (==2'd0) Do CRC-field check in VHTSIGB over VHTSIGA and VHTSIGB (==2'd1) Do CRC-field check in VHTSIGB over LSIG and VHTSIGA and VHTSIGB (==2'd2 or 2'd3) Reset State: 0x0002
0	CRCCHK_EN_VHTSIGA	Do CRC-field check of VHTSIGA over VHTSIGA only (==0) or check over LSIG and VHTSIGA (==1) Reset State: 0x0000

0x3000170 RACTL_RACTL_FEEDBACKCFG

Type: read-write
Reset State: 0x0000

RACTL_RACTL_FEEDBACKCFG

Bits	Name	Description
1:0	FEEDBACK_TYPE	Feedback-type to ber sent to MCFG from PHY. 0 and 1 for CSI, 2 for uncompressed vector feedback; 3 for compressed vector feedback Reset State: 0x0000

0x3000174 RACTL_RACTL_ENABLE_AC

Type: read-write
Reset State: 0x0001

RACTL_RACTL_ENABLE_AC

Bits	Name	Description
1	BEHAV_11N	When enabled, the signal-field check of 11ac will be similar to 11n, i.e., the crc failure will be treated as a packet-abort condition. Any other condition will qualify for unsupported packet and deferral will be based on lsig. If this bit is 0, irrespective of unsupported or crc-failed vhtsiga, deferral will be done based on lsig. Reset State: 0x0000
0	CFG	Enables reception of AC packets Reset State: 0x0001

0x3000178 RACTL_RACTL_PKTCOUNT_AC20

Type: write-only

Number of AC20 packets detected by RACTL

RACTL_RACTL_PKTCOUNT_AC20

Bits	Name	Description
7:0	AC20_SPKTCOUNT	

0x300017C RACTL_RACTL_PKTCOUNT_AC40

Type: write-only

Number of AC40 packets detected by RACTL

RACTL_RACTL_PKTCOUNT_AC40

Bits	Name	Description
7:0	AC40_SPKTCOUNT	

0x3000180 RACTL_RACTL_PKTCOUNT_AC80

Type: write-only

Number of AC80 packets detected by RACTL

RACTL_RACTL_PKTCOUNT_AC80

Bits	Name	Description
7:0	AC80_SPKTCOUNT	

0x3000184 RACTL_LAST_LSIG0

Type: read-only
Reset State: 0x0000

This register will be used to primarily diagnose 11n MM and 11AC packet demodulation issues.

RACTL_LAST_LSIG0

Bits	Name	Description
15:0	VALUE	Reset State: 0x0000

0x3000188 RACTL_LAST_LSIG1

Type: read-only
Reset State: 0x0000

This register will be used to primarily diagnose 11n MM and 11AC packet demodulation issues.

RACTL_LAST_LSIG1

Bits	Name	Description
7:0	VALUE	Reset State: 0x0000

0x300018C RACTL_CHE_PKTCOUNT

Type: write-only

Number of packet burst start signals received by the CHE module

RACTL_CHE_PKTCOUNT

Bits	Name	Description
7:0	CHE_SPKTCOUNT	Number of packet burst start signals received by the CHE module

0x3000190 RACTL_LMAP_OPSCALE1_SISO

Type: read-write
Reset State: 0x28EC

This registers provides the rate-qam-size dependent output scaling to LMAP simo distance outputs

RACTL_LMAP_OPSCALE1_SISO

Bits	Name	Description
14:12	SISO_MCS4_16QA3BY4	Reset State: 0x0002
11:9	SISO_MCS3_16QA1BY2	Reset State: 0x0004
8:6	SISO_MCS2_QPSK3BY4	Reset State: 0x0003
5:3	SISO_MCS1_QPSK1BY2	Reset State: 0x0005
2:0	SISO_MCS0_BPSK1BY2	Reset State: 0x0004

0x3000194 RACTL_LMAP_OPSCALE2_SISO

Type: read-write
Reset State: 0x0053

This registers provides the rate-qam-size dependent output scaling to LMAP simo distance outputs

RACTL_LMAP_OPSCALE2_SISO

Bits	Name	Description
14:12	SISO_MCS9_256QA5BY6	Reset State: 0x0000
11:9	SISO_MCS8_256QA3BY4	Reset State: 0x0000
8:6	SISO_MCS7_64QA5BY6	Reset State: 0x0001
5:3	SISO_MCS6_64QA3BY4	Reset State: 0x0002
2:0	SISO_MCS5_64QA2BY3	Reset State: 0x0003

0x3000198 RACTL_LMAP_OPSCALE1_STBC

Type: read-write
Reset State: 0x26E4

This registers provides the rate-qam-size dependent output scaling to LMAP stbc distance outputs

RACTL_LMAP_OPSCALE1_STBC

Bits	Name	Description
14:12	STBC_MCS4_16QA3BY4	Reset State: 0x0002
11:9	STBC_MCS3_16QA1BY2	Reset State: 0x0003
8:6	STBC_MCS2_QPSK3BY4	Reset State: 0x0003
5:3	STBC_MCS1_QPSK1BY2	Reset State: 0x0004
2:0	STBC_MCS0_BPSK1BY2	Reset State: 0x0004

0x300019C RACTL_LMAP_OPSCALE2_STBC

Type: read-write
Reset State: 0x0052

This registers provides the rate-qam-size dependent output scaling to LMAP stbc distance outputs

RACTL_LMAP_OPSCALE2_STBC

Bits	Name	Description
14:12	STBC_MCS9_256QA5BY6	Reset State: 0x0000
11:9	STBC_MCS8_256QA3BY4	Reset State: 0x0000
8:6	STBC_MCS7_64QA5BY6	Reset State: 0x0001
5:3	STBC_MCS6_64QA3BY4	Reset State: 0x0002
2:0	STBC_MCS5_64QA2BY3	Reset State: 0x0002

0x30001A0 RACTL_LMAP_OPSCALE3

Type: read-write
Reset State: 0x0109

This registers provides the rate-qam-size dependent output scaling to LMAP distance outputs

RACTL_LMAP_OPSCALE3

Bits	Name	Description
8:6	LGCY_BPSK3BY4	Reset State: 0x0004
5:3	STBC_MCS10_256QA7BY8	Reset State: 0x0001
2:0	SISO_MCS10_256QA7BY8	Reset State: 0x0001

0x30001A4 RACTL_FORCE_DBGPKTTYPE

Type: read-write
Reset State: 0x0000

Forces the packet-type of received packet based on forced Ibpsk or Qbpskchecks in RACTL main FSM Note that the following packet-types will be inferred from the combination of symtype checks: {sym0_Ibpskforce, sym1_Ibpskforce, sym2_Ibpskforce} implies Legacy 6 mbps {sym0_Ibpskforce, sym1_Ibpskforce, sym2_Qbpskforce} implies 11AC {sym0_Ibpskforce, sym1_Qbpskforce, Not applicable } implies 11n_MM {sym0_Qbpskforce, Not applicable , Not applicable } implies 11n_GF

RACTL_FORCE_DBGPKTTYPE

Bits	Name	Description
5	SYM2_QBPSKFORCE	Reset State: 0x0000
4	SYM2_IBPSKFORCE	Reset State: 0x0000
3	SYM1_QBPSKFORCE	Reset State: 0x0000

RACTL_FORCE_DBGPKTTYPE (cont.)

Bits	Name	Description
2	SYM1_IBPSKFORCE	Reset State: 0x0000
1	SYM0_QBPSKFORCE	Reset State: 0x0000
0	SYM0_IBPSKFORCE	Reset State: 0x0000

16.2.20 rbapb

0x3000000 RBAPB_CONTROL_RXB_DSCR

Type: read-write

Controls RXB Descrambler.

RBAPB_CONTROL_RXB_DSCR

Bits	Name	Description
1	SFD_DETECT	Disable descrambled short SFD detector. 0x0: ENABLE 0x1: DISABLE
0	DESCRAMBLER	Disable RXB Descrambler. 0x0: ENABLE 0x1: DISABLE

0x3000004 RBAPB_COUNT_SSFD

Type: write-only

Counts the number of short Start-of-Frame delimiters detected.

RBAPB_COUNT_SSFD

Bits	Name	Description
15:0	COUNT	Number of short Start-of-Frame delimiters detected

0x3000008 RBAPB_COUNT_LSFD

Type: write-only

Counts the number of logn Start-of-Frame delimiters detected.

RBAPB_COUNT_LSFD

Bits	Name	Description
15:0	COUNT	Number of long Start-of-Frame delimiters detected

0x300000C RBAPB_IGN_ILL_PLCP

Type: read-write
Reset State: 0x00FB

This register is used to enable checking of the following fields of the PLCP header: CRC16, Rate field and Service Field. These correctness check are all described in standard IEEE802.11b. The CRC16 should check, the service field should have its reserved bits set to zero and the rate field should contain one of the supported rates (in multiples of 100 kbit/s): 8'd10, 8'd20, 8'd55 or 8'd110.

RBAPB_IGN_ILL_PLCP

Bits	Name	Description
10	IGN_SIG	Used to ignore check for valid signal fields and pass packets with signal field errors Valid rate fields conents are 10, 20, 55 and 110 (decimal), denoting 1,2, 5.5 and 11 Mbit/s. 0x0: ENABLE 0x1: IGNORE
9	IGN_SVC	Used to ignore check for valid service fields and pass packets with signal field errors A valid service fields has all bits equal to zero for 1, 2 and 5.5 Mbit/s mode. The most significant bit may be non-zero in 11 Mbits/s mode. 0x0: ENABLE 0x1: IGNORE
8	IGN_CRC	Used to ignore CRC check and pass packets with PLCP CRC errors. 0x0: ENABLE 0x1: IGNORE
7:0	SVC_MASK	Service Field Mask. The field is applied using a logical 'and' to the service field before the illegal service field check is applied. By default the 'coupled clocks' bit is masked out, in order not to reject packets tranmsitted by products with uincoupled clocks or products which couple clocks only for higher bit rates. Reset State: 0x00FB

0x3000010 RBAPB_COUNT_PLCP_CRC_ERRORS

Type: write-only

Counter number of CRC errors.

RBAPB_COUNT_PLCP_CRC_ERRORS

Bits	Name	Description
15:0	COUNT	CRC error counter.

0x3000014 RBAPB_COUNT_PLCP_SIG_ERRORS

Type: write-only

Counter number of signal field errors.

RBAPB_COUNT_PLCP_SIG_ERRORS

Bits	Name	Description
15:0	COUNT	Illegal signal field counter.

0x3000018 RBAPB_COUNT_PLCP_SVC_ERRORS

Type: write-only

Counter number of service field errors.

RBAPB_COUNT_PLCP_SVC_ERRORS

Bits	Name	Description
15:0	COUNT	Illegals service field counter.

0x300001C RBAPB_COUNT_RX_BYTES

Type: write-only

Counts number of payload bytes received by the RXB receiver (output by the header processor).

RBAPB_COUNT_RX_BYTES

Bits	Name	Description
15:0	COUNT	Byte counter.

0x3000020 RBAPB_COUNT_MPI_SOF

Type: write-only

Countrs number of Start-Of_Frame signals generated by header processor and sent to MPI.

RBAPB_COUNT_MPI_SOF

Bits	Name	Description
15:0	COUNT	rbhdr_mpi_sof event counter.

0x3000024 RBAPB_COUNT_MPI_EOF

Type: write-only

Countrs number of End-Of_Frame signals generated by header processor and sent to MPI.

RBAPB_COUNT_MPI_EOF

Bits	Name	Description
15:0	COUNT	rbhdr_mpi_eof event counter.

0x3000028 RBAPB_SFD_DET_TMO

Type: read-write
Reset State: 0x007D

SFD Detetction threshold is specified in microseconds. Power-on reset value is 125 decimal. Includes demodulation and descrambling delay. This register is used to lead a timer that aborts the SFD detection process. It should be as set as low as possible to reduce the receiver dead time to a minimum.

RBAPB_SFD_DET_TMO

Bits	Name	Description
7:0	TIME	SFD detection timeout. 0x7D: POR Reset State: 0x007D

0x300002C RBAPB_SLR_SFD_DET_TMO

Type: read-write
Reset State: 0x01F4

SFD Detetction threshold is specified in microseconds. Power-on reset value is 500 decimal. Includes demodulation and descrambling delay. This register is used to set a timer that aborts the SFD detection process for SLR packets. It should be as set as low as possible to reduce the receiver dead time to a minimum.

RBAPB_SLR_SFD_DET_TMO

Bits	Name	Description
8:0	TIME	SLR SFD detection timeout. 0x1F4: POR Reset State: 0x01F4

0x3000030 RBAPB_COUNT_RXB_START

Type: write-only

Counts number of RXB_START events received by the RXB controler.

RBAPB_COUNT_RXB_START

Bits	Name	Description
15:0	COUNT	RXB_START Counter

0x3000038 RBAPB_COUNT_RXB_ABORT

Type: write-only

Counts number of RXB_ABORT events received by the RXB controler.

RBAPB_COUNT_RXB_ABORT

Bits	Name	Description
15:0	COUNT	RXB_ABORT event counter.

0x300003C RBAPB_RXB_RESET

Type: command

Resets RXB controller state machine.

RBAPB_RXB_RESET

Bits	Name	Description
0	RST	Reset RXB.

0x3000040 RBAPB_CONTROL_BARKER_TIMING_TRACKING

Type: read-write
Reset State: 0x0006

Control Barker timing tracking.

RBAPB_CONTROL_BARKER_TIMING_TRACKING

Bits	Name	Description
2	FEEDBACK	Enable Barker timing tracking. 0x0: DISABLE 0x1: ENABLE Reset State: 0x0001
1:0	THRESHOLD	Timing error threshold. Reset State: 0x0002

0x3000048 RBAPB_CMF_PLL_COEFF_A

Type: read-write
Reset State: 0x02DE

CMF PLL Loop Coefficient A

RBAPB_CMF_PLL_COEFF_A

Bits	Name	Description
9:0	COEFF_A	default value -290 Reset State: 0x02DE

0x300004C RBAPB_CMF_PLL_COEFF_B

Type: read-write
Reset State: 0x0127

CMF PLL Loop Coefficient B

RBAPB_CMF_PLL_COEFF_B

Bits	Name	Description
9:0	COEFF_B	default value 295 Reset State: 0x0127

0x3000050 RBAPB_CMF_PLL_COEFF_A_SLR_TRACK

Type: read-write
Reset State: 0x0378

CMF PLL Loop Coefficient A used for SLR packets after SFD has been detected

RBAPB_CMF_PLL_COEFF_A_SLR_TRACK

Bits	Name	Description
9:0	COEFF_A_TRACK	default value -136 Reset State: 0x0378

0x3000054 RBAPB_CMF_PLL_COEFF_B_SLR_TRACK

Type: read-write
Reset State: 0x008A

CMF PLL Loop Coefficient B used for SLR packets after SFD has been detected

RBAPB_CMF_PLL_COEFF_B_SLR_TRACK

Bits	Name	Description
9:0	COEFF_B_TRACK	default value 138 Reset State: 0x008A

0x3000058 RBAPB_ANTENNA_DIVERSITY_MODE

Type: read-write
Reset State: 0x0000

This register defines the behaviour of the antenna diversity logic.

RBAPB_ANTENNA_DIVERSITY_MODE

Bits	Name	Description
1:0	VALUE	Antenna diversity selector mode field 0x0: DISABLE 0x1: ALWAYS 0x2: SNR_SWITCH 0x3: RESV Reset State: 0x0000

0x300005C RBAPB_SNR_THRESHOLD

Type: read-write
Reset State: 0x0019

This threshold is used to decide whether the SNR of the current packet is sufficient to support diversity

RBAPB_SNR_THRESHOLD

Bits	Name	Description
5:0	VALUE	SNR threshold value Reset State: 0x0019

0x3000060 RBAPB_SNR_AVERAGER_GAIN

Type: read-write
Reset State: 0x0028

Barker and CCK demod SNR averager loop gain

RBAPB_SNR_AVERAGER_GAIN

Bits	Name	Description
5:4	RBCCK_HANDOFF	CCK demod SNR averager loop gain - default value = 2^6 Reset State: 0x0002
3:2	RBBRK_HANDOFF	Barker demod SNR averager loop gain after antenna diversity selection - default value = 2^6 Reset State: 0x0002
1:0	RBBRK_ANTSEL	Barker demod SNR averager loop gain during antenna diversity selection - default value = 2^4 Reset State: 0x0000

0x3000064 RBAPB_LMS_AVERAGER_SHIFT

Type: read-write
Reset State: 0x0014

Channel equaliser averager loop gain

RBAPB_LMS_AVERAGER_SHIFT

Bits	Name	Description
5:3	SLR	LMS averager loop gain - range 2^(0-7), default value = 2^2 Reset State: 0x0002
2:0	NON_SLR	LMS averager loop gain - range 2^(0-7), default value = 2^4 Reset State: 0x0004

0x3000068 RBAPB_COUNT_DYNSEL_ANT0

Type: write-only

Counts the number of times antenna0 is selected when dynamic antena selection is enabled.

RBAPB_COUNT_DYNSEL_ANT0

Bits	Name	Description
15:0	COUNT	antenna0 event counter.

0x300006C RBAPB_COUNT_DYNSEL_ANT1

Type: write-only

Counts the number of times antenna1 is selected when dynamic antena selection is enabled.

RBAPB_COUNT_DYNSEL_ANT1

Bits	Name	Description
15:0	COUNT	antenna1 event counter.

0x3000070 RBAPB_COUNT_DYNSEL_2ANT

Type: write-only

Counts the number of times both antennae are selected when dynamic antena selection is enabled.

RBAPB_COUNT_DYNSEL_2ANT

Bits	Name	Description
15:0	COUNT	both antennae event counter.

16.2.21 bbana

0x3000000 BBANA_ADC_CTRL

Type: read-write
Reset State: 0x0000

This set of registers are used to control ADC operations.

BBANA_ADC_CTRL

Bits	Name	Description
9	OFFSET_MEAS	Enable ADCs to do offset calibration. Reset State: 0x0000
8:7	INTLV_CTRL	Used to control ADC interleaving. Reset State: 0x0000
6	ADC_PWR_DOWN_N	Power down I & Q reference, clock and output (active low). Not currently used. 0x0: PWR_DOWN 0x1: ENABLED Reset State: 0x0000
5	OUTPUT_DISABLE_Q	Output disable control for ADC Q data rail. 0x0: NORMAL 0x1: MID Reset State: 0x0000
4	EN_Q_OVERRIDE	Enable override control for ADC Q data rail. 0x0: NO_OVERRIDE 0x1: OVERRIDE Reset State: 0x0000
3	EN_Q	Enable ADC for Q data rail. 0x0: DISABLED 0x1: ENABLED Reset State: 0x0000
2	OUTPUT_DISABLE_I	Output disable control for ADC I data rail. 0x0: NORMAL 0x1: MID Reset State: 0x0000
1	EN_I_OVERRIDE	Enable override control for ADC I data rail. 0x0: NO_OVERRIDE 0x1: OVERRIDE Reset State: 0x0000
0	EN_I	Enable ADC for I data rail. 0x0: DISABLED 0x1: ENABLED Reset State: 0x0000

0x3000004 BBANA_ADC_CLK_CTRL

Type: read-write
Reset State: 0x0000

This set of registers are used for controlling the ADC clock settings.

BBANA_ADC_CLK_CTRL

Bits	Name	Description
5:4	ADJ_DUTY_CYCLE_PW	Setting used to adjust the duty cycle pulse width Reset State: 0x0000
3	DUTY_CYCLE_EN	Setting used to enable/disable the duty cycle circuit 0x0: DISABLED 0x1: ENABLED Reset State: 0x0000
2	CLKEDGE_SEL	Setting used to select the edge of the clock to be used by the ADCs 0x0: POSEDGE 0x1: NEGEDGE Reset State: 0x0000
1	CLKSRC_SEL	Setting used to select the clock source to the ADCs Reset State: 0x0000
0	DISABLE_CLK	Used to enable/disable clock to ADCs. 0x0: ENABLED 0x1: DISABLED Reset State: 0x0000

0x3000008 BBANA_ADC_REF_CTRL

Type: read-write
Reset State: 0x0000

This set of registers are used for controlling the reference circuit settings.

BBANA_ADC_REF_CTRL

Bits	Name	Description
6	REF_PWRDOWN	Power down the reference. Reset State: 0x0000
5	VDD_SEL	Switch the reference to VDD. Reset State: 0x0000
4	BIAS_SEL	Selects the source of the reference bias. Reset State: 0x0000

BBANA_ADC_REF_CTRL (cont.)

Bits	Name	Description
3:2	OUT_BIAS	Used to adjust the bias current of the reference generator. Reset State: 0x0000
1:0	V_ADJUST	Register value used to adjust the ADC reference voltage. Reset State: 0x0000

0x300000C BBANA_ADC_CONV_ADJ

Type: read-write
Reset State: 0x0000

This set of registers are used for adjusting various conversion settings.

BBANA_ADC_CONV_ADJ

Bits	Name	Description
8:7	INP_FILT_POLE	Register value used to modify the input filter pole frequency. Reset State: 0x0000
6:5	CONV_DLY	Adjust the conversion delay. Reset State: 0x0000
4:3	COMM_BIAS	Adjust the common mode bias. Reset State: 0x0000
2:0	REG_ADJUST	Register value used to adjust the regulator. Reset State: 0x0000

0x3000010 BBANA_ADC_SPARE

Type: read-write
Reset State: 0x0000

This register contains the ADC spare1 and spare2 bits.

BBANA_ADC_SPARE

Bits	Name	Description
15:14	DELAY_SEL	Delay select control register. 0x0: DSEL_UNDEF_0 0x1: DSEL_UNDEF_1 0x2: DSEL_UNDEF_2 0x3: DSEL_UNDEF_3 Reset State: 0x0000

BBANA_ADC_SPARE (cont.)

Bits	Name	Description
13	RESET_MODE	Controls the current reset mode in operation. 0x0: SAMP_BF_RST 0x1: RST_BF_SAMP Reset State: 0x0000
12:9	NON_OVL_TIM_CTRL	Controls timing in non overlap circuit. 0x0: NON_OVL_TYP 0x1: SAMPB_TRK 0x2: TRK_TRST 0x4: TRST_TRK 0x8: TRK_SAMPB Reset State: 0x0000
8	TEST_SIG_CTRL	Controls test signal outputs on clock and core sel signals. 0x0: DEF_OUT_CK_CRSEL 0x1: HSTST_OUT_CK_CRSEL Reset State: 0x0000
7	TIMING_MODE	Controls the timing mode being used. 0x0: TIMG_MD_UNUSED_0 0x1: TIMG_MD_UNUSED_1 Reset State: 0x0000
6	IQ_CONV_SYNC_MODE	Controls whether I and Q conversions are synchronized. 0x0: NO_IQ_SYNC 0x1: IQ_CNV_SYNC Reset State: 0x0000
5	GLOBAL_INTLV_CTRL	Controls the interleaving function (global level). 0x0: INTRL_DIS 0x1: INTRL_EN Reset State: 0x0000
4	CAP_VALUE_CTRL_SEL	Selects the bits that control the capacitor value. 0x0: BW_FILC 0x1: CAPC_FILC Reset State: 0x0000
3	BG_PWR_MODE	Bandgap power mode register. 0x0: BG_POWER_UP 0x1: BG_SLEEP Reset State: 0x0000
2	REGULATOR_CTRL	ADC regulator control register. 0x0: REGL_ENABLED 0x1: REGL_DISABLED Reset State: 0x0000

BBANA_ADC_SPARE (cont.)

Bits	Name	Description
1	STB_CIRCUIT_CTRL	Low current stability circuit control register. 0x0: STB_ENABLED 0x1: STB_DISABLED Reset State: 0x0000
0	BG_PWR_CTRL	Bandgap power control register. 0x0: BYP_OFF 0x1: BYP_ON Reset State: 0x0000

0x3000014 BBANA_ADC_SPARE3

Type: read-write
Reset State: 0x0000

This register contains the third set of ADC spare bits.

BBANA_ADC_SPARE3

Bits	Name	Description
7:4	SPARE3_UNUSED	Register value holding unused (unmapped) ADC spare3 bits. Reset State: 0x0000
3	CONV_CTRL	Conversion control register. 0x0: CONV_UNDEF_0 0x1: CONV_UNDEF_1 Reset State: 0x0000
2:0	FILT_CTRL	ADC filter control register. 0x0: FILT_UNDEF_0 0x1: FILT_UNDEF_1 0x2: FILT_UNDEF_2 0x3: FILT_UNDEF_3 0x4: FILT_UNDEF_4 0x5: FILT_UNDEF_5 0x6: FILT_UNDEF_6 0x7: FILT_UNDEF_7 Reset State: 0x0000

0x3000018 BBANA_DAC_CTRL

Type: read-write
Reset State: 0x0022

This set of registers are used to control DAC operations.

BBANA_DAC_CTRL

Bits	Name	Description
13:10	DAC_CFG	Register for DAC configuration settings. Reset State: 0x0000
9	CLKEDGE_SEL	Setting used to select the edge of the clock to be used by the DACs 0x0: POSEDGE 0x1: NEGEDGE Reset State: 0x0000
8	INPUT_STANDBY_EN_CTRL	Note: This bit is no longer used. Control of TXAIF input signal on to DAC enable/standby signal. 0x0: ENABLE_DRIVEN 0x1: STANDBY_DRIVEN Reset State: 0x0000
7	STANDBY_Q_OVERRIDE	Standby override control for DAC Q data rail. 0x0: NO_OVERRIDE 0x1: OVERRIDE Reset State: 0x0000
6	STANDBY_Q	Standby control for DAC Q data rail. 0x0: NORMAL 0x1: MID Reset State: 0x0000
5	EN_Q_OVERRIDE	Enable override control for DAC Q data rail. 0x0: NO_OVERRIDE 0x1: OVERRIDE Reset State: 0x0001
4	EN_Q	Enable DAC for Q data rail. 0x0: DISABLED 0x1: ENABLED Reset State: 0x0000
3	STANDBY_I_OVERRIDE	Standby override control for DAC I data rail. 0x0: NO_OVERRIDE 0x1: OVERRIDE Reset State: 0x0000
2	STANDBY_I	Standby control for DAC I data rail. 0x0: NORMAL 0x1: STANDBY Reset State: 0x0000
1	EN_I_OVERRIDE	Enable override control for DAC I data rail. 0x0: NO_OVERRIDE 0x1: OVERRIDE Reset State: 0x0001

BBANA_DAC_CTRL (cont.)

Bits	Name	Description
0	EN_I	Enable DAC for I data rail. 0x0: DISABLED 0x1: ENABLED Reset State: 0x0000

0x300001C BBANA_DAC_BIAS

Type: read-write
Reset State: 0x0000

This set of registers are used to control the DAC bias.

BBANA_DAC_BIAS

Bits	Name	Description
5:0	TX_BIAS	Select output current value. Reset State: 0x0000

0x3000020 BBANA_DEBUG

Type: read-write
Reset State: 0x0000

This set of registers are used for test mode functions.

BBANA_DEBUG

Bits	Name	Description
6:5	ATB_ADDR	Selects atest0 or atest1 Reset State: 0x0000
4	DAC_TEST_EN	Enable the analog test muxes for driving atest0/1. Reset State: 0x0000
3:2	ATEST	Select analog signal on test pad. These signals directly control the atest signals on the ADC. Reset State: 0x0000
1:0	DTEST	Mux digital signals onto I/Q output signals. These signals directly control the dtest signals on the ADC. Reset State: 0x0000

16.2.22 RFIF

0x3000000 RFIF_RF_BUS_CONTROL

Type: read-write
Reset State: 0x0201

This set of registers are used to adjust timing parameters used, and to issue special commands, over the RF bus interface.

RFIF_RF_BUS_CONTROL

Bits	Name	Description
11:8	IRIS_ASYNC_CAP_DLY	Iris begins driving asynchronous signals to Riva at the completion of an RF command. This field is used to delay the sampling of this data after a command has completed. The default value represents a delay of approx. 25 ns ((2+1) x 120M clocks - spec requirement) when bit 3 of this register is 0. The delay changes to be in units of 60M clocks after completion of a register read command when bit 3 in this register is 1. Reset State: 0x0002
7	ENABLE_80M_IRIS_CLK_OVERRIDE	This bit is used to override the control of the 80M clock used for RF calibration mode. When disabled, the clock enable for the 80M Iris clock is automatically disabled when we observe a calibration done signal from Iris (software must still enable the clock via bit 6 below). If there are any issues with this automatic clock disabling feature, this override bit can be enabled to re-activate manual control of disabling the 80M clock via bit 6 below. 0x0: OVERRIDE_DISABLED 0x1: OVERRIDE_ENABLED Reset State: 0x0000
6	ENABLE_80M_IRIS_CLK	This bit is used to enable/disable the 80M clock used for RF calibration mode. During RF calibration mode, an 80 MHz clock must be fed out on the cmd_clk signal, and it is this bit that is used to enable/disable that clock. Bit 2 in this register is used to select this clock as the source to Iris. Bit 2 must be set first, followed by this bit. And after RF calibration, this bit must be disabled first, followed by bit 2. 0x0: DISABLED 0x1: ENABLED Reset State: 0x0000

RFIF_RF_BUS_CONTROL (cont.)

Bits	Name	Description
5:4	SET_RF_BUS_RD_DELAY	Controls the delay value used by the RF bus interface state machine for register reads. By default (2'b00), the RF bus interface state machine inserts 3 cmd_clk cycles before it samples the read data (on the 4th cmd_clk cycle). Each value set in this register increases the delay inserted by the RF bus interface state machine before it samples the read data, by 1/2 cmd_clk cycle - i.e., 2'b01 causes the insertion of 3.5 cmd_clk cycles, and 2'b10 causes the insertion of 4 cmd_clk cycles. 0x0: DEFAULT 0x1: HALF_CYCLE 0x2: ONE_CYCLE 0x3: INVALID Reset State: 0x0000
3	SET_RF_BUS_FREQ	Controls the frequency setting of the RF bus interface cmd_clk signal. For Riva, two RF bus frequency values are supported - 60 MHz (default) and 30 MHz. When set to 1, this bit sets the RF bus frequency to be 30 MHz. When 0, the default mode of 60 MHz is selected. 0x0: V_60M_MODE 0x1: V_30M_MODE Reset State: 0x0000
2	ENABLE_RF_CALIBRATION	This bit is used to enable/disable the RF calibration mode. During RF calibration mode, an 80 MHz clock must be fed out on the cmd_clk signal, and it is this bit that is used to enable the selection of the 80 MHz clock onto cmd_clk. The entire RF calibration mode is under software control - software needs to set this bit when the 80 MHz clock is required, and disable this bit when calibration is complete. 0x0: DISABLED 0x1: ENABLED Reset State: 0x0000
1	ENABLE_DEBUG_MODE	This bit enables/disables debug mode. When this bit is set, and enable_rf_bus (bit 0) is 0, the RFIF will direct the agc_testbus signal and tx_en signal onto cmd_data and cmd_set respectively. This mode is disabled if enable_rf_bus is set (1), or this bit is disabled. 0x0: DISABLED 0x1: ENABLED Reset State: 0x0000
0	ENABLE_RF_BUS	This bit enables/disables access to the RF bus. When this bit is 0 (disabled), the RF bus pins are not driven by internal RFIF logic, but may be used to drive debug data over the RF bus. The ENABLE_DEBUG_MODE bit must be set for the debug mode to be in effect. To avoid any pin conflict, debug data is only driven on the RF bus pins, when both ENABLE_DEBUG_MODE is set and ENABLE_RF_BUS is disabled. 0x0: DISABLED 0x1: ENABLED Reset State: 0x0001

0x3000004 RFIF_RF_BUS_STATUS

Type: read-only
Reset State: 0x0000

These registers capture the status of the RF bus interface state machine and controlling logic.

RFIF_RF_BUS_STATUS

Bits	Name	Description
4	CALIB_DONE	Holds the current state of the Iris calibration mode done signal. When calibration mode is selected, this signal will reset to 0. On completion of calibration, this signal will capture the done signal returned from Iris. Reset State: 0x0000
3:0	RF_BUS_SM_STATE	Current state of the RF bus interface state machine. Reset State: 0x0000

0x3000008 RFIF_ARB_CONTROL

Type: read-write
Reset State: 0x000F

This set of registers are used by the arbitration module to enable/disable data path access to the RF bus interface.

RFIF_ARB_CONTROL

Bits	Name	Description
3	ENABLE_TXGAIN_COMMANDS	Enables/disables the Tx gain commands coming from the TXFIR. 0x0: DISABLED 0x1: ENABLED Reset State: 0x0001
2	ENABLE_RXGAIN_COMMANDS	Enables/disables the Rx gain commands coming from the AGC. 0x0: DISABLED 0x1: ENABLED Reset State: 0x0001
1	ENABLE_PHYHW_COMMANDS	This bit enables/disables accesses by PHY H/W over the RF bus interface. 0x0: DISABLED 0x1: ENABLED Reset State: 0x0001

RFIF_ARB_CONTROL (cont.)

Bits	Name	Description
0	ENABLE_RFAPB_COMMANDS	This bit enables/disables accesses by the RFAPB interface over the RF bus interface. 0x0: DISABLED 0x1: ENABLED Reset State: 0x0001

0x300000C RFIF_ARB_COMMAND

Type: read-write
Reset State: 0x000F

This set of registers are used by the arbitration module to issue RF commands requested by software over the RF interface bus.

RFIF_ARB_COMMAND

Bits	Name	Description
6:4	RF_CMD_DATA_WRD1	This field holds the first data word of the software requested RF command. Currently the only commands with data supported are the RF clock enable command, and the RF reset command, of which both require only a single data word. The encoding definitions provided are for the clock enable command only. The RF reset command data word should be set to all zero. 0x0: DISABLE_19P2 0x1: ENABLE_19P2 0x2: DISABLE_38P4 0x3: ENABLE_38P4 0x4: RESERVED_WRD4 0x5: RESERVED_WRD5 0x6: DISABLE_48 0x7: ENABLE_48 Reset State: 0x0000
3:1	RF_CMD	This field holds the RF_CMD to be issued. Default command is set to RF_RESET command. 0x0: CLOCK_ENABLE_CMD 0x1: MODE_CMD 0x2: RESERVED_CMD2 0x3: RESERVED_CMD3 0x4: RESERVED_CMD4 0x5: RESERVED_CMD5 0x6: RESERVED_CMD6 0x7: RESET_CMD Reset State: 0x0007

RFIF_ARB_COMMAND (cont.)

Bits	Name	Description
0	ISSUE_RF_CMD	This bit is used to initiate an RF command over the RF bus interface. Writing a 1 to this bit requests the arbiter to issue the command loaded in the RF_CMD field. Note that only RF commands with 1 data word are currently supported by this means. When issuing a command (by writing a 1 to this bit), the value in this bit will clear to zero to indicate that the current command is in progress. When the command has completed, the value of this bit will return to 1. Reading this bit returns the status described in the encoding section. 0x0: CMD_IN_PROGRESS 0x1: IDLE Reset State: 0x0001

0x3000010 RFIF_ARB_STATUS

Type: read-only
Reset State: 0x0000

These registers hold the current status of the arbitration module, and are used for debug and status checking.

RFIF_ARB_STATUS

Bits	Name	Description
15:12	RXGAIN_ABORTED_CMDS	Holds the number of RXGAIN commands aborted (by request). Reset State: 0x0000
11:8	RFAPB_DROPPED_CMDS	Holds the number of commands dropped because RFAPB accesses are disabled. Reset State: 0x0000
7:4	BLOCKED_CMDS	Holds the total number of RF commands blocked because the RF Bus has not been enabled. Reset State: 0x0000
3:0	ARB_SM_STATE	Captures the current state of the Arbitration state machine module. Used for debugging purposes. Reset State: 0x0000

0x3000014 RFIF_BT_CTRL_CFG

Type: read-write
Reset State: 0x0003

This register configures the behavior of the BT input signals with regards to the PHY.

RFIF_BT_CTRL_CFG

Bits	Name	Description
2	BT_RX_SHARING_EN	Enables simultaneous RX sharing of antenna with the BT device. Reset State: 0x0000
1	BT_MEDIUM_SHUTDOWN	Controls whether or not the bt_medium input is used to shutdown the PHY. 1 means it will, 0 means it won't. Reset State: 0x0001
0	BT_TX_SHUTDOWN	Controls whether or not the bt_tx input is used to shutdown the PHY. 1 means it will, 0 means it won't. Reset State: 0x0001

0x3000018 RFIF_TX_EN_CFG

Type: read-write
Reset State: 0x0000

This register controls the behaviour of the TX_EN signal.

RFIF_TX_EN_CFG

Bits	Name	Description
1	TX_OVERRIDE_VAL	If the Tx enable override is enabled, then this is the overriding value for the Tx. Reset State: 0x0000
0	OVERRIDE_EN	Setting this bit to 1 enables the override of the Tx enable. Reset State: 0x0000

0x300001C RFIF_RESET_CTRL

Type: read-write
Reset State: 0x0000

Reset control register.

RFIF_RESET_CTRL

Bits	Name	Description
4	STATS_RESET	Setting this to 1 resets all of the current debug statistics counters. Reset State: 0x0000
3	PHYHW_SM_RESET	Setting this to 1 resets all of the PHY H/W interface state machines. Reset State: 0x0000

RFIF_RESET_CTRL (cont.)

Bits	Name	Description
2	RF_BUS_IF_SM_RESET	Setting this to 1 resets the RF bus interface state machine. This should only be used if hang has somehow occurred in this state machine. Reset State: 0x0000
1	ARB_SM_RESET	Setting this to 1 resets the arbitration state machine. This should only be used if hang has somehow occurred in this state machine. Reset State: 0x0000
0	RFAPB_SM_RESET	Setting this to 1 resets the RFAPB state machine. This should only be used if hang has somehow occurred in this state machine. Reset State: 0x0000

0x3000020 RFIF_PHY_HW_STATUS

Type: read-only
Reset State: 0x0000

These registers hold the current status of the PHY HW module, and are used for debug and status checking.

RFIF_PHY_HW_STATUS

Bits	Name	Description
15:10	PHYHW_DROPPED_CMDS	Holds the number of commands dropped because PHY H/W and/or TX & RX gain commands are disabled. Reset State: 0x0000
9:8	MODE_SM_STATE	Captures the current state of the MODE state machine module. Used for debugging purposes. Reset State: 0x0000
7:5	REG_RDWR_SM_STATE	Captures the current state of the Register read/write state machine module. Used for debugging purposes. Reset State: 0x0000
4:3	TXGAIN_SM_STATE	Captures the current state of the TXGAIN state machine module. Used for debugging purposes. Reset State: 0x0000
2:0	RXGAIN_SM_STATE	Captures the current state of the RXGAIN state machine module. Used for debugging purposes. Reset State: 0x0000

0x3000024 RFIF_RFAPB_STATUS

Type: read-only
Reset State: 0x0000

Captures current status of the RFAPB module.

RFIF_RFAPB_STATUS

Bits	Name	Description
2:0	RFAPB_SM_STATE	Captures the current state of the RFAPB state machine module. Used for debugging purposes. Reset State: 0x0000

0x3000028 RFIF_ERROR_CONDS

Type: read-write
Reset State: 0x0000

Captures error conditions if they occur.

RFIF_ERROR_CONDS

Bits	Name	Description
0	WR_FIFO_RD_EMPTY_ERR	This condition indicates that the write data fifo (data to be written to IRIS) became empty. This should never occur. A write of 1 will clear this condition. Reset State: 0x0000

0x300002C RFIF_HKADC_RD_ADDR

Type: read-write
Reset State: 0x0535

Specifies the Iris read address for HKADC operations.

RFIF_HKADC_RD_ADDR

Bits	Name	Description
10:0	RD_ADDR	This field contains the read address for HKADC operations. Reset State: 0x0535

0x3000030 RFIF_HKADC_WR_ADDR

Type: read-write
Reset State: 0x0532

Specifies the Iris write address for HKADC operations.

RFIF_HKADC_WR_ADDR

Bits	Name	Description
10:0	WR_ADDR	This field contains the write address for HKADC operations. Reset State: 0x0532

0x3000034 RFIF_HKADC_CONV_TIMER

Type: read-write
Reset State: 0x007F

Specifies the time in units of 12.5ns (80MHz) that the RFIF will wait for the HKADC conversion to occur, before issuing a read to read the data from Iris.

RFIF_HKADC_CONV_TIMER

Bits	Name	Description
6:0	WAIT_CNT	Total time to wait for the HKADC conversion to complete (in units of 12.5ns). Reset State: 0x007F

0x3000400+0x10*n RFIF_RX_GAINn_0, n=[0..47]

Type: read-write
Reset State: 0x0000

Read write interface to the RX Gain look up Table

RFIF_RX_GAINn_0

Bits	Name	Description
15:0	RXGAIN_VALUE_0	Reset State: 0x0000

0x3000404+0x10*n RFIF_RX_GAINn_1, n=[0..47]

Type: read-write
Reset State: 0x0000

Read write interface to the RX Gain look up Table

RFIF_RX_GAINn_1

Bits	Name	Description
15:0	RXGAIN_VALUE_1	Reset State: 0x0000

0x3000408+0x10*n RFIF_RX_GAINn_2, n=[0..47]

Type: read-write
Reset State: 0x0000

Read write interface to the RX Gain look up Table

RFIF_RX_GAINn_2

Bits	Name	Description
6:0	RXGAIN_VALUE_2	Reset State: 0x0000

0x3000800+0x20*n RFIF_TX_GAINn_0, n=[0..31]

Type: read-write
Reset State: 0x0000

Read write interface to the TX Gain look up Table

RFIF_TX_GAINn_0

Bits	Name	Description
15:0	TXGAIN_VALUE_0	Reset State: 0x0000

0x3000804+0x20*n RFIF_TX_GAINn_1, n=[0..31]

Type: read-write
Reset State: 0x0000

Read write interface to the TX Gain look up Table

RFIF_TX_GAINn_1

Bits	Name	Description
15:0	TXGAIN_VALUE_1	Reset State: 0x0000

0x3000808+0x20*n RFIF_TX_GAINn_2, n=[0..31]

Type: read-write
Reset State: 0x0000

Read write interface to the TX Gain look up Table

RFIF_TX_GAINn_2

Bits	Name	Description
15:0	TXGAIN_VALUE_2	Reset State: 0x0000

0x300080C+0x20*n RFIF_TX_GAINn_3, n=[0..31]

Type: read-write
Reset State: 0x0000

Read write interface to the TX Gain look up Table

RFIF_TX_GAINn_3

Bits	Name	Description
15:0	TXGAIN_VALUE_3	Reset State: 0x0000

0x3000810+0x20*n RFIF_TX_GAINn_4, n=[0..31]

Type: read-write
Reset State: 0x0000

Read write interface to the TX Gain look up Table

RFIF_TX_GAINn_4

Bits	Name	Description
15:0	TXGAIN_VALUE_4	Reset State: 0x0000

0x3000814+0x20*n RFIF_TX_GAINn_5, n=[0..31]

Type: read-write
Reset State: 0x0000

Read write interface to the TX Gain look up Table

RFIF_TX_GAINn_5

Bits	Name	Description
10:0	TXGAIN_VALUE_5	Reset State: 0x0000

16.2.23 rxaclkctrl

0x3000000 RXACLKCTRL_ROOT_CLK_EN

Type: read-write
Reset State: 0x0000

RXACLKCTRL_ROOT_CLK_EN

Bits	Name	Description
2	CLK80_40D	Reset State: 0x0000
1	CLK160	Reset State: 0x0000
0	CLK80	Reset State: 0x0000

0x3000004 RXACLKCTRL_APB_BLOCK_CLK_EN

Type: read-write
Reset State: 0xFFFF

RXACLKCTRL_APB_BLOCK_CLK_EN

Bits	Name	Description
15	PHYCSXI	Reset State: 0x0001
14	FSCALE	Reset State: 0x0001
13	RXA	Reset State: 0x0001
12	RAHDR	Reset State: 0x0001
11	RADSCR	Reset State: 0x0001
10	VIT	Reset State: 0x0001
9	DINT	Reset State: 0x0001

RXACLKCTRL_APB_BLOCK_CLK_EN (cont.)

Bits	Name	Description
8	LMAP	Reset State: 0x0001
7	PTC	Reset State: 0x0001
6	RACTL_APB	Reset State: 0x0001
5	CHE	Reset State: 0x0001
4	INF	Reset State: 0x0001
3	FFT	Reset State: 0x0001
2	TDC	Reset State: 0x0001
1	BTCF	Reset State: 0x0001
0	RACTL	Reset State: 0x0001

0x3000008 RXACLKCTRL_APB_BLOCK_DYN_CLKG_DISABLE

Type: read-write
Reset State: 0x0040

RXACLKCTRL_APB_BLOCK_DYN_CLKG_DISABLE

Bits	Name	Description
15	PHYCSXI	Reset State: 0x0000
14	FSCALE	Reset State: 0x0000
13	RXA	Reset State: 0x0000
12	RAHDR	Reset State: 0x0000
11	RADSCR	Reset State: 0x0000
10	VIT	Reset State: 0x0000
9	DINT	Reset State: 0x0000
8	LMAP	Reset State: 0x0000
7	PTC	Reset State: 0x0000
6	RACTL_APB	Reset State: 0x0001
5	CHE	Reset State: 0x0000
4	INF	Reset State: 0x0000
3	FFT	Reset State: 0x0000
2	TDC	Reset State: 0x0000
1	BTCF	Reset State: 0x0000
0	RACTL	Reset State: 0x0000

0x300000C RXACLKCTRL_DYN_ANTSW_CLK_CTRL_DISABLE

Type: read-write
Reset State: 0x0000

RXACLKCTRL_DYN_ANTSW_CLK_CTRL_DISABLE

Bits	Name	Description
0	ANTSW_CTRL	Reset State: 0x0000

0x3000010 RXACLKCTRL_MAIN1_FAST_CLK_CTRL

Type: read-write
Reset State: 0x0152

Control for the auxiliary fast clock coming to Phy from external clock control logic.

RXACLKCTRL_MAIN1_FAST_CLK_CTRL

Bits	Name	Description
12	DBG_FORCE_FAST_ALWAYS	This is a debug-only mode configuration. Should always be left at 0 for normal purposes. When high, forces the fast_clk to be the source of clock for ALL 11AC packet types. Reset State: 0x0000
11	COMPLIANT_BEHAV	This bit when set to 1 enforces phy-mac interface signalling (related to 256qam processing) to comply with other modes (11a, 11n and 11ac) at the cost of increased latency in 20M and 40M modes depending on tx_bw setting. The following applies to how the clkdivratio for 20M packets is decided in compliant_behav case: *** The design forces this value to 1 when tx_bw_config is 1 or more. *** The value is forced to 0 when tx_bw_config is 0. The following applies to how the clkdivratio for 40M packets is decided- *** The design forces the value to 1 if tx_bw_config is 1. Otherwise a value of 1 or 2 can be used. When this bit is set to 0, all 256QAM STBC 20M packets will get 160MHz fastclk; all 256QAM STBC 40M packets will get either 160 or 320 MHz clock depending on extnclkdivmode40 above. Reset State: 0x0000
10:5	CLKCHGDLY	Specifies the delay (in number of 80MHz clocks) between assertion of fast_clk_en in ractl (in main2 domain) to when the processing of MCS 8 and 9 STBC data-symbols is going to start. This delay is required so as to allow multi-cycle operation of the enable. This delay should include CDC delays inside PHY as well as clock-generation delay. Tune this to the minimum required delay. Reset State: 0x000A

RXACLKCTRL_MAIN1_FAST_CLK_CTRL (cont.)

Bits	Name	Description
4:3	EXTNCLKDIVMODE40	This divmode determines the frequency of the clock being used by functional logic to demodulate 40MHz MCS8 and 9 STBC pkts. A value of 2 implies the clk used has same freq as that of the input fast clk. A value of 1 implies the clk used has one-half freq as that of the input fast clk. A value of 0 implies the clk used has one-quarter freq as that of the input fast clk. Compare this with the clock-division mechanism based on channel bandwidth configuration. Note that setting the value to < 2 will increase the latency of 40M packets to > 11 microseconds. Reset State: 0x0002
2:1	EXTNCLKDIVMODE20	This divmode determines the frequency of the clock being used by functional logic to demodulate 20MHz MCS8 and 9 STBC pkts. A value of 2 implies the clk used has same freq as that of the input fast clk. A value of 1 implies the clk used has one-half freq as that of the input fast clk. A value of 0 implies the clk used has one-quarter freq as that of the input fast clk. Compare this with the clock-division mechanism based on channel bandwidth configuration. Note that setting the value to 0 will increase the latency of 20M packets to > 12 microseconds so a value of 0 should never be used. A value of 2 is usable at the expense of power consumption penalty. *** NOT actually used *** Reset State: 0x0001
0	FORCE_CLK_DISABLE	When high, forcefully disables the clock to save power. When low, the functional logic decides the duration of the enable. Note that functional logic will ensure this clock is enabled only when STBC data symbols in 11AC MCS8 and MCS9 packets mode are being demodulated by RX. Reset State: 0x0000

16.2.24 rxclkctrl

0x3000000 RXCLKCTRL_ROOT_CLK_EN

Type: read-write
Reset State: 0x0000

RXCLKCTRL_ROOT_CLK_EN

Bits	Name	Description
9	CLK3BY4_S	Reset State: 0x0000
8	CLK1BY4_S	Reset State: 0x0000
7	CLK160_D	Reset State: 0x0000
6	CLK80_S	Reset State: 0x0000
5	CLK40	Reset State: 0x0000
4	CLK80_40D	Reset State: 0x0000

RXCLKCTRL_ROOT_CLK_EN (cont.)

Bits	Name	Description
3	CLK80_40S	Reset State: 0x0000
2	CLK160	Reset State: 0x0000
1	CLK_MIF_PHYDBG_INTF	Reset State: 0x0000
0	CLK80	0x0: DISABLE 0x0: ENABLE Reset State: 0x0000

0x3000004 RXCLKCTRL_APB_BLOCK_CLK_EN

Type: read-write
Reset State: 0x1531

RXCLKCTRL_APB_BLOCK_CLK_EN

Bits	Name	Description
13	RXFIR_DWNS	Reset State: 0x0000
12	AGC_APB	Reset State: 0x0001
11	AGC	Reset State: 0x0000
10	XBAR	Reset State: 0x0001
9	RFIF	Reset State: 0x0000
8	PHYDBG_APB	Reset State: 0x0001
7	PHYDBG	Reset State: 0x0000
6	CAL_EST	Reset State: 0x0000
5	CAL	Reset State: 0x0001
4	RXFIR	Reset State: 0x0001
3	PMI	Reset State: 0x0000
2	PHYINT	Reset State: 0x0000
1	TMUX	Reset State: 0x0000
0	RXB	0x0: DISABLE 0x1: ENABLE Reset State: 0x0001

0x3000008 RXCLKCTRL_APB_BLOCK_DYN_CLKG_DISABLE

Type: read-write
Reset State: 0x0010

RXCLKCTRL_APB_BLOCK_DYN_CLKG_DISABLE

Bits	Name	Description
8	PMIRDET	Reset State: 0x0000
6	PMICCA	Reset State: 0x0000
5	XBAR	Reset State: 0x0000
4	CAL_APB	Reset State: 0x0001
3	CAL	Reset State: 0x0000
2	RXFIR	Reset State: 0x0000
1	PMI	Reset State: 0x0000
0	RXB	0x0: ENABLE 0x1: DISABLE Reset State: 0x0000

0x300000C RXCLKCTRL_APB_BLOCK_DYN_CLKG_DISABLE_AGC

Type: read-write
Reset State: 0x0008

Since AGC has a bunch of sub blocks they need to have their own dynamic clock gate disable

RXCLKCTRL_APB_BLOCK_DYN_CLKG_DISABLE_AGC

Bits	Name	Description
8	CCADET	Reset State: 0x0000
7	DET11AC80	Reset State: 0x0000
6	DET11N40	Reset State: 0x0000
5	DET11A	Reset State: 0x0000
4	DET11B	Reset State: 0x0000
3	APB	Reset State: 0x0001
2	RDET	Reset State: 0x0000
1	PWR	Reset State: 0x0000
0	MAIN	Reset State: 0x0000

0x3000010 RXCLKCTRL_APB_SYNC_RESET

Type: command
Reset State: 0x0000

RXCLKCTRL_APB_SYNC_RESET

Bits	Name	Description
0	VALUE	Reset State: 0x0000

0x3000014 RXCLKCTRL_CLK_PHY_MAIN2_3BY4_DIV_BYPASS

Type: read-write
Reset State: 0x0000

RXCLKCTRL_CLK_PHY_MAIN2_3BY4_DIV_BYPASS

Bits	Name	Description
0	BYP	Reset State: 0x0000

0x3000018 RXCLKCTRL_BW_CONFIG

Type: read-only

RXCLKCTRL_BW_CONFIG

Bits	Name	Description
3:2	TX_VAL	
1:0	RX_VAL	

0x3000020 RXCLKCTRL_PHY_VERSION

Type: read-only
Reset State: 0xAA80

Contains information about the PHY variant type and revision number.

RXCLKCTRL_PHY_VERSION

Bits	Name	Description
15:6	REG_ID	This is an ID number that uniquely identifies this register as a PHY version register. Reset State: 0x02AA
5:3	REVISION	Revision number.
2:0	VARIANT	0x0: RIVA

16.2.25 tactl

0x3000000 TACTL_CFG

Type: read-write
Reset State: 0x0006

Tx-A Block Configuration and Setup Register

TACTL_CFG

Bits	Name	Description
3:2	B_11AC_CRC_MODE	When set instructs the TAHDR module to generate an 11n CRC and insert it into the HT-SIG2 symbol. 0x0: NO_CRC 0x1: OPT1 0x2: OPT2 0x3: OPT3 Reset State: 0x0001
1	B_11N_CRC_ENABLE	When set instructs the TAHDR module to generate an 11n CRC and insert it into the HT-SIG2 symbol. Reset State: 0x0001
0	TACTL_ABORT	When set instructs the tactl module to abort and return to idle state Reset State: 0x0000

0x3000004 TACTL_SCR_CONFIG

Type: read-write
Reset State: 0x007F

Configures the Tx-a scrambler with a programmable seed

TACTL_SCR_CONFIG

Bits	Name	Description
9	TASCR_BYPASS	When set puts the Scrambler in bypass mode Reset State: 0x0000
8	TASCR_LOAD	When set, the scrambler seed is immediately loaded with the programmed value. Thereafter, the seed is reset to the programmed value at the start of every 11a/n packet. Reset State: 0x0000
6:0	TASCR_SEED	Programmable seed for the scrambler Reset State: 0x007F

0x3000008 TACTL_TATMUX_CONFIG

Type: read-write
Reset State: 0x0000

The mux in txa_tmux will be selected using the select lines from this register

TACTL_TATMUX_CONFIG

Bits	Name	Description
5:0	MUX_SEL	Defaults to the 0th group Reset State: 0x0000

0x300000C TACTL_SCALE_20

Type: read-write
Reset State: 0x0080

This register contains an 8-bit amplitude scaling factor to be applied to all short preamble symbols of 20MHz packets.

TACTL_SCALE_20

Bits	Name	Description
7:0	VALUES	Reset State: 0x0080

0x3000010 TACTL_SCALE_40

Type: read-write
Reset State: 0x0080

This register contains an 8-bit amplitude scaling factor to be applied to all short preamble symbols of 40MHz packets.

TACTL_SCALE_40

Bits	Name	Description
7:0	VALUES	Reset State: 0x0080

0x3000014 TACTL_SCALE_80

Type: read-write
Reset State: 0x0080

This register contains an 8-bit amplitude scaling factor to be applied to all short preamble symbols of 80MHz packets.

TACTL_SCALE_80

Bits	Name	Description
7:0	VALUES	Reset State: 0x0080

0x3000018 TACTL_DOT11AC_SERVICE_OVERRIDE

Type: read-write
Reset State: 0x0000

Flag to insert APB-programmable value into SERVICE field for 11ac packets

TACTL_DOT11AC_SERVICE_OVERRIDE

Bits	Name	Description
0	FLAG	Reset State: 0x0000

0x300001C TACTL_DOT11AC_APB_SERVICE

Type: read-write
Reset State: 0x0000

Contains the 16-bit SERVICE field value

TACTL_DOT11AC_APB_SERVICE

Bits	Name	Description
15:0	VALUE	Reset State: 0x0000

0x3000020 TACTL_CTRL_STATE

Type: read-only

Indicates the last 4 states of the TXA controller

TACTL_CTRL_STATE

Bits	Name	Description
15:0	VALUE	Bits[15:12] = Prev (N-3) state Bits[11:8] = Prev (N-2) state Bits[7:4] = Prev (N-1) state Bits[3:0] = Current state

0x3000024 TACTL_PKT_REQ_COUNT

Type: read-only

TACTL_PKT_REQ_COUNT

Bits	Name	Description
15:0	VALUE	Counts number of requests made to MPI for current packet

0x3000028 TACTL_TAHDR_SYM_COUNT

Type: read-only

TACTL_TAHDR_SYM_COUNT

Bits	Name	Description
15:0	VALUE	Counts number of TXA_HDR symbol starts for current packet

0x300002C TACTL_TAQAM_SYM_COUNT

Type: read-only

TACTL_TAQAM_SYM_COUNT

Bits	Name	Description
15:0	VALUE	Counts number of TXA_QAM symbol starts for current packet

0x3000030 TACTL_LAST_SYM_PARAMS

Type: read-only

TACTL_LAST_SYM_PARAMS

Bits	Name	Description
15:10	RATE	Rate field for last TAHDR symbol processed
9:8	BW	Bandwidth of last packet processed
7:3	SYM_TYPE	Symbol type of last symbol processed in QAM module
2:0	PKT_TYPE	Packet type for last packet processed

0x3000034 TACTL_QAM_NSYMS

Type: write-only

TACTL_QAM_NSYMS

Bits	Name	Description
15:0	SYMCNT	Counts the total number of OFDM Symbols through the TX-A QAM Mapper

0x3000038 TACTL_NPKTS

Type: write-only

TACTL_NPKTS

Bits	Name	Description
15:0	PKTCNT	Counts the number of packet starts received from TXCTL

0x300003C TACTL_SCR_LFSR

Type: read-only
Reset State: 0x0000

State of LFSR in txa_scr

TACTL_SCR_LFSR

Bits	Name	Description
6:0	TASCR_LFSR	Current state of LFSR Reset State: 0x0000

0x3000040 TACTL_ALARMS

Type: read-only
Reset State: 0x0000

Monitor of all contributors to TXA abort

TACTL_ALARMS

Bits	Name	Description
5:0	VALUE	Bit[0] = Abort received from TXCTL Bit[1] = TXA Header error Bit[2] = Invalid data rate error Bit[3] = TXA Interleaver error Bit[4] = TXCTL packet start received when state machine busy Bit[5] = Incorrect bandwidth field in command word Reset State: 0x0000

0x3000044 TACTL_RESET_ALARMS

Type: command
Reset State: 0x0000

Resets the alarm flags

TACTL_RESET_ALARMS

Bits	Name	Description
0	RESET_ALARMS	When this register is written to with any value, a active high pulse is generated which will reset all alarm flags in the TACTL alarms register. Reset State: 0x0000

16.2.26 taqam

0x3000000 TAQAM_SCALE_BPSK

Type: read-write
Reset State: 0x007F

Amplitude scale factor for BPSK modulation

TAQAM_SCALE_BPSK

Bits	Name	Description
8:0	REG	Reset State: 0x007F

0x3000008 TAQAM_SCALE_QPSK

Type: read-write
Reset State: 0x005A

Amplitude scale factor for QPSK modulation

TAQAM_SCALE_QPSK

Bits	Name	Description
8:0	REG	Reset State: 0x005A

0x300000C TAQAM_SCALE_QAM16

Type: read-write
Reset State: 0x0050

Amplitude scale factor for 16QAM modulation

TAQAM_SCALE_QAM16

Bits	Name	Description
8:0	REG	Reset State: 0x0050

0x3000010 TAQAM_SCALE_QAM64

Type: read-write
Reset State: 0x004E

Amplitude scale factor for 64QAM modulation

TAQAM_SCALE_QAM64

Bits	Name	Description
8:0	REG	Reset State: 0x004E

0x3000014 TAQAM_SCALE_QAM256

Type: read-write
Reset State: 0x004E

Amplitude scale factor for 256QAM modulation

TAQAM_SCALE_QAM256

Bits	Name	Description
8:0	REG	Reset State: 0x004E

0x3000018 TAQAM_SCALE_LEGACY20

Type: read-write
Reset State: 0x0089

Amplitude scale factor for legacy packets and 11n/ac legacy symbols

TAQAM_SCALE_LEGACY20

Bits	Name	Description
8:0	REG	Reset State: 0x0089

0x300001C TAQAM_SCALE_LEGACY40

Type: read-write
Reset State: 0x0060

Amplitude scale factor for legacy 40MHz duplicate packets and 11n/ac 40MHz legacy symbols

TAQAM_SCALE_LEGACY40

Bits	Name	Description
8:0	REG	Reset State: 0x0060

0x3000020 TAQAM_SCALE_LEGACY80

Type: read-write
Reset State: 0x0085

Amplitude scale factor for legacy 80MHz duplicate packets and 11n/ac 80MHz legacy symbols

TAQAM_SCALE_LEGACY80

Bits	Name	Description
8:0	REG	Reset State: 0x0085

0x3000024 TAQAM_SCALE_HT20

Type: read-write
Reset State: 0x0085

Amplitude scale factor for (V)HT-LTF, HT-SIG in GF mode, VHT-SIG-B and Data 11n/ac 20MHz symbols

TAQAM_SCALE_HT20

Bits	Name	Description
8:0	REG	Reset State: 0x0085

0x3000028 TAQAM_SCALE_HT40

Type: read-write
Reset State: 0x005B

Amplitude scale factor for (V)HT-LTF, HT-SIG in GF mode, VHT-SIG-B and Data 11n/ac 40MHz symbols

TAQAM_SCALE_HT40

Bits	Name	Description
8:0	REG	Reset State: 0x005B

0x300002C TAQAM_SCALE_HT80

Type: read-write
Reset State: 0x007B

Amplitude scale factor for VHT-LTF, VHT-SIG-B and Data 11ac 80MHz symbols

TAQAM_SCALE_HT80

Bits	Name	Description
8:0	REG	Reset State: 0x007B

0x3000030 TAQAM_AC

Type: read-write
Reset State: 0x03E7

Programmable features to mitigate risk of spec change

TAQAM_AC

Bits	Name	Description
9	SB_ROT_EN	Reset State: 0x0001
8	CYC_ROT_EN	Reset State: 0x0001
7:0	PILOT80	Reset State: 0x00E7

16.2.27 tbapb

0x3000000 TBAPB_CRC16_CTRL

Type: read-write
Reset State: 0x0000

Controls CRC16 generator operation that calculates IEEE802.11b PLCP header CRC. For debugging purposes.

TBAPB_CRC16_CTRL

Bits	Name	Description
0	DIS	When set disables CRC16 calculation. Should be 0 (enabled) for normal operation. 0x0: ENABLE 0x1: DISABLE Reset State: 0x0000

0x3000004 TBAPB_SCRAMBLE_CTRL

Type: read-write
Reset State: 0x0000

Controls data scrambler operation that scrambled IEEE802.11b frame. For debugging purposes.

TBAPB_SCRAMBLE_CTRL

Bits	Name	Description
0	DIS	When set disables data scrambling by bypassing scrambler. Should be 0 (enabled) for normal operation. 0x0: ENABLE 0x1: DISABLE Reset State: 0x0000

0x3000008 TBAPB_TXB_DEBUG

Type: write-only
Reset State: 0x0000

Debug counter, counts bytes entered into the CRC16 generator module.

TBAPB_TXB_DEBUG

Bits	Name	Description
15:0	COUNT	Byte counters reset on read. Reset State: 0x0000

0x300000C TBAPB_LINEAR_DELAY_ANT1

Type: read-write
Reset State: 0x0002

Stores the select for the delay diversity value to be applied to txb chain2 samples in barker and cck modulated data

TBAPB_LINEAR_DELAY_ANT1

Bits	Name	Description
7:6	CCK11DIVDLY	0 implies no delay to chain2 cck11 modulated data 1 implies 1 delay (1 20MHz sample) to chain2 cck11 modulated data 2 implies 2 delays 3 implies 3 delays Reset State: 0x0000
5:3	CCK5DIVDLY	0 implies no delay to chain2 cck5 modulated data 1 implies 1 delay (1 20MHz sample) to chain2 cck5 modulated data 2 implies 2 delays 3 implies 3 delays 4 implies 4 delays 5 implies 5 delays 6 implies 6 delays 7 implies 7 delays Reset State: 0x0000
2:0	BRKDIVDLY	0 implies no delay to chain2 barker modulated data 1 implies 1 delay (1 20MHz sample) to chain2 barker modulated data 2 implies 2 delays 3 implies 3 delays 4 implies 4 delays 5 implies 5 delays 6 implies 6 delays 7 implies 7 delays Reset State: 0x0002

0x3000010 TBAPB_LINEAR_DELAY_ANT2

Type: read-write
Reset State: 0x0004

Stores the select for the delay diversity value to be applied to txb chain3 samples in barker and cck modulated data

TBAPB_LINEAR_DELAY_ANT2

Bits	Name	Description
7:6	CCK11DIVDLY	0 implies no delay to chain3 cck11 modulated data 1 implies 1 delay (1 20MHz sample) to chain3 cck11 modulated data 2 implies 2 delays 3 implies 3 delays Reset State: 0x0000
5:3	CCK5DIVDLY	0 implies no delay to chain3 cck5 modulated data 1 implies 1 delay (1 20MHz sample) to chain3 cck5 modulated data 2 implies 2 delays 3 implies 3 delays 4 implies 4 delays 5 implies 5 delays 6 implies 6 delays 7 implies 7 delays Reset State: 0x0000
2:0	BRKDIVDLY	0 implies no delay to chain3 barker modulated data 1 implies 1 delay (1 20MHz sample) to chain3 barker modulated data 2 implies 2 delays 3 implies 3 delays 4 implies 4 delays 5 implies 5 delays 6 implies 6 delays 7 implies 7 delays Reset State: 0x0004

0x3000014 TBAPB_LINEAR_DELAY_ANT3

Type: read-write
Reset State: 0x0006

Stores the select for the delay diversity value to be applied to txb chain4 samples in barker and cck modulated data

TBAPB_LINEAR_DELAY_ANT3

Bits	Name	Description
7:6	CCK11DIVDLY	0 implies no delay to chain4 cck11 modulated data 1 implies 1 delay (1 20MHz sample) to chain4 cck11 modulated data 2 implies 2 delays 3 implies 3 delays Reset State: 0x0000
5:3	CCK5DIVDLY	0 implies no delay to chain4 cck5 modulated data 1 implies 1 delay (1 20MHz sample) to chain4 cck5 modulated data 2 implies 2 delays 3 implies 3 delays 4 implies 4 delays 5 implies 5 delays 6 implies 6 delays 7 implies 7 delays Reset State: 0x0000
2:0	BRKDIVDLY	0 implies no delay to chain4 barker modulated data 1 implies 1 delay (1 20MHz sample) to chain4 barker modulated data 2 implies 2 delays 3 implies 3 delays 4 implies 4 delays 5 implies 5 delays 6 implies 6 delays 7 implies 7 delays Reset State: 0x0006

16.2.28 tdc

0x3000000 TDC_TDCSYM_IN

Type: write-only

Number of multiples of 80 baseband samples received by the TDC module (from the AGC module)

TDC_TDCSYM_IN

Bits	Name	Description
15:0	TDCSYM_IN	Number of multiples of 80 baseband samples received by the TDC module (from the AGC module)

0x3000004 TDC_TDCSYM_OUT

Type: write-only

Number of symbol start pulses received by the TDC module (from the RACTL module)

TDC_TDCSYM_OUT

Bits	Name	Description
15:0	TDCSYM_OUT	Number of symbol start pulses received by the TDC module (from the RACTL module)

0x3000008 TDC_TDCPKT_IN

Type: write-only

Number of packet start signals received by the TDC module

TDC_TDCPKT_IN

Bits	Name	Description
15:0	TDCPKT_IN	Number of packet start signals received by the TDC module

0x300000C TDC_CWDET_COUNT

Type: write-only

Number of times that the CW detector was triggered

TDC_CWDET_COUNT

Bits	Name	Description
15:0	CW_COUNT	Number of times that the CW detector was triggered

0x3000010 TDC_CWDET_STATUS

Type: read-only

Indicates whether CW has been detected by CWDET module, and if so at what location.

TDC_CWDET_STATUS

Bits	Name	Description
6	CWDET_EN	Indicates that CW notch is currently enabled.
5:0	CWDET_LOC	Location of last CW notch detected.

0x3000014 TDC_CWDET_OVERRIDE

Type: read-write
Reset State: 0x0000

Location of APB-programmable fixed CW notch

TDC_CWDET_OVERRIDE

Bits	Name	Description
6	APB_MODE	APB control of CW notch_location signal If this bit is set, the CW detector will override the calculated value of this signal with the APB-programmed value in the CWDET_NOTCH_LOC register. Default value = 1'b0; Reset State: 0x0000
5:0	NOTCH_LOC	Location of APB-programmable fixed CW notch Default value = 6'h0 Reset State: 0x0000

0x3000018 TDC_CWDET_TRIGGER

Type: command
Reset State: 0x0000

This register manually triggers the update of the CW notch enable and location in the AGC

TDC_CWDET_TRIGGER

Bits	Name	Description
0	TRIGGER	Writing any value to this register will pulse the cw_detected signal to the AGC if the APB_MODE bit has been set in the CWDET_NOTCH_LOC register Reset State: 0x0000

0x300001C TDC_APB_GAIN_THRESH_LLP64_1RX

Type: read-write
Reset State: 0x0016

This register contains the desired value of the TDC power calculator for 1 active chain for an ideal target backoff when receiving non-11n or 20MHz 11n packets.

TDC_APB_GAIN_THRESH_LLP64_1RX

Bits	Name	Description
4:0	THRESH	Default value = 5'd23 Adjusting this value will result in a different peak-to-mean ratio for the input data to the RXA engine. The default value, 5'd23, will result in a backoff value of 12dB. To set a different backoff, set to: round(16+2*log2(175)-T*log2(10)/5), where T is the target backoff in dB Reset State: 0x0016

0x3000020 TDC_APB_GAIN_THRESH_LLP64_2RX

Type: read-write
Reset State: 0x0016

This register contains the desired value of the TDC power calculator for 2 active chains for an ideal target backoff when receiving non-11n or 20MHz 11n packets.

TDC_APB_GAIN_THRESH_LLP64_2RX

Bits	Name	Description
4:0	THRESH	Default value = 5'd23 Adjusting this value will result in a different peak-to-mean ratio for the input data to the RXA engine. The default value, 5'd23, will result in a backoff value of 12dB. To set a different backoff, set to: round(16+2*log2(175)-T*log2(10)/5), where T is the target backoff in dB Reset State: 0x0016

0x3000024 TDC_APB_GAIN_THRESH_LLP128_1RX

Type: read-write
Reset State: 0x0014

This register contains the desired value of the TDC power calculator for 1 active chain for an ideal target backoff when receiving 40MHz 11n packets.

TDC_APB_GAIN_THRESH_LLP128_1RX

Bits	Name	Description
4:0	THRESH	Default value = 5'd21 Adjusting this value will result in a different peak-to-mean ratio for the input data to the RXA engine. The default value, 5'd21, will result in a backoff value of 12dB. To set a different backoff, set to: round(14+2*log2(175)-T*log2(10)/5), where T is the target backoff in dB Reset State: 0x0014

0x3000028 TDC_APB_GAIN_THRESH_LLP128_2RX

Type: read-write
Reset State: 0x0014

This register contains the desired value of the TDC power calculator for 2 active chains for an ideal target backoff when receiving 40MHz 11n packets.

TDC_APB_GAIN_THRESH_LLP128_2RX

Bits	Name	Description
4:0	THRESH	Default value = 5'd21 Adjusting this value will result in a different peak-to-mean ratio for the input data to the RXA engine. The default value, 5'd21, will result in a backoff value of 12dB. To set a different backoff, set to: round(14+2*log2(175)-T*log2(10)/5), where T is the target backoff in dB Reset State: 0x0014

0x300002C TDC_APB_GAIN_THRESH_HTLTF64_1RX

Type: read-write
Reset State: 0x0016

This register contains the desired value of the TDC power calculator for 1 active chain for an ideal target backoff when receiving 20MHz 11n mixed-mode packets with 1 active chain.

TDC_APB_GAIN_THRESH_HTLTF64_1RX

Bits	Name	Description
4:0	THRESH	Default value = 5'd23 Adjusting this value will result in a different peak-to-mean ratio for the input data to the RXA engine. The default value, 5'd23, will result in a backoff value of 12dB. To set a different backoff, set to: round(18+2*log2(79)-T*log2(10)/5), where T is the target backoff in dB Reset State: 0x0016

0x3000030 TDC_APB_GAIN_THRESH_HTLTF64_2RX

Type: read-write
Reset State: 0x0016

This register contains the desired value of the TDC power calculator for 2 active chains for an ideal target backoff when receiving 20MHz 11n mixed-mode packets with 2 active chains.

TDC_APB_GAIN_THRESH_HTLTF64_2RX

Bits	Name	Description
4:0	THRESH	Default value = 5'd23 Adjusting this value will result in a different peak-to-mean ratio for the input data to the RXA engine. The default value, 5'd23, will result in a backoff value of 12dB. To set a different backoff, set to: round(18+2*log2(79)-T*log2(10)/5), where T is the target backoff in dB Reset State: 0x0016

0x3000034 TDC_APB_GAIN_THRESH_HTLTF128_1RX

Type: read-write
Reset State: 0x0014

This register contains the desired value of the TDC power calculator for 1 active chain for an ideal target backoff when receiving 40MHz 11n mixed-mode packets with 1 active chain.

TDC_APB_GAIN_THRESH_HTLTF128_1RX

Bits	Name	Description
4:0	THRESH	Default value = 5'd21 Adjusting this value will result in a different peak-to-mean ratio for the input data to the RXA engine. The default value, 5'd21, will result in a backoff value of 12dB. To set a different backoff, set to: round(16+2*log2(79)-T*log2(10)/5), where T is the target backoff in dB Reset State: 0x0014

0x3000038 TDC_APB_GAIN_THRESH_HTLTF128_2RX

Type: read-write
Reset State: 0x0014

This register contains the desired value of the TDC power calculator for 2 active chains for an ideal target backoff when receiving 40MHz 11n mixed-mode packets with 2 active chains.

TDC_APB_GAIN_THRESH_HTLTF128_2RX

Bits	Name	Description
4:0	THRESH	Default value = 5'd21 Adjusting this value will result in a different peak-to-mean ratio for the input data to the RXA engine. The default value, 5'd21, will result in a backoff value of 12dB. To set a different backoff, set to: round(16+2*log2(79)-T*log2(10)/5), where T is the target backoff in dB Reset State: 0x0014

0x300003C TDC_APB_GAIN_THRESH_LLP256_1RX

Type: read-write
Reset State: 0x0016

This register contains the desired value of the TDC power calculator for 1 active chain for an ideal target backoff when receiving 40MHz 11n packets.

TDC_APB_GAIN_THRESH_LLP256_1RX

Bits	Name	Description
4:0	THRESH	Default value = 5'd21 Adjusting this value will result in a different peak-to-mean ratio for the input data to the RXA engine. The default value, 5'd21, will result in a backoff value of 12dB. To set a different backoff, set to: round(14+2*log2(175)-T*log2(10)/5), where T is the target backoff in dB Reset State: 0x0016

0x3000040 TDC_APB_GAIN_THRESH_LLP256_2RX

Type: read-write
Reset State: 0x0014

This register contains the desired value of the TDC power calculator for 2 active chains for an ideal target backoff when receiving 40MHz 11n packets.

TDC_APB_GAIN_THRESH_LLP256_2RX

Bits	Name	Description
4:0	THRESH	Default value = 5'd21 Adjusting this value will result in a different peak-to-mean ratio for the input data to the RXA engine. The default value, 5'd21, will result in a backoff value of 12dB. To set a different backoff, set to: round(14+2*log2(175)-T*log2(10)/5), where T is the target backoff in dB Reset State: 0x0014

0x3000044 TDC_APB_GAIN_THRESH_VHTLTF256_1RX

Type: read-write
Reset State: 0x0016

This register contains the desired value of the TDC power calculator for 1 active chain for an ideal target backoff when receiving 40MHz 11n mixed-mode packets with 1 active chain.

TDC_APB_GAIN_THRESH_VHTLTF256_1RX

Bits	Name	Description
4:0	THRESH	Default value = 5'd21 Adjusting this value will result in a different peak-to-mean ratio for the input data to the RXA engine. The default value, 5'd21, will result in a backoff value of 12dB. To set a different backoff, set to: round(16+2*log2(79)-T*log2(10)/5), where T is the target backoff in dB Reset State: 0x0016

0x3000048 TDC_APB_GAIN_THRESH_VHTLTF256_2RX

Type: read-write
Reset State: 0x0014

This register contains the desired value of the TDC power calculator for 2 active chains for an ideal target backoff when receiving 80MHz 11n mixed-mode packets with 2 active chains.

TDC_APB_GAIN_THRESH_VHTLTF256_2RX

Bits	Name	Description
4:0	THRESH	Default value = 5'd21 Adjusting this value will result in a different peak-to-mean ratio for the input data to the RXA engine. The default value, 5'd21, will result in a backoff value of 12dB. To set a different backoff, set to: round(16+2*log2(79)-T*log2(10)/5), where T is the target backoff in dB Reset State: 0x0014

0x300004C TDC_RAM_OVERFLOW

Type: read-only

Bit[0] of this register indicates the value of the TDC RAM overflow flag

TDC_RAM_OVERFLOW

Bits	Name	Description
0	RAM_OVERFLOW	Bit[0] of this register indicates the value of the TDC RAM overflow flag

16.2.29 tpc

0x3000000 TPC_TXPWR_OVERRIDE0

Type: read-write
Reset State: 0x0033

Register allows to override the automatic power control algorithm on transmit chains.

TPC_TXPWR_OVERRIDE0

Bits	Name	Description
10:6	RF_POWER	Override power control loop and write directly to the RF chip Reset State: 0x0000
5:0	FINE_POWER	Override power control loop and write directly to the gain multipliers Reset State: 0x0033

0x3000004 TPC_TXPWR_ENABLE

Type: read-write
Reset State: 0x0003

controls the power gain mode.

TPC_TXPWR_ENABLE

Bits	Name	Description
2	FIXED_RF_GAIN	fixed_rf_gain and en (clpc_en) are used to set the tpc mode. When fixed_rf_gain is set, a single rf gain value is used for the tx power control. CLPC Modes 1 and 2 require fixed_rf_gain be set. In Mode 1, rf gain will be static, in Mode 2, the gain value will be adjusted based on feadback from the PDADC. Reset State: 0x0000

TPC_TXPWR_ENABLE (cont.)

Bits	Name	Description
1	OVERRIDE	When set the rf and digital gain values from the TXPWR_OVERRIDE register are used for all transmit power values. Reset State: 0x0001
0	EN	en (clpc_en) and fixed_rf_gain are used to set the tpc mode. When en is set, the gain LUTs will be updated based on the feedback from the PDADC. CLPC Modes 2 and 3 require en be set. Reset State: 0x0001

0x3000008 TPC_ADC_CTRL_GET_ADC

Type: command

ADC control port. Starts conversion.

TPC_ADC_CTRL_GET_ADC

Bits	Name	Description
0	GET_ADC	Write to this register to get ADC readout (start the conversion). This register was used in Titan to perform temperature measurement. Not used in Taurus.

0x300000C TPC_ADC_STATUS

Type: read-only

ADC status port, shows when ADC is ready (conversion finished).

TPC_ADC_STATUS

Bits	Name	Description
2	FAILED	0x0: SUCCESS 0x1: FAILURE
1	BUSY_P	When 0, either failure happened or result of power measurement is available in SENSED_PWR register. 0x0: IDLE 0x1: BUSY
0	BUSY_T	Busy with a APB-initiated conversion. To be polled until 0. When 0, either failure happened or result of conversion is available in ADC_DATA register. 0x0: IDLE 0x1: BUSY

0x3000010 TPC_MAN_TXPWR

Type: command

Manual TX gain command strobe.

TPC_MAN_TXPWR

Bits	Name	Description
0	STRB	Write to this register to manually send out a TX gain command when in override mode.

0x3000014 TPC_MAX_RF_GAIN

Type: read-write
Reset State: 0x001F

Contains the maximum RF gain to which the power control loop operates. This is different for the 2.4 vs. 5GHz bands.

TPC_MAX_RF_GAIN

Bits	Name	Description
4:0	VALUE	Default 15, i.e., 20dBm (2.4GHz value) Should be set to 9 (16dBm) for 5GHz. Reset State: 0x001F

0x3000018 TPC_MIN_RF_GAIN

Type: read-write
Reset State: 0x0000

Contains the minimum RF gain to which the power control loop operates. This is different for the 2.4 vs. 5GHz bands.

TPC_MIN_RF_GAIN

Bits	Name	Description
4:0	VALUE	Default 15, i.e., 20dBm (2.4GHz value) Should be set to 9 (16dBm) for 5GHz. Reset State: 0x0000

0x300001C TPC_MAX_DIGITAL_GAIN

Type: read-write
Reset State: 0x000F

Max value of tx digital gain range.

TPC_MAX_DIGITAL_GAIN

Bits	Name	Description
3:0	VALUE	Default value = 15 Reset State: 0x000F

0x3000020 TPC_MID_DIGITAL_GAIN

Type: read-write
Reset State: 0x0008

Mid value of tx digital gain range. Must be set to 1 or more!

TPC_MID_DIGITAL_GAIN

Bits	Name	Description
3:0	VALUE	Default value = 8 Reset State: 0x0008

0x3000024 TPC_MIN_DIGITAL_GAIN

Type: read-write
Reset State: 0x0000

Min value of tx digital gain range.

TPC_MIN_DIGITAL_GAIN

Bits	Name	Description
3:0	VALUE	Default value = 0 Reset State: 0x0000

0x300002C TPC_RC_DELAY

Type: read-write
Reset State: 0x04B0

Contains the delay between the start of TX and the start of power measurement.

TPC_RC_DELAY

Bits	Name	Description
12:0	DELAY	Default 1200, i.e., 15uS @ 80MHz clock. Value automatically adjusted for static bandwidth so that duration for given APB value is constant for all bandwidths. Reset State: 0x04B0

0x3000030 TPC_SENSED_PWR0

Type: read-only

Contains data from the Pwr ADCs which sensed the cygnus power during transmit operation

TPC_SENSED_PWR0

Bits	Name	Description
10:0	VALUE	PWRADC0 readback during transmit.

0x3000034 TPC_ADCTIMEOUT

Type: read-write
Reset State: 0x0900

Contains Pwr ADC response timeout value

TPC_ADCTIMEOUT

Bits	Name	Description
15:0	VALUE	Specifies the number of operating clocks that power-adc state machine can be in non-idle state and beyond that point, the power-adc response failure will be declared and state machine will be brought to idle. Value automatically adjusted for static bandwidth so that duration for given APB value is constant for all bandwidths. Reset State: 0x0900

0x3000038 TPC_APBACCESS

Type: read-write
Reset State: 0x0000

Selects APB access control

TPC_APBACCESS

Bits	Name	Description
0	SELECT	Set this bit to high to enable APB access of TPC memory Reset State: 0x0000

0x300003C TPC_PTADC_FSM_RST

Type: command

This register does the resetting of the state machine which interacts with power-adc analog interface

TPC_PTADC_FSM_RST

Bits	Name	Description
0	RST	Write to this register to reset

0x3000044 TPC_PDADC_RANGE

Type: read-write
Reset State: 0x0001

This register defines which portion of the 11-bit input PDADC sample is fed to the 8-bit LUT

TPC_PDADC_RANGE

Bits	Name	Description
1:0	SELECT	2'h0 : selects bits [10:3] of input PDADC sample 2'h1 : selects bits [9:2] of input PDADC sample 2'h2 : selects bits [8:1] of input PDADC sample 2'h3 : selects bits [7:0] of input PDADC sample Reset State: 0x0001

0x3000048 TPC_PDADC_OFFSET

Type: read-write
Reset State: 0x0000

Offset value to be subtracted from raw PDADC value

TPC_PDADC_OFFSET

Bits	Name	Description
10:0	VALUE	Reset State: 0x0000

0x300004C TPC_GAIN_OFFSET1

Type: read-write
Reset State: 0x0000

Open Loop gain values for converting digital to an absolute digital gain value for the TXFIR fine gain block.

TPC_GAIN_OFFSET1

Bits	Name	Description
11:6	OL_11B	Reset State: 0x0000
5:0	OL_OFDM	Reset State: 0x0000

0x3000050 TPC_GAIN_OFFSET2

Type: read-write
Reset State: 0x030C

Closed Loop gain values for converting digital to an absolute digital gain value for the TXFIR fine gain block.

TPC_GAIN_OFFSET2

Bits	Name	Description
11:6	CL_11B	Reset State: 0x000C
5:0	CL_OFDM	Reset State: 0x000C

0x3000800+0x4*n TPC_POWERDET0_RAMn, n=[0..255]

Type: read-write

Calibration data for the power detector

TPC_POWERDET0_RAMn

Bits	Name	Description
5:0	POWER	

0x3000C00+0x4*n TPC_RF_GAIN_LUT0n, n=[0..31]

Type: read-write

RF Course gain LUT

TPC_RF_GAIN_LUT0n

Bits	Name	Description
4:0	RF_GAIN	

0x3000C80+0 x4*n TPC_DIGITAL_GAIN_LUT0n, n=[0..31]

Type: read-write

Digital fine gain LUT

TPC_DIGITAL_GAIN_LUT0n

Bits	Name	Description
3:0	DIG_GAIN	

16.2.30 txclkctrl

0x3000000 TXCLKCTRL_ROOT_CLK_EN

Type: read-write
Reset State: 0x0000

TXCLKCTRL_ROOT_CLK_EN

Bits	Name	Description
3	CLK60	Reset State: 0x0000
2	CLK80_3BY4	Reset State: 0x0000
1	CLK160	Reset State: 0x0000
0	CLK80	Reset State: 0x0000

0x3000004 TXCLKCTRL_APB_BLOCK_CLK_EN

Type: read-write
Reset State: 0x01FF

TXCLKCTRL_APB_BLOCK_CLK_EN

Bits	Name	Description
9	TATMUX	Reset State: 0x0000
8	TPC	Reset State: 0x0001
7	TXFIR_APB	Reset State: 0x0001

TXCLKCTRL_APB_BLOCK_CLK_EN (cont.)

Bits	Name	Description
6	TXFIR	Reset State: 0x0001
5	TXB	Reset State: 0x0001
4	TXA_APB	Reset State: 0x0001
3	TXA	Reset State: 0x0001
2	TXCTL_APB	Reset State: 0x0001
1	TXCTL	Reset State: 0x0001
0	MPI	Reset State: 0x0001

0x3000008 TXCLKCTRL_APB_BLOCK_DYN_CLKG_DISABLE

Type: read-write
Reset State: 0x0094

TXCLKCTRL_APB_BLOCK_DYN_CLKG_DISABLE

Bits	Name	Description
8	TPC	Reset State: 0x0000
7	TXFIR_APB	Reset State: 0x0001
6	TXFIR	Reset State: 0x0000
5	TXB	Reset State: 0x0000
4	TXA_APB	Reset State: 0x0001
3	TXA	Reset State: 0x0000
2	TXCTL_APB	Reset State: 0x0001
1	TXCTL	Reset State: 0x0000
0	MPI	Reset State: 0x0000

16.2.31 txctl

0x3000000 TXCTL_FIR_MODE

Type: read-write
Reset State: 0x00C4

This register is used to switch in a test waveform feed to the TX FIR instead of the normal packet data stream and to manually enable the DACs and RF chains during the test mode.!!

NOTE The user must also appropriately program the DAC_SHUTDOWN register to ensure that the DAC standby and shutdown registers are configured correctly

TXCTL_FIR_MODE

Bits	Name	Description
9:8	TEST_BW_MODE	This field sets the bandwidth parameter when the TX is in WFM (test) mode. Default 2'h0 0x0: V_20MHZ 0x1: V_40MHZ 0x2: V_80MHZ Reset State: 0x0000
7	DIS_11MBPS	When set disables secondary antennae (i.e., all antennae except ant0) for 11 Mbps mode. Should be 1 (antennae disabled) for normal operation. 0x0: ENABLE 0x1: DISABLE Reset State: 0x0001
6	DIS_5MBPS	When set disables secondary antennae (i.e., all antennae except ant0) for 5.5 Mbps mode. Should be 1 (antennae disabled) for normal operation. 0x0: ENABLE 0x1: DISABLE Reset State: 0x0001
2	ANT_EN	4'bxxx0 -> none (No DAC/RF chains enabled) 4'bxxx1 -> zero (DAC/RF chain 0 enabled) This field defines which TX CHAINS (DAC and RF) are enabled in the waveform (test) mode of operation and also for packets that request the default TX enable configuration. Default 1'b1, i.e., Chain 0 enabled. Reset State: 0x0001
1	TEST_FILTER_SELECT	This bit selects the filter coefficients in the TX FIR when in test mode. Default 0 0x0: OFDM 0x1: V_11B Reset State: 0x0000
0	SELECT_FIRMODE	This bit selects the input to the TX FIR, 0=Normal, 1=WFM generator. Default 0 0x0: NORMAL 0x1: GENERATOR Reset State: 0x0000

0x3000004 TXCTL_RAMP_UP_11A

Type: read-write
Reset State: 0x004C

Specifies ramp up time for OFDM packets. Delay between RF enable and time that IQ waveform is presented on IQ outputs.

TXCTL_RAMP_UP_11A

Bits	Name	Description
9:0	TIMER	Specifies the time that the TX takes to ramp up before the base band data can be shifted into it. Measured in increments of 6.25 ns for Spica (12.5 ns for Libra) from 0 to 6.4 us (12.8us for Libra). Default 40, ie 0.25us in Gen5, 0.5uS in Libra 0x0: MIN 0x1: STEP 0x3FF: MAX Reset State: 0x004C

0x3000008 TXCTL_RAMP_UP_11B

Type: read-write
Reset State: 0x0024

Specifies ramp up time for 802.11b packets. Delay between RF enable and time that IQ waveform is presented on IQ outputs.

TXCTL_RAMP_UP_11B

Bits	Name	Description
9:0	TIMER	Specifies the time that the TX takes to ramp up before the base band data can be shifted into it. Measured in increments of 6.25 ns for Spica (12.5 ns for Libra) from 0 to 6.4 us (12.8us for Libra). Default 40, ie 0.25us in Gen5, 0.5uS in Libra 0x0: MIN 0x1: STEP 0x3FF: MAX Reset State: 0x0024

0x300000C TXCTL_RAMP_DOWN

Type: read-write
Reset State: 0x0050

Specifies ramp down time. Delay between end of IQ waveform and de-assertion of the RF enable to accommodate the delay through the DACs.

TXCTL_RAMP_DOWN

Bits	Name	Description
9:0	TIMER	Specifies the time that the TX takes to ramp up before the base band data can be shifted into it. Measured in increments of 6.25 ns for Spica (12.5 ns for Libra) from 0 to 6.4 us (12.8us for Libra). Default 80, ie 0.5us in Gen5, 1uS in Libra 0x0: MIN 0x1: STEP 0x3FF: MAX Reset State: 0x0050

0x3000010 TXCTL_TESTMUX_SELECT

Type: read-write
Reset State: 0x0000

Select the input of the test mux

TXCTL_TESTMUX_SELECT

Bits	Name	Description
8	TXFIRIN	0x1: CH0 Reset State: 0x0000
7:4	VIT	0x0: TXSM 0x1: TXCTL 0x2: TPCTXF 0x3: MPITXFA 0x4: MPITXFB 0x5: MPID 0x6: MPIV 0x7: TPC Reset State: 0x0000
2:0	DAT	0x0: DACIN 0x1: TXA 0x2: TXFIR 0x3: TPC 0x4: TXCTRL 0x5: TXCTL_MPI 0x6: MPI_TXCTL Reset State: 0x0000

0x3000014 TXCTL_DAC_CONTROL

Type: read-write
Reset State: 0x0001

This register controls DAC and RF enable signals such as standby and TX enables. Also, can control the DAC STANDBY and RF TX enable signals

TXCTL_DAC_CONTROL

Bits	Name	Description
9	TXEN_OVERRIDE_EN	0x0: NORMAL 0x1: OVERRIDE Reset State: 0x0000
8	DAC_OVERRIDE_EN	0x0: NORMAL 0x1: OVERRIDE Reset State: 0x0000
4	TXEN0_OVERRIDE_VAL	0x0: TXEN_OFF 0x1: TXEN_ON Reset State: 0x0000
0	CH0STDBY_OVERRIDE_VAL	0x0: DAC_ON 0x1: DAC_OFF Reset State: 0x0001

0x3000018 TXCTL_DAC_STDBY

Type: read-write
Reset State: 0x0181

This register controls the timing of DAC STANDBY signals

TXCTL_DAC_STDBY

Bits	Name	Description
8:0	TIMING	Each bit corresponds to one of the possible state of the TXCTL state machine. The states are as follows: Bit 0 = TXCTL_IDLE Bit 1 = TXCTL_RFWARM Bit 2 = TXCTL_START Bit 3 = reserved (unused) Bit 4 = TXCTL_RAMPUP Bit 5 = TXCTL_TX Bit 6 = TXCTL_SHUTOFF Bit 7 = TXCTL_TPC Bit 8 = TXCTL_OVERRIDE Reset State: 0x0181

0x300001C TXCTL_PLCP_OVERRIDE

Type: read-write
Reset State: 0x0000

This register contains an override mask and override values for HT-SIG fields.

TXCTL_PLCP_OVERRIDE

Bits	Name	Description
8:7	NESS	Override value for Ness field Reset State: 0x0000
6	RSVR	Override value for Reserved field Reset State: 0x0000
5	SOUND	Override value for Not-sounding field Reset State: 0x0000
4	SMOOTH	Override value for Smoothing field Reset State: 0x0000
3:0	MASK	Override mask for {Ness, Reserved, Not_sounding, Smoothing} fields Reset State: 0x0000

0x3000020 TXCTL_FSHIFT

Type: read-write
Reset State: 0x0017

When enabled, this register defines the value of the frequency shift applied to quarter and half-bandwidth packets. For instance, a 20MHz packet in an 80MHz channel is considered as a quarter-bandwidth packet and its frequency shift would be defined by the bw14 field. Similarly, the frequency shift for a 20MHz packet in a 40MHz channel or 40MHz packet in an 80MHz channel would be defined by the bw12 field

TXCTL_FSHIFT

Bits	Name	Description
4:2	BW14	0x0: ZERO 0x1: P10 0x2: P20 0x3: P30 0x4: RESERVED 0x5: M30 0x6: M20 0x7: M10 Reset State: 0x0005

TXCTL_FSHIFT (cont.)

Bits	Name	Description
1:0	BW12	0x0: ZERO 0x1: P20 0x2: RESERVED 0x3: M20 Reset State: 0x0003

0x3000024 TXCTL_ROTATION

Type: read-write
Reset State: 0xAAA5

Defines the phase rotation for each 20MHz subband

TXCTL_ROTATION

Bits	Name	Description
15:14	SB3_80V	Rotation value for subband 3 in VHT portion of 80MHz packets Reset State: 0x0002
13:12	SB3_80L	Rotation value for subband 3 in legacy portion of 80MHz packets Reset State: 0x0002
11:10	SB2_80V	Rotation value for subband 2 in VHT portion of 80MHz packets Reset State: 0x0002
9:8	SB2_80L	Rotation value for subband 2 in legacy portion of 80MHz packets Reset State: 0x0002
7:6	SB1_80V	Rotation value for subband 1 in VHT portion of 80MHz packets Reset State: 0x0002
5:4	SB1_80L	Rotation value for subband 1 in legacy portion of 80MHz packets Reset State: 0x0002
3:2	SB1_40V	Rotation value for subband 1 in VHT portion of 40MHz packets Reset State: 0x0001
1:0	SB1_40L	Rotation value for subband 1 in legacy portion of 40MHz packets 0x0: V_0 0x1: V_90 0x2: V_180 0x3: V_270 Reset State: 0x0001

0x3000028 TXCTL_SOFTRESET

Type: command
Reset State: 0x0000

Resets the PHY transmitter

TXCTL_SOFTRESET

Bits	Name	Description
0	RESET	When this register is written to with any value, a active high pulse is generated which will reset the whole of Phy Tx. Reset State: 0x0000

0x300002C TXCTL_WATCHDOG_START

Type: read-write
Reset State: 0x0000

Allowed time for state machine to remain in START state

TXCTL_WATCHDOG_START

Bits	Name	Description
15:0	CYCLES	Allowed period of time in this state = (Register value * 128 * 12.5)ns. The state machine automatically adjusts for 20/40/80MHz bandwidth settings. Setting a value of 0 disables the watchdog. Reset State: 0x0000

0x3000030 TXCTL_WATCHDOG_RFWARM

Type: read-write
Reset State: 0x0009

Allowed time for state machine to remain in RFWARM state

TXCTL_WATCHDOG_RFWARM

Bits	Name	Description
15:0	CYCLES	Allowed period of time in this state = (Register value * 128 * 12.5)ns. The state machine automatically adjusts for 20/40/80MHz bandwidth settings. Setting a value of 0 disables the watchdog. Reset State: 0x0009

0x3000034 TXCTL_WATCHDOG_RAMPUP

Type: read-write
Reset State: 0x0000

Allowed time for state machine to remain in RAMPUP state

TXCTL_WATCHDOG_RAMPUP

Bits	Name	Description
15:0	CYCLES	Allowed period of time in this state = (Register value * 128 * 12.5)ns. The state machine automatically adjusts for 20/40/80MHz bandwidth settings. Setting a value of 0 disables the watchdog. Reset State: 0x0000

0x3000038 TXCTL_WATCHDOG_TX

Type: read-write
Reset State: 0x0000

Allowed time for state machine to remain in TX state

TXCTL_WATCHDOG_TX

Bits	Name	Description
15:0	CYCLES	Allowed period of time in this state = (Register value * 128 * 12.5)ns. The state machine automatically adjusts for 20/40/80MHz bandwidth settings. Setting a value of 0 disables the watchdog. Reset State: 0x0000

0x300003C TXCTL_WATCHDOG_SHUTOFF

Type: read-write
Reset State: 0x0000

Allowed time for state machine to remain in SHUTOFF state

TXCTL_WATCHDOG_SHUTOFF

Bits	Name	Description
15:0	CYCLES	Allowed period of time in this state = (Register value * 128 * 12.5)ns. The state machine automatically adjusts for 20/40/80MHz bandwidth settings. Setting a value of 0 disables the watchdog. Reset State: 0x0000

0x3000040 TXCTL_WATCHDOG_TPC

Type: read-write
Reset State: 0x0000

Allowed time for state machine to remain in TPC state

TXCTL_WATCHDOG_TPC

Bits	Name	Description
15:0	CYCLES	Allowed period of time in this state = (Register value * 128 * 12.5)ns. The state machine automatically adjusts for 20/40/80MHz bandwidth settings. Setting a value of 0 disables the watchdog. Reset State: 0x0000

0x3000044 TXCTL_MAX_TXBUSY

Type: read-write
Reset State: 0x0000

Holds the max active duration of the txctl_mpi_txbusy signal (measured in 160MHz clock cycles) Default value of 0 disables the timeout event

TXCTL_MAX_TXBUSY

Bits	Name	Description
15:0	VALUE	Reset State: 0x0000

0x3000048 TXCTL_MAX_TXENB

Type: read-write
Reset State: 0x0000

Holds the max active duration of the RF TX enables (measured in 160MHz clock cycles) Default value of 0 disables the timeout event

TXCTL_MAX_TXENB

Bits	Name	Description
15:0	VALUE	Reset State: 0x0000

0x300004C TXCTL_TXBUSY_ALARM

Type: write-only

Counts number of TXBUSY timeout events

TXCTL_TXBUSY_ALARM

Bits	Name	Description
15:0	COUNT	

0x3000050 TXCTL_TXEN_ALARM

Type: write-only

Counts number of TXEN timeout events

TXCTL_TXEN_ALARM

Bits	Name	Description
15:0	COUNT	

0x3000054 TXCTL_TXCTL_STATE

Type: read-only

Stores last four states of the TXCTL state machine.

TXCTL_TXCTL_STATE

Bits	Name	Description
15:0	VALUE	Bits[15:12] = Previous (N-3) state Bits[11:8] = Previous (N-2) state Bits[7:4] = Previous (N-1) state Bits[3:0] = Current state

0x3000058 TXCTL_LAST_PKT_PARAMS1

Type: read-only

Stores the packet type, RATE field, Nss, BW mode and subband params for the last command word received.

TXCTL_LAST_PKT_PARAMS1

Bits	Name	Description
12:6	RATE	MCS Rate parameter
5:4	BANDWIDTH	Bandwidth mode parameter 00 = 20MHz packet 01 = 40MHz packet 10 = 80MHz packet 11 = Reserved
3	DUPLICATE	Subband duplicate parameter

TXCTL_LAST_PKT_PARAMS1 (cont.)

Bits	Name	Description
2:0	PKT_TYPE	Packet type parameter

0x300005C TXCTL_LAST_PKT_PACKET_LENGTH

Type: read-only

Stores the PACKET length parameter for the last command word received.

TXCTL_LAST_PKT_PACKET_LENGTH

Bits	Name	Description
15:0	VALUE	PACKET length parameter

0x3000060 TXCTL_LAST_PKT_LSIG_LENGTH

Type: read-only

Stores the LSIG length parameter for the last command word received.

TXCTL_LAST_PKT_LSIG_LENGTH

Bits	Name	Description
11:0	VALUE	LSIG length parameter

0x3000064 TXCTL_LAST_TX_POWER

Type: read-only

Stores the TX power parameter for the last command word received.

TXCTL_LAST_TX_POWER

Bits	Name	Description
4:0	VALUE	Packet TX power parameter

0x3000068 TXCTL_WATCHDOG_ALARM

Type: write-only

Counts number of WATCHDOG_ALARM abort pulses generated by the TXCTL module.

TXCTL_WATCHDOG_ALARM

Bits	Name	Description
15:0	COUNT	

0x300006C TXCTL_PKT_INVALID_ALARM

Type: write-only

Counts number of PKT_INVALID_ALARM abort pulses generated by the TXCTL module.

TXCTL_PKT_INVALID_ALARM

Bits	Name	Description
15:0	COUNT	

0x3000070 TXCTL_TXA_ABORT_ALARM

Type: write-only

Counts number of abort pulses generated by the TXA module.

TXCTL_TXA_ABORT_ALARM

Bits	Name	Description
15:0	COUNT	

0x3000074 TXCTL_LEGACY_PKTS

Type: write-only

Counts number of IEEE 802.11a packets transmitted.

TXCTL_LEGACY_PKTS

Bits	Name	Description
15:0	COUNT	Legacy packet counter.

0x3000078 TXCTL_GF_SIMO_20_PKTS

Type: write-only

Counts number of GF SIMO 20MHz packets transmitted.

TXCTL_GF_SIMO_20_PKTS

Bits	Name	Description
15:0	COUNT	GF SIMO 20MHz packet counter.

0x300007C TXCTL_GF_SIMO_40_PKTS

Type: write-only

Counts number of GF SIMO 40MHz packets transmitted.

TXCTL_GF_SIMO_40_PKTS

Bits	Name	Description
15:0	COUNT	GF SIMO 40MHz packet counter.

0x3000080 TXCTL_MM_SIMO_20_PKTS

Type: write-only

Counts number of mixed-mode SIMO 20MHz packets transmitted.

TXCTL_MM_SIMO_20_PKTS

Bits	Name	Description
15:0	COUNT	mixed-mode SIMO 20MHz packet counter.

0x3000084 TXCTL_MM_SIMO_40_PKTS

Type: write-only

Counts number of mixed-mode SIMO 40MHz packets transmitted.

TXCTL_MM_SIMO_40_PKTS

Bits	Name	Description
15:0	COUNT	mixed-mode SIMO 40MHz packet counter.

0x3000088 TXCTL_AC_SIMO_20_PKTS

Type: write-only

Counts number of 11ac SIMO 20MHz packets transmitted.

TXCTL_AC_SIMO_20_PKTS

Bits	Name	Description
15:0	COUNT	11ac SIMO 20MHz packet counter.

0x300008C TXCTL_AC_SIMO_40_PKTS

Type: write-only

Counts number of 11ac SIMO 40MHz packets transmitted.

TXCTL_AC_SIMO_40_PKTS

Bits	Name	Description
15:0	COUNT	11ac SIMO 40MHz packet counter.

0x3000090 TXCTL_AC_SIMO_80_PKTS

Type: write-only

Counts number of 11ac SIMO 80MHz packets transmitted.

TXCTL_AC_SIMO_80_PKTS

Bits	Name	Description
15:0	COUNT	11ac SIMO 80MHz packet counter.

0x3000094 TXCTL_TXB_SHORT_PKTS

Type: write-only

Counts number of TXB packets with short preamble transmitted.

TXCTL_TXB_SHORT_PKTS

Bits	Name	Description
15:0	COUNT	TXB short packet counter.

0x3000098 TXCTL_TXB_LONG_PKTS

Type: write-only

Counts number of TXB packets with long preamble transmitted.

TXCTL_TXB_LONG_PKTS

Bits	Name	Description
15:0	COUNT	TXB long packet counter.

0x300009C TXCTL_TXFIR_DONE

Type: write-only

Counts the number of packets completed at output of TXFIR.

TXCTL_TXFIR_DONE

Bits	Name	Description
15:0	COUNT	TXFIR done event counter

0x30000A0 TXCTL_MISSING_WARMUP

Type: write-only

Counts the number of packets that are initiated by TXP start pulse rather than the assertion of the TXP RF warmup flag.

TXCTL_MISSING_WARMUP

Bits	Name	Description
15:0	COUNT	Missing RF warmup flag event counter

0x30000A4 TXCTL_ALARMS

Type: read-only
Reset State: 0x0000

Monitor of all contributors to TXA abort

TXCTL_ALARMS

Bits	Name	Description
6:0	VALUE	Bit[0] = TXCTL watchdog timed out Bit[1] = Incorrect bandwidth field in command word Bit[2] = Invalid 11b packet parameters error Bit[3] = TX enable not asserted during active transmission Bit[4] = RF_WARMUP signal not asserted for sufficient length of time Bit[5] = Abort received from TACTL Bit[6] = Abort received from MPI Reset State: 0x0000

0x30000A8 TXCTL_RESET_ALARMS

Type: command
Reset State: 0x0000

Resets the alarm flags

TXCTL_RESET_ALARMS

Bits	Name	Description
0	RESET_ALARMS	When this register is written to with any value, a active high pulse is generated which will reset all alarm flags in the TACTL alarms register. Reset State: 0x0000

16.2.32 txfir

0x3000000 TXFIR_CFG

Type: read-write
Reset State: 0x003E

Sets the various modes for the Tx-FIR

TXFIR_CFG

Bits	Name	Description
5	PEAK_BYPASS_OVERRIDE_EN	When this field is set, dynamic bypass of the smart clipping logic will be disabled (low power) and the peak_bypass field will be used to either statically bypass or not bypass this logic Reset State: 0x0001
4	PEAK_BYPASS	When this field is set, the smart clipping logic is bypassed (as long as the peak_bypass_override_en field is also set) Reset State: 0x0001
3	DPD_BYPASS	When this field is set, the digital pre-distorter logic is bypassed Reset State: 0x0001
2	LOLEAKAGE_BYPASS	When this field is set, the LO leakage correction logic is bypassed Reset State: 0x0001
1	IQIMB_BYPASS	When this field is set, the IQ imbalance correction logic is bypassed Reset State: 0x0001
0	CHAIN0FIRBYPASS	When set bypasses the upsampling and filtering for chain 0 The output of the actual filter is 12-bits and hence drops the LSB of the inputs to present 9-bits at the output Reset State: 0x0000

0x3000004 TXFIR_LOLEAKAGE_SHIFT

Type: read-write
Reset State: 0x0000

This register defines the number of left shifts applied to the LO leakage value derived from the gain-based look-up table in the TXFIR

TXFIR_LOLEAKAGE_SHIFT

Bits	Name	Description
1:0	CH0	Reset State: 0x0000

0x300000C TXFIR_COEFF_QUARTER_0

Type: read-write
Reset State: 0x0099

2's complement 10-bit OFDM quarter-band FIR coefficient 0

TXFIR_COEFF_QUARTER_0

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0099

0x3000010 TXFIR_COEFF_QUARTER_1

Type: read-write
Reset State: 0x006D

2's complement 10-bit OFDM quarter-band FIR coefficient 1

TXFIR_COEFF_QUARTER_1

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x006D

0x3000014 TXFIR_COEFF_QUARTER_2

Type: read-write
Reset State: 0x0099

2's complement 10-bit OFDM quarter-band FIR coefficient 2

TXFIR_COEFF_QUARTER_2

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0099

0x3000018 TXFIR_COEFF_QUARTER_3

Type: read-write
Reset State: 0x03A9

2's complement 10-bit OFDM quarter-band FIR coefficient 3

TXFIR_COEFF_QUARTER_3

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03A9

0x300001C TXFIR_COEFF_QUARTER_4

Type: read-write
Reset State: 0x0035

2's complement 10-bit OFDM quarter-band FIR coefficient 4

TXFIR_COEFF_QUARTER_4

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0035

0x3000020 TXFIR_COEFF_QUARTER_5

Type: read-write
Reset State: 0x002C

2's complement 10-bit OFDM quarter-band FIR coefficient 5

TXFIR_COEFF_QUARTER_5

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x002C

0x3000024 TXFIR_COEFF_QUARTER_6

Type: read-write
Reset State: 0x007D

2's complement 10-bit OFDM quarter-band FIR coefficient 6

TXFIR_COEFF_QUARTER_6

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x007D

0x3000028 TXFIR_COEFF_QUARTER_7

Type: read-write
Reset State: 0x0050

2's complement 10-bit OFDM quarter-band FIR coefficient 7

TXFIR_COEFF_QUARTER_7

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0050

0x300002C TXFIR_COEFF_QUARTER_8

Type: read-write
Reset State: 0x0047

2's complement 10-bit OFDM quarter-band FIR coefficient 8

TXFIR_COEFF_QUARTER_8

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0047

0x3000030 TXFIR_COEFF_QUARTER_9

Type: read-write
Reset State: 0x006F

2's complement 10-bit OFDM quarter-band FIR coefficient 9

TXFIR_COEFF_QUARTER_9

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x006F

0x3000034 TXFIR_COEFF_QUARTER_10

Type: read-write
Reset State: 0x0051

2's complement 10-bit OFDM quarter-band FIR coefficient 10

TXFIR_COEFF_QUARTER_10

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0051

0x3000038 TXFIR_COEFF_QUARTER_11

Type: read-write
Reset State: 0x004C

2's complement 10-bit OFDM quarter-band FIR coefficient 11

TXFIR_COEFF_QUARTER_11

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x004C

0x300003C TXFIR_COEFF_QUARTER_12

Type: read-write
Reset State: 0x0057

2's complement 10-bit OFDM quarter-band FIR coefficient 12

TXFIR_COEFF_QUARTER_12

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0057

0x3000040 TXFIR_COEFF_QUARTER_13

Type: read-write
Reset State: 0x004A

2's complement 10-bit OFDM quarter-band FIR coefficient 13

TXFIR_COEFF_QUARTER_13

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x004A

0x3000044 TXFIR_COEFF_QUARTER_14

Type: read-write
Reset State: 0x0047

2's complement 10-bit OFDM quarter-band FIR coefficient 14

TXFIR_COEFF_QUARTER_14

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0047

0x3000048 TXFIR_COEFF_QUARTER_15

Type: read-write
Reset State: 0x0041

2's complement 10-bit OFDM quarter-band FIR coefficient 15

TXFIR_COEFF_QUARTER_15

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0041

0x300004C TXFIR_COEFF_QUARTER_16

Type: read-write
Reset State: 0x003E

2's complement 10-bit OFDM quarter-band FIR coefficient 16

TXFIR_COEFF_QUARTER_16

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x003E

0x3000050 TXFIR_COEFF_QUARTER_17

Type: read-write
Reset State: 0x003C

2's complement 10-bit OFDM quarter-band FIR coefficient 17

TXFIR_COEFF_QUARTER_17

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x003C

0x3000054 TXFIR_COEFF_QUARTER_18

Type: read-write
Reset State: 0x002D

2's complement 10-bit OFDM quarter-band FIR coefficient 18

TXFIR_COEFF_QUARTER_18

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x002D

0x3000058 TXFIR_COEFF_QUARTER_19

Type: read-write
Reset State: 0x002D

2's complement 10-bit OFDM quarter-band FIR coefficient 19

TXFIR_COEFF_QUARTER_19

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x002D

0x300005C TXFIR_COEFF_QUARTER_20

Type: read-write
Reset State: 0x0027

2's complement 10-bit OFDM quarter-band FIR coefficient 20

TXFIR_COEFF_QUARTER_20

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0027

0x3000060 TXFIR_COEFF_QUARTER_21

Type: read-write
Reset State: 0x0017

2's complement 10-bit OFDM quarter-band FIR coefficient 21

TXFIR_COEFF_QUARTER_21

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0017

0x3000064 TXFIR_COEFF_QUARTER_22

Type: read-write
Reset State: 0x0014

2's complement 10-bit OFDM quarter-band FIR coefficient 22

TXFIR_COEFF_QUARTER_22

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0014

0x3000068 TXFIR_COEFF_QUARTER_23

Type: read-write
Reset State: 0x000C

2's complement 10-bit OFDM quarter-band FIR coefficient 23

TXFIR_COEFF_QUARTER_23

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x000C

0x300006C TXFIR_COEFF_QUARTER_24

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 24

TXFIR_COEFF_QUARTER_24

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000070 TXFIR_COEFF_QUARTER_25

Type: read-write
Reset State: 0x03FC

2's complement 10-bit OFDM quarter-band FIR coefficient 25

TXFIR_COEFF_QUARTER_25

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03FC

0x3000074 TXFIR_COEFF_QUARTER_26

Type: read-write
Reset State: 0x03F9

2's complement 10-bit OFDM quarter-band FIR coefficient 26

TXFIR_COEFF_QUARTER_26

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03F9

0x3000078 TXFIR_COEFF_QUARTER_27

Type: read-write
Reset State: 0x03F8

2's complement 10-bit OFDM quarter-band FIR coefficient 27

TXFIR_COEFF_QUARTER_27

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03F8

0x300007C TXFIR_COEFF_QUARTER_28

Type: read-write
Reset State: 0x03F7

2's complement 10-bit OFDM quarter-band FIR coefficient 28

TXFIR_COEFF_QUARTER_28

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03F7

0x3000080 TXFIR_COEFF_QUARTER_29

Type: read-write
Reset State: 0x03F8

2's complement 10-bit OFDM quarter-band FIR coefficient 29

TXFIR_COEFF_QUARTER_29

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03F8

0x3000084 TXFIR_COEFF_QUARTER_30

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 30

TXFIR_COEFF_QUARTER_30

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000088 TXFIR_COEFF_QUARTER_31

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 31

TXFIR_COEFF_QUARTER_31

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x300008C TXFIR_COEFF_QUARTER_32

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 32

TXFIR_COEFF_QUARTER_32

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000090 TXFIR_COEFF_QUARTER_33

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 33

TXFIR_COEFF_QUARTER_33

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000094 TXFIR_COEFF_QUARTER_34

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 34

TXFIR_COEFF_QUARTER_34

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000098 TXFIR_COEFF_QUARTER_35

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 35

TXFIR_COEFF_QUARTER_35

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x300009C TXFIR_COEFF_QUARTER_36

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 36

TXFIR_COEFF_QUARTER_36

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30000A0 TXFIR_COEFF_QUARTER_37

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 37

TXFIR_COEFF_QUARTER_37

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30000A4 TXFIR_COEFF_QUARTER_38

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 38

TXFIR_COEFF_QUARTER_38

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30000A8 TXFIR_COEFF_QUARTER_39

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 39

TXFIR_COEFF_QUARTER_39

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30000AC TXFIR_COEFF_QUARTER_40

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 40

TXFIR_COEFF_QUARTER_40

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30000B0 TXFIR_COEFF_QUARTER_41

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM quarter-band FIR coefficient 41

TXFIR_COEFF_QUARTER_41

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30000B4 TXFIR_COEFF_HALF_0

Type: read-write
Reset State: 0x003D

2's complement 10-bit OFDM half-band FIR coefficient 0

TXFIR_COEFF_HALF_0

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x003D

0x30000B8 TXFIR_COEFF_HALF_1

Type: read-write
Reset State: 0x0052

2's complement 10-bit OFDM half-band FIR coefficient 1

TXFIR_COEFF_HALF_1

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0052

0x30000BC TXFIR_COEFF_HALF_2

Type: read-write
Reset State: 0x009B

2's complement 10-bit OFDM half-band FIR coefficient 2

TXFIR_COEFF_HALF_2

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x009B

0x30000C0 TXFIR_COEFF_HALF_3

Type: read-write
Reset State: 0x005A

2's complement 10-bit OFDM half-band FIR coefficient 3

TXFIR_COEFF_HALF_3

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x005A

0x30000C4 TXFIR_COEFF_HALF_4

Type: read-write
Reset State: 0x0095

2's complement 10-bit OFDM half-band FIR coefficient 4

TXFIR_COEFF_HALF_4

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0095

0x30000C8 TXFIR_COEFF_HALF_5

Type: read-write
Reset State: 0x006B

2's complement 10-bit OFDM half-band FIR coefficient 5

TXFIR_COEFF_HALF_5

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x006B

0x30000CC TXFIR_COEFF_HALF_6

Type: read-write
Reset State: 0x00BF

2's complement 10-bit OFDM half-band FIR coefficient 6

TXFIR_COEFF_HALF_6

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x00BF

0x30000D0 TXFIR_COEFF_HALF_7

Type: read-write
Reset State: 0x0094

2's complement 10-bit OFDM half-band FIR coefficient 7

TXFIR_COEFF_HALF_7

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0094

0x30000D4 TXFIR_COEFF_HALF_8

Type: read-write
Reset State: 0x009B

2's complement 10-bit OFDM half-band FIR coefficient 8

TXFIR_COEFF_HALF_8

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x009B

0x30000D8 TXFIR_COEFF_HALF_9

Type: read-write
Reset State: 0x0085

2's complement 10-bit OFDM half-band FIR coefficient 9

TXFIR_COEFF_HALF_9

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0085

0x30000DC TXFIR_COEFF_HALF_10

Type: read-write
Reset State: 0x007A

2's complement 10-bit OFDM half-band FIR coefficient 10

TXFIR_COEFF_HALF_10

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x007A

0x30000E0 TXFIR_COEFF_HALF_11

Type: read-write
Reset State: 0x0071

2's complement 10-bit OFDM half-band FIR coefficient 11

TXFIR_COEFF_HALF_11

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0071

0x30000E4 TXFIR_COEFF_HALF_12

Type: read-write
Reset State: 0x0038

2's complement 10-bit OFDM half-band FIR coefficient 12

TXFIR_COEFF_HALF_12

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0038

0x30000E8 TXFIR_COEFF_HALF_13

Type: read-write
Reset State: 0x0027

2's complement 10-bit OFDM half-band FIR coefficient 13

TXFIR_COEFF_HALF_13

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0027

0x30000EC TXFIR_COEFF_HALF_14

Type: read-write
Reset State: 0x0025

2's complement 10-bit OFDM half-band FIR coefficient 14

TXFIR_COEFF_HALF_14

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0025

0x30000F0 TXFIR_COEFF_HALF_15

Type: read-write
Reset State: 0x001F

2's complement 10-bit OFDM half-band FIR coefficient 15

TXFIR_COEFF_HALF_15

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x001F

0x30000F4 TXFIR_COEFF_HALF_16

Type: read-write
Reset State: 0x000B

2's complement 10-bit OFDM half-band FIR coefficient 16

TXFIR_COEFF_HALF_16

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x000B

0x30000F8 TXFIR_COEFF_HALF_17

Type: read-write
Reset State: 0x03C9

2's complement 10-bit OFDM half-band FIR coefficient 17

TXFIR_COEFF_HALF_17

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03C9

0x30000FC TXFIR_COEFF_HALF_18

Type: read-write
Reset State: 0x03D0

2's complement 10-bit OFDM half-band FIR coefficient 18

TXFIR_COEFF_HALF_18

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03D0

0x3000100 TXFIR_COEFF_HALF_19

Type: read-write
Reset State: 0x03D8

2's complement 10-bit OFDM half-band FIR coefficient 19

TXFIR_COEFF_HALF_19

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03D8

0x3000104 TXFIR_COEFF_HALF_20

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 20

TXFIR_COEFF_HALF_20

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000108 TXFIR_COEFF_HALF_21

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 21

TXFIR_COEFF_HALF_21

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x300010C TXFIR_COEFF_HALF_22

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 22

TXFIR_COEFF_HALF_22

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000110 TXFIR_COEFF_HALF_23

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 23

TXFIR_COEFF_HALF_23

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000114 TXFIR_COEFF_HALF_24

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 24

TXFIR_COEFF_HALF_24

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000118 TXFIR_COEFF_HALF_25

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 25

TXFIR_COEFF_HALF_25

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x300011C TXFIR_COEFF_HALF_26

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 26

TXFIR_COEFF_HALF_26

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000120 TXFIR_COEFF_HALF_27

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 27

TXFIR_COEFF_HALF_27

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000124 TXFIR_COEFF_HALF_28

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 28

TXFIR_COEFF_HALF_28

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000128 TXFIR_COEFF_HALF_29

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 29

TXFIR_COEFF_HALF_29

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x300012C TXFIR_COEFF_HALF_30

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 30

TXFIR_COEFF_HALF_30

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000130 TXFIR_COEFF_HALF_31

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 31

TXFIR_COEFF_HALF_31

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000134 TXFIR_COEFF_HALF_32

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 32

TXFIR_COEFF_HALF_32

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000138 TXFIR_COEFF_HALF_33

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 33

TXFIR_COEFF_HALF_33

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x300013C TXFIR_COEFF_HALF_34

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 34

TXFIR_COEFF_HALF_34

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000140 TXFIR_COEFF_HALF_35

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 35

TXFIR_COEFF_HALF_35

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000144 TXFIR_COEFF_HALF_36

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 36

TXFIR_COEFF_HALF_36

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000148 TXFIR_COEFF_HALF_37

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 37

TXFIR_COEFF_HALF_37

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x300014C TXFIR_COEFF_HALF_38

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 38

TXFIR_COEFF_HALF_38

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000150 TXFIR_COEFF_HALF_39

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 39

TXFIR_COEFF_HALF_39

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000154 TXFIR_COEFF_HALF_40

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 40

TXFIR_COEFF_HALF_40

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000158 TXFIR_COEFF_HALF_41

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM half-band FIR coefficient 41

TXFIR_COEFF_HALF_41

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x300015C TXFIR_COEFF_FULL_0

Type: read-write
Reset State: 0x0030

2's complement 10-bit OFDM full-band FIR coefficient 0

TXFIR_COEFF_FULL_0

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0030

0x3000160 TXFIR_COEFF_FULL_1

Type: read-write
Reset State: 0x0072

2's complement 10-bit OFDM full-band FIR coefficient 1

TXFIR_COEFF_FULL_1

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0072

0x3000164 TXFIR_COEFF_FULL_2

Type: read-write
Reset State: 0x00E2

2's complement 10-bit OFDM full-band FIR coefficient 2

TXFIR_COEFF_FULL_2

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x00E2

0x3000168 TXFIR_COEFF_FULL_3

Type: read-write
Reset State: 0x0104

2's complement 10-bit OFDM full-band FIR coefficient 3

TXFIR_COEFF_FULL_3

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0104

0x300016C TXFIR_COEFF_FULL_4

Type: read-write
Reset State: 0x0126

2's complement 10-bit OFDM full-band FIR coefficient 4

TXFIR_COEFF_FULL_4

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0126

0x3000170 TXFIR_COEFF_FULL_5

Type: read-write
Reset State: 0x00EB

2's complement 10-bit OFDM full-band FIR coefficient 5

TXFIR_COEFF_FULL_5

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x00EB

0x3000174 TXFIR_COEFF_FULL_6

Type: read-write
Reset State: 0x00F4

2's complement 10-bit OFDM full-band FIR coefficient 6

TXFIR_COEFF_FULL_6

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x00F4

0x3000178 TXFIR_COEFF_FULL_7

Type: read-write
Reset State: 0x00A8

2's complement 10-bit OFDM full-band FIR coefficient 7

TXFIR_COEFF_FULL_7

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x00A8

0x300017C TXFIR_COEFF_FULL_8

Type: read-write
Reset State: 0x0086

2's complement 10-bit OFDM full-band FIR coefficient 8

TXFIR_COEFF_FULL_8

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0086

0x3000180 TXFIR_COEFF_FULL_9

Type: read-write
Reset State: 0x0004

2's complement 10-bit OFDM full-band FIR coefficient 9

TXFIR_COEFF_FULL_9

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0004

0x3000184 TXFIR_COEFF_FULL_10

Type: read-write
Reset State: 0x03D3

2's complement 10-bit OFDM full-band FIR coefficient 10

TXFIR_COEFF_FULL_10

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03D3

0x3000188 TXFIR_COEFF_FULL_11

Type: read-write
Reset State: 0x039A

2's complement 10-bit OFDM full-band FIR coefficient 11

TXFIR_COEFF_FULL_11

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x039A

0x300018C TXFIR_COEFF_FULL_12

Type: read-write
Reset State: 0x03B8

2's complement 10-bit OFDM full-band FIR coefficient 12

TXFIR_COEFF_FULL_12

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03B8

0x3000190 TXFIR_COEFF_FULL_13

Type: read-write
Reset State: 0x03C0

2's complement 10-bit OFDM full-band FIR coefficient 13

TXFIR_COEFF_FULL_13

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03C0

0x3000194 TXFIR_COEFF_FULL_14

Type: read-write
Reset State: 0x03E6

2's complement 10-bit OFDM full-band FIR coefficient 14

TXFIR_COEFF_FULL_14

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03E6

0x3000198 TXFIR_COEFF_FULL_15

Type: read-write
Reset State: 0x0002

2's complement 10-bit OFDM full-band FIR coefficient 15

TXFIR_COEFF_FULL_15

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0002

0x300019C TXFIR_COEFF_FULL_16

Type: read-write
Reset State: 0x0020

2's complement 10-bit OFDM full-band FIR coefficient 16

TXFIR_COEFF_FULL_16

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0020

0x30001A0 TXFIR_COEFF_FULL_17

Type: read-write
Reset State: 0x002B

2's complement 10-bit OFDM full-band FIR coefficient 17

TXFIR_COEFF_FULL_17

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x002B

0x30001A4 TXFIR_COEFF_FULL_18

Type: read-write
Reset State: 0x001C

2's complement 10-bit OFDM full-band FIR coefficient 18

TXFIR_COEFF_FULL_18

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x001C

0x30001A8 TXFIR_COEFF_FULL_19

Type: read-write
Reset State: 0x000B

2's complement 10-bit OFDM full-band FIR coefficient 19

TXFIR_COEFF_FULL_19

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x000B

0x30001AC TXFIR_COEFF_FULL_20

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 20

TXFIR_COEFF_FULL_20

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001B0 TXFIR_COEFF_FULL_21

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 21

TXFIR_COEFF_FULL_21

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001B4 TXFIR_COEFF_FULL_22

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 22

TXFIR_COEFF_FULL_22

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001B8 TXFIR_COEFF_FULL_23

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 23

TXFIR_COEFF_FULL_23

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001BC TXFIR_COEFF_FULL_24

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 24

TXFIR_COEFF_FULL_24

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001C0 TXFIR_COEFF_FULL_25

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 25

TXFIR_COEFF_FULL_25

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001C4 TXFIR_COEFF_FULL_26

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 26

TXFIR_COEFF_FULL_26

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001C8 TXFIR_COEFF_FULL_27

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 27

TXFIR_COEFF_FULL_27

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001CC TXFIR_COEFF_FULL_28

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 28

TXFIR_COEFF_FULL_28

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001D0 TXFIR_COEFF_FULL_29

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 29

TXFIR_COEFF_FULL_29

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001D4 TXFIR_COEFF_FULL_30

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 30

TXFIR_COEFF_FULL_30

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001D8 TXFIR_COEFF_FULL_31

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 31

TXFIR_COEFF_FULL_31

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001DC TXFIR_COEFF_FULL_32

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 32

TXFIR_COEFF_FULL_32

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001E0 TXFIR_COEFF_FULL_33

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 33

TXFIR_COEFF_FULL_33

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001E4 TXFIR_COEFF_FULL_34

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 34

TXFIR_COEFF_FULL_34

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001E8 TXFIR_COEFF_FULL_35

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 35

TXFIR_COEFF_FULL_35

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001EC TXFIR_COEFF_FULL_36

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 36

TXFIR_COEFF_FULL_36

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001F0 TXFIR_COEFF_FULL_37

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 37

TXFIR_COEFF_FULL_37

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001F4 TXFIR_COEFF_FULL_38

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 38

TXFIR_COEFF_FULL_38

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001F8 TXFIR_COEFF_FULL_39

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 39

TXFIR_COEFF_FULL_39

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30001FC TXFIR_COEFF_FULL_40

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 40

TXFIR_COEFF_FULL_40

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000200 TXFIR_COEFF_FULL_41

Type: read-write
Reset State: 0x0000

2's complement 10-bit OFDM full-band FIR coefficient 41

TXFIR_COEFF_FULL_41

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000204 TXFIR_COEFF_TXB_20_0

Type: read-write
Reset State: 0x0014

2's complement 10-bit Tx-B FIR20 coefficient 0

TXFIR_COEFF_TXB_20_0

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0014

0x3000208 TXFIR_COEFF_TXB_20_1

Type: read-write
Reset State: 0x003D

2's complement 10-bit Tx-B FIR20 coefficient 1

TXFIR_COEFF_TXB_20_1

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x003D

0x300020C TXFIR_COEFF_TXB_20_2

Type: read-write
Reset State: 0x007A

2's complement 10-bit Tx-B FIR20 coefficient 2

TXFIR_COEFF_TXB_20_2

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x007A

0x3000210 TXFIR_COEFF_TXB_20_3

Type: read-write
Reset State: 0x00C2

2's complement 10-bit Tx-B FIR20 coefficient 3

TXFIR_COEFF_TXB_20_3

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x00C2

0x3000214 TXFIR_COEFF_TXB_20_4

Type: read-write
Reset State: 0x00FD

2's complement 10-bit Tx-B FIR20 coefficient 4

TXFIR_COEFF_TXB_20_4

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x00FD

0x3000218 TXFIR_COEFF_TXB_20_5

Type: read-write
Reset State: 0x0114

2's complement 10-bit Tx-B FIR20 coefficient 5

TXFIR_COEFF_TXB_20_5

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0114

0x300021C TXFIR_COEFF_TXB_20_6

Type: read-write
Reset State: 0x00FD

2's complement 10-bit Tx-B FIR20 coefficient 6

TXFIR_COEFF_TXB_20_6

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x00FD

0x3000220 TXFIR_COEFF_TXB_20_7

Type: read-write
Reset State: 0x00BF

2's complement 10-bit Tx-B FIR20 coefficient 7

TXFIR_COEFF_TXB_20_7

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x00BF

0x3000224 TXFIR_COEFF_TXB_20_8

Type: read-write
Reset State: 0x0072

2's complement 10-bit Tx-B FIR20 coefficient 8

TXFIR_COEFF_TXB_20_8

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0072

0x3000228 TXFIR_COEFF_TXB_20_9

Type: read-write
Reset State: 0x0030

2's complement 10-bit Tx-B FIR20 coefficient 9

TXFIR_COEFF_TXB_20_9

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0030

0x300022C TXFIR_COEFF_TXB_20_10

Type: read-write
Reset State: 0x000A

2's complement 10-bit Tx-B FIR20 coefficient 10

TXFIR_COEFF_TXB_20_10

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x000A

0x3000230 TXFIR_COEFF_TXB_20_11

Type: read-write
Reset State: 0x03FA

2's complement 10-bit Tx-B FIR20 coefficient 11

TXFIR_COEFF_TXB_20_11

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03FA

0x3000234 TXFIR_COEFF_TXB_20_12

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR20 coefficient 12

TXFIR_COEFF_TXB_20_12

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000238 TXFIR_COEFF_TXB_20_13

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR20 coefficient 13

TXFIR_COEFF_TXB_20_13

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x300023C TXFIR_COEFF_TXB_20_14

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR20 coefficient 14

TXFIR_COEFF_TXB_20_14

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000240 TXFIR_COEFF_TXB_20_15

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR20 coefficient 15

TXFIR_COEFF_TXB_20_15

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000244 TXFIR_COEFF_TXB_40_0

Type: read-write
Reset State: 0x0008

2's complement 10-bit Tx-B FIR40 coefficient 0

TXFIR_COEFF_TXB_40_0

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0008

0x3000248 TXFIR_COEFF_TXB_40_1

Type: read-write
Reset State: 0x000E

2's complement 10-bit Tx-B FIR40 coefficient 1

TXFIR_COEFF_TXB_40_1

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x000E

0x300024C TXFIR_COEFF_TXB_40_2

Type: read-write
Reset State: 0x0018

2's complement 10-bit Tx-B FIR40 coefficient 2

TXFIR_COEFF_TXB_40_2

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0018

0x3000250 TXFIR_COEFF_TXB_40_3

Type: read-write
Reset State: 0x0025

2's complement 10-bit Tx-B FIR40 coefficient 3

TXFIR_COEFF_TXB_40_3

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0025

0x3000254 TXFIR_COEFF_TXB_40_4

Type: read-write
Reset State: 0x0035

2's complement 10-bit Tx-B FIR40 coefficient 4

TXFIR_COEFF_TXB_40_4

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0035

0x3000258 TXFIR_COEFF_TXB_40_5

Type: read-write
Reset State: 0x0046

2's complement 10-bit Tx-B FIR40 coefficient 5

TXFIR_COEFF_TXB_40_5

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0046

0x300025C TXFIR_COEFF_TXB_40_6

Type: read-write
Reset State: 0x0058

2's complement 10-bit Tx-B FIR40 coefficient 6

TXFIR_COEFF_TXB_40_6

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0058

0x3000260 TXFIR_COEFF_TXB_40_7

Type: read-write
Reset State: 0x0069

2's complement 10-bit Tx-B FIR40 coefficient 7

TXFIR_COEFF_TXB_40_7

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0069

0x3000264 TXFIR_COEFF_TXB_40_8

Type: read-write
Reset State: 0x0078

2's complement 10-bit Tx-B FIR40 coefficient 8

TXFIR_COEFF_TXB_40_8

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0078

0x3000268 TXFIR_COEFF_TXB_40_9

Type: read-write
Reset State: 0x0083

2's complement 10-bit Tx-B FIR40 coefficient 9

TXFIR_COEFF_TXB_40_9

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0083

0x300026C TXFIR_COEFF_TXB_40_10

Type: read-write
Reset State: 0x0089

2's complement 10-bit Tx-B FIR40 coefficient 10

TXFIR_COEFF_TXB_40_10

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0089

0x3000270 TXFIR_COEFF_TXB_40_11

Type: read-write
Reset State: 0x0089

2's complement 10-bit Tx-B FIR40 coefficient 11

TXFIR_COEFF_TXB_40_11

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0089

0x3000274 TXFIR_COEFF_TXB_40_12

Type: read-write
Reset State: 0x0083

2's complement 10-bit Tx-B FIR40 coefficient 12

TXFIR_COEFF_TXB_40_12

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0083

0x3000278 TXFIR_COEFF_TXB_40_13

Type: read-write
Reset State: 0x0078

2's complement 10-bit Tx-B FIR40 coefficient 13

TXFIR_COEFF_TXB_40_13

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0078

0x300027C TXFIR_COEFF_TXB_40_14

Type: read-write
Reset State: 0x0069

2's complement 10-bit Tx-B FIR40 coefficient 14

TXFIR_COEFF_TXB_40_14

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0069

0x3000280 TXFIR_COEFF_TXB_40_15

Type: read-write
Reset State: 0x0056

2's complement 10-bit Tx-B FIR40 coefficient 15

TXFIR_COEFF_TXB_40_15

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0056

0x3000284 TXFIR_COEFF_TXB_40_16

Type: read-write
Reset State: 0x0043

2's complement 10-bit Tx-B FIR40 coefficient 16

TXFIR_COEFF_TXB_40_16

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0043

0x3000288 TXFIR_COEFF_TXB_40_17

Type: read-write
Reset State: 0x0030

2's complement 10-bit Tx-B FIR40 coefficient 17

TXFIR_COEFF_TXB_40_17

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0030

0x300028C TXFIR_COEFF_TXB_40_18

Type: read-write
Reset State: 0x001F

2's complement 10-bit Tx-B FIR40 coefficient 18

TXFIR_COEFF_TXB_40_18

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x001F

0x3000290 TXFIR_COEFF_TXB_40_19

Type: read-write
Reset State: 0x0012

2's complement 10-bit Tx-B FIR40 coefficient 19

TXFIR_COEFF_TXB_40_19

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0012

0x3000294 TXFIR_COEFF_TXB_40_20

Type: read-write
Reset State: 0x0008

2's complement 10-bit Tx-B FIR40 coefficient 20

TXFIR_COEFF_TXB_40_20

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0008

0x3000298 TXFIR_COEFF_TXB_40_21

Type: read-write
Reset State: 0x0002

2's complement 10-bit Tx-B FIR40 coefficient 21

TXFIR_COEFF_TXB_40_21

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0002

0x300029C TXFIR_COEFF_TXB_40_22

Type: read-write
Reset State: 0x03FF

2's complement 10-bit Tx-B FIR40 coefficient 22

TXFIR_COEFF_TXB_40_22

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03FF

0x30002A0 TXFIR_COEFF_TXB_40_23

Type: read-write
Reset State: 0x03FB

2's complement 10-bit Tx-B FIR40 coefficient 23

TXFIR_COEFF_TXB_40_23

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03FB

0x30002A4 TXFIR_COEFF_TXB_40_24

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR40 coefficient 24

TXFIR_COEFF_TXB_40_24

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30002A8 TXFIR_COEFF_TXB_40_25

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR40 coefficient 25

TXFIR_COEFF_TXB_40_25

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30002AC TXFIR_COEFF_TXB_40_26

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR40 coefficient 26

TXFIR_COEFF_TXB_40_26

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30002B0 TXFIR_COEFF_TXB_40_27

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR40 coefficient 27

TXFIR_COEFF_TXB_40_27

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30002B4 TXFIR_COEFF_TXB_40_28

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR40 coefficient 28

TXFIR_COEFF_TXB_40_28

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30002B8 TXFIR_COEFF_TXB_40_29

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR40 coefficient 29

TXFIR_COEFF_TXB_40_29

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30002BC TXFIR_COEFF_TXB_40_30

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR40 coefficient 30

TXFIR_COEFF_TXB_40_30

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30002C0 TXFIR_COEFF_TXB_40_31

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR40 coefficient 31

TXFIR_COEFF_TXB_40_31

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30002C4 TXFIR_COEFF_TXB_80_0

Type: read-write
Reset State: 0x0005

2's complement 10-bit Tx-B FIR80 coefficient 0

TXFIR_COEFF_TXB_80_0

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0005

0x30002C8 TXFIR_COEFF_TXB_80_1

Type: read-write
Reset State: 0x0005

2's complement 10-bit Tx-B FIR80 coefficient 1

TXFIR_COEFF_TXB_80_1

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0005

0x30002CC TXFIR_COEFF_TXB_80_2

Type: read-write
Reset State: 0x0006

2's complement 10-bit Tx-B FIR80 coefficient 2

TXFIR_COEFF_TXB_80_2

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0006

0x30002D0 TXFIR_COEFF_TXB_80_3

Type: read-write
Reset State: 0x0009

2's complement 10-bit Tx-B FIR80 coefficient 3

TXFIR_COEFF_TXB_80_3

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0009

0x30002D4 TXFIR_COEFF_TXB_80_4

Type: read-write
Reset State: 0x000B

2's complement 10-bit Tx-B FIR80 coefficient 4

TXFIR_COEFF_TXB_80_4

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x000B

0x30002D8 TXFIR_COEFF_TXB_80_5

Type: read-write
Reset State: 0x000E

2's complement 10-bit Tx-B FIR80 coefficient 5

TXFIR_COEFF_TXB_80_5

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x000E

0x30002DC TXFIR_COEFF_TXB_80_6

Type: read-write
Reset State: 0x0012

2's complement 10-bit Tx-B FIR80 coefficient 6

TXFIR_COEFF_TXB_80_6

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0012

0x30002E0 TXFIR_COEFF_TXB_80_7

Type: read-write
Reset State: 0x0016

2's complement 10-bit Tx-B FIR80 coefficient 7

TXFIR_COEFF_TXB_80_7

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0016

0x30002E4 TXFIR_COEFF_TXB_80_8

Type: read-write
Reset State: 0x0019

2's complement 10-bit Tx-B FIR80 coefficient 8

TXFIR_COEFF_TXB_80_8

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0019

0x30002E8 TXFIR_COEFF_TXB_80_9

Type: read-write
Reset State: 0x001E

2's complement 10-bit Tx-B FIR80 coefficient 9

TXFIR_COEFF_TXB_80_9

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x001E

0x30002EC TXFIR_COEFF_TXB_80_10

Type: read-write
Reset State: 0x0022

2's complement 10-bit Tx-B FIR80 coefficient 10

TXFIR_COEFF_TXB_80_10

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0022

0x30002F0 TXFIR_COEFF_TXB_80_11

Type: read-write
Reset State: 0x0027

2's complement 10-bit Tx-B FIR80 coefficient 11

TXFIR_COEFF_TXB_80_11

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0027

0x30002F4 TXFIR_COEFF_TXB_80_12

Type: read-write
Reset State: 0x002B

2's complement 10-bit Tx-B FIR80 coefficient 12

TXFIR_COEFF_TXB_80_12

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x002B

0x30002F8 TXFIR_COEFF_TXB_80_13

Type: read-write
Reset State: 0x002F

2's complement 10-bit Tx-B FIR80 coefficient 13

TXFIR_COEFF_TXB_80_13

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x002F

0x30002FC TXFIR_COEFF_TXB_80_14

Type: read-write
Reset State: 0x0034

2's complement 10-bit Tx-B FIR80 coefficient 14

TXFIR_COEFF_TXB_80_14

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0034

0x3000300 TXFIR_COEFF_TXB_80_15

Type: read-write
Reset State: 0x0038

2's complement 10-bit Tx-B FIR80 coefficient 15

TXFIR_COEFF_TXB_80_15

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0038

0x3000304 TXFIR_COEFF_TXB_80_16

Type: read-write
Reset State: 0x003B

2's complement 10-bit Tx-B FIR80 coefficient 16

TXFIR_COEFF_TXB_80_16

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x003B

0x3000308 TXFIR_COEFF_TXB_80_17

Type: read-write
Reset State: 0x003E

2's complement 10-bit Tx-B FIR80 coefficient 17

TXFIR_COEFF_TXB_80_17

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x003E

0x300030C TXFIR_COEFF_TXB_80_18

Type: read-write
Reset State: 0x0041

2's complement 10-bit Tx-B FIR80 coefficient 18

TXFIR_COEFF_TXB_80_18

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0041

0x3000310 TXFIR_COEFF_TXB_80_19

Type: read-write
Reset State: 0x0043

2's complement 10-bit Tx-B FIR80 coefficient 19

TXFIR_COEFF_TXB_80_19

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0043

0x3000314 TXFIR_COEFF_TXB_80_20

Type: read-write
Reset State: 0x0044

2's complement 10-bit Tx-B FIR80 coefficient 20

TXFIR_COEFF_TXB_80_20

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0044

0x3000318 TXFIR_COEFF_TXB_80_21

Type: read-write
Reset State: 0x0045

2's complement 10-bit Tx-B FIR80 coefficient 21

TXFIR_COEFF_TXB_80_21

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0045

0x300031C TXFIR_COEFF_TXB_80_22

Type: read-write
Reset State: 0x0045

2's complement 10-bit Tx-B FIR80 coefficient 22

TXFIR_COEFF_TXB_80_22

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0045

0x3000320 TXFIR_COEFF_TXB_80_23

Type: read-write
Reset State: 0x0044

2's complement 10-bit Tx-B FIR80 coefficient 23

TXFIR_COEFF_TXB_80_23

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0044

0x3000324 TXFIR_COEFF_TXB_80_24

Type: read-write
Reset State: 0x0042

2's complement 10-bit Tx-B FIR80 coefficient 24

TXFIR_COEFF_TXB_80_24

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0042

0x3000328 TXFIR_COEFF_TXB_80_25

Type: read-write
Reset State: 0x0040

2's complement 10-bit Tx-B FIR80 coefficient 25

TXFIR_COEFF_TXB_80_25

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0040

0x300032C TXFIR_COEFF_TXB_80_26

Type: read-write
Reset State: 0x003D

2's complement 10-bit Tx-B FIR80 coefficient 26

TXFIR_COEFF_TXB_80_26

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x003D

0x3000330 TXFIR_COEFF_TXB_80_27

Type: read-write
Reset State: 0x0039

2's complement 10-bit Tx-B FIR80 coefficient 27

TXFIR_COEFF_TXB_80_27

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0039

0x3000334 TXFIR_COEFF_TXB_80_28

Type: read-write
Reset State: 0x0035

2's complement 10-bit Tx-B FIR80 coefficient 28

TXFIR_COEFF_TXB_80_28

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0035

0x3000338 TXFIR_COEFF_TXB_80_29

Type: read-write
Reset State: 0x0031

2's complement 10-bit Tx-B FIR80 coefficient 29

TXFIR_COEFF_TXB_80_29

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0031

0x300033C TXFIR_COEFF_TXB_80_30

Type: read-write
Reset State: 0x002C

2's complement 10-bit Tx-B FIR80 coefficient 30

TXFIR_COEFF_TXB_80_30

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x002C

0x3000340 TXFIR_COEFF_TXB_80_31

Type: read-write
Reset State: 0x0027

2's complement 10-bit Tx-B FIR80 coefficient 31

TXFIR_COEFF_TXB_80_31

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0027

0x3000344 TXFIR_COEFF_TXB_80_32

Type: read-write
Reset State: 0x0023

2's complement 10-bit Tx-B FIR80 coefficient 32

TXFIR_COEFF_TXB_80_32

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0023

0x3000348 TXFIR_COEFF_TXB_80_33

Type: read-write
Reset State: 0x001E

2's complement 10-bit Tx-B FIR80 coefficient 33

TXFIR_COEFF_TXB_80_33

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x001E

0x300034C TXFIR_COEFF_TXB_80_34

Type: read-write
Reset State: 0x0019

2's complement 10-bit Tx-B FIR80 coefficient 34

TXFIR_COEFF_TXB_80_34

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0019

0x3000350 TXFIR_COEFF_TXB_80_35

Type: read-write
Reset State: 0x0015

2's complement 10-bit Tx-B FIR80 coefficient 35

TXFIR_COEFF_TXB_80_35

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0015

0x3000354 TXFIR_COEFF_TXB_80_36

Type: read-write
Reset State: 0x0011

2's complement 10-bit Tx-B FIR80 coefficient 36

TXFIR_COEFF_TXB_80_36

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0011

0x3000358 TXFIR_COEFF_TXB_80_37

Type: read-write
Reset State: 0x000D

2's complement 10-bit Tx-B FIR80 coefficient 37

TXFIR_COEFF_TXB_80_37

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x000D

0x300035C TXFIR_COEFF_TXB_80_38

Type: read-write
Reset State: 0x000A

2's complement 10-bit Tx-B FIR80 coefficient 38

TXFIR_COEFF_TXB_80_38

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x000A

0x3000360 TXFIR_COEFF_TXB_80_39

Type: read-write
Reset State: 0x0007

2's complement 10-bit Tx-B FIR80 coefficient 39

TXFIR_COEFF_TXB_80_39

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0007

0x3000364 TXFIR_COEFF_TXB_80_40

Type: read-write
Reset State: 0x0005

2's complement 10-bit Tx-B FIR80 coefficient 40

TXFIR_COEFF_TXB_80_40

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0005

0x3000368 TXFIR_COEFF_TXB_80_41

Type: read-write
Reset State: 0x0003

2's complement 10-bit Tx-B FIR80 coefficient 41

TXFIR_COEFF_TXB_80_41

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0003

0x300036C TXFIR_COEFF_TXB_80_42

Type: read-write
Reset State: 0x0001

2's complement 10-bit Tx-B FIR80 coefficient 42

TXFIR_COEFF_TXB_80_42

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0001

0x3000370 TXFIR_COEFF_TXB_80_43

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 43

TXFIR_COEFF_TXB_80_43

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000374 TXFIR_COEFF_TXB_80_44

Type: read-write
Reset State: 0x03FF

2's complement 10-bit Tx-B FIR80 coefficient 44

TXFIR_COEFF_TXB_80_44

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03FF

0x3000378 TXFIR_COEFF_TXB_80_45

Type: read-write
Reset State: 0x03FF

2's complement 10-bit Tx-B FIR80 coefficient 45

TXFIR_COEFF_TXB_80_45

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03FF

0x300037C TXFIR_COEFF_TXB_80_46

Type: read-write
Reset State: 0x03FF

2's complement 10-bit Tx-B FIR80 coefficient 46

TXFIR_COEFF_TXB_80_46

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03FF

0x3000380 TXFIR_COEFF_TXB_80_47

Type: read-write
Reset State: 0x03FC

2's complement 10-bit Tx-B FIR80 coefficient 47

TXFIR_COEFF_TXB_80_47

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x03FC

0x3000384 TXFIR_COEFF_TXB_80_48

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 48

TXFIR_COEFF_TXB_80_48

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000388 TXFIR_COEFF_TXB_80_49

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 49

TXFIR_COEFF_TXB_80_49

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x300038C TXFIR_COEFF_TXB_80_50

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 50

TXFIR_COEFF_TXB_80_50

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000390 TXFIR_COEFF_TXB_80_51

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 51

TXFIR_COEFF_TXB_80_51

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000394 TXFIR_COEFF_TXB_80_52

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 52

TXFIR_COEFF_TXB_80_52

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x3000398 TXFIR_COEFF_TXB_80_53

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 53

TXFIR_COEFF_TXB_80_53

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x300039C TXFIR_COEFF_TXB_80_54

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 54

TXFIR_COEFF_TXB_80_54

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30003A0 TXFIR_COEFF_TXB_80_55

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 55

TXFIR_COEFF_TXB_80_55

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30003A4 TXFIR_COEFF_TXB_80_56

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 56

TXFIR_COEFF_TXB_80_56

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30003A8 TXFIR_COEFF_TXB_80_57

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 57

TXFIR_COEFF_TXB_80_57

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30003AC TXFIR_COEFF_TXB_80_58

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 58

TXFIR_COEFF_TXB_80_58

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30003B0 TXFIR_COEFF_TXB_80_59

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 59

TXFIR_COEFF_TXB_80_59

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30003B4 TXFIR_COEFF_TXB_80_60

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 60

TXFIR_COEFF_TXB_80_60

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30003B8 TXFIR_COEFF_TXB_80_61

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 61

TXFIR_COEFF_TXB_80_61

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30003BC TXFIR_COEFF_TXB_80_62

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 62

TXFIR_COEFF_TXB_80_62

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30003C0 TXFIR_COEFF_TXB_80_63

Type: read-write
Reset State: 0x0000

2's complement 10-bit Tx-B FIR80 coefficient 63

TXFIR_COEFF_TXB_80_63

Bits	Name	Description
9:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30003C4 TXFIR_COEFF_PEAKW_0

Type: read-write
Reset State: 0x01FE

2's complement 9-bit peak windowing FIR coefficient 0

TXFIR_COEFF_PEAKW_0

Bits	Name	Description
8:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x01FE

0x30003C8 TXFIR_COEFF_PEAKW_1

Type: read-write
Reset State: 0x01FF

2's complement 9-bit peak windowing FIR coefficient 1

TXFIR_COEFF_PEAKW_1

Bits	Name	Description
8:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x01FF

0x30003CC TXFIR_COEFF_PEAKW_2

Type: read-write
Reset State: 0x0000

2's complement 9-bit peak windowing FIR coefficient 2

TXFIR_COEFF_PEAKW_2

Bits	Name	Description
8:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0000

0x30003D0 TXFIR_COEFF_PEAKW_3

Type: read-write
Reset State: 0x0003

2's complement 9-bit peak windowing FIR coefficient 3

TXFIR_COEFF_PEAKW_3

Bits	Name	Description
8:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0003

0x30003D4 TXFIR_COEFF_PEAKW_4

Type: read-write
Reset State: 0x0006

2's complement 9-bit peak windowing FIR coefficient 4

TXFIR_COEFF_PEAKW_4

Bits	Name	Description
8:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0006

0x30003D8 TXFIR_COEFF_PEAKW_5

Type: read-write
Reset State: 0x000B

2's complement 9-bit peak windowing FIR coefficient 5

TXFIR_COEFF_PEAKW_5

Bits	Name	Description
8:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x000B

0x30003DC TXFIR_COEFF_PEAKW_6

Type: read-write
Reset State: 0x0010

2's complement 9-bit peak windowing FIR coefficient 6

TXFIR_COEFF_PEAKW_6

Bits	Name	Description
8:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0010

0x30003E0 TXFIR_COEFF_PEAKW_7

Type: read-write
Reset State: 0x0016

2's complement 9-bit peak windowing FIR coefficient 7

TXFIR_COEFF_PEAKW_7

Bits	Name	Description
8:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x0016

0x30003E4 TXFIR_COEFF_PEAKW_8

Type: read-write
Reset State: 0x001A

2's complement 9-bit peak windowing FIR coefficient 8

TXFIR_COEFF_PEAKW_8

Bits	Name	Description
8:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x001A

0x30003E8 TXFIR_COEFF_PEAKW_9

Type: read-write
Reset State: 0x001D

2's complement 9-bit peak windowing FIR coefficient 9

TXFIR_COEFF_PEAKW_9

Bits	Name	Description
8:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x001D

0x30003EC TXFIR_COEFF_PEAKW_10

Type: read-write
Reset State: 0x001E

2's complement 9-bit peak windowing FIR coefficient 10

TXFIR_COEFF_PEAKW_10

Bits	Name	Description
8:0	COEFFVAL	2's complement scaled, quantized coefficient Reset State: 0x001E

0x30003F0 TXFIR_PEAKW_CLIP_THRESHOLD_0

Type: read-write
Reset State: 0x0016

8-bit peak windowing clip threshold for power index 0

TXFIR_PEAKW_CLIP_THRESHOLD_0

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 0 Reset State: 0x0016

0x30003F4 TXFIR_PEAKW_CLIP_THRESHOLD_1

Type: read-write
Reset State: 0x0014

8-bit peak windowing clip threshold for power index 1

TXFIR_PEAKW_CLIP_THRESHOLD_1

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 1 Reset State: 0x0014

0x30003F8 TXFIR_PEAKW_CLIP_THRESHOLD_2

Type: read-write
Reset State: 0x0011

8-bit peak windowing clip threshold for power index 2

TXFIR_PEAKW_CLIP_THRESHOLD_2

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 2 Reset State: 0x0011

0x30003FC TXFIR_PEAKW_CLIP_THRESHOLD_3

Type: read-write
Reset State: 0x0010

8-bit peak windowing clip threshold for power index 3

TXFIR_PEAKW_CLIP_THRESHOLD_3

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 3 Reset State: 0x0010

0x3000400 TXFIR_PEAKW_CLIP_THRESHOLD_4

Type: read-write
Reset State: 0x000E

8-bit peak windowing clip threshold for power index 4

TXFIR_PEAKW_CLIP_THRESHOLD_4

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 4 Reset State: 0x000E

0x3000404 TXFIR_PEAKW_CLIP_THRESHOLD_5

Type: read-write
Reset State: 0x000C

8-bit peak windowing clip threshold for power index 5

TXFIR_PEAKW_CLIP_THRESHOLD_5

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 5 Reset State: 0x000C

0x3000408 TXFIR_PEAKW_CLIP_THRESHOLD_6

Type: read-write
Reset State: 0x000B

8-bit peak windowing clip threshold for power index 6

TXFIR_PEAKW_CLIP_THRESHOLD_6

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 6 Reset State: 0x000B

0x300040C TXFIR_PEAKW_CLIP_THRESHOLD_7

Type: read-write
Reset State: 0x000A

8-bit peak windowing clip threshold for power index 7

TXFIR_PEAKW_CLIP_THRESHOLD_7

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 7 Reset State: 0x000A

0x3000410 TXFIR_PEAKW_CLIP_THRESHOLD_8

Type: read-write
Reset State: 0x0008

8-bit peak windowing clip threshold for power index 8

TXFIR_PEAKW_CLIP_THRESHOLD_8

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 8 Reset State: 0x0008

0x3000414 TXFIR_PEAKW_CLIP_THRESHOLD_9

Type: read-write
Reset State: 0x0008

8-bit peak windowing clip threshold for power index 9

TXFIR_PEAKW_CLIP_THRESHOLD_9

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 9 Reset State: 0x0008

0x3000418 TXFIR_PEAKW_CLIP_THRESHOLD_10

Type: read-write
Reset State: 0x0007

8-bit peak windowing clip threshold for power index 10

TXFIR_PEAKW_CLIP_THRESHOLD_10

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 10 Reset State: 0x0007

0x300041C TXFIR_PEAKW_CLIP_THRESHOLD_11

Type: read-write
Reset State: 0x0006

8-bit peak windowing clip threshold for power index 11

TXFIR_PEAKW_CLIP_THRESHOLD_11

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 11 Reset State: 0x0006

0x3000420 TXFIR_PEAKW_CLIP_THRESHOLD_12

Type: read-write
Reset State: 0x0005

8-bit peak windowing clip threshold for power index 12

TXFIR_PEAKW_CLIP_THRESHOLD_12

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 12 Reset State: 0x0005

0x3000424 TXFIR_PEAKW_CLIP_THRESHOLD_13

Type: read-write
Reset State: 0x0005

8-bit peak windowing clip threshold for power index 13

TXFIR_PEAKW_CLIP_THRESHOLD_13

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 13 Reset State: 0x0005

0x3000428 TXFIR_PEAKW_CLIP_THRESHOLD_14

Type: read-write
Reset State: 0x0004

8-bit peak windowing clip threshold for power index 14

TXFIR_PEAKW_CLIP_THRESHOLD_14

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 14 Reset State: 0x0004

0x300042C TXFIR_PEAKW_CLIP_THRESHOLD_15

Type: read-write
Reset State: 0x0004

8-bit peak windowing clip threshold for power index 15

TXFIR_PEAKW_CLIP_THRESHOLD_15

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 15 Reset State: 0x0004

0x3000430 TXFIR_PEAKW_CLIP_THRESHOLD_16

Type: read-write
Reset State: 0x0003

8-bit peak windowing clip threshold for power index 16

TXFIR_PEAKW_CLIP_THRESHOLD_16

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 16 Reset State: 0x0003

0x3000434 TXFIR_PEAKW_CLIP_THRESHOLD_17

Type: read-write
Reset State: 0x0003

8-bit peak windowing clip threshold for power index 17

TXFIR_PEAKW_CLIP_THRESHOLD_17

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 17 Reset State: 0x0003

0x3000438 TXFIR_PEAKW_CLIP_THRESHOLD_18

Type: read-write
Reset State: 0x0002

8-bit peak windowing clip threshold for power index 18

TXFIR_PEAKW_CLIP_THRESHOLD_18

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 18 Reset State: 0x0002

0x300043C TXFIR_PEAKW_CLIP_THRESHOLD_19

Type: read-write
Reset State: 0x0002

8-bit peak windowing clip threshold for power index 19

TXFIR_PEAKW_CLIP_THRESHOLD_19

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 19 Reset State: 0x0002

0x3000440 TXFIR_PEAKW_CLIP_THRESHOLD_20

Type: read-write
Reset State: 0x0002

8-bit peak windowing clip threshold for power index 20

TXFIR_PEAKW_CLIP_THRESHOLD_20

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 20 Reset State: 0x0002

0x3000444 TXFIR_PEAKW_CLIP_THRESHOLD_21

Type: read-write
Reset State: 0x0002

8-bit peak windowing clip threshold for power index 21

TXFIR_PEAKW_CLIP_THRESHOLD_21

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 21 Reset State: 0x0002

0x3000448 TXFIR_PEAKW_CLIP_THRESHOLD_22

Type: read-write
Reset State: 0x0001

8-bit peak windowing clip threshold for power index 22

TXFIR_PEAKW_CLIP_THRESHOLD_22

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 22 Reset State: 0x0001

0x300044C TXFIR_PEAKW_CLIP_THRESHOLD_23

Type: read-write
Reset State: 0x0001

8-bit peak windowing clip threshold for power index 23

TXFIR_PEAKW_CLIP_THRESHOLD_23

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 23 Reset State: 0x0001

0x3000450 TXFIR_PEAKW_CLIP_THRESHOLD_24

Type: read-write
Reset State: 0x0001

8-bit peak windowing clip threshold for power index 24

TXFIR_PEAKW_CLIP_THRESHOLD_24

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 24 Reset State: 0x0001

0x3000454 TXFIR_PEAKW_CLIP_THRESHOLD_25

Type: read-write
Reset State: 0x0001

8-bit peak windowing clip threshold for power index 25

TXFIR_PEAKW_CLIP_THRESHOLD_25

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 25 Reset State: 0x0001

0x3000458 TXFIR_PEAKW_CLIP_THRESHOLD_26

Type: read-write
Reset State: 0x0001

8-bit peak windowing clip threshold for power index 26

TXFIR_PEAKW_CLIP_THRESHOLD_26

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 26 Reset State: 0x0001

0x300045C TXFIR_PEAKW_CLIP_THRESHOLD_27

Type: read-write
Reset State: 0x0001

8-bit peak windowing clip threshold for power index 27

TXFIR_PEAKW_CLIP_THRESHOLD_27

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 27 Reset State: 0x0001

0x3000460 TXFIR_PEAKW_CLIP_THRESHOLD_28

Type: read-write
Reset State: 0x0000

8-bit peak windowing clip threshold for power index 28

TXFIR_PEAKW_CLIP_THRESHOLD_28

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 28 Reset State: 0x0000

0x3000464 TXFIR_PEAKW_CLIP_THRESHOLD_29

Type: read-write
Reset State: 0x0000

8-bit peak windowing clip threshold for power index 29

TXFIR_PEAKW_CLIP_THRESHOLD_29

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 29 Reset State: 0x0000

0x3000468 TXFIR_PEAKW_CLIP_THRESHOLD_30

Type: read-write
Reset State: 0x0000

8-bit peak windowing clip threshold for power index 30

TXFIR_PEAKW_CLIP_THRESHOLD_30

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 30 Reset State: 0x0000

0x300046C TXFIR_PEAKW_CLIP_THRESHOLD_31

Type: read-write
Reset State: 0x0000

8-bit peak windowing clip threshold for power index 31

TXFIR_PEAKW_CLIP_THRESHOLD_31

Bits	Name	Description
7:0	COEFFVAL	Clip threshold for MPI power index 31 Reset State: 0x0000

0x3000470 TXFIR_Q_INVERT

Type: read-write
Reset State: 0x0000

Register to enable sign inversion of the Q component of each chain

TXFIR_Q_INVERT

Bits	Name	Description
0:0	ENABLE	Per-chain enable for Q-component sign inversion of each chain Reset State: 0x0000

0x3000474 TXFIR_INTERP_X2

Type: read-write
Reset State: 0x0000

Register to enable interpolation by 2 instead of 1.5. This is used for P2P emulation

TXFIR_INTERP_X2

Bits	Name	Description
0:0	ENABLE	Interpolation-by-2 enable Reset State: 0x0000

0x3000478 TXFIR_IQCORR_CENTRE_TAP

Type: read-write
Reset State: 0x0002

This register defines the centre tap value in the IQ corrector complex filter

TXFIR_IQCORR_CENTRE_TAP

Bits	Name	Description
2:0	VALUE	IQ corrector centre tap location Reset State: 0x0002

0x300047C TXFIR_GAIN_OFFSET_OFDM

Type: read-write
Reset State: 0x0000

This register stores the gain offset (dB) applied to the demanded power for OFDM packets. The adjusted value is used to adjust the scaling profile applied in the DPD module.

TXFIR_GAIN_OFFSET_OFDM

Bits	Name	Description
5:0	VALUE	Reset State: 0x0000

0x3000480 TXFIR_GAIN_OFFSET_11B

Type: read-write
Reset State: 0x0000

This register stores the gain offset (dB) applied to the demanded power for 11b packets. The adjusted value is used to adjust the scaling profile applied in the DPD module.

TXFIR_GAIN_OFFSET_11B

Bits	Name	Description
5:0	VALUE	Reset State: 0x0000

0x3000800+0x20*n TXFIR_TXCAL_MEM0n_0, n=[0..23]

Type: read-write
Reset State: 0x0000

Contains TX IQ imbalance correction and TX carrier suppression values for each RF gain setting

TXFIR_TXCAL_MEM0n_0

Bits	Name	Description
15:9	IQPHASEIMB_COEFF_Q0_0	2's complement IQ phase imbalance correction value, coefficient q0 for chain 0 Reset State: 0x0000
8:0	IQPHASEIMB_COEFF_I0	2's complement IQ phase imbalance correction value, coefficient i0 for chain 0 Reset State: 0x0000

0x3000804+0x20*n TXFIR_TXCAL_MEM0n_1, n=[0..23]

Type: read-write
Reset State: 0x0000

Contains TX IQ imbalance correction and TX carrier suppression values for each RF gain setting

TXFIR_TXCAL_MEM0n_1

Bits	Name	Description
15:11	IQPHASEIMB_COEFF_Q1_0	2's complement IQ phase imbalance correction value, coefficient q1 for chain 0 Reset State: 0x0000
10:2	IQPHASEIMB_COEFF_I1	2's complement IQ phase imbalance correction value, coefficient i1 for chain 0 Reset State: 0x0000
1:0	IQPHASEIMB_COEFF_Q0_1	2's complement IQ phase imbalance correction value, coefficient q0 for chain 0 Reset State: 0x0000

0x3000808+0x20*n TXFIR_TXCAL_MEM0n_2, n=[0..23]

Type: read-write
Reset State: 0x0000

Contains TX IQ imbalance correction and TX carrier suppression values for each RF gain setting

TXFIR_TXCAL_MEM0n_2

Bits	Name	Description
15:13	IQPHASEIMB_COEFF_Q2_0	2's complement IQ phase imbalance correction value, coefficient q2 for chain 0 Reset State: 0x0000
12:4	IQPHASEIMB_COEFF_I2	2's complement IQ phase imbalance correction value, coefficient i2 for chain 0 Reset State: 0x0000
3:0	IQPHASEIMB_COEFF_Q1_1	2's complement IQ phase imbalance correction value, coefficient q1 for chain 0 Reset State: 0x0000

0x300080C+0x20*n TXFIR_TXCAL_MEM0n_3, n=[0..23]

Type: read-write
Reset State: 0x0000

Contains TX IQ imbalance correction and TX carrier suppression values for each RF gain setting

TXFIR_TXCAL_MEM0n_3

Bits	Name	Description
15	IQPHASEIMB_COEFF_Q3_0	2's complement IQ phase imbalance correction value, coefficient q3 for chain 0 Reset State: 0x0000
14:6	IQPHASEIMB_COEFF_I3	2's complement IQ phase imbalance correction value, coefficient i3 for chain 0 Reset State: 0x0000
5:0	IQPHASEIMB_COEFF_Q2_1	2's complement IQ phase imbalance correction value, coefficient q2 for chain 0 Reset State: 0x0000

0x3000810+0x20*n TXFIR_TXCAL_MEM0n_4, n=[0..23]

Type: read-write
Reset State: 0x0000

Contains TX IQ imbalance correction and TX carrier suppression values for each RF gain setting

TXFIR_TXCAL_MEM0n_4

Bits	Name	Description
15:8	IQPHASEIMB_COEFF_I4_0	2's complement IQ phase imbalance correction value, coefficient i4 for chain 0 Reset State: 0x0000
7:0	IQPHASEIMB_COEFF_Q3_1	2's complement IQ phase imbalance correction value, coefficient q3 for chain 0 Reset State: 0x0000

0x3000814+0x20*n TXFIR_TXCAL_MEM0n_5, n=[0..23]

Type: read-write
Reset State: 0x0000

Contains TX IQ imbalance correction and TX carrier suppression values for each RF gain setting

TXFIR_TXCAL_MEM0n_5

Bits	Name	Description
15:10	IQ_AMPIMB_COEFF_0	2's complement IQ amplitude imbalance correction factor. Reset State: 0x0000

TXFIR_TXCAL_MEM0n_5 (cont.)

Bits	Name	Description
9:1	IQPHASEIMB_COEFF_Q4	2's complement IQ phase imbalance correction value, coefficient q4 for chain 0 Reset State: 0x0000
0	IQPHASEIMB_COEFF_I4_1	2's complement IQ phase imbalance correction value, coefficient i4 for chain 0 Reset State: 0x0000

0x3000818+0x20*n TXFIR_TXCAL_MEM0n_6, n=[0..23]

Type: read-write
Reset State: 0x0000

Contains TX IQ imbalance correction and TX carrier suppression values for each RF gain setting

TXFIR_TXCAL_MEM0n_6

Bits	Name	Description
14:9	TXLOLEAKAGE_Q	2's complement Transmit chain local oscillator leakage for chain 0, Q rail Reset State: 0x0000
8:3	TXLOLEAKAGE_I	2's complement Transmit chain local oscillator leakage for chain 0, I rail Reset State: 0x0000
2:0	IQ_AMPIMB_COEFF_1	2's complement IQ amplitude imbalance correction factor. Reset State: 0x0000

0x3001000+0x10*n TXFIR_DPD_MEM0n_0, n=[0..127]

Type: read-write
Reset State: 0x0000

Contains TX pre-distorter parameter values for each RF gain setting

TXFIR_DPD_MEM0n_0

Bits	Name	Description
15:12	DPD_AOFFSET_0	DPD amplitude gain offset for each section on chain 0 Reset State: 0x0000
11:0	DPD_THRESHOLD	DPD amplitude threshold for each section on chain 0 Reset State: 0x0000

0x3001004+0x10*n TXFIR_DPD_MEM0n_1, n=[0..127]

Type: read-write
Reset State: 0x0000

Contains TX pre-distorter parameter values for each RF gain setting

TXFIR_DPD_MEM0n_1

Bits	Name	Description
15:8	DPD_AGAIN_0	DPD amplitude gain change for each section on chain 0 Reset State: 0x0000
7:0	DPD_AOFFSET_1	DPD amplitude gain offset for each section on chain 0 Reset State: 0x0000

0x3001008+0x10*n TXFIR_DPD_MEM0n_2, n=[0..127]

Type: read-write
Reset State: 0x0000

Contains TX pre-distorter parameter values for each RF gain setting

TXFIR_DPD_MEM0n_2

Bits	Name	Description
15:4	DPD_POFFSET	DPD phase gain offset for each section on chain 0 Reset State: 0x0000
3:0	DPD_AGAIN_1	DPD amplitude gain change for each section on chain 0 Reset State: 0x0000

0x300100C+0x10*n TXFIR_DPD_MEM0n_3, n=[0..127]

Type: read-write
Reset State: 0x0000

Contains TX pre-distorter parameter values for each RF gain setting

TXFIR_DPD_MEM0n_3

Bits	Name	Description
11:0	DPD_PGAIN	DPD phase gain change for each section on chain 0 Reset State: 0x0000

16.2.33 pmu

0x3000000 PMU_INT_OUT_RPM

Type: read-write
Reset State: 0x00000000

Interrupt output to RPM.

PMU_INT_OUT_RPM

Bits	Name	Description
3	RIVA_RPM_GP_LOW_IRQ	riva_rpm_gp_low_irq Reset State: 0x00000000
2	RIVA_RPM_GP_MED_IRQ	riva_rpm_gp_med_irq Reset State: 0x00000000
1	RIVA_RPM_GP_HI_IRQ	riva_rpm_gp_hi_irq Reset State: 0x00000000

0x3000004 PMU_INT_STS

Type: read-only
Reset State: 0x00000000

wake up interrupt status

PMU_INT_STS

Bits	Name	Description
7	BT_SLP_TIME_IRQ	BT sleep timer wake up interrupt Reset State: 0x00000000
6	WLAN_SLP_TIMER_IRQ	WLAN sleep timer wake up interrupt Reset State: 0x00000000
5	CCU_CCPU_WAKEUP_IRQ	WLAN to cCPU wake up interrupt. e.g., Beacon reception/time out interrupt. Reset State: 0x00000000
4	ACPU_RIVA_WAKEUP_IRQ	ACPU to Riva wake up interrupt Reset State: 0x00000000
3	RPM_RIVA_GP_LOW_IRQ	RPM to Riva wake up interrupt Reset State: 0x00000000
2	RPM_RIVA_GP_MED_IRQ	RPM to Riva wake up interrupt Reset State: 0x00000000

PMU_INT_STS (cont.)

Bits	Name	Description
1	RPM_RIVA_GP_HI_IRQ	RPM to Riva wake up interrupt Reset State: 0x00000000
0	RPM_RIVA_WAKEUP_IRQ	RPM to Riva wake up interrupt Reset State: 0x00000000

0x3000008 PMU_INT_EN

Type: read-write
Reset State: 0x00000000

interrupts enable bit.

PMU_INT_EN

Bits	Name	Description
7	BT_SLP_TIMER_IRQ_EN	enable bt_slp_timer_irq to wakeup Riva. Reset State: 0x00000000
6	WLAN_SLP_TIMER_IRQ_EN	enable wlan_slp_timer_irq to wakeup Riva. Reset State: 0x00000000
5	CCU_CCPU_WAKEUP_IRQ_EN	enable ccu_ccpu_wakeup_irq to wakeup clock gated cCPU. Reset State: 0x00000000
4	ACPU_RIVA_WAKEUP_IRQ_EN	enable acpu_riva_wakeup_irq to wakeup Riva. Reset State: 0x00000000
3	RPM_RIVA_GP_LOW_IRQ_EN	enable rpm_riva_gp_low_irq to wakeup Riva. Reset State: 0x00000000
2	RPM_RIVA_GP_MED_IRQ_EN	enable rpm_riva_gp_med_irq to wakeup Riva. Reset State: 0x00000000
1	RPM_RIVA_GP_HI_IRQ_EN	enable rpm_riva_gp_hi_irq to wakeup Riva. Reset State: 0x00000000
0	RPM_RIVA_WAKEUP_IRQ_EN	enable rpm_riva_wakeup_irq to wakeup Riva. Reset State: 0x00000000

0x300000C PMU_INT_STS_RAW

Type: read-only
Reset State: 0x00000000

wake up interrupt status before gating with enable

PMU_INT_STS_RAW

Bits	Name	Description
7	BT_SLP_TIME_IRQ_RAW	status of bt_slp_timer_irq before gating with bt_slp_timer_irq_en. Reset State: 0x00000000
6	WLAN_SLP_TIMER_IRQ_RAW	status of wlan_slp_timer_irq before gating with wlan_slp_timer_irq_en. Reset State: 0x00000000
5	CCU_CCPU_WAKEUP_IRQ_RAW	status of ccu_ccpu_wakeup_irq before gating with ccu_ccpu_wakeup_irq_en. Reset State: 0x00000000
4	ACPU_RIVA_WAKEUP_IRQ_RAW	status of acpu_riva_wakeup_irq before gating with acpu_riva_wakeup_irq_en. Reset State: 0x00000000
3	RPM_RIVA_GP_LOW_IRQ_RAW	status of rpm_riva_gp_low_irq before gating with rpm_riva_gp_low_irq_en. Reset State: 0x00000000
2	RPM_RIVA_GP_MED_IRQ_RAW	status of rpm_riva_gp_med_irq before gating with rpm_riva_gp_med_irq_en. Reset State: 0x00000000
1	RPM_RIVA_GP_HI_IRQ_RAW	status of rpm_riva_gp_hi_irq before gating with rpm_riva_gp_hi_irq_en. Reset State: 0x00000000
0	RPM_RIVA_WAKEUP_IRQ_RAW	status of rpm_riva_wakeup_irq before gating with rpm_riva_wakeup_irq_en. Reset State: 0x00000000

0x3000010 PMU_GFS_CNTL_COMMON

Type: read-write
Reset State: 0x00000002

GFS_CNTL input for Riva_Common_SS

PMU_GFS_CNTL_COMMON

Bits	Name	Description
9:5	GFS_CTL_COMMON	Reserved bits. Reset State: 0x00000000
4:0	GFS_CTL_TMR_COMMON	Timer for staggered switch on. Reset State: 0x00000002

0x3000014 PMU_GFS_CNTL_WLAN

Type: read-write
Reset State: 0x00000102

GFS_CNTL input for WLAN_SS

PMU_GFS_CNTL_WLAN

Bits	Name	Description
13	GLOBAL_CLK_GATE_DISABLE_WLAN	global clock gate disable to WLAN modules Reset State: 0x00000000
12	RESET_N_WLAN	reset, Reset State: 0x00000000
11	CLK_EN_WLAN	clock enable. Reset State: 0x00000000
10	GFS_CTL_CLAMP_IO_WLAN	clamp io. Reset State: 0x00000000
9	GFS_CTL_RET_WLAN	gfs retention bits. Reset State: 0x00000000
8	GFS_CTL_EN_WLAN	gfs enable bits. Default is 1 as headswitch shold be enabled from power on reset. Reset State: 0x00000001
7:5	GFS_CTL_WLAN	Reserved bits. Reset State: 0x00000000
4:0	GFS_CTL_TMR_WLAN	Timer for staggered switch on. Reset State: 0x00000002

0x3000018 PMU_PWR_CNTL_ADCDAC

Type: read-write
Reset State: 0x00000000

power control to ADC/DAC block

PMU_PWR_CNTL_ADCDAC

Bits	Name	Description
1	IDDQ_N_ADC	Freeze IO from ADC. Reset State: 0x00000000
0	SHUTDOWN_N_ADC	shutdown ADC regulator. Reset State: 0x00000000

0x300001C PMU_GFS_STS_COMMON

Type: read-only
Reset State: 0x00000003

GFS_CNTL status for Riva_Common_SS.

PMU_GFS_STS_COMMON

Bits	Name	Description
2	GFS_STS_CLAMP_IO_COMMON	clamp_io output from GFS_CNTL for Riva_Common_SS. Reset State: 0x00000000
1	GFS_STS_EN_FEW_COMMON	en_few output from GFS_CNTL for Riva_Common_SS. Reset State: 0x00000001
0	GFS_STS_EN_REST_COMMON	en_rest output from GFS_CNTL for Riva_Common_SS. Reset State: 0x00000001

0x3000020 PMU_GFS_STS_WLAN

Type: read-only
Reset State: 0x00000003

GFS_CNTL status for WLAN_SS.

PMU_GFS_STS_WLAN

Bits	Name	Description
2	GFS_STS_CLAMP_IO_WLAN	clamp_io output from GFS_CNTL for WLAN_SS. Reset State: 0x00000000
1	GFS_STS_EN_FEW_WLAN	en_few output from GFS_CNTL for WLAN_SS. Reset State: 0x00000001
0	GFS_STS_EN_REST_WLAN	en_rest output from GFS_CNTL for WLAN_SS. Reset State: 0x00000001

0x3000024 PMU_PWR_STS_ADCDAC

Type: read-only
Reset State: 0x00000000

Power status from ADC/DAC.

PMU_PWR_STS_ADCDAC

Bits	Name	Description
31:0	PWR_STS_ADCDAC_RSVD	Reserved. Reset State: 0x00000000

0x3000028 PMU_CFG

Type: read-write
Reset State: 0x00010000

Configuration.

PMU_CFG

Bits	Name	Description
19	ADCDAC_ASYNC_CLK_HALT	Asynchronous clock halt to CXC Reset State: 0x00000000
18	PHYDBG_CLKMUX_SEL	0x0: select PHY 320/120/60 1: select cpu clock For scan mode and MBIST mode it is always set to 0 so that roo1_320_160_60 clock is selected Reset State: 0x00000000
17	PHYDBG_ASYNC_CLK_HALT	Asynchronous clock halt to CXC Reset State: 0x00000000
16	LVMBIST_HARDCODE_EN	LV Mbist hardcode enable Reset State: 0x00000001
15:14	BW_CONFIG_RX	RX BW configuration Reset State: 0x00000000
13:12	BW_CONFIG_TX	TX BW configuration Reset State: 0x00000000
11	AHB_SAW_HPROTNS	SAW2 AHB protection control Reset State: 0x00000000
10	SPM_SYS_SLEEP_STATE	status of spm_sys_sleep_state output from SAW2 Reset State: 0x00000000
9	SPM_CPU_DBG_STAY_AWAKE	status of spm_cpu_dbg_stay_awake output from SAW2 Reset State: 0x00000000
8	SYS_SPM_DBG_NOPWRDWN	sys_spm_dbg_nopwrdwn input to SAW2 Reset State: 0x00000000
6	IRIS_XO_CFG_STS	IRIS XO configuration status.1: in progress0: done or idle Reset State: 0x00000000

PMU_CFG (cont.)

Bits	Name	Description
5	GC_BUS_MUX_SEL	0x1: GC bus is controlled by riva_top0: GC bus is controlled by WLAN PHY Reset State: 0x00000000
4	IRIS_XO_EN	0x1: enable XO during configuration0: disable XO during configuration Reset State: 0x00000000
3	IRIS_XO_CFG	start IRIS XO configuration Reset State: 0x00000000
2:1	IRIS_XO_MODE	IRIS XO mode. 2'b11 : 48MHz XO 2'b01 : 38.4MHz TCXO 2'b00 : 19.2MHz TCXO Reset State: 0x00000000
0	WARM_BOOT	warm/cold boot indication. Reset State: 0x00000000

0x300002C PMU_OVRD_EN

Type: read-write
Reset State: 0x00000003

enable override of controls

PMU_OVRD_EN

Bits	Name	Description
5	PMU_TCXO_CLKGATE_DISABLE_OVRD_EN	override tcxo_clkgate_disable for PMU Reset State: 0x00000000
4	PMU_DISABLE_CLK_GATING_OVRD_EN	override disable_clk_gating for PMU Reset State: 0x00000000
3	COMMON_CLK_EN_OVRD_EN	override clock enable to common SS except cCPU Reset State: 0x00000000
2	COMMON_RESET_N_OVRD_EN	override reset_n to common SS except cCPU Reset State: 0x00000000
1	CCPU_CLK_EN_OVRD_EN	override clock enable to cCPU Reset State: 0x00000001
0	CCPU_RESET_N_OVRD_EN	override reset_n to cCPU Reset State: 0x00000001

0x3000030 PMU_OVRD_VAL

Type: read-write
Reset State: 0x00000000

override value of controls

PMU_OVRD_VAL

Bits	Name	Description
5	PMU_TCXO_CLKGATE_DISABLE_OVRD_VAL	override value of tcxo_clkgate_disable for PMU Reset State: 0x00000000
4	PMU_DISABLE_CLK_GATING_OVRD_VAL	override value of disable_clk_gating for PMU Reset State: 0x00000000
3	COMMON_CLK_EN_OVRD_VAL	override value of clock enable to common SS except cCPU Reset State: 0x00000000
2	COMMON_RESET_N_OVRD_VAL	override value of reset_n to common SS except cCPU Reset State: 0x00000000
1	CCPU_CLK_EN_OVRD_VAL	override value of clock enable to cCPU Reset State: 0x00000000
0	CCPU_RESET_N_OVRD_VAL	override value of reset_n to cCPU Reset State: 0x00000000

0x3000034 PMU_SLP_TMR_CTL

Type: read-write
Reset State: 0x00000000

control for sleep timer

PMU_SLP_TMR_CTL

Bits	Name	Description
7	CLK_INT_CLR	Clear slp_clk_int. Reset State: 0x00000000
6	TMR_EN_INT_CLR	Clear tmr_en_int. Reset State: 0x00000000
5	CLK_INT_EN	Enable interrupt at the next rising edge of sleep clock. Due to synchronization, it may not be the very next risign edge, but could be 1
4	TMR_EN_INT_EN	Enable interrupt when sleep timer is enabled. Interrupt will be asserted at the rising edge of sleep clock when sleep timer starts to increase or decrease. Reset State: 0x00000000

PMU_SLP_TMR_CTL (cont.)

Bits	Name	Description
3	TMR_ADD	add slp_tmr_val_wr[31:0] to the current sleep timer value. Reset State: 0x00000000
2	TMR_LD	load sleep timer with slp_tmr_val_wr[31:0]. Reset State: 0x00000000
1	TMR_DEC	0x1: Decrement sleep timer when tmr_en is set.0: increment sleep timer when tmr_en is set. Reset State: 0x00000000
0	TMR_EN	Enable sleep timer increment or decrement. Reset State: 0x00000000

0x3000038 PMU_SLP_TMR_STS

Type: read-only
Reset State: 0x00000000

Status of sleep timer.

PMU_SLP_TMR_STS

Bits	Name	Description
2	CLK_INT	Status of slp_clk_int. Reset State: 0x00000000
1	TMR_EN_INT	Status of tmr_en_int. Reset State: 0x00000000
0	TOGGLE	This bit toggles at the every rising edge of sleep clock. Reset State: 0x00000000

0x300003C PMU_SLP_TMR_VAL_WR

Type: read-write
Reset State: 0x00000000

sleep timer value to be written

PMU_SLP_TMR_VAL_WR

Bits	Name	Description
31:0	SLP_TMR_WR	sleep timer value to be written. Reset State: 0x00000000

0x3000040 PMU_SLP_TMR_VAL

Type: read-only
Reset State: 0x00000000

current sleep timer value

PMU_SLP_TMR_VAL

Bits	Name	Description
31:0	SLP_TMR	current sleep timer value Reset State: 0x00000000

0x3000044 PMU_WLAN_SLP_TMR_CTL

Type: read-write
Reset State: 0x00000000

WLAN control of sleep timer

PMU_WLAN_SLP_TMR_CTL

Bits	Name	Description
2	WLAN_SLP_TMR_INT_CLR	clear sleep timer interrupt for WLAN. Reset State: 0x00000000
1	WLAN_SLP_TMR_INT_EN	enable sleep timer interrupt for WLAN. Reset State: 0x00000000
0	WLAN_SLP_TMR_EN	enable sleep timer for WLAN. Reset State: 0x00000000

0x3000048 PMU_WLAN_SLP_TMR_STS

Type: read-only
Reset State: 0x00000000

sleep timer status for WLAN

PMU_WLAN_SLP_TMR_STS

Bits	Name	Description
1	WLAN_SLP_TMR_INT	status of WLAN sleep timer interrupt Reset State: 0x00000000
0	WLAN_SLP_TMR_INT_RAW	raw status of WLAN sleep timer interrupt Reset State: 0x00000000

0x300004C PMU_WLAN_SLP_TMR_EXP

Type: read-write
Reset State: 0x00000000

sleep timer expiration value for WLAN

PMU_WLAN_SLP_TMR_EXP

Bits	Name	Description
31:0	WLAN_SLP_TMR_EXP	sleep timer expiration value for WLAN. Reset State: 0x00000000

0x3000050 PMU_BT_SLP_TMR_CTL

Type: read-write
Reset State: 0x00000000

BT control of sleep timer

PMU_BT_SLP_TMR_CTL

Bits	Name	Description
2	BT_SLP_TMR_INT_CLR	clear sleep timer interrupt for BT. Reset State: 0x00000000
1	BT_SLP_TMR_INT_EN	enable sleep timer interrupt for BT. Reset State: 0x00000000
0	BT_SLP_TMR_EN	enable sleep timer for BT. Reset State: 0x00000000

0x3000054 PMU_BT_SLP_TMR_STS

Type: read-only
Reset State: 0x00000000

sleep timer status for BT

PMU_BT_SLP_TMR_STS

Bits	Name	Description
1	BT_SLP_TMR_INT	status of BT sleep timer interrupt Reset State: 0x00000000
0	BT_SLP_TMR_INT_RAW	raw status of BT sleep timer interrupt Reset State: 0x00000000

0x3000058 PMU_BT_SLP_TMR_EXP

Type: read-write
Reset State: 0x00000000

sleep timer expiration value for BT

PMU_BT_SLP_TMR_EXP

Bits	Name	Description
31:0	BT_SLP_TMR_EXP	sleep timer expiration value for BT. Reset State: 0x00000000

0x300005C PMU_FSCXC_CS_AHB_COMMON

Type: read-write
Reset State: 0x0000C051

Control and status of FSCXC hard macro for AHB clock memories in Common_SS (cMEM)

PMU_FSCXC_CS_AHB_COMMON

Bits	Name	Description
15	MEM_CORE_ON	mem_core_on output of FSCXC. It is same as slp_nret_n. Reset State: 0x00000001
14	MEM_PERIPH_ON	mem_periph_on output of FSCXC. It is same as slp_ret_n. Reset State: 0x00000001
13	ROOT_CLOCK_OFF	Indication of clock output from FSCXC is gated. Reset State: 0x00000000
12	SYNC_CLK_HALT	Synchronous clock halt to FSCXC. Reset State: 0x00000000
11	UP_FORCE_PERIPH_OFF	Force slp_ret_n to 0. Reset State: 0x00000000
10	UP_FORCE_PERIPH_ON	Force slp_ret_n to 1. Reset State: 0x00000000
9	UP_FORCE_CORE_ON	Force slp_nret_n to 1. For entering retention sleep mode, this bit should be set to 1 before starting SAW2 power down. Reset State: 0x00000000
8	CLK_INV	Invert clock to memory Reset State: 0x00000000
7:4	W	w input to hm_fscxc. The number of memory clocks after slp_(n)ret_n is de-asserted until clock is enabled. w should meet min 20 ns, so ceil(20ns/(1/240MHz)) =5 is used as default. Reset State: 0x00000005

PMU_FSCXC_CS_AHB_COMMON (cont.)

Bits	Name	Description
3:0	S	s input to hm_fscxc. The number of memory clocks before slp_(n)ret_n is asserted from clock is disabled. Max frquency of ahb clock is 240MHz, and there is slower derived clock. s should meet at least 1 memory clock, so 1 is used as default. Reset State: 0x00000001

0x3000060 PMU_FSCXC_CS_CCPU

Type: read-write
Reset State: 0x00002051

Control and status of FSCXC hard macro for cCPU clock memories (cMEM, cCPU cache)

PMU_FSCXC_CS_CCPU

Bits	Name	Description
15	MEM_CORE_ON	mem_core_on output of FSCXC. It is same as slp_nret_n. Reset State: 0x00000000
14	MEM_PERIPH_ON	mem_periph_on output of FSCXC. It is same as slp_ret_n. Reset State: 0x00000000
13	ROOT_CLOCK_OFF	Indication of clock output from FSCXC is gated. Reset State: 0x00000001
12	SYNC_CLK_HALT	Synchronous clock halt to FSCXC. Reset State: 0x00000000
11	UP_FORCE_PERIPH_OFF	Force slp_ret_n to 0. Reset State: 0x00000000
10	UP_FORCE_PERIPH_ON	Force slp_ret_n to 1. Reset State: 0x00000000
9	UP_FORCE_CORE_ON	Force slp_nret_n to 1. For entering retention sleep mode, this bit should be set to 1 before starting SAW2 power down. Reset State: 0x00000000
8	CLK_INV	Invert clock to memory Reset State: 0x00000000
7:4	W	w input to hm_fscxc. The number of memory clocks after slp_(n)ret_n is de-asserted until clock is enabled. w should meet min 20 ns, so ceil(20ns/(1/240MHz)) =5 is used as default. Reset State: 0x00000005
3:0	S	s input to hm_fscxc. The number of memory clocks before slp_(n)ret_n is asserted from clock is disabled. Max frquency of ccpu clock is 240MHz, and there is slower derived clock. s should meet at least 1 memory clock, so 1 is used as default. Reset State: 0x00000001

0x3000064 PMU_FSCXC_CS_AHB_WLAN

Type: read-write
Reset State: 0x00002051

Control and status of FSCXC hard macro for AHB clock memories in WLAN (cMEM)

PMU_FSCXC_CS_AHB_WLAN

Bits	Name	Description
15	MEM_CORE_ON	mem_core_on output of FSCXC. It is same as slp_nret_n. Reset State: 0x00000000
14	MEM_PERIPH_ON	mem_periph_on output of FSCXC. It is same as slp_ret_n. Reset State: 0x00000000
13	ROOT_CLOCK_OFF	Indication of clock output from FSCXC is gated. Reset State: 0x00000001
12	SYNC_CLK_HALT	Synchronous clock halt to FSCXC. Reset State: 0x00000000
11	UP_FORCE_PERIPH_OFF	Force slp_ret_n to 0. Reset State: 0x00000000
10	UP_FORCE_PERIPH_ON	Force slp_ret_n to 1. Reset State: 0x00000000
9	UP_FORCE_CORE_ON	Force slp_nret_n to 1. For entering retention sleep mode, this bit should be set to 1 before starting SAW2 power down. Reset State: 0x00000000
8	CLK_INV	Invert clock to memory Reset State: 0x00000000
7:4	W	w input to hm_fscxc. The number of memory clocks after slp_(n)ret_n is de-asserted until clock is enabled. w should meet min 20 ns, so ceil(20ns/(1/240MHz)) =5 is used as default. Reset State: 0x00000005
3:0	S	s input to hm_fscxc. The number of memory clocks before slp_(n)ret_n is asserted from clock is disabled. Max frquency of ahb clock is 240MHz, and there is slower derived clock. s should meet at least 1 memory clock, so 1 is used as default. Reset State: 0x00000001

0x3000068 PMU_FSCXC_CS_PHY1

Type: read-write
Reset State: 0x00002071

Control and status of FSCXC hard macro for PHY1 clock memories

PMU_FSCXC_CS_PHY1

Bits	Name	Description
15	MEM_CORE_ON	mem_core_on output of FSCXC. It is same as slp_nret_n. Reset State: 0x00000000
14	MEM_PERIPH_ON	mem_periph_on output of FSCXC. It is same as slp_ret_n. Reset State: 0x00000000
13	ROOT_CLOCK_OFF	Indication of clock output from FSCXC is gated. Reset State: 0x00000001
12	SYNC_CLK_HALT	Synchronous clock halt to FSCXC. Reset State: 0x00000000
11	UP_FORCE_PERIPH_OFF	Force slp_ret_n to 0. Reset State: 0x00000000
10	UP_FORCE_PERIPH_ON	Force slp_ret_n to 1. Reset State: 0x00000000
9	UP_FORCE_CORE_ON	Force slp_nret_n to 1. For entering retention sleep mode, this bit should be set to 1 before starting SAW2 power down. Reset State: 0x00000000
8	CLK_INV	Invert clock to memory Reset State: 0x00000000
7:4	W	w input to hm_fscxc. The number of memory clocks after slp_(n)ret_n is de-asserted until clock is enabled. w should meet min 20 ns, so ceil(20ns/(1/320MHz)) =7 is used as default. Reset State: 0x00000007
3:0	S	s input to hm_fscxc. The number of memory clocks before slp_(n)ret_n is asserted from clock is disabled. Max frquency of phy main1 clock is 320MHz, and there is no slower derived clock. s should meet at least 1 memory clock, so 1 is used as default. Reset State: 0x00000001

0x300006C PMU_FSCXC_CS_PHY2

Type: read-write
Reset State: 0x00002078

Control and status of FSCXC hard macro for PHY1 clock memories

PMU_FSCXC_CS_PHY2

Bits	Name	Description
15	MEM_CORE_ON	mem_core_on output of FSCXC. It is same as slp_nret_n. Reset State: 0x00000000

PMU_FSCXC_CS_PHY2 (cont.)

Bits	Name	Description
14	MEM_PERIPH_ON	mem_periph_on output of FSCXC. It is same as slp_ret_n. Reset State: 0x00000000
13	ROOT_CLOCK_OFF	Indication of clock output from FSCXC is gated. Reset State: 0x00000001
12	SYNC_CLK_HALT	Synchronous clock halt to FSCXC. Reset State: 0x00000000
11	UP_FORCE_PERIPH_OFF	Force slp_ret_n to 0. Reset State: 0x00000000
10	UP_FORCE_PERIPH_ON	Force slp_ret_n to 1. Reset State: 0x00000000
9	UP_FORCE_CORE_ON	Force slp_nret_n to 1. For entering retention sleep mode, this bit should be set to 1 before starting SAW2 power down. Reset State: 0x00000000
8	CLK_INV	Invert clock to memory Reset State: 0x00000000
7:4	W	w input to hm_fscxc. The number of memory clocks after slp_(n)ret_n is de-asserted until clock is enabled. w should meet min 20 ns, so ceil(20ns/(1/320MHz)) =7 is used as default. Reset State: 0x00000007
3:0	S	s input to hm_fscxc. The number of memory clocks before slp_(n)ret_n is asserted from clock is disabled. Max frquency of phy main2 clock is 320MHz, and the slowest derived clock which drives memory is 40MHz. s should meet at least 1 memory clock, so 320/40=8 is used as default. Reset State: 0x00000008

0x3000070 PMU_CLK_ROOT1

Type: read-write
Reset State: 0x00004A01

clock root1 control

PMU_CLK_ROOT1

Bits	Name	Description
15:13	SRC1_SEL	clock root1 src1 sel. This field selects the output of the clock source MUX for SRC1. 000 : XO(19.2M) 001 : Riva PLL (480MHz) 010 : spare0 src 011 : 0 100 : 0 101 : 0 110 : core_bi_clk_test_se 111 : core_bi_pll_test_se Reset State: 0x00000002

PMU_CLK_ROOT1 (cont.)

Bits	Name	Description
12:9	SRC1_DIV	clock root1 src1 div. This field selects to activate or bypass the modulo divider for SRC1 0000 : Bypass 0001 : Div-2 0010 : Div-3 0011 : Div-4 0100 : Div-5 0101 : Div-6 0110 : Div-7 0111 : Div-8 1000 : Div-9 1001 : Div-10 1010 : Div-11 1011 : Div-12 1100 : Div-13 1101 : Div-14 1110 : Div-15 1111 : Div-16 Reset State: 0x00000005
8:6	SRC0_SEL	clock root1 src0 sel. This field selects the output of the clock source MUX for SRC0. 000 : XO(19.2M) 001 : Riva PLL (960MHz) 010 : Riva PLL (480MHz) 011 : spare0 src 100 : 0 101 : 0 110 : core_bi_clk_test_se 111 : core_bi_pll_test_se Reset State: 0x00000000
5:2	SRC0_DIV	clock root1 src0 div. This field selects to activate or bypass the modulo divider for SRC0 0000 : Bypass 0001 : Div-2 0010 : Div-3 0011 : Div-4 0100 : Div-5 0101 : Div-6 0110 : Div-7 0111 : Div-8 1000 : Div-9 1001 : Div-10 1010 : Div-11 1011 : Div-12 1100 : Div-13 1101 : Div-14 1110 : Div-15 1111 : Div-16 Reset State: 0x00000000
0	CLK_ENA	clock root1 enable. Enable clock source for Riva Root1 clk ctrl 1: Enable 0: Disable Reset State: 0x00000001

0x3000074 PMU_CLK_ROOT2

Type: read-write
Reset State: 0x00002E01

clock root2 control

PMU_CLK_ROOT2

Bits	Name	Description
17:16	DIV_MAX_COUNT	clock root2 adc div max count. Reset State: 0x00000000
15:13	SRC1_SEL	clock root2 src1 sel. This field selects the output of the clock source MUX for SRC1. 000 : XO(19.2M) 001 : Riva PLL (480MHz) 010 : spare0 src 011 : 0 100 : 0 101 : 0 110 : core_bi_clk_test_se 111 : core_bi_pll_test_se Reset State: 0x00000001
12:9	SRC1_DIV	clock root2 src1 div. This field selects to activate or bypass the modulo divider for SRC1 0000 : Bypass 0001 : Div-2 0010 : Div-3 0011 : Div-4 0100 : Div-5 0101 : Div-6 0110 : Div-7 0111 : Div-8 1000 : Div-9 1001 : Div-10 1010 : Div-11 1011 : Div-12 1100 : Div-13 1101 : Div-14 1110 : Div-15 1111 : Div-16 Reset State: 0x00000007

PMU_CLK_ROOT2 (cont.)

Bits	Name	Description
8:6	SRC0_SEL	clock root2 src0 sel. This field selects the output of the clock source MUX for SRC0. 000 : XO(19.2M) 001 : Riva PLL (480MHz) 010 : spare0 src 011 : 0 100 : 0 101 : 0 110 : core_bi_clk_test_se 111 : core_bi_pll_test_se Reset State: 0x00000000
5:2	SRC0_DIV	clock root2 src0 div. This field selects to activate or bypass the modulo divider for SRC0 0000 : Bypass 0001 : Div-2 0010 : Div-3 0011 : Div-4 0100 : Div-5 0101 : Div-6 0110 : Div-7 0111 : Div-8 1000 : Div-9 1001 : Div-10 1010 : Div-11 1011 : Div-12 1100 : Div-13 1101 : Div-14 1110 : Div-15 1111 : Div-16 Reset State: 0x00000000
0	CLK_ENA	clock root2 enable. Enable clock source for Riva Root2 clk ctrl 1: Enable 0: Disable Reset State: 0x00000001

0x3000078 PMU_CLK_ROOT3

Type: read-write
Reset State: 0x00012201

clock root3 control

PMU_CLK_ROOT3

Bits	Name	Description
19:16	DIV_MAX_COUNT	clock root3 div max count. Reset State: 0x00000001
15:13	SRC1_SEL	clock root3 src1 sel. This field selects the output of the clock source MUX for SRC1. 000 : XO(19.2M) 001 : Riva PLL (480MHz) 010 : spare0 src 011 : 0 100 : 0 101 : 0 110 : core_bi_clk_test_se 111 : core_bi_pll_test_se Reset State: 0x00000001
12:9	SRC1_DIV	clock root3 src1 div. This field selects to activate or bypass the modulo divider for SRC1 0000 : Bypass 0001 : Div-2 0010 : Div-3 0011 : Div-4 0100 : Div-5 0101 : Div-6 0110 : Div-7 0111 : Div-8 1000 : Div-9 1001 : Div-10 1010 : Div-11 1011 : Div-12 1100 : Div-13 1101 : Div-14 1110 : Div-15 1111 : Div-16 Reset State: 0x00000001
8:6	SRC0_SEL	clock root3 src0 sel. This field selects the output of the clock source MUX for SRC0. 000 : XO(19.2M) 001 : Riva PLL (480MHz) 010 : spare0 src 011 : 0 100 : 0 101 : 0 110 : core_bi_clk_test_se 111 : core_bi_pll_test_se Reset State: 0x00000000

PMU_CLK_ROOT3 (cont.)

Bits	Name	Description
5:2	SRC0_DIV	clock root3 src0 div. This field selects to activate or bypass the modulo divider for SRC0 0000 : Bypass 0001 : Div-2 0010 : Div-3 0011 : Div-4 0100 : Div-5 0101 : Div-6 0110 : Div-7 0111 : Div-8 1000 : Div-9 1001 : Div-10 1010 : Div-11 1011 : Div-12 1100 : Div-13 1101 : Div-14 1110 : Div-15 1111 : Div-16 Reset State: 0x00000000
0	CLK_ENA	clock root3 enable. Enable clock source for Riva Root3 clk ctrl 1: Enable 0: Disable Reset State: 0x00000001

0x300007C PMU_CLK_ROOT4

Type: read-write
Reset State: 0x00002601

clock root4 control

PMU_CLK_ROOT4

Bits	Name	Description
15:13	SRC1_SEL	clock root4 src1 sel. This field selects the output of the clock source MUX for SRC1. 000 : XO(19.2M) 001 : Riva PLL (480MHz) 010 : spare0 src 011 : 0 100 : 0 101 : 0 110 : core_bi_clk_test_se 111 : core_bi_pll_test_se Reset State: 0x00000001
12:9	SRC1_DIV	clock root4 src1 div. This field selects to activate or bypass the modulo divider for SRC1 0000 : Bypass 0001 : Div-2 0010 : Div-3 0011 : Div-4 0100 : Div-5 0101 : Div-6 0110 : Div-7 0111 : Div-8 1000 : Div-9 1001 : Div-10 1010 : Div-11 1011 : Div-12 1100 : Div-13 1101 : Div-14 1110 : Div-15 1111 : Div-16 Reset State: 0x00000003
8:6	SRC0_SEL	clock root4 src0 sel. This field selects the output of the clock source MUX for SRC0. 000 : XO(19.2M) 001 : Riva PLL (480MHz) 010 : spare0 src 011 : 0 100 : 0 101 : 0 110 : core_bi_clk_test_se 111 : core_bi_pll_test_se Reset State: 0x00000000
5:2	SRC0_DIV	clock root4 src0 div. This field selects to activate or bypass the modulo divider for SRC0 0000 : Bypass 0001 : Div-2 0010 : Div-3 0011 : Div-4 0100 : Div-5 0101 : Div-6 0110 : Div-7 0111 : Div-8 1000 : Div-9 1001 : Div-10 1010 : Div-11 1011 : Div-12 1100 : Div-13 1101 : Div-14 1110 : Div-15 1111 : Div-16 Reset State: 0x00000000
0	CLK_ENA	clock root4 enable. Enable clock source for Riva Root4 clk ctrl 1: Enable 0: Disable Reset State: 0x00000001

0x3000080 PMU_CLK_ROOT5

Type: read-write
Reset State: 0x00003C01

clock root5 control

PMU_CLK_ROOT5

Bits	Name	Description
19:16	DIV_MAX_COUNT	clock root5 div max count. NOT-USED Reset State: 0x00000000
15:13	SRC1_SEL	clock root5 src1 sel. This field selects the output of the clock source MUX for SRC1. 000 : XO(19.2M) 001 : Riva PLL (480MHz) 010 : spare0 src 011 : 0 100 : 0 101 : 0 110 : core_bi_clk_test_se 111 : core_bi_pll_test_se Reset State: 0x00000001
12:9	SRC1_DIV	clock root5 src1 div. This field selects to activate or bypass the modulo divider for SRC1 0000 : Bypass 0001 : Div-2 0010 : Div-3 0011 : Div-4 0100 : Div-5 0101 : Div-6 0110 : Div-7 0111 : Div-8 1000 : Div-9 1001 : Div-10 1010 : Div-11 1011 : Div-12 1100 : Div-13 1101 : Div-14 1110 : Div-15 1111 : Div-16 Reset State: 0x0000000E
8:6	SRC0_SEL	clock root5 src0 sel. This field selects the output of the clock source MUX for SRC0. 000 : XO(19.2M) 001 : Riva PLL (480MHz) 010 : spare0 src 011 : 0 100 : 0 101 : 0 110 : core_bi_clk_test_se 111 : core_bi_pll_test_se Reset State: 0x00000000
5:2	SRC0_DIV	clock root5 src0 div. This field selects to activate or bypass the modulo divider for SRC0 0000 : Bypass 0001 : Div-2 0010 : Div-3 0011 : Div-4 0100 : Div-5 0101 : Div-6 0110 : Div-7 0111 : Div-8 1000 : Div-9 1001 : Div-10 1010 : Div-11 1011 : Div-12 1100 : Div-13 1101 : Div-14 1110 : Div-15 1111 : Div-16 Reset State: 0x00000000
0	CLK_ENA	clock root5 enable. Enable clock source for Riva Root5 clk ctrl 1: Enable 0: Disable Reset State: 0x00000001

0x3000084 PMU_CLK_ROOT6

Type: read-write
Reset State: 0x00042801

clock root6 control

PMU_CLK_ROOT6

Bits	Name	Description
19:16	DIV_MAX_COUNT	clock root6 div max count. Reset State: 0x00000004
15:13	SRC1_SEL	clock root6 src1 sel. This field selects the output of the clock source MUX for SRC1. 000 : XO(19.2M) 001 : clk DIV o/p,96Mhz 010 : spare0 src 011 : 0 100 : 0 101 : 0 110 : core_bi_clk_test_se 111 : core_bi_pll_test_se Reset State: 0x00000001
12:9	SRC1_DIV	clock root6 src1 div. This field selects to activate or bypass the modulo divider for SRC1 0000 : Bypass 0001 : Div-2 0010 : Div-3 0011 : Div-4 0100 : Div-5 0101 : Div-6 0110 : Div-7 0111 : Div-8 1000 : Div-9 1001 : Div-10 1010 : Div-11 1011 : Div-12 1100 : Div-13 1101 : Div-14 1110 : Div-15 1111 : Div-16 Reset State: 0x00000004
8:6	SRC0_SEL	clock root6 src0 sel. This field selects the output of the clock source MUX for SRC0. 000 : XO(19.2M) 001 : clk DIV o/p,96Mhz 010 : spare0 src 011 : 0 100 : 0 101 : 0 110 : core_bi_clk_test_se 111 : core_bi_pll_test_se Reset State: 0x00000000
5:2	SRC0_DIV	clock root6 src0 div. This field selects to activate or bypass the modulo divider for SRC0 0000 : Bypass 0001 : Div-2 0010 : Div-3 0011 : Div-4 0100 : Div-5 0101 : Div-6 0110 : Div-7 0111 : Div-8 1000 : Div-9 1001 : Div-10 1010 : Div-11 1011 : Div-12 1100 : Div-13 1101 : Div-14 1110 : Div-15 1111 : Div-16 Reset State: 0x00000000
0	CLK_ENA	clock root6 enable. Enable clock source for Riva Root6 clk ctrl 1: Enable 0: Disable Reset State: 0x00000001

0x3000088 PMU_PHY_MEM_ACC

Type: read-write
Reset State: 0x00000000

acc to PHY memories

PMU_PHY_MEM_ACC

Bits	Name	Description
31:0	ACC	acc to PHY memories Reset State: 0x00000000

0x300008C PMU_WMAC_MEM_ACC

Type: read-write
Reset State: 0x00000000

acc to WMAC memories

PMU_WMAC_MEM_ACC

Bits	Name	Description
31:0	ACC	acc to WMAC memories Reset State: 0x00000000

0x3000090 PMU_CCPU_MEM_ACC

Type: read-write
Reset State: 0x00000000

acc to CCPU memories

PMU_CCPU_MEM_ACC

Bits	Name	Description
31:0	ACC	acc to CCPU memories Reset State: 0x00000000

0x3000094 PMU_COMMON_MEM_ACC

Type: read-write
Reset State: 0x00000000

acc to common memories

PMU_COMMON_MEM_ACC

Bits	Name	Description
31:0	ACC	acc to common memories Reset State: 0x00000000

0x3000098 PMU_WMAC_CSR

Type: read-write
Reset State: 0x00000600

control and status to WMAC modules

PMU_WMAC_CSR

Bits	Name	Description
31:24	RXP_RSSI_ANT1	RXP rssi ant1 Reset State: 0x00000000
23:16	RXP_RSSI_ANT0	RXP rssi ant0 Reset State: 0x00000000
10	MTU_TSF_TIMER_EN_SYNC	TSF timer enable synchronized to the rising edge of sleep clock and synchronized back to AHB clock. TSF timer will be enabled using this signal. Reset State: 0x00000001
9	MTU_TSF_TIMER_EN	TSF timer enable for TSF timer restoration. This signal will be synchronized to the rising edge of sleep clock and synchronized back to AHB clock to actually enable TSF timer. Reset State: 0x00000001
8:7	RXP_WAKEUP_REASON	RXP wake up reason. May need to move it to common SS. Reset State: 0x00000000
4	TPE_CONSIDER_PWRON_BT	TPE consider power on BT Reset State: 0x00000000
3	MCU_QTA_VALID	MCU qta_valid Reset State: 0x00000000
2	MCU_QTA_SEL	MCU qta_sel Reset State: 0x00000000
1	MCU_GAS_CLKGATE_DISABLE	clock gate disable to MCU GAS Reset State: 0x00000000
0	MCU_CLKGATE_DISABLE	clock gate disable to MCU Reset State: 0x00000000

0x300009C PMU_CCPU_CTL

Type: read-write
Reset State: 0x00000000

This register represents Controls for CCPU.

PMU_CCPU_CTL

Bits	Name	Description
8:5	CCPU_TEST_SEL	To select ccpu testbus. Reset State: 0x00000000

PMU_CCPU_CTL (cont.)

Bits	Name	Description
4	CCPU_STANDBYWFI	The status standby wfi signal from arm9. Reset State: 0x00000000
2	CCPU_REMAP_EN	Set to '1' to enable the boot address region to be re-mapped to a different 64K region in the memory map specified in ccpu_remap_addr reg. Reset State: 0x00000000
1	CCPU_INSERT_WAIT_FOR_INTERRUPT_CMD_EN	When set, cCPU logic returns a "wait for interrupt" command at boot address. Reset State: 0x00000000
0	CCPU_HIGH_INTERRUPT_VECTOR_EN	0x1: When set, cCPU fetches instructions from 0xFFFF_0000 0: When clear, cCPU fetches instructions from 0x0 Reset State: 0x00000000

0x30000A0 PMU_CCPU_BOOT_REMAP_ADDR

Type: read-write
Reset State: 0x00000000

The base address for memory re-map the 64K boot address region.

PMU_CCPU_BOOT_REMAP_ADDR

Bits	Name	Description
15:0	CCPU_BOOT_REMAP_ADDR	Base address of the 64K boot window onto the DAHB. Reset State: 0x00000000

0x30000A4 PMU_COMMON_CSR

Type: read-write
Reset State: 0x00003332

This register controls clock and soft reset of common SS and Riva top

PMU_COMMON_CSR

Bits	Name	Description
14	M2VMT_SOFT_RESET	soft reset to M2vMT module Reset State: 0x00000000
13	M2VMT_ROOT_CLK_ENABLE	root clock enable to M2vMT module Reset State: 0x00000001

PMU_COMMON_CSR (cont.)

Bits	Name	Description
12	M2VMT_CLKGATE_DISABLE	clock gate disable to M2vMT module Reset State: 0x00000001
10	ECAHB_SOFT_RESET	soft reset to ECAHB module Reset State: 0x00000000
9	ECAHB_ROOT_CLK_ENABLE	root clock enable to ECAHB module Reset State: 0x00000001
8	ECAHB_CLKGATE_DISABLE	clock gate disable to ECAHB module Reset State: 0x00000001
6	APU_SOFT_RESET	soft reset to APU module Reset State: 0x00000000
5	APU_ROOT_CLK_ENABLE	root clock enable to APU module Reset State: 0x00000001
4	APU_CLKGATE_DISABLE	clock gate disable to APU module Reset State: 0x00000001
2	CRCM_CCU_SOFT_RESET	soft reset to CCU module Reset State: 0x00000000
1	CRCM_CCU_ROOT_CLK_ENABLE	root clock enable to CCU module Reset State: 0x00000001
0	CCU_CLKGATE_DISABLE	clock gate disable to CCU module Reset State: 0x00000000

0x30000A8 PMU_TESTBUS_CTL

Type: read-write
Reset State: 0x00000000

testbus control register

PMU_TESTBUS_CTL

Bits	Name	Description
7:4	AHB_TESTBUS_SEL	testbus selection mux for ahb clock Reset State: 0x00000000
3:0	TCXO_TESTBUS_SEL	testbus selection mux for tcxo clock [3] is treated as enable Reset State: 0x00000000

0x30000AC PMU_TESTBUS_STS

Type: read-only
Reset State: 0x00000000

testbus status register

PMU_TESTBUS_STS

Bits	Name	Description
31:0	TESTBUS_STS	testbus status Reset State: 0x00000000

0x30000B0 PMU_SPARE_IN

Type: read-only
Reset State: 0x00000000

spare in register

PMU_SPARE_IN

Bits	Name	Description
31:0	SPARE_IN	spare input. This captures the riva_test_bus. Since the test bus is async, it may not reflect the actual state of the test bus Reset State: 0x00000000

0x30000B4 PMU_SPARE_OUT

Type: read-write
Reset State: 0x00000000

spare out register

PMU_SPARE_OUT

Bits	Name	Description
31	TESTBUS_FLOP_ENABLE	Enable for test_bus_flopped_stage Reset State: 0x00000000
30:22	SPARE_OUT_30_22	spare out Reset State: 0x00000000

PMU_SPARE_OUT (cont.)

Bits	Name	Description
21	RPM_RIVA_IRQ_CLR	Writing '1' will clear rpm to riva interrupts (rpm_riva_wakeup_irq, rpm_riva_gp_low_irq, rpm_riva_gp_medium_irq, rpm_riva_gp_high_irq) sticky bits. software should toggle this bit to clear the interrupts before going to powerdown. Reset State: 0x00000000
20	SYS_SPM_WAKE_CLR	Writing '1' will clear sys_spm_wakeup sticky bit to SAW2. software should toggle this bit to clear the sticky bit before going to powerdown. Reset State: 0x00000000
19	SPARE_OUT_19	spare out Reset State: 0x00000000
18:0	TESTMODE_SEL	[18] testbus30_31_on_etm_sel [17] testbus_on_etm_sel [16] sw_sel_ccpu_stretch_rst_odd [15:14] common_ss_testbus_sel [13] ext_powersave_en [12] test_wmac_ahb_mode [11:8] sw_ls_clk_debug_sel [7:4] sw_hs_clk_debug_sel [3:0] test_mode Reset State: 0x00000000

0x30000B8 PMU_A2XB_CFG

Type: read-write
Reset State: 0x00000000

A2XB config register

PMU_A2XB_CFG

Bits	Name	Description
0	A2XB_CFG_EN	Set to enable A2XB bridge Reset State: 0x00000000

0x30000BC PMU_ACPU_WAKEUP_INT_EN

Type: read-write
Reset State: 0x00000000

The interrupt enables for generating acpu wakeup interrupt; acpu_riva_wakeup_irq

PMU_ACPU_WAKEUP_INT_EN

Bits	Name	Description
12	CPSS_RIVA_INT_ENABLE	When set, cpss_riva_int will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000

PMU_ACPU_WAKEUP_INT_EN (cont.)

Bits	Name	Description
11	PMIC_RIVA_INT_ENABLE	When set, pmic_riva_int will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000
10	TLMM_RIVA_INT_ENABLE	When set, i_tlmm_riva_int will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000
9	LPASS_RIVA_INT_ENABLE	When set, lpass_riva_int will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000
8	MSS_RIVA_INT_ENABLE	When set, mss_riva_int will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000
7	APPS_RIVA_WLAN_CTRL_ENABLE	When set, i_apps_riva_wlan_ctrl will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000
6	APPS_RIVA_HCI_ENABLE	When set, i_apps_riva_hci will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000
5	APPS_RIVA_FM_CTRL_ENABLE	When set, i_apps_riva_fm_ctrl will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000
4	APPS_RIVA_LOG_CTRL_ENABLE	When set, i_apps_riva_log_ctrl will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000
3	APPS_RIVA_WLAN_SMSM_IRQ_ENABLE	When set, i_apps_riva_wlan_smsm_irq will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000
2	APSS_RIVA_RESET_REQ_ENABLE	When set, i_apss_riva_reset_req will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000
1	APPS_RIVA_SPARE_INTR_ENABLE	When set, i_apps_riva_spare_intr will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000
0	APPS_RIVA_LTECOEX_INTR_ENABLE	When set, i_apps_riva_ltecoex_intr will set acpu_riva_wakeup_irq interrupt. Reset State: 0x00000000

0x30000C0 PMU_ACPU_WAKEUP_INT_STS

Type: read-only
Reset State: 0x00000000

The (enable masked) status of all inputs generating acpu_riva_wakeup_irq interrupt; This is sticky status until cleared; Read-Only

PMU_ACPU_WAKEUP_INT_STS

Bits	Name	Description
12	CPSS_RIVA_INT_STATUS	When set, it indicates that the cpss_riva_int caused the acpu_riva_wakeup_irq. Reset State: 0x00000000
11	PMIC_RIVA_INT_STATUS	When set, it indicates that the pmic_riva_int caused the acpu_riva_wakeup_irq. Reset State: 0x00000000
10	TLMM_RIVA_INT_STATUS	When set, it indicates that the tlmm_riva_int caused the acpu_riva_wakeup_irq. Reset State: 0x00000000
9	LPASS_RIVA_INT_STATUS	When set, it indicates that the lpass_riva_int caused the acpu_riva_wakeup_irq. Reset State: 0x00000000
8	MSS_RIVA_INT_STATUS	When set, it indicates that the mss_riva_int caused the acpu_riva_wakeup_irq. Reset State: 0x00000000
7	APPS_RIVA_WLAN_CTRL_STATUS	When set, it indicates that the i_apps_riva_wlan_ctrl caused the acpu_riva_wakeup_irq. Reset State: 0x00000000
6	APPS_RIVA_HCI_STATUS	When set, it indicates that the i_apps_riva_hci caused the acpu_riva_wakeup_irq. Reset State: 0x00000000
5	APPS_RIVA_FM_CTRL_STATUS	When set, it indicates that the i_apps_riva_fm_ctrl caused the acpu_riva_wakeup_irq. Reset State: 0x00000000
4	APPS_RIVA_LOG_CTRL_STATUS	When set, it indicates that the i_apps_riva_log_ctrl caused the acpu_riva_wakeup_irq. Reset State: 0x00000000
3	APPS_RIVA_WLAN_SMSM_IRQ_STATUS	When set, it indicates that the i_apps_riva_wlan_smsm_irq caused the acpu_riva_wakeup_irq. Reset State: 0x00000000
2	APSS_RIVA_RESET_REQ_STATUS	When set, it indicates that the i_apss_riva_reset_req caused the acpu_riva_wakeup_irq. Reset State: 0x00000000
1	APPS_RIVA_SPARE_INTR_STATUS	When set, it indicates that the i_apps_riva_spare_intr caused the acpu_riva_wakeup_irq. Reset State: 0x00000000
0	APPS_RIVA_LTECOEX_INTR_STATUS	When set, it indicates that the i_apps_riva_ltecoex_intr caused the acpu_riva_wakeup_irq. Reset State: 0x00000000

0x30000C4 PMU_ACPU_WAKEUP_INT_CLR

Type: write-only
Reset State: 0x00000000

This register clears the bits in status register acpu_wakeup_int_sts; Write-Only

PMU_ACPU_WAKEUP_INT_CLR

Bits	Name	Description
12	CPSS_RIVA_INT_CLR	When set, it clears the cpss_riva_int status; Self-clearing bit. Reset State: 0x00000000
11	PMIC_RIVA_INT_CLR	When set, it clears the pmic_riva_int status; Self-clearing bit. Reset State: 0x00000000
10	TLMM_RIVA_INT_CLR	When set, it clears the tlmm_riva_int status; Self-clearing bit. Reset State: 0x00000000
9	LPASS_RIVA_INT_CLR	When set, it clears the lpass_riva_int status; Self-clearing bit. Reset State: 0x00000000
8	MSS_RIVA_INT_CLR	When set, it clears the mss_riva_int status; Self-clearing bit. Reset State: 0x00000000
7	APPS_RIVA_WLAN_CTRL_CLR	When set, it clears the i_apps_riva_wlan_ctrl status; Self-clearing bit. Reset State: 0x00000000
6	APPS_RIVA_HCI_CLR	When set, it clears the i_apps_riva_hci status; Self-clearing bit. Reset State: 0x00000000
5	APPS_RIVA_FM_CTRL_CLR	When set, it clears the i_apps_riva_fm_ctrl status; Self-clearing bit. Reset State: 0x00000000
4	APPS_RIVA_LOG_CTRL_CLR	When set, it clears the i_apps_riva_log_ctrl status; Self-clearing bit. Reset State: 0x00000000
3	APPS_RIVA_WLAN_SMSM_IRQ_CLR	When set, it clears the i_apps_riva_wlan_smsm_irq status; Self-clearing bit. Reset State: 0x00000000
2	APSS_RIVA_RESET_REQ_CLR	When set, it clears the i_apss_riva_reset_req status; Self-clearing bit. Reset State: 0x00000000
1	APPS_RIVA_SPARE_INTR_CLR	When set, it clears the i_apps_riva_spare_intr status; Self-clearing bit. Reset State: 0x00000000
0	APPS_RIVA_LTECOEX_INTR_CLR	When set, it clears the i_apps_riva_ltecoex_intr status; Self-clearing bit. Reset State: 0x00000000

0x30000C8 PMU_ROOT_CLK_OUT_SEL

Type: read-write
Reset State: 0x00000000

Root clock sel control

PMU_ROOT_CLK_OUT_SEL

Bits	Name	Description
5	ROOT6_CLK_OUT_SEL	clock root6 out_sel. This bit selects which internal divider provides the source to the Riva root6 clock tree 0: src0 branch is selected 1: src1 branch is selected Reset State: 0x00000000
4	ROOT5_CLK_OUT_SEL	clock root5 out_sel. This bit selects which internal divider provides the source to the Riva root5 clock tree 0: src0 branch is selected 1: src1 branch is selected Reset State: 0x00000000
3	ROOT4_CLK_OUT_SEL	clock root4 out_sel. This bit selects which internal divider provides the source to the Riva root4 clock tree 0: src0 branch is selected 1: src1 branch is selected Reset State: 0x00000000
2	ROOT3_CLK_OUT_SEL	clock root3 out_sel. This bit selects which internal divider provides the source to the Riva root3 clock tree 0: src0 branch is selected 1: src1 branch is selected Reset State: 0x00000000
1	ROOT2_CLK_OUT_SEL	clock root2 out_sel. This bit selects which internal divider provides the source to the Riva root2 clock tree 0: src0 branch is selected 1: src1 branch is selected Reset State: 0x00000000
0	ROOT1_CLK_OUT_SEL	clock root1 out_sel. This bit selects which internal divider provides the source to the Riva root1 clock tree 0: src0 branch is selected 1: src1 branch is selected Reset State: 0x00000000

0x30000CC PMU_WLAN_POWER_MEASURE_MASK

Type: read-write
Reset State: 0x00000000

wlan_power_measure_mask control: Used to generate a masked vector

PMU_WLAN_POWER_MEASURE_MASK

Bits	Name	Description
4:0	WLAN_POWER_MEASURE_MASK	bit mask for wlan_power_tbusl Reset State: 0x00000000

0x30000D0 PMU_WLAN_POWER_MEASURE_MATCH

Type: read-write
Reset State: 0x00000000

wlan_power_measure_match control: Used to compare the masked vector with a programmable vector and derive a trigger

PMU_WLAN_POWER_MEASURE_MATCH

Bits	Name	Description
4:0	WLAN_POWER_MEASURE_MATCH	bit match for wlan_power_tbusl Reset State: 0x00000000

16.2.34 riva_saw2

0x3000000 RIVA_SAW2_SAW2_SECURE

Type: read-write
Reset State: 0x00000000

The SAW2_SECURE register is used to enable or disable non-secure bus transactions. The bus security status is signaled by ahb_saw_hprotns pin. When ahb_saw_hprotns is set to '0' the state of the SAW2_SECURE register is not considered - a secure transaction is always allowed. When ahb_saw_hprotns is set to '1' the SAW2_SECURE register security treatment bit of that register must be '1' for access to be granted. If the security treatment bit of the register is set to '0' the non-secure (ahb_saw_hprotns = '1') transactions are denied. When access is denied, a write is ignored, and a read will return '0'. No error is signaled. When reading the SAW2_SECURE register, non-secure agents will always read '0' Secure agents will see the actual value of the register. The reset value is controlled by CFGNSINIT input pin.

RIVA_SAW2_SAW2_SECURE

Bits	Name	Description
2	SAW_CTL	0x1: NSEC 0: SEC Controls security treatment for the AVS. registers: SAW2_AVS_CTL, SAW2_VLVL Reset State: 0x00000000

RIVA_SAW2_SAW2_SECURE (cont.)

Bits	Name	Description
1	PWR_CTL	0x1: NSEC 0: SEC Controls security treatment for SPM registers: SAW2_SPM_CTL,SAW2_SPM_PMIC_CTL, SAW2_SPM_PMIC_DLY,SAW2_SPM_SLP_SEQ_ENTRY_n Reset State: 0x00000000
0	VLT_CTL	0x1: NSEC 0: SEC Controls security treatment for SAW2 registers: SAW2_TMR_CFG,SAW2_STS Reset State: 0x00000000

0x3000004 RIVA_SAW2_SAW2_ID

Type: read-only
Reset State: 0x40910000

This read only register reports the revision and parameter information for the SAW2 core.

RIVA_SAW2_SAW2_ID

Bits	Name	Description
30:25	NUM_SPM_ENTRY	SAW2 parameter: Indicates number of SAW2_SPM_SLP_SEQ_ENTRY register implemented. Value can range from 1 - 32 Reset State: 0x00000020
24:20	NUM_PWR_CTL	SAW2 parameter: Indicates number of power control implemented. Value can range from 2 - 16 Reset State: 0x00000009
18	PMIC_ARB_INTF	SAW2 parameter: Indicates PMIC Arbiter Interface function is implemented Reset State: 0x00000000
17	AVS_PRESENT	SAW2 parameter: Indicates AVS. function is implemented Reset State: 0x00000000
16	SPM_PRESENT	SAW2 parameter: Indicates SPM function is implemented Reset State: 0x00000001
7:4	MAJOR	Major variant Reset State: 0x00000000
3:0	MINOR	Minor variant Reset State: 0x00000000

0x3000008 RIVA_SAW2_SAW2_CFG

Type: read-write
Reset State: 0x00000000

The SAW2_CFG register is used to configure the common control between AVS. and SPM.system.

RIVA_SAW2_SAW2_CFG

Bits	Name	Description
12	FRC_REF_CLK_ON	Chicken bit to force saw_sys_ref_clk_on_req ON. Reset State: 0x00000000
11:8	ADR_IDX	PMIC Arbiter Address Index. Drive the saw_pmic_addr_idx output port. Reset State: 0x00000000
5	PMIC_MODE	PMIC Handshake 0: 8K_PMIC (only DONE signal) 1: 7K_PMIC (both ACK and DONE signals) Reset State: 0x00000000
4:0	CLK_DIV	Divider ratio for clock. This is used to generate timer tick for the timer. Timer tick is asserted every (CLK_DIV + 1) sys_ref_clk period. 00000: Timer Tick every sys_ref_clk ..... 11111: Timer Tick every 128 sys_ref_clk. For sys_ref_clk = 20 MHz (53ns) The timer tick range 53 ns to 1.6us. Reset State: 0x00000000

0x300000C RIVA_SAW2_SAW2_STS_0

Type: read-only
Reset State: 0x00000000

This read only register provides software with SAW2 status.

RIVA_SAW2_SAW2_STS_0

Bits	Name	Description
31:27	SPM_STATE	Actual initial value is 'x'. State of the SPM FSM. Reset State: 0x00000000
24:16	CURR_PWR_CTL	Power Control Outputs. Reset State: 0x00000000
15	SHTDWN_REQ	This bit reflects the shutdown request from the SPM (spm_rpm_shutdown_req) to RPM. Reset State: 0x00000000
14	SHTDWN_ACK	This bit reflects the shutdown acknowledgement from the RPM (rpm_spm_shutdown_ack) to SPM. Reset State: 0x00000000
13	BRNGUP_REQ	This bit reflects the bringup request from the SPM (spm_rpm_bringup_req) to RPM. Reset State: 0x00000000

RIVA_SAW2_SAW2_STS_0 (cont.)

Bits	Name	Description
11:10	PMIC_STATE	State of the PMIC FSM: 00: IDLE (waiting for PMIC transaction from AVS. or SPM) 01: ACK (waiting for ACK from PMIC Arb) 10: DONE (waiting for DONE form PMIC Arb before transitions back to IDLE) 11: DELAY (waiting for delay count termination before transitions back to IDLE) This bit reflects the bringup acknowledgement from the RPM (rpm_spm_bringup_ack) to SPM. Reset State: 0x00000000
9:8	RPM_STATE	State of the RPM FSM: 00: RUN (waiting for SPM request) 01: STDNACK (waiting for shutdown ACK from RPM) 10: WAKEUP (waiting for wakeup interrupt) 11: BGUPACK (waiting for bringup ACK from RPM) Reset State: 0x00000000
7	AVS_STATE	State of the AVS. FSM: 0: IDLE (waiting to be enabled or for next UP/DOWN indication) 1: REQ (waiting for PMIC FSM to transition to IDLE) Reset State: 0x00000000
6:0	SPM_CMD_ADDR	Last SPM command executed. Reset State: 0x00000000

0x3000010 RIVA_SAW2_SAW2_STS_1

Type: read-only
Reset State: 0x00000000

This read only register provides software with SAW2 status.

RIVA_SAW2_SAW2_STS_1

Bits	Name	Description
30	SW_WR_PEND	Actual initial value is 'x'. This bit reflects the VLVL state of the request from the SAW2_VCTL write is pending. Reset State: 0x00000000
29	CPU_UP	Actual initial value is 'x'. This bit reflects the VLVL state of the request from the CPU (avs_saw_up) to raise the VLVL. Reset State: 0x00000000
28	CPU_DN	Actual initial value is 'x'. This bit reflects the VLVL state of the request from the CPU (avs_saw_down) to lower the VLVL. Reset State: 0x00000000

RIVA_SAW2_SAW2_STS_1 (cont.)

Bits	Name	Description
27	MAX_INT	Actual initial value is 'x'. IRQ status bit, AVS. controller detected that raising the VLVL by AVS_CTL[VLVL_STEP] would result in a value greater than AVS_CTL[MAX_VLVL]. If AVS_CTL[IRQ_MAX_EN] is set, an interrupt is issued. NOTE that software can set MAX_VLVL lower than current VLVL creating a condition where VLVL is higher than MAX_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MAX. Reset State: 0x00000000
26	MIN_INT	Actual initial value is 'x'. IRQ status bit, AVS. controller detected that lowering the VLVL by SAW2_AVS_CTL[VLVL_STEP] would result in a value less than SAW2_AVS_CTL[MIN_VLVL]. If SAW2_AVS_CTL[IRQ_MIN_EN] is set, an interrupt is issued. NOTE that software can set MIN_VLVL higher than current VLVL creating a condition where VLVL is lower than MIN_VLVL. The AVS. controller can not correct VLVL. However, this condition will set IRQ_MIN. Reset State: 0x00000000
25:16	CURR_DLY	VLVL value of the counter used to calculate the time until the next AVS. controller request for a new VLVL. Reset State: 0x00000000
7:0	CURR_PMIC_DATA	Actual initial value is 'x'. Last PMIC DATA sent to the PMIC Arbiter (and the PMIC). Reset State: 0x00000000

0x3000014 RIVA_SAW2_SAW2_VCTL

Type: read-write
Reset State: 0x00000000

Though this register is read/writable, it also causes a command pulse to the PMIC FSM. Writing this register results in a transaction to the PMIC with SAW2_VCTL being sent to the PMIC. SAW2 support both 8901 and 8058 regulator.

RIVA_SAW2_SAW2_VCTL

Bits	Name	Description
7:0	PMIC_DATA	Actual initial value is 'x'. PMIC DATA sent to the PMIC Arbiter Reset State: 0x00000000

0x3000018 RIVA_SAW2_SAW2_AVS_CTL

Type: read-write
Reset State: 0x00000000

The SAW2_AVS_CTL register is used to control the Adaptive Voltage Scaling (AVS) system. Not used for Riva.

RIVA_SAW2_SAW2_AVS_CTL

Bits	Name	Description
30	VLVL_WIDTH	Defines the VLVL field of PMIC data. SAW2 at minimum supports 8901 and 8058 regulator. See PMIC document for details. 0: 5 bits VLVL (8058 regulator) 1: 6 bits VLVL (8901 regulator) Reset State: 0x00000000
29:28	VLVL_STEP	Controls the step size of each request to PMIC Arbiter. software may use values from 0 to 3. Note that the value 0 will result in no change - that is if the CPU requests UP or DOWN, the CURR_PVLVL will be sent to the PMIC Arbiter. This may be useful for debug. If an increment or decrement operation would cause the current VLVL to transition above or below the MAX_VLVL or MIN_VLVL, the current VLVL will not be changed. An interrupt will be signaled if IRQ_MAX/MIN_EN is 1 Reset State: 0x00000000
27	EN	AVS. Enable. 0: Disable AVS. 1: Enable AVS. NOTE: setting to 0 does not disable any pending interrupts. NOTE: AVS. FSM and SPM FSM are mutually exclusive. Only one FSM is active at a time. software does not have to disable AVS. before going to sleep. Reset State: 0x00000000
26	SW_DONE_INT_EN	Set to 1 to turn on AVS. interrupt for when a software initiated voltage change has completed. Set to 0 to mask it (turn it off). ASSERTION: This interrupt is asserted only after a software write to SAW2_AVS_VLVL. Specifically, after the AVS. FSM traverses through all its states and transitions back to IDLE, the interrupt line is pulsed. The interrupt controller should be set to edge capture to receive this interrupt. CLEARING: None. This interrupt is a pulse, software does not need to clear it (aside from requirements of the interrupt controller). Reset State: 0x00000000
25	MAX_INT_EN	Set to 1 to turn on AVS. interrupt for MAX_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be greater than MAX_VLVL. CLEARING: software may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit. Reset State: 0x00000000
24	MIN_INT_EN	Set to 1 to turn on AVS. interrupt for MIN_VLVL. Set to 0 to disable interrupt. ASSERTION: When on, the AVS. Controller interrupts the processor when a new VLVL would be smaller than MIN_VLVL. CLEARING: software may cause this interrupt to de-assert by a. changing the MAX_VLVL or b. changing AVS_VLVL, or c. disabling the interrupt with this bit Reset State: 0x00000000

RIVA_SAW2_SAW2_AVS_CTL (cont.)

Bits	Name	Description
22:17	MAX_VLVL	Control maximum value of AVS. controller's VLVL. When current VLVL reaches this value it may not grow any larger. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level higher, an interrupt is issued. This value may be updated at anytime. Setting to a value lower than MIN_VLVL is not supported, and unpredictable results may occur. Reset State: 0x00000000
15:10	MIN_VLVL	Control the minimum value of AVS. controller's VLVL. When the current VLVL reaches this level it may not shrink any smaller. If IRQ_EN is set to 1 and the AVS. controller needs to raise the level lower, an interrupt is issued. This value may be updated at anytime. Setting to a value higher than MAX_VLVL is not supported, and unpredictable results may occur. Reset State: 0x00000000
9:0	AVS_DELAY	Control the time between AVS. controller's requests to change the VLVL Reset State: 0x00000000

0x300001C RIVA_SAW2_SAW2_AVS_HYSTERESIS

Type: read-write
Reset State: 0x00000000

The SAW2_AVS_HYSTERESIS register is used to delay the AVS. UP/DN signal to AVS. FSM. This is used to prevent the false PMIC step due to PDN noise.

RIVA_SAW2_SAW2_AVS_HYSTERESIS

Bits	Name	Description
23:16	DN_COUNT	HYSTERESIS DN COUNT. Delays of PMIC DN step operation. Reset State: 0x00000000
7:0	UP_COUNT	HYSTERESIS UP COUNT. Delays of PMIC UP step operation. Reset State: 0x00000000

0x3000020 RIVA_SAW2_SAW2_SPM_CTL

Type: read-write
Reset State: 0x00000000

The SAW2_SPM_CTL register is used to control the subsystem power management system. This are parameters that controls the operation of SPM FSM.

RIVA_SAW2_SAW2_SPM_CTL

Bits	Name	Description
10:4	SPM_START_ADR	Start address for the SPM sequence. Reset State: 0x00000000
3	ISAR	Inhibit Start Address Reset 0: End of program reset the SPM_START_ADR to zero. 1: Inhibit End of program to reset SPM_START_ADR Reset State: 0x00000000
2:1	WAKEUP_CONFIG	Wakeup Configuration 00: sys_spm_wakeup 01: sys_spm_wakeup or !cpu_spm_wait_req 10: sys_spm_wakeup or rising edge of sys_saw_dbg_stay_awake 11: sys_spm_wakeup or !cpu_spm_wait_req or rising edge of sys_saw_dbg_stay_awake Reset State: 0x00000000
0	SPM_EN	SPM En. Reset State: 0x00000000

0x3000024 RIVA_SAW2_SAW2_SPM_PMIC_DLY

Type: read-write
Reset State: 0x00000000

This register provide the PMIC delay values after SPM FSM PMIC transaction. SPM wait for the programmed delay before executing the next SPM command.

RIVA_SAW2_SAW2_SPM_PMIC_DLY

Bits	Name	Description
26:24	DATA_1_VLVL1_DLY	Actual initial value is 'x'. PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms Reset State: 0x00000000
18:16	DATA_1_VLVL0_DLY	Actual initial value is 'x'. PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_1[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms Reset State: 0x00000000
10:8	DATA_0_VLVL1_DLY	Actual initial value is 'x'. PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL1] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms Reset State: 0x00000000

RIVA_SAW2_SAW2_SPM_PMIC_DLY (cont.)

Bits	Name	Description
2:0	DATA_0_VLVL0_DLY	Actual initial value is 'x'. PMIC Delay. Controls the time between SPM_SLP_SEQ PMIC command with SAW2_SPM_PMIC_DATA_0[VLVL0] and the next SPM_SLP_SEQ command. Time range: 13.33us to 1.7ms Reset State: 0x00000000

0x3000028 RIVA_SAW2_SAW2_SPM_PMIC_DATA_0

Type: read-write
Reset State: 0x00000000

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

RIVA_SAW2_SAW2_SPM_PMIC_DATA_0

Bits	Name	Description
31:16	VLVL1	Actual initial value is 'x'. Actual configurable bit width is $PMIC_DATA_WIDTH+15:16. PMIC DATA sent to the PMIC Arbiter Reset State: 0x00000000
15:0	VLVL0	Actual initial value is 'x'. Actual configurable bit width is $PMIC_DATA_WIDTH-1:0. PMIC DATA sent to the PMIC Arbiter Reset State: 0x00000000

0x300002C RIVA_SAW2_SAW2_SPM_PMIC_DATA_1

Type: read-write
Reset State: 0x00000000

This register provide the PMIC data values for SPM FSM PMIC transaction. Refer to PMIC documentation for the detail definition.

RIVA_SAW2_SAW2_SPM_PMIC_DATA_1

Bits	Name	Description
31:16	VLVL1	Actual initial value is 'x'. Actual configurable bit width is $PMIC_DATA_WIDTH+15:16. PMIC DATA sent to the PMIC Arbiter Reset State: 0x00000000
15:0	VLVL0	Actual initial value is 'x'. Actual configurable bit width is $PMIC_DATA_WIDTH-1:0. PMIC DATA sent to the PMIC Arbiter Reset State: 0x00000000

0x3000030 RIVA_SAW2_SAW2_RST

Type: read-write
Reset State: 0x00000000

The SAW2_RST register is used to reset the SAW logic. This register clear itself. It does not reset any SAW2 CSRs. It reset AVS. and SPM FSM and control registers. This is use to clear any hang condition.

RIVA_SAW2_SAW2_RST

Bits	Name	Description
0	RST	Reset AVS. and SPM FSM and control registers. Reset State: 0x00000000

0x3000080+0x4*n RIVA_SAW2_SAW2_SPM_SLP_SEQ_ENTRY_n, n=[0..31]

Type: read-write
Reset State: 0x00000000

The SAW2_SPM_SLP_SEQ_ENTRY_n is an array used to sequence through the steps during various power mode. The register width is defined by CLOG_PWR_CTL parameter. n = [0..31] $clog_pwr_ctl+3:4 3:2 1 0 Command ---------- ---------- ---------- Toggle PWR_CTL bit n Dly(0,1,2,4...64) * Tick 0 Toggle Output Power control bit n X PMIC Sel 0 1 PMIC operation X 00 1 1 Sleep without RPM handshake X 01 1 1 Sleep with RPM handshake X 11 1 1 End of program

RIVA_SAW2_SAW2_SPM_SLP_SEQ_ENTRY_n

Bits	Name	Description
31:24	CMD3	Actual initial value is 'x'. SPM PWR CMD3 Reset State: 0x00000000
23:16	CMD2	Actual initial value is 'x'. SPM PWR CMD2 Reset State: 0x00000000
15:8	CMD1	Actual initial value is 'x'. SPM PWR CMD1 Reset State: 0x00000000
7:0	CMD0	Actual initial value is 'x'. SPM PWR CMD0 Reset State: 0x00000000

16.2.35 adu

0x3000000 ADU_CONTROL

Type: read-write
Reset State: 0x0BFF0002

Contains configuration information for the adu

ADU_CONTROL

Bits	Name	Description
31:24	NEXT_WQ	This field indicates the WQ that the ADU will push the frames to after they have been processed. This field is only used when 'push_wq_selection_mode' is set to '1'. Reset State: 0x0000000B
23:16	WOW_WQ	This field indicates the WQ that the ADU will push the frames during WOW mode. This field is only used when 'push_wq_selection_mode' is set to '1'. Reset State: 0x000000FF
15	REG_REINIT_ERR_STATE_CFG	When set, ADU reg reinit FSM will go back to idle instead of staying in error state. Reset State: 0x00000000
13	REG_REINIT_GOTO_IDLE	When set, ADU reg reinit FSM (BPS, MIMO) will go to idle. Reset State: 0x00000000
8	CLEAR_TIMEOUT_CNT	Writing a '1' will reset the timeout counter and clear timeout error interrupt. Always read 0. Reset State: 0x00000000
7	DISABLE_LENGTH_CHECK	When set, the ADU will not check the subframe length error Reset State: 0x00000000
6	PUSH_WQ_SELECTION_WOW_MODE	This field controls where the ADU finds the index for the WQ to which the processed frames need to be pushed to in WOW mode. This bit should be set (a 0->1 transition) prior to WOW mode to select the WOW_WQ. Upon the assertion of dpu_wakeuphost, ADU will push to the normal WQ. 0: ADU will push the frame to the WQ that is selected by the push_wq_selection_mode 1: ADU will push the frame to the WQ that is indicate in the 'WOW_ WQ' field in this register Reset State: 0x00000000
5	ADU_ERROR_EXIT	Writing a '1' will clear the interrupts and ADU will go back to IDLE from ERROR_STATE. Always read 0 Reset State: 0x00000000
4	ADU_BYPASS_OPTION_ENABLE	When set, ADU will immediately forward the frame and NOT check if the frame is AMSDU Reset State: 0x00000000

ADU_CONTROL (cont.)

Bits	Name	Description
3	CLEAR_COUNTERS	When set, the ADU packet counters are cleared To re-enable theL counters, this bit needs to be cleared again Reset State: 0x00000000
2	DISABLE_HT_FIELD_DETECTION	When set, the ADU will NOT check for the presence of the HT control field Reset State: 0x00000000
1	PUSH_WQ_SELECTION_MODE	This field controls where the ADU finds the index for the WQ to which the processed frames need to be pushed to. 0: ADU will push the frame to the WQ that is indicated in the 'ADU/DPU routing flag' in the BD descriptor. 1: ADU will push the frame to the WQ that is indicate in the 'Next WQ' field in this register Reset State: 0x00000001
0	ADU_ENABLE	When set, the ADU is enabled. When the adu gets disabled in the middle of a transfer, it will finish the ongoing transfer. Reset State: 0x00000000

0x3000004 ADU_INTERRUPT_STATUS

Type: read-only
Reset State: 0x00000000

Contains status information on what interrupt has been generated Note that the interrupt is only passed on to the mCPU when the error interrupt has been enabled in the 'ADU interrupt enable' register.

ADU_INTERRUPT_STATUS

Bits	Name	Description
15:14	RESERVED	The two bits are reserved. Reset State: 0x00000000
13	ADU_POLL_CMD_ERROR	When set, adu poll cmd reached retry timeout error occurred Reset State: 0x00000000
12	UMA_WRONG_WQ_ERROR	When set, adu uma tx push to its own WQ error occurred Reset State: 0x00000000
11	TIMEOUT_ERROR	When set, timeout error occurred Reset State: 0x00000000
10	WRONG_WQ_ERROR	When set, adu push to its own WQ error occurred Reset State: 0x00000000
9	INCORRECT_LINK_ERROR	When set, an incorrect BD/PDU link error occurred Reset State: 0x00000000

ADU_INTERRUPT_STATUS (cont.)

Bits	Name	Description
8	BAD_BD_TYPE_ERROR	When set, a bad bd type error occurred Reset State: 0x00000000
7	GAM_WRITE_ERROR	When set, a gam write error occurred Reset State: 0x00000000
6	SW_REG_REINIT_DONE	When set, the software triggered reg reinit is done Reset State: 0x00000000
5	DELIMITER_LENGTH_NOT_AVAIL_ERROR	When set, the adu was not able to extract the delimiter length from the frame Reset State: 0x00000000
4	GAM_READ_ERROR	When set, the gam reported a read error Reset State: 0x00000000
3	GBI_PUSH_ERROR	When set, the gbi reported an error while a push operation was ongoing Reset State: 0x00000000
2	MPDU_HEADER_NOT_IN_BD_ERROR	When set, the mpdu header was not located fully within the BD Reset State: 0x00000000
1	GBI_POP_ZERO_ERROR	When set, the gbi returned a NULL BD pointer when the BMU was indicating DA in its WQ. Reset State: 0x00000000
0	GBI_POP_ERROR	When set, the gbi reported an error while a pop operation was ongoing Reset State: 0x00000000

0x3000008 ADU_INTERRUPT_ENABLE

Type: read-write
Reset State: 0x00000000

Contains the enable bits for which interrupt has to be generated

ADU_INTERRUPT_ENABLE

Bits	Name	Description
15:14	ADU_RESERVED	The two bits are reserved Reset State: 0x00000000
13	ADU_POLL_CMD_ERROR_ENABLE	When set, adu poll cmd reach retry timeout error will generate error interrupt Reset State: 0x00000000
12	UMA_WRONG_WQ_ERROR_ENABLE	When set, adu uma tx push its own WQ error will generate error interrupt Reset State: 0x00000000

ADU_INTERRUPT_ENABLE (cont.)

Bits	Name	Description
11	TIMEOUT_ERROR_ENABLE	When set, timeout error will generate error interrupt Reset State: 0x00000000
10	WRONG_WQ_ERROR_ENABLE	When set, adu push its own WQ error will generate error interrupt Reset State: 0x00000000
9	INCORRECT_LINK_ERROR_ENABLE	When set, an incorrect BD/PDU link error will generate error interrupt Reset State: 0x00000000
8	BAD_BD_TYPE_ERROR_ENABLE	When set, a bad bd type error will generate error interrupt Reset State: 0x00000000
7	GAM_WRITE_ERROR_ENABLE	When set, a gam write error will generate an adu error interrupt Reset State: 0x00000000
6	SW_REG_REINIT_DONE_ENABLE	When set, when the software triggered reg reinit is done the interrupt will be generated Reset State: 0x00000000
5	DELIMITER_LENGTH_NOT_AVAIL_ERROR_ENABLE	When set, and the adu was not able to extract the delimiter length from the frame an adu error interrupt will be generated Reset State: 0x00000000
4	GAM_READ_ERROR_ENABLE	When set, and the gam reported a read error an adu error interrupt will be generated Reset State: 0x00000000
3	GBI_PUSH_ERROR_ENABLE	When set, and the gbi reported an error while a push operation was ongoing, an adu error interrupt will be generated Reset State: 0x00000000
2	MPDU_HEADER_NOT_IN_BD_ERROR_ENABLE	When set, and the mpdu header was not located fully within the BD an adu error interrupt will be generated Reset State: 0x00000000
1	GBI_POP_ZERO_ERROR_ENABLE	When set, and the gbi returned a NULL BD pointer when the BMU was indicating DA in its WQ, an adu error interrupt will be generated Reset State: 0x00000000
0	GBI_POP_ERROR_ENABLE	When set, and the gbi reported an error while a pop operation was ongoing, an adu error interrupt will be generated Reset State: 0x00000000

0x300000C ADU_ADU_TEST_CTRL

Type: read-write
Reset State: 0x00000004

Selects the test bus configuration for the ADU. Used for hardware debug only

ADU_ADU_TEST_CTRL

Bits	Name	Description
4:0	TEST_BUS_SEL	Enabled different testbusses in the ADU. 0: none 1-3: functional signals 4:gas_testbus 5:dahb_gam_testbus 6:cahb_gam_testbus 7:gbi_testbus 8-b: functional signals c-d: reinit signals e: uma_tx f: uma_rx Reset State: 0x00000004

0x3000010 ADU_ADU_STATUS

Type: read-only
Reset State: 0x00000000

Provides status information about the ADU

ADU_ADU_STATUS

Bits	Name	Description
28:24	ENCODED_ADU_REINIT_FSM	The FSM status of adu reinit Reset State: 0x00000000
23	ADU_SM_STATE_MSB	The MSB of state machine state of the ADU controller Reset State: 0x00000000
22	BMU_UMA_TX_WQ_DA	The status of the bmu_uma_tx_wq_da Reset State: 0x00000000
21	ENCODED_GAS_INTERFACE_SM_STATE	The status of the gas interface. Reset State: 0x00000000
20	UMA_TX_STATUS	The status of the uma tx. 0 means uma tx is idle Reset State: 0x00000000
19:15	UMA_TX_SM_STATE	The state machine state of the uma tx Reset State: 0x00000000
13	ADU_MULTIPLE_RX_UPDATE_ONGOING	shows the status of adu_multiple_rx_update_ongoing Reset State: 0x00000000
12:8	ADU_SM_STATE	The 5LSB of state machine state of the ADU controller Reset State: 0x00000000
5	ADU_FIXED_WQ_PUSH_MODE_WOW_ENABLED	Shows the status of adu_fixed_wq_push_mode_wow_enabled signal. It's set to 1 when control[6] is set to 1, and clear to 0 when control[6] is cleaered or when dpu_wakuphost assert Reset State: 0x00000000
4	DPU_WAKEUPHOST	Shows the status of dpu_wakuphost Reset State: 0x00000000
3	ADU_STATUS	When set, the ADU controller is NOT in it's IDLE state Reset State: 0x00000000

ADU_ADU_STATUS (cont.)

Bits	Name	Description
2	ADU_MCU_ERR_INT	shows the status of the ADU error interrupt signal going to the mcu Reset State: 0x00000000
1	DATA_AVAIL	shows the data_available signal from the bmu Reset State: 0x00000000
0	BD_PDU_AVAIL	shows the bd_pdu_avail signal from the bmu Reset State: 0x00000000

0x3000014 ADU_ADU_DEBUG0

Type: read-only
Reset State: 0x00000000

Contains error debug info

ADU_ADU_DEBUG0

Bits	Name	Description
31:16	ORIGINAL_BD_INDEX	Index of the original BD that was popped Reset State: 0x00000000
9:5	UMA_TX_ERROR_SM_STATE	The state machine state the uma tx was in when it generated an error pulse Reset State: 0x00000000
4:0	ADU_ERROR_SM_STATE	The state machine state the ADU was in when it generated an error pulse Reset State: 0x00000000

0x3000018 ADU_ADU_DEBUG1

Type: read-only
Reset State: 0x00000000

provides access to the testbus

ADU_ADU_DEBUG1

Bits	Name	Description
31:0	ADU_TESTBUS_LOW	The lowest 32 bits of the ADU testbus Reset State: 0x00000000

0x300001C ADU_ADU_DEBUG2

Type: read-only
Reset State: 0x00000000

provides access to the testbus

ADU_ADU_DEBUG2

Bits	Name	Description
12:0	ADU_TESTBUS_HIGH	Bits [44:32] of the ADU testbus Reset State: 0x00000000

0x3000020 ADU_ADU_COUNTERS1

Type: read-only
Reset State: 0x00000000

gives information on the number of frames processed

ADU_ADU_COUNTERS1

Bits	Name	Description
23:16	NUMBER_OF_AMSDU_FRAMES_PROCESSED	Indicates the number of amsdu frames processed by the ADU Reset State: 0x00000000
7:0	NUMBER_OF_FRAMES_POPPED	Indicates the number of frames that were popped by the ADU Reset State: 0x00000000

0x3000024 ADU_ADU_COUNTERS2

Type: read-only
Reset State: 0x00000000

gives information on the number of frames processed

ADU_ADU_COUNTERS2

Bits	Name	Description
23:16	NUMBER_OF_NON_AMSDU_FRAMES_PROCESSED	Indicates the number of non amsdu frames processed by the ADU Reset State: 0x00000000
7:0	NUMBER_OF_BYPASS_FRAMES_PROCESSED	Indicates the number of frames for which the 'ADU bypass' bit in the BD was set Reset State: 0x00000000

0x3000028 ADU_ADU_COUNTERS3

Type: read-only
Reset State: 0x00000000

gives information on the number of frames processed

ADU_ADU_COUNTERS3

Bits	Name	Description
23:16	NR_OF_ERROR_FRAMES	Indicates the number of error frames which has been pushed to error wq. Reset State: 0x00000000
7:0	NR_OF_MISCONFIGURED_AMSDU_FRAMES	Indicates the number of amsdu frames processed that were not correctly configured Reset State: 0x00000000

0x300002C ADU_CONTROL2

Type: read-write
Reset State: 0x03FFF92A

Contains configuration information for the adu

ADU_CONTROL2

Bits	Name	Description
31:26	SPARE_BIT	Spare register bits for ECOs Reset State: 0x00000000
25:12	TIMEOUT_CNT	This field specify the timeout value in unit of 1 us when adu fsm doesn't return to IDLE. Reset State: 0x00003FFF
11:0	MAX_LENGTH	This field specify the max subframe length is allowed. Reset State: 0x0000092A

0x3000030 ADU_TIMEOUT_READ

Type: read-only
Reset State: 0x00000000

Contains timeout counter information for the adu

ADU_TIMEOUT_READ

Bits	Name	Description
19:0	TIMEOUT_CNT_REG	This field read the timeout counter value Reset State: 0x00000000

0x300003C ADU_UMA_CONFIG

Type: read-write
Reset State: 0xA0106000

This register is to config the UMA function

ADU_UMA_CONFIG

Bits	Name	Description
31	UMA_TX_MCUSEBC_EN	When set, mc address will use bc addr for da search. Reset State: 0x00000001
30:26	UMA_TX_QID_FOR_NONQOS	The Queueid to fill the BD when the packet is non QoS frame. Reset State: 0x00000008
25	UMA_TX_EATRACT_TID	When set, uma tx extract the tid from 802.1Q/IP header. Reset State: 0x00000000
24	UMA_RX_LLC_EN	When set and bit 21 is set, enables LLC removal. Reset State: 0x00000000
23	UMA_RX_CHECKSUM_EN	When set and bit 21 is set, enables the TCP checksum validation in RX direction Reset State: 0x00000000
22	UMA_RX_FT_EN	When set and bit 21 is set, enables the frame translation in RX direction Reset State: 0x00000000
21	UMA_RX_EN	When set, enables the data path enhancement in RX direction. When clear, UMA RX simply forward the frame to the specified WQ. Reset State: 0x00000000
20	UMA_TX_PUSH_WQ_SEL	When set, UMA will push the frame to the WQ specified in bit [19:12] When clear, UMA will push the frame to the WQ specified in the routing flag in BD Reset State: 0x00000001
19:12	UMA_TX_PUSH_WQ	Specify the WQ that UMA should push to in TX direction if bit 20 is set. Reset State: 0x00000006
11:4	TX_DEFAULT_STAID	The default descriptor index used for frame translation in TX direction when there's no DA match in the srch table.. Reset State: 0x00000000

ADU_UMA_CONFIG (cont.)

Bits	Name	Description
3	UMA_TX_LLC_EN	When set and bit 0 is set, enables LLC insertion in TX direction Reset State: 0x00000000
2	UMA_TX_CHECKSUM_EN	When set and bit 0 is set, enables TCO checksum computation in TX direction Reset State: 0x00000000
1	UMA_TX_FT_EN	When set and bit 0 is set, enables frame translation in TX direction. Reset State: 0x00000000
0	UMA_TX_EN	When set, enables data path enhancement in TX direction. When clear, UMA simply forward the incoming frame to the specified WQ. Reset State: 0x00000000

0x3000040 ADU_UMA_CTRL

Type: read-write
Reset State: 0x0000FF03

This register is to control the UMA function

ADU_UMA_CTRL

Bits	Name	Description
31:24	UMA_TX_AP_WQ	The WQ UMA will push when there's no match. Reset State: 0x00000000
23:16	UMA_RX_MC_WQ	The WQ UMA will push when DA is a mc/bc address. Reset State: 0x00000000
15:8	UMA_RX_ERROR_WQ	The Error WQ UMA will forward when exception occurs, such as payload size less than 8 bytes. Reset State: 0x000000FF
7	UMA_RX_MCWQ_EN	When set, enable UMA RX push the frame to uma_rx_mc_wq when DA is a mc/bc address Reset State: 0x00000000
6	UMA_TX_APWQ_EN	When set, enable UMA TX push the frame to uma_tx_ap_wq when there's no match Reset State: 0x00000000
5	UMA_DISABLE_MIN_PAYLOAD_CHECK	When set, disable the min payload check Reset State: 0x00000000
4	UMA_COUNTER_CLEAR	Write a '1' to clear the UMA TX Counters. Always read '0'. Reset State: 0x00000000

ADU_UMA_CTRL (cont.)

Bits	Name	Description
3	UMA_TX_QID_FROM_BD	When set, UMA won't update the queue id in BD. When clear, queue id will be a 1-1 mapping from tid(QoS) or register (non-QoS) Reset State: 0x00000000
2	UMA_TX_ERROR_EXIT	Write a '1' to clear the UMA TX interrupts and UMA TX FSM goes back to IDLE. Always read '0'. Reset State: 0x00000000
1	UMA_RX_ENABLE	When set, UMA RX is enabled. When clear, UMA RX is off. adu_ctrl will push the processed frame to the specified WQ. Reset State: 0x00000001
0	UMA_TX_ENABLE	When set, UMA TX is enabled. When clear, UMA TX is off. No frame will be popped from BMU. Reset State: 0x00000001

0x3000044 ADU_UMA_DESP_TABLE_ADDR

Type: read-write
Reset State: 0x00000000

This register contains the base address of uma's descriptor table

ADU_UMA_DESP_TABLE_ADDR

Bits	Name	Description
31:0	UMA_DESP_TABLE_BASE_ADDR	Base address of UMA's descriptor table Reset State: 0x00000000

0x3000048 ADU_UMA_TX_ETHERTYPE_TABLE1

Type: read-write
Reset State: 0x00000000

This register contains 2 entries of the ethertype table for uma tx

ADU_UMA_TX_ETHERTYPE_TABLE1

Bits	Name	Description
31:16	UMA_TX_ETHERTYPE_ENTRY2	One of the entries of uma tx ethertype table Reset State: 0x00000000
15:0	UMA_TX_ETHERTYPE_ENTRY1	One of the entries of uma tx ethertype table Reset State: 0x00000000

0x300004C ADU_UMA_TX_ETHERTYPE_TABLE2

Type: read-write
Reset State: 0x00000000

This register contains 2 entries of the ethertype table for uma tx

ADU_UMA_TX_ETHERTYPE_TABLE2

Bits	Name	Description
31:16	UMA_TX_ETHERTYPE_ENTRY4	One of the entries of uma tx ethertype table Reset State: 0x00000000
15:0	UMA_TX_ETHERTYPE_ENTRY3	One of the entries of uma tx ethertype table Reset State: 0x00000000

0x3000050 ADU_UMA_RX_ETHERTYPE_TABLE1

Type: read-write
Reset State: 0x00000000

This register contains 2 entries of the ethertype table for uma rx

ADU_UMA_RX_ETHERTYPE_TABLE1

Bits	Name	Description
31:16	UMA_RX_ETHERTYPE_ENTRY2	One of the entries of uma rx ethertype table Reset State: 0x00000000
15:0	UMA_RX_ETHERTYPE_ENTRY1	One of the entries of uma rx ethertype table Reset State: 0x00000000

0x3000054 ADU_UMA_RX_ETHERTYPE_TABLE2

Type: read-write
Reset State: 0x00000000

This register contains 2 entries of the ethertype table for uma rx

ADU_UMA_RX_ETHERTYPE_TABLE2

Bits	Name	Description
31:16	UMA_RX_ETHERTYPE_ENTRY4	One of the entries of uma rx ethertype table Reset State: 0x00000000
15:0	UMA_RX_ETHERTYPE_ENTRY3	One of the entries of uma rx ethertype table Reset State: 0x00000000

0x3000058 ADU_UMA_TX_COUNTERS1

Type: read-only
Reset State: 0x00000000

This register contains counters information of uma tx

ADU_UMA_TX_COUNTERS1

Bits	Name	Description
23:16	UMA_TX_PUSHED_COUNTER	Counters of the frame uma tx pushed Reset State: 0x00000000
7:0	UMA_TX_POPPED_COUNTER	Counters of the frame uma tx popped Reset State: 0x00000000

0x300005C ADU_UMA_TX_COUNTERS2

Type: read-only
Reset State: 0x00000000

This register contains counters information of uma tx

ADU_UMA_TX_COUNTERS2

Bits	Name	Description
23:16	UMA_TX_ERROR_COUNTER	Counters of the frames forwarded to error wq by UMA TX Reset State: 0x00000000
7:0	UMA_TX_FT_COUNTER	Counters of the frame translated by uma tx Reset State: 0x00000000

0x3000060 ADU_UMA_LLC_COUNTERS

Type: read-only
Reset State: 0x00000000

This register contains counters information of uma llc insertion/removal

ADU_UMA_LLC_COUNTERS

Bits	Name	Description
23:16	UMA_RX_LLC_COUNTER	Counters of the LLC removal done by uma rx Reset State: 0x00000000
7:0	UMA_TX_LLC_COUNTER	Counters of the LLC insertion done by uma tx Reset State: 0x00000000

0x3000064 ADU_UMA_INDEX_TABLE_WDATA_U

Type: read-write
Reset State: 0x00000000

This register contains the upper bits of the entry of index table

ADU_UMA_INDEX_TABLE_WDATA_U

Bits	Name	Description
23:16	UMA_SRCHTABLE_INDEX	index (in unit of 3 words) to the descriptor table Reset State: 0x00000000
15:0	UMA_SRCHTABLE_WDATA_U	Upper bits of the entry of index table Reset State: 0x00000000

0x3000068 ADU_UMA_INDEX_TABLE_WDATA_L

Type: read-write
Reset State: 0x00000000

This register contains the lower bits of the entry of index table

ADU_UMA_INDEX_TABLE_WDATA_L

Bits	Name	Description
31:0	UMA_SRCHTABLE_WDATA_L	Lower bits of the 1st entry of index table Reset State: 0x00000000

0x300006C ADU_UMA_INDEX_TABLE_ADDR_CTRL

Type: read-write
Reset State: 0x00000000

This register contains the address of index table the data to be written to/read from

ADU_UMA_INDEX_TABLE_ADDR_CTRL

Bits	Name	Description
8	UMA_SRCHTABLE_RW	Always read '0' Write '1' to write the data {uma_index_data_u, uma_index_data_l} to the address uma_index_addr Write '0' to load the contents of the index table addressed by uma_index_addr to uma_index_table_data_[l|u] registers. Reset State: 0x00000000

ADU_UMA_INDEX_TABLE_ADDR_CTRL (cont.)

Bits	Name	Description
7:0	UMA_SRCHTABLE_ADDR	address of the index table to be written to/read from Reset State: 0x00000000

0x3000070 ADU_UMA_INDEX_TABLE_RDATA_U

Type: read-only
Reset State: 0x00000000

This register contains the upper bits of the entry of index table for read

ADU_UMA_INDEX_TABLE_RDATA_U

Bits	Name	Description
23:16	UMA_SRCHTABLE_RDATA_INDEX	Index of the index table for read Reset State: 0x00000000
15:0	UMA_SRCHTABLE_RDATA_U	Upper bits of the entry of index table for read Reset State: 0x00000000

0x3000074 ADU_UMA_INDEX_TABLE_RDATA_L

Type: read-only
Reset State: 0x00000000

This register contains the lower bits of the entry of index table for read

ADU_UMA_INDEX_TABLE_RDATA_L

Bits	Name	Description
31:0	UMA_SRCHTABLE_RDATA_L	Lower bits of the 1st entry of index table for read Reset State: 0x00000000

0x3000078 ADU_UMA_TX_DEFAULT_WMACADDR_U

Type: read-write
Reset State: 0x00000000

This register contains the upper bits of the default wmac addr to be used when there's no DA match

ADU_UMA_TX_DEFAULT_WMACADDR_U

Bits	Name	Description
15:0	UMA_DEFAULT_WMACADDR_U	Upper bits of the default wmac addr Reset State: 0x00000000

0x300007C ADU_UMA_TX_DEFAULT_WMACADDR_L

Type: read-write
Reset State: 0x00000000

This register contains the lower bits of the default wmac addr to be used when there's no DA match

ADU_UMA_TX_DEFAULT_WMACADDR_L

Bits	Name	Description
31:0	UMA_DEFAULT_WMACADDR_L	Lower bits of the default wmac addr Reset State: 0x00000000

0x3000080 ADU_UMA_CTRL2

Type: read-write
Reset State: 0x000104FF

This register is to control the UMA function

ADU_UMA_CTRL2

Bits	Name	Description
17	WOW_WAKEUP_SEL	When set, adu will check the BD for wow wakeup indication. When clear, adu will check the sideband signal from dpu for wow wakeup. Reset State: 0x00000000
16	RX_PRIORITY_ROUTING_WQ_EN	When set, adu will push to the rx_priority_routing_wq when the rx dxe priority routing bit is set in BD Reset State: 0x00000001
15:8	RX_PRIORITY_ROUTING_WQ	The WQ adu will push to when the rx dxe priority routing bit is set in BD Reset State: 0x00000004
7:0	UMA_TX_ERROR_WQ	The WQ uma tx will push the frame when there's error Reset State: 0x000000FF

0x3000084 ADU_UMA_TX_COUNTERS3

Type: read-only
Reset State: 0x00000000

This register contains counters information of uma tx

ADU_UMA_TX_COUNTERS3

Bits	Name	Description
23:16	UMA_TX_SYNC_WQ_COUNTER	Counters of the uma tx push to sync wq Reset State: 0x00000000
7:0	UMA_TX_BYPASS_COUNTER	Counters of the uma tx bypass Reset State: 0x00000000

0x30000B8 ADU_UMA_TX_WQ_QID_CTRL

Type: read-write
Reset State: 0x00000000

This register contains the control signals to enable/disable whether or not checking the threshold value for mCPU/btqm wq push.

ADU_UMA_TX_WQ_QID_CTRL

Bits	Name	Description
24	UMA_TX_BD_FILL_EN	When set, UMA TX fill the extra fields in BD. Reset State: 0x00000000

0x30000C0 ADU_ADU_POLL_CMD_ERROR_ADDR

Type: read-only
Reset State: 0x00000000

This register contains the poll cmd address when it reaches retry timeout error

ADU_ADU_POLL_CMD_ERROR_ADDR

Bits	Name	Description
31:0	ADU_POLL_CMD_ERROR_ADDR	The poll cmd address when adu_poll_cmd_error is generated Reset State: 0x00000000

0x30000C4 ADU_ADU_SW_REG_REINIT_ADDR

Type: read-write
Reset State: 0x00000000

This register contains the software triggered reg reinit table address

ADU_ADU_SW_REG_REINIT_ADDR

Bits	Name	Description
31:2	SW_REG_REINIT_ADDR	The software triggered reg reinit table address. always word address Reset State: 0x00000000

0x30000C8 ADU_ADU_SW_REG_REINIT_TRIGGER

Type: read-only
Reset State: 0x00000000

This register to trigger the reg reinit

ADU_ADU_SW_REG_REINIT_TRIGGER

Bits	Name	Description
0	SW_REG_REINIT_P	Write '1' to trigger the reg reinit. Always read 0. Reset State: 0x00000000

16.2.36 bmu

0x3000000 BMU_CONTROL

Type: read-write
Reset State: 0x03FE03FE

Sets the valid range of BD and PDU indexes in the BMU.

BMU_CONTROL

Bits	Name	Description
31:16	MAX_PDU_INDEX_NR	Typically the MAX PDU index is greater then the MAC BD index. In that case BDs can not be used as PDUs and vice versa. When MAX_BD_Index and MAX_PDU_index are programmed to the same value, the BMU is set in a special mode: Mixed mode. Each PDU can be used as a BD or each BD used as a PDU. At initialization the PDU idle list does not need to be created, just the BD idle list. When PDUs are requested, they will be taken from the BD idle list. During operation BD and PDU idle lists will both be maintained, but all released PDUs will automatically get moved back to the BD idle list. In this mode, the MAX BD and PDU index number can not be greater then the MAX BD index number that the hardware allows. Note that before the WQs get enabled, this value must be programmed accordingly to the amount of packet memory available. This is similar to have to program the bd_pbu_base_address in the MCU. The default value here is just a place holder. In Volans, the BMU should be configured to only operate in Mixed Mode. Reset State: 0x000003FE
10:0	MAX_BD_INDEX_NR	Virgo can maximum support 2K BDs. The maximum value that can therefor be programmed is 2047. Where as Libra and Volans can support only 1023 BDs Note that before the WQs get enabled, this value must be programmed accordingly to the amount of packet memory available. This is similar to have to program the bd_pbu_base_address in the MCU. The default value here is just a place holder. Reset State: 0x000003FE

0x3000004 BMU_ERR_INTR_STATUS

Type: read-only
Reset State: 0x00000000

This register indicates the BMU Error Interrupt Status When one of these errors occur, the status will always reflect this. The Err_Intr_ENABLE register is used to indicate which error bits will cause an interrupt to be generated. Writing a 1'b1 to a particular bit will clear the error status bit. Most of these errors are generated when the BMU receives a command. In this case the command will be stored in the 'err_int_addr' and 'err_int_wdata' registers.

BMU_ERR_INTR_STATUS

Bits	Name	Description
31	BMU_ACCESS_DIRECTION	When one of the error indications below gets set, this bit will indicate if this happened on a read or write BMU access. 1'b1 indicates write access 1'b0 indicates read access On a write access, register err_int_wdata will contain the write data Reset State: 0x00000000

BMU_ERR_INTR_STATUS (cont.)

Bits	Name	Description
30	BMU_INTERRUPT_STATUS	Status of the BMU err interrupt status signal going to the mcu. This is the OR of all interrupts enabled in this registers and bmu_idle_bd_pdu_threshold_interrupt_status bit from register: bmu_idle_bd_pdu_status. Reset State: 0x00000000
28	BTQM_ERR	This is the OR of all the enabled bits from btqm_err_status register Set when the btqm detects an error or some other operational related interrupt in the btqm_err_status register. The details on which btqm error happened can be found in register 'btqm_err_int_status' Reset State: 0x00000000
27	DOUBLE_RELEASE_PDU_ERR	Error set when head or tail of a list of linked PDUs that is being released is equal to the head or tail pointer of the idle PDU list. Note that there can be a delay between the release command and the detection of this problem due to buffering Reset State: 0x00000000
26	DOUBLE_RELEASE_BD_ERR	Error set when head or tail of a list of linked BDs that is being released is equal to the head or tail pointer of the idle BD list. Note that there can be a delay between the release command and the detection of this problem due to buffering Reset State: 0x00000000
25	DOUBLE_PUSH_ERR	Error set when a push command contains a BD index equal to the head or tail pointer of the WQ it is pushed to. Reset State: 0x00000000
24	RELEASE_FRAG_BD_INDEX_ERR	When BMU starts releasing defragmentation BD, if a fragment contains invalid BD index this error will be set Reset State: 0x00000000
23	MULTIPLE_READY_ERR	Error set when multiple modules in the bmu indicate ready. That should not happen. Reset State: 0x00000000
22	RELEASE_INTEGRITY_CHECK_PDU_LINK_ERR	Error set when on a release command, the integrity check failed. The pdu links were incorrect Reset State: 0x00000000
21	PUSH_INTEGRITY_CHECK_PDU_LINK_ERR	Error set when on a push bd command, the integrity check failed. The pdu links were incorrect Reset State: 0x00000000
20	PUSH_INTEGRITY_CHECK_HEAD_TAIL_PDU_ERR	Error set when on a push bd command, the integrity check failed. The head/tail/entries part in the BD was incorrect Reset State: 0x00000000
19	PUSH_INTEGRITY_CHECK_PREV_PDU_ERR	Error set when on a push bd command, the integrity check failed. The prev. pdu pointer in the BD was incorrect Reset State: 0x00000000

BMU_ERR_INTR_STATUS (cont.)

Bits	Name	Description
18	PREV_PDU_INDEX_ERR	Error set when on a release of BD with linked PDUs, and the A-MSDU feature is enabled and the prev PDU pointer has an invalid index. Reset State: 0x00000000
17	NR_OF_PDU_OVERFLOW_ERR	Error set when on a release of PDUs, the number of dle PDUs would gone over the theoretical amount as determined by the MAX BD index and MAX PDU index from the BMU control register Reset State: 0x00000000
16	NR_OF_BD_OVERFLOW_ERR	Error set when on a release of BDs, the number of idle BDs would gone over the theoretical amount as determined by the MAX BD index from the BMU control register Reset State: 0x00000000
15	WRGAM_ERR	Set when the write GAM indicated an internal error Reset State: 0x00000000
14	RDGAM_ERR	Set when the read GAM indicated an internal error Reset State: 0x00000000
13	TIME_OUT_ERR	Set when the BMU internally detected is has been hanging There is a timeout counter in the BMU, which tracks the length of each transaction. The timeout count value can be programmed in register: bmu_watchdog_timout_time For this error the 'err_int_addr' and 'err_int_wdata' registers are updated so it is recorded which bmu command caused this error. Reset State: 0x00000000
12	IDLE_PDU_LIST_TAIL_ERR	The pdu idle list is corrupted. In the PDU idle list the PDU prefetch unit has read the PDU pointer index from the one but last PDU in the PDU idle list. It was expected that this PDU index pointer points to the PDU indicated in the idle_pdu_tail register. This was however not the case. THis is a serious error as it indicates that the idle PDU list is corrupted. Reset State: 0x00000000
11	IDLE_PDU_LIST_CNT_ERR	The pdu idle list is corrupted. In the PDU idle list the PDU prefetch unit has found an PDU who was pointing to the PDU tail index, which would indicate that the end of the idle PDU list has been reached. But this does not correspond with the idle PDU count in the idle_pdu_count register. This error indicates that more PDUs were expected to be in the idle PDU list. THis is a serious error as it indicates that the idle PDU list is corrupted. Reset State: 0x00000000
10	PDU_INDEX_FROM_BD_ERR	When a BD with linked PDUs was released, the BMU detected that in the BD the number of linked PDUs was non zero, but the head or tail PDU pointer index in the BD was greater then the MAX PDU index range. This is an indication that the Idle PDU list is broken and is a serious error. Reset State: 0x00000000

BMU_ERR_INTR_STATUS (cont.)

Bits	Name	Description
9	RELEASE_FIFO_FULL_WARNING	Set when the BMU release fifo got full. This will not break BMU operation, but still should not occur as it can effect latency on the AHB bus. This however is minimized due to the split transaction generated by the BMU GAS if the release takes too long. Reset State: 0x00000000
8	BD_LINKED_LIST_ERR	Set when in the bd idle list a pointer to a bd index was found that is outside of the valid bd index ranges. This is a serious error and the only way to recover is to soft reset the BMU or generate a bmu module reset Reset State: 0x00000000
7	PDU_LINKED_LIST_ERR	Set when in the pdu idle list a pointer to a pdu index was found that is outside of the valid pdu index ranges. This is a serious error and the only way to recover is to soft reset the BMU or generate a bmu module reset Reset State: 0x00000000
6	OUT_OF_MODULE_RANGE_ERR	Set when a BMU command with module index that was out of allowed range was used The valid module index is less than or equal to BMU_HIGHEST_VALID_MASTER_INDEX For this error the 'err_int_addr' and 'err_int_wdata' registers are updated so it is recorded which bmu command caused this error. Reset State: 0x00000000
5	OUT_OF_PDU_RANGE	Set when a BMU command with PDU index that was out of allowed range was used For this error the 'err_int_addr' and 'err_int_wdata' registers are updated so it is recorded which bmu command caused this error. Reset State: 0x00000000
4	OUT_OF_BD_RANGE	Set when a BMU command with BD index that was out of allowed range was used For this error the 'err_int_addr' and 'err_int_wdata' registers are updated so it is recorded which bmu command caused this error. Reset State: 0x00000000
3	UNDEFINED_CMD	Set when an undefined BMU command was given to the BMU For this error the 'err_int_addr' and 'err_int_wdata' registers are updated so it is recorded which bmu command caused this error. Reset State: 0x00000000
2	WQ_INVALID	Set when an un-enabled or undefined WQ was used in a BMU command In Volans, the valid WQs are "2 to 16 and 23 to 26" For this error the 'err_int_addr' and 'err_int_wdata' registers are updated so it is recorded which bmu command caused this error. Reset State: 0x00000000
1	WQ_FULL	This is set with push command when the WQ entries are greater/equal to highest_valid_bd_index value. This shouldn't happen in the system For this error the 'err_int_addr' and 'err_int_wdata' registers are updated so it is recorded which bmu command caused this error. Reset State: 0x00000000

BMU_ERR_INTR_STATUS (cont.)

Bits	Name	Description
0	NOT_ENOUGH_BD_PDU_WARNING	Set when a request for BD_PDUs came in when they were not available. The modules should be able to handle this and resubmit their request at a later time. This is not an error, but is given for informational purposes Reset State: 0x00000000

0x3000008 BMU_ERR_INTR_ENABLE

Type: read-write
Reset State: 0x00000000

This register is used as BMU Interrupt enable Mask. By default all the interrupts are disabled For descriptions of each error interrupt, see register: Err_Intr_STATUS

BMU_ERR_INTR_ENABLE

Bits	Name	Description
28	BTQM_ERR_ENABLE	Reset State: 0x00000000
27	DOUBLE_RELEASE_PDU_ERR_ENABLE	Reset State: 0x00000000
26	DOUBLE_RELEASE_BD_ERR_ENABLE	Reset State: 0x00000000
25	DOUBLE_PUSH_ERR_ENABLE	Reset State: 0x00000000
24	RELEASE_FRAG_BD_INDEX_ERR_ENABLE	Reset State: 0x00000000
23	MULTIPLE_READY_ERR_ENABLE	Reset State: 0x00000000
22	RELEASE_INTEGRITY_CHECK_PDU_LINK_ERR_ENABLE	Reset State: 0x00000000
21	PUSH_INTEGRITY_CHECK_PDU_LINK_ERR_ENABLE	Reset State: 0x00000000
20	PUSH_INTEGRITY_CHECK_HEAD_TAIL_PDU_ERR_ENABLE	Reset State: 0x00000000
19	PUSH_INTEGRITY_CHECK_PREV_PDU_ERR_ENABLE	Reset State: 0x00000000
18	PREV_PDU_INDEX_ERR_ENABLE	Reset State: 0x00000000
17	NR_OF_PDU_OVERFLOW_ERR_ENABLE	Reset State: 0x00000000

BMU_ERR_INTR_ENABLE (cont.)

Bits	Name	Description
16	NR_OF_BD_OVERFLOW_ERR_ENABLE	Reset State: 0x00000000
15	WRGAM_ERR_ENABLE	Reset State: 0x00000000
14	RDGAM_ERR_ENABLE	Reset State: 0x00000000
13	TIMEOUT_ERR_ENABLE	Reset State: 0x00000000
12	IDLE_PDU_LIST_TAIL_ERR_ENABLE	Reset State: 0x00000000
11	IDLE_PDU_LIST_CNT_ERR_ENABLE	Reset State: 0x00000000
10	PDU_INDEX_FROM_BD_ERR_ENABLE	Reset State: 0x00000000
9	RELEASE_FIFO_FULL_WARNING_ENABLE	Reset State: 0x00000000
8	BD_LINKED_LIST_ERR_ENABLE	Reset State: 0x00000000
7	PDU_LINKED_LIST_ERR_ENABLE	Reset State: 0x00000000
6	OUT_OF_MODULE_RANGE_ERR_ENABLE	Reset State: 0x00000000
5	OUT_OF_PDU_RANGE_ERR_ENABLE	Reset State: 0x00000000
4	OUT_OF_BD_RANGE_ERR_ENABLE	Reset State: 0x00000000
3	UNDEFINED_CMD_ERR_ENABLE	Reset State: 0x00000000
2	WQ_INVALID_ERR_ENABLE	Reset State: 0x00000000
1	WQ_FULL_ERR_ENABLE	Reset State: 0x00000000
0	NOT_ENOUGH_BD_PDU_WARNING_ENABLE	Reset State: 0x00000000

0x300000C BMU_ERR_INT_ADDR

Type: read-only
Reset State: 0x00000000

This register contains the BMU access address that caused the last error interrupt is generated This information is for debug purpose only

BMU_ERR_INT_ADDR

Bits	Name	Description
31:0	BMU_ERR_ACCESS_ADDRESS	Reset State: 0x00000000

0x3000010 BMU_ERR_INT_WDATA

Type: read-only
Reset State: 0x00000000

This register contains the BMU access wdata that caused the last error interrupt is generated. This information is for debug purpose only The data in here is only valid when 'BMU_access_direction' in register Err_Intr_STATUS is set.

BMU_ERR_INT_WDATA

Bits	Name	Description
31:0	BMU_ERR_ACCESS_WDATA	Reset State: 0x00000000

0x3000014 BMU_BD_PDU_THRESHOLD0

Type: read-write
Reset State: 0x00000035

Controls the bd_pdu_available[0] signal to RXP. If the available free BDs or PDUs are less or equal to these programmed values, the bd_pdu_available[0] signal to the RXP will not be set, causing that master to stall. The software programmers guide will have guidance on how to program these values.

BMU_BD_PDU_THRESHOLD0

Bits	Name	Description
31:16	PDU_THRESHOLD_0	Reset State: 0x00000000
10:0	BD_THRESHOLD_0	Reset State: 0x00000035

0x3000018 BMU_BD_PDU_THRESHOLD1

Type: read-write
Reset State: 0x00000001

Controls the bd_pdu_available[1] signal to DPU. If the available free BDs or PDUs are less or equal to these programmed values, the bd_pdu_available[1] signal to the DPU will not be set,

causing that master to stall. The software programmers guide will have guidance on how to program these values.

BMU_BD_PDU_THRESHOLD1

Bits	Name	Description
31:16	PDU_THRESHOLD_1	Reset State: 0x00000000
10:0	BD_THRESHOLD_1	Reset State: 0x00000001

0x300001C BMU_BD_PDU_THRESHOLD2

Type: read-write
Reset State: 0x00000001

Controls the bd_pdu_available[2] signal to DPU. If the available free BDs or PDUs are less or equal to these programmed values, the bd_pdu_available[2] signal to the DPU will not be set, causing that master to stall. The software programmers guide will have guidance on how to program these values.

BMU_BD_PDU_THRESHOLD2

Bits	Name	Description
31:16	PDU_THRESHOLD_2	Reset State: 0x00000000
10:0	BD_THRESHOLD_2	Reset State: 0x00000001

0x3000020 BMU_BD_PDU_THRESHOLD3

Type: read-write
Reset State: 0x00000001

Controls the bd_pdu_available[3]. The assignment/usage of this signal is programmable. It could be used by software or used by the DXE If the available free BDs or PDUs are less or equal to these programmed values, the bd_pdu_available[3] signal will not be set, typically preventing that new BDs and/or PDUs get reserved or requested. The software programmers guide will have guidance on how to program these values.

BMU_BD_PDU_THRESHOLD3

Bits	Name	Description
31:16	PDU_THRESHOLD_3	Reset State: 0x00000000
10:0	BD_THRESHOLD_3	Reset State: 0x00000001

0x3000024 BMU_BD_PDU_THRESHOLD4

Type: read-write
Reset State: 0x00000028

Controls the bd_pdu_available[4]. The assignment/usage of this signal is programmable. It could be used by software or used by the DXE If the available free BDs or PDUs are less or equal to these programmed values, the bd_pdu_available[4] signal will not be set, typically preventing that new BDs and/or PDUs get reserved or requested. The software programmers guide will have guidance on how to program these values.

BMU_BD_PDU_THRESHOLD4

Bits	Name	Description
31:16	PDU_THRESHOLD_4	Reset State: 0x00000000
10:0	BD_THRESHOLD_4	Reset State: 0x00000028

0x3000028 BMU_BD_PDU_THRESHOLD5

Type: read-write
Reset State: 0x00000028

Controls the bd_pdu_available[5]. The assignment/usage of this signal is programmable. It could be used by software or used by the DXE If the available free BDs or PDUs are less or equal to these programmed values, the bd_pdu_available[5] signal will not be set, typically preventing that new BDs and/or PDUs get reserved or requested. The software programmers guide will have guidance on how to program these values.

BMU_BD_PDU_THRESHOLD5

Bits	Name	Description
31:16	PDU_THRESHOLD_5	Reset State: 0x00000000
10:0	BD_THRESHOLD_5	Reset State: 0x00000028

0x300002C BMU_BD_PDU_THRESHOLD6

Type: read-write
Reset State: 0x00000001

Controls the bd_pdu_available[6]. The assignment/usage of this signal is programmable. It could be used by software or used by the DXE If the available free BDs or PDUs are less or equal to these programmed values, the bd_pdu_available[6] signal will not be set, typically preventing that new BDs and/or PDUs get reserved or requested. The software programmers guide will have guidance on how to program these values.

BMU_BD_PDU_THRESHOLD6

Bits	Name	Description
31:16	PDU_THRESHOLD_6	Reset State: 0x00000000
10:0	BD_THRESHOLD_6	Reset State: 0x00000001

0x3000030 BMU_BD_PDU_THRESHOLD7

Type: read-write
Reset State: 0x00000029

Controls the bd_pdu_available[7]. The assignment/usage of this signal is programmable. It could be used by software or used by the DXE If the available free BDs or PDUs are less or equal to these programmed values, the bd_pdu_available[7] signal will not be set, typically preventing that new BDs and/or PDUs get reserved or requested. The software programmers guide will have guidance on how to program these values.

BMU_BD_PDU_THRESHOLD7

Bits	Name	Description
31:16	PDU_THRESHOLD_7	Reset State: 0x00000000
10:0	BD_THRESHOLD_7	Reset State: 0x00000029

0x3000034 BMU_BD_PDU_THRESHOLD8

Type: read-write
Reset State: 0x00000029

Controls the bd_pdu_available[8]. The assignment/usage of this signal is programmable. It could be used by software or used by the DXE If the available free BDs or PDUs are less or equal to these programmed values, the bd_pdu_available[8] signal will not be set, typically preventing that new BDs and/or PDUs get reserved or requested. The software programmers guide will have guidance on how to program these values.

BMU_BD_PDU_THRESHOLD8

Bits	Name	Description
31:16	PDU_THRESHOLD_8	Reset State: 0x00000000
10:0	BD_THRESHOLD_8	Reset State: 0x00000029

0x3000038 BMU_BD_PDU_THRESHOLD9

Type: read-write
Reset State: 0x000003FF

Controls the bd_pdu_available[9]. The assignment/usage of this signal is programmable. It could be used by software or used by the DXE If the available free BDs or PDUs are less or equal to these programmed values, the bd_pdu_available[9] signal will not be set, typically preventing that new BDs and/or PDUs get reserved or requested. The software programmers guide will have guidance on how to program these values.

BMU_BD_PDU_THRESHOLD9

Bits	Name	Description
31:16	PDU_THRESHOLD_9	Reset State: 0x00000000
10:0	BD_THRESHOLD_9	Reset State: 0x000003FF

0x300003C BMU_BD_PDU_THRESHOLD10

Type: read-write
Reset State: 0x000003FF

Controls the bd_pdu_available[10]. The assignment/usage of this signal is programmable. It could be used by software or used by the DXE If the available free BDs or PDUs are less or equal to these programmed values, the bd_pdu_available[10] signal will not be set, typically preventing that new BDs and/or PDUs get reserved or requested. The software programmers guide will have guidance on how to program these values.

BMU_BD_PDU_THRESHOLD10

Bits	Name	Description
31:16	PDU_THRESHOLD_10	Reset State: 0x00000000
10:0	BD_THRESHOLD_10	Reset State: 0x000003FF

0x3000040 BMU_BD_PDU_RESERVED0

Type: read-only
Reset State: 0x00000000

Indicates how many BDs or PDUs have been reserved by the RXP A module can use the BMU command Idle BD and PDU reservation request to have the BMU set aside a number of BDs and PDUs for that module. These BDs and PDUs will only be set aside if this does not violate the 'BD and PDU threshold values that were set aside for this master. This register gives inside into how many BDs and PDUs have been set aside to this master. This number will decrement each time the module gets a BD or PDU.

BMU_BD_PDU_RESERVED0

Bits	Name	Description
31:16	NUMBER_RESERVED_PDU	Reset State: 0x00000000
10:0	NUMBER_RESERVED_BD	Reset State: 0x00000000

0x3000044 BMU_BD_PDU_RESERVED1

Type: read-only
Reset State: 0x00000000

Indicates how many BDs or PDUs have been reserved by the DPU A module can use the BMU command Idle BD and PDU reservation request to have the BMU set aside a number of BDs and PDUs for that module. These BDs and PDUs will only be set aside if this does not violate the 'BD and PDU threshold values that were set aside for this master. This register gives inside into how many BDs and PDUs have been set aside to this master. This number will decrement each time the module gets a BD or PDU.

BMU_BD_PDU_RESERVED1

Bits	Name	Description
31:16	NUMBER_RESERVED_PDU	Reset State: 0x00000000
10:0	NUMBER_RESERVED_BD	Reset State: 0x00000000

0x3000048 BMU_BD_PDU_RESERVED2

Type: read-only
Reset State: 0x00000000

Indicates how many BDs or PDUs have been reserved by master 2 (software assignable) A module can use the BMU command Idle BD and PDU reservation request to have the BMU set aside a number of BDs and PDUs for that module. These BDs and PDUs will only be set aside if this does not violate the 'BD and PDU threshold values that were set aside for this master. This register gives inside into how many BDs and PDUs have been set aside to this master. This number will decrement each time the module gets a BD or PDU. Note that this can be used as a mechanism by software to set a number of PDUs and BDs aside for a particular DXE channel.

BMU_BD_PDU_RESERVED2

Bits	Name	Description
31:16	NUMBER_RESERVED_PDU	Reset State: 0x00000000
10:0	NUMBER_RESERVED_BD	Reset State: 0x00000000

0x300004C BMU_BD_PDU_RESERVED3

Type: read-only
Reset State: 0x00000000

Indicates how many BDs or PDUs have been reserved by master 3 (software assignable) A module can use the BMU command Idle BD and PDU reservation request to have the BMU set aside a number of BDs and PDUs for that module. These BDs and PDUs will only be set aside if this does not violate the 'BD and PDU threshold values that were set aside for this master. This register gives inside into how many BDs and PDUs have been set aside to this master. This number will decrement each time the module gets a BD or PDU. Note that this can be used as a mechanism by software to set a number of PDUs and BDs aside for a particular DXE channel.

BMU_BD_PDU_RESERVED3

Bits	Name	Description
31:16	NUMBER_RESERVED_PDU	Reset State: 0x00000000
10:0	NUMBER_RESERVED_BD	Reset State: 0x00000000

0x3000050 BMU_BD_PDU_RESERVED4

Type: read-only
Reset State: 0x00000000

Indicates how many BDs or PDUs have been reserved by master 4 (software assignable) A module can use the BMU command Idle BD and PDU reservation request to have the BMU set aside a number of BDs and PDUs for that module. These BDs and PDUs will only be set aside if this does not violate the 'BD and PDU threshold values that were set aside for this master. This register gives inside into how many BDs and PDUs have been set aside to this master. This number will decrement each time the module gets a BD or PDU. Note that this can be used as a mechanism by software to set a number of PDUs and BDs aside for a particular DXE channel.

BMU_BD_PDU_RESERVED4

Bits	Name	Description
31:16	NUMBER_RESERVED_PDU	Reset State: 0x00000000
10:0	NUMBER_RESERVED_BD	Reset State: 0x00000000

0x3000054 BMU_BD_PDU_RESERVED5

Type: read-only
Reset State: 0x00000000

Indicates how many BDs or PDUs have been reserved by master 5 (software assignable) A module can use the BMU command Idle BD and PDU reservation request to have the BMU set aside a

number of BDs and PDUs for that module. These BDs and PDUs will only be set aside if this does not violate the 'BD and PDU threshold values that were set aside for this master. This register gives inside into how many BDs and PDUs have been set aside to this master. This number will decrement each time the module gets a BD or PDU. Note that this can be used as a mechanism by software to set a number of PDUs and BDs aside for a particular DXE channel.

BMU_BD_PDU_RESERVED5

Bits	Name	Description
31:16	NUMBER_RESERVED_PDU	Reset State: 0x00000000
10:0	NUMBER_RESERVED_BD	Reset State: 0x00000000

0x3000058 BMU_BD_PDU_RESERVED6

Type: read-only
Reset State: 0x00000000

Indicates how many BDs or PDUs have been reserved by master 6 (software assignable) A module can use the BMU command Idle BD and PDU reservation request to have the BMU set aside a number of BDs and PDUs for that module. These BDs and PDUs will only be set aside if this does not violate the 'BD and PDU threshold values that were set aside for this master. This register gives inside into how many BDs and PDUs have been set aside to this master. This number will decrement each time the module gets a BD or PDU. Note that this can be used as a mechanism by software to set a number of PDUs and BDs aside for a particular DXE channel.

BMU_BD_PDU_RESERVED6

Bits	Name	Description
31:16	NUMBER_RESERVED_PDU	Reset State: 0x00000000
10:0	NUMBER_RESERVED_BD	Reset State: 0x00000000

0x300005C BMU_BD_PDU_RESERVED7

Type: read-only
Reset State: 0x00000000

Indicates how many BDs or PDUs have been reserved by master 7 (software assignable) A module can use the BMU command Idle BD and PDU reservation request to have the BMU set aside a number of BDs and PDUs for that module. These BDs and PDUs will only be set aside if this does not violate the 'BD and PDU threshold values that were set aside for this master. This register gives inside into how many BDs and PDUs have been set aside to this master. This number will decrement each time the module gets a BD or PDU. Note that this can be used as a mechanism by software to set a number of PDUs and BDs aside for a particular DXE channel.

BMU_BD_PDU_RESERVED7

Bits	Name	Description
31:16	NUMBER_RESERVED_PDU	Reset State: 0x00000000
10:0	NUMBER_RESERVED_BD	Reset State: 0x00000000

0x3000060 BMU_BD_PDU_RESERVED8

Type: read-only
Reset State: 0x00000000

Indicates how many BDs or PDUs have been reserved by master 8 (software assignable) A module can use the BMU command Idle BD and PDU reservation request to have the BMU set aside a number of BDs and PDUs for that module. These BDs and PDUs will only be set aside if this does not violate the 'BD and PDU threshold values that were set aside for this master. This register gives inside into how many BDs and PDUs have been set aside to this master. This number will decrement each time the module gets a BD or PDU. Note that this can be used as a mechanism by software to set a number of PDUs and BDs aside for a particular DXE channel.

BMU_BD_PDU_RESERVED8

Bits	Name	Description
31:16	NUMBER_RESERVED_PDU	Reset State: 0x00000000
10:0	NUMBER_RESERVED_BD	Reset State: 0x00000000

0x3000064 BMU_BD_PDU_RESERVED9

Type: read-only
Reset State: 0x00000000

Indicates how many BDs or PDUs have been reserved by master 9 (software assignable) A module can use the BMU command Idle BD and PDU reservation request to have the BMU set aside a number of BDs and PDUs for that module. These BDs and PDUs will only be set aside if this does not violate the 'BD and PDU threshold values that were set aside for this master. This register gives inside into how many BDs and PDUs have been set aside to this master. This number will decrement each time the module gets a BD or PDU. Note that this can be used as a mechanism by software to set a number of PDUs and BDs aside for a particular DXE channel.

BMU_BD_PDU_RESERVED9

Bits	Name	Description
31:16	NUMBER_RESERVED_PDU	Reset State: 0x00000000
10:0	NUMBER_RESERVED_BD	Reset State: 0x00000000

0x3000068 BMU_BD_PDU_RESERVED10

Type: read-only
Reset State: 0x00000000

Indicates how many BDs or PDUs have been reserved by master 10 (software assignable) A module can use the BMU command Idle BD and PDU reservation request to have the BMU set aside a number of BDs and PDUs for that module. These BDs and PDUs will only be set aside if this does not violate the 'BD and PDU threshold values that were set aside for this master. This register gives inside into how many BDs and PDUs have been set aside to this master. This number will decrement each time the module gets a BD or PDU. Note that this can be used as a mechanism by software to set a number of PDUs and BDs aside for a particular DXE channel.

BMU_BD_PDU_RESERVED10

Bits	Name	Description
31:16	NUMBER_RESERVED_PDU	Reset State: 0x00000000
10:0	NUMBER_RESERVED_BD	Reset State: 0x00000000

0x300006C BMU_WQ_ENABLE

Type: read-write
Reset State: 0x00000000

Controls which WQ will be enabled. These WQs should be enabled during initialization, after the BD and PDU idle lists have been created and all head an tail pointers for the to be enabled WQs have been configured. The number of WQs to be enabled need to be decided at that time. Once enabled, a WQ should never be disable again, as this can cause BD and PDU leaks. Bit 0 corresponds to WQ0, Bit 26 corresponds to WQ 26.

BMU_WQ_ENABLE

Bits	Name	Description
26:0	WQ_ENABLE	WQ0: Assigned for Idle BD. WQ1: Assigned for Idle PDU WQ2: Assigned for mCPU RX WQ WQ3: Can be assigned to DPU, DXE or mCPU WQ4: Can be assigned to DPU, DXE or mCPU WQ5: Can be assigned to DPU, DXE or mCPU WQ6: Can be assigned to DPU, DXE or mCPU WQ7: Can be assigned to DPU, DXE or mCPU WQ8: Can be assigned to DPU, DXE or mCPU WQ9: Can be assigned to DPU, DXE or mCPU WQ10: Can be assigned to DPU, DXE or mCPU WQ11: Can be assigned to DXE or mCPU WQ12: Can be assigned to DXE or mCPU WQ13: Can be assigned to DXE or mCPU WQ14: Can be assigned to DXE or mCPU WQ15: Can be assigned to DXE or mCPU WQ16: Can be assigned to DXE or mCPU WQ17: Not supported in Volans WQ18: Not supported in Volans WQ19: Not supported in Volans WQ20: Not supported in Volans WQ21: Not supported in Volans WQ22: Not supported in Volans WQ23: Can be assigned to mCPU WQ24: Can be assigned to mCPU, or ADU WQ25: High priority entrance WQ for the BTQM (BMU Transmit Queue Manager) WQ26: Low priority entrance WQ for the BTQM (BMU Transmit Queue Manager) Reset State: 0x00000000

0x3000070 BMU_DPU_WQ_ASSIGNMENT

Type: read-write
Reset State: 0x00000809

WQs 3 to 10 can be assigned to the DPU. This register controls if they are assigned to the DPU and if so, in which direction: TX or RX By default, WQ 3 is enabled and assigned to the TX side of the DPU By default, WQ 4 is enabled and assigned to the RX side of the DPU

BMU_DPU_WQ_ASSIGNMENT

Bits	Name	Description
15	WQ10_DPU_ASSIGNMENT_DIRECTION	Only valid when WQ 10 is assigned to the DPU. When set, WQ 10 is assigned to the TX side of the DPU When NOT set, WQ 10 is assigned to the RX side of the DPU Reset State: 0x00000000
14	WQ9_DPU_ASSIGNMENT_DIRECTION	Only valid when WQ 9 is assigned to the DPU. When set, and WQ 9 is assigned to the TX side of the DPU When NOT set, WQ 9 is assigned to the RX side of the DPU Reset State: 0x00000000
13	WQ8_DPU_ASSIGNMENT_DIRECTION	Only valid when WQ 8 is assigned to the DPU. When set, and WQ 8 is assigned to the TX side of the DPU When NOT set, WQ 8 is assigned to the RX side of the DPU Reset State: 0x00000000

BMU_DPU_WQ_ASSIGNMENT (cont.)

Bits	Name	Description
12	WQ7_DPU_ASSIGNMENT_DIRECTION	Only valid when WQ 7 is assigned to the DPU. When set, and WQ 7 is assigned to the TX side of the DPU When NOT set, WQ 7 is assigned to the RX side of the DPU Reset State: 0x00000000
11	WQ6_DPU_ASSIGNMENT_DIRECTION	Only valid when WQ 6 is assigned to the DPU. When set, and WQ 6 is assigned to the TX side of the DPU When NOT set, WQ 6 is assigned to the RX side of the DPU Reset State: 0x00000001
10	WQ5_DPU_ASSIGNMENT_DIRECTION	Only valid when WQ 5 is assigned to the DPU. When set, and WQ 5 is assigned to the TX side of the DPU When NOT set, WQ 5 is assigned to the RX side of the DPU Reset State: 0x00000000
9	WQ4_DPU_ASSIGNMENT_DIRECTION	Only valid when WQ 4 is assigned to the DPU. When set, and WQ 4 is assigned to the TX side of the DPU When NOT set, WQ 4 is assigned to the RX side of the DPU Reset State: 0x00000000
8	WQ3_DPU_ASSIGNMENT_DIRECTION	Only valid when WQ 3 is assigned to the DPU. When set, and WQ 3 is assigned to the TX side of the DPU When NOT set, WQ 3 is assigned to the RX side of the DPU Reset State: 0x00000000
7	WQ10_DPU_ASSIGNMENT_ENABLE	When set, WQ 10 is assigned to the DPU Reset State: 0x00000000
6	WQ9_DPU_ASSIGNMENT_ENABLE	When set, WQ 9 is assigned to the DPU Reset State: 0x00000000
5	WQ8_DPU_ASSIGNMENT_ENABLE	When set, WQ 8 is assigned to the DPU Reset State: 0x00000000
4	WQ7_DPU_ASSIGNMENT_ENABLE	When set, WQ 7 is assigned to the DPU Reset State: 0x00000000
3	WQ6_DPU_ASSIGNMENT_ENABLE	When set, WQ 6 is assigned to the DPU Reset State: 0x00000001
2	WQ5_DPU_ASSIGNMENT_ENABLE	When set, WQ 5 is assigned to the DPU Reset State: 0x00000000
1	WQ4_DPU_ASSIGNMENT_ENABLE	When set, WQ 4 is assigned to the DPU Reset State: 0x00000000
0	WQ3_DPU_ASSIGNMENT_ENABLE	When set, WQ 3 is assigned to the DPU Reset State: 0x00000001

0x3000074 BMU_TEST_CTRL

Type: read-write
Reset State: 0x00000000

Selects the test bus configuration from the BMU. Used for hardware debug only

BMU_TEST_CTRL

Bits	Name	Description
9:8	TESTBUS_BIT_SWAP_MODE	Controls how the 45 bmu testbus signals are mapped onto the output testbus signals Assignment TBD Reset State: 0x00000000
4:0	TEST_BUS_SEL	Enabled different testbusses in the BMU. Default assignment is gas other assignment TBD Reset State: 0x00000000

0x3000078 BMU_TEST_OUT_LOW

Type: read-only
Reset State: 0x00000000

This is read only register which contains the muxed out bmu_test bus. To select the test bus check the encoding in bmu test control register. test_bus_sel[2:0].

BMU_TEST_OUT_LOW

Bits	Name	Description
31:0	BMU_TEST_BUS	BMU test out bus bits [31:0] Reset State: 0x00000000

0x300007C BMU_TEST_OUT_HIGH

Type: read-only
Reset State: 0x00000000

This is read only register which contains the muxed out bmu_test bus. To select the test bus check the encoding in bmu test control register. test_bus_sel[2:0].

BMU_TEST_OUT_HIGH

Bits	Name	Description
31:0	BMU_TEST_BUS	BMU test out bus bits [43:32] Reset State: 0x00000000

0x3000080 BMU_GAS_CONFIGURATION

Type: read-write
Reset State: 0x000F7F0F

These are the configuration bits for the gas The default values should be OK This register is provided as a backup

BMU_GAS_CONFIGURATION

Bits	Name	Description
19:16	GAS_CFG_HREADY_LIMIT	Reset State: 0x0000000F
15:8	GAS_CFG_HSPLIT_RESP_LIMIT	Reset State: 0x0000007F
7:0	GAS_CFG_HSPLIT_MST_RESP_LIMIT	Reset State: 0x0000000F

0x3000084 BMU_AVAILABLE_BD_PDU_AFTER_RSV

Type: read-only
Reset State: 0x00000000

This register can be used to find out how many idle PDUs and BDs are actually available from the BD and PDU idle list when the number of reserved BDs and PDUs for all the different modules have been taken into account.

BMU_AVAILABLE_BD_PDU_AFTER_RSV

Bits	Name	Description
31:16	AVAILABLE_PDUS	Reset State: 0x00000000
15:0	AVAILABLE_BDS	Reset State: 0x00000000

0x3000088 BMU_CONTROL2

Type: read-write
Reset State: 0x00000001

This register can be used to control bmu A-MSDU support BD/PDU integrity checking by the BMU To enable rxp_bmu_dxe_datalength for DXE wq byte count To enable enhanced reserve all command To enable priority based BD/PDU reservation

BMU_CONTROL2

Bits	Name	Description
31	FREEZE_ONE_ERROR_LESS_STRICKED_ENABLE	When bit 'freeze_one_error' is set, and this bit is set, and an error is detected in the BMU, the BMU will freeze, but in a little less rigorous way then when this bit is not set. Get commands will still go through, and the BD/PDU available signals to the RXP and DPU will not be masked off. This will prevent DPU and RXP getting into some error state. Reset State: 0x00000000
7	BLOCK_RXP_PUSH_INTEGRITY_CHECK	When set, and 'push_data_integrity_check' is also set, the push integrity will be performed on all WQs except WQ 2. That is the WQ that RXP is pushing to. Reset State: 0x00000000
6	FREEZE_ONE_ERROR_ENABLE	When set, and an error is detected in the BMU, the BMU will freeze. That is, release commands are thrown away, get bd/dpu commands will not be successful anymore, and reservation request will return unsuccessful. All wq signals and bd/pdu available signals will be set to low. Reset State: 0x00000000
5	RELEASE_INTEGRITY_CHECK	When set, and a release command is received by the BMU, the BMU will check the integrity of the BD and linked PDUs. If a problem is found with the linked DPU pointers, an error is reported and the frame is not pushed into the WQ, so that the contents remains available for debugging Reset State: 0x00000000
4	PUSH_DATA_INTEGRITY_CHECK	When set, and a push command is received by the BMU, the BMU will check the integrity of the BD and linked PDUs. If a problem is found with the BD/DPU pointers, an error is reported and the frame is not pushed into the WQ, so that the contents remains available for debugging The index of the BD that caused the problem can be read in register: bmu_push_integrity_err_bd_index Reset State: 0x00000000
3	RXP_BMU_DXE_DATALEN_ENABLE	When set, any packet push from Rxp to Dxe, rxp_bmu_dxe_datalen is taken to calculate dxe data length Reset State: 0x00000000
2	ENHANCED_RESERVE_ALL_ENABLE	When set, reserve all command checks for TX memory threshold if tx_threshold is greater than BTQM memory size then it reserves min. of (tx_threshold - BTQM memory size, idle Packet memory size - requested module threshold) Reset State: 0x00000000
1	PRIORITY_BASED_RES_ENABLE	When set, enables priority based BD/PDU reservation command Reset State: 0x00000000

BMU_CONTROL2 (cont.)

Bits	Name	Description
0	AMSDU_RELEASE_SUPPORT_ENABLE	When set, the A-MSDU support for releasing PDUs from BDs is enabled. This means that the BMU will evaluate the setting of the PREV PDU index field in the BD. If this field is zero, the PDUs are release according to the head/tail and PDU count linked to the BD. When the PREV PDU index field is unequal to zero, the BMU will use this index as the 'tail' index of the list of PDUs to release. The amount of PDUs to release is set equal to PDU count minus 1. Reset State: 0x00000001

0x300008C BMU_DISABLE_WQ_DA

Type: read-write
Reset State: 0x00000000

This register can be used to disable the wq da available signals. In that case, modules will think that their WQ is empty.

BMU_DISABLE_WQ_DA

Bits	Name	Description
26:2	DISABLE_WQ_DA	Bit 2 corresponds with WQ 2, bit 3 with WQ 3 etc. When set, the wq da available signal to a WQ will always indicate that the WQ is empty. This overwrites any real amount of frames buffered in a WQ. Reset State: 0x00000000

0x3000090 BMU_DISABLE_BD_PDU_AVAIL

Type: read-write
Reset State: 0x00000000

This register can be used to disable the bd_pdu available signals. In that case, modules will think that no more BDs or PDUs are available, and will stall their operation

BMU_DISABLE_BD_PDU_AVAIL

Bits	Name	Description
10:0	DISABLE_BD_PDU_AVAIL	Bit 0 corresponds with master 0, bit 1 with master 1 etc. When set, the bd_pdu available signal to a master will always indicate that no BDs and PDUs are available. This overwrites any real amount of BDs or PDUs being available for that module. Reset State: 0x00000000

0x3000094 BMU_LAST_FOUR_POP_TRACE_CONTROL

Type: read-write
Reset State: 0x00000000

This register controls the enabling of the last 4 pop command tracing control. The POP command tracing can be enabled for one specific (programmable) WQ. It also provides insight into how many times a pop command was issues for the specified WQ

BMU_LAST_FOUR_POP_TRACE_CONTROL

Bits	Name	Description
31:16	POP_CMD_COUNT	The number of times a POP command was issued on the specified WQ. Reset State: 0x00000000
8	POP_TRACE_ENABLE	When set, the pop tracing functionality for the WQ as specified in field 'pop_trace_wq_index' is enabled. The BD indexes returned for the last 4 pop commands that were issued for the specified WQ, are captured in the registers: pop_cmd_trace_bd_index0, pop_cmd_trace_bd_index1, pop_cmd_trace_bd_index2 and pop_cmd_trace_bd_index3.The index in the pop_cmd_trace_bd_index0 is the BD index returned with the most recent pop command. Whenever the 'pop_trace_wq_index' field gets changed the pop trace functionality first needs to be disabled. That will clear the 4 stored indexes and the pop counter. Reset State: 0x00000000
4:0	POP_TRACE_WQ_INDEX	The WQ index for which the pop commands need to be traced Reset State: 0x00000000

0x3000098 BMU_POP_CMD_TRACE_BD_INDEX0

Type: read-only
Reset State: 0x00000000

This register contains a BD index returned as the result of a POP command on a specific WQ. See the description for the 'last_four_pop_trace_control' register for additional details.

BMU_POP_CMD_TRACE_BD_INDEX0

Bits	Name	Description
11:0	POP_BD_INDEX0	BD index Reset State: 0x00000000

0x300009C BMU_POP_CMD_TRACE_BD_INDEX1

Type: read-only
Reset State: 0x00000000

This register contains a BD index returned as the result of a POP command on a specific WQ. See the description for the 'last_four_pop_trace_control' register for additional details.

BMU_POP_CMD_TRACE_BD_INDEX1

Bits	Name	Description
11:0	POP_BD_INDEX1	BD index Reset State: 0x00000000

0x30000A0 BMU_POP_CMD_TRACE_BD_INDEX2

Type: read-only
Reset State: 0x00000000

This register contains a BD index returned as the result of a POP command on a specific WQ. See the description for the 'last_four_pop_trace_control' register for additional details.

BMU_POP_CMD_TRACE_BD_INDEX2

Bits	Name	Description
11:0	POP_BD_INDEX2	BD index Reset State: 0x00000000

0x30000A4 BMU_POP_CMD_TRACE_BD_INDEX3

Type: read-only
Reset State: 0x00000000

This register contains a BD index returned as the result of a POP command on a specific WQ. See the description for the 'last_four_pop_trace_control' register for additional details.

BMU_POP_CMD_TRACE_BD_INDEX3

Bits	Name	Description
11:0	POP_BD_INDEX3	BD index Reset State: 0x00000000

0x30000AC BMU_BMU_INTERNAL_MEM_TRACE_ADDR

Type: read-only
Reset State: 0x00000000

This register Indicates the head index pointer of where the last BMU command data was written to BMU internal memory

BMU_BMU_INTERNAL_MEM_TRACE_ADDR

Bits	Name	Description
10:0	BMU_INTERNAL_MEM_INDEX	internal BMU memory address that will be used next to store the internal BMU tracing BMU commands and data. In units of BD index. Reset State: 0x00000000

0x30000B0 BMU_RELEASE_ERROR_DETAILS

Type: read-only
Reset State: 0x00000000

When a release error is reported, this register contains PDU index values of current & previous PDUs that caused release error This is debug information

BMU_RELEASE_ERROR_DETAILS

Bits	Name	Description
31:0	RELEASE_ERROR_DETAILS	Bits 31:16 will indicate the previous PDU index Bits 15:0 will indicate the current PDU index Reset State: 0x00000000

0x30000B4 BMU_RELEASE_ERROR_DETAILS_LOW

Type: read-only
Reset State: 0x00000000

When a release error is reported, this register contains debug information

BMU_RELEASE_ERROR_DETAILS_LOW

Bits	Name	Description
23:0	RELEASE_ERROR_DETAILS_LOW	Bit 23: when set, indicates a release of PDU linked list is ongoing when NOT set, bit 22 indicates the ongoing command: Bit 22: when NOT set, indicates a release of BD-PDU command is ongoing when set, indicates a release is ongoing based on a push to the sink WQ: FF That means, this can be a BD-PDU release or a release based on a defrag BD. The BMU will first investigate what the BD type is and process is accordingly. Bits [15:0]: when bit 23 is set: PDU head index of the PDU linked list when bit 23 is NOT set: BD index Reset State: 0x00000000

0x30000B8 BMU_RELEASE_ERROR_DETAILS_HIGH

Type: read-only
Reset State: 0x00000000

When a release error is reported, this register contains debug information It only contains valid info when bit 23 of register release_error_details_low is set

BMU_RELEASE_ERROR_DETAILS_HIGH

Bits	Name	Description
23:0	RELEASE_ERROR_DETAILS_HIGH	Bits [23:16]: number of PDUs in the PDU linked list being released Bits [15:0]: PDU tail index of the PDU linked list Reset State: 0x00000000

0x30000BC BMU_RELEASE_FIFO_ENTRIES

Type: read-only
Reset State: 0x00000000

The register provides insight into how many entries in the release fifo have been used

BMU_RELEASE_FIFO_ENTRIES

Bits	Name	Description
15:8	NR_PDU_LINKS_CHECKED	When a release (integrity) check error is reported, this field can help debug the problem This field will indicate how many PDUs the integrity check has gone down the PDU linked list that is connected to the BD Reset State: 0x00000000
5:0	NR_USED_REL_FIFO_ENTRIES	Reset State: 0x00000000

0x30000C0 BMU_LAST_BD_PREFETCH_HEAD

Type: read-only
Reset State: 0x00000000

The register provides insight info what the last used bd prefetch head was. This information can be useful in case a linked BD list error is reported

BMU_LAST_BD_PREFETCH_HEAD

Bits	Name	Description
26:16	REMAINING_AVAILABLE_BD_FOR_PREFETCH_CNT	Reset State: 0x00000000
10:0	PREFETCH_HEAD_BD_INDEX	Reset State: 0x00000000

0x30000C4 BMU_BD_PREFETCH_HEAD_BD_LINK

Type: read-only
Reset State: 0x00000000

The register provides insight into which BD index was the bd prefetch head was pointing to This information can be useful in case a linked BD list error is reported

BMU_BD_PREFETCH_HEAD_BD_LINK

Bits	Name	Description
10:0	NEXT_PREFETCH_HEAD_BD_INDEX	Reset State: 0x00000000

0x30000C8 BMU_BMU_PUSH_INTEGRITY_ERR_BD_INDEX

Type: read-only
Reset State: 0x00000000

This register indicates the bd index of the BD that was pushed into a WQ, but the integrity check on the BD with linked PDUs failed

BMU_BMU_PUSH_INTEGRITY_ERR_BD_INDEX

Bits	Name	Description
10:0	INTEGRITY_ERR_BD_INDEX	BD index. Reset State: 0x00000000

0x30000CC BMU_BMU_WATCHDOG_TIMEOUT_TIME

Type: read-write
Reset State: 0x0000FFFF

This register indicates the timeout in nr of clock cycles when an ahb access has started but does not get finished

BMU_BMU_WATCHDOG_TIMEOUT_TIME

Bits	Name	Description
19:0	BMU_WATCHDOG_TIMEOUT_TIME	timeout time in nr of clk cycles. When set to zero, the watchdog functionality is disabled Reset State: 0x0000FFFF

0x30000D0 BMU_BMU_SM_STATES_ON_ERROR_LOW

Type: read-only
Reset State: 0x00000000

This register provides a snapshot of the bmu state machines when an error is reported.

BMU_BMU_SM_STATES_ON_ERROR_LOW

Bits	Name	Description
31:0	BMU_SM_STATES_ON_ERROR_LOW	[31:28] = encoded_release_pdu_ctrl_sm_state[3:0]; [27:25] = encoded_release_bd_ctrl_sm_state[2:0]; [24:22] = encoded_release_ctrl_sm_state[2:0]; [21:19] = encoded_pdu_prefetch_mgr_sm_state[2:0]; [18:15] = encoded_bd_prefetch_mgr_sm_state[3:0]; [14:12] = encoded_bd_pdu_mgr_sm_state[2:0]; [11:8] = encoded_integrity_check_state[3:0]; [7:4] = {1'b0, encoded_wq_mgr_state[2:0]}; [3:0] = encoded_gas_interface_sm_state; Reset State: 0x00000000

0x30000D4 BMU_BMU_SM_STATES_ON_ERROR_HIGH

Type: read-only
Reset State: 0x00000000

This register provides a snapshot of the bmu state machines when an error is reported.

BMU_BMU_SM_STATES_ON_ERROR_HIGH

Bits	Name	Description
31	ERROR_CAPTURED	when set, an error state has been captured Reset State: 0x00000000
12:0	BMU_SM_STATES_ON_ERROR_HIGH	[12] = bmu_mcu_err_int; [11] = freeze_bmu_state; [10:4] = test_bus_locally_prefetched_pdu_count[`BMU_HIGH_BIT_PREFETCH_MEM + 1:0]; [3:1] = encoded_prefetch_fifo_ctrl_sm_state[2:0]; [0] = encoded_release_pdu_ctrl_sm_state[4]; Reset State: 0x00000000

0x30000D8 BMU_BMU_PREFETCH_ERROR_DETAILS

Type: read-only
Reset State: 0x00000000

This register provides insight to the error that was reported on an reported prefetch error

BMU_BMU_PREFETCH_ERROR_DETAILS

Bits	Name	Description

31:0	BMU_PREFETCH_ERROR_DETAILS	rdgam_prefetch_pdu_rdata_valid [15:0] = used_pdu_head_index_reg [31:16] = rdgam_prefetch_pdu_rdata[15:0]
		tail_of_pdu_list_reached_based_on_tail_pointer [15:0] = used_pdu_head_index_reg; [23:16] = locally_prefetched_pdu_count_reg; [31:24] = pdu_count_available_for_prefetch[7:0];
		next_tail_of_pdu_list_reached_based_on_pdu_count [15:0] = used_pdu_head_index_reg; [31:16] = local_pdu_head_index_reg;
		Reset State: 0x00000000

0x30000DC BMU_CONTROL3

Type: read-write
Reset State: 0x00000000

This register can be used to control details for the bmu build in BD/PDU integrity checking. The enabling of the overall integrity check is controlled by bits in the control2 register. This register allows that check to tune in into specific WQs (for the push command check) or specific masters (for the release check).

BMU_CONTROL3

Bits	Name	Description
15	PUSH_INTEGRITY_FOR_SPECIF_MASTER_SELECTED	When set, the push WQ integrity check will only be performed on pushes to the WQ identified by "push_integrity_check_wq_nr". Reset State: 0x00000000
12:8	PUSH_INTEGRITY_CHECK_WQ_NR	This is the number of the WQ for which the BD/PDUs pushed into this WQ need to be checked for their integrity. Reset State: 0x00000000
7	RELEASE_INTEGRITY_FOR_SPECIF_MASTER_SELECTED	When set, the release BD/PDU integrity check will only be performed for the master identified by "release_integrity_check_master_id". Reset State: 0x00000000
5:0	RELEASE_INTEGRITY_CHECK_MASTER_ID	This is the id of the master from which the releases need to be checked for it's integrity. Reset State: 0x00000000

0x30000E0 BMU_CONTROL4

Type: read-write
Reset State: 0x00000F28

This register can be used to control the generation of the 'priority' signal to the DAHB arbiter who passes this on to the MIF. This priority setting will help BMU getting faster 'prioritized' access to the MIF memory over other (SYS, mCPU) interfaces to the MIF.

BMU_CONTROL4

Bits	Name	Description
31	PREFETCH_FIFO_ACCESS_PRIORITY_SET	When set, the prefetch fifo priority signal is set, resulting in the MIF giving priority to the DAHB accesses. Reset State: 0x00000000
30	RELEASE_FIFO_ACCESS_PRIORITY_SET	When set, the release fifo priority signal is set, resulting in the MIF giving priority to the DAHB accesses. Reset State: 0x00000000
29	PDU_PREFETCH_ACCESS_PRIORITY_SET	When set, the pdu based prefetch priority signal is set, resulting in the MIF giving priority to the DAHB accesses. Reset State: 0x00000000
28	BD_PREFETCH_ACCESS_PRIORITY_SET	When set, the bd based prefetch priority signal is set, resulting in the MIF giving priority to the DAHB accesses. Reset State: 0x00000000
22:16	NR_OF_PREFETCH_ENTRIES	The number of entries in the PDU prefetch fifo Reset State: 0x00000000

BMU_CONTROL4 (cont.)

Bits	Name	Description
11:8	PREFETCH_FIFO_ACCESS_PRIORITY_THRESHOLD	The 'priority' signal is set when the number of used PDU entries in the prefetch fifo gets below this threshold, and there are still PDUs left that can be prefetched When BMU is operating in the special mode where every 128 byte memory segment can be BD or PDU, the amount of the 'priority' signal is set when the prefetched BDs are below the threshold, and the PDU prefetch fifo has less then this threshold number of used entries. Reset State: 0x0000000F
6:0	RELEASE_FIFO_ACCESS_PRIORITY_THRESHOLD	The 'priority signal is set when the release fifo gets filled above this threshold Reset State: 0x00000028

0x30000E4 BMU_DPU_RSV_STATUS

Type: read-write
Reset State: 0x00000000

This register can be used to observe and clear pending reservation commands that were issued by the dpu to the BMU When a reservation command from the DPU is not granted, the nr of BDs and PDUs that were requested are remembered by the BMU. The BMU uses this number, together with the programmed BD/PDU threshold to control the generation of the bmu_pdu_bd_pdu_avail_for_rsv_req signals for the DPU.

BMU_DPU_RSV_STATUS

Bits	Name	Description
31	BMU_PDU_RX_BD_PDU_AVAIL_CLEAR	When set, will clear the pending DPU rx reservation Reset State: 0x00000000
30	BMU_PDU_RX_BD_PDU_AVAIL_FOR_RSV_REQ	Status of the bmu_pdu_rx_bd_pdu_avail_for_rsv_req signal to the dpu Reset State: 0x00000000
28:24	DPU_RX_PENDING_BD_RSV_REQ	The number of bds the dpu rx has requested Reset State: 0x00000000
23:16	DPU_RX_PENDING_PDU_RSV_REQ	The number of pdus the dpu rx has requested Reset State: 0x00000000
15	BMU_PDU_TX_BD_PDU_AVAIL_CLEAR	When set, will clear the pending DPU tx reservation Reset State: 0x00000000
14	BMU_PDU_TX_BD_PDU_AVAIL_FOR_RSV_REQ	Status of the bmu_pdu_tx_bd_pdu_avail_for_rsv_req signal to the dpu Reset State: 0x00000000
12:8	DPU_TX_PENDING_BD_RSV_REQ	The number of bds the dpu tx has requested Reset State: 0x00000000

BMU_DPU_RSV_STATUS (cont.)

Bits	Name	Description
7:0	DPU_TX_PENDING_PDU_RSV_REQ	The number of pdus the dpu tx has requested Reset State: 0x00000000

0x30000E8 BMU_RECEIVE_DEBUG_CONTROL

Type: read-write
Reset State: 0x00000000

These are debug control registers main for dropping incoming frames for the rxp when this is happening too fast

BMU_RECEIVE_DEBUG_CONTROL

Bits	Name	Description
31	DROP_STATUS	current status of the drop logic When set, frames for wq 2 will be dropped Reset State: 0x00000000
30:16	MIN_INTERVAL_BEFORE_DROP	See minimum_rx_interval_drop_enable Units is in clk cycles Reset State: 0x00000000
15:8	MAX_WQ_ENTRIES_BEFORE_DROP	See max_entries_drop_enable Reset State: 0x00000000
2	BD_WRITE_POINTER_CHECK_DISABLE	When set, the bd write command checks are disabled Reset State: 0x00000000
1	MAX_ENTRIES_DROP_ENABLE	When set, and a push command to the wq2 (RXP) is received which would bring the number of entries in the wq2 above the 'max_wq_entries_before_drop' threshold, the frame will be dropped. Reset State: 0x00000000
0	MINIMUM_RX_INTERVAL_DROP_ENABLE	When set, and 2 sequential push command to the wq2 (RXP) are received within the minimum interval as specified in 'min_interval_before_drop', the second frame will be dropped Reset State: 0x00000000

0x30000EC BMU_BMU_SPARE_REG

Type: read-write
Reset State: 0x00000000

These are reserved bits for future usage

BMU_BMU_SPARE_REG

Bits	Name	Description
15:0	BMU_SPARE_REG	Reset State: 0x00000000

0x30000F0 BMU_BTQM_CONTROL1

Type: read-write
Reset State: 0x00000000

controls BTQM (BMU Transmit Queue Manager) features

BMU_BTQM_CONTROL1

Bits	Name	Description
31	FAST_STAMEM_INIT_STATUS	When set, the fast sta-mem initialization is ongoing Reset State: 0x00000000
28	FAST_STA_MEM_INIT	Writing a 1 to this register bit, the BTQM will initialize the STA mem to all zeros, which means all staids are disabled. It is safest to immediately clear this bit after it was set. Reset State: 0x00000000
27	BTQM_COUNTERS_CLEAR	Writing a 1 to this register bit will clear the btqm related counters This register auto clears. Reset State: 0x00000000
26	CFG_MASK_OFF_APSD_SESSION_ENABLE	When set, the 'get_info_apsd_session_ongoing' signal will never be set. Reset State: 0x00000000
25	CFG_FIXED_BCN_QUEUE_DA_MAPPING	When set, the beacon queueid 0 will always be mapped to BO_DA0, beacon queueid 1 is mapped to BO_DA1, etc. When not set, the same mapping as for the NON beacon STAids is used. Reset State: 0x00000000
24	CFG_CORRECTED_ARBITRATION_ENABLED	When set, the arbitration logic treats the lowest STAid that has data among all STAids that have data for the same queueid, with the same priority as all the others STAids. When NOT set, the lowest STAid that has data among all STAids that have data for the same queueid, might get less opportunity to transmit Reset State: 0x00000000
23	TPE_STATS_BUSY_FLAG_SET_ON_FEEDBACK	When set, the ampdu stats busy signal will be set when a TPE feedback signal is received. It will only get cleared when a BA bitmap has been received and has been fully processed Reset State: 0x00000000
22	APSD_TRIGGER_PM_BIT_SETTING_ENABLE	When set, an incoming apsd frame that has an TID that is of the trigger category, is always considered to be setting the power save status of the STA, irrespective of the pm bit in the frame. Reset State: 0x00000000

BMU_BTQM_CONTROL1 (cont.)

Bits	Name	Description
21	PSPOLL_PM_BIT_SETTING_ENABLE	When set, an incoming pspoll frame is always considered to be setting the power save status of the STA, irrespective of the pm bit in the frame Reset State: 0x00000000
20	APSD_TRIGGER_PM_BIT_MASKING_ENABLE	When set, the PM bit from the received APSD trigger frame is masked off and not interpreted to (properly) indicate the power state of the transmitters STA Reset State: 0x00000000
19	PSPOLL_PM_BIT_MASKING_ENABLE	When set, the PM bit from the received PS-Poll frame is masked off and not interpreted to (properly) indicate the power state of the transmitters STA Reset State: 0x00000000
18	REGISTER_APSD_TRIGGER_WHEN_DA_AVAIL	When set, and QoS Null transmission is NOT enabled as response to an APSD trigger, the APSD trigger will only be registered when there is data in any of the delivery enabled queues Reset State: 0x00000000
17	REGISTER_PSPOLL_TRIGGER_WHEN_DA_AVAIL	When set, and Data Null transmission is NOT enabled as response to a PSPoll, the pspoll trigger will only be registered when there is data in a transmit queue Reset State: 0x00000000
16	ADVANCED_MORE_DATA_BIT_GENERATION_ENABLED	When set, data frames that are pushed into a transmit queue from which a transmission is happening, will be taken into account for the more data bit generation. Reset State: 0x00000000
15	COMBINED_SEARCH_ENABLED	When set, BEACON STA and NON BEACON sta search arbitration will happen in parallel as long as NO NON BEACON sta is in power save mode Reset State: 0x00000000
13	QOS_NULL_TID_SOURCE_IS_TRIGGER_TID	When set, and a qos null frame is transmitted, the TID inserted in the qos null frame is set to the tid field of the trigger frame received. When Not set, the TID inserted in the QoS Null frame will be based on the U-APSD queue with the highest queueid number. Reset State: 0x00000000
12	SW_PROCESSING_OF_PSPOLL_DATA_NULL_ENABLE	When set, and a valid PSPOLL is received, the reception will be registered in the STA descriptor, so that software can find out this trigger was received and the start the handling of it. Reset State: 0x00000000
11	SW_PROCESSING_OF_APSD_QOS_NULL_ENABLE	When set, and a valid APSD trigger is received, the trigger will be registered in the STA descriptor, so that software can find out this trigger was received and the start the handling of it. Reset State: 0x00000000
10	RANDOM_PSPOLL_APSD_TRIGGER_PRIORITY_SCHEDULE_ENABLE	When set, and a valid pspoll or APSD trigger is received, the STA has a 50% chance to be put close to the start of the transmit queue. Reset State: 0x00000000

BMU_BTQM_CONTROL1 (cont.)

Bits	Name	Description
9	PSPOLL_APSD_TRIGGER_PRIORITY_SCHEDULING_ENABLE	When set, and a valid pspoll or APSD trigger is received, the STA is put at close to the start of the transmit queue Reset State: 0x00000000
8	BD_PUSH_OWNERSHIP_CHECK_ENABLE	When set, the ownership check on all the push commands gets enabled Reset State: 0x00000000
7	BD_OWNERSHIP_ASSIGNMENT_DISABLE	When set, the BD_PDU manager module will stop updating the BD ownership assignment when a BD is taken out of the BD idle list and handed over to an other module. Disabling this feature reduces the overhead on the BD SRAM memory Reset State: 0x00000000
6	BD_OWNERSHIP_CHECK_ENABLE	When set, the will start assigning and tracking who owns a BD. There are 4 owners: 0: BD idle list 1: External module 2: WQ managed by the BMU 3: BTQM transmit WQ Reset State: 0x00000000
5	APSD_AMPDU_BA_SUPPORT_ENABLED	When set, the BTQM can handle BA policy transmissions while APSD is enabled. Frames can be aggregated in an AMPDU. Reset State: 0x00000000
4	BTQM_RXP_PWR_INTERFACE_ENABLE	When set, the BMU interface to the RXP related to the power state processing of a station processing is enabled Reset State: 0x00000000
3	BTQM_RXP_BA_INTERFACE_ENABLE	When set, the BMU interface to the RXP related to the Block Ack bitmap processing is enabled Reset State: 0x00000000
2	BTQM_TPE_INTERFACE_ENABLE	When set, the BMU interface to the TPE is enabled Reset State: 0x00000000
1	BTQM_QUEUEING_CTRL_LP_ENABLE	When set, the btqm will start popping frames out of the low priority BTQM entrance WQ 26 and pushing them into the Transmit WQs Reset State: 0x00000000
0	BTQM_QUEUEING_CTRL_HP_ENABLE	When set, the btqm will start popping frames out of the high priority BTQM entrance WQ 25 and pushing them into the Transmit WQs Reset State: 0x00000000

0x30000F4 BMU_BTQM_CONTROL2

Type: read-write
Reset State: 0x00000000

controls BTQM (BMU Transmit Queue Manager) features

BMU_BTQM_CONTROL2

Bits	Name	Description
31	CFG_BA_PARTIAL_BITMAP_UPDATE	When set, and an AMPDU session, if BA is received without sending BAR (Partial bitmap) and received BA SSN is greater than current SSN the frames are not dropped. Reset State: 0x00000000
30	CFG_SW_OWNERSHIP_HAS_PRIORITY	When set, the software access should be getting higher priority over the other ownership request accesses Reset State: 0x00000000
29	CFG_SENT_QOS_NULL_AFTER_EOSP_WITH_RETRY_DROP	When set, and an AMPDU session exchange with the TPE is ongoing for which the EOSP gets set, and any frame for which the EOSP was set gets dropped because the max retry count is reached, the BMU will set the internal' QoS data sent flag, so that when no BA is received in which frames get acknowledged, only one more QoS Null frame will be sent, and not any more data frames. Reset State: 0x00000000
28	CFG_DATA_NULL_SENT_HIGH_PRIORITY_ENABLE	When set, and a data null frame has been sent, but has not yet been acknowledged, the frame will be resent with high priority. Reset State: 0x00000000
27	CFG_QOS_NULL_SENT_HIGH_PRIORITY_ENABLE	When set, and a qos null frame has been sent, but has not yet been acknowledged, the frame will be resent with high priority. Reset State: 0x00000000
26	CFG_AMPDU_APSD_MISSING_EOSP_HANDLING_ENABLE	When set, more frames get acknowledged by an BA then the Remaining frame count and NO EOSP was sent (which should not have happened), the BTQM will force a QOS NULL to be sent next, with the EOSP bit set. Reset State: 0x00000000
25	CFG_END_APSD_AFTER_BA_APSD_EOSP_SENT	When set, and an APSD session with BA is ongoing and an EOSP was set, and the BA gets received, the APSD session will be ended independent of how many frames were acknowledged Reset State: 0x00000000
24	CFG_SEND_QOSNULL_AFTER_BA_APSD_EOSP_SENT	When set, and an APSD session with BA is ongoing and an EOSP was set, and the BA gets received, a QoS null will be sent if the BA is not confirming all frames to be ACKED. Reset State: 0x00000000
10:0	BTQM_QUEUEID_QUEUE_ENABLE	When set, the corresponding queueid transmission is enabled. Bit zero corresponds with queueid0 This register allows high level blocking of all the transmission of frames out of a particular queueid Reset State: 0x00000000

0x30000F8 BMU_BTQM_STATUS

Type: read-only
Reset State: 0x00000000

This register indicates the status of several BTQM features

BMU_BTQM_STATUS

Bits	Name	Description
3	BTQM_TPE_INT_STATUS	When set, the BTQM TPE interface is active providing the TPE queue related information. Reset State: 0x00000000
2	BTQM_ARBITER_STATUS	When set, the BTQM arbiter is active searching for the next STA to transmit a new frame from Reset State: 0x00000000
1	BTQM_BA_HANDLER_STATUS	When set, the BTQM Block Ack handler is processing a Block ACK bitmap Reset State: 0x00000000
0	BTQM_QUEUE_CTRL_STATUS	When set, the BTQM queue controller is active popping a frame out of one of the BTQM entrance WQs and pushing them into the transmit WQs Reset State: 0x00000000

0x30000FC BMU_BTQM_STA_ENABLE_DISABLE_CONTROL

Type: read-write
Reset State: 0x00000000

Controls the enabling or disabling of a STA Whenever a value is written into this register, the BTQM will process the STA settings that came with it. A status bit will indicate if the BTQM is still processing an 'update' command. The next update command should not be issued till the status bit has been cleared. Note that this can sometimes take quite a while. If for example just before a STA-disable command, a transmit exchange sequence with that STA had started, that transmit exchange sequence will be allowed to finish first. This is done to prevent abnormal abortion of sequences.

BMU_BTQM_STA_ENABLE_DISABLE_CONTROL

Bits	Name	Description
31	STA_UPDATE_STATUS	When set to one, BTQM is processing the last STAid configuration command written to this register. Reset State: 0x00000000

BMU_BTQM_STA_ENABLE_DISABLE_CONTROL (cont.)

Bits	Name	Description
10:8	STA_CONFIGURATION_COMMAND	0x0: Enable the transmit queues, but do NOT enable transmission 001: Enable the transmit queues, AND enable transmission 010: Disable the transmit queues AND disable transmission 011: Disable the transmit queues AND disable transmission AND cleanup any data left in the transmit queues 100: Clear the fileds related to control frames (ps-poll bit, apsd trigger bit, data null sent bit, qos null sent bit, remaining apsd frame count and eosp sent bit 101: Disable transmission, but leave transmit queues enabled AND clear the fields related to control frames ps-poll bit, apsd trigger bit, data null sent bit, qos null sent bit, remaining apsd frame count and eosp sent bit 110: Disable transmission, but leave transmit queues enabled) Reset State: 0x00000000
3:0	STAID	The STAid for which the STA operation is intended. Reset State: 0x00000000

0x3000100 BMU_TRANSMIT_QUEUE_ACCESS_CONTROL1

Type: read-write
Reset State: 0x00000000

Selects the queue to access

BMU_TRANSMIT_QUEUE_ACCESS_CONTROL1

Bits	Name	Description
11:8	QUEUEID	Reset State: 0x00000000
3:0	STAID	Reset State: 0x00000000

0x3000104 BMU_TRANSMIT_QUEUE_ACCESS_CONTROL2

Type: read-write
Reset State: 0x00000000

Part 1 of the queue information to write back to the bmu Note that this format corresponds to the first word of the TX queue info in MIF memory

BMU_TRANSMIT_QUEUE_ACCESS_CONTROL2

Bits	Name	Description
31	PREV_TX_DROP_SETTING	Reset State: 0x00000000
30	BAR_REQ_SETTING	Reset State: 0x00000000

BMU_TRANSMIT_QUEUE_ACCESS_CONTROL2 (cont.)

Bits	Name	Description
10:0	NR_OF_FRAMES_IN_QUEUE	Reset State: 0x00000000

0x3000108 BMU_TRANSMIT_QUEUE_ACCESS_CONTROL3

Type: read-write
Reset State: 0x00000000

Part 2 of the queue information to write back to the bmu Note that this format corresponds to the second word of the TX queue info in MIF memory

BMU_TRANSMIT_QUEUE_ACCESS_CONTROL3

Bits	Name	Description
26:16	QUEUE_HEAD_BD_INDEX	Reset State: 0x00000000
10:0	QUEUE_TAIL_BD_INDEX	Reset State: 0x00000000

0x300010C BMU_TRANSMIT_QUEUE_ACCESS_CONTROL4

Type: read-write
Reset State: 0x80000000

controls what kind of access will happen on the transmit queue

BMU_TRANSMIT_QUEUE_ACCESS_CONTROL4

Bits	Name	Description
31	ACCESS_DONE	When set, the queue access control action has finished. Reset State: 0x00000001
0	READ_WRITE_CONTROL	Only valid when 'set_frame_drop_indication' is NOT set When 'read_write_control' is set to 1, a transmit queue read access is initialized The read result will be available in registers 'transmit_queue_access_control5' and 6, after the 'access done' bit is set. When set to 0, a transmit queue write access is initialized. The data that is present in the registers 'transmit_queue_access_control1' and 2, is written back to the transmit queue maintained by the BTQM Reset State: 0x00000000

0x3000110 BMU_TRANSMIT_QUEUE_ACCESS_CONTROL5

Type: read-only
Reset State: 0x00000000

Part 1 of the queue information read from the bmu. Only valid after the 'access done' bit is set in 'transmit_queue_access_control4' Note that this format corresponds to the firxt word of the TX queue info in MIF memory

BMU_TRANSMIT_QUEUE_ACCESS_CONTROL5

Bits	Name	Description
31	PREV_TX_DROP_SETTING	Reset State: 0x00000000
30	BAR_REQ_SETTING	Reset State: 0x00000000
10:0	NR_OF_FRAMES_IN_QUEUE	Reset State: 0x00000000

0x3000114 BMU_TRANSMIT_QUEUE_ACCESS_CONTROL6

Type: read-only
Reset State: 0x00000000

Part 2 of the queue information read from the bmu. Only valid after the 'access done' bit is set in 'transmit_queue_access_control4' Note that this format corresponds to the second word of the TX queue info in MIF memory

BMU_TRANSMIT_QUEUE_ACCESS_CONTROL6

Bits	Name	Description
26:16	QUEUE_HEAD_BD_INDEX	Reset State: 0x00000000
10:0	QUEUE_TAIL_BD_INDEX	Reset State: 0x00000000

0x3000118 BMU_BD_INDEX_INFO_ACCESS_CONTROL1

Type: read-write
Reset State: 0x00000000

Selects the bd index to access

BMU_BD_INDEX_INFO_ACCESS_CONTROL1

Bits	Name	Description
31	BD_INDEX_INFO_ACCESS_STATUS	When set, the BD index memory access is ongoing. The read data will not be valid until this bit is cleared. No new bd index command should be given when this bit is set. Reset State: 0x00000000
16	BD_INDEX_UPDATE	When set, the BD index info in BMU memory will be updated with the data given in registers 'bd_index_info_access_control2 - 4' When NOT set, the BD index info will be read from the BMU memory and will be made available in registers: 'bd_index_info_access_control5 - 7' Reset State: 0x00000000
10:0	BD_INDEX	The bd index for which the BD index info needs to be read or written Reset State: 0x00000000

0x300011C BMU_BD_INDEX_INFO_ACCESS_CONTROL2

Type: read-write
Reset State: 0x00000000

Part 1 of the bd index information to write back to the bmu

BMU_BD_INDEX_INFO_ACCESS_CONTROL2

Bits	Name	Description
31:0	BD_INDEX_INFO_0	Reset State: 0x00000000

0x3000120 BMU_BD_INDEX_INFO_ACCESS_CONTROL3

Type: read-write
Reset State: 0x00000000

Part 2 of the bd index information to write back to the bmu

BMU_BD_INDEX_INFO_ACCESS_CONTROL3

Bits	Name	Description
31:0	BD_INDEX_INFO_1	Reset State: 0x00000000

0x3000124 BMU_BD_INDEX_INFO_ACCESS_CONTROL4

Type: read-write
Reset State: 0x00000000

Part 3 of the bd index information to write back to the bmu

BMU_BD_INDEX_INFO_ACCESS_CONTROL4

Bits	Name	Description
5:0	BD_INDEX_INFO_2	Reset State: 0x00000000

0x3000128 BMU_BD_INDEX_INFO_ACCESS_CONTROL5

Type: read-only
Reset State: 0x00000000

Part 1 of the bd index information read from the bmu. Only valid after the 'access done' bit is set in 'bd_index_info_access_control5'

BMU_BD_INDEX_INFO_ACCESS_CONTROL5

Bits	Name	Description
31:0	BD_INDEX_INFO_0	Reset State: 0x00000000

0x300012C BMU_BD_INDEX_INFO_ACCESS_CONTROL6

Type: read-only
Reset State: 0x00000000

Part 2 of the bd index information read from the bmu. Only valid after the 'access done' bit is set in 'bd_index_info_access_control5'

BMU_BD_INDEX_INFO_ACCESS_CONTROL6

Bits	Name	Description
31:0	BD_INDEX_INFO_1	Reset State: 0x00000000

0x3000130 BMU_BD_INDEX_INFO_ACCESS_CONTROL7

Type: read-only
Reset State: 0x00000000

Part 3 of the bd index information read from the bmu. Only valid after the 'access done' bit is set in 'bd_index_info_access_control5'

BMU_BD_INDEX_INFO_ACCESS_CONTROL7

Bits	Name	Description
5:0	BD_INDEX_INFO_2	Reset State: 0x00000000

0x3000134 BMU_BAR_AND_FRAME_DROP_CONTROL

Type: read-write
Reset State: 0x00000000

controls bar indication and frame drop indication This operation complete is indicated by setting bit-31 of transmit_queue_access_control4 register

BMU_BAR_AND_FRAME_DROP_CONTROL

Bits	Name	Description
2	SET_QUEUE_BAR_INDICATION	When set to 1, the BTQM will force the 'BAR request' setting in the indicated transmit queue to be set. This feature should be used when a Block ack session is to be initialized, and with the 'BAR request' setting set, the TPE will be forced to first transmit a BAR frame. Reset State: 0x00000000
1	SET_FRAME_DROP_INDICATION	When set to 1, the BTQM will force the 'drop frame' setting in the indicated transmit queue to be set. Reset State: 0x00000000

0x3000138 BMU_TX_QUEUE_STAID_QUEUEID_CONFIG

Type: read-write
Reset State: 0x00000000

controls the valid STAid and queueid ranges

BMU_TX_QUEUE_STAID_QUEUEID_CONFIG

Bits	Name	Description
19:16	MAX_VALID_QUEUEID	The maximum allowed queueid. When a frame is pushed to a transmit WQ for a queueid higher then the programmed value, an error indication will be generated. Reset State: 0x00000000

BMU_TX_QUEUE_STAID_QUEUEID_CONFIG (cont.)

Bits	Name	Description
11:8	MAX_VALID_STAID	The maximum allowed staid. When a frame is pushed to a transmit WQ for a STAid higher then the programmed value, an error indication will be generated. Reset State: 0x00000000
3:0	NR_OF_BEACON_STAIDS	The number of staids set aside for beacon handling The STAids reserved start from 0. A number of 5 programmed here, means STAids 0, 1, 2, 3, and 4 are set aside for beacon transmission Reset State: 0x00000000

0x300013C BMU_ENHANCED_TRACING_CONTROL1

Type: read-write
Reset State: 0x00000000

Control for the enhance gen5/6 hardware tracing capabilities

BMU_ENHANCED_TRACING_CONTROL1

Bits	Name	Description
31	SW_BMU_HWTRACE_ENABLE	Implemented: When set, tracing is enabled for software data Reset State: 0x00000000
30	BTQM_ARBITER_SEARCH_HWTRACE_ENABLE	Implemented: When set, tracing is enabled for btqm next STA/qid transmission selection Reset State: 0x00000000
29	BTQM_PWR_STATE_HWTRACE_ENABLE	Implemented: When set, tracing is enabled for receive frames pwr state handling Reset State: 0x00000000
28	TPE_BMU_HWTRACE_ENABLE	Implemented: When set, tracing is enabled for signals from the TPE module Reset State: 0x00000000
27	GET_BD_PDU_TRACE_FOR_PDU_ENABLE	Implemented: When set, get bd and pdu command tracing is enabled for GET commands that request at least one PDU Reset State: 0x00000000
26	NAV_UPDATE_TRACE_ENABLE	Implemented: When set, NAV updated (setting or clearing) are registered Reset State: 0x00000000
25	PHYTX_IDLE_TRACE_ENABLE	Implemented: When set, phytx idle level changes are registered Reset State: 0x00000000
24	RXP_PKDET_N_TRACE_ENABLE	Implemented: When set, pktdet_n level changes are registered Reset State: 0x00000000

BMU_ENHANCED_TRACING_CONTROL1 (cont.)

Bits	Name	Description
23	RXP_SECONDARY_CCA_TRACE_ENABLE	Implemented: When set, secondary cca level changes are registered Reset State: 0x00000000
22	RXP_PRIMARY_CCA_TRACE_ENABLE	Implemented: When set, primary cca level changes are registered Reset State: 0x00000000
21	RXP_RPE_BITMAP_UPDATE_TRACE_ENABLE	Implemented: When set, rxp - rpe bitmap update interaction is registered Reset State: 0x00000000
20	RXP_RPE_DUPL_DETECT_TRACE_ENABLE	Implemented: When set, rxp - rpe dupl detect interaction is registered Reset State: 0x00000000
19	BTQM_QUEUEING_CTRL	Implemented: When set, popping of frames by the BTQM transmit queue controller of frames pushed into the BTQM entrance WQs are registered Reset State: 0x00000000
18	TPE_FEEDBACK_CMD_TRACE_ENABLE	Implemented: When set, tpe feedback info is registered Reset State: 0x00000000
17	TPE_GET_BDIDX_CMD_TRACE_ENABLE	Implemented: When set, tpe bd index info command are registered Reset State: 0x00000000
16	TPE_GET_LENGTH_CMD_TRACE_ENABLE	Implemented: When set, tpe get length info command are registered Reset State: 0x00000000
15	TPE_GET_INFO_CMD_TRACE_ENABLE	Implemented: When set, tpe get info command are registered Reset State: 0x00000000
14	DETAILED_BD_IDLE_LIST_PUSH_HW_TRACE_ENABLE	Implemented: When set, every push to the bd idle list is registered Reset State: 0x00000000
13	BTQM_QUEUEING_DROP_FRAME_TRACE_ENABLE	Implemented: When set, frame drops by the BTQM queue controller tracing is enabled Reset State: 0x00000000
12	RELEASE_TPE_INT_FRAME_TRACE_ENABLE	Implemented: When set, release frames from tpe interface tracing is enabled Reset State: 0x00000000
11	RELEASE_DISABLED_STA_QUEUE_TRACE_ENABLE	Implemented: When set, release disabled_sta queue command tracing is enabled Reset State: 0x00000000
10	RELEASE_BA_DROP_TRACE_ENABLE	When set, release ba_drop command tracing is enabled Reset State: 0x00000000
9	RELEASE_SINK_CMD_TRACE_ENABLE	Implemented: When set, release sink command tracing is enabled Reset State: 0x00000000

BMU_ENHANCED_TRACING_CONTROL1 (cont.)

Bits	Name	Description
8	RELEASE_BD_PDU_CMD_TRACE_ENABLE	Implemented: When set, release bd_pdu command tracing is enabled Reset State: 0x00000000
7	RELEASE_PDU_CMD_TRACE_ENABLE	Implemented: When set, release pdu command tracing is enabled Reset State: 0x00000000
6	RELEASE_BD_CMD_TRACE_ENABLE	Implemented: When set, release bd command tracing is enabled Reset State: 0x00000000
5	BD_PDU_RESERVATION_TRACE_ENABLE	Implemented: When set, bd pdu reservation command tracing is enabled Reset State: 0x00000000
4	GET_BD_PDU_TRACE_FOR_BD_ENABLE	Implemented: When set, get bd and pdu command tracing is enabled for GET commands that request at least one BD Reset State: 0x00000000
3	PUSH_CMD_TRACE_ENABLE	Implemented: When set, push command tracing is enabled Reset State: 0x00000000
2	POP_CMD_TRACE_ENABLE	Implemented: When set, pop command tracing is enabled Reset State: 0x00000000
1	TRACE_FREEZE_ON_ERR	Implemented: When set, the tracing memory will freeze when the bmu detects an internal error for which an BMU error interrupt was enabled. Reset State: 0x00000000
0	ENHANCED_TRACING_ENABLE	Implemented: When set, all legacy (gen 4) modes of BMU HW-TRACING are disabled, and the new mode is enabled. In this mode all legacy tracing control bit settings are discarded Reset State: 0x00000000

0x3000140 BMU_BTQM_QUEUE_INFO_BASE_ADDR

Type: read-write
Reset State: 0x00000000

sets the memory address location where the BTQM is going to find the transmit queues

BMU_BTQM_QUEUE_INFO_BASE_ADDR

Bits	Name	Description
31:2	ADDRESS	The memory address where the BTQM is going to find the transmit queues Reset State: 0x00000000

0x3000144 BMU_QOS_QUEUEID_MAPPING1

Type: read-write
Reset State: 0x000000FF

indicates to the BMU which queueids contain QoS frames

BMU_QOS_QUEUEID_MAPPING1

Bits	Name	Description
10:0	QOS_SETTING	When a bit is set, the corresponding queueid will contain QoS frames Reset State: 0x000000FF

0x3000148 BMU_QOS_QUEUEID_MAPPING2

Type: read-write
Reset State: 0x76543210

indicates to the BMU what QoS TID frames are located in a queue. This setting is only valid for a queueid, if the corresponding 'qos_setting' bit for that queue is set.

BMU_QOS_QUEUEID_MAPPING2

Bits	Name	Description
31:28	TID_FOR_QUEUEID7	Reset State: 0x00000007
27:24	TID_FOR_QUEUEID6	Reset State: 0x00000006
23:20	TID_FOR_QUEUEID5	Reset State: 0x00000005
19:16	TID_FOR_QUEUEID4	Reset State: 0x00000004
15:12	TID_FOR_QUEUEID3	Reset State: 0x00000003
11:8	TID_FOR_QUEUEID2	Reset State: 0x00000002
7:4	TID_FOR_QUEUEID1	Reset State: 0x00000001
3:0	TID_FOR_QUEUEID0	Reset State: 0x00000000

0x300014C BMU_QOS_QUEUEID_MAPPING3

Type: read-write
Reset State: 0x00000000

indicates to the BMU what QoS TID frames are located in a queue. This setting is only valid for a queueid, if the corresponding 'qos_setting' bit for that queue is set.

BMU_QOS_QUEUEID_MAPPING3

Bits	Name	Description
11:8	TID_FOR_QUEUEID10	Reset State: 0x00000000
7:4	TID_FOR_QUEUEID9	Reset State: 0x00000000
3:0	TID_FOR_QUEUEID8	Reset State: 0x00000000

0x3000154 BMU_QUEUEID_BO_MAPPING1

Type: read-write
Reset State: 0x44557667

indicates to the BMU how queueid are mapped to BO engines

BMU_QUEUEID_BO_MAPPING1

Bits	Name	Description
30:28	BO_FOR_QUEUEID7	Reset State: 0x00000004
26:24	BO_FOR_QUEUEID6	Reset State: 0x00000004
22:20	BO_FOR_QUEUEID5	Reset State: 0x00000005
18:16	BO_FOR_QUEUEID4	Reset State: 0x00000005
14:12	BO_FOR_QUEUEID3	Reset State: 0x00000007
10:8	BO_FOR_QUEUEID2	Reset State: 0x00000006
6:4	BO_FOR_QUEUEID1	Reset State: 0x00000006
2:0	BO_FOR_QUEUEID0	Reset State: 0x00000007

0x3000158 BMU_QUEUEID_BO_MAPPING2

Type: read-write
Reset State: 0x00000032

indicates to the BMU how queueid are mapped to BO engines

BMU_QUEUEID_BO_MAPPING2

Bits	Name	Description
10:8	BO_FOR_QUEUEID10	Reset State: 0x00000000
6:4	BO_FOR_QUEUEID9	Reset State: 0x00000003
2:0	BO_FOR_QUEUEID8	Reset State: 0x00000002

0x3000160 BMU_FAST_TRACE_READING_CONTROL

Type: read-write
Reset State: 0x00000000

Indicates the start bd index address from which fast trace reading should start programming this field set the trace reading head ptr automatically back to this programmed index

BMU_FAST_TRACE_READING_CONTROL

Bits	Name	Description
26:16	CURRENT_FAST_TRACE_BD_INDEX_ADDRESS	The current bd index used for the next bd index read. This value gets automatically updated to the 'fast_trace_start_bd_index_address' field when that is reprogrammed. This value also gets automatically updated to point to the trace table entry when 'fast_trace_reading_data2' register is read. The hardware takes care of 'wrapping around', when the end of the trace memory has been reached. Reset State: 0x00000000
10:0	FAST_TRACE_START_BD_INDEX_ADDRESS	Reset State: 0x00000000

0x3000164 BMU_FAST_TRACE_READING_DATA0

Type: read-only
Reset State: 0x00000000

returns the lower 32 bits of the bd index data of the bd index indicated in field: current_fast_trace_bd_index_address

BMU_FAST_TRACE_READING_DATA0

Bits	Name	Description
31:0	TRACE_DATA0	The lower 32 bits of the trace data Reset State: 0x00000000

0x3000168 BMU_FAST_TRACE_READING_DATA1

Type: read-only
Reset State: 0x00000000

returns the middle 32 bits of the bd index data of the bd index indicated in field: current_fast_trace_bd_index_address.

BMU_FAST_TRACE_READING_DATA1

Bits	Name	Description
31:0	TRACE_DATA1	The upper X bits of the trace data Reset State: 0x00000000

0x300016C BMU_FAST_TRACE_READING_DATA2

Type: read-only
Reset State: 0x00000000

returns the upper X bits of the bd index data of the bd index indicated in field: current_fast_trace_bd_index_address. Reading from this register, automatically updates the 'current_fast_trace_bd_index_address' field to point to the next entry in the trace table (exact width of this field: TBD)

BMU_FAST_TRACE_READING_DATA2

Bits	Name	Description
31:0	TRACE_DATA2	The upper X bits of the trace data Reset State: 0x00000000

0x3000170 BMU_FAST_BD_LINK_SETUP_CONTROL

Type: read-write
Reset State: 0x00000000

Initiates fast automated linking of BDs

BMU_FAST_BD_LINK_SETUP_CONTROL

Bits	Name	Description
31	CREATE_BD_LINKED_LIST	When writing a 1 to this field, the BMU will start linking all the BDs indicated by the 'bd_start_index' and 'bd_end_index' fields. Reset State: 0x00000000
30	BD_LINK_LIST_CREATION_STATUS	When set, the BMU is still busy creating the BD linked list Reset State: 0x00000000
26:16	BD_END_INDEX	The index of the last BD in the BD linked list to be created by HW Reset State: 0x00000000
10:0	BD_START_INDEX	The index of the first BD in the BD linked list to be created by HW Reset State: 0x00000000

0x3000174 BMU_STA_CONFIG_STATUS1

Type: read-write
Reset State: 0x00000000

Selects the STAid for which the STA parameters need to be read Whenever this register is written, the hardware will start reading or writing the sta parameters related to this staid

BMU_STA_CONFIG_STATUS1

Bits	Name	Description
31	READ_WRITE_STATUS	When set, the hardware is busy retrieving the station information for the last time this register got programmed Reset State: 0x00000000
8	STA_CONFIG_UPDATE	When NOT set, the hardware will read the staid settings When set, the hardware will write back the staid settings as programmed in the 'sta_config_status2' and 'sta_config_status3' registers. Reset State: 0x00000000
3:0	STAID	The STAid for which the station parameters need to be read Reset State: 0x00000000

0x3000178 BMU_STA_CONFIG_STATUS2

Type: read-write
Reset State: 0x00000000

Provides the STA information corresponding to the 'staid' programmed in the 'sta_config_status1' register This register only has valid contents when the 'read_write_status' bit in the 'sta_config_status1' register is NOT set

BMU_STA_CONFIG_STATUS2

Bits	Name	Description
22	EOSP_SENT_STATUS	When set to one, the BTQM has sent a QoS frame for which the EOSP bit in the QoS field was set. This field is used by the BTQM to track the sending of this indicating in case APSD in combination with AMPDU aggregation is used Reset State: 0x00000000
21	QOS_NULL_SENT_ONCE_STATUS	When set to one, the BTQM has sent a QoS Null frame. This field is used to be able to indicate that the previous transmission was not successful, and the next time around the QoS Null will be resent one more time Reset State: 0x00000000

BMU_STA_CONFIG_STATUS2 (cont.)

Bits	Name	Description
20	DATA_NULL_SENT_ONCE_STATUS	When set to one, the BTQM has sent a Data Null frame. This field is used to be able to indicate that the previous transmission was not successful, and the next time around the Data Null will be resent one more time Reset State: 0x00000000
18:16	CURRENT_REMAINING_TX_FRAME_CNT	This value will be taken as the 'current remaining tx frame count'. Typically this value should be set to zero, and access here is only provided for backup or testing purposes When set to a non zero value, it will only be used when also 'current_apsd_trig_received_setting' has been set, and the 'sta_u_apsd_enable' has been set. Reset State: 0x00000000
14	CURRENT_APSD_TRIG_RECEIVED_SETTING	When set to one, the BTQM will assume that an apsd trigger frame has just been received Reset State: 0x00000000
13	CURRENT_PS_POLL_RECEIVED_SETTING	When set to one, the BTQM will assume that a ps_poll frame has just been received Reset State: 0x00000000
12	CURRENT_PWR_STATE_SETTING	When set to one, the BTQM will assume that the STA is in power save mode. Reset State: 0x00000000
10:8	INITIAL_REMAINING_TX_FRAME_CNT	After receiving an APSD trigger frame, the value in this register will represent the number of response frames that will be sent to the STA. A value of 7 indicates, to drain the complete transmit queue Reset State: 0x00000000
6	QOS_NULL_RESP_ENABLE	When set, and an apsd trigger is received and all APSD delivery enabled queues are empty, the BTQM will indicate to the TPE to transmit a QoS null frame Reset State: 0x00000000
5	U_DATA_NULL_RESP_ENABLE	When set, and a ps-poll apsd trigger is received and all the (non APSD deliver enabled) queues are empty, the BTQM will indicate to the TPE to transmit a Data null frame Reset State: 0x00000000
4	STA_U_APSD_TRACK_ENABLE	When set to one, the BTQM will the reception and handling of APSD trigger frames Reset State: 0x00000000
1	STA_TX_ENABLE	When set, transmission for this sta is enabled Reset State: 0x00000000
0	STA_ENABLE	When set, the STAid is enabled Reset State: 0x00000000

0x300017C BMU_STA_CONFIG_STATUS3

Type: read-write
Reset State: 0x00000000

Provides the STA information corresponding to the 'staid' programmed in the 'sta_config_status1' register This register only has valid contents when the 'read_write_status' bit in the 'sta_config_status1' register is NOT set

BMU_STA_CONFIG_STATUS3

Bits	Name	Description
31:16	DELIVERY_ENABLED_TCID_QUEUES	When set, the corresponding TCID is part of the delivery enabled queues. Bit 0 corresponds with TCID 0 Reset State: 0x00000000
15:0	TRIGGER_ENABLED_TCID	When set, and a QoS Data frame of the corresponding TCID is received, the frame will be interpreted as an APSD trigger frame Reset State: 0x00000000

0x3000180 BMU_STA_CONFIG_STATUS4

Type: read-write
Reset State: 0x00000000

Provides the STA information corresponding to the 'staid' programmed in the 'sta_config_status1' register This register only has valid contents when the 'read_write_status' bit in the 'sta_config_status1' register is NOT set

BMU_STA_CONFIG_STATUS4

Bits	Name	Description
10:0	DATA_AVAILABLE	When set, the corresponding queueid queue contains frames Bit 0, corresponds to queueid 0 Bit 1, corresponds to queueid 1 ... Reset State: 0x00000000

0x3000184 BMU_BTQM_ERR_STATUS

Type: read-only
Reset State: 0x00000000

Provides status information on BTQM internal errors

BMU_BTQM_ERR_STATUS

Bits	Name	Description
27	BTQM_POLL_STATUS_TIMER_INT_STATUS	Reset State: 0x00000000
26	STA_CONFIG_DONE_INT_STATUS	Reset State: 0x00000000
25	BTQM_SW_QUEUE_ACCESS_DONE_INT_STATUS	Reset State: 0x00000000
24	STA_CONTROL_UPDATE_DONE_INT_STATUS	Reset State: 0x00000000
23	RESERVED_ERR	Reset State: 0x00000000
22	BTQM_BA_SEQ_NR_GE_TX_SEQ_NR_ERR	Reset State: 0x00000000
21	BTQM_FRAME_DATA_AVAIL_ERR	Reset State: 0x00000000
20	BTQM_FRAME_TIMEOUT_ERR	Reset State: 0x00000000
19	RELEASE_BTQM_LINK_BD_INDEX_ERR	Reset State: 0x00000000
18	SET_PREV_LAST_FRAME_NULL_BD_INDEX_ERR	Reset State: 0x00000000
17	SET_SECOND_FRAME_NULL_BD_INDEX_ERR	Reset State: 0x00000000
16	RELEASE_BD_PDU_CMD_OWNERSHIP_ERR	Reset State: 0x00000000
15	RELEASE_FRAG_BD_CMD_OWNERSHIP_ERR	Reset State: 0x00000000
14	RELEASE_PDU_TO_BD_CMD_OWNERSHIP_ERR	Reset State: 0x00000000
13	BD_PDU_MGR_OWNERSHIP_ERR	Reset State: 0x00000000
12	BTQM_TPE_INT_OWNERSHIP_ERR	Reset State: 0x00000000
11	BTQM_QUEUE_CTRL_OWNERSHIP_ERR	Reset State: 0x00000000
10	BA_HANDLER_OWNERSHIP_ERR	Reset State: 0x00000000
9	RELEASE_BD_OWNERSHIP_ERR	Reset State: 0x00000000
8	PUSH_BD_OWNERSHIP_ERR	Reset State: 0x00000000

BMU_BTQM_ERR_STATUS (cont.)

Bits	Name	Description
7	EMPTY_TX_QUEUE_PREFETCHED_WARNING	Reset State: 0x00000000
6	CONTROL_FRAME_ERR	Reset State: 0x00000000
5	FRAME_FORMAT_ERR	Reset State: 0x00000000
4	INVALID_BD_PARAMETERS_ERR	Reset State: 0x00000000
3	UNEXPECTED_ARBITER_RESULT_WARNING	Reset State: 0x00000000
2	BROKEN_TRANSMIT_QUEUE_LINK_ERR	Reset State: 0x00000000
1	TPE_INTERACTION_ERR	Reset State: 0x00000000
0	LINKED_LIST_ERR	Reset State: 0x00000000

0x3000188 BMU_BTQM_ERR_ENABLE

Type: read-write
Reset State: 0x00DFFF7F

Enables for the BTQM error or warning interrupt generation

BMU_BTQM_ERR_ENABLE

Bits	Name	Description
27	BTQM_POLL_STATUS_TIMER_INT_ENABLE	Reset State: 0x00000000
26	STA_CONFIG_DONE_INT_ENABLE	Reset State: 0x00000000
25	BTQM_SW_QUEUE_ACCESS_DONE_INT_ENABLE	Reset State: 0x00000000
24	STA_CONTROL_UPDATE_DONE_INT_ENABLE	Reset State: 0x00000000
23	RESERVED_ERR_ENABLE	Reset State: 0x00000001
22	BTQM_BA_SEQ_NR_GE_TX_SEQ_NR_ERR_ENABLE	Reset State: 0x00000001
21	BTQM_FRAME_DATA_AVAIL_ERR_ENABLE	Reset State: 0x00000000
20	BTQM_FRAME_TIMEOUT_ERR_ENABLE	Reset State: 0x00000001
19	RELEASE_BTQM_LINK_BD_INDEX_ERR_ENABLE	Reset State: 0x00000001

BMU_BTQM_ERR_ENABLE (cont.)

Bits	Name	Description
18	SET_PREV_LAST_FRAME_NULL_BD_INDEX_ERR_ENABLE	Reset State: 0x00000001
17	SET_SECOND_FRAME_NULL_BD_INDEX_ERR_ENABLE	Reset State: 0x00000001
16	RELEASE_BD_PDU_CMD_OWNERSHIP_ERR_ENABLE	Reset State: 0x00000001
15	RELEASE_FRAG_BD_CMD_OWNERSHIP_ERR_ENABLE	Reset State: 0x00000001
14	RELEASE_PDU_TO_BD_CMD_OWNERSHIP_ERR_ENABLE	Reset State: 0x00000001
13	BD_PDU_MGR_OWNERSHIP_ERR_ENABLE	Reset State: 0x00000001
12	BTQM_TPE_INT_OWNERSHIP_ERR_ENABLE	Reset State: 0x00000001
11	BTQM_QUEUE_CTRL_OWNERSHIP_ERR_ENABLE	Reset State: 0x00000001
10	BA_HANDLER_OWNERSHIP_ERR_ENABLE	Reset State: 0x00000001
9	RELEASE_BD_OWNERSHIP_ERR_ENABLE	Reset State: 0x00000001
8	PUSH_BD_OWNERSHIP_ERR_ENABLE	Reset State: 0x00000001
7	EMPTY_TX_QUEUE_PREFETCHED_WARNING	Reset State: 0x00000000
6	CONTROL_FRAME_ERR_ENABLE	Reset State: 0x00000001
5	FRAME_FORMAT_ERR_ENABLE	Reset State: 0x00000001
4	INVALID_BD_PARAMETERS_ERR_ENABLE	Reset State: 0x00000001
3	UNEXPECTED_ARBITER_RESULT_WARNING	Reset State: 0x00000001
2	BROKEN_TRANSMIT_QUEUE_LINK_ERR_ENABLE	Reset State: 0x00000001
1	TPE_INTERACTION_ERR_ENABLE	Reset State: 0x00000001
0	LINKED_LIST_ERR_ENABLE	Reset State: 0x00000001

0x300018C BMU_BTQM_ERR_STATE

Type: read-only
Reset State: 0x00000000

Provides the BTQM state machine states when a BMU error interrupt is generated

BMU_BTQM_ERR_STATE

Bits	Name	Description
29:0	BTQM_STATES	Snapshot of the btqm state machines states when a BMU error interrupt is generated Reset State: 0x00000000

0x3000190 BMU_BTQM_ERR_STATE2

Type: read-only
Reset State: 0x00000000

Provides part 2 of the BTQM state machine states when a BMU error interrupt is generated

BMU_BTQM_ERR_STATE2

Bits	Name	Description
19:0	BTQM_STATES	Snapshot of the btqm state machines states when a BMU error interrupt is generated Reset State: 0x00000000

0x3000194 BMU_BTQM_TPE_INT_STATS

Type: read-only
Reset State: 0x00000000

Provides status information on the bmu_tpe interface

BMU_BTQM_TPE_INT_STATS

Bits	Name	Description
19	TPE_INTERACTION_ERROR_STATUS	When set, a TPE interface interaction error occurred Reset State: 0x00000000
18:16	TPE_INTERACTION_ERROR_CODE	indicates the first tpe interface interaction error that happened Reset State: 0x00000000
15:8	BO_DATA_AVAIL	status of the data available signals to the TPE Reset State: 0x00000000

BMU_BTQM_TPE_INT_STATS (cont.)

Bits	Name	Description
4:0	TPE_INT_SM_STATE	Represent the state machine state Reset State: 0x00000000

0x30001B0 BMU_BMU_VERSION

Type: read-only
Reset State: 0x00000000

Provides the BMU label version number

BMU_BMU_VERSION

Bits	Name	Description
9:0	BMU_VERSION	Reset State: 0x00000000

0x30001B4 BMU_RETRY_LIMIT_DROP_CNT

Type: read-only
Reset State: 0x00000000

Provides the number of frames that were dropped by the BTQM because the retry limit was reached.

BMU_RETRY_LIMIT_DROP_CNT

Bits	Name	Description
23:0	RETRY_LIMIT_DROP_CNT	Reset State: 0x00000000

0x30001B8 BMU_TPE_DROP_CNT

Type: read-only
Reset State: 0x00000000

Provides the number of frames that were dropped by the BTQM because the TPE gave a 'DROP feedback' command

BMU_TPE_DROP_CNT

Bits	Name	Description
23:0	TPE_DROP_CNT	Reset State: 0x00000000

0x30001BC BMU_BA_HANDLER_ACKED_DROP_CNT

Type: read-only
Reset State: 0x00000000

Provides the number of frames that were dropped by the BTQM BA handler because the frame reception got acknowledged by the BA bitmap

BMU_BA_HANDLER_ACKED_DROP_CNT

Bits	Name	Description
23:0	BA_HANDLER_ACKED_DROP_CNT	Reset State: 0x00000000

0x30001C0 BMU_BA_HANDLER_WINDOW_MOVED_DROP_CNT

Type: read-only
Reset State: 0x00000000

Provides the number of frames that were dropped by the BTQM BA handler because the BA bitmap SSN moved on beyond the frame Sequence number still in the queue

BMU_BA_HANDLER_WINDOW_MOVED_DROP_CNT

Bits	Name	Description
23:0	BA_HANDLER_WINDOW_MOVED_DROP_CNT	Reset State: 0x00000000

0x30001C4 BMU_GET_INFO_CNT

Type: read-only
Reset State: 0x00000000

Provides the number times the BTQM received a 'get_info' command from the TPE

BMU_GET_INFO_CNT

Bits	Name	Description
23:0	GET_INFO_CNT	Reset State: 0x00000000

0x30001C8 BMU_GET_BD_INDEX_CNT

Type: read-only
Reset State: 0x00000000

Provides the number times the BTQM received a 'get_bd_index' command from the TPE

BMU_GET_BD_INDEX_CNT

Bits	Name	Description
23:0	GET_BD_INDEX_CNT	Reset State: 0x00000000

0x30001CC BMU_PWR_SAVE_STA_CNT

Type: read-write
Reset State: 0x00000000

The number of STAs that are in power save mode & bit map for power save stations

BMU_PWR_SAVE_STA_CNT

Bits	Name	Description
31:16	POWER_SAVE_STAS_BIT_MAP	Reset State: 0x00000000
8:0	PWR_SAVE_STA_CNT	Reset State: 0x00000000

0x30001D0 BMU_BTQM_FRAME_CNT

Type: read-only
Reset State: 0x00000000

The number of frames currently managed by the btqm

BMU_BTQM_FRAME_CNT

Bits	Name	Description
10:0	BTQM_FRAME_CNT	Reset State: 0x00000000

0x30001D4 BMU_BTQM_TIMEOUT_CHECK_CTRL

Type: read-write
Reset State: 0x00000000

The number of clk cycles the BTQM is allowed to empty all btqm transmit queues measured from the point where the last frame got pushed into the BTQM When this number is exceeded, an BTQM timeout error interrupt is generated. A value of zero disables this check

BMU_BTQM_TIMEOUT_CHECK_CTRL

Bits	Name	Description
31:0	BTQM_TIMEOUT_CLK_CYCLE_CNT	Reset State: 0x00000000

0x30001D8 BMU_PWR_STATE_CHANGE_INT_CONTROL

Type: read-write
Reset State: 0x00000000

Provides interrupt control and status of STA power state changes

BMU_PWR_STATE_CHANGE_INT_CONTROL

Bits	Name	Description
31	PWR_STATE_CHANGE_INT_AUTO_CLEAR_ENABLE	Reset State: 0x00000000
30	PWR_STATE_CHANGE_INT_OVERFLOW	Reset State: 0x00000000
29	PWR_STATE_STATUS2	Reset State: 0x00000000
28	PWR_STATE_STATUS1	Reset State: 0x00000000
27	PWR_STATE_STATUS0	Reset State: 0x00000000
26	PWR_STATE_ENTRY2_VALID	Reset State: 0x00000000
25	PWR_STATE_ENTRY1_VALID	Reset State: 0x00000000
24	PWR_STATE_ENTRY0_VALID	Reset State: 0x00000000
23:16	STAID_PWR_INT2	Reset State: 0x00000000
15:8	STAID_PWR_INT1	Reset State: 0x00000000
7:0	STAID_PWR_INT0	Reset State: 0x00000000

0x30001DC BMU_BTQM_INTERRUPT_STATUS

Type: read-only
Reset State: 0x00000000

This register indicates the status of BTQM interrupts When one of the corresponding events occur, the status will reflect this. An interrupt is only generated if the interrupt is also enabled (see next register)

BMU_BTQM_INTERRUPT_STATUS

Bits	Name	Description
2	PWRSTATE_DROP_INTERRUPT	When set, the maximum number of frames in a queue for an STA in power save mode has been reached. Reset State: 0x00000000
1	BTQM_QUEUES_EMPTY_INTERRUPT	When set, the BTQM queues have become empty Reset State: 0x00000000
0	PWRSTATE_CHANGE_INTERRUPT	When set, an STA has indicated a power state change Reset State: 0x00000000

0x30001E0 BMU_BTQM_INTERRUPT_ENABLE

Type: read-write
Reset State: 0x00000000

This register controls the enables of BTQM interrupts

BMU_BTQM_INTERRUPT_ENABLE

Bits	Name	Description
2	PWRSTATE_DROP_INTERRUPT_ENABLE	When set, an interrupt will be generated when the maximum number of frames in a queue for an STA in power save mode has been reached. Reset State: 0x00000000
1	BTQM_QUEUES_EMPTY_INTERRUPT_ENABLE	When set, an interrupt will be generated when the BTQM queues have become empty Reset State: 0x00000000
0	PWRSTATE_CHANGE_INTERRUPT_ENABLE	When set, an interrupt will be generated when an STA has indicated a power state change Reset State: 0x00000000

0x30001E4 BMU_PWR_SAVE_DROP_CTRL

Type: read-write
Reset State: 0x00000000

This register controls dropping of frames for an STA in power save mode

BMU_PWR_SAVE_DROP_CTRL

Bits	Name	Description
8	PWR_SAVE_DROP_ENABLE	When set, and the number of frames in a queue for a STA is larger then this 'drop_threshold' number, the frame will be dropped. Reset State: 0x00000000
3:0	PWR_SAVE_DROP_THRESHOLD	When set, an interrupt will be generated when an STA has indicated a power state change Reset State: 0x00000000

0x30001E8 BMU_PWR_SAVE_DROP_INT_CONTROL

Type: read-write
Reset State: 0x00000000

Provides interrupt control and status for the power save frame DROP interrupt generations (For when BTQM starts dropping frames for an STA in power save mode because the max threshold of frames is reached.)

BMU_PWR_SAVE_DROP_INT_CONTROL

Bits	Name	Description
31	DROP_INT_AUTO_CLEAR_ENABLE	Reset State: 0x00000000
30	DROP_INT_OVERFLOW	Reset State: 0x00000000
29	DROP_ENTRY1_VALID	Reset State: 0x00000000
28	DROP_ENTRY0_VALID	Reset State: 0x00000000
25:21	DROP_QUEUEID_PWR_INT1	Reset State: 0x00000000
20:16	DROP_QUEUEID_PWR_INT0	Reset State: 0x00000000
15:8	DROP_STAID_PWR_INT1	Reset State: 0x00000000
7:0	DROP_STAID_PWR_INT0	Reset State: 0x00000000

0x30001EC BMU_BMU_BACKUP_CONTROL

Type: read-write
Reset State: 0x00000000

This register controls backup functionality build into the BMU

BMU_BMU_BACKUP_CONTROL

Bits	Name	Description
4	SW_TRIGGERED_REARBITRAION_ENABLE	When set, BTQM arbiter to force a re-arbitration for the STAs It removes the current selected STAs from all the prefetched queues, and then re-start the arbitration Once rearbitration is done this bit will be cleared Reset State: 0x00000000
3	CFG_CLEAR_DA_ON_FINDING_EMPTY_QUEUE_ENABLE	When set, and an empty queue is prefetched, the data available signal corresponding to that STA/queueid will be cleared Reset State: 0x00000000
2	STA_DA_AVAIL_BACKUP_MODE_ENABLED	When set, on every frame pushed into a queue, all sta da available settings will be set Reset State: 0x00000000
1	ARBITRATION_BACKUP_MODE_ENABLED	When set, on every frame pushed into a queue, all queue da available and min/max values will be set again Reset State: 0x00000000
0	RESERVED	Do NOT set Reset State: 0x00000000

0x30001F0 BMU_BMU_QUEUE_DELAY_ACCESS_CONTROL

Type: read-write
Reset State: 0x0A0A0000

This register to control the access of Queue/Transmit delay parameters

BMU_BMU_QUEUE_DELAY_ACCESS_CONTROL

Bits	Name	Description
28:24	QUEUE_DELAY_RANGE_FIELD_VALUE	Queue delay Bin 0 Range field value for first bin Reset State: 0x0000000A
20:16	TRANSMIT_DELAY_RANGE_FIELD_VALUE	Transmit delay Bin 0 Range field value for first bin Reset State: 0x0000000A
8	READ_MODIFY_WRITE_ZERO	Control to access Queue/Transmit Delay parameters0: Data read only1: After reading the value, data is initialized to zero Reset State: 0x00000000
7	QUEUE_TRANSMIT_DELAY	Control to access Queue/Transmit Delay parameters0: Queue Delay1: Transmit Delay Reset State: 0x00000000
6:3	TID_INDEX	TID access control Reset State: 0x00000000
2:0	BIN_INDEX	Bin access control 000 : Bin-0 001 : Bin-1 . . 101 : Bin-5 Reset State: 0x00000000

0x30001F4 BMU_QUEUE_TRANSMIT_DELAY_VALUE

Type: read-only
Reset State: 0x00000000

Queue/Transmit delay value, and this register access is controlled through "bmu_queue_delay_access_control" register

BMU_QUEUE_TRANSMIT_DELAY_VALUE

Bits	Name	Description
31:0	QUEUE_TRANSMIT_DELAY_VALUE	Reset State: 0x00000000

0x30001F8 BMU_DXE_RX_WQ_INDEX

Type: read-write
Reset State: 0x0000040B

DXE rx WQ index where the received packed are being pushed. BMU keeps track of byte cnt for this WQ for SIF-DXE interface

BMU_DXE_RX_WQ_INDEX

Bits	Name	Description
15:8	DXE_RX_PRIORITY_WQ_INDEX	DXE high WQ index for high priority traffic Reset State: 0x00000004
7:0	DXE_RX_WQ_INDEX	DXE WQ index for normal traffic Reset State: 0x0000000B

0x30001FC BMU_BMU_SIF_DATA_LENGTH

Type: read-only
Reset State: 0x00000000

Number bytes pushed to DXE Rx WQ

BMU_BMU_SIF_DATA_LENGTH

Bits	Name	Description
16	DXE_WQ_DATA_UNDER_FLOW	When this bit is set, SIF transfer byte count is more than DXE WQ data Reset State: 0x00000000

BMU_BMU_SIF_DATA_LENGTH (cont.)

Bits	Name	Description
15:0	BMU_SIF_DATA_LENGTH	Data accumulated in DXE WQ Reset State: 0x00000000

0x3000200 BMU_SW_BMU_DXE_DATA_LENGTH

Type: read-write
Reset State: 0x00000000

Number bytes pushed to DXE Rx WQ

BMU_SW_BMU_DXE_DATA_LENGTH

Bits	Name	Description
15:0	SW_BMU_DXE_DATA_LENGTH	Data length to be added to DXE Rx WQ count Reset State: 0x00000000

0x3000208 BMU_BTQM_PACKET_MEMORY_UNIT_SIZE

Type: read-write
Reset State: 0x00000001

BTQM reports consumed memory in btqm_packet_memory_unit_size*128-bytes

BMU_BTQM_PACKET_MEMORY_UNIT_SIZE

Bits	Name	Description
3:0	BTQM_PACKET_MEMORY_UNIT_SIZE	Reset State: 0x00000001

0x300020C BMU_SW_ACCESS_DEBUG_STATUS

Type: read-only
Reset State: 0x00000000

Software access debug bits

BMU_SW_ACCESS_DEBUG_STATUS

Bits	Name	Description
31	FINAL_BMU_BTQM_CTRL_CLK_ENABLE	Reset State: 0x00000000

BMU_SW_ACCESS_DEBUG_STATUS (cont.)

Bits	Name	Description
29	ARB_QUEUE_PREFETCH_REQUEST	Reset State: 0x00000000
28	QUEUE_RW_INFO_RETURN_REQUEST	Reset State: 0x00000000
27	QUEUE_RW_INFO_REQUEST	Reset State: 0x00000000
26	BTQM_CTRL_TO_ARB_OWNERSHIP_GRANT	Reset State: 0x00000000
25	ARBITER_QUEUE_OWNERSHIP_GRANT	Reset State: 0x00000000
24	QUEUE_CTRL_OWNERSHIP_GRANT	Reset State: 0x00000000
23	BA_HANDLER_QUEUE_OWNERSHIP_GRANT	Reset State: 0x00000000
22	SW_INT_QUEUE_OWNERSHIP_GRANT	Reset State: 0x00000000
21	FILTERED_ARB_QUEUE_PREFETCH_REQUEST	Reset State: 0x00000000
20	ARB_QUEUE_FLUSH_REQUEST	Reset State: 0x00000000
19	ARBITER_QUEUE_RETURN_QUEUE_OWNERSHIP_REQUEST	Reset State: 0x00000000
18	SW_INT_RETURN_QUEUE_OWNERSHIP_REQUEST	Reset State: 0x00000000
17	QUEUE_CTRL_RETURN_QUEUE_OWNERSHIP_REQUEST	Reset State: 0x00000000
16	BA_HANDLER_RETURN_QUEUE_OWNERSHIP_REQUEST	Reset State: 0x00000000
15	FILTERED_ARBITER_QUEUE_OWNERSHIP_REQUEST	Reset State: 0x00000000
14	FILTERED_SW_INT_QUEUE_OWNERSHIP_REQUEST	Reset State: 0x00000000
13	FILTERED_QUEUE_CTRL_OWNERSHIP_REQUEST	Reset State: 0x00000000
12	FILTERED_BA_HANDLER_QUEUE_OWNERSHIP_REQUEST	Reset State: 0x00000000
11	ARBITER_QUEUE_OWNERSHIP_REQUEST	Reset State: 0x00000000

BMU_SW_ACCESS_DEBUG_STATUS (cont.)

Bits	Name	Description
10	QUEUE_CTRL_OWNERSHIP_REQUEST	Reset State: 0x00000000
9	BA_HANDLER_QUEUE_OWNERSHIP_REQUEST	Reset State: 0x00000000
8	SW_INT_QUEUE_OWNERSHIP_REQUEST	Reset State: 0x00000000
6:4	ENCODED_BTQM_SW_INT_STATE	Reset State: 0x00000000
2:0	ENCODED_BTQM_CTRL_STATE	Reset State: 0x00000000

0x3000210 BMU_BTQM_TX_THRESHOLD

Type: read-write
Reset State: 0x00000080

Controls the memory resources for Tx traffic If the Tx memory usage is greater than equal to this value Any request for BD/PDUs from reserve all command is ignored

BMU_BTQM_TX_THRESHOLD

Bits	Name	Description
10:0	BTQM_MEM_THRESHOLD	Reset State: 0x00000080

0x3000214 BMU_BTQM_STAID_3_TO_0_MEM_STATUS

Type: read-only
Reset State: 0x00000000

BTQM memory status for STAid3 to STAid0. It is multiples of 128bytes. This needs to be multiplied by setting in "btqm_packet_memory_unit_size" register.

BMU_BTQM_STAID_3_TO_0_MEM_STATUS

Bits	Name	Description
31:24	STAID3	Reset State: 0x00000000
23:16	STAID2	Reset State: 0x00000000
15:8	STAID1	Reset State: 0x00000000
7:0	STAID0	Reset State: 0x00000000

0x3000218 BMU_BTQM_STAID_7_TO_4_MEM_STATUS

Type: read-only
Reset State: 0x00000000

BTQM memory status for STAid7 to STAid4. It is multiples of 128bytes. This needs to be multiplied by setting in "btqm_packet_memory_unit_size" register.

BMU_BTQM_STAID_7_TO_4_MEM_STATUS

Bits	Name	Description
31:24	STAID7	Reset State: 0x00000000
23:16	STAID6	Reset State: 0x00000000
15:8	STAID5	Reset State: 0x00000000
7:0	STAID4	Reset State: 0x00000000

0x300021C BMU_BTQM_PKT_MEMORY_STATUS

Type: read-only
Reset State: 0x00000000

BTQM combined memory status for all the stations.

BMU_BTQM_PKT_MEMORY_STATUS

Bits	Name	Description
10:0	BTQM_PKT_MEMORY_STATUS	Reset State: 0x00000000

0x3000220 BMU_HP_RX_MEMORY_UPPER_LIMIT

Type: read-write
Reset State: 0x000000E8

Controls the memory resources for Rx high priority RX traffic. If the Rx memory usage is greater than equal to this value Any request for BD/PDUs from Rx modules is ignored

BMU_HP_RX_MEMORY_UPPER_LIMIT

Bits	Name	Description
10:0	HP_RX_MEMORY_UPPER_LIMIT	Reset State: 0x000000E8

0x3000224 BMU_LP_RX_MEMORY_UPPER_LIMIT

Type: read-write
Reset State: 0x000000D1

Controls the memory resources for Rx high priority RX traffic. If the Rx memory usage is greater than equal to this value Any request for BD/PDUs from Rx modules is ignored

BMU_LP_RX_MEMORY_UPPER_LIMIT

Bits	Name	Description
10:0	LP_RX_MEMORY_UPPER_LIMIT	Reset State: 0x000000D1

0x3000228 BMU_BTQM_STAID_1_TO_0_MEM_THRESHOLD

Type: read-write
Reset State: 0x00000000

BTQM memory threshold for STAid1 to STAid0. It is multiples of 128bytes. BMU generates an interrupt when STAx memory usage is less than this threshold value

BMU_BTQM_STAID_1_TO_0_MEM_THRESHOLD

Bits	Name	Description
25:16	STAID1	Reset State: 0x00000000
9:0	STAID0	Reset State: 0x00000000

0x300022C BMU_BTQM_STAID_3_TO_2_MEM_THRESHOLD

Type: read-write
Reset State: 0x00000000

BTQM memory threshold for STAid3 to STAid2. It is multiples of 128bytes. BMU generates an interrupt when STAx memory usage is less than this threshold value

BMU_BTQM_STAID_3_TO_2_MEM_THRESHOLD

Bits	Name	Description
25:16	STAID3	Reset State: 0x00000000
9:0	STAID2	Reset State: 0x00000000

0x3000230 BMU_BTQM_STAID_5_TO_4_MEM_THRESHOLD

Type: read-write
Reset State: 0x00000000

BTQM memory threshold for STAid5 to STAid4. It is multiples of 128bytes. BMU generates an interrupt when STAx memory usage is less than this threshold value

BMU_BTQM_STAID_5_TO_4_MEM_THRESHOLD

Bits	Name	Description
25:16	STAID5	Reset State: 0x00000000
9:0	STAID4	Reset State: 0x00000000

0x3000234 BMU_BTQM_STAID_7_TO_6_MEM_THRESHOLD

Type: read-write
Reset State: 0x00000000

BTQM memory threshold for STAid7 to STAid6. It is multiples of 128bytes. BMU generates an interrupt when STAx memory usage is less than this threshold value

BMU_BTQM_STAID_7_TO_6_MEM_THRESHOLD

Bits	Name	Description
25:16	STAID7	Reset State: 0x00000000
9:0	STAID6	Reset State: 0x00000000

0x3000238 BMU_BTQM_STAID_15_TO_0_MEM_USAGE_STATUS

Type: read-write
Reset State: 0x00000000

BTQM memory status for STAid15 to STAid0. When the memory usage for STAidX is less than the threshold value the bit will be set

BMU_BTQM_STAID_15_TO_0_MEM_USAGE_STATUS

Bits	Name	Description
31	BMU_MCU_QUEUE_USAGE_THRESHOLD_INTERRUPT_STATUS	Writing one to this register bit will clear the interrupt Reset State: 0x00000000

BMU_BTQM_STAID_15_TO_0_MEM_USAGE_STATUS (cont.)

Bits	Name	Description
30	BMU_MCU_QUEUE_USAGE_THRESHOLD_INTERRUPT_ENABLE	When this bit is set, bmu_mcu_queue_usage_threshold_interrupt is enabled Reset State: 0x00000000
15:0	STAID	Reset State: 0x00000000

0x300023C BMU_POLL_STATUS_TIMER_THRESHOLD

Type: read-write
Reset State: 0x0000FFFF

BTQM poll status threshold, this value represents no.of clock cycles BTQM generates an interrupt when the delay exceeds this value

BMU_POLL_STATUS_TIMER_THRESHOLD

Bits	Name	Description
15:0	POLL_STATUS_TIMER_THRESHOLD	Reset State: 0x0000FFFF

0x3000240 BMU_BMU_IDLE_BD_PDU_STATUS

Type: read-write
Reset State: 0x00000000

BMU keeps track of no.of idle bd/pdus in the system. When this idle bd/pdu number reaches the programmed threshold value it generates an interrupt

BMU_BMU_IDLE_BD_PDU_STATUS

Bits	Name	Description
31	BMU_IDLE_BD_PDU_THRESHOLD_INTERRUPT_STATUS	Writing one to this register bit will clear the interrupt Reset State: 0x00000000
15	BMU_IDLE_BD_PDU_THRESHOLD_INTERRUPT_ENABLE	When this bit is set, bmu_idle_bd_pdu_threshold_interrupt is enabled Reset State: 0x00000000
10:0	BMU_IDLE_BD_PDU_THRESHOLD	Reset State: 0x00000000

0x3000244 BMU_BTQM_STAID_11_TO_8_MEM_STATUS

Type: read-only
Reset State: 0x00000000

BTQM memory status for STAid11 to STAid8. It is multiples of 128bytes. This needs to be multiplied by setting in "btqm_packet_memory_unit_size" register.

BMU_BTQM_STAID_11_TO_8_MEM_STATUS

Bits	Name	Description
31:24	STAID11	Reset State: 0x00000000
23:16	STAID10	Reset State: 0x00000000
15:8	STAID9	Reset State: 0x00000000
7:0	STAID8	Reset State: 0x00000000

0x3000248 BMU_BTQM_STAID_15_TO_12_MEM_STATUS

Type: read-only
Reset State: 0x00000000

BTQM memory status for STAid15 to STAid12. It is multiples of 128bytes. This needs to be multiplied by setting in "btqm_packet_memory_unit_size" register.

BMU_BTQM_STAID_15_TO_12_MEM_STATUS

Bits	Name	Description
31:24	STAID15	Reset State: 0x00000000
23:16	STAID14	Reset State: 0x00000000
15:8	STAID13	Reset State: 0x00000000
7:0	STAID12	Reset State: 0x00000000

0x300024C BMU_BTQM_STAID_9_TO_8_MEM_THRESHOLD

Type: read-write
Reset State: 0x00000000

BTQM memory threshold for STAid9 to STAid8. It is multiples of 128bytes. BMU generates an interrupt when STAx memory usage is less than this threshold value

BMU_BTQM_STAID_9_TO_8_MEM_THRESHOLD

Bits	Name	Description
25:16	STAID9	Reset State: 0x00000000
9:0	STAID8	Reset State: 0x00000000

0x3000250 BMU_BTQM_STAID_11_TO_10_MEM_THRESHOLD

Type: read-write
Reset State: 0x00000000

BTQM memory threshold for STAid11 to STAid10. It is multiples of 128bytes. BMU generates an interrupt when STAx memory usage is less than this threshold value

BMU_BTQM_STAID_11_TO_10_MEM_THRESHOLD

Bits	Name	Description
25:16	STAID11	Reset State: 0x00000000
9:0	STAID10	Reset State: 0x00000000

0x3000254 BMU_BTQM_STAID_13_TO_12_MEM_THRESHOLD

Type: read-write
Reset State: 0x00000000

BTQM memory threshold for STAid13 to STAid12. It is multiples of 128bytes. BMU generates an interrupt when STAx memory usage is less than this threshold value

BMU_BTQM_STAID_13_TO_12_MEM_THRESHOLD

Bits	Name	Description
25:16	STAID13	Reset State: 0x00000000
9:0	STAID12	Reset State: 0x00000000

0x3000258 BMU_BTQM_STAID_15_TO_14_MEM_THRESHOLD

Type: read-write
Reset State: 0x00000000

BTQM memory threshold for STAid15 to STAid14. It is multiples of 128bytes. BMU generates an interrupt when STAx memory usage is less than this threshold value

BMU_BTQM_STAID_15_TO_14_MEM_THRESHOLD

Bits	Name	Description
25:16	STAID15	Reset State: 0x00000000
9:0	STAID14	Reset State: 0x00000000

16.2.37 cahb

0x3000000 CAHB_CAHB_RXP_PL

Type: read-write
Reset State: 0x00000005

cahb Arbiter arbitration priority level for rxp master. In the cahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CAHB_CAHB_RXP_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for rxp master. The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x3000004 CAHB_CAHB_TPE_PL

Type: read-write
Reset State: 0x00000005

cahb Arbiter arbitration priority level for tpe master. In the cahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CAHB_CAHB_TPE_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for tpe master. The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x3000008 CAHB_CAHB_RPE_PL

Type: read-write
Reset State: 0x00000005

cahb Arbiter arbitration priority level for rpe master. In the cahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CAHB_CAHB_RPE_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for rpe master. The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x300000C CAHB_CAHB_RPEM_PL

Type: read-write
Reset State: 0x00000005

cahb Arbiter arbitration priority level for rpem master. In the cahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CAHB_CAHB_RPEM_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for rpem master. The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x3000010 CAHB_CAHB_DPU_PL

Type: read-write
Reset State: 0x00000001

cahb Arbiter arbitration priority level for dpu master. In the cahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CAHB_CAHB_DPU_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for dpu master. The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cahb arbiter will prevent a master from disabling itself. Reset State: 0x00000001

0x3000014 CAHB_CAHB_ADU_PL

Type: read-write
Reset State: 0x00000001

cahb Arbiter arbitration priority level for adu master. In the cahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CAHB_CAHB_ADU_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for adu master. The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cahb arbiter will prevent a master from disabling itself. Reset State: 0x00000001

0x3000018 CAHB_CAHB_CBR_PL

Type: read-write
Reset State: 0x00000004

cahb Arbiter arbitration priority level for cbr master. In the cahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

CAHB_CAHB_CBR_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for cbr master. The lowest priority level is 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the cahb arbiter will prevent a master from disabling itself. Reset State: 0x00000004

0x3000048 CAHB_CAHB_DFLT_MST

Type: read-write
Reset State: 0x00000000

This register identifies the default master for the cahb

CAHB_CAHB_DFLT_MST

Bits	Name	Description
3:0	DFT_MST	Default Master ID number register. The default master is the master that is granted by the bus when no master has requested ownership. NOTE: Writing anything beyond the 4 R/W bits will cause the entire write to be discarded. 0x0: DMY 0x1: RXP 0x2: TPE 0x3: RPE 0x4: RPEM 0x5: DPU 0x6: ADU 0x7: CBR Reset State: 0x00000000

0x3000090 CAHB_CAHB_VERSION

Type: read-only
Reset State: 0x3230382A

ASCII value for each number in the version, followed by '*'. For example 32_30_31_2A represents the version 2.01*.

CAHB_CAHB_VERSION

Bits	Name	Description
31:24	CAHB_COMP_VERSION_BYTE0	Reset State: 0x00000032
23:16	CAHB_COMP_VERSION_BYTE1	Reset State: 0x00000030
15:8	CAHB_COMP_VERSION_BYTE2	Reset State: 0x00000038
7:0	CAHB_COMP_VERSION_BYTE3	Reset State: 0x0000002A

16.2.38 cfg

0x3000000 CFG_CSI_TEMPLATE_DW0

Type: read-write
Reset State: 0x00000000

this register contains first dword of the CSI template

CFG_CSI_TEMPLATE_DW0

Bits	Name	Description
31:0	CFG_TEMPLATE_DW0	First dword of template in stored in register since memory is not big enough. SO this register contains first dword of the template, this is filled by SW. Refer CSI template in to bd_datastructure document for the contents of this dword Reset State: 0x00000000

0x3000004 CFG_CSI_TEMPLATE_MEM

Type: read-write
Reset State: 0x00000000

Registers 000-810 give access to 528 locations of the CSI template that is stored in the local memory refer to BD_Data_structure.doc for template format

CFG_CSI_TEMPLATE_MEM

Bits	Name	Description
31:0	CFG_TEMPLATE_DATA	Check bit 32 of the config register, if it is zero then YOu can either read from any of the locations or write to any of the locations. Reset State: 0x00000000

0x3000844 CFG_CFG_STALL_TIMEOUT

Type: read-write
Reset State: 0x00000A00

Stall timeout functionality - allows CFG to return to idle if PMI interface stalls.

CFG_CFG_STALL_TIMEOUT

Bits	Name	Description
16	STALL_TIMEOUT_EN	Enable stall timeout functionality on the MPI. Reset State: 0x00000000

CFG_CFG_STALL_TIMEOUT (cont.)

Bits	Name	Description
11:0	STALL_TIMEOUT_TIME	Number of cycles of no activity during PMI transaction before stall timeout occurs. Reset State: 0x00000A00

0x3000848 CFG_CFG_CONFIG

Type: read-write
Reset State: 0x00000000

gives some configurations for CFG

CFG_CFG_CONFIG

Bits	Name	Description
31	CSIPROC_REGACCESS_FAIL	when set indicates template is being updates internally hence read or write access failed this needs to be cleared by SW Reset State: 0x00000000
30	CSIPROC_BUSY	when set indicates template is being updates internally Reset State: 0x00000000
29	CSIPROC_TEMPLATE_READY	when set indicates template is ready Reset State: 0x00000000
11	CFG_PHYCLK_TESTBUS_SEL	selects different test buses for CFG in PHY clock domain 0x0: RXIF_BLOCK 0x1: FIFO_PHYCLK_TESTBUS Reset State: 0x00000000
10:8	CFG_TESTBUS_SEL	selects different test buses in CFG in mac clock domain 0x0: CSIPROC_TESTBUS1 0x1: CSIPROC_TESTBUS2 0x2: GAS_TESTBUS 0x3: FIFO_TESTBUS 0x4: MEMIF_TESTBUS 0x5: CONFIG_TESTBUS Reset State: 0x00000000
1	SOFT_PMI_ABORT_EN	Soft PMI abort enable. this is basically to create phy abort thru' software in this case need to make sure stall timeout is enabled Reset State: 0x00000000
0	CFG_CSI_EN	Enables the CSI functionality, by default it is disabled Reset State: 0x00000000

0x300084C CFG_STALL_TIMEOUT_PHY_ABORT_CNT

Type: read-only
Reset State: 0x00000000

Number of times stall timeout occurs with PHY interface. this register also has PHY abort cents

CFG_STALL_TIMEOUT_PHY_ABORT_CNT

Bits	Name	Description
27:24	FIFOFULL_CNT	counts number of times fifo full happened Reset State: 0x00000000
23:16	PHY_CLKSTART_CNT	counts number of clock starts Reset State: 0x00000000
11:8	PHY_ABORT_CNT	PHY Abort Packet Cnt. Reset State: 0x00000000
3:0	STALL_TIMEOUT_COUNT	Number of times the PMI interface encounters a stall timeout Reset State: 0x00000000

0x3000850 CFG_CFG_TESTBUS_LOWER

Type: read-only
Reset State: 0x00000000

This registers gives testbus for lower 32bits

CFG_CFG_TESTBUS_LOWER

Bits	Name	Description
31:0	CFG_TESTBUS_LOWER	lower 32bit of the testbus (31:0) Reset State: 0x00000000

0x3000854 CFG_CFG_TESTBUS_UPPER

Type: read-only
Reset State: 0x00000000

This registers gives bits 44:32 of testbus

CFG_CFG_TESTBUS_UPPER

Bits	Name	Description
12:0	CFG_TESTBUS_UPPER	upper 13bits bits 44:32 of testbus Reset State: 0x00000000

0x3000858 CFG_CFG_SM_STATE

Type: read-only
Reset State: 0x00010001

this register gives the state of the two CFG state machines

CFG_CFG_SM_STATE

Bits	Name	Description
21:16	RXIF_PHY_STATE	RX interface to phy state machine state Reset State: 0x00000001
7:0	CSIPROC_STATE	CSI processing state machine state Reset State: 0x00000001

16.2.39 dahb

0x3000000 DAHB_DAHB_DPUW_PL

Type: read-write
Reset State: 0x00000004

dahb Arbiter arbitration priority level for dpuw master. In the dahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

DAHB_DAHB_DPUW_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for dpuw master. 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the dahb arbiter will prevent a master from disabling itself. Reset State: 0x00000004

0x3000004 DAHB_DAHB_DPUR_PL

Type: read-write
Reset State: 0x00000004

dahb Arbiter arbitration priority level for dpur master. In the dahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

DAHB_DAHB_DPUR_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for dpur master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the dahb arbiter will prevent a master from disabling itself. Reset State: 0x00000004

0x3000008 DAHB_DAHB_BMUW_PL

Type: read-write
Reset State: 0x00000005

dahb Arbiter arbitration priority level for bmuw master. In the dahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

DAHB_DAHB_BMUW_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for bmuw master. 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the dahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x300000C DAHB_DAHB_BMUR_PL

Type: read-write
Reset State: 0x00000005

dahb Arbiter arbitration priority level for bmur master. In the dahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

DAHB_DAHB_BMUR_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for bmur master. 1 and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the dahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x3000010 DAHB_DAHB_ADU_PL

Type: read-write
Reset State: 0x00000002

dahb Arbiter arbitration priority level for adu master. In the dahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

DAHB_DAHB_ADU_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for adu master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the dahb arbiter will prevent a master from disabling itself. Reset State: 0x00000002

0x3000014 DAHB_DAHB_DBR_PL

Type: read-write
Reset State: 0x00000005

dahb Arbiter arbitration priority level for dbr master. In the dahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

DAHB_DAHB_DBR_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for dbr master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the dahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x3000048 DAHB_DAHB_DFLT_MST

Type: read-write
Reset State: 0x00000000

This register identifies the default master for the dahb

DAHB_DAHB_DFLT_MST

Bits	Name	Description
3:0	DFT_MST	Default Master ID number register. The default master is the master that is granted by the bus when no master has requested ownership. NOTE: Writing anything beyond the 4 R/W bits will cause the entire write to be discarded. 0x0: DMY 0x1: DPUW 0x2: DPUR 0x3: BMUW 0x4: BMUR 0x5: ADU 0x6: DBR Reset State: 0x00000000

0x3000090 DAHB_DAHB_VERSION

Type: read-only
Reset State: 0x3230382A

ASCII value for each number in the version, followed by '*'. For example 32_30_31_2A represents the version 2.01*.

DAHB_DAHB_VERSION

Bits	Name	Description
31:24	DAHB_COMP_VERSION_BYTE0	Reset State: 0x00000032
23:16	DAHB_COMP_VERSION_BYTE1	Reset State: 0x00000030
15:8	DAHB_COMP_VERSION_BYTE2	Reset State: 0x00000038
7:0	DAHB_COMP_VERSION_BYTE3	Reset State: 0x0000002A

16.2.40 dpu

0x3000000 DPU_DPU_TXPKTCOUNT

Type: read-write
Reset State: 0x00000000

Total TX packets handled by the PDU

DPU_DPU_TXPKTCOUNT

Bits	Name	Description
15:0	DD_TXPKTCOUNT	Total TX packets handled by the PDU Reset State: 0x00000000

0x3000004 DPU_DPU_RXPKTCOUNT

Type: read-write
Reset State: 0x00000000

Total RX packets handled by the PDU

DPU_DPU_RXPKTCOUNT

Bits	Name	Description
15:0	DD_RXPKTCOUNT	Total RX packets handled by the PDU Reset State: 0x00000000

0x300000C DPU_DPU_BASE_ADDR

Type: read-write
Reset State: 0x00010000

Base address of the DPU data structure

DPU_DPU_BASE_ADDR

Bits	Name	Description
31:0	DD_BASE	Base address of the DPU data structure Reset State: 0x00010000

0x3000010 DPU_DPU_KEYBASE_ADDR

Type: read-write
Reset State: 0x00011000

Base address of the Key data structure

DPU_DPU_KEYBASE_ADDR

Bits	Name	Description
31:0	DD_KEYBASE	Base address of the key data structure Reset State: 0x00011000

0x3000014 DPU_DPU_MICKEYBASE_ADDR

Type: read-write
Reset State: 0x00012000

Base address of the TKIP Mic Key data structure

DPU_DPU_MICKEYBASE_ADDR

Bits	Name	Description
31:0	DD_MICKEYBASE	Base address of the TKIP MIC key data structure Reset State: 0x00012000

0x3000018 DPU_DPU_RCBASE_ADDR

Type: read-write
Reset State: 0x00013000

Base address of the Reply_counter data structure

DPU_DPU_RCBASE_ADDR

Bits	Name	Description
31:0	DD_RCBASE	Base address of the reply-counter data structure Reset State: 0x00013000

0x300001C DPU_DPU_CONTROL

Type: read-write
Reset State: 0x00000006

Holds DPU based configuration fields

DPU_DPU_CONTROL

Bits	Name	Description
31	SP_CLKGATE_DISABLE	Disable clock gating for Security block 0: Clock gating is enabled 1: Clock gating is disabled Reset State: 0x00000000
30	WEP_CLKGATE_DISABLE	Disable clock gating for RC4 engine 0: Clock gating is enabled 1: Clock gating is disabled Reset State: 0x00000000
29	TKIP_CLKGATE_DISABLE	Disable clock gating for TKIP block 0: Clock gating is enabled 1: Clock gating is disabled Reset State: 0x00000000
28	AES_CLKGATE_DISABLE	Disable clock gating for AES engine 0: Clock gating is enabled 1: Clock gating is disabled Reset State: 0x00000000
27	FRAG_CLKGATE_DISABLE	Disable clock gating for fragmentation/defragmentation block 0: Clock gating is enabled 1: Clock gating is disabled Reset State: 0x00000000
26	PDUBD_STALL	DPU is stalled as no PDU/BD's are available and the DPU requires more. 0: DPU is not stalled 1: DPU is stalled Reset State: 0x00000000
25	IGR_BUSY	DPU Egress State-machine is Busy indication. 0: Ingress SM is IDLE. 1: Ingress SM is BUSY. Reset State: 0x00000000
24	EGR_BUSY	DPU Egress State-machine is Busy indication. 0: Egress SM is IDLE. 1: Egress SM is BUSY. Reset State: 0x00000000
23	SP_BUSY	Encryption/Decryption engine is Busy indication. 0: SP is IDLE. 1: SP is BUSY. Reset State: 0x00000000
18	WAPI_BUSY	WAPI Encryption/Decryption engine is Busy indication. 0: WAPI is IDLE. 1: WAPI is BUSY. Reset State: 0x00000000
17	SP_RC4_BUSY	RC4 Encryption/Decryption engine is Busy indication. 0: SP is IDLE. 1: SP is BUSY. Reset State: 0x00000000
16	SP_AES_BUSY	AES Encryption/Decryption engine is Busy indication. 0: SP is IDLE. 1: SP is BUSY. Reset State: 0x00000000
15	WAPI_CLKGATE_DISABLE	Disable clock gating for WAPI engine 0: Clock gating is enabled 1: Clock gating is disabled Reset State: 0x00000000
14	CSR_CLKGATE_DISABLE	Disable clock gating for config reg module 0: Clock gating is enabled 1: Clock gating is disabled Reset State: 0x00000000

DPU_DPU_CONTROL (cont.)

Bits	Name	Description
13	WAPI_REVERSE_IV_ENDIAN_RX	This bit reverses the endianess of WAPI replay counter in rx direction Reset State: 0x00000000
12	INCL_PN_IN_BD_EN	By enabling this bit, DPU writes the packet number in BD(0x38) when replay check is disabled Reset State: 0x00000000
11	WAPI_REVERSE_IV_ENDIAN_TX	This bit reverses the endianess of WAPI replay counter in tx direction Reset State: 0x00000000
10	WAPI_QOS_EN	This bit enables wapi QoS field to calculate MIC value Reset State: 0x00000000
9	RHS_WINCHK_EN	This bit enables right hand side window check Reset State: 0x00000000
8	WQ_TX_RSV_EN	This bit enables reservations on for TX WQ's Reset State: 0x00000000
7	WQ_RX_RSV_EN	This bit enables reservations on for RX WQ's Reset State: 0x00000000
6	DROP_EQ_LEN	Setting this bit drops all envelope only received packets 0: Removes the envelope and passes zero byte packet to Host 1: Drops all envelope only received packets Reset State: 0x00000000
5	ROUTING_FLAG_EN	Setting this bit overrides the BD routing flag 0: Packet will be routed to the value set in BD 1: Packet will be routed to the value set in routing flag register Reset State: 0x00000000
3	SEQUENCE_NO_INS_EN	Setting this bit enables inserting of DPU generated sequence no in frame control 0: Sequence no from Host is passed on 1: Inserts Sequence number generated by DPU Reset State: 0x00000000
2	RX_TAG_CHK_EN	Setting this bit enables BD TAG checking against the DPU TAG for RX packets 0: Don't check BD and DD tag on RX 1: Do check BD and DD tag on RX Reset State: 0x00000001
1	TX_TAG_CHK_EN	Setting this bit enables BD TAG checking against the DPU TAG for TX packets 0: Don't check BD and DD tag on TX 1: Do check BD and DD tag on TX Reset State: 0x00000001
0	WQ_ARB_MODE	Setting this bit selects the arbitration scheme of the Work Queues (WQ). 0: Arbitration priority is ordered RX0->RX7 followed by TX0->TX7, i.e., RX WQ's have higher priority than TX WQ's 1: Arbitration priority is ordered RX0,TX0,RX1,TX1,RX2,TX2,etc.,i.e., RX WQ 0 has higher priority than TX WQ 0, which has higher priority than RX WQ 1 and so on. Reset State: 0x00000000

0x3000020 DPU_DPU_INTERRUPT_MASK

Type: read-write
Reset State: 0x00000000

Enables/Disables the DPU interrupts

DPU_DPU_INTERRUPT_MASK

Bits	Name	Description
31	EGR_WR_ERROR	Setting this bit enables the EGR State Machine Error interrupt. The interrupt occurs when the DPU egress state-machine enters the error state. Such errors are triggered by errors on the Write AHB bus, which should not happen. The DPU does not handle these errors and may result in a DPU lock up. 0: Disabled 1: Enabled Reset State: 0x00000000
30	EGR_GBI_ERROR	Setting this bit enables the EGR State Machine Error interrupt. The interrupt occurs when the DPU egress state-machine enters the error state. Such errors are triggered by errors on the Command AHB bus, which should not happen. The DPU does not handle these errors and may result in a DPU lock up. 0: Disabled 1: Enabled Reset State: 0x00000000
29	IGR_ERROR	Setting this bit enables the IGR State Machine Error interrupt. The interrupt occurs when the DPU ingress state-machine enters the error state. Such errors are triggered by errors on the Read AHB bus, which should not happen. The DPU does not handle these errors and may result in a DPU lock up. 0: Disabled 1: Enabled Reset State: 0x00000000
28	PDUBD_STALL	Setting this bit enables the PDU/BD Stalled interrupt. The interrupt occurs when the DPU requires BD/PDU's but none are available. 0: Disabled 1: Enabled Reset State: 0x00000000
27	WATCHDOG_TIMER	Setting this bit enables the Watchdog Timer interrupt. The interrupt occurs when the Watchdog timer reaches is programmable threshold. 0: Disabled 1: Enabled Reset State: 0x00000000
24	DPU_WAKEUPHOST_EN	Setting this bit enables the wake-up host interrupt In WoWL mode whenever it detects magic packet the interrupt bit is set 0: Disabled 1: Enabled Reset State: 0x00000000
23	MIC_ERR_EN	Setting this bit enables the MIC error interrupt. The interrupt occurs when a TKIP MIC is detected as errored. 0: Disabled 1: Enabled Reset State: 0x00000000
20:0	PKT_ERR_EN	The state of each bit enables/disables an interrupt for the corresponding Packet Error Code. The interrupt occurs when a packet Error is detected. 0: Disabled (per-bit) 1: Enabled (per-bit) Reset State: 0x00000000

0x3000024 DPU_DPU_INTERRUPT_STATUS

Type: read-only
Reset State: 0x00000000

Returns the status of the DPU interrupts

DPU_DPU_INTERRUPT_STATUS

Bits	Name	Description
31	EGR_WR_ERROR	This bit indicates the status of the EGR State Machine Error interrupt. The event occurs when the DPU egress state-machine enters the error state. Such errors are triggered by errors on the Write AHB bus which, should not happen. The DPU does not handle these errors and may result in a DPU lock up. 0: Disabled 1: Enabled Reset State: 0x00000000
30	EGR_GBI_ERROR	This bit indicates the status of the EGR State Machine Error interrupt. The event occurs when the DPU egress state-machine enters the error state. Such errors are triggered by errors on the Command AHB bus which, should not happen. The DPU does not handle these errors and may result in a DPU lock up. 0: Disabled 1: Enabled Reset State: 0x00000000
29	IGR_ERROR	This bit indicates the status of the IGR State Machine Error interrupt. The event occurs when the DPU ingress state-machine enters the error state. Such errors are triggered by errors on the Read AHB bus, which should not happen. The DPU does not handle these errors and may result in a DPU lock up. 0: Disabled 1: Enabled Reset State: 0x00000000
28	PDUBD_STALL	This bit indicates the status of the PDU/BD Stalled interrupt. The event occurs when the DPU requires BD/PDU's but none are available. 0: Disabled 1: Enabled Reset State: 0x00000000
27	WATCHDOG_TIMER	This bit indicates the status of the Watchdog Timer event. The event occurs when the Watchdog timer reaches is programmable threshold. 0: Disabled 1: Enabled Reset State: 0x00000000
23	MIC_ERR	This bit indicates the status of the MIC error event. The event occurs when a TKIP MIC is detected as errored. 0: Disabled 1: Enabled Reset State: 0x00000000

DPU_DPU_INTERRUPT_STATUS (cont.)

Bits	Name	Description
20:0	PKT_ERR	The state of each bit enables/disables an interrupt for the corresponding Packet Error Code. The interrupt occurs when a packet Error is detected. 0: Disabled (per-bit) 1: Enabled (per-bit) 0x2: DPU_BAD_TAG_ERR 0x4: DPU_BAD_BD_ERR 0x20: DPU_FRAG_CNT_ERR 0x40: DPU_BAD_MIC_ERR 0x100: DPU_BAD_DECRYPT_ERR 0x200: DPU_ENV_ONLY_ERR 0x400: DPU_ENV_PART_ERR 0x800: DPU_ZERO_LEN_ERR 0x1000: DPU_BAD_EXTIV_ERR 0x2000: DPU_BAD_KID_ERR 0x4000: DPU_BAD_TSC1_ERR 0x8000: DPU_UNPROT_ERR 0x10000: DPU_PROT_ERR 0x20000: DPU_BAD_RC_ERR 0x40000: DPU_RC_WRAP_ERR 0x80000: DPU_STALL_FLUSH 0x100000: DPU_BD_CHNG_ERR Reset State: 0x00000000

0x3000028 DPU_DPU_BIP_MMIE

Type: read-write
Reset State: 0x00001000

This is the Management MIC Information Element This contains Element ID and Length

DPU_DPU_BIP_MMIE

Bits	Name	Description
15:8	LENGTH	Default this value is 16, This is Length Information Reset State: 0x00000010
7:0	ELEMENT_ID	Default this value is 0, This is MMIE Element ID Reset State: 0x00000000

0x3000048 DPU_DPU_WATCHDOG

Type: read-write
Reset State: 0xFFFF0000

This value represents the DPU watch dog timer and controls. The watchdog self resets to 0 when the DPU is idle and increments by 1 at 128 micro-second intervals when the DPU is not idle. NOTE: The Watchdog does not stop/change the operation of the DPU.

DPU_DPU_WATCHDOG

Bits	Name	Description
31:16	WATCHDOG_THRES	This is the value that if reached the DPU will issue a timeout interrupt. Writing to this register resets the watchdog timer Reset State: 0x0000FFFF
15:0	WATCHDOG_VALUE	This is the current value of the DPU watchdog timer. Reset State: 0x00000000

0x300004C DPU_DPU_BD_IN_COUNTS

Type: read-only
Reset State: 0x00000000

This register provides debug counts of BD's into the DPU

DPU_DPU_BD_IN_COUNTS

Bits	Name	Description
19:16	BD_REQUEST	This is the count of BD's requested by the DPU. Reset State: 0x00000000
3:0	BD_POP	This is the count of BD's poped by the DPU. Reset State: 0x00000000

0x3000050 DPU_DPU_BD_OUT_COUNTS

Type: read-only
Reset State: 0x00000000

This register provides debug counts of BD's out of the DPU

DPU_DPU_BD_OUT_COUNTS

Bits	Name	Description
19:16	BD_RELEASE	This is the count of BD's released by the DPU. Reset State: 0x00000000
3:0	BD_PUSH	This is the count of BD's pushed by the DPU. Reset State: 0x00000000

0x3000054 DPU_DPU_WQ_3_RESERVE

Type: read-write
Reset State: 0x00000110

This register is used to define the number of BD/PDU's the DPU reserves before processing a TX/RX 3 WQ. If the reservation fails the TX/RX 3 to 10 WQ's are disabled from selection until there enough BD/PDU's to satisfy the reservation request. The BD/PDU reservation values must be less than TX/RX 4 WQ reservation values.

DPU_DPU_WQ_3_RESERVE

Bits	Name	Description
12:8	BD_CNT	This the number of BD's the DPU will reserve before processing a WQ 3. Reset State: 0x00000001
6:0	PDU_CNT	This the number of PDU's the DPU will reserve before processing a WQ 3. Reset State: 0x00000010

0x300005C DPU_DPU_WQ_5_RESERVE

Type: read-write
Reset State: 0x00000110

This register is used to define the number of BD/PDU's the DPU reserves before processing a TX/RX 5 WQ. If the reservation fails the TX/RX 5 to 10 WQ's are disabled from selection until there enough BD/PDU's to satisfy the reservation request. The BD/PDU reservation values must be less than TX/RX 6 WQ reservation values.

DPU_DPU_WQ_5_RESERVE

Bits	Name	Description
12:8	BD_CNT	This the number of BD's the DPU will reserve before processing a WQ 5. Reset State: 0x00000001
6:0	PDU_CNT	This the number of PDU's the DPU will reserve before processing a WQ 5. Reset State: 0x00000010

0x3000060 DPU_DPU_WQ_6_RESERVE

Type: read-write
Reset State: 0x00000110

This register is used to define the number of BD/PDU's the DPU reserves before processing a TX/RX 6 WQ. If the reservation fails the TX/RX 6 to 10 WQ's are disabled from selection until there enough BD/PDU's to satisfy the reservation request. The BD/PDU reservation values must be less than TX/RX 7 WQ reservation values.

DPU_DPU_WQ_6_RESERVE

Bits	Name	Description
12:8	BD_CNT	This the number of BD's the DPU will reserve before processing a WQ 6. Reset State: 0x00000001
6:0	PDU_CNT	This the number of PDU's the DPU will reserve before processing a WQ 6. Reset State: 0x00000010

0x3000064 DPU_DPU_WQ_7_RESERVE

Type: read-write
Reset State: 0x00000110

This register is used to define the number of BD/PDU's the DPU reserves before processing a TX/RX 4 WQ. If the reservation fails the TX/RX 7 to 10 WQ's are disabled from selection until there enough BD/PDU's to satisfy the reservation request. The BD/PDU reservation values must be less than TX/RX 8 WQ reservation values.

DPU_DPU_WQ_7_RESERVE

Bits	Name	Description
12:8	BD_CNT	This the number of BD's the DPU will reserve before processing a WQ 7. Reset State: 0x00000001
6:0	PDU_CNT	This the number of PDU's the DPU will reserve before processing a WQ 7. Reset State: 0x00000010

0x3000074 DPU_DPU_ERROR_WQ

Type: read-write
Reset State: 0x0000FF08

This register is used to define two Work Queues to which error packets can be routed. By default, both of these error work queues are set to 0xFF, which is intended to be a 'junk' work queue where data is discarded.

DPU_DPU_ERROR_WQ

Bits	Name	Description
15:8	ERR_WQ_B	This indicates the work queue number for work queue B. Reset State: 0x000000FF
7:0	ERR_WQ_A	This indicates the work queue number for work queue A. Reset State: 0x00000008

0x3000078 DPU_DPU_ERROR_WQ_SELECT

Type: read-write
Reset State: 0x00000000

This register is used to select the work queue routing for error packet with particular error codes. Each error code is represented by a single bit in this register; for example bit 3 is used for selecting routing of packets with error code 3. A set bit will direct error packets with that error code to work queue B. A cleared bit will direct error packets with that error code to work queue A. By default all errors are routed to error work queue A.

DPU_DPU_ERROR_WQ_SELECT

Bits	Name	Description
18:1	ERR_WQ_SELECT	If bit n is set in this field then error packets with error code n are sent to error work queue B; if the bit is clear then they are sent to work queue A. All bit numbers other than valid error codes are reserved and should be left zero. Reset State: 0x00000000

0x300007C DPU_DPU_ERROR_WQ_COUNT

Type: read-write
Reset State: 0x00000000

This register contains counters for errors used to each error work queue. The counts are cleared when it is written.

DPU_DPU_ERROR_WQ_COUNT

Bits	Name	Description
19:16	ERR_WQ_B_CNT	Count of error packets that have been routed to error work queue B. Reset State: 0x00000000
3:0	ERR_WQ_A_CNT	Count of error packets that have been routed to error work queue A. Reset State: 0x00000000

0x3000080 DPU_DPU_FRAG_COUNT

Type: read-write
Reset State: 0x00000000

This register contains counters for fragments received and transmitted. The counts are cleared when it is written.

DPU_DPU_FRAG_COUNT

Bits	Name	Description
31:16	RX_FRAG_CNT	This is a count of fragments de-fragmented by the DPU. Packets that pass through the DPU without being de-fragmented do not increment this count. Reset State: 0x00000000
15:0	TX_FRAG_CNT	This is a count of fragments created by the DPU. Packets that pass through the DPU without being fragmented do not increment this count. Reset State: 0x00000000

0x3000084 DPU_DPU_DBG_TESTBUS_HI

Type: read-write
Reset State: 0x17000000

This register is a debug register and indicates the state of the Testbus high bits and selects the testbus to view

DPU_DPU_DBG_TESTBUS_HI

Bits	Name	Description
31:28	TEST_MODULE_SEL	Selects the different tests bus modules of the DPU. 0x0: NONE 0x1: GBI 0x2: FRAG 0x3: FLOW 0x4: MIC 0x5: SP 0x6: EGR 0x7: IGR 0x8: WDMA 0x9: RDMA 0xA: CSR 0xB: WOW 0xC: WAPI Reset State: 0x00000001

DPU_DPU_DBG_TESTBUS_HI (cont.)

Bits	Name	Description
27:24	TEST_BUS_SEL	Selects the different test buses of the selected module. Reset State: 0x00000007
12:0	TESTBUS_HI	Reset State: 0x00000000

0x3000088 DPU_DPU_DBG_TESTBUS_LO

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the state of the Testbus low bits

DPU_DPU_DBG_TESTBUS_LO

Bits	Name	Description
31:0	TESTBUS_LO	Reset State: 0x00000000

0x300008C DPU_DPU_DBG_WQ_AVAIL

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the state of the WQ available signals

DPU_DPU_DBG_WQ_AVAIL

Bits	Name	Description
31:24	RX_WQ_AVAIL	This indicates the state of the bmu_dpu_dvalid_rx signal Reset State: 0x00000000
17	RX_PDU_AVAIL	This indicates the state of the bmu_dpu_pdu_avail_tx signal Reset State: 0x00000000
16	RX_BD_RSV_AVAIL	This indicates the state of the bmu_dpu_rx_bd_pdu_avail_for_rsv_req signal Reset State: 0x00000000
15:8	TX_WQ_AVAIL	This indicates the state of the bmu_dpu_dvalid_tx Reset State: 0x00000000
1	TX_PDU_AVAIL	This indicates the state of the bmu_dpu_pdu_avail_tx signal Reset State: 0x00000000
0	TX_BD_RSV_AVAIL	This indicates the state of the bmu_dpu_tx_bd_pdu_avail_for_rsv_req signal Reset State: 0x00000000

0x3000090 DPU_DPU_DBG_WQ_ALLOW

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the state of the WQ blocking signals

DPU_DPU_DBG_WQ_ALLOW

Bits	Name	Description
24	WQ_SEL_DIR	This indicates the direction of the current/last selected WQ. Reset State: 0x00000000
23:16	WQ_SEL_IDX	This indicates the current/last selected WQ. Reset State: 0x00000000
15:8	RX_WQ_ALLOW	This indicates the state of allowed RX WQ's to be processed as determined by the reservation logic. Reset State: 0x00000000
7:0	TX_WQ_ALLOW	This indicates the state of allowed TX WQ's to be processed as determined by the reservation logic. Reset State: 0x00000000

0x3000094 DPU_DPU_DBG_SM_STATE

Type: read-only
Reset State: 0x00000000

This registers is a debug register and indicates the state of the DPU state-machines

DPU_DPU_DBG_SM_STATE

Bits	Name	Description
27:23	IGR_IGR_SM	Reset State: 0x00000000
12:8	EGR_EGR_SM	Reset State: 0x00000000
6:4	FRAG_SM_ENC	Reset State: 0x00000000
2:0	FLOW_SM_ENC	Reset State: 0x00000000

0x3000098 DPU_DPU_DBG_BUF_FILL

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the fill level of the internal buffers

DPU_DPU_DBG_BUF_FILL

Bits	Name	Description
17:9	OUTBUF_FILL	Reset State: 0x00000000
8:0	INPBUF_FILL	Reset State: 0x00000000

0x300009C DPU_DPU_DBG_BD_DPU_WORD0

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the BD Word 0 fields relevant to DPU. This also includes the BD Index of the last BD DPU processed.

DPU_DPU_DBG_BD_DPU_WORD0

Bits	Name	Description
31:24	IGR_BD_DPU_RF	Reset State: 0x00000000
23:21	IGR_BD_TAG	Reset State: 0x00000000
20:6	IGR_CUR_BDIDX	Reset State: 0x00000000
5:4	IGR_BD_RX_KID	Reset State: 0x00000000
3	IGR_BD_NE	Reset State: 0x00000000
1:0	IGR_BD_BDT	Reset State: 0x00000000

0x30000A0 DPU_DPU_DBG_BD_DPU_WORD2

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the BD Word 2 fields relevant to DPU.

DPU_DPU_DBG_BD_DPU_WORD2

Bits	Name	Description
31:16	IGR_BD_HDPTR	Reset State: 0x00000000
15:0	IGR_BD_TLPTR	Reset State: 0x00000000

0x30000A4 DPU_DPU_DBG_BD_DPU_WORD3

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the BD Word 3 fields relevant to DPU.

DPU_DPU_DBG_BD_DPU_WORD3

Bits	Name	Description
31:24	IGR_BD_HDRLEN	Reset State: 0x00000000
23:16	IGR_BD_HDRSTRT	Reset State: 0x00000000
15:7	IGR_BD_DTSTRT	Reset State: 0x00000000
6:0	IGR_BD_PDUCNT	Reset State: 0x00000000

0x30000A8 DPU_DPU_DBG_BD_DPU_WORD4

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the BD Word 4 fields relevant to DPU.

DPU_DPU_DBG_BD_DPU_WORD4

Bits	Name	Description
31:16	IGR_BD_MPDULEN	Reset State: 0x00000000
11:8	IGR_BD_TCID	Reset State: 0x00000000

0x30000AC DPU_DPU_DBG_BD_DPU_WORD5

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the BD Word 5 fields relevant to DPU.

DPU_DPU_DBG_BD_DPU_WORD5

Bits	Name	Description
31:24	IGR_BD_DDOFFSET	Reset State: 0x00000000

0x30000D0 DPU_DPU_DBG_DD_WORD_0

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the DD Word 0 fields relevant to DPU.

DPU_DPU_DBG_DD_WORD_0

Bits	Name	Description
27:16	IGR_DD_FRAGSIZE	Reset State: 0x00000000
8:6	IGR_DD_TAG	Reset State: 0x00000000

0x30000D4 DPU_DPU_DBG_DD_WORD_1

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the DD Word 1 fields relevant to DPU.

DPU_DPU_DBG_DD_WORD_1

Bits	Name	Description
31:0	VALUE	Reset State: 0x00000000

0x30000D8 DPU_DPU_DBG_DD_WORD_2

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the DD Word 2 fields relevant to DPU.

DPU_DPU_DBG_DD_WORD_2

Bits	Name	Description
31:0	VALUE	Reset State: 0x00000000

0x30000DC DPU_DPU_DBG_DD_WORD_3

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the DD Word 3 fields relevant to DPU.

DPU_DPU_DBG_DD_WORD_3

Bits	Name	Description
27:24	IGR_DD_RC_BASE_OFFSET	Reset State: 0x00000000
23:16	IGR_DD_MICKEY_OFFSET	Reset State: 0x00000000
15:8	IGR_DD_TX_SPKEY_OFFSET	Reset State: 0x00000000
7:6	IGR_DD_TX_KID	Reset State: 0x00000000
2:0	IGR_SP_MODE	Reset State: 0x00000000

0x30000E0 DPU_DPU_DBG_DD_WORD_4

Type: read-only
Reset State: 0x00000000

This register is a debug register and indicates the DD Word 4 fields relevant to DPU.

DPU_DPU_DBG_DD_WORD_4

Bits	Name	Description
7:0	IGR_DD_RC_OFFSET	Reset State: 0x00000000

0x30000E4 DPU_DPU_WAPIMICKEYBASE_ADDR

Type: read-write
Reset State: 0x00012000

Base address of the WAPI Mic Key data structure

DPU_DPU_WAPIMICKEYBASE_ADDR

Bits	Name	Description
31:0	DD_WAPIMICKEYBASE	Base address of the WAPI MIC key data structure Reset State: 0x00012000

0x30000E8 DPU_DPU_BUG_FIX

Type: read-write
Reset State: 0x00000000

This register holds bug fix controls.

DPU_DPU_BUG_FIX

Bits	Name	Description
2	TKIP_PRIORITY_SEL	Selects the method by which the PRIORITY field is generated for the TKIP MIC calculations. 0: from the BD TID field. PRIORITY = {4'h0,BD_TID} 1: from the QC field. PRIORITY = (QC_VALID) QC[7:0] : 8'h0 Reset State: 0x00000000

0x30000EC DPU_DPU_AES_MASK

Type: read-write
Reset State: 0x80000000

This register holds AES AAD Mask controls.

DPU_DPU_AES_MASK

Bits	Name	Description
31	FRAME_CONTROL_MASK_15	Selects the masking control for Frame Control bit 15 0: Frame Control bit 15 set to 0 1: Frame Control bit 15 set to value in MAC Header Reset State: 0x00000001
7	QOS_MASK_7	Selects the masking control for QOS bit 7 0: QOS bit 7 set to 0 1: QOS bit 7 set to value in MAC Header Reset State: 0x00000000

0x30000F0 DPU_DPU_TKIP_MASK

Type: read-write
Reset State: 0x00000000

This register holds TKIP MIC Mask controls.

DPU_DPU_TKIP_MASK

Bits	Name	Description
7	PRIORITY_MASK_7	Selects the masking control for PRORITY bit 7 0: PRIORITY bit 7 set to 0 1: PRIORITY bit 7 set to value in MAC Header Reset State: 0x00000000

0x30000F4 DPU_DPU_SEQUENCE_NO

Type: read-write
Reset State: 0x00000000

This register holds Sequence number.

DPU_DPU_SEQUENCE_NO

Bits	Name	Description
11:0	SEQUENCE_NO	DPU generated Sequence Number Reset State: 0x00000000

0x30000F8 DPU_DPU_ROUTING_FLAG

Type: read-write
Reset State: 0x0000FF18

This register holds the Routing Flag Value.

DPU_DPU_ROUTING_FLAG

Bits	Name	Description
15:8	WOW_ROUTING_FLAG	Routing flag to rout the packets in WOW mode (This is controlled by wow_routing_flag_en) Reset State: 0x000000FF
7:0	ROUTING_FLAG	Routing flag to rout the packets in WOW mode (This controlled by wow_en) Reset State: 0x00000018

0x30000FC DPU_DPU_HOST_WAKEUP_STATUS_MAGICBD

Type: read-only
Reset State: 0x00000000

This register holds host wakeup reason code and magic BD index Value

DPU_DPU_HOST_WAKEUP_STATUS_MAGICBD

Bits	Name	Description
31:16	MAGIC_PACKET_BD_INDEX	Bd index value for the Magic packet Reset State: 0x00000000
15	HOST_WAKEUP_STATUS	Host wake-up status Reset State: 0x00000000

DPU_DPU_HOST_WAKEUP_STATUS_MAGICBD (cont.)

Bits	Name	Description
6:0	HOST_WAKEUP_REASON_CODE	Host wake-up reason code Reset State: 0x00000000

0x3000100 DPU_DPU_WOW_CONFIG

Type: read-write
Reset State: 0x00000000

Holds WOW based configuration fields

DPU_DPU_WOW_CONFIG

Bits	Name	Description
7	WOW_ROUTING_FLAG_EN	When this bit is enabled 0: 1: Reset State: 0x00000000
6	WOW_PKTERR_EN	When this bit is enabled 0: 1: Reset State: 0x00000000
5	WOW_CHANSWITCH_EN	When this bit is set wow block will also wake up the host if channel switch frame is received 0: 1: When this bit is set wow block will also wake up the host if channel switch frame is received Reset State: 0x00000000
4	WOW_DEAUTH_EN	When this bit is set wow block will also wake up the host if de-authentication packet is received 0: 1: When this bit is set wow block will also wake up the host if de-authentication packet is received Reset State: 0x00000000
3	WOW_DISASS_EN	When this bit is set wow block will also wake up the host if disassociation packet is received 0: 1: When this bit is set wow block will also wake up the host if disassociation packet is received Reset State: 0x00000000
2:1	WOW_MODE	four wow modes from the register data that is programmed by software 00: Magic packet 01: Client only (reserved) 10: AP-Assist(reserved) 11: AP Reset State: 0x00000000
0	WOW_EN	Setting this bit enables/disables the wow mode. 0: WOW blockdisabled 1: WOW block enable Reset State: 0x00000000

0x3000104 DPU_DPU_WOW_TIMERS

Type: read-write
Reset State: 0x00000000

Link down Timer :The value programmed indicates the threshold for consecutive missed beacons. If the timer reaches this value host is woken up. Wake-up Timer : Time out timer if an wakeup even has not occurred and this timer expires we wakeup the host

DPU_DPU_WOW_TIMERS

Bits	Name	Description
31:8	WAKEUP	Reset State: 0x00000000
5:0	LINK_DOWN	Reset State: 0x00000000

0x3000108 DPU_DPU_WOW_MAGIC_PACKET_HI

Type: read-write
Reset State: 0x00000000

This is 48bit mac address that is written by software, this is the pattern that is used for magic packet. It can be any pattern also

DPU_DPU_WOW_MAGIC_PACKET_HI

Bits	Name	Description
15:0	MAGIC_PACKET_47_TO_32	This is 48bit mac address that is written by software Reset State: 0x00000000

0x300010C DPU_DPU_WOW_MAGIC_PACKET_LO

Type: read-write
Reset State: 0x00000000

This is 48bit mac address that is written by software, this is the pattern that is used for magic packet. It can be any pattern also

DPU_DPU_WOW_MAGIC_PACKET_LO

Bits	Name	Description
31:0	MAGIC_PACKET_31_TO_0	This is 48bit mac address that is written by software Reset State: 0x00000000

0x3000110 DPU_WOW_FOUND_MAGIC_COUNTER

Type: read-only
Reset State: 0x00000000

Number of packets received after magic packet has been detected Note That these packets will be pushed to DXE WQ including magic packet, which is something you can verify

DPU_WOW_FOUND_MAGIC_COUNTER

Bits	Name	Description
31:0	VALUE	Reset State: 0x00000000

0x3000114 DPU_WOW_WAITING4MAGIC_COUNTER

Type: read-only
Reset State: 0x00000000

Number of packets received before we detect a magic packet These packets are pushed to drop WQ

DPU_WOW_WAITING4MAGIC_COUNTER

Bits	Name	Description
31:0	VALUE	Reset State: 0x00000000

0x3000118 DPU_WAPI_STA_KEY_INDEX_VALUES

Type: read-only
Reset State: 0x00000000

Station key index values

DPU_WAPI_STA_KEY_INDEX_VALUES

Bits	Name	Description
31:0	VALUE	Reset State: 0x00000000

0x3000120 DPU_WAPI_STA0_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA0_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x3000124 DPU_WAPI_STA1_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA1_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x3000128 DPU_WAPI_STA2_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA2_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x300012C DPU_WAPI_STA3_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA3_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x3000130 DPU_WAPI_STA4_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA4_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x3000134 DPU_WAPI_STA5_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA5_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x3000138 DPU_WAPI_STA6_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA6_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x300013C DPU_WAPI_STA7_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA7_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x3000140 DPU_WAPI_STA8_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA8_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x3000144 DPU_WAPI_STA9_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA9_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x3000148 DPU_WAPI_STA10_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA10_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x300014C DPU_WAPI_STA11_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA11_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x3000150 DPU_WAPI_STA12_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA12_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x3000154 DPU_WAPI_STA13_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA13_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x3000158 DPU_WAPI_STA14_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA14_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

0x300015C DPU_WAPI_STA15_KEY_INDEXES

Type: read-write
Reset State: 0x00000000

This register holds wapi key indexes to map key Ids

DPU_WAPI_STA15_KEY_INDEXES

Bits	Name	Description
31:24	KEY_INDEX3	Key index value to map keyid3 Reset State: 0x00000000
23:16	KEY_INDEX2	Key index value to map keyid2 Reset State: 0x00000000
15:8	KEY_INDEX1	Key index value to map keyid1 Reset State: 0x00000000
7:0	KEY_INDEX0	Key index value to map keyid0 Reset State: 0x00000000

16.2.41 fdahb

0x3000000 FDAHB_FDAHB_RXP_PL

Type: read-write
Reset State: 0x00000004

fdahb Arbiter arbitration priority level for rxp master. In the fdahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

FDAHB_FDAHB_RXP_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for rxp master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the fdahb arbiter will prevent a master from disabling itself. Reset State: 0x00000004

0x3000004 FDAHB_FDAHB_TXP_PL

Type: read-write
Reset State: 0x00000004

fdahb Arbiter arbitration priority level for txp master. In the fdahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

FDAHB_FDAHB_TXP_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for txp master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the fdahb arbiter will prevent a master from disabling itself. Reset State: 0x00000004

0x3000008 FDAHB_FDAHB_TPE_PL

Type: read-write
Reset State: 0x00000004

fdahb Arbiter arbitration priority level for tpe master. In the fdahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

FDAHB_FDAHB_TPE_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for tpe master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the fdahb arbiter will prevent a master from disabling itself. Reset State: 0x00000004

0x300000C FDAHB_FDAHB_FDBR_PL

Type: read-write
Reset State: 0x00000005

fdahb Arbiter arbitration priority level for fdbr master. In the fdahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

FDAHB_FDAHB_FDBR_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for fdbr master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the fdahb arbiter will prevent a master from disabling itself. Reset State: 0x00000005

0x3000010 FDAHB_FDAHB_RPE_PL

Type: read-write
Reset State: 0x00000004

fdahb Arbiter arbitration priority level for rpe master. In the fdahb arbitration scheme the master with highest priority level always wins. Should there be more than one master with the same priority, the winning master will be selected using a round-robin algorithm.

FDAHB_FDAHB_RPE_PL

Bits	Name	Description
3:0	PRIORITY	Arbitration priority for rpe master. and the highest priority level is 15. A priority level of 0 has a special significance, it means that the master is disabled and stops participating in the arbitration scheme. Please note that the fdahb arbiter will prevent a master from disabling itself. Reset State: 0x00000004

0x3000048 FDAHB_FDAHB_DFLT_MST

Type: read-write
Reset State: 0x00000000

This register identifies the default master for the fdahb

FDAHB_FDAHB_DFLT_MST

Bits	Name	Description
3:0	DFT_MST	Default Master ID number register. The default master is the master that is granted by the bus when no master has requested ownership. NOTE: Writing anything beyond the 4 R/W bits will cause the entire write to be discarded. 0x0: DMY 0x1: RXP 0x2: TXP 0x3: TPE 0x4: FDBR 0x5: RPE Reset State: 0x00000000

0x3000090 FDAHB_FDAHB_VERSION

Type: read-only
Reset State: 0x3230382A

ASCII value for each number in the version, followed by '*'. For example 32_30_31_2A represents the version 2.01*.

FDAHB_FDAHB_VERSION

Bits	Name	Description
31:24	FDAHB_COMP_VERSION_BYTE0	Reset State: 0x00000032
23:16	FDAHB_COMP_VERSION_BYTE1	Reset State: 0x00000030
15:8	FDAHB_COMP_VERSION_BYTE2	Reset State: 0x00000038
7:0	FDAHB_COMP_VERSION_BYTE3	Reset State: 0x0000002A

16.2.42 mcu

0x3000000 MCU_BD_PDU_BASE_ADDR

Type: read-write
Reset State: 0x00000000

Sets the memory base address of the BDs and PDUs.

MCU_BD_PDU_BASE_ADDR

Bits	Name	Description
31:7	BD_PDU_BASE_ADDRESS	Base address of the BDs and PDUs. Note that the lowest 8 bits can not be programmed as these bits will always have to be zero. BDs and PDUs are in units of 128 bytes. Reset State: 0x00000000

0x3000004 MCU_MLC_CONTROL

Type: read-write
Reset State: 0x00330000

MAC Loop back Control register

MCU_MLC_CONTROL

Bits	Name	Description
31	MLC_LOOPBACK_ENABLE	When set to 1'b1, the MLC loopback functionality is enabled Reset State: 0x00000000
30	MLC_SNOOPING_ENABLE	When set to 1'b1, the MLC snooping functionality is enabled Reset State: 0x00000000
29	MLC_ADDRESS_SWAP_ENABLE	When set to 1'b1, the MLC will swap address 1 and address2 of the frame received from the TXP Reset State: 0x00000000
23:16	BYTE_FORWARDING_INTERVAL	The number of 160MHz clock cycles in between each data byte requested from the TXP and forwarded to the RXP. A value of 8'd3 corresponds with 315 Mbps. A value of 8'd7 corresponds with 100 mbps. This setting is only used in MLC loopback functionality mode, not snooping mode. bits [17:16] are read only and are always tied to 2'b11 since this is the minimum value that you can program. It is tied to this value preventing user from programming it anything other Reset State: 0x00000033

0x300000C MCU_DBR_STATUS

Type: read-write
Reset State: 0x00000000

Status register of the DBR

MCU_DBR_STATUS

Bits	Name	Description
5	DBR_GAM_ERROR	When set to 1'b1, the gam inside the DBR reported an error to overcome some rtl issue, please write to this bit to clear DBR_incorrect_length_error Reset State: 0x00000000
4	DBR_INCORRECT_LENGTH_ERROR	When set to 1'b1, the DBR reported an error: a module tried an access that was larger then 1 word to overcome some rtl issue, please write to this bit to clear DBR_GAM_error Reset State: 0x00000000

0x3000010 MCU_MCPU_TO_HOST_MB_INT_STAT

Type: read-only
Reset State: 0x00000000

Register indicating for which mailboxes an interrupt to the host is pending.

MCU_MCPU_TO_HOST_MB_INT_STAT

Bits	Name	Description
15:0	MBX_INT_STATUS	Each bit stands for the corresponding mailbox. When set, an interrupt from that Mailbox is pending Reset State: 0x00000000

0x3000014 MCU_HOST_TO_MCPU_MB_INT_STAT

Type: read-only
Reset State: 0x00000000

Register indicating for which mailboxes an interrupt to the mCPU is pending.

MCU_HOST_TO_MCPU_MB_INT_STAT

Bits	Name	Description
15:0	MBX_INT_STATUS	Each bit stands for the corresponding mailbox. When set, an interrupt from that Mailbox is pending Reset State: 0x00000000

0x3000018 MCU_MB0_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the mCPU or to the host.

MCU_MB0_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: mCPU to host, When set to one: host to mCPU Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x300001C MCU_MB0_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt.

MCU_MB0_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb0_control register. This value gets cleared on a mb0 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset. Reset State: 0x00000000

0x3000020 MCU_MB1_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the mCPU or to the host.

MCU_MB1_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: mCPU to host, When set to one: host to mCPU Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x3000024 MCU_MB1_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

MCU_MB1_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb1_control register. This value gets cleared on a mb1 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset. Reset State: 0x00000000

0x3000028 MCU_MB2_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the mCPU or to the host.

MCU_MB2_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver Reset State: 0x00000000
1	INT_DIRECTION	Interrupt direction: When set to zero: mCPU to host, When set to one: host to mCPU Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x300002C MCU_MB2_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt

MCU_MB2_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb2_control register. This value gets cleared on a mb2 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset. Reset State: 0x00000000

0x3000030 MCU_MB3_CONTROL

Type: read-write
Reset State: 0x00000000

General purpose Mailbox register, which can be used to generate interrupts to the mCPU or to the host.

MCU_MB3_CONTROL

Bits	Name	Description
31:2	MAILBOX_VALUE	A 30-bit value from sender to receiver. Reset State: 0x00000000

MCU_MB3_CONTROL (cont.)

Bits	Name	Description
1	INT_DIRECTION	Interrupt direction: When set to zero: mCPU to host, When set to one: host to mCPU Reset State: 0x00000000
0	MB_RESET	When set, all to this MB-related parameters, including the counters, are cleared. Reset State: 0x00000000

0x3000034 MCU_MB3_CONTROL_COUNTERS

Type: read-only
Reset State: 0x00000000

Access counters for tracking the usage and handling of the MB interrupt.

MCU_MB3_CONTROL_COUNTERS

Bits	Name	Description
18:16	WRITE_CNT	A 3-bit value indicating the number of times a none reset write operation has been performed on the mb3_control register. This value gets cleared on a mb3 reset. Reset State: 0x00000000
2:0	READ_CNT	A 3-bit value indicating the number of times a read operation has been performed on the control register of this mailbox This value gets cleared on a MB reset. Reset State: 0x00000000

0x3000098 MCU_MUTEX0

Type: read-only
Reset State: 0x00000101

General purpose semaphore and/or mutex register.

MCU_MUTEX0

Bits	Name	Description
31	RESET	When set, both CURRENTCOUNT and MAXCOUNT fields get initialized with the value written to the MAXCOUNT field. This bit will not get set on a write operation. Reset State: 0x00000000
15:8	MAXCOUNT	The Max count of semaphores available. Can only be set when the Reset bit is written with value 1. Reset State: 0x00000001

MCU_MUTEX0 (cont.)

Bits	Name	Description
7:0	CURRENTCOUNT	Current count of the semaphore. On a read, the current value of the Semaphore is returned and if the CurrentCount > 0, the CurrentCount value is decreased by one. On a write, the current value of the Semaphore is increased by one if the CurrentCount < MaxCount. Reset State: 0x00000001

0x300009C MCU_MUTEX1

Type: read-only
Reset State: 0x00000101

General purpose semaphore and/or mutex register.

MCU_MUTEX1

Bits	Name	Description
31	RESET	When set, both CURRENTCOUNT and MAXCOUNT fields get initialized with the value written to the MAXCOUNT field. This bit will not get set on a write operation. Reset State: 0x00000000
15:8	MAXCOUNT	THe Max count of semaphores available. Can only be set when the Reset bit is written with value 1. Reset State: 0x00000001
7:0	CURRENTCOUNT	Current count of the semaphore. On a read, the current value of the Semaphore is returned and if the CurrentCount > 0, the CurrentCount value is decreased by one. On a write, the current value of the Semaphore is increased by one if the CurrentCount < MaxCount. Reset State: 0x00000001

0x30000A0 MCU_MUTEX2

Type: read-only
Reset State: 0x00000101

General purpose semaphore and/or mutex register.

MCU_MUTEX2

Bits	Name	Description
31	RESET	When set, both CURRENTCOUNT and MAXCOUNT fields get initialized with the value written to the MAXCOUNT field. This bit will not get set on a write operation. Reset State: 0x00000000
15:8	MAXCOUNT	THe Max count of semaphores available. Can only be set when the Reset bit is written with value 1. Reset State: 0x00000001
7:0	CURRENTCOUNT	Current count of the semaphore. On a read, the current value of the Semaphore is returned and if the CurrentCount > 0, the CurrentCount value is decreased by one. On a write, the current value of the Semaphore is increased by one if the CurrentCount < MaxCount. Reset State: 0x00000001

0x30000A4 MCU_MUTEX3

Type: read-only
Reset State: 0x00000101

General purpose semaphore and/or mutex register.

MCU_MUTEX3

Bits	Name	Description
31	RESET	When set, both CURRENTCOUNT and MAXCOUNT fields get initialized with the value written to the MAXCOUNT field. This bit will not get set on a write operation. Reset State: 0x00000000
15:8	MAXCOUNT	THe Max count of semaphores available. Can only be set when the Reset bit is written with value 1. Reset State: 0x00000001
7:0	CURRENTCOUNT	Current count of the semaphore. On a read, the current value of the Semaphore is returned and if the CurrentCount > 0, the CurrentCount value is decreased by one. On a write, the current value of the Semaphore is increased by one if the CurrentCount < MaxCount. Reset State: 0x00000001

0x30000B8 MCU_SOFT_RESET

Type: read-write
Reset State: 0x00000000

Control to soft reset MAC modules. For mCPU reset control, refer to register: MCPU_reset_control.

MCU_SOFT_RESET

Bits	Name	Description
31	TXP_PHYTX_ABORT	When set, the abort signal to the PHYTX is raised. Reset State: 0x00000000
30	CAHB_SOFT_RESET_DOWNCNT_EN	When set, the cahb_soft_reset_downcount starts to count for 63 cycles then reset the mrcm_cahb Reset State: 0x00000000
19	FDAHB_SOFT_RESET	When set, the fdahb is held in soft reset Reset State: 0x00000000
18	FDBR_SOFT_RESET	When set, the fdbr is held in soft reset Reset State: 0x00000000
17	CBR_SOFT_RESET	When set, the cbr is held in soft reset Reset State: 0x00000000
16	QTA_SOFT_RESET	When set, the QTA is held in soft reset Reset State: 0x00000000
15	CFG_SOFT_RESET	When set, the CFG is held in soft reset Reset State: 0x00000000
14	PHY_SOFT_RESET	When set, the PHY is held in soft reset Reset State: 0x00000000
13	ADU_SOFT_RESET	When set, the ADU is held in soft reset Reset State: 0x00000000
12	RPE_SOFT_RESET	When set, the RPE is held in soft reset Reset State: 0x00000000
11	TPE_SOFT_RESET	When set, the TPE is held in soft reset Reset State: 0x00000000
10	DAHB_SOFT_RESET	When set, the DAHB is held in soft reset Reset State: 0x00000000
9	MCU_SOFT_RESET	When set, the MCU is held in soft reset Reset State: 0x00000000
8	PHY_AHB_2_APB_SOFT_RESET	When set, the PHY AHB to APB interface is held in soft reset Reset State: 0x00000000
7	DPU_SOFT_RESET	When set, the DPU is held in soft reset Reset State: 0x00000000
6	BMU_SOFT_RESET	When set, the BMU is held in soft reset Reset State: 0x00000000
5	MTU_SOFT_RESET	When set, the MTU (MAC Timing Unit) is held in soft reset When set, the RXP is held in soft reset Reset State: 0x00000000

MCU_SOFT_RESET (cont.)

Bits	Name	Description
3	TXP_SOFT_RESET	When set, the TXP is held in soft reset Reset State: 0x00000000
2	DBR_SOFT_RESET	Reserved Reset State: 0x00000000
0	MLC_SOFT_RESET	When set, the MLC (MAC Loopback Controller) is held in soft reset Reset State: 0x00000000

0x30000BC MCU_MAC_CLK_GATING_ENABLE

Type: read-write
Reset State: 0x03FF8DE9

Control to enable the dynamic clock gating functionality in the MAC modules.

MCU_MAC_CLK_GATING_ENABLE

Bits	Name	Description
25	MCU_FDAHB_CLK_GATING_ENABLE	When set, the fdahb dynamic clock gating function is enabled Reset State: 0x00000001
24	MCU_FDBR_CLK_GATING_ENABLE	When set, the fdbr dynamic clock gating function is enabled Reset State: 0x00000001
23	MCU_CBR_CLK_GATING_ENABLE	When set, the cbr dynamic clock gating function is enabled Reset State: 0x00000001
22	MCU_CFG_CLK_GATING_ENABLE	When set, the cfg dynamic clock gating function is enabled Reset State: 0x00000001
21	MCU_GAS_CLK_GATING_ENABLE	When set, the MCU gas dynamic clock gating function is enabled Reset State: 0x00000001
20	QTA_CLK_GATING_ENABLE	When set, the QTA dynamic clock gating function is enabled Reset State: 0x00000001
19	ARM_CLK_GATING_ENABLE	When set, the ARM dynamic clock gating function is enabled Reset State: 0x00000001
18	BTC_CLK_GATING_ENABLE	When set, the BTC dynamic clock gating function is enabled Reset State: 0x00000001
17	ADU_CLK_GATING_ENABLE	When set, the ADU dynamic clock gating function is enabled Reset State: 0x00000001
16	TPE_CLK_GATING_ENABLE	When set, the TPE dynamic clock gating function is enabled Reset State: 0x00000001
15	RPE_CLK_GATING_ENABLE	When set, the RPE dynamic clock gating function is enabled Reset State: 0x00000001

MCU_MAC_CLK_GATING_ENABLE (cont.)

Bits	Name	Description
14	DPU_HISTBUF_CLK_ENABLE	This bit is a little bit different since 0-> the clks to hist buff are enabled 1-> the clks are disabled write zero to enable the clock Reset State: 0x00000000
13	DAHB_CLK_GATING_ENABLE	When set, the DAHB bus module dynamic clock gating function is enabled Reset State: 0x00000000
12	CAHB_CLK_GATING_ENABLE	When set, the CAHB module dynamic clock gating function is enabled Reset State: 0x00000000
11	RESERVED1	RESERVED Reset State: 0x00000001
10	MIF_CLK_GATING_ENABLE	Reserved Reset State: 0x00000001
9	MCU_CLK_GATING_ENABLE	When set, the MCU dynamic clock gating function is enabled Reset State: 0x00000000
8	PHY_AHB_2_APB_CLK_GATING_ENABLE	When set, the PHY AHB to APB interface dynamic clock gating function is enabled Reset State: 0x00000001
7	DPU_CLK_GATING_ENABLE	When set, the DPU dynamic clock gating function is enabled Reset State: 0x00000001
6	BMU_CLK_GATING_ENABLE	When set, the BMU dynamic clock gating function is enabled Reset State: 0x00000001
5	MTU_CLK_GATING_ENABLE	When set, the MTU (MAC Timing Unit) dynamic clock gating function is enabled When set, the RXP dynamic clock gating function is enabled Reset State: 0x00000001
3	TXP_CLK_GATING_ENABLE	When set, the TXP dynamic clock gating function is enabled Reset State: 0x00000001
2	DBR_CLK_GATING_ENABLE	When set, the DBR dynamic clock gating function is enabled Reset State: 0x00000000
1	RESERVED2	RESERVED Reset State: 0x00000000
0	MLC_CLK_GATING_ENABLE	When set, the MLC (MAC Loopback Controller) dynamic clock gating function is enabled Reset State: 0x00000001

0x30000C0 MCU_MAC_TESTBUS_CONTROL

Type: read-write
Reset State: 0x3FC0001B

Control to enable the outputs of the MAC module testbusses that do not have programmable registers inside. Control to select which testbus from the MAC is selected to go to the chip top level mux. When set to zero, none of the testbusses are enabled, thus saving power.

MCU_MAC_TESTBUS_CONTROL

Bits	Name	Description
31	MACPHY_TEST_SEL	This bit selects if the vital test signals are from MAC or PHY 0x0: MAC 0x1: PHY Reset State: 0x00000000
30	TESTBUS_MUX_UPPER_LOWER	This bit selects lower 33 bits or upper 33 bits of the 44-bit testbus 1'b0 selects testbus[33:0] 1'b1 selects testbus[44:12] Reset State: 0x00000000
29:28	CBRM_TESTBUS_MODE	testmux select for cbr module 0x1: CBRM_MODE1_TEST 0x2: CBRM_MODE2_TEST 0x3: CBRM_MODE3_TEST Reset State: 0x00000003
27	CAHB_TESTBUS_ENABLE	When set, the CAHB testbus is enabled Reset State: 0x00000001
26	CAHB_VITALS_TESTBUS_ENABLE	When set, the CAHB vitals testbus is enabled Reset State: 0x00000001
25	DAHB_TESTBUS_ENABLE	When set, the DAHB testbus is enabled Reset State: 0x00000001
24	DAHB_VITALS_TESTBUS_ENABLE	When set, the DAHB vitals testbus is enabled Reset State: 0x00000001
23	FDAHB_TESTBUS_ENABLE	When set, the FDAHB testbus is enabled Reset State: 0x00000001
22	FDAHB_VITALS_TESTBUS_ENABLE	When set, the FDAHB vitals testbus is enabled Reset State: 0x00000001
20:16	TBS_PHY_TESTMODE	phy testmode select Reset State: 0x00000000
15:13	WMAC_120_160_TESTBUS_SELECT	These bits select WMAC test bus and the rxp and txp 160,120and160 domain test bus 0x0: WMAC_120 0x1: MTU_120_160 0x2: TXP_160 0x3: TXP_120_160 0x4: RXP_160 0x5: RXP_120_160 0x6: PMU_TESTBUS_CLK_ROSC 0x7: CFG_PHYCLK Reset State: 0x00000000

MCU_MAC_TESTBUS_CONTROL (cont.)

Bits	Name	Description
12:8	WMAC_TESTBUS_SELECT	These bits are used to select wmac testbus from different mac modules see the table for more info 0x0: MCU_TESTBUS 0x1: TXP_TESTBUS 0x2: ACPU_TESTBUS 0x3: RXP_TESTBUS 0x4: CBR_CAHB_TO_CCAHB_TTESTBUS 0x5: MLC_TESTBUS 0x7: DBR_TESTBUS 0x8: MTU_TESTBUS 0x9: BMU_TESTBUS 0xA: DPU_TESTBUS 0xB: AHB2APB_TESTBUS 0xC: CBR_CCAHB_TO_CAHB_TESTBUS 0xD: DBR_DAHB_TO_CDAHB_TESTBUS 0xE: CAHB_TESTBUS 0xF: DAHB_TESTBUS 0x10: DBR_CDAHB_TO_DAHB_TESTBUS 0x11: LRAM_TESTBUS 0x12: MMX_TESTBUS 0x13: MPP_TESTBUS 0x14: DAHB_VITAL_TESTBUS 0x15: PMU_TESTBUS 0x16: RPE_TESTBUS 0x17: ADU_TESTBUS 0x18: TPE_TESTBUS 0x19: BTC_TESTBUS 0x1A: CFG_TESTBUS 0x1B: QTA_TESTBUS 0x1C: FDAHB_VITAL_TESTBUS 0x1D: FDAHB_TESTBUS 0x1E: FDBR_FDAHB_TO_CDAHB_TESTBUS 0x1F: FDBR_CDAHB_TO_FDAHB_TESTBUS Reset State: 0x00000000
4	MCU_TESTBUS	When set, the MCU testbus is enabled Reset State: 0x00000001
3	PHY_AHB_2_APB_TESTBUS	When set, the PHY AHB to APB interface testbus is enabled Reset State: 0x00000001
2:1	DBR_TESTMODE_SELECT	Reserved 0x1: DBR_MODE1_TESTBUS 0x2: DBR_MODE2_TESTBUS Reset State: 0x00000001
0	MLC_TESTBUS_ENABLE	When set, the MLC (MAC Loopback Controller) testbus is enabled Reset State: 0x00000001

0x30000C4 MCU_MAC_FPGA_VERSION

Type: read-only
Reset State: 0x00D0001A

Indicates the version number of the WMAC for FPGA builds.

MCU_MAC_FPGA_VERSION

Bits	Name	Description
31:16	WMAC_TOP_VERSION	The label version number of the WMAC TOP module Reset State: 0x000000D0
15:0	MCU_VERSION	The label version number of the MCU module Reset State: 0x0000001A

0x30000D4 MCU_MAC_MODULES_ROOT_CLK_ENABLES

Type: read-write
Reset State: 0x0003FFED

Control to enable the root clocks for each of the MAC modules.

MCU_MAC_MODULES_ROOT_CLK_ENABLES

Bits	Name	Description
17	FDAHB_ROOT_CLK_ENABLE	When set, the fdahb root clock is enabled Reset State: 0x00000001
16	FDBR_ROOT_CLK_ENABLE	When set, the fdbr root clock is enabled Reset State: 0x00000001
15	CBR_ROOT_CLK_ENABLE	When set, the cbr root clock is enabled Reset State: 0x00000001
14	CFG_ROOT_CLK_ENABLE	When set, the CFG root clock is enabled Reset State: 0x00000001
13	RTCK_ROOT_CLK_ENABLE	Reserved. Reset State: 0x00000001
12	ADU_ROOT_CLK_ENABLE	When set, the ADU root clock is enabled Reset State: 0x00000001
11	RPE_ROOT_CLK_ENABLE	When set, the RPE root clock is enabled Reset State: 0x00000001
10	TPE_ROOT_CLK_ENABLE	When set, the TPE root clock is enabled Reset State: 0x00000001
9	MCPU_ROOT_CLK_ENABLE	When set, the MCPU root clock is enabled Reset State: 0x00000001

MCU_MAC_MODULES_ROOT_CLK_ENABLES (cont.)

Bits	Name	Description
8	PHY_AHB_2_APB_ROOT_CLK_ENABLE	When set, the PHY AHB to APB interface root clock is enabled Reset State: 0x00000001
7	DPU_ROOT_CLK_ENABLE	When set, the DPU root clock is enabled Reset State: 0x00000001
6	BMU_ROOT_CLK_ENABLE	When set, the BMU root clock is enabled Reset State: 0x00000001
5	MTU_ROOT_CLK_ENABLE	When set, the MTU (MAC Timing Unit) root clock is enabled When set, the RXP root clock is enabled Reset State: 0x00000001
3	TXP_ROOT_CLK_ENABLE	When set, the TXP root clock is enabled Reset State: 0x00000001
2	DBR_ROOT_CLK_ENABLE	When set, the DBR root clock is enabled Reset State: 0x00000001
0	MLC_ROOT_CLK_ENABLE	When set, the MLC (MAC Loopback Controller) root clock is enabled Reset State: 0x00000001

0x30000D8 MCU_MAC_MODULES_GOTO_IDLE_CONTROL

Type: read-write
Reset State: 0x00000000

The state machines in the MAC modules can be forced to go back to idle by setting these signals. This resembles somewhat the soft reset functionality, except that the configuration registers maintain their settings. It is therefore less intrusive then a soft reset, and might achieve restoring the modules into a known state.

MCU_MAC_MODULES_GOTO_IDLE_CONTROL

Bits	Name	Description
12	CFG_GOTO_IDLE	When set, the CFG hardware state machines will return to idle Reset State: 0x00000000
11	ADU_GOTO_IDLE	When set, the ADU hardware state machines will return to idle Reset State: 0x00000000
10	TPE_GOTO_IDLE	When set, the TPE hardware state machines will return to idle Reset State: 0x00000000
9	RPE_GOTO_IDLE	When set, the RPE hardware state machines will return to idle Reset State: 0x00000000

MCU_MAC_MODULES_GOTO_IDLE_CONTROL (cont.)

Bits	Name	Description
8	PHY_AHB_2_APB_GOTO_IDLE	When set, the PHY AHB to APB interface hardware state machines will return to idle Reset State: 0x00000000
7	DPU_GOTO_IDLE	When set, the DPU hardware state machines will return to idle Reset State: 0x00000000
6	BMU_GOTO_IDLE	When set, the BMU hardware state machines will return to idle Reset State: 0x00000000
5	MTU_GOTO_IDLE	When set, the MTU (MAC Timing Unit) hardware state machines will return to idle When set, the RXP hardware state machines will return to idle Reset State: 0x00000000
2	DBR_GOTO_IDLE	Reserved Reset State: 0x00000000
0	MLC_GOTO_IDLE	When set, the MLC (MAC Loopback Controller) hardware state machines will return to idle Reset State: 0x00000000

0x30000DC MCU_MAC_TESTBUS_LOW

Type: read-only
Reset State: 0x00000000

The register allows to read the values on the MAC testbus, lower 32 bits.

MCU_MAC_TESTBUS_LOW

Bits	Name	Description
31:0	MAC_TEST_BUS_LOW	Bits [31:0] of the MAC test bus Reset State: 0x00000000

0x30000E0 MCU_MAC_TESTBUS_HIGH

Type: read-only
Reset State: 0x00000000

The register allows to read the values on the MAC testbus, upper bits.

MCU_MAC_TESTBUS_HIGH

Bits	Name	Description
12:0	MAC_TEST_BUS_HIGH	Bits [44:32] of the MAC test bus Reset State: 0x00000000

0x30000E4 MCU_DBR_TRANSLATION_BASE_ADDR

Type: read-write
Reset State: 0x00000000

The DBR allows access to the DAHB from the CAHB. This address is the base address of the window onto the DAHB. It is comparable to the BAR1 base addresses from the PIF when set indicates watchdog 2 interrupt from MTU pending.

MCU_DBR_TRANSLATION_BASE_ADDR

Bits	Name	Description
31:10	DBR_ADDRESS_TRANSLATION_BASE_ADDR	Base address of the 1K window onto the DAHB Reset State: 0x00000000

0x30000EC MCU_APB2PHY_STATUS

Type: read-write
Reset State: 0x00000000

Status register of the apb interface to the PHY.

MCU_APB2PHY_STATUS

Bits	Name	Description
1	AHB2PHY_MCU_TIMOUT_ERROR1	When set to 1'b1, a timeout has happened in the apb2phy interface Reset State: 0x00000000
0	AHB2PHY_MCU_TIMOUT_ERROR2	When set to 1'b1, a timeout has happened in the apb2phy interface Reset State: 0x00000000

0x30000F0 MCU_MLC_STATUS

Type: read-only
Reset State: 0x00000000

Status register of the MLC.

MCU_MLC_STATUS

Bits	Name	Description
31:28	MLC_CONTROLLER_STATE	State that the MLC controller is in: 0x0: idle 0xf:0x1: MLC active Reset State: 0x00000000
27:24	NR_OF_RXP_STARTS	The number of txp_mlc_start pulses received Reset State: 0x00000000
23:22	NR_OF_TXP_MLC_ABORTS	The number of txp_mlc_aborts received. This number freezes on 2'b11. Reset State: 0x00000000
21:20	NR_OF_MLC_ENDS	The number of command bytes passed on to the RXP Reset State: 0x00000000
19:12	NR_OF_COMMAND_BYTES	The number of command bytes passed on to the RXP Reset State: 0x00000000
11:0	NR_OF_DATA_BYTES	The number of data bytes and statistics bytes passed on to the RXP Reset State: 0x00000000

0x30000F4 MCU_MCU_RESERVED

Type: read-write
Reset State: 0x00000000

These bits have been reserved for future use

MCU_MCU_RESERVED

Bits	Name	Description
15:1	MCU_RESERVED	Spare register bits read writable Reset State: 0x00000000
0	PMU_AGC_SLEEP	pmu_agc_sleep Reset State: 0x00000000

0x3000100 MCU_RF_WARMUP_CONTROL

Type: read-write
Reset State: 0x00000000

This register has controls for txp for rf warmup.

MCU_RF_WARMUP_CONTROL

Bits	Name	Description
2	TXP_MCU_RF_WARMUP	This is a read-only signal. It is basically the status of the of the warmup signal that is given by the TXP to the PHY Reset State: 0x00000000
1	MCU_TXP_RF_WARMUP	Reserved. Not used. Reset State: 0x00000000
0	MCU_TXP_RF_WARMUP_END	Reserved. Not used. Reset State: 0x00000000

0x3000104 MCU_BTC

Type: read-write
Reset State: 0x00000040

This register controls the operation of the BTC function. This register also masks the various conditions that this device will be reporting 'ACTIVE' to the Bluetooth device. Setting a bit to "1" enables the condition, while "0" masks (disables) the condition.

MCU_BTC

Bits	Name	Description
23	MTU_BTC_TX_RX_BUSY	Gives status of busy signal going to BTC after the override Reset State: 0x00000000
22	MTU_MCU_TX_RX_BUSY	Gives status of busy signal coming from MTU Reset State: 0x00000000
21	BTC_GPIO_INTEL_WLAN_ACTIVE	Reserved. 2-wire is not supported Reset State: 0x00000000
20	BTC_BSR_WLAN_ACTIVE	Gives status of wlan active signal going to the pad Reset State: 0x00000000
19	BTC_BLUETOOTH_ACTIVE	Gives status input bluetooth active signal Reset State: 0x00000000
18	BTC_WLAN_ACTIVE	Gives status of wlan active signal from logic (before override) Reset State: 0x00000000
17	BTC_INTEL_WLAN_ACTIVE	Reserved. 2-wire is not supported Reset State: 0x00000000
16	CHANNEL_DATA_DONE	Reserved. 2-wire is not supported Reset State: 0x00000000
12	BTC_WLAN_ACTIVE_SW_SEL	When '1', this bit selects override for the wlan active signal Reset State: 0x00000000

MCU_BTC (cont.)

Bits	Name	Description
11	BTC_WLAN_ACTIVE_OVERRIDE	When '1', this bit overrides the wlan active signal from logic Reset State: 0x00000000
10	BTC_INTEL_WLAN_ACTIVE_OVERRIDE	Reserved. 2-wire is not supported Reset State: 0x00000000
9	BTC_INTEL_WLAN_ACTIVE_SW_SEL	Reserved. 2-wire is not supported Reset State: 0x00000000
8	BTC_TX_RX_BUSY_SW_SEL	Reserved Reset State: 0x00000000
7	BTC_TX_RX_BUSY_OVERRIDE	Reserved Reset State: 0x00000000
6	BT_ACTIVE_EN	When '1', this bit enables the sensing of the Bluetooth devices activity on the shared transmission channel for both Dell and Intel modes of operation. Reset State: 0x00000001
5	BTC_MODE	Reserved. 2-wire is not supported Reset State: 0x00000000
4	CHANNEL_DATA_WR_EN	Reserved. 2-wire is not supported Reset State: 0x00000000
3:0	CHANNEL_DATA	Reserved. 2-wire is not supported Reset State: 0x00000000

0x3000108 MCU_RF_ON_OFF_CONTROL

Type: read-only
Reset State: 0x00000000

This register reflects the status of radio on/off hardware pin.

MCU_RF_ON_OFF_CONTROL

Bits	Name	Description
0	RD_ON_OFF_HWPIN_STAT	0x0: radio OFF 1'b1 : radio ON Reset State: 0x00000000

0x3000194 MCU_DEBUGC_CONTROL

Type: read-write
Reset State: 0x00000000

Debug testbus control.

MCU_DEBUGC_CONTROL

Bits	Name	Description
29:16	MIF_DEBUGC_ADDR	Gives the address where the above tracing is stored Reset State: 0x00000000
7:0	DBGC_CONTROL	0x8: Nothing selected 8'd1 : BMU tracing selected 8'd2 : DAHB tracing selected 8'd3 : CAHB tracing selected Reset State: 0x00000000

0x3000210 MCU_DABH_MIF_PRIORITY_GENERATION_CONTROL

Type: read-write
Reset State: 0x00000000

Controls the way the priority signal from the DAHB to the MIF is generated.

MCU_DABH_MIF_PRIORITY_GENERATION_CONTROL

Bits	Name	Description
1:0	DABH_MIF_PRIORITY_MODE	0x0: txp, rxp bus request based, BMU priority request based 01: txp, rxp and bmu bus request based (when BMU priority requested AND mif txp/rxp/bmu busy based 10: same as 01, but with extended bus request version 11: request starts on a rising edge of the busrequest from txp/rxp/bmuwhen bmu priority requested and ends at the falling edge of the txp/rxp/bmu mif busy indication) Reset State: 0x00000000

0x3000214 MCU_BTC_CTRL

Type: read-write
Reset State: 0x0006019F

This register controls the BTC function in 3/4 wire mode.

MCU_BTC_CTRL

Bits	Name	Description
29:27	SCO_RESERVE_SLOT	To setup the sco/esco reserve slot in terms of slot Reset State: 0x00000000
26	FORCE_SYNC_TO_SCO	A 0->1 transition will force pta to sync to the bt_active when the counter reaches 0 within the programmed boundary as sco start. software has to clear this bit. Reset State: 0x00000000
25	STATS_EN	When set, enable the states counters Reset State: 0x00000000

MCU_BTC_CTRL (cont.)

Bits	Name	Description
24	ESCO_WAIT_FOR_RETX_EN	When set, the wlan will not be allow to transmit until the esco retransmission slot is cleared Reset State: 0x00000000
23:21	ESCO_RETRANSMIT_SLOT	To setup the esco retransmission slot in terms of slot Reset State: 0x00000000
20:16	SCO_PERIOD	To setup the sco period in terms of slot Reset State: 0x00000006
15	PERIOD_INT_CLEAR	Reserved. Not required any more Reset State: 0x00000000
14	PRIORITY_INT_CLEAR	Reserved. Not required any more Reset State: 0x00000000
13	BT_SIMUL_TX_NONOVERLAP	Reserved. No simultaneous transmission Reset State: 0x00000000
12	BT_SIMUL_TX_ALL	Reserved. No simultaneous transmission Reset State: 0x00000000
11	PERIOD_INT_DISABLE	Reserved. Not required any more Reset State: 0x00000000
10	PRIORITY_INT_DISABLE	Reserved. Not required any more Reset State: 0x00000000
9:8	BT_3_4WIRE_MODE	Reserved. Only 3-wire is supported Reset State: 0x00000001
7	BT_DELL_PRIORITY	Reserved. 2-wire is not supported Reset State: 0x00000001
6	BT_SVO_MODE	Set this bit if BT is in SVO mode. 0x0: NOT_IN_SVO 0x1: IN_SVO Reset State: 0x00000000
5	BT_SCO_MODE	Set this bit if BT is in SCO mode. 0x0: NOT_IN_SCO 0x1: IN_SCO Reset State: 0x00000000
4	BT_STATUS_POLARITY	Set this bit if BT is operating in 3/4 wire protocol. 0x0: TX_LOW 0x1: TX_HIGH Reset State: 0x00000001
3	WLAN_ACTIVE_POLARITY	To configure the polarity of wlan_active signal from BT. 0x0: ACTIVE_LOW 0x1: ACTIVE_HIGH Reset State: 0x00000001

MCU_BTC_CTRL (cont.)

Bits	Name	Description
2	BT_FREQ_POLARITY	Reserved. 4-wire is not supported Reset State: 0x00000001
1	BT_PRIORITY_POLARITY	To configure the polarity of bt_priority signal from BT 0x0: ACTIVE_LOW 0x1: ACTIVE_HIGH Reset State: 0x00000001
0	BT_ACTIVE_POLARITY	To configure the polarity of bt_active signal from BT 0x0: ACTIVE_LOW 0x1: ACTIVE_HIGH Reset State: 0x00000001

0x3000218 MCU_BTC_CTRL2

Type: read-write
Reset State: 0x01003200

This register is to set up the counter value in 3/4 wire mode.

MCU_BTC_CTRL2

Bits	Name	Description
31:24	OFFSET_UNCERTANTY	To set up the allowed offset value for period validation Reset State: 0x00000001
23	BEFORE_LAG	Reserved 0x0: CNT_LAG 0x1: CNT_PRIORI Reset State: 0x00000000
15:8	EARLY_END_CNT	To set up the number of cycles for wlan to stop to transmit after bt_active assertion.(keep the name of the bit field in case any TB might use it for whatever purpose). Note this value should be larger than t2 to avoid wrong priority bt traffic request signal sent to TPE. Reset State: 0x00000032
7:0	LATE_START_CNT	To set up the number of cycles for wlan to start to transmit after bt_active de-assertion. Reset State: 0x00000000

0x300021C MCU_BTC_CTRL3

Type: read-write
Reset State: 0x00014196

This register is to set up the timing spec in 3/4 wire mode.

MCU_BTC_CTRL3

Bits	Name	Description
17:12	BTC_T3	To setup the T3 number (default to 20us). Reset State: 0x00000014
11:8	BTC_T2	To setup the T2 number (default to 1us). Reset State: 0x00000001
7:0	BTC_T1	To setup the T1 number (default to 150us). Reset State: 0x00000096

0x3000220 MCU_BTC_STATUS

Type: read-write
Reset State: 0x010EA500

This register contains the status of internal signals.

MCU_BTC_STATUS

Bits	Name	Description
31	WAIT_FOR_ESCO_DONE	The status of the esco_bt_is_done signal. If it's in esco mode, and the BTC_CTRL[24] is set, the signal will be asserted until the esco retransmission is done. Otherwise this signal will be 0. Reset State: 0x00000000
30	BTC_MODE	When '1', BT is in tx in current slot. When '0' and bt_active is high, BT is in rx in current slot Reset State: 0x00000000
29:24	SCO_SLOT_CNT	The sco slot counter value Reset State: 0x00000001
23	SCO_SYNC_FLAG	To indicate whether the sco period is locked(1) or not(0) Reset State: 0x00000000
22:8	BT_AVAIL_CNT	The sco period counter which software can write to change the value (The big field name is kept in case any mcs relies on it) Reset State: 0x00000EA5
7	MASTER_SLAVE_STATUS	To indicate whether it's master(1) or slave(0) This is only valid in sco/esco mode. Reset State: 0x00000000
6	BT_PERIOD_STATUS	The status of the bt_period_int signal which validates the bt mode and period (Always read 0 since the interrupt is removed) Reset State: 0x00000000

MCU_BTC_STATUS (cont.)

Bits	Name	Description
5	BT_PRIORITY_STATUS	The status of the bt_priority_int signal which validates the bt mode and priority (Always read 0 since the interrupt is removed) Reset State: 0x00000000
4	BT_PRIORITY_TO_TPE	The status of the bt_priority signal to TPE Reset State: 0x00000000
3	BT_TRAFFIC_REQUEST	The status of the bt_traffic_request signal to TPE Reset State: 0x00000000
2	BT_FREQ	The status of the incoming bt_freq signal (Always read 0 since we only use 3 wire protocol) Reset State: 0x00000000
1	BT_PRIORITY	The status of the incoming bt_priority signal Reset State: 0x00000000
0	BT_ACTIVE_S	The status of the sync-ed bt_active signal Reset State: 0x00000000

0x3000224 MCU_BTC_STATUS2

Type: read-only
Reset State: 0x00007FFF

This register contains the status of internal signals.

MCU_BTC_STATUS2

Bits	Name	Description
31:28	CNT_3750US	Reserved Reset State: 0x00000000
27:24	S_STATE	The encoded state machine status Reset State: 0x00000000
23:16	CNT_T2_T3	The status of the t2_t3 counter Reset State: 0x00000000
14:0	BT_AVAIL_CNT	The down counter to next bt-active assertion in sco/esco mode to TPE Reset State: 0x00007FFF

0x300022C MCU_BTC_FRAME1_STATUS

Type: read-only
Reset State: 0x00000000

This register is obsolete and no longer support.

MCU_BTC_FRAME1_STATUS

Bits	Name	Description
24:12	FRAME1_PERIOD	Reserve Reset State: 0x00000000
11:0	FRAME1_HIGH	Reserve Reset State: 0x00000000

0x3000230 MCU_BTC_FRAME2_STATUS

Type: read-only
Reset State: 0x00000000

This register is obsolete and no longer support.

MCU_BTC_FRAME2_STATUS

Bits	Name	Description
24:12	FRAME2_PERIOD	Reserve Reset State: 0x00000000
11:0	FRAME2_HIGH	Reserve Reset State: 0x00000000

0x3000238 MCU_FIQ_EN

Type: read-write
Reset State: 0x00000000

This register contains the acpu fiq enable signals

MCU_FIQ_EN

Bits	Name	Description
31	SW_1_FIQ_EN	When set, software 1 interrupt is enabled. Reset State: 0x00000000
30	RXP_ERR_FIQ_EN	When set, rxp error interrupt is enabled. Reset State: 0x00000000
29	QTA_FIQ_EN	When set, qta interrupt is enabled. Reset State: 0x00000000

MCU_FIQ_EN (cont.)

Bits	Name	Description
28	MTU_TIMER7_EN	When set, mtu timer7/tsf_timer7 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
27	MTU_TIMER6_EN	When set, mtu timer6/tsf_timer6 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
26	PHY_HIF_FIQ_EN	When set, phy hif interrupt is enabled. Reset State: 0x00000000
25	WQ_DATA_AVAIL_FIQ_EN	When set, wq data available interrupt is enabled. Reset State: 0x00000000
24	PHY_FIQ_IRQ_EN	When set, phy irq interrupt is enabled. Reset State: 0x00000000
23	PHY_FIQ_FIQ_EN	When set, phy fiq interrupt is enabled. Reset State: 0x00000000
22	TPE_FIQ_EN	When set, tpe_mcu_int interrupt is enabled. Reset State: 0x00000000
21	MIF_FIQ_EN	When set, mif interrupt is enabled. Reset State: 0x00000000
20	BT_INACTIVE_FIQ_EN	When set, the bt inactive interrupt is enabled. Reset State: 0x00000000
19	BT_ACTIVE_FIQ_EN	When set, the bt active interrupt is enabled. Reset State: 0x00000000
18	MTU_TIMER5_EN	When set, mtu timer5/tsf_timer5 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
17	ADU_FIQ_EN	When set, adu interrupt is enabled. Reset State: 0x00000000
16	MTU_TIMER4_EN	When set, mtu timer4/tsf_timer4 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
15	RPE_FIQ_EN	When set, rpe interrupt is enabled. Reset State: 0x00000000
13	COMBINED_FIQ_EN	When set, the combined txp/dpu/dbr/ahb2phy interrupt is enabled. See combined_int related registers for detail Reset State: 0x00000000
12	RXP_FIQ_EN	When set, rxp beacon related interrupt is enabled. Reset State: 0x00000000
7	HOST_TO_ACPU_MB3_FIQ_EN	When set, host to acpu MB3 interrupt is enabled. Reset State: 0x00000000

MCU_FIQ_EN (cont.)

Bits	Name	Description
6	HOST_TO_ACPU_MB2_FIQ_EN	When set, host to acpu MB2 interrupt is enabled. Reset State: 0x00000000
5	HOST_TO_ACPU_MB1_FIQ_EN	When set, host to acpu MB1 interrupt is enabled. Reset State: 0x00000000
4	HOST_TO_ACPU_MB0_FIQ_EN	When set, host to acpu MB0 interrupt is enabled. Reset State: 0x00000000
3	MTU_FIQ_EN	When set, combined mtu interrupt is enabled. See mtu_int related registers for detail Reset State: 0x00000000
2	SW_0_FIQ_EN	When set, software 0 interrupt is enabled. Reset State: 0x00000000
1	SCU_UART_FIQ_EN	When set, uart interrupt is enabled. Reset State: 0x00000000
0	MTU_WD_1_FIQ_EN	When set, mtu watchdog timer (warning) interrupt is enabled. Reset State: 0x00000000

0x300023C MCU_FIQ_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the acpu fiq raw status signals

MCU_FIQ_STATUS

Bits	Name	Description
31	SW_1_FIQ_STATUS	sw 1 interrupt status. Reset State: 0x00000000
30	RXP_ERR_FIQ_STATUS	rxp error interrupt status. Reset State: 0x00000000
29	QTA_FIQ_STATUS	qta interrupt status. Reset State: 0x00000000
28	MTU_TIMER7_STATUS	When set, mtu timer7/tsf_timer7 interrupt status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
27	MTU_TIMER6_STATUS	When set, mtu timer6/tsf_timer6 interrupt status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
26	PHY_HIF_FIQ_STATUS	phy hif interrupt status. Reset State: 0x00000000

MCU_FIQ_STATUS (cont.)

Bits	Name	Description
25	WQ_DATA_AVAIL_FIQ_STATUS	wq data available interrupt status. Reset State: 0x00000000
24	PHY_FIQ_IRQ_STATUS	phy irq interrupt status. Reset State: 0x00000000
23	PHY_FIQ_FIQ_STATUS	phy fiq interrupt status. Reset State: 0x00000000
22	TPE_FIQ_STATUS	tpe_mcu_int interrupt status. Reset State: 0x00000000
21	MIF_FIQ_STATUS	mif interrupt status. Reset State: 0x00000000
20	BT_INACTIVE_FIQ_STATUS	bt inactive interrupt status. Reset State: 0x00000000
19	BT_ACTIVE_FIQ_STATUS	bt active interrupt status. Reset State: 0x00000000
18	MTU_TIMER5_STATUS	When set, mtu timer5/tsf_timer5 interrupt status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
17	ADU_FIQ_STATUS	adu interrupt status. Reset State: 0x00000000
16	MTU_TIMER4_STATUS	When set, mtu timer4/tsf_timer4 interrupt status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
15	RPE_FIQ_STATUS	rpe interrupt status. Reset State: 0x00000000
13	COMBINED_FIQ_STATUS	the combined txp/dpu/dbr/ahb2phy interrupt status. See combined_int related registers for detail Reset State: 0x00000000
12	RXP_FIQ_STATUS	rxp beacon related interrupt status. Reset State: 0x00000000
7	HOST_TO_ACPU_MB3_FIQ_STATUS	host to acpu MB3 interrupt status. Reset State: 0x00000000
6	HOST_TO_ACPU_MB2_FIQ_STATUS	host to acpu MB2 interrupt status. Reset State: 0x00000000
5	HOST_TO_ACPU_MB1_FIQ_STATUS	host to acpu MB1 interrupt status. Reset State: 0x00000000
4	HOST_TO_ACPU_MB0_FIQ_STATUS	host to acpu MB0 interrupt status. Reset State: 0x00000000

MCU_FIQ_STATUS (cont.)

Bits	Name	Description
3	MTU_FIQ_STATUS	combined mtu interrupt status. See mtu_int related registers for detail Reset State: 0x00000000
2	SW_0_FIQ_STATUS	sw 0 interrupt status. Reset State: 0x00000000
1	SCU_UART_FIQ_STATUS	uart interrupt status. Reset State: 0x00000000
0	MTU_WD_1_FIQ_STATUS	mtu watchdog timer (warning) interrupt status. Reset State: 0x00000000

0x3000240 MCU_FIQ_MASKED_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the acpu fiq masked status

MCU_FIQ_MASKED_STATUS

Bits	Name	Description
31	SW_1_FIQ_MASKED_STATUS	sw 1 interrupt masked status. Reset State: 0x00000000
30	RXP_ERR_FIQ_MASKED_STATUS	rxp error interrupt masked status. Reset State: 0x00000000
29	QTA_FIQ_MASKED_STATUS	qta interrupt masked status. Reset State: 0x00000000
28	MTU_TIMER7_MASKED_STATUS	When set, mtu timer7/tsf_timer7 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
27	MTU_TIMER6_MASKED_STATUS	When set, mtu timer6/tsf_timer6 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
26	PHY_HIF_FIQ_MASKED_STATUS	phy hif interrupt masked status. Reset State: 0x00000000
25	WQ_DATA_AVAIL_FIQ_MASKED_STATUS	wq data available interrupt masked status. Reset State: 0x00000000
24	PHY_FIQ_IRQ_MASKED_STATUS	phy irq interrupt masked status. Reset State: 0x00000000
23	PHY_FIQ_FIQ_MASKED_STATUS	phy fiq interrupt masked status. Reset State: 0x00000000

MCU_FIQ_MASKED_STATUS (cont.)

Bits	Name	Description
22	TPE_FIQ_MASKED_STATUS	tpe_mcu_int interrupt masked status. Reset State: 0x00000000
21	MIF_FIQ_MASKED_STATUS	mif interrupt masked status. Reset State: 0x00000000
20	BT_INACTIVE_FIQ_MASKED_STATUS	bt inactive interrupt masked status. Reset State: 0x00000000
19	BT_ACTIVE_FIQ_MASKED_STATUS	bt active interrupt masked status. Reset State: 0x00000000
18	MTU_TIMER5_MASKED_STATUS	When set, mtu timer5/tsf_timer5 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
17	ADU_FIQ_MASKED_STATUS	adu interrupt masked status. Reset State: 0x00000000
16	MTU_TIMER4_MASKED_STATUS	When set, mtu timer4/tsf_timer4 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
15	RPE_FIQ_MASKED_STATUS	rpe interrupt masked status. Reset State: 0x00000000
13	COMBINED_FIQ_MASKED_STATUS	the combined txp/dpu/dbr/ahb2phy interrupt masked status. See combined_int related registers for detail Reset State: 0x00000000
12	RXP_FIQ_MASKED_STATUS	rxp beacon related interrupt masked status. Reset State: 0x00000000
11	DXE_MXU_CHAIN_2_FIQ_MASKED_STATUS	dxe channel 2 interrupt masked status. Reset State: 0x00000000
10	DXE_MXU_CHAIN_1_FIQ_MASKED_STATUS	dxe channel 1 interrupt masked status. Reset State: 0x00000000
9	DXE_MXU_CHAIN_0_FIQ_MASKED_STATUS	dxe channel 0 interrupt masked status. Reset State: 0x00000000
8	PMU_PWR_UP_FIQ_MASKED_STATUS	pmu_pwr_up interrupt masked status. Reset State: 0x00000000
7	HOST_TO_ACPU_MB3_FIQ_MASKED_STATUS	host to acpu MB3 interrupt masked status. Reset State: 0x00000000
6	HOST_TO_ACPU_MB2_FIQ_MASKED_STATUS	host to acpu MB2 interrupt masked status. Reset State: 0x00000000
5	HOST_TO_ACPU_MB1_FIQ_MASKED_STATUS	host to acpu MB1 interrupt masked status. Reset State: 0x00000000
4	HOST_TO_ACPU_MB0_FIQ_MASKED_STATUS	host to acpu MB0 interrupt masked status. Reset State: 0x00000000

MCU_FIQ_MASKED_STATUS (cont.)

Bits	Name	Description
3	MTU_FIQ_MASKED_STATUS	combined mtu interrupt masked status. See mtu_int related registers for detail Reset State: 0x00000000
2	SW_0_FIQ_MASKED_STATUS	sw 0 interrupt masked status. Reset State: 0x00000000
1	SCU_UART_FIQ_MASKED_STATUS	uart interrupt masked status. Reset State: 0x00000000
0	MTU_WD_1_FIQ_MASKED_STATUS	mtu watchdog timer (warning) interrupt masked status. Reset State: 0x00000000

0x3000244 MCU_FIQ_CLEAR

Type: write-only
Reset State: 0x00000000

This register contains the acpu fiq clear signals

MCU_FIQ_CLEAR

Bits	Name	Description
31	SW_1_FIQ_CLEAR	When set, software 1 interrupt is cleared. Reset State: 0x00000000
30	RXP_ERR_FIQ_CLEAR	When set, rxp error interrupt is cleared. Reset State: 0x00000000
29	QTA_FIQ_CLEAR	When set, qta interrupt is cleared. Reset State: 0x00000000
28	MTU_TIMER7_CLEAR	When set, mtu timer7/tsf_timer7 interrupt is cleared Reset State: 0x00000000
27	MTU_TIMER6_CLEAR	When set, mtu timer6/tsf_timer6 interrupt is cleared Reset State: 0x00000000
26	PHY_HIF_FIQ_CLEAR	When set, phy hif interrupt is cleared. Reset State: 0x00000000
25	WQ_DATA_AVAIL_FIQ_CLEAR	When set, wq data available interrupt is cleared. Reset State: 0x00000000
24	PHY_FIQ_IRQ_CLEAR	When set, phy irq interrupt is cleared. Reset State: 0x00000000
23	PHY_FIQ_FIQ_CLEAR	When set, phy fiq interrupt is cleared. Reset State: 0x00000000

MCU_FIQ_CLEAR (cont.)

Bits	Name	Description
22	TPE_FIQ_CLEAR	When set, tpe_mcu_int interrupt is cleared. Reset State: 0x00000000
21	MIF_FIQ_CLEAR	When set, mif interrupt is cleared. Reset State: 0x00000000
20	BT_INACTIVE_FIQ_CLEAR	When set, bt inactive interrupt is cleared. Reset State: 0x00000000
19	BT_ACTIVE_FIQ_CLEAR	When set, bt active interrupt is cleared. Reset State: 0x00000000
18	MTU_TIMER5_CLEAR	When set, mtu timer5/tsf_timer5 interrupt is cleared Reset State: 0x00000000
17	ADU_FIQ_CLEAR	When set, adu interrupt is cleared. Reset State: 0x00000000
16	MTU_TIMER4_CLEAR	When set, mtu timer4/tsf_timer4 interrupt is cleared Reset State: 0x00000000
15	RPE_FIQ_CLEAR	When set, rpe interrupt is cleared. Reset State: 0x00000000
13	COMBINED_FIQ_CLEAR	When set, the combined txp/dpu/dbr/ahb2phy interrupt is cleared. See combined_int related registers for detail Reset State: 0x00000000
12	RXP_FIQ_CLEAR	When set, rxp beacon related interrupt is cleared. Reset State: 0x00000000
7	HOST_TO_ACPU_MB3_FIQ_CLEAR	When set, host to acpu MB3 interrupt is cleared. Reset State: 0x00000000
6	HOST_TO_ACPU_MB2_FIQ_CLEAR	When set, host to acpu MB2 interrupt is cleared. Reset State: 0x00000000
5	HOST_TO_ACPU_MB1_FIQ_CLEAR	When set, host to acpu MB1 interrupt is cleared. Reset State: 0x00000000
4	HOST_TO_ACPU_MB0_FIQ_CLEAR	When set, host to acpu MB0 interrupt is cleared. Reset State: 0x00000000
3	MTU_FIQ_CLEAR	When set, combined mtu interrupt is cleared. See mtu_int related registers for detail Reset State: 0x00000000
2	SW_0_FIQ_CLEAR	When set, software 0 interrupt is cleared. Reset State: 0x00000000
1	SCU_UART_FIQ_CLEAR	When set, uart interrupt is cleared. Reset State: 0x00000000
0	MTU_WD_1_FIQ_CLEAR	When set, mtu watchdog timer (warning) interrupt is cleared. Reset State: 0x00000000

0x3000248 MCU_IRQ_EN

Type: read-write
Reset State: 0x00000000

This register contains the acpu irq enable signals

MCU_IRQ_EN

Bits	Name	Description
31	SW_1_IRQ_EN	When set, software 1 interrupt is enabled. Reset State: 0x00000000
30	RXP_ERR_IRQ_EN	When set, rxp error interrupt is enabled. Reset State: 0x00000000
29	QTA_IRQ_EN	When set, qta interrupt is enabled. Reset State: 0x00000000
28	MTU_TIMER7_EN	When set, mtu timer7/tsf_timer7 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
27	MTU_TIMER6_EN	When set, mtu timer6/tsf_timer6 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
26	PHY_HIF_IRQ_EN	When set, phy hif interrupt is enabled. Reset State: 0x00000000
25	WQ_DATA_AVAIL_IRQ_EN	When set, wq data available interrupt is enabled. Reset State: 0x00000000
24	PHY_IRQ_IRQ_EN	When set, phy irq interrupt is enabled. Reset State: 0x00000000
23	PHY_FIQ_IRQ_EN	When set, phy fiq interrupt is enabled. Reset State: 0x00000000
22	TPE_IRQ_EN	When set, tpe_mcu_int interrupt is enabled. Reset State: 0x00000000
21	MIF_IRQ_EN	When set, mif interrupt is enabled. Reset State: 0x00000000
20	BT_INACTIVE_IRQ_EN	When set, bt inactive interrupt is enabled. Reset State: 0x00000000
19	BT_ACTIVE_IRQ_EN	When set, bt active interrupt is enabled. Reset State: 0x00000000
18	MTU_TIMER5_EN	When set, mtu timer5/tsf_timer5 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
17	ADU_IRQ_EN	When set, adu interrupt is enabled. Reset State: 0x00000000

MCU_IRQ_EN (cont.)

Bits	Name	Description
16	MTU_TIMER4_EN	When set, mtu timer4/tsf_timer4 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
15	RPE_IRQ_EN	When set, rpe interrupt is enabled. Reset State: 0x00000000
13	COMBINED_IRQ_EN	When set, the combined txp/dpu/dbr/ahb2phy interrupt is enabled. See combined_int related registers for detail Reset State: 0x00000000
12	RXP_IRQ_EN	When set, rxp beacon related interrupt is enabled. Reset State: 0x00000000
7	HOST_TO_ACPU_MB3_IRQ_EN	When set, host to acpu MB3 interrupt is enabled. Reset State: 0x00000000
6	HOST_TO_ACPU_MB2_IRQ_EN	When set, host to acpu MB2 interrupt is enabled. Reset State: 0x00000000
5	HOST_TO_ACPU_MB1_IRQ_EN	When set, host to acpu MB1 interrupt is enabled. Reset State: 0x00000000
4	HOST_TO_ACPU_MB0_IRQ_EN	When set, host to acpu MB0 interrupt is enabled. Reset State: 0x00000000
3	MTU_IRQ_EN	When set, combined mtu interrupt is enabled. See mtu_int related registers for detail Reset State: 0x00000000
2	SW_0_IRQ_EN	When set, software 0 interrupt is enabled. Reset State: 0x00000000
1	SCU_UART_IRQ_EN	When set, uart interrupt is enabled. Reset State: 0x00000000
0	MTU_WD_1_IRQ_EN	When set, mtu watchdog timer (warning) interrupt is enabled. Reset State: 0x00000000

0x300024C MCU_IRQ_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the acpu irq raw status signals

MCU_IRQ_STATUS

Bits	Name	Description
31	SW_1_IRQ_STATUS	sw 1 interrupt status. Reset State: 0x00000000

MCU_IRQ_STATUS (cont.)

Bits	Name	Description
30	RXP_ERR_IRQ_STATUS	rxp error interrupt status. Reset State: 0x00000000
29	QTA_IRQ_STATUS	qta interrupt status. Reset State: 0x00000000
28	MTU_TIMER7_STATUS	When set, mtu timer7/tsf_timer7 interrupt status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
27	MTU_TIMER6_STATUS	When set, mtu timer6/tsf_timer6 interrupt status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
26	PHY_HIF_IRQ_STATUS	phy hif interrupt status. Reset State: 0x00000000
25	WQ_DATA_AVAIL_IRQ_STATUS	wq data available interrupt status. Reset State: 0x00000000
24	PHY_IRQ_IRQ_STATUS	phy irq interrupt status. Reset State: 0x00000000
23	PHY_FIQ_IRQ_STATUS	phy fiq interrupt status. Reset State: 0x00000000
22	TPE_IRQ_STATUS	tpe_mcu_int interrupt status. Reset State: 0x00000000
21	MIF_IRQ_STATUS	mif interrupt status. Reset State: 0x00000000
20	BT_INACTIVE_IRQ_STATUS	bt inactive interrupt status. Reset State: 0x00000000
19	BT_ACTIVE_IRQ_STATUS	bt_active interrupt status. Reset State: 0x00000000
18	MTU_TIMER5_STATUS	When set, mtu timer5/tsf_timer5 interrupt status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
17	ADU_IRQ_STATUS	adu interrupt status. Reset State: 0x00000000
16	MTU_TIMER4_STATUS	When set, mtu timer4/tsf_timer4 interrupt status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
15	RPE_IRQ_STATUS	rpe interrupt status. Reset State: 0x00000000
13	COMBINED_IRQ_STATUS	the combined txp/dpu/dbr/ahb2phy interrupt status. See combined_int related registers for detail Reset State: 0x00000000

MCU_IRQ_STATUS (cont.)

Bits	Name	Description
12	RXP_IRQ_STATUS	rxp beacon related interrupt status. Reset State: 0x00000000
7	HOST_TO_ACPU_MB3_IRQ_STATUS	host to acpu MB3 interrupt status. Reset State: 0x00000000
6	HOST_TO_ACPU_MB2_IRQ_STATUS	host to acpu MB2 interrupt status. Reset State: 0x00000000
5	HOST_TO_ACPU_MB1_IRQ_STATUS	host to acpu MB1 interrupt status. Reset State: 0x00000000
4	HOST_TO_ACPU_MB0_IRQ_STATUS	host to acpu MB0 interrupt status. Reset State: 0x00000000
3	MTU_IRQ_STATUS	combined mtu interrupt status. See mtu_int related registers for detail Reset State: 0x00000000
2	SW_0_IRQ_STATUS	sw 0 interrupt status. Reset State: 0x00000000
1	SCU_UART_IRQ_STATUS	uart interrupt status. Reset State: 0x00000000
0	MTU_WD_1_IRQ_STATUS	mtu watchdog timer (warning) interrupt status. Reset State: 0x00000000

0x3000250 MCU_IRQ_MASKED_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the acpu irq masked status

MCU_IRQ_MASKED_STATUS

Bits	Name	Description
31	SW_1_IRQ_MASKED_STATUS	sw 1 interrupt masked status. Reset State: 0x00000000
30	RXP_ERR_IRQ_MASKED_STATUS	rxp error interrupt masked status. Reset State: 0x00000000
29	QTA_IRQ_MASKED_STATUS	qta interrupt masked status. Reset State: 0x00000000
28	MTU_TIMER7_MASKED_STATUS	When set, mtu timer7/tsf_timer7 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000

MCU_IRQ_MASKED_STATUS (cont.)

Bits	Name	Description
27	MTU_TIMER6_MASKED_STATUS	When set, mtu timer6/tsf_timer6 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
26	PHY_HIF_IRQ_MASKED_STATUS	phy hif interrupt masked status. Reset State: 0x00000000
25	WQ_DATA_AVAIL_IRQ_MASKED_STATUS	wq data available interrupt masked status. Reset State: 0x00000000
24	PHY_IRQ_IRQ_MASKED_STATUS	phy irq interrupt masked status. Reset State: 0x00000000
23	PHY_FIQ_IRQ_MASKED_STATUS	phy fiq interrupt masked status. Reset State: 0x00000000
22	TPE_IRQ_MASKED_STATUS	tpe_mcu_int interrupt masked status. Reset State: 0x00000000
21	MIF_IRQ_MASKED_STATUS	mif interrupt masked status. Reset State: 0x00000000
20	BT_INACTIVE_IRQ_MASKED_STATUS	bt inactive interrupt masked status. Reset State: 0x00000000
19	BT_ACTIVE_IRQ_MASKED_STATUS	bt_active interrupt masked status. Reset State: 0x00000000
18	MTU_TIMER5_MASKED_STATUS	When set, mtu timer5/tsf_timer5 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
17	ADU_IRQ_MASKED_STATUS	adu interrupt masked status. Reset State: 0x00000000
16	MTU_TIMER4_MASKED_STATUS	When set, mtu timer4/tsf_timer4 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
15	RPE_IRQ_MASKED_STATUS	rpe interrupt masked status. Reset State: 0x00000000
13	COMBINED_IRQ_MASKED_STATUS	the combined txp/dpu/dbr/ahb2phy interrupt masked status. See combined_int related registers for detail Reset State: 0x00000000
12	RXP_IRQ_MASKED_STATUS	rxp beacon related interrupt masked status. Reset State: 0x00000000
7	HOST_TO_ACPU_MB3_IRQ_MASKED_STATUS	host to acpu MB3 interrupt masked status. Reset State: 0x00000000
6	HOST_TO_ACPU_MB2_IRQ_MASKED_STATUS	host to acpu MB2 interrupt masked status. Reset State: 0x00000000

MCU_IRQ_MASKED_STATUS (cont.)

Bits	Name	Description
5	HOST_TO_ACPU_MB1_IRQ_MASKED_STATUS	host to acpu MB1 interrupt masked status. Reset State: 0x00000000
4	HOST_TO_ACPU_MB0_IRQ_MASKED_STATUS	host to acpu MB0 interrupt masked status. Reset State: 0x00000000
3	MTU_IRQ_MASKED_STATUS	combined mtu interrupt masked status. See mtu_int related registers for detail Reset State: 0x00000000
2	SW_0_IRQ_MASKED_STATUS	sw 0 interrupt masked status. Reset State: 0x00000000
1	SCU_UART_IRQ_MASKED_STATUS	uart interrupt masked status. Reset State: 0x00000000
0	MTU_WD_1_IRQ_MASKED_STATUS	mtu watchdog timer (warning) interrupt masked status. Reset State: 0x00000000

0x3000254 MCU_IRQ_CLEAR

Type: write-only
Reset State: 0x00000000

This register contains the acpu irq clear signals

MCU_IRQ_CLEAR

Bits	Name	Description
31	SW_1_IRQ_CLEAR	When set, software 1 interrupt is cleared. Reset State: 0x00000000
30	RXP_ERR_IRQ_CLEAR	When set, rxp error interrupt is cleared. Reset State: 0x00000000
29	QTA_IRQ_CLEAR	When set, qta interrupt is cleared. Reset State: 0x00000000
28	MTU_TIMER7_CLEAR	When set, mtu timer7/tsf_timer7 interrupt is cleared Reset State: 0x00000000
27	MTU_TIMER6_CLEAR	When set, mtu timer6/tsf_timer6 interrupt is cleared Reset State: 0x00000000
26	PHY_HIF_IRQ_CLEAR	When set, phy hif interrupt is cleared. Reset State: 0x00000000
25	WQ_DATA_AVAIL_IRQ_CLEAR	When set, wq data available interrupt is cleared. Reset State: 0x00000000

MCU_IRQ_CLEAR (cont.)

Bits	Name	Description
24	PHY_IRQ_IRQ_CLEAR	When set, phy irq interrupt is cleared. Reset State: 0x00000000
23	PHY_FIQ_IRQ_CLEAR	When set, phy fiq interrupt is cleared. Reset State: 0x00000000
22	TPE_IRQ_CLEAR	When set, tpe_mcu_int interrupt is cleared. Reset State: 0x00000000
21	MIF_IRQ_CLEAR	When set, mif interrupt is cleared. Reset State: 0x00000000
20	BT_INACTIVE_IRQ_CLEAR	When set, bt inactive interrupt is cleared. Reset State: 0x00000000
19	BT_ACTIVE_IRQ_CLEAR	When set, bt active interrupt is cleared. Reset State: 0x00000000
18	MTU_TIMER5_CLEAR	When set, mtu timer5/tsf_timer5 interrupt is cleared Reset State: 0x00000000
17	ADU_IRQ_CLEAR	When set, adu interrupt is cleared. Reset State: 0x00000000
16	MTU_TIMER4_CLEAR	When set, mtu timer4/tsf_timer4 interrupt is cleared Reset State: 0x00000000
15	RPE_IRQ_CLEAR	When set, rpe interrupt is cleared. Reset State: 0x00000000
13	COMBINED_IRQ_CLEAR	When set, the combined txp/dpu/dbr/ahb2phy interrupt is cleared. See combined_int related registers for detail Reset State: 0x00000000
12	RXP_IRQ_CLEAR	When set, rxp beacon related interrupt is cleared. Reset State: 0x00000000
7	HOST_TO_ACPU_MB3_IRQ_CLEAR	When set, host to acpu MB3 interrupt is cleared. Reset State: 0x00000000
6	HOST_TO_ACPU_MB2_IRQ_CLEAR	When set, host to acpu MB2 interrupt is cleared. Reset State: 0x00000000
5	HOST_TO_ACPU_MB1_IRQ_CLEAR	When set, host to acpu MB1 interrupt is cleared. Reset State: 0x00000000
4	HOST_TO_ACPU_MB0_IRQ_CLEAR	When set, host to acpu MB0 interrupt is cleared. Reset State: 0x00000000
3	MTU_IRQ_CLEAR	When set, combined mtu interrupt is cleared. See mtu_int related registers for detail Reset State: 0x00000000
2	SW_0_IRQ_CLEAR	When set, software 0 interrupt is cleared. Reset State: 0x00000000

MCU_IRQ_CLEAR (cont.)

Bits	Name	Description
1	SCU_UART_IRQ_CLEAR	When set, uart interrupt is cleared. Reset State: 0x00000000
0	MTU_WD_1_IRQ_CLEAR	When set, mtu watchdog timer (warning) interrupt is cleared. Reset State: 0x00000000

0x3000258 MCU_MTU_INT_EN

Type: read-write
Reset State: 0x00000000

This register contains the mtu interrupt enable signals

MCU_MTU_INT_EN

Bits	Name	Description
14	MTU_MCU_TX_BOUNDARY_INT_EN	When set, mtu-tpe transmit boundary interrupt is enabled Reset State: 0x00000000
13	MTU_ERR_EN	When set, mtu error interrupt is enabled Reset State: 0x00000000
12	WD_ENABLE_DISABLE_ERROR_EN	When set, mtu wd_enable_disable_error interrupt is enabled Reset State: 0x00000000
11	WD_PROTECTION_ERROR_EN	When set, mtu wd_protection_error interrupt is enabled Reset State: 0x00000000
10	RESP_TIMEOUT_MISSING_PKT_PUSH_EN	When set, mtu resp_timeout_missing_pkt_push interrupt is enabled Reset State: 0x00000000
9	RESP_TIMEOUT_MISSING_PKTDET_EN	When set, mtu resp_timeout_missing_pktdet interrupt is enabled Reset State: 0x00000000
8	RESP_TIMEOUT_MISSING_EARLY_PKTDET_EN	When set, mtu resp_timeout_missing_early_pktdet interrupt is enabled Reset State: 0x00000000
7	MTU_PIFS_TO_EN	When set, mtu pifs timeout interrupt is enabled Reset State: 0x00000000
6	MTU_SIFS_TO_EN	When set, mtu sifs timeout interrupt is enabled Reset State: 0x00000000
5	MTU_BKOF1_EN	When set, mtu bkof1 interrupt is enabled Reset State: 0x00000000
4	MTU_BKOF0_EN	When set, mtu bkof0 interrupt is enabled Reset State: 0x00000000

MCU_MTU_INT_EN (cont.)

Bits	Name	Description
3	MTU_TIMER3_EN	When set, mtu timer3/tsf_timer3 interrupt is enabled See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
2	MTU_TIMER2_EN	When set, mtu timer2/tsf_timer2 interrupt is enabled See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
1	MTU_TIMER1_EN	When set, mtu timer1/tsf_timer1 interrupt is enabled See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
0	MTU_TIMER0_EN	When set, mtu timer0/tsf_timer0 interrupt is enabled See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000

0x300025C MCU_MTU_INT_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the mtu interrupt raw status signals

MCU_MTU_INT_STATUS

Bits	Name	Description
14	MTU_MCU_TX_BOUNDARY_INT_STATUS	mtu-tpe transmit boundary interrupt status Reset State: 0x00000000
13	MTU_ERR_STATUS	mtu error interrupt status Reset State: 0x00000000
12	WD_ENABLE_DISABLE_ERROR_STATUS	mtu wd_enable_disable_error interrupt status Reset State: 0x00000000
11	WD_PROTECTION_ERROR_STATUS	mtu wd_protection_error interrupt status Reset State: 0x00000000
10	RESP_TIMEOUT_MISSING_PKT_PUSH_STATUS	mtu resp_timeout_missing_pkt_push interrupt status Reset State: 0x00000000
9	RESP_TIMEOUT_MISSING_PKTDET_STATUS	mtu resp_timeout_missing_pktdet interrupt status Reset State: 0x00000000
8	RESP_TIMEOUT_MISSING_EARLY_PKTDET_STATUS	mtu resp_timeout_missing_early_pktdet interrupt status Reset State: 0x00000000
7	MTU_PIFS_TO_STATUS	mtu pifs timeout interrupt status Reset State: 0x00000000

MCU_MTU_INT_STATUS (cont.)

Bits	Name	Description
6	MTU_SIFS_TO_STATUS	mtu sifs timeout interrupt status Reset State: 0x00000000
5	MTU_BKOF1_STATUS	mtu bkof1 interrupt status Reset State: 0x00000000
4	MTU_BKOF0_STATUS	mtu bkof0 interrupt status Reset State: 0x00000000
3	MTU_TIMER3_STATUS	mtu timer3/tsf timer3 interrupt status Reset State: 0x00000000
2	MTU_TIMER2_STATUS	mtu timer2/tsf timer2 interrupt status Reset State: 0x00000000
1	MTU_TIMER1_STATUS	mtu timer1/tsf timer1 interrupt status Reset State: 0x00000000
0	MTU_TIMER0_STATUS	mtu timer0/tsf timer0 interrupt status Reset State: 0x00000000

0x3000260 MCU_MTU_INT_MASKED_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the mtu interrupt masked status signals

MCU_MTU_INT_MASKED_STATUS

Bits	Name	Description
14	MTU_MCU_TX_BOUNDARY_INT_MASK_STATUS	mtu-tpe transmit boundary interrupt masked status Reset State: 0x00000000
13	MTU_ERR_MASK_STATUS	mtu error interrupt masked status Reset State: 0x00000000
12	WD_ENABLE_DISABLE_ERROR_MASK_STATUS	mtu wd_enable_disable_error interrupt masked status Reset State: 0x00000000
11	WD_PROTECTION_ERROR_MASK_STATUS	mtu wd_protection_error interrupt masked status Reset State: 0x00000000
10	RESP_TIMEOUT_MISSING_PKT_PUSH_MASK_STATUS	mtu resp_timeout_missing_pkt_push interrupt masked status Reset State: 0x00000000
9	RESP_TIMEOUT_MISSING_PKTDET_MASK_STATUS	mtu resp_timeout_missing_pktdet interrupt masked status Reset State: 0x00000000

MCU_MTU_INT_MASKED_STATUS (cont.)

Bits	Name	Description
8	RESP_TIMEOUT_MISSING_EARLY_PKTDET_MASK_STATUS	mtu resp_timeout_missing_early_pktdet interrupt masked status Reset State: 0x00000000
7	MTU_PIFS_TO_MASK_STATUS	mtu pifs timeout interrupt masked status Reset State: 0x00000000
6	MTU_SIFS_TO_MASK_STATUS	mtu sifs timeout interrupt masked status Reset State: 0x00000000
5	MTU_BKOF1_MASK_STATUS	mtu bkof1 interrupt masked status Reset State: 0x00000000
4	MTU_BKOF0_MASK_STATUS	mtu bkof0 interrupt masked status Reset State: 0x00000000
3	MTU_TIMER3_MASK_STATUS	mtu timer3/tsf timer3 interrupt masked status Reset State: 0x00000000
2	MTU_TIMER2_MASK_STATUS	mtu timer2/tsf timer2 interrupt masked status Reset State: 0x00000000
1	MTU_TIMER1_MASK_STATUS	mtu timer1/tsf timer1 interrupt masked status Reset State: 0x00000000
0	MTU_TIMER0_MASK_STATUS	mtu timer0/tsf timer0 interrupt masked status Reset State: 0x00000000

0x3000264 MCU_MTU_INT_CLEAR

Type: write-only
Reset State: 0x00000000

This register contains the mtu interrupt clear signals

MCU_MTU_INT_CLEAR

Bits	Name	Description
14	MTU_MCU_TX_BOUNDARY_INT_CLEAR	When set, mtu-tpe transmit boundary interrupt is cleared Reset State: 0x00000000
13	MTU_ERR_CLEAR	When set, mtu error interrupt is cleared Reset State: 0x00000000
12	WD_ENABLE_DISABLE_ERROR_CLEAR	When set, mtu wd_enable_disable_error interrupt is cleared Reset State: 0x00000000
11	WD_PROTECTION_ERROR_CLEAR	When set, mtu wd_protection_error interrupt is cleared Reset State: 0x00000000

MCU_MTU_INT_CLEAR (cont.)

Bits	Name	Description
10	RESP_TIMEOUT_MISSING_PKT_PUSH_CLEAR	When set, mtu resp_timeout_missing_pkt_push interrupt is cleared Reset State: 0x00000000
9	RESP_TIMEOUT_MISSING_PKTDET_CLEAR	When set, mtu resp_timeout_missing_pktdet interrupt is cleared Reset State: 0x00000000
8	RESP_TIMEOUT_MISSING_EARLY_PKTDET_CLEAR	When set, mtu resp_timeout_missing_early_pktdet interrupt is cleared Reset State: 0x00000000
7	MTU_PIFS_TO_CLEAR	When set, mtu pifs timeout interrupt is cleared Reset State: 0x00000000
6	MTU_SIFS_TO_CLEAR	When set, mtu sifs timeout interrupt is cleared Reset State: 0x00000000
5	MTU_BKOF1_CLEAR	When set, mtu bkof1 interrupt is cleared Reset State: 0x00000000
4	MTU_BKOF0_CLEAR	When set, mtu bkof0 interrupt is cleared Reset State: 0x00000000
3	MTU_TIMER3_CLEAR	When set, mtu timer3/tsf timer3 interrupt is cleared Reset State: 0x00000000
2	MTU_TIMER2_CLEAR	When set, mtu timer2/tsf timer2 interrupt is cleared Reset State: 0x00000000
1	MTU_TIMER1_CLEAR	When set, mtu timer1/tsf timer1 interrupt is cleared Reset State: 0x00000000
0	MTU_TIMER0_CLEAR	When set, mtu timer0/tsf timer0 interrupt is cleared Reset State: 0x00000000

0x3000268 MCU_COMBINED_INT_EN

Type: read-write
Reset State: 0x00000000

This register contains the combined interrupt enable signals

MCU_COMBINED_INT_EN

Bits	Name	Description
23	WLAN_BRIDGE_AHB_ERR_INT_EN	When set, the wlan bridge ahb error interrupt is enabled Reset State: 0x00000000
21	BTC_PATTERN_DET_INT_EN	When set, btc_pattern_det_int_p interrupt is enabled Reset State: 0x00000000

MCU_COMBINED_INT_EN (cont.)

Bits	Name	Description
20	BTC_SCO_INT_EN	When set, btc_sco_int_p interrupt is enabled Reset State: 0x00000000
19	TPE_MCU_WRONG_SSN_OR_TID_ERROR_P_EN	When set, tpe_mcu_wrong_ssn_or_tid_error_p interrupt is enabled Reset State: 0x00000000
18	TPE_MCU_BD_BASED_TX_INT_1_P_EN	When set, tpe_mcu_bd_based_tx_int_1_p interrupt is enabled Reset State: 0x00000000
17	TPE_MCU_BD_BASED_TX_INT_0_P_EN	When set, tpe_mcu_bd_based_tx_int_0_p interrupt is enabled Reset State: 0x00000000
16	TPE_MCU_ERROR_VAILD_P_EN	When set, tpe_mcu_error_vaild_p interrupt is enabled Reset State: 0x00000000
15	TPE_MCU_GOT_ACK_FOR_BACK_P_EN	When set, tpe_mcu_got_ack_for_back_p interrupt is enabled Reset State: 0x00000000
14	BMU_MCU_PWRSTATE_DROP_INT_EN	When set, bmu_mcu_pwrstate_drop_interrupt is enabled Reset State: 0x00000000
13	BMU_MCU_PWRSTATE_CHANGE_INT_EN	When set, bmu_mcu_pwrstate_change_interrupt is enabled Reset State: 0x00000000
12	BMU_MCU_BTQM_QUEUES_EMPTY_INTERRUPT_EN	When set, bmu_mcu_btqm_queues_empty_interrupt interrupt is enabled Reset State: 0x00000000
11	BMU_MCU_ERR_INT_EN	When set, bmu_mcu_err_int interrupt is enabled Reset State: 0x00000000
10	AHB2PHY_MCU_TIMOUT_ERROR2_EN	When set, ahb2phy_mcu_timout_error2 interrupt is enabled Reset State: 0x00000000
9	AHB2PHY_MCU_TIMOUT_ERROR1_EN	When set, ahb2phy_mcu_timout_error1 interrupt is enabled Reset State: 0x00000000
8	DBR_MCU_GAM_ERR_EN	When set, dbr_mcu_gam_err interrupt is enabled Reset State: 0x00000000
7	DBR_MCU_INCORRECT_LENGTH_ERR_EN	When set, dbr_mcu_incorrect_length_err interrupt is enabled Reset State: 0x00000000
6	DPU_MCU_MICERR_P_EN	When set, dpu_mcu_micerr_p interrupt is enabled Reset State: 0x00000000
5	DPU_MCU_ERRINTR_P_EN	When set, dpu_mcu_errintr_p interrupt is enabled Reset State: 0x00000000
4	BMU_MCU_QUEUE_USAGE_THRESHOLD_INTERRUPT_EN	When set, bmu_mcu_queue_usage_threshold_interrupt is enabled Reset State: 0x00000000
3	ACPU_MCU_MIF_TIMEOUT_INT_P_EN	When set, acpu_mcu_mif_timeout_int_p interrupt is enabled Reset State: 0x00000000

MCU_COMBINED_INT_EN (cont.)

Bits	Name	Description
2	ACPU_MCU_AHB_ERR_INT_P_EN	When set, acpu_mcu_ahb_err_int_p interrupt is enabled Reset State: 0x00000000
1	TXP_MCU_TXP_TIMEOUT_INT_P_EN	When set, txp_mcu_txp_timeout_int_p interrupt is enabled Reset State: 0x00000000
0	TXP_MCU_ERR_INT_EN	When set, txp_mcu_err_int interrupt is enabled Reset State: 0x00000000

0x300026C MCU_COMBINED_INT_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the combined interrupt raw status signals

MCU_COMBINED_INT_STATUS

Bits	Name	Description
23	WLAN_BRIDGE_AHB_ERR_INT_STATUS	wlan bridge ahb error interrupt status Reset State: 0x00000000
21	BTC_PATTERN_DET_INT_P_STATUS	btc_pattern_det_int_p interrupt status Reset State: 0x00000000
20	BTC_SCO_INT_P_STATUS	btc_sco_int_p interrupt status Reset State: 0x00000000
19	TPE_MCU_WRONG_SSN_OR_TID_ERROR_P_STATUS	tpe_mcu_wrong_ssn_or_tid_error_p interrupt status Reset State: 0x00000000
18	TPE_MCU_BD_BASED_TX_INT_1_P_STATUS	tpe_mcu_bd_based_tx_int_1_p interrupt status Reset State: 0x00000000
17	TPE_MCU_BD_BASED_TX_INT_0_P_STATUS	tpe_mcu_bd_based_tx_int_0_p interrupt status Reset State: 0x00000000
16	TPE_MCU_ERROR_VAILD_P_STATUS	tpe_mcu_error_vaild_p interrupt status Reset State: 0x00000000
15	TPE_MCU_GOT_ACK_FOR_BACK_P_STATUS	tpe_mcu_got_ack_for_back_p interrupt status Reset State: 0x00000000
14	BMU_MCU_PWRSTATE_DROP_INT_STATUS	bmu_mcu_pwrstate_drop_interrupt status Reset State: 0x00000000
13	BMU_MCU_PWRSTATE_CHANGE_INT_STATUS	bmu_mcu_pwrstate_change_interrupt status Reset State: 0x00000000

MCU_COMBINED_INT_STATUS (cont.)

Bits	Name	Description
12	BMU_MCU_BTQM_QUEUES_EMPTY_INTERRUPT_STATUS	bmu_mcu_btqm_queues_empty_interrupt interrupt status Reset State: 0x00000000
11	BMU_MCU_ERR_INT_STATUS	bmu_mcu_err_int interrupt status Reset State: 0x00000000
10	AHB2PHY_MCU_TIMOUT_ERROR2_STATUS	ahb2phy_mcu_timout_error2 interrupt status Reset State: 0x00000000
9	AHB2PHY_MCU_TIMOUT_ERROR1_STATUS	ahb2phy_mcu_timout_error1 interrupt status Reset State: 0x00000000
8	DBR_MCU_GAM_ERR_STATUS	dbr_mcu_gam_err interrupt status Reset State: 0x00000000
7	DBR_MCU_INCORRECT_LENGTH_ERR_STATUS	dbr_mcu_incorrect_length_err interrupt status Reset State: 0x00000000
6	DPU_MCU_MICERR_P_STATUS	dpu_mcu_micerr_p interrupt status Reset State: 0x00000000
5	DPU_MCU_ERRINTR_P_STATUS	dpu_mcu_errintr_p interrupt status Reset State: 0x00000000
4	BMU_MCU_QUEUE_USAGE_THRESHOLD_INTERRUPT_STATUS	bmu_mcu_queue_usage_threshold_interrupt interrupt status Reset State: 0x00000000
3	ACPU_MCU_MIF_TIMEOUT_INT_P_STATUS	acpu_mcu_mif_timeout_int_p interrupt status Reset State: 0x00000000
2	ACPU_MCU_AHB_ERR_INT_P_STATUS	acpu_mcu_ahb_err_int_p interrupt status Reset State: 0x00000000
1	TXP_MCU_TXP_TIMEOUT_INT_P_STATUS	txp_mcu_txp_timeout_int_p interrupt status Reset State: 0x00000000
0	TXP_MCU_ERR_INT_STATUS	txp_mcu_err_int interrupt status Reset State: 0x00000000

0x3000270 MCU_COMBINED_INT_MASKED_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the combined interrupt masked status signals

MCU_COMBINED_INT_MASKED_STATUS

Bits	Name	Description
23	WLAN_BRIDGE_AHB_ERR_INT_MASK_STATUS	wlan bridge ahb error interrupt masked status Reset State: 0x00000000
21	BTC_PATTERN_DET_INT_P_MASK_STATUS	btc_pattern_det_int_p interrupt masked status Reset State: 0x00000000
20	BTC_SCO_INT_P_MASK_STATUS	btc_sco_int_p interrupt masked status Reset State: 0x00000000
19	TPE_MCU_WRONG_SSN_OR_TID_ERROR_P_MASK_STATUS	tpe_mcu_wrong_ssn_or_tid_error_p interrupt masked status Reset State: 0x00000000
18	TPE_MCU_BD_BASED_TX_INT_1_P_MASK_STATUS	tpe_mcu_bd_based_tx_int_1_p interrupt masked status Reset State: 0x00000000
17	TPE_MCU_BD_BASED_TX_INT_0_P_MASK_STATUS	tpe_mcu_bd_based_tx_int_0_p interrupt masked status Reset State: 0x00000000
16	TPE_MCU_ERROR_VAILD_P_MASK_STATUS	tpe_mcu_error_vaild_p interrupt masked status Reset State: 0x00000000
15	TPE_MCU_GOT_ACK_FOR_BACK_P_MASK_STATUS	tpe_mcu_got_ack_for_back_p interrupt masked status Reset State: 0x00000000
14	BMU_MCU_PWRSTATE_DROP_INT_MASK_STATUS	bmu_mcu_pwrstate_drop_interrupt masked status Reset State: 0x00000000
13	BMU_MCU_PWRSTATE_CHANGE_INT_MASK_STATUS	bmu_mcu_pwrstate_change_interrupt masked status Reset State: 0x00000000
12	BMU_MCU_BTQM_QUEUES_EMPTY_INTERRUPT_MASK_STATUS	bmu_mcu_btqm_queues_empty_interrupt interrupt masked status Reset State: 0x00000000
11	BMU_MCU_ERR_INT_MASK_STATUS	bmu_mcu_err_int interrupt masked status Reset State: 0x00000000
10	AHB2PHY_MCU_TIMOUT_ERROR2_MASK_STATUS	ahb2phy_mcu_timout_error2 interrupt masked status Reset State: 0x00000000
9	AHB2PHY_MCU_TIMOUT_ERROR1_MASK_STATUS	ahb2phy_mcu_timout_error1 interrupt masked status Reset State: 0x00000000
8	DBR_MCU_GAM_ERR_MASK_STATUS	dbr_mcu_gam_err interrupt masked status Reset State: 0x00000000
7	DBR_MCU_INCORRECT_LENGTH_ERR_MASK_STATUS	dbr_mcu_incorrect_length_err interrupt masked status Reset State: 0x00000000
6	DPU_MCU_MICERR_P_MASK_STATUS	dpu_mcu_micerr_p interrupt masked status Reset State: 0x00000000
5	DPU_MCU_ERRINTR_P_MASK_STATUS	dpu_mcu_errintr_p interrupt masked status Reset State: 0x00000000

MCU_COMBINED_INT_MASKED_STATUS (cont.)

Bits	Name	Description
4	BMU_MCU_QUEUE_USAGE_THRESHOLD_INTERRUPT_MASK_STATUS	bmu_mcu_queue_usage_threshold_interrupt interrupt masked status Reset State: 0x00000000
3	ACPU_MCU_MIF_TIMEOUT_INT_P_MASK_STATUS	acpu_mcu_mif_timeout_int_p interrupt masked status Reset State: 0x00000000
2	ACPU_MCU_AHB_ERR_INT_P_MASK_STATUS	acpu_mcu_ahb_err_int_p interrupt masked status Reset State: 0x00000000
1	TXP_MCU_TXP_TIMEOUT_INT_P_MASK_STATUS	txp_mcu_txp_timeout_int_p interrupt masked status Reset State: 0x00000000
0	TXP_MCU_ERR_INT_MASK_STATUS	txp_mcu_err_int interrupt masked status Reset State: 0x00000000

0x3000274 MCU_COMBINED_INT_CLEAR

Type: read-write
Reset State: 0x00000000

This register contains the combined interrupt clear signals

MCU_COMBINED_INT_CLEAR

Bits	Name	Description
23	WLAN_BRIDGE_AHB_ERR_INT_CLEAR	When set, wlan bridge ahb error interrupt is cleared Reset State: 0x00000000
21	BTC_PATTERN_DET_INT_CLEAR	When set, btc_pattern_det_int_p interrupt is cleared Reset State: 0x00000000
20	BTC_SCO_INT_CLEAR	When set, btc_sco_int_p interrupt is cleared Reset State: 0x00000000
19	TPE_MCU_WRONG_SSN_OR_TID_ERROR_P_CLEAR	When set, tpe_mcu_wrong_ssn_or_tid_error_p interrupt is cleared Reset State: 0x00000000
18	TPE_MCU_BD_BASED_TX_INT_1_P_CLEAR	When set, tpe_mcu_bd_based_tx_int_1_p interrupt is cleared Reset State: 0x00000000
17	TPE_MCU_BD_BASED_TX_INT_0_P_CLEAR	When set, tpe_mcu_bd_based_tx_int_0_p interrupt is cleared Reset State: 0x00000000
16	TPE_MCU_ERROR_VAILD_P_CLEAR	When set, tpe_mcu_error_vaild_p interrupt is cleared Reset State: 0x00000000
15	TPE_MCU_GOT_ACK_FOR_BACK_P_CLEAR	When set, tpe_mcu_got_ack_for_back_p interrupt is cleared Reset State: 0x00000000

MCU_COMBINED_INT_CLEAR (cont.)

Bits	Name	Description
14	BMU_MCU_PWRSTATE_DROP_INT_CLEAR	When set, bmu_mcu_pwrstate_drop_interrupt is cleared Reset State: 0x00000000
13	BMU_MCU_PWRSTATE_CHANGE_INT_CLEAR	When set, bmu_mcu_pwrstate_change_interrupt is cleared Reset State: 0x00000000
12	BMU_MCU_BTQM_QUEUES_EMPTY_INTERRUPT_CLEAR	When set, bmu_mcu_btqm_queues_empty_interrupt interrupt is cleared Reset State: 0x00000000
11	BMU_MCU_ERR_INT_CLEAR	When set, bmu_mcu_err_int interrupt is cleared Reset State: 0x00000000
10	AHB2PHY_MCU_TIMOUT_ERROR2_CLEAR	When set, ahb2phy_mcu_timout_error2 interrupt is cleared Reset State: 0x00000000
9	AHB2PHY_MCU_TIMOUT_ERROR1_CLEAR	When set, ahb2phy_mcu_timout_error1 interrupt is cleared Reset State: 0x00000000
8	DBR_MCU_GAM_ERR_CLEAR	When set, dbr_mcu_gam_err interrupt is cleared Reset State: 0x00000000
7	DBR_MCU_INCORRECT_LENGTH_ERR_CLEAR	When set, dbr_mcu_incorrect_length_err interrupt is cleared Reset State: 0x00000000
6	DPU_MCU_MICERR_P_CLEAR	When set, dpu_mcu_micerr_p interrupt is cleared Reset State: 0x00000000
5	DPU_MCU_ERRINTR_P_CLEAR	When set, dpu_mcu_errintr_p interrupt is cleared Reset State: 0x00000000
4	BMU_MCU_QUEUE_USAGE_THRESHOLD_INTERRUPT_CLEAR	When set, bmu_mcu_queue_usage_threshold_interrupt_clear interrupt is cleared Reset State: 0x00000000
3	ACPU_MCU_MIF_TIMEOUT_INT_P_CLEAR	When set, acpu_mcu_mif_timeout_int_p interrupt is cleared Reset State: 0x00000000
2	ACPU_MCU_AHB_ERR_INT_P_CLEAR	When set, acpu_mcu_ahb_err_int_p interrupt is cleared Reset State: 0x00000000
1	TXP_MCU_TXP_TIMEOUT_INT_P_CLEAR	When set, txp_mcu_txp_timeout_int_p interrupt is cleared Reset State: 0x00000000
0	TXP_MCU_ERR_INT_CLEAR	When set, txp_mcu_err_int interrupt is cleared Reset State: 0x00000000

0x3000278 MCU_BMU_WQ_INT_EN

Type: read-write
Reset State: 0x00000000

This register contains the bmu wq data available interrupt enable signals

MCU_BMU_WQ_INT_EN

Bits	Name	Description
24:2	BMU_WQ_INT_EN	BMU WQ 2-24 data available Reset State: 0x00000000

0x300027C MCU_BMU_WQ_INT_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the bmu wq data available interrupt raw status signals

MCU_BMU_WQ_INT_STATUS

Bits	Name	Description
24:2	BMU_WQ_INT_STATUS	BMU WQ 2-24 data available Reset State: 0x00000000

0x3000280 MCU_BMU_WQ_INT_MASKED_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the bmu wq data available interrupt masked status signals

MCU_BMU_WQ_INT_MASKED_STATUS

Bits	Name	Description
24:2	BMU_WQ_INT_MASKED_STATUS	BMU WQ 2-24 data available Reset State: 0x00000000

0x3000284 MCU_BMU_WQ_INT_CLEAR

Type: write-only
Reset State: 0x00000000

This register contains the bmu wq data available interrupt clear signals

MCU_BMU_WQ_INT_CLEAR

Bits	Name	Description
24:2	BMU_WQ_INT_CLEAR	BMU WQ 2-24 data available Reset State: 0x00000000

0x3000298 MCU_SW_INT_0

Type: read-write
Reset State: 0x00000000

This register contains the software interrupt signals

MCU_SW_INT_0

Bits	Name	Description
0	COMBINED_INT_EN	SW generated interrupt Reset State: 0x00000000

0x300029C MCU_SW_INT_1

Type: read-write
Reset State: 0x00000000

This register contains the software interrupt signals

MCU_SW_INT_1

Bits	Name	Description
0	COMBINED_INT_EN	SW generated interrupt1 Reset State: 0x00000000

0x30002A0 MCU_MCU_HOST_INT_EN

Type: read-write
Reset State: 0x00000000

This register contains the mcu_host interrupt enable signals

MCU_MCU_HOST_INT_EN

Bits	Name	Description
11	RESERVE	This bit is reserved. Reset State: 0x00000000
10	ADU_ERR_WQ_DA_AVAIL_EN	When set, adu_err_wq_da_avail interrupt is enabled Reset State: 0x00000000
9	DPU_ERR_WQ_DA_AVAIL_EN	When set, dpu_err_wq_da_avail interrupt is enabled Reset State: 0x00000000
8	MTU_TIMER3_EN	When set, mtu timer3/tsf_timer3 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
7	MTU_TIMER2_EN	When set, mtu timer2/tsf_timer2 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
6	MB3_EN	When set, mb3 interrupt is enabled Reset State: 0x00000000
5	MB2_EN	When set, mb2 interrupt is enabled Reset State: 0x00000000
4	MB1_EN	When set, mb1 interrupt is enabled Reset State: 0x00000000
3	MB0_EN	When set, mb0 interrupt is enabled Reset State: 0x00000000
2	DPU_MIC_ERROR_EN	When set, dpu mic error interrupt is enabled Reset State: 0x00000000
1	MTU_WATCHDOG_EN	When set, mtu watchdog interrupt is enabled Reset State: 0x00000000

0x30002A4 MCU_MCU_HOST_INT_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the mcu_host interrupt raw status signals

MCU_MCU_HOST_INT_STATUS

Bits	Name	Description
11	RESERVE	This bit is reserve Reset State: 0x00000000
10	ADU_ERR_WQ_DA_AVAIL_STATUS	adu_err_wq_da_avail status Reset State: 0x00000000

MCU_MCU_HOST_INT_STATUS (cont.)

Bits	Name	Description
9	DPU_ERR_WQ_DA_AVAIL_STATUS	dpu_err_wq_da_avail status Reset State: 0x00000000
8	MTU_TIMER3_STATUS	mtu timer3/tsf_timer3 status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
7	MTU_TIMER2_STATUS	mtu timer2/tsf_timer2 status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
6	MB3_STATUS	mb3 status Reset State: 0x00000000
5	MB2_STATUS	mb2 status Reset State: 0x00000000
4	MB1_STATUS	mb1 status Reset State: 0x00000000
3	MB0_STATUS	mb0 status Reset State: 0x00000000
2	DPU_MIC_ERROR_STATUS	dpu mic error status Reset State: 0x00000000
1	MTU_WATCHDOG_STATUS	mtu watchdog status Reset State: 0x00000000

0x30002A8 MCU_MCU_HOST_INT_MASKED_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the mcu_host interrupt masked status signals

MCU_MCU_HOST_INT_MASKED_STATUS

Bits	Name	Description
11	RESERVE	This bit is reserve Reset State: 0x00000000
10	ADU_ERR_WQ_DA_AVAIL_MASK_STATUS	adu_err_wq_da_avail masked status Reset State: 0x00000000
9	DPU_ERR_WQ_DA_AVAIL_MASK_STATUS	dpu_err_wq_da_avail masked status Reset State: 0x00000000
8	MTU_TIMER3_MASK_STATUS	mtu timer2/tsf_timer2 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000

MCU_MCU_HOST_INT_MASKED_STATUS (cont.)

Bits	Name	Description
7	MTU_TIMER2_MASK_STATUS	mtu timer2/tsf_timer2 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
6	MB3_MASK_STATUS	mb3 masked status Reset State: 0x00000000
5	MB2_MASK_STATUS	mb2 masked status Reset State: 0x00000000
4	MB1_MASK_STATUS	mb1 masked status Reset State: 0x00000000
3	MB0_MASK_STATUS	mb0 masked status Reset State: 0x00000000
2	DPU_MIC_ERROR_MASK_STATUS	dpu mic error masked status Reset State: 0x00000000
1	MTU_WATCHDOG_MASK_STATUS	mtu watchdog masked status Reset State: 0x00000000

0x30002AC MCU_MCU_HOST_INT_CLEAR

Type: write-only
Reset State: 0x00000000

This register contains the mcu_host interrupt clear signals

MCU_MCU_HOST_INT_CLEAR

Bits	Name	Description
11	RESERVE	This bit is reserve for future usage Reset State: 0x00000000
10	ADU_ERR_WQ_DA_AVAIL_CLEAR	When set, clear adu_err_wq_da_avail interrupt Reset State: 0x00000000
9	DPU_ERR_WQ_DA_AVAIL_CLEAR	When set, clear dpu_err_wq_da_avail interrupt Reset State: 0x00000000
8	MTU_TIMER3_CLEAR	When set, clear mtu timer3/tsf_timer3 interrupt Reset State: 0x00000000
7	MTU_TIMER2_CLEAR	When set, clear mtu timer2/tsf_timer2 interrupt Reset State: 0x00000000
6	MB3_CLEAR	When set, clear mb3 interrupt Reset State: 0x00000000

MCU_MCU_HOST_INT_CLEAR (cont.)

Bits	Name	Description
5	MB2_CLEAR	When set, clear mb2 interrupt Reset State: 0x00000000
4	MB1_CLEAR	When set, clear mb1 interrupt Reset State: 0x00000000
3	MB0_CLEAR	When set, clear mb0 interrupt Reset State: 0x00000000
2	DPU_MIC_ERROR_CLEAR	When set, clear dpu mic error interrupt Reset State: 0x00000000
1	MTU_WATCHDOG_CLEAR	When set, clear mtu watchdog interrupt Reset State: 0x00000000

0x30002B0 MCU_MCU_PMU_INFO

Type: read-write
Reset State: 0x00000000

This register contains the RF register reinitialization is done information

MCU_MCU_PMU_INFO

Bits	Name	Description
0	MCU_PMU_RF_REINIT_DONE	SW writes to this register to tell pmu that RF reg reinit is done. Reset State: 0x00000000

0x30002B4 MCU_MCU_WMAC_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the wmac modules status

MCU_MCU_WMAC_STATUS

Bits	Name	Description
10	ACPU_MCU_STATUS	When set, acpu is busy. Reset State: 0x00000000
9	SIF_MCU_STATUS	When set, sif is busy. Reset State: 0x00000000
8	BTQM_MCU_STATUS	When set, btqm queue is not empty. Reset State: 0x00000000

MCU_MCU_WMAC_STATUS (cont.)

Bits	Name	Description
7	BMU_MCU_STATUS	When set, bmu wq is not empty. Reset State: 0x00000000
6	TPE_MCU_STATUS	When set, tpe is busy. Reset State: 0x00000000
5	TXP_MCU_STATUS	When set, txp is busy. Reset State: 0x00000000
4	DXE_MCU_STATUS	When set, dxe is busy. Reset State: 0x00000000
3	ADU_MCU_STATUS	When set, adu is busy. Reset State: 0x00000000
2	DPU_MCU_STATUS	When set, dpu is busy. Reset State: 0x00000000
1	RPE_MCU_STATUS	When set, rpe is busy. Reset State: 0x00000000
0	RXP_MCU_STATUS	When set, rxp is busy. Reset State: 0x00000000

0x30002B8 MCU_MAC_HOST_INT_EN

Type: read-write
Reset State: 0x00000000

This register contains the mac to host interrupt enable signals. The bit order is the same as those in the IRQ/FIQ register which are used by acpu, this is dedicated for host.

MCU_MAC_HOST_INT_EN

Bits	Name	Description
31	SW_1_INT_EN	When set, software 1 interrupt is enabled. Reset State: 0x00000000
30	RXP_ERR_INT_EN	When set, rxp error interrupt is enabled. Reset State: 0x00000000
29	QTA_INT_EN	When set, qta interrupt is enabled. Reset State: 0x00000000
28	MTU_TIMER7_EN	When set, mtu timer7/tsf_timer7 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
27	MTU_TIMER6_EN	When set, mtu timer6/tsf_timer6 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000

MCU_MAC_HOST_INT_EN (cont.)

Bits	Name	Description
26	PHY_HIF_INT_EN	When set, phy hif interrupt is enabled. Reset State: 0x00000000
25	WQ_DATA_AVAIL_INT_EN	When set, wq data available interrupt is enabled. Reset State: 0x00000000
24	PHY_IRQ_INT_EN	When set, phy irq interrupt is enabled. Reset State: 0x00000000
23	PHY_FIQ_INT_EN	When set, phy fiq interrupt is enabled. Reset State: 0x00000000
22	TPE_INT_EN	When set, tpe_mcu_int interrupt is enabled. Reset State: 0x00000000
21	MIF_INT_EN	When set, mif interrupt is enabled. Reset State: 0x00000000
20	BT_INACTIVE_INT_EN	When set, bt_inactive interrupt is enabled. Reset State: 0x00000000
19	BT_ACTIVE_INT_EN	When set, bt active interrupt is enabled. Reset State: 0x00000000
18	MTU_TIMER5_EN	When set, mtu timer5/tsf_timer5 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
17	ADU_INT_EN	When set, adu interrupt is enabled. Reset State: 0x00000000
16	MTU_TIMER4_EN	When set, mtu timer4/tsf_timer4 interrupt is enabled. See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
15	RPE_INT_EN	When set, rpe interrupt is enabled. Reset State: 0x00000000
13	COMBINED_INT_EN	When set, the combined txp/dpu/dbr/ahb2phy interrupt is enabled. See combined_int related registers for detail Reset State: 0x00000000
12	RXP_INT_EN	When set, rxp beacon related interrupt is enabled. Reset State: 0x00000000
7	ACPU_TO_HOST_MB3_INT_EN	When set, acpu to host MB3 interrupt is enabled. Reset State: 0x00000000
6	ACPU_TO_HOST_MB2_INT_EN	When set, acpu to host MB2 interrupt is enabled. Reset State: 0x00000000
5	ACPU_TO_HOST_MB1_INT_EN	When set, acpu to host MB1 interrupt is enabled. Reset State: 0x00000000
4	ACPU_TO_HOST_MB0_INT_EN	When set, acpu to host MB0 interrupt is enabled. Reset State: 0x00000000

MCU_MAC_HOST_INT_EN (cont.)

Bits	Name	Description
3	MTU_INT_EN	When set, combined mtu interrupt is enabled. See mtu_int related registers for detail Reset State: 0x00000000
2	SW_0_INT_EN	When set, software 0 interrupt is enabled. Reset State: 0x00000000
1	SCU_UART_INT_EN	When set, uart interrupt is enabled. Reset State: 0x00000000
0	MTU_WD_1_INT_EN	When set, mtu watchdog timer (warning) interrupt is enabled. Reset State: 0x00000000

0x30002BC MCU_MAC_HOST_INT_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the mac to host interrupt raw status signals. The bit order is the same as those in the IRQ/FIQ register which are used by acpu, this is dedicated for host.

MCU_MAC_HOST_INT_STATUS

Bits	Name	Description
31	SW_1_INT_STATUS	sw 1 interrupt status. Reset State: 0x00000000
30	RXP_ERR_INT_STATUS	rxp error interrupt status. Reset State: 0x00000000
29	QTA_INT_STATUS	qta interrupt status Reset State: 0x00000000
28	MTU_TIMER7_STATUS	When set, mtu timer7/tsf_timer7 interrupt status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
27	MTU_TIMER6_STATUS	When set, mtu timer6/tsf_timer6 interrupt status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
26	PHY_HIF_INT_STATUS	phy hif interrupt status. Reset State: 0x00000000
25	WQ_DATA_AVAIL_INT_STATUS	wq data available interrupt status. Reset State: 0x00000000
24	PHY_IRQ_INT_STATUS	phy irq interrupt status. Reset State: 0x00000000

MCU_MAC_HOST_INT_STATUS (cont.)

Bits	Name	Description
23	PHY_FIQ_INT_STATUS	phy fiq interrupt status. Reset State: 0x00000000
22	TPE_INT_STATUS	tpe_mcu_int interrupt status. Reset State: 0x00000000
21	MIF_INT_STATUS	mif interrupt status. Reset State: 0x00000000
20	BT_INACTIVE_INT_STATUS	bt inactive interrupt status. Reset State: 0x00000000
19	BT_ACTIVE_INT_STATUS	bt active interrupt status. Reset State: 0x00000000
18	MTU_TIMER5_STATUS	When set, mtu timer5/tsf_timer5 interrupt status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
17	ADU_INT_STATUS	adu interrupt status. Reset State: 0x00000000
16	MTU_TIMER4_STATUS	When set, mtu timer4/tsf_timer4 interrupt status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
15	RPE_INT_STATUS	rpe interrupt status. Reset State: 0x00000000
13	COMBINED_INT_STATUS	the combined txp/dpu/dbr/ahb2phy interrupt status. See combined_int related registers for detail Reset State: 0x00000000
12	RXP_INT_STATUS	rxp beacon related interrupt status. Reset State: 0x00000000
7	ACPU_TO_HOST_MB3_INT_STATUS	acpu to host MB3 interrupt status. Reset State: 0x00000000
6	ACPU_TO_HOST_MB2_INT_STATUS	acpu to host MB2 interrupt status. Reset State: 0x00000000
5	ACPU_TO_HOST_MB1_INT_STATUS	acpu to host MB1 interrupt status. Reset State: 0x00000000
4	ACPU_TO_HOST_MB0_INT_STATUS	acpu to host MB0 interrupt status. Reset State: 0x00000000
3	MTU_INT_STATUS	combined mtu interrupt status. See mtu_int related registers for detail Reset State: 0x00000000
2	SW_0_INT_STATUS	sw 0 interrupt status. Reset State: 0x00000000

MCU_MAC_HOST_INT_STATUS (cont.)

Bits	Name	Description
1	SCU_UART_INT_STATUS	uart interrupt status. Reset State: 0x00000000
0	MTU_WD_1_INT_STATUS	mtu watchdog timer (warning) interrupt status. Reset State: 0x00000000

0x30002C0 MCU_MAC_HOST_INT_MASKED_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the mac to host interrupt masked status. The bit order is the same as those in the IRQ/FIQ register which are used by acpu, this is dedicated for host.

MCU_MAC_HOST_INT_MASKED_STATUS

Bits	Name	Description
31	SW_1_INT_MASKED_STATUS	sw 1 interrupt masked status. Reset State: 0x00000000
30	RXP_ERR_INT_MASKED_STATUS	rxp error interrupt masked status. Reset State: 0x00000000
29	QTA_INT_MASKED_STATUS	qta interrupt masked status Reset State: 0x00000000
28	MTU_TIMER7_MASKED_STATUS	When set, mtu timer7/tsf_timer7 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
27	MTU_TIMER6_MASKED_STATUS	When set, mtu timer6/tsf_timer6 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
26	PHY_HIF_INT_MASKED_STATUS	phy hif interrupt masked status. Reset State: 0x00000000
25	WQ_DATA_AVAIL_INT_MASKED_STATUS	wq data available interrupt masked status. Reset State: 0x00000000
24	PHY_IRQ_INT_MASKED_STATUS	phy irq interrupt masked status. Reset State: 0x00000000
23	PHY_FIQ_INT_MASKED_STATUS	phy fiq interrupt masked status. Reset State: 0x00000000
22	TPE_INT_MASKED_STATUS	tpe_mcu_int interrupt masked status. Reset State: 0x00000000
21	MIF_INT_MASKED_STATUS	mif interrupt masked status. Reset State: 0x00000000

MCU_MAC_HOST_INT_MASKED_STATUS (cont.)

Bits	Name	Description
20	BT_INACTIVE_INT_MASKED_STATUS	bt inactive interrupt masked status. Reset State: 0x00000000
19	BT_ACTIVE_INT_MASKED_STATUS	bt active interrupt masked status. Reset State: 0x00000000
18	MTU_TIMER5_MASKED_STATUS	When set, mtu timer5/tsf_timer5 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
17	ADU_INT_MASKED_STATUS	adu interrupt masked status. Reset State: 0x00000000
16	MTU_TIMER4_MASKED_STATUS	When set, mtu timer4/tsf_timer4 masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
15	RPE_INT_MASKED_STATUS	rpe interrupt masked status. Reset State: 0x00000000
13	COMBINED_INT_MASKED_STATUS	the combined txp/dpu/dbr/ahb2phy interrupt masked status. See combined_int related registers for detail Reset State: 0x00000000
12	RXP_INT_MASKED_STATUS	rxp beacon related interrupt masked status. Reset State: 0x00000000
7	ACPU_TO_HOST_MB3_INT_MASKED_STATUS	acpu to host MB3 interrupt masked status. Reset State: 0x00000000
6	ACPU_TO_HOST_MB2_INT_MASKED_STATUS	acpu to host MB2 interrupt masked status. Reset State: 0x00000000
5	ACPU_TO_HOST_MB1_INT_MASKED_STATUS	acpu to host MB1 interrupt masked status. Reset State: 0x00000000
4	ACPU_TO_HOST_MB0_INT_MASKED_STATUS	acpu to host MB0 interrupt masked status. Reset State: 0x00000000
3	MTU_INT_MASKED_STATUS	combined mtu interrupt masked status. See mtu_int related registers for detail Reset State: 0x00000000
2	SW_0_INT_MASKED_STATUS	sw 0 interrupt masked status. Reset State: 0x00000000
1	SCU_UART_INT_MASKED_STATUS	uart interrupt masked status. Reset State: 0x00000000
0	MTU_WD_1_INT_MASKED_STATUS	mtu watchdog timer (warning) interrupt masked status. Reset State: 0x00000000

0x30002C4 MCU_MAC_HOST_INT_CLEAR

Type: write-only
Reset State: 0x00000000

This register contains the mac to host interrupt clear signals. The bit order is the same as those in the IRQ/FIQ register which are used by acpu, this is dedicated for host.

MCU_MAC_HOST_INT_CLEAR

Bits	Name	Description
31	SW_1_INT_CLEAR	When set, software 1 interrupt is cleared. Reset State: 0x00000000
30	RXP_ERR_INT_CLEAR	When set, rxp error interrupt is cleared. Reset State: 0x00000000
29	QTA_INT_CLEAR	When set, qta interrupt is cleared. Reset State: 0x00000000
28	MTU_TIMER7_CLEAR	When set, mtu timer7/tsf_timer7 interrupt is cleared Reset State: 0x00000000
27	MTU_TIMER6_CLEAR	When set, mtu timer6/tsf_timer6 interrupt is cleared Reset State: 0x00000000
26	PHY_HIF_INT_CLEAR	When set, phy hif interrupt is cleared. Reset State: 0x00000000
25	WQ_DATA_AVAIL_INT_CLEAR	When set, wq data available interrupt is cleared. Reset State: 0x00000000
24	PHY_IRQ_INT_CLEAR	When set, phy irq interrupt is cleared. Reset State: 0x00000000
23	PHY_FIQ_INT_CLEAR	When set, phy fiq interrupt is cleared. Reset State: 0x00000000
22	TPE_INT_CLEAR	When set, tpe_mcu_int interrupt is cleared. Reset State: 0x00000000
21	MIF_INT_CLEAR	When set, mif interrupt is cleared. Reset State: 0x00000000
20	BT_INACTIVE_INT_CLEAR	When set, bt inactive interrupt is cleared. Reset State: 0x00000000
19	BT_ACTIVE_INT_CLEAR	When set, bt active interrupt is cleared. Reset State: 0x00000000
18	MTU_TIMER5_CLEAR	When set, mtu timer5/tsf_timer5 interrupt is cleared Reset State: 0x00000000
17	ADU_INT_CLEAR	When set, adu interrupt is cleared. Reset State: 0x00000000

MCU_MAC_HOST_INT_CLEAR (cont.)

Bits	Name	Description
16	MTU_TIMER4_CLEAR	When set, mtu timer4/tsf_timer4 interrupt is cleared Reset State: 0x00000000
15	RPE_INT_CLEAR	When set, rpe interrupt is cleared. Reset State: 0x00000000
13	COMBINED_INT_CLEAR	When set, the combined txp/dpu/dbr/ahb2phy interrupt is cleared. See combined_int related registers for detail Reset State: 0x00000000
12	RXP_INT_CLEAR	When set, rxp beacon related interrupt is cleared. Reset State: 0x00000000
7	ACPU_TO_HOST_MB3_INT_CLEAR	When set, acpu to host MB3 interrupt is cleared. Reset State: 0x00000000
6	ACPU_TO_HOST_MB2_INT_CLEAR	When set, acpu to host MB2 interrupt is cleared. Reset State: 0x00000000
5	ACPU_TO_HOST_MB1_INT_CLEAR	When set, acpu to host MB1 interrupt is cleared. Reset State: 0x00000000
4	ACPU_TO_HOST_MB0_INT_CLEAR	When set, acpu to host MB0 interrupt is cleared. Reset State: 0x00000000
3	MTU_INT_CLEAR	When set, combined mtu interrupt is cleared. See mtu_int related registers for detail Reset State: 0x00000000
2	SW_0_INT_CLEAR	When set, software 0 interrupt is cleared. Reset State: 0x00000000
1	SCU_UART_INT_CLEAR	When set, uart interrupt is cleared. Reset State: 0x00000000
0	MTU_WD_1_INT_CLEAR	When set, mtu watchdog timer (warning) interrupt is cleared. Reset State: 0x00000000

0x30002C8 MCU_MTU_HOST_INT_EN

Type: read-write
Reset State: 0x00000000

This register contains the mtu interrupt enable signals

MCU_MTU_HOST_INT_EN

Bits	Name	Description
14	MTU_MCU_TX_BOUNDARY_INT_HOSTINT_EN	When set, mtu_mcu_tx_boundary_int interrupt is enabled Reset State: 0x00000000

MCU_MTU_HOST_INT_EN (cont.)

Bits	Name	Description
13	MTU_ERR_HOSTINT_EN	When set, mtu error interrupt is enabled Reset State: 0x00000000
12	WD_ENABLE_DISABLE_ERROR_HOSTINT_EN	When set, mtu wd_enable_disable_error interrupt is enabled Reset State: 0x00000000
11	WD_PROTECTION_ERROR_HOSTINT_EN	When set, mtu wd_protection_error interrupt is enabled Reset State: 0x00000000
10	RESP_TIMEOUT_MISSING_PKT_PUSH_HOSTINT_EN	When set, mtu resp_timeout_missing_pkt_push interrupt is enabled Reset State: 0x00000000
9	RESP_TIMEOUT_MISSING_PKTDET_HOSTINT_EN	When set, mtu resp_timeout_missing_pktdet interrupt is enabled Reset State: 0x00000000
8	RESP_TIMEOUT_MISSING_EARLY_PKTDET_HOSTINT_EN	When set, mtu resp_timeout_missing_early_pktdet interrupt is enabled Reset State: 0x00000000
7	MTU_PIFS_TO_HOSTINT_EN	When set, mtu pifs timeout interrupt is enabled Reset State: 0x00000000
6	MTU_SIFS_TO_HOSTINT_EN	When set, mtu sifs timeout interrupt is enabled Reset State: 0x00000000
5	MTU_BKOF1_HOSTINT_EN	When set, mtu bkof1 interrupt is enabled Reset State: 0x00000000
4	MTU_BKOF0_HOSTINT_EN	When set, mtu bkof0 interrupt is enabled Reset State: 0x00000000
3	MTU_TIMER3_HOSTINT_EN	When set, mtu timer3/tsf_timer3 interrupt is enabled See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
2	MTU_TIMER2_HOSTINT_EN	When set, mtu timer2/tsf_timer2 interrupt is enabled See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
1	MTU_TIMER1_HOSTINT_EN	When set, mtu timer1/tsf_timer1 interrupt is enabled See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
0	MTU_TIMER0_HOSTINT_EN	When set, mtu timer0/tsf_timer0 interrupt is enabled See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000

0x30002CC MCU_MTU_HOST_INT_MASKED_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the mtu interrupt masked status signals

MCU_MTU_HOST_INT_MASKED_STATUS

Bits	Name	Description
14	MTU_MCU_TX_BOUNDARY_INT_HOSTINT_MASK_STATUS	tu_mcu_tx_boundary_int interrupt masked status Reset State: 0x00000000
13	MTU_ERR_HOSTINT_MASK_STATUS	mtu error interrupt masked status Reset State: 0x00000000
12	WD_ENABLE_DISABLE_ERROR_HOSTINT_MASK_STATUS	mtu wd_enable_disable_error interrupt masked status Reset State: 0x00000000
11	WD_PROTECTION_ERROR_HOSTINT_MASK_STATUS	mtu wd_protection_error interrupt masked status Reset State: 0x00000000
10	RESP_TIMEOUT_MISSING_PKT_PUSH_HOSTINT_MASK_STATUS	mtu resp_timeout_missing_pkt_push interrupt masked status Reset State: 0x00000000
9	RESP_TIMEOUT_MISSING_PKTDET_HOSTINT_MASK_STATUS	mtu resp_timeout_missing_pktdet interrupt masked status Reset State: 0x00000000
8	RESP_TIMEOUT_MISSING_EARLY_PKTDET_HOSTINT_MASK_STATUS	mtu resp_timeout_missing_early_pktdet interrupt masked status Reset State: 0x00000000
7	MTU_PIFS_TO_HOSTINT_MASK_STATUS	mtu pifs timeout interrupt masked status Reset State: 0x00000000
6	MTU_SIFS_TO_HOSTINT_MASK_STATUS	mtu sifs timeout interrupt masked status Reset State: 0x00000000
5	MTU_BKOF1_HOSTINT_MASK_STATUS	mtu bkof1 interrupt masked status Reset State: 0x00000000
4	MTU_BKOF0_HOSTINT_MASK_STATUS	mtu bkof0 interrupt masked status Reset State: 0x00000000
3	MTU_TIMER3_HOSTINT_MASK_STATUS	mtu timer3/tsf_timer3 interrupt masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
2	MTU_TIMER2_HOSTINT_MASK_STATUS	mtu timer2/tsf_timer2 interrupt masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
1	MTU_TIMER1_HOSTINT_MASK_STATUS	mtu timer1/tsf_timer1 interrupt masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000
0	MTU_TIMER0_HOSTINT_MASK_STATUS	mtu timer0/tsf_timer0 interrupt masked status See register 'MTU_TIMER_INTERRUPT_SOURCE' for timer selection Reset State: 0x00000000

0x30002D0 MCU_COMBINED_HOST_INT_EN

Type: read-write
Reset State: 0x00000000

This register contains the combined interrupt enable signals

MCU_COMBINED_HOST_INT_EN

Bits	Name	Description
23	WLAN_BRIDGE_AHB_ERR_INT_HOSTINT_EN	When set, wlan bridge ahb error interrupt is enabled Reset State: 0x00000000
21	BTC_PATTERN_DET_INT_HOSTINT_EN	When set, btc_pattern_det_int_p interrupt is enabled Reset State: 0x00000000
20	BTC_SCO_INT_HOSTINT_EN	When set, btc_sco_int_p interrupt is enabled Reset State: 0x00000000
19	TPE_MCU_WRONG_SSN_OR_TID_ERROR_P_HOSTINT_EN	When set, tpe_mcu_wrong_ssn_or_tid_error_p interrupt is enabled Reset State: 0x00000000
18	TPE_MCU_BD_BASED_TX_INT_1_P_HOSTINT_EN	When set, tpe_mcu_bd_based_tx_int_1_p interrupt is enabled Reset State: 0x00000000
17	TPE_MCU_BD_BASED_TX_INT_0_P_HOSTINT_EN	When set, tpe_mcu_bd_based_tx_int_0_p interrupt is enabled Reset State: 0x00000000
16	TPE_MCU_ERROR_VAILD_P_HOSTINT_EN	When set, tpe_mcu_error_vaild_p interrupt is enabled Reset State: 0x00000000
15	TPE_MCU_GOT_ACK_FOR_BACK_P_HOSTINT_EN	When set, tpe_mcu_got_ack_for_back_p interrupt is enabled Reset State: 0x00000000
14	BMU_MCU_PWRSTATE_DROP_INT_EN	When set, bmu_mcu_pwrstate_drop_interrupt interrupt is enabled Reset State: 0x00000000
13	BMU_MCU_PWRSTATE_CHANGE_INT_EN	When set, bmu_mcu_pwrstate_change_interrupt interrupt is enabled Reset State: 0x00000000
12	BMU_MCU_BTQM_QUEUES_EMPTY_INTERRUPT_HOSTINT_EN	When set, bmu_mcu_btqm_queues_empty_interrupt interrupt is enabled Reset State: 0x00000000
11	BMU_MCU_ERR_INT_HOSTINT_EN	When set, bmu_mcu_err_int interrupt is enabled Reset State: 0x00000000
10	AHB2PHY_MCU_TIMOUT_ERROR2_HOSTINT_EN	When set, ahb2phy_mcu_timout_error2 interrupt is enabled Reset State: 0x00000000
9	AHB2PHY_MCU_TIMOUT_ERROR1_HOSTINT_EN	When set, ahb2phy_mcu_timout_error1 interrupt is enabled Reset State: 0x00000000
8	DBR_MCU_GAM_ERR_HOSTINT_EN	When set, dbr_mcu_gam_err interrupt is enabled Reset State: 0x00000000

MCU_COMBINED_HOST_INT_EN (cont.)

Bits	Name	Description
7	DBR_MCU_INCORRECT_LENGTH_ERR_HOSTINT_EN	When set, dbr_mcu_incorrect_length_err interrupt is enabled Reset State: 0x00000000
6	DPU_MCU_MICERR_P_HOSTINT_EN	When set, dpu_mcu_micerr_p interrupt is enabled Reset State: 0x00000000
5	DPU_MCU_ERRINTR_P_HOSTINT_EN	When set, dpu_mcu_errintr_p interrupt is enabled Reset State: 0x00000000
4	BMU_MCU_QUEUE_USAGE_THRESHOLD_INTERRUPT_EN	When set, bmu_mcu_queue_usage_threshold_interrupt is enabled Reset State: 0x00000000
3	ACPU_MCU_MIF_TIMEOUT_INT_P_HOSTINT_EN	When set, acpu_mcu_mif_timeout_int_p interrupt is enabled Reset State: 0x00000000
2	ACPU_MCU_AHB_ERR_INT_P_HOSTINT_EN	When set, acpu_mcu_ahb_err_int_p interrupt is enabled Reset State: 0x00000000
1	TXP_MCU_TXP_TIMEOUT_INT_P_HOSTINT_EN	When set, txp_mcu_txp_timeout_int_p interrupt is enabled Reset State: 0x00000000
0	TXP_MCU_ERR_INT_HOSTINT_EN	When set, txp_mcu_err_int interrupt is enabled Reset State: 0x00000000

0x30002D4 MCU_COMBINED_HOST_INT_MASKED_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the combined interrupt masked status signals

MCU_COMBINED_HOST_INT_MASKED_STATUS

Bits	Name	Description
23	WLAN_BRIDGE_AHB_ERR_INT_HOSTINT_MASK_STATUS	wlan bridge ahb error interrupt masked status Reset State: 0x00000000
21	BTC_PATTERN_DET_INT_P_HOSTINT_MASK_STATUS	btc_pattern_det_int_p interrupt masked status Reset State: 0x00000000
20	BTC_SCO_INT_P_HOSTINT_MASK_STATUS	btc_sco_int_p interrupt masked status Reset State: 0x00000000
19	TPE_MCU_WRONG_SSN_OR_TID_ERROR_P_HOSTINT_MASK_STATUS	tpe_mcu_wrong_ssn_or_tid_error_p interrupt masked status Reset State: 0x00000000
18	TPE_MCU_BD_BASED_TX_INT_1_P_HOSTINT_MASK_STATUS	tpe_mcu_bd_based_tx_int_1_p interrupt masked status Reset State: 0x00000000

MCU_COMBINED_HOST_INT_MASKED_STATUS (cont.)

Bits	Name	Description
17	TPE_MCU_BD_BASED_TX_INT_0_P_HOSTINT_MASK_STATUS	tpe_mcu_bd_based_tx_int_0_p interrupt masked status Reset State: 0x00000000
16	TPE_MCU_ERROR_VAILD_P_HOSTINT_MASK_STATUS	tpe_mcu_error_vaild_p interrupt masked status Reset State: 0x00000000
15	TPE_MCU_GOT_ACK_FOR_BACK_P_HOSTINT_MASK_STATUS	tpe_mcu_got_ack_for_back_p interrupt masked status Reset State: 0x00000000
14	BMU_MCU_PWRSTATE_DROP_INT_STATUS	bmu_mcu_pwrstate_drop_interrupt masked status Reset State: 0x00000000
13	BMU_MCU_PWRSTATE_CHANGE_INT_STATUS	bmu_mcu_pwrstate_change_interrupt masked status Reset State: 0x00000000
12	BMU_MCU_BTQM_QUEUES_EMPTY_INTERRUPT_HOSTINT_MASK_STATUS	bmu_mcu_btqm_queues_empty_interrupt interrupt masked status Reset State: 0x00000000
11	BMU_MCU_ERR_INT_HOSTINT_MASK_STATUS	bmu_mcu_err_int interrupt masked status Reset State: 0x00000000
10	AHB2PHY_MCU_TIMOUT_ERROR2_HOSTINT_MASK_STATUS	ahb2phy_mcu_timout_error2 interrupt masked status Reset State: 0x00000000
9	AHB2PHY_MCU_TIMOUT_ERROR1_HOSTINT_MASK_STATUS	ahb2phy_mcu_timout_error1 interrupt masked status Reset State: 0x00000000
8	DBR_MCU_GAM_ERR_HOSTINT_MASK_STATUS	dbr_mcu_gam_err interrupt masked status Reset State: 0x00000000
7	DBR_MCU_INCORRECT_LENGTH_ERR_HOSTINT_MASK_STATUS	dbr_mcu_incorrect_length_err interrupt masked status Reset State: 0x00000000
6	DPU_MCU_MICERR_P_HOSTINT_MASK_STATUS	dpu_mcu_micerr_p interrupt masked status Reset State: 0x00000000
5	DPU_MCU_ERRINTR_P_HOSTINT_MASK_STATUS	dpu_mcu_errintr_p interrupt masked status Reset State: 0x00000000
4	BMU_MCU_QUEUE_USAGE_THRESHOLD_INTERRUPT_STATUS	bmu_mcu_queue_usage_threshold_interrupt interrupt status Reset State: 0x00000000
3	ACPU_MCU_MIF_TIMEOUT_INT_P_HOSTINT_MASK_STATUS	acpu_mcu_mif_timeout_int_p interrupt masked status Reset State: 0x00000000
2	ACPU_MCU_AHB_ERR_INT_P_HOSTINT_MASK_STATUS	acpu_mcu_ahb_err_int_p interrupt masked status Reset State: 0x00000000

MCU_COMBINED_HOST_INT_MASKED_STATUS (cont.)

Bits	Name	Description
1	TXP_MCU_TXP_TIMEOUT_INT_P_HOSTINT_MASK_STATUS	txp_mcu_txp_timeout_int_p interrupt masked status Reset State: 0x00000000
0	TXP_MCU_ERR_INT_HOSTINT_MASK_STATUS	txp_mcu_err_int interrupt masked status Reset State: 0x00000000

0x30002D8 MCU_BMU_WQ_HOST_INT_EN

Type: read-write
Reset State: 0x00000000

This register contains the bmu wq data available interrupt enable signals

MCU_BMU_WQ_HOST_INT_EN

Bits	Name	Description
24:2	BMU_WQ_HOST_INT_EN	BMU WQ 2-24 data available Reset State: 0x00000000

0x30002DC MCU_BMU_WQ_HOST_INT_MASKED_STATUS

Type: read-only
Reset State: 0x00000000

This register contains the bmu wq data available interrupt masked status signals

MCU_BMU_WQ_HOST_INT_MASKED_STATUS

Bits	Name	Description
24:2	BMU_WQ_HOST_INT_MASKED_STATUS	BMU WQ 2-24 data available Reset State: 0x00000000

0x30002E0 MCU_MTU_TIMER_INTERRUPT_SOURCE

Type: read-write
Reset State: 0x00000000

This register controls which interrupt, TSF based or timer based, interrupt from MTU is selected

MCU_MTU_TIMER_INTERRUPT_SOURCE

Bits	Name	Description
7	TSF_TIMER7_INT_SELECT	When set, in all interrupt related registers indicating mtu timer7/tsf_timer7 interrupt, the interrupt source is set to TSF. When NOT set, the interrupt source is set to mtu timer 7 Reset State: 0x00000000
6	TSF_TIMER6_INT_SELECT	When set, in all interrupt related registers indicating mtu timer6/tsf_timer6 interrupt, the interrupt source is set to TSF. When NOT set, the interrupt source is set to mtu timer 6 Reset State: 0x00000000
5	TSF_TIMER5_INT_SELECT	When set, in all interrupt related registers indicating mtu timer5/tsf_timer5 interrupt, the interrupt source is set to TSF. When NOT set, the interrupt source is set to mtu timer 5 Reset State: 0x00000000
4	TSF_TIMER4_INT_SELECT	When set, in all interrupt related registers indicating mtu timer4/tsf_timer4 interrupt, the interrupt source is set to TSF. When NOT set, the interrupt source is set to mtu timer 4 Reset State: 0x00000000
3	TSF_TIMER3_INT_SELECT	When set, in all interrupt related registers indicating mtu timer3/tsf_timer3 interrupt, the interrupt source is set to TSF. When NOT set, the interrupt source is set to mtu timer 3 Reset State: 0x00000000
2	TSF_TIMER2_INT_SELECT	When set, in all interrupt related registers indicating mtu timer2/tsf_timer2 interrupt, the interrupt source is set to TSF. When NOT set, the interrupt source is set to mtu timer 2 Reset State: 0x00000000
1	TSF_TIMER1_INT_SELECT	When set, in all interrupt related registers indicating mtu timer1/tsf_timer1 interrupt, the interrupt source is set to TSF. When NOT set, the interrupt source is set to mtu timer 1 Reset State: 0x00000000
0	TSF_TIMER0_INT_SELECT	When set, in all interrupt related registers indicating mtu timer0/tsf_timer0 interrupt, the interrupt source is set to TSF. When NOT set, the interrupt source is set to mtu timer 0 Reset State: 0x00000000

0x3000300 MCU_BTC_CTRL4

Type: read-write
Reset State: 0x00000000

This register is to set up the pta.

MCU_BTC_CTRL4

Bits	Name	Description
15:0	SCO_INTERRUPT_OFFSET	The btc_sco_int will be trigger when the sco period counter matches the value When MSB is '1', the interrupt is to be triggered the programmed time after the bt_active assertion When MSB is '0', the interrupt is to be triggered the programmed time before the bt_active assertion Reset State: 0x00000000

0x3000304 MCU_BTC_PATTERN_DET1

Type: read-write
Reset State: 0x00000000

This register contains the info for pattern detection

MCU_BTC_PATTERN_DET1

Bits	Name	Description
15:0	DATA	The mask bits for pattern detection. The LSB should be 1. Reset State: 0x00000000

0x3000308 MCU_BTC_PATTERN_DET2

Type: read-write
Reset State: 0x00000000

This register contains the set up for pattern detection

MCU_BTC_PATTERN_DET2

Bits	Name	Description
31:16	BT_PRIORITY_PATTERN_DET	The bt_priority pattern for pattern detection Reset State: 0x00000000
15:0	BT_ACTIVE_PATTERN_DET	The bt_active pattern for pattern detection Reset State: 0x00000000

0x300030C MCU_BTC_PATTERN_HISTORY

Type: read-only
Reset State: 0x00000000

This register contains the history of bt_active and bt_priority

MCU_BTC_PATTERN_HISTORY

Bits	Name	Description
31:16	BT_PRIORITY_HISTORY	The bt_prioroity history Reset State: 0x00000000
15:0	BT_ACTIVE_HISTORY	The bt_active history Reset State: 0x00000000

0x3000310 MCU_BTC_HI_GRANT

Type: read-write
Reset State: 0x00000000

This register counts the stats of bt high priority grant

MCU_BTC_HI_GRANT

Bits	Name	Description
31:20	BT_HI_PRI_GRANT_CNT	BT high priority grant counts Reset State: 0x00000000
19:0	BT_HI_PRI_GRANT_TIME	BT high priority grant time in microseconds. Reset State: 0x00000000

0x3000314 MCU_BTC_LOW_GRANT

Type: read-write
Reset State: 0x00000000

This register contains the stats of bt log priority grant

MCU_BTC_LOW_GRANT

Bits	Name	Description
31:20	BT_LOW_PRI_GRANT_CNT	BT low priority grant counts Reset State: 0x00000000
19:0	BT_LOW_PRI_GRANT_TIME	BT low priority grant time in microseconds. Reset State: 0x00000000

0x3000318 MCU_BTC_REQ_CNT

Type: read-write
Reset State: 0x00000000

This register is to set up the pta.

MCU_BTC_REQ_CNT

Bits	Name	Description
23:12	BT_LO_PRI_REQ_CNT	BT low priority requests. Reset State: 0x00000000
11:0	BT_HI_PRI_REQ_CNT	BT high priority requests. Reset State: 0x00000000

0x300031C MCU_MRCM_CLK_GATE_DISABLE

Type: read-write
Reset State: 0x00003883

This register controls the dynamic clock gating of the wmac modules in mrcm

MCU_MRCM_CLK_GATE_DISABLE

Bits	Name	Description
13	MCU_MRCM_FDAHB_GCU_CLK_GATE_DISABLE	When set, disable fdahb dynamic clock gating Reset State: 0x00000001
12	MCU_MRCM_FDBR_GCU_CLK_GATE_DISABLE	When set, disable fdbr dynamic clock gating Reset State: 0x00000001
11	MCU_MRCM_CBR_GCU_CLK_GATE_DISABLE	When set, disable cbr dynamic clock gating Reset State: 0x00000001
10	MCU_MRCM_TXP_GCU_CLK_GATE_DISABLE	When set, disable txp dynamic clock gating Reset State: 0x00000000
9	MCU_MRCM_CFG_GCU_CLK_GATE_DISABLE	When set, disable cfg dynamic clock gating Reset State: 0x00000000
8	MCU_MRCM_RXP_GCU_CLK_GATE_DISABLE	When set, disable rxp dynamic clock gating Reset State: 0x00000000
7	MCU_MRCM_DBR_GCU_CLK_GATE_DISABLE	When set, disable dbr dynamic clock gating Reset State: 0x00000001
6	MCU_MRCM_BMU_GCU_CLK_GATE_DISABLE	When set, disable bmu dynamic clock gating Reset State: 0x00000000
5	MCU_MRCM_DPU_GCU_CLK_GATE_DISABLE	When set, disable dpu dynamic clock gating Reset State: 0x00000000
4	MCU_MRCM_ADU_GCU_CLK_GATE_DISABLE	When set, disable adu dynamic clock gating Reset State: 0x00000000
3	MCU_MRCM_TPE_GCU_CLK_GATE_DISABLE	When set, disable tpe dynamic clock gating Reset State: 0x00000000

MCU_MRCM_CLK_GATE_DISABLE (cont.)

Bits	Name	Description
2	MCU_MRCM_RPE_GCU_CLK_GATE_DISABLE	When set, disable rpe dynamic clock gating Reset State: 0x00000000
1	MCU_MRCM_CAHB_GCU_CLK_GATE_DISABLE	When set, disable cahb dynamic clock gating Reset State: 0x00000001
0	MCU_MRCM_DAHB_GCU_CLK_GATE_DISABLE	When set, disable dahb dynamic clock gating Reset State: 0x00000001

0x3000320 MCU_TXP_BUSY_CNT

Type: read-write
Reset State: 0x00000000

This register controls the counter counting on the time when txp is busy

MCU_TXP_BUSY_CNT

Bits	Name	Description
23:0	TXP_BUSY_CNT	The time (in unit of us) when txp is busy Reset State: 0x00000000

0x3000324 MCU_WLAN_BRIDGE_CTRL

Type: read-write
Reset State: 0x00000000

This register contains the control signal to the wlan bridges

MCU_WLAN_BRIDGE_CTRL

Bits	Name	Description
23:20	MCU_FDBR_CDAHB2FDAHB_TBUS_SEL	The testbus control signal for fdbr cdahb2fdahb Reset State: 0x00000000
19:16	MCU_FDBR_FDAHB2CDAHB_TBUS_SEL	The testbus control signal for fdbr fdahb2cdahb Reset State: 0x00000000
15:12	MCU_DBR_CDAHB2DAHB_TBUS_SEL	The testbus control signal for dbr dahb2cdahb Reset State: 0x00000000
11:8	MCU_DBR_DAHB2CDAHB_TBUS_SEL	The testbus control signal for dbr dahb2cdahb Reset State: 0x00000000
7:4	MCU_CBR_CCAHB2CAHB_TBUS_SEL	The testbus control signal for cbr ccahb2cahb Reset State: 0x00000000

MCU_WLAN_BRIDGE_CTRL (cont.)

Bits	Name	Description
3:0	MCU_CBR_CAHB2CCAHB_TBUS_SEL	The testbus control signal for cbr cahb2ccahb Reset State: 0x00000000

0x3000328 MCU_WLAN_BRIDGE_AHB_ERR_ADDR

Type: read-only
Reset State: 0x00000000

This register controls the address for which the AHB bus error happened

MCU_WLAN_BRIDGE_AHB_ERR_ADDR

Bits	Name	Description
31:0	ERR_ADDR	The address of the AHB bus error Reset State: 0x00000000

0x300032C MCU_WLAN_BRIDGE_AHB_ERR_SRC

Type: read-only
Reset State: 0x00000000

This register controls the bridge which generate the ahb error

MCU_WLAN_BRIDGE_AHB_ERR_SRC

Bits	Name	Description
5	FDBR_MCU_FDAHB_ERR	The source of the ahb error is fdbr fdahb Reset State: 0x00000000
4	FDBR_MCU_CDAHB_ERR	The source of the ahb error is fdbr cdahb Reset State: 0x00000000
3	DBR_MCU_DAHB_ERR	The source of the ahb error is dbr cahb Reset State: 0x00000000
2	DBR_MCU_CDAHB_ERR	The source of the ahb error is dbr cdahb Reset State: 0x00000000
1	CBR_MCU_CAHB_ERR	The source of the ahb error is cbr cahb Reset State: 0x00000000
0	CBR_MCU_CCAHB_ERR	The source of the ahb error is cbr ccahb Reset State: 0x00000000

16.2.43 mtu

0x3000000 MTU_DIFS_LIMIT_0TO3

Type: read-write
Reset State: 0x1C1C2525

AIFS limit register for 0 to 3 back off engines. The value is in micro seconds Though the name is DIFS, it is used for both DIFS,AIFS. It is up to software to select the value

MTU_DIFS_LIMIT_0TO3

Bits	Name	Description
31:24	SW_MTU_DIFS_LIMIT_3	AIFS value in micro seconds for the back-off engine 3 Reset State: 0x0000001C
23:16	SW_MTU_DIFS_LIMIT_2	AIFS value in micro seconds for the back-off engine 2 Reset State: 0x0000001C
15:8	SW_MTU_DIFS_LIMIT_1	AIFS value in micro seconds for the back-off engine 1 Reset State: 0x00000025
7:0	SW_MTU_DIFS_LIMIT_0	AIFS value in micro seconds for the back-off engine 0 Reset State: 0x00000025

0x3000004 MTU_DIFS_LIMIT_4TO7

Type: read-write
Reset State: 0x1F431616

AIFS limit register for 4 to 7 back off engines. The value is in micro seconds Though the name is DIFS, it is used for both DIFS,AIFS. It is up to software to select the value

MTU_DIFS_LIMIT_4TO7

Bits	Name	Description
31:24	SW_MTU_DIFS_LIMIT_7	AIFS value in micro seconds for the back-off engine 7 Reset State: 0x0000001F
23:16	SW_MTU_DIFS_LIMIT_6	AIFS value in micro seconds for the back-off engine 6 Reset State: 0x00000043
15:8	SW_MTU_DIFS_LIMIT_5	AIFS value in micro seconds for the back-off engine 5 Reset State: 0x00000016
7:0	SW_MTU_DIFS_LIMIT_4	AIFS value in micro seconds for the back-off engine 4 Reset State: 0x00000016

0x3000008 MTU_EIFS_PIFS_SLOT_LIMIT

Type: read-write
Reset State: 0x005A1309

This register contains the limits for eifs, pifs and the slot_limit for data and bcn

MTU_EIFS_PIFS_SLOT_LIMIT

Bits	Name	Description
31:16	SW_MTU_EIFS_LIMIT	EIFS value in micro seconds Reset State: 0x0000005A
15:8	SW_PIFS_LIMIT	PIFS value in micro seconds Reset State: 0x00000013
7:0	SW_MTU_SLOT_LIMIT	slot limit value in micro seconds for all the back-off engines Reset State: 0x00000009

0x300000C MTU_SW_MTU_BCN_SLOT_USEC_SIFS_LIMIT

Type: read-write
Reset State: 0x20007714

This register contains the limits for beacon slot microseconds pulse generation sifs.

MTU_SW_MTU_BCN_SLOT_USEC_SIFS_LIMIT

Bits	Name	Description
31:24	SW_MTU_EARLY_PKT_DET_MISS_LIMIT	sw_mtu_early_pkt_det_miss_limit-- this is used in respons_to(ack_to) logic if the system is expecting a response and if the early pkt_det is HIGH for this limit, an interrupt is generated (old name is cca_miss_limit) Reset State: 0x00000020
15:8	SW_MTU_ONE_USEC_LIMIT	limit value to be programmed to get one microseconds pulse. Basically this is number of clk cycles. this value is loaded into a counter and keep getting decremented at every clk. Reset State: 0x00000077
7:0	SW_MTU_BCN_SLOT_LIMIT	slot limit value in micro seconds for all the back-off engines Reset State: 0x00000014

0x3000010 MTU_SW_MTU_MISC_LIMITS

Type: read-write
Reset State: 0x0C20091E

This register contains the limits for one microseconds puls and for programmable pulse generation the programmable pulse is sued by the timers in one of the modes and the software delay limits

MTU_SW_MTU_MISC_LIMITS

Bits	Name	Description
31:24	SW_MTU_PUSH_MISS_LIMIT	Limit to control the missing_push interrupt. If pkt_det goes high and we don't get a packet from the rxp before this limit, the interrupt will go. Reset State: 0x0000000C
21:16	SW_MTU_TXP_DELAY_LIMIT	TXP is indicated earlier indication of transmission of a pkt. The number in this register indicates the delay between the indication to software and the corresponding flag set that goes to txp The actual delay is the number programmed multiplied by the sw_mtu_txp_delay_pulse_limit multiplied by 8ns Reset State: 0x00000020
11:8	SW_MTU_TXP_DELAY_PULSE_LIMIT	this number dictates the resolution of the delay between the software interrupt and the corresponding txp flag Reset State: 0x00000009
7:0	TIMER_RESOLUTION_LIMIT	A pulse is generated at the end of 'this limit' number of 120mhz pulses. This pulse represents the resolution in timers. Reset State: 0x0000001E

0x3000014 MTU_NAV_CNT

Type: read-write
Reset State: 0x000000FF

This register contains the nav value. NAV is updated by hardware as well as by the software. Software has higher priority over the hardware updates

MTU_NAV_CNT

Bits	Name	Description
31:0	NAV_CNT	This register contains the nav value. The value is in micro seconds Reset State: 0x000000FF

0x3000018 MTU_TSF_TIMER_LO

Type: read-write
Reset State: 0x00000000

This register contains the lower 32 bits of the tsf timer

MTU_TSF_TIMER_LO

Bits	Name	Description
31:0	TSF_TIMER_LO	This register contains the lower 32 bits of tsf timer Reset State: 0x00000000

0x300001C MTU_TSF_TIMER_HI

Type: read-write
Reset State: 0x00000000

This register contains the upper 32 bits of the tsf timer

MTU_TSF_TIMER_HI

Bits	Name	Description
31:0	TSF_TIMER_HI	This register contains the upper 32 bits of tsf timer Reset State: 0x00000000

0x3000020 MTU_TIMER_0

Type: read-write
Reset State: 0x00EFFFFF

This register contains the timer 0 value. This timer is rd/writable,up/down Based on the configuration, this can be used either for up or down counter and generates an interrupt on reaching Zero in down mode. in up mode interrupt is generated when the timer reaches the sw_match_register_0.

MTU_TIMER_0

Bits	Name	Description
23:0	TIMER_0	This register contains the timer 0 value. This timer is rd/writable,up/down Reset State: 0x00EFFFFF

0x3000024 MTU_TIMER_1

Type: read-write
Reset State: 0x00EFFFFF

This register contains the timer 1 value. This timer is rd/writable,up/down Based on the configuration, this can be used either for up or down counter and generates an interrupt on

reaching Zero in down mode. in up mode interrupt is generated when the timer reaches the sw_match_register_1.

MTU_TIMER_1

Bits	Name	Description
23:0	TIMER_1	This register contains the timer 1 value. This timer is rd/writable,up/down Reset State: 0x00EFFFFF

0x3000028 MTU_TIMER_2

Type: read-write
Reset State: 0x00EFFFFF

This register contains the timer 2 value. This timer is rd/writable,up/down Based on the configuration, this can be used either for up or down counter and generates an interrupt on reaching Zero in down mode. in up mode interrupt is generated when the timer reaches the sw_match_register_2.

MTU_TIMER_2

Bits	Name	Description
23:0	TIMER_2	This register contains the timer 2 value. This timer is rd/writable,up/down Reset State: 0x00EFFFFF

0x300002C MTU_TIMER_3

Type: read-write
Reset State: 0x00EFFFFF

This register contains the timer 3 value. This timer is rd/writable,up/down Based on the configuration, this can be used either for up or down counter and generates an interrupt on reaching Zero in down mode. in up mode interrupt is generated when the timer reaches the sw_match_register_3.

MTU_TIMER_3

Bits	Name	Description
23:0	TIMER_3	This register contains the timer 3 value. This timer is rd/writable,up/down Reset State: 0x00EFFFFF

0x3000030 MTU_TIMER_4

Type: read-write
Reset State: 0x00EFFFFF

This register contains the timer 4 value. This timer is rd/writable,up/down Based on the configuration, this can be used either for up or down counter and generates an interrupt on reaching Zero in down mode. in up mode interrupt is generated when the timer reaches the sw_match_register_4.

MTU_TIMER_4

Bits	Name	Description
23:0	TIMER_4	This register contains the timer 4 value. This timer is rd/writable,up/down Reset State: 0x00EFFFFF

0x3000034 MTU_TIMER_5

Type: read-write
Reset State: 0x00EFFFFF

This register contains the timer 5 value. This timer is rd/writable,up/down Based on the configuration, this can be used either for up or down counter and generates an interrupt on reaching Zero in down mode. in up mode interrupt is generated when the timer reaches the sw_match_register_5.

MTU_TIMER_5

Bits	Name	Description
23:0	TIMER_5	This register contains the timer 5 value. This timer is rd/writable,up/down Reset State: 0x00EFFFFF

0x3000038 MTU_TIMER_6

Type: read-write
Reset State: 0x00EFFFFF

This register contains the timer 6 value. This timer is rd/writable,up/down Based on the configuration, this can be used either for up or down counter and generates an interrupt on reaching Zero in down mode. in up mode interrupt is generated when the timer reaches the sw_match_register_6.

MTU_TIMER_6

Bits	Name	Description
23:0	TIMER_6	This register contains the timer 6 value. This timer is rd/writable,up/down Reset State: 0x00EFFFFF

0x300003C MTU_TIMER_7

Type: read-write
Reset State: 0x00EFFFFF

This register contains the timer 7 value. This timer is rd/writable,up/down Based on the configuration, this can be used either for up or down counter and generates an interrupt on reaching Zero in down mode. in up mode interrupt is generated when the timer reaches the sw_match_register_7.

MTU_TIMER_7

Bits	Name	Description
23:0	TIMER_7	This register contains the timer 7 value. This timer is rd/writable,up/down Reset State: 0x00EFFFFF

0x3000040 MTU_TIMER_CONTROL

Type: read-write
Reset State: 0x00000000

This register contains all the controls for the timers.

MTU_TIMER_CONTROL

Bits	Name	Description
31:16	SW_MTU_BASIC_UNIT_SELECT	2 bit for each timer is provided. bit [1:0] for timer 0, bit [3:2] for timer 1... To make these timers more flexible, 3 basic units are provided. if the control =0, the timer will be stopped (this is the only way to disable the counters if the control =01, timer is ++ at every clk if the control =10, timer is ++ at every one us if the control =11, timer is ++ at every programmable pulse. Basically in this mode, the period of the pulse is also controlled by software. Note that this programmable pulse is only one for all the timers Reset State: 0x00000000

MTU_TIMER_CONTROL (cont.)

Bits	Name	Description
11:0	SW_MTU_TIMER_UP_DOWN_CNTRL	1 bit for each timer is provided. bit 0 for timer 0, bit 1 for timer 1... This controls the up/down functionality of the timers. 1-> up, 0->down. Reset State: 0x00000000

0x3000044 MTU_BKOF_CNT_0

Type: read-write
Reset State: 0x00000003

This register contains the bkof_cnt of bkof 0. The units are slot number.In one of the modes, software can control this counter and run the back offs with this value. But this is normal way of operating In this mode, software needs to take care of the random number generation also

MTU_BKOF_CNT_0

Bits	Name	Description
15:0	BKOF_CNT_0	This register contains the bkof_counter value for the back-off 0 In the software controlled mode, (sw_mtu_use_sw_bkof_counter = 1), software will have to write this register before starting the back-off. if sw_mtu_use_sw_bkof_counter =0, hardware generates this value = (lfsr_data & sw_mtu_cw_reg) Reset State: 0x00000003

0x3000048 MTU_BKOF_CNT_1

Type: read-write
Reset State: 0x00000004

This register contains the bkof_cnt of bkof 1.In one of the modes, software can control this counter and run the back offs with this value. But this is normal way of operating In this mode, software needs to take care of the random number generation also

MTU_BKOF_CNT_1

Bits	Name	Description
15:0	BKOF_CNT_1	This register contains the bkof_counter value for the back-off 1 In the software controlled mode, (sw_mtu_use_sw_bkof_counter = 1), software will have to write this register before starting the back-off. if sw_mtu_use_sw_bkof_counter =0, hardware generates this value = (lfsr_data & sw_mtu_cw_reg) Reset State: 0x00000004

0x300004C MTU_BKOF_CNT_2

Type: read-write
Reset State: 0x00000007

This register contains the bkof_cnt of bkof 2.In one of the modes, software can control this counter and run the back offs with this value. But this is normal way of operating In this mode, software needs to take care of the random number generation also

MTU_BKOF_CNT_2

Bits	Name	Description
15:0	BKOF_CNT_2	This register contains the bkof_counter value for the back-off 2 In the software controlled mode, (sw_mtu_use_sw_bkof_counter = 1), software will have to write this register before starting the back-off. if sw_mtu_use_sw_bkof_counter =0, hardware generates this value = (lfsr_data & sw_mtu_cw_reg) Reset State: 0x00000007

0x3000050 MTU_BKOF_CNT_3

Type: read-write
Reset State: 0x00000001

This register contains the bkof_cnt of bkof 3.In one of the modes, software can control this counter and run the back offs with this value. But this is normal way of operating In this mode, software needs to take care of the random number generation also

MTU_BKOF_CNT_3

Bits	Name	Description
15:0	BKOF_CNT_3	This register contains the bkof_counter value for the back-off 4 In the software controlled mode, (sw_mtu_use_sw_bkof_counter = 1), software will have to write this register before starting the back-off. if sw_mtu_use_sw_bkof_counter =0, hardware generates this value = (lfsr_data & sw_mtu_cw_reg) Reset State: 0x00000001

0x3000054 MTU_BKOF_CNT_4

Type: read-write
Reset State: 0x00000002

This register contains the bkof_cnt of bkof 4.In one of the modes, software can control this counter and run the back offs with this value. But this is normal way of operating In this mode, software needs to take care of the random number generation also

MTU_BKOF_CNT_4

Bits	Name	Description
15:0	BKOF_CNT_4	This register contains the bkof_counter value for the back-off 4 In the software controlled mode, (sw_mtu_use_sw_bkof_counter = 1), software will have to write this register before starting the back-off. if sw_mtu_use_sw_bkof_counter =0, hardware generates this value = (lfsr_data & sw_mtu_cw_reg) Reset State: 0x00000002

0x3000058 MTU_BKOF_CNT_5

Type: read-write
Reset State: 0x00000005

This register contains the bkof_cnt of bkof 5.In one of the modes, software can control this counter and run the back offs with this value. But this is normal way of operating In this mode, software needs to take care of the random number generation also

MTU_BKOF_CNT_5

Bits	Name	Description
15:0	BKOF_CNT_5	This register contains the bkof_counter value for the back-off 5 In the software controlled mode, (sw_mtu_use_sw_bkof_counter = 1), software will have to write this register before starting the back-off. if sw_mtu_use_sw_bkof_counter =0, hardware generates this value = (lfsr_data & sw_mtu_cw_reg) Reset State: 0x00000005

0x300005C MTU_BKOF_CNT_6

Type: read-write
Reset State: 0x00000006

This register contains the bkof_cnt of bkof 6.In one of the modes, software can control this counter and run the back offs with this value. But this is normal way of operating In this mode, software needs to take care of the random number generation also

MTU_BKOF_CNT_6

Bits	Name	Description
15:0	BKOF_CNT_6	This register contains the bkof_counter value for the back-off 6 In the software controlled mode, (sw_mtu_use_sw_bkof_counter = 1), software will have to write this register before starting the back-off. if sw_mtu_use_sw_bkof_counter =0, hardware generates this value = (lfsr_data & sw_mtu_cw_reg) Reset State: 0x00000006

0x3000060 MTU_BKOF_CNT_7

Type: read-write
Reset State: 0x00000000

This register contains the bkof_cnt of bkof 7.In one of the modes, software can control this counter and run the back offs with this value. But this is normal way of operating In this mode, software needs to take care of the random number generation also

MTU_BKOF_CNT_7

Bits	Name	Description
15:0	BKOF_CNT_7	This register contains the bkof_counter value for the back-off 7 In the software controlled mode, (sw_mtu_use_sw_bkof_counter = 1), software will have to write this register before starting the back-off. if sw_mtu_use_sw_bkof_counter =0, hardware generates this value = (lfsr_data & sw_mtu_cw_reg) Reset State: 0x00000000

0x3000064 MTU_BKOF_CONTROL

Type: read-write
Reset State: 0xFF000000

This register contains all the controls for the back-off engines.

MTU_BKOF_CONTROL

Bits	Name	Description
31:24	SW_MTU_SUPPRESS_COLLISION_INT	1 bit for each back off is provided. bit 0 for back 0, bit 1 for back 1... this bit is set to 1, the back off will not send interrupt to software for collision case (int status = 2'b11) warm up also will not be generated Reset State: 0x000000FF
23:16	SW_MTU_QUEUE_DATA_AVAIL	1 bit for each back is provided. bit 0 for back 0, bit 1 for back 1... data avail bits from the software. Unless this bit is set, software won't get interrupt (irrespective of the status of back-off. Reset State: 0x00000000
15:8	SW_MTU_STALL_BKOF	1 bit for each back is provided. bit 0 for back 0, bit 1 for back 1... if this bit is set, the corresponding back-off will be stalled. Basically the back-off counter -- will be stopped. This is used to stall all the back-offs while beacon is supposed to be sent or for any other reasons. Reset State: 0x00000000
7:0	SW_MTU_USE_SW_BKOF_COUNTER	1 bit for each back is provided. bit 0 for back 0, bit 1 for back 1... if this bit is set, the back_off counter is set by sw. Otherwise, hardware will use the cw_reg &lfsdr Reset State: 0x00000000

0x3000068 MTU_CW_REG_CONTROL_FOR_BACKOFF_0

Type: read-write
Reset State: 0x00000007

This register contains the cw_reg value that needs to be used by hardware . For backoff engine_0 This register also has the control bit that initiates the back-off after the hardware issued an interrupt to software for its attention.

MTU_CW_REG_CONTROL_FOR_BACKOFF_0

Bits	Name	Description
19	SW_MTU_CW_UPDATE_VALID	this is write only register The sw_mtu_cw_reg will be updated only when this bit is set. Otherwise the hardware update will take place Reset State: 0x00000000
18:17	SW_MTU_CW_ACTION_0	This field indicates the action that bkoff-engine need to do to the cw_reg. 00-> no change, 01-> reset cw (cw_reg=cw_min), 10-> ++cw, hardware does the boundary checks and resets the cw if it reaches the cw_max automatically Reset State: 0x00000000
16	SW_MTU_WAIT_DONE_P_0	This bit is write only. The hardware will be waiting for this signal to start the next back-off after issuing the interrupt by the back-off engine Reset State: 0x00000000
15:0	SW_MTU_CW_REG_0	This register contains the cw_reg value for the back-off 0 Reset State: 0x00000007

0x300006C MTU_CW_REG_CONTROL_FOR_BACKOFF_1

Type: read-write
Reset State: 0x00000007

This register contains the cw_reg value that needs to be used by hardware . For backoff engine_1 This register also has the control bit that initiates the back-off after the hardware issued an interrupt to software for its attention.

MTU_CW_REG_CONTROL_FOR_BACKOFF_1

Bits	Name	Description
19	SW_MTU_CW_UPDATE_VALID	this is write only register The sw_mtu_cw_reg will be updated only when this bit is set. Otherwise the hardware update will take place Reset State: 0x00000000

MTU_CW_REG_CONTROL_FOR_BACKOFF_1 (cont.)

Bits	Name	Description
18:17	SW_MTU_CW_ACTION_1	This field indicates the action that bkoff-engine need to do to the cw_reg. 00-> no change, 01-> reset cw (cw_reg=cw_min), 10-> ++cw, hardware does the boundary checks and resets the cw if it reaches the cw_max automatically Reset State: 0x00000000
16	SW_MTU_WAIT_DONE_P_1	This bit is write only. The hardware will be waiting for this signal to start the next back-off after issuing the interrupt by the back-off engine Reset State: 0x00000000
15:0	SW_MTU_CW_REG_1	This register contains the cw_reg value for the back-off 1 Reset State: 0x00000007

0x3000070 MTU_CW_REG_CONTROL_FOR_BACKOFF_2

Type: read-write
Reset State: 0x00000007

This register contains the cw_reg value that needs to be used by hardware . For backoff engine_2 This register also has the control bit that initiates the back-off after the hardware issued an interrupt to software for its attention.

MTU_CW_REG_CONTROL_FOR_BACKOFF_2

Bits	Name	Description
19	SW_MTU_CW_UPDATE_VALID	this is write only register The sw_mtu_cw_reg will be updated only when this bit is set. Otherwise the hardware update will take place Reset State: 0x00000000
18:17	SW_MTU_CW_ACTION_2	This field indicates the action that bkoff-engine need to do to the cw_reg. 00-> no change, 01-> reset cw (cw_reg=cw_min), 10-> ++cw, hardware does the boundary checks and resets the cw if it reaches the cw_max automatically Reset State: 0x00000000
16	SW_MTU_WAIT_DONE_P_2	This bit is write only. The hardware will be waiting for this signal to start the next back-off after issuing the interrupt by the back-off engine Reset State: 0x00000000
15:0	SW_MTU_CW_REG_2	This register contains the cw_reg value for the back-off 2 Reset State: 0x00000007

0x3000074 MTU_CW_REG_CONTROL_FOR_BACKOFF_3

Type: read-write
Reset State: 0x00000007

This register contains the cw_reg value that needs to be used by hardware . For backoff engine_3 This register also has the control bit that initiates the back-off after the hardware issued an interrupt to software for its attention.

MTU_CW_REG_CONTROL_FOR_BACKOFF_3

Bits	Name	Description
19	SW_MTU_CW_UPDATE_VALID	this is write only register The sw_mtu_cw_reg will be updated only when this bit is set. Otherwise the hardware update will take place Reset State: 0x00000000
18:17	SW_MTU_CW_ACTION_3	This field indicates the action that bkoff-engine need to do to the cw_reg. 00-> no change, 01-> reset cw (cw_reg=cw_min), 10-> ++cw, hardware does the boundary checks and resets the cw if it reaches the cw_max automatically Reset State: 0x00000000
16	SW_MTU_WAIT_DONE_P_3	This bit is write only. The hardware will be waiting for this signal to start the next back-off after issuing the interrupt by the back-off engine Reset State: 0x00000000
15:0	SW_MTU_CW_REG_3	This register contains the cw_reg value for the back-off 3 Reset State: 0x00000007

0x3000078 MTU_CW_REG_CONTROL_FOR_BACKOFF_4

Type: read-write
Reset State: 0x00000007

This register contains the cw_reg value that needs to be used by hardware. For backoff engine_4 This register also has the control bit that initiates the back-off after the hardware issued an interrupt to software for its attention.

MTU_CW_REG_CONTROL_FOR_BACKOFF_4

Bits	Name	Description
19	SW_MTU_CW_UPDATE_VALID	this is write only register The sw_mtu_cw_reg will be updated only when this bit is set. Otherwise the hardware update will take place Reset State: 0x00000000

MTU_CW_REG_CONTROL_FOR_BACKOFF_4 (cont.)

Bits	Name	Description
18:17	SW_MTU_CW_ACTION_4	This field indicates the action that bkoff-engine need to do to the cw_reg. 00-> no change, 01-> reset cw (cw_reg=cw_min), 10-> ++cw, hardware does the boundary checks and resets the cw if it reaches the cw_max automatically Reset State: 0x00000000
16	SW_MTU_WAIT_DONE_P_4	This bit is write only. The hardware will be waiting for this signal to start the next back-off after issuing the interrupt by the back-off engine Reset State: 0x00000000
15:0	SW_MTU_CW_REG_4	This register contains the cw_reg value for the back-off 4 Reset State: 0x00000007

0x300007C MTU_CW_REG_CONTROL_FOR_BACKOFF_5

Type: read-write
Reset State: 0x00000007

This register contains the cw_reg value that needs to be used by hardware . For backoff engine_5 This register also has the control bit that initiates the back-off after the hardware issued an interrupt to software for its attention.

MTU_CW_REG_CONTROL_FOR_BACKOFF_5

Bits	Name	Description
19	SW_MTU_CW_UPDATE_VALID	this is write only register The sw_mtu_cw_reg will be updated only when this bit is set. Otherwise the hardware update will take place Reset State: 0x00000000
18:17	SW_MTU_CW_ACTION_5	This field indicates the action that bkoff-engine need to do to the cw_reg. 00-> no change, 01-> reset cw (cw_reg=cw_min), 10-> ++cw, hardware does the boundary checks and resets the cw if it reaches the cw_max automatically Reset State: 0x00000000
16	SW_MTU_WAIT_DONE_P_5	This bit is write only. The hardware will be waiting for this signal to start the next back-off after issuing the interrupt by the back-off engine Reset State: 0x00000000
15:0	SW_MTU_CW_REG_5	This register contains the cw_reg value for the back-off 5 Reset State: 0x00000007

0x3000080 MTU_CW_REG_CONTROL_FOR_BACKOFF_6

Type: read-write
Reset State: 0x00000007

This register contains the cw_reg value that needs to be used by hardware . For backoff engine_6 This register also has the control bit that initiates the back-off after the hardware issued an interrupt to software for its attention.

MTU_CW_REG_CONTROL_FOR_BACKOFF_6

Bits	Name	Description
19	SW_MTU_CW_UPDATE_VALID	this is write only register The sw_mtu_cw_reg will be updated only when this bit is set. Otherwise the hardware update will take place Reset State: 0x00000000
18:17	SW_MTU_CW_ACTION_6	This field indicates the action that bkoff-engine need to do to the cw_reg. 00-> no change, 01-> reset cw (cw_reg=cw_min), 10-> ++cw, hardware does the boundary checks and resets the cw if it reaches the cw_max automatically Reset State: 0x00000000
16	SW_MTU_WAIT_DONE_P_6	This bit is write only. The hardware will be waiting for this signal to start the next back-off after issuing the interrupt by the back-off engine Reset State: 0x00000000
15:0	SW_MTU_CW_REG_6	This register contains the cw_reg value for the back-off 6 Reset State: 0x00000007

0x3000084 MTU_CW_REG_CONTROL_FOR_BACKOFF_7

Type: read-write
Reset State: 0x00000007

This register contains the cw_reg value that needs to be used by hardware . For backoff engine_7 This register also has the control bit that initiates the back-off after the hardware issued an interrupt to software for its attention.

MTU_CW_REG_CONTROL_FOR_BACKOFF_7

Bits	Name	Description
19	SW_MTU_CW_UPDATE_VALID	this is write only register The sw_mtu_cw_reg will be updated only when this bit is set. Otherwise the hardware update will take place Reset State: 0x00000000

MTU_CW_REG_CONTROL_FOR_BACKOFF_7 (cont.)

Bits	Name	Description
18:17	SW_MTU_CW_ACTION_7	This field indicates the action that bkoff-engine need to do to the cw_reg. 00-> no change, 01-> reset cw (cw_reg=cw_min), 10-> ++cw, hardware does the boundary checks and resets the cw if it reaches the cw_max automatically Reset State: 0x00000000
16	SW_MTU_WAIT_DONE_P_7	This bit is write only. The hardware will be waiting for this signal to start the next back-off after issuing the interrupt by the back-off engine Reset State: 0x00000000
15:0	SW_MTU_CW_REG_7	This register contains the cw_reg value for the back-off 7 Reset State: 0x00000007

0x3000088 MTU_MTU_INTERRUPT_STATUS

Type: read-write
Reset State: 0x00000000

This register contains the status of all the interrupts that are generated by mtu. Basically every interrupt has a corresponding register bit which will be set on sending interrupt pulse to the interrupt module and this bit is reset by writing '1' to it. software has higher priority over hardware

MTU_MTU_INTERRUPT_STATUS

Bits	Name	Description
31	SECONDARY_CCA_TO	the secondary_cca_to is sampled and software can read its status through this register Reset State: 0x00000000
30	SIFS_TO	the sifs_to is sampled and software can read its status through this register Reset State: 0x00000000
29	PIFS_TO	the pifs_to is sampled and software can read its status through this register Reset State: 0x00000000
28	MTU_MCU_WATCH_DOG_ENABLE_DISABL_ERROR	if software tries to write wrong combinations to the watch dog enable disable bits this interrupt will be generated Reset State: 0x00000000
27	MTU_MCU_WATCH_DOG_PROTECTION_ERROR	if software tries to write to the watch dog register and if the protection vector matches, this interrupt will be generated. Reset State: 0x00000000
26:24	MTU_MCU_WATCH_DOG_TIMER_FLAG	watch dog interrupt flags. 24 is for thr0, bit 25 is for thr1, bit 26 is fr thr3 Reset State: 0x00000000

MTU_MTU_INTERRUPT_STATUS (cont.)

Bits	Name	Description
23:16	MTU_MCU_TSF_INT_FLAG	8 registers for 8 tsf based match register interrupts. bit 0 for match 0, 1 for match 1 ... Reset State: 0x00000000
15:8	MTU_MCU_BKOF_INT_FLAG	8 registers for 8 back off interrupts. bit 0 for timer 0, 1 for timer 1 ... Reset State: 0x00000000
7:0	MTU_MCU_TIMER_INT_FLAG	8 registers for 8 timer interrupts. bit 0 for timer 0, 1 for timer 1 ... Reset State: 0x00000000

0x300008C MTU_SW_MATCH_REGISTER_0

Type: read-write
Reset State: 0x00000EFF

This register contains the match value for tsf based interrupts. Basically whenever the tsf is equal to this register, corresponding interrupt will be generated. This register is also used the timer 0 in up mode. Basically when the timer is operated in up mode, when the Timer 0 reaches this value, an interrupt is generated

MTU_SW_MATCH_REGISTER_0

Bits	Name	Description
31:30	SW_TSF_SEL_0	To select the tsf will trigger the interrupt when the timer value reaches 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
23:0	SW_MATCH_REGISTER_0	This register contains the match value for tsf based counter interrupt 0, timer 0 (in up mode) Reset State: 0x00000EFF

0x3000090 MTU_SW_MATCH_REGISTER_1

Type: read-write
Reset State: 0x00000EFF

This register contains the match value for tsf based interrupts. Basically whenever the tsf is equal to this register, corresponding interrupt will be generated. This register is also used the timer 1 in up mode. Basically when the timer is operated in up mode, when the Timer 1 reaches this value, an interrupt is generated

MTU_SW_MATCH_REGISTER_1

Bits	Name	Description
31:30	SW_TSF_SEL_1	To select the tsf will trigger the interrupt when the timer value reaches 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
23:0	SW_MATCH_REGISTER_1	This register contains the match value for tsf based counter interrupt 1, timer 1 (in up mode) Reset State: 0x00000EFF

0x3000094 MTU_SW_MATCH_REGISTER_2

Type: read-write
Reset State: 0x00000EFF

This register contains the match value for tsf based interrupts. Basically whenever the tsf is equal to this register, corresponding interrupt will be generated. This register is also used the timer 2 in up mode. Basically when the timer is operated in up mode, when the Timer 2 reaches this value, an interrupt is generated

MTU_SW_MATCH_REGISTER_2

Bits	Name	Description
31:30	SW_TSF_SEL_2	To select the tsf will trigger the interrupt when the timer value reaches 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
23:0	SW_MATCH_REGISTER_2	This register contains the match value for tsf based counter interrupt 2, timer 2 (in up mode) Reset State: 0x00000EFF

0x3000098 MTU_SW_MATCH_REGISTER_3

Type: read-write
Reset State: 0x00000EFF

This register contains the match value for tsf based interrupts. Basically whenever the tsf is equal to this register, corresponding interrupt will be generated. This register is also used the timer 3 in up mode. Basically when the timer is operated in up mode, when the Timer 3 reaches this value, an interrupt is generated

MTU_SW_MATCH_REGISTER_3

Bits	Name	Description
31:30	SW_TSF_SEL_3	To select the tsf will trigger the interrupt when the timer value reaches 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
23:0	SW_MATCH_REGISTER_3	This register contains the match value for tsf based counter interrupt 3, timer 3 (in up mode) Reset State: 0x00000EFF

0x300009C MTU_SW_MATCH_REGISTER_4

Type: read-write
Reset State: 0x00000EFF

This register contains the match value for tsf based interrupts. Basically whenever the tsf is equal to this register, corresponding interrupt will be generated. This register is also used the timer 4 in up mode. Basically when the timer is operated in up mode, when the Timer 4 reaches this value, an interrupt is generated

MTU_SW_MATCH_REGISTER_4

Bits	Name	Description
31:30	SW_TSF_SEL_4	To select the tsf will trigger the interrupt when the timer value reaches 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
23:0	SW_MATCH_REGISTER_4	This register contains the match value for tsf based counter interrupt 4, timer 4 (in up mode) Reset State: 0x00000EFF

0x30000A0 MTU_SW_MATCH_REGISTER_5

Type: read-write
Reset State: 0x00000EFF

This register contains the match value for tsf based interrupts. Basically whenever the tsf is equal to this register, corresponding interrupt will be generated. This register is also used the timer 5 in up mode. Basically when the timer is operated in up mode, when the Timer 5 reaches this value, an interrupt is generated

MTU_SW_MATCH_REGISTER_5

Bits	Name	Description
31:30	SW_TSF_SEL_5	To select the tsf will trigger the interrupt when the timer value reaches 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
23:0	SW_MATCH_REGISTER_5	This register contains the match value for tsf based counter interrupt 5, timer 5 (in up mode) Reset State: 0x00000EFF

0x30000A4 MTU_SW_MATCH_REGISTER_6

Type: read-write
Reset State: 0x00000EFF

This register contains the match value for tsf based interrupts. Basically whenever the tsf is equal to this register, corresponding interrupt will be generated. This register is also used the timer 6 in up mode. Basically when the timer is operated in up mode, when the Timer 6 reaches this value, an interrupt is generated

MTU_SW_MATCH_REGISTER_6

Bits	Name	Description
31:30	SW_TSF_SEL_6	To select the tsf will trigger the interrupt when the timer value reaches 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
23:0	SW_MATCH_REGISTER_6	This register contains the match value for tsf based counter interrupt 6, timer 6 (in up mode) Reset State: 0x00000EFF

0x30000A8 MTU_SW_MATCH_REGISTER_7

Type: read-write
Reset State: 0x00000EFF

This register contains the match value for tsf based interrupts. Basically whenever the tsf is equal to this register, corresponding interrupt will be generated. This register is also used the timer 7 in up mode. Basically when the timer is operated in up mode, when the Timer 7 reaches this value, an interrupt is generated

MTU_SW_MATCH_REGISTER_7

Bits	Name	Description
31:30	SW_TSF_SEL_7	To select the tsf will trigger the interrupt when the timer value reaches 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
23:0	SW_MATCH_REGISTER_7	This register contains the match value for tsf based counter interrupt 7, timer 7 (in up mode) Reset State: 0x00000EFF

0x30000AC MTU_SW_CW_MIN_CW_MAX_0

Type: read-write
Reset State: 0x03FF000F

Contains the cw_min and cw_max for back-off 0

MTU_SW_CW_MIN_CW_MAX_0

Bits	Name	Description
31:16	SW_CW_MAX_0	This register contains the cw_max for back-off 0. The default is 7ff. Any suggested value is welcome Reset State: 0x000003FF
15:0	SW_CW_MIN_0	This register contains the cw_min for back-off 0. The default is 3f. Any suggested value is welcome Reset State: 0x0000000F

0x30000B0 MTU_SW_CW_MIN_CW_MAX_1

Type: read-write
Reset State: 0x03FF000F

Contains the cw_min and cw_max for back-off 1

MTU_SW_CW_MIN_CW_MAX_1

Bits	Name	Description
31:16	SW_CW_MAX_1	This register contains the cw_max for back-off 1. The default is 7ff. Any suggested value is welcome Reset State: 0x000003FF
15:0	SW_CW_MIN_1	This register contains the cw_min for back-off 1. The default is 3f. Any suggested value is welcome Reset State: 0x0000000F

0x30000B4 MTU_SW_CW_MIN_CW_MAX_2

Type: read-write
Reset State: 0x00070003

Contains the cw_min and cw_max for back-off 2

MTU_SW_CW_MIN_CW_MAX_2

Bits	Name	Description
31:16	SW_CW_MAX_2	This register contains the cw_max for back-off 2. The default is 7ff. Any suggested value is welcome Reset State: 0x00000007
15:0	SW_CW_MIN_2	This register contains the cw_min for back-off 2. The default is 3f. Any suggested value is welcome Reset State: 0x00000003

0x30000B8 MTU_SW_CW_MIN_CW_MAX_3

Type: read-write
Reset State: 0x00070003

Contains the cw_min and cw_max for back-off 3

MTU_SW_CW_MIN_CW_MAX_3

Bits	Name	Description
31:16	SW_CW_MAX_3	This register contains the cw_max for back-off 3. The default is 7ff. Any suggested value is welcome Reset State: 0x00000007
15:0	SW_CW_MIN_3	This register contains the cw_min for back-off 3. The default is 3f. Any suggested value is welcome Reset State: 0x00000003

0x30000BC MTU_SW_CW_MIN_CW_MAX_4

Type: read-write
Reset State: 0x00070003

Contains the cw_min and cw_max for back-off 4

MTU_SW_CW_MIN_CW_MAX_4

Bits	Name	Description
31:16	SW_CW_MAX_4	This register contains the cw_max for back-off 4. The default is 7ff. Any suggested value is welcome Reset State: 0x00000007
15:0	SW_CW_MIN_4	This register contains the cw_min for back-off 4. The default is 3f. Any suggested value is welcome Reset State: 0x00000003

0x30000C0 MTU_SW_CW_MIN_CW_MAX_5

Type: read-write
Reset State: 0x000F0007

Contains the cw_min and cw_max for back-off 5

MTU_SW_CW_MIN_CW_MAX_5

Bits	Name	Description
31:16	SW_CW_MAX_5	This register contains the cw_max for back-off 5. The default is 7ff. Any suggested value is welcome Reset State: 0x0000000F
15:0	SW_CW_MIN_5	This register contains the cw_min for back-off 5. The default is 3f. Any suggested value is welcome Reset State: 0x00000007

0x30000C4 MTU_SW_CW_MIN_CW_MAX_6

Type: read-write
Reset State: 0x03FF000F

Contains the cw_min and cw_max for back-off 6

MTU_SW_CW_MIN_CW_MAX_6

Bits	Name	Description
31:16	SW_CW_MAX_6	This register contains the cw_max for back-off 6. The default is 7ff. Any suggested value is welcome Reset State: 0x000003FF
15:0	SW_CW_MIN_6	This register contains the cw_min for back-off 6. The default is 3f. Any suggested value is welcome Reset State: 0x0000000F

0x30000C8 MTU_SW_CW_MIN_CW_MAX_7

Type: read-write
Reset State: 0x03FF000F

Contains the cw_min and cw_max for back-off 7

MTU_SW_CW_MIN_CW_MAX_7

Bits	Name	Description
31:16	SW_CW_MAX_7	This register contains the cw_max for back-off 7. The default is 7ff. Any suggested value is welcome Reset State: 0x000003FF
15:0	SW_CW_MIN_7	This register contains the cw_min for back-off 7. The default is 3f. Any suggested value is welcome Reset State: 0x0000000F

0x30000CC MTU_CCA_COUNTER0

Type: read-write
Reset State: 0x00000000

This register contains the primary cca count. The primary cca is sampled at every us and incremented if the cca is LOW.

MTU_CCA_COUNTER0

Bits	Name	Description
31:0	CCA_COUNTER0	contains the cca primary counter. Software write has higher priority over hardware update Reset State: 0x00000000

0x30000D0 MTU_CCA_COUNTER1

Type: read-write
Reset State: 0x00000000

This register contains the cca count. The selection to the cca used by this counter is programmable.

MTU_CCA_COUNTER1

Bits	Name	Description
31:0	CCA_COUNTER1	Depending on the cca_count1_sel-- a programmable bit, the enable to this counter is selected as shown below. Software write has higher priority over hardware update cca_term0 =

0x30000D4 MTU_CCA_COUNTER2

Type: read-write
Reset State: 0x00000000

This register contains the cca count. The selection to the cca used by this counter is programmable.

MTU_CCA_COUNTER2

Bits	Name	Description
31:0	CCA_COUNTER2	Depending on the cca_count2_sel-- a programmable bit, the enable to this counter is selected as shown below. Software write has higher priority over hardware update 3'b000: cca_count2_en_temp =

0x30000D8 MTU_WATCH_DOG_TIMER

Type: read-write
Reset State: 0x00000000

This is watch dog timer register. Basically, when the watch dog timer is enabled, this timer keeps ++ at every us. Once it reaches watch dog thr0, an interrupt is generated when it reaches thr1 another interrupt is generated (higher priority). On reaching thr3, another higher priority interrupt is generated. Typically this is used to reset the chip.

MTU_WATCH_DOG_TIMER

Bits	Name	Description
31:30	WATCH_DOG_TIMER_ENABLE_DISABLE	Watch dog timer and the corresponding interrupts are enabled only when these bits are 10. 01 is disable. Any other combination will not be accepted and if software writes 00 or 11, the status is maintained. We may have an interrupt to this condition as well as for any writes to the watch dog register without protection vector match. Reset State: 0x00000000
29:24	WATCH_DOG_TIMER_PROTECTION_VECTOR	This is write-only register. When it is read, ZEROs are returned. Writes to the watch dog register can happen (including the enable/disable) only when this field matches the watch_dog_thr0[25:24],thr1[25:24],thr2[25:24]. Reset State: 0x00000000
23:0	WATCH_DOG_TIMER	if it is enabled, it keeps ++ at every us. Software can write to it only when the protection vector matches the concat of the 2-bit protection bits from the watch dog threshold register. The protection vector cannot be 00 or 3f. Reset State: 0x00000000

0x30000DC MTU_WATCH_DOG_THR0

Type: read-write
Reset State: 0x00000000

This register contains thr0 for watch dog.

MTU_WATCH_DOG_THR0

Bits	Name	Description
27:26	THR0_PROTECTION_FIELD	This register is writable only when this field is 11. Reset State: 0x00000000
25:24	WATCH_DOG_PROTECTION_VECTOR0	2 bits of the protection vector of watch_dog_timer. Reset State: 0x00000000
23:0	WATCH_DOG_THR0	Contains the watch dog thr0. It is writable by software only when its protection field =11. Reset State: 0x00000000

0x30000E0 MTU_WATCH_DOG_THR1

Type: read-write
Reset State: 0x00000000

This register contains thr1 for watch dog.

MTU_WATCH_DOG_THR1

Bits	Name	Description
27:26	THR1_PROTECTION_FIELD	This register is writable only when this field is 10. Reset State: 0x00000000
25:24	WATCH_DOG_PROTECTION_VECTOR1	2 bits of the protection vector of watch_dog_timer. Reset State: 0x00000000
23:0	WATCH_DOG_THR1	Contains the watch dog thr1. It is writable by software only when its protection field =10. Reset State: 0x00000000

0x30000E4 MTU_WATCH_DOG_THR2

Type: read-write
Reset State: 0x00000000

This register contains thr2 for watch dog.

MTU_WATCH_DOG_THR2

Bits	Name	Description
27:26	THR2_PROTECTION_FIELD	This register is writable only when this field is 01 Reset State: 0x00000000
25:24	WATCH_DOG_PROTECTION_VECTOR2	2 bits of the protection vector of watch_dog_timer Reset State: 0x00000000
23:0	WATCH_DOG_THR2	Contains the watch dog thr2. It is writable by software only when its protection field =01 Reset State: 0x00000000

0x30000E8 MTU_BKOF_SW_INT_TYPE

Type: read-write
Reset State: 0x00000000

This register contains the status of the interrupt type for the back off engines.

MTU_BKOF_SW_INT_TYPE

Bits	Name	Description
15:0	BKOF_SW_INT_TYPE	Contains the type of the interrupt rom the back off engines. 1:0 is bkoff 0, 3:2 for bkoff 1 and so on. Value 2'b00: No interrupt pending, or cleared by software Value 2'b01: Backoff engine expired successfully (no collision with a higher priority backoff engine) Value 2'b10: There was in internal collision between this and a higher priority backoff engine. software needs to re-initialize the backoff engine. Value 2'b11: Data available got programmed after the backoff engine had already run and reached the BKOFF_DONE state. At the moment of programming Data available, the CCA was low. software needs to re-program the backoff engine. This is read-only register. But any write 1 to this register will clear the status for the corresponding back-off. For example, write of a 1 to bit 0 will clear 1:0, write of a 1 to bit 1 clears the 3:2 and so on. Only 11:0 are enabled for write operation, but will also automatically clear on a write. Corresponds to reset_bkof_sw_int_type_p in RTL Reset State: 0x00000000

0x30000EC MTU_CCA_CONTROL_REG

Type: read-write
Reset State: 0x00000000

This register contains the controls to select the cca that needs to be used for a particular back_off engine.

MTU_CCA_CONTROL_REG

Bits	Name	Description
31	SW_MTU_BKOF_GOTO_IDLE	If the back-offs are stuck for some reason, this bit will take the back-offs to idle We see a hang in the lab on a netlist that has no test buses, but it could not be reproduced. To be on safe side, this bit is added. Reset State: 0x00000000
30	SW_MTU_PIFS_RAW_CCA_SEL_NEW	Work with bit[25:24] to select the cca to be used for pifs. Reset State: 0x00000000
29	SW_MTU_CCA_FLAG	This is software controlled cca. If the sw_mtu_sel is 11, the corresponding back off engine uses this register bit as its cca. Reset State: 0x00000000
28:26	SW_MTU_PIFS_FINAL_CCA_SEL	We want to follow the same strategy we followed for back-off cca. Since the last_slot_time doesn't make sense for pifs, we kept the last_slot_time corresponds to back-off 0 000 -- raw CCA 001 -- (raw CCA && early_pktdet_n) 010 -- (raw CCA && pktdet_n) 011 -- early_pktdet_n 100 -- pktdet_n 101 -- (raw CCA && (early_pktdet_n ||
25:24	SW_MTU_PIFS_RAW_CCA_SEL	It was not clear which cca to be used for pifs. So a programmability is provided for this also. If bit[30] = 0, 00 selects primarcy cca, 01 selects secondary cca, 10 selects combined cca(basically and of both primary and secondary) 11 select the sw_mtu_cca_flag which is software config register bit. if bit[30] = 1, 00 selects tertiary cca, 01 selects quaternary cca, 10 selects all cca (basically and of primary, secondary, tertiary and quaternary) Final cca selection is done based on the next 3 bits-- sw_mtu_pifs_final_cca_sel Reset State: 0x00000000
23:16	SW_MTU_EIFS_CCA_SEL	1 bit for each back off. It was not clear which ccacto use for eifs. So a programmability is provided such that either the same cca that is used for difs is used for eifs also or just primary cca is selected. If this bit is 0, the primary cca is used for eifs (for the corresponding back off). Otherwise the cca that is used for the back off is used for eifs also. Reset State: 0x00000000
15:0	SW_MTU_RAW_CCA_SEL	2 bits for each back off. 1:0 for back off 0, 3:2 back off 1, and so on, if the corresponding mtu_cca_control.sw_mtu_raw_cca_sel=0, 00 selects primarcy cca, 01 selects secondary cca, 10 selects combined cca (basically and of both primary and secondary) 11 selects the sw_mtu_cca_flag, which is software config register bit, if the corresponding mtu_cca_control.sw_mtu_raw_cca_sel=1, 00 selects tertiary cca, 01 selects quaternary cca, 10 selects all cca(basically and of primary, secondary, tertiary and quaternary) Reset State: 0x00000000

0x30000F0 MTU_TIMER_8

Type: read-write
Reset State: 0x00EFFFFF

This register contains the timer 8 value. This timer is rd/writable,up/down Based on the configuration, this can be used either for up or down counter and generates an interrup on reaching Zero in down mode. in up mode interrupt is generated when the timer reaches the sw_match_register_8.

MTU_TIMER_8

Bits	Name	Description
23:0	TIMER_8	This register contains the timer 8 value. This timer is rd/writable,up/down Reset State: 0x00EFFFFF

0x30000F4 MTU_TIMER_9

Type: read-write
Reset State: 0x00EFFFFF

This register contains the timer 9 value. This timer is rd/writable,up/down Based on the configuration, this can be used either for up or down counter and generates an interrup on reaching Zero in down mode. in up mode interrupt is generated when the timer reaches the sw_match_register_9.

MTU_TIMER_9

Bits	Name	Description
23:0	TIMER_9	This register contains the timer 9 value. This timer is rd/writable,up/down Reset State: 0x00EFFFFF

0x30000F8 MTU_TIMER_10

Type: read-write
Reset State: 0x00EFFFFF

This register contains the timer c value. This timer is rd/writable,up/down Based on the configuration, this can be used either for up or down counter and generates an interrup on reaching Zero in down mode. in up mode interrupt is generated when the timer reaches the sw_match_register_10.

MTU_TIMER_10

Bits	Name	Description
23:0	TIMER_10	This register contains the timer 10 value. This timer is rd/writable,up/down Reset State: 0x00EFFFFF

0x30000FC MTU_TIMER_11

Type: read-write
Reset State: 0x00EFFFFF

This register contains the timer 11 value. This timer is rd/writable,up/down Based on the configuration, this can be used either for up or down counter and generates an interrup on reaching Zero in down mode. in up mode interrupt is generated when the timer reaches the sw_match_register_11.

MTU_TIMER_11

Bits	Name	Description
23:0	TIMER_11	This register contains the timer 11 value. This timer is rd/writable,up/down Reset State: 0x00EFFFFF

0x3000110 MTU_SW_MATCH_REGISTER_8

Type: read-write
Reset State: 0x00000EFF

This register contains the match value for tsf based interrupts. Basically whenever the tsf is equal to this register, corresponding interrupt will be generated. This register is also used the timer 8 in up mode. Basically when the timer is operated in up mode, when the Timer 8 reaches this value, an interrupt is generated

MTU_SW_MATCH_REGISTER_8

Bits	Name	Description
31:30	SW_TSF_SEL_8	To select the tsf will trigger the interrupt when the timer value reaches 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
23:0	SW_MATCH_REGISTER_8	This register contains the match value for tsf based counter interrupt 8, timer 8 (in up mode) Reset State: 0x00000EFF

0x3000114 MTU_SW_MATCH_REGISTER_9

Type: read-write
Reset State: 0x00000EFF

This register contains the match value for tsf based interrupts. Basically whenever the tsf is equal to this register, corresponding interrupt will be generated. This register is also used the timer 9 in up mode. Basically when the timer is operated in up mode, when the Timer 9 reaches this value, an interrupt is generated

MTU_SW_MATCH_REGISTER_9

Bits	Name	Description
31:30	SW_TSF_SEL_9	To select the tsf will trigger the interrupt when the timer value reaches 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
23:0	SW_MATCH_REGISTER_9	This register contains the match value for tsf based counter interrupt 9, timer 9 (in up mode) Reset State: 0x00000EFF

0x3000118 MTU_SW_MATCH_REGISTER_10

Type: read-write
Reset State: 0x00000EFF

This register contains the match value for tsf based interrupts. Basically whenever the tsf is equal to this register, corresponding interrupt will be generated. This register is also used the timer 10 in up mode. Basically when the timer is operated in up mode, when the Timer 10 reaches this value, an interrupt is generated

MTU_SW_MATCH_REGISTER_10

Bits	Name	Description
31:30	SW_TSF_SEL_10	To select the tsf will trigger the interrupt when the timer value reaches 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
23:0	SW_MATCH_REGISTER_10	This register contains the match value for tsf based counter interrupt 10, timer 10 (in up mode) Reset State: 0x00000EFF

0x300011C MTU_SW_MATCH_REGISTER_11

Type: read-write
Reset State: 0x00000EFF

This register contains the match value for tsf based interrupts. Basically whenever the tsf is equal to this register, corresponding interrupt will be generated. This register is also used the timer 11 in up mode. Basically when the timer is operated in up mode, when the Timer 11 reaches this value, an interrupt is generated

MTU_SW_MATCH_REGISTER_11

Bits	Name	Description
31:30	SW_TSF_SEL_11	To select the tsf will trigger the interrupt when the timer value reaches 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
23:0	SW_MATCH_REGISTER_11	This register contains the match value for tsf based counter interrupt 11, timer 11 (in up mode) Reset State: 0x00000EFF

0x3000134 MTU_BKOF_CONTROL2

Type: read-write
Reset State: 0x000E0000

This register contains all the controls for the back-off engines.

MTU_BKOF_CONTROL2

Bits	Name	Description
31	SW_MTU_CONSIDER_CSI_BKOF_EN	When set, csi bkof enable signal from MTU for hardware controlled sending CSI frame in calibration and delayed explicit beamform will be enabled Reset State: 0x00000000
30	SW_MTU_CONSIDER_QOSNULL_BKOF_EN	When set, qosnull bkof enable signal from MTU for hardware controlled sending qosnull frame in implicit beamform will be enabled Reset State: 0x00000000
19:16	SW_MTU_PKT_DET_TO_CNT_THR	pkt_det_to_cnt is compared with this register and generates a signal. This is used by tpe to start requesting BA. Basically allow tpe to get the bitmap updated. Reset State: 0x0000000E

0x3000138 MTU_CCA_CONTROL_REG2

Type: read-write
Reset State: 0x00000000

This register contains the controls to select the cca that needs to be used for a particular back_off engine.

MTU_CCA_CONTROL_REG2

Bits	Name	Description
19	CONSIDER_RX_CCA_ONLY	since the cca will be asserted even for the tx, we may want to ave count of only rx busy if this bit is set, the cca counters will be ++ only if txp_mtu_phytx_idle txp_mtu_phytx_idle =1 Reset State: 0x00000000
18:16	CCA_COUNT2_SEL	these bits select the count enable to the cca_count2 3'b000: cca_count2_en_temp = cca_term0; 3'b001: cca_count2_en_temp = cca_term1; 3'b010: cca_count2_en_temp = cca_term2; 3'b011: cca_count2_en_temp = cca_term3; 3'b100: cca_count2_en_temp = cca_term4; 3'b101: cca_count2_en_temp = cca_term5; 3'b110: cca_count2_en_temp = cca_term6; 3'b111: cca_count2_en_temp = cca_term7; cca_count2_en_final = consider_rx_cca_only ? (cca_count2_en_temp &
14:12	CCA_COUNT1_SEL	these bits select the count enable to the cca_count1 3'b000: cca_count1_en_temp = cca_term0; 3'b001: cca_count1_en_temp = cca_term1; 3'b010: cca_count1_en_temp = cca_term2; 3'b011: cca_count1_en_temp = cca_term3; 3'b100: cca_count1_en_temp = cca_term4; 3'b101: cca_count1_en_temp = cca_term5; 3'b110: cca_count1_en_temp = cca_term6; 3'b111: cca_count1_en_temp = cca_term7; cca_count1_en_final = consider_rx_cca_only ? (cca_count1_en_temp &

0x300014C MTU_TIMER_CONTROL11TO8

Type: read-write
Reset State: 0x00000000

This register contains all the controls for the timers 11 to 8.

MTU_TIMER_CONTROL11TO8

Bits	Name	Description
19:8	SW_MTU_CONTINUOUS_VALID	One bit for timer. if this bit is set, the timer will be loaded either with zero or the corresponding match register(depending on up/down). Basically if this bit is set the timer works as divided by N Reset State: 0x00000000

MTU_TIMER_CONTROL11TO8 (cont.)

Bits	Name	Description
7:0	SW_MTU_BASIC_UNIT_SELECT11TO8	2 bit for each timer is provided. bit [1:0] for timer 0, bit [3:2] for timer 1... To make these timers more flexible, 3 basic units are provided. if the control =0, the timer will be stopped (this is the only way to disable the counters if the control =01, timer is ++ at every clk if the control =10, timer is ++ at every one us if the control =11, timer is ++ at every programmable pulse. Basically in this mode, the period of the pulse is also controlled by software. Note that this programmable pulse is only one for all the timers Reset State: 0x00000000

0x3000150 MTU_MTU_GLOBAL_CONTROL

Type: read-write
Reset State: 0x19000000

Contains the global controls for mtu

MTU_MTU_GLOBAL_CONTROL

Bits	Name	Description
31:24	SW_MTU_SECONDARY_CCA_LIMIT	Whenever the secondary cca is hig for this limit (in us) time, mtu_mcu_secondary_cca_to will be generated. This functionality is exactly similar to pifs to except that the cca used is always secondary Reset State: 0x00000019
7:0	SW_MTU_SUPPRESS_RF_WARMUP	If this bit is set, mtu will not send rf_warmup to txp Any suggested value is welcome bit field [19:12] sw_mtu_suppress_rf_warmup_for_collision configuration 8'b0 bit fieldComment If this bit is set, mtu will not send rf_warmup to txp for the collision case Any suggested value is welcome Reset State: 0x00000000

0x3000154 MTU_MTU_INTERRUPT_STATUS11TO8

Type: read-write
Reset State: 0x00000000

This register contains the status of all the interrupts that are generated by mtu Basically every interrupt has a corresponding register bit which will be set on sending interrupt pulse to the interrupt module and this bit is reset by writing '1' to it. software has higher priority over hardware

MTU_MTU_INTERRUPT_STATUS11TO8

Bits	Name	Description
31:21	TXP_SIFS_DELAY_CNT_FORINNAV	The internal count is exposed. Basically this counter keeps ++ after the rising edge of pkt_det. The resolution is one clock (it is 25ns in 40Mhz mode, 12.5 if mac is selected of 80Mhz) Reset State: 0x00000000
11:8	MTU_MCU_TSF_INT_FLAG11TO8	4 registers for upper 4 tsf based match register interrupts. bit 0 for match 0, 1 for match 1 ... Reset State: 0x00000000
7:4	MTU_MCU_BKOF_INT_FLAG11TO8	4 registers for upper 4 back off interrupts. bit 0 for timer 0, 1 for timer 1 ... Reset State: 0x00000000
3:0	MTU_MCU_TIMER_INT_FLAG11TO8	4 registers for upper 4 timer interrupts. bit 0 for timer 0, 1 for timer 1 ... Reset State: 0x00000000

0x3000158 MTU_MTU_GLOBAL_CONTROL2

Type: read-write
Reset State: 0x000000EE

Contains the global controls for mtu

MTU_MTU_GLOBAL_CONTROL2

Bits	Name	Description
10	SW_MTU_CONSIDER_SKIP_DIFS	if this bit is set, the skip_difs from the rxp is used.. to take care of any bug in other module. Since this is not a main line function, better to have a protection Reset State: 0x00000000
9	SW_MTU_SELECT_LATE_PKT_DET_FOR_ACK_TO	if this bit is set, the late pkt_det is used for ack_to. By default the early_pkt-det should be used. This bit should never be set in the system. The configuration is provided for unknown flexibility.. Should be removed in the next spin at least Reset State: 0x00000000
8	SW_MTU_NAV_BASED_ON_RTS_VALID	The shadow_nav_cnt logic is enabled only when this bit is set. The nav update for RTS is done irrespective of this bit but the rts_nav_to logic is not enabled if this bit is set Reset State: 0x00000000

MTU_MTU_GLOBAL_CONTROL2 (cont.)

Bits	Name	Description
7:0	SW_MTU_RTS_NAV_TO_LIMIT	This register represents the timeout count in the following On receiving an RTS based NAV, a shadow NAV counter will keep running the previous NAV setting. The RTS NAV will be used to set the NAV. A (Programmable) timeout counter is started. If no pkdet_n is detected before the timeout count expires, the shadow NAV will be used again to set the NAV. If a pktdet_n is seen before the timeout expires, the RTS based NAV will continue. The 'shadow' NAV can now be discarded. The default is a randomly chosen.Any suggested value is welcome Reset State: 0x000000EE

0x300015C MTU_SW_MTU_SHADOW_NAV_CNT

Type: read-write
Reset State: 0x000000FF

This register contains the nav value in shadow register NAV is updated by hardware as well as by the software. Software has higher priority over the hardware updates

MTU_SW_MTU_SHADOW_NAV_CNT

Bits	Name	Description
31:0	SW_MTU_SHADOW_NAV_CNT	This register contains the nav value. The value is in micro seconds. This register just follows the nav_cnt but it will differ during the rts_nav update. When there is rts NAV update, the current NAV iscopied to this register and keeps updated. If there is rts_nav_to, this value is copied to the nav_cnt. Reset State: 0x000000FF

0x3000160 MTU_PRIMARY_CCA_HISTOGRAM_LO

Type: read-only
Reset State: 0xFFFFFFFF

This register contains the lower 32 bits of primary_cca_histogram

MTU_PRIMARY_CCA_HISTOGRAM_LO

Bits	Name	Description
31:0	PRIMARY_CCA_HISTOGRAM31TO0	the primary cca is sampled at every slot time and shifted through a shift register software can read the shift register value through this address Reset State: 0xFFFFFFFF

0x3000164 MTU_PRIMARY_CCA_HISTOGRAM_HI

Type: read-only
Reset State: 0xFFFFFFFF

This register contains the higher 32 bits of primary_cca_histogram

MTU_PRIMARY_CCA_HISTOGRAM_HI

Bits	Name	Description
31:0	PRIMARY_CCA_HISTOGRAM63TO32	the primary cca is sampled at every slot time and shifted through a shift register software can read the shift register value through this addressaddress Reset State: 0xFFFFFFFF

0x3000168 MTU_SECONDARY_CCA_HISTOGRAM_LO

Type: read-only
Reset State: 0xFFFFFFFF

This register contains the lower 32 bits of secondary_cca_histogram

MTU_SECONDARY_CCA_HISTOGRAM_LO

Bits	Name	Description
31:0	SECONDARY_CCA_HISTOGRAM31TO0	the secondary cca is sampled at every slot time and shifted through a shift register software can read the shift register value through this address Reset State: 0xFFFFFFFF

0x300016C MTU_SECONDARY_CCA_HISTOGRAM_HI

Type: read-only
Reset State: 0xFFFFFFFF

This register contains the higher 32 bits of secondary_cca_histogram

MTU_SECONDARY_CCA_HISTOGRAM_HI

Bits	Name	Description
31:0	SECONDARY_CCA_HISTOGRAM63TO32	the secondary cca is sampled at every slot time and shifted through a shift register software can read the shift register value through this address Reset State: 0xFFFFFFFF

0x3000170 MTU_TIMEOUT_LIMIT

Type: read-write
Reset State: 0x000640F5

This register contains the Timeouts for rsp_to and ..

MTU_TIMEOUT_LIMIT

Bits	Name	Description
20:10	SW_MTU_SIFS_LIMIT_FOR_WARMUP	This is the time within SIFS up to which we will mask out warmup (in clks) The default is 10 microseconds. This needs to be changed. Right now it is made same as what we have in Libra (10 microseconds) for 40Mhz clock (25ns*4000 = 10,000ns=10microseconds). If the clock is 80Mhz, this should be 2*400=800 Reset State: 0x00000190
9	SW_MTU_NOT_A_BUG_FIX	if the interrupts are back to back, though it should not be, there is a corner case the system could hang. So configurable fix.. Reset State: 0x00000000
8	SW_MTU_FORGET_PKT_DET_TO	Since this logic is to take care of fsm lock or misbehavior of early pkt det, we don't want this to be enabled by default Reset State: 0x00000000
7:0	SW_MTU_PKT_DET_TO_LIMIT	To make sure the fsm don't get in a loop while waiting for response time out, we use more reliable pkt_det from PHY and run a counter when the fsm is not in idle and the pkt_det is HIGH. When the counter reaches this limit, the fsm comes out and gives a time out interrupt to software. The default is f5. Basically a big value The limit is in micro seconds Reset State: 0x000000F5

0x3000174 MTU_CCA_FINAL_CONTROL_REG

Type: read-write
Reset State: 0x00000000

this register contains the controls to select the final cca that needs to be used for a particular back_off engine

MTU_CCA_FINAL_CONTROL_REG

Bits	Name	Description
23:0	SW_MTU_FINAL_CCA_SEL	3 bits for each back off. 2:0 for back off 0, 5:3 back off 1,... and so on 000 -- CCA 001 -- (CCA && early_pktdet_n) 010 -- (CCA && pktdet_n) 011 -- early_pktdet_n 100 -- pktdet_n 101 -- (CCA && (early_pktdet_n ||

0x300017C MTU_EARLY_INTERRUPT_LIMITS

Type: read-write
Reset State: 0x00050104

this register contains the time limits for early interrupt to s/w, txp back_off engine. The early interrupt to software is sw_mtu_early_sw_int_limit_us+sw_mtu_early_sw_int_limit_us_clks

MTU_EARLY_INTERRUPT_LIMITS

Bits	Name	Description
21:16	SW_MTU_TXP_SIFS_WIDTH_LIMIT	sw_mtu_txp_sifs_flag will be set as per the limit. After this limit the flag will just follow the pkt_det Reset State: 0x00000005
15:8	SW_MTU_EARLY_SW_INT_LIMIT_CLKS	This gives the delay in clks -- used by pifs and the back off interrupts See the comments in above field for mor info Reset State: 0x00000001
7:0	SW_MTU_EARLY_SW_INT_LIMIT_US	This gives the delay in microseconds -- used by back off interrupts basically an early slot pulse is generated whenever the slot count == this limit and one_microseconds count == sw_mtu_early_sw_int_limit_clks. The sw_mtu_early_sw_int_limit_clks is used to provide a resolution of one clk. Since the one_microseconds counter is a down counter the programming should be in terms of delay. Basically we want .25 microseconds early, we should program 1-.25 =.75=90 clks (approx) Reset State: 0x00000004

0x3000180 MTU_BTC_CONFIG_REGISTERS

Type: read-write
Reset State: 0x00000000

this register contains the Controls for btc

MTU_BTC_CONFIG_REGISTERS

Bits	Name	Description
25	SW_MTU_TX_GRANT_SEL	0x0: select bt_active, '1': select lte_tx_grant signal for sw_mtu_btc_cca_control Reset State: 0x00000000
24	SW_MTU_CONSIDER_QUATERNARY_CCA	If this is set rxp_mtu_quaternary_cca is considered in generation of mtu_btc_tx_rx_busy Reset State: 0x00000000
23	SW_MTU_CONSIDER_TERTIARY_CCA	If this is set rxp_mtu_tertiary_cca is considered in generation of mtu_btc_tx_rx_busy Reset State: 0x00000000

MTU_BTC_CONFIG_REGISTERS (cont.)

Bits	Name	Description
22	SW_MTU_BTC_PIFS_CONTROL	If this is set the final btc signals are considered in pifs. To consider both high and low prio sw_mtu_consider_low_pri_btc_active also need to be set Reset State: 0x00000000
21:6	SW_MTU_BTC_CCA_CONTROL	This controls the ANDING of BTC to CCA of the 8 back-offs 2 bits for each back-off (Only 8 nack-offs are considered) 21:6 00 --> don't consider btc from mcu/btc 01 --> Just simply aND with CCA 10 --> Don't consider till the slot count = 1 Reset State: 0x00000000
5	SW_MTU_CONSIDER_SECONDARYCCA	If this is set rxp_mtu_secondary_cca is considered in generation of mtu_btc_tx_rx_busy Reset State: 0x00000000
4	SW_MTU_CONSIDER_PRIMARYCCA	If this is set rxp_mtu_primary_cca is considered in generation of mtu_btc_tx_rx_busy Reset State: 0x00000000
3	SW_MTU_CONSIDER_EARLYPKTDETN	If this is set rxp_mtu_early_pktdet_n is considered in generation of mtu_btc_tx_rx_busy Reset State: 0x00000000
2	SW_MTU_CONSIDER_PKTDETN	If this is set rxp_mtu_pktdet_n is considered in generation of mtu_btc_tx_rx_busy Reset State: 0x00000000
1	SW_MTU_CONSIDER_PHYTXIDLE	If this is set txp_mtu_phytx_idle is considered in generation of mtu_btc_tx_rx_busy Reset State: 0x00000000
0	SW_MTU_CONSIDER_NAVACTIVE	If this is set nav_active is considered in generation of mtu_btc_tx_rx_busy Reset State: 0x00000000

0x3000184 MTU_MTU_TESTBUS_LOW

Type: read-only
Reset State: 0x00000000

This register contains the lower 32 bits of mtu testbus

MTU_MTU_TESTBUS_LOW

Bits	Name	Description
31:0	MTU_MCU_TESTBUS31TO0	This register contains the lower 32 bits of mtu testbus Reset State: 0x00000000

0x3000188 MTU_MTU_TESTBUS_HIGH

Type: read-write
Reset State: 0x00000000

This register contains the higher 13 bits of mtu testbus

MTU_MTU_TESTBUS_HIGH

Bits	Name	Description
20:16	SW_MTU_TEST_SEL	MTU test bus selection Reset State: 0x00000000
12:0	MTU_MCU_TESTBUS44TO32	This register contains the upper lower 13 bits of mtu testbus Reset State: 0x00000000

0x300018C MTU_MTU_FOR_HMAC_CONTROLS

Type: read-write
Reset State: 0xFF181003

This register contains the new registers that are added for hmac -- gen5/6

MTU_MTU_FOR_HMAC_CONTROLS

Bits	Name	Description
31:24	SW_MTU_HW_BACKOFF_VALID	if this bit is set the hardware back-offs will be enabled. By default this bit is enabled One per backoff. Reset State: 0x000000FF
20	SW_MTU_ALLOW_PMU_DISABLE	When cleared, the tsf timer will be always running When set, the tsf timer will be run when pmu_mtu_tsf_timer_en is asserted. Reset State: 0x00000001
19	SW_MTU_ALLOW_PMU_UPDATE	For UAPSD, we allowed PMU to be able to restore the tsf in MTU. This is made programmable to avoid any issues with this Reset State: 0x00000001
17	SW_MTU_BTAMP_MODE	When set, indicates it's in bt-amp mode. Reset State: 0x00000000
16	SW_MTU_SLR_LIMITS_ARE_VALID	SLR limits are valid only if this bit is set and the data rate is SLR Reset State: 0x00000000
15:8	SW_MTU_SLR_EARLY_PKT_DET_MISS_LIMIT	This is used in respons_to (ack_to) logic for SLR if the system is expecting a response and if the early pkt_det is HIGH for this limit, an interrupt is generated (old name is cca_miss_limit) Units are 4 microseconds Reset State: 0x00000010

MTU_MTU_FOR_HMAC_CONTROLS (cont.)

Bits	Name	Description
7	SW_MTU_CONSIDER_LSIG_CCA	only when this bit is set, the lsig from phy is considered in MTU Reset State: 0x00000000
6	SW_MTU_CONSIDER_LOW_PRI_BTC_ACTIVE	only when this bit is set, the mcu_mtu_bt_low_pri_active is considered in generation of final cca Reset State: 0x00000000
5	SW_MTU_IBSS_VALID	If this bit is set the back-off 0 is assigned for beacon... Reset State: 0x00000000
4	SW_MTU_DTIM_CNT_EN	Enables dtim counter. This bit needs to be set to enable dtim logic to be enabled Reset State: 0x00000000
2:0	SW_RSP_TO_CONSIDER_VECTOR	This register contains valid vector for ack_to. Basically bit 0 -- corresponds to mtu_mcu_timout_missing_early_pkt_det_p bit 1 -- corresponds to mtu_mcu_timout_missing_push_p bit 2 -- corresponds to mtu_mcu_timout_pkt_det_p Reset State: 0x00000003

0x3000190 MTU_MTU_DTIM_CNT_AND_PERIOD

Type: read-write
Reset State: 0x00000001

This register contains dtim_cnt dtim_period

MTU_MTU_DTIM_CNT_AND_PERIOD

Bits	Name	Description
31:16	DTIM_CNT	Basically this is the internal dtim counter. basically whenever this counter reaches, dtim_period -1 is loaded. this keeps ++ at every tbtt Reset State: 0x00000000
15:0	DTIM_PERIOD	This register contains the dtim period. The period is defined in number of beacons if this is 1, every beacon is DTIM. 2 means alternate beacons are dtim Reset State: 0x00000001

0x3000194 MTU_DTIM_THRSH_CNT_AND_LIMIT

Type: read-write
Reset State: 0x00000000

This register contains dtim_thrsh_limit and dtim_thrsh_limit

MTU_DTIM_THRSH_CNT_AND_LIMIT

Bits	Name	Description
31:16	DTIM_THRSH_CNT	Internal counter ++ at every microseconds to keep track of the dtim_thrsh_limit. This counter is effective only when sw_mtu_dtim_cnt_en is 1 Reset State: 0x00000000
15:0	DTIM_THRSH_LIMIT	This register contains the dtim_thrsh_limit. This number indicates the time in microseconds. Basically this number indicates up to what time during the DTIM beacon, MC and BC can be transmited Reset State: 0x00000000

0x3000198 MTU_TBTT_L

Type: read-write
Reset State: 0x7FFFFFFF

Lower 32 bits of tbtt register

MTU_TBTT_L

Bits	Name	Description
31:0	TBTT_L	Lower 32 bits of TBTT register. Reset State: 0x7FFFFFFF

0x300019C MTU_TBTT_H

Type: read-write
Reset State: 0x00000000

Upper 32 bits of tbtt rosewater

MTU_TBTT_H

Bits	Name	Description
31:0	TBTT_H	Upper 32 bits of TBTT register. Reset State: 0x00000000

0x30001A0 MTU_M_TBTT_L

Type: read-write
Reset State: 0x7FFFFFFF

Lower 32 bits of multiple bssid tbtt register

MTU_M_TBTT_L

Bits	Name	Description
31:0	M_TBTT_L	Lower 32 bits of TBTT register. Reset State: 0x7FFFFFFF

0x30001A4 MTU_M_TBTT_H

Type: read-write
Reset State: 0x00000000

Upper 32 bits of multiple bssid tbtt register.

MTU_M_TBTT_H

Bits	Name	Description
31:0	M_TBTT_H	Upper 32 bits of TBTT register. Reset State: 0x00000000

0x30001A8 MTU_BCN_BSSID_INTV

Type: read-write
Reset State: 0x00100064

Beacon Interval Register is programmed by software and it determined the period between two consecutive TBTT. This also contains the mbssid interval in microseconds

MTU_BCN_BSSID_INTV

Bits	Name	Description
29	SW_MTU_MBSSID_ENABLE	Multiple bssid are enabled only when this bit is set Reset State: 0x00000000
28	SW_MTU_TBTT_ENABLE	Beacons are enabled only when this bit is set Reset State: 0x00000000
27:24	SW_MTU_MAX_BSSIDS	Beacons are enabled only when this bit is set Reset State: 0x00000000
23:16	SW_MTU_BSSID_INTV	This bits determine the period between two consecutive beacons of different bssids. This value is in n 256 micro seconds. Each count is 256 microseconds Reset State: 0x00000010
15:0	SW_MTU_BEACON_INTV	This bits determine the period between two consecutive beacon. This value is in ms message. Reset State: 0x00000064

0x30001AC MTU_VALID_BSSID_BITMAP

Type: read-write
Reset State: 0x00070001

This register contains the valid bssids in the system

MTU_VALID_BSSID_BITMAP

Bits	Name	Description
31:16	IBSS_BCN_CW_LIMIT	This register contains the cw limit for ibss Reset State: 0x00000007
15:0	SW_MTU_VALID_BSSID_BITMAP	A 16 bit register indicates which bssid is enabled Bit 0 should be enabled for single bssid By default only one bssid is enabled message. Reset State: 0x00000001

0x30001B0 MTU_IBSS_BKOF_CNT

Type: read-write
Reset State: 0x00000000

This register contains the bkof_cnt of ibss. The units are slot number.

MTU_IBSS_BKOF_CNT

Bits	Name	Description
15:0	IBSS_BKOF_CNT	This register contains the bkof_counter value for the ibss_bkof_cnt this value = (lfsr_data & lfsr_value) Reset State: 0x00000000

0x30001B4 MTU_LFSR_DATA_1_0

Type: read-only
Reset State: 0x00000000

This register contains the lfsr_data of bkof 1 and 0.

MTU_LFSR_DATA_1_0

Bits	Name	Description
31:16	LFSR_DATA_1	This register contains the lfsr_data value for the bkof_1 Reset State: 0x00000000

MTU_LFSR_DATA_1_0 (cont.)

Bits	Name	Description
15:0	LFSR_DATA_0	This register contains the lfsr_data value for the bkof_0 Reset State: 0x00000000

0x30001B8 MTU_LFSR_DATA_3_2

Type: read-only
Reset State: 0x00000000

This register contains the lfsr_data of bkof 3 and 2.

MTU_LFSR_DATA_3_2

Bits	Name	Description
31:16	LFSR_DATA_3	This register contains the lfsr_data value for the bkof_3 Reset State: 0x00000000
15:0	LFSR_DATA_2	This register contains the lfsr_data value for the bkof_2 Reset State: 0x00000000

0x30001BC MTU_LFSR_DATA_5_4

Type: read-only
Reset State: 0x00000000

This register contains the lfsr_data of bkof 5 and 4.

MTU_LFSR_DATA_5_4

Bits	Name	Description
31:16	LFSR_DATA_5	This register contains the lfsr_data value for the bkof_5 Reset State: 0x00000000
15:0	LFSR_DATA_4	This register contains the lfsr_data value for the bkof_4 Reset State: 0x00000000

0x30001C0 MTU_LFSR_DATA_7_6

Type: read-only
Reset State: 0x00000000

This register contains the lfsr_data of bkof 7 and 6.

MTU_LFSR_DATA_7_6

Bits	Name	Description
31:16	LFSR_DATA_7	This register contains the lfsr_data value for the bkof_7 Reset State: 0x00000000
15:0	LFSR_DATA_6	This register contains the lfsr_data value for the bkof_6 Reset State: 0x00000000

0x30001C4 MTU_LONG_SHORT_XMIT_LIMIT_BKOF_3_TO_0

Type: read-only
Reset State: 0x47474747

This register contains the sort and long retry limits for backoff cw adjustment

MTU_LONG_SHORT_XMIT_LIMIT_BKOF_3_TO_0

Bits	Name	Description
31:0	SW_LONG_SHORT_XMIT_LIMIT_BKOF_3_TO_0	This register contains the short and long retry limts for bkof-3 to 0. 3:0 is short, 7:4 is long for back off 0. 11:8 is short, 15:12 is long for back off 1. 19:16 is short, 23:20 is long for back off 2. 27:24 is short, 31:28 is long for back off 3. Reset State: 0x47474747

0x30001C8 MTU_LONG_SHORT_XMIT_LIMIT_BKOF_7_TO_4

Type: read-only
Reset State: 0x47474747

This register contains the sort and long retry limts for backoff cw adjustment

MTU_LONG_SHORT_XMIT_LIMIT_BKOF_7_TO_4

Bits	Name	Description
31:0	SW_LONG_SHORT_XMIT_LIMIT_BKOF_7_TO_4	This register contains the short and long retry limits for bkof-7 to 4. 3:0 is short, 7:4 is long for back off 4. 11:8 is short, 15:12 is long for back off 5. 19:16 is short, 23:20 is long for back off 6. 27:24 is short, 31:28 is long for back off 7. Reset State: 0x47474747

0x30001CC MTU_WARMUP_LIMIT

Type: read-write
Reset State: 0x00000025

This register contains the threshold number for txp_mpi_rf_warmup.

MTU_WARMUP_LIMIT

Bits	Name	Description
11:8	TXP_MPI_RF_WARMUP_CNT	counter number of txp_mpi_rf_warmup high duration. Reset State: 0x00000000
7	TXP_MPI_RF_WARMUP_LOW_FLAG	When assert, indicates the duration of txp_mpi_rf_warmup is less than sw_mtu_warmup_thrd_low. Reset State: 0x00000000
6	TXP_MPI_RF_WARMUP_HIGH_FLAG	When assert, indicates the duration of txp_mpi_rf_warmup is longer than sw_mtu_warmup_thrd_high. Reset State: 0x00000000
5:4	SW_MTU_WARMUP_THRD_LOW	This register contains the lower limit value (in unit of microseconds) for txp_mpi_rf_warmup. Reset State: 0x00000002
3:0	SW_MTU_WARMUP_THRD_HIGH	This register contains the upper limit value (in unit of microseconds) for txp_mpi_rf_warmup. Reset State: 0x00000005

0x30001D0 MTU_ONE_SEC_LIMIT

Type: read-write
Reset State: 0x000F423F

This register contains the threshold number for one_sec pulse

MTU_ONE_SEC_LIMIT

Bits	Name	Description
19:0	SW_MTU_ONE_SEC_LIMIT	limit value to be programmed to get one sec pulse. Basically this is number of microseconds. this value is loaded into a counter and keep getting decremented at every one_microseconds_p. Reset State: 0x000F423F

0x30001D4 MTU_MTU_GLOBAL_TIMER

Type: read-write
Reset State: 0x00000000

This register contains a global timer to be used by all modules including software if it wants

MTU_MTU_GLOBAL_TIMER

Bits	Name	Description
31:0	MTU_GLOBAL_TIMER	This is a global timer increments at every one microseconds. This is different from tsf timer Reset State: 0x00000000

0x30001D8 MTU_TSF_TIMER_FOR_SIM_BSS_LO

Type: read-write
Reset State: 0x00000000

This register contains the lower 32 bits of the tsf timer used only during simultaneous bss and ibss mode This corresponds to BSS tsf during simultaneous mode. In none Simultaneous mode, this is not valid

MTU_TSF_TIMER_FOR_SIM_BSS_LO

Bits	Name	Description
31:0	TSF_TIMER_FOR_SIM_BSS_LO	This register contains the lower 32 bits of the tsf timer used only during simultaneous bss and ibss mode This corresponds to BSS tsf during simultaneous mode. In none Simultaneous mode, this is not valid Reset State: 0x00000000

0x30001DC MTU_TSF_TIMER_FOR_SIM_BSS_HI

Type: read-write
Reset State: 0x00000000

This register contains the upper 32 bits of the tsf timer used only during simultaneous bss and ibss mode This corresponds to BSS tsf during simultaneous mode. In none Simultaneous mode, this is not valid

MTU_TSF_TIMER_FOR_SIM_BSS_HI

Bits	Name	Description
31:0	TSF_TIMER_FOR_SIM_BSS_HI	This register contains the upper 32 bits of the tsf timer used only during simultaneous bss and ibss mode This corresponds to BSS tsf during simultaneous mode. In none Simultaneous mode, this is not valid Reset State: 0x00000000

0x30001E0 MTU_SW_MTU_SIFS_LIMIT_FORINNAV

Type: read-write
Reset State: 0x00000190

This is register that contains the SIFS Limit specified in number of clocks rather than in microseconds

MTU_SW_MTU_SIFS_LIMIT_FORINNAV

Bits	Name	Description
10:0	SW_MTU_SIFS_LIMIT_FORINNAV	This is register that contains the SIFS Limit specified in number of clocks rather than in microseconds The default is 15 microseconds. This needs to be changed. Right now it is made same as what we have in Libra (14 microseconds) for 40Mhz clock (25ns*560 = 14,000ns=14microseconds). If the clock is 80Mhz, this should be 2*560 = 1130 Reset State: 0x00000190

0x30001E4 MTU_SW_MTU_P2P_GO_TSF_TIMER_LO

Type: read-write
Reset State: 0x00000000

This is register that contains the lower 32 bits of the p2p group owner tsf timer

MTU_SW_MTU_P2P_GO_TSF_TIMER_LO

Bits	Name	Description
31:0	P2P_GO_TSF_TIMER_LO	The lower 32 bits of the p2p group owner tsf timer In unit of us. Reset State: 0x00000000

0x30001E8 MTU_SW_MTU_P2P_GO_TSF_TIMER_HI

Type: read-write
Reset State: 0x00000000

This is register that contains the upper 32 bits of the p2p group owner tsf timer

MTU_SW_MTU_P2P_GO_TSF_TIMER_HI

Bits	Name	Description
31:0	P2P_GO_TSF_TIMER_HI	The upper 32 bits of the p2p group owner tsf timer In unit of us. Reset State: 0x00000000

0x30001EC MTU_SW_MTU_P2P_CLIENT_TSF_TIMER_LO

Type: read-write
Reset State: 0x00000000

This is register that contains the lower 32 bits of the p2p client owner tsf timer

MTU_SW_MTU_P2P_CLIENT_TSF_TIMER_LO

Bits	Name	Description
31:0	P2P_CLIENT_TSF_TIMER_LO	The lower 32 bits of the p2p client owner tsf timer In unit of us. Reset State: 0x00000000

0x30001F0 MTU_SW_MTU_P2P_CLIENT_TSF_TIMER_HI

Type: read-write
Reset State: 0x00000000

This is register that contains the upper 32 bits of the p2p client owner tsf timer

MTU_SW_MTU_P2P_CLIENT_TSF_TIMER_HI

Bits	Name	Description
31:0	P2P_CLIENT_TSF_TIMER_HI	The upper 32 bits of the p2p client owner tsf timer In unit of us. Reset State: 0x00000000

0x30001F4 MTU_SW_MTU_P2P_CTRL

Type: read-write
Reset State: 0x00000040

This is register that contains the control bits for p2p feature

MTU_SW_MTU_P2P_CTRL

Bits	Name	Description
18:17	LTE_TSF_INSERTION_SEL	To select the TSF value to be provided to lte cxm 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
16	SW_BEACON_TRANSMIT_EN	Writing a '1' to trigger a beacon transmission. Always read zero Reset State: 0x00000000

MTU_SW_MTU_P2P_CTRL (cont.)

Bits	Name	Description
15:8	P2P_TX_BOUNDARY_THRESHOLD	The bcoff will be disabled after the transmit_boundary_timer reaches this value Reset State: 0x00000000
6:4	GLOBAL_TIMER_SRC_SEL	To select the source for the global timer 3'b000: BSS TSF; 3'b001: IBSS TSF; 3'b010: P2P group owner TSF; 3'b011: P2P client TSF 3'b100: internal timer Reset State: 0x00000004
3:2	P2P_TSF_INSERTION_SEL	To select the TSF value to be inserted in beacons in TPE 2'b00: BSS TSF; 2'b01: IBSS TSF; 2'b10: P2P group owner TSF; 2'b11: P2P client TSF Reset State: 0x00000000
1	P2P_CLIENT_TSF_TIMER_EN	Set to 1 to enable the p2p client timer Reset State: 0x00000000
0	P2P_GO_TSF_TIMER_EN	Set to 1 to enable the p2p group owner timer Reset State: 0x00000000

0x30001F8 MTU_SW_MTU_P2P_TRANSMIT_BOUNDARY

Type: read-write
Reset State: 0x00000000

This is register that contains the config bits of the transmit boundary timer

MTU_SW_MTU_P2P_TRANSMIT_BOUNDARY

Bits	Name	Description
31	P2P_TRANSMIT_BOUNDARY_EN	Set 1 to enable the transmit boundary feature. Reset State: 0x00000000
27:20	P2P_INT_BOUNDARY	When the counter reaches this value, an interrupt will be generated. In unit of us. Reset State: 0x00000000
18:0	P2P_TRANSMIT_BOUNDARY	A down counter that software can program so that no frame exchanges will go over this boundary. When value 0 is reached, no more transmissions happen, until a new none zero value is programmed or this feature is disabled. In unit of us. Reset State: 0x00000000

0x30001FC MTU_SW_MTU_P2P_WAIT_FOR_BEACON

Type: read-write
Reset State: 0x00020000

This is register that contains the config bits of the wait for beacon timer

MTU_SW_MTU_P2P_WAIT_FOR_BEACON

Bits	Name	Description
31	P2P_WAIT_FOR_BEACON_EN	Set 1 to enable the wait for beacon feature. Reset State: 0x00000000
17:16	P2P_WAIT_FOR_BEACON_SEL	To select which beacon to wait for. 2'b00: IBSS beacon, 2'b01: BSS beacon, 2'b10: p2p client beacon. Reset State: 0x00000002
15:0	P2P_MAX_WAIT_DURATION	max duration of waiting for the p2p beacon. Start at p2p tbtt. In unit of us. Reset State: 0x00000000

0x3000200 MTU_TERTIARY_CCA_HISTOGRAM_LO

Type: read-only
Reset State: 0xFFFFFFFF

This register contains the lower 32 bits of tertiary_cca_histogram

MTU_TERTIARY_CCA_HISTOGRAM_LO

Bits	Name	Description
31:0	TERTIARY_CCA_HISTOGRAM31TO0	the tertiary cca is sampled at every slot time and shifted through a shift register software can read the shift register value through this address Reset State: 0xFFFFFFFF

0x3000204 MTU_TERTIARY_CCA_HISTOGRAM_HI

Type: read-only
Reset State: 0xFFFFFFFF

This register contains the higher 32 bits of tertiary_cca_histogram

MTU_TERTIARY_CCA_HISTOGRAM_HI

Bits	Name	Description
31:0	TERTIARY_CCA_HISTOGRAM63TO32	the tertiary cca is sampled at every slot time and shifted through a shift register software can read the shift register value through this address Reset State: 0xFFFFFFFF

0x3000208 MTU_QUATERNARY_CCA_HISTOGRAM_LO

Type: read-only
Reset State: 0xFFFFFFFF

This register contains the lower 32 bits of quaternary_cca_histogram

MTU_QUATERNARY_CCA_HISTOGRAM_LO

Bits	Name	Description
31:0	QUATERNARY_CCA_HISTOGRAM31TO0	the quaternary cca is sampled at every slot time and shifted through a shift register software can read the shift register value through this address Reset State: 0xFFFFFFFF

0x300020C MTU_QUATERNARY_CCA_HISTOGRAM_HI

Type: read-only
Reset State: 0xFFFFFFFF

This register contains the higher 32 bits of quaternary_cca_histogram

MTU_QUATERNARY_CCA_HISTOGRAM_HI

Bits	Name	Description
31:0	QUATERNARY_CCA_HISTOGRAM63TO32	the quaternary cca is sampled at every slot time and shifted through a shift register software can read the shift register value through this address Reset State: 0xFFFFFFFF

0x3000210 MTU_MTU_CCA_CONTROL

Type: read-write
Reset State: 0x00001919

Contains the 3rd and 4th cca controls for mtu

MTU_MTU_CCA_CONTROL

Bits	Name	Description
23:16	SW_MTU_RAW_CCA_SEL_NEW	Work with cca_control_reg.sw_mtu_raw_cca_sel to select the cca for backoffs. bit16 for bkof0, bit17 for bkof1 ... Reset State: 0x00000000

MTU_MTU_CCA_CONTROL (cont.)

Bits	Name	Description
15:8	SW_MTU_QUATERNARY_CCA_LIMIT	Whenever the quaternary cca is high for this limit (in us) time, mtu_mcu_quaternary_cca_to will be generated. Reset State: 0x00000019
7:0	SW_MTU_TERTIARY_CCA_LIMIT	Whenever the tertiary cca is high for this limit (in us) time, mtu_mcu_tertiary_cca_to will be generated. Reset State: 0x00000019

0x3000214 MTU_MTU_CCA_STATUS

Type: read-only
Reset State: 0x00000000

Contains the 3rd and 4th cca status for mtu

MTU_MTU_CCA_STATUS

Bits	Name	Description
1	QUATERNARY_CCA_TO	the quaternary_cca_to is sampled and software can read its status through this register Reset State: 0x00000000
0	TERTIARY_CCA_TO	the tertiary_cca_to is sampled and software can read its status through this register Reset State: 0x00000000

0x3000218 MTU_ADD_TSF_TIMER_LO

Type: read-write
Reset State: 0x00000000

This register contains the lower 32 bits of the value to be added to the tsf timer

MTU_ADD_TSF_TIMER_LO

Bits	Name	Description
31:0	ADD_TSF_TIMER_LO	This register contains the lower 32 bits of the value to be added to the tsf timer Reset State: 0x00000000

0x300021C MTU_ADD_TSF_TIMER_HI

Type: read-write
Reset State: 0x00000000

This register contains the upper 32 bits of the value to be added to the tsf timer

MTU_ADD_TSF_TIMER_HI

Bits	Name	Description
31:0	ADD_TSF_TIMER_HI	This register contains the upper 32 bits of the value to be added to the tsf timer Reset State: 0x00000000

0x3000220 MTU_TSF_TIMER_CTRL

Type: read-only
Reset State: 0x00000000

This register control the add function to the tsf timer

MTU_TSF_TIMER_CTRL

Bits	Name	Description
0	ADD_TSF_TIMER	Write 1 to this bit so the sum of the add_tsf_timer_[hi|lo] value and the current tsf timer will be loaded to the tsf timer. Reset State: 0x00000000

0x3000224 MTU_MTU_LTE_CXM_TSF_LOW

Type: read-only
Reset State: 0x00000000

This register contains the lower 32-bits tsf value captured by the coex_frame_sync signal

MTU_MTU_LTE_CXM_TSF_LOW

Bits	Name	Description
31:0	MTU_LTE_CXM_TSF_LOW	The lower 32-bits tsf value captured by the capture_clk signal Reset State: 0x00000000

0x3000228 MTU_MTU_LTE_CXM_TSF_HIGH

Type: read-only
Reset State: 0x00000000

This register contains the upper 32-bits tsf value captured by the coex_frame_sync signal

MTU_MTU_LTE_CXM_TSF_HIGH

Bits	Name	Description
31:0	MTU_LTE_CXM_TSF_HIGH	The upper 32-bits tsf value captured by the capture_clk signal Reset State: 0x00000000

0x300022C MTU_SW_SECONDARY_CCA_HISTOGRAM_MASK

Type: read-write
Reset State: 0x0007F800

This register contains the mask bits of the secondary cca histogram for the bw signaling frame exchange

MTU_SW_SECONDARY_CCA_HISTOGRAM_MASK

Bits	Name	Description
31:0	SW_SECONDARY_CCA_HISTOGRAM_MASK	The mask bits for the secondary cca histogram for 6mbps rts data in unit of 3microseconds. Reset State: 0x0007F800

0x3000230 MTU_SW_TERTIARY_CCA_HISTOGRAM_MASK

Type: read-write
Reset State: 0x0007F800

This register contains the mask bits of the tertiary cca histogram for the bw signaling frame exchange

MTU_SW_TERTIARY_CCA_HISTOGRAM_MASK

Bits	Name	Description
31:0	SW_TERTIARY_CCA_HISTOGRAM_MASK	The mask bits for the tertiary cca histogram for 6mbps rts data in unit of 3 microseconds. Reset State: 0x0007F800

0x3000234 MTU_SW_QUATERNARY_CCA_HISTOGRAM_MASK

Type: read-write
Reset State: 0x0007F800

This register contains the mask bits of the quaternary cca histogram for the bw signaling frame exchange

MTU_SW_QUATERNARY_CCA_HISTOGRAM_MASK

Bits	Name	Description
31:0	SW_QUATERNARY_CCA_HISTOGRAM_MASK	The mask bits for the quaternary cca histogram for 6mbps rts data in unit of 3 microseconds. Reset State: 0x0007F800

0x3000238 MTU_SW_CCA_HISTOGRAM_MASK_MISC

Type: read-write
Reset State: 0x00000002

This register contains the shift value of the cca histogram for the bw signaling frame exchange

MTU_SW_CCA_HISTOGRAM_MASK_MISC

Bits	Name	Description
6	MTU_TPE_80MHZ_CCA_IS_IDLE_NON6MBPS	The 80mhz cca status (masked and shift) Reset State: 0x00000000
5	MTU_TPE_40MHZ_CCA_IS_IDLE_NON6MBPS	The 40mhz cca status (masked and shift) Reset State: 0x00000000
4	MTU_TPE_80MHZ_CCA_IS_IDLE_6MBPS	The 80mhz cca status (masked without shift) Reset State: 0x00000000
3	MTU_TPE_40MHZ_CCA_IS_IDLE_6MBPS	The 40mhz cca status (masked without shift) Reset State: 0x00000000
2:0	SW_CCA_HISTOGRAM_MASK_SHIFT	Right shift the mask bits of the cca histogram for non-6mbps rts data Reset State: 0x00000002

0x300023C MTU_CCA_SECONDARY_HISTOGRAM

Type: read-only
Reset State: 0xFFFFFFFF

This register contains the secondary cca histogram

MTU_CCA_SECONDARY_HISTOGRAM

Bits	Name	Description
31:0	CCA_SECONDARY_HISTOGRAM	The secondary cca is sampled at every 2us time and shifted through a shift register Reset State: 0xFFFFFFFF

0x3000240 MTU_CCA_TERTIARY_HISTOGRAM

Type: read-only
Reset State: 0xFFFFFFFF

This register contains the tertiary cca histogram

MTU_CCA_TERTIARY_HISTOGRAM

Bits	Name	Description
31:0	CCA_TERTIARY_HISTOGRAM	The tertiary cca is sampled at every 2us time and shifted through a shift register Reset State: 0xFFFFFFFF

0x3000244 MTU_CCA_QUATERNARY_HISTOGRAM

Type: read-only
Reset State: 0xFFFFFFFF

This register contains the quaternary cca histogram

MTU_CCA_QUATERNARY_HISTOGRAM

Bits	Name	Description
31:0	CCA_QUATERNARY_HISTOGRAM	The quaternary cca is sampled at every 2us time and shifted through a shift register Reset State: 0xFFFFFFFF

16.2.44 QTA

0x3000000 QTA_INTR

Type: read-write
Reset State: 0x00000000

Interrupt status register.

QTA_INTR

Bits	Name	Description
26	RX_FIFO_UFLOW_INTR	Receive FIFO Underflow interrupt status bit. Software must write a 1 to this bit to clear it. Reset State: 0x00000000
25	RX_FIFO_OFLOW_INTR	Receive FIFO Overflow interrupt status bit. Software must write a 1 to this bit to clear it. Reset State: 0x00000000
24	RX_FIFO_RDY_INTR	Receive FIFO Ready interrupt status bit: Indicates when the Receive FIFO is ready to be drained of software characters. This interrupt is set every clock cycle while the FIFO fill level is greater than the Receive FIFO Trigger Level (rx_trig_level). Software must write a 1 to this bit to clear it. Reset State: 0x00000000
17	TX_FIFO_OFLOW_INTR	Transmit FIFO Overflow interrupt status bit. Software must write a 1 to this bit to clear it. Reset State: 0x00000000
16	TX_FIFO_RDY_INTR	Transmit FIFO Ready interrupt status bit: Indicates when the Transmit FIFO is ready to accept more software characters for transmission. This interrupt is set every clock cycle while the FIFO fill level is less than or equal to the Transmit FIFO Trigger Level (tx_trig_level). Software must write a 1 to this bit to clear it. Reset State: 0x00000000
8	RX_HW_CHAR_INTR	Received Hardware Character interrupt status bit. Software must write a 1 to this bit to clear it. Reset State: 0x00000000
1	PARITY_ERR_INTR	UART Parity Error interrupt status bit. Software must write a 1 to this bit to clear it. Reset State: 0x00000000
0	FRAME_ERR_INTR	UART Frame Error interrupt status bit. Software must write a 1 to this bit to clear it. Reset State: 0x00000000

0x3000004 QTA_INTR_EN

Type: read-write
Reset State: 0x00000000

Interrupt enable register.

QTA_INTR_EN

Bits	Name	Description
26	RX_FIFO_UFLOW_INTR_EN	Interrupt enable for the Receive FIFO Underflow interrupt. Reset State: 0x00000000
25	RX_FIFO_OFLOW_INTR_EN	Interrupt enable for the Receive FIFO Overflow interrupt. Reset State: 0x00000000
24	RX_FIFO_RDY_INTR_EN	Interrupt enable for the Receive FIFO Ready interrupt. Reset State: 0x00000000
17	TX_FIFO_OFLOW_INTR_EN	Interrupt enable for the Transmit FIFO Overflow interrupt. Reset State: 0x00000000
16	TX_FIFO_RDY_INTR_EN	Interrupt enable for the Transmit FIFO Ready interrupt. Reset State: 0x00000000
8	RX_HW_CHAR_INTR_EN	Interrupt enable for the Received Hardware Character interrupt. Reset State: 0x00000000
1	PARITY_ERR_INTR_EN	Interrupt enable for the Parity Error interrupt. Reset State: 0x00000000
0	FRAME_ERR_INTR_EN	Interrupt enable for the Frame Error interrupt. Reset State: 0x00000000

0x3000008 QTA_UART_CTRL

Type: read-write
Reset State: 0x03280060

UART control register.

QTA_UART_CTRL

Bits	Name	Description
31:24	BAUD_RATE_NUMERATOR	Sets the numerator for the ratio of the system clock frequency to the baud rate. Reset State: 0x00000003
23:16	BAUD_RATE_DENOMINATOR	Sets the denominator for the ratio of the system clock frequency to the baud rate. Reset State: 0x00000028
6	TX_INV_EN	When set, enables the UART's serial TX output inverter. Reset State: 0x00000001
5	RX_INV_EN	When set, enables the UART's serial RX input inverter. Reset State: 0x00000001

QTA_UART_CTRL (cont.)

Bits	Name	Description
4	POWER_DOWN	When set, puts the UART into power-down mode. The UART transmitter will complete its current transmission and then disable all further transmissions. The UART receiver will discard the current character being received and then ignore all further receptions. Reset State: 0x00000000
3	PARITY_EN	Enables parity bit generation in the UART transmitter, and parity checking in the UART receiver. Reset State: 0x00000000
2	PARITY_ODD	When parity is enabled, this bit specifies whether the parity is odd or even. When 1, the parity is odd; when 0, it is even. Reset State: 0x00000000
1:0	NUM_STOPS	Specifies the number of stop bits (1-4) at the end of each character. The number of stop bits per character = num_stops + 1. Reset State: 0x00000000

0x300000C QTA_HW_CTRL

Type: command
Reset State: 0x00000014

Hardware layer control register.

QTA_HW_CTRL

Bits	Name	Description
31:24	LAST_RX_HW_CHAR	This field captures the last received hardware character that was passed on to the Signaling layer. Reset State: 0x00000000
15	TX_BUFFER_STATE	State of the 1-character-deep Hardware TX Buffer. When 1, the buffer is full; when 0, the buffer is empty. Reset State: 0x00000000
14:8	TX_BUFFER_CONTENTS	This field captures the hardware character presently stored in the TX Buffer. Resend bit excluded as only non-Resend-Requests are stored in this buffer. Reset State: 0x00000000
7	RESEND_REQ_FLAG	Indicates the present state of the Resend Request flag. When set, it indicates that a Resend Request is pending transmission. Reset State: 0x00000000
4	EXCLUSIVE_RESEND_EN	Exclusive Resend Enable: When set, the QTA module will treat Signal State bits within Resend Request characters as invalid. When clear, the Signal State bits are valid regardless of whether the character is a Resend Request. Reset State: 0x00000001

QTA_HW_CTRL (cont.)

Bits	Name	Description
3	RESEND_REQ_PASSTHRU_EN	Resend Request Pass-Through Enable: When set, the QTA module will pass received Resend Request characters through to the Signaling layer for processing. NB: This feature is unsupported for the WLAN version of the QTA module, because the Signaling interface for the WLAN version does not support Resend signaling. Reset State: 0x00000000
2	RESEND_RESP_EN	Resend Response Enable: When this bit is set, the QTA module will automatically respond to received Resend Requests by resending its last (non-Resend-Request) hardware character. Otherwise, the QTA module will not respond to Resend Requests received from the peer device. Reset State: 0x00000001
1	RETRANSMIT	Retransmit TX Buffer contents: Writing a 1 to this bit causes the last (non-Resend-Request) hardware character to be re-transmitted. This bit is self-clearing. Reset State: 0x00000000
0	RESEND_REQUEST	Send a Resend Request: Writing a 1 to this bit causes a Resend Request character to be queued for transmission. This bit is self-clearing. Reset State: 0x00000000

0x3000010 QTA_HW_TX_BUFFER_MODIFY

Type: write-only
Reset State: 0x00000000

TX Buffer modify register.

QTA_HW_TX_BUFFER_MODIFY

Bits	Name	Description
6:0	DATA	Data to be written to the TX Buffer. Writing to this register causes the contents of the TX Buffer to be modified to the value of the data field, and causes the TX buffer state to be set to full. Reset State: 0x00000000

0x3000014 QTA_SW_CTRL

Type: read-write
Reset State: 0x00000000

Software layer control register.

QTA_SW_CTRL

Bits	Name	Description
29:24	RX_FILL	Indicates the number of software characters presently queued in the Receive FIFO. Reset State: 0x00000000
21	RX_FLUSH	Receive FIFO Flush: Writing a 1 to this bit flushes the contents of the Receive FIFO. This bit is self-clearing. Reset State: 0x00000000
20:16	RX_TRIG_LEVEL	Receive FIFO Trigger Level. See the rx_fifo_rdy_int interrupt status register description. Reset State: 0x00000000
13:8	TX_FILL	Indicates the number of software characters presently queued in the Transmit FIFO. Reset State: 0x00000000
5	TX_FLUSH	Transmit FIFO Flush: Writing a 1 to this bit flushes the contents of the Transmit FIFO. This bit is self-clearing. Reset State: 0x00000000
4:0	TX_TRIG_LEVEL	Transmit FIFO Trigger Level. See the tx_fifo_rdy_int interrupt status register description. Reset State: 0x00000000

0x3000018 QTA_SW_TX_FIFO_IN

Type: write-only
Reset State: 0x00000000

Software Transmit FIFO write data register.

QTA_SW_TX_FIFO_IN

Bits	Name	Description
7:0	DATA	Software character to be transmitted. Reset State: 0x00000000

0x300001C QTA_SW_RX_FIFO_OUT

Type: read-only
Reset State: 0x00000000

Software Receive FIFO read data register.

QTA_SW_RX_FIFO_OUT

Bits	Name	Description
7:0	DATA	Software character received. Reset State: 0x00000000

0x3000020 QTA_TESTBUS

Type: read-write
Reset State: 0x00000000

Test bus control register.

QTA_TESTBUS

Bits	Name	Description
3:0	SEL	Select input for the test bus multiplexer. 0x0: QTA_TESTBUS_NONE 0x1: QTA_TESTBUS_UART_RX 0x2: QTA_TESTBUS_UART_TX 0x3: QTA_TESTBUS_SW_FIFOS 0x4: QTA_TESTBUS_SW_RX 0x5: QTA_TESTBUS_SW_TX 0x6: QTA_TESTBUS_HW_RX 0x7: QTA_TESTBUS_HW_TX 0x8: QTA_TESTBUS_CONV_RX 0x9: QTA_TESTBUS_CONV_TX 0xA: QTA_TESTBUS_RESERVED_10 0xB: QTA_TESTBUS_RESERVED_11 0xC: QTA_TESTBUS_RESERVED_12 0xD: QTA_TESTBUS_RESERVED_13 0xE: QTA_TESTBUS_RESERVED_14 0xF: QTA_TESTBUS_RESERVED_15 Reset State: 0x00000000

16.2.45 rpe

0x3000000 RPE_MEM_BASE_ADDR

Type: read-write
Reset State: 0x00000000

It gives the base address of the memory where all bitmaps and related flags are stored per station and per queue basis

RPE_MEM_BASE_ADDR

Bits	Name	Description
25:0	CFG_BASEADDR	Base address for the RPE data descriptor memory Reset State: 0x00000000

0x3000004 RPE_FULLSTATE_STATIONS_QUEUES

Type: read-write
Reset State: 0x00080006

This register indicates the max number of stations we are associated with and the max number of Queues per station

RPE_FULLSTATE_STATIONS_QUEUES

Bits	Name	Description
19:16	CFG_FULLSTATE_QUEUES	Max number of Queues per station default value 8 indicates 8 queues qids 0-7 Reset State: 0x00000008
4:0	CFG_FULLSTATE_STATIONS	The number here indicates the number of stations default value 6 indicates station ids 0- 5 Reset State: 0x00000006

0x3000008 RPE_SM_STUCK_CNT_VALUE

Type: read-write
Reset State: 0x00000600

The register has the time out value used by RPE when any state machine hangs

RPE_SM_STUCK_CNT_VALUE

Bits	Name	Description
11:0	SM_STUCK_CNT_VALUE	This value indicates the timeout value in terms of number of clock cycles for riva it is 40Mhz Reset State: 0x00000600

0x300000C RPE_RPE_CONFIG

Type: read-write
Reset State: 0x60000000

gives some configurations for RPE

RPE_RPE_CONFIG

Bits	Name	Description
31:29	CMDFIFO_FULL_THRESHOLD	Value here basically determines how many entries left will indicate fifo almost full, by default it is 3 entries when cmd fifo is almost full it is indicated to RXP, so that rxp can drop the incoming packets and indicate to TPE that no ack is sent on this packet Reset State: 0x00000003
28	SET_AVERAGE_TIMESTAMP	0x0: Record current timestamp for staid/qid whenever we forward packets 1'b1: Record current/average timestamp. If reorder bitmap after forward of packets all zero then Record current time stamp. else Record timestamp = stored_time stamp + current_time stamp / 2 This helps us store timestamp closer to the queued packets in the memory Reset State: 0x00000000
27	RPE_CLEAR_COUNTERS	writing 1 will clear all counters, hardware will make it zero Reset State: 0x00000000
19:16	RPE_TESTBUS_SEL	selects different test buses in RPE 0x0: ARBITER_BLOCK 0x1: BITMAP_BLOCK 0x2: DUPLICATE_BLOCK 0x3: REASSEMBLY_BLOCK 0x4: REORDER_BLOCK 0x5: DMA_BLOCK 0x6: GBI_TESTBUS 0x7: GAM_TESTBUS 0x8: GAS_TESTBUS 0x9: REORDER_PACKET_TESTBUS 0xA: REORDER_PACKET_TESTBUS2 0xB: REORDER_BUFFER_TESTBUS2 0xC: DMA_CONTROL_TESTBUS2 0xD: ARBITER_BLOCK_TESTBUS2 0xE: COMMAND_FIFO_TESTBUS2 Reset State: 0x00000000
15	TIMER_DIS	0x1: aging timer disabled 1'b0: aging timer enabled Reset State: 0x00000000
14:8	RSRC_ENTRY_DIS	This field controls the number of resources used for fragmentation. one resource is always used. (for only 2 resources are used only bit 0 is useful here) These seven bits can be used to turn of any resource table entry for fragment gathering. Each bit indicates the resource table entry number. bit 8 is for resource table 1, resource table 0 is always on. Resource entries should be on/off sequentially only, not randomly. for example 7'b0001111 is okay 7'b0101011 is not okay Reset State: 0x00000000

RPE_RPE_CONFIG (cont.)

Bits	Name	Description
7	OUOFORD_PKT_FWD	Whenever a window moves due to one of internal flushing events (internal events described in bit field 1) then the BA bitmap does not change but reorder bitmap changes if any packets that arrive in reorder for the holes then those packets need to be forwarded when this bit is set else they are dropped 0: Drop out of order packets arriving in reorder 1: Forward out of order packets arriving in reorder Reset State: 0x00000000
6	REORDER_PKT_IN_HW_DIS	When set the actual reordering (reorder buffer support the new feature in Volans) of the packets in hardware is disabled. Note that we have per STA based control in Station descriptor also. IF this feature is disabled, the STA descriptor setting is irrelevant Reset State: 0x00000000
5	NONFRAG_FLUSH_DIS	0x1: When set resource entries for frag pkts are not flushed when non-frag packets are received for a staid/qid which has valid entry 1'b0: When non-frag pkts are received for a staid/qid which has valid resource entry then that resource is flushed Reset State: 0x00000000
4	HOST_BAR_DROP_DIS	0x1: when set then the BAR packets which have same sequence number as next expected packet will be dropped by RPE and not host 1'b0: The BAR packet which has same sequence number as next expected packet will be sent to host with opcode DROP_CUR and host will drop the packet Reset State: 0x00000000
3	BDPDU_NOTAVAIL_DROP_DIS	THis is mostly relevant fragmented packets since we create frag BD. set to 1'b1: the packets will not be dropped when bmu indicates no bdpdu is avail, then we will wait for it to be available and will not drop the packet. 1'b0: default we will drop the packets when bdpdu is not available Reset State: 0x00000000
2	REORDER_DIS	when set the hardware buffer reordering support is disabled. Reset State: 0x00000000
1	FLUSH_EVENT_FWD_MODE_SEL	This bit selects between two modes of forwarding packets dpu due to internal flushing events. These events could be that 1.polling timer expired and we found a staid/qid which is aged 2. RPE memory threshold is reached and we can not hold packets 3. software requests these packets to be forwarded 1'b0: Mode1 flushing rule is selected For the selected staid/qid bitmap all the queues packets in all slots are forwarded to DPU New SSN = old SSN + slot of last queued packet 1b1: Mode2 flushing rule is selected For the selected staid/qid bitmap find the first queued packet and forward all the queued packets till next hole Reset State: 0x00000000
0	LRU_OR_RR	This register should always be set to Zero. Initially it was reserved for LRU which was not implemented. No one should touch this register. If it is set to 1-> RPE will not work Reset State: 0x00000000

0x3000010 RPE_ROUTING_FLAG

Type: read-write
Reset State: 0x00FF0003

This register will allow you to program routing table for RPE

RPE_ROUTING_FLAG

Bits	Name	Description
23:16	ROUTING_DROP_PACKET	All the BAD (error) packets will be pushed to this WQ default value gives the DROP wq == decimal 255 -- duplicate det packets during bit map updated -- duplicate or flushing fragments -- out of order etc --... Reset State: 0x000000FF
7:0	ROUTING_GOOD_PACKET	All good packets will be forwarded to WQ programmed in this field Default WQ is DPU Reset State: 0x00000003

0x3000014 RPE_SW_FLUSH_BITMAP_CACHE

Type: read-write
Reset State: 0x00000000

This register allows software to flush the caches for full state or partial state bitmaps

RPE_SW_FLUSH_BITMAP_CACHE

Bits	Name	Description
28:24	CFG_FWD_TO_DPU_STAID	This is basically used for software controlled forward packets to DPU This field has the STAID for which the software wants to forward the packets to DPU Write the staid whose packets all need to be forwarded to DPU by also enabling bit 21 in this register Reset State: 0x00000000
23	FWD_TO_DPU_FAIL_STATUS	Whenever this bit is set that means the forward to dpu is failed due to fifo full. Writing zero to this bit will clear it if this bit is set software need to reissue fwd to DPU Reset State: 0x00000000
22	FWD_TO_DPU_DONE_STATUS	This bit indicates status when software initiated fwd to dpu. Whenever this bit is set that means the forward to dpu is done Writing zero to this bit will clear it Reset State: 0x00000000
21	CFG_FWD_TO_DPU	Enabling this bit will allow RPE to forward all the packets queued in all the slots for the staid and qid written in this register bits 19:16= qid, 26:24 staid Reset State: 0x00000000

RPE_SW_FLUSH_BITMAP_CACHE (cont.)

Bits	Name	Description
19:16	CFG_FWD_TO_DPU_QID	This is basically used for software controlled forward packets to DPU This field has the QID for which the software wants to forward the packets to DPU Write the qid whose packets all need to be forwarded to DPU. The stationid is in bits 26:24 and the enable for this Reset State: 0x00000000
4	CFG_FLUSH_PARTIALSTATE_CACHE	Writing to this will flush the bitmap maintained in the cache set to 1'b1: fullstate bitmap in the cache is written to memory after the flush H/W will invalidate the cache Reset State: 0x00000000
0	CFG_FLUSH_FULLSTATE_CACHE	Writing to this will flush the fullstate bitmap maintained in the cache set to 1'b1: fullstate bitmap in the cache is written to memory after the flush H/W will invalidate the cache Reset State: 0x00000000

0x3000018 RPE_FULLSTATE_BITMAP_CACHE_DW1

Type: read-only
Reset State: 0x00000000

When read, it gives the lower 32 bits of fullstate bitmap that is in the cache. The staid/qid of this cache is in register stationid_qid_4_fullstate_bitmap

RPE_FULLSTATE_BITMAP_CACHE_DW1

Bits	Name	Description
31:0	BITMAP_CACHE_DW1	Indicates following fields ENTRY_VAL 0 RSVD 6:1 REORDR_BUF 7 RETRY_CHK 8 FLUSH_FRAG 9 ORDR_CHK 10 FRAG_CHK 11 IEEE_2K_CHK 12 WIN_SIZE 18:13 SSN_VAL 19 SSN 31:20 Reset State: 0x00000000

0x300001C RPE_FULLSTATE_BITMAP_CACHE_DW2

Type: read-only
Reset State: 0x00000000

When read, it gives the middle 32 bits 63:32 of fullstate bitmap that is in the cache. The staid/qid of this cache is in register stationid_qid_4_fullstate_bitmap

RPE_FULLSTATE_BITMAP_CACHE_DW2

Bits	Name	Description
31:0	BITMAP_CACHE_DW2	This is the actual bitmap which shows lower 32 bits 31:0 Reset State: 0x00000000

0x3000020 RPE_FULLSTATE_BITMAP_CACHE_DW3

Type: read-only
Reset State: 0x00000000

When read, it gives the upper 32 bits 95:64 of fullstate bitmap that is in the cache. The staid/qid of this cache is in register stationid_qid_4_fullstate_bitmap

RPE_FULLSTATE_BITMAP_CACHE_DW3

Bits	Name	Description
31:0	BITMAP_CACHE_DW3	This is bitmap which shows upper 32 bits Reset State: 0x00000000

0x3000024 RPE_STATIONID_QID_4_FULLSTATE_BITMAP

Type: read-only
Reset State: 0x00000000

When read, it gives you the station/qid the above bitmap belongs to.

RPE_STATIONID_QID_4_FULLSTATE_BITMAP

Bits	Name	Description
19:16	QID_4_FULLSTATE_BITMAP	Qid for the fullstate bitmap in cache Reset State: 0x00000000
4:0	STATIONID_4_FULLSTATE_BITMAP	Station id for the fullstate bitmap in cache Reset State: 0x00000000

0x3000028 RPE_PARTIALSTATE_BITMAP_CACHE_DW1

Type: read-only
Reset State: 0x00000000

When read, it gives the lower 32 bits 31:0 of partialstate bitmap that is in the cache. The staid/qid of this cache is in register stationid_qid_4_partialstate_bitmap.

RPE_PARTIALSTATE_BITMAP_CACHE_DW1

Bits	Name	Description
31:0	BITMAP_CACHE_DW1	Indicates following fields ENTRY_VAL 0 RSVD 6:1 REORDR_BUF 7 RETRY_CHK 8 FLUSH_FRAG 9 ORDR_CHK 10 FRAG_CHK 11 IEEE_2K_CHK 12 WIN_SIZE 18:13 SSN_VAL 19 SSN 31:20 Reset State: 0x00000000

0x300002C RPE_PARTIALSTATE_BITMAP_CACHE_DW2

Type: read-only
Reset State: 0x00000000

When read, it gives the middle 32 bits 63:32 of partialstate bitmap that is in the cache. The staid/qid of this cache is in register stationid_qid_4_partialstate_bitmap.

RPE_PARTIALSTATE_BITMAP_CACHE_DW2

Bits	Name	Description
31:0	BITMAP_CACHE_DW2	This is the actual bitmap which shows lower 32 bits Reset State: 0x00000000

0x3000030 RPE_PARTIALSTATE_BITMAP_CACHE_DW3

Type: read-only
Reset State: 0x00000000

When read, it gives you upper 32 bits of partialstate bitmap.

RPE_PARTIALSTATE_BITMAP_CACHE_DW3

Bits	Name	Description
31:0	BITMAP_CACHE_DW3	This is bitmap which shows upper 32 bits Reset State: 0x00000000

0x3000034 RPE_STATIONID_QID_4_PARTIALSTATE_BITMAP

Type: read-only
Reset State: 0x00000000

When read, it gives you which station/qid the above bitmap belongs to

RPE_STATIONID_QID_4_PARTIALSTATE_BITMAP

Bits	Name	Description
19:16	QID_4_PARTIALSTATE_BITMAP	Qid for the partialstate bitmap in cache Reset State: 0x00000000
4:0	STATIONID_4_PARTIALSTATE_BITMAP	Station id for the partialstate bitmap in cache Reset State: 0x00000000

0x3000038 RPE_FRAGMENT_RESRC_ENTRY1_DW1

Type: read-only
Reset State: 0x00000000

When read, it gives you lower 32 bits of 1st resource of the 8 MPDUs maintained in RPE.

RPE_FRAGMENT_RESRC_ENTRY1_DW1

Bits	Name	Description
31:0	RESRC1_DW1	Indicates following fields ENTRY_VAL 0 STAID 8:1 QID 13:9 SSN 25:14 FRAG_NUM 29:26 LRU_ORDR 30 RSRC_ENA 31 Reset State: 0x00000000

0x300003C RPE_FRAGMENT_RESRC_ENTRY1_DW2

Type: read-only
Reset State: 0x00000000

When read, it gives you upper 32 bits of 1st resource of the 8 MPDUs maintained in RPE.

RPE_FRAGMENT_RESRC_ENTRY1_DW2

Bits	Name	Description
31:0	RESRC1_DW2	Indicates following fields BD_INDX 19:0 RSVD 31:20 Reset State: 0x00000000

0x3000040 RPE_FRAGMENT_RESRC_ENTRY2_DW1

Type: read-only
Reset State: 0x00000000

When read, it gives you lower 32 bits of 2nd resource of the 8 MPDUs maintained in RPE.

RPE_FRAGMENT_RESRC_ENTRY2_DW1

Bits	Name	Description
31:0	RESRC2_DW1	Indicates following fields ENTRY_VAL 0 STAID 8:1 QID 13:9 SSN 25:14 FRAG_NUM 29:26 LRU_ORDR 30 RSRC_ENA 31 Reset State: 0x00000000

0x3000044 RPE_FRAGMENT_RESRC_ENTRY2_DW2

Type: read-only
Reset State: 0x00000000

When read, it gives you upper 32 bits of 2nd resource of the 8 MPDUs maintained in RPE.

RPE_FRAGMENT_RESRC_ENTRY2_DW2

Bits	Name	Description
31:0	RESRC2_DW2	Indicates following fields BD_INDX 19:0 RSVD 31:20 Reset State: 0x00000000

0x3000078 RPE_ERR_INT_ENABLE

Type: read-write
Reset State: 0x00000000

This register allows you to enable any error interrupt.

RPE_ERR_INT_ENABLE

Bits	Name	Description
10	RP_SM_STUCK_ERR_INT_EN	When a 1 is written to this bit, it will enable interrupt when reorder packet state machine is hung Reset State: 0x00000000
9	REORDER_CMD_FIFO_FULL_INT_EN	When a 1 is written to this bit, it will enable interrupt whenever reorder command fifo is full Reset State: 0x00000000
8	B_2K_JUMP_SN_IN_BASESSION_INT_EN	When a 1 is written to this bit, it will enable interrupt whenever AMPDU packet is received whose SN has 2k jump Reset State: 0x00000000
7	B_2K_JUMP_SSN_IN_BAR_INT_EN	When a 1 is written to this bit, it will enable interrupt whenever BAR frame whose SSN has 2k jump Reset State: 0x00000000

RPE_ERR_INT_ENABLE (cont.)

Bits	Name	Description
6	BAR_IN_NON_BASESSION_INT_EN	When a 1 is written to this bit, it will enable interrupt whenever BAR frames are received in BA session Reset State: 0x00000000
5	FRAGPKT_IN_BASESSION_INT_EN	When a 1 is written to this bit, it will enable interrupt whenever fragmented packets are received in BA session Reset State: 0x00000000
4	BU_SM_STUCK_ERR_INT_EN	When a 1 is written to this bit, it will enable interrupt when bitmap update state machine is hung Reset State: 0x00000000
3	DD_SM_STUCK_ERR_INT_EN	When a 1 is written to this bit, it will enable interrupt when duplicate detect state machine is hung Reset State: 0x00000000
2	BMU_BD_AVAIL_ERR_INT_ENABLE	When a 1 is written to this bit, it will enable interrupt due to no available Bd/PDU in BMU Reset State: 0x00000000
1	GBI_ERR_INT_EN	When a 1 is written to this bit, it will enable interrupt due to gbi error Reset State: 0x00000000
0	GAM_ERR_INT_EN	When a 1 is written to this bit, it will enable interrupt due to gam error Reset State: 0x00000000

0x300007C RPE_ERR_INT_STATUS

Type: read-write
Reset State: 0x00000000

This register gives the status of error interrupt.

RPE_ERR_INT_STATUS

Bits	Name	Description
31:28	REASON_CODE	Gives the reason for which the above 4 BA session related interrupts have occurred 4'b0000 : No error 4'b0001 : Fragmented packets received in BA session 4'b0010 : BAR frame received in NON BA session 4'b0100 : BAR frame received with a 2k jump in SSN 4'b1000 : AMPDU frame received with 2k jump in Seq Number Reset State: 0x00000000
24:21	INT_QID	Gives QID for which above interrupt occured, if two interrupts happen one after another, the later one will overwrite the old one. Reason code will indicate which one of the interrupt was caused by this qid. Reset State: 0x00000000

RPE_ERR_INT_STATUS (cont.)

Bits	Name	Description
20:16	INT_STAID	Gives STAID of for which above interrupt occurred, if two interrupts happen one after another, the later one will overwrite the old one. Reason code will indicate which interrupt was caused by this STAID Reset State: 0x00000000
10	RP_SM_STUCK_ERR_INT_STATUS	When this bit is 1 indicates reorder packet state machine is hung, writing a 1 to this bit will clear the interrupt Reset State: 0x00000000
9	REORDER_CMD_FIFO_FULL_INT_STATUS	When this bit is set it will indicate reorder command fifo is full. Writing a 1 will clear this interrupt Reset State: 0x00000000
8	B_2K_JUMP_SN_IN_BASESSION_INT_STATUS	When this bit is set it indicates that a AMPDU packet is received whose SN has 2k jump. Writing a 1 will clear this interrupt and the reason code. Reset State: 0x00000000
7	B_2K_JUMP_SSN_IN_BAR_INT_STATUS	When this bit is set it indicates that a BAR frame is received whose SSN has 2k jump. Writing a 1 will clear this interrupt and the reason code Reset State: 0x00000000
6	BAR_IN_NON_BASESSION_INT_STATUS	When this bit is set it indicates that a BAR frame is received in a non BA session. Writing a 1 will clear this interrupt and the reason code Reset State: 0x00000000
5	FRAGPKT_IN_BASESSION_INT_STATUS	When this bit is 1 it will indicate that fragmented packets are received in BA session. Writing a 1 will clear this interrupt and the reason code Reset State: 0x00000000
4	BU_SM_STUCK_ERR_INT_STATUS	When this bit is 1 indicates bitmap update state machine is hung, writing a 1 to this bit will clear the interrupt Reset State: 0x00000000
3	DD_SM_STUCK_ERR_INT_STATUS	When this bit is 1 indicates duplicate detect state machine is hung, writing a 1 to this bit will clear the interrupt Reset State: 0x00000000
2	BMU_BD_AVAIL_ERR_INT_STATUS	When this bit is 1 indicates BMU has rUn out of BDs, writing a 1 to this bit will clear the interrupt. Reset State: 0x00000000
1	GBI_ERR_INT_STATUS	When this bit is 1 indicates gbi error interrupt has occurred, writing a 1 to this bit will clear the interrupt. Reset State: 0x00000000
0	GAM_ERR_INT_STATUS	When this bit is 1 indicates gam error interrupt has occurred, writing a 1 to this bit will clear the interrupt. Reset State: 0x00000000

0x3000080 RPE_CUR_STATE_BU_DD

Type: read-only
Reset State: 0x00010001

Gives current state of state machine bitmap update and duplicate detect. This register can be used to check the state if bit 5 or 6 in err_int_status is set.

RPE_CUR_STATE_BU_DD

Bits	Name	Description
28:16	CUR_STATE_BU	current status of bitmap update state machine Reset State: 0x00000001
7:0	CUR_STATE_DD	current status of duplicate detect state machine Reset State: 0x00000001

0x3000084 RPE_CUR_STATE_RA_RR

Type: read-only
Reset State: 0x00010001

Gives current state of state machine reassembly and reorder. This register can be used to check the state if bit 3 or 4 in err_int_status is set.

RPE_CUR_STATE_RA_RR

Bits	Name	Description
27:16	CUR_STATE_RA	current status of reassembly state machine Reset State: 0x00000001
4:0	CUR_STATE_RR	current status of reorder state machine Reset State: 0x00000001

0x3000088 RPE_CUR_STATE_DMA

Type: read-only
Reset State: 0x00010001

Gives current state of state machine DMA control. This register can be used to check the state if bit 7 in err_int_status is set.

RPE_CUR_STATE_DMA

Bits	Name	Description
22:16	CUR_STATE_RP	current status of reorder packet control state machine Reset State: 0x00000001
15:0	CUR_STATE_DMA	current status of DMA control state machine Reset State: 0x00000001

0x300008C RPE_SEND_PKT_STATS

Type: read-write
Reset State: 0x00000000

This registers gives the count of all packets sent. It rolls over after reaching max count.

RPE_SEND_PKT_STATS

Bits	Name	Description
31:0	SEND_PKT_STATS	gives stats for sent packets Reset State: 0x00000000

0x3000090 RPE_DROP_PKT_STATS

Type: read-write
Reset State: 0x00000000

This register gives the count of all packets dropped by RPE. It rolls over after reaching max count.

RPE_DROP_PKT_STATS

Bits	Name	Description
31:0	DROP_PKT_STATS	gives stats for drop packets Reset State: 0x00000000

0x3000094 RPE_GET_BMU_FAIL_STATS

Type: read-only
Reset State: 0x00000000

This registers gives statistics for how many times get bmu failed. It rolls over after reaching max count.

RPE_GET_BMU_FAIL_STATS

Bits	Name	Description
15:0	GET_BMU_FAIL_STATS	Gives stats for get bmu failures Reset State: 0x00000000

0x3000098 RPE_RPE_TESTBUS_LOWER

Type: read-only
Reset State: 0x00000000

This registers gives testbus for lower 32bits.

RPE_RPE_TESTBUS_LOWER

Bits	Name	Description
31:0	RPE_TESTBUS_LOWER	lower 32bit of the testbus (31:0) Reset State: 0x00000000

0x300009C RPE_RPE_TESTBUS_UPPER

Type: read-only
Reset State: 0x00000000

This registers gives bits 44:32 of testbus.

RPE_RPE_TESTBUS_UPPER

Bits	Name	Description
12:0	RPE_TESTBUS_UPPER	upper 13bits bits 44:32 of testbus Reset State: 0x00000000

0x3000100 RPE_RPE_BITMAP_DUPLICATE_CNTR

Type: read-only
Reset State: 0x00000000

Gives the number of bitmap updates and duplicate detect received from RXP.

RPE_RPE_BITMAP_DUPLICATE_CNTR

Bits	Name	Description
28:16	BITMAP_UPDATE_CNTR	Counter value for bitmap update and it rolls over after reaching max cnt Reset State: 0x00000000
11:0	DUPLICATE_DETECT_CNTR	Counter value for duplicate detect and it rolls over after reaching max cnt Reset State: 0x00000000

0x3000104 RPE_RPE_SW_FLUSH_RSRC_ENTRY

Type: read-write
Reset State: 0x00000000

This register allows software flush any fragment resources software can program staid and qid for which if an resource entry for reassembly exists then it needs to be flushed.

RPE_RPE_SW_FLUSH_RSRC_ENTRY

Bits	Name	Description
19:16	SW_FLUSH_RSRC_ENTRY_QUEUE	This register gives queue id along with above station for which entry needs to be flushed Reset State: 0x00000000
12:8	SW_FLUSH_RSRC_STAID	This register indicates the station for which software wants to flush any resource held for this station Reset State: 0x00000000
1	SW_FLUSH_RSRC_ENTRY_STATUS	This gives status of flush if high that means it is still ongoing when it is zero it indicates we are ready for another flush Reset State: 0x00000000
0	SW_FLUSH_RSRC_ENTRY	Writing 1 to this bit and then writing staid and qid in this same register will allow H/w to flush any resource held for this station and queue this bit is automatically cleared when flush is done Reset State: 0x00000000

0x3000108 RPE_RPE_SW_BLOCK_PKTS

Type: read-write
Reset State: 0x00000000

This register gives staid and qid for which all packets needs to be blocked. blocking means all packets to that staid/qid will be dropped If there are any packets in reorder buffer before block software needs to forward them using fwd dpu feature by sw

RPE_RPE_SW_BLOCK_PKTS

Bits	Name	Description
19:16	SW_BLOCK_QID	This register gives queue id along with above station for which packets needs to be blocked Reset State: 0x00000000
12:8	SW_BLOCK_STAID	This register indicates the station for which software wants to block any packets coming in to this station and the qid given below Reset State: 0x00000000
0	SW_BLOCK_REQ	Writing 1 to this bit and then writing staid and qid in this same register will make RPE drop any packets coming to this particular staid and qid Reset State: 0x00000000

0x300010C RPE_REORDER_BITMAP_CACHE_DW1

Type: read-only
Reset State: 0x00000000

When read, it gives the lower 32 bits of reorder bitmap.

RPE_REORDER_BITMAP_CACHE_DW1

Bits	Name	Description
31:0	REORDER_CACHE_DW1	This is the actual reorder bitmap which shows lower 32 bits Reset State: 0x00000000

0x3000110 RPE_REORDER_BITMAP_CACHE_DW2

Type: read-only
Reset State: 0x00000000

When read, it gives the middle 32 bits of reorder bitmap.

RPE_REORDER_BITMAP_CACHE_DW2

Bits	Name	Description
31:0	REORDER_CACHE_DW2	This is the actual reorder bitmap which shows upper 32 bits Reset State: 0x00000000

0x3000114 RPE_REORDER_BITMAP_CACHE_DW3

Type: read-only
Reset State: 0x00000000

When read, it gives the upper 32 bits of reorder bitmap.

RPE_REORDER_BITMAP_CACHE_DW3

Bits	Name	Description
31:0	BITMAP_CACHE_DW3	[11:0] reorder SSN [12] reorder SSN val [18:13]reorder window size [31:19] reserved Reset State: 0x00000000

0x3000120 RPE_MEMORY_THRESHOLD_FOR_RPE

Type: read-write
Reset State: 0x000DFFFF

This register contains the memory threshold value up to which RPE can hold the packets. When threshold is reached, RPE will start forwarding packets to DPU until the memory threshold value goes down.

RPE_MEMORY_THRESHOLD_FOR_RPE

Bits	Name	Description
19:18	MEMORY_UNITS	The number of pdus that are stored per packet in memory. In terms of PDUS this number can be either multiple of 128/256/512/1024, depending on what is programmed in these registers 00 - 128bytes 01 - 256 10 - 512 11 - 1024 Reset State: 0x00000003
16:0	MEMORY_THRESHOLD	Program the memory threshold (in bytes) for RPE by default this value is high so that it does not get triggered Reset State: 0x0001FFFF

0x3000124 RPE_POLLING_THRESHOLD_FOR_RPE

Type: read-write
Reset State: 0x00FFFFFF

This register contains the polling timer threshold value. Once the threshold value is reached, RPE will in a round-robin way look at the timestamp of the particular staid/qid value and compare it to one of the four aging threshold (registers below). Then all the packets held for that staid/qid are forwarded to DPU.

RPE_POLLING_THRESHOLD_FOR_RPE

Bits	Name	Description
23:0	POLLING_THRESHOLD	Program the polling threshold for RPE, this is count of number of microseconds by default this value is high so that it does not get triggered Polling timeout value is calculated as follows = Aging timeout ---------- Aging timeout is programmed in the register, stations and queues registers already exist, C is some constant number which can vary depending on number of stations and Queues By default this value is 1ms Reset State: 0x00FFFFFF

0x3000128 RPE_AGING_THRESHOLD_FOR_AC0

Type: read-write
Reset State: 0x00000000

This register contains the aging threshold value for qids that are in ac0. This is the value that tells whether the staid/qid needs to be aged out; the units are in microseconds.

RPE_AGING_THRESHOLD_FOR_AC0

Bits	Name	Description
31:0	AGING_THRESHOLD_FOR_AC0	Program the aging threshold for RPE Reset State: 0x00000000

0x300012C RPE_AGING_THRESHOLD_FOR_AC1

Type: read-write
Reset State: 0x00000000

This register contains the aging threshold value for qids that are in ac1. This is the value that tells whether the staid/qid needs to be aged out; the units are in microseconds.

RPE_AGING_THRESHOLD_FOR_AC1

Bits	Name	Description
31:0	AGING_THRESHOLD_FOR_AC1	Program the aging threshold for RPE Reset State: 0x00000000

0x3000130 RPE_AGING_THRESHOLD_FOR_AC2

Type: read-write
Reset State: 0x00000000

This register contains the aging threshold value for qids that are in ac2. This is the value that tells whether the staid/qid needs to be aged out; the units are in microseconds.

RPE_AGING_THRESHOLD_FOR_AC2

Bits	Name	Description
31:0	AGING_THRESHOLD_FOR_AC2	Program the aging threshold for RPE Reset State: 0x00000000

0x3000134 RPE_AGING_THRESHOLD_FOR_AC3

Type: read-write
Reset State: 0x00000000

This register contains the aging threshold value qids for ac3. This is the value that tells whether the staid/qid needs to be aged out; the units are in microseconds.

RPE_AGING_THRESHOLD_FOR_AC3

Bits	Name	Description
31:0	AGING_THRESHOLD_FOR_AC3	Program the aging threshold for RPE Reset State: 0x00000000

0x3000138 RPE_QID_TO_AC0_MAPPING

Type: read-write
Reset State: 0x0F0F0F0F

This register contains qid to ac0 mapping.

RPE_QID_TO_AC0_MAPPING

Bits	Name	Description
27:24	QID3_AC0_MAPPING	Program in this field the third qid, which belongs to access category 0 Reset State: 0x0000000F
19:16	QID2_AC0_MAPPING	Program in this field the third qid, which belongs to access category 0 Reset State: 0x0000000F
11:8	QID1_AC0_MAPPING	Program in this field the second qid, which belongs to access category 0 Reset State: 0x0000000F

RPE_QID_TO_AC0_MAPPING (cont.)

Bits	Name	Description
3:0	QID0_AC0_MAPPING	Program in this field the first qid, which belongs to access category 0 Reset State: 0x0000000F

0x300013C RPE_QID_TO_AC1_MAPPING

Type: read-write
Reset State: 0x0F0F0F0F

This register contains qid to ac1 mapping.

RPE_QID_TO_AC1_MAPPING

Bits	Name	Description
27:24	QID3_AC1_MAPPING	Program in this field the third qid, which belongs to access category 1 Reset State: 0x0000000F
19:16	QID2_AC1_MAPPING	Program in this field the third qid, which belongs to access category 1 Reset State: 0x0000000F
11:8	QID1_AC1_MAPPING	Program in this field the second qid, which belongs to access category 1 Reset State: 0x0000000F
3:0	QID0_AC1_MAPPING	Program in this field the first qid, which belongs to access category 1 Reset State: 0x0000000F

0x3000140 RPE_QID_TO_AC2_MAPPING

Type: read-write
Reset State: 0x0F0F0F0F

This register contains qid to ac2 mapping

RPE_QID_TO_AC2_MAPPING

Bits	Name	Description
27:24	QID3_AC2_MAPPING	Program in this field the third qid, which belongs to access category 2 Reset State: 0x0000000F

RPE_QID_TO_AC2_MAPPING (cont.)

Bits	Name	Description
19:16	QID2_AC2_MAPPING	Program in this field the third qid, which belongs to access category 2 Reset State: 0x0000000F
11:8	QID1_AC2_MAPPING	Program in this field the second qid, which belongs to access category 2 Reset State: 0x0000000F
3:0	QID0_AC2_MAPPING	Program in this field the first qid which belongs to access category 2 Reset State: 0x0000000F

0x3000144 RPE_QID_TO_AC3_MAPPING

Type: read-write
Reset State: 0x0F0F0F0F

This register contains qid to ac3 mapping.

RPE_QID_TO_AC3_MAPPING

Bits	Name	Description
27:24	QID3_AC3_MAPPING	Program in this field the third qid, which belongs to access category 3 Reset State: 0x0000000F
19:16	QID2_AC3_MAPPING	Program in this field the third qid, which belongs to access category 3 Reset State: 0x0000000F
11:8	QID1_AC3_MAPPING	Program in this field the second qid, which belongs to access category 3 Reset State: 0x0000000F
3:0	QID0_AC3_MAPPING	Program in this field the first qid, which belongs to access category 3 Reset State: 0x0000000F

0x3000148 RPE_RPE_MEM_BYTES_USED

Type: read-only
Reset State: 0x00000000

This register will give the amount of memory used by RPE in bytes.

RPE_RPE_MEM_BYTES_USED

Bits	Name	Description
16:0	RPE_MEM_BYTES_USED	when RPE does reordering it may have to hold some packets in the memory this register gives the total memory used in bytes Reset State: 0x00000000

0x300014C RPE_FWD_TO_DPU_EVENT_PKT_STATS

Type: read-only
Reset State: 0x00000000

This register gives count of all packets forwarded by RPE due to internal events like aging, mem threshold reached and software request. It rolls over after reaching max count.

RPE_FWD_TO_DPU_EVENT_PKT_STATS

Bits	Name	Description
15:0	FWD_TO_DPU_EVENT_PKT_STATS	gives stats for packets forwarded to DPU due to internal events Reset State: 0x00000000

0x3000150 RPE_SPARE_AND_CLK_GATE_DISABLE

Type: read-write
Reset State: 0x00000000

This register has some spare bits and local clock gating disable bits

RPE_SPARE_AND_CLK_GATE_DISABLE

Bits	Name	Description
23:16	SPARE_BITS	read writable spare bits Reset State: 0x00000000
7:0	LOCAL_CLK_GATE_DISABLE	local clock gate disable bit0: config module bit1: duplicate_detect and arbiter module bit 2 : bitmap_update bit 3 : dma_control bit 4 : reassembly bit 5 : command_fifo bit 6 : reorder_packet bit 7 : reorder_buffer Reset State: 0x00000000

16.2.46 rxp

0x3000000 RXP_CONFIG

Type: read-write
Reset State: 0x00000100

It contains RXP Configuration registers. These configurations (with the exception of soft abort and mask_subsq_fcs_err_within_ampdu) can be changed at any time by software, but hardware will take effect only during the gap of packets so that software will not corrupt packets during configuration.

RXP_CONFIG

Bits	Name	Description
15	CFG_RESERVED	These are reserved for future configuration. Reset State: 0x00000000
14	CFG_MPR_DISABLE_WAIT_FOR_FILTER_IDLE	When set, this will disable the 'wait for filter to finish, when eop is received' function. This is a bug fix. This configuration bit will allow the bug fix to be disabled and the rxp logic to be reverted to the original implementation. This allows for backwards compatibility. Reset State: 0x00000000
13	RRI_CLEAR_ON_FCS_FAIL	If set, this will enable RRI regeneration when the first RRI got followed by and FCS err. Reset State: 0x00000000
12	MASK_SUBSQ_FCS_ERR_WITHIN_AMPDU	If set, this will mask out fcs error notification to the MTU after an MPDU within an AMPDU passes FCS check. This is to prevent doing EIFS in this case. Reset State: 0x00000000
11	SOFT_PMI_ABORT_EN	Soft PMI abort enable. Reset State: 0x00000000
10	CFG_HAS_FCS_EN	If set, RXP will enable writing 4-byte fcs into BD/PDU and RXP flag has_fcs flag will be set to 1. By default, the RXP DMA will NOT write fcs into BD/PDU and MPDU length does not include the 4-byte fcs. Reset State: 0x00000000
9	CFG_RSV_BMU_EN	If set, RXP will enable sending reservation command to BMU. By default, the RXP DMA will NOT send reservation command to BMU at start of packet. Reset State: 0x00000000
8	CFG_HAS_PHY_CMD	If set, RXP will write PHY Command into BD. By default, the PHY Command will not be put into BD so that software can adjust the "mpdu_header_start_offset" to save the BD space for MPDU data. Note that the TimeStamp will be in BD in any case. Reset State: 0x00000001

RXP_CONFIG (cont.)

Bits	Name	Description
7	CFG_HAS_DLM	This is not implemented! If set, the Delimiter of A-MPDU packet will be treated as part of MPDU and be written into BD starting at "MPDU header start offset". This is used to preserve and write Delimiter into BD after Delimiter processing. By default, the Delimiter is consumed by Delimiter Processing and will not be written into BD. Reset State: 0x00000000
6	CFG_DISABLE_DLM_PROC	If set to disable, the Delimiter Processing is disabled for A-MPDU packets and the whole A-MPDU packet will be sent to mCPU without MPDU Processing. The byp_dlm_proc and byp_mpdu_proc will be asserted for A-MPDU packets. By default, Delimiter Processing is enabled. Note: This cfg_disable_dlm_proc will affect only A-MPDU packets, but not MPDU packets. Reset State: 0x00000000
5	CFG_DISABLE_MPDU_PROC	If set to disable, the MPDU Processing is disabled for MPDU packets and the MPDU packets will be sent to mCPU without MPDU processing. This means NO FCS check, NO address filtering, and NO binary search. The packets are assumed passing MPDU processing. By default, MPDU Prcessing is enabled. Note: This cfg_disable_mpdu_proc will affect only MPDU packets, but not A-MPDU packets. This means MPDU within A-MPDU will be processed normally (without bypass) if cfg_disable_dlm_proc is not asserted for A-MPDU packets. Reset State: 0x00000000
4	CFG_DISABLE_FCS_CHECK	If set to disable, the FCS Check is disabled and all packets will be treated as passing FCS Check. By default, it is enabled and RXP will check FCS on MPDU packets. The counter associated with this config is fcs_err_cnt. If not disabled, this counter will increment if a packet has FCS error. Reset State: 0x00000000
3	CFG_MAX_PKTLEN_CHECK_EN	The max packet length check enable bit. By default, the max_pktlen check is disabled. If set, it will check MPDU packet length against max_pktlen register and check A-MPDU packet length against max_len_ampdu register. But it will not affect max_len_mpdu_in_ampdu which is checked in delimiter processing and can be disabled by asserting cfg_disable_dlm_proc. Reset State: 0x00000000
2	CFG_ADDR_FILTER_EN	If set, the Address Filter will be enabled. By default, it is disabled and all packets will be treated as passing Address Filtering. Reset State: 0x00000000
1	CFG_GEN_SHUTOFF_EN	If set, RXP will generate shutoff signal to PHY. By default, it will NOT generate shutoff signal. If shutoff is generated to PHY, PHY will stop receiving the current packet. This is used to save power. Reset State: 0x00000000

RXP_CONFIG (cont.)

Bits	Name	Description
0	CFG_RXP_EN	If enabled, RXP will receive packets from PHY. By default, the RXP is disabled and will not receive any packet from PHY. This bit can be changed at any time, but will only take effect when there is start pulse from PHY. Reset State: 0x00000000

0x3000008 RXP_MAX_PKTLEN

Type: read-write
Reset State: 0x00000040

The Max MPDU Packet Length in terms of the number bytes. It includes mac_header+payload+fcs, but does not include PHY data.

RXP_MAX_PKTLEN

Bits	Name	Description
6:0	MAX_PKTLEN	The Max MPDU Packet Length in terms of the number 128 bytes. Reset State: 0x00000040

0x300000C RXP_ROUTING_FLAG

Type: read-write
Reset State: 0x00000000

The Routing flag in BD.

RXP_ROUTING_FLAG

Bits	Name	Description
16:11	ROUTING_FLAG	This register is used to fill the reserved bits in the first Dword of the RxBD This location matches the reserved bits in first Dword, Software mainly uses this Reset State: 0x00000000

0x3000010 RXP_MPDU_HEADER_START_OFFSET

Type: read-write
Reset State: 0x00000040

The MPDU header start offset in BD, which is in the unit of data word (4-byte).

RXP_MPDU_HEADER_START_OFFSET

Bits	Name	Description
7:2	MPDU_HEADER_START_OFFSET	MPDU header start offset in BD. Note that the programmable bits are [7:2] and the lower [1:0] bits are always 2'b00 to guarantee the offset address is 4-byte aligned. If bit[7] is 0, the MPDU header starts at BD, but if bit[7] is 1, the MPDU header starts at PDU. Note that It is not valid to have the value of 6'h3f for bit[7:2] (or 8'hfc for bit[7:0]). The default value is 6'ha which means the offset address of 8'h28. In this case, the PHY Cmd bytes will not be written in BD so that the MPDU header can start right after TimeStamp field. However, for diagnostic purpose, the PHY Cmd can be written into BD by setting cfg_has_phy_cmd bit in config register so that this offset value will be adjusted to 6'h10 which means the offset address of 8'h40. Reset State: 0x00000010

0x300002C RXP_SEARCH_ADDR1_PTR

Type: read-write
Reset State: 0x00000000

SW can set the addr1 pointers of Binary Search.

RXP_SEARCH_ADDR1_PTR

Bits	Name	Description
16	ADDR1_POINTERS_VALID	When set, the pointers are valid. Reset State: 0x00000000
12:8	ADDR1_SEARCH_HI_PTR	Indicate the addr1 pointer of Binary Search upper bound. Reset State: 0x00000000
4:0	ADDR1_SEARCH_LO_PTR	Indicate the addr1 pointer of Binary Search lower bound. Reset State: 0x00000000

0x3000030 RXP_SEARCH_ADDR2_PTR

Type: read-write
Reset State: 0x00000000

SW can set the addr2 pointers of Binary Search.

RXP_SEARCH_ADDR2_PTR

Bits	Name	Description
16	ADDR2_POINTERS_VALID	When set, the pointers are valid. Reset State: 0x00000000
12:8	ADDR2_SEARCH_HI_PTR	Indicate the addr2 pointer of Binary Search upper bound. Reset State: 0x00000000
4:0	ADDR2_SEARCH_LO_PTR	Indicate the addr2 pointer of Binary Search lower bound. Reset State: 0x00000000

0x3000034 RXP_SEARCH_ADDR3_PTR

Type: read-write
Reset State: 0x00000000

SW can set the addr3 pointers of Binary Search.

RXP_SEARCH_ADDR3_PTR

Bits	Name	Description
16	ADDR3_POINTERS_VALID	When set, the pointers are valid. Reset State: 0x00000000
12:8	ADDR3_SEARCH_HI_PTR	Indicate the addr3 pointer of Binary Search upper bound. Reset State: 0x00000000
4:0	ADDR3_SEARCH_LO_PTR	Indicate the addr3 pointer of Binary Search lower bound. Reset State: 0x00000000

0x3000038 RXP_SEARCH_TABLE_CMD

Type: read-write
Reset State: 0x00000000

This is action register for indirect access to Binary Search Table. When software writes to this action register, it will trigger the interaction between Search_Table_Data[0-1] registers and Binary Search Table. For writing data into memory table, it is important for software to write into Search_Table_Data[0-1] registers before Search_Table_Cmd. For reading data from memory table, software only needs to write into Search_Table_Cmd and the read data will be available in Search_Table_Data[0-1] registers.

RXP_SEARCH_TABLE_CMD

Bits	Name	Description
9	STATUS	read only: If set to 1 a binary search table read or write is ongoing. Software should read and make sure this bit is 0 before issuing another cmd write into this register. Reset State: 0x00000000
8	WRITE	Indicate write/read. If 1, write. If 0, read. Reset State: 0x00000000
4:0	TABLE_PTR	Indicate the action should take effect on this entry number in Binary Search Table. Reset State: 0x00000000

0x300003C RXP_SEARCH_TABLE_DATA0

Type: read-write
Reset State: 0x00000000

This is data register 0 for indirect access to Binary Search Table. There are totally 3 Data registers for Binary Search address Table.

RXP_SEARCH_TABLE_DATA0

Bits	Name	Description
31:0	MAC_ADDR	MAC_Addr[31:0] portion of MAC_Addr[47:0]. Note: The order is Little Endian: MAC_Addr[31:0] = {Byte_3, Byte_2, Byte_1, Byte_0} Reset State: 0x00000000

0x3000040 RXP_SEARCH_TABLE_DATA1

Type: read-write
Reset State: 0x00000000

This is data register 1 for indirect access to Binary Search Table. There are totally 3 Data registers for Binary Search address Table.

RXP_SEARCH_TABLE_DATA1

Bits	Name	Description
31:29	DPU_MAN_MC_BC_SIG	This field is used to configure the DPU signature for Management mc/bc packets Reset State: 0x00000000
28	RSVD	reserved for future use Reset State: 0x00000000

RXP_SEARCH_TABLE_DATA1 (cont.)

Bits	Name	Description
27	VALID	Set when the sta address is valid Reset State: 0x00000000
26	RMF	Set when robust management frames require BIP or decryption Reset State: 0x00000000
25	FRAME_TRANSLATION	This bit is used to decide if a per station frame translation is required. When this bit is set and the bit in type/subtype is set then those packets for that station will require frame translation, so FT bit in BD will be set Reset State: 0x00000000
24	DROP	When set, on a address hit, the frame will be dropped. The setting of this bit is only valid when 'valid configuration' is set Reset State: 0x00000000
23:16	ADDR_ID	The addr_id[7:0]. Reset State: 0x00000000
15:0	MAC_ADDR	MAC_Addr[47:32] portion of MAC_Addr[47:0]. Note: The order is Little Endian: MAC_Addr[47:32] = {Byte_5, Byte_4} Reset State: 0x00000000

0x3000044 RXP_MAX_LEN_AMPDU

Type: read-write
Reset State: 0x0000FFFF

The Max Length for A-MPDU packet.

RXP_MAX_LEN_AMPDU

Bits	Name	Description
16:0	MAX_LEN	The Max Length for A-MPDU packet. Reset State: 0x0000FFFF

0x3000048 RXP_MAX_LEN_MPDU_IN_AMPDU

Type: read-write
Reset State: 0x00000FFF

The Max Length for MPDU in A-MPDU packet. This is used for delimiter processing to determine whether it finds a good delimiter.

RXP_MAX_LEN_MPDU_IN_AMPDU

Bits	Name	Description
13:0	MAX_LEN	The Max Length for MPDU in A-MPDU packet. Reset State: 0x00000FFF

0x300004C RXP_DMA_MAX_RSV_PDU

Type: read-write
Reset State: 0x00000008

The Max number of PDUs that RXP DMA can reserve at a time. The is to avoid the scenario that RXP drop big packet just because it fails to reserve a huge number of PDUs at the start of the packet.

RXP_DMA_MAX_RSV_PDU

Bits	Name	Description
3:0	MAX_RSV_PDU	The Max number of PDUs that RXP DMA can reserve at a time. Reset State: 0x00000008

0x3000050 RXP_DMA_BURST_THRESHOLD

Type: read-write
Reset State: 0x00000008

The data word threshold that RXP DMA control can start burst MPDU data to MIF. The data unit is 1 word (or 4 bytes). By default, the threshold is 8 words (or 32 bytes). RXP MPDU data is accumulated in DMA FIFO. The DMA control will not send data to MIF if the number of data word in DMA FIFO does not reach the threshold. This is to used to control the burstness of RXP data on AHB.

RXP_DMA_BURST_THRESHOLD

Bits	Name	Description
5:0	BURST_THRESHOLD	The data word threshold that DMA can start burst MPDU data to MIF. Reset State: 0x00000008

0x3000054 RXP_CLEAR_STATS

Type: read-write
Reset State: 0x00000000

This register is used to clear all stats.

RXP_CLEAR_STATS

Bits	Name	Description
0	CLEAR_STATS	When set, all statistics counters will be cleared When set, the hardware will automatically clear this bit. Reset State: 0x00000000

0x3000058 RXP_PHY_MPDU_CNT

Type: read-only
Reset State: 0x00000000

The number of MPDU packets that are received from PHY.

RXP_PHY_MPDU_CNT

Bits	Name	Description
31:0	PHY_MPDU_CNT	PHY MPDU Cnt. Reset State: 0x00000000

0x300005C RXP_PHY_AMPDU_CNT

Type: read-only
Reset State: 0x00000000

The number of A-MPDU packets that are received from PHY.

RXP_PHY_AMPDU_CNT

Bits	Name	Description
31:0	PHY_AMPDU_CNT	PHY A-MPDU Cnt. Reset State: 0x00000000

0x3000064 RXP_PHY_ABORT_CNT

Type: read-only
Reset State: 0x00000000

The number of aborted packets from PHY.

RXP_PHY_ABORT_CNT

Bits	Name	Description
7:0	PHY_ABORT_CNT	PHY Abort Packet Cnt. Reset State: 0x00000000

0x3000068 RXP_PHY_SHUTOFF_CNT

Type: read-only
Reset State: 0x00000000

The number of shutoff pulses that are generated by RXP to PHY.

RXP_PHY_SHUTOFF_CNT

Bits	Name	Description
7:0	PHY_SHUTOFF_CNT	PHY Shutoff Cnt. Reset State: 0x00000000

0x300006C RXP_DLM_FIFO_FULL_CNT

Type: read-only
Reset State: 0x00000000

The number of packets that have an error because DLM FIFO is full.

RXP_DLM_FIFO_FULL_CNT

Bits	Name	Description
7:0	DLM_FIFO_FULL_CNT	DLM FIFO Full Cnt. Reset State: 0x00000000

0x3000070 RXP_DLM_ERR_CNT

Type: read-only
Reset State: 0x00000000

The number of packets have error because Delimiter is bad. When a error is detected in the A-MPDU delimiter this count is incremented. But when RXP starts searching for the next A-MPDU delimiter, this count is NOT incremented. The implementation uses 'seen_dlm_err' flag. This flag is cleared for the first delimiter or after a good delimiter is found. It is set after a bad delimiter is found. If this flag is set, then don't increment the counter. This will increment whenever the next delimiter (using the previous good delimiter information) is not found in the expected location, or is bad.

RXP_DLM_ERR_CNT

Bits	Name	Description
7:0	DLM_ERR_CNT	DLM Error Cnt. Reset State: 0x00000000

0x3000074 RXP_FAIL_FILTER_CNT

Type: read-only
Reset State: 0x00000000

The number of packets that failed Address Filtering.

RXP_FAIL_FILTER_CNT

Bits	Name	Description
15:0	FAIL_FILTER_CNT	Fail Address Filter Cnt. Reset State: 0x00000000

0x3000078 RXP_FAIL_MAX_PKTLEN_CNT

Type: read-only
Reset State: 0x00000000

The number of packets that failed Max MPDU or AMPDU packet length check.

RXP_FAIL_MAX_PKTLEN_CNT

Bits	Name	Description
7:0	FAIL_MAX_PKTLEN_CNT	Fail Max MPDU or AMPDU Packet Length Check Cnt. Reset State: 0x00000000

0x300007C RXP_FCS_ERR_CNT

Type: read-only
Reset State: 0x00000000

The number of packets with FCS error.

RXP_FCS_ERR_CNT

Bits	Name	Description
31:0	FCS_ERR_CNT	FCS Error Cnt. Reset State: 0x00000000

0x3000080 RXP_DMA_SEND_CNT

Type: read-only
Reset State: 0x00000000

The number of packets sent to CPU by RXP Write DMA.

RXP_DMA_SEND_CNT

Bits	Name	Description
31:0	DMA_SEND_CNT	The number of packets are sent to CPU by RXP Write DMA. All packets in current system are all pushed by RXp refer to rpe dma send cnt for that. This counter increments only if RXP pushes packets directly to DXE Reset State: 0x00000000

0x3000084 RXP_DMA_DROP_CNT

Type: read-only
Reset State: 0x00000000

The number of packets are dropped by RXP Write DMA. This could increment due to: Failed filter PHY Abort AFTER the 9th command word BD/PDU errors If packet with command phase shorter or longer than actual command length specified is sent, the RXP will increment dma_drop_cnt instead of phy_err_drop_cnt (unless actual command phase < 9 words, in which case phy_err_drop_cnt will be incremented) Will NOT increment if end of psdu (as defined in psdu length by PHY command) occurs during search for next delimiter in AMPDU; this is because a new packet is not found, so there should not be a drop)

RXP_DMA_DROP_CNT

Bits	Name	Description
15:0	DMA_DROP_CNT	The number of packets are dropped by RXP Write DMA. Drop due to filter error, packet len error or Get bmu error any packet dropped at DMA due to any of above errors, these can be drop at DMA marked packets which may have filter fail errors Reset State: 0x00000000

0x3000088 RXP_DMA_GET_BMU_FAIL_CNT

Type: read-only
Reset State: 0x00000000

The number of packets dropped due to insufficient BD/PDUs BMU BD or PDU.

RXP_DMA_GET_BMU_FAIL_CNT

Bits	Name	Description
15:0	DMA_GET_BMU_FAIL_CNT	DMA No BMU BD/PDU Cnt. Reset State: 0x00000000

0x300008C RXP_PROTOCOL_VERSION_FILTER_CNT

Type: read-only
Reset State: 0x00000000

The number of packets dropped because of protocol version error.

RXP_PROTOCOL_VERSION_FILTER_CNT

Bits	Name	Description
7:0	DROPPED_COUNT	number of frames dropped Reset State: 0x00000000

0x3000090 RXP_TYPE_SUBTYPE_FILTER_CNT

Type: read-only
Reset State: 0x00000000

The number of packets dropped because of their type/subtype

RXP_TYPE_SUBTYPE_FILTER_CNT

Bits	Name	Description
7:0	DROPPED_COUNT	number of frames dropped Reset State: 0x00000000

0x3000094 RXP_INCORRECT_LENGTH_FILTER_CNT

Type: read-only
Reset State: 0x00000000

The length of the frame was not sufficient to do all the address filter checks. This may increment if dlm_fifo_full occurs.

RXP_INCORRECT_LENGTH_FILTER_CNT

Bits	Name	Description
7:0	DROPPED_COUNT	number of frames dropped Reset State: 0x00000000

0x3000098 RXP_ADDR1_BLOCK_FILTER_CNT

Type: read-only
Reset State: 0x00000000

Number of frames blocked based on the address one

RXP_ADDR1_BLOCK_FILTER_CNT

Bits	Name	Description
7:0	DROPPED_COUNT	number of frames dropped Reset State: 0x00000000

0x300009C RXP_ADDR1_HIT_NO_PASS_CNT

Type: read-only
Reset State: 0x00000000

Number of frames that got a hit in the binary search table but were instructed to be dropped because of the drop setting in the binary search table

RXP_ADDR1_HIT_NO_PASS_CNT

Bits	Name	Description
7:0	DROPPED_COUNT	number of frames dropped Reset State: 0x00000000

0x30000A0 RXP_ADDR1_DROP_CNT

Type: read-only
Reset State: 0x00000000

Number of frames that got dropped because there was no hit in the binary search table

RXP_ADDR1_DROP_CNT

Bits	Name	Description
7:0	DROPPED_COUNT	number of frames dropped Reset State: 0x00000000

0x30000A4 RXP_ADDR2_HIT_NO_PASS_CNT

Type: read-only
Reset State: 0x00000000

Number of frames that got a hit in the binary search table but were instructed to be dropped because of the drop setting in the binary search table

RXP_ADDR2_HIT_NO_PASS_CNT

Bits	Name	Description
7:0	DROPPED_COUNT	number of frames dropped Reset State: 0x00000000

0x30000A8 RXP_ADDR2_DROP_CNT

Type: read-only
Reset State: 0x00000000

Number of frames that got dropped because there was no hit in the binary search table

RXP_ADDR2_DROP_CNT

Bits	Name	Description
7:0	DROPPED_COUNT	number of frames dropped Reset State: 0x00000000

0x30000AC RXP_ADDR3_HIT_NO_PASS_CNT

Type: read-only
Reset State: 0x00000000

Number of frames that got a hit in the binary search table but were instructed to be dropped because of the drop setting in the binary search table

RXP_ADDR3_HIT_NO_PASS_CNT

Bits	Name	Description
7:0	DROPPED_COUNT	number of frames dropped Reset State: 0x00000000

0x30000B0 RXP_ADDR3_DROP_CNT

Type: read-only
Reset State: 0x00000000

Number of frames that got dropped because there was no hit in the binary search table

RXP_ADDR3_DROP_CNT

Bits	Name	Description
7:0	DROPPED_COUNT	number of frames dropped Reset State: 0x00000000

0x30000B4 RXP_MPDU_IN_AMPDU_CNT

Type: read-only
Reset State: 0x00000000

The number of MPDU packets are split from A-MPDU packets.

RXP_MPDU_IN_AMPDU_CNT

Bits	Name	Description
31:0	MPDU_IN_AMPDU_CNT	The number of MPDU packets are split from A-MPDU packets. Reset State: 0x00000000

0x30000B8 RXP_PHY_ERR_DROP_CNT

Type: read-only
Reset State: 0x00000000

The number of packets are dropped by RXP PHY Processing because of some apparent PHY protocol errors, such as: PHY Cmd Len is smaller than 9 bytes. PHY Cmd Len is larger than 28 bytes. PHY Stats Len is not equal to 8 bytes. Exception - if packet with command phase shorter longer than actual command length is sent, the RXP will increment dma_drop_cnt instead (however, if actual command length is < 9, this will be counted as a phy_err_drop) Note: The packets are dropped before reaching RXP Write DMA.

RXP_PHY_ERR_DROP_CNT

Bits	Name	Description
7:0	PHY_ERR_DROP_CNT	The number of packets are dropped by RXP PHY Processing. Reset State: 0x00000000

0x30000BC RXP_RADAR_DETECT_STATUS

Type: read-write
Reset State: 0x00000000

Radar detect status register. Pointers in radar detect circular buffer. Equal pointers means that the buffer is empty. There can be 0-63 entries in this circular buffer.

RXP_RADAR_DETECT_STATUS

Bits	Name	Description
24	RDR_DETECT_INT	status of the radar detect interrupt signal Reset State: 0x00000000
21:16	NR_ENTRIES	Number of entries filled in radar detect circular buffer. (0-63) Reset State: 0x00000000
13:8	TAIL_PTR	tail pointer of radar detect circular buffer Reset State: 0x00000000
5:0	HEAD_PTR	head pointer of radar detect circular buffer Reset State: 0x00000000

0x30000C0 RXP_RADAR_DETECT_CONTROL

Type: read-write
Reset State: 0x00000000

Radar detect control register.

RXP_RADAR_DETECT_CONTROL

Bits	Name	Description
8	RADAR_DETECT_ENABLE	Enable/disable storing of radar detect logs Reset State: 0x00000000
5:0	MIN_NR_LOGS_GEN_INT	Minimum number of stored logs to generate radar detect interrupt. 0 is a special case, which means to disable the interrupt. Reset State: 0x00000000

0x30000C4 RXP_RADAR_DETECT_LLOGS

Type: read-write
Reset State: 0x00000000

Radar detect lower word register.

RXP_RADAR_DETECT_LLOGS

Bits	Name	Description
31:0	RADAR_DETECT_LDATA	On read, the lower 4 bytes from the radar detect log as pointed by the tail pointer is returned. On write, the lower 4 bytes are written into the location pointed by the head pointer. Reset State: 0x00000000

0x30000C8 RXP_RADAR_DETECT_ULOGS

Type: read-write
Reset State: 0x00000000

Radar detect upper word register.

RXP_RADAR_DETECT_ULOGS

Bits	Name	Description
31:0	RADAR_DETECT_UDATA	On read, the lower 4 bytes from the radar detect log as pointed by the tail pointer is returned. After the read, the tail pointer is increased by one, except if that would cause it to become greater than the head pointer. On write, the lower 4 bytes are written into the location pointed by the head pointer. After the write, the head pointer is increased by one. If this would cause the head pointer to become equal to the tail pointer, the tail pointer would also be incremented. Reset State: 0x00000000

0x30000CC RXP_RADAR_DETECT_LOGS

Type: read-write
Reset State: 0x00000000

Radar detect logs counter register

RXP_RADAR_DETECT_LOGS

Bits	Name	Description
31	RADAR_DETECT_LOGS_CNT_CLEAR	When set, clears count of PHY written radar detect logs. This bit will automatically be cleared by HW. Reset State: 0x00000000
15:0	RADAR_DETECT_LOGS_CNT	Number of radar detect logs received from PHY. Reset State: 0x00000000

0x30000D0 RXP_SOFT_PMI_ABORT

Type: read-write
Reset State: 0x00000000

Soft PMI Abort register

RXP_SOFT_PMI_ABORT

Bits	Name	Description
0	SOFT_PMI_ABORT	Write only bit; when 1 is written to this bit, and soft_pmi_abort_en is 1, then a soft PHY abort will be generated. Error counters will be incremented as if an actual abort had occurred. Reset State: 0x00000000

0x30000D4 RXP_START_ERR_CNT

Type: read-only
Reset State: 0x00000000

The number of start errors on the PMI interface (pmi_rxp_starts received while still waiting for previous packet to complete).

RXP_START_ERR_CNT

Bits	Name	Description
7:0	PHY_START_ERR_CNT	PHY Start Error Cnt. Reset State: 0x00000000

0x30000D8 RXP_CCA_AND_EXT_TIMEOUT

Type: read-write
Reset State: 0x3C064090

Configuration bits for cca extensions and timeout functionality.

RXP_CCA_AND_EXT_TIMEOUT

Bits	Name	Description
31:21	CCA_PKTDET_6US_EXT_VALUE	THis is extension of packet detect, which is done only for 11b packets for 80Mhz clock : 11'd480 for 160Mhz clock : 11'd960 for 320Mhz clock : 11'd1920 Reset State: 0x000001E0
20:10	CCA_PKTDET_EXT_VALUE	THis is an additional extension of packet detect, if this is not needed it should be programmed to 1, otherwise hardware will use the default value of 11'd400 80Mhz clocks 80Hmz clock : 11'd400 160Mhz clock: 11'd800 320Mhz clock: 11'd1600. Reset State: 0x00000190
9	CCA_PKDET_EXTENTION_ALLOWED	when set it allows for 6us extension on ofdm packets Reset State: 0x00000000
8:4	FLT_TIMEOUT_TIME	This value represent that maximum time (in 256 OR 4096 120MHz clk cycle units) that the rxp filter will wait for two sequential MPDU header bytes to be received. If this time is not met, the rxp filter will drop the frame by indicating that the filter is done, but the frame does not pass the filter. The 'timeout_error_cnt' register contents will increase by 1. Reset State: 0x00000009
2	CCA_PKDET_EXTENTION_OLDLOGIC_DIS	when packet det gets de-asserted 5us extension is done, and at the end of 5us we look for command byte 6 for packet type whether it is ofdm and then do 6us additional extension. But PHY may not always give this info within 5us hence ofdm signal is used for this (which is the new logic). This logic is only enabled when you write 1 to this bit. Reset State: 0x00000000
1	FLT_TIMOUT_COUNT_UNIT	When clear, the timeout will count in 256 clk cycle units When set, the timeout counter will count in 4096 clk cycle units Reset State: 0x00000000
0	FLT_TIMEOUT_CHECK_DISABLED	When set, the rxp filter timeout check is disabled Reset State: 0x00000000

0x30000DC RXP_TIMEOUT_ERROR_CNT

Type: read-only
Reset State: 0x00000000

Number of times the rxp filter encounters a timeout As a result of this, the frame will be dropped

RXP_TIMEOUT_ERROR_CNT

Bits	Name	Description
7:0	TIMEOUT_COUNT	Number of times the rxp filter encounters a timeout Reset State: 0x00000000

0x30000E0 RXP_STALL_TIMEOUT_CNT

Type: read-only
Reset State: 0x00000000

Number of times stall timeout occurs. As a result of this, the frame will be dropped

RXP_STALL_TIMEOUT_CNT

Bits	Name	Description
7:0	STALL_TIMEOUT_COUNT	Number of times the PMI interface encounters a stall timeout Reset State: 0x00000000

0x30000EC RXP_CFG_FLT_NAV_CONTROL_RESPONSE_REQ

Type: read-write
Reset State: 0x00000000

NAV control register and response requested register. The NAV PHY delay compensation can be programmed here. Also the control of how the NAV needs to be updated, or not at all, when the CCA was not asserted when a frame got received (and dropped) is configured here.

RXP_CFG_FLT_NAV_CONTROL_RESPONSE_REQ

Bits	Name	Description
25	CFG_FLT_RESPONSE_REQ_WITH_HT_CONTROL	When set and the Response interrupt is generated, and the incoming frame has an HT control field (this is: incoming frame is QoS data frame and has the 'order' bit in the frame control field set), the response interrupt is only generated after the HT control field has been fully received and will be located in the reponse_header_info5 field. Setting this bit will also enable the generation of the 'HTC present' reporting in the enhanced_sequence_number_message_type Reset State: 0x00000000
24:21	CFG_FLT_NAV_RESERVED	reserved bits Reset State: 0x00000000
20	CFG_FLT_NAV_DELAY_COMPENSATION_VALUE_EN	When set, enables the NAV delay compensation functionality. This is, the NAV update value given to the MTU is compensated for the PHY delay. The compensation value is given in the bits: cfg_flt_nav_delay_compensation_value Reset State: 0x00000000
19:16	CFG_FLT_NAV_DELAY_COMPENSATION_VALUE	NAV compensation value in microseconds. Reset State: 0x00000000

RXP_CFG_FLT_NAV_CONTROL_RESPONSE_REQ (cont.)

Bits	Name	Description
10	CFG_FLT_REGISTER_CCA_AT_START_OF_OBSERVE_TIME	When NOT set: no action When set: The RXP filter samples the setting of the primary cca signal at the start of the cca observe time. This sampled CCA is later used to determine if an NAV update is needed or NOT. The cca observe time is configured with other bits in this register. Reset State: 0x00000000
9	CFG_FLT_REGISTER_CCA_AT_END_OF_OBSERVE_TIME	When NOT set: no action When set: The RXP filter samples the setting of the primary cca signal at the end of the cca observe time. This sampled CCA is later used to determine if an NAV update is needed or NOT. The cca observe time is configured with other bits in this register. Reset State: 0x00000000
8	CFG_FLT_REGISTER_CCA_DURING_OBSERVE_TIME	When NOT set: no action When set: The RXP filter samples the setting of the primary cca signal during the entire duration of the cca observe time. If the cca goes low anywhere during this time, this is recorded and fixed. In that case, even if the CCA went high a little later, the sampled CCA value that is later used to determine if an NAV update is needed or NOT, will have a low value. The cca observe time is configured with other bits in this register. Reset State: 0x00000000
7	CFG_FLT_REGISTER_CCA_LEVEL_DURING_DATA_TIME	When NOT set: no action When set: The 'data reception time' as indicated by pktdet_n being low, is part of the cca observe time. Reset State: 0x00000000
6	CFG_FLT_REGISTER_CCA_LEVEL_DURING_PREAMBLE_TIME	When NOT set: no action When set: The 'data reception time as determined by early_pktdet_n being low, is part of the cca observe time. Reset State: 0x00000000
5	CFG_FLT_SKIP_DIFS_WHEN_NAV_UPDATE_MASKED	When NOT set: no action When set: When the RXP filter drops a frame and the NAV update is masked (due to enabling the NAV update masking features in this register), the 'skip_difs' signal to the MTU will be set. Reset State: 0x00000000
4	CFG_FLT_NO_NAV_UPDATE_ON_DROP_AND_BELOW_CCA	When NOT set: no action When set: When the RXP filter drops a frame due to any reason, AND the cca at the sample point was high, the RXP will NOT generate a NAV update based on the dropped frame. Reset State: 0x00000000
3	CFG_FLT_NO_NAV_UPDATE_ON_EXPLICIT_DROP_AND_BELOW_CCA	When NOT set: no action When set: When the RXP filter drops a frame due to an explicit drop configuration in the address table, AND the cca at the sample point was high, the RXP will NOT generate a NAV update based on the dropped frame. Reset State: 0x00000000
2	CFG_FLT_NO_NAV_UPDATE_ON_EXPLICIT_DROP	When NOT set: no action When set: When the RXP filter drops a frame due to an explicit drop configuration in the address table, the RXP will not generate a NAV update based on the dropped frame. The setting of the CCA is NOT taken into account Reset State: 0x00000000

RXP_CFG_FLT_NAV_CONTROL_RESPONSE_REQ (cont.)

Bits	Name	Description
1	CFG_FLT_CLEAR_SKIP_NEXT_DIFS_ON_EARLY_PKTDET	When NOT set: no action When set: The RXP filter can generate a signal to the MTU to skip DIFS. See other register bits to enable this. This 'skip' signal will be cleared when early_pktdet_n gets asserted. Reset State: 0x00000000
0	CFG_FLT_CLEAR_SKIP_NEXT_DIFS_ON_CCA	When NOT set: no action When set: The RXP filter can generate a signal to the MTU to skip DIFS. See other register bits to enable this. This 'skip' signal will be cleared when primary cca gets asserted. Reset State: 0x00000000

0x30000F0 RXP_CFG_FLT_TYPE_SUBTYPE_RX_DISABLE0

Type: read-write
Reset State: 0x00000000

Control overwrite functionality for what was programmed in type/subtype config table (upper 32 bits)

RXP_CFG_FLT_TYPE_SUBTYPE_RX_DISABLE0

Bits	Name	Description
31:0	CFG_FLT_TYPE_SUBTYPE_RX_DISABLE0	Control some overwrite functionality for whatever was programmed in the Type/subtype configuration table. When set, a frame of the corresponding type should be dropped. Reset State: 0x00000000

0x30000F4 RXP_CFG_FLT_TYPE_SUBTYPE_RX_DISABLE1

Type: read-write
Reset State: 0x00000000

Control overwrite functionality for what was programmed in type/subtype config table (lower 32 bits)

RXP_CFG_FLT_TYPE_SUBTYPE_RX_DISABLE1

Bits	Name	Description
31:0	CFG_FLT_TYPE_SUBTYPE_RX_DISABLE1	Control some overwrite functionality for whatever was programmed in the Type/subtype configuration table. When set, a frame of the corresponding type should be dropped. Reset State: 0x00000000

0x30000F8 RXP_DIAG_STATUS

Type: read-only
Reset State: 0x00000000

The RXP diagnostic status.

RXP_DIAG_STATUS

Bits	Name	Description
31:0	DIAG_STATUS	The RXP diagnostic status. If status[5:0] is 6'h0, all the RXP state machines are IDLE. If status[10:6] is 5'h0, all the RXP FIFOs are empty. The following list the meaning of each status bit: status[28:25]: enc_cur_phy_st[3:0], status[24:21]: enc_cur_dlm_st[3:0], status[20:16]: enc_cur_mpdu_st[4:0], status[15:11]: enc_cur_dma_st[4:0], status[10]: !dma_ctl_st_idle, status[9]: !mpdu_proc_st_idle, status[8]: !dlm_proc_st_idle, status[7]: !phy_proc_st_idle, status[6]: !phy_rxi_ctl_st_idle, status[5]: !dma_tfifo_empty, status[4]: !dma_dfifo_empty, status[3]: !dma_hfifo_empty, status[2]: !dlm_tfifo_empty, status[1]: !dlm_dfifo_empty, status[0]: !dlm_hfifo_empty Reset State: 0x00000000

0x30000FC RXP_DIAG_TESTBUS_SEL

Type: read-write
Reset State: 0x00000000

The diagnostic testbus selection signal.

RXP_DIAG_TESTBUS_SEL

Bits	Name	Description
23:16	TESTBUS120AND160_SEL	The diagnostic testbus selection signal for 120/160 signals. 8'h0 is disabled. Valid values are from 0-1. testbus[44:19] will be from testbus120, pktdet_n, primary_cca, secondary_cca, early_pktdet_n, [13:9] will be rxi_testbus[36:32], [8:0] will be rxi_testbus[8:0]. Reset State: 0x00000000
15:8	TESTBUS160_SEL	The diagnostic testbus selection signal for 160 signals. 8'h0 is diabled. Valid values are from 0-2. rxi_testbus - 2, rdp_testbus - 1. Reset State: 0x00000000

RXP_DIAG_TESTBUS_SEL (cont.)

Bits	Name	Description
7:0	TESTBUS120_SEL	The diagnostic testbus selection signal for 120 signals. 8'h0 is diabled. Valid values are from 0-22 {13'h1fff, rxp_diag_status}, mpdu_proc_testbus2, // 21 dlm_proc_testbus4, dlm_proc_testbus3, dlm_proc_testbus2, rxp_drop_testbus2, // 17 rxp_dlm_fifo_full_testbus, dma_gam_testbus, dma_gbi_testbus, rxp_drop_testbus, phy_proc_testbus, dlm_proc_testbus, mpdu_proc_testbus, filter_testbus, binary_search_testbus, dma_ctl_testbus, {9'h0, gas_testbus}, {9'h0, gam_testbus}, {9'h0, gbi_testbus}, cfg_testbus, apm_testbus, rdm_testbus // 1 Reset State: 0x00000000

0x3000100 RXP_FRAME_FILTER_CONFIG

Type: read-write
Reset State: 0x00000000

This is a register set of 64 sequential word addresses: Each of these 64 words represent the filter configuration for a incoming frame type/subtype The register programming address per type/subtype is created as follows: ("This registers address" + {Type [b3, b2], Subtype [b7,b6,b5,b4], 2'b00}) where 'Type [b3,b2]' and 'Subtype [b7,b6,b5,b4]' are the IEEE standard encodings for the frames. A detailed description of the RXP filter specification can be found in the NOVA MAC architecture document. A summary of the bit functions is as follows:

RXP_FRAME_FILTER_CONFIG

Bits	Name	Description
21	G5_DROP_AT_DMA	When set, the RXP will drop the incoming frame (even when the CRC and filter function passes) at the RXP DMA engine. This feature is useful to prevent that control frames like the TRS, ACK etc, get unnecessarily written into memory Reset State: 0x00000000
20	NONHT_BW_INDICATION_ENABLE	when set then the this particular type/subtype will need to be checked for bw information. If bit 0 of TA is checked to see if BW information is valid. Reset State: 0x00000000
19	ROUTING_FLAG_SEL	when set : rxp will use dpu routing flag that is programmed in config3 bits 29:24 when not set : rxp will use dpu routing flag that is programmed in config3 bits 21:16 Reset State: 0x00000000
18	FRAME_TRANSLATION_REQ_EN	When set Frame translation by UMA is enabled Reset State: 0x00000000
17	PM_BIT_EVAL_REQUIRED_ENABLE	when this bit is set the pm bit is evaluated for this type/subtype packet Reset State: 0x00000000

RXP_FRAME_FILTER_CONFIG (cont.)

Bits	Name	Description
16	RESERVED3	It is reserved for future use, it is read writable Reset State: 0x00000000
15	ADDR3_ACCEPT_REMAINING_ENABLE	when enabled, and no hit was found for the Addr3 binary search, the incoming frame for this type/subtype will pass the Addr3 filter. The ADDR3 index code returned is 255 for multicast/broadcast and 254 for unicast. Reset State: 0x00000000
14	ADDR3_BINARY_SEARCH_FILTER_ENABLE	When enabled, Addr3 is submitted to the RXP Addr3 binary search filter. When not enabled, Addr3 filtering is NOT done, The returned ADDR3 index code is 253 and the 'Addr3_index_invalid' bit in the RXP status flags in the BD will be set Reset State: 0x00000000
13	ADDR2_ACCEPT_REMAINING_ENABLE	when enabled, and no hit was found for the Addr2 binary search, the incoming frame for this type/subtype will pass the Addr2 filter. The ADDR2 index code returned is 255 for multicast/broadcast and 254 for unicast. Reset State: 0x00000000
12	ADDR2_BINARY_SEARCH_FILTER_ENABLE	When enabled, Addr2 is submitted to the RXP Addr2 binary search filter. When not enabled, Addr2 filtering is NOT done, The returned ADDR2 index code is 253 and the 'Addr2_index_invalid' bit in the RXP status flags in the BD will be set Reset State: 0x00000000
11	ADDR1_ACCEPT_REMAINING_UNICAST_ENABLE	when enabled, and no hit was found for the unicast address in the Addr1 binary search, the incoming unicast frame for this type/subtype will pass the Addr1 filter. The index code returned is: 254 Reset State: 0x00000000
10	ADDR1_ACCEPT_REMAINING_MULTICAST_ENABLE	when enabled, and no hit was found for the multicast/broadcast address in the Addr1 binary search, the incoming multicast/broadcast frame for this type/subtype will pass the Addr1 filter. The index code returned is: 255. Reset State: 0x00000000
9	ADDR1_BINARY_SEARCH_FILTER_ENABLE	When enabled, Addr1 is submitted to the RXP Addr1 binary search filter. When not enabled, Addr1 filtering is NOT done, The returned ADDR1 index code is 253 and the 'Addr1_index_invalid' bit in the RXP status flags in the BD will be set Reset State: 0x00000000
8	ADDR1_BLOCK_UNICAST_ENABLE	when enabled, a unicast frame for this type/subtype will not pass the filter. Reset State: 0x00000000
7	ADDR1_BLOCK_MULTICAST_ENABLE	when enabled, a multicast frame for this type/subtype will not pass the filter. Reset State: 0x00000000

RXP_FRAME_FILTER_CONFIG (cont.)

Bits	Name	Description
6	ADDR1_BLOCK_BROADCAST_ENABLE	when enabled, a broadcast frame for this type/subtype will not pass the filter. Reset State: 0x00000000
5	RESERVED4	It is reserved for future use, it is read writable Reset State: 0x00000000
4	RESERVED5	It is reserved for future use, it is read writable Reset State: 0x00000000
3	RESERVED6	It is reserved for future use, it is read writable Reset State: 0x00000000
2	RESERVED7	It is reserved for future use, it is read writable Reset State: 0x00000000
1	BLOCK_RECEPTION_ENABLE	When enabled, all frames of this type/subtype will be blocked and will NOT pass the type/subtype/address filter check. Reset State: 0x00000000
0	RESERVED8	It is reserved for future use, it is read writable Reset State: 0x00000000

0x3000204 RXP_STALL_TIMEOUT

Type: read-write
Reset State: 0x00012000

Stall timeout functionality - allows RXP to return to idle if PMI interface stalls.

RXP_STALL_TIMEOUT

Bits	Name	Description
16	STALL_TIMEOUT_EN	Enable stall timeout functionality on the MPI. Reset State: 0x00000001
15:0	STALL_TIMEOUT_TIME	Number of cycles of no activity during PMI transaction before stall timeout occurs. Reset State: 0x00002000

0x3000250 RXP_CONFIG2

Type: read-write
Reset State: 0x010381DF

It contains RXP Configuration registers, related to gen5_6 functionality added

RXP_CONFIG2

Bits	Name	Description
31:29	CFG_CONFIG2_RESERVED	reserved for future use Reset State: 0x00000000
28	NAV_UPDATE_DOES_NOT_EXCLUDE_SELF	When set, the NAV will also be set for frames destined to this STA When NOT set, the NAV is only set for unicast frames received that are destined for other STAs For both settings the NAV will be set for all BC/MC frames. Reset State: 0x00000000
27	MASK_OUT_AMSDU_FRAMES_IN_AMPDU_ENABLE	When set, and amsdu frames embedded in AMPDU frames are received, the amsdu frames will be dropped Reset State: 0x00000000
26	ADDR2_AUTH_EXTRACT_ENABLE	When set, the RXP will extract the 'authentication setting from the addr 2 binary search entry (bit 2 of the 3 bit wide DPU tag entry), and insert in the BE. In this mode, the DPU tag when based on the ADDR 2 DPU TAG entry will only be 2 bits wide in stead of the regular 3 bits. Reset State: 0x00000000
25	PASS_LSIG_PROT_INFO_TO_TPE_ENABLE	When set, the RXP will pass the setting of the LSIG protection signal to the TPE together with the other response required info. Reset State: 0x00000000
24	DEFAULT_PUSH_WQ_OVERWRITE_ENABLE	When set, the RXP will by default push frames to WQ indicated in "default_push_wq". When NOT set, the RXP will by default push frames to WQ 2. Reset State: 0x00000001
23:16	DEFAULT_PUSH_WQ	Field is only used when Reset State: 0x00000003
15	BD_CLEAR_ENABLE_ENABLE	When set, the RXP will clear (set to zero) the bytes located in the BD between the PMI command bytes and the MPDU header bytes. Reset State: 0x00000001
14	FILTER_RPE_TRACE_ENABLE	When set, the RXP filter interaction result with the RPE will be passed on to the BMU. That can result in the BMU pushing this info into the BMU hardware tracing list Reset State: 0x00000000
13	DMA_RPE_TRACE_ENABLE	When set, the RXP DMA interaction result with the RPE will be passed on to the BMU. That can result in the BMU pushing this info into the BMU hardware tracing list Reset State: 0x00000000
12	CFG_FLT_DEFAULT_ROUTING_DIS	By default rxp uses the cfg_flt_dpu_man_rtg_flg,cfg_flu_dpu_data_rtg_flag to fill in dpu routing flags. If this bit is set then RXP will use the per type/subtype routing selection Reset State: 0x00000000

RXP_CONFIG2 (cont.)

Bits	Name	Description
11	CFG_FLT_PHY_ABORT_DIS	by default phy abort is enabled when this bit is set it is disabled By default PHY RX will be aborted (shutdown) when the frame does not pass the type/subtype/address filter. This will save extra power Reset State: 0x00000000
10	CFG_FLT_NAV_SET_ENABLE_ON_ABORT	When enabled and the incoming frame does not pass the type/subtype/address filter and is aborted before the FCS is calculated, update the NAV, Reset State: 0x00000000
9	CFG_FLT_NAV_CLEAR_ENABLE_ON_ABORT	When enabled, and the incoming frame does not pass the type/subtype/address filter and is aborted before the FCS is calculated, the NAV will be cleared. Reset State: 0x00000000
8	CFG_FLT_HW_SW_BASED_RESPONSE_SELECTION_ENABLE	when set, the response generation path: Software based or hardware based is controlled based on programming in the type/subtype configuration table, done through register "frame_filter_config". Note that if this control is required, the 'cfg_flt_generate_hw_response_enabled' should be cleared, otherwise this programming is overruled. When 'cfg_flt_hw_sw_based_response_selection_enable' is set, 'cfg_flt_generate_hw_response_enabled' is clear and 'G5_generate_HW_Response' for an incoming frame is set, the RXP will generate a pulse to the TPE to generate a response frame if also the following conditions are met: addr1 is a unicast address, caused a hit in the addr. lookup table AND incoming frame is a: Management frame OR data frame OR QoS data frame with ack policy set to normal OR RTS frame OR PSPOLL frame OR BAR_frame When 'cfg_flt_hw_sw_based_response_selection_enable' is set, 'cfg_flt_generate_hw_response_enabled' is clear and 'G5_generate_SW_RRI' for an incoming frame is set, the RXP will generate the RRI interrupt, so that software can start generating the response frame, if also the following conditions are met: addr1 is a unicast address, caused a hit in the addr. lookup table AND incoming frame is a: Management frame OR data frame OR QoS data frame with ack policy set to normal OR RTS frame OR PSPOLL frame OR BAR_frame Reset State: 0x00000001
7	CFG_FLT_FILTER_GO_TO_IDLE_ON_CLEAR_ENABLED	Gen 4 workaround: When set, and the MPDU PROC state machine signals 'clear' to the filter, the filter will return to its idle state, forcing it to break of all interaction with other modules Reset State: 0x00000001
6	CFG_MPR_BMU_BA_UPDATE_ENABLED	When set, enables the rxp interface with the BMU for Block Ack update Reset State: 0x00000001
5	CFG_MPDU_PROC_WAIT_FOR_IDLE_FILTER_ENABLED	When set, enables bug fix from gen 4. This forces the MPDU PROC state machine to wait for the rxp filter to get into an idle state before aborting a frame. Reset State: 0x00000000

RXP_CONFIG2 (cont.)

Bits	Name	Description
4	CFG_MPR_TPE_INTERFACE_ENABLED	When set to 1 the interface to the TPE is enabled Reset State: 0x00000001
3	CFG_FLT_GENERATE_HW_RESPONSE_ENABLED	When set to 1 the global hardware response generation logic within the RXP filter is enabled for the following conditions: addr1 is a unicast address, caused a hit in the addr. lookup table AND incoming frame is a: Management frame OR data frame OR QoS data frame with ack policy set to normal OR RTS frame OR PSPOLL frame OR BAR_frame Reset State: 0x00000001
2	BMU_PWR_UPDATE_ENABLED	When set, enables the rxp interface with the BMU for power management updates related to PWR Mgt bit in frame control field, PS POLL reception and APSD trigger frame reception Reset State: 0x00000001
1	CFG_BD_DPU_SOFTMACFIELDS_UPDATE_ENABLE	when you write a 1 the DPU related fields that softmac updates is enabled Reset State: 0x00000001
0	CFG_RPE_INTERFACE_ENABLE	when you write a 1 rpe interface is enabled That means duplicate detect interface function from the rxp filter is enabled as well as the bitmap update function from the rxp dma controller Reset State: 0x00000001

0x3000254 RXP_CONFIG3

Type: read-write
Reset State: 0x07180200

It contains RXP Configuration registers, related to gen5_6 functionality added

RXP_CONFIG3

Bits	Name	Description
29:24	CFG_FLT_DPU_MAN_RTG_FLG	This is the routing flag to which DPU will push management packets to, this is the value that is in the dpu_routing field in RXBD for management packets Reset State: 0x00000007
21:16	CFG_FLT_DPU_DATA_RTG_FLG	This is the routing flag to which DPU will push data packets to, this is the value that is in the dpu_routing field in RXBD for data packets Reset State: 0x00000018
14	CFG_RSSI_MODE_SEL	This bit selects the two modes of rssi data collection when this bit is 1'b0 : select Mode 0, the byte2(RxFIR0) and Byte3(RxFIR1) of PHY STATS are selected to be stored when this bit is 1'b1 : select Mode 1, the greater of Byte2 and Byte3 and Byte4(SNR) of PHY stats are selected to be stored Reset State: 0x00000000

RXP_CONFIG3 (cont.)

Bits	Name	Description
11:0	CFG_FLT_RPE_HANDSHAKE_TIMEOUT_VALUE	The RXP filter interacts with the RPE. At the start of this interaction a timeout counter is initialized. This register provides the timeout value for this interaction in number of clk cycles Reset State: 0x00000200

0x3000258 RXP_SEARCH_TABLE_DATA2

Type: read-write
Reset State: 0x00000000

This is data register 2 for indirect access to Binary Search Table. It contains all the DPU related configurations that the RXP will insert into the BD There are totally 3 Data registers for Binary Search address Table.

RXP_SEARCH_TABLE_DATA2

Bits	Name	Description
31:29	DPU_MC_BC_TAG	THe DPU routing flag that will be inserted in the BD Reset State: 0x00000000
28:21	DPU_MAN_MC_BC_DESCRIPTOR_INDEX	THe DPU descriptor index that will be inserted in the BD for mc/bc management packets Reset State: 0x00000000
20	DPU_NE	When set, the RXP will set the 'ne' field in the bd to 1'b1 Reset State: 0x00000000
19	WEP_KEY_ID_EXTRACT_ENABLE	When set, the RXP filter will extract the Key id from encrypted frames (assuming that the encryption is wep) Reset State: 0x00000000
18:16	DPU_TAG	THe DPU routing flag that will be inserted in the BD Reset State: 0x00000000
15:8	DPU_MC_BC_DPU_DESC	This field contains dpu descriptor index for BC/MC QoS/NonQoS frames RXP will insert this field in the DPU descriptor field in the BD. Reset State: 0x00000000
7:0	DPU_DESCRIPTOR_INDEX	THe DPU descriptor index that will be inserted in the BD for unicast data or unicast robust management frames (RMF) Reset State: 0x00000000

0x300025C RXP_BEACON_TSF_TIM_EXTRACT_CTRL

Type: read-write
Reset State: 0x00000003

This is controls what information needs to be extracted from the beacon and under what condition

RXP_BEACON_TSF_TIM_EXTRACT_CTRL

Bits	Name	Description
30	EARLY_TIM_PROCESS	when this bit is set then the tim not set interrupt is generated immediately after TIM bit is received and will not wait for the FCS complete Reset State: 0x00000000
29	P2P_BEACON_PARS_EN	when this bit is set then the system is indicating that we can receive p2p beacons so the beacon parsing checks whether received beacon is for P2P or BSS mode and accordingly TSF comparison and update is done 1'b0: no P2P beacons allowed, only BSS beacons allowed 1'b1: P2P/BSS beacons allowed Reset State: 0x00000000
28	SIM_IBSS_BSS_BEACON_PARS_EN	when this bit is set then the system is indicating that there is IBSS/BSS co-existence so the beacon parsing checks whether received beacon is for IBSS or BSS mode and accordingly TSF comparison and update is done 1'b1: IBSS/BSS beacons allowed 1'b0: no IBSS beacons allowed only BSS beacons allowed NOTE: when bit[29:28] = 2'b11 P2P/IBSS/BSS beacons allowed Reset State: 0x00000000
27	BEACON_CFP_AWARENESS_ENABLE	When set, and beacon processing is enabled, the beacon will also be evaluated for the presence of the CF parameter set. If present, the CFP remaining duration period is extracted and the NAV is set to that value. Reset State: 0x00000000
26:16	ASSOCIATION_ID	The association id of the station. This field is used to know which tim bit from the TIM element is related to this station Reset State: 0x00000000
15:8	CFG_MPR_SSID_LENGTH	When 'enable_beacon_ssid_check' is set and 'enable_beacon_partial_ssid_check_ok' is NOT set, RXP will check the SSID length field of the received beacon. That length field will need to have the same value as this register, otherwise the beacon filter will indicate a mismatch. When 'enable_beacon_ssid_check' is set and 'enable_beacon_partial_ssid_check_ok' is set as well, this length field indicates how many sequential bytes in a row of the beacon SSID field, starting from the first byte of the SSID field received, will have to match the programmed SSID bytes, in order for the beacon to pass the filter. Note that in this case, the SSID length field itself does not necessarily need to match, except that the length field in the beacon needs to be larger then the value programmed here. Reset State: 0x00000000
5	ENABLE_BEACON_SSID_CHECK	When set, the tsf update (based on IBSS of BSS rules) or tim field extraction will only happen if the incoming beacon has an SSID 3 field which matches the contents of the 'SSID_field' register, and 'SSID_length' field in this register Reset State: 0x00000000

RXP_BEACON_TSF_TIM_EXTRACT_CTRL (cont.)

Bits	Name	Description
1	ENABLE_BEACON_TIM_PARSING	When set, beacon tim field extraction and TIM field interrupt pulse generation is enabled Reset State: 0x00000001
0	ENABLE_BEACON_TSF_PARSING	When set, beacon timestamp extraction and TSF update are enabled Reset State: 0x00000001

0x3000260 RXP_TSF_COMPENSATION1_VALUE

Type: read-write
Reset State: 0x00000000

This register contains offset values to add the received TSF value to compensate for the delay in the PHY receive chain

RXP_TSF_COMPENSATION1_VALUE

Bits	Name	Description
31:24	TSF_11B_11MBPS_COMP_VALUE	The TSF compensation value when the beacon is received at a 11b rate of 11Mbps Reset State: 0x00000000
23:16	TSF_11B_5_5MBPS_COMP_VALUE	The TSF compensation value when the beacon is received at a 11b rate of 5.5Mbps Reset State: 0x00000000
15:8	TSF_11B_2MBPS_COMP_VALUE	The TSF compensation value when the beacon is received at a 11b rate of 2Mbps Reset State: 0x00000000
7:0	TSF_11B_1MBPS_COMP_VALUE	The TSF compensation value when the beacon is received at a 11b rate of 1Mbps Reset State: 0x00000000

0x3000264 RXP_TSF_COMPENSATION2_VALUE

Type: read-write
Reset State: 0x00000000

This register contains offset values to add the received TSF value to compensate for the delay in the PHY receive chain

RXP_TSF_COMPENSATION2_VALUE

Bits	Name	Description
23:16	TSF_11AG_OTHER_RATE_COMP_VALUE	THe TSF compensation value when the beacon is received at any other 11a or 11g rate Reset State: 0x00000000
15:8	TSF_11AG_54MBPS_COMP_VALUE	THe TSF compensation value when the beacon is received at an 11a or 11g rate of 54Mbps Reset State: 0x00000000
7:0	TSF_11AG_6MBPS_COMP_VALUE	THe TSF compensation value when the beacon is received at an 11a or 11g rate of 6Mbps Reset State: 0x00000000

0x3000268 RXP_SSID_VALUES_B0_B3

Type: read-write
Reset State: 0x00000000

This register contains SSID bytes 0 - 3

RXP_SSID_VALUES_B0_B3

Bits	Name	Description
31:0	SSID_VALUES_BYTES_B0_B3	The SSID bytes, in LE format Reset State: 0x00000000

0x300026C RXP_SSID_VALUES_B4_B7

Type: read-write
Reset State: 0x00000000

This register contains SSID bytes 4 - 7

RXP_SSID_VALUES_B4_B7

Bits	Name	Description
31:0	SSID_VALUES_BYTES_B4_B7	The SSID bytes, in LE format Reset State: 0x00000000

0x3000270 RXP_SSID_VALUES_B8_B11

Type: read-write
Reset State: 0x00000000

This register contains SSID bytes 8 - 11

RXP_SSID_VALUES_B8_B11

Bits	Name	Description
31:0	SSID_VALUES_BYTES_B8_11	The SSID bytes, in LE format Reset State: 0x00000000

0x3000274 RXP_SSID_VALUES_B12_B15

Type: read-write
Reset State: 0x00000000

This register contains SSID bytes 12 - 15

RXP_SSID_VALUES_B12_B15

Bits	Name	Description
31:0	SSID_VALUES_BYTES_B12_15	The SSID bytes, in LE format Reset State: 0x00000000

0x3000278 RXP_SSID_VALUES_B16_B19

Type: read-write
Reset State: 0x00000000

This register contains SSID bytes 16 - 19

RXP_SSID_VALUES_B16_B19

Bits	Name	Description
31:0	SSID_VALUES_BYTES_B16_19	The SSID bytes, in LE format Reset State: 0x00000000

0x300027C RXP_SSID_VALUES_B20_B23

Type: read-write
Reset State: 0x00000000

This register contains SSID bytes 20 - 23

RXP_SSID_VALUES_B20_B23

Bits	Name	Description
31:0	SSID_VALUES_BYTES_B20_23	The SSID bytes, in LE format Reset State: 0x00000000

0x3000280 RXP_SSID_VALUES_B24_B27

Type: read-write
Reset State: 0x00000000

This register contains SSID bytes 24 - 27

RXP_SSID_VALUES_B24_B27

Bits	Name	Description
31:0	SSID_VALUES_BYTES_B24_27	The SSID bytes, in LE format Reset State: 0x00000000

0x3000284 RXP_SSID_VALUES_B28_B31

Type: read-write
Reset State: 0x00000000

This register contains SSID bytes 28 - 31

RXP_SSID_VALUES_B28_B31

Bits	Name	Description
31:0	SSID_VALUES_BYTES_B28_31	The SSID bytes, in LE format Reset State: 0x00000000

0x3000288 RXP_BEACON_ADDR2_LOW_FIELD

Type: read-write
Reset State: 0x00000000

This register contains the lowest 4 bytes of the address 2 field of the beacon, in case a match function is enabled

RXP_BEACON_ADDR2_LOW_FIELD

Bits	Name	Description
31:0	BEACON_ADDR2_LSB_BYTES	The 4 LS Bytes of the addr2, LE format Reset State: 0x00000000

0x300028C RXP_BEACON_ADDR2_HIGH_FIELD

Type: read-write
Reset State: 0x00000000

This register contains the highest 2 bytes of the address 2 field of the beacon, in case a match function is enabled

RXP_BEACON_ADDR2_HIGH_FIELD

Bits	Name	Description
15:0	BEACON_ADDR2_MSB_BYTES	The 2 MS Bytes of the addr2, LE format Reset State: 0x00000000

0x3000290 RXP_BEACON_ADDR3_LOW_FIELD

Type: read-write
Reset State: 0x00000000

This register contains the lowest 4 bytes of the address 3 field of the beacon, in case a match function is enabled

RXP_BEACON_ADDR3_LOW_FIELD

Bits	Name	Description
31:0	BEACON_ADDR3_LSB_BYTES	The 4 LS Bytes of the addr3, LE format Reset State: 0x00000000

0x3000294 RXP_BEACON_ADDR3_HIGH_FIELD

Type: read-write
Reset State: 0x00000000

This register contains the highest 2 bytes of the address 3 field of the beacon, in case a match function is enabled

RXP_BEACON_ADDR3_HIGH_FIELD

Bits	Name	Description
15:0	BEACON_ADDR3_MSB_BYTES	The 2 MS Bytes of the addr3, LE format Reset State: 0x00000000

0x3000298 RXP_FLT_DUPL_CNT

Type: read-only
Reset State: 0x00000000

Number of frames that got dropped at the rxp filter because the RPE indicated to the RXP filter that the frame was a duplicate

RXP_FLT_DUPL_CNT

Bits	Name	Description
7:0	FLT_DUPL_DROPPED_COUNT	number of frames dropped Reset State: 0x00000000

0x300029C RXP_FLT_RPE_HANDSHAKE_TIMEOUT_CNT

Type: read-only
Reset State: 0x00000000

Number of times that the handshake between the rxp filter and the RPE timed out.

RXP_FLT_RPE_HANDSHAKE_TIMEOUT_CNT

Bits	Name	Description
19:16	DMA_RPE_TIMEOUT_COUNT	number of timeouts that occurred on the RXP DMA <-> RPE interface Reset State: 0x00000000
3:0	FLT_RPE_TIMEOUT_COUNT	number of timeouts that occurred on the RXP Filter <-> RPE interface Reset State: 0x00000000

0x3000300 RXP_QID_MAPPING0

Type: read-write
Reset State: 0x00000008

Controls how incoming data flows get mapped to a qid

RXP_QID_MAPPING0

Bits	Name	Description
4:0	MAN_AND_DATA_QID	When the incoming frame is a management frame or plain (NON QoS) data frame, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000008

0x3000304 RXP_QID_MAPPING1

Type: read-write
Reset State: 0x03020100

Controls how incoming data flows get mapped to a qid

RXP_QID_MAPPING1

Bits	Name	Description
28:24	QOS_TID3_QID	When the incoming frame is a QoS data frame with TID set to 3, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000003
20:16	QOS_TID2_QID	When the incoming frame is a QoS data frame with TID set to 2, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000002
12:8	QOS_TID1_QID	When the incoming frame is a QoS data frame with TID set to 1, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000001
4:0	QOS_TID0_QID	When the incoming frame is a QoS data frame with TID set to 0, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000000

0x3000308 RXP_QID_MAPPING2

Type: read-write
Reset State: 0x07060504

Controls how incoming data flows get mapped to a qid

RXP_QID_MAPPING2

Bits	Name	Description
28:24	QOS_TID7_QID	When the incoming frame is a QoS data frame with TID set to 7, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000007
20:16	QOS_TID6_QID	When the incoming frame is a QoS data frame with TID set to 6, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000006
12:8	QOS_TID5_QID	When the incoming frame is a QoS data frame with TID set to 5, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000005
4:0	QOS_TID4_QID	When the incoming frame is a QoS data frame with TID set to 4, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000004

0x300030C RXP_QID_MAPPING3

Type: read-write
Reset State: 0x00000000

Controls how incoming data flows get mapped to a qid

RXP_QID_MAPPING3

Bits	Name	Description
28:24	QOS_TID11_QID	When the incoming frame is a QoS data frame with TID set to 11, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000000
20:16	QOS_TID10_QID	When the incoming frame is a QoS data frame with TID set to 10, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000000
12:8	QOS_TID9_QID	When the incoming frame is a QoS data frame with TID set to 9, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000000
4:0	QOS_TID8_QID	When the incoming frame is a QoS data frame with TID set to 8, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000000

0x3000310 RXP_QID_MAPPING4

Type: read-write
Reset State: 0x00000000

Controls how incoming data flows get mapped to a qid

RXP_QID_MAPPING4

Bits	Name	Description
28:24	QOS_TID15_QID	When the incoming frame is a QoS data frame with TID set to 15, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000000
20:16	QOS_TID14_QID	When the incoming frame is a QoS data frame with TID set to 14, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000000
12:8	QOS_TID13_QID	When the incoming frame is a QoS data frame with TID set to 13, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000000
4:0	QOS_TID12_QID	When the incoming frame is a QoS data frame with TID set to 12, the contents of this register represents the qid assigned to this type of frames Reset State: 0x00000000

0x3000314 RXP_PUSH_WQ_CTRL

Type: read-write
Reset State: 0x02020202

Controls how frames that fall in the unicast other of multicast 'other categories' get routed through the system

RXP_PUSH_WQ_CTRL

Bits	Name	Description
31:24	ADDR2_255_CATEGORY_PUSH_WQ_INDEX	When the incoming frame will end up with staid 255 for addr 2, the frame will be routed to this WQ. Reset State: 0x00000002
23:16	ADDR2_254_CATEGORY_PUSH_WQ_INDEX	When the incoming frame will end up with staid 254 for addr 2, the frame will be routed to this WQ. Reset State: 0x00000002

RXP_PUSH_WQ_CTRL (cont.)

Bits	Name	Description
15:8	ADDR1_255_CATEGORY_PUSH_WQ_INDEX	When the incoming frame will end up with staid 255 for addr 1 (multicast other), the frame will be routed to this WQ. Reset State: 0x00000002
7:0	ADDR1_254_CATEGORY_PUSH_WQ_INDEX	When the incoming frame will end up with staid 254 for addr 1(unicast other), the frame will be routed to this WQ. Reset State: 0x00000002

0x3000318 RXP_PUSH_WQ_CTRL2

Type: read-write
Reset State: 0x00020202

Controls how frames that fall in the unicast other of multicast 'other categories' get routed through the system

RXP_PUSH_WQ_CTRL2

Bits	Name	Description
23:16	UNFILTERED_FRAME_PUSH_WQ_INDEX	When the incoming frame will does not get processed in any address filtering, all three staid indexes are invalid and set to 253, the frame will be routed to this WQ Reset State: 0x00000002
15:8	ADDR3_255_CATEGORY_PUSH_WQ_INDEX	When the incoming frame will end up with staid 255 for addr 3, the frame will be routed to this WQ. Reset State: 0x00000002
7:0	ADDR3_254_CATEGORY_PUSH_WQ_INDEX	When the incoming frame will end up with staid 254 for addr 3, the frame will be routed to this WQ. Reset State: 0x00000002

0x300031C RXP_EXTRA_FRAME_FILTER_CONTROL

Type: read-write
Reset State: 0x000001DD

additional control for how frames are filtered

RXP_EXTRA_FRAME_FILTER_CONTROL

Bits	Name	Description
15:9	RESERVED	Reserved for future filter functions Reset State: 0x00000000

RXP_EXTRA_FRAME_FILTER_CONTROL (cont.)

Bits	Name	Description
8	BLOCK_FRAMES_WITH_HT_CONTROL_FIELD	When set, frames that have a HT-control field present as specified in 11n are blocked from being received Reset State: 0x00000001
7	BLOCK_MULTI_TID_BLOCK_ACK_REQ	When set, the multi TID block ACK Request variant as specified in 11n is blocked from being received Reset State: 0x00000001
6	BLOCK_RESERVED_BLOCK_ACK_REQ	When set, the reserved block ACK Request variant as specified in 11n is blocked from being received Reset State: 0x00000001
5	BLOCK_COMPRESSED_BLOCK_ACK_REQ	When set, the compressed block ACK Request variant as specified in 11n is blocked from being received Reset State: 0x00000000
4	BLOCK_BASIC_BLOCK_ACK_REQ	When set, the basic block ACK Request variant as specified in 11n is blocked from being received Reset State: 0x00000001
3	BLOCK_MULTI_TID_BLOCK_ACK	When set, the multi TID block ACK variant as specified in 11n is blocked from being received Reset State: 0x00000001
2	BLOCK_RESERVED_BLOCK_ACK	When set, the reserved block ACK variant as specified in 11n is blocked from being received Reset State: 0x00000001
1	BLOCK_COMPRESSED_BLOCK_ACK	When set, the compressed block ACK variant as specified in 11n is blocked from being received Reset State: 0x00000000
0	BLOCK_BASIC_BLOCK_ACK	When set, the basic block ACK variant as specified in 11n is blocked from being received Reset State: 0x00000001

0x3000320 RXP_RXP_GROUPED_INTERRUPT_ENABLE

Type: read-write
Reset State: 0x00000000

interrupt Enables for RXP errors

RXP_RXP_GROUPED_INTERRUPT_ENABLE

Bits	Name	Description
26	RXP_SYSTEM_OUT_OF_MEMORY_FIRMWARE	Write 1 to enable this interrupt, so that whenever system runs out of memory this interrupt will be set. this is duplicate the one in bit 13 goes to host and this interrupt goes to firmware only Reset State: 0x00000000

RXP_RXP_GROUPED_INTERRUPT_ENABLE (cont.)

Bits	Name	Description
25	P2P_BEACON_CTWIN_CHNG_DETECT_INT	when set enables this interrupt The NOA CTWin value is compared with the value programmed in p2p_parsing_control2 register if there is any change then this interrupt is generated Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
24	P2P_BEACON_OPPPS_CHNG_DETECT_INT_EN	when set enables this interrupt The NOA OppPS value is compared with the value programmed in p2p_parsing_control2 register if there is any change then this interrupt is generated this interrupt goes to firmware only Reset State: 0x00000000
23	P2P_TIM_BIT_CLEAR_INT	When set, p2p beacon has tim bit clear this interrupt goes to firmware only Reset State: 0x00000000
22	P2P_TIM_BIT_SET_INT	When set, tim bit set in p2p beacon this interrupt goes to firmware only Reset State: 0x00000000
21	P2P_TIM_BEACON_CRC_ERR_INT	When set, p2p beacon has CRC error this interrupt goes to firmware only Reset State: 0x00000000
20	P2P_TIM_BASED_BROADCAST_FRAMES_PENDING_INT	When set, indicates tim bit indicates broadcast frames are pending from a p2p beacon this interrupt goes to firmware only Reset State: 0x00000000
19	P2P_BEACON_NOA_ABSENT_INT_EN	When set, P2P beacon which has no NOA element interrupt will be enabled this interrupt goes to firmware only Reset State: 0x00000000
18	P2P_BEACON_NOA_INDX_EQ_ONE_DETECT_INT_EN	when set, P2P beacon NOA index value equal to one interrupt will be enabled this interrupt goes to firmware only Reset State: 0x00000000
17	P2P_BEACON_NOA_INDX_CHNG_DETECT_INT_EN	The NOA, index field is compared with the index value programmed in p2p_parsing_control register if there is any change the this interrupt is generated When set, P2p Beacon NOA index value change detect interrupt is enabled this interrupt goes to firmware only Reset State: 0x00000000
16	RXP_RADAR_INTERRUPT	When set, radar detect interrupt will be generated Reset State: 0x00000000
15	RXP_MORE_DATA_SET_INTERRUPT	When set, and a frame is received that passes the filter, is a management, data or QoS data frame and the more data bit in the frame is SET an interrupt pulse will be generated. That status info of the corresponding frame is captured in the other fields more_data_int_control register. this interrupt goes to host only Reset State: 0x00000000

RXP_RXP_GROUPED_INTERRUPT_ENABLE (cont.)

Bits	Name	Description
14	RXP_RMF_FRAME_LEN_ERR	Write 1 to enable this interrupt, whenever we receive a RMF BC/MC frame with frame less than 48bytes(which is minimum) then this interrupt is generated. this interrupt goes to host only Reset State: 0x00000000
13	RXP_SYSTEM_OUT_OF_MEMORY	Write 1 to enable this interrupt, so that whenever system runs out of memory this interrupt will be set. this interrupt goes to host only Reset State: 0x00000000
12	RXP_MORE_DATA_CLEAR_INTERRUPT	When set, and a frame is received that passes the filter, is a management, data or QoS data frame and the more data bit in the frame is NOT set an interrupt pulse will be generated. That status info of the corresponding frame is captured in the other fields more_data_int_control register. this interrupt goes to host only Reset State: 0x00000000
11	RXP_ADDR2_MISS_INTERRUPT	When set, and a frame is received that has an addr2 miss (and addr 1 is a hit), an 'addr2 miss interrupt will be generated. this interrupt goes to host only Reset State: 0x00000000
10	RXP_MISSED_EOSP_INT	When set, interrupt is generated when at least one other frame with EOSP got received while the first EOSP frame reception got reported this interrupt goes to firmware only Reset State: 0x00000000
9	RXP_EOSP_INT	When set, the EOSP interrupt will get generated if eosp frame is received this interrupt goes to firmware only Reset State: 0x00000000
8	TIM_BIT_CLEAR_INT	When set, beacon has tim bit clear this interrupt goes to firmware only Reset State: 0x00000000
7	TIM_BIT_SET_INT	When set, tim bit set in beacon this interrupt goes to firmware only Reset State: 0x00000000
6	TIM_BEACON_CRC_ERR_INT	When set, beacon has CRC error this interrupt goes to firmware only Reset State: 0x00000000
5	TIM_BASED_BROADCAST_FRAMES_PENDING_INT	When set, indicates tim bit indicates broadcast frames are pending this interrupt goes to host only Reset State: 0x00000000
4	ASYNC_FIFO_FULL_ERR_INT_ENABLE	When set, and the async fifo gets full, an interrupt will be generated this interrupt goes to host only Reset State: 0x00000000
3	GET_BMU_ERR_INT_ENABLE	When set, and the interaction with the bmu causes an error, an interrupt will be generated this interrupt goes to host only Reset State: 0x00000000

RXP_RXP_GROUPED_INTERRUPT_ENABLE (cont.)

Bits	Name	Description
2	INVALID_RATE_INDEX_INT_ENABLE	When set, and an invalid rate index is generated based on information from the PHY, an interrupt will be generated this interrupt goes to host only Reset State: 0x00000000
1	RPE_DUPL_INTERFACE_TIMEOUT_INT_ENABLE	When set, the rpe duplicate detect interface handshake timeout error interrupt generation is enabled this interrupt goes to host only Reset State: 0x00000000
0	RPE_BITMAP_INTERFACE_TIMEOUT_INT_ENABLE	When set, the rpe bitmap interface handshake timeout error interrupt generation is enabled this interrupt goes to host only Reset State: 0x00000000

0x3000324 RXP_RXP_GROUPED_INTERRUPT_STATUS

Type: read-write
Reset State: 0x00000000

RXP combined interrupt status, writing 1 to any bit will clear the corresponding interrupt

RXP_RXP_GROUPED_INTERRUPT_STATUS

Bits	Name	Description
31	DROP_RPE_FIFO_FULL	whenever a frame is dropped due to system out of memory this bit will indicate if there was a rpe fifo full that caused this packet drop 1: if syste_out_of memory is set and this bit is one packet dropped due RPE fifo full 0: if syste_out_of memory is set and this bit is zero then there may BMU BD/PDU issue Writing 1 to this bit will clear this status Reset State: 0x00000000
30	PACKET_PRIORITY	whenever a frame is dropped due to system out of memory this bt will indicate what was the priority of the frame that was dropped 1: high priority frame dropped 0: Low priority frame dropped Writing 1 to this bit will clear this status Reset State: 0x00000000
26	RXP_SYSTEM_OUT_OF_MEMORY_FIRMWARE_INT	when set it indicates system is running out of memory, which allows software to indicate to AP to back off on sending frames by sending frames with PM bit set Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
25	P2P_BEACON_CTWIN_CHNG_DETECT_INT	The NOA CTWin value is compared with the value programmed in p2p_parsing_control2 register if there is any change then this interrupt is generated Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000

RXP_RXP_GROUPED_INTERRUPT_STATUS (cont.)

Bits	Name	Description
24	P2P_BEACON_OPPPS_CHNG_DETECT_INT	The NOA OppPS value is compared with the value programmed in p2p_parsing_control2 register if there is any change then this interrupt is generated this interrupt goes to firmware only Reset State: 0x00000000
23	P2P_TIM_BIT_CLEAR_INT	When set, p2p beacon has tim bit clear Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
22	P2P_TIM_BIT_SET_INT	When set, tim bit set in p2p beacon Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
21	P2P_TIM_BEACON_CRC_ERR_INT	When set, p2p beacon has CRC error Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
20	P2P_TIM_BASED_BROADCAST_FRAMES_PENDING_INT	When set, indicates tim bit in p2p beacon indicates broadcast frames are pending Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
19	P2P_BEACON_NOA_ABSENT_INT	When set, P2P beacon which has no NOA element interrupt is generated Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
18	P2P_BEACON_NOA_INDX_EQ_ONE_DETECT_INT	when set, indicates P2P beacon NOA index value equal to one interrupt is generated Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
17	P2P_BEACON_NOA_INDX_CHNG_DETECT_INT	The NOA, index field is compared with the index value programmed in p2p_parsing_control register if there is any change the this interrupt is generated Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
16	RXP_RADAR_INTERRUPT	When set, radar detect interrupt will be generated Writing 1 to this bit will clear this interrupt Reset State: 0x00000000
15	RXP_MORE_DATA_SET_INTERRUPT	When set, and a frame is received that passes the filter, is a management, data or QoS data frame and the more data bit in the frame is SET an interrupt pulse will be generated. That status info of the corresponding frame is captured in the other fields more_data_int_control register. Writing 1 to this bit will clear this interrupt this interrupt goes to host only Reset State: 0x00000000
14	RXP_RMF_FRAME_LEN_ERR_INT	When set it indicates that we have received a RMF BC/MC frame with frame less than 48bytes(which is minimum) then this interrupt is generated. Writing 1 to this bit will clear this interrupt this interrupt goes to host only Reset State: 0x00000000

RXP_RXP_GROUPED_INTERRUPT_STATUS (cont.)

Bits	Name	Description
13	RXP_SYSTEM_OUT_OF_MEMORY_INT	when set it indicates system is running out of memory, which allows software to indicate to AP to back off on sending frames by sending frames with PM bit set Writing 1 to this bit will clear this interrupt this interrupt goes to host only Reset State: 0x00000000
12	RXP_MORE_DATA_CLEAR_INTERRUPT	When set, and a frame is received that passes the filter, is a management, data or QoS data frame and the more data bit in the frame is NOT set an interrupt pulse will be generated. That status info of the corresponding frame is captured in the other fields more_data_int_control register. Writing 1 to this bit will clear this interrupt this interrupt goes to host only Reset State: 0x00000000
11	RXP_ADDR2_MISS_INTERRUPT	When set, and a frame is received that has an addr2 miss (and addr 1 is a hit), an 'addr2 miss interrupt will be generated. Writing 1 to this bit will clear this interrupt this interrupt goes to host only Reset State: 0x00000000
10	RXP_MISSED_EOSP_INT	When set, interrupt is generated when at least one other frame with EOSP got received while the first EOSP frame reception got reported Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
9	RXP_EOSP_INT	When set, the EOSP interrupt will get generated if eosp frame is received Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
8	TIM_BIT_CLEAR_INT	When set, beacon has tim bit clear Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
7	TIM_BIT_SET_INT	When set, tim bit set in beacon Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
6	TIM_BEACON_CRC_ERR_INT	When set, beacon has CRC error Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
5	TIM_BASED_BROADCAST_FRAMES_PENDING_INT	When set, indicates tim bit indicates broadcast frames are pending Writing 1 to this bit will clear this interrupt this interrupt goes to firmware only Reset State: 0x00000000
4	ASYNC_FIFO_FULL_ERR_INT	When set, and the async fifo got full Writing 1 to this bit will clear this interrupt this interrupt goes to host only Reset State: 0x00000000
3	GET_BMU_ERR_INT	When set, the interaction with the bmu caused an error Writing 1 to this bit will clear this interrupt this interrupt goes to host only Reset State: 0x00000000

RXP_RXP_GROUPED_INTERRUPT_STATUS (cont.)

Bits	Name	Description
2	INVALID_RATE_INDEX_INT	When set, an invalid rate index is generated based on information from the PHY Writing 1 to this bit will clear this interrupt this interrupt goes to host only Reset State: 0x00000000
1	RPE_DUPL_INTERFACE_TIMEOUT_INT	When set, the rpe duplicate detect interface handshake timeout error has been detected Writing 1 to this bit will clear this interrupt this interrupt goes to host only Reset State: 0x00000000
0	RPE_BITMAP_INTERFACE_TIMEOUT_INT	When set, the rpe bitmap interface handshake timeout error has been detected Writing 1 to this bit will clear this interrupt this interrupt goes to host only Reset State: 0x00000000

0x3000328 RXP_DEFAULT_HW_INSERT_DPU_PARAM

Type: read-write
Reset State: 0x00000000

DPU related parameters to be put in the BD when the "bd_dpu_softmacfields_update_enable" is set and the frame that is received does not cause a hit in the filter, but falls in the unicast/multicast others category, and is still allowed to come in.

RXP_DEFAULT_HW_INSERT_DPU_PARAM

Bits	Name	Description
14:7	DPU_ROUTING_FLAG	The setting for the DPU_routing_flag bits in the BD Reset State: 0x00000000
6:4	DPU_TAG	The setting for the DPU TAG bits in the BD Reset State: 0x00000000
3:1	RX_KEY_ID_BITS	The setting for the RX KEY ID bits in the BD Reset State: 0x00000000
0	NE_BIT	The setting for the NE bit in the BD Reset State: 0x00000000

0x3000344 RXP_PSPOLL_NAV_VALUE

Type: read-write
Reset State: 0x00000000

indicates the NAV value that will be passed on to the MTU when a PSPOLL frame is received

RXP_PSPOLL_NAV_VALUE

Bits	Name	Description
7:0	PSPOLL_NAV_VALUE	The NAV value that will be passed on to the MTU when a PSPOLL frame is received Reset State: 0x00000000

0x3000348 RXP_PMU_INTERFACE_CONTROL

Type: read-write
Reset State: 0x00000000

Controls the PMU interfacing for Beacon Mode Power Save.

RXP_PMU_INTERFACE_CONTROL

Bits	Name	Description
10	PMU_SLEEP_PULSE_GENERATED	When set, a sleep pulse has been generated to the PMU Write 0 to clear this bit Reset State: 0x00000000
9	WAKEUP_ON_BC_TIM_SET_PULSE_GENERATED	When set, a wakeup pulse has been generated to the PMU indicating a beacon is received with the broadcast tim bit set Write 0 to clear this bit Reset State: 0x00000000
8	WAKEUP_ON_STA_TIM_SET_PULSE_GENERATED	When set, a wakeup pulse has been generated to the PMU indicating a beacon is received with the STA tim bit set Write 0 to clear this bit Reset State: 0x00000000
3	SLEEP_ON_BC_TIM_CLEAR	When set, a sleep pulse will be generated to the PMU when a beacon is received with the broadcast tim bit clear NOTE: when both 'pmu_sleep_on_sta_tim_clear' and 'sleep_on_bc_tim_clear' are set, both requirements need to be met in order to generate the sleep pulse Reset State: 0x00000000
2	PMU_SLEEP_ON_STA_TIM_CLEAR	When set, a sleep pulse will be generated to the PMU when a beacon is received with the sta tim bit clear Reset State: 0x00000000
1	WAKEUP_ON_SBC_TIM_SET	When set, a wakeup pulse will be generated to the PMU when a beacon is received with the broadcast tim bit set Reset State: 0x00000000
0	WAKEUP_ON_STA_TIM_SET	When set, a wakeup pulse will be generated to the PMU when a beacon is received with the STA tim bit set Reset State: 0x00000000

0x3000350 RXP_RATE_INDEX_HISTORY

Type: read-only
Reset State: 0x00000000

Gives an overview of the rate indexes of the last 2 frames received

RXP_RATE_INDEX_HISTORY

Bits	Name	Description
24:16	PREVIOUS_RECEIVED_RATE_INDEX	The rate index of the previous frame received Reset State: 0x00000000
8:0	LAST_RECEIVED_RATE_INDEX	The rate index of the last frame received Reset State: 0x00000000

0x3000358 RXP_ADDR2_MISS_INFO

Type: read-only
Reset State: 0x00000000

The lowest 32 bits of the addr 2 received that caused an addr 2 miss interrupt

RXP_ADDR2_MISS_INFO

Bits	Name	Description
31:0	ADDR2_BIT31_0	The lowest 32 bits of the addr 2 received Reset State: 0x00000000

0x300035C RXP_ADDR2_MISS_CTRL

Type: read-only
Reset State: 0x00000000

Addr 2 miss interrupt control and status

RXP_ADDR2_MISS_CTRL

Bits	Name	Description
23:16	ADDR1_INDEX	The corresponding addr 1 index of the frame received Reset State: 0x00000000
15:0	ADDR2_BIT47_32	The upper 16 bits of the addr 2 received Reset State: 0x00000000

0x3000360 RXP_EOSP_INT_CONTROL

Type: read-write
Reset State: 0x00000000

EOSP interrupt control and status

RXP_EOSP_INT_CONTROL

Bits	Name	Description
31	EOSP_INT_ENABLE	When set, and a frame is received that passes the filter and the EOSP bit in the QoS control field is set, an interrupt pulse will be generated. That status info of the corresponding frame is captured in the other fields in this register. Reset State: 0x00000000
30	EOSP_INT_STATUS	When set, the EOSP interrupt got generated Reset State: 0x00000000
29	EOSP_INT_MISSED	When set, at least one other frame with EOSP set got received while the first EOSP frame reception got reported Reset State: 0x00000000
27:24	TID	The tid of the qos control field Reset State: 0x00000000
23:16	ADDR3_INDEX	The Addr 3 index of the frame received Reset State: 0x00000000
15:8	ADDR2_INDEX	The Addr 2 index of the frame received Reset State: 0x00000000
7:0	ADDR1_INDEX	The Addr 1 index of the frame received Reset State: 0x00000000

0x3000364 RXP_MORE_DATA_CLEAR_INT_CONTROL

Type: read-write
Reset State: 0x00000000

More data bit clear interrupt control and status

RXP_MORE_DATA_CLEAR_INT_CONTROL

Bits	Name	Description
31	MORE_DATA_CLEAR_INT_ENABLE	When set, and a frame is received that passes the filter, is a management, data or QoS data frame and the more data bit in the frame is NOT set an interrupt pulse will be generated. That status info of the corresponding frame is captured in the other fields in this register. Reset State: 0x00000000

RXP_MORE_DATA_CLEAR_INT_CONTROL (cont.)

Bits	Name	Description
30	MORE_DATA_CLEAR_INT_STATUS	When set, the more data bit clear interrupt got generated Reset State: 0x00000000
29	MORE_DATA_INT_MISSED	When set, at least one other frame with more data bit clear got received before software got to process the interrupt. while the first EOSP frame reception got reported Reset State: 0x00000000
28	QOS_FRAME	when set indicates it is a qos frame Reset State: 0x00000000
27:24	TID	tid of qos control field Reset State: 0x00000000
23:16	ADDR3_INDEX	The Addr 3 index of the frame received Reset State: 0x00000000
15:8	ADDR2_INDEX	The Addr 2 index of the frame received Reset State: 0x00000000
7:0	ADDR1_INDEX	The Addr 1 index of the frame received Reset State: 0x00000000

0x300036C RXP_CONFIG4

Type: read-write
Reset State: 0x00000000

It contains RXP Configuration registers.

RXP_CONFIG4

Bits	Name	Description
28	WLAN_RX_GRANT	This bit gives status of wlan_rx_grant. Write 1 to this bit to clear it 0: No rx grant generated 1: rx grant is generated Reset State: 0x00000000
27	WLAN_RX_GRANT_ENABLE	This bit is used to enable the wlan_rx grant feature 0: disable the WLAN_RX_Grants control of WLAN RX 1: enable the WLAN_RX_Grants control of WLAN RX Reset State: 0x00000000
26:11	TID_PRIORITY	This bit gives priority for frames on a tid basis this is used in support for Better Qos By default TID 6 and 7 have high priority 1: High priority 0: Low priority Reset State: 0x00000000
10	MANAGEMENT_PRIORITY	This bit gives priority for management frames this is used in support for Better Qos 1: High priority 0: Low priority Reset State: 0x00000000

RXP_CONFIG4 (cont.)

Bits	Name	Description
9	NONQOS_PRIORITY	This bit gives priority for non qos frames this is used in support for Better Qos 1: High priority 0: Low priority Reset State: 0x00000000
8:1	UNKNOWN_MC_STAID	when bit 0 is set then that means we are continuing address2 look up for an unknown multicast so the staid assigned for these types of packet should be set here Reset State: 0x00000000
0	CFG_FLT_ADDR1_BC_ENTRY_PRESENT	When this bit is set it indicates that a broadcast entry is present in address 1 when it is set it allows RXP to accept unknown multicast packets and continue address2 lookup Reset State: 0x00000000

0x3000374 RXP_BEACON_P2P_CLIENT_ADDR_LOW_FIELD

Type: read-write
Reset State: 0x00000000

This register contains the lowest 4 bytes of the address 2 field of the p2p beacon, in case a match function is enabled

RXP_BEACON_P2P_CLIENT_ADDR_LOW_FIELD

Bits	Name	Description
31:0	BEACON_P2P_CLIENT_ADDR_LSB_BYTES	The 4 LS Bytes of the addr2, LE format Reset State: 0x00000000

0x3000378 RXP_BEACON_P2P_CLIENT_ADDR_HIGH_FIELD

Type: read-write
Reset State: 0x00000000

This register contains the highest 2 bytes of the address 3 field of the beacon, in case a match function is enabled

RXP_BEACON_P2P_CLIENT_ADDR_HIGH_FIELD

Bits	Name	Description
15:0	BEACON_P2P_CLIENT_ADDR_MSB_BYTES	The 2 MS Bytes of the addr2, LE format Reset State: 0x00000000

0x300037C RXP_P2P_BEACON_PARSE_CONTROL

Type: read-write
Reset State: 0x09000000

This register contains all the configurations necessary for handling p2p beacon

RXP_P2P_BEACON_PARSE_CONTROL

Bits	Name	Description
31:24	OUI_TYPE_VALUE	This is the OUI type value in P2P IE in the beacon. By default it is 09 indicating it is P2P version 1.0 Reset State: 0x00000009
23:16	NOA_INDEX_VALUE	The Index field value of NOA sub-element in P2P element in beacon RXP will parse the beacon for this index field and if there is any change in value an interrupt is generated. Reset State: 0x00000000
15:5	P2P_ASSOCIATION_ID	The association id of the station for p2p beacons. This field is used to know which tim bit from the TIM element is related to this station Reset State: 0x00000000
2	P2P_BEACON_NOA_PARSING_DIS	as long as riva is configured to receive p2p beacons, no parsing will be done. NOA parsing can be disabled by writing 1 to this bit Reset State: 0x00000000

0x3000380 RXP_MORE_DATA_SET_INT_CONTROL

Type: read-write
Reset State: 0x00000000

More data bit set interrupt related status

RXP_MORE_DATA_SET_INT_CONTROL

Bits	Name	Description
29	MORE_DATA_INT_MISSED	When set, at least one other frame with more data bit set got received before software got to process the interrupt. Reset State: 0x00000000
28	QOS_FRAME	when set indicates it is a qos frame Reset State: 0x00000000
27:24	TID	tid of qos control field Reset State: 0x00000000
23:16	ADDR3_INDEX	The Addr 3 index of the frame received Reset State: 0x00000000

RXP_MORE_DATA_SET_INT_CONTROL (cont.)

Bits	Name	Description
15:8	ADDR2_INDEX	The Addr 2 index of the frame received Reset State: 0x00000000
7:0	ADDR1_INDEX	The Addr 1 index of the frame received Reset State: 0x00000000

0x3000384 RXP_RULE1_CNTR_CTRL

Type: read-write
Reset State: 0x00000000

Has all controls to generate rule1 counter

RXP_RULE1_CNTR_CTRL

Bits	Name	Description
31:28	RULE1_QID_MASK	Only the bit that are set here are considered for counting when mask is set for any bit the corresponding bit in rule1_qid_en is valid Reset State: 0x00000000
27:24	RULE1_QID_EN	Only the bit that are set here are considered for counting Program all the qid bit values that needs to be considered for counting The setting of the bits whose corresponding bits in the rule1_qid_mask are set to 0 are ignored. Reset State: 0x00000000
23:20	RULE1_STAID_MASK	Only the bit that are set here are considered for counting when mask is set for any bit the corresponding bit in rule1_staid_en is valid Reset State: 0x00000000
19:16	RULE1_STAID_EN	Program all the staid bit values that needs to be considered for counting The setting of the bits whose corresponding bits in the rule1_staid_mask are set to 0 are ignored Reset State: 0x00000000
15:10	RULE1_TYPESUBTYPE_MASK	Only the bit that are set here are considered for counting when mask is set for any bit the corresponding bit in rule1_typesubtype_en is valid bits[15:14] = FC type bits[13:10] = FC subtype Reset State: 0x00000000
9:4	RULE1_TYPESUBTYPE_EN	Program all the type/subtype bit values that needs to be considered for counting.The setting of the bits whose corresponding bits in the rule1_typesubtype_mask are set to 0 are ignored. bits[9:8] = FC type bits[7:4] = FC subtype Reset State: 0x00000000
3	RULE1_HT_PRESENT_MASK	When set, ht present/or not present check is enabled Reset State: 0x00000000

RXP_RULE1_CNTR_CTRL (cont.)

Bits	Name	Description
2	RULE1_HT_PRESENT_EN	program the requirement of HT being present or not. This field is ignored if bit rule1_ht_present_mask is not set. Reset State: 0x00000000
0	RULE1_CNTR_EN	when set enables the counter Reset State: 0x00000000

0x3000388 RXP_RULE2_CNTR_CTRL

Type: read-write
Reset State: 0x00000000

Has all controls to generate rule1 counter

RXP_RULE2_CNTR_CTRL

Bits	Name	Description
31:28	RULE2_QID_MASK	Only the bit that are set here are considered for counting when mask is set for any bit the corresponding bit in rule2_qid_en is valid Reset State: 0x00000000
27:24	RULE2_QID_EN	Only the bit that are set here are considered for counting Program all the qid bit values that needs to be considered for counting The setting of the bits whose corresponding bits in the rule2_qid_mask are set to 0 are ignored. Reset State: 0x00000000
23:20	RULE2_STAID_MASK	Only the bit that are set here are considered for counting when mask is set for any bit the corresponding bit in rule2_staid_en is valid Reset State: 0x00000000
19:16	RULE2_STAID_EN	Program all the staid bit values that needs to be considered for counting The setting of the bits whose corresponding bits in the rule2_staid_mask are set to 0 are ignored Reset State: 0x00000000
15:10	RULE2_TYPESUBTYPE_MASK	Only the bit that are set here are considered for counting when mask is set for any bit the corresponding bit in rule2_typesubtype_en is valid bits[15:14] = FC type bits[13:10] = FC subtype Reset State: 0x00000000
9:4	RULE2_TYPESUBTYPE_EN	Program all the type/subtype bit values that needs to be considered for counting.The setting of the bits whose corresponding bits in the rule2_typesubtype_mask are set to 0 are ignored. bits[9:8] = FC type bits[7:4] = FC subtype Reset State: 0x00000000

RXP_RULE2_CNTR_CTRL (cont.)

Bits	Name	Description
3	RULE2_HT_PRESENT_MASK	When set, ht present/or not present check is enabled Reset State: 0x00000000
2	RULE2_HT_PRESENT_EN	program the requirement of HT being present or not. This field is ignored if bit rule2_ht_present_mask is not set. Reset State: 0x00000000
0	RULE2_CNTR_EN	when set enables the counter Reset State: 0x00000000

0x300038C RXP_RULE1_CNTR

Type: read-only
Reset State: 0x00000000

Rule 1 counter, if all conditions in rule1_ctrl pass then this counter gets incremented

RXP_RULE1_CNTR

Bits	Name	Description
7:0	RULE1_CNTR	This counter indicates number of packets received which passes rule 1 control conditions Reset State: 0x00000000

0x3000390 RXP_RULE2_CNTR

Type: read-only
Reset State: 0x00000000

Rule 2 counter, if all conditions in rule2_ctrl pass then this counter gets incremented

RXP_RULE2_CNTR

Bits	Name	Description
7:0	RULE2_CNTR	This counter indicates number of packets received which passes rule 2 control conditions Reset State: 0x00000000

0x3000394 RXP_DROP_DUE_TO_DROP_AT_DMA_CNT

Type: read-only
Reset State: 0x00000000

The number of packets are dropped by RXP due to drop at DMA bit set in type/subtype filter (these are mostly control packets)

RXP_DROP_DUE_TO_DROP_AT_DMA_CNT

Bits	Name	Description
15:0	DROP_DUE_TO_DROP_DMA_CMD_CNT	The number of packets are dropped by RXP due to drop at DMA bit being set these are usually all control packets. Reset State: 0x00000000

0x3000398 RXP_RX_TIME_CNTR

Type: read-only
Reset State: 0x00000000

The number of early pkt detect at every microseconds

RXP_RX_TIME_CNTR

Bits	Name	Description
23:0	RX_TIME_CNT	The number of microseconds that have early pkt detect high Reset State: 0x00000000

0x300039C RXP_SPARE_AND_CLKGATE_DIS

Type: read-write
Reset State: 0x00000000

this register has spare bits and local clock gate disable

RXP_SPARE_AND_CLKGATE_DIS

Bits	Name	Description
23:16	SPARE_BIT	read writable spare bits Reset State: 0x00000000
7:0	BLOCK_CLKGATE_DIS	when set to 1 the block level clock gating is disabled bit0 - phy_proc bit1 - dlm_proc,dlm_fifo bit2 - mpdu_proc,mpdu_hdr,crc32 bit3 - dma_fifo,dma_ctrl bit4 - config bit5 - filter,param_to_mem,binarysearch bit6 - rxi_ctrl,async_fifo Reset State: 0x00000000

0x30003A0 RXP_NDP_PKT_CNTR

Type: read-only
Reset State: 0x00000000

The number of NDP pkts received

RXP_NDP_PKT_CNTR

Bits	Name	Description
15:0	NDP_PKT_CNT	Number of NDP packets received Reset State: 0x00000000

0x30003A4 RXP_P2P_BEACON_PARSE_CONTROL2

Type: read-write
Reset State: 0x00000000

This register contains some more configurations necessary for handling p2p beacon

RXP_P2P_BEACON_PARSE_CONTROL2

Bits	Name	Description
7	NOA_OPPPS_VALUE	This value is set by SW, set 1 indicates group owner is using opportunistic power save, set to 0 indicates that it is disabled This value is compared to that in the beacon any change in this will generate a interrupt Reset State: 0x00000000
6:0	NOA_CTWIN_VALUE	Client Traffic window of value 0-6 is programmed in this register RXP will parse the beacon for this n CTWin of NOA element and if there is any change in value an interrupt is generated. This value is a period of time in TU after TBTT during which P2P group owner is present Reset State: 0x00000000

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0x3000000 TPE_EDCF_TXOP_0_1

Type: read-write
Reset State: 0x06000600

edcf txop corresponds to back-offs 0 and 1

TPE_EDCF_TXOP_0_1

Bits	Name	Description
31:16	EDCF_TXOP_1	TXOP that is used while transmitting mpdus from the q corresponds to back-off 1 This values is in micro seconds. Reset State: 0x00000600
15:0	EDCF_TXOP_0	TXOP that is used while transmitting mpdus from the q corresponds to back-off 0 This values is in micro seconds. Reset State: 0x00000600

0x3000004 TPE_EDCF_TXOP_2_3

Type: read-write
Reset State: 0x06000600

edcf txop corresponds to back-offs 1 and 2

TPE_EDCF_TXOP_2_3

Bits	Name	Description
31:16	EDCF_TXOP_3	TXOP that is used while transmitting mpdus from the q corresponds to back-off 3 This value is in micro seconds. Reset State: 0x00000600
15:0	EDCF_TXOP_2	TXOP that is used while transmitting mpdus from the q corresponds to back-off 2 This value is in micro seconds. Reset State: 0x00000600

0x3000008 TPE_EDCF_TXOP_4_5

Type: read-write
Reset State: 0x06000600

edcf txop corresponds to back-offs 4 and 5

TPE_EDCF_TXOP_4_5

Bits	Name	Description
31:16	EDCF_TXOP_5	TXOP that is used while transmitting mpdus from the q corresponds to back-off 5 This value is in micro seconds. Reset State: 0x00000600
15:0	EDCF_TXOP_4	TXOP that is used while transmitting mpdus from the q corresponds to back-off 4 This value is in micro seconds. Reset State: 0x00000600

0x300000C TPE_EDCF_TXOP_6_7

Type: read-write
Reset State: 0x06000600

edcf txop corresponds to back-offs 6 and 7

TPE_EDCF_TXOP_6_7

Bits	Name	Description
31:16	EDCF_TXOP_7	TXOP that is used while transmitting mpdus from the q corresponds to back-off 7 This value is in micro seconds. Reset State: 0x00000600
15:0	EDCF_TXOP_6	TXOP that is used while transmitting mpdus from the q corresponds to back-off 6 This value is in micro seconds. Reset State: 0x00000600

0x3000010 TPE_SW_TEMPLATE_BASE_ADDR

Type: read-write
Reset State: 0x00005000

This register contains the implicit beamform bkof qosnull template address.

TPE_SW_TEMPLATE_BASE_ADDR

Bits	Name	Description
31:0	SW_BKOF_QOSNULL_TEMPLATE_ADDR	This address is used to specify the implicit beamform bkof qosnull template address. (Was used for hardware template which is removed in Riva). Reset State: 0x00005000

0x3000014 TPE_SW_TPE_HW_CONTROL_REG

Type: read-write
Reset State: 0x01840A01

This register contains all the hardware control config registers. software needs to set them as per hardware requirements. These may be either config for bug fixes or for future feature expansion.

TPE_SW_TPE_HW_CONTROL_REG

Bits	Name	Description
31	IGNORE_TXP_ERROR_INT_ECO	Set '1' to ignore the txp_mim_internal_error_int_p, so tpe won't issue soft reset because of the assertion of the interrupt Reset State: 0x00000000
30:25	RESERVED	Reserved spare register bit Reset State: 0x00000000
24:16	SW_11G_DUPLICATE_CTRL_INDEX_OFFSET	This is same as sw_11g_ctrl_index_offset but is used only for (40Mhz) pkts If 11b stations are in, in 11g protection This sw_11g_duplicate_ctrl_index_offset + 11G Rate index of the ctrl pkt from rate table is used to derive the actual ctrl rate index -- used for RTS,CTS,BAR there is no separate valid bit for duplicate rate. sw_11g_ctrl_index_offset_valid is used Reset State: 0x00000184
11	SW_DTIM_TERMINATE_VALID	when set, dtim will be terminated when p2p/bt/lte termination happened. When cleared, same behavior as in Volans. Reset State: 0x00000001
10	SW_P2P_TX_BOUNDARY_TERMINATE_VALID	when set, TPE will terminate the current transmission when p2p tx boundary txop reaches 0. Reset State: 0x00000000
9	SW_GEN6_3WIRE_VALID	when set, the gen6 bt functionality is enabled to generate wlan_Active Reset State: 0x00000001
8	SW_11G_OFDM_VALID	If this bit is set, the compensation reg is added to duration Also the sifs value in duration calculation is made 10 Reset State: 0x00000000
7:4	SW_11G_OFDM_COMPENSATION	In the case of 11G OFDM, we add 6microseconds to duration. The value is given in Register for flexibility Reset State: 0x00000000
1:0	SW_COMP_DIV_DELAY_REG	The div function delay is specified in this register. Actual MCP is = sw_comp_div_delay_reg+2. By default 1+2=3 cycles Reset State: 0x00000001

0x3000018 TPE_SW_SOFTWARE_TX_CONTROL_REG1

Type: read-write
Reset State: 0x00300000

This register contains the controls needed for software triggered transmission

TPE_SW_SOFTWARE_TX_CONTROL_REG1

Bits	Name	Description
29:24	SW_WAIT_COMMAND2	This register contains the wait command2. This command is used by TXP while sending pkt in the case of TXOP burst, it is used only first time and later onwards follows the station parameters Reset State: 0x00000000
21:16	SW_WAIT_COMMAND1	This register contains the wait command1. The tpe main waits as per this wait command before the request is considered for arbitration. The definition is as per TXP wait command. Any value beyond 21Hex is treated as no wait. by default it is no wait Reset State: 0x00000030
9:7	SW_TX_SESSION_CONTROL	This register contains the type of transmission software wants 000 --> nothing 001 --> data and use back-off index provided by software 010 --> data and use the staid, Qid given by software 011 --> template transmission, addr given by template addr Reset State: 0x00000000
5	SW_TX_RAW_PKT_VALID	if this bit is set the transmission is done in raw pkt mode Reset State: 0x00000000
4	SW_TX_TERMINATE_VALID	during software controlled tx, if this bit is set, the on going transmission will be terminated as if the txop is not available. The current transmission is ended gracefully. Reset State: 0x00000000
3:1	TPE_TX_TIMING_FEEDBACK	the feedback bits from h/w. They will be made zero on start_valid 000 --> Nothing is going on 001 --> waiting in commad1 010 --> command1 is done and command2 is going on 011 --> tx done 111 --> ack to 100 --> aging Reset State: 0x00000000
0	SW_TX_START_VALID	by writing 1 to this bit software indicates to hardware that the software tx controls are valid and hardware should start working on the software request software needs to toggle this by writing 0 and then 1 Reset State: 0x00000000

0x300001C TPE_SW_SOFTWARE_TX_ADDRESS

Type: read-write
Reset State: 0x00005000

This register contains the template address.

TPE_SW_SOFTWARE_TX_ADDRESS

Bits	Name	Description
31:0	SW_SOFTWARE_TX_ADDRESS	S/W programs this register during the software initiated transmission in the case of template transmission, this is templated address session control 001 --> [3:0] = backoff index, other bits are not used [31:16] = txop for this transmission 010 --> [3:0] = QID of the stream [11:4] = STAID [31:16] = txop for this transmission 011 --> [31:0] = template memory address --> template transmission is always txop=0 Reset State: 0x00005000

0x3000020 TPE_SW_MAX_BYTES_AND_TX_TIME_IN_AMPDU

Type: read-write
Reset State: 0x02000200

This register contains the max_tx (in micro sec) time that needs to be considered to terminate the AMPDU

TPE_SW_MAX_BYTES_AND_TX_TIME_IN_AMPDU

Bits	Name	Description
28:16	SW_MAX_AMPDU_TX_TIME	This is the max tx_time that an AMPDU can take. This is another AMPDU termination condition Reset State: 0x00000200
12:0	SW_MAX_AMPDU_TX_TIME_FOR_MIXED_MODE	During the mixed mode, we should not exceed this limit. This is considered in mixed mode only Reset State: 0x00000200

0x3000024 TPE_SW_MAX_MPDUS_IN_AMPDU_AND_MISC

Type: read-write
Reset State: 0x7F000010

This register contains the max no. of mpdus that can be packed in one AMPDU

TPE_SW_MAX_MPDUS_IN_AMPDU_AND_MISC

Bits	Name	Description
31:16	SW_PROTECTION_THR	The threshold that needs to be used for protection... RTS/CTS to self etc Reset State: 0x00007F00

TPE_SW_MAX_MPDUS_IN_AMPDU_AND_MISC (cont.)

Bits	Name	Description
15	SW_TX_AMPDU_TERMINATE_AT_RATE_CHANGE	if this bit is set, Wnever there is a rate change, ampdu will be terminated Reset State: 0x00000000
14	SW_TX_AMPDU_WINDOW_CHECK_VALID	the AMPDU window shcek is done in TX only when this bit is set Once the sata structure init is done in lab also, we can take out this bit. Reset State: 0x00000000
9	SW_CONSIDER_80_MHZ	80MHZ rates are considered only when this bit is set Reset State: 0x00000000
8	SW_GLOBAL_SB_MODE	indicates the side band mode. MAC simply copies this bit in the phy commands This bit is meaningful only when the CB is valid. Reset State: 0x00000000
7	SW_GLOBAL_CB_VALID	40MHZ rates are considered only when this bit is set Reset State: 0x00000000
6:0	SW_MAX_MPDUS_IN_AMPDU	This field indicates the number of MPDUs that can be packed in one AMPDU Reset State: 0x00000010

0x3000028 TPE_SW_STA_DESCR_ADDR

Type: read-write
Reset State: 0x00005000

This register contains the sta descriptor start address

TPE_SW_STA_DESCR_ADDR

Bits	Name	Description
31:0	SW_STA_DESCR_ADDR	the actual start address of descr is sw_sta_descr_addr + staid * (sw_global_no_of_qids * 16*4) Basically 64 bytes are reserved for each sta Reset State: 0x00005000

0x3000030 TPE_SW_TPE_TEST_AND_MISC

Type: read-write
Reset State: 0x00000000

This register contains the test bus select and upper test bus

TPE_SW_TPE_TEST_AND_MISC

Bits	Name	Description
29:21	SW_TPE_TRACE_SELECT_VECTOR	bmu trace controls used internally to control the tracing functionality Reset State: 0x00000000
20:8	SW_TPE_TEST_BUS_UPPER	this contains the upper 13 bits of tpe test bus Reset State: 0x00000000
4:0	SW_TPE_TEST_SEL	this controls the test bus mux selection in tpe 0-> test_bus_0 1-> test_bus_1 ... test_bus_... 0x13 internal_tpe_bus_1 [29:26] - tpe_main_cs_enc (0 is IDLE), [38:33] - tpe_mproc_cs_enc (0 is IDLE) Reset State: 0x00000000

0x3000034 TPE_SW_PM

Type: read-write
Reset State: 0xF096280A

S/W-configurable PM bit

TPE_SW_PM

Bits	Name	Description
31:24	SW_TX_SIFS_A_MODE_CYCLES	The SIFS cycles that needs to be programmed in tXP commands for A and G (non B) mode pkts This number is multiplied by 8 and used internally. F0 corresponds to hex 780 corresponds 1920(decimal) which is 16microseconds. Reset State: 0x000000F0
23:16	SW_TX_SIFS_B_MODE_CYCLES	The SIFS cycles that needs to be programmed in tXP commands for B mode pkts This number is multiplied by 8 and used internally. 96 corresponds to hex x4b0 corresponds 1200(decimal) which is 10microseconds. Reset State: 0x00000096
15	SW_PROMOTE_BT_LOW_PRI	if this bit is set, the lower priority BT is treated as Higher priority This should not be set in normal conditions. I don't think we ever set this bit Provided so that if we get in to any system issues, this can be turned on Reset State: 0x00000000
14	SW_CONSIDER_TXP_ERROR_IN_TPE_ERROR	If this bit is set the tpe_mcu_error includes the TXP Error too Reset State: 0x00000000
13	SW_CONSIDER_RESPONSE_WHILE_WAITING	if this bit is set, response pkt will be sent even tpe is busy Reset State: 0x00000001
12	SW_IGNORE_DMA_INDEX	The dma index from rxp is ignored Reset State: 0x00000000

TPE_SW_PM (cont.)

Bits	Name	Description
11	SW_IGNORE_DMA_CONFIRM	The dma_confirm from RXP is ignored -- to eliminate any potential Hangs in the rxp-tpe interface Reset State: 0x00000001
10	SW_LSIG_PROTECTION_TYPE	If this bit is set the entire TXOP is used for LSIG protection. Otherwise what ever duration is seen in pkt is used for lsig Reset State: 0x00000000
9	SW_LSIG_PROTECTION_VALID	If this bit is set the lsig protection is considered. Entire TXOP or only the next_pkt is done based on lsig_protection_type Reset State: 0x00000000
8	SW_CONSIDER_SECOND_PKT_READ	If this bit is set the next_pkt read and the duration computation for non zero TXOP and frags is done as per spec. Otherwise we don't include next pkt for the computation. This will be removed once the verification is done Reset State: 0x00000000
7	SW_CONSIDER_TX_BOUNDARY_TXOP	if this bit is set, the tx_boundary_txop is considered in TPE Reset State: 0x00000000
6	SW_BT_TERMINATE_VALID	if this bit is set, mproc will terminate if the btc_is_active (after validating it with configs) btc_active_final & sw_bt_terminate_valid = terminate mproc Reset State: 0x00000000
5	SW_CONSIDER_BT_AVAIL_TIME_CNT	if this bit is set, the btc_tpe_avail_time_cnt is considered in tPE Reset State: 0x00000000
4	SW_CONSIDER_BT_LOW_PRI	if this bit is set, the btc low priority request is considered Reset State: 0x00000000
3	SW_CONSIDER_BT_HIGH_PRI	if this bit is set, the btc high priority request is considered Reset State: 0x00000001
2	SW_CONSIDER_WARMUP_DELAY_FOR_SIFS_CMD	If this bit is set, all the sifs_ommand instructions will wait warm_upenable signal from mtu. This is to reduce the warmup pulse width for the cases in which PHY has less delay. Setting this bit to 0 is Taurus com[atible Reset State: 0x00000000
1	SW_BCN_TERMINATE_VALID	if this bit is set, the current transmission will be terminated if it is TBTT time Reset State: 0x00000001
0	SW_PM	Reserved. The pm bit for data is in sta decriptor now. Reset State: 0x00000000

0x3000038 TPE_SW_TPE_TEST_BUS_LOWER

Type: read-only
Reset State: 0x00000000

This register contains the test bus lower 31:0

TPE_SW_TPE_TEST_BUS_LOWER

Bits	Name	Description
31:0	SW_TPE_TEST_BUS_LOWER	this contains the lower 32 bits of tpe test bus Reset State: 0x00000000

0x300003C TPE_SW_11G_CTRL_INDEX_OFFSET

Type: read-write
Reset State: 0x0003FC00

offset for 11g protection rates

TPE_SW_11G_CTRL_INDEX_OFFSET

Bits	Name	Description
31:24	SW_AMPDU_EXTRA_DURATION	This value is added to AMPDU duration if the current one is not last one in the TXOP. Since we don't know the exact duration of the next AMPDU, we just add a constant value. By default it is ZERO Reset State: 0x00000000
18:10	SW_CF_END_TXOP_THR	CF-END Will be sent only if the remaining TXOP is more than this value Default is 255 microseconds Reset State: 0x000000FF
9	SW_11G_CTRL_INDEX_OFFSET_VALID	if this bit is set, sw_11g_ctrl_index_offset is used basically this is nothing but use_11b_protection_mode. Reset State: 0x00000000
8:0	SW_11G_CTRL_INDEX_OFFSET	If 11b stations are in, in 11g protection This sw_11g_index_offset + 11G Rate index of the ctrl pkt from rate table is used to derive the actual ctrl rate index -- used for RTS,CTS,BAR Reset State: 0x00000000

0x3000040 TPE_RATE_TABLE_SRAM_CONTROL

Type: read-write
Reset State: 0x80000000

controls software operations on TPE rate table. To start a read transaction, check first if bit 31 is 1. If 1, then proceed, writing 0 to bit 31, address to [29:21], 0 to bit 1, and 1 to bit 0. When bit 31 turns 1, then read the data bits. To start a write operation, check first if bit 31 is 1. If 1, then proceed, write 0 to bit 31, address to [29:21], data to [20:4], 1 to bit 1, and 1 to bit 0. When bit 31 turns 1, then write is done.

TPE_RATE_TABLE_SRAM_CONTROL

Bits	Name	Description
31	RATE_SRAM_XACT_DONE	1 indicates transaction complete - write to 0 at start of operation Reset State: 0x00000001
29:21	RATE_SRAM_XACT_ADDR	address for software rate table sram read/write Reset State: 0x00000000
20:3	RATE_SRAM_XACT_DATA	rate table sram data [3] - ctrl resp lpe bit ([26] in rate table) [7:4] - ctrl rate index ([17:14] in rate table) [12:8] - cntrl rep tx power ([31:27] in rate table) [16:13] - resp rate index ([35:32] in rate table) [20:17] - 11g cntrl rate index minus 11b base offset ([61:58] in rate table) Reset State: 0x00000000
1	RATE_SRAM_XACT_WRITE_READZ	1 indicates write operation, 0 indicates read operation Reset State: 0x00000000
0	RATE_SRAM_XACT_START	Write only bit that initiates software rate sram transaction Reset State: 0x00000000

0x3000044 TPE_RATE_TABLE_SRAM_CONTROL2

Type: read-write
Reset State: 0x00000000

controls software operations on TPE rate table.

TPE_RATE_TABLE_SRAM_CONTROL2

Bits	Name	Description
9:0	RATE_SRAM_XACT_DATA	rate table sram data [4:0] - upper bits of ctrl rate index ([22:18] in rate table) [9:5] - upper bits of resp rate index ([40:36] in rate table) Reset State: 0x00000000

0x3000050 TPE_SW_BEACON_BASE_ADDR

Type: read-write
Reset State: 0x00005000

This register contains the beacon base address. THIS REGISTER CAN BE REMOVED -- SIMPLY USE THE OFFSET FROM THE TEMPLATE

TPE_SW_BEACON_BASE_ADDR

Bits	Name	Description
31:0	SW_BEACON_BASE_ADDR	S/w needs to program this register based on the chip configuration hardware uses this base address and depending on the sw_beacon_max_size, it derives the beacon addresses for all the bssids accordingly Reset State: 0x00005000

0x3000054 TPE_SW_BEACON_MAX_SIZE_MISC

Type: read-write
Reset State: 0x00000800

This register contains the max size of the beacon. Make sure the size is in bytes but always word boundary, i.e., the lsb 2 bits are always expected to be Zeros

TPE_SW_BEACON_MAX_SIZE_MISC

Bits	Name	Description
22	SW_BCN_UN_LOCK_BY_SW	s/w unlocks the beacon ownership by writing 1 to this register. Typically after updating the beacon, software writes to this register It is write only register Reset State: 0x00000000
21:18	SW_UPDATE_BCN_INDEX	the beacon index that software wants to update Reset State: 0x00000000
17	MAIN_SW_UPDATE_BCN_GNT_BY_HW	h/w grant to the software request to update beacon. Basically after requesting to update a beacon software will poll this register. Once this bit is set software can go ahead and update the beacon template. Once the software changes the beacon it needs to unlock by writing 1 to sw_bcn_un_lock_by_sw Reset State: 0x00000000
16	SW_UPDATE_BCN_REQ	by writing this bit software requests hardware to grant to update beacon. when it is read, main_sw_bcn_update_pending_valid is reflected this bit will be set when software is written but reset by writing to sw_bcn_un_lock_by_sw Reset State: 0x00000000
15:0	SW_BEACON_MAX_SIZE	This register is used to derive the start address of the beacons. This is used in multiple bssid base_address of beacon [index] = sw_beacon_base_addr + index * sw_beacon_max_size Reset State: 0x00000800

0x3000058 TPE_SW_GLOBAL_CF_END_DATA_POWER_TEMPLATE

Type: read-write
Reset State: 0x00000000

TPE_SW_GLOBAL_CF_END_DATA_POWER_TEMPLATE

Bits	Name	Description
30	FEC_MODE	Reset State: 0x00000000
29	LPE_BIT	Reset State: 0x00000000
27:26	SW_CONSIDER_WLAN_RX_FOR_BT_ECO_VECTOR	basically this is config register to enable the ECO in Libra 2.0. While giving channel to BT Low priority request, the RX path (the packet det from PHY) is used. Two bits are provide for pkt_det and rxp filter pass Bit 0 of the vector i.e., bit 26 of this register enables consideration of rxp_tpe_flt_pass in the logic, Bit 1 of the vector i.e., bit 27 of this register enables consideration of rxp_mtu_pktdet_n in the logic, Reset State: 0x00000000
25	AMPDU_VALID	Reset State: 0x00000000
24:20	TX_POWER	Reset State: 0x00000000
18:16	TX_ANTENNA_EN	Reset State: 0x00000000
15:14	STBC_VALID	Reset State: 0x00000000
13	SGI_VALID	Reset State: 0x00000000
12:11	NSS_11B_MODE	Reset State: 0x00000000
8:3	STA_RATE	Reset State: 0x00000000
2:0	STA_MODE	Reset State: 0x00000000

0x3000080 TPE_TPE_BMU_INTERFACE_CNTS

Type: read-only
Reset State: 0x00000000

TPE<->BMU interface counters

TPE_TPE_BMU_INTERFACE_CNTS

Bits	Name	Description
31:24	TPE_BMU_FEEDBACK_CNT	Increments when tpe_bmu_feedback_p is sent. Reset State: 0x00000000
23:16	BMU_TPE_FEEDBACK_DONE_CNT	Increments when bmu_tpe_feedback_done_p is sent. Reset State: 0x00000000
15:8	TPE_BMU_GET_INFO_CNT	Increments when tpe_bmu_get_info_p is sent. Reset State: 0x00000000

TPE_TPE_BMU_INTERFACE_CNTS (cont.)

Bits	Name	Description
7:0	BMU_TPE_GET_INFO_VALID_CNT	Increments when bmu_tpe_get_info_valid_p is sent. Reset State: 0x00000000

0x3000084 TPE_RXP_TPE_INTERFACE_CNTS

Type: read-only
Reset State: 0x00000000

RXP<->TPE interface counters

TPE_RXP_TPE_INTERFACE_CNTS

Bits	Name	Description
31:24	RXP_TPE_FRAME_INFO_CNT	Increments when rxp_tpe_frame_info_p is sent. Reset State: 0x00000000
23:16	RXP_TPE_AMPDU_END_CNT	Increments when rxp_tpe_ampdu_end_p is sent. Reset State: 0x00000000
15:8	RXP_TPE_DMA_CONFIRM_CNT	Increments when rxp_tpe_dma_confirm_p is sent. Reset State: 0x00000000
7:0	RXP_TPE_BAR_INFO_CNT	Increments when rxp_tpe_bar_info_p is sent. Reset State: 0x00000000

0x3000088 TPE_MTU_TPE_INTERFACE_CNTS

Type: read-only
Reset State: 0x00000000

MTU<->TPE interface counters

TPE_MTU_TPE_INTERFACE_CNTS

Bits	Name	Description
23:16	MTU_TPE_BCN_REQ_VALID_CNT	Increments when mtu_tpe_bcn_req_valid_p is sent. Reset State: 0x00000000
15:8	MTU_TPE_REQ_VALID_CNT	Increments when mtu_tpe_req_valid_p is sent. Reset State: 0x00000000
7:0	TPE_MTU_FEEDBACK_VALID_CNT	Increments when tpe_mtu_feedback_valid_p is sent. Reset State: 0x00000000

0x300008C TPE_RPE_TPE_INTERFACE_CNTS

Type: read-only
Reset State: 0x00000000

RPE<->TPE interface counters

TPE_RPE_TPE_INTERFACE_CNTS

Bits	Name	Description
15:8	TPE_RPE_BITMAP_REQ_CNT	Increments when tpe_rpe_bitmap_req_p is sent. Reset State: 0x00000000
7:0	RPE_TPE_BITMAP_VLD_CNT	Increments when rpe_tpe_bitmap_vld_p is sent. Reset State: 0x00000000

0x3000090 TPE_ERROR_INT_CNTS

Type: read-only
Reset State: 0x00000000

Error counters

TPE_ERROR_INT_CNTS

Bits	Name	Description
23:16	MPROC_ERROR2_CNT	Reset State: 0x00000000
15:8	MPROC_ERROR1_CNT	Reset State: 0x00000000
7:0	TXP_ERROR_INT_CNT	Increments when txp signals error interrupt Reset State: 0x00000000

0x30000C0 TPE_UNICAST_BYTES_LOWER

Type: read-only
Reset State: 0x00000000

lower unicast bytes

TPE_UNICAST_BYTES_LOWER

Bits	Name	Description
31:0	TX_UNICAST_BYTES_LOWER	Reset State: 0x00000000

0x30000C4 TPE_UNICAST_BYTES_UPPER

Type: read-only
Reset State: 0x00000000

upper unicast bytes

TPE_UNICAST_BYTES_UPPER

Bits	Name	Description
31:0	TX_UNICAST_BYTES_UPPER	Reset State: 0x00000000

0x30000C8 TPE_MULTICAST_BYTES_LOWER

Type: read-only
Reset State: 0x00000000

lower multicast bytes

TPE_MULTICAST_BYTES_LOWER

Bits	Name	Description
31:0	TX_MULTICAST_BYTES_LOWER	Reset State: 0x00000000

0x30000CC TPE_MULTICAST_BYTES_UPPER

Type: read-only
Reset State: 0x00000000

upper multicast bytes

TPE_MULTICAST_BYTES_UPPER

Bits	Name	Description
31:0	TX_MULTICAST_BYTES_UPPER	Reset State: 0x00000000

0x30000D0 TPE_BROADCAST_BYTES_LOWER

Type: read-only
Reset State: 0x00000000

lower broadcast bytes

TPE_BROADCAST_BYTES_LOWER

Bits	Name	Description
31:0	TX_BROADCAST_BYTES_LOWER	Reset State: 0x00000000

0x30000D4 TPE_BROADCAST_BYTES_UPPER

Type: read-only
Reset State: 0x00000000

upper broadcast bytes

TPE_BROADCAST_BYTES_UPPER

Bits	Name	Description
31:0	TX_BROADCAST_BYTES_UPPER	Reset State: 0x00000000

0x3000100 TPE_STATISTIC_COUNTERS_CNTL

Type: read-write
Reset State: 0x00000004

statistic counters control

TPE_STATISTIC_COUNTERS_CNTL

Bits	Name	Description
2	COPY_VISTA_COUNTERS	copy 64 vista counters over into stats registers Reset State: 0x00000001
1	CLEAR_VISTA_COUNTERS	clear vista counters Reset State: 0x00000000
0	CLEAR_GLOBAL_COUNTERS	clear global counters Reset State: 0x00000000

0x3000104 TPE_TPE_STATUS_REG_LOWER

Type: read-only
Reset State: 0x00000000

tpe status - should be all 0 when idle and da are all 0

TPE_TPE_STATUS_REG_LOWER

Bits	Name	Description
31:0	TPE_STATUS	uspu_testbus[4:0], // 32:28 uspm_testbus[5:0], // 27:22 wpg_testbus[4:0], // 21:17 twr_testbus[5:0], // 16:11 tpe_mproc_test[5:0], // 10:5 tpe_main_test[22:18] // 4:0 Reset State: 0x00000000

0x3000108 TPE_TPE_STATUS_REG_UPPER

Type: read-only
Reset State: 0x00000000

tpe status upper - should be all 0 when idle and da are all 0 mtu_tpe_response_to, // 44 bmu_tpe_bo_data_avail[5:0], // 43:38 usps_testbus[4:0], // 37:33

TPE_TPE_STATUS_REG_UPPER

Bits	Name	Description
12:0	TPE_STATUS	Reset State: 0x00000000

0x3000110 TPE_GOT_ACK_FOR_BACK_INFO_REG

Type: read-only
Reset State: 0x00000000

staid, qid for got_ack_for_back_info interrupt got ack for back staid got ack for back qid

TPE_GOT_ACK_FOR_BACK_INFO_REG

Bits	Name	Description
12:5	GOT_ACK_FOR_BACK_STAID	Reset State: 0x00000000
4:0	GOT_ACK_FOR_BACK_QID	Reset State: 0x00000000

0x3000118 TPE_SW_DELAY_WAIT_CMD_CNT_REG

Type: read-write
Reset State: 0xFF1E801E

This is used to delay the wait command (so that the warmup pulse can be sent ahead in time This is in terms of 8 clk cycles, so a value of 'd30 would mean 240 clk cycles, or 2us For beacons,

Template tx, the transmission will happen immediately This is a problem for Warm up. We can't use pifs because the trigger to TPE already after pifs_to. send warmup later when we send wait_cycles (e.g. after cts-to-self) instead of right at the beginning of sifs. this "later" is determined by sw_wait_cycles_threshold (in terms of 8 cycles). This value is number of clocks before we send warmup. we will be delaying the wait command, sending warmup, and then sending the wait command with sw_wait_cycles_threshold to the txp. The default value is 240 cycles, which is 2 us (in terms of 16 us). The sw_template request if not sent after this threshold time will be dropped

TPE_SW_DELAY_WAIT_CMD_CNT_REG

Bits	Name	Description
31:24	SW_AGING_CNT_THRSHLD	Reset State: 0x000000FF
23:16	SW_WAIT_CYCLES_THRESHOLD	Reset State: 0x0000001E
15	SW_SEND_WARMUP_LATER_EN	Reset State: 0x00000001
13:8	SW_DELAY_CYCLE_FOR_NO_WAIT_TX	Reset State: 0x00000000
5:0	SW_DELAY_WAIT_CMD_CNT	Reset State: 0x0000001E

0x300011C TPE_SW_MEDIUM_TIME_USED_AC0

Type: read-write
Reset State: 0x00000000

This register contains the medium time used for AC0 This is internal to h/w. software can write to these register at its risk. Basically the corresponding AC should not be enabled for Admission control while updating this register (update should be only only in debug mode). To make sure that there are no side effects, software needs to disable the hardware control over the backoffs by writing appropriate value to sw_mtu_bckof_disable_valid_vector Medium time used for AC0. Each count corresponds to 32microseconds

TPE_SW_MEDIUM_TIME_USED_AC0

Bits	Name	Description
15:0	SW_MEDIUM_TIME_USED_AC0	Reset State: 0x00000000

0x3000120 TPE_SW_MEDIUM_TIME_USED_AC1

Type: read-write
Reset State: 0x00000000

This register contains the medium time used for AC1 This is internal to h/w. software can write to these register at its risk. Basically the corresponding AC should not be enabled for Admission control while updating this register (update should be only in debug mode.) To make sure that there are no side effects, software needs to disable the hardware control over the backoffs by writing appropriate value to sw_mtu_bckof_disable_valid_vector Medium time used for AC1. Each count corresponds to 32microseconds

TPE_SW_MEDIUM_TIME_USED_AC1

Bits	Name	Description
15:0	SW_MEDIUM_TIME_USED_AC1	Reset State: 0x00000000

0x3000124 TPE_SW_MEDIUM_TIME_USED_AC2

Type: read-write
Reset State: 0x00000000

This register contains the medium time used for AC2 This is internal to h/w. software can write to these register at its risk. Basically the corresponding AC should not be enabled for Admission control while updating this register (update should be only in debug mode.) To make sure that there are no side effects, software needs to disable the hardware control over the backoffs by writing appropriate value to sw_mtu_bckof_disable_valid_vector Medium time used for AC2. Each count corresponds to 32microseconds

TPE_SW_MEDIUM_TIME_USED_AC2

Bits	Name	Description
15:0	SW_MEDIUM_TIME_USED_AC2	Reset State: 0x00000000

0x3000128 TPE_SW_MEDIUM_TIME_USED_AC3

Type: read-write
Reset State: 0x00000000

This register contains the medium time used for AC3 This is internal to h/w. software can write to these register at its risk. BasicallyBasically the corresponding AC should not be enabled for Admission control while updating this register(update should be only only in debug mode.) To make sure that there are no side effects, software needs to disable the hardware control over the backoffs by writing appropriate value to sw_mtu_bckof_disable_valid_vector Medium time used for AC3. Each count corresponds to 32microseconds

TPE_SW_MEDIUM_TIME_USED_AC3

Bits	Name	Description
15:0	SW_MEDIUM_TIME_USED_AC3	Reset State: 0x00000000

0x300012C TPE_SW_MEDIUM_TIME_THR_AC0_AC1

Type: read-write
Reset State: 0xEFFFEFFF

This register contains the medium time threshold used for AC0 and AC1 Though the register will be written immediately, the internal logic will take this value at next one second pulse or or when a pkt has been transmitted from the correponding AC Medium time threshold for AC0. Each count corresponds to 32microseconds Medium time threshold for AC1. Each count corresponds to 32microseconds

TPE_SW_MEDIUM_TIME_THR_AC0_AC1

Bits	Name	Description
31:16	SW_MEDIUM_TIME_THR_AC1	Reset State: 0x0000EFFF
15:0	SW_MEDIUM_TIME_THR_AC0	Reset State: 0x0000EFFF

0x3000130 TPE_SW_MEDIUM_TIME_THR_AC2_AC3

Type: read-write
Reset State: 0xEFFFEFFF

This register contains the medium time threshold used for AC2 and AC3 Though the register will be written immediately, the internal logic will take this value at next one second pulse or or when a pkt has been transmitted from the correponding AC Medium time threshold for AC2. Each count corresponds to 32microseconds Medium time threshold for AC3. Each count corresponds to 32microseconds

TPE_SW_MEDIUM_TIME_THR_AC2_AC3

Bits	Name	Description
31:16	SW_MEDIUM_TIME_THR_AC3	Reset State: 0x0000EFFF
15:0	SW_MEDIUM_TIME_THR_AC2	Reset State: 0x0000EFFF

0x3000134 TPE_SW_ADMISSION_CONTROL_CONTROL_REG

Type: read-write
Reset State: 0x0000E4E4

This register contains the control for Admission Control feature. Basically it contains the back-off to AC mapping and enables to Admission control The AC that needs to be used for back-off 0, 1, 2, ...7 [1:0] -> bkof0, [3:2] ->bakof1,..[15:14]--> bkof7 Enable bits for Admission control. [16] --> bkof0, [17]-> bkof 1, [23] -> bkof 7 Only the traffic that corresponds to the back-off for which the enable is set is considered for admission control Enable bits for backoff disable control. [24] --> bkof0, [25]-> bkof 1, [26] -> bkof 27 This is override to disable back-off. Bug protection + also used if software wants to update the sw_medium_time_used_acs.

TPE_SW_ADMISSION_CONTROL_CONTROL_REG

Bits	Name	Description
31:24	SW_MTU_BCKOF_DISABLE_VALID_VECTOR	Reset State: 0x00000000
23:16	SW_AC_VALID_FOR_BKOF_VECTOR	Reset State: 0x00000000
15:0	SW_AC_TO_BKOF_LOOKUP_VECTOR	Reset State: 0x0000E4E4

0x300013C TPE_SW_LIFE_TIME_DROP_CNT

Type: read-write
Reset State: 0x00000000

Counter that counts the dropped pkts due to life time enforcement Whenever a pkt is dropped due to life time enforce ment, this count will be incremented. Writining to this register clears the counter. software is given higher priority over h/w

TPE_SW_LIFE_TIME_DROP_CNT

Bits	Name	Description
31:0	SW_LIFE_TIME_DROP_CNT	Reset State: 0x00000000

0x3000140 TPE_TPE_MCU_BD_BASED_TX_INT_FEEDBACK

Type: read-only
Reset State: 0x00000000

Contains the feedback info for the bd based tx interrupt [0] is ack_to_valid [2:0] feedback taht is sent to bmu -- Definition is as follows. S/w Doesn't need this. Kept this for any debug purpose and if software comes up with new requirement in future, these can be used TPE_BMU_FB_RESET

3'b000 TPE_BMU_FB_DROP 3'b001 TPE_BMU_FB_DROP_AND_REARB 3'b010 TPE_BMU_FB_RESET_AND_REARB 3'b011 TPE_BMU_FB_RESET_AND_CHK_RETRY 3'b100 TPE_BMU_FB_RESET_CHK_RTRY_AND_REARB 3'b101 TPE_BMU_FB_RESET_AND_REARB_UPDATE_RETRY 3'b110

TPE_TPE_MCU_BD_BASED_TX_INT_FEEDBACK

Bits	Name	Description
3:0	TPE_MCU_BD_BASED_TX_INT_FEEDBACK	Reset State: 0x00000000

0x3000144 TPE_TPE_MCU_BD_BASED_TX_INT_FEEDBACK_1

Type: read-only
Reset State: 0x00000000

Contains the feedback info for the bd based tx interrupt [0] is ack_to_valid [2:0] feedback taht is sent to bmu -- Definition is as follows. S/w Doesn't need this. Kept this for any debug purpose and if software comes up with new requirement in future, these can be used TPE_BMU_FB_RESET 3'b000 TPE_BMU_FB_DROP 3'b001 TPE_BMU_FB_DROP_AND_REARB 3'b010 TPE_BMU_FB_RESET_AND_REARB 3'b011 TPE_BMU_FB_RESET_AND_CHK_RETRY 3'b100 TPE_BMU_FB_RESET_CHK_RTRY_AND_REARB 3'b101 TPE_BMU_FB_RESET_AND_REARB_UPDATE_RETRY 3'b110

TPE_TPE_MCU_BD_BASED_TX_INT_FEEDBACK_1

Bits	Name	Description
3:0	TPE_MCU_BD_BASED_TX_INT_FEEDBACK_1	Reset State: 0x00000000

0x3000148 TPE_WRONG_BA_SSN_TID_FEEDBACK

Type: read-only
Reset State: 0x00000000

Contains the feedback info for the wrong BA interrupt. For the BAR sent, it a BA is received with different SSN or TID, an interrupt is set This register contains the Staid and tid of the corresponding flow This contains the station id of the flow for which a wrong BA is received This contains the tid of the flow for which a wrong BA is received

TPE_WRONG_BA_SSN_TID_FEEDBACK

Bits	Name	Description
11:8	WRONG_BA_TID_FEEDBACK	Reset State: 0x00000000

TPE_WRONG_BA_SSN_TID_FEEDBACK (cont.)

Bits	Name	Description
7:0	WRONG_BA_STAID_FEEDBACK	Reset State: 0x00000000

0x300014C TPE_SW_CAPPED_POWER_CONTROL

Type: read-write
Reset State: 0x00000000

This register contains the capped power controls -- bit vector and the capped power Station bit vector for capped power. If the corresponding bit is set, only then the capped power is used for the data and ack The capped power. The power that needs to be used for data and ack. Note the minimum of this and the one specified in R2P is used The capped power is used only if the corresponding bit is set Bit 0 is for All response pkts -- ack, ba, cts in respnse to RTS Bit 1 is for RTS,CTS to self Bit 2 is for the rest of types

TPE_SW_CAPPED_POWER_CONTROL

Bits	Name	Description
26:24	SW_PKT_BASED_POWER_BITMAP	Reset State: 0x00000000
20:16	SW_CAPPED_POWER_VALUE	Reset State: 0x00000000
15:0	SW_CAPPED_POWER_BIT_MAP	Reset State: 0x00000000

0x3000150 TPE_SW_ACK_TO_DUE_TO_BTC_COUNT

Type: read-write
Reset State: 0x00000000

A counter which increments every time when there is ack_to due to BTC Whenever there is ack_to due to BTC, this counter is ++

TPE_SW_ACK_TO_DUE_TO_BTC_COUNT

Bits	Name	Description
15:0	SW_ACK_TO_DUE_TO_BTC_COUNT	Reset State: 0x00000000

0x3000154 TPE_SW_LOW_PRIORITY_BT_REJECTED_COUNT

Type: read-write
Reset State: 0x00000000

A counter which ++ whenever the low priority BT is rejected due to the wlan is busy Whenever there is no grant to BT due to the wlan is busy (for low priority BT) this counter increments

TPE_SW_LOW_PRIORITY_BT_REJECTED_COUNT

Bits	Name	Description
15:0	SW_LOW_PRIORITY_BT_REJECTED_COUNT	Reset State: 0x00000000

0x3000158 TPE_SW_TERMINATE_CURRENT_TX_VALID

Type: read-write
Reset State: 0x00000000

To support terminate at TBTT in STA mode

TPE_SW_TERMINATE_CURRENT_TX_VALID

Bits	Name	Description
0	SW_TERMINATE_CURRENT_TX_VALID	If this bit is set, tpe will terminate the current transmisson. Basically this needs to be used by software when the chip is in station mode. Though we lived with this in earlier chips, it is realized that we might occupy the channel such that the AP might delay the beacons which is not good for the power save of other stations. Basically software simply have tsf based timers to trigger TBTT and enable this bit. This is not a sticky bit. This bit is reset if the tpe is in idle Reset State: 0x00000000

0x300015C TPE_RTT_REGISTER

Type: read-write
Reset State: 0x00000000

RTT registers for InNav Positioning

TPE_RTT_REGISTER

Bits	Name	Description
31	RTT_INFO_VALID	When set to 1, this RTT register contains new valid information. The software can clear this bit by writing '0'. Reset State: 0x00000000
30:24	FIR0_RSSI	The measured RSSI value from FIR-0 Reset State: 0x00000000
23:16	SNR	The measured SBR value Reset State: 0x00000000
15:10	TX_STAID	The TX STAID corresponding to this measurement Reset State: 0x00000000
9:0	RTT	The measured RTT value in 40MHz clk cycles Reset State: 0x00000000

0x3000160 TPE_BEAMFORM_CTRL

Type: read-write
Reset State: 0x00000000

Contains the control signals for calibration and beamform

TPE_BEAMFORM_CTRL

Bits	Name	Description
31:26	RESERVED	Move to ndp_beamform_ctrl.sounding_frame_response_rate_index due to bit-width increased because of new rate. Reset State: 0x00000000
25	CLEAR_WAITING_FOR_SENDING_QOSNULL	In software controlled implicit beamform, software has to write this bit so new qosnull request will be accepted software can also use this to clear the waiting if anything goes wrong Reset State: 0x00000000
24	ENABLE_MPI_CSI_EN	The mcfg_phycsxi_xfercsi_nonndp will be always on (as a backup if anything goes wrong). Reset State: 0x00000000
23	CLEAR_WAITING_FOR_SENDING_CSI	In software controlled calibration/explicit beamform, software has to write this bit so new csi request will be accepted software can also use this to clear the waiting if anything goes wrong Reset State: 0x00000000
22	EXPLICIT_IMMIDIATE_CTS_RSP_EN	When set, the 'cts response' explicit beamform will be acked with immediate cts and later ack+csi feedback, regardless of the setting in bit19. This is not currently implemented. It's here as a place holder. When cleared, delayed feedback will be used if bit19 is set. Reset State: 0x00000000

TPE_BEAMFORM_CTRL (cont.)

Bits	Name	Description
21	EXPLICIT_IMMIDIATE_ACK_RSP_EN	When set, the ack 'response ' explicit beamform will be acked with immediate ack/ba+csi feedback, regardless the setting in bit19. When cleared, delayed feedback will be used if bit19 is set. Reset State: 0x00000000
20	EXPLICIT_IMMIDIATE_NO_RSP_EN	When set, the 'no response' explicit beamform will be acked with immediate csi feedback, regardless the setting in bit19. When cleared, delayed feedback will be used if bit19 is set. Reset State: 0x00000000
19	HW_EXPLICIT_BEAMFORM_DELAY_FEEDBACK	Set to '1' to enable the hardware control csi delayed feedback for explicit beamform (when the support is enabled, and not ruled by the immediate feedback bits). Reset State: 0x00000000
18	EXPLICIT_BEAMFORM_EN	Set to '1' to enable the CSI explicit beamform support. Reset State: 0x00000000
17:14	SENDING_BKOF_QOSNULL_RETRY_THRSHLD	To setup the retry threshold when sending the bkof qosnull in hardware-controlled implicit beamform mode. Reset State: 0x00000000
13:10	SENDING_BKOF_CSI_RETRY_THRSHLD	To setup the retry threshold when sending the bkof csi in hardware-controlled calibration and explicit beamform mode. Reset State: 0x00000000
7	SW_NONCOMPRESSED_EXPLICIT_BEAMFORM_EN	When set, software control noncompressed explicit beamform is enabled. Note no hardware support for this mode. Reset State: 0x00000000
6	SW_COMPRESSED_EXPLICIT_BEAMFORM_EN	When set, software control compressed explicit beamform is enabled. Note no hardware support for this mode. Reset State: 0x00000000
5	HW_CONTROLLED_IMPLICIT_BEAMFORM_EN	When set, implicit is under hardware control. If a qosnull is waiting to be sent and bakoff 6 expires. The qosnull will be sent. Reset State: 0x00000000
4	HW_CONTROLLED_CALIBRATION_EN	When set, calibration is under hardware control. If a csi is waiting to be sent and bakoff 7 expires. The csi will be sent. Reset State: 0x00000000
3	IGNORE_CSI_FIELD_FOR_CAL_START_NDP	Set to '1' to ignore the csi field for ndp based calibration cal start frame Reset State: 0x00000000
2	SW_SEND_NDP2_VALID	Set to '1' to force the hardware to send the ndp frame to respond to the ndp frame in the ndp based calibration. The first response for this frame exchange will be a normal ack/cts. Clear to '0' so no ndp is sent. The first response for the ndp based calibration will be a sounding frame. Reset State: 0x00000000
1	IMPLICIT_BEAMFORM_EN	Set to '1' to enable implicit beamform support Reset State: 0x00000000

TPE_BEAMFORM_CTRL (cont.)

Bits	Name	Description
0	SW_CALIBRATION_FRAME_EXCHANGE_ENABLED	Set to '1' to enable calibration support Reset State: 0x00000000

0x3000164 TPE_CFG_CSI_ADDR

Type: read-write
Reset State: 0x00000000

Contains the address of the CSI template

TPE_CFG_CSI_ADDR

Bits	Name	Description
31:0	CFG_CSI_ADDR	Contains the address of the CSI frame template Reset State: 0x00000000

0x3000168 TPE_INTERRUPT_ENABLE

Type: read-write
Reset State: 0x00000000

Contains the enable bits for which interrupt has to be generated

TPE_INTERRUPT_ENABLE

Bits	Name	Description
10	SW_TEMPLATE_WRONG_CMD_INT_EN	Set to '1' to enable the invalid software command interrupt Reset State: 0x00000000
9	EXPLICITBF_QOSNULL_INT_EN	Set to '1' to enable the explicit beamform qosnull+ndp interrupt when the ndp is received followed by the qosnull request frame. Reset State: 0x00000000
8	SW_TEMPLATE_SENT_INT_EN	Set to '1' to enable interrupt after software template is sent Reset State: 0x00000000
7	GOT_ACK_FOR_BACK_INT_EN	Set to '1' to enable got_ack_for_back interrupt when expecting ba but received ack Reset State: 0x00000000
6	ERROR_VALID_INT_EN	Set to '1' to enable error interrupt. It can be either the mproc enters error state (pkt length is '0' for non qosnull/datanull pkt), or when enabled by sw, the txp timeout or internal error interrupts Reset State: 0x00000000

TPE_INTERRUPT_ENABLE (cont.)

Bits	Name	Description
5	WRONG_SSN_OR_TID_ERROR_INT_EN	Set to '1' to enable wrong_ssn_or_tid interrupt when bar is sent and the tid/ssn of the received ba are not matched Reset State: 0x00000000
4	NONCOMPRESSED_EXPLICIT_BEAMFORM_INT_EN	Set to '1' to enable noncompressed explicit beamform interrupt for sw-controlled non compressed explicit beamform transmission Reset State: 0x00000000
3	COMPRESSED_EXPLICIT_BEAMFORM_INT_EN	Set to '1' to enable compressed explicit beamform interrupt for sw-controlled compressed explicit beamform transmission Reset State: 0x00000000
2	CSI_EXPLICIT_BEAMFORM_INT_EN	Set to '1' to enable csi explicit beamform interrupt for software controlled delayed csi explicit beamform transmission Reset State: 0x00000000
1	IMPLICIT_BEAMFORM_INT_EN	Set to '1' to enable implicit beamform interrupt for software controlled non-SIFS sounding frame transmission Reset State: 0x00000000
0	CALIBRATION_INT_EN	Set to '1' to enable calibration interrupt for software controlled calibration CSI frame transmission Reset State: 0x00000000

0x300016C TPE_INTERRUPT_STATUS

Type: read-write
Reset State: 0x00000000

Contains the interrupt status, writing 1 to any bit will clear the corresponding interrupt

TPE_INTERRUPT_STATUS

Bits	Name	Description
10	SW_TEMPLATE_WRONG_CMD_INT_STATUS	When set, indicates that there's an invalid software template command Write '1' to clear the interrupt. Reset State: 0x00000000
9	EXPLICITBF_QOSNULL_INT_STATUS	When set, indicates that explicit bf qosdata+ndp frame exchange is received Write '1' to clear the interrupt. Reset State: 0x00000000
8	SW_TEMPLATE_SENT_INT_STATUS	When set, indicates that software template transmit is completed Write '1' to clear the interrupt. Reset State: 0x00000000
7	GOT_ACK_FOR_BACK_INT_STATUS	When set, indicates that when expecting ba but received ack Write '1' to clear the interrupt. Reset State: 0x00000000

TPE_INTERRUPT_STATUS (cont.)

Bits	Name	Description
6	ERROR_VALID_INT_STATUS	When set, indicates the mproc error state, or when enabled by sw, the txp timeout or internal error interrupts Write '1' to clear the interrupt. Reset State: 0x00000000
5	WRONG_SSN_OR_TID_ERROR_INT_STATUS	When set, indicates that bar is sent and the tid/ssn of the received ba are not matched Write '1' to clear the interrupt. Reset State: 0x00000000
4	NONCOMPRESSED_EXPLICIT_BEAMFORM_INT_STATUS	When set, indicates the noncompressed explicit beamform frame request is received. software has to control the non compressed explicit beamform transmission Write '1' to clear the interrupt. Reset State: 0x00000000
3	COMPRESSED_EXPLICIT_BEAMFORM_INT_STATUS	When set, indicate the compressed explicit beamform frame req is received. software has to control the compressed explicit beamform transmission Write '1' to clear the interrupt. Reset State: 0x00000000
2	CSI_EXPLICIT_BEAMFORM_INT_STATUS	When set, indicates the explicit beamform frame is received. software has to control the delayed csi explicit beamform transmission Write '1' to clear the interrupt. Reset State: 0x00000000
1	IMPLICIT_BEAMFORM_INT_STATUS	When set, indicates the implicit beamform frame is received. software has to send the non-SIFS sounding frame transmission at bkof Write '1' to clear the interrupt. Reset State: 0x00000000
0	CALIBRATION_INT_STATUS	When set, indicates the calibration frame exchange step1 is done. software has to control the CSI frame transmission Write '1' to clear the interrupt. Reset State: 0x00000000

0x3000170 TPE_BEAMFORM_STATUS

Type: read-only
Reset State: 0x00000000

Contains the status for calibration and beamform.

TPE_BEAMFORM_STATUS

Bits	Name	Description
25	WAITING_FOR_SEND_QOSNULL	A qosnull is waiting to be sent. Hardware won't accept any new qosnull request until the signal is cleared by 1. qosnull is sent. 2. dropped due to retry limit 3. software write to the clear register bit Reset State: 0x00000000

TPE_BEAMFORM_STATUS (cont.)

Bits	Name	Description
24	WAITING_FOR_SEND_CSI	A CSI is waiting to be sent. Hardware won't accept any new csi request until the signal is cleared by 1. csi is sent. 2. csi is dropped due to retry limit 3. software write to the clear register bit Reset State: 0x00000000
23:20	SENDING_QOSNULL_CSI_RETRY_CNT	Retry counter for the bkof qosnull Reset State: 0x00000000
19:16	SENDING_BKOF_CSI_RETRY_CNT	Retry counter for the bkof csi Reset State: 0x00000000
15:8	ADDR2_STAID	The addr2_staid for software to send the bkof qosnull in software controlled implicit beamform Reset State: 0x00000000
7:0	ADDR1_STAID	The addr1_staid for software to send the bkof qosnull in software controlled implicit beamform Reset State: 0x00000000

0x3000174 TPE_CALIBRATION_CNT

Type: read-only
Reset State: 0x00000000

Contains the debug counter for calibration

TPE_CALIBRATION_CNT

Bits	Name	Description
23:16	CALIBRATION_SENT_CNT	Calibration sent count, increase when the bkof csi is sent or dropped. Reset State: 0x00000000
15:8	CALIBRATION_ABORT_CNT	Calibration abort count, increase when calibration complete frame is not received Reset State: 0x00000000
7:0	CALIBRATION_REQ_CNT	Calibration request count Reset State: 0x00000000

0x3000178 TPE_BEAMFORM_CNT

Type: read-only
Reset State: 0x00000000

Contains the debug counter for implicit/explicit beamform`

TPE_BEAMFORM_CNT

Bits	Name	Description
31:24	EXPLICIT_BEAMFORM_CSI_SENT_CNT	Explicit Beamform sent count, increase when the bkof csi is sent or dropped Reset State: 0x00000000
23:16	EXPLICIT_BEAMFORM_REQ_CNT	Explicit beamform request count Reset State: 0x00000000
15:8	IMPLICIT_BEAMFORM_QOSNULL_SENT_CNT	Implicit Beamform sent count, increase when the bkof qosnull is sent or dropped Reset State: 0x00000000
7:0	IMPLICIT_BEAMFORM_REQ_CNT	Implicit Beamform request count Reset State: 0x00000000

0x300017C TPE_SW_PM_2

Type: read-write
Reset State: 0x00000000

sw controlled pm bit

TPE_SW_PM_2

Bits	Name	Description
7:0	SW_PM	SW configurable PM bit for control/response frame which were sent by hardware template before. bit0 - ACK. bit1 - RTS. bit2 - CTS. bit3 - BAR. bit4 - BA. bit5 - CF_END bit6 - ACK CTRL WRAPPER. bit7 - CTS CTRL WRAPPER. Reset State: 0x00000000

0x3000198 TPE_SW_11AC_PADDING

Type: read-write
Reset State: 0x00000000

The SMDA version of A-MPDU delimiters to fill in the last ofdm symbol for 11ac

TPE_SW_11AC_PADDING

Bits	Name	Description
31:0	SW_11AC_PADDING_CONTENTS	The SMDA version of A-MPDU delimiters to fill in the last ofdm symbol for 11ac Reset State: 0x00000000

0x30001B0 TPE_NDP_BEAMFORM_CTRL

Type: read-write
Reset State: 0x00000000

Contains the control signals for beamform qosnull + ndp

TPE_NDP_BEAMFORM_CTRL

Bits	Name	Description
12:4	SOUNDING_FRAME_RESPONSE_RATE_INDEX	To be used in a sounding frame response when the response rate from the rate table is 11b or 11g rate. Reset State: 0x00000000
3	ENABLE_MPI_NDP_EN	The mcfg_phycsxi_xfercsi_ndp will be always on (as a backup if anything goes wrong). Reset State: 0x00000000
2	SW_EXPLICITBF_QOSNULL_HW_CTRL_EN	Set to '1' to enable the hardware controlled delay feedback of beamform qosnull+ndp Reset State: 0x00000000
1	SW_EXPLICITBF_QOSNULL_IMME_EN	Set to '1' to enable the immediate feedback of beamform qosnull+ndp Reset State: 0x00000000
0	SW_EXPLICITBF_QOSNULL_NDP_EN	Set to '1' to enable the explicit beamform qosnull + ndp Reset State: 0x00000000

0x30001B4 TPE_BEAMFORM_QOSNULL_NDP_CNT

Type: read-only
Reset State: 0x00000000

Contains the debug counter for beamform qosnull+ndp

TPE_BEAMFORM_QOSNULL_NDP_CNT

Bits	Name	Description
23:16	EXPLICITBF_QOSNULL_SENT_CNT	explicit beamform feedback sent count Reset State: 0x00000000
15:8	EXPLICITBF_QOSNULL_NDP_CNT	explicit beamform ndp receive count Reset State: 0x00000000
7:0	EXPLICITBF_QOSNULL_REQ_CNT	explicit beamform qosnull request count Reset State: 0x00000000

0x30001B8 TPE_CXM_CTRL

Type: read-write
Reset State: 0x00000000

Contains the control and status of cxm logic

TPE_CXM_CTRL

Bits	Name	Description
4	BTC_ACTIVE_FINAL	btc_active_final status Reset State: 0x00000000
3	LTE_CXM_WLAN_TX_GRANT	lte_cxm_wlan_tx_grant status Reset State: 0x00000000
2	WLAN_TX_GRANT	wlan_tx_grant status Reset State: 0x00000000
1	SW_WLAN_TX_GRANT_SEL	When enabled(bit[0]), 0: btc_active from pta controls tx, 1:lte_cxm_wlan_tx_grant from timer controls tx Reset State: 0x00000000
0	SW_WLAN_TX_GRANT_CTRL_EN	Set 1 to enable the wlan_tx_grant control logic. Clear 0 to always allow transmission Reset State: 0x00000000

0x30001BC TPE_SW_11AC_CTRL

Type: read-write
Reset State: 0x00000200

Contains the control signals 11ac related

TPE_SW_11AC_CTRL

Bits	Name	Description
15:0	SW_MAX_AMPDU_TX_TIME_11AC	The maximum ampdu tx time in 11ac mode Reset State: 0x00000200

0x30001C0 TPE_SW_AID_01

Type: read-write
Reset State: 0x00000000

Contains the AID for staid0, 1

TPE_SW_AID_01

Bits	Name	Description
21:11	SW_AID_01_1	The AID for staid1 Reset State: 0x00000000
10:0	SW_AID_01_0	The AID for staid0 Reset State: 0x00000000

0x30001C4 TPE_SW_AID_23

Type: read-write
Reset State: 0x00000000

Contains the AID for staid2, 3

TPE_SW_AID_23

Bits	Name	Description
21:11	SW_AID_23_3	The AID for staid3 Reset State: 0x00000000
10:0	SW_AID_23_2	The AID for staid2 Reset State: 0x00000000

0x30001C8 TPE_SW_AID_45

Type: read-write
Reset State: 0x00000000

Contains the AID for staid4, 5

TPE_SW_AID_45

Bits	Name	Description
21:11	SW_AID_45_5	The AID for staid5 Reset State: 0x00000000
10:0	SW_AID_45_4	The AID for staid4 Reset State: 0x00000000

0x30001CC TPE_SW_AID_67

Type: read-write
Reset State: 0x00000000

Contains the AID for staid6, 7

TPE_SW_AID_67

Bits	Name	Description
21:11	SW_AID_67_7	The AID for staid7 Reset State: 0x00000000
10:0	SW_AID_67_6	The AID for staid6 Reset State: 0x00000000

0x30001D0 TPE_SW_AID_89

Type: read-write
Reset State: 0x00000000

Contains the AID for staid8, 9

TPE_SW_AID_89

Bits	Name	Description
21:11	SW_AID_89_9	The AID for staid9 Reset State: 0x00000000
10:0	SW_AID_89_8	The AID for staid8 Reset State: 0x00000000

0x30001D4 TPE_SW_AID_AB

Type: read-write
Reset State: 0x00000000

Contains the AID for staid10, 11

TPE_SW_AID_AB

Bits	Name	Description
21:11	SW_AID_AB_11	The AID for staid11 Reset State: 0x00000000
10:0	SW_AID_AB_10	The AID for staid10 Reset State: 0x00000000

0x30001D8 TPE_SW_AID_CD

Type: read-write
Reset State: 0x00000000

Contains the AID for staid12, 13

TPE_SW_AID_CD

Bits	Name	Description
21:11	SW_AID_CD_13	The AID for staid13 Reset State: 0x00000000
10:0	SW_AID_CD_12	The AID for staid12 Reset State: 0x00000000

0x30001DC TPE_SW_AID_EF

Type: read-write
Reset State: 0x00000000

Contains the AID for staid14, 15

TPE_SW_AID_EF

Bits	Name	Description
21:11	SW_AID_EF_15	The AID for staid15 Reset State: 0x00000000
10:0	SW_AID_EF_14	The AID for staid14 Reset State: 0x00000000

0x30001E0 TPE_SW_GID_SEL

Type: read-write
Reset State: 0x00000000

Contains the GID selection for all stations

TPE_SW_GID_SEL

Bits	Name	Description
31:30	SW_GID_SEL_15	The gid selection for sta15 Reset State: 0x00000000
29:28	SW_GID_SEL_14	The gid selection for sta14 Reset State: 0x00000000

TPE_SW_GID_SEL (cont.)

Bits	Name	Description
27:26	SW_GID_SEL_13	The gid selection for sta13 Reset State: 0x00000000
25:24	SW_GID_SEL_12	The gid selection for sta12 Reset State: 0x00000000
23:22	SW_GID_SEL_11	The gid selection for sta11 Reset State: 0x00000000
21:20	SW_GID_SEL_10	The gid selection for sta10 Reset State: 0x00000000
19:18	SW_GID_SEL_9	The gid selection for sta9 Reset State: 0x00000000
17:16	SW_GID_SEL_8	The gid selection for sta8 Reset State: 0x00000000
15:14	SW_GID_SEL_7	The gid selection for sta7 Reset State: 0x00000000
13:12	SW_GID_SEL_6	The gid selection for sta6 Reset State: 0x00000000
11:10	SW_GID_SEL_5	The gid selection for sta5 Reset State: 0x00000000
9:8	SW_GID_SEL_4	The gid selection for sta4 Reset State: 0x00000000
7:6	SW_GID_SEL_3	The gid selection for sta3 Reset State: 0x00000000
5:4	SW_GID_SEL_2	The gid selection for sta2 Reset State: 0x00000000
3:2	SW_GID_SEL_1	The gid selection for sta1 Reset State: 0x00000000
1:0	SW_GID_SEL_0	The gid selection for sta0 Reset State: 0x00000000

0x30001E4 TPE_SW_NONHT_BW_CTRL

Type: read-write
Reset State: 0x00000000

Contains the BW indication configuration

TPE_SW_NONHT_BW_CTRL

Bits	Name	Description
6	SW_NAV_CHECK_FOR_RTS_EN	When set, always check if nav is zero before sending cts. Otherwise it will only be checked for BW signaling. Reset State: 0x00000000
5:0	SW_RTS_BW_RETRY_THRESHOLD	In static mode, when rts retry counters is larger than the threshold, data will be sent out at 20Mhz rate. Reset State: 0x00000000

0x30001E8 TPE_SW_GLOBAL_CF_END_DATA_POWER_TEMPLATE_40MHZ

Type: read-write
Reset State: 0x00000000

TPE_SW_GLOBAL_CF_END_DATA_POWER_TEMPLATE_40MHZ

Bits	Name	Description
30	FEC_MODE	Reset State: 0x00000000
29	LPE_BIT	Reset State: 0x00000000
25	AMPDU_VALID	Reset State: 0x00000000
24:20	TX_POWER	Reset State: 0x00000000
19	RESERVED	Reset State: 0x00000000
18:16	TX_ANTENNA_EN	Reset State: 0x00000000
15:14	STBC_VALID	Reset State: 0x00000000
13	SGI_VALID	Reset State: 0x00000000
12:11	NSS_11B_MODE	Reset State: 0x00000000
8:3	STA_RATE	Reset State: 0x00000000
2:0	STA_MODE	Reset State: 0x00000000

0x30001EC TPE_SW_GLOBAL_CF_END_DATA_POWER_TEMPLATE_80MHZ

Type: read-write
Reset State: 0x00000000

TPE_SW_GLOBAL_CF_END_DATA_POWER_TEMPLATE_80MHZ

Bits	Name	Description
30	FEC_MODE	Reset State: 0x00000000
29	LPE_BIT	Reset State: 0x00000000

TPE_SW_GLOBAL_CF_END_DATA_POWER_TEMPLATE_80MHZ (cont.)

Bits	Name	Description
25	AMPDU_VALID	Reset State: 0x00000000
24:20	TX_POWER	Reset State: 0x00000000
19	RESERVED	Reset State: 0x00000000
18:16	TX_ANTENNA_EN	Reset State: 0x00000000
15:14	STBC_VALID	Reset State: 0x00000000
13	SGI_VALID	Reset State: 0x00000000
12:11	NSS_11B_MODE	Reset State: 0x00000000
8:3	STA_RATE	Reset State: 0x00000000
2:0	STA_MODE	Reset State: 0x00000000

0x30001F0 TPE_SW_WARMUP_DELAY

Type: read-write
Reset State: 0x00000000

This register contains the control signals for warmup

TPE_SW_WARMUP_DELAY

Bits	Name	Description
11	SW_FIX_WARMUP_DELAY_EN	Set this bit to 1 to enable the fix warmup delay Reset State: 0x00000000
10:0	SW_WARMUP_TIME	The wait time to be programmed in txp commands. This is the time between tpe asserts the warmup and the time when txp sends the first phy cmd. Reset State: 0x00000000

0x30001F4 TPE_MAIN_MPROC_REQ_CNT

Type: read-only
Reset State: 0x00000000

This register contains the main_mproc request counter per session

TPE_MAIN_MPROC_REQ_CNT

Bits	Name	Description
27:24	SESSION_IS_BACKOFF_CSI_QOSNULL_CNT	Reset State: 0x00000000

TPE_MAIN_MPROC_REQ_CNT (cont.)

Bits	Name	Description
23:20	SESSION_IS_BACKOFF_CNT	Reset State: 0x00000000
19:16	SESSION_IS_BEACON_CN	Reset State: 0x00000000
15:12	SESSION_IS_SW_TEMPLATE_CNT	Reset State: 0x00000000
11:8	SESSION_IS_SW_STA_QID_CNT	Reset State: 0x00000000
7:4	SESSION_IS_SW_BACK_OFF_INDEX_CNT	Reset State: 0x00000000
3:0	SESSION_IS_RXP_CNT	Reset State: 0x00000000

16.2.48 txp

0x3000000 TXP_TXP_CMDF_DIN

Type: read-write
Reset State: 0x00000000

Command write port of TXP FIFO.

TXP_TXP_CMDF_DIN

Bits	Name	Description
31:0	TXP_CMDF_WDATA	Write-only, 32-bit field for commands from the software to the TXP. Reset State: 0x00000000

0x3000004 TXP_TXP_CMDF_CONTROL

Type: read-write
Reset State: 0x00010024

TXP command FIFO control register.

TXP_TXP_CMDF_CONTROL

Bits	Name	Description
16	TPE_CAHBZ	This bit controls where the TXP commands will come from. 1 for TPE, 0 for CAHB (i.e., from SW). Reset State: 0x00000001

TXP_TXP_CMDF_CONTROL (cont.)

Bits	Name	Description
7:0	FREE_ENTRIES	Read-only field that shows free entries remaining in TXP command FIFO Reset State: 0x00000024

0x3000008 TXP_TXP_TIMEOUT_TIMER

Type: read-write
Reset State: 0x00000000

TXP Timeout Timer - will interrupt cpu if TXP state machines do not return to idle within pre-specified time.

TXP_TXP_TIMEOUT_TIMER

Bits	Name	Description
31	TIMER_EN	Timeout timer enable bit. Reset State: 0x00000000
23:0	TIMEOUT_TIMER_VAL	Timeout timer value - in microseconds. Reset State: 0x00000000

0x300000C TXP_TXP_STATUS

Type: read-only
Reset State: 0x00000000

Shows status of TXP.

TXP_TXP_STATUS

Bits	Name	Description
18:17	GAS_STATUS	Status of GAS in TXP. Reset State: 0x00000000
16	GAM_BUSY	Shows whether GAM in TXP is busy. Reset State: 0x00000000

TXP_TXP_STATUS (cont.)

Bits	Name	Description
15:8	ERROR_CODE	Read-only field that shows TXP error code (0 if no error). Command FIFO - Over flow: 8'b0001_0000; GAM control - AHB error returned from GAM: 8'b0010_0000; Invalid BD header: 8'b0010_0001; tx_size with 0 bytes: 8'b0010_0010; MPDU Header longer than 1st pdu: 8'b0010_0011; Data starts outside 1st pdu: 8'b0010_0100; MPDU header longer than MPDU: 8'b0010_0101; MPDU data_offset < MPDU hdr_off: 8'b0010_0110; PINF - PHY sends abort/BTC Active: 8'b0011_0000; - FIFO underrun: 8'b0011_0001; - New transmission with no PHY clkstart: 8'b0011_0010; - New transmission, but PHY not idle: 8'b0011_0011; - PHY goes idle prematurely: 8'b0011_0100; FCS - Two consecutive FCS Starts received: 8'b0100_0000; - Two consecutive FCS Stops received (last was FCS32): 8'b0100_0001; - FCS8 Start followed by FCS8 Start: 8'b0100_0010; - Two consecutive FCS Stops received (last was FCS8): 8'b0100_0011; - FCS32 Start followed by FCS8 Start: 8'b0100_0100; - FCS32 Start followed by FCS8 Stop: 8'b0100_0101; - FCS8 Start followed by FCS32 Start: 8'b0100_0110; - FCS8 Start followed by FCS32 Stop: 8'b0100_0111; Main FSM - Invalid command type: 8'b0101_0000; - PHY command with 0 bytes: 8'b0101_0001; - tx_sw with 0 bytes: 8'b0101_0010; Reset State: 0x00000000
7:0	LAST_CMD_NR	Read-only field that shows last command number successfully completed by TXP. TXP extracts the last 8 bits of the command and blindly copies it to this register This is the CMD index nr field supplied by software. Reset State: 0x00000000

0x3000010 TXP_TXP_BTC_ACTIVE_ABORT_ENABLE

Type: read-write
Reset State: 0x00000000

Controls if BTC active will cause TXP to be abort. software would then have to soft reset the TXP.

TXP_TXP_BTC_ACTIVE_ABORT_ENABLE

Bits	Name	Description
0	BTC_ACTIVE	Allows BTC active to cause TXP abort. Reset State: 0x00000000

0x3000014 TXP_TXP_TESTBUS

Type: read-write
Reset State: 0x00000008

testbus register.

TXP_TXP_TESTBUS

Bits	Name	Description
31	ENABLE_WAIT_GAM_IDLE_ECO	Set '1' to enable the eco, so the txp_tpe_main_error_hang won't be asserted until gam is idle Reset State: 0x00000000
11:8	MAC_PHY_TESTBUS_SEL	MAC/PHY testbus select. Reset State: 0x00000000
7:4	PHY_TESTBUS_SEL	PHY testbus select. Reset State: 0x00000000
3:0	MAC_TESTBUS_SEL	MAC testbus select. Reset State: 0x00000008

0x3000018 TXP_TXP_WARMUP_CNTL

Type: read-write
Reset State: 0x00000030

TXP warmup control register - added for Virgo

TXP_TXP_WARMUP_CNTL

Bits	Name	Description
5	TPE_TXP_RF_WARMUP_END_P_EN	allow tpe_txp_rf_warmup_end_p to affect txp_mpi_warmup Reset State: 0x00000001
4	TPE_TXP_RF_WARMUP_P_EN	allow tpe_txp_rf_warmup_p to affect txp_mpi_warmup Reset State: 0x00000001

0x3000080 TXP_TXP_DEBUG_CLEAR

Type: write-only
Reset State: 0x00000000

Write-only register; clears all debug registers.

TXP_TXP_DEBUG_CLEAR

Bits	Name	Description
0	CLR_DEBUG_REGS	Write only-bit; write 1 to clear all debug registers. Reset State: 0x00000000

0x3000084 TXP_TXP_NR_FRAMES_XMIT

Type: read-write
Reset State: 0x00000000

Number of frames (PPDU) transmitted

TXP_TXP_NR_FRAMES_XMIT

Bits	Name	Description
15:0	NR_FRAMES_XMIT	Number of frames transmitted; stuck at 0xffff Reset State: 0x00000000

0x3000088 TXP_TXP_PHY_ABORTS

Type: read-write
Reset State: 0x00000000

Number of times that txp_mpi_abort or mpi_txp_abort is asserted (counter is located before the loopback mux). The counters increment once for every low to high transition in the signal.

TXP_TXP_PHY_ABORTS

Bits	Name	Description
31:16	NR_PHY_ABORT_RCVD	Number of times mpi_txp_abort (or fphy_txp_abort) is asserted. Reset State: 0x00000000
15:0	NR_PHY_ABORT_GEN	Number of times txp_mpi_abort (or txp_fphy_abort) is asserted Reset State: 0x00000000

0x300008C TXP_TXP_NR_END_INTERRUPTS

Type: read-write
Reset State: 0x00000000

Number of end interrupts sent by TXP.

TXP_TXP_NR_END_INTERRUPTS

Bits	Name	Description
15:0	TXP_NR_END_INTERRUPTS	Number of end interrupts sent to software. Once it is reached max(0xFFFF), hardware stops updating software needs to reset to restart this counter again Reset State: 0x00000000

0x3000090 TXP_TXP_NR_CMDS

Type: read-write
Reset State: 0x00000000

Number of TXP commands processed.

TXP_TXP_NR_CMDS

Bits	Name	Description
15:0	TXP_NR_CMDS	Number of commands processed Reset State: 0x00000000

16.2.49 dpi

0x30003E0 DPI_LMAP_SYM

Type: read-write
Reset State: 0x00000000

NOT PHYSICALLY IN ASIC, used for RTL simulator debug. Shows only a particular OFDM symbol. val==0xffff shows all symbols. val==0 turns off debug messages. Assumes C++ is compiled with debugging turned on too.

DPI_LMAP_SYM

Bits	Name	Description
15:0	VAL	0x0: OFF 0xFFFF: ALL Reset State: 0x00000000

0x30003E4 DPI_LMAP_TONE_MIN

Type: read-write
Reset State: 0x00000000

NOT PHYSICALLY IN ASIC, used for RTL simulator debug. Shows debug values tone_min <= tone <= tone_max.

DPI_LMAP_TONE_MIN

Bits	Name	Description
15:0	VAL	Reset State: 0x00000000

0x30003E8 DPI_LMAP_TONE_MAX

Type: read-write
Reset State: 0x00000000

NOT PHYSICALLY IN ASIC, used for RTL simulator debug. Shows debug values tone_min <= tone <= tone_max.

DPI_LMAP_TONE_MAX

Bits	Name	Description
15:0	VAL	Reset State: 0x00000000

0x30003EC DPI_LMAP_ROT

Type: read-write
Reset State: 0x00000000

NOT PHYSICALLY IN ASIC, used for RTL simulator debug. Shows only a particular QR rotation.

DPI_LMAP_ROT

Bits	Name	Description
15:0	VAL	Reset State: 0x00000000

0x30003F0 DPI_LMAP_CONSTEL

Type: read-write
Reset State: 0x00000000

NOT PHYSICALLY IN ASIC, used for RTL simulator debug. On some calculations shows only a particular constellation point.

DPI_LMAP_CONSTEL

Bits	Name	Description
15:0	VAL	Reset State: 0x00000000

16.2.50 riva_bt_link_ctrl

0x3000000 BT_INT_0_INTERRUPT_CONTROL

Type: read-write
Reset State: 0x00000000

BT_INT_0_INTERRUPT_CONTROL

Bits	Name	Description
0	INT0EN	0x0: DISABLE 0x1: ENABLE_ALLOWS_UNMASKED_EVENTS_TO_GENERATE_AN_INTERRUPT Reset State: 0xxxxxxxxx

0x3000004 BT_INT_0_BTC_INTERRUPT_MASK

Type: read-write
Reset State: 0x00000000

BT_INT_0_BTC_INTERRUPT_MASK

Bits	Name	Description
9	MASKRXABORT	0x0: MASKED 0x1: UNMASKED Reset State: 0xxxxxxxxx
8	MASKRSSI	0x0: MASKED 0x1: UNMASKED Reset State: 0xxxxxxxxx
7	MASKFS	0x0: MASKED 0x1: UNMASKED Reset State: 0xxxxxxxxx
6	MASKTXABORT	0x0: MASKED 0x1: UNMASKED Reset State: 0xxxxxxxxx
5	MASKTX	0x0: MASKED 0x1: UNMASKED Reset State: 0xxxxxxxxx
4	MASKLC	0x0: MASKED 0x1: UNMASKED Reset State: 0xxxxxxxxx
3	MASKHALF	0x0: MASKED 0x1: UNMASKED Reset State: 0xxxxxxxxx

BT_INT_0_BTC_INTERRUPT_MASK (cont.)

Bits	Name	Description
2	MASKRX	0x0: MASKED 0x1: UNMASKED Reset State: 0xxxxxxxxx
1	MASKSLOT	0x0: MASKED 0x1: UNMASKED Reset State: 0xxxxxxxxx
0	MASKPRE	0x0: MASKED 0x1: UNMASKED Reset State: 0xxxxxxxxx

0x3000008 BT_INT_0_BTC_INTERRUPT_STATUS_AND_ACKNOWLEDGE

Type: read-write
Reset State: 0xxxxxxxxx

BT_INT_0_BTC_INTERRUPT_STATUS_AND_ACKNOWLEDGE

Bits	Name	Description
9	STATRXABORT	0x0: NO_CHANGE 0x1: CLEAR_RAW_STATUS Reset State: 0xxxxxxxxx
8	STATRSSI	0x0: NO_CHANGE 0x1: CLEAR_RAW_STATUS Reset State: 0xxxxxxxxx
7	STATFS	0x0: NO_CHANGE 0x1: CLEAR_RAW_STATUS Reset State: 0xxxxxxxxx
6	STATTXABORT	0x0: NO_CHANGE 0x1: CLEAR_RAW_STATUS Reset State: 0xxxxxxxxx
5	STATTX	0x0: NO_CHANGE 0x1: CLEAR_RAW_STATUS Reset State: 0xxxxxxxxx
4	STATLC	0x0: NO_CHANGE 0x1: CLEAR_RAW_STATUS Reset State: 0xxxxxxxxx
3	STATHALF	0x0: NO_CHANGE 0x1: CLEAR_RAW_STATUS Reset State: 0xxxxxxxxx

BT_INT_0_BTC_INTERRUPT_STATUS_AND_ACKNOWLEDGE (cont.)

Bits	Name	Description
2	STATRX	0x0: NO_CHANGE 0x1: CLEAR_RAW_STATUS Reset State: 0xxxxxxxxx
1	STATSLOT	0x0: NO_CHANGE 0x1: CLEAR_RAW_STATUS Reset State: 0xxxxxxxxx
0	STATPRE	0x0: NO_CHANGE 0x1: CLEAR_RAW_STATUS Reset State: 0xxxxxxxxx

0x300000C BT_INT_0_BTC_PRESLOT_FILTER

Type: read-write
Reset State: 0x00000000

BT_INT_0_BTC_PRESLOT_FILTER

Bits	Name	Description
7:0	PRESLOTFLTR	Reset State: 0xxxxxxxxx

0x3000010 BT_INT_0_BTC_SLOT_BURST_TIMER

Type: read-write
Reset State: 0x00000000

BT_INT_0_BTC_SLOT_BURST_TIMER

Bits	Name	Description
13:0	SLOTTIMER	Sub-Section 2.3.5: Bluetooth clock registers Reset State: 0xxxxxxxxx

0x3000014 BT_BLUETOOTH_CLOCK_N_COMPARATOR_INTERRUPT_CONTROL_STATUS

Type: read-write
Reset State: 0x00000000

BT_BLUETOOTH_CLOCK_N_COMPARATOR_INTERRUPT_CONTROL_STATUS

Bits	Name	Description
5	CLKCMPINT2	0x0: NO_INTERRUPT 0x1: INTERRUPT_IS_PENDING Reset State: 0xxxxxxxxx
4	CLKCMPEN2	0x0: DISABLES_INTERRUPT_AND_CLEARS_INTERRUPT_STATUS_CLKCMPINT_0 0x1: ENABLES_INTERRUPT Reset State: 0xxxxxxxxx
3	CLKCMPINT1	0x0: NO_INTERRUPT 0x1: INTERRUPT_IS_PENDING Reset State: 0xxxxxxxxx
2	CLKCMPEN1	0x0: DISABLES_INTERRUPT_AND_CLEARS_INTERRUPT_STATUS_CLKCMPINT_0 0x1: ENABLES_INTERRUPT Reset State: 0xxxxxxxxx
1	CLKCMPINT0	0x0: NO_INTERRUPT 0x1: INTERRUPT_IS_PENDING Reset State: 0xxxxxxxxx
0	CLKCMPEN0	0x0: DISABLES_INTERRUPT_AND_CLEARS_INTERRUPT_STATUS_CLKCMPINT_0 0x1: ENABLES_INTERRUPT Reset State: 0xxxxxxxxx

0x3000018 BT_CAPTURED_BT_CLKN_INTEGER_PORTION

Type: read-only
Reset State: 0x00000000

BT_CAPTURED_BT_CLKN_INTEGER_PORTION

Bits	Name	Description
27:0	BTCLKN_40_13	Reset State: 0xxxxxxxxx

0x300001C BT_CAPTURED_BT_CLKN_FRACTIONAL_PORTION

Type: read-only
Reset State: 0x00000000

BT_CAPTURED_BT_CLKN_FRACTIONAL_PORTION

Bits	Name	Description
12:0	BTCLKN_12_0	Reset State: 0xxxxxxxxx

0x3000020 BT_CAPTURED_BT_CLKA_INTEGER_PORTION

Type: read-only
Reset State: 0x00000000

BT_CAPTURED_BT_CLKA_INTEGER_PORTION

Bits	Name	Description
27:0	BTCLKA_40_13	Reset State: 0xxxxxxxxx

0x3000024 BT_CAPTURED_BT_CLKA_FRACTIONAL_PORTION

Type: read-only
Reset State: 0x00000000

BT_CAPTURED_BT_CLKA_FRACTIONAL_PORTION

Bits	Name	Description
12:0	BTCLKA_12_0	Reset State: 0xxxxxxxxx

0x3000028 BT_BT_CLOCK_CONTROL

Type: read-write
Reset State: 0x00000000

BT_BT_CLOCK_CONTROL

Bits	Name	Description
2	CLKNLDSEL	0x0: USE_QCT_EDGE_DETECT_COMPONENT 0x1: USE_EDGE_DETECTOR_FROM_REGISTER_DELAYS Reset State: 0xxxxxxxxx
1	CLKNLDEN	0x0: DISABLED 0x1: LOAD_BT_CLKN_VALUE_INTO_LTE_FRAME_SYNC_CAPTURED_CLKN_REGISTERS_16_17_ON_RISING_EDGE_OF_COEX_FRAME_SYNC Reset State: 0xxxxxxxxx

BT_BT_CLOCK_CONTROL (cont.)

Bits	Name	Description
0	LDFHS	0x0: NO_CHANGE 0x1: LOAD_FHS_CLK_27_2_INTO_BT_CLKA27_2_FRACTIONAL_BITS_STALL_DURING_THE_LOAD Reset State: 0xxxxxxxxx

0x300002C BT_BT_CLOCK_ALU_COMMAND

Type: read-write
Reset State: 0x00000000

BT_BT_CLOCK_ALU_COMMAND

Bits	Name	Description
18:16	OP_0	0x0: ZEROES 0x1: BT_CLK_OPERAND_REGISTER 0x2: BT_CLKN 0x3: BT_CLKA 0x4: BT_CLK_ACCUMULATOR_REGISTER 0x5: BT_CLK_CAP_AND_ZEROES Reset State: 0xxxxxxxxx
14:12	OP_1	0x0: ZEROES 0x1: BT_CLK_OPERAND_REGISTER 0x2: BT_CLKN 0x3: BT_CLKA 0x4: BT_CLK_ACCUMULATOR_REGISTER 0x5: BT_CLK_CAP_AND_ZEROES Reset State: 0xxxxxxxxx
8	OP	0x0: ADD_OP_0_OP_1 0x1: SUBTRACT_OP_0_OP_1 Reset State: 0xxxxxxxxx
6	LR	0x0: DO_NOT_CAPTURE_ALU_RESULT_IN_ACCUMULATOR_REGISTER 0x1: UPDATE_THE_INTEGER_INTGRACC_AND_FRACTIONAL_FRACACC_ACCUMULATOR_REGISTERS_WITH_THE_ALU_RESULT_FOR_READ_BACK_OR_ACCUMULATION_OR_BOTH Reset State: 0xxxxxxxxx

BT_BT_CLOCK_ALU_COMMAND (cont.)

Bits	Name	Description
5	LN	0x0: DO_NOT_CAPTURE_ALU_RESULT_IN_BT_CLKN 0x1: UPDATE_THE_ENTIRE_OR_PARTIAL_INTEGER_AND_FRACTIONAL_BT_CLKN_COUNTERS_WITH_THE_ALU_RESULT_ACCORDING_TO_THE_UPDATE_FIELDS_FRACTIONAL_BITS_STALL_DURING_THE_LOAD Reset State: 0xxxxxxxxx
4	LA	0x0: DO_NOT_CAPTURE_ALU_RESULT_IN_BT_CLKA 0x1: UPDATE_THE_ENTIRE_OR_PARTIAL_INTEGER_AND_FRACTIONAL_BT_CLKA_COUNTERS_WITH_THE_ALU_RESULT_ACCORDING_TO_UPDATE_FIELDS_FRACTIONAL_BITS_STALL_DURING_LOAD Reset State: 0xxxxxxxxx
3	UU	0x0: DO_NOT_UPDATE_BIT_27_2 0x1: UPDATE_BIT_27_2 Reset State: 0xxxxxxxxx
2	U1	0x0: DO_NOT_UPDATE_BIT_1 0x1: UPDATE_BIT_1 Reset State: 0xxxxxxxxx
1	U0	0x0: DO_NOT_UPDATE_BIT_0 0x1: UPDATE_BIT_0 Reset State: 0xxxxxxxxx
0	UF	0x0: DO_NOT_UPDATE_FRACTIONAL_BITS 0x1: UPDATE_FRACTIONAL_BITS Reset State: 0xxxxxxxxx

0x3000030 BT_BT_CLOCK_ALU_INTEGER_OPERAND

Type: read-write
Reset State: 0x00000000

BT_BT_CLOCK_ALU_INTEGER_OPERAND

Bits	Name	Description
27:0	INTGROPRND	Reset State: 0xxxxxxxxx

0x3000034 BT_BT_CLOCK_ALU_FRACTIONAL_OPERAND

Type: read-write
Reset State: 0x00000000

BT_BT_CLOCK_ALU_FRACTIONAL_OPERAND

Bits	Name	Description
12:0	FRACOPRND	Reset State: 0xxxxxxxxx

0x3000038 BT_BT_CLOCK_ALU_INTEGER_ACCUMULATOR

Type: read-write
Reset State: 0x00000000

BT_BT_CLOCK_ALU_INTEGER_ACCUMULATOR

Bits	Name	Description
27:0	INTGRACC	Reset State: 0xxxxxxxxx

0x300003C BT_BT_CLOCK_ALU_FRACTIONAL_ACCUMULATOR

Type: read-write
Reset State: 0x00000000

BT_BT_CLOCK_ALU_FRACTIONAL_ACCUMULATOR

Bits	Name	Description
12:0	FRACACC	Reset State: 0xxxxxxxxx

0x3000040 BT_LTE_FRAME_SYNC_CAPTURED_BT_CLKN_INTEGER_PORTION

Type: read-only
Reset State: 0x00000000

BT_LTE_FRAME_SYNC_CAPTURED_BT_CLKN_INTEGER_PORTION

Bits	Name	Description
27:0	BTCLKN_40_13	Reset State: 0xxxxxxxxx

0x3000044 BT_LTE_FRAME_SYNC_CAPTURED_BT_CLKN_FRACTIONAL_PORTION

Type: read-only
Reset State: 0x00000000

BT_LTE_FRAME_SYNC_CAPTURED_BT_CLKN_FRACTIONAL_PORTION

Bits	Name	Description
12:0	BTCLKN_12_0	Sub-Section 2.3.6: Encryption registers Reset State: 0xxxxxxxxx

0x3000048 BT_ENCRYPTION_CONTROL

Type: read-write
Reset State: 0x00000000

BT_ENCRYPTION_CONTROL

Bits	Name	Description
3	MIC_EN	0x0: DISABLE_MIC 0x1: ENABLE_MIC Reset State: 0xxxxxxxxx
2	CRYPTO_EN	0x0: DISABLE_CRYPTO 0x1: ENABLE_CRYPTO_FOR_ENCRYPTION_DECRYPTION Reset State: 0xxxxxxxxx
1	BRENCREN	0x0: DISABLE_BROADCAST_ENCRYPTION 0x1: ENABLE_BROADCAST_ENCRYPTION_EXCEPT_FOR_FHS_PACKETS Reset State: 0xxxxxxxxx
0	ENCREN	0x0: DISABLE_NON_BROADCAST_ENCRYPTION 0x1: ENABLE_NON_BROADCAST_ENCRYPTION_EXCEPT_FOR_FHS_PACKETS Reset State: 0xxxxxxxxx

0x300004C BT_ENCRYPTION_K_C_KEY_0_ULP_SESSION_KEY_0

Type: read-write
Reset State: 0x00000000

BT_ENCRYPTION_K_C_KEY_0_ULP_SESSION_KEY_0

Bits	Name	Description
31:0	ENCRKEY_31_0	Reset State: 0xxxxxxxxx

0x3000050 BT_ENCRYPTION_K_C_KEY_1_ULP_SESSION_KEY_1

Type: read-write
Reset State: 0x00000000

BT_ENCRYPTION_K_C_KEY_1_ULP_SESSION_KEY_1

Bits	Name	Description
31:0	ENCRKEY_63_32	Reset State: 0xxxxxxxxx

0x3000054 BT_ENCRYPTION_K_C_KEY_2_ULP_SESSION_KEY_2

Type: read-write
Reset State: 0x00000000

BT_ENCRYPTION_K_C_KEY_2_ULP_SESSION_KEY_2

Bits	Name	Description
31:0	ENCRKEY_95_64	Reset State: 0xxxxxxxxx

0x3000058 BT_ENCRYPTION_K_C_KEY_3_ULP_SESSION_KEY_3

Type: read-write
Reset State: 0x00000000

BT_ENCRYPTION_K_C_KEY_3_ULP_SESSION_KEY_3

Bits	Name	Description
31:0	ENCRKEY_127_96	Sub-Section 2.3.7: Device address registers Reset State: 0xxxxxxxxx

0x300005C BT_CAPTURED_UAP

Type: read-only
Reset State: 0x00000000

BT_CAPTURED_UAP

Bits	Name	Description
7:0	UAPCAP	Reset State: 0xxxxxxxxx

0x3000060 BT_BT_DEVICE_ADDRESS_0

Type: read-write
Reset State: 0x00000000

BT_BT_DEVICE_ADDRESS_0

Bits	Name	Description
31:0	BDADDR_31_0	Reset State: 0xxxxxxxxx

0x3000064 BT_BT_DEVICE_ADDRESS_1

Type: read-write
Reset State: 0x00000000

BT_BT_DEVICE_ADDRESS_1

Bits	Name	Description
15:0	BDADDR_47_32	Sub-Section 2.3.8: Hop kernel registers Reset State: 0xxxxxxxxx

0x3000068 BT_HOP_CONTROL

Type: read-write
Reset State: 0x00000000

BT_HOP_CONTROL

Bits	Name	Description
7	AFHEN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
6	OFFSETONLY	0x0: ADD_HOPOFFSET_AND_THE_CALCULATED_CHANNEL_TO_GENERATE_HOPFREQ_NORMAL 0x1: USE_HOPOFFSET_DIRECTLY_TO_GENERATE_HOPFREQ_TESTING_ULP_FUNCTIONAL Reset State: 0xxxxxxxxx
4	FRZCLK	0x0: UPDATE_ENTIRE_CAPTURED_BLUETOOTH_CLOCK_WITH_THE_SELECTED_BLUETOOTH_CLOCK_1 0x1: FREEZE_BITS_16_12_4_2_0_OF_THE_CAPTURED_BLUETOOTH_CLOCK_UPDATE_REST_OF_THE_CAPTURED_BLUETOOTH_CLOCK_WITH_THE_SELECTED_BLUETOOTH_CLOCK_1 Reset State: 0xxxxxxxxx

BT_HOP_CONTROL (cont.)

Bits	Name	Description
3	PGTRAIN	0x0: USE_A_TRAIN_KOFFSET_24 0x1: USE_B_TRAIN_KOFFSET_8 Reset State: 0xxxxxxxxx
2:0	HOPTYPE	0x0: PAGE_SCAN_INQUIRY_SCAN_X00 0x1: PAGE_INQUIRY_X01 Reset State: 0xxxxxxxxx

0x300006C BT_HOP_N_COUNT

Type: read-write
Reset State: 0x00000000

BT_HOP_N_COUNT

Bits	Name	Description
4:0	HOPNCNT	Reset State: 0xxxxxxxxx

0x3000070 BT_HOP_OFFSET

Type: read-write
Reset State: 0x00000000

BT_HOP_OFFSET

Bits	Name	Description
6:0	HOPOFFSET	Reset State: 0xxxxxxxxx

0x3000074 BT_HOP_COEXISTENCE_LOW_CHANNEL

Type: read-write
Reset State: 0x00000000

BT_HOP_COEXISTENCE_LOW_CHANNEL

Bits	Name	Description
6:0	LOWCHAN	Reset State: 0xxxxxxxxx

0x3000078 BT_HOP_COEXISTENCE_HIGH_CHANNEL

Type: read-write
Reset State: 0x00000000

BT_HOP_COEXISTENCE_HIGH_CHANNEL

Bits	Name	Description
6:0	HIGHCHAN	Reset State: 0xxxxxxxxx

0x300007C BT_HOP_AFH_CHANNEL_MAP_0

Type: read-write
Reset State: 0x00000000

BT_HOP_AFH_CHANNEL_MAP_0

Bits	Name	Description
31:0	AFHMAP_31_0	Reset State: 0xxxxxxxxx

0x3000080 BT_HOP_AFH_CHANNEL_MAP_1

Type: read-write
Reset State: 0x00000000

BT_HOP_AFH_CHANNEL_MAP_1

Bits	Name	Description
31:0	AFHMAP_63_32	Reset State: 0xxxxxxxxx

0x3000084 BT_HOP_AFH_CHANNEL_MAP_2

Type: read-write
Reset State: 0x00000000

BT_HOP_AFH_CHANNEL_MAP_2

Bits	Name	Description
14:0	AFHMAP_78_64	0x0: INDICATES_A_BAD_CHANNEL_TO_BE_AVOIDED 0x1: INDICATES_A_VALID_CHANNEL Reset State: 0xxxxxxxxx

0x3000088 BT_HOP_HALF_SLOT_0_BCA_CHANNEL

Type: read-write
Reset State: 0x00000000

BT_HOP_HALF_SLOT_0_BCA_CHANNEL

Bits	Name	Description
6:0	BCA0CHAN	Reset State: 0xxxxxxxxx

0x300008C BT_HOP_HALF_SLOT_1_BCA_CHANNEL

Type: read-write
Reset State: 0x00000000

BT_HOP_HALF_SLOT_1_BCA_CHANNEL

Bits	Name	Description
6:0	BCA1CHAN	Reset State: 0xxxxxxxxx

0x3000090 BT_HOP_FREQUENCY

Type: read-only
Reset State: 0x00000000

BT_HOP_FREQUENCY

Bits	Name	Description
6:0	HOPFREQ	Reset State: 0xxxxxxxxx

0x3000094 BT_ULP_CHANNEL_INDEX

Type: read-write
Reset State: 0x00000000

BT_ULP_CHANNEL_INDEX

Bits	Name	Description
5:0	ULPCHANNELINDEX	Sub-Section 2.3.9: Link controller commands Reset State: 0xxxxxxxxx

0x30000A0 BT_LC_COMMAND_HALF_SLOT_0

Type: read-write
Reset State: 0x00000000

BT_LC_COMMAND_HALF_SLOT_0

Bits	Name	Description
7	MODMODE	0x0: BR_EDR 0x1: ULP Reset State: 0xxxxxxxxx
6	CAPT0	0x0: DISABLE_CAPTURING 0x1: ENABLE_CAPTURING Reset State: 0xxxxxxxxx
5:4	CALC0	0x0: LINK_CONTROLLER_AUTOMATICALLY_RUNS_THE_HOP_CALCULATOR 0x1: FORCE_THE_HOP_CALCULATOR_TO_RUN_REGARDLESS_OF_CMD0 0x2: FORCE_DISABLING_OF_THE_HOP_CALCULATOR_REGARDLESS_OF_CMD0 Reset State: 0xxxxxxxxx
3:0	CMD0	0x0: IDLE_DO_NOT_TX_OR_RX 0x1: TX 0x2: RX_DATA 0x3: RX_DATA_X_SCRAMBLER_INITIALIZED_WITH_HOP_CALCULATOR_X_INPUT 0x4: RX_ID 0x6: RX_SCAN_DATA 0x7: RX_SCAN_DATA_X_SCRAMBLER_INITIALIZED_WITH_HOP_CALCULATOR_X_INPUT 0x8: RX_SCAN_ID 0x9: RX_BCA_BAD_CHANNEL_ASSESSMENT_POWER_BURST_MEASUREMENT 0xA: CONTINUOUS_TX_TEST_MODE_CONFIGURED_BY_TRANSMIT_BUFFER 0xB: CONTINUOUS_RX_TEST_MOD_1_1_MBPS_DATA 0xC: CONTINUOUS_RX_TEST_MOD_2_2_MBPS_DATA 0xD: CONTINUOUS_RX_TEST_MOD_3_3_MBPS_DATA 0xE: TX_X_SCRAMBLER_INITIALIZED_WITH_HOP_CALCULATOR_X_INPUT Reset State: 0xxxxxxxxx

0x30000A4 BT_LC_COMMAND_HALF_SLOT_1

Type: read-write
Reset State: 0x00000000

BT_LC_COMMAND_HALF_SLOT_1

Bits	Name	Description
7	MODMODE	0x0: BR_EDR 0x1: ULP Reset State: 0xxxxxxxxx
6	CAPT1	0x0: DISABLE_CAPTURING 0x1: ENABLE_CAPTURING_DEFAULT Reset State: 0xxxxxxxxx
5:4	CALC1	0x0: THE_LINK_CONTROLLER_AUTOMATICALLY_RUNS_THE_HOP_CALCULATOR 0x1: FORCE_THE_HOP_CALCULATOR_TO_RUN_REGARDLESS_OF_CMD1 0x2: FORCE_DISABLING_OF_THE_HOP_CALCULATOR_REGARDLESS_OF_CMD1 Reset State: 0xxxxxxxxx
3:0	CMD1	0x0: IDLE_DO_NOT_TX_OR_RX 0x1: TX 0x2: RX_DATA 0x3: RX_DATA_X_SCRAMBLER_INITIALIZED_WITH_HOP_KERNEL_X_INPUT 0x4: RX_ID 0x6: RX_SCAN_DATA 0x7: RX_SCAN_DATA_X_SCRAMBLER_INITIALIZED_WITH_HOP_KERNEL_X_INPUT 0x8: RX_SCAN_ID 0x9: RX_BCA_BAD_CHANNEL_ASSESSMENT_POWER_BURST_MEASUREMENT 0xA: CONTINUOUS_TX_TEST_MODE_CONFIGURED_BY_TRANSMIT_BUFFER 0xB: CONTINUOUS_RX_TEST_MOD_1_1_MBPS_DATA 0xC: CONTINUOUS_RX_TEST_MOD_2_2_MBPS_DATA 0xD: CONTINUOUS_RX_TEST_MOD_3_3_MBPS_DATA 0xE: TX_X_SCRAMBLER_INITIALIZED_WITH_HOP_CALCULATOR_X_INPUT Reset State: 0xxxxxxxxx

0x30000A8 BT_LC_ABORT_ISSUE_AND_STATUS

Type: read-write
Reset State: 0xxxxxxxxx

BT_LC_ABORT_ISSUE_AND_STATUS

Bits	Name	Description
6	COEXLATE	0x0: COEXISTENCE_COMMAND_WAS_ISSUED_ON_TIME 0x1: COEXISTENCE_COMMAND_WAS_ISSUED_LATE Reset State: 0xxxxxxxxx
5	LC1LATE	0x0: LC_COMMAND_HALFSLOT_1_WAS_ISSUED_ON_TIME 0x1: LC_COMMAND_HALFSLOT_1_WAS_ISSUED_LATE Reset State: 0xxxxxxxxx
4	LC0LATE	0x0: LC_COMMAND_HALFSLOT_0_WAS_ISSUED_ON_TIME 0x1: LC_COMMAND_HALFSLOT_0_WAS_ISSUED_LATE Reset State: 0xxxxxxxxx
3	HOPDONE	0x0: HOP_CALCULATOR_STATE_MACHINE_IS_CALCULATING_A_FREQUENCY_NOT_DONE 0x1: HOP_CALCULATOR_STATE_MACHINE_IS_NOT_CALCULATING_A_FREQUENCY_DONE Reset State: 0xxxxxxxxx
2	COEXDONE	0x0: COEXISTENCE_STATE_MACHINE_IS_PROCESSING_A_COMMAND_NOT_DONE 0x1: COEXISTENCE_STATE_MACHINE_IS_NOT_PROCESSING_A_COMMAND_DONE Reset State: 0xxxxxxxxx
1	LCDONE	0x0: LINK_CONTROLLER_STATE_MACHINE_IS_PROCESSING_A_COMMAND_NOT_DONE 0x1: LINK_CONTROLLER_STATE_MACHINE_IS_NOT_PROCESSING_A_COMMAND_DONE Reset State: 0xxxxxxxxx
0	LCABORT	Sub-Section 2.3.10: Receive setup registers 0x0: NO_CHANGE 0x1: ISSUE_AN_ABORT_TO_THE_LINK_CONTROLER Reset State: 0xxxxxxxxx

0x30000B0 BT_RX_CONTROL

Type: read-write
Reset State: 0x00000000

BT_RX_CONTROL

Bits	Name	Description
6	CDWINEN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
5	HECALL	0x0: CHECK_THE_HEC_ON_THE_FLY_AS_THE_BITS_ARE_RECEIVED_AND_ABORT_THE_RECEIVE_IMMEDIATELY_IF_A_HEC_MISMATCH_IS_DETECTED 0x1: RECEIVE_ALL_THE_HEC_BITS_BEFORE_CHECKING_FOR_A_POSSIBLE_HEC_MISMATCH Reset State: 0xxxxxxxxx
4	HEC1SLOT	0x0: IMMEDIATELY_ABORT_RECEIVING_A_1_SLOT_PACKET_DUE_TO_AN_AM_ADDRESS_MISMATCH 0x1: ALWAYS_CHECK_THE_HEC_BEFORE_ABORTING_THE_RECEIVE_OF_A_1_SLOT_PACKET_DUE_TO_AN_AM_ADDRESS_MISMATCH Reset State: 0xxxxxxxxx
3	RXAMADIS	0x0: ENABLE_THE_AM_ADDRESS_FILTER_ONLY_PACKETS_WITH_A_VALID_AM_ADDRESS_IN_THE_BASE_AM_ADDRESS_ARRAY_TO_BE_RECEIVED_RECEIVE_OF_PACKETS_WITH_AN_INVALID_AM_ADDRESS_ARE_ABORTED_AND_THE_AMADDRBAD_STATUS_IS_SET 0x1: DISABLE_THE_AM_ADDRESS_FILTER_PACKETS_WITH_ANY_AM_ADDRESS_ARE_RECEIVED_AND_THE_AMADDRBAD_STATUS_IS_NEVER_SET Reset State: 0xxxxxxxxx
2	WININTEN	0x0: PREVENTS_A_RECEIVE_WINDOW_TIME_OUT_FROM_ASSERT_RX_INTERRUPT 0x1: ENABLES_A_RECEIVE_WINDOW_TIME_OUT_TO_ASSERT_RX_INTERRUPT Reset State: 0xxxxxxxxx
1	HDRALIGNEN	0x0: DISABLE_NON_ID_PACKET_SLOT_ALIGNMENT 0x1: ENABLE_NON_ID_PACKET_SLOT_ALIGNMENT_ON_A_VALID_PACKET_HEADER_FIRST_CAPTURE_THE_FRAMEERR_BEFORE_SLOT_ALIGNMENT Reset State: 0xxxxxxxxx

BT_RX_CONTROL (cont.)

Bits	Name	Description
0	ACDALIGNEN	0x0: DISABLE_ID_PACKET_SLOT_ALIGNMENT 0x1: ENABLE_ID_PACKET_SLOT_ALIGNMENT_ON_A_VALID_ACCESS_CODE_DETECT Reset State: 0xxxxxxxxx

0x30000B4 BT_RX_NORMAL_APERTURE_WINDOW

Type: read-write
Reset State: 0x00000000

BT_RX_NORMAL_APERTURE_WINDOW

Bits	Name	Description
5:0	ACDWIN	Reset State: 0xxxxxxxxx

0x30000B8 BT_RX_WIDE_APERTURE_WINDOW

Type: read-write
Reset State: 0x00000000

BT_RX_WIDE_APERTURE_WINDOW

Bits	Name	Description
21:0	SCANWIN	Reset State: 0xxxxxxxxx

0x30000BC BT_RX_BCA_WINDOW

Type: read-write
Reset State: 0x00000000

BT_RX_BCA_WINDOW

Bits	Name	Description
8:0	BCAWIN	Reset State: 0xxxxxxxxx

0x30000C4 BT_RX_ACL_HEADER_THRESHOLD

Type: read-write
Reset State: 0x00000000

BT_RX_ACL_HEADER_THRESHOLD

Bits	Name	Description
4:0	ACLTHRESH	Reset State: 0xxxxxxxxx

0x30000C8 BT_RX_SCO_HEADER_THRESHOLD

Type: read-write
Reset State: 0x00000000

BT_RX_SCO_HEADER_THRESHOLD

Bits	Name	Description
4:0	SCOTHRESH	Reset State: 0xxxxxxxxx

0x30000D0 BT_RX_SYNC_WORD_0

Type: read-write
Reset State: 0x00000000

BT_RX_SYNC_WORD_0

Bits	Name	Description
31:0	RX_SYNC_WORD_0	Reset State: 0xxxxxxxxx

0x30000D4 BT_RX_SYNC_WORD_1

Type: read-write
Reset State: 0x00000000

BT_RX_SYNC_WORD_1

Bits	Name	Description
31:0	RX_SYNC_WORD_1	Reset State: 0xxxxxxxxx

0x30000D8 BT_RX_SCO_PAYLOAD_LENGTH

Type: read-write
Reset State: 0x00000000

BT_RX_SCO_PAYLOAD_LENGTH

Bits	Name	Description
9:0	RXSCOLNGTH	Reset State: 0xxxxxxxxx

0x30000DC BT_RX_AM_ADDRESS_ARRAY_POINTER

Type: read-write
Reset State: 0x00000000

BT_RX_AM_ADDRESS_ARRAY_POINTER

Bits	Name	Description
15:2	RXAMAPTR	Reset State: 0xxxxxxxxx

0x30000E0 BT_RX_BUFFER_SCO_POINTER

Type: read-write
Reset State: 0x00000000

BT_RX_BUFFER_SCO_POINTER

Bits	Name	Description
15:2	RXSCOPTR	Reset State: 0xxxxxxxxx

0x30000E4 BT_RX_BUFFER_ACL_POINTER

Type: read-write
Reset State: 0x00000000

BT_RX_BUFFER_ACL_POINTER

Bits	Name	Description
15:2	RXACLPTR	Reset State: 0xxxxxxxxx

0x30000E8 BT_RX_BUFFER_LMP_POINTER

Type: read-write
Reset State: 0x00000000

BT_RX_BUFFER_LMP_POINTER

Bits	Name	Description
15:2	RXLMPPTR	Reset State: 0xxxxxxxxx

0x30000EC BT_RX_BUFFER_CONTROL_POINTER

Type: read-write
Reset State: 0x00000000

BT_RX_BUFFER_CONTROL_POINTER

Bits	Name	Description
15:2	RXCNTRLPTR	Reset State: 0xxxxxxxxx

0x30000F0 BT_RX_BUFFER_ULP_POINTER

Type: read-write
Reset State: 0x00000000

BT_RX_BUFFER_ULP_POINTER

Bits	Name	Description
15:2	RXULPLPTR	Reset State: 0xxxxxxxxx

0x30000F4 BT_RX_LOW_POWER_CONTROL

Type: read-write
Reset State: 0x00000000

BT_RX_LOW_POWER_CONTROL

Bits	Name	Description
4	LPPSBISTDONE	0x0: BIST_NOT_DONE 0x1: BIST_COMPLETE Reset State: 0xxxxxxxxx
3	LPPSBISTSTART	0x0: NO_ACTION 0x1: START_LPPS_BIST Reset State: 0xxxxxxxxx
2	LPPSBISTEN	0x0: DISABLE_LPPS_BIST 0x1: ENABLE_LPPS_BIST Reset State: 0xxxxxxxxx

BT_RX_LOW_POWER_CONTROL (cont.)

Bits	Name	Description
1	EDABORTEN	0x0: LEAVE_RECEIVER_ON_DURING_DURATION_OF_THE_SCAN_WINDOW_HARDWARE_SHUTS_RECEIVER_OFF_ONLY_AT_THE_WINDOW_TIME_OUT_INTERRUPT_SOFTWARE_STILL_HAS_OPTION_TO_WRITE_AN_LC_ABORT_DURING_THIS_PERIOD 0x1: IMMEDIATELY_TURN_THE_RECEIVER_OFF_AFTER_THE_FIRST_ENERGY_DETECT_INTERRUPT_IS_RECEIVED Reset State: 0xxxxxxxxx
0	LOWPWREN	0x0: DISABLE_LOW_POWER_MODE 0x1: ENABLE_LOW_POWER_MODE Reset State: 0xxxxxxxxx

0x30000F8 BT_RX_LPPS_BIST_TIMER_INIT_VALUE

Type: read-write
Reset State: 0x00000000

BT_RX_LPPS_BIST_TIMER_INIT_VALUE

Bits	Name	Description
15:0	LPPSBISTTIMER	Sub-Section 2.3.11: Receive status registers Reset State: 0xxxxxxxxx

0x3000100 BT_RX_COMPOSITE_STATUS

Type: read-write
Reset State: 0x00000000

BT_RX_COMPOSITE_STATUS

Bits	Name	Description
8	RXABORT	0x0: COEXISTENCE_RX_ABORT_HAS_NOT_BEEN_ENCOUNTERED 0x1: THE_RECEIVE_OPERATION_HAS_BEEN_ABORTED_BY_COEXISTENCE Reset State: 0xxxxxxxxx

BT_RX_COMPOSITE_STATUS (cont.)

Bits	Name	Description
7	STATVALID	0x0: THE_RECEIVE_STATUS_REGISTERS_HAS_NOT_BEEN_UPDATED_BY_HARDWARE 0x1: THE_RECEIVE_STATUS_REGISTERS_HAS_BEEN_UPDATED_WITH_THE_LATEST_STATUS Reset State: 0xxxxxxxxx
6	RXBUFERR	0x0: NULL_POINTER_HAS_NOT_BEEN_ENCOUNTERED 0x1: THE_RECEIVE_OPERATION_WAS_ABORTED_DUE_TO_A_NULL_POINTER_THAT_WAS_READ_FROM_ONE_OF_THE_RECEIVE_LINK_LISTS Reset State: 0xxxxxxxxx
5	AMADDRBAD	0x0: INVALID_AM_ADDRESS_HAS_NOT_BEEN_ENCOUNTERED 0x1: RECEIVE_OPERATION_HAS_BEEN_ABORTED_FOR_AN_INVALID_AM_ADDRESS_PKTHDR_CONTAINS_NEW_AM_ADDRESS_AND_PACKET_INDEX_FIELDS Reset State: 0xxxxxxxxx
4	ACDVALID	0x0: A_VALID_ACCESS_CODE_HAS_NOT_BEEN_DETECTED 0x1: A_VALID_ACCESS_CODE_HAS_BEEN_DETECTED_WHILE_THE_RECEIVE_WINDOW_WAS_OPEN_AND_ENERGY_WAS_DETECTED_CONTROLLED_BY_ACDCARRIER 0x0: NO_ENERGY_DETECTED 0x1: PACKET_DETECTOR_HAS_DETECTED_ENERGY Reset State: 0xxxxxxxxx
3	RXHALFSLOT	0x0: RECEIVE_STATUS_IS_GENERATED_BY_CMD0_FIRST_HALFSLOT 0x1: RECEIVE_STATUS_IS_GENERATED_BY_CMD1_SECOND_HALFSLOT Reset State: 0xxxxxxxxx
2	PYLDBAD	Reset State: 0xxxxxxxxx
1	PKTHDRBAD	Reset State: 0xxxxxxxxx
0	WINTO	0x0: RECEIVE_WINDOW_HAS_NOT_TIMED_OUT 0x1: RECEIVE_OPERATION_ENDED_DUE_TO_A_RECEIVE_WINDOW_TIME_OUT_VALID_ACCESS_CODE_WAS_NOT_DETECTED_OR_THE_BCA_WINDOW_TIMED_OUT Reset State: 0xxxxxxxxx

0x3000104 BT_RX_DETAILED_BAD_STATUS

Type: read-only
Reset State: 0x00000000

BT_RX_DETAILED_BAD_STATUS

Bits	Name	Description
7	PYLDFECBAD	0x0: AN_UNCORRECTABLE_2_3_FEC_ERROR_HAS_NOT_BEEN_ENCOUNTERED_DURING_THE_PAYLOAD 0x1: THE_RECEIVE_OPERATION_HAS_BEEN_ABORTED_DUE_TO_A_2_3_FEC_UNCORRECTABLE_DOUBLE_ERROR_IN_THE_PAYLOAD Reset State: 0xxxxxxxxx
6	CRCBAD	0x0: A_CRC_MISMATCH_HAS_NOT_BEEN_ENCOUNTERED 0x1: THE_RECEIVE_OPERATION_HAS_BEEN_ABORTED_FOR_A_CRC_MISMATCH_TIMING_OF_THE_CRC_CHECK_IS_BASED_ON_THE_HECCRCCAPT_CONTROL_REGISTER Reset State: 0xxxxxxxxx
5	LENGTHBAD	0x0: PAYLOAD_BYTE_LENGTH_IS_LESS_THAN_OR_EQUAL_TO_THE_ALLOWED_MAXIMUM 0x1: RECEIVE_OPERATION_HAS_BEEN_ABORTED_FOR_A_PAYLOAD_BYTE_LENGTH_THAT_EXCEEDS_THE_MAXIMUM_FOR_THAT_PARTICULAR_PACKET_TYPE_PAYLOAD_LENGTH_FROM_THE_RECEIVE_PAYLOAD_HEADER_IS_USED_HOWEVER_FOR_SCO_AND_ESCO_PACKETS_THE_PROGRAMMED_EXPECTED_PAYLOAD_LENGTH_RXSCOLNGTH_IS_USED Reset State: 0xxxxxxxxx
3	HDRFECBAD	0x0: NUMBER_OF_1_3_FEC_ERRORS_DURING_THE_PACKET_HEADER_IS_WITHIN_LIMITS 0x1: RECEIVE_OPERATION_HAS_BEEN_ABORTED_BECAUSE_THE_NUMBER_OF_1_3_FEC_ERRORS_DURING_THE_PACKET_HEADER_HAS_EXCEEDED_THE_ACLTHRESH_OR_SCOTHRESH_THRESHOLD_THIS_CHECK_OCCURS_AT_THE_END_OF_THE_PACKET_HEADER_AND_MAY_NOT_OCCUR_IF_AN_HEC_ERROR_CHECKED_ON_THE_FLY_ABORTS_THE_RECEIVE_OPERATION_EARLY Reset State: 0xxxxxxxxx
2	HECBAD	0x0: HEC_MISMATCH_HAS_NOT_BEEN_ENCOUNTERED 0x1: RECEIVE_OPERATION_HAS_BEEN_ABORTED_DUE_TO_A_HEC_MISMATCH_TIMING_OF_THE_HEC_CHECK_IS_BASED_ON_THE_HECALL_AND_HECCRCCAPT_CONTROL_REGISTERS Reset State: 0xxxxxxxxx

BT_RX_DETAILED_BAD_STATUS (cont.)

Bits	Name	Description
1	AMADDRBAD	Reset State: 0xxxxxxxxx
0	WINTO	Reset State: 0xxxxxxxxx

0x3000108 BT_RX_FEC_AND_DONE_STATUS

Type: read-only
Reset State: 0x00000010

BT_RX_FEC_AND_DONE_STATUS

Bits	Name	Description
6	CRCGOOD	0x0: CRC_HAS_NOT_BEEN_CHECKED_OR_A_MISMATCH_WAS_ENCOUNTERED 0x1: 16_BIT_CRC_FIELD_WAS_RECEIVED_WITHOUT_ANY_MISMATCHES Reset State: 0xxxxxxxxx
5	HECGOOD	0x0: HEC_HAS_NOT_BEEN_CHECKED_OR_A_MISMATCH_WAS_ENCOUNTERED 0x1: 8_BIT_HEC_FIELD_WAS_RECEIVED_WITHOUT_ANY_MISMATCHES Reset State: 0xxxxxxxxx
4	RXPKTDONE	0x0: RECEIVE_LOGIC_IS_BUSY_WITH_A_RECEIVE_OPERATION 0x1: RECEIVE_LOGIC_IS_NOT_BUSY_WITH_A_RECEIVE_OPERATION Reset State: 0xxxxxxxxx
3	FECHDRFLAG	0x0: FECHDRCNT_COUNTER_IS_EQUAL_TO_ZERO 0x1: FECHDRCNT_COUNTER_IS_NOT_EQUAL_TO_ZERO Reset State: 0xxxxxxxxx
1	FECCORFLAG	0x0: FECCORCNT_COUNTER_IS_EQUAL_TO_ZERO 0x1: FECCORCNT_COUNTER_IS_NOT_EQUAL_TO_ZERO Reset State: 0xxxxxxxxx
0	FECDETFLAG	0x0: FECDETCNT_COUNTER_IS_EQUAL_TO_ZERO 0x1: FECDETCNT_COUNTER_IS_NOT_EQUAL_TO_ZERO Reset State: 0xxxxxxxxx

0x300010C BT_RX_FRAME_TIMING_ERROR

Type: read-only
Reset State: 0x00000000

BT_RX_FRAME_TIMING_ERROR

Bits	Name	Description
13:0	FRAMEERR	Reset State: 0xxxxxxxxx

0x300011C BT_RX_PACKET_HEADER_ERROR_COUNT

Type: read-only
Reset State: 0x00000000

BT_RX_PACKET_HEADER_ERROR_COUNT

Bits	Name	Description
4:0	FECHDRCNT	Reset State: 0xxxxxxxxx

0x3000124 BT_RX_PAYLOAD_2_3_FEC_ERROR_DETECTED_COUNT

Type: read-only
Reset State: 0x00000000

BT_RX_PAYLOAD_2_3_FEC_ERROR_DETECTED_COUNT

Bits	Name	Description
7:0	FECDETCNT	Reset State: 0xxxxxxxxx

0x3000128 BT_RX_PAYLOAD_FEC_ERROR_CORRECTED_COUNT

Type: read-only
Reset State: 0x00000000

BT_RX_PAYLOAD_FEC_ERROR_CORRECTED_COUNT

Bits	Name	Description
7:0	FECCORCNT	Reset State: 0xxxxxxxxx

0x300012C BT_RX_ENERGY_DETECT_COUNT

Type: read-only
Reset State: 0x00000000

BT_RX_ENERGY_DETECT_COUNT

Bits	Name	Description
15:0	EDCNT	Sub-Section 2.3.12: Receive data registers Reset State: 0xxxxxxxxx

0x3000134 BT_RX_ULP_PAYLOAD_HEADER_DATA

Type: read-only
Reset State: 0x00000000

BT_RX_ULP_PAYLOAD_HEADER_DATA

Bits	Name	Description
31:0	ULPHDR_31_0	Reset State: 0xxxxxxxxx
25:24	B_1	Reset State: 0xxxxxxxxx
23:16	ULPLENGTH	Reset State: 0xxxxxxxxx
7:0	ULPHDR	Reset State: 0xxxxxxxxx

0x3000138 BT_RX_PACKET_HEADER_DATA

Type: read-only
Reset State: 0x00007f00

BT_RX_PACKET_HEADER_DATA

Bits	Name	Description
31:0	PKTHDR_31_0	Reset State: 0xxxxxxxxx
18	SEQN	Reset State: 0xxxxxxxxx
17	ARQN	Reset State: 0xxxxxxxxx
16	FLOW1	Reset State: 0xxxxxxxxx
14:8	PKTINDEX	Reset State: 0xxxxxxxxx
2:0	BASEAMA	Reset State: 0xxxxxxxxx

0x300013C BT_RX_PAYLOAD_HEADER_DATA

Type: read-only
Reset State: 0x00000000

BT_RX_PAYLOAD_HEADER_DATA

Bits	Name	Description
31:0	PYLDHDR_31_0	Reset State: 0xxxxxxxxx
25:16	PYLDLNGTH	Reset State: 0xxxxxxxxx
11:8	UNDEF	Reset State: 0xxxxxxxxx
2	FLOW2	Reset State: 0xxxxxxxxx
1:0	LCH	Reset State: 0xxxxxxxxx

0x3000144 BT_RX_PACKET_HEADER_HEC

Type: read-only
Reset State: 0x00000000

BT_RX_PACKET_HEADER_HEC

Bits	Name	Description
7:0	PKTHDRHEC	Reset State: 0xxxxxxxxx

0x3000148 BT_RX_PAYLOAD_CRC

Type: read-only
Reset State: 0x00000000

BT_RX_PAYLOAD_CRC

Bits	Name	Description
23:0	PYLDCRC	Sub-Section 2.3.13: Transmit setup registers Reset State: 0xxxxxxxxx

0x300014C BT_TX_SCO_PAYLOAD_LENGTH

Type: read-write
Reset State: 0x00000000

BT_TX_SCO_PAYLOAD_LENGTH

Bits	Name	Description
9:0	TXSCOLNGTH	Reset State: 0xxxxxxxxx

0x3000150 BT_TX_BUFFER_POINTER

Type: read-write
Reset State: 0x00000000

BT_TX_BUFFER_POINTER

Bits	Name	Description
15:2	TXBUFPTR	Sub-Section 2.3.14: Transmit status registers Reset State: 0xxxxxxxxx

0x3000158 BT_TX_STATUS

Type: read-only
Reset State: 0x00000000

BT_TX_STATUS

Bits	Name	Description
1	TXBUFERR	0x0: NULL_POINTER_HAS_NOT_BEEN_ENCOUNTERED_OR_ONLY_ONE_EXTRA_READ_HAS_BEEN_REQUESTED_BY_THE_TRANSMIT_LOGIC 0x1: TRANSMIT_LOGIC_HAS_REQUESTED_TWO_MORE_READS_FROM_THE_TRANSMIT_BUFFER_SINCE_THE_NULL_POINTER_WAS_READ_FROM_THE_TRANSMIT_BUFFER_LINK_LIST Reset State: 0xxxxxxxxx
0	TXABORT	Sub-Section 2.3.15: Coexistence registers 0x0: TRANSMIT_OPERATION_WAS_NOT_ABORTED 0x1: TRANSMIT_OPERATION_WAS_ABORTED_BECAUSE_THIS_BLUETOOTH_DEVICE_HAS_LOW_PRIORITY_BTPRIORITY_0_AND_THE_CALCULATED_CHANNEL_FELL_WITHIN_THE_RANGE_OF_802_11_CHANNELS_LOWCHAN_CALCULATED_CHANNEL_HIGHCHAN Reset State: 0xxxxxxxxx

0x300015C BT_COEXISTENCE_RF_ACTIVE_DELAY_TIMER

Type: read-write
Reset State: 0x00000000

BT_COEXISTENCE_RF_ACTIVE_DELAY_TIMER

Bits	Name	Description
6:0	COEXRFDELAY	Reset State: 0xxxxxxxxx

0x3000160 BT_SOFTWARE_CAPTURE_CALCULATE_COMMAND

Type: read-write
Reset State: 0x00000000

BT_SOFTWARE_CAPTURE_CALCULATE_COMMAND

Bits	Name	Description
2	SWCAPT	0x0: DO_NOT_CAPTURE_THE_CLOCK_AND_UAP 0x1: CAPTURE_THE_CLOCK_AND_UAP Reset State: 0xxxxxxxxx
1:0	SWCALC	0x0: DO_NOT_RUN_THE_HOP_CAL_1 0x1: FORCE_THE_HOP_CALCULATOR_WHEN_THIS_COMMAND_IS_ISSUED 0x2: DO_NOT_RUN_THE_HOP_CAL_2 0x3: AUTOMATICALLY_RUNS_THE_HOP_CALCULATOR Reset State: 0xxxxxxxxx

0x3000164 BT_COEXISTENCE_COMMAND

Type: read-write
Reset State: 0x00000000

BT_COEXISTENCE_COMMAND

Bits	Name	Description
15	QTABTRESEND	0x0: LAST_WLAN_HARDWARE_STATE_RESEND_NOT_REQUESTED 0x1: LAST_WLAN_HARDWARE_STATE_RESEND_REQUESTED Reset State: 0xxxxxxxxx
14	QTABTMODE	0x0: RECEIVE_SLOT 0x1: TRANSMIT_SLOT Reset State: 0xxxxxxxxx

BT_COEXISTENCE_COMMAND (cont.)

Bits	Name	Description
13	QTABTMOREDATA	0x0: ACL_BUFFERS_EMPTY 0x1: ACL_BUFFERS_STILL_CONTAIN_DATA Reset State: 0xxxxxxxxx
12:10	QTABTPRIORITY	0x0: PRIORITY_0 0x1: PRIORITY_1 0x2: PRIORITY_2 0x3: PRIORITY_3 0x4: PRIORITY_4 0x5: PRIORITY_5 0x6: PRIORITY_6 0x7: PRIORITY_7 Reset State: 0xxxxxxxxx
9	QTABTAIESYNC	0x0: EVEN_ANCHOR 0x1: ODD_ANCHOR Reset State: 0xxxxxxxxx
8	QTABTACTIVE	0x0: BT_ACTIVE_0 0x1: BT_ACTIVE_1 Reset State: 0xxxxxxxxx
7	STOPSLOT2	0x0: DISABLE_CAPTURING 0x1: ENABLE_CAPTURING Reset State: 0xxxxxxxxx
6	COEXCAPT	0x0: ALLOW_SLOT2_MODE_EXIT_ONLY_IF_A_LINK_CONTROLLER_COMMAND_IS_PRESENT_IN_HALF_SLOT_1 0x1: ALLOW_SLOT2_MODE_EXIT_AFTER_THE_NEXT_TX_OR_RX_COMMAND_TIMEOUT_EXPIRES_COEX_WAITS_FOR_THE_LINK_CONTROLLER_TO_FINISH_PROCESSING Reset State: 0xxxxxxxxx
5:4	COEXCALC	0x0: AUTOMATICALLY_RUNS_THE_HOP_CALCULATOR 0x1: FORCE_THE_HOP_CALCULATOR_TO_RUN 0x2: FORCE_DISABLING_OF_THE_HOP_CALCULATOR Reset State: 0xxxxxxxxx
3	COEXPRI	0x0: LOW_PRIORITY 0x1: HIGH_PRIORITY Reset State: 0xxxxxxxxx
2	COEXMODE	0x0: RECEIVE 0x1: TRANSMIT Reset State: 0xxxxxxxxx

BT_COEXISTENCE_COMMAND (cont.)

Bits	Name	Description
1:0	COEXCMD	0x0: STOP_ACTIVITY_ON_THE_INTERFACE_IMMEDIATELY_BUT_WAIT_FOR_HOP_CALCULATOR_TO_FINISH 0x1: START_SLOT_1_ACTIVITY_THEN_HOLD_THE_INTERFACE_SIGNALS_UNTIL_A_SLOT_2_COMMAND_IS_ISSUED_STATE_MACHINE_MUST_BE_IN_IDLE_WHEN_ISSUING_THIS_COMMAND 0x2: START_AND_FINISH_SLOT_2_ACTIVITY_STATE_MACHINE_SHOULD_ALREADY_BE_WAITING_FOR_A_SLOT_2_COMMAND 0x3: START_AND_FINISH_SLOT_1_ACTIVITY_STATE_MACHINE_MUST_BE_IN_IDLE_WHEN_ISSUING_THIS_COMMAND Reset State: 0xxxxxxxxx

0x3000168 BT_COEXISTENCE_CONTROL

Type: read-write
Reset State: 0x00000000

BT_COEXISTENCE_CONTROL

Bits	Name	Description
15	PTAABORTRX	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
13	CXMABORTRXEN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
12	CXMABORTTXEN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
11	QTAABORTRXEN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
10	QTAABORTTXEN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
9	QTABYPASS	0x0: QTA_BT_TIMING_UNDER_HARDWARE_CONTROL 0x1: QTA_BT_HARDWARE_TIMING_BYPASSED Reset State: 0xxxxxxxxx

BT_COEXISTENCE_CONTROL (cont.)

Bits	Name	Description
7	PTATXHIPRI	0x0: DISABLE_A_TRANSMIT_ABORTED_ACCORDING_TO_THE_PTAABORTTX_AND_PTAABORTTXON_CONTROL_REGISTERS 0x1: ENABLE_TX_CONFX_INPUT_IGNORED_FOR_AN_ENTIRE_FRAME_WHEN_A_HIGH_PRIORITY_TRANSMIT_COMMAND_HAS_BEEN_ISSUED Reset State: 0xxxxxxxxx
6	PTAABORTTXON	0x0: DISABLE 0x1: ENABLE_ABORT_OCCURS_ONLY_IF_PTAABORTTX_1_AND_COEXEN_1_AND_TX_CONFX_1 Reset State: 0xxxxxxxxx
5	PTAABORTTX	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
4	PTAEN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
3	CAVPRIRX	0x0: A_HIGH_PRIORITY_RECEIVE_DOES_NOT_AFFECT_BT_PRIORITY 0x1: SET_BT_PRIORITY_FOR_A_HIGH_PRIORITY_RECEIVE_THAT_IS_IN_THE_802_11X_BAND Reset State: 0xxxxxxxxx
2	CAVPRITX	0x0: HIGH_PRIORITY_TRANSMIT_DOES_NOT_AFFECT_BT_PRIORITY 0x1: SET_BT_PRIORITY_FOR_A_HIGH_PRIORITY_TRANSMIT Reset State: 0xxxxxxxxx
1	CAVABORTTX	0x0: DISABLE_THE_TRANSMIT_ABORT 0x1: ENABLE_THE_TRANSMIT_ABORT_OCCURS_ONLY_IF_COEXEN_1_AND_COEXPRI_0_AND_HOPABORT_1_ON_802_11X_CHANNEL Reset State: 0xxxxxxxxx
0	CAVEN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx

0x300016C BT_COEXISTENCE_ENABLE_AND_POLARITY

Type: read-write
Reset State: 0x00000000

BT_COEXISTENCE_ENABLE_AND_POLARITY

Bits	Name	Description
8	POLCXMGRANT	0x0: NORMAL_HIGH_INPUT_INDICATES_THAT_THE_BLUETOOTH_SHOULD_BE_PREVENTED 0x1: INVERTED_LOW_INPUT_INDICATES_THAT_THE_BLUETOOTH_SHOULD_BE_PREVENTED Reset State: 0xxxxxxxxx
7	COEXEN	0x0: DISABLE_BY_GATING_THE_CLOCK 0x1: ENABLE_BY_UNGATING_THE_CLOCK Reset State: 0xxxxxxxxx
6	QTAEN	0x0: DISABLE_QTA_USE_IN_PTA_MODE_ACCORDING_TO_PTAEN 0x1: ENABLE_QTA Reset State: 0xxxxxxxxx
5	POLCHDATA	0x0: NORMAL_HIGH_INPUT_PREVENTS_BT_PRIORITY_FROM_UPDATING 0x1: INVERTED_LOW_INPUT_PREVENTS_BT_PRIORITY_FROM_UPDATING Reset State: 0xxxxxxxxx
4	POLBTPRI	0x0: NORMAL_HIGH_OUTPUT_INDICATES_A_HIGH_PRIORITY_BLUETOOTH_EVENT 0x1: INVERTED_LOW_OUTPUT_INDICATES_A_HIGH_PRIORITY_BLUETOOTH_EVENT Reset State: 0xxxxxxxxx
3	POLRFACT	0x0: NORMAL_HIGH_OUTPUT_INDICATES_THAT_BLUETOOTH_IS_ACTIVE 0x1: INVERTED_LOW_OUTPUT_INDICATES_THAT_BLUETOOTH_IS_ACTIVE Reset State: 0xxxxxxxxx

BT_COEXISTENCE_ENABLE_AND_POLARITY (cont.)

Bits	Name	Description
2	POLSTAT	0x0: NORMAL_HIGH_OUTPUT_INDICATES_BLUETOOTH_HIGH_PRIORITY_OR_BLUETOOTH_TX 0x1: INVERTED_LOW_OUTPUT_INDICATES_BLUETOOTH_HIGH_PRIORITY_OR_BLUETOOTH_TX Reset State: 0xxxxxxxxx
1	POLFREQ	0x0: NORMAL_HIGH_OUTPUT_INDICATES_A_FREQUENCY_OVERLAP 0x1: INVERTED_LOW_OUTPUT_INDICATES_A_FREQUENCY_OVERLAP Reset State: 0xxxxxxxxx
0	POLTXCNFX	0x0: NORMAL_HIGH_INPUT_INDICATES_THAT_THE_BLUETOOTH_SHOULD_BE_PREVENTED 0x1: INVERTED_LOW_INPUT_INDICATES_THAT_THE_BLUETOOTH_SHOULD_BE_PREVENTED Reset State: 0xxxxxxxxx

0x3000170 BT_COEXISTENCE_STATUS

Type: read-only
Reset State: 0x00000080

BT_COEXISTENCE_STATUS

Bits	Name	Description
15	QTAWLRESEND	0x0: LAST_BLUETOOTH_HARDWARE_STATE_RESEND_NOT_REQUESTED 0x1: LAST_BLUETOOTH_HARDWARE_STATE_RESEND_REQUESTED Reset State: 0xxxxxxxxx
14	QTAWL7	0x0: RESERVED_1 0x1: RESERVED_2 Reset State: 0xxxxxxxxx
13	QTAWL6	0x0: RESERVED_1 0x1: RESERVED_2 Reset State: 0xxxxxxxxx

BT_COEXISTENCE_STATUS (cont.)

Bits	Name	Description
12	QTAWL5	0x0: RESERVED_1 0x1: RESERVED_2 Reset State: 0xxxxxxxxx
11	QTAWL4	0x0: RESERVED_1 0x1: RESERVED_2 Reset State: 0xxxxxxxxx
10	QTAWL3	0x0: RESERVED_1 0x1: RESERVED_2 Reset State: 0xxxxxxxxx
9	QTAWL2	0x0: RESERVED_1 0x1: RESERVED_2 Reset State: 0xxxxxxxxx
8	QTAWLCNFX	0x0: LOW_SIGNAL_IS_BEING_RECEIVED 0x1: HIGH_SIGNAL_IS_BEING_RECEIVED Reset State: 0xxxxxxxxx
7	HOPABORT	0x0: CHANNEL_IS_OUTSIDE_OF_THE_802_11X_CHANNEL_BAND 0x1: CHANNEL_IS_WITHIN_THE_802_11X_CHANNEL_BAND_DOES_NOT_MEAN_TX_ABORT_OCCURRED Reset State: 0xxxxxxxxx
6	TXABORT	Reset State: 0xxxxxxxxx
5	COEXCHDATA	0x0: LOW_SIGNAL_IS_BEING_RECEIVED 0x1: HIGH_SIGNAL_IS_BEING_RECEIVED Reset State: 0xxxxxxxxx
4	COEXBTPRI	0x0: LOW_SIGNAL_IS_BEING_GENERATED 0x1: HIGH_SIGNAL_IS_BEING_GENERATED Reset State: 0xxxxxxxxx
3	COEXRFACT	0x0: LOW_SIGNAL_IS_BEING_GENERATED 0x1: HIGH_SIGNAL_IS_BEING_GENERATED Reset State: 0xxxxxxxxx
2	COEXSTAT	0x0: LOW_SIGNAL_IS_BEING_GENERATED 0x1: HIGH_SIGNAL_IS_BEING_GENERATED Reset State: 0xxxxxxxxx
1	COEXFREQ	0x0: LOW_SIGNAL_IS_BEING_GENERATED 0x1: HIGH_SIGNAL_IS_BEING_GENERATED Reset State: 0xxxxxxxxx
0	COEXTXCNFX	Sub-Section 2.3.16: Test MUX registers 0x0: LOW_SIGNAL_IS_BEING_RECEIVED 0x1: HIGH_SIGNAL_IS_BEING_RECEIVED Reset State: 0xxxxxxxxx

0x3000178 BT_TEST_MUX_CONTROL

Type: read-write
Reset State: 0x00000000

BT_TEST_MUX_CONTROL

Bits	Name	Description
9	TMXFRQ	0x0: HOP_FREQUENCY_IS_ALIGNED_TO_TRANSITIONS_OF_BIT_0_OF_THE_SELECTED_BLUETOOTH_CLOCK 0x1: HOP_FREQUENCY_IS_AVAILABLE_IMMEDIATELY Reset State: 0xxxxxxxxx
8	TMXPAGE	Reset State: 0xxxxxxxxx
7:4	TMXSEL1	Reset State: 0xxxxxxxxx
3:0	TMXSEL0	Reset State: 0xxxxxxxxx

0x300017C BT_TEST_MUX_DEBUG_OUTPUT

Type: read-write
Reset State: 0x00000000

BT_TEST_MUX_DEBUG_OUTPUT

Bits	Name	Description
15:0	TMXDEBUG	Sub-Section 2.3.17: Test MUX output selection Sub-Section 2.3.18: Hardware verification registers Reset State: 0xxxxxxxxx

0x3000184 BT_HARDWARE_VERIFICATION_CONTROL_1

Type: read-write
Reset State: 0x00000000

BT_HARDWARE_VERIFICATION_CONTROL_1

Bits	Name	Description
2	BBIF_ENABLE	Reset State: 0xxxxxxxxx
1	PKTRPTEN	Reset State: 0xxxxxxxxx
0	BBIFDEBUG	0x0: DISABLE_NORMAL 0x1: ENABLE_FOR_TESTING Reset State: 0xxxxxxxxx

0x3000188 BT_HARDWARE_VERIFICATION_CONTROL_2

Type: read-write
Reset State: 0x00000000

BT_HARDWARE_VERIFICATION_CONTROL_2

Bits	Name	Description
5:4	LCCONT	0x0: SINGLE_OVERLAID_EXECUTION_ON_HALFSLOT_BOUNDARIES_NORMAL 0x1: CONTINUOUS_OVERLAID_EXECUTION_ON_HALFSLOT_BOUNDARIES_FOR_TESTING 0x2: CONTINUOUS_PING_PONGED_EXECUTION_ON_SLOT_BOUNDARIES_FOR_TESTING 0x3: CONTINUOUS_EXTERNALLY_TRIGGERED_EXECUTION_ON_HALFSLOT_BOUNDARIES_FOR_TESTING Reset State: 0xxxxxxxxx
3:2	BTCLKDIS	0x0: BT_CLKN_IS_RUNNING_FRE_1_NORMAL 0x1: BT_CLKN_IS_RUNNING_FRE_2_TESTING 0x2: BT_CLKN_INTEGER_AND_FRACTIONAL_PORTION_IS_FROZEN_USED_FOR_BERT_TESTING 0x3: BT_CLKN_INTEGER_AND_FRACTIONAL_PORTION_IS_FROZEN_TESTING Reset State: 0xxxxxxxxx
1	BERTPRBS	0x0: PRBS_9_PATTERN_INITIALIZED_WITH_ALL_ONES 0x1: PRBS_15_PATTERN_INITIALIZED_WITH_ALL_ONES Reset State: 0xxxxxxxxx
0	BTCLKSEL	0x0: SELECT_BT_CLKA 0x1: SELECT_BT_CLKN Reset State: 0xxxxxxxxx

0x300018C BT_HARDWARE_VERIFICATION_CONTROL_3

Type: read-write
Reset State: 0x00000000

BT_HARDWARE_VERIFICATION_CONTROL_3

Bits	Name	Description
2:0	RMIF_FORCE	Reset State: 0xxxxxxxxx

0x3000190 BT_HARDWARE_VERIFICATION_CLEAR_STATE_MACHINES

Type: read-write
Reset State: 0x00000000

BT_HARDWARE_VERIFICATION_CLEAR_STATE_MACHINES

Bits	Name	Description
6	CLRCOEXFSM	0x0: NO_CHANGE 0x1: FORCE_THE_COEXISTENCE_FSM_AND_PENDING_COMMAND_BACK_TO_IDLE Reset State: 0xxxxxxxxx
5	CLRBUFFSM	0x0: NO_CHANGE 0x1: FORCE_THE_BUFFER_CONTROL_FSM_IDLE Reset State: 0xxxxxxxxx
4	CLRBBIFFSM	0x0: NO_CHANGE 0x1: FORCE_THE_BBIF_FSM_TO_IDLE Reset State: 0xxxxxxxxx
3	CLRHOPFSM	0x0: NO_CHANGE 0x1: FORCE_THE_HOP_CALCULATOR_AND_MODULO_DIVIDER_FSM_TO_IDLE_ALL_OTHER_STATE_MACHINE_OUTPUTS_DIVIDEND_DIVISOR_HOP_CHANNEL_ARE_FORCED_TO_ZERO Reset State: 0xxxxxxxxx
2	CLRLCFSM	0x0: NO_CHANGE 0x1: FORCE_THE_LC_FSM_AND_PENDING_COMMANDS_TO_IDLE Reset State: 0xxxxxxxxx
1	CLRTXFSM	0x0: NO_CHANGE 0x1: FORCE_THE_TX_CONTROL_FSM_TO_IDLE Reset State: 0xxxxxxxxx
0	CLRRXFSM	0x0: NO_CHANGE 0x1: FORCE_THE_RX_CONTROL_FSM_TO_IDLE_DISABLE_RX_SCAN_WINDOW Reset State: 0xxxxxxxxx

0x3000194 BT_HARDWARE_VERIFICATION_STATUS_1

Type: read-only
Reset State: 0x00000000

BT_HARDWARE_VERIFICATION_STATUS_1

Bits	Name	Description
15:0	RXHDRERR	Reset State: 0xxxxxxxxx

0x3000198 BT_HARDWARE_VERIFICATION_STATUS_2

Type: read-only
Reset State: 0x00000000

BT_HARDWARE_VERIFICATION_STATUS_2

Bits	Name	Description
15:0	RXPYLDERR	Sub-Section 2.3.19: Core Version register Reset State: 0xxxxxxxxx

0x300019C BT_BT_CORE_VERSION

Type: read-only
Reset State: 0x10010000

BT_BT_CORE_VERSION

Bits	Name	Description
31:28	MAJORVERSION	Reset State: 0xxxxxxxxx
27:16	MINORVERSION	Reset State: 0xxxxxxxxx
15:0	STEP	Sub-Section 2.3.20: Hardware initialization registers Reset State: 0xxxxxxxxx

0x30001A0 BT_PACKET_CONTROL

Type: read-write
Reset State: 0x00000000

BT_PACKET_CONTROL

Bits	Name	Description
6	CMDABORTDIS	0x0: ENABLE 0x1: DISABLE Reset State: 0xxxxxxxxx

BT_PACKET_CONTROL (cont.)

Bits	Name	Description
5	HECCRCCAPT	0x0: TIMING_OF_THE_HEC_CHECK_IS_BASED_ON_THE_HECALL_CONTROL_REGISTER_CHECK_THE_CRC_ON_THE_FLY_AS_THE_BITS_ARE_RECEIVED_AND_ABORT_THE_RECEIVE_IMMEDIATELY_IF_A_CRC_MISMATCH_IS_DETECTED 0x1: RECEIVE_ALL_THE_HEC_AND_CRC_BITS_BEFORE_CHECKING_FOR_POSSIBLE_MISMATCHES Reset State: 0xxxxxxxxx
4	SCRDIS	0x0: ENABLE_SCRAMBLING_OF_PACKET_HEADER_AND_PAYLOAD 0x1: DISABLE_ALL_SCRAMBLING Reset State: 0xxxxxxxxx
2	SCOCRCEN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
1	AUX1FECEN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
0	AUX1CRCEN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx

0x30001A4 BT_TEST_CONTROL

Type: read-write
Reset State: 0x00000000

BT_TEST_CONTROL

Bits	Name	Description
7	TXINVCRC	0x0: TRANSMIT_CORRECT_CRC_BITS 0x1: INVERT_CRC_BITS_BEFORE_TRANSMIT Reset State: 0xxxxxxxxx
6	ACDCARRIER	0x0: IGNORE_THE_CARRIER_DETECT_INPUT_FROM_THE_RM_AND_FORCES_AN_ACTIVE_ENERGY_STICKY_BIT 0x1: MODEM_CORRELATOR_OUTPUT_IS_ONLY_VALID_WHEN_THE_ENERGY_STICKY_BIT_IS_ACTIVE_BIT_IS_CLEARED_AT_THE_BEGINNING_OF_A_RECEIVE_OPERATION_AND_IS_SET_WHEN_CARRIER_DETECT_1_FOR_AT_LEAST_125_NSEC Reset State: 0xxxxxxxxx

BT_TEST_CONTROL (cont.)

Bits	Name	Description
5	RXABORTDIS	0x0: ENABLE 0x1: DISABLE_ALL_RECEIVE_ABORT_MECHANISMS_ALLOWS_ABORT_STATUS_TO_BE_GENERATED_WITHOUT_ACTUALLY_ABORTING_THE_RECEIVE_OPERATION Reset State: 0xxxxxxxxx
4	RXBUFDIS	0x0: RECEIVE_OPERATION_IS_ABORTED_WHEN_A_NULL_POINTER_IS_READ_FROM_ONE_OF_THE_RECEIVE_LINK_LISTS 0x1: RECEIVE_OPERATION_NOT_TO_BE_ABORTED_WHEN_A_NULL_POINTER_IS_READ_FROM_ONE_OF_THE_RECEIVE_LINK_LISTS_WHILE_THE_RECEIVE_OPERATION_CONTINUES_FURTHER_WRITES_TO_THE_SHARED_RAM_ARE_PREVENTED_DISABLES_STATUS Reset State: 0xxxxxxxxx
3	RXCRCDIS	0x0: ENABLE_CRC_IS_CHECKED_ON_THE_FLY_AND_IMMEDIATELY_ABORTS_UPON_A_MISMATCH 0x1: DISABLE Reset State: 0xxxxxxxxx
2	RXLNGTHDIS	0x0: ENABLE_THE_PAYLOAD_BYTE_LENGTH_CHECKER_RECEIVE_TO_BE_ABORTED_WHEN_A_PAYLOAD_BYTE_LENGTH_EXCEEDS_THE_MAXIMUM_FOR_THAT_PACKET_TYPE_PAYLOAD_LENGTH_FROM_THE_RECEIVE_PAYLOAD_HEADER_IS_USED_EXCEPT_FOR_SCO_AND_ESCO_PACKETS_THEN_THE_EXPECTED_PAYLOAD_LENGTH_RXSCOLNGTH_IS_USED 0x1: DISABLE Reset State: 0xxxxxxxxx
1	RXFECDIS	0x0: ENABLE_RECEIVE_OPERATION_TO_BE_ABORTED_WHEN_A_2_3_FEC_UNCORRECTABLE_DOUBLE_ERROR_IS_DETECTED_IN_THE_PAYLOAD 0x1: DISABLE Reset State: 0xxxxxxxxx
0	RXHECDIS	0x0: ENABLE_RECEIVE_OPERATION_TO_BE_ABORTED_WHEN_A_HEC_MISMATCH_OCCURS_TIMING_IS_BASED_ON_THE_HECALL_CONTROL_REGISTER 0x1: DISABLE Reset State: 0xxxxxxxxx

0x30001A8 BT_ULP_CONTROL_2

Type: read-write
Reset State: 0x00000000

BT_ULP_CONTROL_2

Bits	Name	Description
0	ULPSCANABORTMODE	0x0: STOP_SCAN_ONLY_UPON_RECEIVING_A_PACKET_WITH_A_GOOD_CRC 0x0: STOP_SCAN_ONLY_UPON_RECEIVING_A_PACKET_WITH_A_GOOD_OR_BAD_CRC Reset State: 0xxxxxxxxx

0x30001AC BT_BLUETOOTH_CLOCK_N_INTEGER_COMPARE_VALUE_0

Type: read-write
Reset State: 0x00000000

BT_BLUETOOTH_CLOCK_N_INTEGER_COMPARE_VALUE_0

Bits	Name	Description
27:0	CLKCMPINTGR_27_0	Reset State: 0xxxxxxxxx

0x30001B0 BT_BLUETOOTH_CLOCK_N_FRACTIONAL_COMPARE_VALUE_0

Type: read-write
Reset State: 0x00000000

BT_BLUETOOTH_CLOCK_N_FRACTIONAL_COMPARE_VALUE_0

Bits	Name	Description
12:0	CLKCMPFRACT_12_0	Reset State: 0xxxxxxxxx

0x30001B4 BT_BLUETOOTH_CLOCK_N_INTEGER_COMPARE_VALUE_1

Type: read-write
Reset State: 0x00000000

BT_BLUETOOTH_CLOCK_N_INTEGER_COMPARE_VALUE_1

Bits	Name	Description
27:0	CLKCMPINTGR_27_0	Reset State: 0xxxxxxxxx

0x30001B8 BT_BLUETOOTH_CLOCK_N_FRACTIONAL_COMPARE_VALUE_1

Type: read-write
Reset State: 0x00000000

BT_BLUETOOTH_CLOCK_N_FRACTIONAL_COMPARE_VALUE_1

Bits	Name	Description
12:0	CLKCMPFRACT_12_0	Reset State: 0xxxxxxxxx

0x30001BC BT_BURST_COEXISTENCE_COMMAND

Type: read-write
Reset State: 0x00000000

BT_BURST_COEXISTENCE_COMMAND

Bits	Name	Description
13:0	BRSTCOEXCMD	Reset State: 0xxxxxxxxx

0x30001C0 BT_BURST_COEXISTENCE_STATUS

Type: read-write
Reset State: 0x00000000

BT_BURST_COEXISTENCE_STATUS

Bits	Name	Description
13:0	BRSTCOEXSTAT	Reset State: 0xxxxxxxxx

0x30001C4 BT_BURST_PRESLOT

Type: read-write
Reset State: 0x00000000

BT_BURST_PRESLOT

Bits	Name	Description
12:0	BRSTPRESLOT	Reset State: 0xxxxxxxxx

0x30001C8 BT_BURST_TX_COMMAND

Type: read-write
Reset State: 0x00000000

BT_BURST_TX_COMMAND

Bits	Name	Description
12:0	BRSTTXCMD	Reset State: 0xxxxxxxxx

0x30001CC BT_BURST_TX_HOP_STROBE

Type: read-write
Reset State: 0x00000000

BT_BURST_TX_HOP_STROBE

Bits	Name	Description
12:0	BRSTTXHSTB	Reset State: 0xxxxxxxxx

0x30001D0 BT_BURST_TX_ON

Type: read-write
Reset State: 0x00000000

BT_BURST_TX_ON

Bits	Name	Description
12:0	BRSTTXON	Reset State: 0xxxxxxxxx

0x30001D4 BT_BURST_RX_COMMAND

Type: read-write
Reset State: 0x00000000

BT_BURST_RX_COMMAND

Bits	Name	Description
12:0	BRSTRXCMD	Reset State: 0xxxxxxxxx

0x30001D8 BT_BURST_RX_HOP_STROBE

Type: read-write
Reset State: 0x00000000

BT_BURST_RX_HOP_STROBE

Bits	Name	Description
12:0	BRSTRXHSTB	Reset State: 0xxxxxxxxx

0x30001DC BT_BURST_RX_ON

Type: read-write
Reset State: 0x00000000

BT_BURST_RX_ON

Bits	Name	Description
12:0	BRSTRXON	Reset State: 0xxxxxxxxx

0x30001E0 BT_RX_ACCESS_CODE_DETECT_HARD_ALIGN

Type: read-write
Reset State: 0x00000000

BT_RX_ACCESS_CODE_DETECT_HARD_ALIGN

Bits	Name	Description
12:0	RXACDALIGN	Reset State: 0xxxxxxxxx

0x30001E4 BT_RX_PACKET_HEADER_HARD_ALIGN

Type: read-write
Reset State: 0x00000000

BT_RX_PACKET_HEADER_HARD_ALIGN

Bits	Name	Description
13:0	RXHDRALIGN	Reset State: 0xxxxxxxxx

0x30001E8 BT_TX_GUARD_SYNC_LENGTH

Type: read-write
Reset State: 0x00000000

BT_TX_GUARD_SYNC_LENGTH

Bits	Name	Description
4:0	TXGSLNGTH	Reset State: 0xxxxxxxxx

0x30001EC BT_SOFTWARE_INTERRUPT_LATENCY

Type: read-write
Reset State: 0x00000000

BT_SOFTWARE_INTERRUPT_LATENCY

Bits	Name	Description
4:0	SWINTLAT	Reset State: 0xxxxxxxxx

0x30001F0 BT_RX_DEMODULATOR_DELAY

Type: read-write
Reset State: 0x00000000

BT_RX_DEMODULATOR_DELAY

Bits	Name	Description
3:0	RXDMDDLY	Reset State: 0xxxxxxxxx

0x30001F4 BT_TX_PACKET_HEADER_HARD_ALIGN

Type: read-write
Reset State: 0x00000000

BT_TX_PACKET_HEADER_HARD_ALIGN

Bits	Name	Description
13:0	TXHDRALIGN	Reset State: 0xxxxxxxxx

0x30001FC BT_BT_TO_LPASS_AUDIO

Type: read-write
Reset State: 0x00000000

BT_BT_TO_LPASS_AUDIO

Bits	Name	Description
0	BTLAPSSAUDIORXINTR	Reset State: 0xxxxxxxxx

0x3000200 BT_LC_RX_AGC_RSSI_OUT_0

Type: read-only
Reset State: 0x00000000

BT_LC_RX_AGC_RSSI_OUT_0

Bits	Name	Description
17:16	LNA_AGC_GAIN	0x0: HIGH 0x1: NOMINAL 0x3: LOW Reset State: 0xxxxxxxxx
15:0	AGC_RSSI	Reset State: 0xxxxxxxxx

0x3000204 BT_LC_RX_AGC_RSSI_OUT_1

Type: read-only
Reset State: 0x00000000

BT_LC_RX_AGC_RSSI_OUT_1

Bits	Name	Description
17:16	LNA_AGC_GAIN	0x0: HIGH 0x1: NOMINAL 0x3: LOW Reset State: 0xxxxxxxxx
15:0	AGC_RSSI	Reset State: 0xxxxxxxxx

0x3000208 BT_LC_SIF_CTRL

Type: read-write
Reset State: 0x00000000

BT_LC_SIF_CTRL

Bits	Name	Description
0	LC_SIF_SW_RESET	Sub-Section 2.3.21: Hardware upgrade registers Sub-Section 2.3.21.1: ULP registers Reset State: 0xxxxxxxxx

0x3000348 BT_INT_0_ULP_BTC_SLOT_BURST_TIMER

Type: read-write
Reset State: 0x00000000

BT_INT_0_ULP_BTC_SLOT_BURST_TIMER

Bits	Name	Description
13:0	SLOTTIMER	Reset State: 0xxxxxxxxx

0x300034C BT_ULP_BURST_COEXISTENCE_COMMAND

Type: read-write
Reset State: 0x00000000

BT_ULP_BURST_COEXISTENCE_COMMAND

Bits	Name	Description
13:0	BRSTCOEXCMD	Reset State: 0xxxxxxxxx

0x3000350 BT_ULP_BURST_COEXISTENCE_STATUS

Type: read-write
Reset State: 0x00000000

BT_ULP_BURST_COEXISTENCE_STATUS

Bits	Name	Description
13:0	BRSTCOEXSTAT	Reset State: 0xxxxxxxxx

0x3000354 BT_ULP_BURST_PRESLOT

Type: read-write
Reset State: 0x00000000

BT_ULP_BURST_PRESLOT

Bits	Name	Description
13:0	BRSTPRESLOT	Reset State: 0xxxxxxxxx

0x3000358 BT_ULP_BURST_TX_COMMAND

Type: read-write
Reset State: 0x00000000

BT_ULP_BURST_TX_COMMAND

Bits	Name	Description
13:0	BRSTTXCMD	Reset State: 0xxxxxxxxx

0x300035C BT_ULP_BURST_TX_HOP_STROBE

Type: read-write
Reset State: 0x00000000

BT_ULP_BURST_TX_HOP_STROBE

Bits	Name	Description
13:0	BRSTTXHSTB	Reset State: 0xxxxxxxxx

0x3000360 BT_ULP_BURST_TX_ON

Type: read-write
Reset State: 0x00000000

BT_ULP_BURST_TX_ON

Bits	Name	Description
13:0	BRSTTXON	Reset State: 0xxxxxxxxx

0x3000364 BT_ULP_BURST_RX_COMMAND

Type: read-write
Reset State: 0x00000000

BT_ULP_BURST_RX_COMMAND

Bits	Name	Description
13:0	BRSTRXCMD	Reset State: 0xxxxxxxxx

0x3000368 BT_ULP_BURST_RX_HOP_STROBE

Type: read-write
Reset State: 0x00000000

BT_ULP_BURST_RX_HOP_STROBE

Bits	Name	Description
13:0	BRSTRXHSTB	Reset State: 0xxxxxxxxx

0x300036C BT_ULP_BURST_RX_ON

Type: read-write
Reset State: 0x00000000

BT_ULP_BURST_RX_ON

Bits	Name	Description
13:0	BRSTRXON	Reset State: 0xxxxxxxxx

0x3000370 BT_PACKET_REPEAT_NUMBER

Type: read-write
Reset State: 0x00000000

BT_PACKET_REPEAT_NUMBER

Bits	Name	Description
15:0	PKTRPTNUM	Reset State: 0xxxxxxxxx

0x3000374 BT_GOOD_CRC_COUNTER

Type: read-only
Reset State: 0x00000000

BT_GOOD_CRC_COUNTER

Bits	Name	Description
15:0	GOODCRCCTR	Reset State: 0xxxxxxxxx

0x3000378 BT_ULP_RX_HARD_ALIGN

Type: read-write
Reset State: 0x00000000

BT_ULP_RX_HARD_ALIGN

Bits	Name	Description
13:0	RXHDRALIGN	Reset State: 0xxxxxxxxx

0x300037C BT_ULP_CONTROL

Type: read-write
Reset State: 0x00000000

BT_ULP_CONTROL

Bits	Name	Description
7	RESETFRACCLK	0x0: NO_EFFECT 0x1: RESET_FRACTIONAL_CLOCK Reset State: 0xxxxxxxxx
6	SKIPCALC	0x0: PROCESS_HOP_CALCULATION_EVEN_IF_IT_IS_NOT_NEEDED 0x1: SKIP_HOP_CALCULATION_STATE_HOPSTROBE_BURST_TIMER_IS_IGNORED Reset State: 0xxxxxxxxx
5	CMD0EN	0x0: USE_LEGACY_COMMAND_0_1_PROCESSING_BASED_ON_BLUETOOTH_CLOCK 0x1: ALWAYS_USE_COMMAND_0 Reset State: 0xxxxxxxxx
4	ULPMODMODE	0x0: MODULATION_MOD_IS_GFSK_BR 0x1: MODULATION_MODE_IS_GMSK_ULP Reset State: 0xxxxxxxxx

BT_ULP_CONTROL (cont.)

Bits	Name	Description
3	ULPMODBYP	0x0: DO_NOT_BYPASS_MODULATION_IS_GMSK_ONLY_DURING_ULP_MODE 0x1: SET_MODULATION_MODE_ACCORDING_TO_ULPMODMODE_BIT Reset State: 0xxxxxxxxx
2	TXHDRALIGNEN	0x0: DISABLE_ULP_TX_HEADER_SLOT_ALIGNMENT 0x1: ENABLE_ULP_TX_HEADER_SLOT_ALIGNMENT_WHEN_A_VALID_PAYLOAD_LENGTH_HAS_BEEN_CAPTURED Reset State: 0xxxxxxxxx
1	ULPCORRMODE	0x0: CORRELATE_AGAINST_32_BIT_SYNC_WORD_DEFAULT 0x1: CORRELATE_AGAINST_32_BIT_SYNC_WORD_AND_4_MSBS_OF_PREAMBLE Reset State: 0xxxxxxxxx
0	ULPEN	0x0: ENABLE_BLUETOOTH_TIME_DOMAIN 0x1: ENABLE_ULP_TIME_DOMAIN Reset State: 0xxxxxxxxx

0x3000380 BT_ULP_HOP_OFFSET

Type: read-write
Reset State: 0x00000000

BT_ULP_HOP_OFFSET

Bits	Name	Description
6:0	HOPOFFSET	Reset State: 0xxxxxxxxx

0x3000388 BT_BLUETOOTH_CLOCK_N_INTEGER_COMPARE_VALUE_2

Type: read-write
Reset State: 0x00000000

BT_BLUETOOTH_CLOCK_N_INTEGER_COMPARE_VALUE_2

Bits	Name	Description
27:0	CLKCMPINTGR_27_0	Reset State: 0xxxxxxxxx

0x300038C BT_BLUETOOTH_CLOCK_N_FRACTIONAL_COMPARE_VALUE_2

Type: read-write
Reset State: 0x00000000

BT_BLUETOOTH_CLOCK_N_FRACTIONAL_COMPARE_VALUE_2

Bits	Name	Description
12:0	CLKCMPFRACT_12_0	Reset State: 0xxxxxxxxx

0x3000390 BT_CRYPTO_TX_PAYLOAD_BUFFER_POINTER_AND_LENGTH

Type: read-write
Reset State: 0x00000000

BT_CRYPTO_TX_PAYLOAD_BUFFER_POINTER_AND_LENGTH

Bits	Name	Description
31:18	PAYLOAD_PTR	Reset State: 0xxxxxxxxx
9:0	PAYLOAD_LENGTH	Reset State: 0xxxxxxxxx

0x3000394 BT_CRYPTO_KEYN

Type: read-write
Reset State: 0x00000000

BT_CRYPTO_KEYN

Bits	Name	Description
15:2	KEYN_ADDR	Reset State: 0xxxxxxxxx

0x3000398 BT_CRYPTO_A0_B0_B1

Type: read-write
Reset State: 0x00000000

BT_CRYPTO_A0_B0_B1

Bits	Name	Description
15:2	A0_B0_B1_ADDR	Reset State: 0xxxxxxxxx

0x300039C BT_ERROR_STATUS_REGISTER

Type: read-only
Reset State: 0x00000000

BT_ERROR_STATUS_REGISTER

Bits	Name	Description
3	ERROR_CRPT_WR	0x1: BTC_W_REQ_CC_ERROR_FROM_CRYPTO_AHB_CTRL Reset State: 0xxxxxxxxx
2	ERROR_CRPT_RD	0x1: BTC_R_REQ_CC_ERROR_FROM_CRYPTO_AHB_CTRL Reset State: 0xxxxxxxxx
1	ERROR_CTRL_WR	0x1: BTC_W_REQ_ERROR_FROM_BUFFER_CONTROLLER Reset State: 0xxxxxxxxx
0	ERROR_CTRL_RD	0x1: BTC_R_REQ_ERROR_FROM_BUFFER_CONTROLLER Reset State: 0xxxxxxxxx

0x30003A0 BT_CLOCK_GATING

Type: read-write
Reset State: 0x00000000

BT_CLOCK_GATING

Bits	Name	Description
3	DIS_GAS_CLK_GATING	0x0: ALLOWS_HARDWARE_TO_CLOCK_GATE_FOR_LOW_POWER 0x1: FORCES_CLOCK_ON Reset State: 0xxxxxxxxx
2	DIS_GAM_CLK_GATING	0x0: ALLOWS_HARDWARE_TO_CLOCK_GATE_FOR_LOW_POWER 0x1: FORCES_CLOCK_ON Reset State: 0xxxxxxxxx
1	SW_RESET	0x0: NORMAL 0x1: RESET Reset State: 0xxxxxxxxx
0	CRYPTO_CLK_GATING_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx

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0x3000050 BT_CMPR_EN

Type: read-write
Reset State: 0x00000000

BT_CMPR_EN

Bits	Name	Description
1	CMPR_INT_STAT_1	Reset State: 0xxxxxxxxx
0	CMPR_EN_0	0x1: ENABLE Reset State: 0xxxxxxxxx

0x3000054 BT_CMPR_INTGR

Type: read-write
Reset State: 0x00000000

BT_CMPR_INTGR

Bits	Name	Description
27:0	CMPR_INTGR_27_0	Reset State: 0xxxxxxxxx

0x3000058 BT_CMPR_FRACT

Type: read-write
Reset State: 0x00000000

BT_CMPR_FRACT

Bits	Name	Description
12:0	CMPR_FRACT_12_0	Reset State: 0xxxxxxxxx

0x3000070 BT_COUNTVAL

Type: read-write
Reset State: 0x0000fa00

BT_COUNTVAL

Bits	Name	Description
16:0	COUNTVAL_16_0	Reset State: 0xxxxxxxxx

0x30000A0 BT_PVC_SSBI2_INTR

Type: read-write
Reset State: 0x00000008

BT_PVC_SSBI2_INTR

Bits	Name	Description
5	PVC_BUSY	0x1: PVC_SSBI2_HARDWARE_PORT_IS_BUSY 0x0: SOFTWARE_PERFORMS_SSBI2_READS_WRITES_WHEN_THIS_BIT_IS_UNSET_TO_ALLOW_PVC_TRAFFIC_PRIORITY Reset State: 0xxxxxxxxx
4	SSBI2_INT	0x1: SSBI2_INT_ENABLE_0_IS_SET_AND_SSBI2_RD_STATUS_27_IS_SET Reset State: 0xxxxxxxxx
3	PVC_FIFO_EMPTY	Reset State: 0xxxxxxxxx
2	ENABLE_PVC_FIFO_EMPTY_INTR	0x1: ENABLE_PVC_FIFO_EMPTY_CONDITION_TO_ACTIVATE_SSBI2_INTR_INTRERRUPT_LINE Reset State: 0xxxxxxxxx
1	PVC_FIFO_FULL	Reset State: 0xxxxxxxxx
0	ENABLE_PVC_FIFO_FULL_INTR	0x1: ENABLE_PVC_FIFO_FULL_CONDITION_TO_ACTIVATE_SSBI2_INTR_INTERRUPT_LINE Reset State: 0xxxxxxxxx

0x30000CC BT_DEBUG_SEL

Type: read-write
Reset State: 0x00000000

BT_DEBUG_SEL

Bits	Name	Description
2:0	DEBUG_SEL	0x0: 32M_SERIAL_INTERFACE_BLOCK 0x1: 32M_LINK_CONTROLLER 0x2: 32M_RESERVED 0x3: 32M_RESERVEDZ 0x4: 32M_RESERVEDZZ 0x5: 32M_SERIAL_INTERFACE_BLOCKZ Reset State: 0xxxxxxxxx

0x3000100 BT_CONTROL

Type: read-write
Reset State: 0x00000000

BT_CONTROL

Bits	Name	Description
2	CONTROL_2	0x0: SELECTS_CALIBRATION_LENGTH_OF_64 0x1: SELECTS_CALIBRATION_LENGTH_OF_128 Reset State: 0xxxxxxxxx
1:0	CONTROL_1_0	0x0: CALIBRATOR_DISABLED 0x1: CALIBRATE_ONCE_WHEN_ISSUED 0x2: CALIBRATE_WHEN_ISSUED_REPEAT_CALIBRATION_AFTER_EXITING_DEEP_SLEEP 0x3: CALIBRATE_CONTINUOUSLY Reset State: 0xxxxxxxxx

0x3000104 BT_COMPLETE

Type: read-write
Reset State: 0x00000000

BT_COMPLETE

Bits	Name	Description
0	COMPLETE_0	Reset State: 0xxxxxxxxx

0x3000120 BT_CLKN_CAPTURE_CTL

Type: read-write
Reset State: 0x00000000

BT_CLKN_CAPTURE_CTL

Bits	Name	Description
2	CLKN_CAPTURE_BUSY	0x0: IDLE 0x1: BUSY Reset State: 0xxxxxxxxx
1	CLKN_PULSE_32K	Reset State: 0xxxxxxxxx
0	CLKN_CAPTURE_PULSE_EN	Reset State: 0xxxxxxxxx

0x3000124 BT_CLKN_CAPTURE_INTEGER_VAL

Type: read-only
Reset State: 0x00000000

BT_CLKN_CAPTURE_INTEGER_VAL

Bits	Name	Description
27:0	CLKN_INTEGER	Reset State: 0xxxxxxxxx

0x3000128 BT_CLKN_CAPTURE_FRACT_VAL

Type: read-only
Reset State: 0x00000000

BT_CLKN_CAPTURE_FRACT_VAL

Bits	Name	Description
12:0	CLKN_FRACT	Reset State: 0xxxxxxxxx

0x3000130 BT_MASTER_MEM_ADDR

Type: read-write
Reset State: 0x00000328

BT_MASTER_MEM_ADDR

Bits	Name	Description
15:0	MASTER_ADDR	Reset State: 0xxxxxxxxx

0x3000134 BT_SLAVE_BT_ADDR

Type: read-write
Reset State: 0x00000300

BT_SLAVE_BT_ADDR

Bits	Name	Description
15:7	SLAVE_ADDR	Reset State: 0xxxxxxxxx
6:0	RESERVED_X134	Reset State: 0xxxxxxxxx

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0x3000000 BT_INTR

Type: write-only
Reset State: 0x00000000

BT_INTR

Bits	Name	Description
26	RX_FIFO_UFLOW_INTR	Receive FIFO Underflow interrupt status bit. Software must write a 1 to this bit to clear it. Reset State: 0x00000000
25	RX_FIFO_OFLOW_INTR	Receive FIFO Overflow interrupt status bit. Software must write a 1 to this bit to clear it. Reset State: 0x00000000
24	RX_FIFO_RDY_INTR	Receive FIFO Ready interrupt status bit: Indicates when the Receive FIFO is ready to be drained of software characters. This interrupt is set every clock cycle while the FIFO fill level is greater than the Receive FIFO Trigger Level (rx_trig_level). Software must write a 1 to this bit to clear it. Reset State: 0x00000000
17	TX_FIFO_OFLOW_INTR	Transmit FIFO Overflow interrupt status bit. Software must write a 1 to this bit to clear it. Reset State: 0x00000000
16	TX_FIFO_RDY_INTR	Transmit FIFO Ready interrupt status bit: Indicates when the Transmit FIFO is ready to accept more software characters for transmission. This interrupt is set every clock cycle while the FIFO fill level is less than or equal to the Transmit FIFO Trigger Level (tx_trig_level). Software must write a 1 to this bit to clear it. Reset State: 0x00000000
8	RX_HW_CHAR_INTR	Received Hardware Character interrupt status bit. Software must write a 1 to this bit to clear it. Reset State: 0x00000000
1	PARITY_ERR_INTR	UART Parity Error interrupt status bit. Software must write a 1 to this bit to clear it. Reset State: 0x00000000
0	FRAME_ERR_INTR	UART Frame Error interrupt status bit. Software must write a 1 to this bit to clear it. Reset State: 0x00000000

0x3000004 BT_INTR_EN

Type: read-write
Reset State: 0x00000000

BT_INTR_EN

Bits	Name	Description
26	RX_FIFO_UFLOW_INTR_EN	Interrupt enable for the Receive FIFO Underflow interrupt. Reset State: 0x00000000
25	RX_FIFO_OFLOW_INTR_EN	Interrupt enable for the Receive FIFO Overflow interrupt. Reset State: 0x00000000
24	RX_FIFO_RDY_INTR_EN	Interrupt enable for the Receive FIFO Ready interrupt. Reset State: 0x00000000
17	TX_FIFO_OFLOW_INTR_EN	Interrupt enable for the Transmit FIFO Overflow interrupt. Reset State: 0x00000000
16	TX_FIFO_RDY_INTR_EN	Interrupt enable for the Transmit FIFO Ready interrupt. Reset State: 0x00000000
8	RX_HW_CHAR_INTR_EN	Interrupt enable for the Received Hardware Character interrupt. Reset State: 0x00000000
1	PARITY_ERR_INTR_EN	Interrupt enable for the Parity Error interrupt. Reset State: 0x00000000
0	FRAME_ERR_INTR_EN	Interrupt enable for the Frame Error interrupt. Reset State: 0x00000000

0x3000008 BT_UART_CTRL

Type: read-write
Reset State: 0x03280060

BT_UART_CTRL

Bits	Name	Description
31:24	BAUD_RATE_NUMERATOR	Sets the numerator for the ratio of the system clock frequency to the baud rate. Reset State: 0x00000003
23:16	BAUD_RATE_DENOMINATOR	Sets the denominator for the ratio of the system clock frequency to the baud rate. Reset State: 0x00000028
6	TX_INV_EN	When set, enables the UART's serial TX output inverter. Reset State: 0x00000001
5	RX_INV_EN	When set, enables the UART's serial RX input inverter. Reset State: 0x00000001

BT_UART_CTRL (cont.)

Bits	Name	Description
4	POWER_DOWN	When set, puts the UART into power-down mode. The UART transmitter will complete its current transmission and then disable all further transmissions. The UART receiver will discard the current character being received and then ignore all further receptions. Reset State: 0x00000000
3	PARITY_EN	Enables parity bit generation in the UART transmitter, and parity checking in the UART receiver. Reset State: 0x00000000
2	PARITY_ODD	When parity is enabled, this bit specifies whether the parity is odd or even. When 1, the parity is odd; when 0, it is even. Reset State: 0x00000000
1:0	NUM_STOPS	Specifies the number of stop bits (1-4) at the end of each character. The number of stop bits per character = num_stops + 1. Reset State: 0x00000000

0x300000C BT_HW_CTRL

Type: command
Reset State: 0x00000014

BT_HW_CTRL

Bits	Name	Description
31:24	LAST_RX_HW_CHAR	This field captures the last received hardware character that was passed on to the Signaling layer. Reset State: 0x00000000
15	TX_BUFFER_STATE	State of the 1-character-deep Hardware TX Buffer. When 1, the buffer is full; when 0, the buffer is empty. Reset State: 0x00000000
14:8	TX_BUFFER_CONTENTS	This field captures the hardware character presently stored in the TX Buffer. Resend bit excluded as only non-Resend-Requests are stored in this buffer. Reset State: 0x00000000
7	RESEND_REQ_FLAG	Indicates the present state of the Resend Request flag. When set, it indicates that a Resend Request is pending transmission. Reset State: 0x00000000
4	EXCLUSIVE_RESEND_EN	Exclusive Resend Enable: When set, the QTA module will treat Signal State bits within Resend Request characters as invalid. When clear, the Signal State bits are valid regardless of whether the character is a Resend Request. Reset State: 0x00000001

BT_HW_CTRL (cont.)

Bits	Name	Description
3	RESEND_REQ_PASSTHRU_EN	Resend Request Pass-Through Enable: When set, the QTA module will pass received Resend Request characters through to the Signaling layer for processing. NB: This feature is unsupported for the WLAN version of the QTA module, because the Signaling interface for the WLAN version does not support Resend signaling. Reset State: 0x00000000
2	RESEND_RESP_EN	Resend Response Enable: When this bit is set, the QTA module will automatically respond to received Resend Requests by resending its last (non-Resend-Request) hardware character. Otherwise, the QTA module will not respond to Resend Requests received from the peer device. Reset State: 0x00000001
1	RETRANSMIT	Retransmit TX Buffer contents: Writing a 1 to this bit causes the last (non-Resend-Request) hardware character to be re-transmitted. This bit is self-clearing. Reset State: 0x00000000
0	RESEND_REQUEST	Send a Resend Request: Writing a 1 to this bit causes a Resend Request character to be queued for transmission. This bit is self-clearing. Reset State: 0x00000000

0x3000010 BT_HW_TX_BUFFER_MODIFY

Type: write-only
Reset State: 0x00000000

BT_HW_TX_BUFFER_MODIFY

Bits	Name	Description
6:0	DATA	Data to be written to the TX Buffer. Writing to this register causes the contents of the TX Buffer to be modified to the value of the data field, and causes the TX buffer state to be set to full. Reset State: 0x00000000

0x3000014 BT_SW_CTRL

Type: read-write
Reset State: 0x00000000

BT_SW_CTRL

Bits	Name	Description
29:24	RX_FILL	Indicates the number of software characters presently queued in the Receive FIFO. Reset State: 0x00000000
21	RX_FLUSH	Receive FIFO Flush: Writing a 1 to this bit flushes the contents of the Receive FIFO. This bit is self-clearing. Reset State: 0x00000000
20:16	RX_TRIG_LEVEL	Receive FIFO Trigger Level. See the rx_fifo_rdy_int interrupt status register description. Reset State: 0x00000000
13:8	TX_FILL	Indicates the number of software characters presently queued in the Transmit FIFO. Reset State: 0x00000000
5	TX_FLUSH	Transmit FIFO Flush: Writing a 1 to this bit flushes the contents of the Transmit FIFO. This bit is self-clearing. Reset State: 0x00000000
4:0	TX_TRIG_LEVEL	Transmit FIFO Trigger Level. See the tx_fifo_rdy_int interrupt status register description. Reset State: 0x00000000

0x3000018 BT_SW_TX_FIFO_IN

Type: write-only
Reset State: 0x00000000

BT_SW_TX_FIFO_IN

Bits	Name	Description
7:0	DATA	Software character to be transmitted. Reset State: 0x00000000

0x300001C BT_SW_RX_FIFO_OUT

Type: read-only
Reset State: 0x00000000

BT_SW_RX_FIFO_OUT

Bits	Name	Description
7:0	DATA	Software character received. Reset State: 0x00000000

0x3000020 BT_TESTBUS

Type: read-write
Reset State: 0x00000000

BT_TESTBUS

Bits	Name	Description
3:0	SEL	Select input for the test bus multiplexer. 0x0: QTA_TESTBUS_NONE 0x1: QTA_TESTBUS_UART_RX 0x2: QTA_TESTBUS_UART_TX 0x3: QTA_TESTBUS_SW_FIFOS 0x4: QTA_TESTBUS_SW_RX 0x5: QTA_TESTBUS_SW_TX 0x6: QTA_TESTBUS_HW_RX 0x7: QTA_TESTBUS_HW_TX 0x8: QTA_TESTBUS_CONV_RX 0x9: QTA_TESTBUS_CONV_TX 0xA: QTA_TESTBUS_RESERVED_10 0xB: QTA_TESTBUS_RESERVED_11 0xC: QTA_TESTBUS_RESERVED_12 0xD: QTA_TESTBUS_RESERVED_13 0xE: QTA_TESTBUS_RESERVED_14 0xF: QTA_TESTBUS_RESERVED_15 Reset State: 0x00000000

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0x300FFFC BT_SSBI2_PVC_FIFO

Type: write-only
Reset State: 0x00000000

BT_SSBI2_PVC_FIFO

Bits	Name	Description
12:8	PVC_INDEX	Reset State: 0xxxxxxxxx
7:0	PVC_DATA	Sub-Section 2.2.1: Crystal calibration Stop Parsing at Section 2.3: Link controller registers Start Parsing at Section 1.2: SSBI2 Configuration Micro ARM registers Reset State: 0xxxxxxxxx

0x3000000 BT_SSBI2_CTL

Type: read-write
Reset State: 0x00083005

BT_SSBI2_CTL

Bits	Name	Description
19:16	NUM_FCLK	Reset State: 0xxxxxxxxx
15	FCLK_SW_OVERRIDE	Reset State: 0xxxxxxxxx
14	FCLK_MODE	Reset State: 0xxxxxxxxx
13	SSBI2_DATA_PDEN	Reset State: 0xxxxxxxxx
12	PA_CGC_CTRL	Reset State: 0xxxxxxxxx
10:8	SSBI2_ADDR_WIDTH	0x0: 8_BIT_ADDRESSING_MODE 0x1: 9_BIT_ADDRESSING_MODE_AND_SO_ON Reset State: 0xxxxxxxxx
7	SSBI2_MODE	Reset State: 0xxxxxxxxx
5:4	SEL_RD_DATA	Reset State: 0xxxxxxxxx
3:2	SSBI2_DATA_DEL	Reset State: 0xxxxxxxxx
1:0	IDLE_SYMS	Reset State: 0xxxxxxxxx

0x3000004 BT_SSBI2_INT_ENABLE

Type: read-write
Reset State: 0x00000000

BT_SSBI2_INT_ENABLE

Bits	Name	Description
6:0	ENABLE_SSBI2_INT	Reset State: 0xxxxxxxxx

0x3000008 BT_SSBI2_PRIORITIES

Type: read-write
Reset State: 0x00000000

BT_SSBI2_PRIORITIES

Bits	Name	Description
11:9	PRIORITY3	Reset State: 0xxxxxxxxx
8:6	PRIORITY2	Reset State: 0xxxxxxxxx

BT_SSBI2_PRIORITIES (cont.)

Bits	Name	Description
5:3	PRIORITY1	Reset State: 0xxxxxxxxx
2:0	PRIORITY0	Reset State: 0xxxxxxxxx

0x300000C BT_SSBI2_BANKS_2_3_CTL

Type: read-write
Reset State: 0xffffffff

BT_SSBI2_BANKS_2_3_CTL

Bits	Name	Description
31:0	ACCESS_CONTROL	Reset State: 0xxxxxxxxx

0x3000010 BT_SSBI2_ILLEGAL_STATUS

Type: read-only
Reset State: 0x00000000

BT_SSBI2_ILLEGAL_STATUS

Bits	Name	Description
5:1	ILLEGAL_VMID	Reset State: 0xxxxxxxxx
0	ILLEGAL_ACCESS	Reset State: 0xxxxxxxxx

0x3000014 BT_SSBI2_TEST_BUS_CTL

Type: read-write
Reset State: 0x00000000

BT_SSBI2_TEST_BUS_CTL

Bits	Name	Description
0	TEST_BUS_EN	Reset State: 0xxxxxxxxx

0x3000020+4*SSBI2_VITn, n=[0..6] n

Type: read-write
Reset State: 0x00000000

SSBI2_VITn

Bits	Name	Description
4:0	VMID	Reset State: 0xxxxxxxxx

0x30000A0 BT_SSBI2_PVC_CTL

Type: read-write
Reset State: 0x00000000

BT_SSBI2_PVC_CTL

Bits	Name	Description
8	PVC_INTF_BUSY	Reset State: 0xxxxxxxxx
3	PVC_PORT3_EN	Reset State: 0xxxxxxxxx
2	PVC_PORT2_EN	Reset State: 0xxxxxxxxx
1	PVC_PORT1_EN	Reset State: 0xxxxxxxxx
0	PVC_INTF_EN	Reset State: 0xxxxxxxxx

0x30000A4+4*n SSBI2_PVC_TABLEn, n=[0..11]

Type: read-write
Reset State: 0x00000000

SSBI2_PVC_TABLEn

Bits	Name	Description
14:0	ADDR	Stop Parsing at Section 1.3: SSBI2 Command Micro ARM registers Reset State: 0xxxxxxxxx

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0x3000000 BT_SSBI2_CMD

Type: write-only
Reset State: 0x00000000

BT_SSBI2_CMD

Bits	Name	Description
24	RDWRN	Reset State: 0xxxxxxxxx

BT_SSBI2_CMD (cont.)

Bits	Name	Description
22:16	REG_ADDR_14_8	Reset State: 0xxxxxxxxx
15:8	REG_ADDR_7_0	Reset State: 0xxxxxxxxx
7:0	REG_DATA	Reset State: 0xxxxxxxxx

0x3000004 BT_SSBI2_RD_STATUS

Type: read-only
Reset State: 0x00000000

BT_SSBI2_RD_STATUS

Bits	Name	Description
27	TRANS_DONE	Reset State: 0xxxxxxxxx
26	TRANS_DENIED	Reset State: 0xxxxxxxxx
25	TRANS_PROG	Reset State: 0xxxxxxxxx
24	RDWRN	Reset State: 0xxxxxxxxx
22:8	REG_ADDR	Reset State: 0xxxxxxxxx
7:0	REG_DATA	Reset State: 0xxxxxxxxx

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0x3000000 FM_TX_CONTROL

Type: read-write
Reset State: 0x00000000

FM_TX_CONTROL

Bits	Name	Description
11:10	AUDIO_IN_SHIFT_CTRL	Reset State: 0xxxxxxxxx
9:5	PRE_EMPH_CONST	Reset State: 0xxxxxxxxx
4:3	DC_BLOCK	Reset State: 0xxxxxxxxx
2	PRE_EMPH_EN	0x1: ENABLE 0x0: DISABLE Reset State: 0xxxxxxxxx
1	STEREO	0x1: STEREO 0x0: MONO Reset State: 0xxxxxxxxx

FM_TX_CONTROL (cont.)

Bits	Name	Description
0	TX_EN	0x1: ENABLE 0x0: DISABLE Reset State: 0xxxxxxxxx

0x3000004 FM_TX_MODULATION

Type: read-write
Reset State: 0x00000000

FM_TX_MODULATION

Bits	Name	Description
31:24	MOD_RDS	Reset State: 0xxxxxxxxx
23:16	MOD_PILOT	Reset State: 0xxxxxxxxx
15:8	MOD_STEREO	Reset State: 0xxxxxxxxx
7:0	MOD_MONO	Reset State: 0xxxxxxxxx

0x3000008 FM_TX_AUDIO_LIMIT

Type: read-write
Reset State: 0x00000000

FM_TX_AUDIO_LIMIT

Bits	Name	Description
27:14	AUDIO_LIMIT_2	Reset State: 0xxxxxxxxx
13:0	AUDIO_LIMIT_1	Reset State: 0xxxxxxxxx

0x300000C FM_TX_RDS_CONTROL

Type: read-write
Reset State: 0x00000000

FM_TX_RDS_CONTROL

Bits	Name	Description
1	INV_RDS_SYMBOL	0x1: INVERT 0x0: NORMAL Reset State: 0xxxxxxxxx

FM_TX_RDS_CONTROL (cont.)

Bits	Name	Description
0	RDS_EN	0x1: ENABLE 0x0: DISABLE Reset State: 0xxxxxxxxx

0x3000010 FM_TX_RDS_BLK_DATA_A_B

Type: read-write
Reset State: 0x00000000

FM_TX_RDS_BLK_DATA_A_B

Bits	Name	Description
31:16	RDS_BLK_DATA_A	Reset State: 0xxxxxxxxx
15:0	RDS_BLK_DATA_B	Reset State: 0xxxxxxxxx

0x3000014 FM_TX_RDS_BLK_DATA_C_D

Type: read-write
Reset State: 0x00000000

FM_TX_RDS_BLK_DATA_C_D

Bits	Name	Description
31:16	RDS_BLK_DATA_C	Reset State: 0xxxxxxxxx
15:0	RDS_BLK_DATA_D	Reset State: 0xxxxxxxxx

0x3000018 FM_TX_SOFT_RESET

Type: read-write
Reset State: 0x00000000

FM_TX_SOFT_RESET

Bits	Name	Description
0	SOFT_RESET	0x0: OPERATION 0x1: RESET Reset State: 0xxxxxxxxx

0x300001C FM_TX_TMUX_SEL

Type: read-write
Reset State: 0x00000000

FM_TX_TMUX_SEL

Bits	Name	Description
4:0	TMUX_CNTL	Reset State: 0xxxxxxxxx

0x3010000 FM_RX_CONTROL

Type: read-write
Reset State: 0x00000000

FM_RX_CONTROL

Bits	Name	Description
0	RX_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx

0x3010004 FM_RX_SOFT_RESET

Type: read-write
Reset State: 0x00000000

FM_RX_SOFT_RESET

Bits	Name	Description
0	SOFT_RESET	0x0: OPERATION 0x1: RESET Reset State: 0xxxxxxxxx

0x3010024 FM_RX_TMUX_SEL

Type: read-write
Reset State: 0x00000000

FM_RX_TMUX_SEL

Bits	Name	Description
11:6	TMUX_CNTL_1	Reset State: 0xxxxxxxxx
5:0	TMUX_CNTL_0	Reset State: 0xxxxxxxxx

0x3010028 FM_RX_DEMOD_GLITCH_THRESHOLD

Type: read-write
Reset State: 0x00000000

FM_RX_DEMOD_GLITCH_THRESHOLD

Bits	Name	Description
14:0	DEMOD_GLITCH_THRESHOLD	Reset State: 0xxxxxxxxx

0x301002C FM_RX_GLITCH_STOP_SRCH_CNT

Type: read-write
Reset State: 0x00000000

FM_RX_GLITCH_STOP_SRCH_CNT

Bits	Name	Description
6:0	STOP_SRCH_CNT	Reset State: 0xxxxxxxxx

0x3010030 FM_RX_GLITCH_START_SRCH_CNT

Type: read-write
Reset State: 0x00000000

FM_RX_GLITCH_START_SRCH_CNT

Bits	Name	Description
6:0	GLITCH_START_SRCH_CNT	Reset State: 0xxxxxxxxx

0x3010034 FM_RX_GLITCH_BLANK_CNT_TH

Type: read-write
Reset State: 0x00000000

FM_RX_GLITCH_BLANK_CNT_TH

Bits	Name	Description
3:0	BLANK_CNT_TH	Reset State: 0xxxxxxxxx

0x3010038 FM_RX_PLL_BANK_CHG_STB

Type: read-write
Reset State: 0x00000000

FM_RX_PLL_BANK_CHG_STB

Bits	Name	Description
0	PLL_BANK_CHG_STB	0x0: NOT_START 0x1: START Reset State: 0xxxxxxxxx

0x301003C FM_RX_PHASE_COMP_BYPASS

Type: read-write
Reset State: 0x00000000

FM_RX_PHASE_COMP_BYPASS

Bits	Name	Description
0	PHASE_COMP_BYPASS	0x0: ENABLE 0x1: BYPASS Reset State: 0xxxxxxxxx

0x3010040 FM_RX_MPX_DCC_CTRL

Type: read-write
Reset State: 0x00000000

FM_RX_MPX_DCC_CTRL

Bits	Name	Description
2:1	MPX_DCC_SEL	Reset State: 0xxxxxxxxx
0	MPX_DCC_BYPASS	0x0: ENABLE 0x1: BYPASS Reset State: 0xxxxxxxxx

0x3010044 FM_RX_MPX_DCC_Z_DELAY_REGISTER

Type: read-write
Reset State: 0x00000000

FM_RX_MPX_DCC_Z_DELAY_REGISTER

Bits	Name	Description
19:0	MPX_DCC_Z_M1	Reset State: 0xxxxxxxxx

0x3010048 FM_RX_PILOT_DET_THRESHOLD

Type: read-write
Reset State: 0x00000000

FM_RX_PILOT_DET_THRESHOLD

Bits	Name	Description
19:10	PDET_LO_THRESHOLD	Reset State: 0xxxxxxxxx
9:0	PDET_HI_THRESHOLD	Reset State: 0xxxxxxxxx

0x301004C FM_RX_DELTA_R57K_PHASE_ADJUST

Type: read-write
Reset State: 0x00000000

FM_RX_DELTA_R57K_PHASE_ADJUST

Bits	Name	Description
12:0	DELTA_IDX3	Reset State: 0xxxxxxxxx

0x3010050 FM_RX_BLEND_WEIGHT

Type: read-write
Reset State: 0x00000000

FM_RX_BLEND_WEIGHT

Bits	Name	Description
9:0	BLEND_WEIGHT	Reset State: 0xxxxxxxxx

0x3010054 FM_RX_SOFTMUTE_WEIGHT

Type: read-write
Reset State: 0x00000000

FM_RX_SOFTMUTE_WEIGHT

Bits	Name	Description
8:0	SOFTMUTE_WEIGHT	Reset State: 0xxxxxxxxx

0x3010058 FM_RX_BLEND_SOFTMUTE_LPF_M_SEL

Type: read-write
Reset State: 0x00000000

FM_RX_BLEND_SOFTMUTE_LPF_M_SEL

Bits	Name	Description
31:6	RESERVED_0	Reset State: 0xxxxxxxxx
5:4	SF_WGHT_M	Reset State: 0xxxxxxxxx
3:2	RESERVED_1	Reset State: 0xxxxxxxxx
1:0	BLEND_WGHT_M	Reset State: 0xxxxxxxxx

0x301005C FM_RX_MS_DECODER_CNTL

Type: read-write
Reset State: 0x00000000

FM_RX_MS_DECODER_CNTL

Bits	Name	Description
31:6	RESERVED_0	Reset State: 0xxxxxxxxx
5	R_HARD_MUTE	0x0: NO_MUTE Reset State: 0xxxxxxxxx
4	L_HARD_MUTE	0x0: NO_MUTE 0x1: MUTE Reset State: 0xxxxxxxxx
3:2	RESERVED_1	Reset State: 0xxxxxxxxx
1	DE_EMPS_TC	0x0: TC_50US 0x1: TC_75US Reset State: 0xxxxxxxxx
0	MONO_DEC	0x0: NORMAL 0x1: FORCE_MONO Reset State: 0xxxxxxxxx

0x3010060 FM_RX_MS_DECODER_STEREO_ON

Type: read-only
Reset State: 0x00000000

FM_RX_MS_DECODER_STEREO_ON

Bits	Name	Description
0	STEREO_ON	Reset State: 0xxxxxxxxx

0x3010064 FM_RX_RDS_CTRL

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_CTRL

Bits	Name	Description
2	RDS_SOFT_RESET	0x0: OPERATION 0x1: RESET Reset State: 0xxxxxxxxx
1	IQ_AN_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
0	RDS_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx

0x3010068 FM_RX_RDS_IQ_DET_CTRL

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_IQ_DET_CTRL

Bits	Name	Description
21:4	IQ_DET_THRESH	Reset State: 0xxxxxxxxx
3:0	IQ_INT_DUR	Reset State: 0xxxxxxxxx

0x301006C FM_RX_RDS_ACQ_MODE

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_ACQ_MODE

Bits	Name	Description
1:0	ACQ_MODE	Reset State: 0xxxxxxxxx

0x3010070 FM_RX_RDS_TRK_MODE

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_TRK_MODE

Bits	Name	Description
1:0	TRK_MODE	Reset State: 0xxxxxxxxx

0x3010074 FM_RX_RDS_STROBE_MARGIN

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_STROBE_MARGIN

Bits	Name	Description
1:0	STROBE_MARGIN	Reset State: 0xxxxxxxxx

0x3010078 FM_RX_RDS_MF_LPF_CNT

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_MF_LPF_CNT

Bits	Name	Description
7:4	MF_CNT	Reset State: 0xxxxxxxxx
3:0	LPF_CNT	Reset State: 0xxxxxxxxx

0x301007C FM_RX_RDS_IQ_AN_INT_DUR_SEL

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_IQ_AN_INT_DUR_SEL

Bits	Name	Description
2:0	IQ_AN_INT_DUR_SEL	Reset State: 0xxxxxxxxx

0x3010080 FM_RX_RDS_IQ_ANALYZER_SELECT

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_IQ_ANALYZER_SELECT

Bits	Name	Description
31:2	RESERVED_1	Reset State: 0xxxxxxxxx
1	IQ_ANA_SIG_DET_SEL	0x0: SELECT_SIG_DET_FROM_IQ_DETECTOR 0x1: SELECT_SIG_DET_FROM_IQ_ANALYZER Reset State: 0xxxxxxxxx

0x3010084 FM_RX_RDS_IQ_AN_DET_THRESH

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_IQ_AN_DET_THRESH

Bits	Name	Description
13:0	IQ_AN_DET_THRESH	Reset State: 0xxxxxxxxx

0x3010088 FM_RX_RDS_RECEIVE_MODE_SELECT

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_RECEIVE_MODE_SELECT

Bits	Name	Description
0	RDS_MODE_SELECT	0x0: COHERENT 0x1: NON_COHERENT Reset State: 0xxxxxxxxx

0x301008C FM_RX_RDS_STATUS

Type: read-only
Reset State: 0x00000000

FM_RX_RDS_STATUS

Bits	Name	Description
2	IQ_AN_SIG_DET	0x0: NOT_DETECTED 0x1: DETECTED Reset State: 0xxxxxxxxx
1	IQ_AN_SELECT	0x0: I_ARM 0x1: Q_ARM Reset State: 0xxxxxxxxx
0	IQ_DET_SELECT	0x0: I_ARM 0x1: Q_ARM Reset State: 0xxxxxxxxx

0x3010090 FM_RX_RDS_IQ_BUFFER

Type: read-only
Reset State: 0x00000000

FM_RX_RDS_IQ_BUFFER

Bits	Name	Description
27:14	RX_RDS_Q_BUFFER	Reset State: 0xxxxxxxxx
13:0	RX_RDS_I_BUFFER	Reset State: 0xxxxxxxxx

0x3010094 FM_RX_RDS_TIME_TRACKING_THRESHOLD

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_TIME_TRACKING_THRESHOLD

Bits	Name	Description
9:5	DROP_THRESHOLD	Reset State: 0xxxxxxxxx
4:0	REPEAT_THRESHOLD	Reset State: 0xxxxxxxxx

0x3010098 FM_RX_RDS_PEAK_INDEX

Type: read-only
Reset State: 0x00000000

FM_RX_RDS_PEAK_INDEX

Bits	Name	Description
15:0	RDS_PEAK_INDEX	Reset State: 0xxxxxxxxx

0x301009C FM_RX_RDS_DL_CONFIG

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_DL_CONFIG

Bits	Name	Description
2	C_CP_ADAPT	0x0: NO_ADAPT 0x1: ADAPT Reset State: 0xxxxxxxxx
1	C_CP_TYPE	0x0: A_TYPE 0x1: B_TYPE Reset State: 0xxxxxxxxx
0	SYSTEM_TYPE	0x0: RBDS 0x1: RDS Reset State: 0xxxxxxxxx

0x30100A0 FM_RX_RDS_T1Q1E

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_T1Q1E

Bits	Name	Description
3:0	T1Q1E	Reset State: 0xxxxxxxxx

0x30100A4 FM_RX_RDS_T1Q2E

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_T1Q2E

Bits	Name	Description
3:0	T1Q2E	Reset State: 0xxxxxxxxx

0x30100A8 FM_RX_RDS_BLOCK_DATA_0_1

Type: read-only
Reset State: 0x00000000

FM_RX_RDS_BLOCK_DATA_0_1

Bits	Name	Description
31:16	RDS_BLOCK_DATA_0	Reset State: 0xxxxxxxxx
15:0	RDS_BLOCK_DATA_1	Reset State: 0xxxxxxxxx

0x30100AC FM_RX_RDS_BLOCK_DATA_2_3

Type: read-only
Reset State: 0x00000000

FM_RX_RDS_BLOCK_DATA_2_3

Bits	Name	Description
31:16	RDS_BLOCK_DATA_2	Reset State: 0xxxxxxxxx
15:0	RDS_BLOCK_DATA_3	Reset State: 0xxxxxxxxx

0x30100B0 FM_RX_RDS_BLOCK_STATUS

Type: read-only
Reset State: 0x00000000

FM_RX_RDS_BLOCK_STATUS

Bits	Name	Description
31	RESERVED_0	Reset State: 0xxxxxxxxx
30:24	RDS_BLOCK_STATUS_0	Reset State: 0xxxxxxxxx
23	RESERVED_1	Reset State: 0xxxxxxxxx
22:16	RDS_BLOCK_STATUS_1	Reset State: 0xxxxxxxxx
15	RESERVED_2	Reset State: 0xxxxxxxxx
14:8	RDS_BLOCK_STATUS_2	Reset State: 0xxxxxxxxx

FM_RX_RDS_BLOCK_STATUS (cont.)

Bits	Name	Description
7	RESERVED_3	Reset State: 0xxxxxxxxx
6:0	RDS_BLOCK_STATUS_3	Reset State: 0xxxxxxxxx

0x30100B4 FM_RX_RDS_BLOCK_DATA_RAW_0

Type: read-only
Reset State: 0x00000000

FM_RX_RDS_BLOCK_DATA_RAW_0

Bits	Name	Description
25:16	RDS_BLOCK_OFFSET_0	Reset State: 0xxxxxxxxx
15:0	RDS_BLOCK_DATA_RAW_0	Reset State: 0xxxxxxxxx

0x30100B8 FM_RX_RDS_BLOCK_DATA_RAW_1

Type: read-only
Reset State: 0x00000000

FM_RX_RDS_BLOCK_DATA_RAW_1

Bits	Name	Description
25:16	RDS_BLOCK_OFFSET_1	Reset State: 0xxxxxxxxx
15:0	RDS_BLOCK_DATA_RAW_1	Reset State: 0xxxxxxxxx

0x30100BC FM_RX_RDS_BLOCK_DATA_RAW_2

Type: read-only
Reset State: 0x00000000

FM_RX_RDS_BLOCK_DATA_RAW_2

Bits	Name	Description
25:16	RDS_BLOCK_OFFSET_2	Reset State: 0xxxxxxxxx
15:0	RDS_BLOCK_DATA_RAW_2	Reset State: 0xxxxxxxxx

0x30100C0 FM_RX_RDS_BLOCK_DATA_RAW_3

Type: read-only
Reset State: 0x00000000

FM_RX_RDS_BLOCK_DATA_RAW_3

Bits	Name	Description
25:16	RDS_BLOCK_OFFSET_3	Reset State: 0xxxxxxxxx
15:0	RDS_BLOCK_DATA_RAW_3	Reset State: 0xxxxxxxxx

0x30100C4 FM_RX_RDS_TMUX_SEL

Type: read-write
Reset State: 0x00000000

FM_RX_RDS_TMUX_SEL

Bits	Name	Description
18:0	RDS_DBG_BIT_SEL	Reset State: 0xxxxxxxxx

0x30100C8 FM_RX_BLENDING_READBACK

Type: read-only
Reset State: 0x00000000

FM_RX_BLENDING_READBACK

Bits	Name	Description
9:0	BLEND_WEIGHT_RB	Reset State: 0xxxxxxxxx

0x30100CC FM_RX_MUTE_READBACK

Type: read-only
Reset State: 0x00000000

FM_RX_MUTE_READBACK

Bits	Name	Description
8:0	SOFT_MUTE_WEIGHT_RB	Reset State: 0xxxxxxxxx

0x30100D0 FM_RX_PLL_FREERUN_EN

Type: read-write
Reset State: 0x00000000

FM_RX_PLL_FREERUN_EN

Bits	Name	Description
0	FREE_RUN_ENABLE	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx

0x30100D4 FM_RX_ROT_CTRL

Type: read-write
Reset State: 0x00000000

FM_RX_ROT_CTRL

Bits	Name	Description
15	BYPASS_IN_G1G2G3	0x0: NORMAL 0x1: BYPASS_IN_G1G2G3 Reset State: 0xxxxxxxxx
14:7	ROT_FREQ	Reset State: 0xxxxxxxxx
6	FORCE_DC_TRACK	0x0: USE_DC 0x1: USE_SPUR Reset State: 0xxxxxxxxx
5	SPUR_DC_DELAY	0x0: DELAY_2048 0x1: DELAY_4096 Reset State: 0xxxxxxxxx
4	SPUR_1K_ROT_ENABLE	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
3:2	SPUR_DC_IIR_RND	Reset State: 0xxxxxxxxx
1:0	SPUR_INT_SETTING	Reset State: 0xxxxxxxxx

0x30100D8 FM_SPUR_COMP_FIXED_VALUE

Type: read-write
Reset State: 0x00000000

FM_SPUR_COMP_FIXED_VALUE

Bits	Name	Description
31:16	SPUR_COMP_Q	Reset State: 0xxxxxxxxx
15:0	SPUR_COMP_I	Reset State: 0xxxxxxxxx

0x30100E0 FM_DEMOD_DC_IF_OFFSET

Type: read-write
Reset State: 0x00000000

FM_DEMOD_DC_IF_OFFSET

Bits	Name	Description
15:0	DEMOD_DC_IF_OFFSET	Reset State: 0xxxxxxxxx

0x3020000 FM_GAS_GAM_CTRL

Type: read-write
Reset State: 0x00000000

FM_GAS_GAM_CTRL

Bits	Name	Description
25	DISABLE_GAM_CLK_GATE	0x0: ENABLE 0x1: DISABLE Reset State: 0xxxxxxxxx
24	DISABLE_GAS_CLK_GATE	0x0: ENABLE 0x1: DISABLE Reset State: 0xxxxxxxxx
23:20	GAM_CFG_BUSY_LIMIT	Reset State: 0xxxxxxxxx
19:12	CFG_HSPLIT_RESP_LIMIT	Reset State: 0xxxxxxxxx
11:4	CFG_SPLIT_MST_RESP_LIMIT	Reset State: 0xxxxxxxxx
3:0	CFG_HREADY_LIMIT	Reset State: 0xxxxxxxxx

0x3020004 FM_FM_INTR_EVENT

Type: read-only
Reset State: 0x00000000

FM_FM_INTR_EVENT

Bits	Name	Description
18	SSBI_INTR	Reset State: 0xxxxxxxxx
17	AHB_ACESS_ERROR	Reset State: 0xxxxxxxxx
16	UNDER_FLOW	Reset State: 0xxxxxxxxx
15	OVER_FLOW	Reset State: 0xxxxxxxxx
14	AUDIO_SAMPLES_RDY	Reset State: 0xxxxxxxxx
13	TX_RDS_INTR	Reset State: 0xxxxxxxxx
12	PILOT_DET_DEASSERT_INTR	Reset State: 0xxxxxxxxx
11	PILOT_DET_INTR	Reset State: 0xxxxxxxxx
10	IQ_AN_SEGMENT_DONE_INTR	Reset State: 0xxxxxxxxx
9	C_CP_CHANGE_INTR	Reset State: 0xxxxxxxxx
8	RDS_SYNCH_LOSS_INTR	Reset State: 0xxxxxxxxx
7	RDS_NOT_SYNCH_INTR	Reset State: 0xxxxxxxxx
6	RDS_SYNCH_INTR	Reset State: 0xxxxxxxxx
5	SIG_NOT_DET_INTR	Reset State: 0xxxxxxxxx
4	SIG_DET_INTR	Reset State: 0xxxxxxxxx
3	RDS_BLOCK_3_INTR	Reset State: 0xxxxxxxxx
2	RDS_BLOCK_2_INTR	Reset State: 0xxxxxxxxx
1	RDS_BLOCK_1_INTR	Reset State: 0xxxxxxxxx
0	RDS_BLOCK_0_INTR	Reset State: 0xxxxxxxxx

0x3020008 FM_FM_INTR_ENABLE

Type: read-write
Reset State: 0x00000000

FM_FM_INTR_ENABLE

Bits	Name	Description
18	SSBI_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
17	AHB_ACESS_ERROR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx

FM_FM_INTR_ENABLE (cont.)

Bits	Name	Description
16	UNDER_FLOW_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
15	OVER_FLOW_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
14	AUDIO_SAMPLES_RDY_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
13	TX_RDS_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
12	PILOT_DET_DEASSERT_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
11	PILOT_DET_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
10	IQ_AN_SEGMENT_DONE_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
9	C_CP_CHANGE_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
8	RDS_SYNCH_LOSS_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
7	RDS_NOT_SYNCH_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
6	RDS_SYNCH_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
5	SIG_NOT_DET_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
4	SIG_DET_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx

FM_FM_INTR_ENABLE (cont.)

Bits	Name	Description
3	RDS_BLOCK_3_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
2	RDS_BLOCK_2_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
1	RDS_BLOCK_1_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx
0	RDS_BLOCK_0_INTR_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx

0x302000C FM_FM_BUFFER_START_ADDRESS

Type: read-write
Reset State: 0x00000000

FM_FM_BUFFER_START_ADDRESS

Bits	Name	Description
31:2	BUFFER_START	Reset State: 0xxxxxxxxx

0x3020010 FM_FM_BUFFER_LENGTH

Type: read-write
Reset State: 0x00000000

FM_FM_BUFFER_LENGTH

Bits	Name	Description
14:0	BUFFER_LENGTH	Reset State: 0xxxxxxxxx

0x3020014 FM_FM_BUFFER_HEAD

Type: read-write
Reset State: 0x00000000

FM_FM_BUFFER_HEAD

Bits	Name	Description
14:0	BUFFER_HEAD	Reset State: 0xxxxxxxxx

0x3020018 FM_FM_BUFFER_TAIL

Type: read-write
Reset State: 0x00000000

FM_FM_BUFFER_TAIL

Bits	Name	Description
14:0	BUFFER_TAIL	Reset State: 0xxxxxxxxx

0x302001C FM_AUDIO_INTR_CONTROL

Type: read-write
Reset State: 0x00000000

FM_AUDIO_INTR_CONTROL

Bits	Name	Description
18	PULSE_LEVEL_SEL	0x0: LEVEL 0x1: PULSE Reset State: 0xxxxxxxxx
17	CLR_AUDIO_SAMPLE_COUNTER	0x0: RUNNING 0x1: REST Reset State: 0xxxxxxxxx
16:15	RESERVED_0	Reset State: 0xxxxxxxxx
14:0	AUDIO_INTR_INTERVAL	Reset State: 0xxxxxxxxx

0x3020020 FM_CLR_AUDIO_LEVEL_INTR

Type: read-only
Reset State: 0x00000000

FM_CLR_AUDIO_LEVEL_INTR

Bits	Name	Description
0	CLR_AUDIO_INTR	Reset State: 0xxxxxxxxx

0x3020024 FM_AUDIO_SAMPLES_COUNTER_VFR_SNAP_READBACK

Type: read-only
Reset State: 0x00000000

FM_AUDIO_SAMPLES_COUNTER_VFR_SNAP_READBACK

Bits	Name	Description
31:0	AUDIO_SAMPLES_VFR_COUNT	Reset State: 0xxxxxxxxx

0x3020028 FM_AUDIO_SAMPLES_COUNTER_READBACK

Type: read-only
Reset State: 0x00000000

FM_AUDIO_SAMPLES_COUNTER_READBACK

Bits	Name	Description
31:0	AUDIO_SAMPLES_COUNT	Reset State: 0xxxxxxxxx

0x302002C FM_SW_RESET

Type: read-write
Reset State: 0x00000000

FM_SW_RESET

Bits	Name	Description
2	SLV_SW_RESET	0x0: NORMAL 0x1: RESET Reset State: 0xxxxxxxxx
1	MSTR_SW_RESET	0x0: NORMAL 0x1: RESET Reset State: 0xxxxxxxxx
0	SDI_SW_RESET	0x0: NORMAL 0x1: RESET Reset State: 0xxxxxxxxx

0x3020030 FM_RIVA_TEST_MUX

Type: read-write
Reset State: 0x00000000

FM_RIVA_TEST_MUX

Bits	Name	Description
11:8	SLAVE_DBG_MUX_SEL	Reset State: 0xxxxxxxxx
7:4	MASTR_DBG_MUX_SEL	Reset State: 0xxxxxxxxx
2:0	BLK_DEBUG_MUX_SEL	0x0: NOT_ENABLED 0x1: RX 0x2: TX 0x3: MASTER 0x4: SLAVE 0x5: SDI Reset State: 0xxxxxxxxx

0x3020034 FM_SDI_CTRL

Type: read-write
Reset State: 0x00000000

FM_SDI_CTRL

Bits	Name	Description
0	SDI_EN	0x0: DISABLE 0x1: ENABLE Reset State: 0xxxxxxxxx

0x3020038 FM_SCRAMBLER_CTRL

Type: read-write
Reset State: 0x00000000

FM_SCRAMBLER_CTRL

Bits	Name	Description
2	SCRM_TYPE	0x0: ADDITIVE 0x1: MULTIPLICATIVE Reset State: 0xxxxxxxxx
1	SCRM_DESCRM_SEL	0x0: SCRAMBLER_ENABLED 0x1: DE_SCRAMBLER_ENABLED Reset State: 0xxxxxxxxx
0	SCRM_EN	0x1: RUNNING 0x0: BYPASS Reset State: 0xxxxxxxxx

0x302003C FM_SCRAMBLER_POLY

Type: read-write
Reset State: 0x00000000

FM_SCRAMBLER_POLY

Bits	Name	Description
16:0	SCRM_POLY	Reset State: 0xxxxxxxxx

0x3020040 FM_FM_INTR_CTRL

Type: read-write
Reset State: 0x00000000

FM_FM_INTR_CTRL

Bits	Name	Description
0	FM_INTR_PULSE_LVL_SEL	0x0: PULSE 0x1: LEVEL Reset State: 0xxxxxxxxx

0x3020044 FM_AUDIO_DATA_CONTROL

Type: read-write
Reset State: 0x00000000

FM_AUDIO_DATA_CONTROL

Bits	Name	Description
1	SWAP_AUDIO_BYTES	0x0: NORMAL 0x1: SWAP Reset State: 0xxxxxxxxx
0	SWAP_AUDIO	0x0: NORMAL 0x1: SWAP Reset State: 0xxxxxxxxx

0x3020048 FM_FM_HW_VERSION

Type: read-only
Reset State: 0x10010000

FM_FM_HW_VERSION

Bits	Name	Description
31:28	MAJOR	Reset State: 0xxxxxxxxx
27:16	MINOR	Reset State: 0xxxxxxxxx
15:0	STEP	Reset State: 0xxxxxxxxx

0x3040000 FM_SSBI2_CMD

Type: write-only
Reset State: 0x00000000

FM_SSBI2_CMD

Bits	Name	Description
24	RDWRN	Reset State: 0xxxxxxxxx
22:16	REG_ADDR_14_8	Reset State: 0xxxxxxxxx
15:8	REG_ADDR_7_0	Reset State: 0xxxxxxxxx
7:0	REG_DATA	Reset State: 0xxxxxxxxx

0x3040004 FM_SSBI2_RD_STATUS

Type: read-only
Reset State: 0x00000000

FM_SSBI2_RD_STATUS

Bits	Name	Description
27	TRANS_DONE	Reset State: 0xxxxxxxxx
26	TRANS_DENIED	Reset State: 0xxxxxxxxx
25	TRANS_PROG	Reset State: 0xxxxxxxxx
24	RDWRN	Reset State: 0xxxxxxxxx
22:8	REG_ADDR	Reset State: 0xxxxxxxxx
7:0	REG_DATA	Reset State: 0xxxxxxxxx

0x3060000 FM_SSBI2_CTL

Type: read-write
Reset State: 0x00083005

FM_SSBI2_CTL

Bits	Name	Description
19:16	NUM_FCLK	Reset State: 0xxxxxxxxx
15	FCLK_SW_OVERRIDE	Reset State: 0xxxxxxxxx
14	FCLK_MODE	Reset State: 0xxxxxxxxx
13	SSBI2_DATA_PDEN	Reset State: 0xxxxxxxxx
12	PA_CGC_CTRL	Reset State: 0xxxxxxxxx
11	RESERVED_0	Reset State: 0xxxxxxxxx
10:8	SSBI2_ADDR_WIDTH	0x0: 8_BIT_ADDRESSING_MODE 0x1: 9_BIT_ADDRESSING_MODE_AND_SO_ON Reset State: 0xxxxxxxxx
7	SSBI2_MODE	Reset State: 0xxxxxxxxx
6	RESERVED_1	Reset State: 0xxxxxxxxx
5:4	SEL_RD_DATA	Reset State: 0xxxxxxxxx
3:2	SSBI2_DATA_DEL	Reset State: 0xxxxxxxxx
1:0	IDLE_SYMS	Reset State: 0xxxxxxxxx

0x3060004 FM_SSBI2_INT_ENABLE

Type: read-write
Reset State: 0x00000000

FM_SSBI2_INT_ENABLE

Bits	Name	Description
0	ENABLE_SSBI2_INT	Reset State: 0xxxxxxxxx

0x3060014 FM_SSBI2_TEST_BUS_CTL

Type: read-write
Reset State: 0x00000000

FM_SSBI2_TEST_BUS_CTL

Bits	Name	Description
0	TEST_BUS_EN	Reset State: 0xxxxxxxxx

16.2.56 riva_apu

0x3000000+4*RIVA_APU_RGn_RACR, n=[0..0]
n

Type: read-write
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type APU. These registers include a single bit per VMID granting read access.

RIVA_APU_RGn_RACR

Bits	Name	Description
31:0	RE	Read enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read access to the registers in the associated resource group.

0x3000400+4*RIVA_APU_RGn_WACR, n=[0..0]
n

Type: read-write
Reset State: 0x00000000

These registers exist only for the case when APU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs.read-only access permission type APU.

RIVA_APU_RGn_WACR

Bits	Name	Description
31:0	WE	Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID write access to the registers in the associated resource group.

0x3000F80 RIVA_APU_CR

Type: read-write
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

RIVA_APU_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved

RIVA_APU_CR (cont.)

Bits	Name	Description
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresse) are recorded as such. 0xDCDEE: V_0_DO_NOT_RECORD_DECODE_ERRORS_DO_NOT_SET_APU_ESR_APU_EAR_AND_APU_ESYNR0_NOT_UPDATED 0xDCDEE: V_1_RECORD_DECODE_ERRORS_SET_APU_ESR_APU_EAR_AND_APU_ESYNR0_UPDATED_WITH_ADDRESS_AND_SYNDROME_OF_ERROR
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x3000F84 RIVA_APU_EAR

Type: read-write
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port.

RIVA_APU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x3000F88 RIVA_APU_ESR

Type: read-write
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port. This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the APU_ESYNRn registers, which are merely the "syndrome" of an error indicated by APU_ESR.

RIVA_APU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x3000F8C RIVA_APU_ESRRESTORE

Type: read-write
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

RIVA_APU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.

RIVA_APU_ESRRESTORE (cont.)

Bits	Name	Description
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x3000F90 RIVA_APU_ESYNR0

Type: read-write
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

RIVA_APU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x3000F94 RIVA_APU_ESYNR1

Type: read-write
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

RIVA_APU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.

RIVA_APU_ESYNR1 (cont.)

Bits	Name	Description
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x3000FF4 RIVA_APU_REV

Type: read-only
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

RIVA_APU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x3000FF8 RIVA_APU_IDR

Type: read-only
Reset State: 0x00001C05

APU ID Register: Read-only register that defines various configuration attributes of the APU instance.

RIVA_APU_IDR

Bits	Name	Description
31:29	RESERVED31_21	Reserved
28:24	MSB	Indicates most significant address bit number used to select a resource group
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: RESERVED
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.
9	RESERVED9	Reserved
8:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

0x3000FFC RIVA_APU_ACR

Type: read-write
Reset State: 0xFFFFFFFF

APU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the APU (including the APU_APU_ACR itself).

RIVA_APU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the APU's 4KB address region (including the APU_APU_ACR itself). For single VMID type APUs (APU_IDR[MV] = 0) the APU_APU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

16.2.57 riva_m2vmt

0x3000000+0x4*n RIVA_M2VMT_M2VMRn, n=[0..1]

Type: read-write
Reset State: 0xxxxxxxxx

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID. Where n = NUM_M2VMT_ENTRIES from the design generics and we map NUM_M2VMT_ENTRIES to NUM_MASTERS.

RIVA_M2VMT_M2VMRn

Bits	Name	Description
31:5	RESERVED	
4:0	VMID	Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRn address associations. n = NUM_M2VMT_ENTRIES from the design generic/parameter.

0x3000F80 RIVA_M2VMT_CR

Type: read-write
Reset State: 0xxxxxxxxx

Global configuration register.

Note: When REMOVE_M2VMT_RPU = ‘1’, this register is not available. Also, bit [2], is not valid or has no effect when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT =‘1’.

RIVA_M2VMT_CR

Bits	Name	Description
31:4	RESERVED	
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., in valid addresses) are recorded as such. Decode error is asserted when config access to un-implemented and/or unmapped register/address are done. Also, note that decode error is never asserted for client port accesses. When value is set to '0' i.e., "do not record", decode errors do not set the M2VMT_ESR[CFG], and M2VMT_EAR & M2VMT_SYNRn is not updated. When value is set to '1', i.e., "record", decode errors set M2VMT_ESR[CFG] and M2VMT_EAR & M2VMT_SYNRn is updated with the address and the syndrome of the error. Reset State: 0xxxxxxxxx
2	RPUEIE	RPU error interrupt Enable: When set, configuration port errors are reported directly to the interrupt controller via the M2VMT_intr, interrupt output signal. Interrupt output is asserted if M2VMT_CR[RPUIE_EN] is '1' and ANY bit is set in the M2VMT_ESR register. Special Note: Not valid or has no effect on the interrupt when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT='1'. Reset State: 0xxxxxxxxx
1	RPUERE	RPU error report enable: When set, M2VMT reports configuration port errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via CRIF port will use a decode error, rather than a slave error. Regardless of the value of this field, both configuration port errors are terminated by the M2VMT as RAZ/WI, and are recorded in M2VMT_ESR register. Reset State: 0xxxxxxxxx
0	RPUE	RPU Enable: Governs whether M2VMT_RPU_ACR is enabled to check the VMID of the configuration request. When set, all configuration port accesses are checked against M2VMT_RPU_ACR register for access permissions. It's cleared by reset. Set once SROT configures MID->VMID mapping tables Reset State: 0x00000000

0x3000F84 RIVA_M2VMT_EAR

Type: read-only
Reset State: 0xxxxxxxxx

When there is an error, this register holds the physical address of the errant transaction.

RIVA_M2VMT_EAR

Bits	Name	Description
31:0	PA	M2VMT Error Address Register: Physical address[31:0]. Contains the physical address of the errant request. Based on implementation, it may not contain the full 32 bits of the address. Captures the address on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. Special Note: When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT = '1', this register is not available and therefore access to this register are treated as RAZ/WI.

0x3000F88 RIVA_M2VMT_ESR

Type: read-write
Reset State: 0xxxxxxxxx

M2VMT Error Status Register: Captures the status upon M2VMT configuration errors, as determined by the M2VMT_RPU_ACR. This register has read/write-clear access, meaning that reads simply provide a value in the register, while writes are performed by clearing those bits corresponding to '1's in the value written data, and leaving unchanged those bits corresponding to 0s n the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old error. A write with a '1' set in a bit field will result in clearing that bit. Writes with a 0 have no effect. The presence of an asserted value on any bit in this register is what prompts the assertion when enabled by M2VMT_CR[RPUEIE] of the M2MVT's interrupt output. Therefore these bits must be cleared by the interrupt handler. This is contrasted with the fields in the M2VMT_ESYNRn register, which are merely the "syndrome" of an error indicated by the M2VMT_ESR. For M2VMT, there is only one defined error status bit in the M2VMT_SER (actually two, if you count multi-error).

RIVA_M2VMT_ESR

Bits	Name	Description
31	MULTI	Multi-Error: When set to '1', indicates that an additional error occurred while M2VMT_ESR is non-zero. The M2VMT_EAR,M2VMT_ESYNRn and M2VMT_ESR registers (with the exception of this bit) lock on the first error, and must be cleared to unlock. Therefore, the status and the syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost. i.e., syndrome register and status register only stores details of the first error.
30:1	RESERVED	
0	CFG	Configuration Port Error: When set to '1', indicates an error associated with a configuration port request. Special Note: When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this register is treated as RAZ/WI.

0x3000F8C RIVA_M2VMT_ESRRESTORE

Type: read-write
Reset State: 0xxxxxxxxx

RIVA_M2VMT_ESRRESTORE

Bits	Name	Description
31:0	M2VMT_ESRRTORE	M2VMT Error Status Register Restore This is just an aliased address for M2VMT_ESR, which provides direct write access (rather than write-clear) for restoration purpose Special Note: When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this register is treated as RAZ/WI.

0x3000F90 RIVA_M2VMT_ESYNR0

Type: read-only
Reset State: 0xxxxxxxxx

Error Syndrome Register 0: Captures the syndrome on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) "lock" upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., the syndrome register and the status register stores only details of the first error.

RIVA_M2VMT_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request.
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request.
15:0	AMID	AMID[15:0] field of errant request. Special Note: When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT="1", this register is not available and therefore access to this register is treated as RAZ/WI.

0x3000F94 RIVA_M2VMT_ESYNR1

Type: read-only
Reset State: 0xxxxxxxxx

Error Syndrome Register 1: Captures syndrome upon M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for

the MULTI bit) “lock” upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is ‘1’ are lost, i.e., the syndrome register and the status register only stores details of the first error.

RIVA_M2VMT_ESYNR1

Bits	Name	Description
31	DCD	Decode: Indicates configuration port error due to invalid/ unrecognized/ unmapped/ un-implemented address (e.g., a reserved register address). Includes decode errors within the global address space. Also, note that decode error is never asserted for client port accesses.
30	AC	Access control: Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED_1	
24	AFULL	AFULL field of the errant request
23	AOOOWR	AOOOWR field of the errant request
22	AOOORD	AOOORD field of the errant request.
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request).
19	RESERVED_2	
18:16	ASIZE	ASIZE[2:0] field of the errant request).
15:12	ALEN	ALEN[3:0] field of the errant request.
11:10	ABURST	ABURST[1:0] field of the errant request.
9	RESERVED	
8	AWRITE	AWRITE field of the errant request.
7	AINST	AINST field of the errant request.
6	APROTNS	APROTNS field of the errant request.
5	APRIV	APRIV field of the errant request.
4	AINNERSHARED	AINNERSHARED field of the errant request.
3	ASHARED	ASHARED field of the errant request.
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

0x3000FF4 RIVA_M2VMT_REV

Type: read-only
Reset State: 0xxxxxxxxx

Reports the revision information for the M2VMT core and wrapper.

RIVA_M2VMT_REV

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field.

0x3000FF8 RIVA_M2VMT_IDR

Type: read-only
Reset State: 0xxxxxxxxx

Reports the size of the M2VMT table. It is a read-only register.

RIVA_M2VMT_IDR

Bits	Name	Description
31:9	RESERVED	
8:0	M2VMTSIZE	M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping. M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

0x3000FFC RIVA_M2VMT_RPU_ACR

Type: read-write
Reset State: 0xxxxxxxxx

Using the incoming VMID, this register controls access to the global register space.

RIVA_M2VMT_RPU_ACR

Bits	Name	Description
31:0	RWE	M2VMT local RPU Access control Register. Each bit position corresponds to a VMID. When set to ‘1’, that VMID is granted VMID read/write access to the entire block of registers within the M2VMT’s 4KB global address space, including this register itself. In practice, this register designates the VMID(s) that can act as SROT (e.g., scorpion-secure) or pseudo SROT (e.g. RPM ARM11). Special Note: When REMOVE_M2VMT_RPU=’1’, this register is not available and therefore access to this register is treated as RAZ/WI.

17 RPM Registers

17.1 Overview

Table 17-1 RPM Bases

Base Name	Parent	Address
RPM_GICD_CTLR	RPM_BASE	0x00000000
RPM_GICC_CTLR	RPM_BASE	0x00000000
RPM_TMR0_MTCH	RPM_BASE	0x00000000
RPM_BUS_CLK_FORCE_ON	RPM_BASE	0x00000000
RPM_APU_RGn_RACR	RPM_BASE	0x00000000
RPM_2x3_SFPB_CTRL_STATUS	RPM_BASE	0x00000000
RPM_SFPB_CTRL_STATUS	RPM_BASE	0x00000000
MSG_RAM_RPU_RGn_ACR	RPM_MSG_RAM_XPU_BASE	0x00100000
MPM_PMIC_VDD_CFG	MPM_BASE	0x00200000
PA1_SSBI2_CTL	PA1_SSBI2_CFG_BASE	0x00300000
PA1_RPU_CR	PA1_XPU_BASE	0x00400000
PA1_SSBI2_CMD	PA1_SSBI2_CMD_BASE	0x00500000
PA2_SSBI2_CTL	PA2_SSBI2_CFG_BASE	0x00600000
PA2_SSBI2_CMD	PA2_SSBI2_CMD_BASE	0x00C00000

17.2 RPM GIC D Registers (0x00000000 RPM_BASE)

This section contains the RPM GIC D registers.

The Generic Interrupt Controller (GIC) is a reusable configurable soft core. This generic interrupt controller specification conforms to ARM's Generic Interrupt Controller architecture specification. Where differences exist, either additional features were added or this document must change to conform to ARM's specified architecture. Where additional features were added, they will be clearly marked. The generic interrupt controller design supports ARM's TrustZone architecture, with two security zones: secure and non-secure.

The generic interrupt controller is made of two parts: the Distributor and CPU Interfaces (up to eight). Each of these interfaces contains a CRIF slave interface. There must be at least one CPU Interface in the design.

Only word and byte accesses are supported on these registers. Half-word accesses are not supported. Byte access is supported by a subset of the registers.

Security treatment of registers in the generic interrupt controller is divided into four types of registers. These are:

- 'Common' indicates that both secure and non-secure software have full access to the register.
- 'NS-int Dependent' indicates that state belonging to both secure and non-secure interrupts may be present in the register, depending on the value set in the Interrupt Security Register. Secure accesses to such a register are able to access all of the register's state, regardless of the Interrupt Security Register setting. Non-secure accesses may only access state belonging to non-secure interrupts. For non-secure accesses to state belonging to secure interrupts, writes are ignored and reads return zero.
- 'Banked', indicates that the register exhibits different functionality according to whether it is accessed with a secure or non-secure request.
- 'Restricted' indicates that only secure requests may access this register. If non-secure accesses are attempted, writes are ignored and reads return zero.

The type of register is specified for each register individual. Table 17-2 explains security treatment for register bits.

Table 17-2 Register security treatment

bus NS bit	SECURITY BIT	ALLOW Access
0	0	1
0	1	1
1	0	0
1	1	1

Glossary:

CPU Interface: That part of the GIC2 responsible for receiving the next interrupt from the Distributor and, if the interrupt has sufficient priority, asserting an interrupt indication to the CPU.

CPU MID: The Master ID of a CPU interface (as in AXI's AMID). The CPU MID reaching the Distributor must match the CPU Interface connected to that master.

Distributor: That part of the GIC2 responsible for detecting, disabling, prioritizing, and directing interrupts to CPU(s). The Distributor also accepts requests from and signals software interrupts to the CPU(s).

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NS-int: Security status of a particular interrupt ID. The value 0x0 is "secure", 0x1 is "non-secure".

NS-prot: Security status of the a bus transaction (read or write) according to the NS bit.

PPI: Private Peripheral Interrupt, interrupt from a peripheral whose interrupt line is destined to a particular CPU and can't be physically connected/directed to any other.

SGI: Software Generated Interrupt, interrupt from one CPU (or thread) to another.

SPI: Shared Peripheral Interrupt, interrupt from a peripheral whose interrupt line's CPU target is programmable to one or more CPU interface by the Distributor.

17.2.1 Generic Interrupt Controller Distributor

Table 17-3 GIC Distributor Register Summary*

Address	Name	Type	Reset	Security Treatment	Description
0x0000	GICD_CTLR	RW	0x0	Banked	distributor control
0x0004	GICD_TYPER	R	Unknown	Common	distributor type
0x0008	GICD_IIDR	R	0x0000_0070	Common	distributor ID
0x0080 + 4n	GICD_ISR	RW	0x0	Restricted	distributor interrupt security
0x0100 + 4n	GICD_ISENABLER	RW	0x0	NS-int dependent	distributor interrupt set-enable
0x0180 + 4n	GICD_ICENABLER	RW	0x0	NS-int dependent	distributor interrupt clear-enable
0x0200 + 4n	GICD_ISPENDR	RW	0x0	NS-int dependent	distributor interrupt set-pending

Table 17-3 GIC Distributor Register Summary*

Address	Name	Type	Reset	Security Treatment	Description
0x0280 + 4n	GICD_ICPENDR	RW	0x0	NS-int dependent	distributor interrupt clear-pending
0x0300 + 4n	GICD_IACTIVER	R	0x0	NS-int dependent	distributor interrupt active
0x0400 + 4n	GICD_IPRIORITYR	RW	0x0	NS-int dependent	distributor interrupt priority
0x0800 + 4n	GICD_ITARGETSR	RW	0x0	NS-int dependent	distributor interrupt targets
0x0C00 + 4n	GICD_ICFGR	RW	0x0	NS-int dependent	distributor interrupt configuration
0x0D00-0x0EFF	Reserved				
0x0F00	GICD_SGIR	W	N/A	Banked	distributor software-generated interrupt
0x0FD0	GICD_PIDR0	R	0x0000_0090	Common	distributor peripheral ID
0x0FD4	GICD_PIDR1	R	0x0000_0003	Common	
0x0FD8	GICD_PIDR2	R	0x0000_001F	Common	
0x0FDC	GICD_PIDR3	R	0x0000_0000	Common	
0x0FE0	GICD_PIDR4	R	0x0000_0000	Common	
0x0FE4	GICD_PIDR5	R	0x0000_0000	Common	
0x0FE8	GICD_PIDR6	R	0x0000_0000	Common	
0x0FEC	GICD_PIDR7	R	0x0000_0000	Common	
0xFF0	GICD_CIDR0	R	0x0000_000D	Common	distributor component ID
0xFF4	GICD_CIDR1	R	0x0000_00F0	Common	
0xFF8	GICD_CIDR2	R	0x0000_0005	Common	
0xFFC	GICD_CIDR3	R	0x0000_00B1	Common	

17.2.2 Generic Interrupt Controller distributor registers

0x00060000 RPM_GICD_CTLR

Type: Read/write
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICD_CTLR register controls if the Distributor responds to external interrupt stimulus changes.

Non-secure access: Distributor provides access to the enable_ns register in bit 0.

Secure access: Distributor provides access to the enable_s register in bit 0, and the enable_ns register in bit 1.

RPM_GICD_CTLR

Bits	Name	Description
31:2	RESERVED	
1	ENABLE_NS	This bit is an alias of the enable_ns bit. This bit is only usable by Secure software. 0x0: CLR 0x1: SET
0	ENABLE	This bit is the enable bit for both Secure and Non-secure software. Secure software accesses enbale_s at this location. Non-secure software accesses enable_ns. 0x0: CLR 0x1: SET

0x00060004 RPM_GICD_TYPER

Type: Read
Clock: AHB_CLK
Reset State: Unknown

Security Treatment: Common

The GICD_TYPER register provides information about the configuration of the GIC.

RPM_GICD_TYPER

Bits	Name	Description
31:16	RESERVED	
15:11	LSPI	Returns the number of Lockable Shared Peripheral Interrupts (LSPIs) that the generic interrupt controller contains. The generic interrupt controller does not support lockable SPIs, always reads back 0x0.
10	TZ	TrustZone support. The generic interrupt controller supports TrustZone, always reads back 0x1.
9:8	RESERVED_BITS9_TO_8	

RPM_GICD_TYPER (cont.)

Bits	Name	Description
7:5	CPU_NUM	Returns the number of CPU interfaces that the generic interrupt controller provides. The generic interrupt controller provides either: 0b 000 = one CPU interface 0b 001 = two CPU interfaces 0b 010 = three CPU interfaces 0b 011 = four CPU interfaces 0b 100 = five CPU interfaces 0b 101 = six CPU interfaces 0b 110 = seven CPU interfaces 0b 111 = eight CPU interfaces.
4:0	IT_LINES	Returns the number of INTIDs, to the nearest 32, that the Distributor provides. Read as: 0b 00000 = the Distributor is configured for up to 32 INTIDs 0b 00001 = the Distributor is configured for up to 64 INTIDs 0b 00010 = the Distributor is configured for up to 96 INTIDs 0b 00011 = the Distributor is configured for up to 128 INTIDs . . . 0b 11110 = the Distributor is configured for up to 992 INTIDs 0b 11111 = the Distributor is configured for up to 1020 INTIDs.

0x00060008 RPM_GICD_IIDR

Type: Read
Clock: AHB_CLK
Reset State: 0x00000070

Security Treatment: Common

The GICD_IIDR register provides information the implementer of the Distributor and the revision of the Distributor.

RPM_GICD_IIDR

Bits	Name	Description
31:24	RESERVED	
15:12	REVISION	Returns the revision number of the Distributor, 0x0
11:0	IMPLEMENTOR	Returns JEP106 ID number, 0b 01110000

0x00060020 RPM_GICD_ANSACR

Type: Read/write
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: Restricted

The auxiliary non-secure access control register (GICD_ANSACR) is used to control non-secure access to GICD_CGCR.

RPM_GICD_ANSACR

Bits	Name	Description
31:1	RESERVED	
0	GICD_CGCR	0x0: SEC (Dis-allows non-secure access.) 0x1: NS (Allows non-secure access.)

0x00060024 RPM_GICD_CGCR

Type: Read/write
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: Restricted

The clock gate control register (GICD_CGCR) is used to control localized clock gating over-ride logic. Setting bits in GICD_CGCR disables the corresponding local clock gating logic. The local clock gating logic normally turns off a local (small subset) clock tree automatically if there is no need for the clock. If any error is found in the gating logic, these bits can be used to over-ride it.

RPM_GICD_CGCR

Bits	Name	Description
31:17	RESERVED_31_TO_17	
16	TOP	Controls the top level clock gate (which gates entire GIC). 0x1: DISABLE 0x0: ENABLE
15:4	RESERVED_15_TO_4	
3	DI_SGI_STATE	Controls the clock gate for Distributer interrupt state data base registers for SGI interrupts. 0x1: DISABLE 0x0: ENABLE
2	DI_PPI_SPI_STATE	Controls the clock gate for Distributer interrupt state data base registers for PPI and SPI interrupts. 0x1: DISABLE 0x0: ENABLE

RPM_GICD_CGCR (cont.)

Bits	Name	Description
1	DI_DEMET	Controls the clock gate for Distributer interrupt input demet registers. 0x1: DISABLE 0x0: ENABLE
0	DI_RD	Controls the clock gate for Distributer CRIF Read Data. 0x1: DISABLE 0x0: ENABLE

0x00060080+4*n RPM_GICD_ISRn, n=[0..8]

Type: Read/write
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: Restricted

Each bit in an GICD_ISR register controls the security state of an interrupt, to be either secure or non-secure. You can only access these registers with secure read or secure write accesses.

NOTE The GICD_ISR register at address offset 0x0080 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

RPM_GICD_ISRn

Bits	Name	Description
31:0	INT_NS	0x0: SEC (Assigns INTID N to the Secure state.) 0x1: NS (Assigns INTID N to the Non-secure state.)

0x00060100+4*n RPM_GICD_ISENABLERn, n=[0..8]

Type: Write (command - readable)
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in an GICD_ISENABLER register controls the enabling of an interrupt.

Reading this register returns the currently enabled interrupts subject to NS-int dependent access rules.

NOTE The GICD_ISENABLER register at address offset 0x0100 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

RPM_GICD_ISENABLERn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ICENABLER register.) 0x1: SET (Enables INTID N.)

0x00060180+4*n RPM_GICD_ICENABLERn, n=[0..8]

Type: Write (command - readable)
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in an GICD_ICENABLER register controls the disabling of an interrupt.

Reading this register returns the currently enabled interrupts subject to NS-int dependent access rules.

NOTE The GICD_ICENABLER register at address offset 0x0180 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

RPM_GICD_ICENABLERn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ISENABLER register.) 0x1: CLR (Enables INTID N.)

0x00060200+4*n RPM_GICD_ISPENDRn, n=[0..8]

Type: Write (command - readable)
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in an GICD_ISPENDR register controls the enabling of an interrupt.

Reading this register returns the currently pending interrupts subject to NS-int dependent access rules.

NOTE The GICD_ISPENDR register at address offset 0x0200 is repeated once per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI interrupts. SGI interrupt bits are read-only, however the distributor updates these using the GICD_SGIR register. The remaining registers control the SPI interrupts.

RPM_GICD_ISPENDRn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ICPENDR register.) 0x1: SET (Sets INTID N to the Pending state.)

0x00060280+4*n RPM_GICD_ICPENDRn, n=[0..8]

Type: Write (command - readable)
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in an GICD_ICPENDR register controls the disabling of an interrupt.

Reading this register returns the currently pending interrupts subject to NS-int dependent access rules.

NOTE The GICD_ICPENDR register at address offset 0x0280 is banked, that is there is one per CPU Interface. It is only accessible from the designated CPU and controls that CPU's PPI interrupts. SGI interrupt bits are read-only, however the distributor updates these using the GICD_SGIR register. The remaining registers control the SPI interrupts.

RPM_GICD_ICPENDRn

Bits	Name	Description
31:0	INT	0x0: NA (No effect. Use GICD_ISPENDR register.) 0x1: CLR (Clears INTID N. from the pending state.)

0x00060300+4*n RPM_GICD_IACTIVERn, n=[0..8]

Type: Read
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each bit in the GICD_IACTIVER register provides the active status of an interrupt.

NOTE The GICD_IACTIVER register at address offset 0x0300 is repeated once per CPU Interface. It is only accessible from the designated CPU and provides information for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

RPM_GICD_IACTIVERn

Bits	Name	Description
31:0	INT	0x0: CLR 0x1: SET

0x00060400+4*n RPM_GICD_IPRIORITYRn, n=[0..71]

Type: Read/write
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each field in the GICD_IPRIORITYR registers controls the priority level of an interrupt.

NOTE The GICD_IPRIORITYR registers at address offsets 0x0400 to 0x41C are repeated once per CPU Interface. These are only accessible from the designated CPU and control the priority levels for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupt priority levels.

NOTE This register is byte addressable.

The GICD_IPRIORITYR register behaves differently depending on the security setting of interrupt associated with the address written (NS-int) and the security of the bus transaction (NS-prot). Figure 26-1 shows how these differences affect different types of access.

Figure 26-1 Summary of the secure and non-secure views of interrupt priority

RPM_GICD_IPRIORITYRn

Bits	Name	Description
31:24	INT3	
23:16	INT2	
15:8	INT1	

RPM_GICD_IPRIORITYRn (cont.)

Bits	Name	Description
7:0	INT0	All bits cleared (0x0) is the highest priority. All bits set (0xFF) is the lowest priority. For non-secure write access, the MSB is always set (0x1). For non-secure read access, the MSB is always clear (0x0). Non-secure entities can't use the highest priorities without secure software setting such a priority. The highest priorities are typically reserved for secure software. On the other hand, secure software can, if needed, write and read the MSB. Secure entities have access to all priorities. Secure interrupts can use priority numbers 0x80-0xFF (the lower half of the priority spectrum) if needed. Due to strict 'less than' comparisons used in the CPU interface, setting an interrupt's priority to 0xFF effectively disables that interrupt. The number of priorities actually supported is determined by NUM_PRI generic. Software can determine this number by writing 0xFF and reading back the result.

0x00060800+4*n RPM_GICD_ITARGETSRn, n=[0..71]

Type: Read/write
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each field in the GICD_ITARGETSR registers controls the destination CPU(s) of an interrupt.

NOTE The GICD_ITARGETSR registers at address offsets 0x0800 to 0x81C are not actually implemented. These are place holders PPI and SGI interrupts. PPI interrupts, being private, only have one destination CPU. SGI interrupts are generated by the QGIC_DI_SOFT_INT register only. The remaining registers control the SPI interrupt destinations.

NOTE This register is byte addressable.

RPM_GICD_ITARGETSRn

Bits	Name	Description
31:24	INT3	
23:16	INT2	
15:8	INT1	

RPM_GICD_ITARGETSRn (cont.)

Bits	Name	Description
7:0	INT0	Each bit represents one of 8 CPUs. Bit 0 represents the zeroth CPU, bit 7 represents the seventh CPU. Setting this field to 0 will disable the interrupt as no CPU will see it set. For INTIDs < 32 (the SGI and PPI) the CPU ID (of the master) is returned on reads. Writes are ignored. The number of CPUs actually supported is determined by NUM_CPU generic. Software can determine this number by writing 0xFF and reading back the result.

0x00060C00+4*n RPM_GICD_ICFGRn, n=[0..17]

Type: Read/write
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: NS-int dependent

Each field in the GICD_ICFGR registers allows:

- control of type of an SPI:
- level-sensitive
- edge-sensitive
- reading the type of PPIs and sgis

NOTE The GICD_ICFGR registers at address offsets 0x0C00 to 0xC04 are repeated once per CPU Interface. These are only accessible from the designated CPU and allow read access for that CPU's PPI and SGI interrupts. The remaining registers control the SPI interrupts.

NOTE This register is not byte addressable, interrupts should be disabled before configuring their type.

RPM_GICD_ICFGRn

Bits	Name	Description
31:30	INT15	
29:28	INT14	
27:26	INT13	
25:24	INT12	
23:22	INT11	

RPM_GICD_ICFGRn (cont.)

Bits	Name	Description
21:20	INT10	
19:18	INT9	
17:16	INT8	
15:14	INT7	
13:12	INT6	
11:10	INT5	
9:8	INT4	
7:6	INT3	
5:4	INT2	
3:2	INT1	
1:0	INT0	These bits behave differently for each of the three interrupt types as follows: 0x0: LVL N to N 0x1: LVL 1 to N 0x2: EDGE N to N 0x3: EDGE 1 to N 0x0: For SGI, read back as 0b10 - SGI interrupts are edge-sensitive and use the N-N model. 0x0: For PPI/SPI, read/writable as 0b01 or 0b11 - PPI/SPI interrupts can be edge or level sensitive and use the 1-N model.

0x00060F00 RPM_GICD_SGIR

Type: Write (command)
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICD_SGIR register provides the method by which software may cause interrupts to become pending for designated target CPU(s). The generic interrupt controller maintains an internal database of all outstanding software interrupt requests pended to each CPU Interface and rotates through them in Round Robin fashion. Signaling the same interrupt a second time before it is serviced will result in only one interrupt from the source CPU to the target CPU(s).

Table 17-4 Security status of the write event

Security status of the write event to the GICD_SGIR register (the state of the NS bit)	SATT Value	Interrupt's security status as set by GICD_ISR	Requested Interrupt set as pending on the target CPU
Secure	0	Secure	YES
Secure	0	Non-secure	NO
Secure	1	Secure	NO
Secure	1	Non-secure	YES
Non-secure	X	Secure	NO
Non-secure	X	Non-secure	YES

RPM_GICD_SGIR

Bits	Name	Description
31:26	RESERVED_BITS31_TO_26	
25:24	T_FILTER	Target Filter 0x0: LIST (Use the T_LIST as is) 0x1: OTHERS (Send to all CPUs except the CPU MID making the request, ignoring T_LIST) 0x2: MID (Send to only the CPU MID making the request, ignoring T_LIST) 0x3: NA (Reserved)
23:16	T_LIST	Target List. Each bit set represents a CPU target for the INT_ID, subject to the T_FILTER field. 0x1: CPU0 0x2: CPU1 0x4: CPU2 0x8: CPU3 0x10: CPU4 0x20: CPU5 0x40: CPU6 0x80: CPU7
15	SATT	Security ATTribute. This bit is only programmable by secure Software. See 0x0: SECURE (Secure interrupt is issued) 0x1: NONSECURE (Non-secure interrupt is issued.)
14:4	RESERVED_BITS14_TO_4	
3:0	INT_ID	The INT ID number (0-15) of the SGI to be set as pending. See the See Table 10-4 Security Status SGI pending truth table for security status Table 17-4 (SATT vs. NS-prot) for information on the conditions that allow an SGI to be set pending.

0x00060FD0 RPM_GICD_PIDR0

Type: Read
Clock: AHB_CLK
Reset State: 0x00000090

Security Treatment: Common

The GICD_PIDR0 provides access to generic interrupt controller peripheral identification.

RPM_GICD_PIDR0

Bits	Name	Description
31:8	RESERVED	
7:0	PART_NUM	Returns lower byte of the generic interrupt controller part number 0xB390, 0x90

0x00060FD4 RPM_GICD_PIDR1

Type: Read
Clock: AHB_CLK
Reset State: 0x00000003

Security Treatment: Common

The GICD_PIDR1 provides access to generic interrupt controller peripheral identification.

RPM_GICD_PIDR1

Bits	Name	Description
31:8	RESERVED	
7:4	DESIGNER	Returns JEDEC JEP code bits 3:0, 0x0.
3:0	PART_NUM	Returns upper nibble of the generic interrupt controller part number 0x390, 0x3

0x00060FD8 RPM_GICD_PIDR2

Type: Read
Clock: AHB_CLK
Reset State: 0x0000001F

Security Treatment: Common

The GICD_PIDR2 provides access to generic interrupt controller peripheral identification.

RPM_GICD_PIDR2

Bits	Name	Description
31:8	RESERVED	
4	ARCH_VERSION	Returns the generic interrupt controller architecture revision number, 0x1
3	USES_JEP_CODE	Reads 0x1.
2:0	DESIGNER	Returns JEDEC JEP code bits 6:4, 0x7.

0x00060FDC RPM_GICD_PIDR3

Type: Read
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR3 provides access to generic interrupt controller peripheral identification.

RPM_GICD_PIDR3

Bits	Name	Description
31:0	RESERVED_1	
7:4	REVISION	Returns 0x0.
3:0	RESERVED_2	ARM defined field.

0x00060FE0 RPM_GICD_PIDR4

Type: Read
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR4 provides access to generic interrupt controller peripheral identification.

RPM_GICD_PIDR4

Bits	Name	Description
31:8	RESERVED_1	
7:4	RESERVED_2	ARM defined field.
3:0	DESIGNER	JEDEC JEP code bits 10:7, 0x0

0x00060FE4 RPM_GICD_PIDR5

Type: Read
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR5 provides access to generic interrupt controller peripheral identification.

RPM_GICD_PIDR5

Bits	Name	Description
31:0	RESERVED	

0x00060FE8 RPM_GICD_PIDR6

Type: Read
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR6 provides access to generic interrupt controller peripheral identification.

RPM_GICD_PIDR6

Bits	Name	Description
31:0	RESERVED	

0x00060FEC RPM_GICD_PIDR7

Type: Read
Clock: AHB_CLK
Reset State: 0x00000000

Security Treatment: Common

The GICD_PIDR7 provides access to generic interrupt controller peripheral identification.

RPM_GICD_PIDR7

Bits	Name	Description
31:0	RESERVED	

0x00060FF0 RPM_GICD_CIDR0

Type: Read
Clock: AHB_CLK
Reset State: 0x0000000D

Security Treatment: Common

The GICD_CIDR0 provides access to generic interrupt controller component identification.

RPM_GICD_CIDR0

Bits	Name	Description
31:8	RESERVED	
7:0	COMP_ID_0	Reads back as 0x0D.

0x00060FF4 RPM_GICD_CIDR1

Type: Read
Clock: AHB_CLK
Reset State: 0x000000F0

Security Treatment: Common

The GICD_CIDR1 provides access to generic interrupt controller component identification.

RPM_GICD_CIDR1

Bits	Name	Description
31:8	RESERVED	
7:0	COMP_ID_1	Reads back as 0xF0.

0x00060FF8 RPM_GICD_CIDR2

Type: Read
Clock: AHB_CLK
Reset State: 0x00000005

Security Treatment: Common

The GICD_CIDR2 provides access to generic interrupt controller component identification.

RPM_GICD_CIDR2

Bits	Name	Description
31:8	RESERVED	
7:0	COMP_ID_2	Reads back as 0x05.

0x00060FFC RPM_GICD_CIDR3

Type: Read
Clock: AHB_CLK
Reset State: 0x000000B1

Security Treatment: Common

The GICD_CIDR3 provides access to generic interrupt controller component identification.

RPM_GICD_CIDR3

Bits	Name	Description
31:8	RESERVED	
7:0	COMP_ID_3	Reads back as 0xB1.

17.3 RPM GIC GICC Registers (0x00000000 RPM_BASE)

This section contains the RPM GIC C registers.

The Generic Interrupt Controller (GIC) is a reusable configurable soft core. This GIC specification conforms to ARM's Generic Interrupt Controller architecture specification. Where differences exist, either additional features were added or this document must change to conform to ARM's specified architecture. Where additional features are added they will be clearly marked. The generic interrupt controller design supports ARM's TrustZone architecture with two security zones: secure and non-secure.

The generic interrupt controller is made of two parts: the Distributor and CPU Interfaces (up to eight). Each of these interfaces contains a CRIF slave interface. There must be at least one CPU Interface in the design.

Only word and byte accesses are supported on these registers. Half-word accesses are not supported. Byte access is supported by a subset of the registers.

Security treatment of registers in the generic interrupt controller is divided into four types of registers. These are:

- 'Common' indicates that both secure and non-secure software have full access to the register.
- 'NS-int Dependent' indicates that state belonging to both secure and non-secure interrupts may be present in the register, depending on the value set in the Interrupt Security Register. Secure accesses to such a register are able to access all of the register's state, regardless of the Interrupt Security Register setting. Non-secure accesses may only access state belonging to non-secure interrupts. For non-secure accesses to state belonging to secure interrupts, writes are ignored and reads return zero.
- 'Banked', indicates that the register exhibits different functionality according to whether it is accessed with a secure or non-secure request.
- 'Restricted' indicates that only secure requests may access this register. If non-secure accesses are attempted, writes are ignored and reads return zero.

The type of register is specified for each register individual. Table 17-5 explains security treatment for register bits.

Table 17-5 Register security treatment

bus NS bit	SECURITY BIT	ALLOW Access
0	0	1
0	1	1
1	0	0
1	1	1

Glossary:

CPU Interface: That part of the GIC2 responsible for receiving the next interrupt from the Distributor and, if the interrupt has sufficient priority, asserting an interrupt indication to the CPU.

CPU MID: The Master ID of a CPU interface (as in AXI's AMID). The CPU MID reaching the Distributor must match the CPU Interface connected to that master.

Distributor: That part of the GIC2 responsible for detecting, disabling, prioritizing, and directing interrupts to CPU(s). The Distributor also accepts requests from and signals software interrupts to the CPU(s).

FABRIC: Flexible Advanced Buses & Reusable Interconnect Cores

NS-int: Security status of a particular interrupt ID. The value 0x0 is "secure", 0x1 is "non-secure".

NS-prot: Security status of the a bus transaction (read or write) according to the NS bit.

PPI: Private Peripheral Interrupt, interrupt from a peripheral whose interrupt line is destined to a particular CPU and can't be physically connected/directed to any other.

SGI: Software Generated Interrupt, interrupt from one CPU (or thread) to another.

SPI: Shared Peripheral Interrupt, interrupt from a peripheral whose interrupt line's CPU target is programmable to one or more CPU interface by the Distributor.

17.3.1 Generic Interrupt Controller CPU Interface

Table 17-6 GIC CPU Interface Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x1000	GICC_CTLR	RW	0x0000_0000	Banked	CPU interface control register
0x1004	GICC_PMR	RW	0x0000_0000	Banked	CPU interface priority mask
0x1008	GICC_BPR	RW	0x0000_0000	Banked	CPU interface binary point
0x100C	GICC_IAR	R (CMD)	0x0000_0000	Banked	CPU interface interrupt acknowledge
0x1010	GICC_EOIR	W (CMD)	0x0000_0000	Banked	CPU interface end-of-interrupt
0x1014	GICC_RPR	R	0x0000_0000	Banked	CPU interface running priority
0x1018	GICC_HPPIR	R	0x0000_0000	Banked	CPU interface highest priority pending

Table 17-6 GIC CPU Interface Register Summary

Address	Name	Type	Reset	Security Treatment	Description
0x101C	GICC_ABPR	RW	0x0000_0000	Restricted	CPU interface aliased binary point
0x10FC	GICC_IIDR	R	0x0001_0070	Common	CPU interface ID register

17.3.1.1 GIC CPU interface registers

0x00061000 RPM_GICC_CTLR

Type: Read/write
Clock: ACC_AHB_CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_CTLR configures the generic interrupt controller CPU interface.

Non-secure access: Access is granted only to bit 0, the enable register bit for non-secure interrupts.

Secure access: Access is granted to all register bits. Note that enable is aliased as bit 1, enable_ns. It is modifiable in that position and any such modifications will be seen by non secure accesses as changes to the enable bit (bit 0).

RPM_GICC_CTLR

Bits	Name	Description
31:5	RESERVED	
4	SBPR	Controls which binary point register is used to calculate preemption. 0x0: BANKED (secure interrupts use the secure Binary Point Register, non-secure interrupts use the non-secure Binary Point Register) 0x1: RESTRICTED (all interrupts use the secure Binary Point Register)
3	S_DEST	Controls destination of secure interrupts. 0x0: IRQ 0x1: FIQ

RPM_GICC_CTLR (cont.)

Bits	Name	Description
2	S_ACK	Controls the side effect behavior of a secure read request to the Interrupt Acknowledge Register in the case where the highest priority pending interrupt is non-secure. If AckCtl is set to 0, a secure read request to the Interrupt Acknowledge Register returns an Interrupt ID value of 1022, and the read request does not cause the interrupt to be acknowledged (that is the Pending status of the interrupt remains unchanged). If AckCtl is set to 1, a secure read request to the Interrupt Acknowledge Register returns the Interrupt ID value of the non-secure interrupt, and causes the interrupt to be acknowledged (that is the interrupt becomes Active, or Active and Pending). 0x0: DISABLE ACK OF NS PENDING 0x1: ENABLE ACK OF NS PENDING
1	ENABLE_NS	For secure software, a read/writable alias of non secure software's enable bit (bit 0 of this same register in non secure space). 0x0: CLR 0x1: SET
0	ENABLE	For non-secure software, this bit enables/disables non secure interrupts. For secure software, this bit enables/disables secure interrupts. 0x0: CLR 0x1: SET

0x00061004 RPM_GICC_PMR

Type: Read/write
Clock: ACC_AHB_CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_PMR register configures the generic interrupt controller CPU interface Priority Mask. The Priority Mask can be used to limit the interrupts that can cause an interrupt request to the CPU based on priority levels.

- Non-secure access: Write access is granted only if bit 7 is 0x1, writes are ignored otherwise. Reads are always granted, however, bit 7 is always set in the data returned. Bit 0 is always zero.
- Secure access: Access is granted to all register bits.

RPM_GICC_PMR

Bits	Name	Description
31:8	RESERVED	
7:0	LEVEL	Set the Priority Mask Level. The CPU interface asserts an interrupt request to CPU if the priority of the highest Pending interrupt sent by the interrupt Distributor is strictly higher than at least the mask set in Priority Mask Register.

0x00061008 RPM_GICC_BPR

Type: Read/write
Clock: ACC_AHB_CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_BPR register configures the generic interrupt controller CPU interface Binary Point. The Binary Point is used to limit interrupts that can cause an interrupt request to the CPU based on the interrupt's priority and the interrupt priority that currently being serviced by the CPU (if there is one). If the CPU is not servicing an interrupt, the Binary Point register is not used.

- Non-secure access: Provides access to the non-secure Binary Point register.
- Secure access: Provides access to the secure Binary Point register. Secure software may access the non secure Binary Point register at offset 0x001C

Table 17-7 Interpretation of Binary Point Register value

register value	Priority bits used to determine preemption for secure interrupts.	Priority bits used to determine preemption for non-secure interrupts. (Bit 7 is always 0x1)
0	7:1	7:0
1	7:2	7:1
2	7:3	7:2
3	7:4	7:3
4	7:5	7:4
5	7:6	7:5
6	7	7:6
7	No preemption	No preemption

RPM_GICC_BPR

Bits	Name	Description
31:3	RESERVED	

RPM_GICC_BPR (cont.)

Bits	Name	Description
2:0	VAL	The VAL setting is used according to determine the priority bits used for preemption according to Table 17-7 Interpretation of Binary Point Register value.

0x0006100C RPM_GICC_IAR

Type: Read (Command)
Clock: ACC_AHB_CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_IAR register is used by the CPU to obtain the ID of the interrupt which caused the assertion if IRQn or FIQn.

Performing this read has the side effect of causing the Distributor to change the interrupt from the Pending state to the Active or Active and Pending state.

- Non-secure access: See Table 17-8.
- Secure access: See Table 17-8.

Table 17-8 Access

Highest Pending interrupt security status (NS-int)	Security status of the read request (NS-prot)	GICC_CTLR register S_ACK bit	Security Match	Interrupt ID returned
Non-secure	Non-secure	x	Yes	Non-secure Interrupt ID
Secure	Secure	x	Yes	Secure Interrupt ID
Non-secure	Secure	1	Yes	Non-secure Interrupt ID
Non-secure	Secure	0	No	Highest outstanding interrupt is non-secure (1022)
Secure	Non-secure	x	No	No outstanding interrupts (1023)
No pending interrupts	x	x	No	No outstanding interrupts (1023)

RPM_GICC_IAR

Bits	Name	Description
31:13	RESERVED	

RPM_GICC_IAR (cont.)

Bits	Name	Description
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier. The value returned in this field is dependent on the security state of the access to the register, and the security state of any outstanding interrupts, as described in Table 17-7 Interpretation of Binary Point Register value.

0x00061010 RPM_GICC_EOIR

Type: Write (Command)
Clock: ACC_AHB_CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_EOIR (End Of Interrupt) register is written to indicate when software has finished handling an interrupt. Writing to this register will set the interrupt to Inactive or Pending (if prior to writing to this register, the interrupt was both Active and Pending) in the Distributor. The value written must be the interrupt ID, and the CPU Source ID for SGIs, of the interrupt that is being completed. The security status of the write to this register (NS-prot) must match the security status (NS-int) of the interrupt ID, according to Table 17-9 for the interrupt to be successfully cleared.

- Non-secure access: See Table 17-9**.**
- Secure access: See Table 17-9.

Currently Active interrupt

Table 17-9 GICC_EIOR security (and source CPU) match definition

security status (NS-int)	Security status of the write request (NS-prot)	GICC_CTLR register S_ACK bit	Written values of CPU Source ID and Interrupt ID match an Active interrupt' (sgis only)	Interrupt successfully returned to being Inactive or Pending'
Non-secure	Non-secure	x	Yes	Yes
Secure	Secure	x	Yes	Yes
Non-secure	Secure	1	Yes	Yes
Non-secure	Secure	0	Yes	No
Secure	Non-secure	x	Yes	No
No pending interrupts	x	x	No	No

RPM_GICC_EOIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it must match the ID of the CPU which requested the Interrupt. As described in Table 17-9, the CPU Source ID must match an active interrupt in order for the GICC_EOIR to take effect. The CPU_ID is written must match that delivered to software when GICC_IAR is read. For PPIs and SPIs the CPU source ID field is ignored.
9:0	INT_ID	Interrupt Identifier. The value must match the interrupt ID that software received when reading the GICC_IAR register. If the security settings match (see Table 17-9) the Active state in the Distributor for the corresponding interrupt will be cleared.

0x00061014 RPM_GICC_RPR

Type: Read
Clock: ACC_AHB_CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_RPR (Running Priority) register provides access to the highest priority of all the Active interrupts on this CPU. The priority value returned is sensitive to the security status (NS-int) of the interrupt currently running and the NS-prot

Non-secure access: If the currently interrupt is secure (NS-int = 0), and a non-secure read of the Running Priority register is attempted (NS-prot = 1), then the value 0 (maximum priority) is returned.

Secure access: Returns the true value in the register.

RPM_GICC_RPR

Bits	Name	Description
31:8	RESERVED	
7:0	VAL	Running Priority

0x00061018 RPM_GICC_HPPIR

Type: Read
Clock: ACC_AHB_CLK
Reset State: 0x00000000

Security Treatment: Banked

The GICC_HPPIR register provides access to the highest priority pending interrupt to the CPU Interface.

NOTE Interrupts that are Active and Pending in the Distributor are not considered candidates to be come the highest priority pending interrupt.

- Non-secure access: Same as for GICC_IAR register. See Table 17-7.
- Secure access: Same as for GICC_IAR register. See Table 17-7, Interpretation of Binary Point Register value.

RPM_GICC_HPPIR

Bits	Name	Description
31:13	RESERVED	
12:10	CPU_ID	CPU Source ID value is only valid if the interrupt is a Software Interrupt, in which case it contains the ID of the CPU which requested the Interrupt. For PPIs and SPIs the CPU source ID field is read as zero and should be ignored.
9:0	INT_ID	Interrupt Identifier. The value returned in this field is dependent on the security state of the access to the register, and the security state of any outstanding interrupts, as described in Table 17-7

0x0006101C RPM_GICC_ABPR

Type: Read/write
Clock: ACC_AHB_CLK
Reset State: 0x00000000

Security Treatment: Restricted

The GICC_ABPR register provides a copy of the non-secure binary point register for use by secure software. See the definition of the GICC_BPR register for details on the use of this register.

- Non-secure access: No access.
- Secure access: Access granted, updates are reflected to non-secure software at the GICC_BPR register at address offset 0x08.

RPM_GICC_ABPR

Bits	Name	Description
31:3	RESERVED	
2:0	VAL	Same as the GICC_BPR register - affects only non-secure interrupts.

0x000610FC RPM_GICC_IIDR

Type: Read
Clock: ACC_AHB_CLK
Reset State: 0x00010070

Security Treatment: Common

The GICC_IIDR register provides information about the generic interrupt controller CPU Interface version and device implementer information.

RPM_GICC_IIDR

Bits	Name	Description
31:20	PART_NUM	Part Number: 0x390
19:16	ARCH_VERSION	Architecture Version : 0x1
15:12	REVISION	Revision number: 0x0
11:0	IMPLEMENTOR	Bits[11:8] contain the implementer's JEP106 continuation code, 0x0 Bit[7] is always 0 Bits[6:0] contain bits [6:0] of the implementer's JEP106 code,

17.4 RPM Timer Registers (0x00000000 RPM_BASE)

This section contains RPM timer registers.

17.4.1 RPM timers

RPM timers block consists of three timers. Tmr0 is an XO time, i.e., its clock source is either PXO or CXO. TMR1 is a slow clock timer i.e., it is supposed to run on sleep clock. RPM also has a wdog timer. The clock source for this again is sleep clock.

17.4.1.1 RPM timers registers

0x00062000 RPM_RPM_TMR0_MTCH

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0000_0000

RPM TMR0 will signal interrupt when its counter value has reached the value stored in the RPM_TMR0_MTCH register.

RPM_RPM_TMR0_MTCH

Bits	Name	Description
31:0	MTCH	The value of RPM_TMR0_CNT at which an interrupt will be generated.

0x00062004 RPM_RPM_TMR0_CNT

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0000_0000

The RPM_TMR0_CNT register contains the current value of RPM TMR0. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the RPM_TMR0_MTCH register at the same time due to HW re-use. The procedure for writing the RPM_TMR0_CNT is as follows:

- Disable the timer by clearing the EN bit in RPM_TMR0_EN.
- Write RPM_TMR0_CNT.
- Write RPM_TMR0_MTCH, to restore match value.
- Enable the timer by setting the EN bit in RPM_TMR0_EN.

RPM_RPM_TMR0_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer count

0x00062008 RPM_RPM_TMR0_EN

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_TMR0_EN register is used to enable the RPM TMR0.

RPM_RPM_TMR0_EN

Bits	Name	Description
1	CLR_ON_MTCH_EN	When reset (0), the timer will not clear when it reaches the match value. When set (1), the timer will clear when it reaches the match value. 0x0: Don't clear timer 0x1: Clear timer
0	EN	When reset (0), the timer is disabled. When set (1), the timer is enabled and counts with frequency of timerO clock. 0x0: Disable timer 0x1: Enable timer

0x0006200C RPM_RPM_TMR0_CLR

Type: Write (Command)
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_TMR0_CLR register is a one-shot command register that, when written with any value, resets RPM TMR0 to a value of 0. This occurs regardless of the state of the RPM_TMR0_EN register.

RPM_RPM_TMR0_CLR

Bits	Name	Description
0	CLR	Data written is not used.

0x00062010 RPM_RPM_TMR0_CLK_CTL

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x3

The RPM_TMR0_CLK_CTL controls the clock divider inside RPM TMR0.

NOTE Due to the particular synchronization logic that the timer circuit uses, the timer clock should always run at least 4x slower than the AHB clock. So if both the AHB bus and XO are running at the same frequency, the RPM_TMR0_CLK_CTL register can be programmed to 3 to get the 4 to 1 divide ratio between bus clock and timer clock.

RPM_RPM_TMR0_CLK_CTL

Bits	Name	Description
1:0	DIV	0x3: 4 0x2: 3 0x1: 2 0x0: 1

0x00062040 RPM_RPM_TMR1_MTCH

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0000_0000

RPM TMR1 will signal interrupt when its counter value has reached the value stored in the RPM_TMR1_MTCH register.

RPM_RPM_TMR1_MTCH

Bits	Name	Description
31:0	MTCH	The value of RPM_TMR1_CNT at which an interrupt will be generated.

0x00062044 RPM_RPM_TMR1_CNT

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0000_0000

The RPM_TMR1_CNT register contains the current value of RPM TMR1. The current value can be set by software.

The count value is writable as a test/debug only feature. Writing this register ALSO changes the RPM_TMR1_MTCH register at the same time due to HW re-use. The procedure for writing the RPM_TMR1_CNT is as follows:

- Disable the timer by clearing the EN bit in RPM_TMR1_EN.
- Write RPM_TMR1_CNT.
- Write RPM_TMR1_MTCH, to restore match value.
- Enable the timer by setting the EN bit in RPM_TMR1_EN.

RPM_RPM_TMR1_CNT

Bits	Name	Description
31:0	CNT	The current value of the timer count

0x00062048 RPM_RPM_TMR1_EN

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_TMR1_EN register is used to enable the RPM TMR1.

RPM_RPM_TMR1_EN

Bits	Name	Description
1	CLR_ON_MTCH_EN	When reset (0), the timer will not clear when it reaches the match value. When set (1), the timer will clear when it reaches the match value. 0x0: Don't clear timer 0x1: Clear timer
0	EN	When reset (0), the timer is disabled. When set (1), the timer is enabled and counts with frequency of sleep clock. 0x0: Disable timer 0x1: Enable timer

0x0006204C RPM_RPM_TMR1_CLR

Type: Write (Command)
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_TMR1_CLR register is a one-shot command register that, when written with any value, resets RPM TMR1 to a value of 0. This occurs regardless of the state of the RPM_TMR1_EN register.

NOTE Since RPM TMR1 runs on sleep clock, the 4-to-1 minimum ratio between bus clock and timer clock is implicitly met and the RPM_TMR1_CLK_CTL register is not needed.

RPM_RPM_TMR1_CLR

Bits	Name	Description
0	CLR	Data written is not used.

0x00062060 RPM_RPM_WDOG_RESET

Type: Write
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_WDOG_RESET register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset watch dog. This command register also disables the watchdog freeze.

RPM_RPM_WDOG_RESET

Bits	Name	Description
0	WDOG_RESET	This bit generates the WDOG_STB during the non-sleep mode. A pulse is generated on WDOG_STB when this bit is written with a ’1’.

0x00062064 RPM_RPM_WDOG_FREEZE

Type: Write/Command
Clock: RPM_BUS_CLK
Reset State: 0x0

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

The RPM_WDOG_FREEZE register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the RPM_WDOG_RESET register.

RPM_RPM_WDOG_FREEZE

Bits	Name	Description
0	WDOG_FREEZE	This bit is used to freeze the watchdog timer at count 0. To enable the watchdog timer auto-kicker, write a '1'.

0x00062068 RPM_RPM_WDOG_UNMASKED_INT_EN

Type: Write/Command
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_WDOG_UNMASKED_INT_EN register enables unmasked IRQs and FIQs to enable the watch dog.

RPM_RPM_WDOG_UNMASKED_INT_EN

Bits	Name	Description
1	ENABLE	Enable wdog timer Do not enable wdog timer 0x1: enable 0x0: don't enable
0	UNMASKED_INT_ENABLE	Unmasked IRQ or FIQ will enable wdog timer Unmasked IRQ or FIQ will not enable wdog timer 0x1: enable 0x0: don't enable

0x0006206C RPM_RPM_WDOG_STATUS

Type: Read
Clock: RPM_BUS_CLK
Reset State: 0x4

The RPM_WDOG_STATUS register is the watchdog status register.

RPM_RPM_WDOG_STATUS

Bits	Name	Description
16:3	WDOG_COUNT	Counter value [13:0] of watch dog counter. Note: the sleep counter value is sampled using the rpm bus clk. Multiple reads are required to determine the value (assuming rpm bus clk is much faster than sleep clock)
2	WDOG_CNT_RESET_STATUS	Show the status of wdog_res signal (for test).

RPM_RPM_WDOG_STATUS (cont.)

Bits	Name	Description
1	WDOG_FROZEN	This bit indicates whether or not wdog is frozen at count '0'. 0x1: frozen 0x0: not frozen
0	WDOG_EXPIRED_STATUS	Watchdog timer has expired. Wdog timer has not expired. 0x1: expired 0x0: not expired

0x00062070 RPM_RPM_WDOG_EXPIRED_WIDTH

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0xC7C

The RPM_WDOG_EXPIRED_WIDTH register defines the width of the wdog_expired pulse in the number of sleep_clk cycles. The default value is 0x0C7C = 3196.

RPM_RPM_WDOG_EXPIRED_WIDTH

Bits	Name	Description
14	SYNC_STATUS	When set (1), the wdog expired width data is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STATUS bit is clear (0). This bit is read only.
13:0	DATA	Wdog counter value to de-assert the wdog_expired pulse. The wdog counter is14 bits.

0x00062074 RPM_RPM_WDOG_BARK_TIME

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x3FFF

The RPM_WDOG_BARK_TIME register defines the time in sleep_clk when to assert the watchdog ('bark') interrupts. The value can be between 1and 12787 (the time when the watchdog times out). The default value is 0x3FFF, which is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog ('bark') interrupt.

NOTE A bark time of 0x0 is not allowed.

RPM_RPM_WDOG_BARK_TIME

Bits	Name	Description
14	SYNC_STATUS	When set (1), the wdog bark time is synchronizing to the SLEEP_CLK. The data value is not guaranteed until the SYNC_STATUS bit is clear (0). This bit is read only.
13:0	DATA	The wdog counter value on which to trigger the bark interrupt

0x00062078 RPM_RPM_WDOG_TEST_LOAD_STATUS

Type: Read
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_WDOG_TEST_LOAD_STATUS register indicates when the watchdog test load is synchronizing to sleep_clk.

RPM_RPM_WDOG_TEST_LOAD_STATUS

Bits	Name	Description
0	SYNC_STATUS	When set (1) wdog test load is synchronizing to SLEEP_XTAL_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x0006207C RPM_RPM_WDOG_TEST_LOAD

Type: Write (Command)
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_WDOG_TEST_LOAD register loads the RPM_WDOG_TEST register value into the watchdog counter. Any write to this register, irrespective of the value written, will create a load pulse.

RPM_RPM_WDOG_TEST_LOAD

Bits	Name	Description
0	LOAD	

0x00062080 RPM_RPM_WDOG_TEST

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_WDOG_TEST register indicates that the watchdog test is synchronizing to sleep_clk and contains the watchdog counter test load value.

RPM_RPM_WDOG_TEST

Bits	Name	Description
14	SYNC_STATUS	When set (1), the watchdog test is synchronizing to SLEEP_ XTAL_CLK. The data value is not guaranteed until the SYNC_STATUS bit is clear (0).
13:0	LOAD_VALUE	The watchdog counter test load value [13:0]. The watchdog counter is 14 bits.

0x00062100 RPM_RPM_TMR_STS

Type: Read
Clock: RPM_BUS_CLK
Reset State: 0x0000_0000

The RPM_TMR_STS can be used to determine the status of each of the RPM timers in the timer's resident clock domain. Since the timer clock domain may be much slower than the AHB clock, AHB transactions may be delayed in taking effect. This information can be used to qualify other actions or used simply for debug purposes. For example, software can determine when a write to RPM_TMR0_CLR has taken effect by examining the TMR0_CLR_PEND bit.

RPM_RPM_TMR_STS

Bits	Name	Description
17	WDOG_EN	Wdog enable
16	WDOG_UNMASKED_INT_E N	An unmasked interrupt will enable the timer (1) or not (0)
15:12	RESERVED_BITS15_12	
11	TMR1_WR_PEND	Timer has a write pending (1) or not (0)
10	TMR1_CLR_PEND	Timer has a clear pending (1) or not (0)
9	TMR1_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
8	TMR1_EN	Timer is enabled (1) or not (0)
7:4	RESERVED_BITS7_4	
3	TMR0_WR_PEND	Timer has a write pending (1) or not (0)

RPM_RPM_TMR_STS (cont.)

Bits	Name	Description
2	TMR0_CLR_PEND	Timer has a clear pending (1) or not (0)
1	TMR0_CLR_ON_MTCH	Timer will reset (1) or hold (0) when it reaches the match value
0	TMR0_EN	Timer is enabled (1) or not (0)

17.5 RPM General Purpose Registers (0x00000000 RPM_BASE)

This section contains RPM general purpose control and status registers.

17.5.1 RPM general purpose control and status registers

The RPM GP CSR block, as the name implies, houses general purpose control and status registers. These include registers related to enabling power saving as well as registers to set RPM general purpose outputs. Test mux control as well as RPM code RAM FS CGC control registers also reside in this block.

Only word accesses are supported to these registers.

17.5.1.1 RPM GP CS registers

0x00063000 RPM_RPM_BUS_CLK_FORCE_ON

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_BUS_CLK_FORCE_ON register provides a way to force the RPM bus_clk on irrespective of a write to RPM_PROC_BUS_CLK_OFF_CTL.

NOTE A write to RPM_BUS_CLK_FORCE_ON cannot be immediately followed by a write to RPM_PROC_BUS_CLK_OFF_CTL in the very next cycle, otherwise bus clock will not stay ON.

RPM_RPM_BUS_CLK_FORCE_ON

Bits	Name	Description
0	BUS_CLK_FORCE_ON	Programming this bit to 0 has no affect on bus clk Programming this bit to 1 will force bus clock ON irrespective of a write to RPM_PROC_BUS_CLK_OFF_CTL register. 0x0: No Affect 0x1: Clock ON

0x00063004 RPM_RPM_PROC_BUS_CLK_OFF_CTL

Type: Write (Command)
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_PROC_BUS_CLK_OFF_CTL register provides a way to turn off RPM processor, and bus clocks and clock to the RPM sFPB master interface, when these clocks are not needed.

The CLK_OFF bits are inverted to create CLKON request signals to the clock control block.

NOTE Any write to this register, irrespective of the value written, will turn off rpm processor clock and clock to the RPM sFPB master interface. The bus clock will also be turned off by a write to this register, if RPM_BUS_CLK_FORCE_ON register hasn't already been programmed to force the bus clk ON.

RPM_RPM_PROC_BUS_CLK_OFF_CTL

Bits	Name	Description
0	PROC_BUS_CLK_OFF	Turn OFF RPM processor/bus/sFPB interface clocks.

0x00063008 RPM_RPM_TIMERS_CLK_OFF_CTL

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x3

The RPM_TIMERS_CLK_OFF_CTL register provides a way to turn off clock to RPM gp and wdog timers when they are not needed.

The CLK_OFF bits are inverted to create CLKON request signals to the clock control block.

NOTE Both TIMER1 and WDOG timer have sleep clock as their clock source. TIMER1_CLK_OFF and WDOG_TIMER_CLK_OFF provide a means to locally gate off sleep clock to TIMER1 and WDOG timer respectively.

NOTE Please refer to the clock control block SWI for details on how to enable/disable RPM timer0 as well as rpm sleep clock.

RPM_RPM_TIMERS_CLK_OFF_CTL

Bits	Name	Description
1	WDOG_TIMER_CLK_OFF	RPM wdog timer clock should keep running. Turn OFF RPM wdog timer clock. 0x0: Clock ON 0x1: Clock OFF
0	TIMER1_CLK_OFF	RPM timer1 clock should keep running. Turn OFF RPM timer1 clock. 0x0: Clock ON 0x1: Clock OFF

0x0006300C RPM_RPM_SW_DONE

Type: Write (Command)
Clock: RPM_BUS_CLK
Reset State: 0x0

THe RPM_SW_DONE register provides a means to signal to MPM that it is safe to initiate sleep mode.

NOTE Writing to RPM_SW_DONE, in addition to creating the sw_done pulse, will also turn off rpm_proc_clk, rpm_bus_clk, and rpm_sfpb_clk. SW needs to make sure that clocks to RPM timers have been turned off (by writing to RPM_TIMERS_CLK_OFF) prior to writing to the SW_DONE register.

RPM_RPM_SW_DONE

Bits	Name	Description
0	SW_DONE	

0x00063020+ 0x4*n RPM_RPM_GPO_WDATAn, n=[0..1]

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x00000000

The RPM_GPO_WDATA register is used to set the corresponding RPM GPO outputs high or low, based on the value written to it.

RPM_RPM_GPO_WDATAn

Bits	Name	Description
31:0	WDATA	Load or read the Write Data register.

0x00063040+ 0x4*n RPM_RPM_GPO_WDSETn, n=[0..1]

Type: Write
Clock: RPM_BUS_CLK
Reset State: NA

The RPM_GPO_WDSET register provides a way to individually set RPM_ GPO_WDATA bits.

RPM_RPM_GPO_WDSETn

Bits	Name	Description
31:0	WDSET	Set bits in the Write Data register. For each bit in the GPO bus, (Don't set corresponding bit in RPM_GPO_WDATA) (Set corresponding bit in RPM_GPO_WDATA) 0x0: Don't set 0x1: Set

0x00063060+ 0x4*n RPM_RPM_GPO_WDCLRn, n=[0..1]

Type: Write
Clock: RPM_BUS_CLK
Reset State: NA

The RPM_GPO_WDCLR register provides a way to individually clear RPM_GPO_WDATA bits.

RPM_RPM_GPO_WDCLRn

Bits	Name	Description
31:0	WDCLR	Clear bits in the Write Data register. For each bit in the GPO bus, (Don't clear corresponding bit in RPM_GPO_WDATA) (Clear corresponding bit in RPM_GPO_WDATA) 0x0: Don't clear 0x1: Clear

0x00063080 RPM_RPM_TEST_BUS_SEL

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_TEST_BUS_SEL register selects RPM test bus contents.

NOTE For RPM AHB test bus, SFPB_CTRL_STATUS needs to be configured in addition to RPM_TEST_BUS_SEL.

RPM_RPM_TEST_BUS_SEL

Bits	Name	Description
31	B_0X00000000	0x55555555
30	B_1	
29	B_1	

RPM_RPM_TEST_BUS_SEL (cont.)

Bits	Name	Description
28	B_1	
27	B_1	
26	B_1	
25	B_1	
24	B_1	
23	B_1	
22	B_1	
21	B_1	
20	B_1	
19	B_1	
18	B_1	
17	B_1	
16	B_1	
15	B_1	
14	B_1	
13	B_1	
12	B_1	
11	B_1	
10	B_1	
9	B_1	
8	B_1	
7	B_1	
6	B_1	
5	B_1	
4	B_1	
3	B_1	

RPM_RPM_TEST_BUS_SEL (cont.)

Bits	Name	Description
2:0	VAL	0x4:: RPM peripherals test bus Selects RPM peripherals (csr, timers, int_ctrl) test bus. Selects RPM AHB test bus. Selects 0xAAAAAAAA Selects 0x55555555 Selects 0x00000000 0x7: Reserved_7 0x6: Reserved_6 0x5: Reserved_5 0x3: RPM AHB test bus 0x1: All A 0x1: All 5 0x0: All 0
2	B_1	
1	B_1	
0	B_1	

0x0006308C RPM_RPM_CODE_RAM_FS_CTL

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0xF

The RPM_CODE_RAM_FS_CTL register provides software override of RPM code RAM core/periphery foot switch controls.

NOTE Memory core/periphery foot switches are forced ON by default. This register needs to be programmed appropriately to get the full benefits of memory power down.

RPM_RPM_CODE_RAM_FS_CTL

Bits	Name	Description
3	GRP1_FORCE_CORE_ON	This bit provides software override of core FS control (slp_nret_n) for code RAM 64KB- 128KB. 0x1: RAM core forced ON 0x0: RAM core not forced ON
2	GRP1_FORCE_PERPH_ON	This bit provides software override of periphery FS control (slp_ret_n) for code RAM 64KB- 128KB. 0x1: RAM periphery forced ON 0x0: RAM periphery not forced ON

RPM_RPM_CODE_RAM_FS_CTL (cont.)

Bits	Name	Description
1	GRP0_FORCE_CORE_ON	This bit provides software override of core FS control (slp_nret_n) for code RAM 0KB - 64KB. 0x1: RAM core forced ON 0x0: RAM core not forced ON
0	GRP0_FORCE_PERPH_ON	This bit provides software override of periphery FS control (slp_ret_n) for code RAM 0KB - 64KB. 0x1: RAM periphery forced ON 0x0: RAM periphery not forced ON

0x00063090 RPM_RPM_CODE_RAM_FS_AHALT_CTL

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_CODE_RAM_FS_AHALT_CTL register provides software a means to halt clock to RPM code RAM FS CGCs.

This register also provides a means to put the memory core/periphery in sleep mode, if they are not forced ON via bits in RPM_CODE_RAM_FS_CTL register.

RPM_RPM_CODE_RAM_FS_AHALT_CTL

Bits	Name	Description
1	GRP1_ASYNC_HALT	This bit asserts/de-asserts asynchronous clock halt signal to the FS CGC for code RAM 64KB - 128KB. 0x1: Halt clock 0x0: Enable clock
0	GRP0_ASYNC_HALT	This bit asserts/de-asserts asynchronous clock halt signal to FS CGC for code RAM 0KB - 64KB. 0x1: Halt clock 0x0: Enable clock

0x00063094 RPM_RPM_CODE_RAM_FS_WS_CTL

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0xF

The RPM_CODE_RAM_FS_WS_CTL register controls the number of cycles before the code RAM goes to sleep or wakes-up.

For sleep, the output clock is gated off immediately while the sleep signals are asserted low only after s clock cycles.

For wake-up, the sleep signals are de-asserted immediately while the clock starts toggling only after w wake-up clock cycles.

RPM_RPM_CODE_RAM_FS_WS_CTL

Bits	Name	Description
3:0	GRP_W_S_VAL	These bits control the number of clock cycles for the RAM to go to sleep or wake-up from sleep. 0x0: Clocks - 0 0x1: Clocks - 1 0x2: Clocks - 2 0x3: Clocks - 3 0x4: Clocks - 4 0x5: Clocks - 5 0x6: Clocks - 6 0x7: Clocks - 7 0x8: Clocks - 8 0x9: Clocks - 9 0xA: Clocks - 10 0xB: Clocks - 11 0xC: Clocks - 12 0xD: Clocks - 13 0xE: Clocks - 14 0xF: Clocks - 15

0x00063098 RPM_RPM_CODE_RAM_FS_CLK_STATUS

Type: Read
Clock: RPM_BUS_CLK
Reset State: 0x0

The RPM_CODE_RAM_FS_CLK_STATUS register provides status information about the clock at the output of RPM code RAM FS CGCs.

RPM_RPM_CODE_RAM_FS_CLK_STATUS

Bits	Name	Description
1	GRP1_CLOCK_STATUS	0x1: Clock OFF 0x0: Clock ON
0	GRP0_CLK_STATUS	0x1: Clock OFF 0x0: Clock ON

17.6 RPM XPU Registers (0x00000000 RPM_BASE)

This section contains the RPM XPU registers.

17.6.1 RPM AHB SS

RPM AHB SS is a wrapper around system_fpb. It consists of a 2x3 SFPB_v2 bus and a 2x6 SFPB based RPM local AHB bus.The sections below list the software interface for the two SFPBs in RPM AHB SS, the XPU in the 2x6 bus and the M2VMT in the 2x3 bus.

17.6.1.1 RPM XPU registers

The RPM local AHB(2x6) bus has an XPU configured as an APU that protects slaves 0,1,2 & 3. Slaves 4 & 5 are protected via ACR registers.

NOTE An RPM_ prefix is expected in the ARM_ADDRESS_FILE.flat for these registers, so they do not collide with other APUs used in the system.

0x00064000+ 4*n RPM_APU_RGn_RACR, n=[0..3]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type APU. These registers include a single bit per VMID granting read access.

RPM_APU_RGn_RACR

Bits	Name	Description
31:0	RE	Read enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read access to the registers in the associated resource group.

0x00064400+ 4*n RPM_APU_RGn_WACR, n=[0..3]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

These registers exist only for the case when APU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type APU.

RPM_APU_RGn_WACR

Bits	Name	Description
31:0	WE	Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID write access to the registers in the associated resource group.

0x00064F80 RPM_APU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

RPM_APU_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set APU_ESR. APU_EAR and APU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set APU_ESR. APU_EAR and APU_ESYNR0 updated with address and syndrome of error.
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x00064F84 RPM_APU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port.

RPM_APU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x00064F88 RPM_APU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the APU_ESYNRn registers, which are merely the 'syndrome' of an error indicated by APU_ESR.

RPM_APU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) 'lock' upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x00064F8C RPM_APU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

RPM_APU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) 'lock' upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x00064F90 RPM_APU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

RPM_APU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x00064F94 RPM_APU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

RPM_APU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x00064FF4 RPM_APU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

RPM_APU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x00064FF8 RPM_APU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x00001C03

APU ID Register: Read-only register that defines various configuration attributes of the APU instance.

RPM_APU_IDR

Bits	Name	Description
31:29	RESERVED31_21	Reserved
28:24	MSB	Indicates most significant address bit number used to select a resource group
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved

RPM_APU_IDR (cont.)

Bits	Name	Description
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only 'owner' VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit 'owner' VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.
9	RESERVED9	Reserved
8:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

0x00064FFC RPM_APU_APU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

APU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the APU (including the APU_APU_ACR itself).

RPM_APU_APU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the APU's 4KB address region (including the APU_APU_ACR itself). For single VMID type APUs (APU_IDR[MV] = 0) the APU_APU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

17.7 RPM 2x3 System FPB Registers (0x00000000 RPM_BASE)

This section contains RPM 2x3 System FPB registers.

17.7.1 RPM AHB SS

RPM AHB SS is a wrapper around system_fpb. It consists of a 2x3 SFPB_v2 bus and a 2x6 SFPB based RPM local AHB bus.The sections below list the software interface for the two SFPBs in RPM AHB SS, the XPU in the 2x6 bus and the M2VMT in the 2x3 bus.

17.7.1.1 RPM AHB 2x6 registers

Table 1-11 lists the differences between the standard system FPB SW interface and system FPB SW interface as it corresponds to RPM local AHB bus. The changes in the SW interface are due to RPM customization of system FPB (via generics) for use as its local AHB bus.

Table 17-10 System FPB SWI changes for RPM

Register	Change for RPM
SFPB_CTRL_STATUS	No change.
SFPB_AHB2AHB_CFG_Ma, a=[0..15]	Removed. Since RPM local AHB does not instantiate an AHB2AHB bridge on any of its master interfaces, this register will not be generated.
SFPB_PORT_EN	Size reduced from 16 bits to 2 bits, since RPM local AHB has only 2 masters.
SFPB_AHB2AHB_CFG_Sa, a=[0..1]	Removed. Sa_Ma interfaces are used as slave interfaces on RPM local AHB without any AHB2AHB bridge, so these registers will not be generated.
SFPB_ERROR_STAT	No change.
SFPB_ERROR_ADDR	No change.
SFPB_GPREG	Size changed from 16 bits to 1 bit. RPM local AHB does not need this register, so it sets the generic that controls the size of this register to 1, which is the minimum allowed size.
SFPB_XPU_ACR	No change.
SFPB_HW_CLK_GATING_CFG	Removed. RPM sets the ENABLE_HW_CLK_GATING generic to 0, so this register is not generated.

NOTE An RPM_2x3 prefix is expected in the ARM_ADDRESS_FILE.flat for these registers, so they do not collide with other system FPBs used in the system.

0x00068000 RPM_SFPB_CTRL_STATUS

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0000

The SFPB_CTRL_STATUS register is a general configuration register.

RPM_SFPB_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables NOTE Power up value is clear (0)
11	RPM_ARM7_IRQ_EN	SW: RW, HW: R ARM7InterruptEnable When set, the ARM7 receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	SC_IRQ_EN	SW: RW, HW: R Scorpion Interrupt Enable When set, the Scorpion receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

RPM_SFPB_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x5: Select the S0_M0 ahb2ahb bridge test bus. 0x6: Select the S1_M1 ahb2ahb bridge test bus. 0x7: Select the M0 ahb2ahb bridge test bus. 0x8: Select the M1 ahb2ahb bridge test bus. 0x9: Select the M2 ahb2ahb bridge test bus. 0xA: Select the M3 ahb2ahb bridge test bus. 0xB: Select the M4 ahb2ahb bridge test bus. 0xC: Select the M5 ahb2ahb bridge test bus. 0xD: Select the M6 ahb2ahb bridge test bus. 0xE: Select the M7 ahb2ahb bridge test bus. 0xF: Select the M8 ahb2ahb bridge test bus. 0x10: Select the M9 ahb2ahb bridge test bus. 0x11: Select the M10 ahb2ahb bridge test bus. 0x12: Select the M11 ahb2ahb bridge test bus. 0x13: Select the M12 ahb2ahb bridge test bus. 0x14: Select the M13 ahb2ahb bridge test bus. 0x15: Select the M14 ahb2ahb bridge test bus. 0x16: Select the M15 ahb2ahb bridge test bus.

0x00068044 RPM_SFPB_PORT_EN

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x3

The SFPB_PORT_EN register is a SFPB master port enable register.

RPM_SFPB_PORT_EN

Bits	Name	Description
31:2	RESERVED_BIT31_2	

RPM_SFPB_PORT_EN (cont.)

Bits	Name	Description
1	M1_PORT_EN	SW: RW, HW: R M1PortEnable When cleared (0), M1 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)
0	M0_PORT_EN	SW: RW, HW: R M0PortEnable When cleared (0), M0 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

0x00068050 RPM_SFPB_ERROR_STAT

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000000

The SFPB_ERROR_STAT register is the bus error status register.

RPM_SFPB_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the DM channel ID that caused the detected error when the DM is the master of the access. If the DM is not the master of the access, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Applications DM 0x1: MDP 0x2: ARM9 0x3: ARM11 0x4: ADSP

RPM_SFPB_ERROR_STAT (cont.)

Bits	Name	Description
11:10	RESERVED_BITS11_10	
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit
3:2	RESERVED_BIT3_2	
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted based on PBUS_IRQ_EN settings. Clearing (0) this bit clears any interrupts asserted as well as enables the PBUS_ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x00068054 RPM_SFPB_ERROR_ADDR

Type: Read
Clock: CC_SFPB_CLK
Reset State: 0x00000000

The SFPB_ERROR_ADDR register contains the bus error address.

RPM_SFPB_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when PBUS_ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x00068058 RPM_SFPB_GPREG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0

The SFPB_GPREG register is a configurable general purpose register.

RPM_SFPB_GPREG

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	GPREG_CONTENT	SW: RW, HW: W GpregContent User defines the content of this register. The size of this register is defined by the generic-SFPB_GPREG_SIZE (1 - 32 bits). Power up value is clear (0)

0x0006805C RPM_SFPB_XPU_ACR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFFFFFF

The SFPB_XPU_ACR register is a SFPB Access Control Register for configure register protection.

RPM_SFPB_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R M15PortEnable SFPB XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the SFPB configure space, including this register itself. Power up value is set (1)

17.7.1.2 RPM AHB 2x3 registers

This table lists the differences between the standard systemFPB SW interface and system FPB SW interface as it corresponds to RPM 2x3 splitter. The changes in the SW interface are due to RPM customization of system FPB (via generics) for use as a 2x3 arbiter to direct traffic from ARM7/TIC/JTAG2AHB or COresight DAP to either the local AHB bus, chip systemFPB, or chip FABRIC.

Table 17-11 System FPB SWI changes for RPM

Register	Change for RPM
SFPB_CTRL_STATUS	No change.
SFPB_AHB2AHB_CFG_Ma, a=[0..15]	Removed. Since RPM 2x3 arbiter does not instantiate an AHB2AHB bridge on its single master interface, this register will not be generated.
SFPB_PORT_EN	Size reduced from 16 bits to 2 bits, since the RPM 2x3 arbiter has only 2 masters.
SFPB_AHB2AHB_CFG_Sa, a=[0..1]	Removed. The Sa_Ma interfaces in RPM 2x3 arbiter do not instantiate any AHB2AHB bridges, so this register will not be generated.
SFPB_ERROR_STAT	No change.
SFPB_ERROR_ADDR	No change.
SFPB_GPREG	Size changed from 16 bits to 1 bit. RPM 2x3 arbiter does not need this register, so it sets the GENERIC that controls the size of this register to 1, which is the minimum allowed size.
SFPB_XPU_ACR	No change.
SFPB_HW_CLK_GATING_CFG	Removed. RPM sets the ENABLE_HW_CLK_GATING generic to 0, so this register will not be generated.

NOTE An RPM_2x3 prefix is expected in the ARM_ADDRESS_FILE.flat for these registers, so they do not collide with other system FPBs used in the chip.

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0x00068000 RPM_SFPB_CTRL_STATUS

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0000

The SFPB_CTRL_STATUS register is a general configuration register.

NOTE The XPU_EN bit should never be set for RPM. Security needs to be set external to RPM (example systemFPB level). RPM should only receive secure accesses.

RPM_SFPB_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables Power up value is clear (0) NOTE This bit should never be set for RPM. Setting to 1 will result in unpredictable behavior.
11	RPM_ARM7_IRQ_EN	SW: RW, HW: R ARM7InterruptEnable When set, the ARM7 receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	SC_IRQ_EN	SW: RW, HW: R Scorpion Interrupt Enable When set, the Scorpion receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

RPM_SFPB_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x5: Select the S0_M0 ahb2ahb bridge test bus. 0x6: Select the S1_M1 ahb2ahb bridge test bus. 0x7: Select the M0 ahb2ahb bridge test bus. 0x8: Select the M1 ahb2ahb bridge test bus. 0x9: Select the M2 ahb2ahb bridge test bus. 0xA: Select the M3 ahb2ahb bridge test bus. 0xB: Select the M4 ahb2ahb bridge test bus. 0xC: Select the M5 ahb2ahb bridge test bus. 0xD: Select the M6 ahb2ahb bridge test bus. 0xE: Select the M7 ahb2ahb bridge test bus. 0xF: Select the M8 ahb2ahb bridge test bus. 0x10: Select the M9 ahb2ahb bridge test bus. 0x11: Select the M10 ahb2ahb bridge test bus. 0x12: Select the M11 ahb2ahb bridge test bus. 0x13: Select the M12 ahb2ahb bridge test bus. 0x14: Select the M13 ahb2ahb bridge test bus. 0x15: Select the M14 ahb2ahb bridge test bus. 0x16: Select the M15 ahb2ahb bridge test bus.

0x00068044 RPM_SFPB_PORT_EN

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x3

The SFPB_PORT_EN register is a SFPB master port enable register.

RPM_SFPB_PORT_EN

Bits	Name	Description
31:2	RESERVED_BIT31_2	

RPM_SFPB_PORT_EN (cont.)

Bits	Name	Description
1	M1_PORT_EN	SW: RW, HW: R M1PortEnable When cleared (0), M1 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)
0	M0_PORT_EN	SW: RW, HW: R M0PortEnable When cleared (0), M0 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

0x00068050 RPM_SFPB_ERROR_STAT

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000000

The SFPB_ERROR_STAT register is the bus error status register.

RPM_SFPB_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the DM channel ID that caused the detected error when the DM is the master of the access. If the DM is not the master of the access, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Applications DM 0x1: MDP 0x2: ARM9 0x3: ARM11 0x4: ADSP

RPM_SFPB_ERROR_STAT (cont.)

Bits	Name	Description
11:10	RESERVED_BITS11_10	
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit
3:2	RESERVED_BIT3_2	
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted based on PBUS_IRQ_EN settings. Clearing (0) this bit clears any interrupts asserted as well as enables the PBUS_ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x00068054 RPM_SFPB_ERROR_ADDR

Type: Read
Clock: CC_SFPB_CLK
Reset State: 0x00000000

The SFPB_ERROR_ADDR register contains the bus error address.

RPM_SFPB_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when PBUS_ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x00068058 RPM_SFPB_GPREG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0

The SFPB_GPREG register is a configurable general purpose register.

RPM_SFPB_GPREG

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	GPREG_CONTENT	SW: RW, HW: W GpregContent User defines the content of this register. The size of this register is defined by the generic-SFPB_GPREG_SIZE (1 - 32 bits). Power up value is clear (0)

0x0006805C RPM_SFPB_XPU_ACR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFFFFFF

The SFPB_XPU_ACR register is a SFPB Access Control Register for configure register protection.

NOTE The XPU_EN bit in SFPB_CTRL_STATUS register should never be set for RPM. This register, therefore, will never be needed since it is used only when the XPU_EN bit is set.

RPM_SFPB_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R M15PortEnable SFPB XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the SFPB configure space, including this register itself. Power up value is set (1)

17.7.1.2.1 M2VMT (hmaster index) registers

The M2VMT block is part of the system_fpb_v2 2 x3 bus. The mapper is a 2 entry mapper, but only one entry of the mapper is used for VMID generation - this is port M0 on which ARM7/TIC/JTAG2AHB can be masters (mutually exclusive). Port M1 of the 2x3 is configured as a link master, so the incoming VMID is passed through and the port ID is NOT used to index into the M2VMT to generate a VMID.

0x00069000+ 0x4*n RPM_SFPB_M2VMT_M2VMRn, n=[0..1]

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where n = NUM_M2VMT_ENTRIES from the design generics and we map NUM_M2VMT_ENTRIES to NUM_MASTERS.

NOTE Although the M2VMT hardware is configured for 2 VMID mapper entries, only one of the register's(SFPB_M2VMT_M2VMR0) VMID entry is actually used. This is for the M0 port on which either ARM7/TIC/JTAG2AHB can be masters.

RPM_SFPB_M2VMT_M2VMRn

Bits	Name	Description
31:5	RESERVED	
4:0	VMID	Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRn address associations. n = NUM_M2VMT_ENTRIES from the design generic/parameter.

0x00069F80 RPM_SFPB_M2VMT_CR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: xxx0

Global configuration register.

Special Note: When REMOVE_M2VMT_RPU = ’1’, this register is not available. Also, bit [2], is not valid or has no effect when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT =‘1’.

RPM_SFPB_M2VMT_CR

Bits	Name	Description
31:4	RESERVED	
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., in valid addresses) are recorded as such. Decode error is asserted when config access to un-implemented and/or unmapped register/address are done. Also, note that decode error is never asserted for client port accesses. When value is set to ’0’ i.e., ’do not record’, decode errors do not set the M2VMT_ESR[CFG], and M2VMT_EAR & M2VMT_SYNRn is not updated. When value is set to ’1’, i.e., ’record’, decode errors set M2VMT_ESR[CFG] and M2VMT_EAR & M2VMT_SYNRn is updated with the address and the syndrome of the error. Reset State: x
2	RPUEIE	RPU error interrupt Enable: When set, configuration port errors are reported directly to the interrupt controller via the M2VMT_intr, interrupt output signal. Interrupt output is asserted if M2VMT_CR[RPUIE_EN] is ’1’ and ANY bit is set in the M2VMT_ESR register. Special Note: Not valid or has no effect on the interrupt when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT=’1’. Reset State: x
1	RPUERE	RPU error report enable: When set, M2VMT reports configuration port errors to the requesting bus master, according to the respective port’s bus protocol. All error types reported via CRIF port will use a decode error, rather than a slave error. Regardless of the value of this field, both configuration port errors are terminated by the M2VMT as RAZ/WI, and are recorded in M2VMT_ESR register. Reset State: X

RPM_SFPB_M2VMT_CR (cont.)

Bits	Name	Description
0	RPUE	RPU Enable: Governs whether M2VMT_RPU_ACR is enabled to check the VMID of the configuration request. When set, all configuration port accesses are checked against M2VMT_RPU_ACR register for access permissions. It's cleared by reset. Set once SROT configures MID->VMID mapping tables Reset State: 0

0x00069F84 RPM_SFPB_M2VMT_EAR

Type: Read
Clock: CC_SFPB_CLK
Reset State: unknown

When there is an error, this register holds the physical address of the errant transaction.

RPM_SFPB_M2VMT_EAR

Bits	Name	Description
31:0	PA	M2VMT Error Address Register: Physical address[31:0]. Contains the physical address of the errant request. Based on implementation, it may not contain the full 32 bits of the address. Captures the address on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. Special Note: When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT = '1', this register is not available and therefore access to this register are treated as RAZ/WI.

0x00069F88 RPM_SFPB_M2VMT_ESR

Type: Read/Write to clear
Clock: CC_SFPB_CLK
Reset State: Undefined

M2VMT Error Status Register:

Captures the status upon M2VMT configuration errors, as determined by the M2VMT_RPU_ACR.

This register has read/write-clear access, meaning that reads simply provide a value in the register, while writes are performed by clearing those bits corresponding to '1's in the value written data, and leaving unchanged those bits corresponding to 0s n the written data. This prevents inadvertent

clearing of new errors when writing the register to clear an old error. A write with a ’1’ set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

The presence of an asserted value on any bit in this register is what prompts the assertion when enabled by M2VMT_CR[RPUEIE] of the M2MVT’s interrupt output. Therefore these bits must be cleared by the interrupt handler. This is contrasted with the fields in the M2VMT_ESYNRn register, which are merely the ’syndrome’ of an error indicated by the M2VMT_ESR.

For M2VMT, there is only one defined error status bit in the M2VMT_SER (actually two, if you count multi-error).

RPM_SFPB_M2VMT_ESR

Bits	Name	Description
31	MULTI	Multi-Error: When set to ’1’, indicates that an additional error occurred while M2VMT_ESR is non-zero. The M2VMT_EAR,M2VMT_ESYNRn and M2VMT_ESR registers (with the exception of this bit) lock on the first error, and must be cleared to unlock. Therefore, the status and the syndrome of errors that occurred while M2VMT_ESR[CFG] is ’1’ are lost, i.e., syndrome register and status register stores only details of the first error.
30:1	RESERVED	
0	CFG	Configuration Port Error: When set to ’1’, indicates an error associated with a configuration port request. **NOTE** When REMOVE_M2VMT_RPU=’1’ OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT=’1’, this register is not available and therefore access to this register is treated as RAZ/WI.

0x00069F8C RPM_SFPB_M2VMT_ESRRESTORE

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: unknown

RPM_SFPB_M2VMT_ESRRESTORE

Bits	Name	Description
31:0	M2VMT_ESRRTORE	M2VMT Error Status Register Restore This is just an aliased address for M2VMT_ESR, which provides direct write access (rather than write-clear) for restoration purpose Special Note: When REMOVE_M2VMT_RPU=’1’ OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT=’1’, this register is not available and therefore access to this register is treated as RAZ/WI.

0x00069F90 RPM_SFPB_M2VMT_ESYNR0

Type: Read
Clock: CC_SFPB_CLK
Reset State: undefined

Error Syndrome Register 0:

Captures the syndrome on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) 'lock' upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., the syndrome register and the status register stores only details of the first error.

RPM_SFPB_M2VMT_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request.
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request.
15:0	AMID	AMID[15:0] field of errant request. Special Note: When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT="1", this register is not available and therefore access to this register is treated as RAZ/WI.

0x00069F94 RPM_SFPB_M2VMT_ESYNR1

Type: Read
Clock: CC_SFPB_CLK
Reset State: Undefined

Error Syndrome Register 1:

Captures syndrome upon M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) 'lock' upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost. That is, the syndrome register and the status register only stores details of the first error.

RPM_SFPB_M2VMT_ESYNR1

Bits	Name	Description
31	DCD	Decode: Indicates configuration port error due to invalid/ unrecognized/ unmapped/ un-implemented address (e.g., a reserved register address). Includes decode errors within the global address space. Also, note that decode error is never asserted for client port accesses.
30	AC	Access control: Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED_1	
24	AFULL	AFULL field of the errant request
23	AOOOWR	AOOOWR field of the errant request
22	AOOORD	AOOORD field of the errant request.
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request).
19	RESERVED_2	
18:16	ASIZE	ASIZE[2:0] field of the errant request).
15:12	ALEN	ALEN[3:0] field of the errant request.
11:10	ABURST	ABURST[1:0] field of the errant request.
9	RESERVED	
8	AWRITE	AWRITE field of the errant request.
7	AINST	AINST field of the errant request.
6	APROTNS	APROTNS field of the errant request.
5	APRIV	APRIV field of the errant request.
4	AINNERSHARED	AINNERSHARED field of the errant request.
3	ASHARED	ASHARED field of the errant request.
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request. **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this registers is treated as RAZ/WI.

0x00069FF4 RPM_SFPB_M2VMT_REV

Type: Read
Clock: CC_SFPB_CLK
Reset State: ’10000000’b

Reports the revision information for the M2VMT core and wrapper.

RPM_SFPB_M2VMT_REV

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	Major variant field APQ8064: MAJOR = 0001
3:0	MINOR	Minor variant field. MINOR = 0000

0x00069FF8 RPM_SFPB_M2VMT_IDR

Type: Read
Clock: CC_SFPB_CLK
Reset State: 0x2

Reports the size of the M2VMT table. It is a read-only register.

RPM_SFPB_M2VMT_IDR

Bits	Name	Description
31:9	RESERVED	
8:0	M2VMTSIZE	.M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping. M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

0x00069FFC RPM_SFPB_M2VMT_RPU_ACR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: Undefined

Using the incoming VMID, this register controls access to the global register space.

RPM_SFPB_M2VMT_RPU_ACR

Bits	Name	Description
31:0	RWE	M2VMT local RPU Access control Register. Each bit position corresponds to a VMID. When set to ’1’, that VMID is granted VMID read/write access to the entire block of registers within the M2VMT’s 4KB global address space, including this register itself. In practice, this register designates the VMID(s) that can act as SROT (e.g., scorpion-secure) or pseudo SROT (e.g. RPM ARM11). Special Note: When REMOVE_M2VMT_RPU=’1’, this register is not available and therefore access to this register is treated as RAZ/WI.

17.8 RPM System FPB Registers (0x00000000 RPM_BASE)

This section contains RPM System FPB registers.

17.8.1 RPM AHB SS

RPM AHB SS is a wrapper around system_fpb. It consists of a 2x3 SFPB_v2 bus and a 2x6 SFPB based RPM local AHB bus.The sections below list the registers for the two SFPBs in RPM AHB SS, the XPU in the 2x6 bus and the M2VMT in the 2x3 bus.

17.8.1.1 RPM AHB 2x6 registers

Table 1-11 lists the differences between the standard system FPB SW interface and system FPB SW interface as it corresponds to RPM local AHB bus. The changes in the SW interface are due to RPM customization of system FPB (via generics) for use as its local AHB bus.

Table 17-12 System FPB SWI changes for RPM

Register	Change for RPM
SFPB_CTRL_STATUS	No change.
SFPB_AHB2AHB_CFG_Ma, a=[0..15]	Removed. Since RPM local AHB does not instantiate an AHB2AHB bridge on any of its master interfaces, this register will not be generated.
SFPB_PORT_EN	Size reduced from 16 bits to 2 bits, since RPM local AHB has only 2 masters.
SFPB_AHB2AHB_CFG_Sa, a=[0..1]	Removed. Sa_Ma interfaces are used as slave interfaces on RPM local AHB without any AHB2AHB bridge, so these registers will not be generated.
SFPB_ERROR_STAT	No change.
SFPB_ERROR_ADDR	No change.
SFPB_GPREG	Size changed from 16 bits to 1 bit. RPM local AHB does not need this register, so it sets the generic that controls the size of this register to 1, which is the minimum allowed size.
SFPB_XPU_ACR	No change.
SFPB_HW_CLK_GATING_CFG	Removed. RPM sets the ENABLE_HW_CLK_GATING generic to 0, so this register is not generated.

NOTE An RPM_2x3 prefix is expected in the ARM_ADDRESS_FILE.flat for these registers, so they do not collide with other system FPBs used in the system.

0x0006C000 RPM_SFPB_CTRL_STATUS

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0000

The SFPB_CTRL_STATUS register is a general configuration register.

RPM_SFPB_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables NOTE Power up value is clear (0)
11	RPM_ARM7_IRQ_EN	SW: RW, HW: R ARM7InterruptEnable When set, the ARM7 receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	SC_IRQ_EN	SW: RW, HW: R Scorpion Interrupt Enable When set, the Scorpion receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

RPM_SFPB_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x5: Select the S0_M0 ahb2ahb bridge test bus. 0x6: Select the S1_M1 ahb2ahb bridge test bus. 0x7: Select the M0 ahb2ahb bridge test bus. 0x8: Select the M1 ahb2ahb bridge test bus. 0x9: Select the M2 ahb2ahb bridge test bus. 0xA: Select the M3 ahb2ahb bridge test bus. 0xB: Select the M4 ahb2ahb bridge test bus. 0xC: Select the M5 ahb2ahb bridge test bus. 0xD: Select the M6 ahb2ahb bridge test bus. 0xE: Select the M7 ahb2ahb bridge test bus. 0xF: Select the M8 ahb2ahb bridge test bus. 0x10: Select the M9 ahb2ahb bridge test bus. 0x11: Select the M10 ahb2ahb bridge test bus. 0x12: Select the M11 ahb2ahb bridge test bus. 0x13: Select the M12 ahb2ahb bridge test bus. 0x14: Select the M13 ahb2ahb bridge test bus. 0x15: Select the M14 ahb2ahb bridge test bus. 0x16: Select the M15 ahb2ahb bridge test bus.

0x0006C044 RPM_SFPB_PORT_EN

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x3

The SFPB_PORT_EN register is a SFPB master port enable register.

RPM_SFPB_PORT_EN

Bits	Name	Description
31:2	RESERVED_BIT31_2	

RPM_SFPB_PORT_EN (cont.)

Bits	Name	Description
1	M1_PORT_EN	SW: RW, HW: R M1PortEnable When cleared (0), M1 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)
0	M0_PORT_EN	SW: RW, HW: R M0PortEnable When cleared (0), M0 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

0x0006C050 RPM_SFPB_ERROR_STAT

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000000

The SFPB_ERROR_STAT register is the bus error status register.

RPM_SFPB_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the DM channel ID that caused the detected error when the DM is the master of the access. If the DM is not the master of the access, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Applications DM 0x1: MDP 0x2: ARM9 0x3: ARM11 0x4: ADSP

RPM_SFPB_ERROR_STAT (cont.)

Bits	Name	Description
11:10	RESERVED_BITS11_10	
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit
3:2	RESERVED_BIT3_2	
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted based on PBUS_IRQ_EN settings. Clearing (0) this bit clears any interrupts asserted as well as enables the PBUS_ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x0006C054 RPM_SFPB_ERROR_ADDR

Type: Read
Clock: CC_SFPB_CLK
Reset State: 0x00000000

The SFPB_ERROR_ADDR register contains the bus error address.

RPM_SFPB_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when PBUS_ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x0006C058 RPM_SFPB_GPREG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0

The SFPB_GPREG register is a configurable general purpose register.

RPM_SFPB_GPREG

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	GPREG_CONTENT	SW: RW, HW: W GpregContent User defines the content of this register. The size of this register is defined by the generic-SFPB_GPREG_SIZE (1 - 32 bits). Power up value is clear (0)

0x0006C05C RPM_SFPB_XPU_ACR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFFFFFF

The SFPB_XPU_ACR register is a SFPB Access Control Register for configure register protection.

RPM_SFPB_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R M15PortEnable SFPB XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the SFPB configure space, including this register itself. Power up value is set (1)

17.8.1.2 RPM AHB 2x3 registers

Table 1-12 lists the differences between the standard systemFPB SW interface and system FPB SW interface as it corresponds to RPM 2x3 splitter. The changes in the SW interface are due to RPM customization of system FPB (via generics) for use as a 2x3 arbiter to direct traffic from ARM7/TIC/JTAG2AHB or COresight DAP to either the local AHB bus, chip systemFPB, or chip FABRIC.

Table 17-13 System FPB SWI changes for RPM

Register	Change for RPM
SFPB_CTRL_STATUS	No change.
SFPB_AHB2AHB_CFG_Ma, a=[0..15]	Removed. Since RPM 2x3 arbiter does not instantiate an AHB2AHB bridge on its single master interface, this register will not be generated.
SFPB_PORT_EN	Size reduced from 16 bits to 2 bits, since the RPM 2x3 arbiter has only 2 masters.
SFPB_AHB2AHB_CFG_Sa, a=[0..1]	Removed. The Sa_Ma interfaces in RPM 2x3 arbiter do not instantiate any AHB2AHB bridges, so this register will not be generated.
SFPB_ERROR_STAT	No change.
SFPB_ERROR_ADDR	No change.
SFPB_GPREG	Size changed from 16 bits to 1 bit. RPM 2x3 arbiter does not need this register, so it sets the GENERIC that controls the size of this register to 1, which is the minimum allowed size.
SFPB_XPU_ACR	No change.
SFPB_HW_CLK_GATING_CFG	Removed. RPM sets the ENABLE_HW_CLK_GATING generic to 0, so this register will not be generated.

NOTE An RPM_2x3 prefix is expected in the ARM_ADDRESS_FILE.flat for these registers, so they do not collide with other system FPBs used in the chip

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0x0006C000 RPM_SFPB_CTRL_STATUS

Type: Read/Write
Clock: RPM_BUS_CLK
Reset State: 0x0000

The SFPB_CTRL_STATUS register is a general configuration register.

NOTE The XPU_EN bit should never be set for RPM. Security needs to be set external to RPM (example system FPB level). RPM should only receive secure accesses.

RPM_SFPB_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables Power up value is clear (0) NOTE This bit should never be set for RPM. Setting to 1 will result in unpredictable behavior.
11	RPM_ARM7_IRQ_EN	SW: RW, HW: R ARM7InterruptEnable When set, the ARM7 receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	SC_IRQ_EN	SW: RW, HW: R Scorpion Interrupt Enable When set, the Scorpion receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

RPM_SFPB_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x5: Select the S0_M0 ahb2ahb bridge test bus. 0x6: Select the S1_M1 ahb2ahb bridge test bus. 0x7: Select the M0 ahb2ahb bridge test bus. 0x8: Select the M1 ahb2ahb bridge test bus. 0x9: Select the M2 ahb2ahb bridge test bus. 0xA: Select the M3 ahb2ahb bridge test bus. 0xB: Select the M4 ahb2ahb bridge test bus. 0xC: Select the M5 ahb2ahb bridge test bus. 0xD: Select the M6 ahb2ahb bridge test bus. 0xE: Select the M7 ahb2ahb bridge test bus. 0xF: Select the M8 ahb2ahb bridge test bus. 0x10: Select the M9 ahb2ahb bridge test bus. 0x11: Select the M10 ahb2ahb bridge test bus. 0x12: Select the M11 ahb2ahb bridge test bus. 0x13: Select the M12 ahb2ahb bridge test bus. 0x14: Select the M13 ahb2ahb bridge test bus. 0x15: Select the M14 ahb2ahb bridge test bus. 0x16: Select the M15 ahb2ahb bridge test bus.

0x0006C044 RPM_SFPB_PORT_EN

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x3

The SFPB_PORT_EN register is a SFPB master port enable register.

RPM_SFPB_PORT_EN

Bits	Name	Description
31:2	RESERVED_BIT31_2	

RPM_SFPB_PORT_EN (cont.)

Bits	Name	Description
1	M1_PORT_EN	SW: RW, HW: R M1PortEnable When cleared (0), M1 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)
0	M0_PORT_EN	SW: RW, HW: R M0PortEnable When cleared (0), M0 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

0x0006C050 RPM_SFPB_ERROR_STAT

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000000

The SFPB_ERROR_STAT register is the bus error status register.

RPM_SFPB_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the DM channel ID that caused the detected error when the DM is the master of the access. If the DM is not the master of the access, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Applications DM 0x1: MDP 0x2: ARM9 0x3: ARM11 0x4: ADSP

RPM_SFPB_ERROR_STAT (cont.)

Bits	Name	Description
11:10	RESERVED_BITS11_10	
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit
3:2	RESERVED_BIT3_2	
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted based on PBUS_IRQ_EN settings. Clearing (0) this bit clears any interrupts asserted as well as enables the PBUS_ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x0006C054 RPM_SFPB_ERROR_ADDR

Type: Read
Clock: CC_SFPB_CLK
Reset State: 0x00000000

The SFPB_ERROR_ADDR register contains the bus error address.

RPM_SFPB_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when PBUS_ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x0006C058 RPM_SFPB_GPREG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0

The SFPB_GPREG register is a configurable general purpose register.

RPM_SFPB_GPREG

Bits	Name	Description
31:1	RESERVED_BITS31_1	
0	GPREG_CONTENT	SW: RW, HW: W GpregContent User defines the content of this register. The size of this register is defined by the generic-SFPB_GPREG_SIZE (1 - 32 bits). Power up value is clear (0)

0x0006C05C RPM_SFPB_XPU_ACR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFFFFFF

The SFPB_XPU_ACR register is a SFPB Access Control Register for configure register protection.

NOTE The XPU_EN bit in SFPB_CTRL_STATUS register should never be set for RPM. This register, therefore, will never be needed since it is used only when the XPU_EN bit is set.

RPM_SFPB_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R M15PortEnable SFPB XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the SFPB configure space, including this register itself. Power up value is set (1)

17.9 MSG RAM XPU Registers (0x00100000 RPM_MSG_RAM_XPU_BASE)

This section contains MSG RAM XPU registers.

17.9.1 XPU Registers

0x00100000+4*n MSG_RAM_RPU_RGn_ACR, n=[0..47]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when RPU_IDR[MV, PT] = 01, i.e., a single VMID, read/write access vs. read-only access permission type RPU. These registers include two separate 5-bit "owner" VMID fields.

MSG_RAM_RPU_RGn_ACR

Bits	Name	Description
31:26	RESERVED31_26	Reserved.
25	ROGE	Read-only global enable: Opens up read-only access for this resource group to all VMIDs if: ROGE | (ROE & (VMID = ROVMID)) | RPU_RPU_ACR[VMID] = 1
24	ROE	Read-only enable. This is a "valid" bit for the ROVMID field.
23:21	RESERVED23_21	Reserved
20:16	ROVMID	Read-only VMID. Specifies "owner" VMID with read-only access to the registers in the associated resource group.
15:10	RESERVED15_10	Reserved
9	RWGE	Read/Write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/Write enable. This is a "valid" bit for the RWVMID field
7:5	RESERVED7_5	Reserved
4:0	RWVMID	Read/Write VMID. Specifies "owner" VMID with full read/write access to the registers in the associated resource group.

0x00100F80 MSG_RAM_RPU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

RPU Configuration Register: This register includes fields governing various RPU behaviors.

MSG_RAM_RPU_CR

Bits	Name	Description
31:2	RESERVED31_2	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set RPU_ESR. RPU_EAR and RPU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set RPU_ESR. RPU_EAR and RPU_ESYNR0 updated with address and syndrome of error.
2	RPUEIE	RPU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the RPU. Interrupt output is asserted if RPU_CR[RPUEIE] = 1 and any bit is set in RPU_ESR
1	RPUERE	RPU Error Report Enable. RPUERE = 0 causes the RPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master RPUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective RPU port. Errors from either port are terminated by the RPU as RAZ/WI Both client and configuration port errors are recorded in RPU_ESR, independent of the value of RPU_CR[RPUERE]
0	RPUE	RPU Enable. Governs whether RPU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures RPU and the MID to VMID mapping tables.

0x00100F84 MSG_RAM_RPU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the RPU, for both the client port and the configuration port.

MSG_RAM_RPU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x00100F88 MSG_RAM_RPU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the RPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the RPU's interrupt output (when enabled by RPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the RPU_ESYNRn registers, which are merely the "syndrome" of an error indicated by RPU_ESR.

MSG_RAM_RPU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while RPU_ESR[CFG, CLIENT] still non-zero. RPU_EAR and RPU_ESYNRn registers (and RPU_ESR itself, except for the MULTI bit) "lock" upon first error, RPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while RPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x00100F8C MSG_RAM_RPU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for RPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

MSG_RAM_RPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while RPU_ESR[CFG, CLIENT] still non-zero. RPU_EAR and RPU_ESYNRn registers (and RPU_ESR itself, except for the MULTI bit) "lock" upon first error, RPU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while RPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x00100F90 MSG_RAM_RPU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the RPU, for both the client port and the configuration port.

MSG_RAM_RPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x00100F94 MSG_RAM_RPU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the RPU, for both the client port and the configuration port.

MSG_RAM_RPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x00100FF4 MSG_RAM_RPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

MSG_RAM_RPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved

MSG_RAM_RPU_REV (cont.)

Bits	Name	Description
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x00100FF8 MSG_RAM_RPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x0009082F

RPU ID Register: Read-only register that defines various configuration attributes of the RPU instance.

MSG_RAM_RPU_IDR

Bits	Name	Description
31:21	RESERVED31_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only RPU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate RPU_RGn_RACR and RPU_RGn_WACR registers govern read vs. write access. For single VMID, RPU_RGn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. RPU_RGn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMD type access control. RPU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.
9:8	RESERVED9_8	Reserved

MSG_RAM_RPU_IDR (cont.)

Bits	Name	Description
7:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the RPU. Value can range between 0 and 255 (1-256 resource groups).

0x00100FFC MSG_RAM_RPU_RPU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

RPU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the RPU (including the RPU_RPU_ACR itself).

MSG_RAM_RPU_RPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the RPU's 4KB address region (including the RPU_RPU_ACR itself). For single VMID type RPUs (RPU_IDR[MV] = 0) the RPU_RPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

17.10 MPM PMIC Registers (0x00200000 MPM_BASE)

This section contains MPM PMIC registers.

17.10.1 SBI registers

MPM can issue up to four SSBI transactions when entering and exiting sleep modes. The number of transactions issued is configurable.

The following registers provide the configuration and content of these SSBI transactions.

0x00200000 MPM_PMIC_VDD_CFG

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register programs the SSBI SEQ for the first SSBI command during shutdown, and the last SSBI command when wake-up. It can turn on/off voltage of any voltage rail (memory or logic). In a split-rail memory system, this register is usually used to set the PMIC regulator setting for VDDCX power rail when entering sleep mode (SLAVE_DATA_OFF) and when exiting sleep mode (SLAVE_DATA_ON). The OFF setting would be customized for either power collapse or VDDCX_MIN (retention). The ON setting would reflect the voltage level to restore upon wake-up from power collapse or VDDCX_MIN.

NOTE VDDCX is the nomenclature for the parent/main logic power rail for APQ chip.

MPM_PMIC_VDD_CFG

Bits	Name	Description
25:24	SLAVE_ADDR_PREFIX	The 2-bit address prefix for slave used in SSBI 2.0.
23:16	SLAVE_ADDR	PMIC VDDCX voltage regulator SSBI register address.
15:8	SLAVE_DATA_OFF	Data to turn off/lower VDDCX power domain.
7:0	SLAVE_DATA_ON	Data to turn on/increase VDDCX power domain.

0x00200004 MPM_PMIC_VDD_CFG_1

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register programs the SSBI SEQ for the second SSBI command shutdown, and the next to last SSBI command upon wake-up. It can turn on/off voltage of any voltage rail (memory or logic). In a split-rail memory system, this register is usually used to set the PMIC regulator setting for

VDDMX power rail when entering sleep mode (SLAVE_DATA_OFF) and when exiting sleep mode (SLAVE_DATA_ON). The OFF setting would be customized for either power collapse or VDDMX_MIN (retention). The ON setting would reflect the voltage level to restore upon wake-up from power collapse or VDDMX_MIN.

NOTE VDDMX is the nomenclature for the memory power rail for APQ chip. If SSBI_CNT_MAX = 0 this is not used. If SSBI_CNT_MAX = 1, 2 or 3, it will be used.

MPM_PMIC_VDD_CFG_1

Bits	Name	Description
25:24	SLAVE_ADDR_PREFIX_1	The 2-bit address prefix for slave used in SSBI 2.0.
23:16	SLAVE_ADDR_1	PMIC VDDMX voltage regulator SSBI register address.
15:8	SLAVE_DATA_OFF_1	Data to turn off/lower VDDMX power domain.
7:0	SLAVE_DATA_ON_1	Data to turn on/increase VDDMX power domain.

0x00200008 MPM_PMIC_VDD_CFG_2

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register supports the SSBI SEQ by sending up to four SSBI commands. It programs the SSBI SEQ for the third SSBI command shutdown, and the next to next to last SSBI command upon wake-up. If SSBI_CNT_MAX = 0 or 1, it will not be used. If SSBI_CNT_MAX = 2 or 3, it will be used.

MPM_PMIC_VDD_CFG_2

Bits	Name	Description
25:24	SLAVE_ADDR_PREFIX_2	The 2-bit address prefix for slave used in SSBI 2.0.
23:16	SLAVE_ADDR_2	PMIC VDD voltage regulator SSBI register address.
15:8	SLAVE_DATA_OFF_2	Data to turn off/lower VDD power domain.
7:0	SLAVE_DATA_ON_2	Data to turn on/increase VDD power domain.

0x0020000C MPM_PMIC_VDD_CFG_3

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register supports the SSBI SEQ by sending up to four SSBI commands. When SSBI_CNT_MAX = 3, it programs the SSBI SEQ for the fourth SSBI command shutdown, and the first SSBI command upon wake-up. The values in the register will not be used if SSBI sequencer is programmed to send up to three SSBI commands only.

MPM_PMIC_VDD_CFG_3

Bits	Name	Description
25:24	SLAVE_ADDR_PREFIX_3	The 2-bit address prefix for slave used in SSBI 2.0.
23:16	SLAVE_ADDR_3	PMIC VDD voltage regulator SSBI register address.
15:8	SLAVE_DATA_OFF_3	Data to turn off/lower VDD power domain.
7:0	SLAVE_DATA_ON_3	Data to turn on/increase VDD power domain.

0x00200010 MPM_PMIC_SSBI_SEL_CFG

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0x003

This register is used to select SSBI controls among the two SSBI output lines from MPM. It also selects SSBI 2.0 versus SSBI 1.0 and SSBI_CLKs, etc.

MPM_PMIC_SSBI_SEL_CFG

Bits	Name	Description
10:9	MPM_SSBICLK_DIV	Specifies the clock divider for SSBI_FCLK. When 00: div1 (default) When 01: div2 When 10: div3 When 11: div4
8	MPM_SSBICLK_SEL	When 0: CXO (default) When 1: PXO
7	SSBI_FCLK_MODE	Which clock to be used as forwarding clock and transmit ssbi command is determined by bit 8. When 0: Legacy tcxo mode (default) When 1: Enable forwarding clock mode
6	MPM_NS_BIT	Security bit setting for MPM used in the SSBI 2.0 protocol. Default is 0 (secured). No current use on the PM8058 side for this bit.
5:4	SSBI_VERSION	When 00: SSBI 1.0 (default) When 01: SSBI 2.0 When 10 or 11: Reserved

MPM_PMIC_SSBI_SEL_CFG (cont.)

Bits	Name	Description
3	MPM_SSBI2_ENABLE	Enable MPM to send SSBI command through SSBI2 port. This SSBI2 port is not related to the SSBI 2.0 protocol. When MPM does not drive SSBI, MPM allows the SSBI from the core to pass through regardless of this setting. When 0: Disable (default) When 1: Enable default = 0
2	MPM_SSBI1_ENABLE	Enable MPM to send SSBI command through SSBI1 port. When MPM does not drive SSBI, MPM lets the SSBI from the core pass through regardless of this setting. When 0: Disable (default) When 1: Enable
1	SSBI2_FORCE_LOW	This bit becomes SSBI2_FORCE_LOW. It forces the secondary SSBI outputs low when asserted. Write '0' enables normal SSBI signals drive pads. Default value after POR is '1'. Software must must reset this bit to enable normal SSBI function. When analog_test_mode pin is asserted, then this bit has no effect on SSBI outputs.
0	SSBI1_FORCE_LOW	This bit becomes SSBI1_FORCE_LOW. It forces the primary SSBI outputs low when asserted. Write '0' enables normal SSBI signals drive pads. Default value after POR is '1'. Software must reset this bit to enable normal SSBI function. When analog_test_mode pin is asserted, then this bit has no effect on SSBI outputs.

17.10.2 MPM CXO and PXO CONTROL registers

0x00200014 MPM_CXO_CTRL

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register controls turning on/off of CXO, as well as CXOPAD_EN, which is the clock-gating at the CXO_PAD to gate the CXO output to the core.

MPM_CXO_CTRL

Bits	Name	Description
2	ALT_FUNC_SEL	When 0: Not enabled; CXO_EN chip-level IO is controlled by bit 0 in this register (default) When 1: CXO_EN chip-level IO is not controlled by the bit 0 in this register. Instead, it is controlled by the MPM input port (core_cxo_po) directly
1	CXOPAD_DIS	When 0: CXOPAD clock to the core passes through ungated (default) When 1: Gate the CXOPAD clock to the core off

MPM_CXO_CTRL (cont.)

Bits	Name	Description
0	CXO_DIS	When 0: CXO_EN = 1 (default) When 1: Disabled, CXO is shut-off (when alt_func_sel = 0)

0x00200018 MPM_PXO_OSC_CTRL

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register controls the on-chip PXO OSC. To enable the low-power sleep mode of PXO, we use the following setting. PXO_OSC_RF_BYPASS = 1; PXOPAD_CORE_DIS = PXOPAD_HV_DIS = 1; PXO_OSC_SLEEP = 1.

MPM_PXO_OSC_CTRL

Bits	Name	Description
6:4	PXO_OSC_GAIN	When 000: Default When 111: Highest gain (8 levels)
3	PXOPAD_CORE_DIS	When 0: Enabled (default). Be sure to gate the clock to core before vddcx collapse. When 1: Disabled (clock-gated). This is for PXOPAD clock gating to the chip core.This will gate the main PXO source to the chip's clock controllers.
2	PXO_OSC_SLEEP	When 0: On (default) When 1: Enable sleep mode of the PXO oscillator.
1	PXOPAD_HV_DIS	When 0: Normal operation (default) When 1: Disabled. This is the PXOPAD clock gating to the HV branch of the output clock. The MPM uses this as a refclk source.
0	PXO_OSC_RF_BYPASS	When 0: Normal operation When 1: Enable by-pass mode and use chip input directly.

17.10.3 Sleep timer registers

0x0020001C MPM_SLEEP_TIMETICK_WAKEUP_TIME

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register specifies the MPM sleep crystal timetick counter value at which to generate a wake-up interrupt to initiate the warm-up process.

MPM_SLEEP_TIMETICK_WAKEUP_TIME

Bits	Name	Description
31:0	DATA	When wake-up time is reached, the counter will continue instead of resetting.

0x00200020 MPM_SLEEP_TIMETICK_WAKEUP_TIME_LATCH

Type: Read
Clock: REFCLK_DIV2
Reset State: 0

This register is used for synchronizing the MPM_SLEEP_TIMETICK_WAKEUP_TIME data to sleep_clk.

MPM_SLEEP_TIMETICK_WAKEUP_TIME_LATCH

Bits	Name	Description
0	LATCHING	When this bit is set (1), MPM_SLEEP_TIMETICK_WAKEUP_TIME data is synchronizing to sleep_clk. The microprocessor cannot re-write to MPM_SLEEP_TIMETICK_WAKEUP_TIME register until this bit is cleared (0).

0x00200024 MPM_SLEEP_TIMETICK_COUNT_VAL

Type: Read (async)
Clock: REFCLK_DIV2
Reset State: 0

This register returns the current value of the sleep crystal timetick counter.

MPM_SLEEP_TIMETICK_COUNT_VAL

Bits	Name	Description
31:0	DATA	This counter is reset at power-on (true power-on, not resume from power collapse) and is free-running afterwards, rolling over at 2^32-1. The coarse sleep counter value is sampled using the REFCLK_DIV2. Repeat reads until 2 consecutive values match.

17.10.4 Power controller registers

0x00200028 MPM_LOW_POWER_CFG

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register is used to configure MPM to go to one of the SLEEP states, such as XOs_SD, (XOs_SHUTDOWN), VDDCX_PC_VDDMX_PC (both logic and memory rails collapsed), VDDCX_PC_VDDMX_MIN (logic collapse with memory in retention), and VDDCX_MIN_VDDMX_MIN (both logic and memory in retention). It is an asynchronous reset register. In blackbird/phantom MPM, support for split-rail memory and support of individual shutdown of either or both crystals (PXO and CXO) was added. Many bits in this register are enable/disable bits for clamp_* and freeze_* signals. These clamp_* and freeze_* signals are for isolating different power domains and interfaces during sleep. It is beneficial to understand these freeze* and clamp* MPM outputs and their function during sleep.

MPM_LOW_POWER_CFG

Bits	Name	Description
24	ENABLE_PXOPAD_HV_GATING	When at '1', enables MPM HW to gate the PXOPAD HV clock source during sleep and wake-up. When at '0', no gating can be applied by MPM HW. Note: CXO clock to the core is always un-gated, and only set by SW
23	SSBICLK2_DIS	Disables SSBI logic/symbol clock to save power when not used. When 0: Enable (default) When 1: Disable
22	SELECT_CLAMP_SSBI	Selects the de-assertion timing (early or normal) of the MPM's input clamp on the core's SSBI control inputs during warm boot. When 0: clamp_io (default) When 1: preclamp_io to give SSBI line early access during RPM BOOT
21:20	SSBI_CNT_MAX	Configures how many SSBI commands the MPM HW will send out. When 00: Send 1 SSBI command (default) When 01: Send 2 SSBI commands When 10: Sends 3 SSBI commands When 11: Sends 4 SSBI commands For split-rail memory system, normally, set it at '01'. For non-split-rail memory system, set it at '00'.
19	SMEM_EN	This bit is to enable split-rail memory support. If the chip is not split-rail memory chip, assert it at '0'. If it is a split-rail memory design, set it at '1'.

MPM_LOW_POWER_CFG (cont.)

Bits	Name	Description
18	DISABLE_FREEZE_IO_M	Only applies to freeze_io_m/freeze_io_jtag_dbg_m signals, not other freeze_io* signals. When 0: Freeze_io_m is asserted (default) When 1: Freeze_io_m is disabled
17	DISABLE_CLAMP_MEM	This enable bit applies only to clamp_mem signal, not other clamp_io* signals. When 0: Enable CLAMP_MEM (default) When 1: Disable CLAMP_MEM
16	DISABLE_HW_RESTORED	When disabled, MPM FSM will not wait for hw_restored to be asserted before exiting wake-up. When 0: Enable (default) When 1: Disable hw_restored signal
15	ENABLE_PXOPAD_CORE_GATING	When 0: Disabled. No gating can be applied by MPM HW. In this mode, only SW can control via MPM_PXO_OSC_CTRL[PXOPAD_CORE_DIS] When 1: Enables MPM HW gate the PXOPAD clock source to the chips during sleep and wake-up
14	ENABLE_CXOPAD_GATING	When 0: CXO clock input to the chip is ungated and free running When 1: Enables MPM HW to apply CXOPAD gating during sleep and wake-up.
13	ENABLE_RPM_GROUPED_INT	No longer used in this version. The grouped interrupt from RPM is a dedicated interrupt to MPM INTC, bit 3. See MPM INT MAP for details.
12	DISABLE_TRST_N	Disables mpm_trst_n assertion at warm boot and allows SW to disable the trst_n and preserve breakpoints and debug information while the core is being reset.
11	DISABLE_CORE_RESET	Disables mpm_core_reset assertion at warm boot and allows pending MPM interrupts to the core to be seen at the end of PWR_UP state. For example, a chip reset by MPM is not needed for VDD_MIN sleep mode when chip state is retained.
10	DISABLE_CLAMPS	Disables all clamp_io signals including clamp_jtag, clamp_io, preclamp_io, clamp_ssbi, (except for clamp_mem).
9	DISABLE_FREEZE	Disables all freeze_io_* signals except for freeze_io_*_m signals.
8	DEBUG_ON	Enables debugging power collapse using JTAG. When asserted (1), the processor will be stopped when emerging from the next power collapse cycle via the MPM assertion of dbg_req to the processor tap controller.
7	SW_EBI1_CTL_ENABLE	Enable software control of Freeze_io_ebi1.
6	SW_EBI1_CTL_VALUE	SW value for freeze_io_ebi1.
5	VDDMX_MIN_EN	To enable VDDMX rail minimization (memory retention).
4	VDDMX_PC_EN	To enable VDDMX rail power collapse (off). It is only valid to assert this when also asserting VDDCX_PC_EN.

MPM_LOW_POWER_CFG (cont.)

Bits	Name	Description
3	VDDCX_MIN_EN	To enable VDDCX rail minimization (retention).
2	VDDCX_PC_EN	To enable VDDCX rail power collapse (off).
1	PXO_SD_EN	When 0: MPM HW is not controlling PXO. PXO control will be configured as defined by the MPM_PXO_OSC_CTRL register settings When 1: Enable MPM HW control PXO shutdown and wake-up
0	CXO_SD_EN	When 0: MPM HW is not controlling CXO. CXO control will be configured as defined by the MPM _CXO_CTRL register settings When 1: Enable MPM HW control CXO shutdown and wake-up

0x0020002C MPM_LOW_POWER_STATUS

Type: Read (async)
Clock: REFCLK_DIV2
Reset State: 0

This is an asynchronous reset register, which provides power collapse/VDD_MIN/XOs_SD status information. It is recommended that SW check this register first to make sure MPM FSM is in IDLE state before issuing any MPM-function-related actions/commands.

MPM_LOW_POWER_STATUS

Bits	Name	Description
13:12	SSBI_SEQ_FSM	The state value for SSBI_SEQ_FSM inside MPM (for debugging purpose). When 00: Idle When 01: Tx When 11: Delay When 10: Done
11:9	SMEM_FSM_STATE	The state value for SMEM_FSM inside MPM (for debugging purpose). When 000: SMEM_IDLE When 110: SMEM_CLAMP When 111: SMEM_MEMCLK_DIS When 101: SMEM_UNCLAMP
8	VDDMX_DOWN	This bit can be checked by software as part of the warm boot process prior to writing HW_RESTORED to determine which type of boot to take: full boot if this bit is set (1) meaning the sleep event did involve VDDMX power collapse; partial boot if this bit is clear (0), meaning the sleep event did not involve VDDMX power collapse. When set (1), indicates that the chip is up from VDDMX power collapse. This bit is reset upon exiting the sleep mode (software writing to the HW_RESTORED register).

MPM_LOW_POWER_STATUS (cont.)

Bits	Name	Description
7	VDDCX_DOWN	This bit can be checked by software as part of the warm boot process prior to writing HW_RESTORED to determine which type of boot to take: full boot if this bit is set (1) meaning the sleep event did involve VDDCX power collapse, or partial boot if this bit is clear (0), meaning the sleep event did not involve VDDCX power collapse. When set (1), indicates that the chip is up from VDDCX power collapse. This bit is reset upon exiting the sleep mode (software writing to the HW_RESTORED register).
6	PXO_DOWN	When set (1), indicates that the PXO is off.
5	CXO_DOWN	When set (1), indicates that the external TCXO crystal is off.
4	POWER_DOWN	This bit has been superseded with VDDMX_DOWN and VDDCX_DOWN bits, which provide more granularity in the power down.
3:0	FSM_STATE	Power collapse FSM current state, changed to output coding. The FSM state value is sampled using the REFCLK_DIV2. Repeat reads until 2 consecutive values match. The output coding is used in FSM. This is the encoded version. When 0000: IDLE When 0001: FREEZE When 0011: PWR_OFF When 0111: CLK_OFF When 1111: CLK_ON When 1110: CLK_WU When 1100: PWR_ON When 1000: PWR_UP When 1001: BOOT When 1101: UNCLAMP When 0101: UNFREEZE

0x00200030 MPM_CXO_POWER_RAMPUP_TIME

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register specifies the required CXO warm-up and power ramp-up times in unit of 32 KHz. This power ramp-up time (Tpwr_up) is the TOTAL power ramp-up time, which includes the warm-up time for both memory and logic rails, and the SSBI TX time. For example, it takes two SSBI commands to ramp up memory rail first and logic rail second, each takes Tssbi_tx time. The memory warm up time is specified in MPM_SPLIT_MEM_DELAY_TIME as Tmem_wu, The logic warm-up time is Tlogic_wu.

SW must program Tpwr_up as: Tpwr_up >= 2 * Tssbi_tx + (2 -1) *Tmem_wu + Tlogic_wu.

MPM_CXO_POWER_RAMPUP_TIME

Bits	Name	Description
31:16	CXO_WARMUP_TIME	Specifies time needed to tcxo to warm up in sleep clock periods. Can specify up to 8192 ms ramp-up time.
15:0	POWER_RAMPUP_TIME	Specifies time needed to power to ramp up in sleep clock periods. Can specify up to 8192 ms warm-up time.

0x00200034 MPM_PXO_WARMUP_TIME

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register specifies the required PXO warm-up. It is in unit of 32 KHz clock.

MPM_PXO_WARMUP_TIME

Bits	Name	Description
15:0	PXO_WARMUP_TIME	Specifies time needed to power to ramp/warm-up in sleep clock periods. Can specify up to 8192 ms warm-up time.

0x00200038 MPM_SPLIT_MEM_DELAY_TIME

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register specifies the required PXO warm-up. It is in unit of SSBI symbol clock period (ssbiclk_div2).

MPM_SPLIT_MEM_DELAY_TIME

Bits	Name	Description
31:16	RAMP_UP_DELAY_TIME	Specifies the delay time needed between the two SSBI commands during ramping up, first one for powering up memory rail (VDDMX), and the second for powering up logic rail. It is in ssbi_clk_div2 periods. For 20 MHz ssbi clk, It can specify up to 6.5 ms warm-up time
15:0	RAMP_DOWN_DELAY_TIME	Specifies the delay time needed between the two SSBI commands during ramping down, first one for shutting down/lower logic rail (VDDCX) and the second for shutting down/lower memory rail (VDDMX). It is given in ssbi_clk_div2 periods. For 20 MHz ssbi clk, it can specify up to 6.5 ms warm-up time.

0x0020003C MPM_HARDWARE_RESTORED

Type: Write
Clock: REFCLK_DIV2
Reset State: Undefined

If the disable_hardware_restored bit in the MPM_POWER_COLLAPSE_CONFIG register is set at ’1’, this command will be bypassed by MPM FSM and it will not wait for this SW command to complete the power-up process.

MPM_HARDWARE_RESTORED

Bits	Name	Description
0	DATA	Set (1) when resumed power-up (state restoration for warm boot) is complete.

17.10.5 Interrupt controller registers

Each chip has its own MPM power up interrupt source mapping. However the bottom four interrupts are treated differently since they have fixed and known uses common to all chips, as described in Table 2-2.

Table 17-14 MPM_INT mapping

Bits	MPM INT source	MPM INT source comments
63:4	<chip dependent>	
3	grouped_int	From RPM INTC grouped IRQ (i.e., clk_on_req), and level-shifted to the always-on domain.
2	spare_int	A spared interrupt source, used to be codec_hssd_irq_n.
1	penirq_n_debounced	From penirq_n input, after debounced.
0	mpm_wakeup_int	Internal MPM timetick interrupt. See MPM_SLEEP_TIMETICK_WAKEUP_TIME.

0x00200040 MPM_INT_CLEAR_1

Type: Write
Clock: REFCLK_DIV2
Reset State: Undefined

This register is used to clear the status bits of the various interrupts. In previous MPM, it was necessary to have only up to 32 bit interrupts. But now we have both MPM_INT_CLEAR_1 and MPM_INT_CLEAR_2, supporting up to 64 interrupts.

MPM_INT_CLEAR_1

Bits	Name	Description
31:0	INT_CLEAR_1	Set (1) to clear status of interrupt.

0x00200044 MPM_INT_CLEAR_2

Type: Write
Clock: REFCLK_DIV2
Reset State: Undefined

The expanded second set to support up to 64 interrupts.

MPM_INT_CLEAR_2

Bits	Name	Description
31:0	INT_CLEAR_2	Set (1) to clear status of interrupt.

0x00200048 MPM_INT_EN_1

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register is used to enable the various interrupts (first set).

MPM_INT_EN_1

Bits	Name	Description
31:0	INT_EN_1	Set (1) to enable interrupt.

0x0020004C MPM_INT_EN_2

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register is used to enable the various interrupts (second set).

MPM_INT_EN_2

Bits	Name	Description
31:0	INT_EN_2	Set (1) to enable interrupt.

0x00200050 MPM_INT_POLARITY_1

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register is to set the polarity of the interrupts.

MPM_INT_POLARITY_1

Bits	Name	Description
31:0	INT_POLARITY_1	Sets the polarity value of interrupt. When 0: Low When 1: High

0x00200054 MPM_INT_POLARITY_2

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register sets the polarity of the interrupts (second set).

MPM_INT_POLARITY_2

Bits	Name	Description
31:0	INT_POLARITY_2	Sets the polarity value of interrupt. When 0: Low When 1: High

0x00200058 MPM_DETECT_CTL_1

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register controls the interrupt triggering mechanism and must be initialized before an interrupt is enabled. Clear (0) for level trigger and set (1) for edge trigger.

MPM_DETECT_CTL_1

Bits	Name	Description
31:0	DETECT_CTL_1	Controls the interrupt triggering mechanism. Clear (0) for level trigger and set (1) for edge trigger.

0x0020005C MPM_DETECT_CTL_2

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register controls the interrupt triggering mechanism and must be initialized before an interrupt is enabled. Clear (0) for level trigger and set (1) for edge trigger.

MPM_DETECT_CTL_2

Bits	Name	Description
31:0	DETECT_CTL_2	Controls the interrupt triggering mechanism. Clear (0) for level trigger and set (1) for edge trigger.

0x00200060 MPM_INT_STATUS_1

Type: Read
Clock: REFCLK_DIV2
Reset State: Undefined

This register provides the status bits for the interrupts. This bit is sticky. This means that once a bit is set here, the source of the interrupt request must be reset, and the corresponding bit in the clear register must be set in order to reset the status bit (in the said order).

MPM_INT_STATUS_1

Bits	Name	Description
31:0	INT_STATUS_1	Status bit value for interrupt.

0x00200064 MPM_INT_STATUS_2

Type: Read
Clock: REFCLK_DIV2
Reset State: Undefined

This register provides the status bits for the interrupts. This bit is sticky. This means that once a bit is set here, the source of the interrupt request must be reset, and the corresponding bit in the clear register must be set in order to reset the status bit (in the said order).

MPM_INT_STATUS_2

Bits	Name	Description
31:0	INT_STATUS_2	Status bit value for interrupt.

0x00200068 MPM_INT_WKUP_CLK_SEL_1

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register specifies if any additional clock source (other than RPM/MPM reference clock (REFCLK)) must bring up for that specific triggered interrupt. (0) means no additional clock must be brought up for that particular interrupt. (1) means the other clock than REFCLK must be brought up in parallel with REFCLK. Therefore, it is possible to warm-up two clocks in parallel to save system overhead.

MPM_INT_WKUP_CLK_SEL_1

Bits	Name	Description
31:0	MPM_INT_WKUP_CLK_SEL_1	Specify the wake-up clock associated with each interrupt.

0x0020006C MPM_INT_WKUP_CLK_SEL_2

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register specifies if any additional clock source (other than RPM/MPM reference clock (REFCLK)) must bring up for that specific triggered interrupt. (0) means no additional clock must be brought up for that particular interrupt. (1) means the other clock than REFCLK must be brought up in parallel with REFCLK. Therefore, it is possible to warm-up two clocks in parallel to save system overhead. This is the second set.

MPM_INT_WKUP_CLK_SEL_2

Bits	Name	Description
31:0	MPM_INT_WKUP_CLK_SEL_2	Specify the wake-up clock associated with each interrupt.

0x00200070 MPM_CLOCK_SEL

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This is to select MPM REFCLK source, either CXO or PXO. Default is CXO. The divided-2 of refclk is used to clock the crif interface to access the MPM registers. MPM_REFCLK uses the same clock source.

MPM_CLOCK_SEL

Bits	Name	Description
0	MPM_REFCLK_SEL	MPM_REFCLK should be using the same clock source, either PXO or CXO. The crif interface inside MPM uses this REFCLK divided by 2. When 0: CXO (default) When 1: PXO

17.10.6 Debug registers

0x00200074 MPM_DEBUG_BUS_EN

Type: Read/Write
Clock: REFCLK_DIV2
Both bits cannot be set to (1) at the same time. The default is (0) for both bits.

MPM_DEBUG_BUS_EN

Bits	Name	Description
1	DEBUG_EN_1	dbg_rd_bus_1 <= altclk_needs_on & -- [31] pwr_up_expire & -- [30] timer_expire & -- [29] clamp_ssbi_loc & -- [28] switch_off & -- [27] pen_irq_n_debounced & -- [26] warm_boot_ebi2_en_local & -- [25] warm_boot_ebi1_en_local & -- [24] refclk_en & -- [23] any_int_sync & -- [22] refclk_div2_halt & -- [21] timetick_int & --[20] '0' & --[19] refclk_div2_dbg & --[18] cxopad_en_hw & -- [17] cxopad_en_pipe_1 & --[16] pxopad_core_en_comb & --[15] ssbiclk_div2_halt & -- [14] mpm_drives_ssbi & -- [13] ssbiclk_div2_dbg & -- [12] all_ssbi_done_sync & -- [11] mpm_ssbi_fclk_po & -- [10] mpm_ssbi_fclk_oe & -- [9] ssbi1_oe_mux_ana & -- [8] ssbi1_po_mux_ana & -- [7] ssbi2_oe_mux_ana & -- [6] ssbi2_po_mux_ana & -- [5] sw_done & -- [4] pxo_osc_rf_bypass_loc & -- [3] grouped_int & -- [2] pxopad_hv_en_comb & -- [1] pxo_osc_sleep_loc -- [0]

MPM_DEBUG_BUS_EN (cont.)

Bits	Name	Description
0	DEBUG_EN	dbg_rd_bus <= mpm_core_reset & -- [31] wdog_expired_async_hv & -- [30] mpm_sw_reset_async_hv & -- [29] msm_req_hv & -- [28] mpm_msm_ack & -- [27] mpm_dbg_req & -- [26] dbg_ack_hv & -- [25] mpm_marm_trst_n &--[24] mpm_int_hv & -- [23] preclamp_io_raw & -- [22] freeze_io_t & -- [21] freeze_io_ebi1_t & -- [20] freeze_io_jtag_dbg_t & -- [19] clamp_io_n & -- [18] clamp_mem_t & -- [17] '0' & -- [16] freeze_io_m_t & -- [15] show_int_dbg & -- [14] low_power_status_dbg [13:0]

17.10.7 JTAG state registers

0x00200078 MPM_JTAG_STATE

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register is used to store the JTAG efuse shadow register state after a full (cold) boot, and used to restore the shadow registered state after a partial (warm) boot.

MPM_JTAG_STATE

Bits	Name	Description
31:0	STATE	This register is one-time writable after a resin_n reset or a wdog_expired reset.

0x0020007C MPM_ENABLE_JTAG

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This is a write-once-only register used to enable JTAG debugging immediately after resin.

MPM_ENABLE_JTAG

Bits	Name	Description
0	ENABLE	This is a write-once-only register. Writing a '1' will enable the ARM JTAG.

17.10.8 Touch screen debounce registers

0x00200080 MPM_PEN_DEBOUNCE_CTL

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register is used to control the pen debounce logic.

MPM_PEN_DEBOUNCE_CTL

Bits	Name	Description
3	ENABLE	Controls the pen down debounce logic (logic is bypassed when disabled). This bit should be set (1) before going to the power-down mode. This bit should be cleared (0) upon a wake-up interrupt due to pen-touch or before enabling the TSSC in the master mode. When 0: Disabled When 1: Enabled
2:0	TIME	Determines the debounce time used by the debounce pen-down interrupt. When 000: 400 ms When 001: 800 ms When 010: 1.2 ms When 011: 1.6 ms When 100: 2.0 ms When 101: 3.0 ms When 110: 4.0 ms When 111: 6.0 ms

17.10.9 Control for EBI bus freeze during warm boot

0x00200084 MPM_WARM_BOOT_CFG

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register controls either freezing or not freezing EBI1/2 buses during warm boot, so that warm boot can have access to the unfrozen EBI buses.

NOTE This register is only implemented in DOrA65; it is not available for Phoenix2 because Phoenix2 is hardwired to enable EBI1 and disable EBI2 during warm boot.

MPM_WARM_BOOT_CFG

Bits	Name	Description
1	ENABLE_EBI2	When 0: Freeze EBI2 bus during warm boot When 1: Unfreeze EBI2 bus during warm boot
0	ENABLE_EBI1	When 0: Freeze EBI1 bus during warm boot When 1: Unfreeze EBI1 bus during warm boot

17.10.10 Regfile registers

0x00200088+4*n MPM_REGn_FILE, n=[0..8]

Type: Read/Write
Clock: REFCLK_DIV2
Reset State: 0

This register provides software configuration data that is needed for a warm boot-up.

MPM_REGn_FILE

Bits	Name	Description
31:0	DATA	Software configuration data needed for warm boot-up.

17.11 PA1 SSBI2 Registers (0x00300000 PA1_SSBI2_CFG_BASE)

This section contains SSBI2 configuration registers.

0x00300000 PA1_SSBI2_CTL

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0x83005

Specifies various generic SSBI2 control information. Bits 19:13 comprising of fields SSBI2_DATA_PDEN, FCLK_MODE, FCLK_SW_OVERRIDE and NUM_FCLK are either asynchronously reset or set. This is because they control the signals going directly to a pad. Remaining bits 12:0 are synchronously reset or set.

The delay between the master and the slave, by design, should be budgeted according to the ssbi2 timing specification. The reset default setting on the SEL_RD_DATA and SSBI2_DATA_DEL fields is expected to typically work out of the box for most PMIC to APQ, SURF, FFA routing in normal and forward clocking mode, provided the master and slave close timing based on the ssbi2 timing specification.

PA1_SSBI2_CTL

Bits	Name	Description
19:16	NUM_FCLK	Indicates a programmable number of active forwarding clock cycles following a SSBI2 'transaction done' for a corresponding SSBI2 request. Unless there is a new SSBI2 transaction request, the forwarding clock is shut off after toggling NUM_FCLK cycles at the PMIC SSBI2 clock frequency. The suggested setting (default value) for APQ8064 is 8 clock cycles.
15	FCLK_SW_OVERRIDE	This is a software override bit to control the CGC for forwarding clock. Set this bit to 1 to allow the SSBI2 clock to continue as a forwarding clock through the CGC (provided FLCK_MODE = 1). This override bit is provided to allow continuous toggling clock to SSBI2 slave irrespective of how the HW logic controls the CGC. Set this bit to 0 to enable pure HW control on the forwarding clock CGC.
14	FCLK_MODE	Set this bit to 1 to activate forwarding clock mode. When this bit is 0, the FCLK_SW_OVERRIDE field has no meaning. Out of reset, the mode is set to 0 indicating that the SSBI2 slave does not work off the forwarding clock. When FCLK_MODE = 0; no forwarding clock. When FCLK_MODE = 1; FCLK_SW_OVERRIDE = 1; forwarding clock always toggles. When FCLK_MODE = 1; FCLK_SW_OVERRIDE = 0; forwarding clock is controlled by HW logic.
13	SSBI2_DATA_PDEN	Pulldown enable for SSBI2_DATA pad.

PA1_SSBI2_CTL (cont.)

Bits	Name	Description
12	PA_CGC_CTRL	This is to control the SSBI2 clock going to this PMIC arbiter. Set this bit to 1 when you want to allow the clock to flow through the CGC. Set this bit to 0 to shut off clock to PMIC arbiter. Out of reset, this bit is set to 1.
11	RESERVED_1	Reserved bit.
10:8	SSBI2_ADDR_WIDTH	Specifies what is the addressing mode in SSBI2 mode. This field is only applicable in SSBI2 mode. 0x0: 8-bit addressing mode 0x1: 9-bit addressing mode 0x2: 10-bit addressing mode and so on
7	SSBI2_MODE	Set this bit to 1 when SW wants to switch to new SSBI2 mode. Set this is 0 when in old SSBI mode. 0x0: SSBI 1.0 Mode 0x1: SSBI 2.0 Mode
6	RESERVED_2	Reserved bit.
5:4	SEL_RD_DATA	Specifies which RD_DATA value to select out of four possible combinations. This signal allows the returned data from the slave to be captured inside the master, 1, 2, or 3 symbols late in order to accommodate a large range of routing delay. Based on this field, the entire read transaction length will increase by SEL_RD_DATA number of symbols.
3:2	SSBI2_DATA_DEL	Specifies the number of 1/2 clock periods, SSBI2_DATA will be delayed before sampling inside.
1:0	IDLE_SYMS	The master will ensure there are at least this number of idle symbol periods in between the accesses. The idle time is inserted at the end of the read or write transaction. This supported values are always between 1 - 3.

0x00300004 PA1_SSBI2_INT_ENABLE

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0

Provides control on whether the TRANSACTION-DONE interrupts can be generated or not (per SW master).

PA1_SSBI2_INT_ENABLE

Bits	Name	Description
9:0	ENABLE_SSBI2_INT	SSBI2 transaction done interrupts for each SW master are generated only when the corresponding bits are set. The following list provides the interrupt mapping information. 0x9: Unused: SW to set to 0_1 0x8: Riva A9 0x7: Unused: SW to set to 0_2 0x6: KPSS CPU1 non-secure 0x5: KPSS CPU1 secure 0x4: GSS A5 0x3: LPASS Q6 0x2: KPSS CPU0 non-secure 0x1: KPSS CPU0 secure 0x0: RPM

0x00300008 PA1_SSBI2_PRIORITIES

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0

Specifies the priorities for SSBI2 arbiter ports. The SSBI2 block supports up to maximum of 8 ports for arbitration. Each port has 3 bits to denote its priority. The bits are synchronously reset.

CAUTION Since the reset state value of SSBI2_PRIORITIES is 0, only SW requests (hard-coded to port # 0) can get through. SW has to program this register to allow hardware requests through the SSBI2 arbiter.

NOTE For APQ8064, 6 arbiter ports are used (5 ports for hardware PVC requests and 1 port for software command request). This register will scale based on the number of PVC ports. The port mapping for the HW PVC ports in mentioned in the SSBI2_PVC_CTL register.

PA1_SSBI2_PRIORITIES

Bits	Name	Description
17:15	PRIORITY5	Specifies the port number of host, with a priority that is 1 less then PRIORITY4.
14:12	PRIORITY4	Specifies the port number of host, with a priority that is 1 less then PRIORITY3.
11:9	PRIORITY3	Specifies the port number of host, with a priority that is 1 less then PRIORITY2.

PA1_SSBI2_PRIORITIES (cont.)

Bits	Name	Description
8:6	PRIORITY2	Specifies the port number of host, with a priority that is 1 less then PRIORITY1.
5:3	PRIORITY1	Specifies the port number of host, with a priority that is 1 less then PRIORITY0.
2:0	PRIORITY0	Specifies the port number of the highest priority host.

0x0030000C PA1_SSBI2_BANKS_2_3_CTL

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0xFFFFFFFF

This register specifies whether an access is allowed to banks (pages) 2 and 3 of PM8921. The access control to the banks (pages) 2 and 3 of PM8921 is set per VMID. Bit 0 corresponds to access control for VMID 0 and bit 31 corresponds to access control for VMID 31.

NOTE This register has no meaning when used in conjunction with control for other PMICs such as PM8018.

PA1_SSBI2_BANKS_2_3_CTL

Bits	Name	Description
31:0	ACCESS_CONTROL	Set each of the 32 bits to 1 if the master corresponding to that VMID wishes to initiate SW requests to banks (pages) 2 and 3 of PM8921. For other PMICs, this value has no meaning and is ignored.

0x00300010 PA1_SSBI2_ILLEGAL_STATUS

Type: Read
Clock: AHB_BUS_CLOCK
Reset State: 0

Returns status information of the software master that tried to access a SSBI2 command micro register, and failed security through the VIT table.

PA1_SSBI2_ILLEGAL_STATUS

Bits	Name	Description
5:1	ILLEGAL_VMID_4_0	Indicates the VMID of the master that performed the most recent illegal access. The value in this field is only meaningful when the ILLEGAL_ACCESS bit is set. On software reads, the value is retained unless another illegal access with a different VMID happens. In that case, this field will have the VMID corresponding to the most recent illegal master.
0	ILLEGAL_ACCESS	When set (1) indicates an illegal access. An illegal access is defined as an access that does not find a matching VMID in the SSBI2_VITn registers. This bit is cleared on a software read provided there is no other illegal access in the same clock cycle that a software read happens.

0x00300014 PA1_SSBI2_TEST_BUS_CTL

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0x0

This register is used for test bus (32 bits) control. The following is the bit mapping for the 32 bits. Bits 15:0 correspond to PMIC arbiter # 1 signals and bits 31:16 are the same as 15:0, but for PMIC arbiter # 2.

In the current form, only enabling/disabling the test bus is supported. In the future, this register will be expanded to include several test modes.

Table 17-15 PMIC arbiter signals

15	ssbi2_master_req	Request from SSBI arbiter to master.
14	ssbi2_master_read	Access type information from SSBI2 arbiter to master.
13	ssbi2_master_ack	Ack from SSBI2 master to arbiter.
12	ssbi2_sw_cmd_done	SW cmd done flag from SSBI2 arbiter to SMD micro.
11	ssbi2_sw_cmd_ack	SW cmd ack from SSBI2 arbiter to CMD micro.
10:8	winner	Arbitration winner.
7	pvc_intf_busy	Indicates that PVC interface is busy.
6	xpu_slave_summary_sel	Indicates xPU security permission for client access.
5	client_valid	xPU signal indicating that access to client region is valid.
4	client_wr	xPU signal indicating the access type to client region.
3	ssbi2_fclk_en_loc	Local signal that controls the CGC for FCLK.
2	fclk_en_hw	Hardware enable to logic that controls the CGC for FCLK.
1	ssbi2_cmd_micro_crif_error	CRIF error from SSBI2 CMD micro.
0	ssbi2_cfg_micro_crif_error	CRIF error from SSBI2 CFG micro.

PA1_SSBI2_TEST_BUS_CTL

Bits	Name	Description
0	TEST_BUS_EN	Set this bit to enable the 32-bit test bus. When reset, the test bus drives all zeros.

0x00300020+4*n PA1_SSBI2_VITn, n=[0..9]

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0

This is the VMID index table used for enabling concurrent SSBI2 SW requests among multiple SW masters. Secure entities are expected to assign a VMID for the SW master corresponding to an index. The SSBI2_VIT0 has the VMID associated with index 0, SSBI2_VIT1 has the VMID associated with index 1 and so on.

CAUTION By default, only the SW master with a VMID of '0' has access to registers in SSBI2 command micro space. SROT/RPM has to populate this table before valid SW masters can initiate SSBI2 SW transactions.

NOTE APQ8064 will have 10 SW masters. The maximum range of n will be 0-31 corresponding to a maximum of 32 VMID masters. Also, the indices n(0-9) should match the interrupt index mapping to processor given in SSBI2_INT_ENABLE.

PA1_SSBI2_VITn

Bits	Name	Description
4:0	VMID	VMID corresponding to index n.

0x003000A0 PA1_SSBI2_PVC_CTL

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0

This register provides the global enable/disable for the PVC interface module, per PVC port enable/disable as well as captures PVC interface busy status.

NOTE In APQ8064, there are 5 PVC ports (to connect to KPSS SAW CPU0 & CPU1,LPASS SAW, Q6SW & Q6FW). This register will scale in size based on the number of PVC ports (set as a RTL GENERIC).

WARNING In a PMIC arbiter wrapper system having more than 1 PMIC arbiter module; if a PVC port(x) is enabled in one of the PMIC arbiters, the corresponding PVC_port(x) in all

the other PMIC arbiters shall be disabled. If multiple PVC_port(x)'s enabled simultaneously, the hardware does not guarantee correct operation.

PA1_SSBI2_PVC_CTL

Bits	Name	Description
8	PVC_INTF_BUSY	This is a status bit. When set (1) indicates that the PVC interface module is busy (meaning there is at least one PVC transaction being serviced). Busy line goes high when PVC interface detects a new request on one of the PVC ports and stays high until it samples a done from SSBI2 arbiter. Writes to this bit will not have any effect and will be ignored.
7:6	RESERVED	Reserved bits.
5	PVC_PORT5_EN	Set this bit to 1 to enable PVC port 5. PVC port 5 maps to Q6FW
4	PVC_PORT4_EN	Set this bit to 1 to enable PVC port 4. PVC port 4 maps to Q6SW
3	PVC_PORT3_EN	Set this bit to 1 to enable PVC port 3. PVC port 3 maps to SMPSS CPU1 SAW.
2	PVC_PORT2_EN	Set this bit to 1 to enable PVC port 2. PVC port 2 maps to SMPSS CPU 0 SAW.
1	PVC_PORT1_EN	Set this bit to 1 to enable PVC port 1. PVC port 1 maps to LPASS Q6 SAW.
0	PVC_INTF_EN	Set this bit to 1 to enable PVC interface module.

0x003000A4+4*n PA1_SSBI2_PVC_TABLEn, n=[0..19]

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0

This set of registers indicates the full PVC table corresponding to all the PVC ports. There are 4 entries per PVC port and there are 5 PVC ports in APQ8064; hence the 20 entries. Each entry is 15-bit address to the SSBI2 slave registers. This indirect addressing from the PVC ports to the SSBI2 slave registers provides a way to enforce security on hardware SSBI2 requests.

NOTE Though this current document shows 20 entries, the number of entries should scale based on the GENERIC settings for the number of PVC ports and the address index width. Also though 15-bit addresses are supported, 10-bit addressing is all that is expected for current PMICs.

PA1_SSBI2_PVC_TABLEn

Bits	Name	Description
14:0	ADDR	15-bit address of the SSBI2 slave registers.

17.12 PA1 XPU Registers (0x00400000 PA1_XPU_BASE)

This section contains PMIC Arbiter 1 XPU registers.

Treatment of invalid accesses

XPU registers occupy the first 8 Kb of the total 1 MB XPU configuration space. Any accesses outside the 8 Kb space will be aliased on 8-Kb boundaries over the complete 1 MB decode region.

0x00400F80 PA1_RPU_CR

Type: Read/write
Clock: XPU_CLK
Reset State: 0x00000000

RPU configuration register. This register includes fields governing various RPU behaviors.

PA1_RPU_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved.
3	DCDEE	Decode error enable. Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0x0: Do not record. Decode errors do not set RPU_ESR. RPU_EAR and RPU_ESYNR0 not updated. 0x1: Record. Decode errors set RPU_ESR. RPU_EAR and RPU_ESYNR0 updated with address and syndrome of error.
2	RPUEIE	RPU error interrupt enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the RPU. Interrupt output is asserted if RPU_CR[RPUEIE] = 1 and any bit is set in RPU_ESR.
1	RPUERE	RPU error report enable. Both client and configuration port errors are recorded in RPU_ESR, independent of the value of RPU_CR[RPUERE]. 0x0: Causes the RPU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master. 0x1: Enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective RPU port. Errors from either port are terminated by the RPU as RAZ/WI.
0	RPUE	RPU enable. Governs whether RPU checking occurs for both the client port and the configuration port. 0x0: Reset 0x1: Set once SROT configures RPU and the MID to VMID mapping tables

0x00400F84 PA1_RPU_EAR

Type: Read/write
Clock: XPU_CLK
Reset State: 0x00000000

Error address register. This register captures the address upon errors detected by the RPU, for both the client port and the configuration port.

PA1_RPU_EAR

Bits	Name	Description
31:0	PA	Physical address of the errant request.

0x00400F88 PA1_RPU_ESR

Type: Read/write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error status register. This register captures the status upon errors detected by the RPU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old. The presence of an asserted value on any bit in this register is what prompts the assertion of the RPU's interrupt output (when enabled by RPU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the RPU_ESYNRn registers, which are merely the 'syndrome' of an error indicated by RPU_ESR.

PA1_RPU_ESR

Bits	Name	Description
31	MULTI	Multi-error. Indicates additional error occurred while RPU_ESR[CFG, CLIENT] still non-zero. RPU_EAR and RPU_ESYNRn registers (and RPU_ESR itself, except for the MULTI bit) "lock" upon first error, RPU_ESR must be cleared to unlock. Status, address and syndrome of errors that occur while RPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved.
1	CLIENT	Client port error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration port error. Indicates error (access control or decode) associated with a configuration port request.

0x00400F8C PA1_RPU_ESRRESTORE

Type: Read/write
Clock: XPU_CLK
Reset State: 0x00000000

Error restore register. This is simply an aliased address for RPU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

PA1_RPU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error. Indicates additional error occurred while RPU_ESR[CFG, CLIENT] still non-zero. RPU_EAR and RPU_ESYNRn registers (and RPU_ESR itself, except for the MULTI bit) "lock" upon first error, RPU_ESR must be cleared to unlock. Status, address and syndrome of errors that occur while RPU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved.
1	CLIENT	Client port error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration port error. Indicates error (access control or decode) associated with a configuration port request.

0x00400F90 PA1_RPU_ESYNR0

Type: Read/write
Clock: XPU_CLK
Reset State: 0x00000000

Error syndrome register. Captures the syndrome upon errors detected by the RPU, for both the client port and the configuration port.

PA1_RPU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved.
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x00400F94 PA1_RPU_ESYNR1

Type: Read/write
Clock: XPU_CLK
Reset State: 0x00000000

Error syndrome register. Captures the syndrome upon errors detected by the RPU, for both the client port and the configuration port.

PA1_RPU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved.
24	AFULL	AFULL field of errant request.
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request.
21:20	ALOCK	ALOCK field of errant request.
19	RESERVED19	Reserved.
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x00400FF4 PA1_RPU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision register. This register provides major/minor revision codes for the implementation.

PA1_RPU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved.
7:4	MAJOR	Major variant field.
3:0	MINOR	Minor variant field.

0x00400FF8 PA1_RPU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x000009FF

RPU ID register. Read-only register that defines various configuration attributes of the RPU instance.

PA1_RPU_IDR

Bits	Name	Description
31:21	RESERVED31_21	Reserved.
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved.
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU) 0x0: RPU 0x1: APU 0x2: MPU 0x3: Reserved
11	PT	Permission type. 0x0: Indicates full access vs. no access type. Only RPU_RGn_ACR registers needed, and they specify which VMID (s have full access other VMIDs have no access.) 0x1: Indicates read/write access type vs. read-only access type. For multi-VMID, separate RPU_RGn_RACR and RPU_RGn_WACR registers govern read vs. write access. For single VMID, RPU_RGn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields.

PA1_RPU_IDR (cont.)

Bits	Name	Description
10	MV	Multi-VMID. 0x0: Indicates single VMID type access control. RPU_RGn_ACR registers indicate single 5-bit "owner" VMID field for governing access. 0x1: Indicates multi-VMD type access control. RPU_RGn_xACR registers include separate bit per VMID (32 bits for governing access.)
9:8	RESERVED9_8	Reserved.
7:0	NRG	Number of resource groups. Indicates number of resource groups (minus 1) supported by the RPU. Value can range between 0 and 255 (1-256 resource groups).

0x00400FFC PA1_RPU_RPU_ACR

Type: Read/write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

RPU access control register. This register includes a bit per VMID governing configuration port access to the registers of the RPU (including the RPU_RPU_ACR itself).

PA1_RPU_RPU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the RPU's 4-Kb address region (including the RPU_RPU_ACR itself). For single VMID type RPUs (RPU_IDR[MV] = 0) the RPU_RPU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

0x00401000+4*n PA1_RPU_RGn_RACR, n=[0..511]

Type: Read/write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) access control registers. This description is for the case when RPU_IDR[MV, PT] = 01, i.e., a single VMID, read/write access vs. read-only access permission type RPU. These registers include 2 separate 5 bit 'owner' VMID fields.

PA1_RPU_RGn_RACR

Bits	Name	Description
31:26	RESERVED31_26	Reserved.
25	ROGE	Read-only global enable. Opens up read-only access for this resource group to all VMIDs if: ROGE | (ROE & (VMID = ROVMID)) | RPU_RPU_ACR[VMID] = 1
24	ROE	Read-only enable. This is a valid bit for the ROVMID field.
23:21	RESERVED23_21	Reserved.
20:16	ROVMID	Read-only VMID. Specifies "owner" VMID with read-only access to the registers in the associated resource group.
15:10	RESERVED15_10	Reserved.
9	RWGE	Read/write global enable. Opens up read/write access for this resource group to all VMIDs if: RWGE | (RWE & (VMID = RWVMID)) | RPU_RPU_ACR[VMID] = 1
8	RWE	Read/write enable. This is a valid bit for the RWVMID field.
7:5	RESERVED7_5	Reserved.
4:0	RWVMID	Read/write VMID. Specifies owner VMID with full read/write access to the registers in the associated resource group.

17.13 PA1 SSBI2 Registers (0x00500000 PA1_SSBI2_CMD_BASE)

This section lists the ARM registers associated with the SSBI2 command micro space.

Following are all the SSBI2 command micro software registers. These registers are open to access by all bus masters that have access to the slave port.

Table 17-16 lists all the SSBI2 command registers along with the type of software access.

Table 17-16 Summary of SW registers

Address offset	Register	SW access type
0x0	SSBI2_CMD	Command write
0x4	SSBI2_RD_STATUS	Read

Treatment of invalid accesses

An invalid access is any read or write access to addresses that do not have a valid SSBI2 command SW register associated with that particular address in the aliased 32-KB regions within the 1-MB space. Invalid write accesses are ignored and invalid read accesses return all zeroes. An invalid access also triggers a CRIF error which is captured in the test bus.

0x00500000 PA1_SSBI2_CMD

Type: Write (cmd)
Clock: AHB_BUS_CLOCK
Reset State: 0

The SW masters write to this register to initiate either a read or a write SSBI2 transaction. Through this register, the SW can address up to 32 Kb of SSBI2 slave register space. However, the PMICs only house a maximum of 1024 registers and hence the values on the most significant 5-bits of the REG_ADDR_14_8 field are ignored. The REG_DATA field is only applicable for write transaction and is ignored for reads. The read data returned back from the SSBI2 slave is directed to the SSBI2_RD_STATUS register. Bit 23 is left as a reserved bit to enable slave address to grow to 16-bits in the future.

PA1_SSBI2_CMD

Bits	Name	Description
24	RDWRN	Denotes whether the command to perform is a register write (0) or read (1).
23	RESERVED	Reserved bit.
22:16	REG_ADDR_14_8	Specifies the upper 7 bits, 14:8, of SSBI slave register address.
15:8	REG_ADDR_7_0	Lower 8 bits, 7:0, of SSBI slave register address.
7:0	REG_DATA	Write data for a slave register.

0x00500004 PA1_SSBI2_RD_STATUS

Type: Read
Clock: AHB_BUS_CLOCK
Reset State: 0

This register provides the read data as well as the status of the transaction. This register also returns back information associated with the transaction such as the SSBI2 slave register address and the transaction access type. SW is expected to poll TRANS_DONE and TRANS_DENIED until either of these bits are set to 1.

- TRANS_DONE = 0, TRANS_DENIED = 1; indicates to SW that the current transaction was rejected because the master did not have permissions to access the corresponding SSBI2 slave register.
- TRANS_DONE = 1, TRANS_DENIED = 0; indicates to SW that the current transaction was completed successfully. For writes, it means that the write data was sent out on the SSBI wire and for reads, it means that the read data is returned back and is now in SSBI2_RD_STATUS[REG_DATA]. At this point, the SW is said to have completed one transaction.
- Both TRANS_DONE and TRANS_DENIED is either 0 or 1; does not happen and is not a valid combination.

PA1_SSBI2_RD_STATUS

Bits	Name	Description
27	TRANS_DONE	When set (1), indicates that the SSBI2 has completed the transaction. If this was a write request, the write has completed. If this was a read request, the read data has returned back. This bit is not set for security violations via xPU or PM8921 banks (pages) 2 & 3 access control. NOTE This bit is cleared on read.
26	TRANS_DENIED	When set (1), indicates that a SSBI2 transaction was denied because the master did not have access to the particular SSBI2 slave SW register to where the access was intended. For PM88921 banks (pages) 0 and 1, this bit is set based on xPU blocking the transaction. For PM8921 banks (pages) 2 and 3, this bit is set based on the settings in SSBI2_BANKS_2_3_CTL register that blocked the transaction. NOTE This bit is cleared on read.
25	TRANS_PROG	When set (1), indicates that a SSBI2 transaction is in progress. This signal will be set for the duration from REQ assertion until DONE assertion.
24	RDWRN	Returns the access type of transaction. A value of 1 implies a read transaction and a value of 0 implies a write transaction.
23	RESERVED	Reserved bit.
22:8	REG_ADDR	Returns the address to which the SSBI2 transaction was performed.

PA1_SSBI2_RD_STATUS (cont.)

Bits	Name	Description
7:0	REG_DATA	Returned read register data. NOTE: The read data is not cleared on reads, however will return all zeros for a SW master whose transaction was denied or was an illegal SW master.

17.14 PA2 SSBI2 Registers (0x00600000 PA2_SSBI2_CFG_BASE)

This section lists the ARM registers associated with the SSBI2 configuration micro space.

Following are all the SSBI2 configuration micro software registers. These registers shall be accessed only by a secure-entity (RPM/sROT).

Table 17-17 lists all the SSBI2 configuration registers, along with the type of software access.

Table 17-17 Summary of SW registers

Address offset	Register	SW access type
0x0	SSBI2_CTL	Pseudo-static R/W
0x4	SSBI2_INT_ENABLE	Pseudo-static R/W
0x8	SSBI2_PRIORITIES	Pseudo-static R/W
0xC	SSBI2_BANKS_2_3_CTL	Pseudo-static R/W
0x10	SSBI2_ILLEGAL_STATUS	Read
0x14	SSBI2_TEST_BUS_CTL	R/W
0x20+4n	SSBI2_VITn, n=[0... 9]	Pseudo-static R/W
0xA0	SSBI2_PVC_CTL	Pseudo-static R/W
0xA4+4n	SSBI2_PVC_TABLEn, n=[0...11]	Pseudo-static R/W

Treatment of invalid accesses

An invalid access is any read or write access to addresses that do not have a valid SSBI2 configuration SW register associated with that particular address in the aliased 256 KB regions within the 1 MB space. Invalid write accesses are ignored and invalid read accesses return all zeros. An invalid access also triggers a CRIF error which is captured in the test bus.

Chip-specific configurations

Depending on which chipset the PMIC arbiter wrapper is used in, certain SW registers may scale in size and width. Table 17-18 lists the SW registers and the APQ8064 specific settings.

Table 17-18 SW register configurations in APQ8064

Register	APQ8064
SSBI2_INT_ENABLE	10 enables
SSBI2_PRIORITIES	6 priority settings
SSBI2_VITn	n=[0... 9]
SSBI2_PVC_CTRL	Provides enables for 5 PVC ports
SSBI2_PVC_TABLEn	n=[0... 19]

0x00600000 PA2_SSBI2_CTL

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0x83005

Specifies various generic SSBI2 control information. Bits 19:13 comprising of fields SSBI2_DATA_PDEN, FCLK_MODE, FCLK_SW_OVERRIDE and NUM_FCLK are either asynchronously reset or set. This is because they control the signals going directly to a pad. Remaining bits 12:0 are synchronously reset or set.

The delay between the master and the slave, by design, should be budgeted according to the ssbi2 timing specification. The reset default setting on the SEL_RD_DATA and SSBI2_DATA_DEL fields is expected to typically work out of the box for most PMIC to APQ, SURF, FFA routing in normal and forward clocking mode provided the master and slave close timing based on the ssbi2 timing specification.

PA2_SSBI2_CTL

Bits	Name	Description
19:16	NUM_FCLK	Indicates a programmable number of active forwarding clock cycles following a SSBI2 'transaction done' for a corresponding SSBI2 request. Unless there is a new SSBI2 transaction request, the forwarding clock is shut off after toggling NUM_FCLK cycles at the PMIC SSBI2 clock frequency. The suggested setting (default value) for APQ8064 is 8 clock cycles.
15	FCLK_SW_OVERRIDE	This is a software override bit to control the CGC for forwarding clock. Set this bit to 1 to allow the SSBI2 clock to continue as a forwarding clock through the CGC (provided FLCK_MODE = 1). This override bit is provided to allow continuous toggling clock to SSBI2 slave irrespective of how the HW logic controls the CGC. Set this bit to 0 to enable pure HW control on the forwarding clock CGC.
14	FCLK_MODE	Set this bit to 1 to activate forwarding clock mode. When this bit is 0, the FCLK_SW_OVERRIDE field has no meaning. Out of reset, the mode is set to 0 indicating that the SSBI2 slave does not work off the forwarding clock. When FCLK_MODE = 0; no forwarding clock. When FCLK_MODE = 1; FCLK_SW_OVERRIDE = 1; forwarding clock always toggles. When FCLK_MODE = 1; FCLK_SW_OVERRIDE = 0; forwarding clock is controlled by HW logic.
13	SSBI2_DATA_PDEN	Pulldown enable for SSBI2_DATA pad.
12	PA_CGC_CTRL	This is to control the SSBI2 clock going to this PMIC arbiter. Set this bit to 1 when you want to allow the clock to flow through the CGC. Set this bit to 0 to shut off clock to PMIC arbiter. Out of reset, this bit is set to 1.
11	RESERVED_1	Reserved bit.

PA2_SSBI2_CTL (cont.)

Bits	Name	Description
10:8	SSBI2_ADDR_WIDTH	Specifies what is the addressing mode in SSBI2 mode. This field is only applicable in SSBI2 mode. 0x0: 8-bit addressing mode 0x1: 9-bit addressing mode 0x2: 10-bit addressing mode and so on
7	SSBI2_MODE	Set this bit to 1 when SW wants to switch to new SSBI2 mode. Set this is 0 when in old SSBI mode. 0x0: SSBI 1.0 Mode 0x1: SSBI 2.0 Mode
6	RESERVED_2	Reserved bit.
5:4	SEL_RD_DATA	Specifies which RD_DATA value to select out of four possible combinations. This signal allows the returned data from the slave to be captured inside the master, 1, 2, or 3 symbols late in order to accommodate a large range of routing delay. Based on this field, the entire read transaction length will increase by SEL_RD_DATA number of symbols.
3:2	SSBI2_DATA_DEL	Specifies the number of 1/2 clock periods, SSBI2_DATA will be delayed before sampling inside.
1:0	IDLE_SYMS	The master will ensure there are at least this number of idle symbol periods in between the accesses. The idle time is inserted at the end of the read or write transaction. This supported values are always between 1 - 3.

0x00600004 PA2_SSBI2_INT_ENABLE

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0

Provides control on whether the TRANSACTION-DONE interrupts can be generated or not (per SW master).

PA2_SSBI2_INT_ENABLE

Bits	Name	Description
9:0	ENABLE_SSBI2_INT	SSBI2 transaction done interrupts for each SW master are generated only when the corresponding bits are set. The following list provides the interrupt mapping information. 0x9: Unused: SW to set to 0_1 0x8: Riva A9 0x7: Unused: SW to set to 0_2 0x6: KPSS CPU1 non-secure 0x5: KPSS CPU1 secure 0x4: GSS A5 0x3: LPASS Q6 0x2: KPSS CPU0 non-secure 0x1: KPSS CPU0 secure 0x0: RPM

0x00600008 PA2_SSBI2_PRIORITIES

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0

Specifies the priorities for SSBI2 arbiter ports. The SSBI2 block supports up to maximum of 8 ports for arbitration. Each port has 3 bits to denote its priority. The bits are synchronously reset.

CAUTION Since the reset state value of SSBI2_PRIORITIES is 0, only SW requests (hard-coded to port # 0) can get through. SW has to program this register to allow hardware requests through the SSBI2 arbiter.

NOTE For APQ8064, 6 arbiter ports are used (5 ports for hardware PVC requests and 1 port for software command request). This register will scale based on the number of PVC ports. The port mapping for the HW PVC ports in mentioned in the SSBI2_PVC_CTL register.

PA2_SSBI2_PRIORITIES

Bits	Name	Description
17:15	PRIORITY5	Specifies the port number of host, with a priority that is 1 less then PRIORITY4.
14:12	PRIORITY4	Specifies the port number of host, with a priority that is 1 less then PRIORITY3.
11:9	PRIORITY3	Specifies the port number of host, with a priority that is 1 less then PRIORITY2.

PA2_SSBI2_PRIORITIES (cont.)

Bits	Name	Description
8:6	PRIORITY2	Specifies the port number of host, with a priority that is 1 less then PRIORITY1.
5:3	PRIORITY1	Specifies the port number of host, with a priority that is 1 less then PRIORITY0.
2:0	PRIORITY0	Specifies the port number of the highest priority host.

0x0060000C PA2_SSBI2_BANKS_2_3_CTL

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0xFFFFFFFF

This register specifies whether an access is allowed to banks (pages) 2 and 3 of PM8921. The access control to the banks (pages) 2 and 3 of PM8921 is set per VMID. Bit 0 corresponds to access control for VMID 0 and bit 31 corresponds to access control for VMID 31.

NOTE This register has no meaning when used in conjunction with control for other PMICs such as PM8018.

PA2_SSBI2_BANKS_2_3_CTL

Bits	Name	Description
31:0	ACCESS_CONTROL	Set each of the 32 bits to 1 if the master corresponding to that VMID wishes to initiate SW requests to banks (pages) 2 and 3 of PM8921. For other PMICs, this value has no meaning and is ignored.

0x00600010 PA2_SSBI2_ILLEGAL_STATUS

Type: Read
Clock: AHB_BUS_CLOCK
Reset State: 0

Returns status information of the software master that tried to access a SSBI2 command micro register, and failed security through the VIT table.

PA2_SSBI2_ILLEGAL_STATUS

Bits	Name	Description
5:1	ILLEGAL_VMID_4_0	Indicates the VMID of the master that performed the most recent illegal access. The value in this field is only meaningful when the ILLEGAL_ACCESS bit is set. On software reads, the value is retained unless another illegal access with a different VMID happens. In that case, this field will have the VMID corresponding to the most recent illegal master.
0	ILLEGAL_ACCESS	When set (1) indicates an illegal access. An illegal access is defined as an access that does not find a matching VMID in the SSBI2_VITn registers. This bit is cleared on a software read provided there is no other illegal access in the same clock cycle that a software read happens.

0x00600014 PA2_SSBI2_TEST_BUS_CTL

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0x0

This register is used for test bus (32 bits) control. The following is the bit mapping for the 32 bits. Bits 15:0 correspond to PMIC arbiter # 1 signals and bits 31:16 are the same as 15:0, but for PMIC arbiter # 2.

In the current form, only enabling/disabling the test bus supported. In the future, this register will be expanded to include several test modes.

Table 17-19 Bit mapping

15	ssbi2_master_req	Request from SSBI arbiter to master.
14	ssbi2_master_read	Access type information from SSBI2 arbiter to master.
13	ssbi2_master_ack	Ack from SSBI2 master to arbiter.
12	ssbi2_sw_cmd_done	SW cmd done flag from SSBI2 arbiter to SMD micro.
11	ssbi2_sw_cmd_ack	SW cmd ack from SSBI2 arbiter to CMD micro.
10:8	winner	Arbitration winner.
7	pvc_intf_busy	Indicates that PVC interface is busy.
6	xpu_slave_summary_sel	Indicates xPU security permission for client access.
5	client_valid	xPU signal indicating that access to client region is valid.
4	client_wr	xPU signal indicating the access type to client region.
3	ssbi2_fclk_en_loc	Local signal that controls the CGC for FCLK.
2	fclk_en_hw	Hardware enable to logic that controls the CGC for FCLK.
1	ssbi2_cmd_micro_crif_error	CRIF error from SSBI2 CMD micro.
0	ssbi2_cfg_micro_crif_error	CRIF error from SSBI2 CFG micro.

PA2_SSBI2_TEST_BUS_CTL

Bits	Name	Description
0	TEST_BUS_EN	Set this bit to enable the 32-bit test bus. When reset, the test bus drives all zeros.

0x00600020+4*n PA2_SSBI2_VITn, n=[0..9]

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0

This is the VMID index table used for enabling concurrent SSBI2 SW requests among multiple SW masters. Secure entities are expected to assign a VMID for the SW master corresponding to an index. The SSBI2_VIT0 has the VMID associated with index 0, SSBI2_VIT1 has the VMID associated with index 1 and so on.

CAUTION By default, only the SW master with a VMID of '0' has access to registers in SSBI2 command micro space. SROT/RPM has to populate this table before valid SW masters can initiate SSBI2 SW transactions.

NOTE APQ8064 will have 10 SW masters. The maximum range of n will be 0-31 corresponding to a maximum of 32 VMID masters. Also, the indices n(0-9) should match the interrupt index mapping to processor given in SSBI2_INT_ENABLE.

PA2_SSBI2_VITn

Bits	Name	Description
4:0	VMID	VMID corresponding to index n.

0x006000A0 PA2_SSBI2_PVC_CTL

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0

This register provides the global enable/disable for the PVC interface module, per PVC port enable/disable as well as captures PVC interface busy status.

NOTE In APQ8064 , there are 5 PVC ports (to connect to KPSS SAW CPU0 & CPU1,LPASS SAW, Q6SW & Q6FW). This register will scale in size based on the number of PVC ports (set as a RTL GENERIC).

WARNING In a PMIC arbiter wrapper system having more than 1 PMIC arbiter module; if a PVC port(x) is enabled in one of the PMIC arbiters, the corresponding PVC_port(x) in all

the other PMIC arbiters shall be disabled. If multiple PVC_port(x)'s enabled simultaneously, the hardware does not guarantee correct operation.

PA2_SSBI2_PVC_CTL

Bits	Name	Description
8	PVC_INTF_BUSY	This is a status bit. When set (1) indicates that the PVC interface module is busy (meaning there is at least one PVC transaction being serviced). Busy line goes high when PVC interface detects a new request on one of the PVC ports and stays high until it samples a done from SSBI2 arbiter. Writes to this bit will not have any effect and will be ignored.
7:6	RESERVED	Reserved bits.
5	PVC_PORT5_EN	Set this bit to 1 to enable PVC port 5. PVC port 5 maps to Q6FW
4	PVC_PORT4_EN	Set this bit to 1 to enable PVC port 4. PVC port 4 maps to Q6SW
3	PVC_PORT3_EN	Set this bit to 1 to enable PVC port 3. PVC port 3 maps to SMPSS CPU1 SAW.
2	PVC_PORT2_EN	Set this bit to 1 to enable PVC port 2. PVC port 2 maps to SMPSS CPU 0 SAW.
1	PVC_PORT1_EN	Set this bit to 1 to enable PVC port 1. PVC port 1 maps to LPASS Q6 SAW.
0	PVC_INTF_EN	Set this bit to 1 to enable PVC interface module.

0x006000A4+4*n PA2_SSBI2_PVC_TABLEn, n=[0..19]

Type: Read/write
Clock: AHB_BUS_CLOCK
Reset State: 0

This set of registers indicates the full PVC table corresponding to all the PVC ports. There are 4 entries per PVC port and there are 5 PVC ports in APQ8064 and hence the 20 entries. Each entry is 15-bit address to the SSBI2 slave registers. This indirect addressing from the PVC ports to the SSBI2 slave registers provides a way to enforce security on hardware SSBI2 requests.

NOTE Though this current document shows 20 entries, the number of entries should scale based on the GENERIC settings for the number of PVC ports and the address index width. Also though 15-bit addresses are supported, 10-bit addressing is all that is expected for current PMICs.

PA2_SSBI2_PVC_TABLEn

Bits	Name	Description
14:0	ADDR	15-bit address of the SSBI2 slave registers.

17.15 PA2 SSBI2 Registers (0x00C00000 PA2_SSBI2_CMD_BASE)

This section lists the ARM registers associated with the SSBI2 command micro space.

Following are all the SSBI2 command micro software registers. These registers are open to access by all bus masters that have access to the slave port.

Table 17-20 lists all the SSBI2 command registers along with the type of software access.

Table 17-20 Summary of SW registers

Address offset	Register	SW access type
0x0	SSBI2_CMD	Command write
0x4	SSBI2_RD_STATUS	Read

Treatment of invalid accesses

An invalid access is any read or write access to addresses that do not have a valid SSBI2 command SW register associated with that particular address in the aliased 32-Kb regions within the 1-MB space. Invalid write accesses are ignored and invalid read accesses return all zeroes. An invalid access also triggers a CRIF error which is captured in the test bus.

0x00C00000 PA2_SSBI2_CMD

Type: Write (cmd)
Clock: AHB_BUS_CLOCK
Reset State: 0

The SW masters write to this register to initiate either a read or a write SSBI2 transaction. Through this register, the SW can address up to 32 Kb of SSBI2 slave register space. However the PMICs only house a maximum of 1024 registers and hence the values on the most significant 5-bits of the REG_ADDR_14_8 field are ignored. The REG_DATA field is only applicable for write transaction and is ignored for reads. The read data returned back from the SSBI2 slave is directed to the SSBI2_RD_STATUS register. Bit 23 is left as a reserved bit to enable slave address to grow to 16-bits in the future.

PA2_SSBI2_CMD

Bits	Name	Description
24	RDWRN	Denotes whether the command to perform is a register write (0) or read (1).
23	RESERVED	Reserved bit.
22:16	REG_ADDR_14_8	Specifies the upper 7 bits, 14:8, of SSBI slave register address.
15:8	REG_ADDR_7_0	Lower 8 bits, 7:0, of SSBI slave register address.
7:0	REG_DATA	Write data for a slave register.

0x00C00004 PA2_SSBI2_RD_STATUS

Type: Read
Clock: AHB_BUS_CLOCK
Reset State: 0

This register provides the read data as well as the status of the transaction. This register also returns back information associated with the transaction such as the SSBI2 slave register address and the transaction access type. SW is expected to poll TRANS_DONE and TRANS_DENIED until either of these bits are set to 1.

- TRANS_DONE = 0, TRANS_DENIED = 1; indicates to SW that the current transaction was rejected because the master did not have permissions to access the corresponding SSBI2 slave register.
- TRANS_DONE = 1, TRANS_DENIED = 0; indicates to SW that the current transaction was completed successfully. For writes, it means that the write data was sent out on the SSBI wire and for reads, it means that the read data is returned back and is now in SSBI2_RD_STATUS[REG_DATA]. At this point, the SW is said to have completed one transaction.
- Both TRANS_DONE and TRANS_DENIED is either 0 or 1; does not happen and is not a valid combination.

PA2_SSBI2_RD_STATUS

Bits	Name	Description
27	TRANS_DONE	When set (1), indicates that the SSBI2 has completed the transaction. If this was a write request, the write has completed. If this was a read request, the read data has returned back. This bit is not set for security violations via xPU or PM8921 banks (pages) 2 & 3 access control. NOTE This bit is cleared on read.
26	TRANS_DENIED	When set (1), indicates that a SSBI2 transaction was denied because the master did not have access to the particular SSBI2 slave SW register to where the access was intended. For PM88921 banks (pages) 0 and 1, this bit is set based on xPU blocking the transaction. For PM8921 banks (pages) 2 and 3, this bit is set based on the settings in SSBI2_BANKS_2_3_CTL register that blocked the transaction. NOTE This bit is cleared on read.
25	TRANS_PROG	When set (1), indicates that a SSBI2 transaction is in progress. This signal will be set for the duration from REQ assertion until DONE assertion.
24	RDWRN	Returns the access type of transaction. A value of 1 implies a read transaction and a value of 0 implies a write transaction.
23	RESERVED	Reserved bit.
22:8	REG_ADDR	Returns the address to which the SSBI2 transaction was performed.

PA2_SSBI2_RD_STATUS (cont.)

Bits	Name	Description
7:0	REG_DATA	Returned read register data. NOTE The read data is not cleared on reads, however will return all zeros for a SW master whose transaction was denied or was an illegal SW master.

18 SATA Registers

18.1 Overview

Table 18-1 SATA Bases

Base Name	Parent	Address
SATA_CAP	SATA_BASE	0x29000000
UNIPHY_PLL_REFCLK_CFG	SATA_PHY_BASE	0x1B400000

18.2 SATA Registers (0x29000000 SATA_BASE)

This section contains the description for the registers inside the SATA Host Controller core that can be accessed through the AXI slave interface.

18.2.1 Generic host register descriptions

0x29000000 SATA_CAP

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x6716FF80

SATA_CAP

Bits	Name	Description
31	S64A	Supports 64-bit Addressing DWC_ahsata supports 64-bit addressable data structures by utilizing P FBU and P CLBU registers. Reset Value: Configurable. 0x1: when M_HADDR_WIDTH=64 0x0: when M_HADDR_WIDTH=32 (RO)
30	SNCQ	Supports Native Command Queuing DWC_ahsata supports SATA native command queueing by handling DMA Setup FIS natively. (RO)
29	SSNTF	Supports SNotification Register DWC_ahsata supports P SNTF (SNotification) register and its associated functionality. (RO)
28	SMPS	The bit is Reserved in the current DWC_ahsata configuration, Supports Mechanical Presence Switch This bit is set by the system firmware/BIOS when the platform supports mechanical presence switch for hot plug operation. To use this feature with the DWC_ahsata, the parameter DEV_MP_SWITCH must be set to include in coreConsultant. Otherwise this bit reads 0. Configurable in coreConsultant: This field is implemented when DEV_MP_SWITCH==Include in coreConsultant. When this field is not implemented, this field is reserved, and reads 1b0. (RO)

SATA_CAP (cont.)

Bits	Name	Description
27	SSS	Supports Staggered Spin-up This bit is set by the system firmware/BIOS to indicate platform support for staggered devices spin-up. DWC_ahsata supports this feature through the P CMD.SUD bit functionality. (RO)
26	SALP	Supports Aggressive Link Power Management DWC_ahsata supports auto-generating (Port-initiated) Link Layer requests to the PARTIAL or SLUMBER power management states when there are no commands to process. (RO)
25	SAL	Supports Activity LED DWC_ahsata supports activity indication using signal p _act_led. (RO)
24	SCLO	Supports Command List Override DWC_ahsata supports the P CMD.CLO bit functionality for port multiplier devices enumeration. (RO)
23:20	ISS	Interface Speed Support Selects maximum SATA speed supported: 1.5 GB/sec, 3.0 GB/sec, or 6.0 GB/sec Values: 1.5 GB/sec (1) 3.0 GB/sec (2) 6.0 GB/sec (3) (RO)
19	SNZO	Supports Non-Zero DMA Offsets This feature is not supported. (RO)
18	SAM	Supports AHCI Mode Only DWC_ahsata supports AHCI mode only and does not support legacy, task-file based register interface. (RO)
17	SPM	Supports Port Multiplier DWC_ahsata supports command-based switching port multiplier on any of its ports. (RO)
16	RESERVED_BITS16	Reserved (RO)
15	PMD	PIO Multiple DRQ Block DWC_ahsata supports multiple DRQ block data transfers for the PIO command protocol. (RO)

SATA_CAP (cont.)

Bits	Name	Description
14	SSC	Slumber State Capable DWC_ahsata supports transitions to the interface SLUMBER power management state. (RO)
13	PSC	Partial State Capable DWC_ahsata supports transitions to the interface PARTIAL power management state. (RO)
12:8	NCS	Number of Command Slots DWC_ahsata supports 32 command slots per Port. (RO)
7	CCCS	Command Completion Coalescing Support DWC_ahsata supports command completion coalescing. (RO)
6	EMS	Enclosure Management Support DWC_ahsata does not support enclosure management. (RO)
5	SXS	Supports External SATA The options for this field are: 0x1: Indicates that the DWC_ahsata has one or more Ports that has a signal only connector (power is not part of that connector) that is externally accessible. When this bit is set to 1, the software can refer to the P CMD.ESP bit to determine whether a specific Port has its signal connector externally accessible. 0x0: Indicates that the DWC_ahsata has no Ports that have a signal only connector externally accessible. Reset Value: 0x1: when any of the P CMD.ESP=1 0x0: when all of the P CMD.ESP=0 (RO)
4:0	NP	Number of Ports 0s based value indicating the number of Ports supported by the DWC_ahsata: The options for this field are: 0x00: 1 Port 0x01: 2 Ports 0x02: 3 Ports ...etc. Reset Value: Configurable (AHSATA_NUM_PORTS-1) (RO)

0x29000004 SATA_GHC

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x8000_0000

SATA_GHC

Bits	Name	Description
31	AE	AHCI Enable This bit is always set since DWC_ahsata supports only AHCI mode as indicated by the CAP.SAM=1. (RO) Register type: Read
30:2	RESERVED_BITS30_2	Reserved (RO) Register type: Read
1	IE	Interrupt Enable This global bit enables interrupts from the DWC_ahsata. When cleared, all interrupt sources from all the Ports are disabled (masked). When set, interrupts are enabled and any DWC_ahsata interrupt event causes intrq output assertion. This field is reset on Global reset (GHC.HR=1). (RW) Register type: Read/Write
0	HR	HBA Reset When set by the software, this bit causes an internal Global reset of the DWC_ahsata. All state machines that relate to data transfers and queueing return to an idle state, and all the Ports are re-initialized by sending COMRESET when staggered spin-up is not supported. When staggered spin-up is supported, the software must spin-up each Port after this reset has completed. The DWC_ahsata clears this bit when the reset action is done. A software write of 0 has no effect. (WO) Register type: Write

0x29000008 SATA_IS

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_00000

SATA_IS

Bits	Name	Description
31:2	RESERVED_BITS31_2	Reserved (RO) Register type: Read
1:0	IPS	Interrupt Pending Status When set, this bit indicates that the corresponding Port or Command Completion Coalescing (CCC) logic has an interrupt pending. The software can use this information to determine which ports require service after an interrupt. The bits of this field are set by the ports that have interrupt events pending in the P IS bits and enabled by the P IE or CCC interrupt is generated. Set bits are cleared by the software writing 1 to all bits to clear. (RW1C) Register type: Read/Write (1 clear)

0x2900000C SATA_PI

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x00000000

This register indicates which Ports are exposed by the DWC_ahsata and are available for the software to use. It is loaded by the BIOS. For example, when the DWC_ahsata supports 8 Ports as indicated in the CAP.NP, only Ports 1, 3, 5, and 7 could be available, while Ports 0, 2, 4, and 6 unavailable.

SATA_PI

Bits	Name	Description
31:1	RESERVED_BITS31_1	Reserved (RO) Register type: Read

SATA_PI (cont.)

Bits	Name	Description
0	PI	Ports Implemented This register is bit significant. 1: The corresponding Port is available for the software to use. 0: The Port is not available for the software to use. The maximum number of bits that can be set to 1 is CAP.NP+1. At least one bit must be set to 1. NOTE The contents of this register are relevant to the CCC_PORTS (Command Completion Coalescing Ports) register. The PI register is HwInit. This means that the value is initialized at reset by a system firmware (BIOS). These bits are write-once after power-on reset, then they become read-only. (RO) Register type: Read/Write

0x29000010 SATA_VS

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x00010300

This register indicates the major and minor version of the AHCI specification that the DWC_ahsata implementation supports. The DWC_ahsata supports version 1.30.

BIST register locations (BISTAFR, BISTCR, BISTFCTR, BISTSR, and BISTDECR) are shared between the DWC_ahsata Ports. Before accessing any of the BIST registers, the software must first select the required Port by writing the Port number to the TESTR.PSEL field.

SATA_VS

Bits	Name	Description
31:16	MJR	Major Version Number Indicates that the major AHCI version is 1. (RO)
15:0	MNR	Minor Version Number Indicates that the minor AHCI version is 30. (RO)

0x29000014 SATA_CCC_CTL

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x00010108

This register is used to configure the command completion coalescing (CCC) feature for the DWC_ahsata core. It is reset on global reset.

SATA_CCC_CTL

Bits	Name	Description
31:16	TV	Time-out Value This field specifies the CCC time-out value in 1 ms intervals. The software loads this value prior to enabling CCC. The options for this field are: RW when CCC_CTL.EN==0. RO when CCC_CTL.EN==1. A time-out value of 0x0000 is reserved and should not be used. (RW/RO) Register type: Read/Write
15:8	CC	Command Completions This field specifies the number of command completions that are necessary to cause a CCC interrupt. The value 0x00 for this field disables CCC interrupts being generated based on the number of commands completed. In this case, CCC interrupts are only generated based on the timer. The software loads this value prior to enabling CCC: Field access is: RW when CCC_CTL.EN==0 RO when CCC_CTL.EN==1 (RW/RO) Register type: Read/Write
7:3	INT	Interrupt This field specifies the interrupt used by the CCC feature, using the number of Ports configured for the core. For example, when AHSATA_NUM_PORTS==6 then This field CCC_CTL.INT==6. When a CCC interrupt occurs, the field IS.IPS[INT] is set to 1. (RO) Register type: Read
2:1	RESERVED_BITS2_1	Reserved (RO) Register type: Read

SATA_CCC_CTL (cont.)

Bits	Name	Description
0	EN	Enable The options for this field are: 0x0: CCC feature is disabled and no CCC interrupts are generated. 0x1: CCC feature is enabled and CCC interrupts may be generated based on the time-out or command completion conditions. NOTE When field CCC_CTL.EN==1, the software can not change the fields CCC_CTL.TV and CCC_CTL.CC. (RW) Register type: Read/Write

0x29000018 SATA_CCC_PORTS

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This register specifies the Ports that are coalesced as part of the command completion coalescing (CCC) feature when CCC_CTL.EN==1. It is reset on global reset.

SATA_CCC_PORTS

Bits	Name	Description
31:0	PRT	Ports This field is bit significant. Each bit corresponds to a particular Port, where bit 0 corresponds to Port0. The options for this field are: 1: the corresponding Port is part of the CCC feature. 0: the corresponding Port is not part of the CCC feature. Bits set to ’1’ in this register must also have the corresponding bit set to ’1’ in the PI (Ports Implemented Register). (RW)

0x29000024 SATA_CAP2

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0004

This register indicates capabilities of the DWC_ahsata core to the software.

SATA_CAP2

Bits	Name	Description
31:3	RESERVED_BITS31_3	Reserved (RO)
2	APST	Automatic Partial to Slumber Transitions DWC_ahsata supports automatic partial to slumber transitions. (RO)
1:0	RESERVED_BITS1_0	Reserved (RO)

0x290000A0 SATA_BISTAFR

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This register contains the pattern definition (bits [23:16] of the first DWORD) and data pattern (bits [7:0] of the second DWORD) fields of the received BIST Activate FIS. These fields define the DWC_ahsata loopback responder mode requested by the device. It is updated every time a new BIST Activate FIS is received from the device. Reset on Global or Port reset.

SATA_BISTAFR

Bits	Name	Description
31:16	RESERVED_BITS31_16	Reserved (RO)
15:8	NCP	Non-compliant pattern Least significant byte of the received BIST Activate FIS second DWORD (bits [7:0]). This value defines the required pattern for far-end transmit only mode (BISTAFR.PD=0x80 or 0xA0): 0xF1: Low transition density pattern (LTDP) 0xB5: High transition density pattern (HTDP) 0xAB: Low frequency spectral component pattern (LFSCP) 0x7F: Simultaneous switching outputs pattern (SSOP) 0x8B: Lone bit pattern (LBP) 0x78: Mid frequency test pattern (MFTP) 0x4A: High frequency test pattern (HFTP) 0x7E: Low frequency test pattern (LFTP) When none of these values is decoded, the simultaneous switching pattern is transmitted by default. (RO)

SATA_BISTAFR (cont.)

Bits	Name	Description
7:0	PD	Pattern Definition Indicates the pattern definition field of the received BIST Activate FIS - bits [23:16] of the first DWORD. It is used to put the DWC_ahsata in one of the following BIST modes: 0x10: Far-end retimed 0x08: Far-end analog (when PHY supports this mode) 0x80: Far-end transmit only 0xA0: Far-end transmit only with scrambler bypassed All other values should not be used by the device, otherwise, the FIS is negatively acknowledged with R_ERRp. For far-end transmit only modes BISTAFR.NCP field contains the required data pattern. (RO)

0x290000A4 SATA_BISTCR

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x0000_0700

This register is used in BIST initiator modes. It is loaded by the host software prior to sending BIST Activate FIS to the device (via TXBISTPD write). It is reset on a Global or Port reset.

SATA_BISTCR

Bits	Name	Description
31:25	RESERVED_BITS31_25	Reserved (RO) Register type: Read
24	LATE_PHY_READY	Late phy_ready When set, this bit changes monitoring of phy_ready to be the □OR□ of phy_ready or phy_rx_data_vld so that a □late arriving□, or even never asserting□ phy_ready, still functions when RX_OOB_MODE = □Exclude□. This requires that phy_rx_data_vld does not become valid until after the PHY has locked onto post OOB incoming ALIGNs, and the ALIGNs are valid from the PHY. This will not work if phy_rx_data_vld is asserted during OOB data bursts. This behavior is intended for PHYs that assert phy_ready late, but will also work if phy_ready never asserts or is not present. This bit is read/write when RX_OOB_MODE=□Exclude□ and read-only when RX_OOB_MODE=□Include□. (RW) Register type: Read/Write

SATA_BISTCR (cont.)

Bits	Name	Description
23:21	RESERVED_BITS23_21	Reserved (RO) Register type: Read
20	FERLB	Far-end Retimed Loopback When set, this bit is used to put the DWC_ahsata Link into Far-end Retimed mode, without the BIST Activate FIS, regardless whether the device is connected or disconnected (Link in NOCOMM state). This field is one-shot type and reads returns 0. (WO) Register type: Write
19	RESERVED_BIT19	Reserved (RO) Register type: Read
18	TXO	Transmit Only This bit is used to initiate transmission of one of the non-compliant patterns defined by the BISTCR.PATTERN value when the device is disconnected. (WO) Register type: Write
17	CNTCLR	Counter Clear This bit clears BIST error count registers. It is treated as one-shot and reads as 0: No Clear 1: Clear BISTFCTR, BISTSR, and BISTDECR registers. (WO) Register type: Write
16	NEALB	Near-end Analog Loopback This bit places the Port PHY into near-end analog loopback mode. It is treated as one-shot and reads as 0: No Near-end analog loopback 1: Near-end analog loopback request. BISTCR.PATTERN field contains the appropriate pattern. This mode should be initiated either in the PARTIAL or SLUMBER power mode, or with the device disconnected from the Port PHY (Link NOCOMM state). BIST Activate FIS is not sent to the device in this mode. (WO) Register type: Write

SATA_BISTCR (cont.)

Bits	Name	Description
15	LLB	Lab Loopback Mode When set, masks out phy_sig_det from the OOB Detector in BIST Loopback Mode, and the only way to exit BIST Loopback mode is to clear the register bit (requires access to the Device AMBA register interface), then issue COMRESET or receive COMINIT as normal. Alternately, a power on reset will automatically clear the BIST Loopback Mode register bit. (RW) Register type: Read/Write
14	QPHYINIT	The bit is Reserved in the current DWC_ahsata configuration, Quick PHY Init Enable When set, this bit enables quick PHY initialization feature. The Link does not require any ALIGNs to transition from OOB to normal operation. Note: This bit is available only when TX_OOB_MODE = Exclude (0) and ALIGN_MODE = Aligned (1), otherwise it is reserved. (RW) Register type: Read/Write
13	ERRLOSSEN	Error Loss Detect Enable This bit is set on power-up or asynchronous reset if PHY_INTERFACE_TYPE=Synopsys_SATA_6G (2) or PHY_INTERFACE_TYPE = Synopsys_SATA_6G_FPGA_TestChip (3). Note: This feature is present only when RX_OOB_MODE = Include, however, the bit is present in any configuration. This bit controls OOB initialization behavior and signal loss detection for use with Synopsys 6G PHY. Do not change the value of this register bit. (RW) Register type: Read/Write
12	SDFE	Signal Detect Feature Enable 1: Link layer feature to handle unstable/absent phy_sig_det signal is enabled 0: Link layer feature to handle unstable/absent phy_sig_det signal is disabled. This bit is cleared on power-up or asynchronous reset until it is set via programming. It is not affected by a Global reset or COMRESET. Note: For special handling in systems where phy_sig_det may not be present or stable after OOB signalling and during normal operation. For these systems, phy_rx_data_vld must not be tied high and must go low when no data is detected on the wires. (RW) Register type: Read/Write

SATA_BISTCR (cont.)

Bits	Name	Description
11	RESERVED_BIT11	Reserved (RO) Register type: Read
10:8	LLC	Link Layer Control This field controls the Port Link Layer functions: scrambler, descrambler, and repeat primitive drop. Note the different meanings for normal and BIST modes of operation: Bit8SCRAM The options for this field are: 0: Scrambler disabled in normal mode, enabled in BIST mode 1: Scrambler enabled in normal mode, disabled in BIST mode Bit9DESCRAM The options for this field are: 0: Descrambler disabled in normal mode, enabled in BIST mode 1: Descrambler enabled in normal mode, disabled in BIST mode Bit10RPD The options for this field are: 0: Repeat primitive drop function disabled in normal mode, enabled in BIST mode 1: Repeat primitive drop function enabled in normal mode, disabled in BIST mode The SCRAM bit is cleared (enabled) by the Port when the Port enters a responder far-end transmit BIST mode with scrambling enabled (BISTAFR.PD=0x80). In normal mode, the functions scrambler, descrambler, or RPD can be changed only during Port reset (P SCTL.DET=0x1) (RW) Register type: Read/Write
7	RESERVED_BITS7	Reserved (RO) Register type: Read
6	ERREN	Error Enable This bit is used to allow or filter (disable) PHY internal errors outside the FIS boundary to set corresponding P SERR bits. The options for this field are: 0: Filter errors outside the FIS, allow errors inside the FIS; 1: Allow errors outside or inside the FIS. (RW) Register type: Read/Write
5	FLIP	Flip disparity This bit is used to change disparity of the current test pattern to the opposite every time its state is changed by the software. (RW) Register type: Read/Write

SATA_BISTCR (cont.)

Bits	Name	Description
4	PV	Pattern Version This bit is used to select either short or long version of the SSOP, HTDP, LTDP, LFSCP, COMP patterns. The options for this field are: 0: Short pattern version 1: Long pattern version (RW) Register type: Read/Write
3:0	PATTERN	This field defines one of the following SATA compliant patterns for far-end retimed/ far-end analog/ near-end analog initiator modes, or non-compliant patterns for transmit-only responder mode when initiated by the software writing to the BISTCR.TXO bit. The options for this field are: 0000b: Simultaneous switching outputs pattern (SSOP) 0001b: High transition density pattern (HTDP) 0010b: Low transition density pattern (LTDP) 0011b: Low frequency spectral component pattern (LFSCP) 0100b: Composite pattern (COMP) 0101b: Lone bit pattern (LBP) 0110b: Mid frequency test pattern (MFTP) 0111b: High frequency test pattern (HFTP) 1000b: Low frequency test pattern (LFTP) All other values are reserved and should not be used. If the value is none of the listed above, Composite pattern (COMP) is transmitted by default. (RW) Register type: Read/Write

0x290000A8 SATA_BISTFCTR

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This register contains the received BIST FIS count in the loopback initiator far-end retimed, far-end analog and near-end analog modes. It is updated each time a new BIST FIS is received. It is reset by Global reset, Port reset (COMRESET) or by setting the BISTCR.CNTCLR bit. This register does not roll over and freezes when the FFFF_FFFFh value is reached. It takes approximately 65 hours of continuous BIST operation to reach this value.

SATA_BISTFCTR

Bits	Name	Description
31:0	CNT	Received BIST FIS count (RO)

0x290000AC SATA_BISTSR

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This register contains errors detected in the received BIST FIS in the loopback initiator far-end retimed, far-end analog and near-end analog modes. It is updated each time a new BIST FIS is received. It is reset by Global reset, Port reset (COMRESET) or by setting the BISTCR.CNTCLR bit.

SATA_BISTSR

Bits	Name	Description
31:24	RESERVED_BITS31_24	Reserved (RO)
23:16	BRSTERR	Burst Error This field contains the burst error count. It is accumulated each time a burst error condition is detected: DWORD error is detected in the received frame and 1.5 seconds (27,000 frames) passed since the previous burst error was detected. The BRSTERR value does not roll over and freezes at FFh. This field is updated when parameter BIST_MODE=DWORD.(RO)
15:0	FRAMERR	Frame Error This field contains the frame error count. It is accumulated (new value is added to the old value) each time a new BIST frame with a CRC error is received. The FRAMERR value does not roll over and freezes at FFFFh.(RO)

0x290000B0 SATA_BISTDECR

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This register contains the number of DWORD errors detected in the received BIST frame in the loopback initiator far-end retimed, far-end analog and near-end analog modes. It is updated each time a new BIST frame is received. It is reset by Global reset, Port reset (COMRESET) or by setting the BISTCR.CNTCLR bit. This register is updated only when the parameter BIST_MODE=DWORD.

SATA_BISTDECR

Bits	Name	Description
31:0	DWERR	DWORD Error Count This field contains the DWORD error count. It is accumulated (new value is added to the old value) each time a new BIST frame is received. The DWERR value does not roll over and freezes when it exceeds 0xFFFF_F000. (RO)

0x290000B4 SATA_DIAGNR

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0003_E000

The register is for debug purposes only (not documented register in Synopsys Databook).

This register reflects the states of the DWC_ahsata FSMs and couple bits from the TCHK Transport errors.

SATA_DIAGNR

Bits	Name	Description
31	E31	err_rxfov (RW1C) Register type: Read/Write (1 clear)
30	E30	tlerr_alps (RW1C) Register type: Read/Write (1 clear)
29	RESERVED_BITS29	Reserved (RO) Register type: Read
28:24	LSM	Link State Machine State Link state machine current state (RO) Register type: Read Only
23:19	TCHK	TCHK State Machine State (RO) Register type: Read Only

SATA_DIAGNR (cont.)

Bits	Name	Description
18:13	TSM	Tx State Machine State (RO) Register type: Read Only
12:7	RFSM	Rx FIS State Machine State (RO) Register type: Read Only
6:0	PDMASM	Port DMA State Machine State (RO) Register type: Read Only

0x290000B8 SATA_DIAGNR1

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

The register is for debug purposes only (not documented register in Synopsys Databook).

This register reflects the states of the DWC_ahsata FSMs and couple of other debug info.

SATA_DIAGNR1

Bits	Name	Description
31	LINK_PRIM_ERR	Link Primitive Error (RO) Register type: Read Only
30	LINK_DATA_DISP	Link Data Disparity Error (RO) Register type: Read Only
29	LINK_DATA_DEC	Link Data 10b8b Decoding Error (RO) Register type: Read Only
28	CMD_ABORT	Cmd Abort status in Reg or SDB FIS (e.g. 51h) (RO) Register type: Read Only

SATA_DIAGNR1 (cont.)

Bits	Name	Description
27	CMD_GOOD	Cmd Good status in Reg or SDB FIS (e.g. 50h) (RO) Register type: Read Only
26	LINK_BAD	Link Bad End (WTRM instead of EOF) Error (RO) Register type: Read Only
25	TLERR_BLPS	TL before Link/Phy error (RW1C) Register type: Read/Write (1 clear)
24:20	RESERVED_BITS24_20	Reserved (RO) Register type: Read Only
19	SHORT_TO	Error loss test bit (short timeout) (RW) Register type: Read/Write
18	RESERVED_BITS18	Reserved (RO) Register type: Read
17	PRD_PREF_DIS	PRD Prefetch Disable (RW) Register type: Read/Write
16	RESERVED_BITS16	Reserved (RO) Register type: Read
15:8	RXFISM_LBFS	PDMA RXFISM last state before PORTSM Fatal (RO) Register type: Read Only
7:0	PORTSM_LBFS	PDMA PORTSM last state before Fatal (RO) Register type: Read Only

0x290000BC SATA_OOBR

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x070E182B

This register controls the Link layer OOB detection counters. The default values, MIN_COMWAKE, MAX_COMWAKE, MIN_COMINIT and MAX_COMINIT are calculated based on the RXOOB_CLK_FREQ parameter and loaded on power-up or asynchronous DWC_ahsata reset.

SATA_OOBR

Bits	Name	Description
31	WE	Write Enable The options for this field are: 1: OOBR bits [30:0] can be written 0: OOBR bits [30:0] are read-only This bit is cleared when COMRESET is detected. (RW)
30:24	CWMIN	COMWAKE Minimum value (Default = 7'd6) This field is RW when WE=1 and RO when WE=0. (RW/RO)
23:16	CWMAX	COMWAKE Maximum value (Default = 7'd16) This field is RW when WE=1 and RO when WE=0 (RW/RO)
15:8	CIMIN	COMINIT Minimum value (Default = 7'd18) This field is RW when WE=1 and RO when WE=0. (RW/RO)
7:0	CIMAX	COMINIT Maximum value (Default = 7'd51) This field is RW when WE=1 and RO when WE=0. (RW/RO)

0x290000D0 GPCR

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

General Purpose Control Register

This 32-bit register is used for general purpose control. This register only exists when GP_CTRL parameter s set to □Include□ otherwise this location is reserved. The bits of this register are connected to the corresponding bits of the gp_ctrl output. Resets on power-up (system reset) only to the GP_CTRL_DEF value.

GPCR

Bits	Name	Description
31:0	GP_CTRL	bit31: sel_1k ’ when set(1), 1K boundary is preserved by SATA AXI master, in order to support QSB limitation. ’ when clear(0), 4K boundary is supported by SATA AXI master, as AXI 1.0 requires. bits30:0: for future use (RW) Register type: Read/Write

0x290000D4 GPSR

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x1002_0000

General Purpose Status Register

This 32-bit register is used to monitor the general purpose status. This register only exists when GP_STAT parameter is set to □Include□, otherwise, this location is reserved.

The bits of this register reflect the state of the corresponding bits of the gp_status input. Signals connected to the gp_status input can be asynchronous to any of the DWC_ahsata clocks, however they must not change faster than five hclk/aclk periods, otherwise the GPSR register may never be updated with the intermediate changing values.

The register contains the HW version of SATA controller, as defined in IP Catalog Guidelines.

GPSR

Bits	Name	Description
31:28	MAJOR	Indicates different interface version. Major version changes are not backward compatible. There will be a new Programming Guide document per major revision (RO) Register type: Read Only
27:16	MINOR	Indicates expanded functionality. Minor version adds functionality while being backward compatibility for existing features. (RO) Register type: Read Only
15:0	STEP	Indicates a change in the HW which is not intended to impact SW compatibility. (RO) Register type: Read Only

0x290000E0 SATA_TIMER1MS

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x0001_86A0

This register is used to generate a 1-ms tick for the command completion coalescing (CCC) logic, based on the AMBA bus clock frequency. The Software must initialize this register with the required value after power up before using the CCC feature. This register is reset to 100,000d (TIMV value for 100-MHz hclk/aclk) on power up and is not affected by Global reset.

SATA_TIMER1MS

Bits	Name	Description
31:20	RESERVED_BITS31_20	Reserved (RO) Register type: Read
19:0	TIMV	1ms Timer Value This field contains the following value for the internal timer to generate 1-ms tick: Fappclk*1000 where Fappclk = AMBA clock frequency in MHz The options for this field are: RW when CCC_CTL.EN=0 RO when CCC_CTL.EN=1. (RW/RO) Register type: Read/Write

0x290000E8 SATA_GPARAM1R

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x5C10_2409

SATA_GPARAM1R

Bits	Name	Description
31	ALIGN_M	Rx Data Alignment This value is derived from the ALIGN_MODE parameter. The options for this field are: 0: Misaligned 1: Aligned (RO)

SATA_GPARAM1R (cont.)

Bits	Name	Description
30	RX_BUFFER	Rx Data Buffer This value is derived from the RX_BUFFER_MODE parameter: 0: Exclude 1: Include (RO)
29:28	PHY_DATA	PHY Data Width This value is derived from the PHY_DATA_WIDTH parameter: The options for this field are: 0x0: 1 0x1: 2 0x2: 4 Other values are reserved. (RO)
27	PHY_RST	PHY Reset Mode This value is derived from the PHY_RST_MODE parameter. The options for this field are: 0: Low 1: High (RO)
26:21	PHY_CTRL	PHY Control Width This value reflects the PHY_CTRL_W parameter. (RO)
20:15	PHY_STAT	PHY Status Width This value reflects the PHY_STAT_W parameter. (RO)
14	LATCH_M	LATCH_M: This value is derived from the LATCH_MODE parameter: The options for this field are: 0: Exclude 1: Include (RO)
13	BIST_M	BIST Loopback Checking Depth This value is derived from the BIST_MODE parameter. The options for this field are: 0: FIS 1: DWORD (RO)

SATA_GPARAM1R (cont.)

Bits	Name	Description
12:11	PHY_TYPE	PHY Interface Type This value is derived from the PHY_INTERFACE_TYPE parameter: The options for this field are: □ 0x0: Configurable □ 0x1: Synopsys_SATA_II □ 0x2: Synopsys_SATA_6G □ 0x3: Synopsys_SATA_6G_FPGA_TestChip (RO)
10	RETURN_ERR	AMBA Error Response This value is derived from the RETURN_ERR_RESP parameter: The options for this field are: 0: False 1: True (RO)
9:8	AHB_ENDIAN	AHB Bus Endianness This value is derived from the AHB_ENDIANESS parameter: The options for this field are: 0: Little 1: Big 2: Dynamic (RO)
7	S_HADDR	AMBA Slave Address Bus Width This value is derived from the S_HADDR_WIDTH parameter: The options for this field are: 0: 32 bits 1: 64 bits (RO)
6	M_HADDR	AMBA Master Address Bus Width This value is derived from the M_HADDR_WIDTH parameter: The options for this field are: 0: 32 bits 1: 64 bits (RO)
5:3	S_HDATA	AMBA Slave Data Bus Width This value is derived from the S_HDATA_WIDTH parameter: The options for this field are: 0: 32 bits 1: 64 bits 2: 128 bits 3: 256 bits (RO)

SATA_GPARAM1R (cont.)

Bits	Name	Description
2:0	M_HDATA	AMBA Master Data Bus Width This value is derived from the M_HDATA_WIDTH parameter: The options for this field are: 0: 32 bits 1: 64 bits 2: 128 bits 3: 256 bits (RO)

0x290000EC SATA_GPARAM2R

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_1E64

This read-only register contains encoded information about the DWC_ahsata global configuration parameters settings.

SATA_GPARAM2R

Bits	Name	Description
31:15	RESERVED_BITS31_15	Reserved (RO)
14	DEV_CP	Cold Presence Detect This value is derived from the DEV_CP_DET parameter. The options for this field are: 0: Exclude 1: Include (RO)
13	DEV_MP	Mechanical Presence Switch This value is derived from the DEV_MP_SWITCH parameter. The options for this field are: 0: Exclude 1: Include (RO)
12	ENCODE_M	8b/10b Encoding/Decoding This value is derived from the ENCODE_MODE parameter. The options for this field are: 0: Exclude 1: Include (RO)

SATA_GPARAM2R (cont.)

Bits	Name	Description
11	RXOOB_CLK_M	Rx OOB Clock Mode This value is derived from the RXOOB_CLK_MODE parameter, The options for this field are: 0: RxClock 1: Separate (RO)
10	RX_OOB_M	Rx OOB Mode This value is derived from the RX_OOB_MODE parameter: The options for this field are: 0: Exclude 1: Include (RO)
9	TX_OOB_M	Tx OOB Mode This value is derived from the TX_OOB_MODE parameter: The options for this field are: 0: Exclude 1: Include (RO)
8:0	RXOOB_CLK	Rx OOB Clock Frequency This value reflects the hexadecimal value of the RXOOB_CLK_FREQ parameter. (RO)

0x290000F0 SATA_PPARAMR

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x00000a77

This read-only register contains encoded information about the selected port configuration parameters settings. The port is selected by the TESTR.PSEL field.

SATA_PPARAMR

Bits	Name	Description
31:12	RESERVED_BITS31_12	Reserved (RO)
11	TX_MEM_M	Tx FIFO Memory Read Port Type This value is derived from the P _TX_MEM_MODE parameter: The options for this field are: 0: Async 1: Sync (RO)

SATA_PPARAMR (cont.)

Bits	Name	Description
10	TX_MEM_S	Tx FIFO Memory Type This value is derived from the P _TX_MEM_SELECT parameter: The options for this field are: 0: External 1: Internal (RO)
9	RX_MEM_M	Rx FIFO Memory Read Port Type This value is derived from the P _RX_MEM_MODE parameter: The options for this field are: 0: Async 1: Sync (RO)
8	RX_MEM_S	Rx FIFO Memory Type This value is derived from the P _RX_MEM_SELECT parameter: The options for this field are: 0: External 1: Internal (RO)
7:4	TXFIFO_DEPTH	TX FIFO Depth (in FIFO words) This value is derived from the P _TXFIFO_CAP and M_HDATA_WIDTH parameters: The options for this field are: 0x0 - 0x2: Reserved 0x3: 8 0x4: 16 0x5: 32 0x6: 64 0x7: 128 0x8: 256 0x9: 512 0xA: 1024 0xB: 2048 0xC - 0xF: Reserved (RO)

SATA_PPARAMR (cont.)

Bits	Name	Description
3:0	RXFIFO_DEPTH	RX FIFO Depth (in FIFO words) This value is derived from the P _RXFIFO_CAP and M_HDATA_WIDTH parameters: The options for this field are: 0x0 - 0x3: Reserved 0x4: 16 0x5: 32 0x6: 64 0x7: 128 0x8: 256 0x9: 512 0xA: 1024 0xB: 2048 0xC - 0xF: Reserved (RO)

0x290000F4 SATA_TESTR

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This register is used to put the DWC_ahsata slave interface into a test mode and to select a Port for BIST operation.

SATA_TESTR

Bits	Name	Description
31:19	RESERVED_BITS31_19	Reserved (RO) Register type: Read
18:16	PSEL	Port Select This field is used to select a Port for BIST operation. The options for this field are: 0x0: Port0 is selected 0x1: Port1 is selected 0x2: Port2 is selected 0x3: Port3 is selected 0x4: Port4 is selected 0x5: Port5 is selected 0x6: Port6 is selected 0x7: Port7 is selected (RW) Register type: Read/Write

SATA_TESTR (cont.)

Bits	Name	Description
15:1	RESERVED_BITS15_1	Reserved (RO) Register type: Read

SATA_TESTR (cont.)

Bits	Name	Description
0	TEST_IF	TEST_IF: Test Interface This bit is used to put the DWC_ahsata slave interface into the test mode: The options for this field are: 0: Normal mode: the read back value of some registers is a function of the DWC_ahsata state and does not match the value written. 1: Test mode: the read back value of the registers matches the value written. Normal operation is disabled. The following registers can be accessed in this mode: - GHC register IE bit - BISTAFR register NCP and PD bits become read-write - BISTCR register LLC, ERREN, FLIP, PV, PATTERN - BISTFCTR, BISTSR, BISTDECR become read-write - P CLB/CLBU, P FB/FBU registers - P IS register RW1C and UFS bits become read-write - P IE register RW bits (CPDE is RO if DEV_CP_DET = Exclude, DMPE bit is RO if DEV_MP_SWITCH = Exclude) - P CMD register ASP, ALPE, DLAE, ATAPI, PMA bits - P TFD, P SIG registers become read-write - P SCTL register RW bits [9:8], [5:4], and [2:0] (Bits [2:0] can't be written with the 3'b001 value if P CMD.SUD=0) - P SERR register RW1C bits become read-write bits - P SACT, P CI, P SNTF registers become read-write - P DMACR register - P PHYCR register - P PHYSR register becomes read-write - GPSR register becomes read-write (if it is included by GP_STAT=Include(1)) Notes: Interrupt is asserted when any of the IS register bits is set after setting the corresponding P IS and P IE registers and GHC.IE = 1. CAP.SMPS/SSS, PI, P CMD.ESP/CPD/MPSP/HPCP register bits are HwInit type and can not be used in Test mode. They are written once after power-on reset and become read-only. Global DWC_ahsata reset must be issued (GHC.HR=1) after TEST_IF bit is cleared following the Test mode operation. (RW) Register type: Read/Write

0x290000F8 SATA_VERSIONR

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x3332_302a

This 32-bit read-only register contains hard-coded hexadecimal DWC_ahsata component version value set by the AHSATA_VERSION_NUM parameter. The value represents an ASCII code of the version number. For example, version 1.24* is coded as 0x3132_342A.

SATA_VERSIONR

Bits	Name	Description
31:0	VERSION_NUM	DWC_ahsata hard-coded hexadecimal version value. (RO)

0x290000FC SATA_IDR

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_008C

This register contains a hard-coded hexadecimal DWC_ahsata identification value, as determined by the configuration parameter External User Core ID Port:

SATA_IDR

Bits	Name	Description
31:0	CORE_ID	DWC_ahsata hard-coded hexadecimal identification value. (RO)

18.2.2 Port register descriptions

0x29000100 SATA_P0CLB

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

SATA_P0CLB

Bits	Name	Description
31:10	CLB	Command List Base Address Indicates the 32-bit base physical address for the command list for this Port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1Kbyte in length. This address must be 1Kbyte-aligned as indicated by bits [9:0] being read only. (RW) Register type: Read/Write
9:0	RESERVED_BITS9_0	Reserved (RO) Register type: Read

0x29000104 SATA_P0CLBU

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This register exists when M_HADDR_WIDTH=64, otherwise this location is reserved.

SATA_P0CLBU

Bits	Name	Description
31:0	CLBU	Command List Base Address Upper Indicates the upper 32 bits for the command list base physical address for this Port. This base is used when fetching commands to execute. (RW)

0x29000108 SATA_P0FB

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

SATA_P0FB

Bits	Name	Description
31:8	FB	FIS Base Address Indicates the 32-bit base physical address for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256byte-aligned as indicated by bits [7:0] being read only. (RW) Register type: Read/Write
7:0	RESERVED_BITS7_0	Reserved (RO) Register type: Read

0x2900010C SATA_P0FBU

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This register exists when M_HADDR_WIDTH=64, otherwise this location is reserved.

SATA_P0FBU

Bits	Name	Description
31:0	FBU	FIS Base Address Upper Indicates the upper 32 bits for the received FIS base physical address for this Port. (RW)

0x29000110 SATA_P0IS

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This register is used to generate DWC_ahsata interrupt when any of the bits are set. Bits in this register are set by some internal conditions, and cleared by the software writing ones in the positions it wants to clear. This register is reset on Global DWC_ahsata reset.

SATA_P0IS

Bits	Name	Description
31	CPDS	Cold Port Detect Status This bit is set when the p _cp_det input changes its state due to the insertion or removal of the device. This bit is only valid when the Port supports cold presence detect as indicated by the P CMD.CPD set to 1. This field is RW1C when DEV_CP_DET=Include This field is read-only 0 when DEV_CP_DET =Exclude (RW1C/RO) Register type: Read
30	TFES	Task File Error Status This bit is set whenever the P TFD.STS register is updated by the device and the error bit (bit 0) is set. (RW1C) Register type: Read/Write (1 clear)
29	HBFS	Host Bus Fatal Error Status This bit is set when DWC_ahsata AMBA Master detects an ERROR response from the slave. (RW1C) Register type: Read/Write (1 clear)
28	HBDS	Host Bus Data Error Status This bit is always cleared to 0. (RW1C) Register type: Read/Write (1 clear)
27	IFS	Interface Fatal Error Status This bit is set when any of the following conditions is detected: SYNC escape is received from the device during H2D Register or Data FIS transmission; One or more of the following errors are detected during Data FIS transfer - Protocol (P SERR.ERR_P), CRC (P SERR.DIAG_C), Handshake (P SERR.DIAG_H), PHY Not Ready (P SERR.ERR_C); Unknown FIS is received with good CRC, but the length exceeds 64 bytes; PRD table byte count is zero. Port DMA transitions to a fatal state until the software clears P CMD.ST bit or resets the interface by way of Port or Global reset. (RW1C) Register type: Read/Write (1 clear)

SATA_P0IS (cont.)

Bits	Name	Description
26	INFS	Interface Non-fatal Error Status This bit is set when any of the following conditions is detected: One or more of the following errors are detected during non-data FIS transfer - Protocol (P SERR.ERR_P) - CRC (P SERR.DIAG_C), - Handshake (P SERR.DIAG_H) - PHY Not Ready (P SERR.ERR_C); Command list underflow during read operation (i.e., DMA read) when the software builds command table that has more total bytes than the transaction given to the device. In both cases Port operation continues normally. When error is detected during non-data FIS transmission, this FIS is retransmitted continuously until it succeeds, or until the software times out and resets the interface. (RW1C) Register type: Read/Write (1 clear)
25	RESERVED_BITS25	Reserved (RO) Register type: Read
24	OFS	Overflow Status This bit is set when command list overflow is detected during read or write operation when the software builds command table that has fever total bytes than the transaction given to the device. Port DMA transitions to a fatal state until the software clears P CMD.ST bit or resets the interface by way of Port or Global reset. (RW1C) Register type: Read/Write (1 clear)
23	IPMS	Incorrect Port Multiplier Status Indicates that the HBA received a FIS from a device whose Port Multiplier field did not match what was expected. This bit may be set during enumeration of devices on a Port Multiplier due to the normal Port Multiplier enumeration process. The software must use the IPMS bit only after enumeration is complete on the Port Multiplier. (RW1C) Register type: Read/Write (1 clear)
22	PRCS	PHY Ready Change Status This bit reflects the state of the P SERR.DIAG_N bit. When set to 1, indicates the internal p _phy_ready signal changed state. To clear this bit, the software must clear the P SERR.DIAG_N bit to 0. (RO) Register type: Read

SATA_P0IS (cont.)

Bits	Name	Description
21:8	RESERVED_BITS21_8	Reserved (RO) Register type: Read
7	DMPS	Device Mechanical Presence Status This bit is set when the p _mp_switch input changes its state as a result of a mechanical switch attached to this Port opening or closing. Dependencies: This bit is valid only when both CAP.SMPS and P CMD.MPSP are set to 1. This bit is RW1C when DEV_CP_DET=Include. This bit is read-only 0. when DEV_CP_DET=Exclude,', (RW1C/RO) Register type: Read
6	PCS	Port Connect Change Status This bit reflects the state of the P SERR.DIAG_X bit: 0x1: Change in Current Connect Status; 0x0: No change in Current Connect Status. This bit is cleared only when P SERR.DIAG_X is cleared. (RO) Register type: Read
5	DPS	Descriptor Processed A PRD with the I bit set has transferred all of its data. NOTE This is an opportunistic interrupt and must not be used to definitively indicate the end of a transfer. Two PRD interrupts could happen close in time such that the second interrupt is missed when the first PRD interrupt is being cleared. (RW1C) Register type: Read/Write (1 clear)
4	UFS	Unknown FIS Interrupt When set to 1, indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by the software clearing the P SERR.DIAG_F bit to 0. NOTE The UFS bit does not directly reflect the P SERR.DIAG_F bit. P SERR.DIAG_F bit is set immediately when an unknown FIS is detected, whereas the UFS bit is set when that FIS is posted to memory. The software should wait to act on an unknown FIS until the UFS bit is set to 1 or the two bits may become out of sync. (RO) Register type: Read
3	SDBS	Set Device Bits Interrupt A Set Device Bits FIS has been received with the I bit set and has been copied into system memory. (RW1C) Register type: Read/Write (1 clear)

SATA_P0IS (cont.)

Bits	Name	Description
2	DSS	DMA Setup FIS Interrupt A DMA Setup FIS has been received with the I bit set and has been copied into system memory. (RW1C) Register type: Read/Write (1 clear)
1	PSS	PIO Setup FIS Interrupt A PIO Setup FIS has been received with the I bit set, it has been copied into system memory, and the data related to that FIS has been transferred. NOTE This bit is set even when the data transfer resulted in an error. (RW1C) Register type: Read/Write (1 clear)
0	DHRS	Device to Host Register FIS Interrupt A D2H Register FIS has been received with the I bit set and has been copied into system memory. (RW1C) Register type: Read/Write (1 clear)

0x29000114 SATA_P0IE

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This register enables and disables reporting the corresponding interrupt to the software. When a bit is set (1), and the corresponding interrupt condition is active, then the DWC_ahsata intrq output is asserted. Interrupt sources that are disabled (0) are still reflected in the status registers. This register is symmetrical with the P IS register. This register is reset on Global DWC_ahsata reset.

SATA_P0IE

Bits	Name	Description
31	CPDE	Cold Port Detect Enable The options for this field are: When DEV_CP_DET=Include, this bit is read/write. When DEV_CP_DET=Exclude, this bit is read-only 0. Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.CPDS=1 (RW/RO) Register type: Read

SATA_P0IE (cont.)

Bits	Name	Description
30	TFEE	Task File Error Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.TFES=1 (RW) Register type: Read/Write
29	HBFE	Host Bus Fatal Error Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.HBFS=1 (RW) Register type: Read/Write
28	HBDE	Host Bus Data Error Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.HBDS=1 (RW) Register type: Read/Write
27	IFE	Interface Fatal Error Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.IFS=1 (RW) Register type: Read/Write
26	INFE	Interface Non-fatal Error Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.INFS=1 (RW) Register type: Read/Write
25	RESERVED_BITS25	Reserved (RO) Register type: Read

SATA_P0IE (cont.)

Bits	Name	Description
24	OFE	Overflow Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.OFS=1 (RW) Register type: Read/Write
23	IPME	Incorrect Port Multiplier Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.IPMS=1 (RW) Register type: Read/Write
22	PRCE	PHYReady Change Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.PRCS=1 (RW) Register type: Read/Write
21:8	RESERVED_BITS21_8	Reserved (RO) Register type: Read
7	DMPE	Device Mechanical Presence Enable DEV_MP_SWITCH=Include, this bit is read/write. DEV_MP_SWITCH=Exclude, this bit is read-only 0. Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.DMPS=1 (RW/RO) Register type: Read
6	PCE	Port Change Interrupt Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.PCS=1 (RW) Register type: Read/Write

SATA_P0IE (cont.)

Bits	Name	Description
5	DPE	Descriptor Processed Interrupt Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.DPS=1 (RW) Register type: Read/Write
4	UFE	Unknown FIS Interrupt Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.UFS=1 (RW) Register type: Read/Write
3	SDBE	Set Device Bits FIS Interrupt Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.SDBS=1 (RW) Register type: Read/Write
2	DSE	DMA Setup FIS Interrupt Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.DSS=1 (RW) Register type: Read/Write
1	PSE	PIO Setup FIS Interrupt Enable Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.PSS=1 (RW) Register type: Read/Write

SATA_P0IE (cont.)

Bits	Name	Description
0	DHRE	Device to Host Register FIS Interrupt Dependencies: when the following conditions are true, the intrq output signal is asserted: This bit=1 GHC.IE=1 P IS.DHRS=1 (RW) Register type: Read/Write

0x29000118 SATA_P0CMD

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x0000_0004

This register contains bits controlling various Port functions. All RW bits are reset on Global reset.

SATA_P0CMD

Bits	Name	Description
31:28	ICC	Interface Communication Control This field is used to control power management states of the interface. When the Link layer is currently in the L_IDLE state, writes to this field cause the Port to initiate a transition to the interface power management state requested. When the Link layer is not currently in the L_IDLE state, writes to this field have no effect. 0xF - 0x7: Reserved 0x6: Slumber. This causes the Port to request a transition of the interface to the Slumber state. The SATA device can reject the request and the interface remains in its current state. 0x5 - 0x3: Reserved 0x2: Partial. This causes the Port to request a transition of the interface to the Partial state. The SATA device can reject the request and the interface remains in its current state. 0x1: Active. This causes the Port to request a transition of the interface into the active state. 0x0: No-Op/ Idle. This value indicates to the software that the Port is ready to accept a new interface control command, although the transition to the previously selected state may not yet have occurred. When the software writes a non-reserved value other than No-Op (0x0), the Port performs the action and update this field back to Idle (0x0). When the software writes to this field to change the state to a state the link is already in (i.e., interface is in the active state and a request is made to go to the active state), the Port takes no action and returns this field to Idle. When the interface is in a low power state and the software wants to transition to a different low power state, the software must first bring the link to active and then initiate the transition to the desired low power state. NOTE: In the AHCI specification the transition to low power mode is only from the P:Idle state. To get to the P:Idle state, the P0CMD.ST bit has to be set. (RW) Register type: Read/Write

SATA_P0CMD (cont.)

Bits	Name	Description
27	ASP	Aggressive Slumber/ Partial The options for this field are: When set to 1, and P CMD.ALPE=1, the Port aggressively enters the SLUMBER state when one of the following conditions is true: - The Port clears the P CI and the P SACT register is cleared. - The Port clears the P SACT register and P CI is cleared. When cleared to 0, and P CMD.ALPE=1, the Port aggressively enters the PARTIAL state when one of the following conditions is true: - The Port clears the P CI register and the P SACT register is cleared. - The Port clears the P SACT register and P CI is cleared. (RW) Register type: Read/Write
26	ALPE	Aggressive Link Power Management Enable When set to 1, the Port aggressively enters a lower link power state (PARTIAL or SLUMBER) based on the setting of the P CMD.ASP bit. When cleared to 0, aggressive power management state transition is disabled. (RW) Register type: Read/Write
25	DLAE	Drive LED on ATAPI Enable When set to 1, P CMD.ATAPI=1, and commands are active, the Port asserts p _act_led output (RW) Register type: Read/Write
24	ATAPI	Device is ATAPI This bit is used by the Port to control whether to assert p0_act_led output when commands are active The options for this field are: 0: non-ATAPI device 1: ATAPI device (RW) Register type: Read/Write
23	APSTE	Automatic Partial to Slumber Transitions Enable When this bit is set, the DWC_ahsata Link layer transitions from its Partial power management state into Slumber state automatically, regardless whether it was host software-, Port (aggressive)-, or device initiated. (RW) Register type: Read/Write
22	RESERVED_BITS22	Reserved (RO) Register type: Read

SATA_P0CMD (cont.)

Bits	Name	Description
21	ESP	External SATA Port When set to 1, indicates that this Ports signal only connector is externally accessible. When set to 1, CAP.SXS is also set to 1. When cleared to 0, indicates that this Ports signal only connector is not externally accessible. Note: The ESP bit is mutually exclusive with P CMD.HPCP. (RO) Register type: Read
20	CPD	Cold Presence Detection To enable the DWC_ahsata cold presence detection feature, DEV_CP_DET must be set to Include. Otherwise this bit is read-only 0 on reset. The options for this field are: 1: Platform supports cold presence detection on this Port. When this bit is set to 1, P CMD.HPCP must also be set to 1. 0: Platform does not support cold presence detection on this Port. (RO) Register type: Read
19	MPSP	Mechanical Presence Switch Attached to Port To enable the DWC_ahsata mechanical presence detection feature, the DEV_MP_SWITCH parameter must beset to Include, otherwise this bit is read-only 0 on reset. The options for this field are: 1: Indicates the platform supports a mechanical presence switch attached to this Port. 0: Indicates the platform does not support a mechanical presence switch attached to this Port. When this bit is set to 1, P CMD.HPCP should also be set to 1. (RO) Register type: Read
18	HPCP	Hot Plug Capable Port The options for this field are: 1: Indicates that this Ports signal and power connectors are externally accessible via a joint signal-power connector for blindmate device hot plug. 0: Indicates that this Ports signal and power connectors are not externally accessible. Note: The HPCP bit is mutually exclusive with P CMD.ESP. (RO) Register type: Read

SATA_P0CMD (cont.)

Bits	Name	Description
17	PMA	Port Multiplier Attached The software is responsible for detecting whether a Port Multiplier is present; the DWC_ahsata Port does not auto-detect the presence of a Port Multiplier. The options for this field are: 1: A Port Multiplier is attached to this Port. 0: A Port Multiplier is not attached to this Port. (RW) Register type: Read/Write
16	CPS	Cold Presence State This bit reports whether a device is currently detected on this Port as indicated by the p _cp_det input state (assuming P CMD.CPD=1). The options for this field are: 1: device is attached to this Port 0: no device attached to this Port (RO) Register type: Read
15	CR	Command List Running When this bit is set to 1, the command list DMA engine for this Port is running. Register type: Read
14	FR	FIS Receive Running When set to 1, the FIS Receive DMA engine for the Port is running. (RO) Register type: Read
13	MPSS	Mechanical Presence Switch State The software must use this bit only when both CAP.SMPS and P CMD.MPSP are set to 1. This bit reports the state of a mechanical presence switch attached to this Port as indicated by the p _mp_switch input state (assuming CAP.SMPS=1 and P CMD.MPSP=1). The options for this field are: 0: Switch is closed 1: Switch is open When CAP.SMPS=0 then this bit is cleared to 0. (RO) Register type: Read

SATA_P0CMD (cont.)

Bits	Name	Description
12:8	CCS	Current Command Slot This field is set to the command slot value of the command that is currently being issued by the Port. When P CMD.ST transitions from 1 to 0, this field is recleared to 0x00. After P CMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is P CMD.CCS+1. For example, after the Port has issued its first command, when CCS=0x00 and P CI is cleared to 0x3, the next command issued is from command slot 1. This field is valid only when P CMD.ST is set to 1. (RO) Register type: Read
7:5	RESERVED_BITS7_5	Reserved (RO) Register type: Read
4	FRE	FIS Receive Enable When set to 1, the Port may post received FISes into the FIS receive area pointed to by P FB (and P FBU when M_HADDR_WIDTH=64). When cleared, received FISes are not accepted by the Port, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. The software must not set this bit until P FB (P FBU) has been programmed with a valid pointer to the FIS receive area When the software wishes to move the base, this bit must first be cleared, and the software must wait for the P CMD.FR bit to be cleared. (RW) Register type: Read/Write
3	CLO	Command List Override Setting this bit to 1 causes P TFD.STS.BSY and P TFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the P TFD.STS register. This bit is cleared to 0 when P TFD.STS.BSY and P TFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 has no effect. This bit should only be set to 1 immediately prior to setting P CMD.ST bit to 1 from a previous value of 0. Setting this bit to 1 at any other time is not supported and results in indeterminate behavior. (WO) Register type: Write

SATA_P0CMD (cont.)

Bits	Name	Description
2	POD	Power On Device This bit is read/write when cold presence detection is supported on this Port as indicated by P CMD.CPD=1. This bit is read-only 1 when cold presence detection is not supported and P CMD.CPD=0. When set, the Port asserts the p _cp_pod output pin so that it may be used to provide power to a cold-presence detectable Port. (RW/RO) Register type: Read
1	SUD	Spin-Up Device This bit is read/write when staggered spin-up is supported as indicated by the CAP.SSS=1. This bit is read-only 1 when staggered spin-up is not supported and CAP.SSS=0. On an edge detect from 0 to 1, the Port starts a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface. Note: The SUD bit is read-only 0 on power-up until CAP.SSS bit is written with the required value. (RW/RO) Register type: Read
0	ST	Start When set to 1, the Port processes the command list. When cleared, the Port does not process the command list. Whenever this bit is changed from a 0 to a 1, the Port starts processing the command list at entry0. Whenever this bit is changed from a 1 to a 0, the P CI register is cleared by the Port upon transition into an idle state. Refer to AHCI specification, section 10.3.1, for important restrictions on when this bit can be set to 1. Note: P SERR register must be cleared prior to setting ST bit to 1. (RW) Register type: Read/Write

0x29000120 SATA_P0TFD

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_007F

This register contains Error and Status registers updated every time a new Register FIS, PIO Setup FIS, or Set Device Bits FIS is received from the device. Reset on Global or Port reset (COMRESET).

SATA_P0TFD

Bits	Name	Description
31:16	RESERVED_BITS31_16	Reserved (RO)
15:8	ERR	Error This field contains the latest copy of the task file error register. (RO)
7:0	STS	Status This field contains the latest copy of the task file status register. The bits that affect DWC_ahsata operation are: Bit [7] BSY - Indicates the interface is busy Bits [6:4] cs - Command specific Bit [3] DRQ - Indicates a data transfer is requested Bits [2:1] cs - Command specific Bit [0] ERR - Indicates an error during the transfer Note: The Port updates the entire 8-bit field, not just the bits noted above. (RO)

0x29000124 SATA_P0SIG

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0xFFFF_FFFF

SATA_P0SIG

Bits	Name	Description
31:0	SIG	Signature This field contains the signature received from a device on the first D2H Register FIS. The bit order as follows: Bits [31:24] - LBA High (Cylinder High) Register Bits [23:16] - LBA Mid (Cylinder Low) Register Bits [15:8] - LBA Low (Sector Number) Register Bits [7:0] - Sector Count Register This field is updated once after a reset sequence. Reset on Global or Port reset. (RO)

0x29000128 SATA_P0SSTS

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This 32-bit register conveys the current state of the interface and host. The Port updates it continuously and asynchronously. When the Port transmits a COMRESET to the device, this register is updated to its reset values (i.e., Global reset, Port reset, or COMINIT from the device.

SATA_P0SSTS

Bits	Name	Description
31:12	RESERVED_BITS31_12	Reserved (RO)
11:8	IPM	Interface Power Management Indicates the current interface state. The options for this field are: 0x0: Device not present or communication not established 0x1: Interface in active state 0x2: Interface in Partial power management state 0x6: Interface in Slumber power management state All other values are reserved. (RO)
7:4	SPD	Current Interface Speed Indicates the negotiated interface communication speed. The options for this field are: 0x0: Device not present or communication not established 0x1: Generation 1 communication rate negotiated 0x2: Generation 2 communication rate negotiated All other values reserved. (RO)
3:0	DET	Device Detection Indicates the interface device detection and PHY state. The options for this field are: 0x0: No device detected and PHY communication not established 0x1: Device presence detected but PHY communication not established (COMINIT is detected) 0x3: Device presence detected and PHY communication established (PHY Ready is detected) 0x4: PHY in offline mode as a result of the interface being disabled or running in a BIST loopback mode. All other values reserved. (RO)

0x2900012C SATA_P0SCTL

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This 32-bit read-write register is used by the software to control SATA interface capabilities. Writes to this register result in an action being taken by the port PHY interface. Reads from the

register return the last value written to it. Reset on global reset. These bits are static and should not be changed frequently due to the clock crossing between the transport and link layers. The software must wait for at least seven periods of the slower clock (clk_asic or hclk) before changing this register.

SATA_P0SCTL

Bits	Name	Description
31:12	RESERVED_BITS31_12	Reserved (RO) Register type: Read
11:8	IPM	Interface Power Management Transitions Allowed This field indicates which power states the Port PHY interface is allowed to transition to. When an interface power management state is disabled, the Port does not initiate that state and any request from the device to enter that state is rejected via PMNAKp. The options for this field are: 0x0: No interface power management state restrictions 0x1: Transitions to the Partial state disabled 0x2: Transitions to the Slumber state disabled 0x3: Transitions to both Partial and Slumber states disabled All other values reserved and should not be used. (RW) Register type: Read/Write
7:4	SPD	Speed Allowed This field indicates the highest allowable speed of the Port PHY interface. The options for this field are: 0x0: No speed negotiation restrictions 0x1: Limit speed negotiation to Generation 1 communication rate 0x2: Limit speed negotiation to a rate not greater than Generation 2 communication rate All other values reserved and should not be used. Note: When the host software must change this field value, the host must also reset the Port (P SCTL.DET = 0x1) at the same time to ensure proper speed negotiation. (RW) Register type: Read/Write

SATA_P0SCTL (cont.)

Bits	Name	Description
3:0	DET	Device Detection Initialization Controls the Ports device detection and interface initialization. The options for this field are: 0x0: No device detection or initialization action requested 0x1: Perform interface initialization sequence to establish communication. This results in the interface being reset and communication re initialized. 0x4: Disable the Serial ATA interface and put the Port PHY in offline mode. All other values reserved. Note1: This field may only be modified when P CMD.ST is 0. Changing this field while the P CMD.ST=1 results in undefined behavior. When P CMD.ST is set to 1, this field should have a value of 0x0. Note2: The sequence consists of setting DET to 0x1, and after 1 ms clearing DET to 0x0. The actual behavior is little different than that described in the AHCI spec. The difference is that the COMRESET transmission starts only after clearing DET to 0x0, and not after setting DET to 0x1. However, this does not impact the port reset SW sequence. (RW) Register type: Read/Write

0x29000130 SATA_P0SERR

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This 32-bit register represents all the detected interface errors accumulated since the last time it was cleared. The set bits in the SError register indicate that the corresponding error condition became true one or more times since the last time the bit was cleared. The set bits in this register are explicitly cleared by a write operation to the register, Global reset, or Port reset (COMRESET). The value written to clear the set error bits should have ones encoded in the bit positions corresponding to the bits that are to be cleared. All bits in the following table have a reset value of 0.

SATA_P0SERR

Bits	Name	Description
31:27	RESERVED_BITS31_27	Reserved (RO)

SATA_P0SERR (cont.)

Bits	Name	Description
26	DIAG_X	Exchanged This bit is set to 1 when PHY COMINIT signal is detected. This bit is reflected in the P IS.PCS bit. (RW1C) Register type: Read/Write (1 clear)
25	DIAG_F	Unknown FIS Type This bit indicates that one or more FISes were received by the transport layer with good CRC, but had a type field that was not recognized/known and the length was less than or equal to 64 bytes. Note: When the Unknown FIS length exceeds 64 bytes, the DIAG_F bit is not set and the DIAG_T bit is set instead. (RW1C) Register type: Read/Write (1 clear)
24	DIAG_T	Transport State Transition Error This bit indicates that a transport layer protocol violation was detected since the last time this bit was cleared. (RW1C) Register type: Read/Write (1 clear)
23	DIAG_S	Link Sequence Error This bit indicates that one or more link state machine error conditions was encountered. One of the conditions that cause this bit to be set is device doing SYNC escape during FIS transmission. (RW1C) Register type: Read/Write (1 clear)
22	DIAG_H	Handshake Error This bit indicates that one or more R_ERRp was received in response to frame transmission. Such errors may be the result of a CRC error detected by the device, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame. (RW1C) Register type: Read/Write (1 clear)
21	DIAG_C	CRC Error This bit indicates that one or more CRC errors were detected by the Link layer during FIS reception. (RW1C) Register type: Read/Write (1 clear)
20	DIAG_D	Disparity Error This bit is always cleared to 0 since it is not used by the AHCI specification. (RO) Register type: Read

SATA_P0SERR (cont.)

Bits	Name	Description
19	DIAG_B	10B to 8B Decode Error This bit indicates errors were detected by 10b8b decoder. Note: This bit is set only when an error is detected on the received FIS data dword. This bit is not set when an error is detected on the primitive, regardless whether it is inside or outside the FIS. (RW1C) Register type: Read/Write (1 clear)
18	DIAG_W	Comm Wake This bit is set when PHY COMWAKE signal is detected. (RW1C) Register type: Read/Write (1 clear)
17	DIAG_I	PHY Internal Error This bit is set when the PHY detects some internal error as indicated by the assertion of the p _phy_rx_err input. Note: The setting of this bit is controlled by the BISTCR.ERREN bit: when ERREN==0 (default), only errors occurring inside the received FIS cause DIAG_I bit to be set; when ERREN==1, any error inside or outside the FIS causes the DIAG_I bit to be set. (RW1C) Register type: Read/Write (1 clear)
16	DIAG_N	PHY Ready Change This bit indicates that the PHY Ready signal changed state. This bit is reflected in the P IS.PRCS bit. (RW1C) Register type: Read/Write (1 clear)
15:12	RESERVED_BITS15_12	Reserved (RO) Register type: Read
11	ERR_E	Internal Error This bit is set to 1 when one or more AMBA bus ERROR responses are detected on the master interface. (RW1C) Register type: Read/Write (1 clear)
10	ERR_P	Protocol Error This bit is set to 1 when any of the following conditions are detected. Transport state transition error (DIAG_T) Link sequence error (DIAG_S) RxFIFO overflow Link bad end error (WTRM instead of EOF is received). (RW1C) Register type: Read/Write (1 clear)

SATA_P0SERR (cont.)

Bits	Name	Description
9	ERR_C	Non-recovered Persistent Communication Error This bit is set to 1 when PHY Ready signal is negated due to the loss of communication with the device or problems with interface, but not after transition from active to Partial or Slumber power management state. (RW1C) Register type: Read/Write (1 clear)
8	ERR_T	Non-recovered Transient Data Integrity Error This bit is set when any of the following P SERR register bits is set during Data FIS transfer: ERR_P (Protocol) DIAG_C (CRC) DIAG_H (Handshake) ERR_C (PHY Ready negation) (RW1C) Register type: Read/Write (1 clear)
7:2	RESERVED_BITS7_2	Reserved (RO) Register type: Read
1	ERR_M	Recovered Communication Error This bit is set to 1 when PHY ready condition is detected after interface initialization, but not after transition from partial or slumber power management state to active state. (RW1C) Register type: Read/Write (1 clear)
0	ERR_I	Recovered Data Integrity This bit is set when any of the following P SERR register bits is set during non- Data FIS transfer: ERR_P (Protocol) DIAG_C (CRC) DIAG_H (Handshake) ERR_C (PHY Ready negation) (RW1C) Register type: Read/Write (1 clear)

0x29000134 SATA_P0SACT

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

SATA_P0SACT

Bits	Name	Description
31:0	DS	Device Status This field is bit significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. Software sets this field prior to issuing a native queued command for a particular command slot. Prior to writing P CI[TAG] to 1, the software sets DS[TAG] to 1 to indicate that a command with that TAG is outstanding. This field is cleared to 0 when: The software writes P CMD.ST from a 1 to a 0. The device sends a Set Device Bits FIS to the Port. The Port clears bits in this field that are set to 1 in the SActive field of the Set Device Bits FIS. he Port clears only bits that correspond to native queued commands that have completed successfully. This field is not cleared by the following: Port reset (COMRESET). Software reset. Note: Software must write this field only when P CMD.ST bit is set to 1. (RW1S) Register type: Read/Write (1 set)

0x29000138 SATA_P0CI

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

SATA_P0CI

Bits	Name	Description
31:0	CI	Command Issued This field is bit significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by the software to indicate to the Port that a command has been built in system memory for a command slot and may be sent to the device. When the Port receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field can only be set to 1 by the software when P CMD.ST is set to 1. Note: This field is reset when P CMD.ST is written from a 1 to a 0 by the software. (RW1S) Register type: Read/Write (1 set)

0x2900013C SATA_P0SNTF

Type: Read
Clock: CC_SATA_ACLK
Reset State: 0x0000_0000

This register is used to determine when asynchronous notification events have occurred for directly connected devices and devices connected to a port multiplier.

SATA_P0SNTF

Bits	Name	Description
31:16	RESERVED_BITS31_16	Reserved (RO) Register type: Read
15:0	PMN	PM Notify This field indicates whether a particular device with the corresponding PM Port number issued a Set Device Bits FIS to the DWC_ahsata Port with the Notification bit set: PM Port 0h sets bit 0, PM Port 1h sets bit 1, ... PM Port Fh sets bit 15. Individual bits are cleared by the software writing 1s to the corresponding bit positions. This field is reset on Global reset, but it is not reset by Port reset (COMRESET) or software reset. (RW1C) Register type: Read/Write (1 clear)

0x29000170 SATA_P0DMACR

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x0000_0044

This register contains bits for controlling the Port DMA engine. The software can change the fields of this register only when P CMD.ST=0. Power-up (system reset), Global reset, or Port reset (COMRESET) reset this register to the default value.

SATA_P0DMACR

Bits	Name	Description
31:8	RESERVED_BITS31_8	Reserved (RO) Register type: Read

SATA_P0DMACR (cont.)

Bits	Name	Description
7:4	RXTS	Receive Transaction Size This field defines the Port DMA transaction size in DWORDs for receive (system bus write, device read) operation. The options for this field are: 0x0: 1 DWORD 0x1: 2 DWORDs 0x2: 4 DWORDs 0x3: 8 DWORDs 0x4: 16 DWORDs (maximum value when P _RXFIFO_DEPTH=64) 0x5: 32 DWORDs 0x6: 64 DWORDs (maximum value when P _RXFIFO_DEPTH=128) 0x7: 128 DWORDs (maximum value when P _RXFIFO_DEPTH=256) 0x8: 256 DWORDs (maximum value when P _RXFIFO_DEPTH=512) 0x9: 512 DWORDs (maximum value when P _RXFIFO_DEPTH=1024) 0xA: 1024 DWORDs (maximum value when P _RXFIFO_DEPTH=2048) All other values are reserved and should not be used. This field is read-write when P CMD.ST=0 and read-only when P CMD.ST=1. The maximum value of this field is determined by the RxFIFO depth set by the P _RXFIFO_DEPTH parameter. When the software attempts to write a value exceeding this value, the maximum value would be set instead. (RW/RO) Register type: Read/Write

SATA_P0DMACR (cont.)

Bits	Name	Description
3:0	TXTS	Transmit Transaction Size This field defines the DMA transaction size in DWORDs for transmit (system bus read, device write) operation. The options for this field are: 0x0: 1 DWORD 0x1: 2 DWORDs 0x2: 4 DWORDs 0x3: 8 DWORDs 0x4: 16 DWORDs (maximum value when P_TXFIFO_DEPTH=32) 0x5: 32 DWORDs (maximum value when P_TXFIFO_DEPTH=64) 0x6: 64 DWORDs (maximum value when _TXFIFO_DEPTH=128) 0x7: 128 DWORDs (maximum value when P_TXFIFO_DEPTH=256) 0x8: 256 DWORDs (maximum value when P_TXFIFO_DEPTH=512) 0x9: 512 DWORDs (maximum value when P_TXFIFO_DEPTH=1024) 0xA: 1024 DWORDs (maximum value when P_TXFIFO_DEPTH=2048) All other values are reserved and should not be used. This field is read-write when P CMD.ST=0 and read-only when P CMD.ST=1. The maximum value of this field is determined by the TxFIFO depth set by the P _TXFIFO_DEPTH parameter. When the software attempts to write a value exceeding this value, the maximum value would be set instead. (RW/RO) Register type: Read/Write

0x29000178 SATA_P0PHYCR

Type: Read/Write
Clock: CC_SATA_ACLK
Reset State: 0x00000000

This register is used for Port PHY control. This register only exists when PHY_CTRL_W parameter is set to a non-zero value, otherwise this location is reserved. The width is set by the PHY_CTRL_W parameter (valid range: 0 to 32). When PHY_CTRL_W < 32, the remaining bits are reserved: reads return zeros, writes have no effect. Bits of this register are connected to the corresponding bits of the p _phy_ctrl output Port. Resets on power-up (system reset) only to the PHY_CTRL_DEF value.

SATA_P0PHYCR

Bits	Name	Description
31:16	NOP_BITS31_16	NO operation bits(RW) Register type: Read/Write

SATA_P0PHYCR (cont.)

Bits	Name	Description
15	SET_RXOOB0_CLKON_NOT	SET_RXOOB0_CLKON_NOT When this bit is clear(0), sata_rxoob0_clkon is constantly asserted. This bit should not be set if device initiated wakeup is expected. Register type: Read/Write
14	SET_PMALIVE_CLKON_NOT	SET_PMALIVE_CLKON_NOT When this bit is clear(0), sata_pmalive_clkon is constantly asserted. This bit should not be set if device initiated wakeup is expected. Register type: Read/Write
13	SET_PHY_CFG_CLKON_NOT	SET_PHY_CFG_CLKON_NOT When this bit is clear(0), sata_phy_cfg_clkon is constantly asserted. Register type: Read/Write
12	SET_AXI_CLKON_NOT	SET_AXI_CLKON_NOT When this bit is clear(0), sata_axi_clkon is constantly asserted. Register type: Read/Write
11:9	NOP_BITS11_9	NO operation bits (RW) Register type: Read/Write
8	FORCE_RX_DATA_VLD	When this bit is set(1), rx_data_vld input port is constant ’11’. (RW) Register type: Read/Write
7:4	TBS	Test Bus Select This field is used to select the input to the 32-bit SATA controller test bus port (sata_test_bus). The TBS pins selects from eight possible pages each with 32 possible observability points. When TBS[3:0] = 3’b0000 the output of the 32-bit test bus is set to logical 0’s. (RW) Register type: Read/Write
3	TSTB_FEED	SATA Testbus Feedthru This field is directly connected to output pin sata_test_bus[31] when TBS /= 0 and TBS[MSB] /= 1. It is used for debug and FPGA control. (RW) Register type: Read/Write

SATA_P0PHYCR (cont.)

Bits	Name	Description
2	NLB_M	Near-End Analog Mode This field is used to allow the SATA controller to enter a low power mode (partial/slumber) without actually placing the SATA PHY in that low power mode. This bit masks the p0_phy_partial and p0_phy_slumber signals to the SATA PHY. The Link can only get to the NEALB state through the L_POWER_DOWN state see (DW_SATA_link_sm) or the NO_CONN sate. But the SATA PHY cannot be placed into low power states since the clocks are turned off. When set to 1, the PHY will not enter any low power mode. (RW) Register type: Read/Write
1	PHY_PHYRESET_DISABLE	When this bit is set(1), p0_phy_phyreset output port is never asserted.
0	PHY_SRST	PHY Software Reset This field provides an active-high software reset to the SATA PHY. (RW) Register type: Read/Write

0x2900017C SATA_P0PHYSR

Type: Read
Clock: CC_SATA_ACLK
Reset State: Undefined

This register is used to monitor PHY status. This register only exists when PHY_STAT_W parameter is set to a non-zero value, otherwise this location is reserved. The width is set by the PHY_STAT_W parameter (valid range: 0 to 32). When PHY_CTRL_W < 32, the remaining bits are reserved: reads return zeros, writes have no effect. The bits of this register reflect the state of the corresponding bits of the p0_phy_status input.

Signals connected to the p _phy_status input can be asynchronous to any of the DWC_ahsata clocks, however they must not change faster than five hclk periods, otherwise the P PHYSR register may never be updated with the intermediate changing values.

SATA_P0PHYSR

Bits	Name	Description
31:15	RESERVED_BITS31_15	Reserved (RO) Register type: Read Only

SATA_P0PHYSR (cont.)

Bits	Name	Description
14	P0_PHY_RX_ERR	Value of p0_phy_rx_err input port. (RO) Register type: Read Only
13	P0_PHY_RX_ENABLE	Value of p0_phy_rx_enable output port. (RO) Register type: Read Only
12:11	P0_PHY_RX_DATA_VLD	Value of p0_phy_rx_data_vld input port. (RO) Register type: Read Only
10	P0_PHY_SIG_DET	Value of p0_phy_sig_det input port. (RO) Register type: Read Only
9	P0_PHY_TX_ENABLE	Value of p0_phy_tx_enable output port. (RO) Register type: Read Only
8	P0_PHY_TX_DATA_VLD	Value of p0_phy_tx_data_vld output port. (RO) Register type: Read Only
7	P0_PHY_NEARAFELB	Value of p0_phy_nearafelb output port. (RO) Register type: Read Only
6	P0_PHY_FARAFELB	Value of p0_phy_farafelb output port. (RO) Register type: Read Only
5	P0_PHY_SLUMBER	Value of p0_phy_slumber output port. In case of NEALB mode, p0_phy_slumber is masked towards SATA PHY. The value of this of this status bit reflects the value of p0_phy_slumber before the mask. (RO) Register type: Read Only
4	P0_PHY_PARTIAL	Value of p0_phy_partial output port. In case of NEALB mode, p0_phy_partial is masked towards SATA PHY. The value of this of this status bit reflects the value of p0_phy_partial before the mask. (RO) Register type: Read Only
3	P0_PHY_SPDSEL	Value of p0_phy_spdsel output port. (RO) Register type: Read Only
2	P0_PHY_SPDMODE	Value of p0_phy_spdmode input port. (RO) Register type: Read Only

SATA_P0PHYSR (cont.)

Bits	Name	Description
1	P0_PHY_CALIBRATED	Value of p0_phy_calibrated input port. (RO) Register type: Read Only
0	P0_PHY_PHYRESET	Value of p0_phy_phyreset output port. The value is before the mask SATA_P0PHYCR.PHY_PHYRESET_DISABLE is applied. (RO) Register type: Read Only

18.3 SATA UNI PHY PLL Registers (0x1B400000 SATA_PHY_BASE)

This section contains the SATA UNI PHY PLL registers.

0x1B400000 UNIPHY_PLL_REFCLK_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Reference clock divider and feedback pre-dividers

UNIPHY_PLL_REFCLK_CFG

Bits	Name	Description
31:8	UNUSED_1	
7	RESERVED_1	
6	UNUSED_2	
5:4	PLL_FBCLK_PREDIV	FB pre-divider Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Default value is 00 0x0: divide FB clock by 1 0x1: divide FB clock by 2
3:2	PLL_REFCLK_DIV	Reference clock divider ratio. - 00 : div by 1 - 01 : div by 2 - 10 : div by 3 - 11 : div by 4 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Defalut value is 0000
1	RESERVED_2	
0	PLL_REFCLK_DBLR	Reference clock doubler ratio. - 0: div by 1 - 1: div by 2 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Default value is 0

0x1B400004 UNIPHY_PLL_POSTDIV1_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000009

Divide ratio for post-divider 1 and SVS. mode selection

UNIPHY_PLL_POSTDIV1_CFG

Bits	Name	Description
31:8	UNUSED	
7:5	RESERVED	
4	PLL_SVS_MODE	SVS. Mode Enable - 0: Normal operation mode - 1: SVS. operation mode In SVS. mode, all clocks will be half the frequency of normal operation mode. Normal operational mode setting is 0. Defalut value is 0
3:0	PLL_POSTDIV1	Output Divider setting for oCLK1. - 0000: div by1 - 0001: div by2 ... - 1111: div by16 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Default up value is 0000

0x1B400008 UNIPHY_PLL_CHGPUMP_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000002

Charge pump Control

UNIPHY_PLL_CHGPUMP_CFG

Bits	Name	Description
31:8	UNUSED	
7:4	RESERVED	
3:0	PLL_CP_IDAC	Charge charge pump current Normal operational mode setting is 0010 Default value is 0010

0x1B40000C UNIPHY_PLL_VCOLPF_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000030

Loop filter and VCO control

UNIPHY_PLL_VCOLPF_CFG

Bits	Name	Description
31:8	UNUSED	
7:6	RESERVED	
5	PD_HP_VCO	Power down high-performance VCO Default value is 1 Normal value: refer to frequency plan
4	PD_LP_VCO	Power down low-power VCO Default value is 1 Normal value: refer to frequency plan
3	PLL_VCO_SEL	Select VCO (LP or HP) Normal operational mode setting is 0 Default value is 0
2:1	PLL_C3_SEL	Select C3 in LPF Normal operational mode setting is 00 Default value is 00
0	PLL_BYPASS_P3	Bypass P3 in LPF Normal operational mode setting is 0 Default value is 0

0x1B400010 UNIPHY_PLL_VREG_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Regulator control

UNIPHY_PLL_VREG_CFG

Bits	Name	Description
31:8	UNUSED	
7:3	RESERVED_1	

UNIPHY_PLL_VREG_CFG (cont.)

Bits	Name	Description
2	PLL_VREG_TEST_EN	Enable test mode of voltage regulator Normal operational mode setting is 0 Default value is 0
1:0	RESERVED_2	

0x1B400014 UNIPHY_PLL_PWRGEN_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Powergen control

UNIPHY_PLL_PWRGEN_CFG

Bits	Name	Description
31:8	UNUSED	
7:3	RESERVED	
2:0	PLL_PWRGEN_CTRL	PWRGEN block control (reserved) Normal operational mode setting is 000 Default value is 000

0x1B400018 UNIPHY_PLL_DMUX_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Digital mux control setting

UNIPHY_PLL_DMUX_CFG

Bits	Name	Description
31:8	UNUSED	
7:5	RESERVED	
4:1	PLL_DMUX_SEL	PLL digital test mux select Defalut value is 00000
0	PLL_DMUX_EN	PLL digital test mux enable Defalut value is 0

0x1B40001C UNIPHY_PLL_AMUX_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Analog mux control setting

UNIPHY_PLL_AMUX_CFG

Bits	Name	Description
31:8	UNUSED	
7:5	RESERVED	
4:1	PLL_AMUX_SEL	PLL analog test mux select Defalut value is 00000
0	PLL_AMUX_EN	PLL analog test mux enable Defalut value is 0

0x1B400020 UNIPHY_PLL_GLB_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Global configuration for PLL

UNIPHY_PLL_GLB_CFG

Bits	Name	Description
31:8	UNUSED	
7:3	PLL_GLB_CFG	Reserved Normal operational mode setting is 000000 Default value is 000000
2	PLL_PWRGEN_PWRDN_B	power down the powergen block Normal operational mode setting is 1 Default value is 0
1	PLL_LDO_PWRDN_B	LDO Power Down. - 1---Normal operation - 0---Digital block power down mode Normal operational mode setting is 1 Default value is 0

UNIPHY_PLL_GLB_CFG (cont.)

Bits	Name	Description
0	PLL_PWRDN_B	Global power-down signal for PLL; this is an active low singal, i.e., when PLL_PWRDN_B = 0, PLL is in power-down mode. CSR is still accessable Normal operational mode setting is 1 Default value is 0

0x1B400024 UNIPHY_PLL_POSTDIV2_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000007

Divide ratio for post divider number 2

UNIPHY_PLL_POSTDIV2_CFG

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_POSTDIV2	Output Divider setting for oCLK2 - 00000000: div by1 - 00000001: div by2 ... - 11111111: div by256 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Defalut value is 0000_0111

0x1B400028 UNIPHY_PLL_POSTDIV3_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000007

Divide ratio for post divider number 3

UNIPHY_PLL_POSTDIV3_CFG

Bits	Name	Description
31:8	UNUSED	

UNIPHY_PLL_POSTDIV3_CFG (cont.)

Bits	Name	Description
7:0	PLL_POSTDIV3	Output Divider setting for oCLK3 - 00000000: div by1 - 00000001: div by2 ... - 11111111: div by256 Normal operational value: Refer to PLL Frequency programming table in Integration guideline. Defalut value is 0000_0111

0x1B40002C UNIPHY_PLL_LPFR_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Resistance setting of loop filter

UNIPHY_PLL_LPFR_CFG

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_LPF_R	Loop filter resistance selection Normal operational mode setting is 00000000 Default value is 00000000

0x1B400030 UNIPHY_PLL_LPFC1_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000003

Capacitance C1 setting of loop filter

UNIPHY_PLL_LPFC1_CFG

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_LPF_C1	Loop filter C1 selection Normal operational mode setting is 00000011 Default value is 00000011

0x1B400034 UNIPHY_PLL_LPFC2_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000003

Capacitance C2 setting of loop filter

UNIPHY_PLL_LPFC2_CFG

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_LPF_C2	Loop filter C2 selection Normal operational mode setting is 00000011 Default value is 00000011

0x1B400038 UNIPHY_PLL_SDM_CFG0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000076

Sigma-delta modulator setting- cfg0

UNIPHY_PLL_SDM_CFG0

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6	PLL_SDM_BYP	Bypass SDM (integer N mode) Normal operational mode setting is 1 Default value is 1
5:0	PLL_SDM_BYP_DIV	Integer N mode feedback clock divider value Normal operational mode setting is 110110 Default value is 110110

0x1B40003C UNIPHY_PLL_SDM_CFG1

Type: Read/Write
Clock: WCLK
Reset State: 0x0000004C

Sigma-delta modulator setting- cfg1

UNIPHY_PLL_SDM_CFG1

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6	PLL_SDM_DITHER_EN	Enable dithering Normal operational mode setting is 1 Default value is 1
5:0	PLL_SDM_DC_OFFSET	Integer portion of fractional N mode divider Normal operational mode setting is 001100 Default value is 001100

0x1B400040 UNIPHY_PLL_SDM_CFG2

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Sigma-delta modulator setting- cfg2

UNIPHY_PLL_SDM_CFG2

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_SDM_FREQ_SEED_7_0	Fractional N mode divider fractional portion, bits 7:0 sdm_freq_seed[17:16] are always 00. fdiv value= (sdm_dc_+1)+(sdm_freq_seed<15:0>/2^16) ex:(6+1)+2^15/2^16)=7+0.5=7.5 Normal operational mode setting is 00000000 Default value is 00000000

0x1B400044 UNIPHY_PLL_SDM_CFG3

Type: Read/Write
Clock: WCLK
Reset State: 0x000000C0

Sigma-delta modulator setting- cfg3

UNIPHY_PLL_SDM_CFG3

Bits	Name	Description
31:8	UNUSED	

UNIPHY_PLL_SDM_CFG3 (cont.)

Bits	Name	Description
7:0	PLL_SDM_FREQ_SEED_15_8	Fractional N mode divider fractional portion, bits 15:8 Normal operational mode setting is 11000000 Default value is 11000000

0x1B400048 UNIPHY_PLL_SDM_CFG4

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Sigma-delta modulator setting- cfg4

UNIPHY_PLL_SDM_CFG4

Bits	Name	Description
31:8	UNUSED	
7:2	RESERVED	
1:0	PLL_SDM_FREQ_SEED_17_16	Fractional N mode divider fractional portion, bits 17:16 Normal operational mode setting is 00 Default value is 00

0x1B40004C UNIPHY_PLL_SSC_CFG0

Type: Read/Write
Clock: WCLK
Reset State: 0x0000009A

Spread-spectrum clocking setting- cfg0

UNIPHY_PLL_SSC_CFG0

Bits	Name	Description
31:8	UNUSED	
7	PLL_SSC_BYP	Bypass SSC circuit Normal operational mode setting is 1 Default value is 1

UNIPHY_PLL_SSC_CFG0 (cont.)

Bits	Name	Description
6:0	PLL_SSC_KDIV	Divider to generate 2MHz clock from refclk. This clock is used by the Spread spectrum portion of the sigma-delta block. It is mainly changing the fractional portion of feedback divider value, e.g. if refclk=100MHz, kdiv = 00110001 Normal operational mode setting is 0011010 Default value is 0011010

0x1B400050 UNIPHY_PLL_SSC_CFG1

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Spread-spectrum clocking setting- cfg1

UNIPHY_PLL_SSC_CFG1

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_SSC_TRIANG_INC_7_0	SSC triangle incr, bits 7:0 Normal operational mode setting is 00000000 Default value is 00000000

0x1B400054 UNIPHY_PLL_SSC_CFG2

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Spread-spectrum clocking setting- cfg2

UNIPHY_PLL_SSC_CFG2

Bits	Name	Description
31:8	UNUSED	
7:2	RESERVED	
1:0	PLL_SSC_TRIANG_INC_9_8	SSC triangle incr, bits 9:8 Normal operational mode setting is 00 Default value is 00

0x1B400058 UNIPHY_PLL_SSC_CFG3

Type: Read/Write
Clock: WCLK
Reset State: 0x00000020

Spread-spectrum clocking setting- cfg2

UNIPHY_PLL_SSC_CFG3

Bits	Name	Description
31:8	UNUSED	
7:6	RESERVED	
5:0	PLL_SSC_TRIANG_STEPS	SSC triangle steps Normal operational mode setting is 100000 Default value is 100000

0x1B40005C UNIPHY_PLL_LKDET_CFG0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000010

Lock detect setting - cfg0

UNIPHY_PLL_LKDET_CFG0

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_LCKDET_MCNT	mpll lock detect maximum count value for the fref and fdiv counters Normal operational mode setting is 00010000 Default value is 00010000

0x1B400060 UNIPHY_PLL_LKDET_CFG1

Type: Read/Write
Clock: WCLK
Reset State: 0x0000001A

Lock detect setting - cfg1

UNIPHY_PLL_LKDET_CFG1

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_LOCKDET_WAIT	Number of cycles to wait (2 cycles incremental) Normal operational mode setting is 00011010 Default value is 00011010

0x1B400064 UNIPHY_PLL_LKDET_CFG2

Type: Read/Write
Clock: WCLK
Reset State: 0x0000000D

Lock detect setting - cfg2

UNIPHY_PLL_LKDET_CFG2

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6	FORCE_PLL_LOCK	- 0: PLL_RDY and pll_lockdet from PLL Lock detect will be used - 1: PLL_RDY and pll_lockdet from PLL Lock detect will be bypassed. In other words, it will force the PLL_RDY to go high and pll_unlockdet to go low. This bit is only used as a back up in case the PLL Lock Detect circuit does not operate correctly. Normal operational mode setting is 0 Default value is 0
5:2	PLL_LOCKDET_PPM	PPM setting for PLL lock detect circuitry Normal operational mode setting is 0011 Default value is 0011
1	PLL_LOCKDET_CTRL	control phy_tx_lockdet Normal operational mode setting is 0 Default value is 0
0	PLL_LOCKDET_EN	Enable lockdet Normal operational mode setting is 1 Default value is 1

0x1B400068 UNIPHY_PLL_TEST_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Setting for sanity check and PLL bypass mode

UNIPHY_PLL_TEST_CFG

Bits	Name	Description
31:8	UNUSED	
7:3	RESERVED	
2	PLL_CLOCK_BYPASS	Output Clock Control (Debug Purpose). When it is '1', the output clocks will be generated from reference clock. When it is '0', output clocks will be generated from PLL VCO clock. Normal operational mode setting is 0 Defalut value is 0
1	PLL_SANITY_CHECK	- 1: PLL clock frequency based on power up value. OUTCLK1 = 810MHz, OUTCLK2=OUTCLK3=(OUTCLK1/8). 0: PLL clock frequency based on PLL software configuration Normal operational mode setting is 0. Defalut value is 0
0	PLL_SW_RESET	PLL software reset; resets all blocks except CSR Normal operational mode setting is 0 Default value is 0

0x1B40006C UNIPHY_PLL_CAL_CFG0

Type: Read/Write
Clock: WCLK
Reset State: 0x0000000A

PLL calibration setting - cfg0

UNIPHY_PLL_CAL_CFG0

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6	PLL_LOAD_CAL_STR	Load saved PLL calibration string for offset, vco, and kvdd calibration Normal operational mode setting is 0 Default value is 0

UNIPHY_PLL_CAL_CFG0 (cont.)

Bits	Name	Description
5	PLL_OPEN_LOOP	Configure PLL in open loop mode Normal operational mode setting is 0 Default value is 0
4:3	PLL_CAL_WAITTIME	Idle time for VCO frequency adjustment during Calibration Normal operational mode setting is 01 Default value is 01
2:0	PLL_CAL_MODE	Calibration Mode Normal operational mode setting is 010 Default value is 010

0x1B400070 UNIPHY_PLL_CAL_CFG1

Type: Read/Write
Clock: WCLK
Reset State: 0x00000004

PLL calibration setting - cfg1

UNIPHY_PLL_CAL_CFG1

Bits	Name	Description
31:8	UNUSED	
7	PLL_POS_KVSLP	Slope polarity of KVCO Normal operational mode setting is 0 Default value is 0
6:4	RESERVED	
3:0	PLL_VREF_CONF	KVCO Calibration Reference voltage setting Normal operational mode setting is 0100 Default value is 0100

0x1B400074 UNIPHY_PLL_CAL_CFG2

Type: Read/Write
Clock: WCLK
Reset State: 0x00000004

PLL calibration setting - cfg2

UNIPHY_PLL_CAL_CFG2

Bits	Name	Description
31:8	UNUSED	
7:4	RESERVED	
3:0	PLL_VREG_CONF	KVDD Calibration Reference voltage setting Normal operational mode setting is 0100 Default value is 0100

0x1B400078 UNIPHY_PLL_CAL_CFG3

Type: Read/Write
Clock: WCLK
Reset State: 0x0000002B

PLL calibration setting - cfg3

UNIPHY_PLL_CAL_CFG3

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_VCO_MAN_OFFSET	Manual selection of VCO frequency sub-banding (offset) Normal operational mode setting is 0101011 Default value is 0101011

0x1B40007C UNIPHY_PLL_CAL_CFG4

Type: Read/Write
Clock: WCLK
Reset State: 0x00000006

PLL calibration setting - cfg4

UNIPHY_PLL_CAL_CFG4

Bits	Name	Description
31:8	UNUSED	
7:5	RESERVED	
4:0	PLL_VCO_MAN_SLOPE	Manual selection of Kvco slope Normal operational mode setting is 00110 Default value is 00110

0x1B400080 UNIPHY_PLL_CAL_CFG5

Type: Read/Write
Clock: WCLK
Reset State: 0x00000006

PLL calibration setting - cfg5

UNIPHY_PLL_CAL_CFG5

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6:0	PLL_VCO_MAN_KVDD	Manual selction of KVDD parameters Normal operational mode setting is 00110 Default value is 00110

0x1B400084 UNIPHY_PLL_CAL_CFG6

Type: Read/Write
Clock: WCLK
Reset State: 0x0000002B

PLL calibration setting - cfg6

UNIPHY_PLL_CAL_CFG6

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_CAL_KVCO_COUNT_7_0	Target Calibration KVCO Use This equation: KV_COUNT = kvco *vdd/6, bits 7:0 Normal operational mode setting is 00101011 Default value is 00101011

0x1B400088 UNIPHY_PLL_CAL_CFG7

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

PLL calibration setting - cfg7

UNIPHY_PLL_CAL_CFG7

Bits	Name	Description
31:8	UNUSED	
7:2	RESERVED	
1:0	PLL_CAL_KVCO_COUNT_9_8	Target Calibration KVCO Use This equation: KV_COUNT = kvco *vdd/6, bits 9:8 Normal operational mode setting is 00 Default value is 00

0x1B40008C UNIPHY_PLL_CAL_CFG8

Type: Read/Write
Clock: WCLK
Reset State: 0x00000086

PLL calibration setting - cfg8

UNIPHY_PLL_CAL_CFG8

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_CAL_REFCLK_DIV_7_0	Reference divider number to get to 5us measurement period, bits 7:0 Normal operational mode setting is 10000110 Default value is 10000110

0x1B400090 UNIPHY_PLL_CAL_CFG9

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

PLL calibration setting - cfg9

UNIPHY_PLL_CAL_CFG9

Bits	Name	Description
31:8	UNUSED	
7:2	RESERVED	

UNIPHY_PLL_CAL_CFG9 (cont.)

Bits	Name	Description
1:0	PLL_CAL_REFCLK_DIV_9_8	Reference divider number to get to 5us measurement period, bits 9:8 Normal operational mode setting is 00 Default value is 00

0x1B400094 UNIPHY_PLL_CAL_CFG10

Type: Read/Write
Clock: WCLK
Reset State: 0x000000E6

PLL calibration setting - cfg10

UNIPHY_PLL_CAL_CFG10

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_VCO_FREQ_7_0	Target Calibration VCO frequency, bits 7:0 Normal operational mode setting is 11100110 Default value is 11100110

0x1B400098 UNIPHY_PLL_CAL_CFG11

Type: Read/Write
Clock: WCLK
Reset State: 0x00000002

PLL calibration setting - cfg11

UNIPHY_PLL_CAL_CFG11

Bits	Name	Description
31:8	UNUSED	
7:3	RESERVED	
2:0	PLL_VCO_FREQ_10_8	Target Calibration VCO frequency, bits 10:8 Normal operational mode setting is 010 Default value is 010

0x1B40009C UNIPHY_PLL_EFUSE_CFG

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

PLL efuse setting

UNIPHY_PLL_EFUSE_CFG

Bits	Name	Description
31:8	UNUSED	
7:6	RESERVED	
5	PLL_EFUSE_OVRRIDE_SEL	- 0: Use EFUSE value selected by PLLPHY_DRVSTR_EFUSE_SEL - 1: Override with PLLPHY_EFUSE value. Defalut value is 0
4	PLL_DRVSTR_EFUSE_SEL	- 1: Select the efuse used for datalane impedence calibration - 0: Select dedicated PLL calibration efuse Defalut value is 0
3:0	PLL_EFUSE	efuse override value Defalut value is 0000

0x1B4000A0 UNIPHY_PLL_DEBUG_BUS_SEL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Debug select setting

UNIPHY_PLL_DEBUG_BUS_SEL

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_DEBUG_SEL	PLL Debug bus select Normal operational mode setting is 00000000 Default value is 00000000

0x1B4000A4 UNIPHY_PLL_CTRL_42

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

No description provided for this register.

UNIPHY_PLL_CTRL_42

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B4000A8 UNIPHY_PLL_CTRL_43

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

No description provided for this register.

UNIPHY_PLL_CTRL_43

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B4000AC UNIPHY_PLL_CTRL_44

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

No description provided for this register.

UNIPHY_PLL_CTRL_44

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B4000B0 UNIPHY_PLL_CTRL_45

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

No description provided for this register.

UNIPHY_PLL_CTRL_45

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B4000B4 UNIPHY_PLL_CTRL_46

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

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UNIPHY_PLL_CTRL_46

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B4000B8 UNIPHY_PLL_CTRL_47

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

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UNIPHY_PLL_CTRL_47

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B4000BC UNIPHY_PLL_CTRL_48

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

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UNIPHY_PLL_CTRL_48

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B4000C0 UNIPHY_PLL_STATUS

Type: Read
Clock: WCLK
Reset State: 0x00000000

PLL status signals

.

UNIPHY_PLL_STATUS

Bits	Name	Description
31:8	UNUSED	
7:1	RESERVED	
0	PLL_RDY	READ ONLY Status of pll_lockdet signal Default value is 0

0x1B4000C4 UNIPHY_PLL_DEBUG_BUS0

Type: Read
Clock: WCLK
Reset State: 0x00000000

PLL debug bus - bits 7:0

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UNIPHY_PLL_DEBUG_BUS0

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_DEBUG_BUS_7_0	READ ONLY Default value is 00000000

0x1B4000C8 UNIPHY_PLL_DEBUG_BUS1

Type: Read
Clock: WCLK
Reset State: 0x00000000

.PLL debug buss - bits 15:8

UNIPHY_PLL_DEBUG_BUS1

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_DEBUG_BUS_15_8	READ ONLY Default value is 00000000

0x1B4000CC UNIPHY_PLL_DEBUG_BUS2

Type: Read
Clock: WCLK
Reset State: 0x00000000

PLL debug bus - bits 23:16

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UNIPHY_PLL_DEBUG_BUS2

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_DEBUG_BUS_23_16	READ ONLY Default value is 00000000

0x1B4000D0 UNIPHY_PLL_DEBUG_BUS3

Type: Read
Clock: WCLK
Reset State: 0x00000000

PLL debug bus - bits 31:24

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UNIPHY_PLL_DEBUG_BUS3

Bits	Name	Description
31:8	UNUSED	
7:0	PLL_DEBUG_BUS_31_24	READ ONLY Default value is 0

0x1B4000D4 UNIPHY_PLL_CTRL_54

Type: Read
Clock: WCLK
Reset State: 0x00000000

No description provided for this register.

UNIPHY_PLL_CTRL_54

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

3.3.1 SATA PHY

0x1B400100 SATA_PHY_SER_CTRL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately

This register configures the serializer clock edge

SATA_PHY_SER_CTRL

Bits	Name	Description
31:8	UNUSED	
7:1	RESERVED	
0	SERIALIZER_FALL_EDGE	TX byte clock invert enable at serializer input - 0: latch on rising edge - 1: latch on falling edge

0x1B400104 SATA_PHY_TX_DRIV_CTRL0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000009

Action Time: Writes to this register take effect immediately

This register configures the TX Driver Control.

SATA_PHY_TX_DRIV_CTRL0

Bits	Name	Description
31:8	UNUSED	
7:4	RESERVED	
3:0	PE	Pre-emphasis setting. Change De-emphasis strength (in dB): - 1100: No de-emphasis (0dB) - 1001: De-emphasos (-1 dB) - 0110: De-emphasos (-2 dB) - 0011: Max de-emphasis (-3dB) Other coding: not recommended to use

0x1B400108 SATA_PHY_TX_DRIV_CTRL1

Type: Read/Write
Clock: WCLK
Reset State: 0x00000009

Action Time: Writes to this register take effect immediately

This register configures the TX Driver Control

SATA_PHY_TX_DRIV_CTRL1

Bits	Name	Description
31:8	UNUSED	
7:4	RESERVED	
3:1	TX_SWING_CTRL_FINE	Fine selection of TX output swing, use together with TX_SWING_HIGH: TX_SWING_CTRL_COARSE = Setting: 1 / 0 - 000: 300mV / 160mV ... - 111: 650mV / 480mV Output swing increases with control code.
0	TX_SWING_CTRL_COARSE	Coarse selection of TX output Swing: - 0: Low swing Vswing < 400mV - 1: High swing Vswing > 400mV

0x1B40010C SATA_PHY_TX_DRIV_CTRL2

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately

This register configures the TX Driver Control

SATA_PHY_TX_DRIV_CTRL2

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B400110 SATA_PHY_TX_DRIV_CTRL3

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately

This register configures the TX Driver Control

SATA_PHY_TX_DRIV_CTRL3

Bits	Name	Description
31:8	UNUSED	
7:6	DRV_TEST_SEL	TX driver analog voltage signal test selection (to TPA): - 00: Vimcal (impcal comparator input node voltage) - 01: Vreg_drv (swing voltage LDO output) - 10: Vreg_predrv (drv gate max input voltage) - 11: Vb (drv fine tune bias voltage)
5:0	RESERVED	

0x1B400114 SATA_PHY_TX_RESV0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately

This register configures the TX Driver Control

SATA_PHY_TX_RESV0

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B400118 SATA_PHY_TX_RESV1

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately

This register configures the TX Driver Control

SATA_PHY_TX_RESV1

Bits	Name	Description
31:8	UNUSED	

SATA_PHY_TX_RESV1 (cont.)

Bits	Name	Description
7	TBC_CLK_SEL	Selection used when retime loopback is enabled - 0: sataphy_tbc_clk external input selected to drive retime buffer. - 1: Internal asic_clk output selected to drive retime buffer.
6:0	RESERVED	

0x1B40011C SATA_PHY_TX_IMCAL0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

This register is for impedance calibration related logic on the digital side.

SATA_PHY_TX_IMCAL0

Bits	Name	Description
31:8	UNUSED	
7	FORCE_TX_IMCAL_DONE	Impedance calibration done - 0: disabled - 1: enabled
6	TX_IMCAL_OVERWRT	The control bit has two purposes: - 1. When TX_IMCAL_EN=1, assertion of this control add Imp_val as bias value to calibrated control value - 2. When TX_IMCAL_EN=0, ’
5:1	TX_IMCAL_STR_VAL_ADJ	If TX_IMCAL_OVERWRT=1: Overwrite value for Tx calibration string If TX_IMCAL_OVERWRT=0: Manual offset for Tx calibration string which will be added to calibrated vector
0	TX_IMCAL_EN	Impedance calibration enable - 0: disabled - 1: enabled

0x1B400120 SATA_PHY_TX_IMCAL1

Type: Read/Write
Clock: WCLK
Reset State: 0x00000005

This register is for impedance calibration related logic on the digital side.

SATA_PHY_TX_IMCAL1

Bits	Name	Description
31:8	UNUSED	
7:0	TX_IMCAL_WAITTIME	calibration wait time

0x1B400124 SATA_PHY_TX_IMCAL2

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

This register is for impedance calibration related logic on the digital side.

SATA_PHY_TX_IMCAL2

Bits	Name	Description
31:8	UNUSED	
7:2	RESERVED	
1	TX_IMCAL_COMP_POL	Polarity of comparator for Tx calibration - 0: polarity is positive - 1: polarity is negative
0	TX_AUTOIMCAL	calibration enable or disable during phyreset - 0: calibration enabled by SW bit TX_IMCAL_EN - 1: calibration restart automaticaly every time when OOB Init re-start.

0x1B400128 SATA_PHY_RX_IMCAL0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

This register is for impedance calibration related logic on the digital side.

SATA_PHY_RX_IMCAL0

Bits	Name	Description
31:8	UNUSED	
7	FORCE_RX_IMCAL_DONE	Impedance calibration done - 0: disabled - 1: enabled

SATA_PHY_RX_IMCAL0 (cont.)

Bits	Name	Description
6	RX_IMCAL_OVERWRT	The control bit has two purposes: - 1. When RX_IMCAL_EN=1, assertion of this control add Imp_val as bias value to calibrated control value - 2. When RX_IMCAL_EN=0, ’
5:1	RX_IMCAL_STR_VAL_ADJ	If RX_IMCAL_OVERWRT=1: Overwrite value for Rx calibration string If RX_IMCAL_OVERWRT=0: Manual offset for Rx calibration string which will be added to calibrated vector
0	RX_IMCAL_EN	Impedance calibration enable - 0: disabled - 1: enabled

0x1B40012C SATA_PHY_RX_IMCAL1

Type: Read/Write
Clock: WCLK
Reset State: 0x00000005

This register is for impedance calibration related logic on the digital side.

SATA_PHY_RX_IMCAL1

Bits	Name	Description
31:8	UNUSED	
7:0	RX_IMCAL_WAITTIME	calibration wait time

0x1B400130 SATA_PHY_RX_IMCAL2

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

This register is for impedance calibration related logic on the digital side.

SATA_PHY_RX_IMCAL2

Bits	Name	Description
31:8	UNUSED	
7:2	RESERVED	

SATA_PHY_RX_IMCAL2 (cont.)

Bits	Name	Description
1	RX_IMCAL_COMP_POL	Polarity of comparator for Rx calibration - 0: polarity is positive - 1: polarity is negative
0	RX_AUTOIMCAL	calibration enable or disable during phyreset - 0: calibration enabled by SW bit TX_IMCAL_EN - 1: calibration restart automaticaly every time when OOB Init re-start.

0x1B400134 SATA_PHY_RX_TERM

Type: Read/Write
Clock: WCLK
Reset State: 0x00000041

Action Time: Writes to this register take effect immediately.

This register configures the RX termination settings.

SATA_PHY_RX_TERM

Bits	Name	Description
31:8	UNUSED	
7	RESERVED_1	
6	RX_TERMINATION_EN	Enable the termination at RX input - 0: RX termination impedance is open and high > 100 Kohm - 1: RX termination impedance is enabled. Target 50Ohm single-ended
5:2	RESERVED_2	
1	DC_TERM_EN	Enable DC reference voltage with in DC coupling connection: - 0: DC reference voltage not defined - 1: DC reference voltage is set to 240mV for input common mode
0	AC_TERM_EN	Enable AC reference voltage with in AC coupling connection: - 0: AC reference voltage not defined - 1: AC reference voltage is set to 0V for input common mode

0x1B400138 SATA_PHY_RX_TERM_RESV

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately.

This register configures the RX termination settings.

SATA_PHY_RX_TERM_RESV

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B40013C SATA_PHY_EQUAL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately.

This register configures the Equalization settings.

SATA_PHY_EQUAL

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6:2	EQ_SEL	Equalizer DC to peak gain setting: - 00000: Min peak/DC gain 0 dB - 01111: Max peak/DC gain
1:0	EQ_PEAK_INC	Equalizer peak starting frequency setting. - 00: The peaking starts at lowest frequency (

0x1B400140 SATA_PHY_EQUAL_RESV

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately.

This register configures the RX termination settings.

SATA_PHY_EQUAL_RESV

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B400144 SATA_PHY_OOB_CTRL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000001

Action Time: Writes to this register take effect immediately.

This register configure OOB & RX Termination settings.

SATA_PHY_OOB_CTRL

Bits	Name	Description
31:8	UNUSED	
7:3	RESERVED	
2:0	OOB_RX_SEN	OOB input sensitivity (mV pp-diff) Smaller setting is more sensitive: - 000 :50mV p2p input voltage - 001 : 75mV p2p input voltage - 01x : 125mV p2p input voltage - 1xx : 185mV p2p input voltage

0x1B400148 SATA_PHY_CDR_CTRL0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000058

Action Time: Writes to this register take effect immediately.

This register configures CDR settings relating to the Ki and Kp gain controls in the DLP.

SATA_PHY_CDR_CTRL0

Bits	Name	Description
31:8	UNUSED	

SATA_PHY_CDR_CTRL0 (cont.)

Bits	Name	Description
7:4	KI	CDR loop filter integral gain select: Gain = 2^(Ki)
3:0	KP	CDR loop filter proportional gain select: Gain = 2^(Kp)

0x1B40014C SATA_PHY_CDR_CTRL1

Type: Read/Write
Clock: WCLK
Reset State: 0x00000004

Action Time: Writes to this register take effect immediately.

This register configures the CDR settings.

SATA_PHY_CDR_CTRL1

Bits	Name	Description
31:8	UNUSED	
7:5	RESERVED_1	
4:2	DECIM_SEL	CDR Decimation rate control (Default 3 = 001): - 000: 2 100: 4 - 001: 3 101: 6 - 010: 5 110: 10 - 011: 7 111: 14 DLF performance has to meet Fvco/Decim
1	RESERVED_2	
0	CDR_FLIP_DIR	Change the direction of CDR tracking for different type of integration - 0: CDR phase output positive speed up PI output clock - 1: CDR phase output positive slow down PI output clock

0x1B400150 SATA_PHY_CDR_CTRL2

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately.

This register configure CDR settings.

SATA_PHY_CDR_CTRL2

Bits	Name	Description
31:8	UNUSED	
7:4	RESERVED	
3	SET_FA	Open integral loop in CDR and load FA value in REG SATA_PHY_FA_LOAD0 and SATA_PHY_FA_LOAD1
2	PHX1_IN	Phase error information when bypass phase detector (for test) PHX1_IN/PHX0_IN - 00: Hold (0) - 01: Early (1) - 11: Late (-1) - 10: Illegal input
1	PHX0_IN	Description combined with PHX1_IN above
0	SET_PE	Open CDR loop and load phase error information from PHX1_IN/PHX0_IN

0x1B400154 SATA_PHY_CDR_CTRL3

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately.

This register configure CDR settings.

SATA_PHY_CDR_CTRL3

Bits	Name	Description
31:8	UNUSED	
7:1	RESERVED	
0	CDR_CLOSED_LOOP_ALWAYS_ON	Set this control to always close CDR loop; CDR initialization and self-recovery are ignored when this set high

0x1B400158 SATA_PHY_CDR_CTRL4

Type: Read/Write
Clock: WCLK
Reset State: 0x000000FF

Action Time: Writes to this register take effect immediately.

This register configure CDR settings.

SATA_PHY_CDR_CTRL4

Bits	Name	Description
31:8	UNUSED	
7:0	CDR_MAX_CNT	Wait time from rx_signal active to CDR start

0x1B40015C SATA_PHY_FA_LOAD0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately.

This register configures the FA Load bits [7:0].

SATA_PHY_FA_LOAD0

Bits	Name	Description
31:8	UNUSED	
7:0	FA_LOAD_7_0	Freq. offset value loaded to CDR intergal path register. Loaded with SET_FA is high

0x1B400160 SATA_PHY_FA_LOAD1

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately.

This register configures FA Load bits [15:8].

SATA_PHY_FA_LOAD1

Bits	Name	Description
31:8	UNUSED	
7:0	FA_LOAD_15_8	Freq. offset value loaded to CDR intergal path register. Loaded with SET_FA is high

0x1B400164 SATA_PHY_CDR_CTRL_RESV

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately.

This register configures the RX termination settings.

SATA_PHY_CDR_CTRL_RESV

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B400168 SATA_PHY_PI_CTRL0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately.

This register configure CDR settings.

SATA_PHY_PI_CTRL0

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6:1	PI_ADDR_SET	PI output phase control value directly loaded when SET_PI is high.
0	SET_PI	Break CDR loop for test. Load PI phase control directly

0x1B40016C SATA_PHY_PI_CTRL1

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately.

This register configure CDR settings.

SATA_PHY_PI_CTRL1

Bits	Name	Description
31:8	UNUSED	
7:2	RESERVED	
1:0	PI_FILTER_BW_SEL	PI mixer Bandwidth select.

0x1B400170 SATA_PHY_DESER_RESV

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately

This register configures the Deser.

SATA_PHY_DESER_RESV

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B400174 SATA_PHY_RX_RESV0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately

This register configures the Deser.

SATA_PHY_RX_RESV0

Bits	Name	Description
31:8	UNUSED	
7:0	RESERVED	

0x1B400178 SATA_PHY_AD_TPA_CTRL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately

This register configures the A/D and TPA

SATA_PHY_AD_TPA_CTRL

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6:5	IDAC_MUX_SEL	Select source of IDAC MUX output fed to TPA analog path. Need AMUX_PAD_ENA=1 and AMUX_TOP_SEL=000 to observe. - 00: TX impedance calibration bit - 01: RX impedance calibration bit - 10: CDR phase control top 5 bits - 11: CDR frequency control top 5 bits
4	AMUX_PAD_ENA	Send analog test signal to TPA. Exclusive w.r.t. AMUX_PAD_ENA
3:1	AMUX_TOP_SEL	Analog test signal output selection: - 000 : From IDAC_MUX output. Refer to IDAC_MUX_SEL control table - 001 : vbg_1p20v_test observation - 010 : RX impedance calibration generated voltage - 011 : Iref_50uA_test Sink resistor 500Ohm needed for observation - 100: Test voltage from TX Refer to REG SATA_TX_DRIV_CTRL3 - 101: Test voltage from PLL top - 110: Test voltage from PLL regulator - 111: OOB squalch detector output raw signal
0	DMUX_PAD_ENA	Send digital test signal to TPA. Exclusive w.r.t. AMUX_PAD_ENA - 0: High Impedance - 1: Digital test signal out. Refer to REG <<">> for test LUT

0x1B40017C SATA_PHY_REFCLK_CTRL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately

This register configures the MPLL.

SATA_PHY_REFCLK_CTRL

Bits	Name	Description
31:8	UNUSED	
7:1	RESERVED	
0	CLK_SEL	Select reference clock source for SATA PLL: - 0: Default 100MHz diff. clock - 1: 27MHz on chip ref clock for test support

0x1B400180 SATA_PHY_POW_DWN_CTRL0

Type: Read/Write
Clock: WCLK
Reset State: 0x000000FE

Action Time: Writes to this register take effect immediately

This register configures the Power Down control.

SATA_PHY_POW_DWN_CTRL0

Bits	Name	Description
31:8	UNUSED	
7	PD_IMAC_IDAC	Power down imcal_idac in test MUX
6	RESERVED	
5	PD_SER_CTRL	Power down serializer
4	PD_TX_DRV_CTRL	Power down TX Driver
3	PD_POWER_GEN_CTRL	Power down PowerGen block
2	PD_REFCLK_BUFF	Power down Reference Clock Buffer(e.g. with 27MHz ref_clk)
1	PD_TX_IMCAL	Power down TX impedance calibration block
0	PWRDN_B	Power down all PHY blocks with software - 0: Power down all blocks,can overwrite other setting in REG SATA_PHY_POW_DWN_CTRL0 and SATA_PHY_POW_DWN_CTRL1 - 1: Normal function

0x1B400184 SATA_PHY_POW_DWN_CTRL1

Type: Read/Write
Clock: WCLK
Reset State: 0x000000FE

Action Time: Writes to this register take effect immediately

This register configures the Power Down Control.

SATA_PHY_POW_DWN_CTRL1

Bits	Name	Description
31:8	UNUSED	
7	PD_RX_IMCAL	Power down RX impedance calibration block
6	RESERVED	
5	PD_PI_CTRL	Power down phase interpolator (PI)
4	PD_EQ_CTRL	Power down Equalizer
3	PD_CDR_CTRL	Power down CDR
2	PD_DESER_CTRL	Power down de-serializer
1	PD_OOB_CTRL	Power down oob
0	PD_SEL_CTRL	Power down control mux selection - 0: normal operation - 1: SW control register override

0x1B400188 SATA_PHY_TX_DATA_CTRL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000011

Action Time: Writes to this register take effect immediately

This register configures the TX Data path

SATA_PHY_TX_DATA_CTRL

Bits	Name	Description
31:8	UNUSED	
7:5	RESERVED	
4	TX_BUF_RETIME_ENA	Enable for TX Datapath Re-time buffer.

SATA_PHY_TX_DATA_CTRL (cont.)

Bits	Name	Description
3:2	TX_MUX	Clock and data selection to serializer {tx_mux2, tx_mux1} - 00: tx_data, tx_hs_clk, asic_clkin - 01: bist_data, tx_hs_clk, bist_clk - 10: rx_lbk_data, rx_lbk_hs_clk, rx_byte_clk - 11: invalid during mission mode, MUX output tied LOW during test mode
1	DRV_TX_EN	Driver enable - 0: tx_en is controlled by en_bist or en_alignp or en_test_pattern or en_oob or phy_tx_enable_control (BIT 0 of SATA_PHY_TX_DATA_CTRL register) - 1: TX driver is enabled
0	PHY_TX_ENABLE_CONTROL	Control bit to gate tx driver enable - 0: tx is enabled by en_alignp or en_oob or en_test_pattern or en_prbs10b or drv_tx_en (BIT 1of SATA_PHY_TX_DATA_CTRL register) - 1: tx is enabled by phy_tx_enable

0x1B40018C SATA_PHY_BIST_GEN0

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately

This register configures the BIST Generation logic.

SATA_PHY_BIST_GEN0

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6	EN_PRBS10B	BIST prbs/10bit pattern generation enable. Note: bist_sel needs to be set. If the rx checker is used, this bit should be set to 0. - 0: disabled (0 output) - 1: enabled
5	PRBS10B_SEL	prbs/10bit pattern selection en_prbs10b has to be ’1’ - 0: prbs pattern - 1: 10 bit pattern

SATA_PHY_BIST_GEN0 (cont.)

Bits	Name	Description
4:0	P10B_SEL	- 10bit pattern selection p10b_sel[4:0] test10b[9:0] - 00000 1111100000 - 00001 1111000001 - 00010 1110100010 - 00011 1110000011 - 00100 1101100100 - 00101 1101000101 - 00110 1100100110 - 00111 1100000111 - 01000 1011101000 - 01001 1011001001 - 01010 1010101010 - 01011 1010001011 - 01100 1001101100 - 01101 1001001101 - 01110 1000101110 - 01111 1000001111 - 10000 0111110000 - 10001 0111010001 - 10010 0110110010 - 10011 0110010011 - 10100 0101110100 - 10101 0101010101 - 10110 0100110110 - 10111 0100010111 - 11000 0011111000 - 11001 0011011001 - 11010 0010111010 - 11011 0010011011 - 11100 0001111100 - 11101 0001011101 - 11110 0000111110 - 11111 0000011111

0x1B400190 SATA_PHY_BIST_GEN1

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

This register configures the BIST Generation logic

SATA_PHY_BIST_GEN1

Bits	Name	Description
31:8	UNUSED	
7	EN_LBP	BIST Lone Bit Pattern (LBP) generation enable. If the rx checker is used, this bit should be set to 0. - 0: disabled - 1: enabled
6	EN_ALIGNP	BIST ALIGNp pattern generation enable . - 0: disabled - 1: enabled
5	ALIGNP_SEL	ALINGp pattern selection - 0: K28.5- D10.2 D10.2 D27.3- - 1: K28.5+ D10.2 D10.2 D27.3+
4	EN_OOB	BIST OOB pattern generation enable
3	OOB_TYPE	OOB signal selection - 0: OOB comreset 320ns - 1: OOB comwake 106ns
2	EN_CHAN	Channel pattern generation enable. Note: bist_sel needs to be set. If the rx checker is used, this bit should be set to 0. - 0: disabled (0 output) - 1: enabled
1:0	PSEL	Selection of channel test pattern generation - 00: medium frequency test pattern - 01: low frequency test pattern - 10: high frequency test pattern - 11: not used

0x1B400194 SATA_PHY_BIST_GEN2

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

This register configures the BIST Generation logic.

SATA_PHY_BIST_GEN2

Bits	Name	Description
31:8	UNUSED	
7	RESERVED_1	

SATA_PHY_BIST_GEN2 (cont.)

Bits	Name	Description
6	COMP_PATTERN_SHORT	BIST comp pattern selection - 0: long composite pattern - 1: short composite pattern
5	EN_COMP	Composite pattern generation enable. Note: bist_sel needs to be set.m If the rx checker is used, this bit should be set to 0. - 0: disabled (0 output) - 1: enabled
4:2	BIST_SEL	MUX selection for BIST output bist[9:0]. The individual pattern related enables need to be set properly. Please refer to Figure 3-18 'BIST block diagram' in the QSerDes SATA Phy Integration guidelines. - 000 : comma pattern - 001 : channel test pattern - 010 : oob pattern - 011 : prbs /10 bit pattern gen - 10x : composite pattern - 11x : lone bit pattern
1	RD_SEL	Lone Bit Pattern (LBP) Running Disparity Select for LBP and Composite Pattern - 0: rd+ - 1: rd-
0	RESERVED_2	

0x1B400198 SATA_PHY_BIST_GEN3

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

This register configures the BIST Generation logic.

SATA_PHY_BIST_GEN3

Bits	Name	Description
31:8	UNUSED	
7:6	RESERVED_1	
5:4	RX_PAT_CHK_EN	Selects which RX BIST checker is to be activated - 00: Disabled - 01: PRBS Pattern checker. - 10: Channel Test Pattern checker. - 11: Composite Pattern checker.
3:2	RESERVED_2	

SATA_PHY_BIST_GEN3 (cont.)

Bits	Name	Description
1	RX_CHK_ERR_EN	Enable generation three error bits during PRBS/COMP/CHANNEL check loop - 0: disabled - 1: enabled
0	GEN_SHORT_PATTERN	- 0: Generate pattern data until rx_pat_chk_en set to 00 - 1: Generate 1composite pattern or N Channel Test Patterns (N is set by SATA_PHY_CHAN_COMP_CHK register), or PRBS generate 2^10 pattern then stop, depending on which is selected by rx_pat_chk_en.

0x1B40019C SATA_PHY_LBK_CTRL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

This register configures.

SATA_PHY_LBK_CTRL

Bits	Name	Description
31:8	UNUSED	
7:2	RESERVED	
1	NE_LBK_EN_SEL	MUX selection for NE_lbk_en - 0: control by external nearafelb - 1: control by register bits
0	NEARAFELB_EN	MUX selection for NE_lbk_en - 0: control by external nearafelb - 1: control by register bits

0x1B4001A0 SATA_PHY_TEST_DEBUG_CTRL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

This register configures.

SATA_PHY_TEST_DEBUG_CTRL

Bits	Name	Description
31:8	UNUSED	
7:5	DEBUG_BUS_SEL	MUX selection for 32 bit debug bus - 000: 32 bit debug bus value is zero. - 001: 32 bit debug bus value from SATA_PHY_DEBUG_BUS_STAT3/2/1/0. - 010: 32 bit debug bus value from UNIPHY PLL debug bus selected by UNIPHY_PLL_DEBUG_BUS_SEL[7:0]
4:0	DTESTMUX_SEL	- 32 internal digital signals to be selected to a single TPA pad

0x1B4001A4 SATA_PHY_ALIGNP

Type: Read/Write
Clock: WCLK
Reset State: 0x0000004F

This register configures the ALIGNp counter settings.

SATA_PHY_ALIGNP

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6	COM_DET_ENA	Enables comma detection output - 0: Disabled - 1: Enabled
5	CFG_ALIGNP_DET_DIS	Disables alignp detection. - 0: Not disabled - 1: Disabled.
4:0	CFG_MAX_ALIGNP_CONT	Alignp counter settings - 5 bits - 64 continous ALIGNp Dword per cont including the align dword count cfg_max_alignp_cont is the maximum upper 5 bits of the 11 bit counter - 00000 : 2^6 Dword - 00001 : 2^7 Dword - 00011 : 2^8 Dword - 00111 : 2^9 Dword - 01111 : 2^10 Dword - 11111: 2^11 Dword The default max alignp dword is 2^10-1, the max upper 5 bits, is 5b0_1111 as the default value

0x1B4001A8 SATA_PHY_PRBS_CFG0

Type: Read/Write
Clock: WCLK
Reset State: 0x000000FF

Action Time: Writes to this register take effect immediately.

This register configures the PRBS settings. A seed value of 0x67 should not be used.

SATA_PHY_PRBS_CFG0

Bits	Name	Description
31:8	UNUSED	
7:0	PRBS_SEED_7_0	User defined PRBS seed for the Generator and Checker. Some example seeds for the user: data_seed[9:0]: - 1010110010 - 1101000111 - 0111110101 - 1000010000

0x1B4001AC SATA_PHY_PRBS_CFG1

Type: Read/Write
Clock: WCLK
Reset State: 0x00000003

Action Time: Writes to this register take effect immediately.

This register configures the PRBS settings. A seed value of 0x67 should not be used.

SATA_PHY_PRBS_CFG1

Bits	Name	Description
31:8	UNUSED	
7:2	RESERVED	
1:0	PRBS_SEED_9_8	User defined PRBS seed for the Generator and Checker.

0x1B4001B0 SATA_PHY_PRBS_CFG2

Type: Read/Write
Clock: WCLK
Reset State: 0x00000009

Action Time: Writes to this register take effect immediately.

This register configures the PRBS settings.

SATA_PHY_PRBS_CFG2

Bits	Name	Description
31:8	UNUSED	
7:0	PRBS_POLYNOM_7_0	User defined PRBS polynomial for the Generator and Checker. An example polynomial for the user: prbs_polynom[10:0]: - 100_0000_1001

0x1B4001B4 SATA_PHY_PRBS_CFG3

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

Action Time: Writes to this register take effect immediately.

This register configures the PRBS settings.

SATA_PHY_PRBS_CFG3

Bits	Name	Description
31:8	UNUSED	
7:2	RESERVED	
1:0	PRBS_POLYNOM_9_8	User defined PRBS polynomial for the Generator and Checker. Bit 10 is assumed to be 1 and therefore ommitting the need to explicity specify via register write.

0x1B4001B8 SATA_PHY_CHAN_COMP_CHK_CNT

Type: Read/Write
Clock: WCLK
Reset State: 0x0000003F

This register configures the error checker duration for short Channel and Composite error checks.

SATA_PHY_CHAN_COMP_CHK_CNT

Bits	Name	Description
31:8	UNUSED	

SATA_PHY_CHAN_COMP_CHK_CNT (cont.)

Bits	Name	Description
7:0	CHAN_COMP_CHK_CNT	When the short pattern option is set and the Channel Test Pattersn type is selected, this counter specifies how long the active error check duration is. This is user programmable from 15 to 4095 cycles, in 16 cycle increments. chan_comp_chk_cnt[7:0] - 0000_0000: 15 cycles - 0000_0001: 31 cycles - 0000_0010: 47 cycles ... - 1111_1111: 4095 cycles

0x1B4001BC SATA_PHY_RESET_CTRL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

This register allows the application of the S/W Reset.

SATA_PHY_RESET_CTRL

Bits	Name	Description
31:8	UNUSED	
7:1	RESERVED	
0	SW_RESET	S/W Reset Control

0x1B4001C0 SATA_PHY_RX_CLR

Type: Read/Write
Clock: WCLK
Reset State: 0x00000000

This register allows for the clearing of select SATA_PHY_RX related registers.

SATA_PHY_RX_CLR

Bits	Name	Description
31:8	UNUSED	
7:5	RESERVED_1	
4	FORCE_RX_ENABLE_ON	When asserted, the PHY offline mode feature is disabled
3:1	RESERVED_2	

SATA_PHY_RX_CLR (cont.)

Bits	Name	Description
0	RX_STAT_CLR	When asserted, the contents of SATA_PHY_RX_CHK_ERR_CNT0, SATA_PHY_RX_CHK_ERR_CNT1will be cleared. SW should assert this bit then de-assert the bit after the registers values have been cleared.

0x1B4001C4 SATA_PHY_RX_EBUF_CTRL

Type: Read/Write
Clock: WCLK
Reset State: 0x00000002

This register is for elastic buffer retime loop back for debug purpose.

SATA_PHY_RX_EBUF_CTRL

Bits	Name	Description
31:8	UNUSED	
7:4	RESERVED	
3	RX_EBUF_COMMA_INSERT_EN	When EBUF empty, 1 => comma symbol inserted,0 => zero inserted
2	RX_EBUF_ALIGNP_INSERT_EN	When EBUF empty, two back-back ALIGNP inserted
1	RX_EBUF_ALIGNP_DROP_EN	Drop ALIGNP before RX data pushed into EBUF
0	RX_EBUF_EN	Enable elastic buffer retime loopback

0x1B4001C8 SATA_PHY_REVISION_ID0

Type: Read
Clock: WCLK
Reset State: 0x00000000

This register shows the status of the ID0 <7:0>.

SATA_PHY_REVISION_ID0

Bits	Name	Description
31:8	UNUSED	
7:0	STEP_7_0	READ ONLY No description for this yet.

0x1B4001CC SATA_PHY_REVISION_ID1

Type: Read
Clock: WCLK
Reset State: 0x00000000

This register shows the status of the ID1 <7:0>.

SATA_PHY_REVISION_ID1

Bits	Name	Description
31:8	UNUSED	
7:0	STEP_15_8	READ ONLY No description for this yet.

0x1B4001D0 SATA_PHY_REVISION_ID2

Type: Read
Clock: WCLK
Reset State: 0x00000000

This register shows the status of the ID2 <7:0>.

SATA_PHY_REVISION_ID2

Bits	Name	Description
31:8	UNUSED	
7:0	MINOR_7_0	READ ONLY No description for this yet.

0x1B4001D4 SATA_PHY_REVISION_ID3

Type: Read
Clock: WCLK
Reset State: 0x00000010

This register shows the status of the ID3 <7:0>.

SATA_PHY_REVISION_ID3

Bits	Name	Description
31:8	UNUSED	
7:4	MAJOR	READ ONLY No description for this yet.

SATA_PHY_REVISION_ID3 (cont.)

Bits	Name	Description
3:0	MINOR_11_8	READ ONLY No description for this yet.

0x1B4001D8 SATA_PHY_RX_CHK_ERR_CNT0

Type: Read
Clock: WCLK
Reset State: 0x00000000

This register shows the status of the RX Checker Error Counter.

SATA_PHY_RX_CHK_ERR_CNT0

Bits	Name	Description
31:8	UNUSED	
7:0	RX_CHK_ERR_CNT_7_0	READ ONLY LSBs of the 16 bit RX BIST Error Checker Counter

0x1B4001DC SATA_PHY_RX_CHK_ERR_CNT1

Type: Read
Clock: WCLK
Reset State: 0x00000000

This register shows the status of the RX Checker Error Counter.

SATA_PHY_RX_CHK_ERR_CNT1

Bits	Name	Description
31:8	UNUSED	
7:0	RX_CHK_ERR_CNT_15_8	READ ONLY MSBs of the 16 bit RX BIST Error Checker Counter.

0x1B4001E0 SATA_PHY_RX_CHK_STAT

Type: Read
Clock: WCLK
Reset State: 0x00000000

This register shows the status of the RX BIST Checker.

SATA_PHY_RX_CHK_STAT

Bits	Name	Description
31:8	UNUSED	
7	RESERVED_1	
6	CDR_ALIGN_DET	READ ONLY Asserts when the specified number of ALIGNp patterns have been detected.
5	RX_SIGNAL_VALID	READ ONLY High indicates that the concurrent RX_DATA outputs are valid. Low indicates that the RX_DATA outputs should be ignored.
4	RXCHK_HEADER_SEL	READ ONLY Indicates whether the rxchk header is used.
3	RESERVED_2	
2	PAT_DATA_NOT_FOUND	READ ONLY Indicates that the RX Checker FSM has found the Header but can not find the Pattern data and timeout has occurred. - 0: Pattern Data check timeout has not occurred. - 1: Can not find Pattern Data, timeout has occurred.
1	HEADER_NOT_FOUND	READ ONLY Indicates that the RX Checker FSM has not found the Header for the pattern. - 0: Header Timeout has not occured. - 1: Can not find Header, timeout has occurred.
0	CHECK_DONE	READ ONLY Indicates when the RX Checker FSM has finished the short pattern check

0x1B4001E4 SATA_PHY_TX_IMCAL_STAT

Type: Read
Clock: WCLK
Reset State: 0x00000020

This register shows the status of the TX calibration.

SATA_PHY_TX_IMCAL_STAT

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6	TX_IMCAL_VOTER_ERROR	READ ONLY

SATA_PHY_TX_IMCAL_STAT (cont.)

Bits	Name	Description
5:1	TX_IMCAL_STR	READ ONLY Value of calibraton string.
0	TX_IMCAL_DONE	READ ONLY Value of calibration done.

0x1B4001E8 SATA_PHY_RX_IMCAL_STAT

Type: Read
Clock: WCLK
Reset State: 0x00000020

This register shows the status of the RX calibration.

SATA_PHY_RX_IMCAL_STAT

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6	RX_IMCAL_VOTER_ERRO R	READ ONLY
5:1	RX_IMCAL_STR	READ ONLY Value of calibraton string.
0	RX_IMCAL_DONE	READ ONLY Value of calibration done.

0x1B4001EC SATA_PHY_RX_EBUF_STAT

Type: Read
Clock: WCLK
Reset State: 0x00000000

This register shows elastic buffer error status

SATA_PHY_RX_EBUF_STAT

Bits	Name	Description
31:8	UNUSED	
7	RESERVED	
6:5	RX_EBUF_ERR_OVERFLO W	READ ONLY Bit 0 => FIFO overflow, 1 => Tx data buffer overflow

SATA_PHY_RX_EBUF_STAT (cont.)

Bits	Name	Description
4:0	RX_EBUF_ERR_CNT	READ ONLY Number of RX data ALIGNP errors

0x1B4001F0 SATA_PHY_DEBUG_BUS_STAT0

Type: Read
Clock: WCLK
Reset State: 0x00000000

This register shows debug bus status

SATA_PHY_DEBUG_BUS_STAT0

Bits	Name	Description
31:8	UNUSED	
7:0	DEBUG_BUS_STAT0	READ ONLY Status of debug bus zero

0x1B4001F4 SATA_PHY_DEBUG_BUS_STAT1

Type: Read
Clock: WCLK
Reset State: 0x00000000

This register shows debug bus status

SATA_PHY_DEBUG_BUS_STAT1

Bits	Name	Description
31:8	UNUSED	
7:0	DEBUG_BUS_STAT1	READ ONLY Status of debug bus zero

0x1B4001F8 SATA_PHY_DEBUG_BUS_STAT2

Type: Read
Clock: WCLK
Reset State: 0x00000000

This register shows debug bus status

SATA_PHY_DEBUG_BUS_STAT2

Bits	Name	Description
31:8	UNUSED	
7:0	DEBUG_BUS_STAT2	READ ONLY Status of debug bus zero

0x1B4001FC SATA_PHY_DEBUG_BUS_STAT3

Type: Read
Clock: WCLK
Reset State: 0x00000000

This register shows debug bus status

SATA_PHY_DEBUG_BUS_STAT3

Bits	Name	Description
31:8	UNUSED	
7:0	DEBUG_BUS_STAT3	READ ONLY Status of debug bus zero

19 SFPB Wrapper Registers

19.1 Overview

Table 19-1 SFPB_Wrapper Bases

Base Name	Parent	Address
SFPB_XPU_APU_RGn_RACR	SFPB_WRAPPER_XPU_BASE	0x00E00000
SFPB_SFPB_CTRL_STATUS	SFPB_WRAPPER_BASE	0x00F00000
SFPB_MUTEX_MUTEX_SW_RESET	SFPB_WRAPPER_MUTEX_BASE	0x01200000
SFPB_1x2_SFPB_CTRL_STATUS	SFPB_WRAPPER_1x2_BASE	0x01600000
SFPB_2x1_SFPB_CTRL_STATUS	SFPB_WRAPPER_2x1_BASE	0x01800000

19.2 SFPB XPU Registers (0x00E00000 SFPB_WRAPPER_XPU_BASE)

This section contains System FPB XPU registers.

19.2 XPU Registers

0x00E00000+ 4*n SFPB_XPU_APU_RGn_RACR, n=[0..23]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type APU. These registers include a single bit per VMID granting read access.

SFPB_XPU_APU_RGn_RACR

Bits	Name	Description
31:0	RE	Read enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read access to the registers in the associated resource group.

0x00E00400+ 4*n SFPB_XPU_APU_RGn_WACR, n=[0..23]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

These registers exist only for the case when APU_IDR[MV, PT] = 11, i.e., a multi-VMID, read/write access vs. read-only access permission type APU.

SFPB_XPU_APU_RGn_WACR

Bits	Name	Description
31:0	WE	Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID write access to the registers in the associated resource group.

0x00E00F80 SFPB_XPU_APU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

SFPB_XPU_APU_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set APU_ESR. APU_EAR and APU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set APU_ESR. APU_EAR and APU_ESYNR0 updated with address and syndrome of error.
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x00E00F84 SFPB_XPU_APU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port.

SFPB_XPU_APU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x00E00F88 SFPB_XPU_APU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is contrasted with the fields in the APU_ESYNRn registers, which are merely the "syndrome" of an error indicated by APU_ESR.

SFPB_XPU_APU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x00E00F8C SFPB_XPU_APU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

SFPB_XPU_APU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x00E00F90 SFPB_XPU_APU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

SFPB_XPU_APU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x00E00F94 SFPB_XPU_APU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

SFPB_XPU_APU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x00E00FF4 SFPB_XPU_APU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

SFPB_XPU_APU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved

SFPB_XPU_APU_REV (cont.)

Bits	Name	Description
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x00E00FF8 SFPB_XPU_APU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x00001C17

APU ID Register: Read-only register that defines various configuration attributes of the APU instance.

SFPB_XPU_APU_IDR

Bits	Name	Description
31:29	RESERVED31_21	Reserved
28:24	MSB	Indicates most significant address bit number used to select a resource group
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.

SFPB_XPU_APU_IDR (cont.)

Bits	Name	Description
9:8	RESERVED9_8	Reserved
7:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

0x00E00FFC SFPB_XPU_APU_APU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

APU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the APU (including the APU_APU_ACR itself).

SFPB_XPU_APU_APU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the APU's 4KB address region (including the APU_APU_ACR itself). For single VMID type APUs (APU_IDR[MV] = 0) the APU_APU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

19.3 System FPB 2x23 Registers (0x00F00000 SFPB_WRAPPER_BASE)

This section contains System FPB configuration registers.

19.3.1 Configuration registers

0x00F00000 SFPB_SFPB_CTRL_STATUS

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000

The SFPB_CTRL_STATUS register is a general configuration register.

SFPB_SFPB_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables Power up value is clear (0)
11	RPM_ARM7_IRQ_EN	SW: RW, HW: R ARM7InterruptEnable When set, the ARM7 receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	SC_IRQ_EN	SW: RW, HW: R ScorpionInterruptEnable When set, the Scorpion receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

SFPB_SFPB_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x6: Select the S1_M1 ahb2ahb bdg tbus.

0x00F00044 SFPB_SFPB_PORT_EN

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFF

The SFPB_PORT_EN register is a SFPB master port enable register.

SFPB_SFPB_PORT_EN

Bits	Name	Description
31:2	RESERVED_BIT31_2	
1	M1_PORT_EN	SW: RW, HW: R M1PortEnable When cleared (0), M1 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)
0	M0_PORT_EN	SW: RW, HW: R M0PortEnable When cleared (0), M0 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

19.3.2 Bus error registers and additional configure registers

0x00F00050 SFPB_SFPB_ERROR_STAT

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000000

The SFPB_ERROR_STAT register is the bus error status register.

SFPB_SFPB_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the channel ID that caused the detected error when CID is valid for the master of the access. If not, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Master0 0x1: Master1
11:10	RESERVED_BITS11_10	
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit
3:2	RESERVED_BIT3_2	

SFPB_SFPB_ERROR_STAT (cont.)

Bits	Name	Description
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted. Clearing (0) this bit clears any interrupts asserted as well as enables the SFPB_ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x00F00054 SFPB_SFPB_ERROR_ADDR

Type: Read
Clock: CC_SFPB_CLK
Reset State: 0x00000000

The SFPB_ERROR_ADDR register contains the bus error address.

SFPB_SFPB_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when SFPB_ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x00F00058 SFPB_SFPB_GPREG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0000

The SFPB_GPREG register is a configurable general purpose register.

SFPB_SFPB_GPREG

Bits	Name	Description
31:18	RESERVED_BITS31_18	
17	SFPB_MSM_BRIDGE_TIME_OUT_EN	SW: RW, HW: W GpregContent Enable/Disable SFPB APQ BRIDGE TIME OUT EN. Power up value is clear (0)
16:9	SFPB_MSM_BRIDGE_TIME_OUT_VAL	SW: RW, HW: W GpregContent Set SFPB APQ BRIDGE TIME OUT COUNTER. Power up value is clear (0)
8	MPM_MSM_BRIDGE_TIME_OUT_EN	SW: RW, HW: W GpregContent Enable/Disable MPM APQ BRIDGE TIME OUT EN. Power up value is clear (0)
7:0	MPM_MSM_BRIDGE_TIME_OUT_VAL	SW: RW, HW: W GpregContent Set MPM APQ BRIDGE TIME OUT COUNTER. Power up value is clear (0)

0x00F0005C SFPB_SFPB_XPU_ACR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFFFFFF

The SFPB_XPU_ACR register is a SFPB Access Control Register for configure register protection.

SFPB_SFPB_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R ACR RWE SFPB XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the SFPB configure space, including this register itself. Power up value is set (1)

0x00F00060 SFPB_SFPB_HW_CLK_GATING_CFG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0000

The SFPB_HW_CLK_GATING_CFG register is for hardware clock gating configuration register.

SFPB_SFPB_HW_CLK_GATING_CFG

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	HYSTERESIS_CNT_SW	SW: RW, HW: R Hysteresis Conter Value The value of this field is from SW to set the hysteresis counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING set to 1. Power up value is clear (0)
3:0	WAKE_CNT_SW	SW: RW, HW: R Wakeup Counter Value The value of this field is from SW to set the wakeup counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING set to 1. Power up value is clear (0)

19.4 SFPB MUTEX Registers (0x01200000 SFPB_WRAPPER_MUTEX_BASE)

This section describes all of the System FPM MUTEX registers including behavior. The behavior of any MUTEX register is split into read and write. On a Processor read, the value stored is simply returned. On a Processor write, if the value to be written is `0' then it is written; if the value to be written is non-zero, then it is written only if the stored value is `0'.

0x01200600 SFPB_MUTEX_MUTEX_SW_RESET

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0

MUTEX_SW_RESET register resets the MUTEX_REGn blocks. Software has to assert and then de-assert the reset in order to clear the MUTEX_REGn.

SFPB_MUTEX_MUTEX_SW_RESET

Bits	Name	Description
0	RESET	0x0: de-asserts reset 0x1: asserts reset

0x01200604+4*n SFPB_MUTEX_MUTEX_REGn, n=[0..31]

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0

The MUTEX_REGn register specifies the information regarding the access status of each of the 32 sections of memory, which is denoted by n. Register contents of 0 imply that the respective section of memory is free to use, and therefore unlocked. Non-zero contents would imply that the respective section of memory is in use, and therefore locked.

SFPB_MUTEX_MUTEX_REGn

Bits	Name	Description
3:0	REG_DATA	Mutex register data.

19.5 System FPB 1x2 Registers (0x01600000 SFPB_WRAPPER_1x2_BASE)

This section contains the System FPB 1x2 registers.

19.5.1 Configuration registers

0x01600000 SFPB_1X2_SFPB_CTRL_STATUS

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000

The SFPB_CTRL_STATUS register is a general configuration register

SFPB_1X2_SFPB_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables Power up value is clear (0)
11	RPM_ARM7_IRQ_EN	SW: RW, HW: R ARM7InterruptEnable When set, the ARM7 receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	SC_IRQ_EN	SW: RW, HW: R ScorpionInterruptEnable When set, the Scorpion receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

SFPB_1X2_SFPB_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x7: Select the M0 ahb2ahb bridge test bus.

0x01600004+ 0x4*a SFPB_1X2_SFPB_AHB2AHB_CFG_Ma, a=[0..0]

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x09

The SFPB_AHB2AHB_CFG_Ma register is to configure the AHB2AHB bridge of master Ma. The AHB2AHB bridge is instantiated if the AHB interface is async (Generic: MASTER_ASYNC_IF(a) = ’1’). Otherwise this register is reserved.

SFPB_1X2_SFPB_AHB2AHB_CFG_Ma

Bits	Name	Description
30:6	RESERVED_BITS30_6	
5:4	M_AHB2AHB_TEST_EN	SW: RW, HW: R Test enable for the Sa lite_bridge. Power up value is 00 0x0: DISABLED 0x1: Select slave side test signals 0x2: Select master side test signals 0x3: RESERVED_PROGRAMMING
3	M_WPOST_EN	SW: RW, HW: R MaWritePostEnable When set (1), the ahb2ahb bridge will support posting of write data. When cleared (0), each write request must complete across the bus before the next is accepted. Power up value is set (1)
2	M_HALT_ACK	SW:R, HW:W Indicates the Ma acknowledgement of halt_req asserted by software. Power up value is clear (0).

SFPB_1X2_SFPB_AHB2AHB_CFG_Ma (cont.)

Bits	Name	Description
1	M_HALT_REQ	SW:RW, HW:R Software should write to this register to request the Ma lite_bridge master to cleanly halt. Power up value is clear (0).
0	M_IDLE	SW:R, HW:W Indicates that the Ma lite bridge master FSM is in IDLE state. Power up value is set (1).

0x01600044 SFPB_1X2_SFPB_PORT_EN

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x1

The SFPB_PORT_EN register is a SFPB master port enable register.

SFPB_1X2_SFPB_PORT_EN

Bits	Name	Description
31:1	RESERVED_BIT31_1	
0	M0_PORT_EN	SW: RW, HW: R M0PortEnable When cleared (0), M0 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

19.5.2 Bus error registers and additional configure registers

0x01600050 SFPB_1X2_SFPB_ERROR_STAT

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000000

The SFPB_ERROR_STAT register is the bus error status register.

SFPB_1X2_SFPB_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	

SFPB_1X2_SFPB_ERROR_STAT (cont.)

Bits	Name	Description
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the channel ID that caused the detected error when CID is valid for the master of the access. If not, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Master0 0x1: Master1 0x2: Master2 0x3: Master3 0x4: Master4 0x5: Master5 0x6: Master6 0x7: Master7 0x8: Master8 0x9: Master9 0xA: Master10 0xB: Master11 0xC: Master12 0xD: Master13 0xE: Master14 0xF: Master15
11:10	RESERVED_BITS11_10	
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	

SFPB_1X2_SFPB_ERROR_STAT (cont.)

Bits	Name	Description
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit
3:2	RESERVED_BIT3_2	
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted. Clearing (0) this bit clears any interrupts asserted as well as enables the SFPB_ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x01600054 SFPB_1X2_SFPB_ERROR_ADDR

Type: Read
Clock: CC_SFPB_CLK
Reset State: 0x00000000

The SFPB_ERROR_ADDR register contains the bus error address.

SFPB_1X2_SFPB_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when SFPB_ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x01600058 SFPB_1X2_SFPB_GPREG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0000

The SFPB_GPREG register is a configurable general purpose register.

SFPB_1X2_SFPB_GPREG

Bits	Name	Description
31:0	RESERVED_BIT31_0	

0x0160005C SFPB_1X2_SFPB_XPU_ACR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFFFFFF

The SFPB_XPU_ACR register is a SFPB Access Control Register for configure register protection.

SFPB_1X2_SFPB_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R ACR RWE SFPB XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the SFPB configure space, including this register itself. Power up value is set (1)

0x01600060 SFPB_1X2_SFPB_HW_CLK_GATING_CFG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0000

The SFPB_HW_CLK_GATING_CFG register is for hardware clock gating configuration register.

SFPB_1X2_SFPB_HW_CLK_GATING_CFG

Bits	Name	Description
31:11	RESERVED_BITS31_11	

SFPB_1X2_SFPB_HW_CLK_GATING_CFG (cont.)

Bits	Name	Description
10:4	HYSTERESIS_CNT_SW	SW: RW, HW: R Hysteresis Counter Value The value of this field is from SW to set the hysteresis counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING set to 1. Power up value is clear (0)
3:0	WAKE_CNT_SW	SW: RW, HW: R Wakeup Counter Value The value of this field is from SW to set the wakeup counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING set to 1. Power up value is clear (0)

19.6 System FPB 2x1 Registers (0x01800000 SFPB_WRAPPER_2x1_BASE)

This section contains the System FPB 2x1 registers.

19.6.1 System FPB 2x1 Registers

19.6.1.1 Configuration registers

0x01800000 SFPB_2X1_SFPB_CTRL_STATUS

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000

The SFPB_CTRL_STATUS register is a general configuration register.

SFPB_2X1_SFPB_CTRL_STATUS

Bits	Name	Description
31:13	RESERVED_BIT31_13	
12	XPU_EN	SW: RW, HW: R Default slave xpu enable bit When set, default slave xpu ACR register enables Power up value is clear (0)
11	RPM_ARM7_IRQ_EN	SW: RW, HW: R ARM7InterruptEnable When set, the ARM7 receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
10	SC_IRQ_EN	SW: RW, HW: R ScorpionInterruptEnable When set, the Scorpion (or other application processors such as Krait) receives an interrupt whenever SFPB_ERROR_STAT:ERROR_DETECT is set (1). Power up value is clear (0).
9	SFPB_ADDR_DEC_HALT_EN	SW:RW, HW:R This bit enables the gating of FPB slaves' hsel with clk halt signals from the clock control block. Power up value is clear (0) (disabled).
8:5	DEFAULT_MASTER	SW: RW, HW: R Power up value is 0000

SFPB_2X1_SFPB_CTRL_STATUS (cont.)

Bits	Name	Description
4:0	SFPB_TEST_EN	SW: RW, HW: R Test enable for the system_fpb bus. Others: RESERVED_PROGRAMMING Power up value is 00000 0x0: DISABLED 0x1: Select the test_bus_sfpb (AHB BUS.) 0x2: Select the test_bus_sfpb1 (AHB BUS.) 0x3: Select the test_bus_sfpb2 (AHB BUS.) 0x4: Select the test_bus_sfpb3 (AHB BUS.) 0x6: Select the S1_M1 ahb2ahb bdg tbus.

0x01800044 SFPB_2X1_SFPB_PORT_EN

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFF

The SFPB_PORT_EN register is a SFPB master port enable register.

SFPB_2X1_SFPB_PORT_EN

Bits	Name	Description
31:2	RESERVED_BIT31_2	
1	M1_PORT_EN	SW: RW, HW: R M1PortEnable When cleared (0), M1 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)
0	M0_PORT_EN	SW: RW, HW: R M0PortEnable When cleared (0), M0 bridge is prevented from arbitrating on the system_fpb bus. Power up value is set (1)

19.6.1.2 Bus error registers and additional configure registers

0x01800050 SFPB_2X1_SFPB_ERROR_STAT

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x000000

The SFPB_ERROR_STAT register is the bus error status register.

SFPB_2X1_SFPB_ERROR_STAT

Bits	Name	Description
31:22	RESERVED_BITS31_22	
21:18	ERROR_CID	SW: R, HW: W ErrorDMChannelIDStatus Indicates the channel ID that caused the detected error when CID is valid for the master of the access. If not, this field is reserved. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
17:16	RESERVED_BITS17_16	
15:12	ERROR_PID	SW: R, HW: W ErrorPortIDStatus Indicates the port ID of the master that generated the detected error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: Master0 0x1: Master1
11:10	RESERVED_BITS11_10	
9:8	ERROR_TYPE	SW: R, HW: W ErrorTypeStatus Indicates the type of error detected. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: System FPB xPU security violation 0x1: Invalid FPB address 0x2: Slave asserted error (also includes invalid SPB addresses and SPB bus timeouts) 0x3: RESERVED
7	RESERVED_BIT7_6	
6:4	ERROR_HSIZE	SW: R, HW: W ErrorHSizeStatus Indicates the width of the transfer to cause a bus error. Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0). 0x0: 8-bit 0x1: 16-bit 0x2: 32-bit
3:2	RESERVED_BIT3_2	

SFPB_2X1_SFPB_ERROR_STAT (cont.)

Bits	Name	Description
1	ERROR_HWRITE	SW: R, HW: W ErrorHWriteStatus Only valid when ERROR_DETECT is set (1). ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).
0	ERROR_DETECT	SW: RW, HW: RW ErrorDetect When set (1), a bus error has been detected and interrupts will be asserted. Clearing (0) this bit clears any interrupts asserted as well as enables the SFPB_ERROR_ STAT register to capture the next error detected. Power up value is clear (0)

0x01800054 SFPB_2X1_SFPB_ERROR_ADDR

Type: Read
Clock: CC_SFPB_CLK
Reset State: 0x00000000

The SFPB_ERROR_ADDR register contains the bus error address.

SFPB_2X1_SFPB_ERROR_ADDR

Bits	Name	Description
31:0	ERROR_ADDR	SW: R, HW: W ErrorAddress Indicates the bus address that caused the captured bus error. Only valid when SFPB_ERROR_STAT:ERROR_DETECT = 1. ERROR_DETECT must be clear (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT has been cleared (0).

0x01800058 SFPB_2X1_SFPB_GPREG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0000

The SFPB_GPREG register is a configurable general purpose register.

SFPB_2X1_SFPB_GPREG

Bits	Name	Description
31:0	RESERVED_BITS31_0	

0x0180005C SFPB_2X1_SFPB_XPU_ACR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0xFFFFFFFF

The SFPB_XPU_ACR register is a SFPB Access Control Register for configure register protection.

SFPB_2X1_SFPB_XPU_ACR

Bits	Name	Description
31:0	RWE	SW: RW, HW: R ACR RWE SFPB XPU Access control Register. Each bit position corresponds to a VMID. When set to 1, that VMID is granted VMID read/write access to the SFPB configure space, including this register itself. Power up value is set (1)

0x01800060 SFPB_2X1_SFPB_HW_CLK_GATING_CFG

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0000

The SFPB_HW_CLK_GATING_CFG register is for hardware clock gating configuration register.

SFPB_2X1_SFPB_HW_CLK_GATING_CFG

Bits	Name	Description
31:11	RESERVED_BITS31_11	
10:4	HYSTERESIS_CNT_SW	SW: RW, HW: R Hysteresis Counter Value The value of this field is from SW to set the hysteresis counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING set to 1. Power up value is clear (0)

SFPB_2X1_SFPB_HW_CLK_GATING_CFG (cont.)

Bits	Name	Description
3:0	WAKE_CNT_SW	SW: RW, HW: R Wakeup Counter Value The value of this field is from SW to set the wakeup counter for hardware clock gating scheme. This field is used when ENABLE_HW_CLK_GATING set to 1. Power up value is clear (0)

0x01800064 SFPB_2X1_SFPB_XPU_ACR_ERR_STATUS

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: 0x0000

The SFPB_XPU_ACR_ERR_STATUS register is for capturing the status when there is an XPU (ACR) access error.

SFPB_2X1_SFPB_XPU_ACR_ERR_STATUS

Bits	Name	Description
31:27	RESERVED_BITS31_27	
26:22	HVMID	SW: RW, HW: W HVMID of the CSR access that caused an Error. Only valid when ERROR_DETECT_CSR is set (1). ERROR_DETECT_CSR must be cleared (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT_CSR has been cleared (0).
21	HWRITE	SW: RW, HW: W HVMID of the CSR access that caused an Error. Only valid when ERROR_DETECT_CSR is set (1). ERROR_DETECT_CSR must be cleared (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT_CSR has been cleared (0).
20:9	HADDR	SW: RW, HW: W HADDR of the CSR access that caused an Error. Only valid when ERROR_DETECT_CSR is set (1). ERROR_DETECT_CSR must be cleared (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT_CSR has been cleared (0).
8:6	HSIZE	SW: RW, HW: W HSIZE of the CSR access that caused an Error. Only valid when ERROR_DETECT_CSR is set (1). ERROR_DETECT_CSR must be cleared (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT_CSR has been cleared (0).

SFPB_2X1_SFPB_XPU_ACR_ERR_STATUS (cont.)

Bits	Name	Description
5	HPROTNS	SW: RW, HW: W HPROTNS of the CSR access that caused an Error. Only valid when ERROR_DETECT_CSR is set (1). ERROR_DETECT_CSR must be cleared (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT_CSR has been cleared (0).
4:1	HPROT	SW: RW, HW: W HPROT of the CSR access that caused an Error. Only valid when ERROR_DETECT_CSR is set (1). ERROR_DETECT_CSR must be cleared (0) for this field to load - that is, it only loads the first detected error after ERROR_DETECT_CSR has been cleared (0).
0	ERROR_DETECT_CSR	SW: RW, HW: RW ErrorDetect during CSR accesses. When set (1), a bus error has been detected and interrupts will be asserted. Clearing (0) this bit clears any interrupts asserted as well as enables the SFPB_XPU_ACR_ERR_STATUS register to capture the next error detected. Power up value is clear (0)

19.6.1.3 M2VMT (hmaster index) registers(existing when VMIDMAPPER=1)

0x01801000+ 0x4*n SFPB_2X1_M2VMT_M2VMRn, n=[0..1]

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: Undefined

M2VMT_M2VMRn registers are used to map from the input client port M2VCBMT index to a context bank and VMID.

Where n = NUM_M2VMT_ENTRIES from the design generics

SFPB_2X1_M2VMT_M2VMRn

Bits	Name	Description
31:5	RESERVED	n = NUM_M2VMT_ENTRIES from the design generic/parameter.

SFPB_2X1_M2VMT_M2VMRn (cont.)

Bits	Name	Description
4:0	VMID	Virtual machine ID Defines VMID value associated with the M2VMT index. Maximum of 512 entries (9 bit M2VMT index). Initialization software must be aware of specific bit-level assignment of the signal that makes up the M2VMT index in order to make the proper master to M2VMT_M2VRn address associations.

0x01801F80 SFPB_2X1_M2VMT_CR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: xxx0

Global configuration register.

Note: When REMOVE_M2VMT_RPU = ’1’, this register is not available. Also, bit [2], is not valid or has no effect when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT =‘1’.

SFPB_2X1_M2VMT_CR

Bits	Name	Description
31:4	RESERVED	
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., in valid addresses) are recorded as such. Decode error is asserted when config access to un-implemented and/or unmapped register/address are done. Also, note that decode error is never asserted for client port accesses. When value is set to ’0’ i.e., ’do not record’, decode errors do not set the M2VMT_ESR[CFG], and M2VMT_EAR & M2VMT_SYNRn is not updated. When value is set to ’1’, i.e., ’record’, decode errors set M2VMT_ESR[CFG] and M2VMT_EAR & M2VMT_SYNRn is updated with the address and the syndrome of the error. Reset State: x
2	RPUEIE	RPU error interrupt Enable: When set, configuration port errors are reported directly to the interrupt controller via the M2VMT_intr, interrupt output signal. Interrupt output is asserted if M2VMT_CR[RPUIE_EN] is ’1’ and ANY bit is set in the M2VMT_ESR register. Special Note: Not valid or has no effect on the interrupt when REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT=’1’. Reset State: x

SFPB_2X1_M2VMT_CR (cont.)

Bits	Name	Description
1	RPUERE	RPU error report enable: When set, M2VMT reports configuration port errors to the requesting bus master, according to the respective port's bus protocol. All error types reported via CRIF port will use a decode error, rather than a slave error. Regardless of the value of this field, both configuration port errors are terminated by the M2VMT as RAZ/WI, and are recorded in M2VMT_ESR register. Reset State: X
0	RPUE	RPU Enable: Governs whether M2VMT_RPU_ACR is enabled to check the VMID of the configuration request. When set, all configuration port accesses are checked against M2VMT_RPU_ACR register for access permissions. It's cleared by reset. Set once SROT configures MID->VMID mapping tables Reset State: 0

0x01801F84 SFPB_2X1_M2VMT_EAR

Type: Read
Clock: CC_SFPB_CLK
Reset State: unknown

When there is an error, this register holds the physical address of the errant transaction.

SFPB_2X1_M2VMT_EAR

Bits	Name	Description
31:0	PA	M2VMT Error Address Register: Physical address[31:0]. Contains the physical address of the errant request. Based on implementation, it may not contain the full 32 bits of the address. Captures the address on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. Special Note: When REMOVE_M2VMT_RPU='1' OR REMOVE_M2VMT_SYND_REG_IF_RPU_PRESENT = '1', this register is not available and therefore access to this register are treated as RAZ/WI.

0x01801F88 SFPB_2X1_M2VMT_ESR

Type: Read/Write to clear
Clock: CC_SFPB_CLK
Reset State: Undefined

M2VMT Error Status Register:

Captures the status upon M2VMT configuration errors, as determined by the M2VMT_RPU_ACR.

This register has read/write-clear access, meaning that reads simply provide a value in the register, while writes are performed by clearing those bits corresponding to ’1’s in the value written data, and leaving unchanged those bits corresponding to 0s n the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old error. A write with a ’1’ set in a bit field will result in clearing that bit. Writes with a 0 have no effect.

The presence of an asserted value on any bit in this register is what prompts the assertion when enabled by M2VMT_CR[RPUEIE] of the M2MVT’s interrupt output. Therefore these bits must be cleared by the interrupt handler. This is contrasted with the fields in the M2VMT_ESYNRn register, which are merely the ’syndrome’ of an error indicated by the M2VMT_ESR.

For M2VMT, there is only one defined error status bit in the M2VMT_SER (actually two, if you count multi-error).

SFPB_2X1_M2VMT_ESR

Bits	Name	Description
31	MULTI	Multi-Error: When set to ’1’, indicates that an additional error occurred while M2VMT_ESR is non-zero. The M2VMT_EAR,M2VMT_ESYNRn and M2VMT_ESR registers (with the exception of this bit) lock on the first error, and must be cleared to unlock. Therefore, the status and the syndrome of errors that occurred while M2VMT_ESR[CFG] is ’1’ are lost, i.e., syndrome register and status register stores only details of the first error. **NOTE** When REMOVE_M2VMT_RPU=’1’ OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT=’1’, this register is not available and therefore access to this register is treated as RAZ/WI.
30:1	RESERVED	
0	CFG	Configuration Port Error: When set to ’1’, indicates an error associated with a configuration port request.

0x01801F8C SFPB_2X1_M2VMT_ESRRESTORE

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: unknown

SFPB_2X1_M2VMT_ESRRESTORE

Bits	Name	Description
31:0	M2VMT_ESRRTORE	M2VMT Error Status Register Restore This is just an aliased address for M2VMT_ESR, which provides direct write access (rather than write-clear) for restoration purpose **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this register is treated as RAZ/WI.

0x01801F90 SFPB_2X1_M2VMT_ESYNR0

Type: Read
Clock: CC_SFPB_CLK
Reset State: undefined

Error Syndrome Register 0:

Captures the syndrome on M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) 'lock' upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., the syndrome register and the status register stores details of only the first error.

SFPB_2X1_M2VMT_ESYNR0

Bits	Name	Description
31:24	ATID	ATID[7:0] field of errant request. **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT="1", this register is not available and therefore access to this register is treated as RAZ/WI.
23:21	RESERVED	
20:16	AVMID	AVMID[4:0] field of errant request.
15:0	AMID	AMID[15:0] field of errant request.

0x01801F94 SFPB_2X1_M2VMT_ESYNR1

Type: Read
Clock: CC_SFPB_CLK
Reset State: Undefined

Error Syndrome Register 1:

Captures syndrome upon M2VMT configuration errors as determined by the M2VMT_RPU_ACR. M2VMT_ESYNRn registers and M2VMT_ESR itself (except for the MULTI bit) 'lock' upon first error. M2VMT_ESR must be cleared to unlock. Therefore, the status and syndrome of errors that occurred while M2VMT_ESR[CFG] is '1' are lost, i.e., the syndrome register and the status register stores details of only the first error.

SFPB_2X1_M2VMT_ESYNR1

Bits	Name	Description
31	DCD	Decode: Indicates configuration port error due to invalid/ unrecognized/ unmapped/ un-implemented address (e.g., a reserved register address). Includes decode errors within the global address space. Also, note that decode error is never asserted for client port accesses. For APQ8064, all other bit values will be tied to zero except, bit [6]= APROTNS. **NOTE** When REMOVE_M2VMT_RPU='1' OR REMOVE_ M2VMT_SYND_REG_IF_RPU_PRESENT='1', this register is not available and therefore access to this registers is treated as RAZ/WI.
30	AC	Access control: Indicates configuration port error due to lack of permission, as specified by the access control registers
29:25	RESERVED	
24	AFULL	AFULL field of the errant request
23	AOOOWR	AOOOWR field of the errant request
22	AOOORD	AOOORD field of the errant request.
21:20	ALOCK	ALOCK[1:0] (ALOCK field of the errant request).
19	RESERVED_2	
18:16	ASIZE	ASIZE[2:0] field of the errant request).
15:12	ALEN	ALEN[3:0] field of the errant request.
11:10	ABURST	ABURST[1:0] field of the errant request.
9	RESERVED_1	
8	AWRITE	AWRITE field of the errant request.
7	AINST	AINST field of the errant request.
6	APROTNS	APROTNS field of the errant request.
5	APRIV	APRIV field of the errant request.
4	AINNERSHARED	AINNERSHARED field of the errant request.

SFPB_2X1_M2VMT_ESYNR1 (cont.)

Bits	Name	Description
3	ASHARED	ASHARED field of the errant request.
2:0	AMEMTYPE	AMEMTYPE[2:0] field of the errant request.

0x01801FF4 SFPB_2X1_M2VMT_REV

Type: Read
Clock: CC_SFPB_CLK
Reset State: 0x00000010

Reports the revision information for the M2VMT core and wrapper.

SFPB_2X1_M2VMT_REV

Bits	Name	Description
31:8	RESERVED	
7:4	MAJOR	Major variant field. APQ8064: MAJOR = 0001
3:0	MINOR	Minor variant field. MINOR = 0000.

0x01801FF8 SFPB_2X1_M2VMT_IDR

Type: Read
Clock: CC_SFPB_CLK
Reset State: Undefined

Reports the size of the M2VMT table. It is a read-only register.

SFPB_2X1_M2VMT_IDR

Bits	Name	Description
31:9	RESERVED	M2VMTSIZE=NUM_M2VMT_ENTRIES from the design generic/parameter.

SFPB_2X1_M2VMT_IDR (cont.)

Bits	Name	Description
8:0	M2VMTSIZE	.M2VMTSIZE[8:0] Indicates actual number of M2VMT entries. Minimum of 1 and maximum of 512 entries is the valid range. This value is the same as the bit width of the M2VMT index input (maximum value is 9). [8:0]=M2VMTSIZE=NUM_M2VMT_ENTRIES Allows for up to a 7-bit MID field, plus NS-prot. 1 bit of the MID field must be used by the System MMU itself for hardware page table walk. Must also take into account any use of R/W or other fields used to select mapping.

0x01801FFC SFPB_2X1_M2VMT_RPU_ACR

Type: Read/Write
Clock: CC_SFPB_CLK
Reset State: Undefined

Using the incoming VMID, this register controls access to the global register space.

SFPB_2X1_M2VMT_RPU_ACR

Bits	Name	Description
31:0	RWE	M2VMT local RPU Access control Register. Each bit position corresponds to a VMID. When set to ’1’, that VMID is granted VMID read/write access to the entire block of registers within the M2VMT’s 4KB global address space, including this register itself. In practice, this register designates the VMID(s) that can act as SROT (e.g., scorpion-secure) or pseudo SROT (e.g. RPM ARM11). Special Note: When REMOVE_M2VMT_RPU=’1’, this register is not available and therefore access to this register is treated as RAZ/WI.

20 Smart Peripheral Subsystem Registers

20.1 Overview

Table 20-1 Daytona_SPS Bases

Base Name	Parent	Address
SIC_DISTRIB0_REG0	SIC_BASE	0x120C0000
SPS_SIC_APU_RGn_ACR	SIC_APU_BASE	0x120C2000
INTCTL0_INT_SELECT_0	INTCTL0_BASE	0x12100000
SIC_MESS_TRIG_IRQ0	SIC_NON_SECURE_BASE	0x12100000
INTCTL1_INT_SELECT_0	INTCTL1_BASE	0x12100800
INTCTL2_INT_SELECT_0	INTCTL2_BASE	0x12101000
INTCTL3_INT_SELECT_0	INTCTL3_BASE	0x12101800
INTCTL4_INT_SELECT_0	INTCTL4_BASE	0x12102000
INTCTL5_INT_SELECT_0	INTCTL5_BASE	0x12102800
INTCTL6_INT_SELECT_0	INTCTL6_BASE	0x12103000
INTCTL7_INT_SELECT_0	INTCTL7_BASE	0x12103800
SDC2_MCI_POWER	SDC2_BASE	0x12140000
SDC2_DML_CONFIG	SDC2_DML_BASE	0x12140800
SDC2_BAM_CTRL	SDC2_BAM_BASE	0x12142000
SDC3_MCI_POWER	SDC3_BASE	0x12180000
SDC3_DML_CONFIG	SDC3_DML_BASE	0x12180800
SDC3_BAM_CTRL	SDC3_BAM_BASE	0x12182000
SDC4_MCI_POWER	SDC4_BASE	0x121C0000
SDC4_DML_CONFIG	SDC4_DML_BASE	0x121C0800
SDC4_BAM_CTRL	SDC4_BAM_BASE	0x121C2000
BAM_DMA_DMA_ENBL	BAM_DMA_BASE	0x12240000
BAM_DMA_BAM_CTRL	BAM_DMA_BAM_BASE	0x12244000
BAM_DMA_APU_RGn_ACR	BAM_DMA_BAM_XPU_BASE	0x12246000
SDC1_MCI_POWER	SDC1_BASE	0x12400000
SDC1_DML_CONFIG	SDC1_DML_BASE	0x12400800
SDC1_BAM_CTRL	SDC1_BAM_BASE	0x12402000

Table 20-1 Daytona_SPS Bases (cont.)

Base Name	Parent	Address
USB1_HS_USB_OTG_HS_ID	USB1_HS_BASE	0x12500000
USB1_HS_BAM_CTRL	USB1_HS_BAM_BASE	0x12502000
USB2_HSIC_USB_OTG_HS_ID	USB2_HSIC_BASE	0x12510000
USB3_HS_USB_OTG_HS_ID	USB3_HS_BASE	0x12520000
USB3_HS_BAM_CTRL	USB3_HS_BAM_BASE	0x12522000
USB4_HS_USB_OTG_HS_ID	USB4_HS_BASE	0x12530000
USB4_HS_BAM_CTRL	USB4_HS_BAM_BASE	0x12532000
SPS_GSBI1_GSBI_CTRL_REG	SPS_GSBI1_BASE	0x12440000
SPS_GSBI1_UART_DM_MR1	SPS_UART1_DM_BASE	0x12450000
SPS_GSBI1_QUP_CONFIG	SPS_QUP1_BASE	0x12460000
SPS_GSBI2_GSBI_CTRL_REG	SPS_GSBI2_BASE	0x12480000
SPS_GSBI2_UART_DM_MR1	SPS_UART2_DM_BASE	0x12490000
SPS_GSBI2_QUP_CONFIG	SPS_QUP2_BASE	0x124A0000
IRQSTATUSA	PPSS_BASE	0x12080000
XO_TMRn_MATCH_VAL	PPSS_BASE	0x12080000
A_PAUSE	PPSS_BASE	0x12080000
A_GPIO_n_DIR	PPSS_BASE	0x12080000

20.2 SPS SIC Secure Registers (0x120C0000 SIC_BASE)

This section contains the Smart Peripheral System registers for the secure domain.

Smart Peripheral System (SPS) Interrupt Controller (SIC) has two domains of registers. One is non secure domain, the other is secure domain.

0x120C0000 SIC_DISTRIB0_REG0

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 31 to 0. This is reserved for SIC Distributor 0

SIC_DISTRIB0_REG0

Bits	Name	Description
31:0	SIC_DISTRIB0_REG0	Enable bit for Interrupt [31:0].

0x120C0004 SIC_DISTRIB0_REG1

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 63 to 32. This is reserved for SIC Distributor 0

SIC_DISTRIB0_REG1

Bits	Name	Description
31:0	SIC_DISTRIB0_REG1	Enable bit for Interrupt [63:32].

0x120C0008 SIC_DISTRIB0_REG2

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 95 to 64. This is reserved for SIC Distributor 0

SIC_DISTRIB0_REG2

Bits	Name	Description
31:0	SIC_DISTRIB0_REG2	Enable bit for Interrupt [95:64].

0x120C000C SIC_DISTRIB0_REG3

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 127 to 96. This is reserved for SIC Distributor 0

SIC_DISTRIB0_REG3

Bits	Name	Description
31:0	SIC_DISTRIB0_REG3	Enable bit for Interrupt [127:96].

0x120C0080 SIC_VMID0

Type: Read /Write
Clock: CRIF_CLK
Reset State: 0x00000000

SIC Virtual Master ID Setup for Interrupt Controller 0.

SIC_VMID0

Bits	Name	Description
31:29	RESERVED_1	RESERVED
28	SIC_VMID0_EN	SIC VMID0 Compare Enable
27:5	RESERVED_2	RESERVED
4:0	SIC_VMID0	SIC VMID Setup for Interrupt Controller 0

0x120C0100 SIC_DISTRIB1_REG0

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 31 to 0. This is reserved for SIC Distributor 1

SIC_DISTRIB1_REG0

Bits	Name	Description
31:0	SIC_DISTRIB1_REG1	Enable bit for Interrupt [31:0].

0x120C0104 SIC_DISTRIB1_REG1

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 63 to 32. This is reserved for SIC Distributor 1

SIC_DISTRIB1_REG1

Bits	Name	Description
31:0	SIC_DISTRIB1_REG1	Enable bit for Interrupt [63:32].

0x120C0108 SIC_DISTRIB1_REG2

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 95 to 64. This is reserved for SIC Distributor 1

SIC_DISTRIB1_REG2

Bits	Name	Description
31:0	SIC_DISTRIB1_REG2	Enable bit for Interrupt [95:64].

0x120C010C SIC_DISTRIB1_REG3

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 127 to 96. This is reserved for SIC Distributor 1

SIC_DISTRIB1_REG3

Bits	Name	Description
31:0	SIC_DISTRIB1_REG3	Enable bit for Interrupt [127:96].

0x120C0180 SIC_VMID1

Type: Read /Write
Clock: CRIF_CLK
Reset State: 0x00000000

SIC VMID Setup for Interrupt Controller 1.

SIC_VMID1

Bits	Name	Description
31:29	RESERVED_1	RESERVED
28	SIC_VMID1_EN	SIC VMID 1 Compare Enable
27:5	RESERVED_2	RESERVED
4:0	SIC_VMID1	SIC VMID Setup for Interrupt Controller 1

0x120C0200 SIC_DISTRIB2_REG0

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 31 to 0. This is reserved for SIC Distributor 2

SIC_DISTRIB2_REG0

Bits	Name	Description
31:0	SIC_DISTRIB1_REG0	Enable bit for Interrupt [31:0].

0x120C0204 SIC_DISTRIB2_REG1

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 63 to 32. This is reserved for SIC Distributor 2

SIC_DISTRIB2_REG1

Bits	Name	Description
31:0	SIC_DISTRIB2_REG1	Enable bit for Interrupt [63:32].

0x120C0208 SIC_DISTRIB2_REG2

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 95 to 64. This is reserved for SIC Distributor 2

SIC_DISTRIB2_REG2

Bits	Name	Description
31:0	SIC_DISTRIB2_REG2	Enable bit for Interrupt [95:64].

0x120C020C SIC_DISTRIB2_REG3

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 127 to 96. This is reserved for SIC Distributor 2

SIC_DISTRIB2_REG3

Bits	Name	Description
31:0	SIC_DISTRIB2_REG3	Enable bit for Interrupt [127:96].

0x120C0280 SIC_VMID2

Type: Read /Write
Clock: CRIF_CLK
Reset State: 0x00000000

SIC VMID Setup for Interrupt Controller 2.

SIC_VMID2

Bits	Name	Description
31:29	RESERVED_1	RESERVED
28	SIC_VMID2_EN	SIC VMD 2 Compare Enable
27:5	RESERVED_2	RESERVED
4:0	SIC_VMID2	SIC VMID Setup for Interrupt Controller 2

0x120C0300 SIC_DISTRIB3_REG0

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 31 to 0. This is reserved for SIC Distributor 3

SIC_DISTRIB3_REG0

Bits	Name	Description
31:0	SIC_DISTRIB3_REG1	Enable bit for Interrupt [31:0].

0x120C0304 SIC_DISTRIB3_REG1

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 63 to 32. This is reserved for SIC Distributor 3

SIC_DISTRIB3_REG1

Bits	Name	Description
31:0	SIC_DISTRIB3_REG1	Enable bit for Interrupt [63:32].

0x120C0308 SIC_DISTRIB3_REG2

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 95 to 64. This is reserved for SIC Distributor 3

SIC_DISTRIB3_REG2

Bits	Name	Description
31:0	SIC_DISTRIB3_REG2	Enable bit for Interrupt [95:64].

0x120C030C SIC_DISTRIB3_REG3

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 127 to 96. This is reserved for SIC Distributor 3

SIC_DISTRIB3_REG3

Bits	Name	Description
31:0	SIC_DISTRIB3_REG3	Enable bit for Interrupt [127:96].

0x120C0380 SIC_VMID3

Type: Read /Write
Clock: CRIF_CLK
Reset State: 0x00000000

SIC VMID Setup for Interrupt Controller 3.

SIC_VMID3

Bits	Name	Description
31:29	RESERVED_1	RESERVED
28	SIC_VMID3_EN	SIC VMID 3 Compare Enable
27:5	RESERVED_2	RESERVED
4:0	SIC_VMID3	SIC VMID Setup for Interrupt Controller 3

0x120C0400 SIC_DISTRIB4_REG0

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 31 to 0. This is reserved for SIC Distributor 4

SIC_DISTRIB4_REG0

Bits	Name	Description
31:0	SIC_DISTRIB4_REG0	Enable bit for Interrupt [31:0].

0x120C0404 SIC_DISTRIB4_REG1

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 63 to 32. This is reserved for SIC Distributor 4

SIC_DISTRIB4_REG1

Bits	Name	Description
31:0	SIC_DISTRIB4_REG1	Enable bit for Interrupt [63:32].

0x120C0408 SIC_DISTRIB4_REG2

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 95 to 64. This is reserved for SIC Distributor 4

SIC_DISTRIB4_REG2

Bits	Name	Description
31:0	SIC_DISTRIB4_REG2	Enable bit for Interrupt [95:64].

0x120C040C SIC_DISTRIB4_REG3

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 127 to 96. This is reserved for SIC Distributor 4

SIC_DISTRIB4_REG3

Bits	Name	Description
31:0	SIC_DISTRIB4_REG3	Enable bit for Interrupt [127:96].

0x120C0480 SIC_VMID4

Type: Read /Write
Clock: CRIF_CLK
Reset State: 0x00000000

SIC VMID Setup for Interrupt Controller 4.

SIC_VMID4

Bits	Name	Description
31:29	RESERVED_1	RESERVED
28	SIC_VMID4_EN	SIC VMID 4 Compare Enable
27:5	RESERVED_2	RESERVED
4:0	SIC_VMID4	SIC VMID Setup for Interrupt Controller 4

0x120C0500 SIC_DISTRIB5_REG0

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 31 to 0. This is reserved for SIC Distributor 5

SIC_DISTRIB5_REG0

Bits	Name	Description
31:0	SIC_DISTRIB5_REG1	Enable bit for Interrupt [31:0].

0x120C0504 SIC_DISTRIB5_REG1

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 63 to 32. This is reserved for SIC Distributor 5

SIC_DISTRIB5_REG1

Bits	Name	Description
31:0	SIC_DISTRIB5_REG1	Enable bit for Interrupt [63:32].

0x120C0508 SIC_DISTRIB5_REG2

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 95 to 64. This is reserved for SIC Distributor 5

SIC_DISTRIB5_REG2

Bits	Name	Description
31:0	SIC_DISTRIB5_REG2	Enable bit for Interrupt [95:64].

0x120C050C SIC_DISTRIB5_REG3

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 127 to 96. This is reserved for SIC Distributor 5

SIC_DISTRIB5_REG3

Bits	Name	Description
31:0	SIC_DISTRIB5_REG3	Enable bit for Interrupt [127:96].

0x120C0580 SIC_VMID5

Type: Read /Write
Clock: CRIF_CLK
Reset State: 0x00000000

SIC VMID Setup for Interrupt Controller 5.

SIC_VMID5

Bits	Name	Description
31:29	RESERVED_1	RESERVED
28	SIC_VMID5_EN	SIC VMID 5 Compare Enable
27:5	RESERVED_2	RESERVED
4:0	SIC_VMID5	SIC VMID Setup for Interrupt Controller 5

0x120C0600 SIC_DISTRIB6_REG0

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 31 to 0. This is reserved for SIC Distributor 6

SIC_DISTRIB6_REG0

Bits	Name	Description
31:0	SIC_DISTRIB6_REG0	Enable bit for Interrupt [31:0].

0x120C0604 SIC_DISTRIB6_REG1

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 63 to 32. This is reserved for SIC Distributor 6

SIC_DISTRIB6_REG1

Bits	Name	Description
31:0	SIC_DISTRIB6_REG1	Enable bit for Interrupt [63:32].

0x120C0608 SIC_DISTRIB6_REG2

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 95 to 64. This is reserved for SIC Distributor 6

SIC_DISTRIB6_REG2

Bits	Name	Description
31:0	SIC_DISTRIB6_REG2	Enable bit for Interrupt [95:64].

0x120C060C SIC_DISTRIB6_REG3

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 127 to 96. This is reserved for SIC Distributor 6

SIC_DISTRIB6_REG3

Bits	Name	Description
31:0	SIC_DISTRIB6_REG3	Enable bit for Interrupt [127:96].

0x120C0680 SIC_VMID6

Type: Read /Write
Clock: CRIF_CLK
Reset State: 0x00000000

SIC VMID Setup for Interrupt Controller 6.

SIC_VMID6

Bits	Name	Description
31:29	RESERVED_1	RESERVED
28	SIC_VMID6_EN	SIC VMID 6 Compare Enable
27:5	RESERVED_2	RESERVED
4:0	SIC_VMID6	SIC VMID Setup for Interrupt Controller 6

0x120C0700 SIC_DISTRIB7_REG0

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 31 to 0. This is reserved for SIC Distributor 7

SIC_DISTRIB7_REG0

Bits	Name	Description
31:0	SIC_DISTRIB7_REG1	Enable bit for Interrupt [31:0].

0x120C0704 SIC_DISTRIB7_REG1

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 63 to 32. This is reserved for SIC Distributor 7

SIC_DISTRIB7_REG1

Bits	Name	Description
31:0	SIC_DISTRIB7_REG1	Enable bit for Interrupt [63:32].

0x120C0708 SIC_DISTRIB7_REG2

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 95 to 64. This is reserved for SIC Distributor 7

SIC_DISTRIB7_REG2

Bits	Name	Description
31:0	SIC_DISTRIB7_REG2	Enable bit for Interrupt [95:64].

0x120C070C SIC_DISTRIB7_REG3

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

Enabled bit for interrupt source 127 to 96. This is reserved for SIC Distributor 7

SIC_DISTRIB7_REG3

Bits	Name	Description
31:0	SIC_DISTRIB7_REG3	Enable bit for Interrupt [127:96].

0x120C0780 SIC_VMID7

Type: Read /Write
Clock: CRIF_CLK
Reset State: 0x00000000

SIC VMID Setup for Interrupt Controller 7.

SIC_VMID7

Bits	Name	Description
31:29	RESERVED_1	RESERVED Field
28	SIC_VMID7_EN	Enable MAster ID 7 compare
27:5	RESERVED_2	RESERVED Field
4:0	SIC_VMID7	SIC VMID Setup for Interrupt Controller 7

0x120C1100 SIC_ERROR_REG

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

SIC Error Register Setup.

SIC_ERROR_REG

Bits	Name	Description
31	SIC_CNTRL_VIOL_IRQ	SIC Controller Violation Interrupt
30:16	ADDR_VIOL	Address Which is Violated
15:0	MID_VIOL	Master ID Which is Violated

0x120C11F0 SIC_TEST_BUS_SEL

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0x00000000

SIC TEST BUS SELECT.

SIC_TEST_BUS_SEL

Bits	Name	Description
31:4	RESERVED	RESERVED

SIC_TEST_BUS_SEL (cont.)

Bits	Name	Description
3:0	SIC_TEST_BUS_SEL	Select from the following debug bus 0x0: select debug bus from interrupt controller 0 0x1: select debug bus from interrupt controller 1 0x2: select debug bus from interrupt controller 2 0x3: select debug bus from interrupt controller 3 0x4: select debug bus from interrupt controller 4 0x5: select debug bus from interrupt controller 5 0x6: select debug bus from interrupt controller 6 0x7: select debug bus from interrupt controller 7 0x8: select debug bus from _1 (regarding to IIFS0) 0x9: select debug bus from _2 (regarding to IIFS1) 0xA: select debug bus from _3 (regarding to IIFS2) 0xB: select debug bus from _4 (regarding to IIFS3) 0xC: select debug bus from _5 (regarding to IIFS4) 0xD: select debug bus from _6 (regarding to IIFS5) 0xE: select debug bus from _7 (regarding to IIFS6) 0xF: select debug bus from _8 (regarding to IIFS7)

0x120C1200 SIC_DIST_DEF_REG0

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0xffffffff

Default enabled bit for interrupt source 31 to 0.

SIC_DIST_DEF_REG0

Bits	Name	Description
31:0	SIC_DIST_DEF_REG0	Enable bit for Interrupt [31:0].

0x120C1204 SIC_DIST_DEF_REG1

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0xffffffff

Default enabled bit for interrupt source 63to 32.

SIC_DIST_DEF_REG1

Bits	Name	Description
31:0	SIC_DIST_DEF_REG1	Enable bit for Interrupt [63:32].

0x120C1208 SIC_DIST_DEF_REG2

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0xffffffff

EDefault enabled bit for interrupt source 95 to 64.

SIC_DIST_DEF_REG2

Bits	Name	Description
31:0	SIC_DIST_DEF_REG2	Enable bit for Interrupt [95:64].

0x120C120C SIC_DIST_DEF_REG3

Type: Read/Write
Clock: CRIF_CLK
Reset State: 0xffffffff

Default enabled bit for interrupt source 127 to 96.

SIC_DIST_DEF_REG3

Bits	Name	Description
31:0	SIC_DIST_DEF_REG3	Enable bit for Interrupt [127:96].

20.3 SPS SIC XPU Registers (0x120C2000 SIC_APU_BASE)

This section contains the Smart Peripheral System SIC XPU registers.

0x120C2000+ 4*n SPS_SIC_APU_RGn_ACR, n=[0..31]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 10, i.e, a multi-VMID full access vs. no access permission type APU. These registers include a single bit per VMID granting full access

SPS_SIC_APU_RGn_ACR

Bits	Name	Description
31:0	RWE	Read/Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the registers in the associated resource group.

0x120C2F80 SPS_SIC_APU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

SPS_SIC_APU_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set APU_ESR. APU_EAR and APU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set APU_ESR. APU_EAR and APU_ESYNR0 updated with address and syndrome of error.
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR

SPS_SIC_APU_CR (cont.)

Bits	Name	Description
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x120C2F84 SPS_SIC_APU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port.

SPS_SIC_APU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x120C2F88 SPS_SIC_APU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is

contrasted with the fields in the APU_ESYNRn registers, which are merely the "syndrome" of an error indicated by APU_ESR.

SPS_SIC_APU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x120C2F8C SPS_SIC_APU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

SPS_SIC_APU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x120C2F90 SPS_SIC_APU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

SPS_SIC_APU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x120C2F94 SPS_SIC_APU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

SPS_SIC_APU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved

SPS_SIC_APU_ESYNR1 (cont.)

Bits	Name	Description
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x120C2FF4 SPS_SIC_APU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

SPS_SIC_APU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x120C2FF8 SPS_SIC_APU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x0000141F

APU ID Register: Read-only register that defines various configuration attributes of the APU instance.

SPS_SIC_APU_IDR

Bits	Name	Description
31:29	RESERVED31_21	Reserved
28:24	MSB	Indicates most significant address bit number used to select a resource group
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.
9:8	RESERVED9_8	Reserved
7:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

0x120C2FFC SPS_SIC_APU_APU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

APU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the APU (including the APU_APU_ACR itself).

SPS_SIC_APU_APU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the APU's 4KB address region (including the APU_APU_ACR itself). For single VMID type APUs (APU_IDR[MV] = 0) the APU_APU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

20.4 Interrupt Controller 0 Registers (0x12100000 INTCTL0_BASE)

This section contains Interrupt Controller 0 registers.

20.4.1 Configuration registers

These registers are used to configure the Interrupt Controller

0x12100000 INTCTL0_INT_SELECT_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_0 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL0_INT_SELECT_0

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12100004 INTCTL0_INT_SELECT_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_1 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL0_INT_SELECT_1

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12100010 INTCTL0_INT_ENABLE_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_0 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor.

INTCTL0_INT_ENABLE_0

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12100014 INTCTL0_INT_ENABLE_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_1 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor

INTCTL0_INT_ENABLE_1

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12100020 INTCTL0_INT_ENABLE_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_0 register is used to clear (to 0) the bits of the INT_ENABLE_0 register.

INTCTL0_INT_ENABLE_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear.

0x12100024 INTCTL0_INT_ENABLE_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_1 register is used to clear (to 0) the bits of the INT_ENABLE_1 register.

INTCTL0_INT_ENABLE_CLEAR_1

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Clear.

0x12100030 INTCTL0_INT_ENABLE_SET_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_0 register is used to set (to 1) the bits of the INT_ENABLE_0 register.

INTCTL0_INT_ENABLE_SET_0

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Set.

0x12100034 INTCTL0_INT_ENABLE_SET_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_1 register is used to set (to 1) the bits of the INT_ENABLE_1 register.

INTCTL0_INT_ENABLE_SET_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Set.

0x12100040 INTCTL0_INT_TYPE_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL0_INT_TYPE_0

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12100044 INTCTL0_INT_TYPE_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL0_INT_TYPE_1

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12100050 INTCTL0_INT_POLARITY_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL0_INT_POLARITY_0

Bits	Name	Description
31:0	POL	0x1: neg 0x0: pos

0x12100054 INTCTL0_INT_POLARITY_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL0_INT_POLARITY_1

Bits	Name	Description
31:0	POL	0x1: neg 0x0: posl

0x12100060 INTCTL0_NO_PEND_VAL

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

The NO_PEND_VALUE indicates the 32-bit value returned when reading VEC_RD or PEND_RD when there is no available interrupt. The reset value is the traditional indicator of no pending interrupt. It is convenient to refer to this value as the NULL interrupt.

When using the Interrupt Controller in Vector Mode, it may be useful to set this register to a value where software can jump to perform common end of ISR handling.

INTCTL0_NO_PEND_VAL

Bits	Name	Description
31:0	NULL_VALUE	This value is returned when VEC_RD or PEND_RD when there is no available interrupt

0x12100064 INTCTL0_MASTER_ENABLE

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The MASTER_ENABLE register is the IRQ and FIQ master enable register. The two bits in this register can be used to block the IRQ and/or FIQ signals from reaching the processor. These enables are used to gate off the interrupt signals at IRQ_STATUS and FIQ_STATUS. This will cause irq_n and fiq_n de-asserted if they were previously asserted and stay de-asserted. Note that if a Vector Port transaction has started, it will complete with irq_n still held asserted by the Vector Port logic.

Writing this register has no affect on the INT_ENABLE register.

NOTE The RAW_STATUS register will hold interrupts that have been detected by the Interrupt Controller even if disabled by INT_ENABLE.

INTCTL0_MASTER_ENABLE

Bits	Name	Description
1	FIQ_ENABLE	0x0: Disable 0x1: Enable.
0	IRQ_ENABLE	0x0: Disable 0x1: Enable.

0x12100068 INTCTL0_VIC_CONFIG

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The VIC_CONFIG register is used to enable Vector Port interface.

INTCTL0_VIC_CONFIG

Bits	Name	Description
0	VECTOR_MODE	0x1: Enable 0x0: Disable

0x1210006C INTCTL0_SECURITY

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The SECURITY register is used to enable or disable non-secure bus transactions. The bus security status is signaled to the Interrupt Controller via the ns pin. When ns is set to 0 the state of the SECURITY register is not considered - a secure transaction is allowed if the device is set to non-secure mode. When ns is set to 1, the SECURITY register's SECURE bit must be 0 for access to be granted. If set to 1, the non-secure (ns) transaction is denied. When access is denied, a write is ignored, and a read will return 0x0. No error is signaled.

INTCTL0_SECURITY

Bits	Name	Description
0	SECURE	When enabled, only secure agents can access the registers. When disabled, both secure and non-secure agents can access the registers. 0x1: Enable 0x0: Disable

0x12100200+4*n INTCTL0_PRIORITYn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x0

The PRIORITYn registers are used to determine the priority for each interrupt source.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

NOTE Only IRQs are prioritized. Thus PRIORITYn registers have no affect on FIQ.

INTCTL0_PRIORITYn

Bits	Name	Description
2:0	PRIORITY	Priority for each interrupt source.

0x12100400+4*n INTCTL0_VECT_ADDRn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: NA

The VECT_ADDRn registers provide the vector handle address for each interrupt source N.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

INTCTL0_VECT_ADDRn

Bits	Name	Description
31:2	ADDR	Vector handle (the ISR's starting address) for interrupt source n

INTCTL0_VECT_ADDRn (cont.)

Bits	Name	Description
1:0	RESERVED_BITS1_0	

20.4.2 Operational registers

0x12100080 INTCTL0_IRQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_0 shows which interrupt sources zero to 31 designated for irq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_0.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL0_IRQ_STATUS_0

Bits	Name	Description
31	INT_SRC31	See bit 0's description.
30	INT_SRC30	
29	INT_SRC29	
28	INT_SRC28	
27	INT_SRC27	
26	INT_SRC26	
25	INT_SRC25	
24	INT_SRC24	
23	INT_SRC23	
22	INT_SRC22	
21	INT_SRC21	
20	INT_SRC20	
19	INT_SRC19	
18	INT_SRC18	
17	INT_SRC17	
16	INT_SRC16	
15	INT_SRC15	

INTCTL0_IRQ_STATUS_0 (cont.)

Bits	Name	Description
14	INT_SRC14	
13	INT_SRC13	
12	INT_SRC12	
11	INT_SRC11	
10	INT_SRC10	
9	INT_SRC9	
8	INT_SRC8	
7	INT_SRC7	
6	INT_SRC6	
5	INT_SRC5	
4	INT_SRC4	
3	INT_SRC3	
2	INT_SRC2	
1	INT_SRC1	
0	INT_SRC0	Data for interrupt source bit 0 0x1: active 0x0: inactive

0x12100084 INTCTL0_IRQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_1 shows which interrupt sources 32 to 63 designated for irq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_1.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL0_IRQ_STATUS_1

Bits	Name	Description
31	INT_SRC63	See bit 0's description
30	INT_SRC62	
29	INT_SRC61	

INTCTL0_IRQ_STATUS_1 (cont.)

Bits	Name	Description
28	INT_SRC60	
27	INT_SRC59	
26	INT_SRC58	
25	INT_SRC57	
24	INT_SRC56	
23	INT_SRC55	
22	INT_SRC54	
21	INT_SRC53	
20	INT_SRC52	
19	INT_SRC51	
18	INT_SRC50	
17	INT_SRC49	
16	INT_SRC48	
15	INT_SRC47	
14	INT_SRC46	
13	INT_SRC45	
12	INT_SRC44	
11	INT_SRC43	
10	INT_SRC42	
9	INT_SRC41	
8	INT_SRC40	
7	INT_SRC39	
6	INT_SRC38	
5	INT_SRC37	
4	INT_SRC36	
3	INT_SRC35	
2	INT_SRC34	
1	INT_SRC33	
0	INT_SRC32	Data for interrupt source bit 32 0x1: active 0x0: inactive

0x12100090 INTCTL0_FIQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_0 shows which interrupt sources zero to 31 designated for fiq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_0.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL0_FIQ_STATUS_0

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_0 fields

0x12100094 INTCTL0_FIQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_1 shows which interrupt sources 32 to 63 designated for fiq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_1.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL0_FIQ_STATUS_1

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_1 fields

0x121000A0 INTCTL0_RAW_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_0 shows which interrupt sources zero to 31 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_0. Bits set in RAW_STATUS_0 are steered to generate irq_n or fiq_n by INT_SELECT_0 if enabled by both INT_ENABLE_0 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_0 by writing SOFT_INT_0.

INTCTL0_RAW_STATUS_0

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_0

0x121000A4 INTCTL0_RAW_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_1 shows which interrupt sources 32 to 63 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_1. Bits set in RAW_STATUS_1 are steered to generate irq_n or fiq_n by INT_SELECT_1 if enabled by both INT_ENABLE _1 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_1 by writing SOFT_INT_1.

INTCTL0_RAW_STATUS_1

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_1

0x121000B0 INTCTL0_INT_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_0 is used to clear bits in RAW_STATUS_0. For any bit written 0x1 to INT_CLEAR_0, the corresponding bit position is cleared in RAW_STATUS_0.

INTCTL0_INT_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121000B4 INTCTL0_INT_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_1 is used to clear bits in RAW_STATUS_1. For any bit written 0x1 to INT_CLEAR_1, the corresponding bit position is cleared in RAW_STATUS_1.

INTCTL0_INT_CLEAR_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121000C0 INTCTL0_SOFT_INT_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_0 is used to set bits in RAW_STATUS_0 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_0, the corresponding bit position is set in RAW_STATUS_0.

INTCTL0_SOFT_INT_0

Bits	Name	Description
31:0	SW_INT	0x0: Do nothing 0x1: Set

0x121000C4 INTCTL0_SOFT_INT_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_1 is used to set bits in RAW_STATUS_1 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_1, the corresponding bit position is set in RAW_STATUS_1.

INTCTL0_SOFT_INT_1

Bits	Name	Description
31:0	SW_INT	See IRQ_STATUS_1 for bit map. 0x0: Do nothing 0x1: Set

0x121000D0 INTCTL0_VEC_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack PUSH in the PIC, and if an interrupt is causing irq_n returns it.

Assuming an interrupt is available and irq_n is asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU has seen irq_n.
- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine.
- The PIC will set a bit in IN_STACK for the sw level that has been interrupted (including "main").
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that caused the irq_n.
- Subsequently irq_n may only be asserted for an interrupt source designated at a higher priority level than the highest priority level indicated by IN_SERVICE.

If irq_n is asserted, the value returned when reading VEC_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If irq_n is not asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When the Interrupt Controller is in Vector Mode, as designated by VIC_CONFIG, VEC_RD should not be read. The controller still needs to be informed that the CPU is taking the interrupt. This is done by a Vector Port transaction. However, if VEC_RD is read in while in Vector Mode, the read will have the same effect as in PIC mode. However, the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE Using this register while the system is in Vector Mode may not be reliable as CPU hardware may initiate a Vector Port transaction while launching the read transaction to VEC_RD. This race condition could have undesirable results.

INTCTL0_VEC_RD

Bits	Name	Description
31:0	INDEX	Reading from this register provides the index of the current interrupt selected by the PIC, and indicates to the priority hardware that the interrupt is being serviced. Though the practice is not recommended, if this register is read in Vector Mode, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to VEC_RD. The commanded PUSH is performed. If irq_n is not currently active, reading this register returns the value stored in NO_PEND_VAL. There are no side effects in this case - the commanded PUSH is not performed.

0x121000D4 INTCTL0_PEND_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack POP in the PIC, and if an interrupt is pending returns it.

Assuming an interrupt is available and irq_n is not asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine, and ending the previous ISR routine.
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that is now starting.
- The PIC will clear the most significant bit found set in IN_SERVICE for the priority of the interrupt ISR routine just ended if the priority of the interrupt now starting is different.

If an interrupt is available and irq_n is asserted or if no interrupt is available the PIC will behave as if the VEC_WR command register was written. That is, the command issued to the PIC will be interpreted as a POP.

The value returned when reading PEND_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If no interrupt is asserted or if irq_n is asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When Vector Mode is enabled, unlike the VEC_RD register, PEND_RD must be read in order to inform the PIC that the ISR has finished processing. There is no equivalent

Vector Port transaction. When not in Vector Mode, the interrupts index (bit position) is returned.

NOTE In Vector Mode the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE VEC_WR can be substituted for PEND_RD to inform the PIC that the ISR has finished processing without returning a pending interrupt.

INTCTL0_PEND_RD

Bits	Name	Description
31:0	HANDLE	Reading from this register provides the index of the current interrupt selected by the PIC as a pending interrupt. It also indicates to the priority hardware that the current ISR is finished, and if an interrupt is pending that a new ISR is starting. In Vector Mode, when an interrupt is pending, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to PEND_RD. The commanded POP is performed. If an interrupt is not pending, reading this register returns the value stored in NO_PEND_VAL. The commanded POP is still performed.

0x121000D8 INTCTL0_VEC_WR

Type: Write (command)
Clock: INT_CTL_CLK
Reset State: NA

This is a write command register. It affects a logical stack POP in the PIC without returning any (possibly) pending interrupt. The resulting state of the PIC is to request a new irq_n if any bits are set in IRQ_STATUS.

Writing this register has the following side effects:

- Informs the PIC logic that the CPU is ending the current ISR routine.
- The PIC will clear the most significant bit found set in IN_SERVICE.
- The PIC will clear the most significant bit found set in IN_STACK.

NOTE PEND_RD can be substituted for VEC_WR to inform the PIC that the ISR has finished processing and to return a pending interrupt at the same time.

INTCTL0_VEC_WR

Bits	Name	Description
31:0	RESERVED	Data written is not used.

20.4.3 Debug and legacy registers

0x121000E0 INTCTL0_IN_SERVICE

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_SERVICE register provides the Interrupt Controller's state information regarding which ISR priority levels are currently in service by the processor. This is provided for debug purposes only.

INTCTL0_IN_SERVICE

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL7	0x1: In service 0x0: Not in service
6	LEVEL6	0x1: In service 0x0: Not in service
5	LEVEL5	0x1: In service 0x0: Not in service
4	LEVEL4	0x1: In service 0x0: Not in service
3	LEVEL3	0x1: In service 0x0: Not in service
2	LEVEL2	0x1: In service 0x0: Not in service
1	LEVEL1	0x1: In service 0x0: Not in service
0	LEVEL0	0x1: In service 0x0: Not in service

0x121000E4 INTCTL0_IN_STACK

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_STACK register provides the Interrupt Controller's state information regarding which ISR priority levels are currently nested (stacked) in the CPU. This is provided for debug purposes only.

INTCTL0_IN_STACK

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL6	0x1: Nested 0x0: Not nested
6	LEVEL5	0x1: Nested 0x0: Not nested
5	LEVEL4	0x1: Nested 0x0: Not nested
4	LEVEL3	0x1: Nested 0x0: Not nested
3	LEVEL2	0x1: Nested 0x0: Not nested
2	LEVEL1	0x1: Nested 0x0: Not nested
1	LEVEL0	0x1: Nested 0x0: Not nested
0	MAIN	0x1: Nested 0x0: Not nested

0x121000E8 INTCTL0_TEST_BUS_SEL

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

Select signals to be directed to Interrupt Controller test_bus 32-bit output port.

INTCTL0_TEST_BUS_SEL

Bits	Name	Description
31:2	RESERVED	
1:0	SEL	NOTE The Interrupt Controller may have as few as 33 interrupts. Setting to HIGH_INTS will not have meaning if there are less than 61 interrupt inputs. 0x0: NONE (output 0x0) 0x1: LOW_INTS (31 - IRQn, 30 - FIQn, intsource[29:0]) 0x2: MID_INTS (31 - IRQn, 30 - FIQn, pad 0 as needed, intsource[N up to 59:30]) 0x3: HIGH_INTS (31 - IRQn, 30 - FIQn, 28 bits 0, intsource[63:60])

0x121000EC INTCTL0_INT_CTL_CONFIG

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

The INT_CTL_CONFIG register provides additional configuration options for the interrupt controller used for debug purposes.

INTCTL0_INT_CTL_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_1	
0	NO_NESTING_MODE	Default : 0 This register bit is used to configure the interrupt controller before any interrupts occur. When this bit is cleared (0), the PIC priority logic is used to determine when to assert irq_n. When the software allows hardware interrupt nesting, this bit should be cleared (0). If this bit is set (1), irq_n is asserted whenever there is at least one bit set in IRQ_STATUS. This bit should be set (1) right after power up if the software does not need any hardware nesting functions. 0x0: NESTED 0x1: NOT NESTED

20.5 SPS SIC Non-Secure Registers (0x12100000 SIC_NON_SECURE_BASE)

This section contains the Smart Peripheral System registers for the non-secure domain.

Smart Peripheral System (SPS) Interrupt Controller (SIC) has two domains of registers. One is non secure domain, the other is secure domain..

Addresses are offset from zero. When constants are exported, they are re-assigned to the appropriate base address.

Only word accesses are supported by the SIC. Byte and half-word accesses are not supported.

20.5.1 BSIC Non Secure Registers

0x12104000 SIC_MESS_TRIG_IRQ0

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 0

SIC_MESS_TRIG_IRQ0

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104004 SIC_MESS_TRIG_IRQ1

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 1

SIC_MESS_TRIG_IRQ1

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104008 SIC_MESS_TRIG_IRQ2

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 2

SIC_MESS_TRIG_IRQ2

Bits	Name	Description
31:0	RESERVED	RESERVED

0x1210400C SIC_MESS_TRIG_IRQ3

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 3

SIC_MESS_TRIG_IRQ3

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104010 SIC_MESS_TRIG_IRQ4

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 4

SIC_MESS_TRIG_IRQ4

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104014 SIC_MESS_TRIG_IRQ5

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 5

SIC_MESS_TRIG_IRQ5

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104018 SIC_MESS_TRIG_IRQ6

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 6

SIC_MESS_TRIG_IRQ6

Bits	Name	Description
31:0	RESERVED	RESERVED

0x1210401C SIC_MESS_TRIG_IRQ7

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 7

SIC_MESS_TRIG_IRQ7

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104020 SIC_MESS_TRIG_IRQ8

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 8

SIC_MESS_TRIG_IRQ8

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104024 SIC_MESS_TRIG_IRQ9

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 9

SIC_MESS_TRIG_IRQ9

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104028 SIC_MESS_TRIG_IRQ10

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 10

SIC_MESS_TRIG_IRQ10

Bits	Name	Description
31:0	RESERVED	RESERVED

0x1210402C SIC_MESS_TRIG_IRQ11

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 11

SIC_MESS_TRIG_IRQ11

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104030 SIC_MESS_TRIG_IRQ12

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 12

SIC_MESS_TRIG_IRQ12

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104034 SIC_MESS_TRIG_IRQ13

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 13

SIC_MESS_TRIG_IRQ13

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104038 SIC_MESS_TRIG_IRQ14

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 14

SIC_MESS_TRIG_IRQ14

Bits	Name	Description
31:0	RESERVED	RESERVED

0x1210403C SIC_MESS_TRIG_IRQ15

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 15

SIC_MESS_TRIG_IRQ15

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104040 SIC_MESS_TRIG_IRQ16

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 16

SIC_MESS_TRIG_IRQ16

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104044 SIC_MESS_TRIG_IRQ17

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 17

SIC_MESS_TRIG_IRQ17

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104048 SIC_MESS_TRIG_IRQ18

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 18

SIC_MESS_TRIG_IRQ18

Bits	Name	Description
31:0	RESERVED	RESERVED

0x1210404C SIC_MESS_TRIG_IRQ19

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 19

SIC_MESS_TRIG_IRQ19

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104050 SIC_MESS_TRIG_IRQ20

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 20

SIC_MESS_TRIG_IRQ20

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104054 SIC_MESS_TRIG_IRQ21

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 21

SIC_MESS_TRIG_IRQ21

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104058 SIC_MESS_TRIG_IRQ22

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 22

SIC_MESS_TRIG_IRQ22

Bits	Name	Description
31:0	RESERVED	RESERVED

0x1210405C SIC_MESS_TRIG_IRQ23

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 23/

SIC_MESS_TRIG_IRQ23

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104060 SIC_MESS_TRIG_IRQ24

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 24

SIC_MESS_TRIG_IRQ24

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104064 SIC_MESS_TRIG_IRQ25

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 25

SIC_MESS_TRIG_IRQ25

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104068 SIC_MESS_TRIG_IRQ26

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 26

SIC_MESS_TRIG_IRQ26

Bits	Name	Description
31:0	RESERVED	RESERVED

0x1210406C SIC_MESS_TRIG_IRQ27

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 27

SIC_MESS_TRIG_IRQ27

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104070 SIC_MESS_TRIG_IRQ28

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 28

SIC_MESS_TRIG_IRQ28

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104074 SIC_MESS_TRIG_IRQ29

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 29

SIC_MESS_TRIG_IRQ29

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104078 SIC_MESS_TRIG_IRQ30

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 30

SIC_MESS_TRIG_IRQ30

Bits	Name	Description
31:0	RESERVED	RESERVED

0x1210407C SIC_MESS_TRIG_IRQ31

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 31

SIC_MESS_TRIG_IRQ31

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104080 SIC_MESS_TRIG_IRQ32

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 32

SIC_MESS_TRIG_IRQ32

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104084 SIC_MESS_TRIG_IRQ33

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 33

SIC_MESS_TRIG_IRQ33

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104088 SIC_MESS_TRIG_IRQ34

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 34

SIC_MESS_TRIG_IRQ34

Bits	Name	Description
31:0	RESERVED	RESERVED

0x1210408C SIC_MESS_TRIG_IRQ35

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 35

SIC_MESS_TRIG_IRQ35

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104090 SIC_MESS_TRIG_IRQ36

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 36

SIC_MESS_TRIG_IRQ36

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104094 SIC_MESS_TRIG_IRQ37

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 37

SIC_MESS_TRIG_IRQ37

Bits	Name	Description
31:0	RESERVED	RESERVED

0x12104098 SIC_MESS_TRIG_IRQ38

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 38

SIC_MESS_TRIG_IRQ38

Bits	Name	Description
31:0	RESERVED	RESERVED

0x1210409C SIC_MESS_TRIG_IRQ39

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 39

SIC_MESS_TRIG_IRQ39

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040A0 SIC_MESS_TRIG_IRQ40

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 40

SIC_MESS_TRIG_IRQ40

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040A4 SIC_MESS_TRIG_IRQ41

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 41

SIC_MESS_TRIG_IRQ41

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040A8 SIC_MESS_TRIG_IRQ42

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 42

SIC_MESS_TRIG_IRQ42

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040AC SIC_MESS_TRIG_IRQ43

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 19

SIC_MESS_TRIG_IRQ43

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040B0 SIC_MESS_TRIG_IRQ44

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 44

SIC_MESS_TRIG_IRQ44

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040B4 SIC_MESS_TRIG_IRQ45

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 45

SIC_MESS_TRIG_IRQ45

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040B8 SIC_MESS_TRIG_IRQ46

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 46

SIC_MESS_TRIG_IRQ46

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040BC SIC_MESS_TRIG_IRQ47

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 47

SIC_MESS_TRIG_IRQ47

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040C0 SIC_MESS_TRIG_IRQ48

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 48

SIC_MESS_TRIG_IRQ48

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040C4 SIC_MESS_TRIG_IRQ49

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 49

SIC_MESS_TRIG_IRQ49

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040C8 SIC_MESS_TRIG_IRQ50

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 50

SIC_MESS_TRIG_IRQ50

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040CC SIC_MESS_TRIG_IRQ51

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 51

SIC_MESS_TRIG_IRQ51

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040D0 SIC_MESS_TRIG_IRQ52

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 52

SIC_MESS_TRIG_IRQ52

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040D4 SIC_MESS_TRIG_IRQ53

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 53

SIC_MESS_TRIG_IRQ53

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040D8 SIC_MESS_TRIG_IRQ54

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 54

SIC_MESS_TRIG_IRQ54

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040DC SIC_MESS_TRIG_IRQ55

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 55

SIC_MESS_TRIG_IRQ55

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040E0 SIC_MESS_TRIG_IRQ56

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 56

SIC_MESS_TRIG_IRQ56

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040E4 SIC_MESS_TRIG_IRQ57

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 57

SIC_MESS_TRIG_IRQ57

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040E8 SIC_MESS_TRIG_IRQ58

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 58

SIC_MESS_TRIG_IRQ58

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040EC SIC_MESS_TRIG_IRQ59

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 59

SIC_MESS_TRIG_IRQ59

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040F0 SIC_MESS_TRIG_IRQ60

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 60

SIC_MESS_TRIG_IRQ60

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040F4 SIC_MESS_TRIG_IRQ61

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 61

SIC_MESS_TRIG_IRQ61

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040F8 SIC_MESS_TRIG_IRQ62

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 62

SIC_MESS_TRIG_IRQ62

Bits	Name	Description
31:0	RESERVED	RESERVED

0x121040FC SIC_MESS_TRIG_IRQ63

Type: Write Only
Clock: CRIF_CLK
Reset State: 0x00000000

Message Trigger Interrupt 63

SIC_MESS_TRIG_IRQ63

Bits	Name	Description
31:0	RESERVED	RESERVED

20.6 Interrupt Controller 1 Registers (0x12100800 INTCTL1_BASE)

This section contains Interrupt Controller 1 registers.

20.6.1 Configuration registers

These registers are used to configure the Interrupt Controller.

0x12100800 INTCTL1_INT_SELECT_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_0 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL1_INT_SELECT_0

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12100804 INTCTL1_INT_SELECT_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_1 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL1_INT_SELECT_1

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12100810 INTCTL1_INT_ENABLE_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_0 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor.

INTCTL1_INT_ENABLE_0

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12100814 INTCTL1_INT_ENABLE_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_1 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor

INTCTL1_INT_ENABLE_1

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12100820 INTCTL1_INT_ENABLE_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_0 register is used to clear (to 0) the bits of the INT_ENABLE_0 register.

INTCTL1_INT_ENABLE_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear.

0x12100824 INTCTL1_INT_ENABLE_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_1 register is used to clear (to 0) the bits of the INT_ENABLE_1 register.

INTCTL1_INT_ENABLE_CLEAR_1

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Clear.

0x12100830 INTCTL1_INT_ENABLE_SET_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_0 register is used to set (to 1) the bits of the INT_ENABLE_0 register.

INTCTL1_INT_ENABLE_SET_0

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Set.

0x12100834 INTCTL1_INT_ENABLE_SET_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_1 register is used to set (to 1) the bits of the INT_ENABLE_1 register.

INTCTL1_INT_ENABLE_SET_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Set.

0x12100840 INTCTL1_INT_TYPE_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL1_INT_TYPE_0

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12100844 INTCTL1_INT_TYPE_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL1_INT_TYPE_1

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12100850 INTCTL1_INT_POLARITY_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL1_INT_POLARITY_0

Bits	Name	Description
31:0	POL	0x1: neg 0x0: pos

0x12100854 INTCTL1_INT_POLARITY_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL1_INT_POLARITY_1

Bits	Name	Description
31:0	POL	0x1: neg 0x0: posl

0x12100860 INTCTL1_NO_PEND_VAL

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

The NO_PEND_VALUE indicates the 32-bit value returned when reading VEC_RD or PEND_RD when there is no available interrupt. The reset value is the traditional indicator of no pending interrupt. It is convenient to refer to this value as the NULL interrupt.

When using the Interrupt Controller in Vector Mode, it may be useful to set this register to a value where software can jump to perform common end of ISR handling.

INTCTL1_NO_PEND_VAL

Bits	Name	Description
31:0	NULL_VALUE	This value is returned when VEC_RD or PEND_RD when there is no available interrupt

0x12100864 INTCTL1_MASTER_ENABLE

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The MASTER_ENABLE register is the IRQ and FIQ master enable register. The two bits in this register can be used to block the IRQ and/or FIQ signals from reaching the processor. These enables are used to gate off the interrupt signals at IRQ_STATUS and FIQ_STATUS. This will cause irq_n and fiq_n de-asserted if they were previously asserted and stay de-asserted. Note that if a Vector Port transaction has started, it will complete with irq_n still held asserted by the Vector Port logic.

Writing this register has no affect on the INT_ENABLE register.

NOTE The RAW_STATUS register will hold interrupts that have been detected by the Interrupt Controller even if disabled by INT_ENABLE.

INTCTL1_MASTER_ENABLE

Bits	Name	Description
1	FIQ_ENABLE	0x0: Disable 0x1: Enable.
0	IRQ_ENABLE	0x0: Disable 0x1: Enable.

0x12100868 INTCTL1_VIC_CONFIG

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The VIC_CONFIG register is used to enable Vector Port interface.

INTCTL1_VIC_CONFIG

Bits	Name	Description
0	VECTOR_MODE	0x1: Enable 0x0: Disable

0x1210086C INTCTL1_SECURITY

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The SECURITY register is used to enable or disable non-secure bus transactions. The bus security status is signaled to the Interrupt Controller via the ns pin. When ns is set to 0 the state of the SECURITY register is not considered - a secure transaction is allowed if the device is set to non-secure mode. When ns is set to 1, the SECURITY register's SECURE bit must be 0 for access to be granted. If set to 1, the non-secure (ns) transaction is denied. When access is denied, a write is ignored, and a read will return 0x0. No error is signaled.

INTCTL1_SECURITY

Bits	Name	Description
0	SECURE	When enabled, only secure agents can access the registers. When disabled, both secure and non-secure agents can access the registers. 0x1: Enable 0x0: Disable

0x12100A00+ 4*n INTCTL1_PRIORITYn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x0

The PRIORITYn registers are used to determine the priority for each interrupt source.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

NOTE Only IRQs are prioritized. Thus PRIORITYn registers have no affect on FIQ.

INTCTL1_PRIORITYn

Bits	Name	Description
2:0	PRIORITY	Priority for each interrupt source.

0x12100C00+ 4*n INTCTL1_VECT_ADDRn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: NA

The VECT_ADDRn registers provide the vector handle address for each interrupt source N.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

INTCTL1_VECT_ADDRn

Bits	Name	Description
31:2	ADDR	Vector handle (the ISR's starting address) for interrupt source n

INTCTL1_VECT_ADDRn (cont.)

Bits	Name	Description
1:0	RESERVED_BITS1_0	

20.6.2 Operational registers

0x12100880 INTCTL1_IRQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_0 shows which interrupt sources zero to 31 designated for irq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_0.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL1_IRQ_STATUS_0

Bits	Name	Description
31	INT_SRC31	See bit 0's description.
30	INT_SRC30	
29	INT_SRC29	
28	INT_SRC28	
27	INT_SRC27	
26	INT_SRC26	
25	INT_SRC25	
24	INT_SRC24	
23	INT_SRC23	
22	INT_SRC22	
21	INT_SRC21	
20	INT_SRC20	
19	INT_SRC19	
18	INT_SRC18	
17	INT_SRC17	
16	INT_SRC16	
15	INT_SRC15	

INTCTL1_IRQ_STATUS_0 (cont.)

Bits	Name	Description
14	INT_SRC14	
13	INT_SRC13	
12	INT_SRC12	
11	INT_SRC11	
10	INT_SRC10	
9	INT_SRC9	
8	INT_SRC8	
7	INT_SRC7	
6	INT_SRC6	
5	INT_SRC5	
4	INT_SRC4	
3	INT_SRC3	
2	INT_SRC2	
1	INT_SRC1	
0	INT_SRC0	Data for interrupt source bit 0 0x1: active 0x0: inactive

0x12100884 INTCTL1_IRQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_1 shows which interrupt sources 32 to 63 designated for irq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_1.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL1_IRQ_STATUS_1

Bits	Name	Description
31	INT_SRC63	See bit 0's description
30	INT_SRC62	
29	INT_SRC61	

INTCTL1_IRQ_STATUS_1 (cont.)

Bits	Name	Description
28	INT_SRC60	
27	INT_SRC59	
26	INT_SRC58	
25	INT_SRC57	
24	INT_SRC56	
23	INT_SRC55	
22	INT_SRC54	
21	INT_SRC53	
20	INT_SRC52	
19	INT_SRC51	
18	INT_SRC50	
17	INT_SRC49	
16	INT_SRC48	
15	INT_SRC47	
14	INT_SRC46	
13	INT_SRC45	
12	INT_SRC44	
11	INT_SRC43	
10	INT_SRC42	
9	INT_SRC41	
8	INT_SRC40	
7	INT_SRC39	
6	INT_SRC38	
5	INT_SRC37	
4	INT_SRC36	
3	INT_SRC35	
2	INT_SRC34	
1	INT_SRC33	
0	INT_SRC32	Data for interrupt source bit 32 0x1: active 0x0: inactive

0x12100890 INTCTL1_FIQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_0 shows which interrupt sources zero to 31 designated for fiq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_0.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL1_FIQ_STATUS_0

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_0 fields

0x12100894 INTCTL1_FIQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_1 shows which interrupt sources 32 to 63 designated for fiq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_1.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL1_FIQ_STATUS_1

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_1 fields

0x121008A0 INTCTL1_RAW_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_0 shows which interrupt sources zero to 31 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_0. Bits set in RAW_STATUS_0 are steered to generate irq_n or fiq_n by INT_SELECT_0 if enabled by both INT_ENABLE_0 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_0 by writing SOFT_INT_0.

INTCTL1_RAW_STATUS_0

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_0

0x121008A4 INTCTL1_RAW_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_1 shows which interrupt sources 32 to 63 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_1. Bits set in RAW_STATUS_1 are steered to generate irq_n or fiq_n by INT_SELECT_1 if enabled by both INT_ENABLE _1 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_1 by writing SOFT_INT_1.

INTCTL1_RAW_STATUS_1

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_1

0x121008B0 INTCTL1_INT_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_0 is used to clear bits in RAW_STATUS_0. For any bit written 0x1 to INT_CLEAR_0, the corresponding bit position is cleared in RAW_STATUS_0.

INTCTL1_INT_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121008B4 INTCTL1_INT_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_1 is used to clear bits in RAW_STATUS_1. For any bit written 0x1 to INT_CLEAR_1, the corresponding bit position is cleared in RAW_STATUS_1.

INTCTL1_INT_CLEAR_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121008C0 INTCTL1_SOFT_INT_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_0 is used to set bits in RAW_STATUS_0 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_0, the corresponding bit position is set in RAW_STATUS_0.

INTCTL1_SOFT_INT_0

Bits	Name	Description
31:0	SW_INT	0x0: Do nothing 0x1: Set

0x121008C4 INTCTL1_SOFT_INT_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_1 is used to set bits in RAW_STATUS_1 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_1, the corresponding bit position is set in RAW_STATUS_1.

INTCTL1_SOFT_INT_1

Bits	Name	Description
31:0	SW_INT	See IRQ_STATUS_1 for bit map. 0x0: Do nothing 0x1: Set

0x121008D0 INTCTL1_VEC_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack PUSH in the PIC, and if an interrupt is causing irq_n returns it.

Assuming an interrupt is available and irq_n is asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU has seen irq_n.
- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine.
- The PIC will set a bit in IN_STACK for the sw level that has been interrupted (including "main").
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that caused the irq_n.
- Subsequently irq_n may only be asserted for an interrupt source designated at a higher priority level than the highest priority level indicated by IN_SERVICE.

If irq_n is asserted, the value returned when reading VEC_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If irq_n is not asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When the Interrupt Controller is in Vector Mode, as designated by VIC_CONFIG, VEC_RD should not be read. The controller still needs to be informed that the CPU is taking the interrupt. This is done by a Vector Port transaction. However, if VEC_RD is read in while in Vector Mode, the read will have the same effect as in PIC mode. However, the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE Using this register while the system is in Vector Mode may not be reliable as CPU hardware may initiate a Vector Port transaction while launching the read transaction to VEC_RD. This race condition could have undesirable results.

INTCTL1_VEC_RD

Bits	Name	Description
31:0	INDEX	Reading from this register provides the index of the current interrupt selected by the PIC, and indicates to the priority hardware that the interrupt is being serviced. Though the practice is not recommended, if this register is read in Vector Mode, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to VEC_RD. The commanded PUSH is performed. If irq_n is not currently active, reading this register returns the value stored in NO_PEND_VAL. There are no side effects in this case - the commanded PUSH is not performed.

0x121008D4 INTCTL1_PEND_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack POP in the PIC, and if an interrupt is pending returns it.

Assuming an interrupt is available and irq_n is not asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine, and ending the previous ISR routine.
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that is now starting.
- The PIC will clear the most significant bit found set in IN_SERVICE for the priority of the interrupt ISR routine just ended if the priority of the interrupt now starting is different.

If an interrupt is available and irq_n is asserted or if no interrupt is available, the PIC will behave as if the VEC_WR command register was written. That is, the command issued to the PIC will be interpreted as a POP.

The value returned when reading PEND_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If no interrupt is asserted or if irq_n is asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When Vector Mode is enabled, unlike the VEC_RD register, PEND_RD must be read in order to inform the PIC that the ISR has finished processing. There is no equivalent

Vector Port transaction. When not in Vector Mode, the interrupts index (bit position) is returned.

NOTE In Vector Mode the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE VEC_WR can be substituted for PEND_RD to inform the PIC that the ISR has finished processing without returning a pending interrupt.

INTCTL1_PEND_RD

Bits	Name	Description
31:0	HANDLE	Reading from this register provides the index of the current interrupt selected by the PIC as a pending interrupt. It also indicates to the priority hardware that the current ISR is finished, and if an interrupt is pending that a new ISR is starting. In Vector Mode, when an interrupt is pending, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to PEND_RD. The commanded POP is performed. If an interrupt is not pending, reading this register returns the value stored in NO_PEND_VAL. The commanded POP is still performed.

0x121008D8 INTCTL1_VEC_WR

Type: Write (command)
Clock: INT_CTL_CLK
Reset State: NA

This is a write command register. It affects a logical stack POP in the PIC without returning any (possibly) pending interrupt. The resulting state of the PIC is to request a new irq_n if any bits are set in IRQ_STATUS.

Writing this register has the following side effects:

- Informs the PIC logic that the CPU is ending the current ISR routine.
- The PIC will clear the most significant bit found set in IN_SERVICE.
- The PIC will clear the most significant bit found set in IN_STACK.

NOTE PEND_RD can be substituted for VEC_WR to inform the PIC that the ISR has finished processing and to return a pending interrupt at the same time.

INTCTL1_VEC_WR

Bits	Name	Description
31:0	RESERVED	Data written is not used.

20.6.3 Debug and legacy registers

0x121008E0 INTCTL1_IN_SERVICE

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_SERVICE register provides the Interrupt Controller's state information regarding which ISR priority levels are currently in service by the processor. This is provided for debug purposes only.

INTCTL1_IN_SERVICE

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL7	0x1: In service 0x0: Not in service
6	LEVEL6	0x1: In service 0x0: Not in service
5	LEVEL5	0x1: In service 0x0: Not in service
4	LEVEL4	0x1: In service 0x0: Not in service
3	LEVEL3	0x1: In service 0x0: Not in service
2	LEVEL2	0x1: In service 0x0: Not in service
1	LEVEL1	0x1: In service 0x0: Not in service
0	LEVEL0	0x1: In service 0x0: Not in service

0x121008E4 INTCTL1_IN_STACK

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_STACK register provides the Interrupt Controller's state information regarding which ISR priority levels are currently nested (stacked) in the CPU. This is provided for debug purposes only.

INTCTL1_IN_STACK

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL6	0x1: Nested 0x0: Not nested
6	LEVEL5	0x1: Nested 0x0: Not nested
5	LEVEL4	0x1: Nested 0x0: Not nested
4	LEVEL3	0x1: Nested 0x0: Not nested
3	LEVEL2	0x1: Nested 0x0: Not nested
2	LEVEL1	0x1: Nested 0x0: Not nested
1	LEVEL0	0x1: Nested 0x0: Not nested
0	MAIN	0x1: Nested 0x0: Not nested

0x121008E8 INTCTL1_TEST_BUS_SEL

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

Select signals to be directed to Interrupt Controller test_bus 32-bit output port.

INTCTL1_TEST_BUS_SEL

Bits	Name	Description
31:2	RESERVED	
1:0	SEL	NOTE The Interrupt Controller may have as few as 33 interrupts. Setting to HIGH_INTS will not have meaning if there are less than 61 interrupt inputs. 0x0: NONE (output 0x0) 0x1: LOW_INTS (31 - IRQn, 30 - FIQn, intsource[29:0]) 0x2: MID_INTS (31 - IRQn, 30 - FIQn, pad 0 as needed, intsource[N up to 59:30]) 0x3: HIGH_INTS (31 - IRQn, 30 - FIQn, 28 bits 0, intsource[63:60])

0x121008EC INTCTL1_INT_CTL_CONFIG

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

The INT_CTL_CONFIG register provides additional configuration options for the interrupt controller used for debug purposes.

INTCTL1_INT_CTL_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_1	
0	NO_NESTING_MODE	Default : 0 This register bit is used to configure the interrupt controller before any interrupts occur. When this bit is cleared (0), the PIC priority logic is used to determine when to assert irq_n. When the software allows hardware interrupt nesting, this bit should be cleared (0). If this bit is set (1), irq_n is asserted whenever there is at least one bit set in IRQ_STATUS. This bit should be set (1) right after power up if the software does not need any hardware nesting functions. 0x0: NESTED 0x1: NOT NESTED

20.7 Interrupt Controller 2 Registers (0x12101000 INTCTL2_BASE)

This section contains Interrupt Controller 2 registers.

20.7.1 Configuration registers

These registers are used to configure the Interrupt Controller

0x12101000 INTCTL2_INT_SELECT_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_0 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL2_INT_SELECT_0

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12101004 INTCTL2_INT_SELECT_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_1 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL2_INT_SELECT_1

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12101010 INTCTL2_INT_ENABLE_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_0 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor.

INTCTL2_INT_ENABLE_0

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12101014 INTCTL2_INT_ENABLE_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_1 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor

INTCTL2_INT_ENABLE_1

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12101020 INTCTL2_INT_ENABLE_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_0 register is used to clear (to 0) the bits of the INT_ENABLE_0 register.

INTCTL2_INT_ENABLE_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear.

0x12101024 INTCTL2_INT_ENABLE_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_1 register is used to clear (to 0) the bits of the INT_ENABLE_1 register.

INTCTL2_INT_ENABLE_CLEAR_1

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Clear.

0x12101030 INTCTL2_INT_ENABLE_SET_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_0 register is used to set (to 1) the bits of the INT_ENABLE_0 register.

INTCTL2_INT_ENABLE_SET_0

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Set.

0x12101034 INTCTL2_INT_ENABLE_SET_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_1 register is used to set (to 1) the bits of the INT_ENABLE_1 register.

INTCTL2_INT_ENABLE_SET_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Set.

0x12101040 INTCTL2_INT_TYPE_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL2_INT_TYPE_0

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12101044 INTCTL2_INT_TYPE_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL2_INT_TYPE_1

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12101050 INTCTL2_INT_POLARITY_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL2_INT_POLARITY_0

Bits	Name	Description
31:0	POL	0x1: neg 0x0: pos

0x12101054 INTCTL2_INT_POLARITY_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL2_INT_POLARITY_1

Bits	Name	Description
31:0	POL	0x1: neg 0x0: posl

0x12101060 INTCTL2_NO_PEND_VAL

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

The NO_PEND_VALUE indicates the 32-bit value returned when reading VEC_RD or PEND_RD when there is no available interrupt. The reset value is the traditional indicator of no pending interrupt. It is convenient to refer to this value as the NULL interrupt.

When using the Interrupt Controller in Vector Mode, it may be useful to set this register to a value where software can jump to perform common end of ISR handling.

INTCTL2_NO_PEND_VAL

Bits	Name	Description
31:0	NULL_VALUE	This value is returned when VEC_RD or PEND_RD when there is no available interrupt

0x12101064 INTCTL2_MASTER_ENABLE

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The MASTER_ENABLE register is the IRQ and FIQ master enable register. The two bits in this register can be used to block the IRQ and/or FIQ signals from reaching the processor. These enables are used to gate off the interrupt signals at IRQ_STATUS and FIQ_STATUS. This will cause irq_n and fiq_n de-asserted if they were previously asserted and stay de-asserted. Note that if a Vector Port transaction has started, it will complete with irq_n still held asserted by the Vector Port logic.

Writing this register has no affect on the INT_ENABLE register.

NOTE The RAW_STATUS register will hold interrupts that have been detected by the Interrupt Controller even if disabled by INT_ENABLE.

INTCTL2_MASTER_ENABLE

Bits	Name	Description
1	FIQ_ENABLE	0x0: Disable 0x1: Enable.
0	IRQ_ENABLE	0x0: Disable 0x1: Enable.

0x12101068 INTCTL2_VIC_CONFIG

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The VIC_CONFIG register is used to enable Vector Port interface.

INTCTL2_VIC_CONFIG

Bits	Name	Description
0	VECTOR_MODE	0x1: Enable 0x0: Disable

0x1210106C INTCTL2_SECURITY

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The SECURITY register is used to enable or disable non-secure bus transactions. The bus security status is signaled to the Interrupt Controller via the ns pin. When ns is set to 0 the state of the SECURITY register is not considered - a secure transaction is allowed if the device is set to non-secure mode. When ns is set to 1, the SECURITY register's SECURE bit must be 0 for access to be granted. If set to 1, the non-secure (ns) transaction is denied. When access is denied, a write is ignored, and a read will return 0x0. No error is signaled.

INTCTL2_SECURITY

Bits	Name	Description
0	SECURE	When enabled, only secure agents can access the registers. When disabled, both secure and non-secure agents can access the registers. 0x1: Enable 0x0: Disable

0x12101200+4*n INTCTL2_PRIORITYn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x0

The PRIORITYn registers are used to determine the priority for each interrupt source.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

NOTE Only IRQs are prioritized. Thus PRIORITYn registers have no affect on FIQ.

INTCTL2_PRIORITYn

Bits	Name	Description
2:0	PRIORITY	Priority for each interrupt source.

0x12101400+4*n INTCTL2_VECT_ADDRn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: NA

The VECT_ADDRn registers provide the vector handle address for each interrupt source N.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

INTCTL2_VECT_ADDRn

Bits	Name	Description
31:2	ADDR	Vector handle (the ISR's starting address) for interrupt source n

INTCTL2_VECT_ADDRn (cont.)

Bits	Name	Description
1:0	RESERVED_BITS1_0	

20.7.2 Operational registers

0x12101080 INTCTL2_IRQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_0 shows which interrupt sources zero to 31 designated for irq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_0.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL2_IRQ_STATUS_0

Bits	Name	Description
31	INT_SRC31	See bit 0's description.
30	INT_SRC30	
29	INT_SRC29	
28	INT_SRC28	
27	INT_SRC27	
26	INT_SRC26	
25	INT_SRC25	
24	INT_SRC24	
23	INT_SRC23	
22	INT_SRC22	
21	INT_SRC21	
20	INT_SRC20	
19	INT_SRC19	
18	INT_SRC18	
17	INT_SRC17	
16	INT_SRC16	
15	INT_SRC15	

INTCTL2_IRQ_STATUS_0 (cont.)

Bits	Name	Description
14	INT_SRC14	
13	INT_SRC13	
12	INT_SRC12	
11	INT_SRC11	
10	INT_SRC10	
9	INT_SRC9	
8	INT_SRC8	
7	INT_SRC7	
6	INT_SRC6	
5	INT_SRC5	
4	INT_SRC4	
3	INT_SRC3	
2	INT_SRC2	
1	INT_SRC1	
0	INT_SRC0	Data for interrupt source bit 0 0x1: active 0x0: inactive

0x12101084 INTCTL2_IRQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_1 shows which interrupt sources 32 to 63 designated for irq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_1.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL2_IRQ_STATUS_1

Bits	Name	Description
31	INT_SRC63	See bit 0's description
30	INT_SRC62	
29	INT_SRC61	

INTCTL2_IRQ_STATUS_1 (cont.)

Bits	Name	Description
28	INT_SRC60	
27	INT_SRC59	
26	INT_SRC58	
25	INT_SRC57	
24	INT_SRC56	
23	INT_SRC55	
22	INT_SRC54	
21	INT_SRC53	
20	INT_SRC52	
19	INT_SRC51	
18	INT_SRC50	
17	INT_SRC49	
16	INT_SRC48	
15	INT_SRC47	
14	INT_SRC46	
13	INT_SRC45	
12	INT_SRC44	
11	INT_SRC43	
10	INT_SRC42	
9	INT_SRC41	
8	INT_SRC40	
7	INT_SRC39	
6	INT_SRC38	
5	INT_SRC37	
4	INT_SRC36	
3	INT_SRC35	
2	INT_SRC34	
1	INT_SRC33	
0	INT_SRC32	Data for interrupt source bit 32 0x1: active 0x0: inactive

0x12101090 INTCTL2_FIQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_0 shows which interrupt sources zero to 31 designated for fiq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_0.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL2_FIQ_STATUS_0

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_0 fields

0x12101094 INTCTL2_FIQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_1 shows which interrupt sources 32 to 63 designated for fiq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_1.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL2_FIQ_STATUS_1

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_1 fields

0x121010A0 INTCTL2_RAW_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_0 shows which interrupt sources zero to 31 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_0. Bits set in RAW_STATUS_0 are steered to generate irq_n or fiq_n by INT_SELECT_0 if enabled by both INT_ENABLE_0 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_0 by writing SOFT_INT_0.

INTCTL2_RAW_STATUS_0

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_0

0x121010A4 INTCTL2_RAW_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_1 shows which interrupt sources 32 to 63 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_1. Bits set in RAW_STATUS_1 are steered to generate irq_n or fiq_n by INT_SELECT_1 if enabled by both INT_ENABLE _1 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_1 by writing SOFT_INT_1.

INTCTL2_RAW_STATUS_1

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_1

0x121010B0 INTCTL2_INT_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_0 is used to clear bits in RAW_STATUS_0. For any bit written 0x1 to INT_CLEAR_0, the corresponding bit position is cleared in RAW_STATUS_0.

INTCTL2_INT_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121010B4 INTCTL2_INT_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_1 is used to clear bits in RAW_STATUS_1. For any bit written 0x1 to INT_CLEAR_1, the corresponding bit position is cleared in RAW_STATUS_1.

INTCTL2_INT_CLEAR_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121010C0 INTCTL2_SOFT_INT_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_0 is used to set bits in RAW_STATUS_0 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_0, the corresponding bit position is set in RAW_STATUS_0.

INTCTL2_SOFT_INT_0

Bits	Name	Description
31:0	SW_INT	0x0: Do nothing 0x1: Set

0x121010C4 INTCTL2_SOFT_INT_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_1 is used to set bits in RAW_STATUS_1 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_1, the corresponding bit position is set in RAW_STATUS_1.

INTCTL2_SOFT_INT_1

Bits	Name	Description
31:0	SW_INT	See IRQ_STATUS_1 for bit map. 0x0: Do nothing 0x1: Set

0x121010D0 INTCTL2_VEC_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack PUSH in the PIC, and if an interrupt is causing irq_n returns it.

Assuming an interrupt is available and irq_n is asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU has seen irq_n.
- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine.
- The PIC will set a bit in IN_STACK for the sw level that has been interrupted (including "main").
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that caused the irq_n.
- Subsequently irq_n may only be asserted for an interrupt source designated at a higher priority level than the highest priority level indicated by IN_SERVICE.

If irq_n is asserted, the value returned when reading VEC_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If irq_n is not asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When the Interrupt Controller is in Vector Mode, as designated by VIC_CONFIG, VEC_RD should not be read. The controller still needs to be informed that the CPU is taking the interrupt. This is done by a Vector Port transaction. However, if VEC_RD is read in while in Vector Mode, the read will have the same effect as in PIC mode. However, the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE Using this register while the system is in Vector Mode may not be reliable as CPU hardware may initiate a Vector Port transaction while launching the read transaction to VEC_RD. This race condition could have undesirable results.

INTCTL2_VEC_RD

Bits	Name	Description
31:0	INDEX	Reading from this register provides the index of the current interrupt selected by the PIC, and indicates to the priority hardware that the interrupt is being serviced. Though the practice is not recommended, if this register is read in Vector Mode, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to VEC_RD. The commanded PUSH is performed. If irq_n is not currently active, reading this register returns the value stored in NO_PEND_VAL. There are no side effects in this case - the commanded PUSH is not performed.

0x121010D4 INTCTL2_PEND_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack POP in the PIC, and if an interrupt is pending returns it.

Assuming an interrupt is available and irq_n is not asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine, and ending the previous ISR routine.
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that is now starting.
- The PIC will clear the most significant bit found set in IN_SERVICE for the priority of the interrupt ISR routine just ended if the priority of the interrupt now starting is different.

If an interrupt is available and irq_n is asserted or if no interrupt is available the PIC will behave as if the VEC_WR command register was written. That is, the command issued to the PIC will be interpreted as a POP.

The value returned when reading PEND_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If no interrupt is asserted or if irq_n is asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When Vector Mode is enabled, unlike the VEC_RD register, PEND_RD must be read in order to inform the PIC that the ISR has finished processing. There is no equivalent

Vector Port transaction. When not in Vector Mode, the interrupts index (bit position) is returned.

NOTE In Vector Mode the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE VEC_WR can be substituted for PEND_RD to inform the PIC that the ISR has finished processing without returning a pending interrupt.

INTCTL2_PEND_RD

Bits	Name	Description
31:0	HANDLE	Reading from this register provides the index of the current interrupt selected by the PIC as a pending interrupt. It also indicates to the priority hardware that the current ISR is finished, and if an interrupt is pending that a new ISR is starting. In Vector Mode, when an interrupt is pending, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to PEND_RD. The commanded POP is performed. If an interrupt is not pending, reading this register returns the value stored in NO_PEND_VAL. The commanded POP is still performed.

0x121010D8 INTCTL2_VEC_WR

Type: Write (command)
Clock: INT_CTL_CLK
Reset State: NA

This is a write command register. It affects a logical stack POP in the PIC without returning any (possibly) pending interrupt. The resulting state of the PIC is to request a new irq_n if any bits are set in IRQ_STATUS.

Writing this register has the following side effects:

- Informs the PIC logic that the CPU is ending the current ISR routine.
- The PIC will clear the most significant bit found set in IN_SERVICE.
- The PIC will clear the most significant bit found set in IN_STACK.

NOTE PEND_RD can be substituted for VEC_WR to inform the PIC that the ISR has finished processing and to return a pending interrupt at the same time.

INTCTL2_VEC_WR

Bits	Name	Description
31:0	RESERVED	Data written is not used.

20.7.3 Debug and legacy registers

0x121010E0 INTCTL2_IN_SERVICE

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_SERVICE register provides the Interrupt Controller's state information regarding which ISR priority levels are currently in service by the processor. This is provided for debug purposes only.

INTCTL2_IN_SERVICE

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL7	0x1: In service 0x0: Not in service
6	LEVEL6	0x1: In service 0x0: Not in service
5	LEVEL5	0x1: In service 0x0: Not in service
4	LEVEL4	0x1: In service 0x0: Not in service
3	LEVEL3	0x1: In service 0x0: Not in service
2	LEVEL2	0x1: In service 0x0: Not in service
1	LEVEL1	0x1: In service 0x0: Not in service
0	LEVEL0	0x1: In service 0x0: Not in service

0x121010E4 INTCTL2_IN_STACK

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_STACK register provides the Interrupt Controller's state information regarding which ISR priority levels are currently nested (stacked) in the CPU. This is provided for debug purposes only.

INTCTL2_IN_STACK

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL6	0x1: Nested 0x0: Not nested
6	LEVEL5	0x1: Nested 0x0: Not nested
5	LEVEL4	0x1: Nested 0x0: Not nested
4	LEVEL3	0x1: Nested 0x0: Not nested
3	LEVEL2	0x1: Nested 0x0: Not nested
2	LEVEL1	0x1: Nested 0x0: Not nested
1	LEVEL0	0x1: Nested 0x0: Not nested
0	MAIN	0x1: Nested 0x0: Not nested

0x121010E8 INTCTL2_TEST_BUS_SEL

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

Select signals to be directed to Interrupt Controller test_bus 32-bit output port.

INTCTL2_TEST_BUS_SEL

Bits	Name	Description
31:2	RESERVED	
1:0	SEL	NOTE The Interrupt Controller may have as few as 33 interrupts. Setting to HIGH_INTS will not have meaning if there are less than 61 interrupt inputs. 0x0: NONE (output 0x0) 0x1: LOW_INTS (31 - IRQn, 30 - FIQn, intsource[29:0]) 0x2: MID_INTS (31 - IRQn, 30 - FIQn, pad 0 as needed, intsource[N up to 59:30]) 0x3: HIGH_INTS (31 - IRQn, 30 - FIQn, 28 bits 0, intsource[63:60])

0x121010EC INTCTL2_INT_CTL_CONFIG

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

The INT_CTL_CONFIG register provides additional configuration options for the interrupt controller used for debug purposes.

INTCTL2_INT_CTL_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_1	
0	NO_NESTING_MODE	Default : 0 This register bit is used to configure the interrupt controller before any interrupts occur. When this bit is cleared (0), the PIC priority logic is used to determine when to assert irq_n. When the software allows hardware interrupt nesting, this bit should be cleared (0). If this bit is set (1), irq_n is asserted whenever there is at least one bit set in IRQ_STATUS. This bit should be set (1) right after power up if the software does not need any hardware nesting functions. 0x0: NESTED 0x1: NOT NESTED

20.8 Interrupt Controller 3 Registers (0x12101800 INTCTL3_BASE)

This section contains Interrupt Controller 3 registers.

20.8.1 Configuration registers

These registers are used to configure the Interrupt Controller

0x12101800 INTCTL3_INT_SELECT_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_0 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL3_INT_SELECT_0

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12101804 INTCTL3_INT_SELECT_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_1 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL3_INT_SELECT_1

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12101810 INTCTL3_INT_ENABLE_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_0 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor.

INTCTL3_INT_ENABLE_0

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12101814 INTCTL3_INT_ENABLE_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_1 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor

INTCTL3_INT_ENABLE_1

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12101820 INTCTL3_INT_ENABLE_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_0 register is used to clear (to 0) the bits of the INT_ENABLE_0 register.

INTCTL3_INT_ENABLE_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear.

0x12101824 INTCTL3_INT_ENABLE_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_1 register is used to clear (to 0) the bits of the INT_ENABLE_1 register.

INTCTL3_INT_ENABLE_CLEAR_1

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Clear.

0x12101830 INTCTL3_INT_ENABLE_SET_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_0 register is used to set (to 1) the bits of the INT_ENABLE_0 register.

INTCTL3_INT_ENABLE_SET_0

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Set.

0x12101834 INTCTL3_INT_ENABLE_SET_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_1 register is used to set (to 1) the bits of the INT_ENABLE_1 register.

INTCTL3_INT_ENABLE_SET_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Set.

0x12101840 INTCTL3_INT_TYPE_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL3_INT_TYPE_0

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12101844 INTCTL3_INT_TYPE_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL3_INT_TYPE_1

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12101850 INTCTL3_INT_POLARITY_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL3_INT_POLARITY_0

Bits	Name	Description
31:0	POL	0x1: neg 0x0: pos

0x12101854 INTCTL3_INT_POLARITY_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL3_INT_POLARITY_1

Bits	Name	Description
31:0	POL	0x1: neg 0x0: posl

0x12101860 INTCTL3_NO_PEND_VAL

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

The NO_PEND_VALUE indicates the 32-bit value returned when reading VEC_RD or PEND_RD when there is no available interrupt. The reset value is the traditional indicator of no pending interrupt. It is convenient to refer to this value as the NULL interrupt.

When using the Interrupt Controller in Vector Mode, it may be useful to set this register to a value where software can jump to perform common end of ISR handling.

INTCTL3_NO_PEND_VAL

Bits	Name	Description
31:0	NULL_VALUE	This value is returned when VEC_RD or PEND_RD when there is no available interrupt

0x12101864 INTCTL3_MASTER_ENABLE

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The MASTER_ENABLE register is the IRQ and FIQ master enable register. The two bits in this register can be used to block the IRQ and/or FIQ signals from reaching the processor. These enables are used to gate off the interrupt signals at IRQ_STATUS and FIQ_STATUS. This will cause irq_n and fiq_n de-asserted if they were previously asserted and stay de-asserted. Note that if a Vector Port transaction has started, it will complete with irq_n still held asserted by the Vector Port logic.

Writing this register has no affect on the INT_ENABLE register.

NOTE The RAW_STATUS register will hold interrupts that have been detected by the Interrupt Controller even if disabled by INT_ENABLE.

INTCTL3_MASTER_ENABLE

Bits	Name	Description
1	FIQ_ENABLE	0x0: Disable 0x1: Enable.
0	IRQ_ENABLE	0x0: Disable 0x1: Enable.

0x12101868 INTCTL3_VIC_CONFIG

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The VIC_CONFIG register is used to enable Vector Port interface.

INTCTL3_VIC_CONFIG

Bits	Name	Description
0	VECTOR_MODE	0x1: Enable 0x0: Disable

0x1210186C INTCTL3_SECURITY

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The SECURITY register is used to enable or disable non-secure bus transactions. The bus security status is signaled to the Interrupt Controller via the ns pin. When ns is set to 0 the state of the SECURITY register is not considered - a secure transaction is allowed if the device is set to non-secure mode. When ns is set to 1, the SECURITY register's SECURE bit must be 0 for access to be granted. If set to 1, the non-secure (ns) transaction is denied. When access is denied, a write is ignored, and a read will return 0x0. No error is signaled.

INTCTL3_SECURITY

Bits	Name	Description
0	SECURE	When enabled, only secure agents can access the registers. When disabled, both secure and non-secure agents can access the registers. 0x1: Enable 0x0: Disable

0x12101A00+ 4*n INTCTL3_PRIORITYn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x0

The PRIORITYn registers are used to determine the priority for each interrupt source.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

NOTE Only IRQs are prioritized. Thus PRIORITYn registers have no affect on FIQ.

INTCTL3_PRIORITYn

Bits	Name	Description
2:0	PRIORITY	Priority for each interrupt source.

0x12101C00+ 4*n INTCTL3_VECT_ADDRn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: NA

The VECT_ADDRn registers provide the vector handle address for each interrupt source N.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

INTCTL3_VECT_ADDRn

Bits	Name	Description
31:2	ADDR	Vector handle (the ISR's starting address) for interrupt source n

INTCTL3_VECT_ADDRn (cont.)

Bits	Name	Description
1:0	RESERVED_BITS1_0	

20.8.2 Operational registers

0x12101880 INTCTL3_IRQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_0 shows which interrupt sources zero to 31 designated for irq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_0.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL3_IRQ_STATUS_0

Bits	Name	Description
31	INT_SRC31	See bit 0's description.
30	INT_SRC30	
29	INT_SRC29	
28	INT_SRC28	
27	INT_SRC27	
26	INT_SRC26	
25	INT_SRC25	
24	INT_SRC24	
23	INT_SRC23	
22	INT_SRC22	
21	INT_SRC21	
20	INT_SRC20	
19	INT_SRC19	
18	INT_SRC18	
17	INT_SRC17	
16	INT_SRC16	
15	INT_SRC15	

INTCTL3_IRQ_STATUS_0 (cont.)

Bits	Name	Description
14	INT_SRC14	
13	INT_SRC13	
12	INT_SRC12	
11	INT_SRC11	
10	INT_SRC10	
9	INT_SRC9	
8	INT_SRC8	
7	INT_SRC7	
6	INT_SRC6	
5	INT_SRC5	
4	INT_SRC4	
3	INT_SRC3	
2	INT_SRC2	
1	INT_SRC1	
0	INT_SRC0	Data for interrupt source bit 0 0x1: active 0x0: inactive

0x12101884 INTCTL3_IRQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_1 shows which interrupt sources 32 to 63 designated for irq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_1.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL3_IRQ_STATUS_1

Bits	Name	Description
31	INT_SRC63	See bit 0's description
30	INT_SRC62	
29	INT_SRC61	

INTCTL3_IRQ_STATUS_1 (cont.)

Bits	Name	Description
28	INT_SRC60	
27	INT_SRC59	
26	INT_SRC58	
25	INT_SRC57	
24	INT_SRC56	
23	INT_SRC55	
22	INT_SRC54	
21	INT_SRC53	
20	INT_SRC52	
19	INT_SRC51	
18	INT_SRC50	
17	INT_SRC49	
16	INT_SRC48	
15	INT_SRC47	
14	INT_SRC46	
13	INT_SRC45	
12	INT_SRC44	
11	INT_SRC43	
10	INT_SRC42	
9	INT_SRC41	
8	INT_SRC40	
7	INT_SRC39	
6	INT_SRC38	
5	INT_SRC37	
4	INT_SRC36	
3	INT_SRC35	
2	INT_SRC34	
1	INT_SRC33	
0	INT_SRC32	Data for interrupt source bit 32 0x1: active 0x0: inactive

0x12101890 INTCTL3_FIQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_0 shows which interrupt sources zero to 31 designated for fiq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_0.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL3_FIQ_STATUS_0

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_0 fields

0x12101894 INTCTL3_FIQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_1 shows which interrupt sources 32 to 63 designated for fiq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_1.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL3_FIQ_STATUS_1

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_1 fields

0x121018A0 INTCTL3_RAW_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_0 shows which interrupt sources zero to 31 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_0. Bits set in RAW_STATUS_0 are steered to generate irq_n or fiq_n by INT_SELECT_0 if enabled by both INT_ENABLE_0 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_0 by writing SOFT_INT_0.

INTCTL3_RAW_STATUS_0

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_0

0x121018A4 INTCTL3_RAW_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_1 shows which interrupt sources 32 to 63 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_1. Bits set in RAW_STATUS_1 are steered to generate irq_n or fiq_n by INT_SELECT_1 if enabled by both INT_ENABLE _1 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_1 by writing SOFT_INT_1.

INTCTL3_RAW_STATUS_1

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_1

0x121018B0 INTCTL3_INT_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_0 is used to clear bits in RAW_STATUS_0. For any bit written 0x1 to INT_CLEAR_0, the corresponding bit position is cleared in RAW_STATUS_0.

INTCTL3_INT_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121018B4 INTCTL3_INT_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_1 is used to clear bits in RAW_STATUS_1. For any bit written 0x1 to INT_CLEAR_1, the corresponding bit position is cleared in RAW_STATUS_1.

INTCTL3_INT_CLEAR_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121018C0 INTCTL3_SOFT_INT_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_0 is used to set bits in RAW_STATUS_0 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_0, the corresponding bit position is set in RAW_STATUS_0.

INTCTL3_SOFT_INT_0

Bits	Name	Description
31:0	SW_INT	0x0: Do nothing 0x1: Set

0x121018C4 INTCTL3_SOFT_INT_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_1 is used to set bits in RAW_STATUS_1 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_1, the corresponding bit position is set in RAW_STATUS_1.

INTCTL3_SOFT_INT_1

Bits	Name	Description
31:0	SW_INT	See IRQ_STATUS_1 for bit map. 0x0: Do nothing 0x1: Set

0x121018D0 INTCTL3_VEC_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack PUSH in the PIC, and if an interrupt is causing irq_n returns it.

Assuming an interrupt is available and irq_n is asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU has seen irq_n.
- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine.
- The PIC will set a bit in IN_STACK for the sw level that has been interrupted (including "main").
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that caused the irq_n.
- Subsequently irq_n may only be asserted for an interrupt source designated at a higher priority level than the highest priority level indicated by IN_SERVICE.

If irq_n is asserted, the value returned when reading VEC_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If irq_n is not asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When the Interrupt Controller is in Vector Mode, as designated by VIC_CONFIG, VEC_RD should not be read. The controller still needs to be informed that the CPU is taking the interrupt. This is done by a Vector Port transaction. However, if VEC_RD is read in while in Vector Mode, the read will have the same effect as in PIC mode. However, the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE Using this register while the system is in Vector Mode may not be reliable as CPU hardware may initiate a Vector Port transaction while launching the read transaction to VEC_RD. This race condition could have undesirable results.

INTCTL3_VEC_RD

Bits	Name	Description
31:0	INDEX	Reading from this register provides the index of the current interrupt selected by the PIC, and indicates to the priority hardware that the interrupt is being serviced. Though the practice is not recommended, if this register is read in Vector Mode, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to VEC_RD. The commanded PUSH is performed. If irq_n is not currently active, reading this register returns the value stored in NO_PEND_VAL. There are no side effects in this case - the commanded PUSH is not performed.

0x121018D4 INTCTL3_PEND_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack POP in the PIC, and if an interrupt is pending returns it.

Assuming an interrupt is available and irq_n is not asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine, and ending the previous ISR routine.
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that is now starting.
- The PIC will clear the most significant bit found set in IN_SERVICE for the priority of the interrupt ISR routine just ended if the priority of the interrupt now starting is different.

If an interrupt is available and irq_n is asserted or if no interrupt is available the PIC will behave as if the VEC_WR command register was written. That is, the command issued to the PIC will be interpreted as a POP.

The value returned when reading PEND_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If no interrupt is asserted or if irq_n is asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When Vector Mode is enabled, unlike the VEC_RD register, PEND_RD must be read in order to inform the PIC that the ISR has finished processing. There is no equivalent

Vector Port transaction. When not in Vector Mode, the interrupts index (bit position) is returned.

NOTE In Vector Mode the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE VEC_WR can be substituted for PEND_RD to inform the PIC that the ISR has finished processing without returning a pending interrupt.

INTCTL3_PEND_RD

Bits	Name	Description
31:0	HANDLE	Reading from this register provides the index of the current interrupt selected by the PIC as a pending interrupt. It also indicates to the priority hardware that the current ISR is finished, and if an interrupt is pending that a new ISR is starting. In Vector Mode, when an interrupt is pending, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to PEND_RD. The commanded POP is performed. If an interrupt is not pending, reading this register returns the value stored in NO_PEND_VAL. The commanded POP is still performed.

0x121018D8 INTCTL3_VEC_WR

Type: Write (command)
Clock: INT_CTL_CLK
Reset State: NA

This is a write command register. It affects a logical stack POP in the PIC without returning any (possibly) pending interrupt. The resulting state of the PIC is to request a new irq_n if any bits are set in IRQ_STATUS.

Writing this register has the following side effects:

- Informs the PIC logic that the CPU is ending the current ISR routine.
- The PIC will clear the most significant bit found set in IN_SERVICE.
- The PIC will clear the most significant bit found set in IN_STACK.

NOTE PEND_RD can be substituted for VEC_WR to inform the PIC that the ISR has finished processing and to return a pending interrupt at the same time.

INTCTL3_VEC_WR

Bits	Name	Description
31:0	RESERVED	Data written is not used.

20.8.3 Debug and legacy registers

0x121018E0 INTCTL3_IN_SERVICE

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_SERVICE register provides the Interrupt Controller's state information regarding which ISR priority levels are currently in service by the processor. This is provided for debug purposes only.

INTCTL3_IN_SERVICE

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL7	0x1: In service 0x0: Not in service
6	LEVEL6	0x1: In service 0x0: Not in service
5	LEVEL5	0x1: In service 0x0: Not in service
4	LEVEL4	0x1: In service 0x0: Not in service
3	LEVEL3	0x1: In service 0x0: Not in service
2	LEVEL2	0x1: In service 0x0: Not in service
1	LEVEL1	0x1: In service 0x0: Not in service
0	LEVEL0	0x1: In service 0x0: Not in service

0x121018E4 INTCTL3_IN_STACK

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_STACK register provides the Interrupt Controller's state information regarding which ISR priority levels are currently nested (stacked) in the CPU. This is provided for debug purposes only.

INTCTL3_IN_STACK

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL6	0x1: Nested 0x0: Not nested
6	LEVEL5	0x1: Nested 0x0: Not nested
5	LEVEL4	0x1: Nested 0x0: Not nested
4	LEVEL3	0x1: Nested 0x0: Not nested
3	LEVEL2	0x1: Nested 0x0: Not nested
2	LEVEL1	0x1: Nested 0x0: Not nested
1	LEVEL0	0x1: Nested 0x0: Not nested
0	MAIN	0x1: Nested 0x0: Not nested

0x121018E8 INTCTL3_TEST_BUS_SEL

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

Select signals to be directed to Interrupt Controller test_bus 32-bit output port.

INTCTL3_TEST_BUS_SEL

Bits	Name	Description
31:2	RESERVED	
1:0	SEL	NOTE The Interrupt Controller may have as few as 33 interrupts. Setting to HIGH_INTS will not have meaning if there are less than 61 interrupt inputs. 0x0: NONE (output 0x0) 0x1: LOW_INTS (31 - IRQn, 30 - FIQn, intsource[29:0]) 0x2: MID_INTS (31 - IRQn, 30 - FIQn, pad 0 as needed, intsource[N up to 59:30]) 0x3: HIGH_INTS (31 - IRQn, 30 - FIQn, 28 bits 0, intsource[63:60])

0x121018EC INTCTL3_INT_CTL_CONFIG

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

The INT_CTL_CONFIG register provides additional configuration options for the interrupt controller used for debug purposes.

INTCTL3_INT_CTL_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_1	
0	NO_NESTING_MODE	Default : 0 This register bit is used to configure the interrupt controller before any interrupts occur. When this bit is cleared (0), the PIC priority logic is used to determine when to assert irq_n. When the software allows hardware interrupt nesting, this bit should be cleared (0). If this bit is set (1), irq_n is asserted whenever there is at least one bit set in IRQ_STATUS. This bit should be set (1) right after power up if the software does not need any hardware nesting functions. 0x0: NESTED 0x1: NOT NESTED

20.9 Interrupt Controller 4 Registers (0x12102000 INTCTL4_BASE)

This section contains Interrupt Controller 4 registers.

20.9.1 Configuration registers

These registers are used to configure the Interrupt Controller.

0x12102000 INTCTL4_INT_SELECT_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_0 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL4_INT_SELECT_0

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12102004 INTCTL4_INT_SELECT_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_1 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL4_INT_SELECT_1

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12102010 INTCTL4_INT_ENABLE_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_0 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor.

INTCTL4_INT_ENABLE_0

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12102014 INTCTL4_INT_ENABLE_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_1 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor

INTCTL4_INT_ENABLE_1

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12102020 INTCTL4_INT_ENABLE_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_0 register is used to clear (to 0) the bits of the INT_ENABLE_0 register.

INTCTL4_INT_ENABLE_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear.

0x12102024 INTCTL4_INT_ENABLE_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_1 register is used to clear (to 0) the bits of the INT_ENABLE_1 register.

INTCTL4_INT_ENABLE_CLEAR_1

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Clear.

0x12102030 INTCTL4_INT_ENABLE_SET_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_0 register is used to set (to 1) the bits of the INT_ENABLE_0 register.

INTCTL4_INT_ENABLE_SET_0

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Set.

0x12102034 INTCTL4_INT_ENABLE_SET_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_1 register is used to set (to 1) the bits of the INT_ENABLE_1 register.

INTCTL4_INT_ENABLE_SET_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Set.

0x12102040 INTCTL4_INT_TYPE_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL4_INT_TYPE_0

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12102044 INTCTL4_INT_TYPE_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL4_INT_TYPE_1

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12102050 INTCTL4_INT_POLARITY_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL4_INT_POLARITY_0

Bits	Name	Description
31:0	POL	0x1: neg 0x0: pos

0x12102054 INTCTL4_INT_POLARITY_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL4_INT_POLARITY_1

Bits	Name	Description
31:0	POL	0x1: neg 0x0: posl

0x12102060 INTCTL4_NO_PEND_VAL

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

The NO_PEND_VALUE indicates the 32-bit value returned when reading VEC_RD or PEND_RD when there is no available interrupt. The reset value is the traditional indicator of no pending interrupt. It is convenient to refer to this value as the NULL interrupt.

When using the Interrupt Controller in Vector Mode, it may be useful to set this register to a value where software can jump to perform common end of ISR handling.

INTCTL4_NO_PEND_VAL

Bits	Name	Description
31:0	NULL_VALUE	This value is returned when VEC_RD or PEND_RD when there is no available interrupt

0x12102064 INTCTL4_MASTER_ENABLE

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The MASTER_ENABLE register is the IRQ and FIQ master enable register. The two bits in this register can be used to block the IRQ and/or FIQ signals from reaching the processor. These enables are used to gate off the interrupt signals at IRQ_STATUS and FIQ_STATUS. This will cause irq_n and fiq_n de-asserted if they were previously asserted and stay de-asserted. Note that if a Vector Port transaction has started, it will complete with irq_n still held asserted by the Vector Port logic.

Writing this register has no affect on the INT_ENABLE register.

NOTE The RAW_STATUS register will hold interrupts that have been detected by the Interrupt Controller even if disabled by INT_ENABLE.

INTCTL4_MASTER_ENABLE

Bits	Name	Description
1	FIQ_ENABLE	0x0: Disable 0x1: Enable.
0	IRQ_ENABLE	0x0: Disable 0x1: Enable.

0x12102068 INTCTL4_VIC_CONFIG

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The VIC_CONFIG register is used to enable Vector Port interface.

INTCTL4_VIC_CONFIG

Bits	Name	Description
0	VECTOR_MODE	0x1: Enable 0x0: Disable

0x1210206C INTCTL4_SECURITY

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The SECURITY register is used to enable or disable non-secure bus transactions. The bus security status is signaled to the Interrupt Controller via the ns pin. When ns is set to 0 the state of the SECURITY register is not considered - a secure transaction is allowed if the device is set to non-secure mode. When ns is set to 1, the SECURITY register's SECURE bit must be 0 for access to be granted. If set to 1, the non-secure (ns) transaction is denied. When access is denied, a write is ignored, and a read will return 0x0. No error is signaled.

INTCTL4_SECURITY

Bits	Name	Description
0	SECURE	When enabled, only secure agents can access the registers. When disabled, both secure and non-secure agents can access the registers. 0x1: Enable 0x0: Disable

0x12102200+4*n INTCTL4_PRIORITYn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x0

The PRIORITYn registers are used to determine the priority for each interrupt source.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

NOTE Only IRQs are prioritized. Thus PRIORITYn registers have no affect on FIQ.

INTCTL4_PRIORITYn

Bits	Name	Description
2:0	PRIORITY	Priority for each interrupt source.

0x12102400+4*n INTCTL4_VECT_ADDRn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: NA

The VECT_ADDRn registers provide the vector handle address for each interrupt source N.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

INTCTL4_VECT_ADDRn

Bits	Name	Description
31:2	ADDR	Vector handle (the ISR's starting address) for interrupt source n

INTCTL4_VECT_ADDRn (cont.)

Bits	Name	Description
1:0	RESERVED_BITS1_0	

20.9.2 Operational registers

0x12102080 INTCTL4_IRQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_0 shows which interrupt sources zero to 31 designated for irq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_0.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL4_IRQ_STATUS_0

Bits	Name	Description
31	INT_SRC31	See bit 0's description.
30	INT_SRC30	
29	INT_SRC29	
28	INT_SRC28	
27	INT_SRC27	
26	INT_SRC26	
25	INT_SRC25	
24	INT_SRC24	
23	INT_SRC23	
22	INT_SRC22	
21	INT_SRC21	
20	INT_SRC20	
19	INT_SRC19	
18	INT_SRC18	
17	INT_SRC17	
16	INT_SRC16	
15	INT_SRC15	

INTCTL4_IRQ_STATUS_0 (cont.)

Bits	Name	Description
14	INT_SRC14	
13	INT_SRC13	
12	INT_SRC12	
11	INT_SRC11	
10	INT_SRC10	
9	INT_SRC9	
8	INT_SRC8	
7	INT_SRC7	
6	INT_SRC6	
5	INT_SRC5	
4	INT_SRC4	
3	INT_SRC3	
2	INT_SRC2	
1	INT_SRC1	
0	INT_SRC0	Data for interrupt source bit 0 0x1: active 0x0: inactive

0x12102084 INTCTL4_IRQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_1 shows which interrupt sources 32 to 63 designated for irq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_1.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL4_IRQ_STATUS_1

Bits	Name	Description
31	INT_SRC63	See bit 0's description
30	INT_SRC62	
29	INT_SRC61	

INTCTL4_IRQ_STATUS_1 (cont.)

Bits	Name	Description
28	INT_SRC60	
27	INT_SRC59	
26	INT_SRC58	
25	INT_SRC57	
24	INT_SRC56	
23	INT_SRC55	
22	INT_SRC54	
21	INT_SRC53	
20	INT_SRC52	
19	INT_SRC51	
18	INT_SRC50	
17	INT_SRC49	
16	INT_SRC48	
15	INT_SRC47	
14	INT_SRC46	
13	INT_SRC45	
12	INT_SRC44	
11	INT_SRC43	
10	INT_SRC42	
9	INT_SRC41	
8	INT_SRC40	
7	INT_SRC39	
6	INT_SRC38	
5	INT_SRC37	
4	INT_SRC36	
3	INT_SRC35	
2	INT_SRC34	
1	INT_SRC33	
0	INT_SRC32	Data for interrupt source bit 32 0x1: active 0x0: inactive

0x12102090 INTCTL4_FIQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_0 shows which interrupt sources zero to 31 designated for fiq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_0.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL4_FIQ_STATUS_0

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_0 fields

0x12102094 INTCTL4_FIQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_1 shows which interrupt sources 32 to 63 designated for fiq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_1.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL4_FIQ_STATUS_1

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_1 fields

0x121020A0 INTCTL4_RAW_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_0 shows which interrupt sources zero to 31 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_0. Bits set in RAW_STATUS_0 are steered to generate irq_n or fiq_n by INT_SELECT_0 if enabled by both INT_ENABLE_0 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_0 by writing SOFT_INT_0.

INTCTL4_RAW_STATUS_0

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_0

0x121020A4 INTCTL4_RAW_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_1 shows which interrupt sources 32 to 63 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_1. Bits set in RAW_STATUS_1 are steered to generate irq_n or fiq_n by INT_SELECT_1 if enabled by both INT_ENABLE _1 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_1 by writing SOFT_INT_1.

INTCTL4_RAW_STATUS_1

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_1

0x121020B0 INTCTL4_INT_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_0 is used to clear bits in RAW_STATUS_0. For any bit written 0x1 to INT_CLEAR_0, the corresponding bit position is cleared in RAW_STATUS_0.

INTCTL4_INT_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121020B4 INTCTL4_INT_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_1 is used to clear bits in RAW_STATUS_1. For any bit written 0x1 to INT_CLEAR_1, the corresponding bit position is cleared in RAW_STATUS_1.

INTCTL4_INT_CLEAR_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121020C0 INTCTL4_SOFT_INT_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_0 is used to set bits in RAW_STATUS_0 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_0, the corresponding bit position is set in RAW_STATUS_0.

INTCTL4_SOFT_INT_0

Bits	Name	Description
31:0	SW_INT	0x0: Do nothing 0x1: Set

0x121020C4 INTCTL4_SOFT_INT_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_1 is used to set bits in RAW_STATUS_1 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_1, the corresponding bit position is set in RAW_STATUS_1.

INTCTL4_SOFT_INT_1

Bits	Name	Description
31:0	SW_INT	See IRQ_STATUS_1 for bit map. 0x0: Do nothing 0x1: Set

0x121020D0 INTCTL4_VEC_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack PUSH in the PIC, and if an interrupt is causing irq_n returns it.

Assuming an interrupt is available and irq_n is asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU has seen irq_n.
- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine.
- The PIC will set a bit in IN_STACK for the sw level that has been interrupted (including "main").
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that caused the irq_n.
- Subsequently irq_n may only be asserted for an interrupt source designated at a higher priority level than the highest priority level indicated by IN_SERVICE.

If irq_n is asserted, the value returned when reading VEC_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If irq_n is not asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When the Interrupt Controller is in Vector Mode, as designated by VIC_CONFIG, VEC_RD should not be read. The controller still needs to be informed that the CPU is taking the interrupt. This is done by a Vector Port transaction. However, if VEC_RD is read in while in Vector Mode, the read will have the same effect as in PIC mode. However, the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE Using this register while the system is in Vector Mode may not be reliable as CPU hardware may initiate a Vector Port transaction while launching the read transaction to VEC_RD. This race condition could have undesirable results.

INTCTL4_VEC_RD

Bits	Name	Description
31:0	INDEX	Reading from this register provides the index of the current interrupt selected by the PIC, and indicates to the priority hardware that the interrupt is being serviced. Though the practice is not recommended, if this register is read in Vector Mode, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to VEC_RD. The commanded PUSH is performed. If irq_n is not currently active, reading this register returns the value stored in NO_PEND_VAL. There are no side effects in this case - the commanded PUSH is not performed.

0x121020D4 INTCTL4_PEND_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack POP in the PIC, and if an interrupt is pending returns it.

Assuming an interrupt is available and irq_n is not asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine, and ending the previous ISR routine.
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that is now starting.
- The PIC will clear the most significant bit found set in IN_SERVICE for the priority of the interrupt ISR routine just ended if the priority of the interrupt now starting is different.

If an interrupt is available and irq_n is asserted or if no interrupt is available the PIC will behave as if the VEC_WR command register was written. That is, the command issued to the PIC will be interpreted as a POP.

The value returned when reading PEND_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If no interrupt is asserted or if irq_n is asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When Vector Mode is enabled, unlike the VEC_RD register, PEND_RD must be read in order to inform the PIC that the ISR has finished processing. There is no equivalent

Vector Port transaction. When not in Vector Mode, the interrupts index (bit position) is returned.

NOTE In Vector Mode the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE VEC_WR can be substituted for PEND_RD to inform the PIC that the ISR has finished processing without returning a pending interrupt.

INTCTL4_PEND_RD

Bits	Name	Description
31:0	HANDLE	Reading from this register provides the index of the current interrupt selected by the PIC as a pending interrupt. It also indicates to the priority hardware that the current ISR is finished, and if an interrupt is pending that a new ISR is starting. In Vector Mode, when an interrupt is pending, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to PEND_RD. The commanded POP is performed. If an interrupt is not pending, reading this register returns the value stored in NO_PEND_VAL. The commanded POP is still performed.

0x121020D8 INTCTL4_VEC_WR

Type: Write (command)
Clock: INT_CTL_CLK
Reset State: NA

This is a write command register. It affects a logical stack POP in the PIC without returning any (possibly) pending interrupt. The resulting state of the PIC is to request a new irq_n if any bits are set in IRQ_STATUS.

Writing this register has the following side effects:

- Informs the PIC logic that the CPU is ending the current ISR routine.
- The PIC will clear the most significant bit found set in IN_SERVICE.
- The PIC will clear the most significant bit found set in IN_STACK.

NOTE PEND_RD can be substituted for VEC_WR to inform the PIC that the ISR has finished processing and to return a pending interrupt at the same time.

INTCTL4_VEC_WR

Bits	Name	Description
31:0	RESERVED	Data written is not used.

20.9.3 Debug and legacy registers

0x121020E0 INTCTL4_IN_SERVICE

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_SERVICE register provides the Interrupt Controller's state information regarding which ISR priority levels are currently in service by the processor. This is provided for debug purposes only.

INTCTL4_IN_SERVICE

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL7	0x1: In service 0x0: Not in service
6	LEVEL6	0x1: In service 0x0: Not in service
5	LEVEL5	0x1: In service 0x0: Not in service
4	LEVEL4	0x1: In service 0x0: Not in service
3	LEVEL3	0x1: In service 0x0: Not in service
2	LEVEL2	0x1: In service 0x0: Not in service
1	LEVEL1	0x1: In service 0x0: Not in service
0	LEVEL0	0x1: In service 0x0: Not in service

0x121020E4 INTCTL4_IN_STACK

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_STACK register provides the Interrupt Controller's state information regarding which ISR priority levels are currently nested (stacked) in the CPU. This is provided for debug purposes only.

INTCTL4_IN_STACK

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL6	0x1: Nested 0x0: Not nested
6	LEVEL5	0x1: Nested 0x0: Not nested
5	LEVEL4	0x1: Nested 0x0: Not nested
4	LEVEL3	0x1: Nested 0x0: Not nested
3	LEVEL2	0x1: Nested 0x0: Not nested
2	LEVEL1	0x1: Nested 0x0: Not nested
1	LEVEL0	0x1: Nested 0x0: Not nested
0	MAIN	0x1: Nested 0x0: Not nested

0x121020E8 INTCTL4_TEST_BUS_SEL

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

Select signals to be directed to Interrupt Controller test_bus 32-bit output port.

INTCTL4_TEST_BUS_SEL

Bits	Name	Description
31:2	RESERVED	
1:0	SEL	NOTE The Interrupt Controller may have as few as 33 interrupts. Setting to HIGH_INTS will not have meaning if there are less than 61 interrupt inputs. 0x0: NONE (output 0x0) 0x1: LOW_INTS (31 - IRQn, 30 - FIQn, intsource[29:0]) 0x2: MID_INTS (31 - IRQn, 30 - FIQn, pad 0 as needed, intsource[N up to 59:30]) 0x3: HIGH_INTS (31 - IRQn, 30 - FIQn, 28 bits 0, intsource[63:60])

0x121020EC INTCTL4_INT_CTL_CONFIG

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

The INT_CTL_CONFIG register provides additional configuration options for the interrupt controller used for debug purposes.

INTCTL4_INT_CTL_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_1	
0	NO_NESTING_MODE	Default : 0 This register bit is used to configure the interrupt controller before any interrupts occur. When this bit is cleared (0), the PIC priority logic is used to determine when to assert irq_n. When the software allows hardware interrupt nesting, this bit should be cleared (0). If this bit is set (1), irq_n is asserted whenever there is at least one bit set in IRQ_STATUS. This bit should be set (1) right after power up if the software does not need any hardware nesting functions. 0x0: NESTED 0x1: NOT NESTED

20.10 Interrupt Controller 5 Registers (0x12102800 INTCTL5_BASE)

This section contains Interrupt Controller 5 registers.

20.10.1 Configuration registers

These registers are used to configure the Interrupt Controller

0x12102800 INTCTL5_INT_SELECT_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_0 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL5_INT_SELECT_0

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12102804 INTCTL5_INT_SELECT_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_1 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL5_INT_SELECT_1

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12102810 INTCTL5_INT_ENABLE_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_0 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor.

INTCTL5_INT_ENABLE_0

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12102814 INTCTL5_INT_ENABLE_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_1 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor

INTCTL5_INT_ENABLE_1

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12102820 INTCTL5_INT_ENABLE_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_0 register is used to clear (to 0) the bits of the INT_ENABLE_0 register.

INTCTL5_INT_ENABLE_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear.

0x12102824 INTCTL5_INT_ENABLE_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_1 register is used to clear (to 0) the bits of the INT_ENABLE_1 register.

INTCTL5_INT_ENABLE_CLEAR_1

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Clear.

0x12102830 INTCTL5_INT_ENABLE_SET_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_0 register is used to set (to 1) the bits of the INT_ENABLE_0 register.

INTCTL5_INT_ENABLE_SET_0

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Set.

0x12102834 INTCTL5_INT_ENABLE_SET_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_1 register is used to set (to 1) the bits of the INT_ENABLE_1 register.

INTCTL5_INT_ENABLE_SET_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Set.

0x12102840 INTCTL5_INT_TYPE_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL5_INT_TYPE_0

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12102844 INTCTL5_INT_TYPE_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL5_INT_TYPE_1

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12102850 INTCTL5_INT_POLARITY_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL5_INT_POLARITY_0

Bits	Name	Description
31:0	POL	0x1: neg 0x0: pos

0x12102854 INTCTL5_INT_POLARITY_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL5_INT_POLARITY_1

Bits	Name	Description
31:0	POL	0x1: neg 0x0: posl

0x12102860 INTCTL5_NO_PEND_VAL

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

The NO_PEND_VALUE indicates the 32-bit value returned when reading VEC_RD or PEND_RD when there is no available interrupt. The reset value is the traditional indicator of no pending interrupt. It is convenient to refer to this value as the NULL interrupt.

When using the Interrupt Controller in Vector Mode, it may be useful to set this register to a value where software can jump to perform common end of ISR handling.

INTCTL5_NO_PEND_VAL

Bits	Name	Description
31:0	NULL_VALUE	This value is returned when VEC_RD or PEND_RD when there is no available interrupt

0x12102864 INTCTL5_MASTER_ENABLE

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The MASTER_ENABLE register is the IRQ and FIQ master enable register. The two bits in this register can be used to block the IRQ and/or FIQ signals from reaching the processor. These enables are used to gate off the interrupt signals at IRQ_STATUS and FIQ_STATUS. This will cause irq_n and fiq_n de-asserted if they were previously asserted and stay de-asserted. Note that if a Vector Port transaction has started, it will complete with irq_n still held asserted by the Vector Port logic.

Writing this register has no affect on the INT_ENABLE register.

NOTE The RAW_STATUS register will hold interrupts that have been detected by the Interrupt Controller even if disabled by INT_ENABLE.

INTCTL5_MASTER_ENABLE

Bits	Name	Description
1	FIQ_ENABLE	0x0: Disable 0x1: Enable.
0	IRQ_ENABLE	0x0: Disable 0x1: Enable.

0x12102868 INTCTL5_VIC_CONFIG

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The VIC_CONFIG register is used to enable Vector Port interface.

INTCTL5_VIC_CONFIG

Bits	Name	Description
0	VECTOR_MODE	0x1: Enable 0x0: Disable

0x1210286C INTCTL5_SECURITY

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The SECURITY register is used to enable or disable non-secure bus transactions. The bus security status is signaled to the Interrupt Controller via the ns pin. When ns is set to 0 the state of the SECURITY register is not considered - a secure transaction is allowed if the device is set to non-secure mode. When ns is set to 1, the SECURITY register's SECURE bit must be 0 for access to be granted. If set to 1, the non-secure (ns) transaction is denied. When access is denied, a write is ignored, and a read will return 0x0. No error is signaled.

INTCTL5_SECURITY

Bits	Name	Description
0	SECURE	When enabled, only secure agents can access the registers. When disabled, both secure and non-secure agents can access the registers. 0x1: Enable 0x0: Disable

0x12102A00+ 4*n INTCTL5_PRIORITYn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x0

The PRIORITYn registers are used to determine the priority for each interrupt source.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

NOTE Only IRQs are prioritized. Thus PRIORITYn registers have no affect on FIQ.

INTCTL5_PRIORITYn

Bits	Name	Description
2:0	PRIORITY	Priority for each interrupt source.

0x12102C00+ 4*n INTCTL5_VECT_ADDRn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: NA

The VECT_ADDRn registers provide the vector handle address for each interrupt source N.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

INTCTL5_VECT_ADDRn

Bits	Name	Description
31:2	ADDR	Vector handle (the ISR's starting address) for interrupt source n

INTCTL5_VECT_ADDRn (cont.)

Bits	Name	Description
1:0	RESERVED_BITS1_0	

20.10.2 Operational registers

0x12102880 INTCTL5_IRQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_0 shows which interrupt sources zero to 31 designated for irq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_0.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL5_IRQ_STATUS_0

Bits	Name	Description
31	INT_SRC31	See bit 0's description.
30	INT_SRC30	
29	INT_SRC29	
28	INT_SRC28	
27	INT_SRC27	
26	INT_SRC26	
25	INT_SRC25	
24	INT_SRC24	
23	INT_SRC23	
22	INT_SRC22	
21	INT_SRC21	
20	INT_SRC20	
19	INT_SRC19	
18	INT_SRC18	
17	INT_SRC17	
16	INT_SRC16	
15	INT_SRC15	

INTCTL5_IRQ_STATUS_0 (cont.)

Bits	Name	Description
14	INT_SRC14	
13	INT_SRC13	
12	INT_SRC12	
11	INT_SRC11	
10	INT_SRC10	
9	INT_SRC9	
8	INT_SRC8	
7	INT_SRC7	
6	INT_SRC6	
5	INT_SRC5	
4	INT_SRC4	
3	INT_SRC3	
2	INT_SRC2	
1	INT_SRC1	
0	INT_SRC0	Data for interrupt source bit 0 0x1: active 0x0: inactive

0x12102884 INTCTL5_IRQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_1 shows which interrupt sources 32 to 63 designated for irq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_1.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL5_IRQ_STATUS_1

Bits	Name	Description
31	INT_SRC63	See bit 0's description
30	INT_SRC62	
29	INT_SRC61	

INTCTL5_IRQ_STATUS_1 (cont.)

Bits	Name	Description
28	INT_SRC60	
27	INT_SRC59	
26	INT_SRC58	
25	INT_SRC57	
24	INT_SRC56	
23	INT_SRC55	
22	INT_SRC54	
21	INT_SRC53	
20	INT_SRC52	
19	INT_SRC51	
18	INT_SRC50	
17	INT_SRC49	
16	INT_SRC48	
15	INT_SRC47	
14	INT_SRC46	
13	INT_SRC45	
12	INT_SRC44	
11	INT_SRC43	
10	INT_SRC42	
9	INT_SRC41	
8	INT_SRC40	
7	INT_SRC39	
6	INT_SRC38	
5	INT_SRC37	
4	INT_SRC36	
3	INT_SRC35	
2	INT_SRC34	
1	INT_SRC33	
0	INT_SRC32	Data for interrupt source bit 32 0x1: active 0x0: inactive

0x12102890 INTCTL5_FIQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_0 shows which interrupt sources zero to 31 designated for fiq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_0.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL5_FIQ_STATUS_0

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_0 fields

0x12102894 INTCTL5_FIQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_1 shows which interrupt sources 32 to 63 designated for fiq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_1.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL5_FIQ_STATUS_1

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_1 fields

0x121028A0 INTCTL5_RAW_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_0 shows which interrupt sources zero to 31 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_0. Bits set in RAW_STATUS_0 are steered to generate irq_n or fiq_n by INT_SELECT_0 if enabled by both INT_ENABLE_0 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_0 by writing SOFT_INT_0.

INTCTL5_RAW_STATUS_0

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_0

0x121028A4 INTCTL5_RAW_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_1 shows which interrupt sources 32 to 63 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_1. Bits set in RAW_STATUS_1 are steered to generate irq_n or fiq_n by INT_SELECT_1 if enabled by both INT_ENABLE _1 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_1 by writing SOFT_INT_1.

INTCTL5_RAW_STATUS_1

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_1

0x121028B0 INTCTL5_INT_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_0 is used to clear bits in RAW_STATUS_0. For any bit written 0x1 to INT_CLEAR_0, the corresponding bit position is cleared in RAW_STATUS_0.

INTCTL5_INT_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121028B4 INTCTL5_INT_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_1 is used to clear bits in RAW_STATUS_1. For any bit written 0x1 to INT_CLEAR_1, the corresponding bit position is cleared in RAW_STATUS_1.

INTCTL5_INT_CLEAR_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121028C0 INTCTL5_SOFT_INT_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_0 is used to set bits in RAW_STATUS_0 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_0, the corresponding bit position is set in RAW_STATUS_0.

INTCTL5_SOFT_INT_0

Bits	Name	Description
31:0	SW_INT	0x0: Do nothing 0x1: Set

0x121028C4 INTCTL5_SOFT_INT_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_1 is used to set bits in RAW_STATUS_1 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_1, the corresponding bit position is set in RAW_STATUS_1.

INTCTL5_SOFT_INT_1

Bits	Name	Description
31:0	SW_INT	See IRQ_STATUS_1 for bit map. 0x0: Do nothing 0x1: Set

0x121028D0 INTCTL5_VEC_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack PUSH in the PIC, and if an interrupt is causing irq_n returns it.

Assuming an interrupt is available and irq_n is asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU has seen irq_n.
- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine.
- The PIC will set a bit in IN_STACK for the sw level that has been interrupted (including "main").
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that caused the irq_n.
- Subsequently irq_n may only be asserted for an interrupt source designated at a higher priority level than the highest priority level indicated by IN_SERVICE.

If irq_n is asserted, the value returned when reading VEC_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If irq_n is not asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When the Interrupt Controller is in Vector Mode, as designated by VIC_CONFIG, VEC_RD should not be read. The controller still needs to be informed that the CPU is taking the interrupt. This is done by a Vector Port transaction. However, if VEC_RD is read in while in Vector Mode, the read will have the same effect as in PIC mode. However, the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE Using this register while the system is in Vector Mode may not be reliable as CPU hardware may initiate a Vector Port transaction while launching the read transaction to VEC_RD. This race condition could have undesirable results.

INTCTL5_VEC_RD

Bits	Name	Description
31:0	INDEX	Reading from this register provides the index of the current interrupt selected by the PIC, and indicates to the priority hardware that the interrupt is being serviced. Though the practice is not recommended, if this register is read in Vector Mode, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to VEC_RD. The commanded PUSH is performed. If irq_n is not currently active, reading this register returns the value stored in NO_PEND_VAL. There are no side effects in this case - the commanded PUSH is not performed.

0x121028D4 INTCTL5_PEND_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack POP in the PIC, and if an interrupt is pending returns it.

Assuming an interrupt is available and irq_n is not asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine, and ending the previous ISR routine.
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that is now starting.
- The PIC will clear the most significant bit found set in IN_SERVICE for the priority of the interrupt ISR routine just ended if the priority of the interrupt now starting is different.

If an interrupt is available and irq_n is asserted or if no interrupt is available the PIC will behave as if the VEC_WR command register was written. That is, the command issued to the PIC will be interpreted as a POP.

The value returned when reading PEND_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If no interrupt is asserted or if irq_n is asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When Vector Mode is enabled, unlike the VEC_RD register, PEND_RD must be read in order to inform the PIC that the ISR has finished processing. There is no equivalent

Vector Port transaction. When not in Vector Mode, the interrupts index (bit position) is returned.

NOTE In Vector Mode the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE VEC_WR can be substituted for PEND_RD to inform the PIC that the ISR has finished processing without returning a pending interrupt.

INTCTL5_PEND_RD

Bits	Name	Description
31:0	HANDLE	Reading from this register provides the index of the current interrupt selected by the PIC as a pending interrupt. It also indicates to the priority hardware that the current ISR is finished, and if an interrupt is pending that a new ISR is starting. In Vector Mode, when an interrupt is pending, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to PEND_RD. The commanded POP is performed. If an interrupt is not pending, reading this register returns the value stored in NO_PEND_VAL. The commanded POP is still performed.

0x121028D8 INTCTL5_VEC_WR

Type: Write (command)
Clock: INT_CTL_CLK
Reset State: NA

This is a write command register. It affects a logical stack POP in the PIC without returning any (possibly) pending interrupt. The resulting state of the PIC is to request a new irq_n if any bits are set in IRQ_STATUS.

Writing this register has the following side effects:

- Informs the PIC logic that the CPU is ending the current ISR routine.
- The PIC will clear the most significant bit found set in IN_SERVICE.
- The PIC will clear the most significant bit found set in IN_STACK.

NOTE PEND_RD can be substituted for VEC_WR to inform the PIC that the ISR has finished processing and to return a pending interrupt at the same time.

INTCTL5_VEC_WR

Bits	Name	Description
31:0	RESERVED	Data written is not used.

20.10.3 Debug and legacy registers

0x121028E0 INTCTL5_IN_SERVICE

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_SERVICE register provides the Interrupt Controller's state information regarding which ISR priority levels are currently in service by the processor. This is provided for debug purposes only.

INTCTL5_IN_SERVICE

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL7	0x1: In service 0x0: Not in service
6	LEVEL6	0x1: In service 0x0: Not in service
5	LEVEL5	0x1: In service 0x0: Not in service
4	LEVEL4	0x1: In service 0x0: Not in service
3	LEVEL3	0x1: In service 0x0: Not in service
2	LEVEL2	0x1: In service 0x0: Not in service
1	LEVEL1	0x1: In service 0x0: Not in service
0	LEVEL0	0x1: In service 0x0: Not in service

0x121028E4 INTCTL5_IN_STACK

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_STACK register provides the Interrupt Controller's state information regarding which ISR priority levels are currently nested (stacked) in the CPU. This is provided for debug purposes only.

INTCTL5_IN_STACK

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL6	0x1: Nested 0x0: Not nested
6	LEVEL5	0x1: Nested 0x0: Not nested
5	LEVEL4	0x1: Nested 0x0: Not nested
4	LEVEL3	0x1: Nested 0x0: Not nested
3	LEVEL2	0x1: Nested 0x0: Not nested
2	LEVEL1	0x1: Nested 0x0: Not nested
1	LEVEL0	0x1: Nested 0x0: Not nested
0	MAIN	0x1: Nested 0x0: Not nested

0x121028E8 INTCTL5_TEST_BUS_SEL

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

Select signals to be directed to Interrupt Controller test_bus 32-bit output port.

INTCTL5_TEST_BUS_SEL

Bits	Name	Description
31:2	RESERVED	
1:0	SEL	NOTE The Interrupt Controller may have as few as 33 interrupts. Setting to HIGH_INTS will not have meaning if there are less than 61 interrupt inputs. 0x0: NONE (output 0x0) 0x1: LOW_INTS (31 - IRQn, 30 - FIQn, intsource[29:0]) 0x2: MID_INTS (31 - IRQn, 30 - FIQn, pad 0 as needed, intsource[N up to 59:30]) 0x3: HIGH_INTS (31 - IRQn, 30 - FIQn, 28 bits 0, intsource[63:60])

0x121028EC INTCTL5_INT_CTL_CONFIG

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

The INT_CTL_CONFIG register provides additional configuration options for the interrupt controller used for debug purposes.

INTCTL5_INT_CTL_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_1	
0	NO_NESTING_MODE	Default : 0 This register bit is used to configure the interrupt controller before any interrupts occur. When this bit is cleared (0), the PIC priority logic is used to determine when to assert irq_n. When the software allows hardware interrupt nesting, this bit should be cleared (0). If this bit is set (1), irq_n is asserted whenever there is at least one bit set in IRQ_STATUS. This bit should be set (1) right after power up if the software does not need any hardware nesting functions. 0x0: NESTED 0x1: NOT NESTED

20.11 Interrupt Controller 6 Registers (0x12103000 INTCTL6_BASE)

This section contains Interrupt Controller 6 registers.

20.11.1 IConfiguration registers

These registers are used to configure the Interrupt Controller

0x12103000 INTCTL6_INT_SELECT_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_0 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL6_INT_SELECT_0

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12103004 INTCTL6_INT_SELECT_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_1 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL6_INT_SELECT_1

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12103010 INTCTL6_INT_ENABLE_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_0 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor.

INTCTL6_INT_ENABLE_0

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12103014 INTCTL6_INT_ENABLE_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_1 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor

INTCTL6_INT_ENABLE_1

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12103020 INTCTL6_INT_ENABLE_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_0 register is used to clear (to 0) the bits of the INT_ENABLE_0 register.

INTCTL6_INT_ENABLE_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear.

0x12103024 INTCTL6_INT_ENABLE_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_1 register is used to clear (to 0) the bits of the INT_ENABLE_1 register.

INTCTL6_INT_ENABLE_CLEAR_1

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Clear.

0x12103030 INTCTL6_INT_ENABLE_SET_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_0 register is used to set (to 1) the bits of the INT_ENABLE_0 register.

INTCTL6_INT_ENABLE_SET_0

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Set.

0x12103034 INTCTL6_INT_ENABLE_SET_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_1 register is used to set (to 1) the bits of the INT_ENABLE_1 register.

INTCTL6_INT_ENABLE_SET_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Set.

0x12103040 INTCTL6_INT_TYPE_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL6_INT_TYPE_0

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12103044 INTCTL6_INT_TYPE_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL6_INT_TYPE_1

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12103050 INTCTL6_INT_POLARITY_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL6_INT_POLARITY_0

Bits	Name	Description
31:0	POL	0x1: neg 0x0: pos

0x12103054 INTCTL6_INT_POLARITY_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL6_INT_POLARITY_1

Bits	Name	Description
31:0	POL	0x1: neg 0x0: posl

0x12103060 INTCTL6_NO_PEND_VAL

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

The NO_PEND_VALUE indicates the 32-bit value returned when reading VEC_RD or PEND_RD when there is no available interrupt. The reset value is the traditional indicator of no pending interrupt. It is convenient to refer to this value as the NULL interrupt.

When using the Interrupt Controller in Vector Mode, it may be useful to set this register to a value where software can jump to perform common end of ISR handling.

INTCTL6_NO_PEND_VAL

Bits	Name	Description
31:0	NULL_VALUE	This value is returned when VEC_RD or PEND_RD when there is no available interrupt

0x12103064 INTCTL6_MASTER_ENABLE

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The MASTER_ENABLE register is the IRQ and FIQ master enable register. The two bits in this register can be used to block the IRQ and/or FIQ signals from reaching the processor. These enables are used to gate off the interrupt signals at IRQ_STATUS and FIQ_STATUS. This will cause irq_n and fiq_n de-asserted if they were previously asserted and stay de-asserted. Note that if a Vector Port transaction has started, it will complete with irq_n still held asserted by the Vector Port logic.

Writing this register has no affect on the INT_ENABLE register.

NOTE The RAW_STATUS register will hold interrupts that have been detected by the Interrupt Controller even if disabled by INT_ENABLE.

INTCTL6_MASTER_ENABLE

Bits	Name	Description
1	FIQ_ENABLE	0x0: Disable 0x1: Enable.
0	IRQ_ENABLE	0x0: Disable 0x1: Enable.

0x12103068 INTCTL6_VIC_CONFIG

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The VIC_CONFIG register is used to enable Vector Port interface.

INTCTL6_VIC_CONFIG

Bits	Name	Description
0	VECTOR_MODE	0x1: Enable 0x0: Disable

0x1210306C INTCTL6_SECURITY

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The SECURITY register is used to enable or disable non-secure bus transactions. The bus security status is signaled to the Interrupt Controller via the ns pin. When ns is set to 0 the state of the SECURITY register is not considered - a secure transaction is allowed if the device is set to non-secure mode. When ns is set to 1, the SECURITY register's SECURE bit must be 0 for access to be granted. If set to 1, the non-secure (ns) transaction is denied. When access is denied, a write is ignored, and a read will return 0x0. No error is signaled.

INTCTL6_SECURITY

Bits	Name	Description
0	SECURE	When enabled, only secure agents can access the registers. When disabled, both secure and non-secure agents can access the registers. 0x1: Enable 0x0: Disable

0x12103200+4*n INTCTL6_PRIORITYn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x0

The PRIORITYn registers are used to determine the priority for each interrupt source.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

NOTE Only IRQs are prioritized. Thus PRIORITYn registers have no affect on FIQ.

INTCTL6_PRIORITYn

Bits	Name	Description
2:0	PRIORITY	Priority for each interrupt source.

0x12103400+4*n INTCTL6_VECT_ADDRn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: NA

The VECT_ADDRn registers provide the vector handle address for each interrupt source N.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

INTCTL6_VECT_ADDRn

Bits	Name	Description
31:2	ADDR	Vector handle (the ISR's starting address) for interrupt source n

INTCTL6_VECT_ADDRn (cont.)

Bits	Name	Description
1:0	RESERVED_BITS1_0	

20.11.2 Operational registers

0x12103080 INTCTL6_IRQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_0 shows which interrupt sources zero to 31 designated for irq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_0.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL6_IRQ_STATUS_0

Bits	Name	Description
31	INT_SRC31	See bit 0's description.
30	INT_SRC30	
29	INT_SRC29	
28	INT_SRC28	
27	INT_SRC27	
26	INT_SRC26	
25	INT_SRC25	
24	INT_SRC24	
23	INT_SRC23	
22	INT_SRC22	
21	INT_SRC21	
20	INT_SRC20	
19	INT_SRC19	
18	INT_SRC18	
17	INT_SRC17	
16	INT_SRC16	
15	INT_SRC15	

INTCTL6_IRQ_STATUS_0 (cont.)

Bits	Name	Description
14	INT_SRC14	
13	INT_SRC13	
12	INT_SRC12	
11	INT_SRC11	
10	INT_SRC10	
9	INT_SRC9	
8	INT_SRC8	
7	INT_SRC7	
6	INT_SRC6	
5	INT_SRC5	
4	INT_SRC4	
3	INT_SRC3	
2	INT_SRC2	
1	INT_SRC1	
0	INT_SRC0	Data for interrupt source bit 0 0x1: active 0x0: inactive

0x12103084 INTCTL6_IRQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_1 shows which interrupt sources 32 to 63 designated for irq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_1.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL6_IRQ_STATUS_1

Bits	Name	Description
31	INT_SRC63	See bit 0's description
30	INT_SRC62	
29	INT_SRC61	

INTCTL6_IRQ_STATUS_1 (cont.)

Bits	Name	Description
28	INT_SRC60	
27	INT_SRC59	
26	INT_SRC58	
25	INT_SRC57	
24	INT_SRC56	
23	INT_SRC55	
22	INT_SRC54	
21	INT_SRC53	
20	INT_SRC52	
19	INT_SRC51	
18	INT_SRC50	
17	INT_SRC49	
16	INT_SRC48	
15	INT_SRC47	
14	INT_SRC46	
13	INT_SRC45	
12	INT_SRC44	
11	INT_SRC43	
10	INT_SRC42	
9	INT_SRC41	
8	INT_SRC40	
7	INT_SRC39	
6	INT_SRC38	
5	INT_SRC37	
4	INT_SRC36	
3	INT_SRC35	
2	INT_SRC34	
1	INT_SRC33	
0	INT_SRC32	Data for interrupt source bit 32 0x1: active 0x0: inactive

0x12103090 INTCTL6_FIQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_0 shows which interrupt sources zero to 31 designated for fiq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_0.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL6_FIQ_STATUS_0

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_0 fields

0x12103094 INTCTL6_FIQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_1 shows which interrupt sources 32 to 63 designated for fiq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_1.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL6_FIQ_STATUS_1

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_1 fields

0x121030A0 INTCTL6_RAW_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_0 shows which interrupt sources zero to 31 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_0. Bits set in RAW_STATUS_0 are steered to generate irq_n or fiq_n by INT_SELECT_0 if enabled by both INT_ENABLE_0 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_0 by writing SOFT_INT_0.

INTCTL6_RAW_STATUS_0

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_0

0x121030A4 INTCTL6_RAW_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_1 shows which interrupt sources 32 to 63 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_1. Bits set in RAW_STATUS_1 are steered to generate irq_n or fiq_n by INT_SELECT_1 if enabled by both INT_ENABLE _1 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_1 by writing SOFT_INT_1.

INTCTL6_RAW_STATUS_1

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_1

0x121030B0 INTCTL6_INT_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_0 is used to clear bits in RAW_STATUS_0. For any bit written 0x1 to INT_CLEAR_0, the corresponding bit position is cleared in RAW_STATUS_0.

INTCTL6_INT_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121030B4 INTCTL6_INT_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_1 is used to clear bits in RAW_STATUS_1. For any bit written 0x1 to INT_CLEAR_1, the corresponding bit position is cleared in RAW_STATUS_1.

INTCTL6_INT_CLEAR_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121030C0 INTCTL6_SOFT_INT_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_0 is used to set bits in RAW_STATUS_0 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_0, the corresponding bit position is set in RAW_STATUS_0.

INTCTL6_SOFT_INT_0

Bits	Name	Description
31:0	SW_INT	0x0: Do nothing 0x1: Set

0x121030C4 INTCTL6_SOFT_INT_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_1 is used to set bits in RAW_STATUS_1 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_1, the corresponding bit position is set in RAW_STATUS_1.

INTCTL6_SOFT_INT_1

Bits	Name	Description
31:0	SW_INT	See IRQ_STATUS_1 for bit map. 0x0: Do nothing 0x1: Set

0x121030D0 INTCTL6_VEC_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack PUSH in the PIC, and if an interrupt is causing irq_n returns it.

Assuming an interrupt is available and irq_n is asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU has seen irq_n.
- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine.
- The PIC will set a bit in IN_STACK for the sw level that has been interrupted (including "main").
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that caused the irq_n.
- Subsequently irq_n may only be asserted for an interrupt source designated at a higher priority level than the highest priority level indicated by IN_SERVICE.

If irq_n is asserted, the value returned when reading VEC_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If irq_n is not asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When the Interrupt Controller is in Vector Mode, as designated by VIC_CONFIG, VEC_RD should not be read. The controller still needs to be informed that the CPU is taking the interrupt. This is done by a Vector Port transaction. However, if VEC_RD is read in while in Vector Mode, the read will have the same effect as in PIC mode. However, the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE Using this register while the system is in Vector Mode may not be reliable as CPU hardware may initiate a Vector Port transaction while launching the read transaction to VEC_RD. This race condition could have undesirable results.

INTCTL6_VEC_RD

Bits	Name	Description
31:0	INDEX	Reading from this register provides the index of the current interrupt selected by the PIC, and indicates to the priority hardware that the interrupt is being serviced. Though the practice is not recommended, if this register is read in Vector Mode, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to VEC_RD. The commanded PUSH is performed. If irq_n is not currently active, reading this register returns the value stored in NO_PEND_VAL. There are no side effects in this case - the commanded PUSH is not performed.

0x121030D4 INTCTL6_PEND_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack POP in the PIC, and if an interrupt is pending returns it.

Assuming an interrupt is available and irq_n is not asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine, and ending the previous ISR routine.
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that is now starting.
- The PIC will clear the most significant bit found set in IN_SERVICE for the priority of the interrupt ISR routine just ended if the priority of the interrupt now starting is different.

If an interrupt is available and irq_n is asserted or if no interrupt is available the PIC will behave as if the VEC_WR command register was written. That is, the command issued to the PIC will be interpreted as a POP.

The value returned when reading PEND_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If no interrupt is asserted or if irq_n is asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When Vector Mode is enabled, unlike the VEC_RD register, PEND_RD must be read in order to inform the PIC that the ISR has finished processing. There is no equivalent

Vector Port transaction. When not in Vector Mode, the interrupts index (bit position) is returned.

NOTE In Vector Mode the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE VEC_WR can be substituted for PEND_RD to inform the PIC that the ISR has finished processing without returning a pending interrupt.

INTCTL6_PEND_RD

Bits	Name	Description
31:0	HANDLE	Reading from this register provides the index of the current interrupt selected by the PIC as a pending interrupt. It also indicates to the priority hardware that the current ISR is finished, and if an interrupt is pending that a new ISR is starting. In Vector Mode, when an interrupt is pending, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to PEND_RD. The commanded POP is performed. If an interrupt is not pending, reading this register returns the value stored in NO_PEND_VAL. The commanded POP is still performed.

0x121030D8 INTCTL6_VEC_WR

Type: Write (command)
Clock: INT_CTL_CLK
Reset State: NA

This is a write command register. It affects a logical stack POP in the PIC without returning any (possibly) pending interrupt. The resulting state of the PIC is to request a new irq_n if any bits are set in IRQ_STATUS.

Writing this register has the following side effects:

- Informs the PIC logic that the CPU is ending the current ISR routine.
- The PIC will clear the most significant bit found set in IN_SERVICE.
- The PIC will clear the most significant bit found set in IN_STACK.

NOTE PEND_RD can be substituted for VEC_WR to inform the PIC that the ISR has finished processing and to return a pending interrupt at the same time.

INTCTL6_VEC_WR

Bits	Name	Description
31:0	RESERVED	Data written is not used.

20.11.3 Debug and legacy registers

0x121030E0 INTCTL6_IN_SERVICE

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_SERVICE register provides the Interrupt Controller's state information regarding which ISR priority levels are currently in service by the processor. This is provided for debug purposes only.

INTCTL6_IN_SERVICE

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL7	0x1: In service 0x0: Not in service
6	LEVEL6	0x1: In service 0x0: Not in service
5	LEVEL5	0x1: In service 0x0: Not in service
4	LEVEL4	0x1: In service 0x0: Not in service
3	LEVEL3	0x1: In service 0x0: Not in service
2	LEVEL2	0x1: In service 0x0: Not in service
1	LEVEL1	0x1: In service 0x0: Not in service
0	LEVEL0	0x1: In service 0x0: Not in service

0x121030E4 INTCTL6_IN_STACK

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_STACK register provides the Interrupt Controller's state information regarding which ISR priority levels are currently nested (stacked) in the CPU. This is provided for debug purposes only.

INTCTL6_IN_STACK

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL6	0x1: Nested 0x0: Not nested
6	LEVEL5	0x1: Nested 0x0: Not nested
5	LEVEL4	0x1: Nested 0x0: Not nested
4	LEVEL3	0x1: Nested 0x0: Not nested
3	LEVEL2	0x1: Nested 0x0: Not nested
2	LEVEL1	0x1: Nested 0x0: Not nested
1	LEVEL0	0x1: Nested 0x0: Not nested
0	MAIN	0x1: Nested 0x0: Not nested

0x121030E8 INTCTL6_TEST_BUS_SEL

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

Select signals to be directed to Interrupt Controller test_bus 32-bit output port.

INTCTL6_TEST_BUS_SEL

Bits	Name	Description
31:2	RESERVED	
1:0	SEL	NOTE The Interrupt Controller may have as few as 33 interrupts. Setting to HIGH_INTS will not have meaning if there are less than 61 interrupt inputs. 0x0: NONE (output 0x0) 0x1: LOW_INTS (31 - IRQn, 30 - FIQn, intsource[29:0]) 0x2: MID_INTS (31 - IRQn, 30 - FIQn, pad 0 as needed, intsource[N up to 59:30]) 0x3: HIGH_INTS (31 - IRQn, 30 - FIQn, 28 bits 0, intsource[63:60])

0x121030EC INTCTL6_INT_CTL_CONFIG

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

The INT_CTL_CONFIG register provides additional configuration options for the interrupt controller used for debug purposes.

INTCTL6_INT_CTL_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_1	
0	NO_NESTING_MODE	Default : 0 This register bit is used to configure the interrupt controller before any interrupts occur. When this bit is cleared (0), the PIC priority logic is used to determine when to assert irq_n. When the software allows hardware interrupt nesting, this bit should be cleared (0). If this bit is set (1), irq_n is asserted whenever there is at least one bit set in IRQ_STATUS. This bit should be set (1) right after power up if the software does not need any hardware nesting functions. 0x0: NESTED 0x1: NOT NESTED

20.12 Interrupt Controller 7 Registers (0x12103800 INTCTL7_BASE)

This section contains Interrupt Controller 7 registers.

20.12.1 Configuration registers

These registers are used to configure the Interrupt Controller

0x12103800 INTCTL7_INT_SELECT_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_0 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL7_INT_SELECT_0

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12103804 INTCTL7_INT_SELECT_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_SELECT_1 register selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt.

INTCTL7_INT_SELECT_1

Bits	Name	Description
31:0	SELECT	Selects whether the corresponding interrupt source generates an FIQ or IRQ interrupt. 0x0: IRQ interrupt 0x1: FIQ interrupt

0x12103810 INTCTL7_INT_ENABLE_0

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_0 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor.

INTCTL7_INT_ENABLE_0

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12103814 INTCTL7_INT_ENABLE_1

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_ENABLE_1 register enables interrupts sources to generate either an IRQ or an FIQ interrupt to the processor

INTCTL7_INT_ENABLE_1

Bits	Name	Description
31:0	ENABLE	0x0: Disable 0x1: Enable

0x12103820 INTCTL7_INT_ENABLE_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_0 register is used to clear (to 0) the bits of the INT_ENABLE_0 register.

INTCTL7_INT_ENABLE_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear.

0x12103824 INTCTL7_INT_ENABLE_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_CLEAR_1 register is used to clear (to 0) the bits of the INT_ENABLE_1 register.

INTCTL7_INT_ENABLE_CLEAR_1

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Clear.

0x12103830 INTCTL7_INT_ENABLE_SET_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_0 register is used to set (to 1) the bits of the INT_ENABLE_0 register.

INTCTL7_INT_ENABLE_SET_0

Bits	Name	Description
31:0	SET	0x0: Do nothing 0x1: Set.

0x12103834 INTCTL7_INT_ENABLE_SET_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

The INT_ENABLE_SET_1 register is used to set (to 1) the bits of the INT_ENABLE_1 register.

INTCTL7_INT_ENABLE_SET_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Set.

0x12103840 INTCTL7_INT_TYPE_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL7_INT_TYPE_0

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12103844 INTCTL7_INT_TYPE_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_TYPE_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL7_INT_TYPE_1

Bits	Name	Description
31:0	SRC_TYPE	0x1: Edge 0x0: Level

0x12103850 INTCTL7_INT_POLARITY_0

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_0 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL7_INT_POLARITY_0

Bits	Name	Description
31:0	POL	0x1: neg 0x0: pos

0x12103854 INTCTL7_INT_POLARITY_1

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x00000000

The INT_POLARITY_1 register determines whether the corresponding interrupt is detected on a rising edge or is detected when asserted high, edge or level sensitive respectively.

INTCTL7_INT_POLARITY_1

Bits	Name	Description
31:0	POL	0x1: neg 0x0: posl

0x12103860 INTCTL7_NO_PEND_VAL

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

The NO_PEND_VALUE indicates the 32-bit value returned when reading VEC_RD or PEND_RD when there is no available interrupt. The reset value is the traditional indicator of no pending interrupt. It is convenient to refer to this value as the NULL interrupt.

When using the Interrupt Controller in Vector Mode, it may be useful to set this register to a value where software can jump to perform common end of ISR handling.

INTCTL7_NO_PEND_VAL

Bits	Name	Description
31:0	NULL_VALUE	This value is returned when VEC_RD or PEND_RD when there is no available interrupt

0x12103864 INTCTL7_MASTER_ENABLE

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The MASTER_ENABLE register is the IRQ and FIQ master enable register. The two bits in this register can be used to block the IRQ and/or FIQ signals from reaching the processor. These enables are used to gate off the interrupt signals at IRQ_STATUS and FIQ_STATUS. This will cause irq_n and fiq_n de-asserted if they were previously asserted and stay de-asserted. Note that if a Vector Port transaction has started, it will complete with irq_n still held asserted by the Vector Port logic.

Writing this register has no affect on the INT_ENABLE register.

NOTE The RAW_STATUS register will hold interrupts that have been detected by the Interrupt Controller even if disabled by INT_ENABLE.

INTCTL7_MASTER_ENABLE

Bits	Name	Description
1	FIQ_ENABLE	0x0: Disable 0x1: Enable.
0	IRQ_ENABLE	0x0: Disable 0x1: Enable.

0x12103868 INTCTL7_VIC_CONFIG

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The VIC_CONFIG register is used to enable Vector Port interface.

INTCTL7_VIC_CONFIG

Bits	Name	Description
0	VECTOR_MODE	0x1: Enable 0x0: Disable

0x1210386C INTCTL7_SECURITY

Type: Read/write
Clock: INT_CTL_CLK
Reset State: 0x0

The SECURITY register is used to enable or disable non-secure bus transactions. The bus security status is signaled to the Interrupt Controller via the ns pin. When ns is set to 0 the state of the SECURITY register is not considered - a secure transaction is allowed if the device is set to non-secure mode. When ns is set to 1, the SECURITY register's SECURE bit must be 0 for access to be granted. If set to 1, the non-secure (ns) transaction is denied. When access is denied, a write is ignored, and a read will return 0x0. No error is signaled.

INTCTL7_SECURITY

Bits	Name	Description
0	SECURE	When enabled, only secure agents can access the registers. When disabled, both secure and non-secure agents can access the registers. 0x1: Enable 0x0: Disable

0x12103A00+ 4*n INTCTL7_PRIORITYn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: 0x0

The PRIORITYn registers are used to determine the priority for each interrupt source.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

NOTE Only IRQs are prioritized. Thus PRIORITYn registers have no affect on FIQ.

INTCTL7_PRIORITYn

Bits	Name	Description
2:0	PRIORITY	Priority for each interrupt source.

0x12103C00+ 4*n INTCTL7_VECT_ADDRn, n=[0..63]

Type: Read/Write
Clock: INT_CTL_CLK
Reset State: NA

The VECT_ADDRn registers provide the vector handle address for each interrupt source N.

NOTE N-1 in the array definition (not "n") needs to be replaced with the number of interrupts (minus one) required by the system. System designers using the Interrupt Controller must copy and update this document in order to use QCT's address generation scripts.

INTCTL7_VECT_ADDRn

Bits	Name	Description
31:2	ADDR	Vector handle (the ISR's starting address) for interrupt source n

INTCTL7_VECT_ADDRn (cont.)

Bits	Name	Description
1:0	RESERVED_BITS1_0	

20.12.2 Operational registers

0x12103880 INTCTL7_IRQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_0 shows which interrupt sources zero to 31 designated for irq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_0.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL7_IRQ_STATUS_0

Bits	Name	Description
31	INT_SRC31	See bit 0's description.
30	INT_SRC30	
29	INT_SRC29	
28	INT_SRC28	
27	INT_SRC27	
26	INT_SRC26	
25	INT_SRC25	
24	INT_SRC24	
23	INT_SRC23	
22	INT_SRC22	
21	INT_SRC21	
20	INT_SRC20	
19	INT_SRC19	
18	INT_SRC18	
17	INT_SRC17	
16	INT_SRC16	
15	INT_SRC15	

INTCTL7_IRQ_STATUS_0 (cont.)

Bits	Name	Description
14	INT_SRC14	
13	INT_SRC13	
12	INT_SRC12	
11	INT_SRC11	
10	INT_SRC10	
9	INT_SRC9	
8	INT_SRC8	
7	INT_SRC7	
6	INT_SRC6	
5	INT_SRC5	
4	INT_SRC4	
3	INT_SRC3	
2	INT_SRC2	
1	INT_SRC1	
0	INT_SRC0	Data for interrupt source bit 0 0x1: active 0x0: inactive

0x12103884 INTCTL7_IRQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

IRQ_STATUS_1 shows which interrupt sources 32 to 63 designated for irq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 0) are currently being held by RAW_STATUS_1.

The bits set in IRQ_STATUS form the inputs to the Interrupt Controller's priority encoder (PIC) logic and ultimately result in asserting irq_n to interrupt the CPU.

INTCTL7_IRQ_STATUS_1

Bits	Name	Description
31	INT_SRC63	See bit 0's description
30	INT_SRC62	
29	INT_SRC61	

INTCTL7_IRQ_STATUS_1 (cont.)

Bits	Name	Description
28	INT_SRC60	
27	INT_SRC59	
26	INT_SRC58	
25	INT_SRC57	
24	INT_SRC56	
23	INT_SRC55	
22	INT_SRC54	
21	INT_SRC53	
20	INT_SRC52	
19	INT_SRC51	
18	INT_SRC50	
17	INT_SRC49	
16	INT_SRC48	
15	INT_SRC47	
14	INT_SRC46	
13	INT_SRC45	
12	INT_SRC44	
11	INT_SRC43	
10	INT_SRC42	
9	INT_SRC41	
8	INT_SRC40	
7	INT_SRC39	
6	INT_SRC38	
5	INT_SRC37	
4	INT_SRC36	
3	INT_SRC35	
2	INT_SRC34	
1	INT_SRC33	
0	INT_SRC32	Data for interrupt source bit 32 0x1: active 0x0: inactive

0x12103890 INTCTL7_FIQ_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_0 shows which interrupt sources zero to 31 designated for fiq_n by INT_SELECT_0 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_0.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL7_FIQ_STATUS_0

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_0 fields

0x12103894 INTCTL7_FIQ_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

FIQ_STATUS_1 shows which interrupt sources 32 to 63 designated for fiq_n by INT_SELECT_1 and enabled by both INT_ENABLE and MASTER_ENABLE (bit 1) are currently being held by RAW_STATUS_1.

The bits set in FIQ_STATUS generate fiq_n to interrupt the CPU.

INTCTL7_FIQ_STATUS_1

Bits	Name	Description
31:0	INT_SRC	Same as IRQ_STATUS_1 fields

0x121038A0 INTCTL7_RAW_STATUS_0

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_0 shows which interrupt sources zero to 31 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_0. Bits set in RAW_STATUS_0 are steered to generate irq_n or fiq_n by INT_SELECT_0 if enabled by both INT_ENABLE_0 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_0 by writing SOFT_INT_0.

INTCTL7_RAW_STATUS_0

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_0

0x121038A4 INTCTL7_RAW_STATUS_1

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

RAW_STATUS_1 shows which interrupt sources 32 to 63 have been detected by the input edge or level detection logic. Interrupt sources are designated for edge or level by INT_TYPE_1. Bits set in RAW_STATUS_1 are steered to generate irq_n or fiq_n by INT_SELECT_1 if enabled by both INT_ENABLE _1 and MASTER_ENABLE.

Software may choose to set one or more bits in RAW_STATUS_1 by writing SOFT_INT_1.

INTCTL7_RAW_STATUS_1

Bits	Name	Description
31:0	STATUS	See IRQ_STATUS_1

0x121038B0 INTCTL7_INT_CLEAR_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_0 is used to clear bits in RAW_STATUS_0. For any bit written 0x1 to INT_CLEAR_0, the corresponding bit position is cleared in RAW_STATUS_0.

INTCTL7_INT_CLEAR_0

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121038B4 INTCTL7_INT_CLEAR_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing INT_CLEAR_1 is used to clear bits in RAW_STATUS_1. For any bit written 0x1 to INT_CLEAR_1, the corresponding bit position is cleared in RAW_STATUS_1.

INTCTL7_INT_CLEAR_1

Bits	Name	Description
31:0	CLEAR	0x0: Do nothing 0x1: Clear

0x121038C0 INTCTL7_SOFT_INT_0

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_0 is used to set bits in RAW_STATUS_0 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_0, the corresponding bit position is set in RAW_STATUS_0.

INTCTL7_SOFT_INT_0

Bits	Name	Description
31:0	SW_INT	0x0: Do nothing 0x1: Set

0x121038C4 INTCTL7_SOFT_INT_1

Type: Write (Command)
Clock: INT_CTL_CLK
Reset State: NA

Writing SOFT_INT_1 is used to set bits in RAW_STATUS_1 for EDGE detected interrupts. For any bit written 0x1 to SOFT_INT_1, the corresponding bit position is set in RAW_STATUS_1.

INTCTL7_SOFT_INT_1

Bits	Name	Description
31:0	SW_INT	See IRQ_STATUS_1 for bit map. 0x0: Do nothing 0x1: Set

0x121038D0 INTCTL7_VEC_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack PUSH in the PIC, and if an interrupt is causing irq_n returns it.

Assuming an interrupt is available and irq_n is asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU has seen irq_n.
- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine.
- The PIC will set a bit in IN_STACK for the sw level that has been interrupted (including "main").
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that caused the irq_n.
- Subsequently irq_n may only be asserted for an interrupt source designated at a higher priority level than the highest priority level indicated by IN_SERVICE.

If irq_n is asserted, the value returned when reading VEC_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If irq_n is not asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When the Interrupt Controller is in Vector Mode, as designated by VIC_CONFIG, VEC_RD should not be read. The controller still needs to be informed that the CPU is taking the interrupt. This is done by a Vector Port transaction. However, if VEC_RD is read in while in Vector Mode, the read will have the same effect as in PIC mode. However, the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE Using this register while the system is in Vector Mode may not be reliable as CPU hardware may initiate a Vector Port transaction while launching the read transaction to VEC_RD. This race condition could have undesirable results.

INTCTL7_VEC_RD

Bits	Name	Description
31:0	INDEX	Reading from this register provides the index of the current interrupt selected by the PIC, and indicates to the priority hardware that the interrupt is being serviced. Though the practice is not recommended, if this register is read in Vector Mode, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to VEC_RD. The commanded PUSH is performed. If irq_n is not currently active, reading this register returns the value stored in NO_PEND_VAL. There are no side effects in this case - the commanded PUSH is not performed.

0x121038D4 INTCTL7_PEND_RD

Type: Read
Clock: INT_CTL_CLK
Reset State: 0xFFFFFFFF

This is a read command register. It affects a logical stack POP in the PIC, and if an interrupt is pending returns it.

Assuming an interrupt is available and irq_n is not asserted, reading this register has the following side effects:

- Informs the PIC logic that the CPU is taking the interrupt.
- Informs the PIC logic that the CPU is starting to process the ISR routine, and ending the previous ISR routine.
- The PIC will set a bit in IN_SERVICE for the priority for the interrupt that is now starting.
- The PIC will clear the most significant bit found set in IN_SERVICE for the priority of the interrupt ISR routine just ended if the priority of the interrupt now starting is different.

If an interrupt is available and irq_n is asserted or if no interrupt is available the PIC will behave as if the VEC_WR command register was written. That is, the command issued to the PIC will be interpreted as a POP.

The value returned when reading PEND_RD is the interrupt index (0..N-1) of the highest priority interrupt of those currently available (set 1) in IRQ_STATUS. If no interrupt is asserted or if irq_n is asserted, the value stored in NO_PEND_VAL is returned instead.

NOTE When Vector Mode is enabled, unlike the VEC_RD register, PEND_RD must be read in order to inform the PIC that the ISR has finished processing. There is no equivalent

Vector Port transaction. When not in Vector Mode, the interrupts index (bit position) is returned.

NOTE In Vector Mode the value returned will be the result of reading the Vector Address Table addressed by the interrupt index.

NOTE VEC_WR can be substituted for PEND_RD to inform the PIC that the ISR has finished processing without returning a pending interrupt.

INTCTL7_PEND_RD

Bits	Name	Description
31:0	HANDLE	Reading from this register provides the index of the current interrupt selected by the PIC as a pending interrupt. It also indicates to the priority hardware that the current ISR is finished, and if an interrupt is pending that a new ISR is starting. In Vector Mode, when an interrupt is pending, the index of the current interrupt is used as the address to read VECT_ADDRn. The result of that read is the data returned for the read to PEND_RD. The commanded POP is performed. If an interrupt is not pending, reading this register returns the value stored in NO_PEND_VAL. The commanded POP is still performed.

0x121038D8 INTCTL7_VEC_WR

Type: Write (command)
Clock: INT_CTL_CLK
Reset State: NA

This is a write command register. It affects a logical stack POP in the PIC without returning any (possibly) pending interrupt. The resulting state of the PIC is to request a new irq_n if any bits are set in IRQ_STATUS.

Writing this register has the following side effects:

- Informs the PIC logic that the CPU is ending the current ISR routine.
- The PIC will clear the most significant bit found set in IN_SERVICE.
- The PIC will clear the most significant bit found set in IN_STACK.

NOTE PEND_RD can be substituted for VEC_WR to inform the PIC that the ISR has finished processing and to return a pending interrupt at the same time.

INTCTL7_VEC_WR

Bits	Name	Description
31:0	RESERVED	Data written is not used.

20.12.3 Debug and legacy registers

0x121038E0 INTCTL7_IN_SERVICE

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_SERVICE register provides the Interrupt Controller's state information regarding which ISR priority levels are currently in service by the processor. This is provided for debug purposes only.

INTCTL7_IN_SERVICE

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL7	0x1: In service 0x0: Not in service
6	LEVEL6	0x1: In service 0x0: Not in service
5	LEVEL5	0x1: In service 0x0: Not in service
4	LEVEL4	0x1: In service 0x0: Not in service
3	LEVEL3	0x1: In service 0x0: Not in service
2	LEVEL2	0x1: In service 0x0: Not in service
1	LEVEL1	0x1: In service 0x0: Not in service
0	LEVEL0	0x1: In service 0x0: Not in service

0x121038E4 INTCTL7_IN_STACK

Type: Read
Clock: INT_CTL_CLK
Reset State: 0x00000000

The IN_STACK register provides the Interrupt Controller's state information regarding which ISR priority levels are currently nested (stacked) in the CPU. This is provided for debug purposes only.

INTCTL7_IN_STACK

Bits	Name	Description
31:8	RESERVED_BITS31_8	
7	LEVEL6	0x1: Nested 0x0: Not nested
6	LEVEL5	0x1: Nested 0x0: Not nested
5	LEVEL4	0x1: Nested 0x0: Not nested
4	LEVEL3	0x1: Nested 0x0: Not nested
3	LEVEL2	0x1: Nested 0x0: Not nested
2	LEVEL1	0x1: Nested 0x0: Not nested
1	LEVEL0	0x1: Nested 0x0: Not nested
0	MAIN	0x1: Nested 0x0: Not nested

0x121038E8 INTCTL7_TEST_BUS_SEL

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

Select signals to be directed to Interrupt Controller test_bus 32-bit output port.

INTCTL7_TEST_BUS_SEL

Bits	Name	Description
31:2	RESERVED	
1:0	SEL	NOTE The Interrupt Controller may have as few as 33 interrupts. Setting to HIGH_INTS will not have meaning if there are less than 61 interrupt inputs. 0x0: NONE (output 0x0) 0x1: LOW_INTS (31 - IRQn, 30 - FIQn, intsource[29:0]) 0x2: MID_INTS (31 - IRQn, 30 - FIQn, pad 0 as needed, intsource[N up to 59:30]) 0x3: HIGH_INTS (31 - IRQn, 30 - FIQn, 28 bits 0, intsource[63:60])

0x121038EC INTCTL7_INT_CTL_CONFIG

Type: Read/Write (Command)
Clock: INT_CTL_CLK
Reset State: 0x0

The INT_CTL_CONFIG register provides additional configuration options for the interrupt controller used for debug purposes.

INTCTL7_INT_CTL_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_1	
0	NO_NESTING_MODE	Default : 0 This register bit is used to configure the interrupt controller before any interrupts occur. When this bit is cleared (0), the PIC priority logic is used to determine when to assert irq_n. When the software allows hardware interrupt nesting, this bit should be cleared (0). If this bit is set (1), irq_n is asserted whenever there is at least one bit set in IRQ_STATUS. This bit should be set (1) right after power up if the software does not need any hardware nesting functions. 0x0: NESTED 0x1: NOT NESTED

20.13 SDC2_MCI_POWER (0x12140000 SDC2_BASE)

This section contains the SDC2 base registers.

0x12140000 SDC2_MCI_POWER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x00000000

(ARM name: MCIPower)

SDC2_MCI_POWER

Bits	Name	Description
31:7	RESERVED_1	Always reads zero. Writes 'don't care' but by convention write zero.
6	OPEN_DRAIN	MCICMD Output Control. See Note 2 below
5:1	RESERVED_2	Always reads zero. Writes 'don't care' by convention write zero.
0	CONTROL	This register is used to control the operation of the memory controller. value 0: power-off value 1: power-on Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_POWER register and before accessing this register again. Note:2 - This bit is reserved for the use mentioned in the Description but it is not implemented in HW. The open drain mode is preserved such that when enabled, the command output is driven low when the logic is low and undriven (so that the pull up can pull high) when the logic is high. Whether this gets used in the system is up to SW/system but the HW does support this mode.

0x12140004 SDC2_MCI_CLK

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x01008000

(ARM name: MCIClock)

SDC2_MCI_CLK

Bits	Name	Description
31:27	RESERVED_1	Always reads zero. Writes ’don’t care’ but by convention write zero.
26	SDCC_CLK_EXT_EN	Value 0 (default) - sdcc_clkout is driven via the clock pad and external clock can’t be used for testing the cm_dll_sdc4. Value 1- External clock can be used as a test clock.
25	RX_FLOW_TIMING	Configuration bit which selects the cycle which RxFlowControl will be asserted when UHS mode is used Value 0 (default) - RxFlowControl is asserted one clock before the end bit is received in DPSM (NextBlkTCnt in DPSM equals to 1). Value 1 - RxFlowControl is asserted two clocks before the end bit is received in DPSM (NextBlkTCnt in DPSM equals to 2).
24:23	SDC4_MCLK_SEL	Selects the sdc4_mclk - input clock of cm_dll_sdc4 Value 0 - gated version of MCLK Value 1 - feedback clock from CLK pad Value 2 (default) - free running mclk (gated between the transactions)
22	CLK_INV	When set(1), the input clock which is inserted into the input macros is inverted.
21	IO_PAD_PWR_SWITCH	Indication to Pad that power has to be switched from 3.3V to 1.8V.
20	CLK_FB_DLY_SEL	Selects the source of feedback clock used by the controller. Value 1 - output of cm_dll_sdc4 is used as feedback clock Value 0 - feedback clock from CLK pad is used
19:18	SD_DEV_SEL	Select the active device if more than one device are connected in shared bus mode. (range: ’00’ - ’11’).
17	HCLKON_SW_EN	SW enable of AHB clock request of SDCC4. value 0: HW clock request mechanism is used value 1: clock request signal is always high
16:14	SELECT_IN	Select to latch data and command coming in: value 000: on the falling edge of internal MCLK. value 001: on the rising edge of internal MCLK. value 010: using feedback clock (default). value 011: DDR mode - In DDR mode, the SDC_CLK output will be SDCn_APPS_CLK divided by 2. value 100: UHS mode - MCLK is used internally. value 101: UHS mode - divided frequency (MCLK/2) is used internally.
13	INVERT_OUT	Clear (0) to change data and command going out on the falling edge. Set (1) to change data and command going out on the rising edge.
12	FLOW_ENA	Enable flow control: value 0: disable (default) value 1: enable

SDC2_MCI_CLK (cont.)

Bits	Name	Description
11:10	WIDEBUS	Enable wide bus mode: value 00: 1 bit mode value 10: 4 bit mode value 01 or 11: 8 bit mode
9	PWRSAVE	Disable Prime-Cell MCI clock output when bus is idle to save power. value 0: Power save disabled - always enabled if bit 8 is set. value 1: Power save enabled - clock enabled only when bus is active and bit 8 is set.
8	ENABLE	Enable Prime-Cell MCI bus clock: value 0: clock disabled value 1: clock enabled
7:0	RESERVED_2	Always reads zero. Writes 'don't care' but by convention write zero. Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_CLK register and before accessing this register again.

0x12140008 SDC2_MCI_ARGUMENT

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC2_MCI_ARGUMENT

Bits	Name	Description
31:0	CMD_ARG	Command argument.

0x1214000C SDC2_MCI_CMD

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x00000000

(ARM name: MMCCommand) CPSM: 'Command Path State Machine'.

SDC2_MCI_CMD

Bits	Name	Description
31:17	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.

SDC2_MCI_CMD (cont.)

Bits	Name	Description
16	AUTO_CMD19	If set (1), CPSM sends CMD19 automatically before sending CMD17 or CMD18. This sequence is needed for CDR auto-calibration of cm_dll_sdc4.
15	CCS_DISABLE	If set (1), CPSM sends Command_Completion_Signal (CCS) disable sequence to the external CE-ATA device.
14	CCS_ENABLE	If set (1), CPSM waits for CCS from external card CE-ATA device.
13	MCIABORT	Signals the next command will be an abort (stop) command. This bit always read as (0) due to the hardware implementation. See note 2 below.
12	DAT_CMD	If set (1) indicates that this is a Command with Data. See note 2 below.
11	PROG_ENA	If set (1), PROG_DONE status bit will be asserted when busy is de-asserted. This bit is to be used with a stop or status command after a block write is performed. Does not effect CPSM.
10	ENABLE	The action of writing to this register (MCI_CMD) with this bit set (1), triggers CPSM to leave the 'Idle State'.
9	PENDING	If set (1), CPSM waits for 'CmdPend' from the DPSM before it starts sending a command. See note 3 below.
8	INTERRUPT	If set (1), CPSM disables command timer and waits for interrupt request (Card Response). See note 4 below.
7	LONGRSP	If set (1), receives a 136-bit long response.
6	RESPONSE	If set (1), CPSM waits for a response subject to INTERRUPT above.

SDC2_MCI_CMD (cont.)

Bits	Name	Description
5:0	CMD_INDEX	Command index. Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_CMD register and before accessing this register again. Note 2: These bits don't have any effect on the CPSM. They are used to signal the SDIO Interrupt state machine that a Multi Block (CMD18, CMD25, CMD53, etc.) data transaction is taking place. The DAT_CMD bit signals the start of the data transaction while the MCIABORT bit signals the end. For a pure SD Memory card, these bits are a 'don't care' and should be set to zero by convention. However, some software drivers may chose to manipulate the bits in order to maintain compatibility with Combo cards and/or pure SDIO cards. Note 3: This bit is designed to be used with SD CMD18 (READ_MULTIPLE_BLOCK) and SD CMD25 (WRITE_MULTIPLE_BLOCK) which must be terminated with a SD CMD12 (STOP_TRANSMISSION). After CMD18 or CMD25 is sent, the DPSM is enabled to send or receive data of amount MCI_DATA_LENGTH. After the DPSM finishes the transferring the data, it sends 'CmdPend' to the CPSM and goes idle. When the CPSM receives this signal, it sends the currently loaded command which software would normally establish as CMD12. Note 4: The START, CMD_INDEX, ARGUMENT, and CRC are a total of 48 bits in length. If the INTERRUPT bit is zero, the CPSM will wait (63-47) 16 MCLK ticks for a response before going back to IDLE. If the INTERRUP bit is set, the CPSM will wait indefinitely for a card response.

0x12140010 SDC2_MCI_RESP_CMD

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIRespCmd)

SDC2_MCI_RESP_CMD

Bits	Name	Description
31:6	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
5:0	RESPCMD	Response command index.

0x12140014+4*n SDC2_MCI_RESPn, n=[0..3]

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIResponse0-3). Note that MCIResponse3 has 31 bits; the other three (*RESP0, *RESP1, *RESP2) have 32 bits.

The card status size can be 32 or 127 bits, depending on the response type (see Table 1-2). The most significant bit of the card status is received first. The MCIResponse3 register LSB is always 0.

Table 20-2 Response type and card status size

Description	Short response	Long response
MCIResponse0	Card Status [31:0]	Card status [127:96]
MCIResponse1	Unused	Card status [95:64]
MCIResponse2	Unused	Card status [63:32]
MCIResponse3	Unused	Card status [31:1]

SDC2_MCI_RESPn

Bits	Name	Description
31:0	STATUS	Card status.

0x12140024 SDC2_MCI_DATA_TIMER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIDataTimer).

There is no way to disable this timer. The timer starts counting as soon as a transaction is initiated. The time counts in MCLK ticks.

SDC2_MCI_DATA_TIMER

Bits	Name	Description
31:0	DATA_TIME	Data timeout period.

0x12140028 SDC2_MCI_DATA_LENGTH

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIDataLength)

Total number of bytes in the transaction regardless of mode (stream or block). In block mode, must be an exact multiple of block size. During an infinite transfer the value of DATALENGTH should be programmed to 0.

SDC2_MCI_DATA_LENGTH

Bits	Name	Description
31:25	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
24:0	DATALENGTH	Data length value.

0x1214002C SDC2_MCI_DATA_CTL

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x00100000

(ARM name: MCIDataCtrl). Data Path State Machine (DPSM).

SDC2_MCI_DATA_CTL

Bits	Name	Description
31:22	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
21	SW_SDC4_CMD19	The input of cm_dll_sdc4 - sdc4_cmd19 can be driven by SW if AUTO_CMD19 (bit 16 in MCI_CMD) feature is not used. Value 1 - sdc4_cmd19 is driven by SW Value 0 (default) - sdc4_cmd19 is driven by HW
20	RX_DATA_PEND	If set (1), timeout counter will start counting only after the RX command (with data) was sent instead of counting from initialization of DPSM. The feature is enabled by default.

SDC2_MCI_DATA_CTL (cont.)

Bits	Name	Description
19	AUTO_PROG_DONE	If set (1), automatic detection of PROG_DONE condition is executed without sending CMD12, CMD13, CMD52 or any other 'dummy' command. SW should set this bit in the following cases only: 1. When sending CMD53 for SDIO write transaction. 2. When sending CMD24. 3. When sending CMD25 and CMD23 was issued before to inform card about the exact number of blocks to be written. 4. When sending CMD19 for testing bus procedure. CMD12 is not required in this case.
18	INFINITE_TRANSFER	If set (1), infinite transfer is enabled. MCI_DATA_LENGTH register should set to 0 during infinite transfer.
17	DATA_PEND	If set (1), DPSM waits for 'DataPend' from the CPSM before it enables the DPSM. See note 2 below.
16:4	BLOCKSIZE	Data block length in bytes (1 to 4096).
3	DM_ENABLE	Enable DM interface: 0: DM disabled 1: DM enabled
2	MODE	Data transfer mode: 0: block data transfer 1: stream data transfer
1	DIRECTION	Data transfer direction: 0: controller to card 1: card to controller
0	ENABLE	Data transfer enabled. If zero, DPSM unconditionally reset. Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_DATA_CTL register and before accessing this register again. Note 2: This bit is designed to be used with SD CMD24 and CMD25 (WRITE_SINGLE_BLOCK and WRITE_MULTIPLE_BLOCK) to automatically start the DPSM after a normal (non-error) response is received. This register should be written with the enable bit and the pending bit asserted before MCI_CMD is enabled.

0x12140030 SDC2_MCI_DATA_COUNT

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIDataCnt)

NOTE There is no mechanism to ensure that a read of this counter will be accurate as it is not synchronized. The reason being the value read is async to the clock domain in which the reading is done. It is only useful as a debug tool for diagnostic purposes only.

SDC2_MCI_DATA_COUNT

Bits	Name	Description
31:25	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
24:0	DATACOUNT	Value of data counter in MciDPSM block. Represents remaining data of transaction.

0x12140034 SDC2_MCI_STATUS

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x000C0000

(ARM name: MCIStatus)

This register may need exclusion for QCSR POR Test for bits 25 and 22.

Static[30:26], [24:23] and [10:0]

These remain asserted until they are cleared by writing to the appropriate bit in the Clear Register (see MCI_CLEAR)

XCIS

The means used to send the SDIO external-card-interrupt-signal (XCIS) to the SDCC depends on the transfer mode: 1-bit, 4-bit, or 8-bit. Under 1 bit transfer mode, the XCIS has a dedicated physical connection to the SDCC. Hence once it is asserted, it remain at a high level. Under 4 and 8 bit transfer modes, the XCIS is time multiplexed with physical connection data bit 1. The XCIS is recognized as valid during specific time slots on data bit 1 by the SDCC. How this 'recognition' takes places shows up as different behaviors on SDIO_INTR_OPER, SDIO_INTR, and the actual interrupt sent to the ARM through MCI_INT_MASKn.

Special[25]

The SDIO_INTR_OPER indicator reflects the true state of XCIS as it would be observed inside the external SDIO card. As such, there is no bit 25 in MCI_CLEAR. The only way to clear SDIO_INTR_OPER is to clear the appropriate bit in the external card Common Card Control Registers (CCCR). Like 'static' above and 'dynamic' below, bit 25 in MCI_INT_MASKn controls actually sending this indicator value to the ARM. This indicator of XCIS is used for normal SDCC operation.

Special[22]

The SDIO_INTR indicator reflects that there has been a low-to-high transition on the connection as explained under XCIS above. This indicator is cleared via bit 22 of MCI_CLEAR but any low-to-high transition on the connection will set this indicator again. Further note that this indicator is not routed through the MCI_INT_MASKn to the ARM. For bit 22, the raw value of the connection is routed through the MCI_INT_MASKn to the ARM. As this raw connection is not aware of 'specific time slots', the signal sent to the ARM generally toggles in an unpredictable fashion. This

is generally not useful during normal SDCC operation. However, for wake-up with clocks off, the raw connection is desirable.

Dynamic[21:11]

These change state depending on the state of the underlying logic (for example, FIFO full and empty flags are asserted and de-asserted as data while written to the FIFO).

SDC2_MCI_STATUS

Bits	Name	Description
31	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
30	AUTO_CMD19_TIMEOUT	Response or tuning pattern wasn't received after automatic CMD19's transmission. This status bit should be read only if AUTO_CMD19 (MCI_CMD(16)) was set.
29	BOOT_TIMEOUT	Data wasn't received within the valid time (according to MCI_CCS_TIMER) from the start of boot operation.
28	BOOT_ACK_ERR	Acknowledge pattern wasn't received correctly or not within the valid time (according to MCI_ACK_TIMER) from the start of boot operation.
27	BOOT_ACK_REC	Acknowledge pattern was received correctly.
26	CCS_TIMEOUT	CE-ATA Command Completion Signal timeout.
25	SDIO_INTR_OPER	SDIO interrupt indicator for normal operation.
24	ATA_CMD_COMPL	CE-ATA Command Completion Signal has been detected.
23	PROG_DONE	Programming done.
22	SDIO_INTR	SDIO interrupt indicator for wake-up.
21	RXDATA_AVLBL	Data available in receive FIFO. At least 1 word in the RX FIFO. SW can read 1 word only from the FIFO.
20	TXDATA_AVLBL	Data available in transmit FIFO. At least 1 word in the TX FIFO.
19	RXFIFO_EMPTY	Receive FIFO empty. SW can't read FIFO.
18	TXFIFO_EMPTY	Transmit FIFO empty. SW can write 8 words into the FIFO.
17	RXFIFO_FULL	Receive FIFO full. SW can read 8 words from the FIFO.
16	TXFIFO_FULL	Transmit FIFO full. TX FIFO contains 8 words. SW can't write to FIFO.
15	RXFIFO_HALF_FULL	Receive FIFO half full. SW can read 8 words from the FIFO.
14	TXFIFO_HALF_FULL	Transmit FIFO half full. SW can write 8 words into the FIFO.
13	RXACTIVE	Data receive in progress.
12	TXACTIVE	Data transmit in progress.
11	CMD_ACTIVE	Command transfer in progress.
10	DATA_BLK_END	Data block sent / received (CRC check passed).

SDC2_MCI_STATUS (cont.)

Bits	Name	Description
9	START_BIT_ERR	Start Bit Error flag
8	DATAEND	Data end (data counter is zero).
7	CMD_SENT	Command sent (no response required).
6	CMD_RESPONSE_END	Command response received (CRC check passed).
5	RX_OVERRUN	Receive FIFO overrun error.
4	TX_UNDERRUN	Transmit FIFO underrun error.
3	DATA_TIMEOUT	Data timeout.
2	CMD_TIMEOUT	Command response timeout.
1	DATA_CRC_FAIL	Data block sent / received (CRC check failed).
0	CMD_CRC_FAIL	Command response received (CRC check failed).

0x12140038 SDC2_MCI_CLEAR

Type: Write
Clock: SAME_RATE_AS_HCLK

(ARM name: MCIClear)

SDC2_MCI_CLEAR

Bits	Name	Description
31	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
30	AUTO_CMD19_TIMEOUT_CLR	Clears AUTO_CMD19_TIMEOUT flag.
29	BOOT_TIMEOUT_CLR	Clears BOOT_TIMEOUT flag.
28	BOOT_ACK_ERR_CLR	Clears BOOT_ACK_ERR flag.
27	BOOT_ACK_REC_CLR	Clears BOOT_ACK_REC flag.
26	CCS_TIMEOUT_CLR	Clears CCSTimeOut flag.
24	ATA_CMD_COMPL_CLR	Clears AtaCmdCompl flag.
23	PROG_DONE_CLR	Clears ProgDone flag.
22	SDIO_INTR_CLR	Clears SDIOInt flag.
10	DATA_BLK_END_CLR	Clears DataBlockEnd flag.
9	START_BIT_ERR_CLR	Clears StartBitErr flag.
8	DATA_END_CLR	Clears DataEnd flag.
7	CMD_SENT_CLR	Clears commandSent flag.

SDC2_MCI_CLEAR (cont.)

Bits	Name	Description
6	CMD_RESP_END_CLT	Clears CmdRespEnd flag.
5	RX_OVERRUN_CLR	Clears RxOverrunClr flag.
4	TX_UNDERRUN_CLR	Clears TxUnderrun flag.
3	DATA_TIMEOUT_CLR	Clears DataTimeOut flag.
2	CMD_TIMOUT_CLR	Clears CmdTimOutflag.
1	DATA_CRC_FAIL_CLR	Clears DataCrcFail flag.
0	CMD_CRC_FAIL_CLR	Clears CmdCrcFail flag.

0x1214003C+ 4*n SDC2_MCI_INT_MASKn, n=[0..1]

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIMask0, MCIMask1)

SDC2_MCI_INT_MASKn

Bits	Name	Description
31	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
30	MASK30	MASK AUTO_CMD19_TIMEOUT flag.
29	MASK29	MASK BOOT_TIMEOUT flag.
28	MASK28	MASK BOOT_ACK_ERR flag.
27	MASK27	MASK BOOT_ACK_REC flag.
26	MASK26	MASK CCSTimeOut flag.
25	MASK25	MASK SDIOIntOper flag.
24	MASK24	MASK AtaCmdCompl flag.
23	MASK23	MASK ProgDone flag.
22	MASK22	MASK SDIOInt flag.
21	MASK21	MASK RxDataAvlbl flag.
20	MASK20	MASK TxDataAvlbl flag.
19	MASK19	MASK RxFifoEmpty flag.
18	MASK18	MASK TxFifoEmpty flag.
17	MASK17	MASK RxFifoFull flag.
16	MASK16	MASK TxFifoFull flag.

SDC2_MCI_INT_MASKn (cont.)

Bits	Name	Description
15	MASK15	MASK RxFifoHalfFull flag.
14	MASK14	MASK TxFifoHalfFull flag.
13	MASK13	MASK RxActive flag.
12	MASK12	MASK TxActive flag.
11	MASK11	MASK CmdActive flag.
10	MASK10	MASK DataBlockEnd flag.
9	MASK9	MASK StartBitErr
8	MASK8	MASK DataEnd flag.
7	MASK7	MASK CmdSent flag.
6	MASK6	MASK CmdRespEnd flag.
5	MASK5	MASK RxOverrun flag.
4	MASK4	MASK TxOverrun flag.
3	MASK3	MASK DataTimeOut flag.
2	MASK2	MASK CmdTimeOut flag.
1	MASK1	MASK DataCmdCrcFail flag.
0	MASK0	MASK CmdCrcFail flag.

0x12140044 SDC2_MCI_FIFO_COUNT

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

The SDCC core operates in two clock domains ’ MCLK and HCLK. The CPSM and DPSM operate in MCLK domain and MciFifoDmaCtl (FIFO/DMA Controller) operates in HCLK domain. The MCI_FIFO_COUNT is a counter of FIFO Controller that monitors how many words of data are still needed to be transferred through the FIFO. At the beginning of data transaction the MCI_FIFO_COUNT counter will be loaded with the (MCI_DATA_LENGTH / 4) value and then will count down during the data transaction until it reach zero. This register is only useful for debug purposes and should not be used for normal operation since it does not reflect data which may or may not be in the pipeline.

SDC2_MCI_FIFO_COUNT

Bits	Name	Description
31:24	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
23:0	DATA_COUNT	Remaining data.

0x12140048 SDC2_MCI_BOOT

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

Handling the boot operation.

SDC2_MCI_BOOT

Bits	Name	Description
31:3	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
2	BOOT_ACK_EN	If set to '1' then Host waits for acknowledge pattern after initiating the boot operation.
1	BOOT_EN	When this bit is asserted, the boot operation is initiated in both of the modes.
0	BOOT_MODE	If set to '1' then CMD line is low during the boot operation. If boot_mode = '0', then CMD0 with the argument 0xFFFFFFFA is sent.

0x1214004C SDC2_MCI_BOOT_ACK_TIMER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

Timer for boot operation - the time until receiving the acknowledge pattern.

SDC2_MCI_BOOT_ACK_TIMER

Bits	Name	Description
31:0	BOOT_ACK_TIMER	Timer for counting the cycles from initiating the boot operation until the acknowledge pattern is accepted.

0x12140050 SDC2_MCI_VERSION

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: see below

This register should be excluded for QCSR POR testing.

SDC2_MCI_VERSION

Bits	Name	Description
31:0	MCI_VERSION	SDCC4 core version. This value corresponds to Z according to core release tag: sdcc4_pXqYrZ.

0x12140054 SDC2_MCI_EMULATION_DLY_LINE

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

The register is responsible for handling DCM which is used in emulation supports 256 values of shift intervals so 8 bits are required (0:255). Bits [31:30] are used for emulation purposes only.

The procedure for activating the DCM is:

1. Setting bit 28 - DCM_RESET.
2. Clearing bit 28 - DCM_RESET.
3. Waiting until bit 29 DCM_LOCKED is high.
4. Writing a new phase in SD_CLK_DLY_CTRL field and setting the DCM_START bit (bit 30).

The clock's placement was executed by the DCM when DCM_DONE is asserted.

SDC2_MCI_EMULATION_DLY_LINE

Bits	Name	Description
31	DCM_DONE	The shift process was finished in DCM and CMD19 can be sent towards the card. This is a read-only bit.
30	DCM_START	A new value of SD_CLK_DLY_CTRL is ready. Clears the DCM_DONE bit.
29	DCM_LOCKED	Reading the status of the LOCKED DCM's output which indicates that the output clock is ready for use.
28	DCM_RESET	Driving reset to DCM.
27:8	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
7:0	SD_CLK_DLY_CTRL	Input to DCM block in FPGA (8 bits). Controlling the change of the delay interval. The value's range may be 0-255 in DCM block.

0x12140058 SDC2_MCI_CCS_TIMER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

This register is used for operation with CE-ATA devices. The CCS timer starts to count at the end of SD transaction and it advances with every MCLK clock cycle. In boot operation this register is used for storing the number of cycles from initiating the boot operation until the first data is received.

SDC2_MCI_CCS_TIMER

Bits	Name	Description
31:0	CCS_TIMER	CE-ATA Command Completion Signal timeout period.

0x1214005C SDC2_MCI_RESPONSE_MASK

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC2_MCI_RESPONSE_MASK

Bits	Name	Description
31:0	RESPONSE_MASK	Mask used to verify the 32 status error bits. Active only when the data pending bit is set in the MCI_DATA_CTL register. When bit of this mask is set, the corresponding bit from response [39:8] is checked to be 0, i.e., shows there is no error. If all bits from mask shows no error, the DPSM will be activated without waiting for software write.

0x12140060 SDC2_MCI_DLL_CONFIG

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x60006400

SDC2_MCI_DLL_CONFIG

Bits	Name	Description
31	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
30	DLL_RST	Setting this bit to 1 resets cm_dll_sdc4. cm_dll_sdc4 should be reset every time the MCLK frequency is changed.

SDC2_MCI_DLL_CONFIG (cont.)

Bits	Name	Description
29	PDN	Power Down Value 0 - analog blocks are enabled Value 1 - analog blocks are powered down (default)
28	CK_INTP_SEL	Selects interpolator output
27	CK_INTP_EN	Enable clock interpolation for finer resolution
26:24	MCLK_FREQ	Frequency of MCLK Value 000 -100 ’ 112 (MHz) Value 001 -112 ’ 125 Value 010 -125 ’ 137 Value 011 -137 ’ 150 Value 100 -150 ’ 162 Value 101 -162 ’ 175 Value 110 -175 ’ 187 Value 111 -187 ’ 200
23:20	CDR_SELEXT	CDR phase select (gray coded) Value 0000 - phase 0 Value 0001 - phase 1 Value 0011 - phase 2 Value 0010 - phase 3 Value 0110 - phase 4 Value 0111 - phase 5 Value 0101 - phase 6 Value 0100 - phase 7 Value 1000 - phase 8 Value 1001 - phase 9 Value 1011 - phase 10 Value 1010 - phase 11 Value 1110 - phase 12 Value 1111 - phase 13 Value 1101 - phase 14 Value 1100 - phase 15
19	CDR_EXT_EN	Enable external control of cdr phase select
18	CK_OUT_EN	Enable output clock (default value is ’1’)
17	CDR_EN	Enable CDR function
16	DLL_EN	Enable DLL function
15:14	CDR_UPD_RATE	CDR update rate, low pass filtering window of CDR Max update rate: Value 00 - 0.5 MCLK frequency Value 01 - 0.25 MCLK Frequency (default) Value 10 - 0.125 MCLK frequency Value 11 - 1/16 MCLK Frequency

SDC2_MCI_DLL_CONFIG (cont.)

Bits	Name	Description
13:12	DLL_UPD_RATE	DLL update rate Value 00 - sdc4_mclk/10 Value 01 - sdc4_mclk/20 Value 10 - sdc4_mclk/40 (default) Value 11 - sdc4_mclk/80
11:10	DLL_PHASE_DET	DLL phase detector low pass average window Value 00 - 4 cycles Value 01 - 8 cycles (default) Value 10 - 16 cycles Value 11 - 32 cycles
9:8	CDR_ALGORITHM_SEL	CDR algorithm select Value 00 - Edge 1 (default) Value 01 - Edge 2 Value 10 - level Value 11- Constant delay
7:6	CMUX0_SHIFT_PHASE	Clock mux0 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable
5:4	CMUX1_SHIFT_PHASE	Clock mux1 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable
3:2	CMUX2_SHIFT_PHASE	Clock mux2 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable
1:0	CMUX3_SHIFT_PHASE	Clock mux3 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable

0x12140064 SDC2_MCI_DLL_TEST_CTL

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC2_MCI_DLL_TEST_CTL

Bits	Name	Description
31:26	VTH_CTRL	Vth control: change current in delay cell. Higher number means less delay.
25:22	DELTA_VGS_CTRL	dVgs control: change current in delay cell. Higher number means less delay.
21	DLL_BIAS_EXT_EN	Enable dll bias external control Value 0 - disable external control (default) Value 1 - enable external control
20:19	CDR_TEST_CTRL	External input to increment or decrement CDR output phase by 1 step Phase is changed on rising edge of signal. Example: To increment phase by 2 steps: 10 -> 00 -> 10 Value 00 - hold (default) Value 01 - decrement Value 10 - increment Value 11 - invalid
18	EXT_UP_DN	external control up/dn signal Value 0 - disable (default) Value 1 - enable
17	ATEST_CTRL	atest control Value 0 - disable (default) Value 1 - enable
16:14	ATEST_OUT_MUX_CTRL	Atest output mux control Value 000 - Avss (default) Value 001 - Vth current Value 010 - delta Vgs current Value 011 - Vthn Value 100- Pbias Value 101 - Nbias Value 110 - reserved Value 111 - External bias current
13	DTEST_CTRL	dtest control Value 0 - disable (default) Value 1 - enable

SDC2_MCI_DLL_TEST_CTL (cont.)

Bits	Name	Description
12:10	DTEST_OUT_MUX_CTRL	dtest output mux control. Output signals are paired for measurements Value 000 - sdc4_mclk, sdc4_mclk (default) Value 001 - da_ phout<0>, da_phout<7> Value 010 - da_ phout<3>, da_phout<4> Value 011 - da_phout<0>, da_phout<15> Value 100 - sd4_clk_out, sd4_data_out<0> Value 101 - sd4_clk_out, sd4_data_out<1> Value 110 - sd4_clk_out, sd4_data_out<2> Value 111 - sd4_clk_out, sd4_data_out<3>
9	DLL_TAP_CTRL	Delay line tap control - change number of unit delay cell in each tap Delay value Value 0 - 1 (default) Value 1 - 2
8:7	DLL_CUR_CTRL	Delay line current control - change current mirror ratio in each delay tap Delay value Value 00 - 1x (default) Value 01 - 2x Value 10 - 3x Value 11 - 4x
6	INT_REF_CLK	Value 0 (default) - use internal generated clock for delay line reference Value 1 - use sdc4_mclk for delay line reference
5	FEEDBACK_CLK_EN	Value 0 (default) - enable delay line feedback Value 1 - disable delay line feedback
4:0	RESERVED	These reserved bits can be accessed by the SW and connected to cm_dll_sdc4's input

0x12140068 SDC2_MCI_DLL_STATUS

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC2_MCI_DLL_STATUS

Bits	Name	Description
31:8	RESERVED_1	Always reads zero. Writes 'don't care' but by convention write zero.
7	DLL_LOCK	DLL lock status Value 0 - Not locked Value 1 - Locked

SDC2_MCI_DLL_STATUS (cont.)

Bits	Name	Description
6:3	CDR_PHASE	CDR phase select (gray coded) Value 0000 - phase 0 Value 0001 - phase 1 Value 0011 - phase 2 Value 0010 - phase 3 Value 0110 - phase 4 Value 0111 - phase 5 Value 0101 - phase 6 Value 0100 - phase 7 Value 1000 - phase 8 Value 1001 - phase 9 Value 1011 - phase 10 Value 1010 - phase 11 Value 1110 - phase 12 Value 1111 - phase 13 Value 1101 - phase 14 Value 1100 - phase 15
2	DDLL_COARSE_CAL	Value 1 - done Value 0 - not done
1:0	RESERVED_2	Connected to cm_dll_sdc4's output.

0x1214006C SDC2_MCI_STATUS2

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC2_MCI_STATUS2

Bits	Name	Description
31:1	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
0	MCLK_REG_WR_ACTIVE	Value 0 - No active register write to MCLK domain Value 1 - Active register write to MCLK domain. The bit indicates if a write operation to one of the following registers is in process (synchronization between HCLK and MCLK): MCI_POWER MCI_CLOCK MCI_CMD MCI_DATA_CTL

0x12140070 SDC2_MCI_GENERICS

Type: Read
Clock: SAME_RATE_AS_HCLK

SDC2_MCI_GENERICS

Bits	Name	Description
31:27	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
26:23	SD_DATA_WIDTH	Number of DAT lines Value 4 - 4 DAT lines (SD, SDIO) Value 8 - 8 DAT lines (MMC, eMMC)
22:10	RAM_SIZE	Size of RAM size: Optional Values: 512, 1024, 2048 or 4096 bytes.
9	USE_SPS	Value 1 - BAM and DML are used and USB core is connected to SDCC4, Value 0 - BAM and DML are not used.
8:6	NUM_OF_DEV	Number of eSD or eSDIO devices supported on shared SD bus. Can be set from 1 to 4.
5:1	MAX_PIPES	Number of simultaneous parallel pipes supported by the BAM and attached peripheral pair. Can be set from 1 to 31.
0	USE_DLL_SDC4	Enables the instantiation of cm_dll_sdc4. Value 0 - cm_dll_sdc4 isn't integrated with SDCC4 Value 1 - cm_dll_sdc4 is used with SDCC4.

0x12140080 SDC2_MCI_FIFO

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC2_MCI_FIFO

Bits	Name	Description
31:0	DATA	FIFO data. This register is aliased to 16 words, 0x080 - 0xBC. In SDCC3, an access to the FIFO was executed with 16 words so 16 addresses were defined. However, in SDCC4 only 8 words are used in each burst so only 8 addresses from the range should be used. When writing to the external SD_Card, writes to the data path FIFO. When reading from the external SD_Card, reads from the data path FIFO.

0x121400CC SDC2_MCI_TESTBUS_CONFIG

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

NOTE mclk_mux is the selected internal mclk: the original mclk or divided mclk during divided frequency mode.

Table 20-3 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus0(0)	sdcc_crif_wr_en	hclk
test_bus0(1)	sdcc_crif_rd_en	hclk
test_bus0(2)	sdcc_crif_core_select	hclk
test_bus0(6 downto 3)	sdcc_crif_wr_data[3:0]	hclk
test_bus0(10 downto 7)	sdcc_crif_rd_data[3:0]	hclk
test_bus0(14 downto 11)	sdcc_crif_addr[5:2]	hclk
test_bus0(15)	sdcc_crif_ready	hclk
test_bus0(16)	adm_crci4_ack	-
test_bus0(17)	adm_crci4_req	hclk
test_bus0(18)	rx_fifo_rd_en	hclk
test_bus0(19)	tx_fifo_wr_en	hclk
test_bus0(20)	dm_cnt_rst	hclk
test_bus0(28 downto 21)	ram_addr	mclk_mux
test_bus0(29)	ram_we_n	mclk_mux
test_bus0(30)	ram_cs_n	mclk_mux
test_bus0(31)	rx_fifo_wr_en	mclk_mux
test_bus1(0)	sdcc_crif_wr_en	hclk
test_bus1(1)	sdcc_crif_rd_en	hclk
test_bus1(2)	sdcc_crif_core_select	hclk
test_bus1(6 downto 3)	sdcc_crif_addr[5:2]	hclk
test_bus1(7)	sdcc_crif_ready	hclk
test_bus1(8)	adm_crci4_ack	-
test_bus1(9)	adm_crci4_req	hclk
test_bus1(10)	rx_fifo_rd_en	hclk
test_bus1(11)	tx_fifo_wr_en	hclk
test_bus1(15 downto 12)	req_rw	hclk
test_bus1(16)	DATEnUpdPulse	hclk
test_bus1(17)	LastRxRdDone	hclk
test_bus1(25 downto 18)	ram_addr	mclk_mux
test_bus1(26)	ram_we_n	mclk_mux

Table 20-3 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus1(27)	ram_cs_n	mclk_mux
test_bus1(28)	rx_fifo_wr_en	mclk_mux
test_bus1(29)	ram_reset	mclk_mux
test_bus1(31 downto 30)	pipeline_fill	mclk_mux
test_bus2(2 downto 0)	CPSMState	mclk_mux
test_bus2(3)	CPSMEn	mclk_mux
test_bus2(4)	nIntCMDEN	mclk_mux
test_bus2(5)	iCMDCnt47	mclk_mux
test_bus2(6)	iCRspE	mclk_mux
test_bus2(7)	start_bit_first(CPSM)	mclk_mux
test_bus2(8)	DivLevelCo	mclk_mux
test_bus2(11 downto 9)	DPSMState	mclk_mux
test_bus2(12)	DPSMEn	mclk_mux
test_bus2(13)	inDAT0EN_sel	mclk_mux
test_bus2(14)	inDATEN_sel	mclk_mux
test_bus2(15)	StartBit	mclk_mux
test_bus2(16)	iDEndSet	mclk_mux
test_bus2(17)	iStopBit	mclk_mux
test_bus2(18)	TxFlowCtrlChk	mclk_mux
test_bus2(19)	iTxFlowControl	mclk_mux
test_bus2(27 downto 20)	ram_addr	mclk_mux
test_bus2(28)	ram_we_n	mclk_mux
test_bus2(29)	ram_cs_n	mclk_mux
test_bus2(30)	LastRxRdDoneL	mclk_mux
test_bus2(31)	start_bit_first(DPSM)	mclk_mux
test_bus3(7 downto 0)	DATIN[7:0]	mclk_mux
test_bus3(8)	Valid	mclk_mux
test_bus3(10 downto 9)	VSMState	mclk_mux
test_bus3(11)	CmdStopBit	mclk_mux
test_bus3(13 downto 12)	StopBitDelCnt	mclk_mux
test_bus3(15 downto 14)	CRspESetDelCnt	mclk_mux
test_bus3(16)	mclkenable	mclk_mux
test_bus3(18 downto 17)	isdcc_irq	-
test_bus3(21 downto 19)	DPSMState	mclk_mux
test_bus3(22)	DPSMEn	mclk_mux
test_bus3(23)	inDAT0EN_sel	mclk_mux
test_bus3(24)	inDATEN_sel	mclk_mux
test_bus3(25)	StartBit	mclk_mux

Table 20-3 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus3(26)	iDEndSet	mclk_mux
test_bus3(27)	iStopBit	mclk_mux
test_bus3(28)	TxFlowCtrlChk	mclk_mux
test_bus3(29)	iTxFlowControl	mclk_mux
test_bus3(31)	LastDataWord	mclk_mux
test_bus4(2 downto 0)	CPSMState	mclk_mux
test_bus4(3)	CPSMEn	mclk_mux
test_bus4(4)	nIntCMDEN	mclk_mux
test_bus4(5)	iCRspE	mclk_mux
test_bus4(13 downto 6)	CMDCNT	mclk_mux
test_bus4(14)	start_bit_first(CPSM)	mclk_mux
test_bus4(15)	DivLevelCo	mclk_mux
test_bus4(16)	async_fifo_out_valid	mclk_mux
test_bus4(18 downto 17)	CMDIN	mclk_mux
test_bus4(21 downto 19)	DPSMState	mclk_mux
test_bus4(22)	DPSMEn	mclk_mux
test_bus4(29 downto 23)	BLKTCnt(6 downto 0)	mclk_mux
test_bus4(30)	iCheckProgDone	mclk_mux
test_bus4(31)	iProgDone	mclk_mux
test_bus5(2 downto 0)	DPSMState	mclk_mux
test_bus5(3)	DPSMEn	mclk_mux
test_bus5(4)	inDAT0EN_sel	mclk_mux
test_bus5(5)	inDATEN_sel	mclk_mux
test_bus5(6)	StartBit	mclk_mux
test_bus5(7)	iDEndSet	mclk_mux
test_bus5(8)	iStopBit	mclk_mux
test_bus5(9)	TxFlowCtrlChk	mclk_mux
test_bus5(10)	iTxFlowControl	mclk_mux
test_bus5(11)	LdDataBuffer	mclk_mux
test_bus5(12)	iRxFlowControl	mclk_mux
test_bus5(13)	LastRxRdDone	mclk_mux
test_bus5(14)	inDATEN_high_sel	mclk_mux
test_bus5(15)	inDATEN_low_sel	mclk_mux
test_bus5(16)	async_fifo_out_valid	mclk_mux
test_bus5(17)	LastDataWord	mclk_mux
test_bus5(18)	pipeline_empty	mclk_mux
test_bus5(19)	ShiftNotE	mclk_mux
test_bus5(20)	start_bit_first (DPSM)	mclk_mux

Table 20-3 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus5(21)	DIVLevelCo	mclk_mux
test_bus5(28 downto 22)	BLKTCnt(6:0)	mclk_mux
test_bus5(29)	iCheckProgDone	mclk_mux
test_bus5(30)	iProgDone	mclk_mux
test_bus5(31)	start_bit_last	mclk_mux
test_bus6(7 downto 0)	ram_addr	mclk_mux
test_bus6(8)	ram_we_n	mclk_mux
test_bus6(9)	ram_cs_n	mclk_mux
test_bus6(11 downto 10)	pipeline_fill	mclk_mux
test_bus6(12)	ram_reset	mclk_mux
test_bus6(13)	rx_fifo_wr_en	mclk_mux
test_bus6(14)	rx_fifo_rd_en	hclk
test_bus6(15)	tx_fifo_wr_en	hclk
test_bus6(19 downto 16)	req_rw	hclk
test_bus6(20)	DATEnUpdPulse	hclk
test_bus6(21)	dm_cnt_rst	hclk
test_bus6(25 downto 22)	rx_fifo_rd_word_cnt	hclk
test_bus6(29 downto 26)	tx_fifo_wr_word_cnt	hclk
test_bus6(30)	iLastRxRdDone	hclk
test_bus6(31)	RxActive	hclk
test_bus7(1 downto 0)	CMDIN	mclk_mux
test_bus7(17 downto 2)	DATIN	mclk_mux
test_bus7(18)	div_freq_cnt_cmd_tx	mclk
test_bus7(19)	div_freq_cnt_dat_tx	mclk
test_bus7(20)	div_freq_cnt_rx	mclk
test_bus7(21)	async_fifo_out_valid	mclk
test_bus7(22)	Rising_DAT0EN_5d	mclk
test_bus7(31 downto 23)	async_fifo_rd_data	mclk

SDC2_MCI_TESTBUS_CONFIG

Bits	Name	Description
31:8	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
7:4	SPARE_FIELD	SW spare bits.
3	TESTBUS_ENA	0x1: Enable 0x0: Disable

SDC2_MCI_TESTBUS_CONFIG (cont.)

Bits	Name	Description
2:0	TESTBUS_SEL	These bits select from different test signals. Refer to Table 1-3 for a list of test signals. TESTBUS_SELBus testbus_sel = 0sdcc_test_bus <= test_bus0 testbus_sel = 1 sdcc_test_bus <= test_bus1 testbus_sel = 2sdcc_test_bus <= test_bus2 testbus_sel = 3sdcc_test_bus <= test_bus3 testbus_sel = 4sdcc_test_bus <= test_bus4 testbus_sel = 5sdcc_test_bus <= test_bus5 testbus_sel = 6sdcc_test_bus <= test_bus6 testbus_sel = 7sdcc_test_bus <= test_bus7

0x121400D0 SDC2_MCI_TEST_CTL

Type: Read/Write
Clock: PCLK
Reset State: 0x00000000

(ARM name: MCITCR)

SDC2_MCI_TEST_CTL

Bits	Name	Description
31:4	RESERVED_1	Always reads zero. Writes ’don’t care’ but by convention write zero.
3	REGTEST	Register Test Bit: Set 0: normal mode (default--accesses to the registers are controlled by the hardware protection circuitry) Set 1: test mode (the hardware protection circuitry is bypassed. Normal Write/Read/Write/ Read tests can be performed independently of the link side.
2:1	RESERVED_2	Always reads zero. Writes ’don’t care’ but by convention write zero.
0	ITEN	Integration Test Enable. This bit places PrimeCell MCI in the following modes: Set 0: normal mode Set 1: Integration test mode

0x121400D4 SDC2_MCI_TEST_INPUT

Type: Read
Clock: PCLK

(ARM name: MCIITIP)

SDC2_MCI_TEST_INPUT

Bits	Name	Description
31:10	RESERVED_1	Always reads zero. Writes ’don’t care’ but by convention write zero.
9:6	MCIDATIN_7_4	Reads return the value on the MCIDATIN[7:4] primary inputs.
5	MCICMDIN	Reads return the value on the MCICMDIN primary input.
4:1	MCIDATIN_3_0	Reads return the value on the MCIDATIN[3:0] primary inputs.
0	RESERVED_2	Always reads zero. Writes ’don’t care’ but by convention write zero.

0x121400D8 SDC2_MCI_TEST_OUT

Type: Read/Write
Clock: PCLK

(ARM name: MCIITOP)

SDC2_MCI_TEST_OUT

Bits	Name	Description
31:16	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
15:12	MCIDATOUT_7_4	Primary output. Writes specify the value to be driven on the MCIDATOUT[7:4] primary output in the integration test mode. Reads return the value written into this field.
10	MCICMDOUT	Primary output. Writes specify the value to be driven on the MCICMDOUT primary output in the integration test mode. Reads return the value written into this field.
9:6	MCIDATOUT_3_0	Primary output. Writes specify the value to be driven on the MCIDATOUT[3:0] primary output in the integration test mode. Reads return the value written into this field.
1	MCIINTR1	Intra-chip output. Writes specify the value to be driven on the intra-chip MCIINTR1 output in the integration test mode. This bit is write-only.
0	MCIINTR0	Intra-chip output. Writes specify the value to be driven on the intra-chip MCIINTR0 output in the integration test mode. This bit is write-only.

20.14 SDC2_DML_CONFIG (0x12140800 SDC2_DML_BASE)

This section contains the SDC2 DML registers.

20.14.1 DML Registers

The address field is a relative address. A base will be supplied by the SOC team and documented at the start of the chip SW Manual.

0x12140800 SDC2_DML_CONFIG

Type: Read/Write
Clock: HCLK
Reset State: 0x00010000

SW has the responsibility to set the CRCI SEL fields correctly when both Consumer and Producer sides are enabled at the same time. For example, setting both to 01 or setting both to 10 is an invalid setting if both producer and consumer sides are kicked off. The DML does NOT assume responsibility for incorrect setting of CRCI SEL fields and hence its function is not defined in such cases.

SDC2_DML_CONFIG

Bits	Name	Description
31:19	RESERVED31	reserved
18	INFINITE_CONS_TRANS	If set, this bit means the consumer transaction is of infinite size. Hence the transaction_end_rec signal from BAM will be ignored.
17	DIRECT_MODE	If set, DML is assumed to directly MASTER the AHB bus, in essence, no BAM or BAM is bypassed. This bit value is also routed to the direct_mode hardware port on the DML to be connected to BAM. See Direct_mode_BASE_addr register.
16	BYPASS	If set, the CRCI pairs will be passed through for legacy central DM support. The config AHB slave interface will be directly accessing the peripheral core for config, command and data movement functions. NOTE: The reset value of this bit is `1' which means the DML come out of PoReset in BYPASS state.
15:6	RESERVED15	reserved
5	PRODUCER_BLOCK_END_HPROT2	If set, DML drives high hprot[2] to BAM when block_end is high, else DML drives low hprot[2] to BAM when block_end is high
4	PRODUCER_TRANS_END_EN	When set, transaction_end signal is asserted at the end of DML transaction. When cleared, transaction_end signal is NOT asserted at the end of DML transaction. This feature allows to divide one BAM transaction to two Peripheral transactions.

SDC2_DML_CONFIG (cont.)

Bits	Name	Description
3:2	CONSUMER_CRCI_SEL	When set to 00, Consumer side is Disabled When set to 01, CRCI-x pair is the consumer CRCI When set to 10, CRCI-y pair is the consumerCRCI If set to 11, its a invalid setting.
1:0	PRODUCER_CRCI_SEL	When set to 00, Producer side is Disabled When set to 01, CRCI-x pair is the producer CRCI When set to 10, CRCI-y pair is the producer CRCI If set to 11, its a invalid setting.

0x12140804 SDC2_DML_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00010001

SDC2_DML_STATUS

Bits	Name	Description
31:17	RESERVED31	reserved
16	CONSUMER_IDLE	0x0: Consumer is busy 0x1: Consumer is IDLE
15:1	RESERVED15	reserved
0	PRODUCER_IDLE	0x0: Producer is busy 0x1: Producer is IDLE

0x12140808 SDC2_DML_SW_RESET

Type: Write
Clock: HCLK
Reset State: 0x00000000

A write to this register resets the DML core. All internal state information will be lost and all register values will be reset as well.

SDC2_DML_SW_RESET

Bits	Name	Description
31:0	RESERVED	reserved

0x1214080C SDC2_DML_PRODUCER_START

Type: Write
Clock: HCLK
Reset State: 0x00000000

A write to this register triggers the DML's Producer state machine. No SW register values will be altered. Only the internal counters and settings related to Producer activity will be reset and started afresh. This register should be written to after POR to kick off producer side. This register should also be used to restart the producer once it has reached IDLE state (as indicated by the STATUS register) after completing the current transaction.

SDC2_DML_PRODUCER_START

Bits	Name	Description
31:0	RESERVED	reserved

0x12140810 SDC2_DML_CONSUMER_START

Type: Write
Clock: HCLK
Reset State: 0x00000000

A write to this register triggers the DML's consumer state machine. No SW register values will be altered. Only the internal counters and settings related to consumer activity will be reset and started afresh. This register should be written to after POR to kick off consumer side. This register should also be used to restart the consumer once it has reached IDLE state (as indicated by the STATUS register) after completing the current transaction..

SDC2_DML_CONSUMER_START

Bits	Name	Description
31:0	RESERVED	reserved

0x12140814 SDC2_DML_PRODUCER_PIPE_LOGICAL_SIZE

Type: Write/Read
Clock: HCLK
Reset State: 0x00000000

This register holds the size of the producer pipe (in units of bytes) _to_ which the peripheral can keep writing data to when its the PRODUCER. The value of this register should be consistent with what the BAM registers are programmed with as well. The DML in response to producer side CRCI requests starts writing out data (generated by the Peripheral) from address 0x0 (on its AHB Master Interface). For subsequent Producer side data accesses, the DML keeps on incrementing

the address. Upon reaching the max value as indicated by this register, the address rolls over back to 0x0. The address also rolls over back to 0x0 after reaching the end of a transaction.

This register value decides the range of addresses seen on the DML AHB Master address bus during Producer activity.

The value of this register is restricted to any power of two and greater than or equal to the Producer BAM Block Size setting. This is to avoid DML overwriting its own data in the pipe as the data is not committed until block_end is received by the BAM.

The recommended value for this register is 4096(decimal)

SDC2_DML_PRODUCER_PIPE_LOGICAL_SIZE

Bits	Name	Description
31:16	RESERVED31	reserved31
15:0	PRODUCER_LOGICAL_SIZE	The size of the producer pipe (in units of bytes) to which a producer peripheral can keep writing the data it produces.

0x12140818 SDC2_DML_CONSUMER_PIPE_LOGICAL_SIZE

Type: Write/Read
Clock: HCLK
Reset State: 0x00000000

This register holds the size of the consumer pipe (in units of bytes) _from_ which the peripheral can keep _reading_ data from when its the CONSUMER. The value of this register should be consistent with what the BAM registers are programmed with as well. The DML in response to consumer side CRCI requests starts reading out data (needed by the Peripheral) from address 0x0 (on its AHB Master Interface). For subsequent consumer side data accesses, the DML keeps on incrementing the address. Upon reaching the max value as indicated by this register, the address rolls over back to 0x0. The address also rolls over back to 0x0 after reaching the end of a transaction.

This register value decides the range of addresses seen on the DML AHB Master address bus during consumer activity.

The value of this register is restricted to any power of two and no smaller than 32 bytes, that is, no smaller than a "beat-8" burst on a 32 bit AHB.

The recommended value for this register is 4096(decimal)

SDC2_DML_CONSUMER_PIPE_LOGICAL_SIZE

Bits	Name	Description
31:16	RESERVED31	reserved31
15:0	CONSUMER_LOGICAL_SIZE	The size of the consumer pipe (in units of bytes) to which a consumer peripheral can keep reading the data from it needs.

0x1214081C SDC2_DML_PIPE_ID

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register holds pipe IDs that services the producer and consumer side of the peripheral.

- The producer pipe ID is fed to the BAM when servicing the producer side of the peripheral.
- The consumer pipe ID is fed to the BAM when servicing the consumer side of the peripheral.
- The DML also uses this ID value to look into the appropriate side band signals from BAM like pipe_empty, pipe_full etc before initiating the said AHB transaction.

SDC2_DML_PIPE_ID

Bits	Name	Description
31:21	RESERVED31	reserved
20:16	CONSUMER_PIPE_ID	consumer pipe ID
15:5	RESERVED15	reserved
4:0	PRODUCER_PIPE_ID	producer pipe ID

0x12140820 SDC2_DML_PRODUCER_TRACKERS

Type: Read
Clock: HCLK
Reset State: 0x00000000

.This register is for debug purposes only. They reflect the value of the producer block and transaction counters when read. The values may be dynamically changing when a transaction is in progress.

SDC2_DML_PRODUCER_TRACKERS

Bits	Name	Description
31:16	PROD_TRANS_CNT	Value of the 16bit tracker tracking the Producer Transaction Count for the current transaction. Should read 0 at the end of the transaction.
15:0	PROD_BLOCK_CNT	Value of the 16 bit tracker that tracks the Producer Block Count. Need not be zero at the end of transaction.

0x12140824 SDC2_DML_PRODUCER_BAM_BLOCK_SIZE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register holds the "block" size, in units of bytes, associated with the Producer BAM. The DML asserts the block_end side band signal to the BAM whenever the producer side of the peripheral has generated the said amount of data. This register value should be an integral multiple of the Producer CRCI Block Size.

Legal values for Producer BAM Block Size are 64, 128, 192, 256, 512, 1024, 2048 and 4096.

The recommended value for this register is 512(decimal)

SDC2_DML_PRODUCER_BAM_BLOCK_SIZE

Bits	Name	Description
31:16	RESERVED	reserved
15:0	PRODUCER_BLK_SIZE	Size of the one "block" on the producer side in units of bytes.

0x12140828 SDC2_DML_PRODUCER_BAM_TRANS_SIZE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register holds the "transaction" size, in units of bytes, associated with the Producer BAM. The DML asserts the transaction_end side band signal to the BAM whenever the producer side of the peripheral has generated the said amount of data. This signal is asserted only during the address phase of the AHB transaction that carries the last byte corresponding to the size mentioned in this register. Once this value is reached for a given transaction, the address for subsequent data access rolls back to 0x0 and all the block size, CRCI size and transaction size counters also get reset to 0 and start all over again. A value of zero in this register during a producer transaction start means infinite size transaction and hence transaction_end may not get asserted.

This value can be anything up to a maximum of 4294967295 bytes (4 GB -1). If this register value is zero when the DML is started, then an infinite transaction size is assumed. No transaction_end will be generated.

SDC2_DML_PRODUCER_BAM_TRANS_SIZE

Bits	Name	Description
31:0	PRODUCER_TRANS_SIZE	Size of the one "transaction" on the producer side in units of bytes or if zero, then infinite transaction size assumed.

0x1214082C SDC2_DML_DIRECT_MODE_BASE_ADDR

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register is used whenever the DIRECT_MODE bit in config register is set. The programmed 16bits will be used as DML AHB Master address bus MSBits for consumer (AHB read) and producer (AHB Write) operations. The lower 16bits would be dictated by the pipe logical size register.

SDC2_DML_DIRECT_MODE_BASE_ADDR

Bits	Name	Description
31:16	CONSUMER_BASE_ADDR	used as AHB Master address (31:16) when doing direct mode consumer operations if direct_mode bit is set.
15:0	PRODUCER_BASE_ADDR	used as AHB Master address (31:16) when doing direct mode producer operations if direct_mode bit is set.

0x12140830 SDC2_DML_DEBUG

Type: Write/Read
Clock: HCLK
Reset State: 0x00000000

Enables Test Bus of the DML and also selects which side signals to drive the test bus with.

SDC2_DML_DEBUG

Bits	Name	Description
31:2	RESERVED	reserved
1	STATUS_2_SEL	If set, selects the set of signals listed out in DML_BAM_SIDE_STATUS_2 register onto Test bus, else selects set of signals listed out in DML_BAM_SIDE_STATUS_1 register to be muxed onto test bus. Valid only if bit 0 is set.
0	TESTBUS_EN	0x0: Disable Test Bus 0x1: Enable Test Bus

0x12140834 SDC2_DML_BAM_SIDE_STATUS_1

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the instantaneous value of the side band signals with BAM.

SDC2_DML_BAM_SIDE_STATUS_1

Bits	Name	Description
31:24	RESERVED31	reserved
23	ACK_ON_SUCCESS_TOGGLE	for selected consumer pipe
22	ACK_BYTES_AVAIL_TOGGLE	for selected consumer pipe
21	PIPE_BYTES_AVAIL_TOGGLE	for selected consumer pipe
20	TRANSACTION_END_REC	transaction end received for selected consumer pipe.
19	PIPE_BYTES_FREE_TOGGLE	bytes free toggle signal for selected producer pipe
18:3	PIPE_BYTES_FREE	bytes free value for selected producer pipe
2	MESSAGING_ONLY	DML output status
1	TRANSACTION_END	DML output status
0	BLOCK_END	DML output status

0x12140838 SDC2_DML_BAM_SIDE_STATUS_2

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the instantaneous value of the side band signals with BAM.

SDC2_DML_BAM_SIDE_STATUS_2

Bits	Name	Description
31:16	ACK_ON_SUCCESS_TOGGLE_SIZE	for selected consumer pipe
15:0	PIPE_BYTES_AVAIL	for selected consumer pipe

0x1214083C SDC2_DML_RTL_GENERICS_1

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the value of the RTL Generics set during the integration of the DML into a SPS Wrapper or other entity.

SDC2_DML_RTL_GENERICS_1

Bits	Name	Description
31:17	RESERVED31	reserved
16:11	PERIPHERAL_ADDR_WIDTH	represents the width set (in binary format)
10:6	MAX_PIPES	represents the number of pipe value set (in binary format)
5:3	CONSUMER_CRCI_BLK	101:.256 bytes 0x0: 16 bytes 0x1: 32 bytes 0x2: 64 bytes 0x3: 128 bytes 0x4: 192 bytes
2:0	PRODUCER_CRCI_BLK	101:.256 bytes 0x0: 16 bytes 0x1: 32 bytes 0x2: 64 bytes 0x3: 128 bytes 0x4: 192 bytes

0x12140840 SDC2_DML_RTL_GENERICS_2

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the value of the PROD_DMR_RD_ADDR Generic set in RTL during the integration of the DML into a SPS Wrapper or other entity.

SDC2_DML_RTL_GENERICS_2

Bits	Name	Description
31:0	PROD_RD_DMR_ADDR	32bit Value of the PROD_DMR_RD_ADDR generic

0x12140844 SDC2_DML_RTL_GENERICS_3

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the value of the CONS_DMR_WR_ADDR Generic set in RTL during the integration of the DML into a SPS Wrapper or other entity.

SDC2_DML_RTL_GENERICS_3

Bits	Name	Description
31:0	CONS_WR_DMR_ADDR	32bit Value of the CONS_DMR_WR_ADDR generic

0x12140848 SDC2_DML_INTERRUPT_ENABLE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

SDC2_DML_INTERRUPT_ENABLE

Bits	Name	Description
31:1	RESERVED31	reserved
0	PROD_IDLE_START_INTR_EN	Enable DML to generate an interrupt when PRODUCER enters an IDLE state.

0x1214084C SDC2_DML_INTERRUPT_CLEAR

Type: Write
Clock: HCLK
Reset State: 0xXXXXXXXX

SDC2_DML_INTERRUPT_CLEAR

Bits	Name	Description
31:1	RESERVED31	reserved
0	PROD_IDLE_START_INTR_CLR	Clear PROD_IDLE_START_INTR interrupt.

20.15 SDC2 BAM Registers (0x12142000 SDC2_BAM_BASE)

This section contains the SDC2 BAM registers.

BAM supports only Word (4 byte) aligned writes and reads on the Configuration Bus interface.

BAM has MAX_PIPES hardware generic parameter defining the number of pipes it supports. Each BAM can have up to 31 pipes supported.

BAM has BAM_CONF_AHBS_ADDR_WIDTH hardware generic parameter defining the Bit Number for selecting BAM access or Peripheral access. Legal Ranges are 14 to 20. Count starts from 1, meaning a value of 17 will set BAM Base address as 0x0001_0000.

20.15.1 BAM control registers

BAM Control registers configure the BAM operational state, SW reset, interrupts and others.

0x12142F80 SDC2_BAM_CTRL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

BAM Control register allows global controls for the BAM.

SDC2_BAM_CTRL

Bits	Name	Description
31:17	RESERVED_BITS31_17	Set to Zero (0)
16	IBC_DISABLE	This Bit enables power saving by disabling the inactivity clock timer/counter. This is useful when: 1) The BAM is Enabled but idling for long periods. 2) The BAM is Enabled and running but the inactivity timers/counters are not required by the SW for operating the BAM. When the BAM is Disabled, it automatically shuts down those timers to save power. 1’b1 - Enable Power Saving Mode 1’b0 - Disable Power Saving Mode

SDC2_BAM_CTRL (cont.)

Bits	Name	Description
15	BAM_CACHED_DESC_STORE	This Bit enables storage of a cached Descriptor into RAM when doing Context Switch and loading it back when returning to this pipe. This is relevant for System Modes Only. BAM to BAM Consumer mode doesn't have this option. Enabling this makes the Context Switch process slightly longer but reduces AHB Descriptor Fetch time later on. It also reduces the number of descriptor fetches done by the BAM if BAM is treating more than 2 pipes. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
14:13	BAM_DESC_CACHE_SEL	This Selector chooses which Descriptor Caching mode will be used. This is relevant for System Producer or Consumer modes only. 2’b00 - Cache when current descriptor has less than 64 bytes left. 2’b01 - Cache when current descriptor has less than 128 bytes left. 2’b10 - Immediate Auto cache - cache will happen whenever there are no descriptors cached. This might cause unnecessary descriptors reads when switching between more than 2 pipes. It is the most effective when each pipe processes more bytes than there are in an average descriptor (small descriptors, big block size), or when working with 2 or less pipes. 2’b11 - Cache when descriptor is needed only. This results in 1 descriptor present in cache at most. Available in BAM only
12	RESERVED_BITS12	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_SIC_SEL
11:5	BAM_TESTBUS_SEL	Set to Zero (0) Obsolete field: BAM_TESTBUS_SEL Test Bus selector. Supported until (including) bam_p3q3r29 (BlackBird). Moved to a dedicated register - BAM_TEST_BUS_SEL in the following releases.
4	BAM_EN_ACCUM	When Enabled, BAM will accumulate data written by the peripheral in Direct Mode into INCR8 Bursts. This is an optimization feature for Producer Direct Mode cases. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
3	RESERVED_BITS3	Set to Zero (0)
2	RESERVED_BITS2	Set to Zero (0)

SDC2_BAM_CTRL (cont.)

Bits	Name	Description
1	BAM_EN	After reset the BAM wakes up in Disabled Mode. While Disabled, BAM operates in Legacy mode (all the transfers from the peripheral go around the BAM as if it doesn't exist) Software Enables this bit to allow BAM operation. This bit doesn't affect the PIPE enable bit in BAM_P_CTRL register. The only possibility to Disable the BAM after it has been enabled is by Hardware or Software reset. 1'b1 - Enabled 1'b0 - Disabled
0	BAM_SW_RST	This will reset the BAM & all Pipes. Software may use this to reset the BAM. As long as the bit remains high the BAM remains in reset state. Software should clear this bit 1'b1 - Reset state 1'b0 - Normal state

0x12142F84 SDC2_BAM_REVISION

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a hard coded revision number of the BAM RTL. This corresponds to the BAM target number in the IMS. Also additional BAM settings are reflected here.

SDC2_BAM_REVISION

Bits	Name	Description
31:24	INACTIV_TMR_BASE	This indicates the width of the inactivity timers base counter
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	NUM_INACTIV_TMRS	This bit is checked only if INACTIV_TMRS_EXST = 1. This bit indicates how many inactivity timers are implemented according to value of INACTIVITY_TIMERS_SUPPORTED generic: 1'b1 - One timer for global BAM activity (INACTIVITY_TIMERS_SUPPORTED = 1) 1'b0 - MAX_PIPES timers for each pipe activity (INACTIVITY_TIMERS_SUPPORTED = 2)
19	INACTIV_TMRS_EXST	This indicates BAM has inactivity timers. 1'b1 - Timers available (INACTIVITY_TIMERS_SUPPORTED = 1 or 2) 1'b0 - No timers available (INACTIVITY_TIMERS_SUPPORTED = 0)

SDC2_BAM_REVISION (cont.)

Bits	Name	Description
18	HIGH_FREQUENCY_BAM	This indicates BAM has Double Sampling on the Ack On Success interface. 1'b1 - Ack On Success double sampled 1'b0 - No double sampling of Ack On Success
17	BAM_HAS_NO_BYPASS	This field indicates BAM has no bypass on the AHB Data bus, from the Peripheral AHB Master to the fabric. When Bypass is available, it is the default routing when BAM is disabled. 1'b1 - No Bypass 1'b0 - Bypass Exists
16	SECURED	This field indicates BAM/BAM-Lite has security support (APU inside) 1'b1 - Secured 1'b0 - Not Secured
15:12	RESERVED_BITS15_12	Set to Zero (0)
11:8	NUM_EES	This indicates the Number of Interrupt Lines (Execution Environments) supported by the BAM. When 1 EE is supported, only the BAM_IRQ_SRCS*_EE0 registers exist. When 4 EEs are supported, all BAM_IRQ_SRCS*_EEn registers exist for n=[0..3].
7:0	REVISION	This field contains the revision number of the core, Hard Coded. 8'h01 - Voyager (bam_p3q3r22 +) 8'h02 - BlackBird (bam_p3q3r27 +) 8'h03 - Waverider BAM (bam_p3q3r30 +) 8'h04 - Aurora BAM (bam_p3q2r43 +) 8'h05 - Shelby BAM (bam_p2q2r45 +) 8'h10 - Waverider BAM Lite (bam_lite_p1q1r0 +) 8'h11 - Aurora BAM Lite (bam_lite_p3q2r16 +) 8'h12 - Shelby BAM Lite (bam_lite_p2q2r18 +)

0x12142FBC SDC2_BAM_NUM_PIPES

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a the hard coded number of pipes in the BAM. Since each BAM may have a different number of pipes instantiated in HW, this register allows the SW to know this parameter. The reset state value doesn't have any meaning in this register since it is a constant.

SDC2_BAM_NUM_PIPES

Bits	Name	Description
31:24	BAM_NON_PIPE_GRP	This field contains the number of BAM Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
23:16	PERIPH_NON_PIPE_GRP	This field contains the number of Peripheral's Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
15:8	RESERVED_BITS15_8	Set to Zero (0)
7:0	BAM_NUM_PIPES	This field contains the number of pipes available in this BAM

0x12142FC0 SDC2_BAM_TIMER

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the BAM (all the pipes are in idle state).

SDC2_BAM_TIMER

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12142FC4 SDC2_BAM_TIMER_CTRL

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The register can be written and read only when INACTIVITY_TIMERS_SUPPORTED generic equals to 1.

The resolution of the BAM inactivity timer are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define

the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * TIMER_TRSHLD.

SDC2_BAM_TIMER_CTRL

Bits	Name	Description
31	TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1 to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	TIMER_RUN	Will be used along with TIMER_MODE Not implemented at this time. Set to zero(0)
29	TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12142F88 SDC2_BAM_DESC_CNT_TRSHLD

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds a threshold value for the counter summing the Size of the Descriptors Provided. This value is Global for all pipes but it is relevant for System Producer BAM mode and Both Consumer modes, where Descriptors summing takes place in order to provide the information to the peripheral via pipe bytes free (producer) or pipe bytes available interfaces.

SDC2_BAM_DESC_CNT_TRSHLD

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0).
15:0	CNT_TRSHLD	Threshold value. The maximum allowed value is 32kByte. Available in BAM only

0x12142F8C SDC2_BAM_IRQ_SRCS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking out this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register points to the physical BAM_IRQ_SRCS_EE0 register.

SDC2_BAM_IRQ_SRCS

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12142F90 SDC2_BAM_IRQ_SRCS_MSK

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register points to the physical BAM_IRQ_SRCS_MSK_EE0 register.

SDC2_BAM_IRQ_SRCS_MSK

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12142FB0 SDC2_BAM_IRQ_SRCS_UNMASKED

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register points to the physical BAM_IRQ_SRCS_UNMASKED_EE0 register.

SDC2_BAM_IRQ_SRCS_UNMASKED

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

0x12142F94 SDC2_BAM_IRQ_STTS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only.

Clearing the interrupt bits is done by writing to BAM_IRQ_CLR register.

SDC2_BAM_IRQ_STTS

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
3	BAM_EMPTY_IRQ	This interrupt is for DEBUG purpose only. It should not be used in normal SW flows. The interrupt indicates the BAMs buffer is empty. This bit can become high only when BAM_DATA_ERASE or BAM_DATA_FLUSH is high in BAM_TEST_BUS_SEL register.
2	BAM_ERROR_IRQ	This Indicates a Fatal Error has happened in the BAM. Currently this might happen due to an UnSuccessful Pipe Reset operation.

SDC2_BAM_IRQ_STTS (cont.)

Bits	Name	Description
1	BAM_HRESP_ERR_IRQ	This interrupt Indicates that an Erroneous HResponse has been received by the AHB Master. Additional Information about the error may be read at BAM_AHB_MASTER_ERR_* Registers. Clearing this interrupt also clears the BAM_AHB_MASTER_ERR_* Registers. Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12142F98 SDC2_BAM_IRQ_CLR

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

SDC2_BAM_IRQ_CLR

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
3	BAM_EMPTY_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM-Lite only
2	BAM_ERROR_CLR	1'b1 - Clear 1'b0 - Unchanged
1	BAM_HRESP_ERR_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12142F9C SDC2_BAM_IRQ_EN

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the BAM Interrupt Status register.

SDC2_BAM_IRQ_EN

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_EN	Enables Inactivity timer interrupt by writing this bit 1'b1 - Enable 1'b0 - Disable
3	BAM_EMPTY_EN	1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
2	BAM_ERROR_EN	1'b1 - Enable 1'b0 - Disable
1	BAM_HRESP_ERR_EN	1'b1 - Enable 1'b0 - Disable Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12142FA0 SDC2_BAM_RESERVED_1

Type: Read
Clock: BAM_CLK
Reset State: 0x00000000

SDC2_BAM_RESERVED_1

Bits	Name	Description
31	RESERVED_BITS31	Set to Zero (0) Obsolete field: BAM_IRQ_SIC_SEL
30:0	RESERVED_BITS30_0	Set to Zero (0) Obsolete field: P_IRQ_SIC_SEL

0x12142FA4 SDC2_BAM_AHB_MASTER_ERR_CTRLS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

SDC2_BAM_AHB_MASTER_ERR_CTRLS

Bits	Name	Description
31:23	RESERVED_BITS31_16	Set to Zero (0)
22:18	BAM_ERR_HVMID	HVMID
17	BAM_ERR_DIRECT_MODE	DIRECT MODE
16:12	BAM_ERR_HCID	HCID
11:8	BAM_ERR_HPROT	HPROT
7:5	BAM_ERR_HBURST	HBURST
4:3	BAM_ERR_HSIZE	HSIZE
2	BAM_ERR_HWRITE	HWRITE
1:0	BAM_ERR_HTRANS	HTRANS

0x12142FA8 SDC2_BAM_AHB_MASTER_ERR_ADDR

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

SDC2_BAM_AHB_MASTER_ERR_ADDR

Bits	Name	Description
31:0	BAM_ERR_ADDR	HADDR

0x12142FAC SDC2_BAM_AHB_MASTER_ERR_DATA

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

SDC2_BAM_AHB_MASTER_ERR_DATA

Bits	Name	Description
31:0	BAM_ERR_DATA	HDATA

0x12142FB4 SDC2_BAM_RESERVED_2

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

SDC2_BAM_RESERVED_2

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_IRQ_DEST_ADDR

0x12142FB8 SDC2_BAM_RESERVED_3

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

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SDC2_BAM_RESERVED_3

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_DEST_ADDR

0x12142FF0 SDC2_BAM_TRUST_REG

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside - SECURED field in the BAM_REVISION register) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

SDC2_BAM_TRUST_REG

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_VMID	Those bits indicate the VMID value to be used when performing BAM type accesses to the bus. BAM Type accesses include BAM MTI (or Direct Mode accesses, not applicable for BAM Lite)
7	BAM_RST_BLOCK	When enabled, the BAM Global SW reset will not be available for usage. This is in order to deny Global SW reset requests by the Global security group. 1'b1 - Enable 1'b0 - Disable
6:2	RESERVED_BITS6_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_EE	This Field Indicates the EE (0,1,2,3) to which the BAM Interrupt belongs to. The pipe interrupts will fire on the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12142FF4 SDC2_BAM_TEST_BUS_SEL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This is the testbus selector register.

Supported in releases after bam_p3q3r29 (BlackBird).

SDC2_BAM_TEST_BUS_SEL

Bits	Name	Description
31:19	RESERVED_BITS31_19	Set to Zero (0)
18	BAM_DATA_ERASE	When enabled, BAM will be instructed to erase all the data it currently has inside. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Erase 1'b0 - Disabled
17	BAM_DATA_FLUSH	When enabled, BAM will be instructed to flush all the data it currently has inside. BAM will only flush the data once it has enough data and a valid destination for it. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Flush 1'b0 - Disabled
16	BAM_CLK_ALWAYS_ON	This bit controls the BAM to issue 'always on' clock request. 1'b1 - Enable Always On clock request. 1'b0 - Disabled
15:7	RESERVED_BITS15_7	Set to Zero (0)
6:0	BAM_TESTBUS_SEL	Test Bus selector. Values with bit[11] set high are reserved for the BAM Lite integrator to provide testbus from outside of the BAM Lite. For example, eDML testbus may reside at X'100_0000' to X'111_1111' selector values. eDML has no registers thus has no test bus selector, so its test bus is combined with the BAM lite's. BAM provides zeroes on its testbus when external values selected. X'000_0000' - Zeros X'000_0001' - Slave test bus X'000_0010' - Pipe state machine test bus X'000_0011' - Buffer test bus X'000_0100' - Sideband test bus X'000_1101' - Bus Manager test bus X'001_0000' - Reg file test bus X'1''_''''' - BAM Lite sets zeroes on the test bus, leaving it for external use

0x12142FF8 SDC2_BAM_TEST_BUS_REG

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the value being output to the testbus of the chip. It is not intended for SW usage but for lab debugging of the BAM. Values here can change every cycle.

SDC2_BAM_TEST_BUS_REG

Bits	Name	Description
31:0	BAM_TESTBUS_REG	32 bit Testbus value. To select the Block in BAM to show here, use the BAM_TESTBUS_SEL field in BAM_CTRL register.

0x12142FFC SDC2_BAM_CNFG_BITS

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM configuration bits for bug fixes. It is highly recommended to follow the directions for each bit and set it accordingly.

SDC2_BAM_CNFG_BITS

Bits	Name	Description
31:27	RESERVED_BITS31_27	Set to Zero (0)
26	BAM_AU_ACCUMED	Recommended value: 1 This bit fixes a bug in the Ack Update state machine, where an overflow happened while counting descriptors and reaching more than 64kB of calculated sizes. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only
25	BAM_PSM_P_HD_DATA	Recommended value: 1 This bit allows pipe state machine to ignore retransmission requests if a pipe has just been initialized and process those as a regular fetch request. (consumer modes only). When this bit disabled, BAM could fetch descriptors for a pipe which was reset and no descriptors were added yet, if a retransmission request followed after the reset. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only

SDC2_BAM_CNFG_BITS (cont.)

Bits	Name	Description
24	BAM_REG_P_EN	Recommended value: 1 This bit fixes the pipe configuration signals mux for the current active pipe in 2 pipes BAM. When disabled, internal state machines might get into enabled states while the pipe is disabled. This would typically happen after pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
23	BAM_WB_DSC_AVL_P_RST	Recommended value: 1 This bit allows the Writeback state machine to reset the vector indicating there are available descriptors when a pipe reset occurs. If disabled, BAM might fetch descriptors after resetting and reconfiguring a pipe, even though no Event (descriptors) was provided.. 1’b1 - Enable 1’b0 - Disable Available in BAM only
22	BAM_WB_RETR_SVPNT	Recommended value: 1 This bit fixes a bug where a pipe which was reset, still stored its retransmission savepoint, but into the illegal’s pipe address space, thus hurting the last pipe of the BAM if the BAM had a total 4, 8 or 16 pipes. This is relevant for Producer to System modes only. (CR-0000151585) 1’b1 - Enabled 1’b0 - Disable Available in BAM only
21	BAM_WB_CSW_ACK_IDL	Recommended value: 1 This bit allows the Writeback state machine to switch into idle state prior to visiting disabled state. This is needed when context switching from mode X to another pipe of mode X is well. This is required to fix a bug in the 2 pipes BAM. 1’b1 - Enable 1’b0 - Disable Available in BAM only
20	BAM_WB_BLK_CSW	Recommended value: 1 When Enabled, this bit does not allow context switch to happen in the Writeback state machine until it has created a descriptor. This is relevant when the descriptor fifo is becoming full and there’s no space to create a descriptor, while another pipe is context switching. This might result in the descriptor not to be created ever, if it was the last one for that pipe. Relevant for Producer BAM-to-BAM mode only. 1’b1 - Enable 1’b0 - Disable Available in BAM only

SDC2_BAM_CNFG_BITS (cont.)

Bits	Name	Description
19	BAM_WB_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Writeback state machine when performing pipe reset. 1'b1 - 1'b0 - Disable Available in BAM only
18	BAM_SI_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Sideband Inform state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
17	BAM_AU_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Ack Update state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
16	BAM_PSM_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Pipe state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
15	BAM_PSM_CSW_REQ	Recommended value: 1 This bit forces the context switch request from pipe state machine to RAM controller not to last longer than the slave requested. (2 Pipes BAM bug fix) 1'b1 - Enable 1'b0 - Disable Available in BAM only
14	BAM_SB_CLK_REQ	Recommended value: 1 This bit allows the clock request from the sideband block to propagate into the BAM's common clock request. 1'b1 - Propagate Sideband Clock Request 1'b0 - Disable Available in BAM only
13	BAM_IBC_DISABLE	Recommended value: 1 This bit helps to save power by allowing the BAM to keep the inactivity base counter in reset when BAM is disabled or when SW configures IBC_DISABLE bit high. 1'b1 - Enable Power Saving 1'b0 - Disable Power Saving

SDC2_BAM_CNFG_BITS (cont.)

Bits	Name	Description
12	BAM_NO_EXT_P_RST	Recommended value: 1 This bit allows the BAM / BAM Lite to ignore the externally connected blocks (eDML) when doing pipe reset. The BAM, once instructed to pipe reset, first thing lets the externally connected block know a reset is needed. Then it waits for the externally connected block to Acknowledge it is ready for the pipe reset (meaning it doesn't push any data for the reset pipe) and then the BAM Lite completes the pipe reset operation internally. When disabled, the BAM doesn't require any Acknowledge from the external block to perform pipe reset. 1’b1 - Enable external block pipe reset 1’b0 - Disable - ignore external block pipe reset
11	BAM_FULL_PIPE	Recommended value: 0 This enables the BAM support for a BAM to BAM Producer which insists to write to a full pipe. When 0, BAM might issue data overflow if producers write to a full pipe. When 1 BAM will not allow this and lower HReady when peripheral tries to do so. Once space is freed in the pipe, Hready will rise and the flow will continue. This functionality has been found to be buggy and was removed from APQ8064. Bit is currently unused. 1’b1 - Enable 1’b0 - Disable Available in BAM only
10:4	RESERVED_BITS10_4	Set to Zero (0)
3	BAM_ADML_SYNC_BRIDGE	0x1: Use a Synchronous Configuration bridge in aDML. 0x0: Use a Asynchronous Configuration bridge in aDML.
2	BAM_PIPE_CNFG	Recommended value: 1 Pipe SM upgrade for writing EOT bit to the previous descriptor. It’s invoked only when EOB arrives in the end of a descriptor. It is highly recommended to set this bit high. Leaving it low might cause incorrect Pipe Bytes Free value reported to peripheral in rare cases. 1’b1 - Enable 1’b0 - Disable Available in BAM only
1	BAM_ADML_DEEP_CONS_FIFO	0x1: Use a deep Consumer FIFO in aDML (16 dwords) 0x0: Use a shallow Consumer FIFO in aDML (8 dwords)
0	BAM_ADML_INCR4_EN_N	0x1: Don’t allow INCR4 aDML-BAM accesses. 0x0: Allow INCR 4 aDML-BAM accesses.

0x12143800+ 128*n SDC2_BAM_IRQ_SRCS_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register has an alias - BAM_IRQ_SRCS register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

SDC2_BAM_IRQ_SRCS_EEn

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12143804+ 128*n SDC2_BAM_IRQ_SRCS_MSK_EEn, n=[0..3]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register has an alias - BAM_IRQ_SRCS_MSK register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

SDC2_BAM_IRQ_SRCS_MSK_EEn

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12143808+ 128*n SDC2_BAM_IRQ_SRCS_UNMASKED_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register has an alias - BAM_IRQ_SRCS_UNMASKED register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

SDC2_BAM_IRQ_SRCS_UNMASKED_EEn

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

20.15.2 BAM PIPE management registers

BAM Pipe management registers control each pipe's parameters. Those reside in physical registers.

0x12142000+ 128*n SDC2_BAM_P_CTRLn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Control register provides various controls for the pipe.

SDC2_BAM_P_CTRLn

Bits	Name	Description
31:11	RESERVED_BITS31_11	Set to Zero (0)
10:9	P_PREFETCH_LIMIT	Bam Lite feature Selects the number of bytes to be pre-fetched by the Bam Lite, once a peripheral requests to read data from a pipe. This feature is relevant for Consumer modes only. 2'b00 - 32 bytes at most (INCR8) 2'b01 - 16 bytes at most (INCR4) 2'b10 - 4 bytes at most (SINGLE) Available in BAM-Lite only

SDC2_BAM_P_CTRLn (cont.)

Bits	Name	Description
8:7	P_AUTO_EOB_SEL	Bam Lite feature. Selects the number of bytes to be processed before creating End Of Block indication internally by the BAM. See P_AUTO_EOB. Descriptors generated by this feature (bam to bam producer mode) will always be of the chosen size, unless an End Of Transfer, causes a smaller descriptor to be created. 2'b00 - 512 Bytes 2'b01 - 256 Bytes 2'b10 - 128 Bytes 2'b11 - 64 Bytes Available in BAM-Lite only
6	P_AUTO_EOB	BAM Lite feature. When Enabled, the BAM Lite will ignore any incoming End Of Block indications from the peripheral (if any). Instead, the BAM Lite will generate it's own End Of Block indications internally, every P_AUTO_EOB_SEL bytes. This feature is relevant for Producer Bam 2 Bam modes only. It is a must for peripherals which are not able to produce End Of Block indications. 1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
5	P_SYS_MODE	This bit sets the pipe to work in System Mode, where the Software is the second side of the pipe. 1'b1 - System mode. 1'b0 - BAM to BAM mode.
4	P_SYS_STRM	Streaming Enable. Relevant to System Producer BAM mode only.When enabled, BAM will not close descriptors with End Of Transfer notifications received from peripheral, but continue writing the data to the same descriptor. 1'b1 - Enable Streaming Mode 1'b0 - None-Streaming Mode
3	P_DIRECTION	This bit denotes pipe direction. 1'b1 - The pipe can be written (producer mode) 1'b0 - The pipe can be read (consumer mode)
2	RESERVED_BITS2	Set to Zero (0)
1	P_EN	1'b1 - Enable Pipe 1'b0 - Disable Pipe
0	RESERVED_BITS0	Set to Zero (0)

0x12142004+ 128*n SDC2_BAM_P_RSTn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Reset register provides Pipe Reset ability. Software needs to write 1 to this register to make the Pipe Reset. Writing 0 to this register will finish the Pipe Reset. Writing zero is needed prior to Peripheral reconfiguration for the same pipe.

SDC2_BAM_P_RSTn

Bits	Name	Description
31:1	RESERVED_BITS31_1	Set to Zero (0)
0	P_SW_RST	This resets the pipe and its' registers, (Both Flip-Flops and RAM). 1'b1 - Reset 1'b0 - Do Nothing

0x12142008+ 128*n SDC2_BAM_P_HALTn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Halt register Enables/Disables the Halt Sequence.

This is a self-modifying register.

SDC2_BAM_P_HALTn

Bits	Name	Description
31:2	RESERVED_BITS31_2	Set to Zero (0)
1	P_PROD_HALTED	This bit is used to inform the Consumer about the Producer being in Halt mode now. This is a part of the Halt procedure. 1'b1 - Sets this bit to 1 1'b0 - Does Nothing This bit will be cleared by the HW.
0	P_HALT	When Enabled, the Pipe will enter Halt Mode. 1'b1 - Enable Halt 1'b0 - Disable Halt For B2B Producer pipes, this bit is self modifying. It doesn't need the SW to clear it.

0x12142030+ 128*n SDC2_BAM_P_TRUST_REGn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

SDC2_BAM_P_TRUST_REGn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_P_VMID	Those bits indicate the VMID value to be used when performing Pipe type accesses to the bus. BAM Type accesses include Pipe MTI, Data and Descriptors.
7:2	RESERVED_BITS7_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_P_EE	This Field Indicates the EE (0,1,2,3) to which the Pipe Interrupt belongs to. The BAM interrupt will fire to the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12142010+ 128*n SDC2_BAM_P_IRQ_STTSn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only. It also has informative bits which are not interrupts.

Clearing the interrupt bits is done by writing to P_IRQ_CLR register.

SDC2_BAM_P_IRQ_STTSn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_IRQ	For producer this interrupt happens whenever the last AHB burst of a transfer happens For Consumer when ack_on_success closes a transfer
4	P_ERR_IRQ	Pipe Error interrupt indicates that an error has happened. TBD: Error reason is not yet defined. Interrupt not in use.
3	P_OUT_OF_DESC_IRQ	Out of descriptors interrupt has several meanings depending on the operation mode: Producer - no free space in the descriptors fifo for adding a descriptor Consumer - no descriptors in the descriptors fifo for processing IO Vectors Producer - No descriptors to read (and therefore no space for data to write to the pipe) IO Vectors Consumer - No descriptors to read (and therefore no data to read from pipe)
2	P_WAKE_IRQ	Wake peripheral interrupt signals the driver to wake up the peripheral (USB for example) for transmission via the current pipe. This interrupt is issued whenever an Event comes to the specific pipe.
1	P_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
0	P_PRCSD_DESC_IRQ	This Interrupt rises when BAM finishes processing an IO Vector which has INT bit selected

0x12142014+128*n SDC2_BAM_P_IRQ_CLRn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

SDC2_BAM_P_IRQ_CLRn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_CLR	1’b1 - Clear 1’b0 - Unchanged
4	P_ERR_CLR	1’b1 - Clear 1’b0 - Unchanged
3	P_OUT_OF_DESC_CLR	1’b1 - Clear 1’b0 - Unchanged

SDC2_BAM_P_IRQ_CLRn (cont.)

Bits	Name	Description
2	P_WAKE_CLR	Clear Wake peripheral interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
1	P_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
0	P_PRCSD_DESC_CLR	Clear Descriptor Processed interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged

0x12142018+ 128*n SDC2_BAM_P_IRQ_ENn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the Pipe Interrupt Status register.

SDC2_BAM_P_IRQ_ENn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_EN	1'b1 - Enable 1'b0 - Disable
4	P_ERR_EN	1'b1 - Enable 1'b0 - Disable
3	P_OUT_OF_DESC_EN	1'b1 - Enable 1'b0 - Disable
2	P_WAKE_EN	Enable Wake peripheral interrupt 1'b1 - Enable 1'b0 - Disable
1	P_TIMER_EN	Enable Inactivity timer Interrupt 1'b1 - Enable 1'b0 - Disable
0	P_PRCSD_DESC_EN	Enable Descriptor Processed Interrupt 1'b1 - Enable 1'b0 - Disable

0x1214201C+ 128*n SDC2_BAM_P_TIMERn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the pipe.

SDC2_BAM_P_TIMERn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12142020+ 128*n SDC2_BAM_P_TIMER_CTRLn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The resolution of the pipe inactivity timers are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the P_TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * P_TIMER_TRSHLD.

SDC2_BAM_P_TIMER_CTRLn

Bits	Name	Description
31	P_TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the P_TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	P_TIMER_RUN	Will be used along with P_TIMER_MODE Not implemented at this time. Set to zero(0)
29	P_TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	P_TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12142024+ 128*n SDC2_BAM_P_PRDCR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Producer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

SDC2_BAM_P_PRDCR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_producer
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	BAM_P_TOGGLE	Pipe Bytes Free Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Free Ctrl value
15:0	BAM_P_BYTES_FREE	Pipe Bytes Free value

0x12142028+ 128*n SDC2_BAM_P_CNSMR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Consumer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

SDC2_BAM_P_CNSMR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_consumer
23	BAM_P_WAIT_4_ACK	waiting_for_ack_bytes_avail_r
22	BAM_P_ACK_TOGGLE	ack_bytes_avail_toggle
21	BAM_P_ACK_TOGGLE_R	ack_bytes_avail_toggle_r
20	BAM_P_TOGGLE	Pipe Bytes Avail Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Avail Ctrl value
15:0	BAM_P_BYTES_AVAIL	Pipe Bytes AVAIL value

20.15.3 BAM PIPE configuration registers (RAM)

BAM Pipe management registers configure each pipes' parameters.

Pipe Address span: currently defining each pipe to have 32 addresses, therefore inter pipe offset is 32*4=128=0x80 bytes.

0x1214302C+ 64*n SDC2_BAM_P_EVNT_DEST_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Event Destination Address which is the address of BAM_P_EVNT_REG in the BAM on the other side of the Pipe.

Producer BAM will send Write Events to this address.

Consumer BAM will send Read Events to this address.

This is relevant only for BAM to BAM modes. In System modes, BAM doesn't issue Write/Read events.

SDC2_BAM_P_EVNT_DEST_ADDRn

Bits	Name	Description
31:0	P_EVNT_DEST_ADDR	Address of the Event Register in the peer BAM (second end of the pipe). Driver will configure this when initializing the pipe.

0x12143018+64*n SDC2_BAM_P_EVNT_REGn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register is where Read/Write events are sent to. If current BAM works as Producer, it will receive Read events into this register from the Consumer. If the Consumer is another BAM, it will write read events to this register. If the Consumer is the Software, it will prepare descriptors in the descriptor FIFO and update the DESC_FIFO_PEER_OFST value in this register.

If current BAM works as Consumer, opposite behavior is assumed.

SDC2_BAM_P_EVNT_REGn

Bits	Name	Description
31:16	P_BYTES_CONSUMED	This field is used only in the B2B mode. It indicates the number of bits consumed by the Consumer. Consumer sends this value to the Producer as a part of a read event, for the Producer to know how many bytes were consumed. When working in System mode, this value should be set to zero. BAM to BAM Producer writes zero in this value.
15:0	P_DESC_FIFO_PEER_OFST	This field indicates the Descriptor Fifo Offset Pointer of the Peer BAM (The BAM or the Software which creates descriptors). For example when current BAM works as consumer for the current pipe, Producer BAM (or the software) updates this value to let the current pipe know about the new descriptors added in the Descriptor Fifo.

0x12143000+64*n SDC2_BAM_P_SW_OFSTSn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register denotes the pointer Offset of the first Not Acknowledged Descriptor. Meaning all Descriptors prior to this one have been processed by the BAM. This register is only used by the Software. After receiving an interrupt, software reads this register in order to know what descriptors has been processed.

When the BAM works as Producer, Software will usually read this value after Descriptor Processed Interrupt or after the End of Transfer Interrupt.

When the BAM works as Consumer, Software will usually read this value after Descriptor Processed Interrupt.

NOTE This is non relevant in BAM to BAM modes.

NOTE Although being Writable, Software should never write to this register.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC2_BAM_P_SW_OFSTSn

Bits	Name	Description
31:16	SW_OFST_IN_DESC	Offset inside the Descriptor. This value is used by the Software only when a BAM is working as System Producer. Then the SW can read this value to know how many Bytes were written to the current descriptor if it was not closed down. This is useful for Streaming mode.
15:0	SW_DESC_OFST	Descriptor FIFO offset.

0x12143024+ 64*n SDC2_BAM_P_DATA_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Beginning of the Data Address space.

This register is non relevant in System Modes.

SDC2_BAM_P_DATA_FIFO_ADDRn

Bits	Name	Description
31:0	P_DATA_FIFO_ADDR	Data Address Space beginning.

0x1214301C+ 64*n SDC2_BAM_P_DESC_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Address of the Descriptor Fifo beginning.

NOTE This register is used by all modes.

SDC2_BAM_P_DESC_FIFO_ADDRn

Bits	Name	Description
31:0	P_DESC_FIFO_ADDR	Address of the Descriptors Fifo. This address must be 8 bytes aligned.

0x12143028+64*n SDC2_BAM_P_EVNT_GEN_TRSHLDn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register configures the threshold value for Read/Write event generation by the BAM towards another BAM. When a BAM pushes/pops this number of bytes to/from the pipe an event to the other BAM will be generated. A counter summing up the bytes pushed/popped is reset when event is issued, thus restarting count for the threshold.

Events are also issued after End Of Transfer received from the peripheral (Producer case), non regarding whether the pushed bytes count has reached the threshold or not.

This register is non relevant in System Modes.

SDC2_BAM_P_EVNT_GEN_TRSHLDn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TRSHLD	Threshold value. The maximum allowed value is 32kByte.

0x12143020+64*n SDC2_BAM_P_FIFO_SIZESn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

The least significant field is the Descriptor Fifo Size.

The most significant field is the Data Fifo Size.

NOTE This Descriptor Fifo Size is used by all modes. The Data Fifo Size is non relevant in System Modes.

SDC2_BAM_P_FIFO_SIZESn

Bits	Name	Description
31:16	P_DATA_FIFO_SIZE	Size of the Data Address Space.
15:0	P_DESC_FIFO_SIZE	Size of the Descriptors Fifo. Must be 8 byte aligned. Each descriptor is 8 bytes. Size of the descriptor fifo must contain an integer number of Descriptors.

20.15.4 BAM PIPE internal state registers (RAM)

BAM Pipe debug registers allow a software look inside on the internal parameters of the BAM State Machines stored in RAM.

Those shouldn't be normally used or altered by the software.

0x12143034+ 64*n SDC2_BAM_P_RETR_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context stored for retransmission.

This is being stored by Ack Update state machine in consumer mode or by the Writeback state machine in producer mode.

This is being loaded by the Writeback state machine when retransmission happens.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC2_BAM_P_RETR_CNTXT_n

Bits	Name	Description
31:16	RETR_DESC_OFST	Descriptor Fifo Offset for retransmission.
15:0	RETR_OFST_IN_DESC	The Offset inside the Descriptor for retransmission.

0x12143038+ 64*n SDC2_BAM_P_SI_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Sideband Inform state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC2_BAM_P_SI_CNTXT_n

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	SI_DESC_OFST	The Descriptor Fifo Offset pointer stored by the Sideband Inform state machine.

0x12143004+ 64*n SDC2_BAM_P_AU_PSM_CNTXT_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Ack Update state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC2_BAM_P_AU_PSM_CNTXT_1_n

Bits	Name	Description
31:16	AU_PSM_ACCUMED	PSM: The acknowledged (EOB/T) number of bytes since last Write Event. AU: The accumulation of the descriptor sizes for the present ack_on_success event. This is never bigger than the ACKED field. Once the ACCUMED values are bigger than Event Threshold, an Event will be issued, the ACKED value will decrease by the ACCUMED size and this value will be zeroed. This also serves as the Bytes Consumed value in the Event.
15:0	AU_ACKED	AU: The left over of the number of bytes that were received via the ack_on_success, that did not cause a descriptor closure. This value is down counting upon issuing Read Event. PSM:

0x12143008+ 64*n SDC2_BAM_P_PSM_CNTXT_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC2_BAM_P_PSM_CNTXT_2_n

Bits	Name	Description
31	PSM_DESC_VALID	The Descriptor Valid bit provided by the Writeback state machine to Pipe state machine.
30	PSM_DESC_IRQ	The Descriptor Interrupt bit provided by the Writeback state machine to pipe state machine.
29	PSM_DESC_IRQ_DONE	The Descriptor Interrupt needed selection bit.
28:25	PSM_GENERAL_BITS	General Context Switch Bits
24:22	PSM_CONS_STATE	State of the Pipe Consumer state machine.
21:19	PSM_PROD_SYS_STATE	State of the Pipe Producer System state machine.
18:16	PSM_PROD_B2B_STATE	State of the Pipe Producer BAM to BAM state machine.
15:0	PSM_DESC_SIZE	The Descriptor Size provided by the Writeback state machine to pipe state machine.

0x1214300C+ 64*n SDC2_BAM_P_PSM_CNTXT_3_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC2_BAM_P_PSM_CNTXT_3_n

Bits	Name	Description
31:0	PSM_DESC_ADDR	The Data Address provided in the current descriptor from the Writeback state machine.

0x12143010+ 64*n SDC2_BAM_P_PSM_CNTXT_4_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC2_BAM_P_PSM_CNTXT_4_n

Bits	Name	Description
31:16	PSM_DESC_OFST	The running Descriptor Fifo Offset of the Writeback state machine
15:0	PSM_SAVED_ACCUMED_SIZE	The Saved Accumulated Size from the Pipe state machine.

0x12143014+64*n SDC2_BAM_P_PSM_CNTXT_5_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC2_BAM_P_PSM_CNTXT_5_n

Bits	Name	Description
31:16	PSM_BLOCK_BYTE_CNT	The Byte count inside the current Block.
15:0	PSM_OFST_IN_DESC	The Offset inside a register. This is used by pipe state machine to compute offset inside a register after retransmission

0x12143030+64*n SDC2_BAM_P_RESERVED_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

SDC2_BAM_P_RESERVED_1_n

Bits	Name	Description
31:0	BAM_P_RES_1	Set to zero (0) Reserved

0x1214303C+64*n SDC2_BAM_P_RESERVED_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

SDC2_BAM_P_RESERVED_2_n

Bits	Name	Description
31:0	BAM_P_RES_2	Set to zero (0) Obsolete Register: BAM_P_IRQ_DEST_ADDRn, n=[0..30]

20.16 SDC3 Registers (0x12180000 SDC3_BASE)

This section contains the SDC3 base registers.

0x12180000 SDC3_MCI_POWER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x00000000

(ARM name: MCIPower)

SDC3_MCI_POWER

Bits	Name	Description
31:7	RESERVED_1	Always reads zero. Writes 'don't care' but by convention write zero.
6	OPEN_DRAIN	MCICMD Output Control. See Note 2 below
5:1	RESERVED_2	Always reads zero. Writes 'don't care' by convention write zero.
0	CONTROL	This register is used to control the operation of the memory controller. value 0: power-off value 1: power-on Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_POWER register and before accessing this register again. Note:2 - This bit is reserved for the use mentioned in the Description but it is not implemented in HW. The open drain mode is preserved such that when enabled, the command output is driven low when the logic is low and undriven (so that the pull up can pull high) when the logic is high. Whether this gets used in the system is up to SW/system but the HW does support this mode.

0x12180004 SDC3_MCI_CLK

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x01008000

(ARM name: MCIClock)

SDC3_MCI_CLK

Bits	Name	Description
31:27	RESERVED_1	Always reads zero. Writes ’don’t care’ but by convention write zero.
26	SDCC_CLK_EXT_EN	Value 0 (default) - sdcc_clkout is driven via the clock pad and external clock can’t be used for testing the cm_dll_sdc4. Value 1- External clock can be used as a test clock.
25	RX_FLOW_TIMING	Configuration bit which selects the cycle which RxFlowControl will be asserted when UHS mode is used Value 0 (default) - RxFlowControl is asserted one clock before the end bit is received in DPSM (NextBlkTCnt in DPSM equals to 1). Value 1 - RxFlowControl is asserted two clocks before the end bit is received in DPSM (NextBlkTCnt in DPSM equals to 2).
24:23	SDC4_MCLK_SEL	Selects the sdc4_mclk - input clock of cm_dll_sdc4 Value 0 - gated version of MCLK Value 1 - feedback clock from CLK pad Value 2 (default) - free running mclk (gated between the transactions)
22	CLK_INV	When set(1), the input clock which is inserted into the input macros is inverted.
21	IO_PAD_PWR_SWITCH	Indication to Pad that power has to be switched from 3.3V to 1.8V.
20	CLK_FB_DLY_SEL	Selects the source of feedback clock used by the controller. Value 1 - output of cm_dll_sdc4 is used as feedback clock Value 0 - feedback clock from CLK pad is used
19:18	SD_DEV_SEL	Select the active device if more than one device are connected in shared bus mode. (range: ’00’ - ’11’).
17	HCLKON_SW_EN	SW enable of AHB clock request of SDCC4. value 0: HW clock request mechanism is used value 1: clock request signal is always high
16:14	SELECT_IN	Select to latch data and command coming in: value 000: on the falling edge of internal MCLK. value 001: on the rising edge of internal MCLK. value 010: using feedback clock (default). value 011: DDR mode - In DDR mode, the SDC_CLK output will be SDCn_APPS_CLK divided by 2. value 100: UHS mode - MCLK is used internally. value 101: UHS mode - divided frequency (MCLK/2) is used internally.
13	INVERT_OUT	Clear (0) to change data and command going out on the falling edge. Set (1) to change data and command going out on the rising edge.
12	FLOW_ENA	Enable flow control: value 0: disable (default) value 1: enable

SDC3_MCI_CLK (cont.)

Bits	Name	Description
11:10	WIDEBUS	Enable wide bus mode: value 00: 1 bit mode value 10: 4 bit mode value 01 or 11: 8 bit mode
9	PWRSAVE	Disable Prime-Cell MCI clock output when bus is idle to save power. value 0: Power save disabled - always enabled if bit 8 is set. value 1: Power save enabled - clock enabled only when bus is active and bit 8 is set.
8	ENABLE	Enable Prime-Cell MCI bus clock: value 0: clock disabled value 1: clock enabled
7:0	RESERVED_2	Always reads zero. Writes 'don't care' but by convention write zero. Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_CLK register and before accessing this register again.

0x12180008 SDC3_MCI_ARGUMENT

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIArgument)

SDC3_MCI_ARGUMENT

Bits	Name	Description
31:0	CMD_ARG	Command argument.

0x1218000C SDC3_MCI_CMD

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x00000000

(ARM name: MMCCommand) CPSM: 'Command Path State Machine'.

SDC3_MCI_CMD

Bits	Name	Description
31:17	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
16	AUTO_CMD19	If set (1), CPSM sends CMD19 automatically before sending CMD17 or CMD18. This sequence is needed for CDR auto-calibration of cm_dll_sdc4.
15	CCS_DISABLE	If set (1), CPSM sends Command_Completion_Signal (CCS) disable sequence to the external CE-ATA device.
14	CCS_ENABLE	If set (1), CPSM waits for CCS from external card CE-ATA device.
13	MCIABORT	Signals the next command will be an abort (stop) command. This bit always read as (0) due to the hardware implementation. See note 2 below.
12	DAT_CMD	If set (1) indicates that this is a Command with Data. See note 2 below.
11	PROG_ENA	If set (1), PROG_DONE status bit will be asserted when busy is de-asserted. This bit is to be used with a stop or status command after a block write is performed. Does not effect CPSM.
10	ENABLE	The action of writing to this register (MCI_CMD) with this bit set (1), triggers CPSM to leave the ’Idle State’.
9	PENDING	If set (1), CPSM waits for ’CmdPend’ from the DPSM before it starts sending a command. See note 3 below.
8	INTERRUPT	If set (1), CPSM disables command timer and waits for interrupt request (Card Response). See note 4 below.
7	LONGRSP	If set (1), receives a 136-bit long response.
6	RESPONSE	If set (1), CPSM waits for a response subject to INTERRUPT above.

SDC3_MCI_CMD (cont.)

Bits	Name	Description
5:0	CMD_INDEX	Command index. Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_CMD register and before accessing this register again. Note 2: These bits don't have any effect on the CPSM. They are used to signal the SDIO Interrupt state machine that a Multi Block (CMD18, CMD25, CMD53, etc.) data transaction is taking place. The DAT_CMD bit signals the start of the data transaction while the MCIABORT bit signals the end. For a pure SD Memory card, these bits are a 'don't care' and should be set to zero by convention. However, some software drivers may chose to manipulate the bits in order to maintain compatibility with Combo cards and/or pure SDIO cards. Note 3: This bit is designed to be used with SD CMD18 (READ_MULTIPLE_BLOCK) and SD CMD25 (WRITE_MULTIPLE_BLOCK) which must be terminated with a SD CMD12 (STOP_TRANSMISSION). After CMD18 or CMD25 is sent, the DPSM is enabled to send or receive data of amount MCI_DATA_LENGTH. After the DPSM finishes the transferring the data, it sends 'CmdPend' to the CPSM and goes idle. When the CPSM receives this signal, it sends the currently loaded command which software would normally establish as CMD12. Note 4: The START, CMD_INDEX, ARGUMENT, and CRC are a total of 48 bits in length. If the INTERRUPT bit is zero, the CPSM will wait (63-47) 16 MCLK ticks for a response before going back to IDLE. If the INTERRUP bit is set, the CPSM will wait indefinitely for a card response.

0x12180010 SDC3_MCI_RESP_CMD

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIRespCmd)

SDC3_MCI_RESP_CMD

Bits	Name	Description
31:6	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
5:0	RESPCMD	Response command index.

0x12180014+4*n SDC3_MCI_RESPn, n=[0..3]

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIResponse0-3). Note that MCIResponse3 has 31 bits; the other three (*RESP0, *RESP1, *RESP2) have 32 bits.

The card status size can be 32 or 127 bits, depending on the response type (see Table 1-2). The most significant bit of the card status is received first. The MCIResponse3 register LSB is always 0.

Table 20-4 MCIResponse and card status size

Description	Short response	Long response
MCIResponse0	Card Status [31:0]	Card status [127:96]
MCIResponse1	Unused	Card status [95:64]
MCIResponse2	Unused	Card status [63:32]
MCIResponse3	Unused	Card status [31:1]

SDC3_MCI_RESPn

Bits	Name	Description
31:0	STATUS	Card status

0x12180024 SDC3_MCI_DATA_TIMER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIDataTimer).

There is no way to disable this timer. The timer starts counting as soon as a transaction is initiated. The time counts in MCLK ticks.

SDC3_MCI_DATA_TIMER

Bits	Name	Description
31:0	DATA_TIME	Data timeout period.

0x12180028 SDC3_MCI_DATA_LENGTH

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIDataLength)

Total number of bytes in the transaction regardless of mode (stream or block). In block mode, must be an exact multiple of block size. During an infinite transfer the value of DATALENGTH should be programmed to 0.

SDC3_MCI_DATA_LENGTH

Bits	Name	Description
31:25	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
24:0	DATALENGTH	Data length value.

0x1218002C SDC3_MCI_DATA_CTL

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x00100000

(ARM name: MCIDataCtrl). Data Path State Machine (DPSM).

SDC3_MCI_DATA_CTL

Bits	Name	Description
31:22	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
21	SW_SDC4_CMD19	The input of cm_dll_sdc4 - sdc4_cmd19 can be driven by SW if AUTO_CMD19 (bit 16 in MCI_CMD) feature is not used. Value 1 - sdc4_cmd19 is driven by SW Value 0 (default) - sdc4_cmd19 is driven by HW
20	RX_DATA_PEND	If set (1), timeout counter will start counting only after the RX command (with data) was sent instead of counting from initialization of DPSM. The feature is enabled by default.

SDC3_MCI_DATA_CTL (cont.)

Bits	Name	Description
19	AUTO_PROG_DONE	If set (1), automatic detection of PROG_DONE condition is executed without sending CMD12, CMD13, CMD52 or any other 'dummy' command. SW should set this bit in the following cases only: 1. When sending CMD53 for SDIO write transaction. 2. When sending CMD24. 3. When sending CMD25 and CMD23 was issued before to inform card about the exact number of blocks to be written. 4. When sending CMD19 for testing bus procedure. CMD12 is not required in this case.
18	INFINITE_TRANSFER	If set (1), infinite transfer is enabled. MCI_DATA_LENGTH register should set to 0 during infinite transfer.
17	DATA_PEND	If set (1), DPSM waits for 'DataPend' from the CPSM before it enables the DPSM. See note 2 below.
16:4	BLOCKSIZE	Data block length in bytes (1 to 4096).
3	DM_ENABLE	Enable DM interface: 0: DM disabled 1: DM enabled
2	MODE	Data transfer mode: 0: block data transfer 1: stream data transfer
1	DIRECTION	Data transfer direction: 0: controller to card 1: card to controller
0	ENABLE	Data transfer enabled. If zero, DPSM unconditionally reset. Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_DATA_CTL register and before accessing this register again. Note 2: This bit is designed to be used with SD CMD24 and CMD25 (WRITE_SINGLE_BLOCK and WRITE_MULTIPLE_BLOCK) to automatically start the DPSM after a normal (non-error) response is received. This register should be written with the enable bit and the pending bit asserted before MCI_CMD is enabled.

0x12180030 SDC3_MCI_DATA_COUNT

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIDataCnt)

NOTE There is no mechanism to ensure that a read of this counter will be accurate as it is not synchronized. The reason being the value read is async to the clock domain in which the reading is done. It is only useful as a debug tool for diagnostic purposes only.

SDC3_MCI_DATA_COUNT

Bits	Name	Description
31:25	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
24:0	DATACOUNT	Value of data counter in MciDPSM block. Represents remaining data of transaction.

0x12180034 SDC3_MCI_STATUS

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x000C0000

(ARM name: MCIStatus)

This register may need exclusion for QCSR POR Test for bits 25 and 22.

Static[30:26], [24:23] and [10:0]

These remain asserted until they are cleared by writing to the appropriate bit in the Clear Register (see MCI_CLEAR)

XCIS

The means used to send the SDIO external-card-interrupt-signal (XCIS) to the SDCC depends on the transfer mode: 1-bit, 4-bit, or 8-bit. Under 1 bit transfer mode, the XCIS has a dedicated physical connection to the SDCC. Hence once it is asserted, it remain at a high level. Under 4 and 8 bit transfer modes, the XCIS is time multiplexed with physical connection data bit 1. The XCIS is recognized as valid during specific time slots on data bit 1 by the SDCC. How this 'recognition' takes places shows up as different behaviors on SDIO_INTR_OPER, SDIO_INTR, and the actual interrupt sent to the ARM through MCI_INT_MASKn.

Special[25]

The SDIO_INTR_OPER indicator reflects the true state of XCIS as it would be observed inside the external SDIO card. As such, there is no bit 25 in MCI_CLEAR. The only way to clear SDIO_INTR_OPER is to clear the appropriate bit in the external card Common Card Control Registers (CCCR). Like 'static' above and 'dynamic' below, bit 25 in MCI_INT_MASKn controls actually sending this indicator value to the ARM. This indicator of XCIS is used for normal SDCC operation.

Special[22]

The SDIO_INTR indicator reflects that there has been a low-to-high transition on the connection as explained under XCIS above. This indicator is cleared via bit 22 of MCI_CLEAR but any low-to-high transition on the connection will set this indicator again. Further note that this indicator is not routed through the MCI_INT_MASKn to the ARM. For bit 22, the raw value of the connection is routed through the MCI_INT_MASKn to the ARM. As this raw connection is not aware of 'specific time slots', the signal sent to the ARM generally toggles in an unpredictable fashion. This

is generally not useful during normal SDCC operation. However, for wake-up with clocks off, the raw connection is desirable.

Dynamic[21:11]

These change state depending on the state of the underlying logic (for example, FIFO full and empty flags are asserted and de-asserted as data while written to the FIFO).

SDC3_MCI_STATUS

Bits	Name	Description
31	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
30	AUTO_CMD19_TIMEOUT	Response or tuning pattern wasn't received after automatic CMD19's transmission. This status bit should be read only if AUTO_CMD19 (MCI_CMD(16)) was set.
29	BOOT_TIMEOUT	Data wasn't received within the valid time (according to MCI_CCS_TIMER) from the start of boot operation.
28	BOOT_ACK_ERR	Acknowledge pattern wasn't received correctly or not within the valid time (according to MCI_ACK_TIMER) from the start of boot operation.
27	BOOT_ACK_REC	Acknowledge pattern was received correctly.
26	CCS_TIMEOUT	CE-ATA Command Completion Signal timeout.
25	SDIO_INTR_OPER	SDIO interrupt indicator for normal operation.
24	ATA_CMD_COMPL	CE-ATA Command Completion Signal has been detected.
23	PROG_DONE	Programming done.
22	SDIO_INTR	SDIO interrupt indicator for wake-up.
21	RXDATA_AVLBL	Data available in receive FIFO. At least 1 word in the RX FIFO. SW can read 1 word only from the FIFO.
20	TXDATA_AVLBL	Data available in transmit FIFO. At least 1 word in the TX FIFO.
19	RXFIFO_EMPTY	Receive FIFO empty. SW can't read FIFO.
18	TXFIFO_EMPTY	Transmit FIFO empty. SW can write 8 words into the FIFO.
17	RXFIFO_FULL	Receive FIFO full. SW can read 8 words from the FIFO.
16	TXFIFO_FULL	Transmit FIFO full. TX FIFO contains 8 words. SW can't write to FIFO.
15	RXFIFO_HALF_FULL	Receive FIFO half full. SW can read 8 words from the FIFO.
14	TXFIFO_HALF_FULL	Transmit FIFO half full. SW can write 8 words into the FIFO.
13	RXACTIVE	Data receive in progress.
12	TXACTIVE	Data transmit in progress.
11	CMD_ACTIVE	Command transfer in progress.
10	DATA_BLK_END	Data block sent / received (CRC check passed).

SDC3_MCI_STATUS (cont.)

Bits	Name	Description
9	START_BIT_ERR	Start Bit Error flag
8	DATAEND	Data end (data counter is zero).
7	CMD_SENT	Command sent (no response required).
6	CMD_RESPONSE_END	Command response received (CRC check passed).
5	RX_OVERRUN	Receive FIFO overrun error.
4	TX_UNDERRUN	Transmit FIFO underrun error.
3	DATA_TIMEOUT	Data timeout.
2	CMD_TIMEOUT	Command response timeout.
1	DATA_CRC_FAIL	Data block sent / received (CRC check failed).
0	CMD_CRC_FAIL	Command response received (CRC check failed).

0x12180038 SDC3_MCI_CLEAR

Type: Write
Clock: SAME_RATE_AS_HCLK

(ARM name: MCIClear)

SDC3_MCI_CLEAR

Bits	Name	Description
31	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
30	AUTO_CMD19_TIMEOUT_CLR	Clears AUTO_CMD19_TIMEOUT flag.
29	BOOT_TIMEOUT_CLR	Clears BOOT_TIMEOUT flag.
28	BOOT_ACK_ERR_CLR	Clears BOOT_ACK_ERR flag.
27	BOOT_ACK_REC_CLR	Clears BOOT_ACK_REC flag.
26	CCS_TIMEOUT_CLR	Clears CCSTimeOut flag.
24	ATA_CMD_COMPL_CLR	Clears AtaCmdCompl flag.
23	PROG_DONE_CLR	Clears ProgDone flag.
22	SDIO_INTR_CLR	Clears SDIOInt flag.
10	DATA_BLK_END_CLR	Clears DataBlockEnd flag.
9	START_BIT_ERR_CLR	Clears StartBitErr flag.
8	DATA_END_CLR	Clears DataEnd flag.
7	CMD_SENT_CLR	Clears commandSent flag.

SDC3_MCI_CLEAR (cont.)

Bits	Name	Description
6	CMD_RESP_END_CLT	Clears CmdRespEnd flag.
5	RX_OVERRUN_CLR	Clears RxOverrunClr flag.
4	TX_UNDERRUN_CLR	Clears TxUnderrun flag.
3	DATA_TIMEOUT_CLR	Clears DataTimeOut flag.
2	CMD_TIMOUT_CLR	Clears CmdTimOutflag.
1	DATA_CRC_FAIL_CLR	Clears DataCrcFail flag.
0	CMD_CRC_FAIL_CLR	Clears CmdCrcFail flag.

0x1218003C+4*n SDC3_MCI_INT_MASKn, n=[0..1]

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIMask0, MCIMask1)

SDC3_MCI_INT_MASKn

Bits	Name	Description
31	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
30	MASK30	MASK AUTO_CMD19_TIMEOUT flag.
29	MASK29	MASK BOOT_TIMEOUT flag.
28	MASK28	MASK BOOT_ACK_ERR flag.
27	MASK27	MASK BOOT_ACK_REC flag.
26	MASK26	MASK CCSTimeOut flag.
25	MASK25	MASK SDIOIntOper flag.
24	MASK24	MASK AtaCmdCompl flag.
23	MASK23	MASK ProgDone flag.
22	MASK22	MASK SDIOInt flag.
21	MASK21	MASK RxDataAvlbl flag.
20	MASK20	MASK TxDataAvlbl flag.
19	MASK19	MASK RxFifoEmpty flag.
18	MASK18	MASK TxFifoEmpty flag.
17	MASK17	MASK RxFifoFull flag.
16	MASK16	MASK TxFifoFull flag.

SDC3_MCI_INT_MASKn (cont.)

Bits	Name	Description
15	MASK15	MASK RxFifoHalfFull flag.
14	MASK14	MASK TxFifoHalfFull flag.
13	MASK13	MASK RxActive flag.
12	MASK12	MASK TxActive flag.
11	MASK11	MASK CmdActive flag.
10	MASK10	MASK DataBlockEnd flag.
9	MASK9	MASK StartBitErr
8	MASK8	MASK DataEnd flag.
7	MASK7	MASK CmdSent flag.
6	MASK6	MASK CmdRespEnd flag.
5	MASK5	MASK RxOverrun flag.
4	MASK4	MASK TxOverrun flag.
3	MASK3	MASK DataTimeOut flag.
2	MASK2	MASK CmdTimeOut flag.
1	MASK1	MASK DataCmdCrcFail flag.
0	MASK0	MASK CmdCrcFail flag.

0x12180044 SDC3_MCI_FIFO_COUNT

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

The SDCC core operates in two clock domains ’ MCLK and HCLK. The CPSM and DPSM operate in MCLK domain and MciFifoDmaCtl (FIFO/DMA Controller) operates in HCLK domain. The MCI_FIFO_COUNT is a counter of FIFO Controller that monitors how many words of data are still needed to be transferred through the FIFO. At the beginning of data transaction the MCI_FIFO_COUNT counter will be loaded with the (MCI_DATA_LENGTH / 4) value and then will count down during the data transaction until it reach zero. This register is only useful for debug purposes and should not be used for normal operation since it does not reflect data which may or may not be in the pipeline.

SDC3_MCI_FIFO_COUNT

Bits	Name	Description
31:24	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
23:0	DATA_COUNT	Remaining data.

0x12180048 SDC3_MCI_BOOT

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

Handling the boot operation.

SDC3_MCI_BOOT

Bits	Name	Description
31:3	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
2	BOOT_ACK_EN	If set to '1' then Host waits for acknowledge pattern after initiating the boot operation.
1	BOOT_EN	When this bit is asserted, the boot operation is initiated in both of the modes.
0	BOOT_MODE	If set to '1' then CMD line is low during the boot operation. If boot_mode = '0', then CMD0 with the argument 0xFFFFFFFA is sent.

0x1218004C SDC3_MCI_BOOT_ACK_TIMER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

Timer for boot operation - the time until receiving the acknowledge pattern.

SDC3_MCI_BOOT_ACK_TIMER

Bits	Name	Description
31:0	BOOT_ACK_TIMER	Timer for counting the cycles from initiating the boot operation until the acknowledge pattern is accepted.

0x12180050 SDC3_MCI_VERSION

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: see below

This register should be excluded for QCSR POR testing.

SDC3_MCI_VERSION

Bits	Name	Description
31:0	MCI_VERSION	SDCC4 core version. This value corresponds to Z according to core release tag: sdcc4_pXqYrZ.

0x12180054 SDC3_MCI_EMULATION_DLY_LINE

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

The register is responsible for handling DCM which is used in emulation supports 256 values of shift intervals so 8 bits are required (0:255). Bits [31:30] are used for emulation purposes only.

The procedure for activating the DCM is:

1. Setting bit 28 - DCM_RESET.
2. Clearing bit 28 - DCM_RESET.
3. Waiting until bit 29 DCM_LOCKED is high.
4. Writing a new phase in SD_CLK_DLY_CTRL field and setting the DCM_START bit (bit 30).

The clock's placement was executed by the DCM when DCM_DONE is asserted.

SDC3_MCI_EMULATION_DLY_LINE

Bits	Name	Description
31	DCM_DONE	The shift process was finished in DCM and CMD19 can be sent towards the card. This is a read-only bit.
30	DCM_START	A new value of SD_CLK_DLY_CTRL is ready. Clears the DCM_DONE bit.
29	DCM_LOCKED	Reading the status of the LOCKED DCM's output which indicates that the output clock is ready for use.
28	DCM_RESET	Driving reset to DCM.
27:8	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
7:0	SD_CLK_DLY_CTRL	Input to DCM block in FPGA (8 bits). Controlling the change of the delay interval. The value's range may be 0-255 in DCM block.

0x12180058 SDC3_MCI_CCS_TIMER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

This register is used for operation with CE-ATA devices. The CCS timer starts to count at the end of SD transaction and it advances with every MCLK clock cycle. In boot operation this register is used for storing the number of cycles from initiating the boot operation until the first data is received.

SDC3_MCI_CCS_TIMER

Bits	Name	Description
31:0	CCS_TIMER	CE-ATA Command Completion Signal timeout period.

0x1218005C SDC3_MCI_RESPONSE_MASK

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC3_MCI_RESPONSE_MASK

Bits	Name	Description
31:0	RESPONSE_MASK	Mask used to verify the 32 status error bits. Active only when the data pending bit is set in the MCI_DATA_CTL register. When bit of this mask is set the corresponding bit from response [39:8] is checked to be 0, i.e., shows there is no error. If all bits from mask shows no error, the DPSM will be activated without waiting for software write.

0x12180060 SDC3_MCI_DLL_CONFIG

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x60006400

SDC3_MCI_DLL_CONFIG

Bits	Name	Description
31	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
30	DLL_RST	Setting this bit to 1 resets cm_dll_sdc4. cm_dll_sdc4 should be reset every time the MCLK frequency is changed.

SDC3_MCI_DLL_CONFIG (cont.)

Bits	Name	Description
29	PDN	Power Down Value 0 - analog blocks are enabled Value 1 - analog blocks are powered down (default)
28	CK_INTP_SEL	Selects interpolator output
27	CK_INTP_EN	Enable clock interpolation for finer resolution
26:24	MCLK_FREQ	Frequency of MCLK Value 000 -100 ’ 112 (MHz) Value 001 -112 ’ 125 Value 010 -125 ’ 137 Value 011 -137 ’ 150 Value 100 -150 ’ 162 Value 101 -162 ’ 175 Value 110 -175 ’ 187 Value 111 -187 ’ 200
23:20	CDR_SELEXT	CDR phase select (gray coded) Value 0000 - phase 0 Value 0001 - phase 1 Value 0011 - phase 2 Value 0010 - phase 3 Value 0110 - phase 4 Value 0111 - phase 5 Value 0101 - phase 6 Value 0100 - phase 7 Value 1000 - phase 8 Value 1001 - phase 9 Value 1011 - phase 10 Value 1010 - phase 11 Value 1110 - phase 12 Value 1111 - phase 13 Value 1101 - phase 14 Value 1100 - phase 15
19	CDR_EXT_EN	Enable external control of cdr phase select
18	CK_OUT_EN	Enable output clock (default value is ’1’)
17	CDR_EN	Enable CDR function
16	DLL_EN	Enable DLL function
15:14	CDR_UPD_RATE	CDR update rate, low pass filtering window of CDR Max update rate: Value 00 - 0.5 MCLK frequency Value 01 - 0.25 MCLK Frequency (default) Value 10 - 0.125 MCLK frequency Value 11 - 1/16 MCLK Frequency

SDC3_MCI_DLL_CONFIG (cont.)

Bits	Name	Description
13:12	DLL_UPD_RATE	DLL update rate Value 00 - sdc4_mclk/10 Value 01 - sdc4_mclk/20 Value 10 - sdc4_mclk/40 (default) Value 11 - sdc4_mclk/80
11:10	DLL_PHASE_DET	DLL phase detector low pass average window Value 00 - 4 cycles Value 01 - 8 cycles (default) Value 10 - 16 cycles Value 11 - 32 cycles
9:8	CDR_ALGORITHM_SEL	CDR algorithm select Value 00 - Edge 1 (default) Value 01 - Edge 2 Value 10 - level Value 11- Constant delay
7:6	CMUX0_SHIFT_PHASE	Clock mux0 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable
5:4	CMUX1_SHIFT_PHASE	Clock mux1 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable
3:2	CMUX2_SHIFT_PHASE	Clock mux2 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable
1:0	CMUX3_SHIFT_PHASE	Clock mux3 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable

0x12180064 SDC3_MCI_DLL_TEST_CTL

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC3_MCI_DLL_TEST_CTL

Bits	Name	Description
31:26	VTH_CTRL	Vth control: change current in delay cell. Higher number means less delay.
25:22	DELTA_VGS_CTRL	dVgs control: change current in delay cell. Higher number means less delay.
21	DLL_BIAS_EXT_EN	Enable dll bias external control Value 0 - disable external control (default) Value 1 - enable external control
20:19	CDR_TEST_CTRL	External input to increment or decrement CDR output phase by 1 step Phase is changed on rising edge of signal. Ex. To increment phase by 2 steps: 10 -> 00 -> 10 Value 00 - hold (default) Value 01 - decrement Value 10 - increment Value 11 - invalid
18	EXT_UP_DN	external control up/dn signal Value 0 - disable (default) Value 1 - enable
17	ATEST_CTRL	atest control Value 0 - disable (default) Value 1 - enable
16:14	ATEST_OUT_MUX_CTRL	Atest output mux control Value 000 - Avss (default) Value 001 - Vth current Value 010 - delta Vgs current Value 011 - Vthn Value 100- Pbias Value 101 - Nbias Value 110 - reserved Value 111 - External bias current
13	DTEST_CTRL	dtest control Value 0 - disable (default) Value 1 - enable

SDC3_MCI_DLL_TEST_CTL (cont.)

Bits	Name	Description
12:10	DTEST_OUT_MUX_CTRL	dtest output mux control. Output signals are paired for measurements Value 000 - sdc4_mclk, sdc4_mclk (default) Value 001 - da_ phout<0>, da_phout<7> Value 010 - da_ phout<3>, da_phout<4> Value 011 - da_phout<0>, da_phout<15> Value 100 - sd4_clk_out, sd4_data_out<0> Value 101 - sd4_clk_out, sd4_data_out<1> Value 110 - sd4_clk_out, sd4_data_out<2> Value 111 - sd4_clk_out, sd4_data_out<3>
9	DLL_TAP_CTRL	Delay line tap control - change number of unit delay cell in each tap Delay value Value 0 - 1 (default) Value 1 - 2
8:7	DLL_CUR_CTRL	Delay line current control - change current mirror ratio in each delay tap Delay value Value 00 - 1x (default) Value 01 - 2x Value 10 - 3x Value 11 - 4x
6	INT_REF_CLK	Value 0 (default) - use internal generated clock for delay line reference Value 1 - use sdc4_mclk for delay line reference
5	FEEDBACK_CLK_EN	Value 0 (default) - enable delay line feedback Value 1 - disable delay line feedback
4:0	RESERVED	These reserved bits can be accessed by the SW and connected to cm_dll_sdc4's input

0x12180068 SDC3_MCI_DLL_STATUS

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC3_MCI_DLL_STATUS

Bits	Name	Description
31:8	RESERVED_1	Always reads zero. Writes 'don't care' but by convention write zero.
7	DLL_LOCK	DLL lock status Value 0 - Not locked Value 1 - Locked

SDC3_MCI_DLL_STATUS (cont.)

Bits	Name	Description
6:3	CDR_PHASE	CDR phase select (gray coded) Value 0000 - phase 0 Value 0001 - phase 1 Value 0011 - phase 2 Value 0010 - phase 3 Value 0110 - phase 4 Value 0111 - phase 5 Value 0101 - phase 6 Value 0100 - phase 7 Value 1000 - phase 8 Value 1001 - phase 9 Value 1011 - phase 10 Value 1010 - phase 11 Value 1110 - phase 12 Value 1111 - phase 13 Value 1101 - phase 14 Value 1100 - phase 15
2	DDLL_COARSE_CAL	Value 1 - done Value 0 - not done
1:0	RESERVED_2	Connected to cm_dll_sdc4's output.

0x1218006C SDC3_MCI_STATUS2

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC3_MCI_STATUS2

Bits	Name	Description
31:1	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
0	MCLK_REG_WR_ACTIVE	Value 0 - No active register write to MCLK domain Value 1 - Active register write to MCLK domain. The bit indicates if a write operation to one of the following registers is in process (synchronization between HCLK and MCLK): MCI_POWER MCI_CLOCK MCI_CMD MCI_DATA_CTL

0x12180070 SDC3_MCI_GENERICS

Type: Read
Clock: SAME_RATE_AS_HCLK

SDC3_MCI_GENERICS

Bits	Name	Description
31:27	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
26:23	SD_DATA_WIDTH	Number of DAT lines Value 4 - 4 DAT lines (SD, SDIO) Value 8 - 8 DAT lines (MMC, eMMC)
22:10	RAM_SIZE	Size of RAM size: Optional Values: 512, 1024, 2048 or 4096 bytes.
9	USE_SPS	Value 1 - BAM and DML are used and USB core is connected to SDCC4, Value 0 - BAM and DML are not used.
8:6	NUM_OF_DEV	Number of eSD or eSDIO devices supported on shared SD bus. Can be set from 1 to 4.
5:1	MAX_PIPES	Number of simultaneous parallel pipes supported by the BAM and attached peripherla pair. Can be set from 1 to 31.
0	USE_DLL_SDC4	Enables the instantiation of cm_dll_sdc4. Value 0 - cm_dll_sdc4 isn't integrated with SDCC4 Value 1 - cm_dll_sdc4 is used with SDCC4.

0x12180080 SDC3_MCI_FIFO

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC3_MCI_FIFO

Bits	Name	Description
31:0	DATA	FIFO data. This register is aliased to 16 words, 0x080 - 0xBC. In SDCC3, an access to the FIFO was executed with 16 words so 16 addresses were defined. However, in SDCC4 only 8 words are used in each burst so only 8 addresses from the range should be used. When writing to the external SD_Card, writes to the data path FIFO. When reading from the external SD_Card, reads from the data path FIFO.

0x121800CC SDC3_MCI_TESTBUS_CONFIG

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

NOTE mclk_mux is the selected internal mclk: the original mclk or divided mclk during divided frequency mode.

Table 20-5 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus0(0)	sdcc_crif_wr_en	hclk
test_bus0(1)	sdcc_crif_rd_en	hclk
test_bus0(2)	sdcc_crif_core_select	hclk
test_bus0(6 downto 3)	sdcc_crif_wr_data[3:0]	hclk
test_bus0(10 downto 7)	sdcc_crif_rd_data[3:0]	hclk
test_bus0(14 downto 11)	sdcc_crif_addr[5:2]	hclk
test_bus0(15)	sdcc_crif_ready	hclk
test_bus0(16)	adm_crci4_ack	-
test_bus0(17)	adm_crci4_req	hclk
test_bus0(18)	rx_fifo_rd_en	hclk
test_bus0(19)	tx_fifo_wr_en	hclk
test_bus0(20)	dm_cnt_rst	hclk
test_bus0(28 downto 21)	ram_addr	mclk_mux
test_bus0(29)	ram_we_n	mclk_mux
test_bus0(30)	ram_cs_n	mclk_mux
test_bus0(31)	rx_fifo_wr_en	mclk_mux
test_bus1(0)	sdcc_crif_wr_en	hclk
test_bus1(1)	sdcc_crif_rd_en	hclk
test_bus1(2)	sdcc_crif_core_select	hclk
test_bus1(6 downto 3)	sdcc_crif_addr[5:2]	hclk
test_bus1(7)	sdcc_crif_ready	hclk
test_bus1(8)	adm_crci4_ack	-
test_bus1(9)	adm_crci4_req	hclk
test_bus1(10)	rx_fifo_rd_en	hclk
test_bus1(11)	tx_fifo_wr_en	hclk
test_bus1(15 downto 12)	req_rw	hclk
test_bus1(16)	DATEnUpdPulse	hclk
test_bus1(17)	LastRxRdDone	hclk
test_bus1(25 downto 18)	ram_addr	mclk_mux

Table 20-5 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus1(26)	ram_we_n	mclk_mux
test_bus1(27)	ram_cs_n	mclk_mux
test_bus1(28)	rx_fifo_wr_en	mclk_mux
test_bus1(29)	ram_reset	mclk_mux
test_bus1(31 downto 30)	pipeline_fill	mclk_mux
test_bus2(2 downto 0)	CPSMState	mclk_mux
test_bus2(3)	CPSMEn	mclk_mux
test_bus2(4)	nIntCMDEN	mclk_mux
test_bus2(5)	iCMDCnt47	mclk_mux
test_bus2(6)	iCRspE	mclk_mux
test_bus2(7)	start_bit_first(CPSM)	mclk_mux
test_bus2(8)	DivLevelCo	mclk_mux
test_bus2(11 downto 9)	DPSMState	mclk_mux
test_bus2(12)	DPSMEn	mclk_mux
test_bus2(13)	inDAT0EN_sel	mclk_mux
test_bus2(14)	inDATEN_sel	mclk_mux
test_bus2(15)	StartBit	mclk_mux
test_bus2(16)	iDEndSet	mclk_mux
test_bus2(17)	iStopBit	mclk_mux
test_bus2(18)	TxFlowCtrlChk	mclk_mux
test_bus2(19)	iTxFlowControl	mclk_mux
test_bus2(27 downto 20)	ram_addr	mclk_mux
test_bus2(28)	ram_we_n	mclk_mux
test_bus2(29)	ram_cs_n	mclk_mux
test_bus2(30)	LastRxRdDoneL	mclk_mux
test_bus2(31)	start_bit_first(DPSM)	mclk_mux
test_bus3(7 downto 0)	DATIN[7:0]	mclk_mux
test_bus3(8)	Valid	mclk_mux
test_bus3(10 downto 9)	VSMState	mclk_mux
test_bus3(11)	CmdStopBit	mclk_mux
test_bus3(13 downto 12)	StopBitDelCnt	mclk_mux
test_bus3(15 downto 14)	CRspESetDelCnt	mclk_mux
test_bus3(16)	mclkenable	mclk_mux
test_bus3(18 downto 17)	isdcc_irq	-
test_bus3(21 downto 19)	DPSMState	mclk_mux
test_bus3(22)	DPSMEn	mclk_mux
test_bus3(23)	inDAT0EN_sel	mclk_mux
test_bus3(24)	inDATEN_sel	mclk_mux

Table 20-5 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus3(25)	StartBit	mclk_mux
test_bus3(26)	iDEndSet	mclk_mux
test_bus3(27)	iStopBit	mclk_mux
test_bus3(28)	TxFlowCtrlChk	mclk_mux
test_bus3(29)	iTxFlowControl	mclk_mux
test_bus3(31)	LastDataWord	mclk_mux
test_bus4(2 downto 0)	CPSMState	mclk_mux
test_bus4(3)	CPSMEn	mclk_mux
test_bus4(4)	nIntCMDEN	mclk_mux
test_bus4(5)	iCRspE	mclk_mux
test_bus4(13 downto 6)	CMDCNT	mclk_mux
test_bus4(14)	start_bit_first(CPSM)	mclk_mux
test_bus4(15)	DivLevelCo	mclk_mux
test_bus4(16)	async_fifo_out_valid	mclk_mux
test_bus4(18 downto 17)	CMDIN	mclk_mux
test_bus4(21 downto 19)	DPSMState	mclk_mux
test_bus4(22)	DPSMEn	mclk_mux
test_bus4(29 downto 23)	BLKTCnt(6 downto 0)	mclk_mux
test_bus4(30)	iCheckProgDone	mclk_mux
test_bus4(31)	iProgDone	mclk_mux
test_bus5(2 downto 0)	DPSMState	mclk_mux
test_bus5(3)	DPSMEn	mclk_mux
test_bus5(4)	inDAT0EN_sel	mclk_mux
test_bus5(5)	inDATEN_sel	mclk_mux
test_bus5(6)	StartBit	mclk_mux
test_bus5(7)	iDEndSet	mclk_mux
test_bus5(8)	iStopBit	mclk_mux
test_bus5(9)	TxFlowCtrlChk	mclk_mux
test_bus5(10)	iTxFlowControl	mclk_mux
test_bus5(11)	LdDataBuffer	mclk_mux
test_bus5(12)	iRxFlowControl	mclk_mux
test_bus5(13)	LastRxRdDone	mclk_mux
test_bus5(14)	inDATEN_high_sel	mclk_mux
test_bus5(15)	inDATEN_low_sel	mclk_mux
test_bus5(16)	async_fifo_out_valid	mclk_mux
test_bus5(17)	LastDataWord	mclk_mux
test_bus5(18)	pipeline_empty	mclk_mux
test_bus5(19)	ShiftNotE	mclk_mux

Table 20-5 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus5(20)	start_bit_first (DPSM)	mclk_mux
test_bus5(21)	DIVLevelCo	mclk_mux
test_bus5(28 downto 22)	BLKTCnt(6:0)	mclk_mux
test_bus5(29)	iCheckProgDone	mclk_mux
test_bus5(30)	iProgDone	mclk_mux
test_bus5(31)	start_bit_last	mclk_mux
test_bus6(7 downto 0)	ram_addr	mclk_mux
test_bus6(8)	ram_we_n	mclk_mux
test_bus6(9)	ram_cs_n	mclk_mux
test_bus6(11 downto 10)	pipeline_fill	mclk_mux
test_bus6(12)	ram_reset	mclk_mux
test_bus6(13)	rx_fifo_wr_en	mclk_mux
test_bus6(14)	rx_fifo_rd_en	hclk
test_bus6(15)	tx_fifo_wr_en	hclk
test_bus6(19 downto 16)	req_rw	hclk
test_bus6(20)	DATEnUpdPulse	hclk
test_bus6(21)	dm_cnt_rst	hclk
test_bus6(25 downto 22)	rx_fifo_rd_word_cnt	hclk
test_bus6(29 downto 26)	tx_fifo_wr_word_cnt	hclk
test_bus6(30)	iLastRxRdDone	hclk
test_bus6(31)	RxActive	hclk
test_bus7(1 downto 0)	CMDIN	mclk_mux
test_bus7(17 downto 2)	DATIN	mclk_mux
test_bus7(18)	div_freq_cnt_cmd_tx	mclk
test_bus7(19)	div_freq_cnt_dat_tx	mclk
test_bus7(20)	div_freq_cnt_rx	mclk
test_bus7(21)	async_fifo_out_valid	mclk
test_bus7(22)	Rising_DAT0EN_5d	mclk
test_bus7(31 downto 23)	async_fifo_rd_data	mclk

SDC3_MCI_TESTBUS_CONFIG

Bits	Name	Description
31:8	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
7:4	SPARE_FIELD	SW spare bits.
3	TESTBUS_ENA	0x1: Enable 0x0: Disable

SDC3_MCI_TESTBUS_CONFIG (cont.)

Bits	Name	Description
2:0	TESTBUS_SEL	These bits select from different test signals. Refer to Table 1-3 for a list of test signals. TESTBUS_SELBus testbus_sel = 0sdcc_test_bus <= test_bus0 testbus_sel = 1 sdcc_test_bus <= test_bus1 testbus_sel = 2sdcc_test_bus <= test_bus2 testbus_sel = 3sdcc_test_bus <= test_bus3 testbus_sel = 4sdcc_test_bus <= test_bus4 testbus_sel = 5sdcc_test_bus <= test_bus5 testbus_sel = 6sdcc_test_bus <= test_bus6 testbus_sel = 7sdcc_test_bus <= test_bus7

0x121800D0 SDC3_MCI_TEST_CTL

Type: Read/Write
Clock: PCLK
Reset State: 0x00000000

(ARM name: MCITCR)

SDC3_MCI_TEST_CTL

Bits	Name	Description
31:4	RESERVED_1	Always reads zero. Writes ’don’t care’ but by convention write zero.
3	REGTEST	Register Test Bit: Set 0: normal mode (default--accesses to the registers are controlled by the hardware protection circuitry) Set 1: test mode (the hardware protection circuitry is bypassed. Normal Write/Read/Write/ Read tests can be performed independently of the link side.
2:1	RESERVED_2	Always reads zero. Writes ’don’t care’ but by convention write zero.
0	ITEN	Integration Test Enable. This bit places PrimeCell MCI in the following modes: Set 0: normal mode Set 1: Integration test mode

0x121800D4 SDC3_MCI_TEST_INPUT

Type: Read
Clock: PCLK

(ARM name: MCIITIP)

SDC3_MCI_TEST_INPUT

Bits	Name	Description
31:10	RESERVED_1	Always reads zero. Writes ’don’t care’ but by convention write zero.
9:6	MCIDATIN_7_4	Reads return the value on the MCIDATIN[7:4] primary inputs.
5	MCICMDIN	Reads return the value on the MCICMDIN primary input.
4:1	MCIDATIN_3_0	Reads return the value on the MCIDATIN[3:0] primary inputs.
0	RESERVED_2	Always reads zero. Writes ’don’t care’ but by convention write zero.

0x121800D8 SDC3_MCI_TEST_OUT

Type: Read/Write
Clock: PCLK

(ARM name: MCIITOP)

SDC3_MCI_TEST_OUT

Bits	Name	Description
31:16	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
15:12	MCIDATOUT_7_4	Primary output. Writes specify the value to be driven on the MCIDATOUT[7:4] primary output in the integration test mode. Reads return the value written into this field.
10	MCICMDOUT	Primary output. Writes specify the value to be driven on the MCICMDOUT primary output in the integration test mode. Reads return the value written into this field.
9:6	MCIDATOUT_3_0	Primary output. Writes specify the value to be driven on the MCIDATOUT[3:0] primary output in the integration test mode. Reads return the value written into this field.
1	MCIINTR1	Intra-chip output. Writes specify the value to be driven on the intra-chip MCIINTR1 output in the integration test mode. This bit is write-only.
0	MCIINTR0	Intra-chip output. Writes specify the value to be driven on the intra-chip MCIINTR0 output in the integration test mode. This bit is write-only.

20.17 SDC3 DML Registers (0x12180800 SDC3_DML_BASE)

This section contains the SDC3 DML registers.

The address field is a relative address. A base will be supplied by the SOC team and documented at the start of the chip SW Manual.

0x12180800 SDC3_DML_CONFIG

Type: Read/Write
Clock: HCLK
Reset State: 0x00010000

SW has the responsibility to set the CRCI SEL fields correctly when both Consumer and Producer sides are enabled at the same time. For example, setting both to 01 or setting both to 10 is an invalid setting if both producer and consumer sides are kicked off. The DML does NOT assume responsibility for incorrect setting of CRCI SEL fields and hence its function is not defined in such cases.

SDC3_DML_CONFIG

Bits	Name	Description
31:19	RESERVED31	reserved
18	INFINITE_CONS_TRANS	If set, this bit means the consumer transaction is of infinite size. Hence the transaction_end_rec signal from BAM will be ignored.
17	DIRECT_MODE	If set, DML is assumed to directly MASTER the AHB bus, in essence, no BAM or BAM is bypassed. This bit value is also routed to the direct_mode hardware port on the DML to be connected to BAM. See Direct_mode_BASE_addr register.
16	BYPASS	If set, the CRCI pairs will be passed through for legacy central DM support. The config AHB slave interface will be directly accessing the peripheral core for config, command and data movement functions. NOTE: The reset value of this bit is `1' which means the DML come out of PoReset in BYPASS state.
15:6	RESERVED15	reserved
5	PRODUCER_BLOCK_END_HPROT2	If set, DML drives high hprot[2] to BAM when block_end is high, else DML drives low hprot[2] to BAM when block_end is high
4	PRODUCER_TRANS_END_EN	When set, transaction_end signal is asserted at the end of DML transaction. When cleared, transaction_end signal is NOT asserted at the end of DML transaction. This feature allows to divide one BAM transaction to two Peripheral transactions.
3:2	CONSUMER_CRCI_SEL	When set to 00, Consumer side is Disabled When set to 01, CRCI-x pair is the consumer CRCI When set to 10, CRCI-y pair is the consumerCRCI If set to 11, its a invalid setting.

SDC3_DML_CONFIG (cont.)

Bits	Name	Description
1:0	PRODUCER_CRCI_SEL	When set to 00, Producer side is Disabled When set to 01, CRCI-x pair is the producer CRCI When set to 10, CRCI-y pair is the producer CRCI If set to 11, its a invalid setting.

0x12180804 SDC3_DML_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00010001

SDC3_DML_STATUS

Bits	Name	Description
31:17	RESERVED31	reserved
16	CONSUMER_IDLE	0x0: Consumer is busy 0x1: Consumer is IDLE
15:1	RESERVED15	reserved
0	PRODUCER_IDLE	0x0: Producer is busy 0x1: Producer is IDLE

0x12180808 SDC3_DML_SW_RESET

Type: Write
Clock: HCLK
Reset State: 0x00000000

A write to this register resets the DML core. All internal state information will be lost and all register values will be reset as well.

SDC3_DML_SW_RESET

Bits	Name	Description
31:0	RESERVED	reserved

0x1218080C SDC3_DML_PRODUCER_START

Type: Write
Clock: HCLK
Reset State: 0x00000000

A write to this register triggers the DML's Producer state machine. No SW register values will be altered. Only the internal counters and settings related to Producer activity will be reset and started afresh. This register should be written to after POR to kick off producer side. This register should also be used to restart the producer once it has reached IDLE state (as indicated by the STATUS register) after completing the current transaction.

SDC3_DML_PRODUCER_START

Bits	Name	Description
31:0	RESERVED	reserved

0x12180810 SDC3_DML_CONSUMER_START

Type: Write
Clock: HCLK
Reset State: 0x00000000

A write to this register triggers the DML's consumer state machine. No SW register values will be altered. Only the internal counters and settings related to consumer activity will be reset and started afresh. This register should be written to after POR to kick off consumer side. This register should also be used to restart the consumer once it has reached IDLE state (as indicated by the STATUS register) after completing the current transaction..

SDC3_DML_CONSUMER_START

Bits	Name	Description
31:0	RESERVED	reserved

0x12180814 SDC3_DML_PRODUCER_PIPE_LOGICAL_SIZE

Type: Write/Read
Clock: HCLK
Reset State: 0x00000000

This register holds the size of the producer pipe (in units of bytes) _to_ which the peripheral can keep writing data to when its the PRODUCER. The value of this register should be consistent with what the BAM registers are programmed with as well. The DML in response to producer side CRCI requests starts writing out data (generated by the Peripheral) from address 0x0 (on its AHB Master Interface). For subsequent Producer side data accesses, the DML keeps on incrementing the address. Upon reaching the max value as indicated by this register, the address rolls over back to 0x0. The address also rolls over back to 0x0 after reaching the end of a transaction.

This register value decides the range of addresses seen on the DML AHB Master address bus during Producer activity.

The value of this register is restricted to any power of two and greater than or equal to the Producer BAM Block Size setting. This is to avoid DML overwriting its own data in the pipe as the data is not committed until block_end is received by the BAM.

The recommended value for this register is 4096(decimal)

SDC3_DML_PRODUCER_PIPE_LOGICAL_SIZE

Bits	Name	Description
31:16	RESERVED31	reserved31
15:0	PRODUCER_LOGICAL_SIZE	The size of the producer pipe (in units of bytes) to which a producer peripheral can keep writing the data it produces.

0x12180818 SDC3_DML_CONSUMER_PIPE_LOGICAL_SIZE

Type: Write/Read
Clock: HCLK
Reset State: 0x00000000

This register holds the size of the consumer pipe (in units of bytes) _from_ which the peripheral can keep _reading_ data from when its the CONSUMER. The value of this register should be consistent with what the BAM registers are programmed with as well. The DML in response to consumer side CRCI requests starts reading out data (needed by the Peripheral) from address 0x0 (on its AHB Master Interface). For subsequent consumer side data accesses, the DML keeps on incrementing the address. Upon reaching the max value as indicated by this register, the address rolls over back to 0x0. The address also rolls over back to 0x0 after reaching the end of a transaction.

This register value decides the range of addresses seen on the DML AHB Master address bus during consumer activity.

The value of this register is restricted to any power of two and no smaller than 32 bytes, that is, no smaller than a "beat-8" burst on a 32 bit AHB.

The recommended value for this register is 4096(decimal)

SDC3_DML_CONSUMER_PIPE_LOGICAL_SIZE

Bits	Name	Description
31:16	RESERVED31	reserved31
15:0	CONSUMER_LOGICAL_SIZE	The size of the consumer pipe (in units of bytes) to which a consumer peripheral can keep reading the data from it needs.

0x1218081C SDC3_DML_PIPE_ID

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register holds pipe IDs that services the producer and consumer side of the peripheral.

- The producer pipe ID is fed to the BAM when servicing the producer side of the peripheral.
- The consumer pipe ID is fed to the BAM when servicing the consumer side of the peripheral.
- The DML also uses this ID value to look into the appropriate side band signals from BAM like pipe_empty, pipe_full etc before initiating the said AHB transaction.

SDC3_DML_PIPE_ID

Bits	Name	Description
31:21	RESERVED31	reserved
20:16	CONSUMER_PIPE_ID	consumer pipe ID
15:5	RESERVED15	reserved
4:0	PRODUCER_PIPE_ID	producer pipe ID

0x12180820 SDC3_DML_PRODUCER_TRACKERS

Type: Read
Clock: HCLK
Reset State: 0x00000000

.This register is for debug purposes only. They reflect the value of the producer block and transaction counters when read. The values may be dynamically changing when a transaction is in progress.

SDC3_DML_PRODUCER_TRACKERS

Bits	Name	Description
31:16	PROD_TRANS_CNT	Value of the 16bit tracker tracking the Producer Transaction Count for the current transaction. Should read 0 at the end of the transaction.
15:0	PROD_BLOCK_CNT	Value of the 16 bit tracker that tracks the Producer Block Count. Need not be zero at the end of transaction.

0x12180824 SDC3_DML_PRODUCER_BAM_BLOCK_SIZE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register holds the "block" size, in units of bytes, associated with the Producer BAM. The DML asserts the block_end side band signal to the BAM whenever the producer side of the peripheral has generated the said amount of data. This register value should be an integral multiple of the Producer CRCI Block Size.

Legal values for Producer BAM Block Size are 64, 128, 192, 256, 512, 1024, 2048 and 4096.

The recommended value for this register is 512(decimal)

SDC3_DML_PRODUCER_BAM_BLOCK_SIZE

Bits	Name	Description
31:16	RESERVED	reserved
15:0	PRODUCER_BLK_SIZE	Size of the one "block" on the producer side in units of bytes.

0x12180828 SDC3_DML_PRODUCER_BAM_TRANS_SIZE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register holds the "transaction" size, in units of bytes, associated with the Producer BAM. The DML asserts the transaction_end side band signal to the BAM whenever the producer side of the peripheral has generated the said amount of data. This signal is asserted only during the address phase of the AHB transaction that carries the last byte corresponding to the size mentioned in this register. Once this value is reached for a given transaction, the address for subsequent data access rolls back to 0x0 and all the block size, CRCI size and transaction size counters also get reset to 0 and start all over again. A value of zero in this register during a producer transaction start means infinite size transaction and hence transaction_end may not get asserted.

This value can be anything up to a maximum of 4294967295 bytes (4 GB -1). If this register value is zero when the DML is started, then an infinite transaction size is assumed. No transaction_end will be generated.

SDC3_DML_PRODUCER_BAM_TRANS_SIZE

Bits	Name	Description
31:0	PRODUCER_TRANS_SIZE	Size of the one "transaction" on the producer side in units of bytes or if zero, then infinite transaction size assumed.

0x1218082C SDC3_DML_DIRECT_MODE_BASE_ADDR

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register is used whenever the DIRECT_MODE bit in config register is set. The programmed 16bits will be used as DML AHB Master address bus MSBits for consumer (AHB read) and producer (AHB Write) operations. The lower 16bits would be dictated by the pipe logical size register.

SDC3_DML_DIRECT_MODE_BASE_ADDR

Bits	Name	Description
31:16	CONSUMER_BASE_ADDR	used as AHB Master address (31:16) when doing direct mode consumer operations if direct_mode bit is set.
15:0	PRODUCER_BASE_ADDR	used as AHB Master address (31:16) when doing direct mode producer operations if direct_mode bit is set.

0x12180830 SDC3_DML_DEBUG

Type: Write/Read
Clock: HCLK
Reset State: 0x00000000

Enables Test Bus of the DML and also selects which side signals to drive the test bus with.

SDC3_DML_DEBUG

Bits	Name	Description
31:2	RESERVED	reserved
1	STATUS_2_SEL	If set, selects the set of signals listed out in DML_BAM_SIDE_STATUS_2 register onto Test bus, else selects set of signals listed out in DML_BAM_SIDE_STATUS_1 register to be muxed onto test bus. Valid only if bit 0 is set.
0	TESTBUS_EN	0x0: Disable Test Bus 0x1: Enable Test Bus

0x12180834 SDC3_DML_BAM_SIDE_STATUS_1

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the instantaneous value of the side band signals with BAM.

SDC3_DML_BAM_SIDE_STATUS_1

Bits	Name	Description
31:24	RESERVED31	reserved
23	ACK_ON_SUCCESS_TOGGLE	for selected consumer pipe
22	ACK_BYTES_AVAIL_TOGGLE	for selected consumer pipe
21	PIPE_BYTES_AVAIL_TOGGLE	for selected consumer pipe
20	TRANSACTION_END_REC	transaction end received for selected consumer pipe.
19	PIPE_BYTES_FREE_TOGGLE	bytes free toggle signal for selected producer pipe
18:3	PIPE_BYTES_FREE	bytes free value for selected producer pipe
2	MESSAGING_ONLY	DML output status
1	TRANSACTION_END	DML output status
0	BLOCK_END	DML output status

0x12180838 SDC3_DML_BAM_SIDE_STATUS_2

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the instantaneous value of the side band signals with BAM.

SDC3_DML_BAM_SIDE_STATUS_2

Bits	Name	Description
31:16	ACK_ON_SUCCESS_TOGGLE_SIZE	for selected consumer pipe
15:0	PIPE_BYTES_AVAIL	for selected consumer pipe

0x1218083C SDC3_DML_RTL_GENERICS_1

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the value of the RTL Generics set during the integration of the DML into a SPS Wrapper or other entity.

SDC3_DML_RTL_GENERICS_1

Bits	Name	Description
31:17	RESERVED31	reserved
16:11	PERIPHERAL_ADDR_WIDTH	represents the width set (in binary format)
10:6	MAX_PIPES	represents the number of pipe value set (in binary format)
5:3	CONSUMER_CRCI_BLK	101:.256 bytes 0x0: 16 bytes 0x1: 32 bytes 0x2: 64 bytes 0x3: 128 bytes 0x4: 192 bytes
2:0	PRODUCER_CRCI_BLK	101:.256 bytes 0x0: 16 bytes 0x1: 32 bytes 0x2: 64 bytes 0x3: 128 bytes 0x4: 192 bytes

0x12180840 SDC3_DML_RTL_GENERICS_2

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the value of the PROD_DMR_RD_ADDR Generic set in RTL during the integration of the DML into a SPS Wrapper or other entity.

SDC3_DML_RTL_GENERICS_2

Bits	Name	Description
31:0	PROD_RD_DMR_ADDR	32bit Value of the PROD_DMR_RD_ADDR generic

0x12180844 SDC3_DML_RTL_GENERICS_3

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the value of the CONS_DMR_WR_ADDR Generic set in RTL during the integration of the DML into a SPS Wrapper or other entity.

SDC3_DML_RTL_GENERICS_3

Bits	Name	Description
31:0	CONS_WR_DMR_ADDR	32bit Value of the CONS_DMR_WR_ADDR generic

0x12180848 SDC3_DML_INTERRUPT_ENABLE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

SDC3_DML_INTERRUPT_ENABLE

Bits	Name	Description
31:1	RESERVED31	reserved
0	PROD_IDLE_START_INTR_EN	Enable DML to generate an interrupt when PRODUCER enters an IDLE state.

0x1218084C SDC3_DML_INTERRUPT_CLEAR

Type: Write
Clock: HCLK
Reset State: 0xXXXXXXXX

SDC3_DML_INTERRUPT_CLEAR

Bits	Name	Description
31:1	RESERVED31	reserved
0	PROD_IDLE_START_INTR_CLR	Clear PROD_IDLE_START_INTR interrupt.

20.18 SDC3 BAM Registers (0x12182000 SDC3_BAM_BASE)

This section contains the SDC3 BAM registers.

BAM supports only Word (4 byte) aligned writes and reads on the Configuration Bus interface.

BAM has MAX_PIPES hardware generic parameter defining the number of pipes it supports. Each BAM can have up to 31 pipes supported.

BAM has BAM_CONF_AHBS_ADDR_WIDTH hardware generic parameter defining the Bit Number for selecting BAM access or Peripheral access. Legal Ranges are 14 to 20. Count starts from 1, meaning a value of 17 will set BAM Base address as 0x0001_0000.

20.18.1 BAM control registers

BAM Control registers configure the BAM operational state, SW reset, interrupts and others.

0x12182F80 SDC3_BAM_CTRL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

BAM Control register allows global controls for the BAM.

SDC3_BAM_CTRL

Bits	Name	Description
31:17	RESERVED_BITS31_17	Set to Zero (0)
16	IBC_DISABLE	This Bit enables power saving by disabling the inactivity clock timer/counter. This is useful when: 1) The BAM is Enabled but idling for long periods. 2) The BAM is Enabled and running but the inactivity timers/counters are not required by the SW for operating the BAM. When the BAM is Disabled, it automatically shuts down those timers to save power. 1’b1 - Enable Power Saving Mode 1’b0 - Disable Power Saving Mode

SDC3_BAM_CTRL (cont.)

Bits	Name	Description
15	BAM_CACHED_DESC_STORE	This Bit enables storage of a cached Descriptor into RAM when doing Context Switch and loading it back when returning to this pipe. This is relevant for System Modes Only. BAM to BAM Consumer mode doesn't have this option. Enabling this makes the Context Switch process slightly longer but reduces AHB Descriptor Fetch time later on. It also reduces the number of descriptor fetches done by the BAM if BAM is treating more than 2 pipes. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
14:13	BAM_DESC_CACHE_SEL	This Selector chooses which Descriptor Caching mode will be used. This is relevant for System Producer or Consumer modes only. 2’b00 - Cache when current descriptor has less than 64 bytes left. 2’b01 - Cache when current descriptor has less than 128 bytes left. 2’b10 - Immediate Auto cache - cache will happen whenever there are no descriptors cached. This might cause unnecessary descriptors reads when switching between more than 2 pipes. It is the most effective when each pipe processes more bytes than there are in an average descriptor (small descriptors, big block size), or when working with 2 or less pipes. 2’b11 - Cache when descriptor is needed only. This results in 1 descriptor present in cache at most. Available in BAM only
12	RESERVED_BITS12	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_SIC_SEL
11:5	BAM_TESTBUS_SEL	Set to Zero (0) Obsolete field: BAM_TESTBUS_SEL Test Bus selector. Supported until (including) bam_p3q3r29 (BlackBird). Moved to a dedicated register - BAM_TEST_BUS_SEL in the following releases.
4	BAM_EN_ACCUM	When Enabled, BAM will accumulate data written by the peripheral in Direct Mode into INCR8 Bursts. This is an optimization feature for Producer Direct Mode cases. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
3	RESERVED_BITS3	Set to Zero (0)
2	RESERVED_BITS2	Set to Zero (0)

SDC3_BAM_CTRL (cont.)

Bits	Name	Description
1	BAM_EN	After reset the BAM wakes up in Disabled Mode. While Disabled, BAM operates in Legacy mode (all the transfers from the peripheral go around the BAM as if it doesn't exist) Software Enables this bit to allow BAM operation. This bit doesn't affect the PIPE enable bit in BAM_P_CTRL register. The only possibility to Disable the BAM after it has been enabled is by Hardware or Software reset. 1'b1 - Enabled 1'b0 - Disabled
0	BAM_SW_RST	This will reset the BAM & all Pipes. Software may use this to reset the BAM. As long as the bit remains high the BAM remains in reset state. Software should clear this bit 1'b1 - Reset state 1'b0 - Normal state

0x12182F84 SDC3_BAM_REVISION

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a hard coded revision number of the BAM RTL. This corresponds to the BAM target number in the IMS. Also additional BAM settings are reflected here.

SDC3_BAM_REVISION

Bits	Name	Description
31:24	INACTIV_TMR_BASE	This indicates the width of the inactivity timers base counter
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	NUM_INACTIV_TMRS	This bit is checked only if INACTIV_TMRS_EXST = 1. This bit indicates how many inactivity timers are implemented according to value of INACTIVITY_TIMERS_SUPPORTED generic: 1'b1 - One timer for global BAM activity (INACTIVITY_TIMERS_SUPPORTED = 1) 1'b0 - MAX_PIPES timers for each pipe activity (INACTIVITY_TIMERS_SUPPORTED = 2)
19	INACTIV_TMRS_EXST	This indicates BAM has inactivity timers. 1'b1 - Timers available (INACTIVITY_TIMERS_SUPPORTED = 1 or 2) 1'b0 - No timers available (INACTIVITY_TIMERS_SUPPORTED = 0)

SDC3_BAM_REVISION (cont.)

Bits	Name	Description
18	HIGH_FREQUENCY_BAM	This indicates BAM has Double Sampling on the Ack On Success interface. 1'b1 - Ack On Success double sampled 1'b0 - No double sampling of Ack On Success
17	BAM_HAS_NO_BYPASS	This field indicates BAM has no bypass on the AHB Data bus, from the Peripheral AHB Master to the fabric. When Bypass is available, it is the default routing when BAM is disabled. 1'b1 - No Bypass 1'b0 - Bypass Exists
16	SECURED	This field indicates BAM/BAM-Lite has security support (APU inside) 1'b1 - Secured 1'b0 - Not Secured
15:12	RESERVED_BITS15_12	Set to Zero (0)
11:8	NUM_EES	This indicates the Number of Interrupt Lines (Execution Environments) supported by the BAM. When 1 EE is supported, only the BAM_IRQ_SRCS*_EE0 registers exist. When 4 EEs are supported, all BAM_IRQ_SRCS*_EEn registers exist for n=[0..3].
7:0	REVISION	This field contains the revision number of the core, Hard Coded. 8'h01 - Voyager (bam_p3q3r22 +) 8'h02 - BlackBird (bam_p3q3r27 +) 8'h03 - Waverider BAM (bam_p3q3r30 +) 8'h04 - Aurora BAM (bam_p3q2r43 +) 8'h05 - Shelby BAM (bam_p2q2r45 +) 8'h10 - Waverider BAM Lite (bam_lite_p1q1r0 +) 8'h11 - Aurora BAM Lite (bam_lite_p3q2r16 +) 8'h12 - Shelby BAM Lite (bam_lite_p2q2r18 +)

0x12182FBC SDC3_BAM_NUM_PIPES

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a the hard coded number of pipes in the BAM. Since each BAM may have a different number of pipes instantiated in HW, this register allows the SW to know this parameter. The reset state value doesn't have any meaning in this register since it is a constant.

SDC3_BAM_NUM_PIPES

Bits	Name	Description
31:24	BAM_NON_PIPE_GRP	This field contains the number of BAM Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
23:16	PERIPH_NON_PIPE_GRP	This field contains the number of Peripheral's Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
15:8	RESERVED_BITS15_8	Set to Zero (0)
7:0	BAM_NUM_PIPES	This field contains the number of pipes available in this BAM

0x12182FC0 SDC3_BAM_TIMER

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the BAM (all the pipes are in idle state).

SDC3_BAM_TIMER

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12182FC4 SDC3_BAM_TIMER_CTRL

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The register can be written and read only when INACTIVITY_TIMERS_SUPPORTED generic equals to 1.

The resolution of the BAM inactivity timer are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define

the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * TIMER_TRSHLD.

SDC3_BAM_TIMER_CTRL

Bits	Name	Description
31	TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1 to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	TIMER_RUN	Will be used along with TIMER_MODE Not implemented at this time. Set to zero(0)
29	TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12182F88 SDC3_BAM_DESC_CNT_TRSHLD

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds a threshold value for the counter summing the Size of the Descriptors Provided. This value is Global for all pipes but it is relevant for System Producer BAM mode and Both Consumer modes, where Descriptors summing takes place in order to provide the information to the peripheral via pipe bytes free (producer) or pipe bytes available interfaces.

SDC3_BAM_DESC_CNT_TRSHLD

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0).
15:0	CNT_TRSHLD	Threshold value. The maximum allowed value is 32kByte. Available in BAM only

0x12182F8C SDC3_BAM_IRQ_SRCS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking out this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register points to the physical BAM_IRQ_SRCS_EE0 register.

SDC3_BAM_IRQ_SRCS

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12182F90 SDC3_BAM_IRQ_SRCS_MSK

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register points to the physical BAM_IRQ_SRCS_MSK_EE0 register.

SDC3_BAM_IRQ_SRCS_MSK

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12182FB0 SDC3_BAM_IRQ_SRCS_UNMASKED

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register points to the physical BAM_IRQ_SRCS_UNMASKED_EE0 register.

SDC3_BAM_IRQ_SRCS_UNMASKED

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

0x12182F94 SDC3_BAM_IRQ_STTS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only.

Clearing the interrupt bits is done by writing to BAM_IRQ_CLR register.

SDC3_BAM_IRQ_STTS

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
3	BAM_EMPTY_IRQ	This interrupt is for DEBUG purpose only. It should not be used in normal SW flows. The interrupt indicates the BAMs buffer is empty. This bit can become high only when BAM_DATA_ERASE or BAM_DATA_FLUSH is high in BAM_TEST_BUS_SEL register.
2	BAM_ERROR_IRQ	This Indicates a Fatal Error has happened in the BAM. Currently this might happen due to an UnSuccessful Pipe Reset operation.

SDC3_BAM_IRQ_STTS (cont.)

Bits	Name	Description
1	BAM_HRESP_ERR_IRQ	This interrupt Indicates that an Erroneous HResponse has been received by the AHB Master. Additional Information about the error may be read at BAM_AHB_MASTER_ERR_* Registers. Clearing this interrupt also clears the BAM_AHB_MASTER_ERR_* Registers. Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12182F98 SDC3_BAM_IRQ_CLR

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

SDC3_BAM_IRQ_CLR

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
3	BAM_EMPTY_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM-Lite only
2	BAM_ERROR_CLR	1'b1 - Clear 1'b0 - Unchanged
1	BAM_HRESP_ERR_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12182F9C SDC3_BAM_IRQ_EN

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the BAM Interrupt Status register.

SDC3_BAM_IRQ_EN

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_EN	Enables Inactivity timer interrupt by writing this bit 1'b1 - Enable 1'b0 - Disable
3	BAM_EMPTY_EN	1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
2	BAM_ERROR_EN	1'b1 - Enable 1'b0 - Disable
1	BAM_HRESP_ERR_EN	1'b1 - Enable 1'b0 - Disable Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12182FA0 SDC3_BAM_RESERVED_1

Type: Read
Clock: BAM_CLK
Reset State: 0x00000000

SDC3_BAM_RESERVED_1

Bits	Name	Description
31	RESERVED_BITS31	Set to Zero (0) Obsolete field: BAM_IRQ_SIC_SEL
30:0	RESERVED_BITS30_0	Set to Zero (0) Obsolete field: P_IRQ_SIC_SEL

0x12182FA4 SDC3_BAM_AHB_MASTER_ERR_CTRLS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

SDC3_BAM_AHB_MASTER_ERR_CTRLS

Bits	Name	Description
31:23	RESERVED_BITS31_16	Set to Zero (0)
22:18	BAM_ERR_HVMID	HVMID
17	BAM_ERR_DIRECT_MODE	DIRECT MODE
16:12	BAM_ERR_HCID	HCID
11:8	BAM_ERR_HPROT	HPROT
7:5	BAM_ERR_HBURST	HBURST
4:3	BAM_ERR_HSIZE	HSIZE
2	BAM_ERR_HWRITE	HWRITE
1:0	BAM_ERR_HTRANS	HTRANS

0x12182FA8 SDC3_BAM_AHB_MASTER_ERR_ADDR

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

SDC3_BAM_AHB_MASTER_ERR_ADDR

Bits	Name	Description
31:0	BAM_ERR_ADDR	HADDR

0x12182FAC SDC3_BAM_AHB_MASTER_ERR_DATA

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

SDC3_BAM_AHB_MASTER_ERR_DATA

Bits	Name	Description
31:0	BAM_ERR_DATA	HDATA

0x12182FB4 SDC3_BAM_RESERVED_2

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

SDC3_BAM_RESERVED_2

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_IRQ_DEST_ADDR

0x12182FB8 SDC3_BAM_RESERVED_3

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

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SDC3_BAM_RESERVED_3

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_DEST_ADDR

0x12182FF0 SDC3_BAM_TRUST_REG

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside - SECURED field in the BAM_REVISION register) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

SDC3_BAM_TRUST_REG

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_VMID	Those bits indicate the VMID value to be used when performing BAM type accesses to the bus. BAM Type accesses include BAM MTI (or Direct Mode accesses, not applicable for BAM Lite)
7	BAM_RST_BLOCK	When enabled, the BAM Global SW reset will not be available for usage. This is in order to deny Global SW reset requests by the Global security group. 1'b1 - Enable 1'b0 - Disable
6:2	RESERVED_BITS6_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_EE	This Field Indicates the EE (0,1,2,3) to which the BAM Interrupt belongs to. The pipe interrupts will fire on the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12182FF4 SDC3_BAM_TEST_BUS_SEL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This is the testbus selector register.

Supported in releases after bam_p3q3r29 (BlackBird).

SDC3_BAM_TEST_BUS_SEL

Bits	Name	Description
31:19	RESERVED_BITS31_19	Set to Zero (0)
18	BAM_DATA_ERASE	When enabled, BAM will be instructed to erase all the data it currently has inside. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Erase 1'b0 - Disabled
17	BAM_DATA_FLUSH	When enabled, BAM will be instructed to flush all the data it currently has inside. BAM will only flush the data once it has enough data and a valid destination for it. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Flush 1'b0 - Disabled
16	BAM_CLK_ALWAYS_ON	This bit controls the BAM to issue 'always on' clock request. 1'b1 - Enable Always On clock request. 1'b0 - Disabled
15:7	RESERVED_BITS15_7	Set to Zero (0)
6:0	BAM_TESTBUS_SEL	Test Bus selector. Values with bit[11] set high are reserved for the BAM Lite integrator to provide testbus from outside of the BAM Lite. For example, eDML testbus may reside at X'100_0000' to X'111_1111' selector values. eDML has no registers thus has no test bus selector, so its test bus is combined with the BAM lite's. BAM provides zeroes on its testbus when external values selected. X'000_0000' - Zeros X'000_0001' - Slave test bus X'000_0010' - Pipe state machine test bus X'000_0011' - Buffer test bus X'000_0100' - Sideband test bus X'000_1101' - Bus Manager test bus X'001_0000' - Reg file test bus X'1''_''''' - BAM Lite sets zeroes on the test bus, leaving it for external use

0x12182FF8 SDC3_BAM_TEST_BUS_REG

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the value being output to the testbus of the chip. It is not intended for SW usage but for lab debugging of the BAM. Values here can change every cycle.

SDC3_BAM_TEST_BUS_REG

Bits	Name	Description
31:0	BAM_TESTBUS_REG	32 bit Testbus value. To select the Block in BAM to show here, use the BAM_TESTBUS_SEL field in BAM_CTRL register.

0x12182FFC SDC3_BAM_CNFG_BITS

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM configuration bits for bug fixes. It is highly recommended to follow the directions for each bit and set it accordingly.

SDC3_BAM_CNFG_BITS

Bits	Name	Description
31:27	RESERVED_BITS31_27	Set to Zero (0)
26	BAM_AU_ACCUMED	Recommended value: 1 This bit fixes a bug in the Ack Update state machine, where an overflow happened while counting descriptors and reaching more than 64kB of calculated sizes. 1'b1 - Enable Fix 1'b0 - Disable Available in BAM only
25	BAM_PSM_P_HD_DATA	Recommended value: 1 This bit allows pipe state machine to ignore retransmission requests if a pipe has just been initialized and process those as a regular fetch request. (consumer modes only). When this bit disabled, BAM could fetch descriptors for a pipe which was reset and no descriptors were added yet, if a retransmission request followed after the reset. 1'b1 - Enable Fix 1'b0 - Disable Available in BAM only

SDC3_BAM_CNFG_BITS (cont.)

Bits	Name	Description
24	BAM_REG_P_EN	Recommended value: 1 This bit fixes the pipe configuration signals mux for the current active pipe in 2 pipes BAM. When disabled, internal state machines might get into enabled states while the pipe is disabled. This would typically happen after pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
23	BAM_WB_DSC_AVL_P_RST	Recommended value: 1 This bit allows the Writeback state machine to reset the vector indicating there are available descriptors when a pipe reset occurs. If disabled, BAM might fetch descriptors after resetting and reconfiguring a pipe, even though no Event (descriptors) was provided.. 1’b1 - Enable 1’b0 - Disable Available in BAM only
22	BAM_WB_RETR_SVPNT	Recommended value: 1 This bit fixes a bug where a pipe which was reset, still stored its retransmission savepoint, but into the illegal’s pipe address space, thus hurting the last pipe of the BAM if the BAM had a total 4, 8 or 16 pipes. This is relevant for Producer to System modes only. (CR-0000151585) 1’b1 - Enabled 1’b0 - Disable Available in BAM only
21	BAM_WB_CSW_ACK_IDL	Recommended value: 1 This bit allows the Writeback state machine to switch into idle state prior to visiting disabled state. This is needed when context switching from mode X to another pipe of mode X is well. This is required to fix a bug in the 2 pipes BAM. 1’b1 - Enable 1’b0 - Disable Available in BAM only
20	BAM_WB_BLK_CSW	Recommended value: 1 When Enabled, this bit does not allow context switch to happen in the Writeback state machine until it has created a descriptor. This is relevant when the descriptor fifo is becoming full and there’s no space to create a descriptor, while another pipe is context switching. This might result in the descriptor not to be created ever, if it was the last one for that pipe. Relevant for Producer BAM-to-BAM mode only. 1’b1 - Enable 1’b0 - Disable Available in BAM only

SDC3_BAM_CNFG_BITS (cont.)

Bits	Name	Description
19	BAM_WB_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Writeback state machine when performing pipe reset. 1'b1 - 1'b0 - Disable Available in BAM only
18	BAM_SI_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Sideband Inform state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
17	BAM_AU_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Ack Update state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
16	BAM_PSM_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Pipe state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
15	BAM_PSM_CSW_REQ	Recommended value: 1 This bit forces the context switch request from pipe state machine to RAM controller not to last longer than the slave requested. (2 Pipes BAM bug fix) 1'b1 - Enable 1'b0 - Disable Available in BAM only
14	BAM_SB_CLK_REQ	Recommended value: 1 This bit allows the clock request from the sideband block to propagate into the BAM's common clock request. 1'b1 - Propagate Sideband Clock Request 1'b0 - Disable Available in BAM only
13	BAM_IBC_DISABLE	Recommended value: 1 This bit helps to save power by allowing the BAM to keep the inactivity base counter in reset when BAM is disabled or when SW configures IBC_DISABLE bit high. 1'b1 - Enable Power Saving 1'b0 - Disable Power Saving

SDC3_BAM_CNFG_BITS (cont.)

Bits	Name	Description
12	BAM_NO_EXT_P_RST	Recommended value: 1 This bit allows the BAM / BAM Lite to ignore the externally connected blocks (eDML) when doing pipe reset. The BAM, once instructed to pipe reset, first thing lets the externally connected block know a reset is needed. Then it waits for the externally connected block to Acknowledge it is ready for the pipe reset (meaning it doesn't push any data for the reset pipe) and then the BAM Lite completes the pipe reset operation internally. When disabled, the BAM doesn't require any Acknowledge from the external block to perform pipe reset. 1’b1 - Enable external block pipe reset 1’b0 - Disable - ignore external block pipe reset
11	BAM_FULL_PIPE	Recommended value: 0 This enables the BAM support for a BAM to BAM Producer which insists to write to a full pipe. When 0, BAM might issue data overflow if producers write to a full pipe. When 1 BAM will not allow this and lower HReady when peripheral tries to do so. Once space is freed in the pipe, Hready will rise and the flow will continue. This functionality has been found to be buggy and was removed from APQ8064. Bit is currently unused. 1’b1 - Enable 1’b0 - Disable Available in BAM only
10:4	RESERVED_BITS10_4	Set to Zero (0)
3	BAM_ADML_SYNC_BRIDGE	0x1: Use a Synchronous Configuration bridge in aDML. 0x0: Use a Asynchronous Configuration bridge in aDML.
2	BAM_PIPE_CNFG	Recommended value: 1 Pipe SM upgrade for writing EOT bit to the previous descriptor. It’s invoked only when EOB arrives in the end of a descriptor. It is highly recommended to set this bit high. Leaving it low might cause incorrect Pipe Bytes Free value reported to peripheral in rare cases. 1’b1 - Enable 1’b0 - Disable Available in BAM only
1	BAM_ADML_DEEP_CONS_FIFO	0x1: Use a deep Consumer FIFO in aDML (16 dwords) 0x0: Use a shallow Consumer FIFO in aDML (8 dwords)
0	BAM_ADML_INCR4_EN_N	0x1: Don’t allow INCR4 aDML-BAM accesses. 0x0: Allow INCR 4 aDML-BAM accesses.

0x12183800+ 128*n SDC3_BAM_IRQ_SRCS_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register has an alias - BAM_IRQ_SRCS register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

SDC3_BAM_IRQ_SRCS_EEn

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12183804+ 128*n SDC3_BAM_IRQ_SRCS_MSK_EEn, n=[0..3]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register has an alias - BAM_IRQ_SRCS_MSK register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

SDC3_BAM_IRQ_SRCS_MSK_EEn

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12183808+ 128*n SDC3_BAM_IRQ_SRCS_UNMASKED_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register has an alias - BAM_IRQ_SRCS_UNMASKED register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

SDC3_BAM_IRQ_SRCS_UNMASKED_EEn

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

20.18.2 BAM PIPE management registers

BAM Pipe management registers control each pipe's parameters. Those reside in physical registers.

0x12182000+ 128*n SDC3_BAM_P_CTRLn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Control register provides various controls for the pipe.

SDC3_BAM_P_CTRLn

Bits	Name	Description
31:11	RESERVED_BITS31_11	Set to Zero (0)
10:9	P_PREFETCH_LIMIT	Bam Lite feature Selects the number of bytes to be pre-fetched by the Bam Lite, once a peripheral requests to read data from a pipe. This feature is relevant for Consumer modes only. 2'b00 - 32 bytes at most (INCR8) 2'b01 - 16 bytes at most (INCR4) 2'b10 - 4 bytes at most (SINGLE) Available in BAM-Lite only

SDC3_BAM_P_CTRLn (cont.)

Bits	Name	Description
8:7	P_AUTO_EOB_SEL	Bam Lite feature. Selects the number of bytes to be processed before creating End Of Block indication internally by the BAM. See P_AUTO_EOB. Descriptors generated by this feature (bam to bam producer mode) will always be of the chosen size, unless an End Of Transfer, causes a smaller descriptor to be created. 2'b00 - 512 Bytes 2'b01 - 256 Bytes 2'b10 - 128 Bytes 2'b11 - 64 Bytes Available in BAM-Lite only
6	P_AUTO_EOB	BAM Lite feature. When Enabled, the BAM Lite will ignore any incoming End Of Block indications from the peripheral (if any). Instead, the BAM Lite will generate it's own End Of Block indications internally, every P_AUTO_EOB_SEL bytes. This feature is relevant for Producer Bam 2 Bam modes only. It is a must for peripherals which are not able to produce End Of Block indications. 1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
5	P_SYS_MODE	This bit sets the pipe to work in System Mode, where the Software is the second side of the pipe. 1'b1 - System mode. 1'b0 - BAM to BAM mode.
4	P_SYS_STRM	Streaming Enable. Relevant to System Producer BAM mode only.When enabled, BAM will not close descriptors with End Of Transfer notifications received from peripheral, but continue writing the data to the same descriptor. 1'b1 - Enable Streaming Mode 1'b0 - None-Streaming Mode
3	P_DIRECTION	This bit denotes pipe direction. 1'b1 - The pipe can be written (producer mode) 1'b0 - The pipe can be read (consumer mode)
2	RESERVED_BITS2	Set to Zero (0)
1	P_EN	1'b1 - Enable Pipe 1'b0 - Disable Pipe
0	RESERVED_BITS0	Set to Zero (0)

0x12182004+ 128*n SDC3_BAM_P_RSTn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Reset register provides Pipe Reset ability. Software needs to write 1 to this register to make the Pipe Reset. Writing 0 to this register will finish the Pipe Reset. Writing zero is needed prior to Peripheral reconfiguration for the same pipe.

SDC3_BAM_P_RSTn

Bits	Name	Description
31:1	RESERVED_BITS31_1	Set to Zero (0)
0	P_SW_RST	This resets the pipe and its' registers, (Both Flip-Flops and RAM). 1'b1 - Reset 1'b0 - Do Nothing

0x12182008+ 128*n SDC3_BAM_P_HALTn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Halt register Enables/Disables the Halt Sequence.

This is a self-modifying register.

SDC3_BAM_P_HALTn

Bits	Name	Description
31:2	RESERVED_BITS31_2	Set to Zero (0)
1	P_PROD_HALTED	This bit is used to inform the Consumer about the Producer being in Halt mode now. This is a part of the Halt procedure. 1'b1 - Sets this bit to 1 1'b0 - Does Nothing This bit will be cleared by the HW.
0	P_HALT	When Enabled, the Pipe will enter Halt Mode. 1'b1 - Enable Halt 1'b0 - Disable Halt For B2B Producer pipes, this bit is self modifying. It doesn't need the SW to clear it.

0x12182030+ 128*n SDC3_BAM_P_TRUST_REGn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

SDC3_BAM_P_TRUST_REGn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_P_VMID	Those bits indicate the VMID value to be used when performing Pipe type accesses to the bus. BAM Type accesses include Pipe MTI, Data and Descriptors.
7:2	RESERVED_BITS7_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_P_EE	This Field Indicates the EE (0,1,2,3) to which the Pipe Interrupt belongs to. The BAM interrupt will fire to the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12182010+ 128*n SDC3_BAM_P_IRQ_STTSn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only. It also has informative bits which are not interrupts.

Clearing the interrupt bits is done by writing to P_IRQ_CLR register.

SDC3_BAM_P_IRQ_STTSn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_IRQ	For producer this interrupt happens whenever the last AHB burst of a transfer happens For Consumer when ack_on_success closes a transfer
4	P_ERR_IRQ	Pipe Error interrupt indicates that an error has happened. TBD: Error reason is not yet defined. Interrupt not in use.
3	P_OUT_OF_DESC_IRQ	Out of descriptors interrupt has several meanings depending on the operation mode: Producer - no free space in the descriptors fifo for adding a descriptor Consumer - no descriptors in the descriptors fifo for processing IO Vectors Producer - No descriptors to read (and therefore no space for data to write to the pipe) IO Vectors Consumer - No descriptors to read (and therefore no data to read from pipe)
2	P_WAKE_IRQ	Wake peripheral interrupt signals the driver to wake up the peripheral (USB for example) for transmission via the current pipe. This interrupt is issued whenever an Event comes to the specific pipe.
1	P_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
0	P_PRCSD_DESC_IRQ	This Interrupt rises when BAM finishes processing an IO Vector which has INT bit selected

0x12182014+128*n SDC3_BAM_P_IRQ_CLRn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

SDC3_BAM_P_IRQ_CLRn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_CLR	1’b1 - Clear 1’b0 - Unchanged
4	P_ERR_CLR	1’b1 - Clear 1’b0 - Unchanged
3	P_OUT_OF_DESC_CLR	1’b1 - Clear 1’b0 - Unchanged

SDC3_BAM_P_IRQ_CLRn (cont.)

Bits	Name	Description
2	P_WAKE_CLR	Clear Wake peripheral interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
1	P_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
0	P_PRCSD_DESC_CLR	Clear Descriptor Processed interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged

0x12182018+128*n SDC3_BAM_P_IRQ_ENn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the Pipe Interrupt Status register.

SDC3_BAM_P_IRQ_ENn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_EN	1'b1 - Enable 1'b0 - Disable
4	P_ERR_EN	1'b1 - Enable 1'b0 - Disable
3	P_OUT_OF_DESC_EN	1'b1 - Enable 1'b0 - Disable
2	P_WAKE_EN	Enable Wake peripheral interrupt 1'b1 - Enable 1'b0 - Disable
1	P_TIMER_EN	Enable Inactivity timer Interrupt 1'b1 - Enable 1'b0 - Disable
0	P_PRCSD_DESC_EN	Enable Descriptor Processed Interrupt 1'b1 - Enable 1'b0 - Disable

0x1218201C+ 128*n SDC3_BAM_P_TIMERn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the pipe.

SDC3_BAM_P_TIMERn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12182020+ 128*n SDC3_BAM_P_TIMER_CTRLn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The resolution of the pipe inactivity timers are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the P_TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * P_TIMER_TRSHLD.

SDC3_BAM_P_TIMER_CTRLn

Bits	Name	Description
31	P_TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the P_TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	P_TIMER_RUN	Will be used along with P_TIMER_MODE Not implemented at this time. Set to zero(0)
29	P_TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	P_TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12182024+ 128*n SDC3_BAM_P_PRDCR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Producer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

SDC3_BAM_P_PRDCR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_producer
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	BAM_P_TOGGLE	Pipe Bytes Free Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Free Ctrl value
15:0	BAM_P_BYTES_FREE	Pipe Bytes Free value

0x12182028+ 128*n SDC3_BAM_P_CNSMR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Consumer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

SDC3_BAM_P_CNSMR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_consumer
23	BAM_P_WAIT_4_ACK	waiting_for_ack_bytes_avail_r
22	BAM_P_ACK_TOGGLE	ack_bytes_avail_toggle
21	BAM_P_ACK_TOGGLE_R	ack_bytes_avail_toggle_r
20	BAM_P_TOGGLE	Pipe Bytes Avail Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Avail Ctrl value
15:0	BAM_P_BYTES_AVAIL	Pipe Bytes AVAIL value

20.18.3 BAM PIPE configuration registers (RAM)

BAM Pipe management registers configure each pipes' parameters.

Pipe Address span: currently defining each pipe to have 32 addresses, therefore inter pipe offset is 32*4=128=0x80 bytes.

0x1218302C+ 64*n SDC3_BAM_P_EVNT_DEST_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Event Destination Address which is the address of BAM_P_EVNT_REG in the BAM on the other side of the Pipe.

Producer BAM will send Write Events to this address.

Consumer BAM will send Read Events to this address.

This is relevant only for BAM to BAM modes. In System modes, BAM doesn't issue Write/Read events.

SDC3_BAM_P_EVNT_DEST_ADDRn

Bits	Name	Description
31:0	P_EVNT_DEST_ADDR	Address of the Event Register in the peer BAM (second end of the pipe). Driver will configure this when initializing the pipe.

0x12183018+64*n SDC3_BAM_P_EVNT_REGn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register is where Read/Write events are sent to. If current BAM works as Producer, it will receive Read events into this register from the Consumer. If the Consumer is another BAM, it will write read events to this register. If the Consumer is the Software, it will prepare descriptors in the descriptor FIFO and update the DESC_FIFO_PEER_OFST value in this register.

If current BAM works as Consumer, opposite behavior is assumed.

SDC3_BAM_P_EVNT_REGn

Bits	Name	Description
31:16	P_BYTES_CONSUMED	This field is used only in the B2B mode. It indicates the number of bits consumed by the Consumer. Consumer sends this value to the Producer as a part of a read event, for the Producer to know how many bytes were consumed. When working in System mode, this value should be set to zero. BAM to BAM Producer writes zero in this value.
15:0	P_DESC_FIFO_PEER_OFST	This field indicates the Descriptor Fifo Offset Pointer of the Peer BAM (The BAM or the Software which creates descriptors). For example when current BAM works as consumer for the current pipe, Producer BAM (or the software) updates this value to let the current pipe know about the new descriptors added in the Descriptor Fifo.

0x12183000+64*n SDC3_BAM_P_SW_OFSTSn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register denotes the pointer Offset of the first Not Acknowledged Descriptor. Meaning all Descriptors prior to this one have been processed by the BAM. This register is only used by the Software. After receiving an interrupt, software reads this register in order to know what descriptors has been processed.

When the BAM works as Producer, Software will usually read this value after Descriptor Processed Interrupt or after the End of Transfer Interrupt.

When the BAM works as Consumer, Software will usually read this value after Descriptor Processed Interrupt.

NOTE This is non relevant in BAM to BAM modes.

NOTE Although being Writable, Software should never write to this register.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC3_BAM_P_SW_OFSTSn

Bits	Name	Description
31:16	SW_OFST_IN_DESC	Offset inside the Descriptor. This value is used by the Software only when a BAM is working as System Producer. Then the SW can read this value to know how many Bytes were written to the current descriptor if it was not closed down. This is useful for Streaming mode.
15:0	SW_DESC_OFST	Descriptor FIFO offset.

0x12183024+ 64*n SDC3_BAM_P_DATA_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Beginning of the Data Address space.

This register is non relevant in System Modes.

SDC3_BAM_P_DATA_FIFO_ADDRn

Bits	Name	Description
31:0	P_DATA_FIFO_ADDR	Data Address Space beginning.

0x1218301C+ 64*n SDC3_BAM_P_DESC_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Address of the Descriptor Fifo beginning.

NOTE This register is used by all modes.

SDC3_BAM_P_DESC_FIFO_ADDRn

Bits	Name	Description
31:0	P_DESC_FIFO_ADDR	Address of the Descriptors Fifo. This address must be 8 bytes aligned.

0x12183028+64*n SDC3_BAM_P_EVNT_GEN_TRSHLDn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register configures the threshold value for Read/Write event generation by the BAM towards another BAM. When aBAM pushes/pops this number of bytes to/from the pipe an event to the other BAM will be generated. A counter summing up the bytes pushed/popped is reset when event is issued, thus restarting count for the threshold.

Events are also issued after End Of Transfer received from the peripheral (Producer case), non regarding whether the pushed bytes count has reached the threshold or not.

This register is non relevant in System Modes.

SDC3_BAM_P_EVNT_GEN_TRSHLDn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TRSHLD	Threshold value. The maximum allowed value is 32kByte.

0x12183020+64*n SDC3_BAM_P_FIFO_SIZESn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

The least significant field is the Descriptor Fifo Size.

The most significant field is the Data Fifo Size.

NOTE This Descriptor Fifo Size is used by all modes. The Data Fifo Size is non relevant in System Modes.

SDC3_BAM_P_FIFO_SIZESn

Bits	Name	Description
31:16	P_DATA_FIFO_SIZE	Size of the Data Address Space.
15:0	P_DESC_FIFO_SIZE	Size of the Descriptors Fifo. Must be 8 byte aligned. Each descriptor is 8 bytes. Size of the descriptor fifo must contain an integer number of Descriptors.

20.18.4 BAM PIPE internal state registers (RAM)

BAM Pipe debug registers allow a software look inside on the internal parameters of the BAM State Machines stored in RAM.

Those shouldn't be normally used or altered by the software.

0x12183034+64*n SDC3_BAM_P_RETR_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context stored for retransmission.

This is being stored by Ack Update state machine in consumer mode or by the Writeback state machine in producer mode.

This is being loaded by the Writeback state machine when retransmission happens.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC3_BAM_P_RETR_CNTXT_n

Bits	Name	Description
31:16	RETR_DESC_OFST	Descriptor Fifo Offset for retransmission.
15:0	RETR_OFST_IN_DESC	The Offset inside the Descriptor for retransmission.

0x12183038+64*n SDC3_BAM_P_SI_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Sideband Inform state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC3_BAM_P_SI_CNTXT_n

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	SI_DESC_OFST	The Descriptor Fifo Offset pointer stored by the Sideband Inform state machine.

0x12183004+ 64*n SDC3_BAM_P_AU_PSM_CNTXT_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Ack Update state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC3_BAM_P_AU_PSM_CNTXT_1_n

Bits	Name	Description
31:16	AU_PSM_ACCUMED	PSM: The acknowledged (EOB/T) number of bytes since last Write Event. AU: The accumulation of the descriptor sizes for the present ack_on_success event. This is never bigger than the ACKED field. Once the ACCUMED values are bigger than Event Threshold, an Event will be issued, the ACKED value will decrease by the ACCUMED size and this value will be zeroed. This also serves as the Bytes Consumed value in the Event.
15:0	AU_ACKED	AU: The left over of the number of bytes that were received via the ack_on_success, that did not cause a descriptor closure. This value is down counting upon issuing Read Event. PSM:

0x12183008+ 64*n SDC3_BAM_P_PSM_CNTXT_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC3_BAM_P_PSM_CNTXT_2_n

Bits	Name	Description
31	PSM_DESC_VALID	The Descriptor Valid bit provided by the Writeback state machine to Pipe state machine.
30	PSM_DESC_IRQ	The Descriptor Interrupt bit provided by the Writeback state machine to pipe state machine.
29	PSM_DESC_IRQ_DONE	The Descriptor Interrupt needed selection bit.
28:25	PSM_GENERAL_BITS	General Context Switch Bits
24:22	PSM_CONS_STATE	State of the Pipe Consumer state machine.
21:19	PSM_PROD_SYS_STATE	State of the Pipe Producer System state machine.
18:16	PSM_PROD_B2B_STATE	State of the Pipe Producer BAM to BAM state machine.
15:0	PSM_DESC_SIZE	The Descriptor Size provided by the Writeback state machine to pipe state machine.

0x1218300C+ 64*n SDC3_BAM_P_PSM_CNTXT_3_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC3_BAM_P_PSM_CNTXT_3_n

Bits	Name	Description
31:0	PSM_DESC_ADDR	The Data Address provided in the current descriptor from the Writeback state machine.

0x12183010+ 64*n SDC3_BAM_P_PSM_CNTXT_4_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC3_BAM_P_PSM_CNTXT_4_n

Bits	Name	Description
31:16	PSM_DESC_OFST	The running Descriptor Fifo Offset of the Writeback state machine
15:0	PSM_SAVED_ACCUMED_SIZE	The Saved Accumulated Size from the Pipe state machine.

0x12183014+64*n SDC3_BAM_P_PSM_CNTXT_5_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC3_BAM_P_PSM_CNTXT_5_n

Bits	Name	Description
31:16	PSM_BLOCK_BYTE_CNT	The Byte count inside the current Block.
15:0	PSM_OFST_IN_DESC	The Offset inside a register. This is used by pipe state machine to compute offset inside a register after retransmission

0x12183030+64*n SDC3_BAM_P_RESERVED_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

SDC3_BAM_P_RESERVED_1_n

Bits	Name	Description
31:0	BAM_P_RES_1	Set to zero (0) Reserved

0x1218303C+64*n SDC3_BAM_P_RESERVED_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

SDC3_BAM_P_RESERVED_2_n

Bits	Name	Description
31:0	BAM_P_RES_2	Set to zero (0) Obsolete Register: BAM_P_IRQ_DEST_ADDRn, n=[0..30]

20.19 SDC4 Registers (0x121C0000 SDC4_BASE)

This section contains the SDC4 base registers.

0x121C0000 SDC4_MCI_POWER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x00000000

(ARM name: MCIPower)

SDC4_MCI_POWER

Bits	Name	Description
31:7	RESERVED_1	Always reads zero. Writes 'don't care' but by convention write zero.
6	OPEN_DRAIN	MCICMD Output Control. See Note 2 below
5:1	RESERVED_2	Always reads zero. Writes 'don't care' by convention write zero.
0	CONTROL	This register is used to control the operation of the memory controller. value 0: power-off value 1: power-on Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_POWER register and before accessing this register again. Note:2 - This bit is reserved for the use mentioned in the Description but it is not implemented in HW. The open drain mode is preserved such that when enabled, the command output is driven low when the logic is low and undriven (so that the pull up can pull high) when the logic is high. Whether this gets used in the system is up to SW/system but the HW does support this mode.

0x121C0004 SDC4_MCI_CLK

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x01008000

(ARM name: MCIClock)

SDC4_MCI_CLK

Bits	Name	Description
31:27	RESERVED_1	Always reads zero. Writes ’don’t care’ but by convention write zero.
26	SDCC_CLK_EXT_EN	Value 0 (default) - sdcc_clkout is driven via the clock pad and external clock can’t be used for testing the cm_dll_sdc4. Value 1- External clock can be used as a test clock.
25	RX_FLOW_TIMING	Configuration bit which selects the cycle which RxFlowControl will be asserted when UHS mode is used Value 0 (default) - RxFlowControl is asserted one clock before the end bit is received in DPSM (NextBlkTCnt in DPSM equals to 1). Value 1 - RxFlowControl is asserted two clocks before the end bit is received in DPSM (NextBlkTCnt in DPSM equals to 2).
24:23	SDC4_MCLK_SEL	Selects the sdc4_mclk - input clock of cm_dll_sdc4 Value 0 - gated version of MCLK Value 1 - feedback clock from CLK pad Value 2 (default) - free running mclk (gated between the transactions)
22	CLK_INV	When set(1), the input clock which is inserted into the input macros is inverted.
21	IO_PAD_PWR_SWITCH	Indication to Pad that power has to be switched from 3.3V to 1.8V.
20	CLK_FB_DLY_SEL	Selects the source of feedback clock used by the controller. Value 1 - output of cm_dll_sdc4 is used as feedback clock Value 0 - feedback clock from CLK pad is used
19:18	SD_DEV_SEL	Select the active device if more than one device are connected in shared bus mode. (range: ’00’ - ’11’).
17	HCLKON_SW_EN	SW enable of AHB clock request of SDCC4. value 0: HW clock request mechanism is used value 1: clock request signal is always high
16:14	SELECT_IN	Select to latch data and command coming in: value 000: on the falling edge of internal MCLK. value 001: on the rising edge of internal MCLK. value 010: using feedback clock (default). value 011: DDR mode - In DDR mode, the SDC_CLK output will be SDCn_APPS_CLK divided by 2. value 100: UHS mode - MCLK is used internally. value 101: UHS mode - divided frequency (MCLK/2) is used internally.
13	INVERT_OUT	Clear (0) to change data and command going out on the falling edge. Set (1) to change data and command going out on the rising edge.
12	FLOW_ENA	Enable flow control: value 0: disable (default) value 1: enable

SDC4_MCI_CLK (cont.)

Bits	Name	Description
11:10	WIDEBUS	Enable wide bus mode: value 00: 1 bit mode value 10: 4 bit mode value 01 or 11: 8 bit mode
9	PWRSAVE	Disable Prime-Cell MCI clock output when bus is idle to save power. value 0: Power save disabled - always enabled if bit 8 is set. value 1: Power save enabled - clock enabled only when bus is active and bit 8 is set.
8	ENABLE	Enable Prime-Cell MCI bus clock: value 0: clock disabled value 1: clock enabled
7:0	RESERVED_2	Always reads zero. Writes 'don't care' but by convention write zero. Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_CLK register and before accessing this register again.

0x121C0008 SDC4_MCI_ARGUMENT

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIArgument)

SDC4_MCI_ARGUMENT

Bits	Name	Description
31:0	CMD_ARG	Command argument.

0x121C000C SDC4_MCI_CMD

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x00000000

(ARM name: MMCCommand) CPSM: 'Command Path State Machine'.

SDC4_MCI_CMD

Bits	Name	Description
31:17	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
16	AUTO_CMD19	If set (1), CPSM sends CMD19 automatically before sending CMD17 or CMD18. This sequence is needed for CDR auto-calibration of cm_dll_sdc4.
15	CCS_DISABLE	If set (1), CPSM sends Command_Completion_Signal (CCS) disable sequence to the external CE-ATA device.
14	CCS_ENABLE	If set (1), CPSM waits for CCS from external card CE-ATA device.
13	MCIABORT	Signals the next command will be an abort (stop) command. This bit always read as (0) due to the hardware implementation. See note 2 below.
12	DAT_CMD	If set (1) indicates that this is a Command with Data. See note 2 below.
11	PROG_ENA	If set (1), PROG_DONE status bit will be asserted when busy is de-asserted. This bit is to be used with a stop or status command after a block write is performed. Does not effect CPSM.
10	ENABLE	The action of writing to this register (MCI_CMD) with this bit set (1), triggers CPSM to leave the ’Idle State’.
9	PENDING	If set (1), CPSM waits for ’CmdPend’ from the DPSM before it starts sending a command. See note 3 below.
8	INTERRUPT	If set (1), CPSM disables command timer and waits for interrupt request (Card Response). See note 4 below.
7	LONGRSP	If set (1), receives a 136-bit long response.
6	RESPONSE	If set (1), CPSM waits for a response subject to INTERRUPT above.

SDC4_MCI_CMD (cont.)

Bits	Name	Description
5:0	CMD_INDEX	Command index. Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_CMD register and before accessing this register again. Note 2: These bits don't have any effect on the CPSM. They are used to signal the SDIO Interrupt state machine that a Multi Block (CMD18, CMD25, CMD53, etc.) data transaction is taking place. The DAT_CMD bit signals the start of the data transaction while the MCIABORT bit signals the end. For a pure SD Memory card, these bits are a 'don't care' and should be set to zero by convention. However, some software drivers may chose to manipulate the bits in order to maintain compatibility with Combo cards and/or pure SDIO cards. Note 3: This bit is designed to be used with SD CMD18 (READ_MULTIPLE_BLOCK) and SD CMD25 (WRITE_MULTIPLE_BLOCK) which must be terminated with a SD CMD12 (STOP_TRANSMISSION). After CMD18 or CMD25 is sent, the DPSM is enabled to send or receive data of amount MCI_DATA_LENGTH. After the DPSM finishes the transferring the data, it sends 'CmdPend' to the CPSM and goes idle. When the CPSM receives this signal, it sends the currently loaded command which software would normally establish as CMD12. Note 4: The START, CMD_INDEX, ARGUMENT, and CRC are a total of 48 bits in length. If the INTERRUPT bit is zero, the CPSM will wait (63-47) 16 MCLK ticks for a response before going back to IDLE. If the INTERRUP bit is set, the CPSM will wait indefinitely for a card response.

0x121C0010 SDC4_MCI_RESP_CMD

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIRespCmd)

SDC4_MCI_RESP_CMD

Bits	Name	Description
31:6	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
5:0	RESPCMD	Response command index.

0x121C0014+4*n SDC4_MCI_RESPn, n=[0..3]

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIResponse0-3). Note that MCIResponse3 has 31 bits; the other three (*RESP0, *RESP1, *RESP2) have 32 bits.

The card status size can be 32 or 127 bits, depending on the response type (see Table 1-2). The most significant bit of the card status is received first. The MCIResponse3 register LSB is always 0.

Table 20-6 MCIResponse and card status size

Description	Short response	Long response
MCIResponse0	Card Status [31:0]	Card status [127:96]
MCIResponse1	Unused	Card status [95:64]
MCIResponse2	Unused	Card status [63:32]
MCIResponse3	Unused	Card status [31:1]

SDC4_MCI_RESPn

Bits	Name	Description
31:0	STATUS	Card status.

0x121C0024 SDC4_MCI_DATA_TIMER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIDataTimer).

There is no way to disable this timer. The timer starts counting as soon as a transaction is initiated. The time counts in MCLK ticks.

SDC4_MCI_DATA_TIMER

Bits	Name	Description
31:0	DATA_TIME	Data timeout period.

0x121C0028 SDC4_MCI_DATA_LENGTH

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIDataLength)

Total number of bytes in the transaction regardless of mode (stream or block). In block mode, must be an exact multiple of block size. During an infinite transfer the value of DATALENGTH should be programmed to 0.

SDC4_MCI_DATA_LENGTH

Bits	Name	Description
31:25	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
24:0	DATALENGTH	Data length value.

0x121C002C SDC4_MCI_DATA_CTL

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x00100000

(ARM name: MCIDataCtrl). Data Path State Machine (DPSM).

SDC4_MCI_DATA_CTL

Bits	Name	Description
31:22	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
21	SW_SDC4_CMD19	The input of cm_dll_sdc4 - sdc4_cmd19 can be driven by SW if AUTO_CMD19 (bit 16 in MCI_CMD) feature is not used. Value 1 - sdc4_cmd19 is driven by SW Value 0 (default) - sdc4_cmd19 is driven by HW
20	RX_DATA_PEND	If set (1), timeout counter will start counting only after the RX command (with data) was sent instead of counting from initialization of DPSM. The feature is enabled by default.

SDC4_MCI_DATA_CTL (cont.)

Bits	Name	Description
19	AUTO_PROG_DONE	If set (1), automatic detection of PROG_DONE condition is executed without sending CMD12, CMD13, CMD52 or any other 'dummy' command. SW should set this bit in the following cases only: 1. When sending CMD53 for SDIO write transaction. 2. When sending CMD24. 3. When sending CMD25 and CMD23 was issued before to inform card about the exact number of blocks to be written. 4. When sending CMD19 for testing bus procedure. CMD12 is not required in this case.
18	INFINITE_TRANSFER	If set (1), infinite transfer is enabled. MCI_DATA_LENGTH register should set to 0 during infinite transfer.
17	DATA_PEND	If set (1), DPSM waits for 'DataPend' from the CPSM before it enables the DPSM. See note 2 below.
16:4	BLOCKSIZE	Data block length in bytes (1 to 4096).
3	DM_ENABLE	Enable DM interface: 0: DM disabled 1: DM enabled
2	MODE	Data transfer mode: 0: block data transfer 1: stream data transfer
1	DIRECTION	Data transfer direction: 0: controller to card 1: card to controller
0	ENABLE	Data transfer enabled. If zero, DPSM unconditionally reset. Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_DATA_CTL register and before accessing this register again. Note 2: This bit is designed to be used with SD CMD24 and CMD25 (WRITE_SINGLE_BLOCK and WRITE_MULTIPLE_BLOCK) to automatically start the DPSM after a normal (non-error) response is received. This register should be written with the enable bit and the pending bit asserted before MCI_CMD is enabled.

0x121C0030 SDC4_MCI_DATA_COUNT

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIDataCnt)

NOTE There is no mechanism to ensure that a read of this counter will be accurate as it is not synchronized. The reason being the value read is async to the clock domain in which the reading is done. It is only useful as a debug tool for diagnostic purposes only.

SDC4_MCI_DATA_COUNT

Bits	Name	Description
31:25	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
24:0	DATACOUNT	Value of data counter in MciDPSM block. Represents remaining data of transaction.

0x121C0034 SDC4_MCI_STATUS

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x000C0000

(ARM name: MCIStatus)

This register may need exclusion for QCSR POR Test for bits 25 and 22.

Static[30:26], [24:23] and [10:0]

These remain asserted until they are cleared by writing to the appropriate bit in the Clear Register (see MCI_CLEAR)

XCIS

The means used to send the SDIO external-card-interrupt-signal (XCIS) to the SDCC depends on the transfer mode: 1-bit, 4-bit, or 8-bit. Under 1 bit transfer mode, the XCIS has a dedicated physical connection to the SDCC. Hence once it is asserted, it remain at a high level. Under 4 and 8 bit transfer modes, the XCIS is time multiplexed with physical connection data bit 1. The XCIS is recognized as valid during specific time slots on data bit 1 by the SDCC. How this 'recognition' takes places shows up as different behaviors on SDIO_INTR_OPER, SDIO_INTR, and the actual interrupt sent to the ARM through MCI_INT_MASKn.

Special[25]

The SDIO_INTR_OPER indicator reflects the true state of XCIS as it would be observed inside the external SDIO card. As such, there is no bit 25 in MCI_CLEAR. The only way to clear SDIO_INTR_OPER is to clear the appropriate bit in the external card Common Card Control Registers (CCCR). Like 'static' above and 'dynamic' below, bit 25 in MCI_INT_MASKn controls actually sending this indicator value to the ARM. This indicator of XCIS is used for normal SDCC operation.

Special[22]

The SDIO_INTR indicator reflects that there has been a low-to-high transition on the connection as explained under XCIS above. This indicator is cleared via bit 22 of MCI_CLEAR but any low-to-high transition on the connection will set this indicator again. Further note that this indicator is not routed through the MCI_INT_MASKn to the ARM. For bit 22, the raw value of the connection is routed through the MCI_INT_MASKn to the ARM. As this raw connection is not aware of 'specific time slots', the signal sent to the ARM generally toggles in an unpredictable fashion. This

is generally not useful during normal SDCC operation. However, for wake-up with clocks off, the raw connection is desirable.

Dynamic[21:11]

These change state depending on the state of the underlying logic (for example, FIFO full and empty flags are asserted and de-asserted as data while written to the FIFO).

SDC4_MCI_STATUS

Bits	Name	Description
31	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
30	AUTO_CMD19_TIMEOUT	Response or tuning pattern wasn't received after automatic CMD19's transmission. This status bit should be read only if AUTO_CMD19 (MCI_CMD(16)) was set.
29	BOOT_TIMEOUT	Data wasn't received within the valid time (according to MCI_CCS_TIMER) from the start of boot operation.
28	BOOT_ACK_ERR	Acknowledge pattern wasn't received correctly or not within the valid time (according to MCI_ACK_TIMER) from the start of boot operation.
27	BOOT_ACK_REC	Acknowledge pattern was received correctly.
26	CCS_TIMEOUT	CE-ATA Command Completion Signal timeout.
25	SDIO_INTR_OPER	SDIO interrupt indicator for normal operation.
24	ATA_CMD_COMPL	CE-ATA Command Completion Signal has been detected.
23	PROG_DONE	Programming done.
22	SDIO_INTR	SDIO interrupt indicator for wake-up.
21	RXDATA_AVLBL	Data available in receive FIFO. At least 1 word in the RX FIFO. SW can read 1 word only from the FIFO.
20	TXDATA_AVLBL	Data available in transmit FIFO. At least 1 word in the TX FIFO.
19	RXFIFO_EMPTY	Receive FIFO empty. SW can't read FIFO.
18	TXFIFO_EMPTY	Transmit FIFO empty. SW can write 8 words into the FIFO.
17	RXFIFO_FULL	Receive FIFO full. SW can read 8 words from the FIFO.
16	TXFIFO_FULL	Transmit FIFO full. TX FIFO contains 8 words. SW can't write to FIFO.
15	RXFIFO_HALF_FULL	Receive FIFO half full. SW can read 8 words from the FIFO.
14	TXFIFO_HALF_FULL	Transmit FIFO half full. SW can write 8 words into the FIFO.
13	RXACTIVE	Data receive in progress.
12	TXACTIVE	Data transmit in progress.
11	CMD_ACTIVE	Command transfer in progress.
10	DATA_BLK_END	Data block sent / received (CRC check passed).

SDC4_MCI_STATUS (cont.)

Bits	Name	Description
9	START_BIT_ERR	Start Bit Error flag
8	DATAEND	Data end (data counter is zero).
7	CMD_SENT	Command sent (no response required).
6	CMD_RESPONSE_END	Command response received (CRC check passed).
5	RX_OVERRUN	Receive FIFO overrun error.
4	TX_UNDERRUN	Transmit FIFO underrun error.
3	DATA_TIMEOUT	Data timeout.
2	CMD_TIMEOUT	Command response timeout.
1	DATA_CRC_FAIL	Data block sent / received (CRC check failed).
0	CMD_CRC_FAIL	Command response received (CRC check failed).

0x121C0038 SDC4_MCI_CLEAR

Type: Write
Clock: SAME_RATE_AS_HCLK

(ARM name: MCIClear)

SDC4_MCI_CLEAR

Bits	Name	Description
31	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
30	AUTO_CMD19_TIMEOUT_CLR	Clears AUTO_CMD19_TIMEOUT flag.
29	BOOT_TIMEOUT_CLR	Clears BOOT_TIMEOUT flag.
28	BOOT_ACK_ERR_CLR	Clears BOOT_ACK_ERR flag.
27	BOOT_ACK_REC_CLR	Clears BOOT_ACK_REC flag.
26	CCS_TIMEOUT_CLR	Clears CCSTimeOut flag.
24	ATA_CMD_COMPL_CLR	Clears AtaCmdCompl flag.
23	PROG_DONE_CLR	Clears ProgDone flag.
22	SDIO_INTR_CLR	Clears SDIOInt flag.
10	DATA_BLK_END_CLR	Clears DataBlockEnd flag.
9	START_BIT_ERR_CLR	Clears StartBitErr flag.
8	DATA_END_CLR	Clears DataEnd flag.
7	CMD_SENT_CLR	Clears commandSent flag.

SDC4_MCI_CLEAR (cont.)

Bits	Name	Description
6	CMD_RESP_END_CLT	Clears CmdRespEnd flag.
5	RX_OVERRUN_CLR	Clears RxOverrunClr flag.
4	TX_UNDERRUN_CLR	Clears TxUnderrun flag.
3	DATA_TIMEOUT_CLR	Clears DataTimeOut flag.
2	CMD_TIMOUT_CLR	Clears CmdTimOutflag.
1	DATA_CRC_FAIL_CLR	Clears DataCrcFail flag.
0	CMD_CRC_FAIL_CLR	Clears CmdCrcFail flag.

0x121C003C+4*n SDC4_MCI_INT_MASKn, n=[0..1]

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIMask0, MCIMask1)

SDC4_MCI_INT_MASKn

Bits	Name	Description
31	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
30	MASK30	MASK AUTO_CMD19_TIMEOUT flag.
29	MASK29	MASK BOOT_TIMEOUT flag.
28	MASK28	MASK BOOT_ACK_ERR flag.
27	MASK27	MASK BOOT_ACK_REC flag.
26	MASK26	MASK CCSTimeOut flag.
25	MASK25	MASK SDIOIntOper flag.
24	MASK24	MASK AtaCmdCompl flag.
23	MASK23	MASK ProgDone flag.
22	MASK22	MASK SDIOInt flag.
21	MASK21	MASK RxDataAvlbl flag.
20	MASK20	MASK TxDataAvlbl flag.
19	MASK19	MASK RxFifoEmpty flag.
18	MASK18	MASK TxFifoEmpty flag.
17	MASK17	MASK RxFifoFull flag.
16	MASK16	MASK TxFifoFull flag.

SDC4_MCI_INT_MASKn (cont.)

Bits	Name	Description
15	MASK15	MASK RxFifoHalfFull flag.
14	MASK14	MASK TxFifoHalfFull flag.
13	MASK13	MASK RxActive flag.
12	MASK12	MASK TxActive flag.
11	MASK11	MASK CmdActive flag.
10	MASK10	MASK DataBlockEnd flag.
9	MASK9	MASK StartBitErr
8	MASK8	MASK DataEnd flag.
7	MASK7	MASK CmdSent flag.
6	MASK6	MASK CmdRespEnd flag.
5	MASK5	MASK RxOverrun flag.
4	MASK4	MASK TxOverrun flag.
3	MASK3	MASK DataTimeOut flag.
2	MASK2	MASK CmdTimeOut flag.
1	MASK1	MASK DataCmdCrcFail flag.
0	MASK0	MASK CmdCrcFail flag.

0x121C0044 SDC4_MCI_FIFO_COUNT

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

The SDCC core operates in two clock domains ’ MCLK and HCLK. The CPSM and DPSM operate in MCLK domain and MciFifoDmaCtl (FIFO/DMA Controller) operates in HCLK domain. The MCI_FIFO_COUNT is a counter of FIFO Controller that monitors how many words of data are still needed to be transferred through the FIFO. At the beginning of data transaction the MCI_FIFO_COUNT counter will be loaded with the (MCI_DATA_LENGTH / 4) value and then will count down during the data transaction until it reach zero. This register is only useful for debug purposes and should not be used for normal operation since it does not reflect data which may or may not be in the pipeline.

SDC4_MCI_FIFO_COUNT

Bits	Name	Description
31:24	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
23:0	DATA_COUNT	Remaining data.

0x121C0048 SDC4_MCI_BOOT

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

Handling the boot operation.

SDC4_MCI_BOOT

Bits	Name	Description
31:3	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
2	BOOT_ACK_EN	If set to '1' then Host waits for acknowledge pattern after initiating the boot operation.
1	BOOT_EN	When this bit is asserted, the boot operation is initiated in both of the modes.
0	BOOT_MODE	If set to '1' then CMD line is low during the boot operation. If boot_mode = '0', then CMD0 with the argument 0xFFFFFFFA is sent.

0x121C004C SDC4_MCI_BOOT_ACK_TIMER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

Timer for boot operation - the time until receiving the acknowledge pattern.

SDC4_MCI_BOOT_ACK_TIMER

Bits	Name	Description
31:0	BOOT_ACK_TIMER	Timer for counting the cycles from initiating the boot operation until the acknowledge pattern is accepted.

0x121C0050 SDC4_MCI_VERSION

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: see below

This register should be excluded for QCSR POR testing.

SDC4_MCI_VERSION

Bits	Name	Description
31:0	MCI_VERSION	SDCC4 core version. This value corresponds to Z according to core release tag: sdcc4_pXqYrZ.

0x121C0054 SDC4_MCI_EMULATION_DLY_LINE

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

The register is responsible for handling DCM which is used in emulation supports 256 values of shift intervals so 8 bits are required (0:255). Bits [31:30] are used for emulation purposes only.

The procedure for activating the DCM is:

1. Setting bit 28 - DCM_RESET.
2. Clearing bit 28 - DCM_RESET.
3. Waiting until bit 29 DCM_LOCKED is high.
4. Writing a new phase in SD_CLK_DLY_CTRL field and setting the DCM_START bit (bit 30).

The clock's placement was executed by the DCM when DCM_DONE is asserted.

SDC4_MCI_EMULATION_DLY_LINE

Bits	Name	Description
31	DCM_DONE	The shift process was finished in DCM and CMD19 can be sent towards the card. This is a read-only bit.
30	DCM_START	A new value of SD_CLK_DLY_CTRL is ready. Clears the DCM_DONE bit.
29	DCM_LOCKED	Reading the status of the LOCKED DCM's output which indicates that the output clock is ready for use.
28	DCM_RESET	Driving reset to DCM.
27:8	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
7:0	SD_CLK_DLY_CTRL	Input to DCM block in FPGA (8 bits). Controlling the change of the delay interval. The value's range may be 0-255 in DCM block.

0x121C0058 SDC4_MCI_CCS_TIMER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

This register is used for operation with CE-ATA devices. The CCS timer starts to count at the end of SD transaction and it advances with every MCLK clock cycle. In boot operation this register is used for storing the number of cycles from initiating the boot operation until the first data is received.

SDC4_MCI_CCS_TIMER

Bits	Name	Description
31:0	CCS_TIMER	CE-ATA Command Completion Signal timeout period.

0x121C005C SDC4_MCI_RESPONSE_MASK

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC4_MCI_RESPONSE_MASK

Bits	Name	Description
31:0	RESPONSE_MASK	Mask used to verify the 32 status error bits. Active only when the data pending bit is set in the MCI_DATA_CTL register. When bit of this mask is set the corresponding bit from response [39:8] is checked to be , i.e., shows there is no error. If all bits from mask shows no error, the DPSM will be activated without waiting for software write.

0x121C0060 SDC4_MCI_DLL_CONFIG

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x60006400

SDC4_MCI_DLL_CONFIG

Bits	Name	Description
31	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
30	DLL_RST	Setting this bit to 1 resets cm_dll_sdc4. cm_dll_sdc4 should be reset every time the MCLK frequency is changed.

SDC4_MCI_DLL_CONFIG (cont.)

Bits	Name	Description
29	PDN	Power Down Value 0 - analog blocks are enabled Value 1 - analog blocks are powered down (default)
28	CK_INTP_SEL	Selects interpolator output
27	CK_INTP_EN	Enable clock interpolation for finer resolution
26:24	MCLK_FREQ	Frequency of MCLK Value 000 -100 ’ 112 (MHz) Value 001 -112 ’ 125 Value 010 -125 ’ 137 Value 011 -137 ’ 150 Value 100 -150 ’ 162 Value 101 -162 ’ 175 Value 110 -175 ’ 187 Value 111 -187 ’ 200
23:20	CDR_SELEXT	CDR phase select (gray coded) Value 0000 - phase 0 Value 0001 - phase 1 Value 0011 - phase 2 Value 0010 - phase 3 Value 0110 - phase 4 Value 0111 - phase 5 Value 0101 - phase 6 Value 0100 - phase 7 Value 1000 - phase 8 Value 1001 - phase 9 Value 1011 - phase 10 Value 1010 - phase 11 Value 1110 - phase 12 Value 1111 - phase 13 Value 1101 - phase 14 Value 1100 - phase 15
19	CDR_EXT_EN	Enable external control of cdr phase select
18	CK_OUT_EN	Enable output clock (default value is ’1’)
17	CDR_EN	Enable CDR function
16	DLL_EN	Enable DLL function
15:14	CDR_UPD_RATE	CDR update rate, low pass filtering window of CDR Max update rate: Value 00 - 0.5 MCLK frequency Value 01 - 0.25 MCLK Frequency (default) Value 10 - 0.125 MCLK frequency Value 11 - 1/16 MCLK Frequency

SDC4_MCI_DLL_CONFIG (cont.)

Bits	Name	Description
13:12	DLL_UPD_RATE	DLL update rate Value 00 - sdc4_mclk/10 Value 01 - sdc4_mclk/20 Value 10 - sdc4_mclk/40 (default) Value 11 - sdc4_mclk/80
11:10	DLL_PHASE_DET	DLL phase detector low pass average window Value 00 - 4 cycles Value 01 - 8 cycles (default) Value 10 - 16 cycles Value 11 - 32 cycles
9:8	CDR_ALGORITHM_SEL	CDR algorithm select Value 00 - Edge 1 (default) Value 01 - Edge 2 Value 10 - level Value 11- Constant delay
7:6	CMUX0_SHIFT_PHASE	Clock mux0 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable
5:4	CMUX1_SHIFT_PHASE	Clock mux1 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable
3:2	CMUX2_SHIFT_PHASE	Clock mux2 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable
1:0	CMUX3_SHIFT_PHASE	Clock mux3 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable

0x121C0064 SDC4_MCI_DLL_TEST_CTL

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC4_MCI_DLL_TEST_CTL

Bits	Name	Description
31:26	VTH_CTRL	Vth control: change current in delay cell. Higher number means less delay.
25:22	DELTA_VGS_CTRL	dVgs control: change current in delay cell. Higher number means less delay.
21	DLL_BIAS_EXT_EN	Enable dll bias external control Value 0 - disable external control (default) Value 1 - enable external control
20:19	CDR_TEST_CTRL	External input to increment or decrement CDR output phase by 1 step Phase is changed on rising edge of signal. Ex. To increment phase by 2 steps: 10 -> 00 -> 10 Value 00 - hold (default) Value 01 - decrement Value 10 - increment Value 11 - invalid
18	EXT_UP_DN	external control up/dn signal Value 0 - disable (default) Value 1 - enable
17	ATEST_CTRL	atest control Value 0 - disable (default) Value 1 - enable
16:14	ATEST_OUT_MUX_CTRL	Atest output mux control Value 000 - Avss (default) Value 001 - Vth current Value 010 - delta Vgs current Value 011 - Vthn Value 100- Pbias Value 101 - Nbias Value 110 - reserved Value 111 - External bias current
13	DTEST_CTRL	dtest control Value 0 - disable (default) Value 1 - enable

SDC4_MCI_DLL_TEST_CTL (cont.)

Bits	Name	Description
12:10	DTEST_OUT_MUX_CTRL	dtest output mux control. Output signals are paired for measurements Value 000 - sdc4_mclk, sdc4_mclk (default) Value 001 - da_ phout<0>, da_phout<7> Value 010 - da_ phout<3>, da_phout<4> Value 011 - da_phout<0>, da_phout<15> Value 100 - sd4_clk_out, sd4_data_out<0> Value 101 - sd4_clk_out, sd4_data_out<1> Value 110 - sd4_clk_out, sd4_data_out<2> Value 111 - sd4_clk_out, sd4_data_out<3>
9	DLL_TAP_CTRL	Delay line tap control - change number of unit delay cell in each tap Delay value Value 0 - 1 (default) Value 1 - 2
8:7	DLL_CUR_CTRL	Delay line current control - change current mirror ratio in each delay tap Delay value Value 00 - 1x (default) Value 01 - 2x Value 10 - 3x Value 11 - 4x
6	INT_REF_CLK	Value 0 (default) - use internal generated clock for delay line reference Value 1 - use sdc4_mclk for delay line reference
5	FEEDBACK_CLK_EN	Value 0 (default) - enable delay line feedback Value 1 - disable delay line feedback
4:0	RESERVED	These reserved bits can be accessed by the SW and connected to cm_dll_sdc4's input

0x121C0068 SDC4_MCI_DLL_STATUS

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC4_MCI_DLL_STATUS

Bits	Name	Description
31:8	RESERVED_1	Always reads zero. Writes 'don't care' but by convention write zero.
7	DLL_LOCK	DLL lock status Value 0 - Not locked Value 1 - Locked

SDC4_MCI_DLL_STATUS (cont.)

Bits	Name	Description
6:3	CDR_PHASE	CDR phase select (gray coded) Value 0000 - phase 0 Value 0001 - phase 1 Value 0011 - phase 2 Value 0010 - phase 3 Value 0110 - phase 4 Value 0111 - phase 5 Value 0101 - phase 6 Value 0100 - phase 7 Value 1000 - phase 8 Value 1001 - phase 9 Value 1011 - phase 10 Value 1010 - phase 11 Value 1110 - phase 12 Value 1111 - phase 13 Value 1101 - phase 14 Value 1100 - phase 15
2	DDLL_COARSE_CAL	Value 1 - done Value 0 - not done
1:0	RESERVED_2	Connected to cm_dll_sdc4's output.

0x121C006C SDC4_MCI_STATUS2

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC4_MCI_STATUS2

Bits	Name	Description
31:1	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
0	MCLK_REG_WR_ACTIVE	Value 0 - No active register write to MCLK domain Value 1 - Active register write to MCLK domain. The bit indicates if a write operation to one of the following registers is in process (synchronization between HCLK and MCLK): MCI_POWER MCI_CLOCK MCI_CMD MCI_DATA_CTL

0x121C0070 SDC4_MCI_GENERICS

Type: Read
Clock: SAME_RATE_AS_HCLK

SDC4_MCI_GENERICS

Bits	Name	Description
31:27	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
26:23	SD_DATA_WIDTH	Number of DAT lines Value 4 - 4 DAT lines (SD, SDIO) Value 8 - 8 DAT lines (MMC, eMMC)
22:10	RAM_SIZE	Size of RAM size: Optional Values: 512, 1024, 2048 or 4096 bytes.
9	USE_SPS	Value 1 - BAM and DML are used and USB core is connected to SDCC4, Value 0 - BAM and DML are not used.
8:6	NUM_OF_DEV	Number of eSD or eSDIO devices supported on shared SD bus. Can be set from 1 to 4.
5:1	MAX_PIPES	Number of simultaneous parallel pipes supported by the BAM and attached peripherla pair. Can be set from 1 to 31.
0	USE_DLL_SDC4	Enables the instantiation of cm_dll_sdc4. Value 0 - cm_dll_sdc4 isn't integrated with SDCC4 Value 1 - cm_dll_sdc4 is used with SDCC4.

0x121C0080 SDC4_MCI_FIFO

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC4_MCI_FIFO

Bits	Name	Description
31:0	DATA	FIFO data. This register is aliased to 16 words, 0x080 - 0xBC. In SDCC3, an access to the FIFO was executed with 16 words so 16 addresses were defined. However, in SDCC4 only 8 words are used in each burst so only 8 addresses from the range should be used. When writing to the external SD_Card, writes to the data path FIFO. When reading from the external SD_Card, reads from the data path FIFO.

0x121C00CC SDC4_MCI_TESTBUS_CONFIG

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

NOTE mclk_mux is the selected internal mclk: the original mclk or divided mclk during divided frequency mode.

Table 20-7 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus0(0)	sdcc_crif_wr_en	hclk
test_bus0(1)	sdcc_crif_rd_en	hclk
test_bus0(2)	sdcc_crif_core_select	hclk
test_bus0(6 downto 3)	sdcc_crif_wr_data[3:0]	hclk
test_bus0(10 downto 7)	sdcc_crif_rd_data[3:0]	hclk
test_bus0(14 downto 11)	sdcc_crif_addr[5:2]	hclk
test_bus0(15)	sdcc_crif_ready	hclk
test_bus0(16)	adm_crci4_ack	-
test_bus0(17)	adm_crci4_req	hclk
test_bus0(18)	rx_fifo_rd_en	hclk
test_bus0(19)	tx_fifo_wr_en	hclk
test_bus0(20)	dm_cnt_rst	hclk
test_bus0(28 downto 21)	ram_addr	mclk_mux
test_bus0(29)	ram_we_n	mclk_mux
test_bus0(30)	ram_cs_n	mclk_mux
test_bus0(31)	rx_fifo_wr_en	mclk_mux
test_bus1(0)	sdcc_crif_wr_en	hclk
test_bus1(1)	sdcc_crif_rd_en	hclk
test_bus1(2)	sdcc_crif_core_select	hclk
test_bus1(6 downto 3)	sdcc_crif_addr[5:2]	hclk
test_bus1(7)	sdcc_crif_ready	hclk
test_bus1(8)	adm_crci4_ack	-
test_bus1(9)	adm_crci4_req	hclk
test_bus1(10)	rx_fifo_rd_en	hclk
test_bus1(11)	tx_fifo_wr_en	hclk
test_bus1(15 downto 12)	req_rw	hclk
test_bus1(16)	DATEnUpdPulse	hclk
test_bus1(17)	LastRxRdDone	hclk
test_bus1(25 downto 18)	ram_addr	mclk_mux

Table 20-7 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus1(26)	ram_we_n	mclk_mux
test_bus1(27)	ram_cs_n	mclk_mux
test_bus1(28)	rx_fifo_wr_en	mclk_mux
test_bus1(29)	ram_reset	mclk_mux
test_bus1(31 downto 30)	pipeline_fill	mclk_mux
test_bus2(2 downto 0)	CPSMState	mclk_mux
test_bus2(3)	CPSMEn	mclk_mux
test_bus2(4)	nIntCMDEN	mclk_mux
test_bus2(5)	iCMDCnt47	mclk_mux
test_bus2(6)	iCRspE	mclk_mux
test_bus2(7)	start_bit_first(CPSM)	mclk_mux
test_bus2(8)	DivLevelCo	mclk_mux
test_bus2(11 downto 9)	DPSMState	mclk_mux
test_bus2(12)	DPSMEn	mclk_mux
test_bus2(13)	inDAT0EN_sel	mclk_mux
test_bus2(14)	inDATEN_sel	mclk_mux
test_bus2(15)	StartBit	mclk_mux
test_bus2(16)	iDEndSet	mclk_mux
test_bus2(17)	iStopBit	mclk_mux
test_bus2(18)	TxFlowCtrlChk	mclk_mux
test_bus2(19)	iTxFlowControl	mclk_mux
test_bus2(27 downto 20)	ram_addr	mclk_mux
test_bus2(28)	ram_we_n	mclk_mux
test_bus2(29)	ram_cs_n	mclk_mux
test_bus2(30)	LastRxRdDoneL	mclk_mux
test_bus2(31)	start_bit_first(DPSM)	mclk_mux
test_bus3(7 downto 0)	DATIN[7:0]	mclk_mux
test_bus3(8)	Valid	mclk_mux
test_bus3(10 downto 9)	VSMState	mclk_mux
test_bus3(11)	CmdStopBit	mclk_mux
test_bus3(13 downto 12)	StopBitDelCnt	mclk_mux
test_bus3(15 downto 14)	CRspESetDelCnt	mclk_mux
test_bus3(16)	mclkenable	mclk_mux
test_bus3(18 downto 17)	isdcc_irq	-
test_bus3(21 downto 19)	DPSMState	mclk_mux
test_bus3(22)	DPSMEn	mclk_mux
test_bus3(23)	inDAT0EN_sel	mclk_mux
test_bus3(24)	inDATEN_sel	mclk_mux

Table 20-7 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus3(25)	StartBit	mclk_mux
test_bus3(26)	iDEndSet	mclk_mux
test_bus3(27)	iStopBit	mclk_mux
test_bus3(28)	TxFlowCtrlChk	mclk_mux
test_bus3(29)	iTxFlowControl	mclk_mux
test_bus3(31)	LastDataWord	mclk_mux
test_bus4(2 downto 0)	CPSMState	mclk_mux
test_bus4(3)	CPSMEn	mclk_mux
test_bus4(4)	nIntCMDEN	mclk_mux
test_bus4(5)	iCRspE	mclk_mux
test_bus4(13 downto 6)	CMDCNT	mclk_mux
test_bus4(14)	start_bit_first(CPSM)	mclk_mux
test_bus4(15)	DivLevelCo	mclk_mux
test_bus4(16)	async_fifo_out_valid	mclk_mux
test_bus4(18 downto 17)	CMDIN	mclk_mux
test_bus4(21 downto 19)	DPSMState	mclk_mux
test_bus4(22)	DPSMEn	mclk_mux
test_bus4(29 downto 23)	BLKTCnt(6 downto 0)	mclk_mux
test_bus4(30)	iCheckProgDone	mclk_mux
test_bus4(31)	iProgDone	mclk_mux
test_bus5(2 downto 0)	DPSMState	mclk_mux
test_bus5(3)	DPSMEn	mclk_mux
test_bus5(4)	inDAT0EN_sel	mclk_mux
test_bus5(5)	inDATEN_sel	mclk_mux
test_bus5(6)	StartBit	mclk_mux
test_bus5(7)	iDEndSet	mclk_mux
test_bus5(8)	iStopBit	mclk_mux
test_bus5(9)	TxFlowCtrlChk	mclk_mux
test_bus5(10)	iTxFlowControl	mclk_mux
test_bus5(11)	LdDataBuffer	mclk_mux
test_bus5(12)	iRxFlowControl	mclk_mux
test_bus5(13)	LastRxRdDone	mclk_mux
test_bus5(14)	inDATEN_high_sel	mclk_mux
test_bus5(15)	inDATEN_low_sel	mclk_mux
test_bus5(16)	async_fifo_out_valid	mclk_mux
test_bus5(17)	LastDataWord	mclk_mux
test_bus5(18)	pipeline_empty	mclk_mux
test_bus5(19)	ShiftNotE	mclk_mux

Table 20-7 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus5(20)	start_bit_first (DPSM)	mclk_mux
test_bus5(21)	DIVLevelCo	mclk_mux
test_bus5(28 downto 22)	BLKTCnt(6:0)	mclk_mux
test_bus5(29)	iCheckProgDone	mclk_mux
test_bus5(30)	iProgDone	mclk_mux
test_bus5(31)	start_bit_last	mclk_mux
test_bus6(7 downto 0)	ram_addr	mclk_mux
test_bus6(8)	ram_we_n	mclk_mux
test_bus6(9)	ram_cs_n	mclk_mux
test_bus6(11 downto 10)	pipeline_fill	mclk_mux
test_bus6(12)	ram_reset	mclk_mux
test_bus6(13)	rx_fifo_wr_en	mclk_mux
test_bus6(14)	rx_fifo_rd_en	hclk
test_bus6(15)	tx_fifo_wr_en	hclk
test_bus6(19 downto 16)	req_rw	hclk
test_bus6(20)	DATEnUpdPulse	hclk
test_bus6(21)	dm_cnt_rst	hclk
test_bus6(25 downto 22)	rx_fifo_rd_word_cnt	hclk
test_bus6(29 downto 26)	tx_fifo_wr_word_cnt	hclk
test_bus6(30)	iLastRxRdDone	hclk
test_bus6(31)	RxActive	hclk
test_bus7(1 downto 0)	CMDIN	mclk_mux
test_bus7(17 downto 2)	DATIN	mclk_mux
test_bus7(18)	div_freq_cnt_cmd_tx	mclk
test_bus7(19)	div_freq_cnt_dat_tx	mclk
test_bus7(20)	div_freq_cnt_rx	mclk
test_bus7(21)	async_fifo_out_valid	mclk
test_bus7(22)	Rising_DAT0EN_5d	mclk
test_bus7(31 downto 23)	async_fifo_rd_data	mclk

SDC4_MCI_TESTBUS_CONFIG

Bits	Name	Description
31:8	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
7:4	SPARE_FIELD	SW spare bits.
3	TESTBUS_ENA	0x1: Enable 0x0: Disable

SDC4_MCI_TESTBUS_CONFIG (cont.)

Bits	Name	Description
2:0	TESTBUS_SEL	These bits select from different test signals. Refer to Table 1-3 for a list of test signals. TESTBUS_SELBus testbus_sel = 0sdcc_test_bus <= test_bus0 testbus_sel = 1 sdcc_test_bus <= test_bus1 testbus_sel = 2sdcc_test_bus <= test_bus2 testbus_sel = 3sdcc_test_bus <= test_bus3 testbus_sel = 4sdcc_test_bus <= test_bus4 testbus_sel = 5sdcc_test_bus <= test_bus5 testbus_sel = 6sdcc_test_bus <= test_bus6 testbus_sel = 7sdcc_test_bus <= test_bus7

0x121C00D0 SDC4_MCI_TEST_CTL

Type: Read/Write
Clock: PCLK
Reset State: 0x00000000

(ARM name: MCITCR)

SDC4_MCI_TEST_CTL

Bits	Name	Description
31:4	RESERVED_1	Always reads zero. Writes ’don’t care’ but by convention write zero.
3	REGTEST	Register Test Bit: Set 0: normal mode (default--accesses to the registers are controlled by the hardware protection circuitry) Set 1: test mode (the hardware protection circuitry is bypassed. Normal Write/Read/Write/ Read tests can be performed independently of the link side.
2:1	RESERVED_2	Always reads zero. Writes ’don’t care’ but by convention write zero.
0	ITEN	Integration Test Enable. This bit places PrimeCell MCI in the following modes: Set 0: normal mode Set 1: Integration test mode

0x121C00D4 SDC4_MCI_TEST_INPUT

Type: Read
Clock: PCLK

(ARM name: MCIITIP)

SDC4_MCI_TEST_INPUT

Bits	Name	Description
31:10	RESERVED_1	Always reads zero. Writes ’don’t care’ but by convention write zero.
9:6	MCIDATIN_7_4	Reads return the value on the MCIDATIN[7:4] primary inputs.
5	MCICMDIN	Reads return the value on the MCICMDIN primary input.
4:1	MCIDATIN_3_0	Reads return the value on the MCIDATIN[3:0] primary inputs.
0	RESERVED_2	Always reads zero. Writes ’don’t care’ but by convention write zero.

0x121C00D8 SDC4_MCI_TEST_OUT

Type: Read/Write
Clock: PCLK

(ARM name: MCIITOP)

SDC4_MCI_TEST_OUT

Bits	Name	Description
31:16	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
15:12	MCIDATOUT_7_4	Primary output. Writes specify the value to be driven on the MCIDATOUT[7:4] primary output in the integration test mode. Reads return the value written into this field.
10	MCICMDOUT	Primary output. Writes specify the value to be driven on the MCICMDOUT primary output in the integration test mode. Reads return the value written into this field.
9:6	MCIDATOUT_3_0	Primary output. Writes specify the value to be driven on the MCIDATOUT[3:0] primary output in the integration test mode. Reads return the value written into this field.
1	MCIINTR1	Intra-chip output. Writes specify the value to be driven on the intra-chip MCIINTR1 output in the integration test mode. This bit is write-only.
0	MCIINTR0	Intra-chip output. Writes specify the value to be driven on the intra-chip MCIINTR0 output in the integration test mode. This bit is write-only.

20.20 SDC4 DML Registers (0x121C0800 SDC4_DML_BASE)

This section contains the SDC4 DML registers.

The address field is a relative address. A base will be supplied by the SOC team and documented at the start of the chip SW Manual.

0x121C0800 SDC4_DML_CONFIG

Type: Read/Write
Clock: HCLK
Reset State: 0x00010000

SW has the responsibility to set the CRCI SEL fields correctly when both Consumer and Producer sides are enabled at the same time. For example, setting both to 01 or setting both to 10 is an invalid setting if both producer and consumer sides are kicked off. The DML does NOT assume responsibility for incorrect setting of CRCI SEL fields and hence its function is not defined in such cases.

SDC4_DML_CONFIG

Bits	Name	Description
31:19	RESERVED31	reserved
18	INFINITE_CONS_TRANS	If set, this bit means the consumer transaction is of infinite size. Hence the transaction_end_rec signal from BAM will be ignored.
17	DIRECT_MODE	If set, DML is assumed to directly MASTER the AHB bus, in essence, no BAM or BAM is bypassed. This bit value is also routed to the direct_mode hardware port on the DML to be connected to BAM. See Direct_mode_BASE_addr register.
16	BYPASS	If set, the CRCI pairs will be passed through for legacy central DM support. The config AHB slave interface will be directly accessing the peripheral core for config, command and data movement functions. NOTE: The reset value of this bit is `1' which means the DML come out of PoReset in BYPASS state.
15:6	RESERVED15	reserved
5	PRODUCER_BLOCK_END_HPROT2	If set, DML drives high hprot[2] to BAM when block_end is high, else DML drives low hprot[2] to BAM when block_end is high
4	PRODUCER_TRANS_END_EN	When set, transaction_end signal is asserted at the end of DML transaction. When cleared, transaction_end signal is NOT asserted at the end of DML transaction. This feature allows to divide one BAM transaction to two Peripheral transactions.
3:2	CONSUMER_CRCI_SEL	When set to 00, Consumer side is Disabled When set to 01, CRCI-x pair is the consumer CRCI When set to 10, CRCI-y pair is the consumerCRCI If set to 11, its a invalid setting.

SDC4_DML_CONFIG (cont.)

Bits	Name	Description
1:0	PRODUCER_CRCI_SEL	When set to 00, Producer side is Disabled When set to 01, CRCI-x pair is the producer CRCI When set to 10, CRCI-y pair is the producer CRCI If set to 11, its a invalid setting.

0x121C0804 SDC4_DML_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00010001

SDC4_DML_STATUS

Bits	Name	Description
31:17	RESERVED31	reserved
16	CONSUMER_IDLE	0x0: Consumer is busy 0x1: Consumer is IDLE
15:1	RESERVED15	reserved
0	PRODUCER_IDLE	0x0: Producer is busy 0x1: Producer is IDLE

0x121C0808 SDC4_DML_SW_RESET

Type: Write
Clock: HCLK
Reset State: 0x00000000

A write to this register resets the DML core. All internal state information will be lost and all register values will be reset as well.

SDC4_DML_SW_RESET

Bits	Name	Description
31:0	RESERVED	reserved

0x121C080C SDC4_DML_PRODUCER_START

Type: Write
Clock: HCLK
Reset State: 0x00000000

A write to this register triggers the DML's Producer state machine. No SW register values will be altered. Only the internal counters and settings related to Producer activity will be reset and started afresh. This register should be written to after POR to kick off producer side. This register should also be used to restart the producer once it has reached IDLE state (as indicated by the STATUS register) after completing the current transaction.

SDC4_DML_PRODUCER_START

Bits	Name	Description
31:0	RESERVED	reserved

0x121C0810 SDC4_DML_CONSUMER_START

Type: Write
Clock: HCLK
Reset State: 0x00000000

A write to this register triggers the DML's consumer state machine. No SW register values will be altered. Only the internal counters and settings related to consumer activity will be reset and started afresh. This register should be written to after POR to kick off consumer side. This register should also be used to restart the consumer once it has reached IDLE state (as indicated by the STATUS register) after completing the current transaction..

SDC4_DML_CONSUMER_START

Bits	Name	Description
31:0	RESERVED	reserved

0x121C0814 SDC4_DML_PRODUCER_PIPE_LOGICAL_SIZE

Type: Write/Read
Clock: HCLK
Reset State: 0x00000000

This register holds the size of the producer pipe (in units of bytes) _to_ which the peripheral can keep writing data to when its the PRODUCER. The value of this register should be consistent with what the BAM registers are programmed with as well. The DML in response to producer side CRCI requests starts writing out data (generated by the Peripheral) from address 0x0 (on its AHB Master Interface). For subsequent Producer side data accesses, the DML keeps on incrementing the address. Upon reaching the max value as indicated by this register, the address rolls over back to 0x0. The address also rolls over back to 0x0 after reaching the end of a transaction.

This register value decides the range of addresses seen on the DML AHB Master address bus during Producer activity.

The value of this register is restricted to any power of two and greater than or equal to the Producer BAM Block Size setting. This is to avoid DML overwriting its own data in the pipe as the data is not committed until block_end is received by the BAM.

The recommended value for this register is 4096(decimal)

SDC4_DML_PRODUCER_PIPE_LOGICAL_SIZE

Bits	Name	Description
31:16	RESERVED31	reserved31
15:0	PRODUCER_LOGICAL_SIZE	The size of the producer pipe (in units of bytes) to which a producer peripheral can keep writing the data it produces.

0x121C0818 SDC4_DML_CONSUMER_PIPE_LOGICAL_SIZE

Type: Write/Read
Clock: HCLK
Reset State: 0x00000000

This register holds the size of the consumer pipe (in units of bytes) _from_ which the peripheral can keep _reading_ data from when its the CONSUMER. The value of this register should be consistent with what the BAM registers are programmed with as well. The DML in response to consumer side CRCI requests starts reading out data (needed by the Peripheral) from address 0x0 (on its AHB Master Interface). For subsequent consumer side data accesses, the DML keeps on incrementing the address. Upon reaching the max value as indicated by this register, the address rolls over back to 0x0. The address also rolls over back to 0x0 after reaching the end of a transaction.

This register value decides the range of addresses seen on the DML AHB Master address bus during consumer activity.

The value of this register is restricted to any power of two and no smaller than 32 bytes, that is, no smaller than a "beat-8" burst on a 32 bit AHB.

The recommended value for this register is 4096(decimal)

SDC4_DML_CONSUMER_PIPE_LOGICAL_SIZE

Bits	Name	Description
31:16	RESERVED31	reserved31
15:0	CONSUMER_LOGICAL_SIZE	The size of the consumer pipe (in units of bytes) to which a consumer peripheral can keep reading the data from it needs.

0x121C081C SDC4_DML_PIPE_ID

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register holds pipe IDs that services the producer and consumer side of the peripheral.

- The producer pipe ID is fed to the BAM when servicing the producer side of the peripheral.
- The consumer pipe ID is fed to the BAM when servicing the consumer side of the peripheral.
- The DML also uses this ID value to look into the appropriate side band signals from BAM like pipe_empty, pipe_full etc before initiating the said AHB transaction.

SDC4_DML_PIPE_ID

Bits	Name	Description
31:21	RESERVED31	reserved
20:16	CONSUMER_PIPE_ID	consumer pipe ID
15:5	RESERVED15	reserved
4:0	PRODUCER_PIPE_ID	producer pipe ID

0x121C0820 SDC4_DML_PRODUCER_TRACKERS

Type: Read
Clock: HCLK
Reset State: 0x00000000

.This register is for debug purposes only. They reflect the value of the producer block and transaction counters when read. The values may be dynamically changing when a transaction is in progress.

SDC4_DML_PRODUCER_TRACKERS

Bits	Name	Description
31:16	PROD_TRANS_CNT	Value of the 16bit tracker tracking the Producer Transaction Count for the current transaction. Should read 0 at the end of the transaction.
15:0	PROD_BLOCK_CNT	Value of the 16 bit tracker that tracks the Producer Block Count. Need not be zero at the end of transaction.

0x121C0824 SDC4_DML_PRODUCER_BAM_BLOCK_SIZE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register holds the "block" size, in units of bytes, associated with the Producer BAM. The DML asserts the block_end side band signal to the BAM whenever the producer side of the peripheral has generated the said amount of data. This register value should be an integral multiple of the Producer CRCI Block Size.

Legal values for Producer BAM Block Size are 64, 128, 192, 256, 512, 1024, 2048 and 4096.

The recommended value for this register is 512(decimal)

SDC4_DML_PRODUCER_BAM_BLOCK_SIZE

Bits	Name	Description
31:16	RESERVED	reserved
15:0	PRODUCER_BLK_SIZE	Size of the one "block" on the producer side in units of bytes.

0x121C0828 SDC4_DML_PRODUCER_BAM_TRANS_SIZE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register holds the "transaction" size, in units of bytes, associated with the Producer BAM. The DML asserts the transaction_end side band signal to the BAM whenever the producer side of the peripheral has generated the said amount of data. This signal is asserted only during the address phase of the AHB transaction that carries the last byte corresponding to the size mentioned in this register. Once this value is reached for a given transaction, the address for subsequent data access rolls back to 0x0 and all the block size, CRCI size and transaction size counters also get reset to 0 and start all over again. A value of zero in this register during a producer transaction start means infinite size transaction and hence transaction_end may not get asserted.

This value can be anything up to a maximum of 4294967295 bytes (4 GB -1). If this register value is zero when the DML is started, then an infinite transaction size is assumed. No transaction_end will be generated.

SDC4_DML_PRODUCER_BAM_TRANS_SIZE

Bits	Name	Description
31:0	PRODUCER_TRANS_SIZE	Size of the one "transaction" on the producer side in units of bytes or if zero, then infinite transaction size assumed.

0x121C082C SDC4_DML_DIRECT_MODE_BASE_ADDR

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register is used whenever the DIRECT_MODE bit in config register is set. The programmed 16bits will be used as DML AHB Master address bus MSBits for consumer (AHB read) and producer (AHB Write) operations. The lower 16bits would be dictated by the pipe logical size register.

SDC4_DML_DIRECT_MODE_BASE_ADDR

Bits	Name	Description
31:16	CONSUMER_BASE_ADDR	used as AHB Master address (31:16) when doing direct mode consumer operations if direct_mode bit is set.
15:0	PRODUCER_BASE_ADDR	used as AHB Master address (31:16) when doing direct mode producer operations if direct_mode bit is set.

0x121C0830 SDC4_DML_DEBUG

Type: Write/Read
Clock: HCLK
Reset State: 0x00000000

Enables Test Bus of the DML and also selects which side signals to drive the test bus with.

SDC4_DML_DEBUG

Bits	Name	Description
31:2	RESERVED	reserved
1	STATUS_2_SEL	If set, selects the set of signals listed out in DML_BAM_SIDE_STATUS_2 register onto Test bus, else selects set of signals listed out in DML_BAM_SIDE_STATUS_1 register to be muxed onto test bus. Valid only if bit 0 is set.
0	TESTBUS_EN	0x0: Disable Test Bus 0x1: Enable Test Bus

0x121C0834 SDC4_DML_BAM_SIDE_STATUS_1

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the instantaneous value of the side band signals with BAM.

SDC4_DML_BAM_SIDE_STATUS_1

Bits	Name	Description
31:24	RESERVED31	reserved
23	ACK_ON_SUCCESS_TOGGLE	for selected consumer pipe
22	ACK_BYTES_AVAIL_TOGGLE	for selected consumer pipe
21	PIPE_BYTES_AVAIL_TOGGLE	for selected consumer pipe
20	TRANSACTION_END_REC	transaction end received for selected consumer pipe.
19	PIPE_BYTES_FREE_TOGGLE	bytes free toggle signal for selected producer pipe
18:3	PIPE_BYTES_FREE	bytes free value for selected producer pipe
2	MESSAGING_ONLY	DML output status
1	TRANSACTION_END	DML output status
0	BLOCK_END	DML output status

0x121C0838 SDC4_DML_BAM_SIDE_STATUS_2

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the instantaneous value of the side band signals with BAM.

SDC4_DML_BAM_SIDE_STATUS_2

Bits	Name	Description
31:16	ACK_ON_SUCCESS_TOGGLE_SIZE	for selected consumer pipe
15:0	PIPE_BYTES_AVAIL	for selected consumer pipe

0x121C083C SDC4_DML_RTL_GENERICS_1

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the value of the RTL Generics set during the integration of the DML into a SPS Wrapper or other entity.

SDC4_DML_RTL_GENERICS_1

Bits	Name	Description
31:17	RESERVED31	reserved
16:11	PERIPHERAL_ADDR_WIDTH	represents the width set (in binary format)
10:6	MAX_PIPES	represents the number of pipe value set (in binary format)
5:3	CONSUMER_CRCI_BLK	101:.256 bytes 0x0: 16 bytes 0x1: 32 bytes 0x2: 64 bytes 0x3: 128 bytes 0x4: 192 bytes
2:0	PRODUCER_CRCI_BLK	101:.256 bytes 0x0: 16 bytes 0x1: 32 bytes 0x2: 64 bytes 0x3: 128 bytes 0x4: 192 bytes

0x121C0840 SDC4_DML_RTL_GENERICS_2

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the value of the PROD_DMR_RD_ADDR Generic set in RTL during the integration of the DML into a SPS Wrapper or other entity.

SDC4_DML_RTL_GENERICS_2

Bits	Name	Description
31:0	PROD_RD_DMR_ADDR	32bit Value of the PROD_DMR_RD_ADDR generic

0x121C0844 SDC4_DML_RTL_GENERICS_3

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the value of the CONS_DMR_WR_ADDR Generic set in RTL during the integration of the DML into a SPS Wrapper or other entity.

SDC4_DML_RTL_GENERICS_3

Bits	Name	Description
31:0	CONS_WR_DMR_ADDR	32bit Value of the CONS_DMR_WR_ADDR generic

0x121C0848 SDC4_DML_INTERRUPT_ENABLE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

SDC4_DML_INTERRUPT_ENABLE

Bits	Name	Description
31:1	RESERVED31	reserved
0	PROD_IDLE_START_INTR_EN	Enable DML to generate an interrupt when PRODUCER enters an IDLE state.

0x121C084C SDC4_DML_INTERRUPT_CLEAR

Type: Write
Clock: HCLK
Reset State: 0xXXXXXXXX

SDC4_DML_INTERRUPT_CLEAR

Bits	Name	Description
31:1	RESERVED31	reserved
0	PROD_IDLE_START_INTR_CLR	Clear PROD_IDLE_START_INTR interrupt.

20.21 SDC4 BAM Registers (0x121C2000 SDC4_BAM_BASE)

This section contains the SDC4 BAM registers.

BAM supports only Word (4 byte) aligned writes and reads on the Configuration Bus interface.

BAM has MAX_PIPES hardware generic parameter defining the number of pipes it supports. Each BAM can have up to 31 pipes supported.

BAM has BAM_CONF_AHBS_ADDR_WIDTH hardware generic parameter defining the Bit Number for selecting BAM access or Peripheral access. Legal Ranges are 14 to 20. Count starts from 1, meaning a value of 17 will set BAM Base address as 0x0001_0000.

20.21.1 BAM control registers

BAM Control registers configure the BAM operational state, SW reset, interrupts and others.

0x121C2F80 SDC4_BAM_CTRL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

BAM Control register allows global controls for the BAM.

SDC4_BAM_CTRL

Bits	Name	Description
31:17	RESERVED_BITS31_17	Set to Zero (0)
16	IBC_DISABLE	This Bit enables power saving by disabling the inactivity clock timer/counter. This is useful when: 1) The BAM is Enabled but idling for long periods. 2) The BAM is Enabled and running but the inactivity timers/counters are not required by the SW for operating the BAM. When the BAM is Disabled, it automatically shuts down those timers to save power. 1’b1 - Enable Power Saving Mode 1’b0 - Disable Power Saving Mode

SDC4_BAM_CTRL (cont.)

Bits	Name	Description
15	BAM_CACHED_DESC_STORE	This Bit enables storage of a cached Descriptor into RAM when doing Context Switch and loading it back when returning to this pipe. This is relevant for System Modes Only. BAM to BAM Consumer mode doesn't have this option. Enabling this makes the Context Switch process slightly longer but reduces AHB Descriptor Fetch time later on. It also reduces the number of descriptor fetches done by the BAM if BAM is treating more than 2 pipes. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
14:13	BAM_DESC_CACHE_SEL	This Selector chooses which Descriptor Caching mode will be used. This is relevant for System Producer or Consumer modes only. 2’b00 - Cache when current descriptor has less than 64 bytes left. 2’b01 - Cache when current descriptor has less than 128 bytes left. 2’b10 - Immediate Auto cache - cache will happen whenever there are no descriptors cached. This might cause unnecessary descriptors reads when switching between more than 2 pipes. It is the most effective when each pipe processes more bytes than there are in an average descriptor (small descriptors, big block size), or when working with 2 or less pipes. 2’b11 - Cache when descriptor is needed only. This results in 1 descriptor present in cache at most. Available in BAM only
12	RESERVED_BITS12	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_SIC_SEL
11:5	BAM_TESTBUS_SEL	Set to Zero (0) Obsolete field: BAM_TESTBUS_SEL Test Bus selector. Supported until (including) bam_p3q3r29 (BlackBird). Moved to a dedicated register - BAM_TEST_BUS_SEL in the following releases.
4	BAM_EN_ACCUM	When Enabled, BAM will accumulate data written by the peripheral in Direct Mode into INCR8 Bursts. This is an optimization feature for Producer Direct Mode cases. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
3	RESERVED_BITS3	Set to Zero (0)
2	RESERVED_BITS2	Set to Zero (0)

SDC4_BAM_CTRL (cont.)

Bits	Name	Description
1	BAM_EN	After reset the BAM wakes up in Disabled Mode. While Disabled, BAM operates in Legacy mode (all the transfers from the peripheral go around the BAM as if it doesn't exist) Software Enables this bit to allow BAM operation. This bit doesn't affect the PIPE enable bit in BAM_P_CTRL register. The only possibility to Disable the BAM after it has been enabled is by Hardware or Software reset. 1'b1 - Enabled 1'b0 - Disabled
0	BAM_SW_RST	This will reset the BAM & all Pipes. Software may use this to reset the BAM. As long as the bit remains high the BAM remains in reset state. Software should clear this bit 1'b1 - Reset state 1'b0 - Normal state

0x121C2F84 SDC4_BAM_REVISION

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a hard coded revision number of the BAM RTL. This corresponds to the BAM target number in the IMS. Also additional BAM settings are reflected here.

SDC4_BAM_REVISION

Bits	Name	Description
31:24	INACTIV_TMR_BASE	This indicates the width of the inactivity timers base counter
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	NUM_INACTIV_TMRS	This bit is checked only if INACTIV_TMRS_EXST = 1. This bit indicates how many inactivity timers are implemented according to value of INACTIVITY_TIMERS_SUPPORTED generic: 1'b1 - One timer for global BAM activity (INACTIVITY_TIMERS_SUPPORTED = 1) 1'b0 - MAX_PIPES timers for each pipe activity (INACTIVITY_TIMERS_SUPPORTED = 2)
19	INACTIV_TMRS_EXST	This indicates BAM has inactivity timers. 1'b1 - Timers available (INACTIVITY_TIMERS_SUPPORTED = 1 or 2) 1'b0 - No timers available (INACTIVITY_TIMERS_SUPPORTED = 0)

SDC4_BAM_REVISION (cont.)

Bits	Name	Description
18	HIGH_FREQUENCY_BAM	This indicates BAM has Double Sampling on the Ack On Success interface. 1'b1 - Ack On Success double sampled 1'b0 - No double sampling of Ack On Success
17	BAM_HAS_NO_BYPASS	This field indicates BAM has no bypass on the AHB Data bus, from the Peripheral AHB Master to the fabric. When Bypass is available, it is the default routing when BAM is disabled. 1'b1 - No Bypass 1'b0 - Bypass Exists
16	SECURED	This field indicates BAM/BAM-Lite has security support (APU inside) 1'b1 - Secured 1'b0 - Not Secured
15:12	RESERVED_BITS15_12	Set to Zero (0)
11:8	NUM_EES	This indicates the Number of Interrupt Lines (Execution Environments) supported by the BAM. When 1 EE is supported, only the BAM_IRQ_SRCS*_EE0 registers exist. When 4 EEs are supported, all BAM_IRQ_SRCS*_EEn registers exist for n=[0..3].
7:0	REVISION	This field contains the revision number of the core, Hard Coded. 8'h01 - Voyager (bam_p3q3r22 +) 8'h02 - BlackBird (bam_p3q3r27 +) 8'h03 - Waverider BAM (bam_p3q3r30 +) 8'h04 - Aurora BAM (bam_p3q2r43 +) 8'h05 - Shelby BAM (bam_p2q2r45 +) 8'h10 - Waverider BAM Lite (bam_lite_p1q1r0 +) 8'h11 - Aurora BAM Lite (bam_lite_p3q2r16 +) 8'h12 - Shelby BAM Lite (bam_lite_p2q2r18 +)

0x121C2FBC SDC4_BAM_NUM_PIPES

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a the hard coded number of pipes in the BAM. Since each BAM may have a different number of pipes instantiated in HW, this register allows the SW to know this parameter. The reset state value doesn't have any meaning in this register since it is a constant.

SDC4_BAM_NUM_PIPES

Bits	Name	Description
31:24	BAM_NON_PIPE_GRP	This field contains the number of BAM Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
23:16	PERIPH_NON_PIPE_GRP	This field contains the number of Peripheral's Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
15:8	RESERVED_BITS15_8	Set to Zero (0)
7:0	BAM_NUM_PIPES	This field contains the number of pipes available in this BAM

0x121C2FC0 SDC4_BAM_TIMER

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the BAM (all the pipes are in idle state).

SDC4_BAM_TIMER

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x121C2FC4 SDC4_BAM_TIMER_CTRL

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The register can be written and read only when INACTIVITY_TIMERS_SUPPORTED generic equals to 1.

The resolution of the BAM inactivity timer are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define

the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * TIMER_TRSHLD.

SDC4_BAM_TIMER_CTRL

Bits	Name	Description
31	TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1 to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	TIMER_RUN	Will be used along with TIMER_MODE Not implemented at this time. Set to zero(0)
29	TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x121C2F88 SDC4_BAM_DESC_CNT_TRSHLD

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds a threshold value for the counter summing the Size of the Descriptors Provided. This value is Global for all pipes but it is relevant for System Producer BAM mode and Both Consumer modes, where Descriptors summing takes place in order to provide the information to the peripheral via pipe bytes free (producer) or pipe bytes available interfaces.

SDC4_BAM_DESC_CNT_TRSHLD

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0).
15:0	CNT_TRSHLD	Threshold value. The maximum allowed value is 32kByte. Available in BAM only

0x121C2F8C SDC4_BAM_IRQ_SRCS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking out this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register points to the physical BAM_IRQ_SRCS_EE0 register.

SDC4_BAM_IRQ_SRCS

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x121C2F90 SDC4_BAM_IRQ_SRCS_MSK

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register points to the physical BAM_IRQ_SRCS_MSK_EE0 register.

SDC4_BAM_IRQ_SRCS_MSK

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x121C2FB0 SDC4_BAM_IRQ_SRCS_UNMASKED

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register points to the physical BAM_IRQ_SRCS_UNMASKED_EE0 register.

SDC4_BAM_IRQ_SRCS_UNMASKED

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

0x121C2F94 SDC4_BAM_IRQ_STTS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only.

Clearing the interrupt bits is done by writing to BAM_IRQ_CLR register.

SDC4_BAM_IRQ_STTS

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
3	BAM_EMPTY_IRQ	This interrupt is for DEBUG purpose only. It should not be used in normal SW flows. The interrupt indicates the BAMs buffer is empty. This bit can become high only when BAM_DATA_ERASE or BAM_DATA_FLUSH is high in BAM_TEST_BUS_SEL register.
2	BAM_ERROR_IRQ	This Indicates a Fatal Error has happened in the BAM. Currently this might happen due to an UnSuccessful Pipe Reset operation.

SDC4_BAM_IRQ_STTS (cont.)

Bits	Name	Description
1	BAM_HRESP_ERR_IRQ	This interrupt Indicates that an Erroneous HResponse has been received by the AHB Master. Additional Information about the error may be read at BAM_AHB_MASTER_ERR_* Registers. Clearing this interrupt also clears the BAM_AHB_MASTER_ERR_* Registers. Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x121C2F98 SDC4_BAM_IRQ_CLR

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

SDC4_BAM_IRQ_CLR

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
3	BAM_EMPTY_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM-Lite only
2	BAM_ERROR_CLR	1'b1 - Clear 1'b0 - Unchanged
1	BAM_HRESP_ERR_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x121C2F9C SDC4_BAM_IRQ_EN

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the BAM Interrupt Status register.

SDC4_BAM_IRQ_EN

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_EN	Enables Inactivity timer interrupt by writing this bit 1'b1 - Enable 1'b0 - Disable
3	BAM_EMPTY_EN	1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
2	BAM_ERROR_EN	1'b1 - Enable 1'b0 - Disable
1	BAM_HRESP_ERR_EN	1'b1 - Enable 1'b0 - Disable Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x121C2FA0 SDC4_BAM_RESERVED_1

Type: Read
Clock: BAM_CLK
Reset State: 0x00000000

SDC4_BAM_RESERVED_1

Bits	Name	Description
31	RESERVED_BITS31	Set to Zero (0) Obsolete field: BAM_IRQ_SIC_SEL
30:0	RESERVED_BITS30_0	Set to Zero (0) Obsolete field: P_IRQ_SIC_SEL

0x121C2FA4 SDC4_BAM_AHB_MASTER_ERR_CTRLS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

SDC4_BAM_AHB_MASTER_ERR_CTRLS

Bits	Name	Description
31:23	RESERVED_BITS31_16	Set to Zero (0)
22:18	BAM_ERR_HVMID	HVMID
17	BAM_ERR_DIRECT_MODE	DIRECT MODE
16:12	BAM_ERR_HCID	HCID
11:8	BAM_ERR_HPROT	HPROT
7:5	BAM_ERR_HBURST	HBURST
4:3	BAM_ERR_HSIZE	HSIZE
2	BAM_ERR_HWRITE	HWRITE
1:0	BAM_ERR_HTRANS	HTRANS

0x121C2FA8 SDC4_BAM_AHB_MASTER_ERR_ADDR

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

SDC4_BAM_AHB_MASTER_ERR_ADDR

Bits	Name	Description
31:0	BAM_ERR_ADDR	HADDR

0x121C2FAC SDC4_BAM_AHB_MASTER_ERR_DATA

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

SDC4_BAM_AHB_MASTER_ERR_DATA

Bits	Name	Description
31:0	BAM_ERR_DATA	HDATA

0x121C2FB4 SDC4_BAM_RESERVED_2

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

SDC4_BAM_RESERVED_2

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_IRQ_DEST_ADDR

0x121C2FB8 SDC4_BAM_RESERVED_3

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

SDC4_BAM_RESERVED_3

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_DEST_ADDR

0x121C2FF0 SDC4_BAM_TRUST_REG

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside - SECURED field in the BAM_REVISION register) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

SDC4_BAM_TRUST_REG

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_VMID	Those bits indicate the VMID value to be used when performing BAM type accesses to the bus. BAM Type accesses include BAM MTI (or Direct Mode accesses, not applicable for BAM Lite)
7	BAM_RST_BLOCK	When enabled, the BAM Global SW reset will not be available for usage. This is in order to deny Global SW reset requests by the Global security group. 1'b1 - Enable 1'b0 - Disable
6:2	RESERVED_BITS6_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_EE	This Field Indicates the EE (0,1,2,3) to which the BAM Interrupt belongs to. The pipe interrupts will fire on the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x121C2FF4 SDC4_BAM_TEST_BUS_SEL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This is the testbus selector register.

Supported in releases after bam_p3q3r29 (BlackBird).

SDC4_BAM_TEST_BUS_SEL

Bits	Name	Description
31:19	RESERVED_BITS31_19	Set to Zero (0)
18	BAM_DATA_ERASE	When enabled, BAM will be instructed to erase all the data it currently has inside. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Erase 1'b0 - Disabled
17	BAM_DATA_FLUSH	When enabled, BAM will be instructed to flush all the data it currently has inside. BAM will only flush the data once it has enough data and a valid destination for it. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Flush 1'b0 - Disabled
16	BAM_CLK_ALWAYS_ON	This bit controls the BAM to issue 'always on' clock request. 1'b1 - Enable Always On clock request. 1'b0 - Disabled
15:7	RESERVED_BITS15_7	Set to Zero (0)
6:0	BAM_TESTBUS_SEL	Test Bus selector. Values with bit[11] set high are reserved for the BAM Lite integrator to provide testbus from outside of the BAM Lite. For example, eDML testbus may reside at X'100_0000' to X'111_1111' selector values. eDML has no registers thus has no test bus selector, so its test bus is combined with the BAM lite's. BAM provides zeroes on its testbus when external values selected. X'000_0000' - Zeros X'000_0001' - Slave test bus X'000_0010' - Pipe state machine test bus X'000_0011' - Buffer test bus X'000_0100' - Sideband test bus X'000_1101' - Bus Manager test bus X'001_0000' - Reg file test bus X'1''_''''' - BAM Lite sets zeroes on the test bus, leaving it for external use

0x121C2FF8 SDC4_BAM_TEST_BUS_REG

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the value being output to the testbus of the chip. It is not intended for SW usage but for lab debugging of the BAM. Values here can change every cycle.

SDC4_BAM_TEST_BUS_REG

Bits	Name	Description
31:0	BAM_TESTBUS_REG	32 bit Testbus value. To select the Block in BAM to show here, use the BAM_TESTBUS_SEL field in BAM_CTRL register.

0x121C2FFC SDC4_BAM_CNFG_BITS

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM configuration bits for bug fixes. It is highly recommended to follow the directions for each bit and set it accordingly.

SDC4_BAM_CNFG_BITS

Bits	Name	Description
31:27	RESERVED_BITS31_27	Set to Zero (0)
26	BAM_AU_ACCUMED	Recommended value: 1 This bit fixes a bug in the Ack Update state machine, where an overflow happened while counting descriptors and reaching more than 64kB of calculated sizes. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only
25	BAM_PSM_P_HD_DATA	Recommended value: 1 This bit allows pipe state machine to ignore retransmission requests if a pipe has just been initialized and process those as a regular fetch request. (consumer modes only). When this bit disabled, BAM could fetch descriptors for a pipe which was reset and no descriptors were added yet, if a retransmission request followed after the reset. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only

SDC4_BAM_CNFG_BITS (cont.)

Bits	Name	Description
24	BAM_REG_P_EN	Recommended value: 1 This bit fixes the pipe configuration signals mux for the current active pipe in 2 pipes BAM. When disabled, internal state machines might get into enabled states while the pipe is disabled. This would typically happen after pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
23	BAM_WB_DSC_AVL_P_RST	Recommended value: 1 This bit allows the Writeback state machine to reset the vector indicating there are available descriptors when a pipe reset occurs. If disabled, BAM might fetch descriptors after resetting and reconfiguring a pipe, even though no Event (descriptors) was provided.. 1’b1 - Enable 1’b0 - Disable Available in BAM only
22	BAM_WB_RETR_SVPNT	Recommended value: 1 This bit fixes a bug where a pipe which was reset, still stored its retransmission savepoint, but into the illegal’s pipe address space, thus hurting the last pipe of the BAM if the BAM had a total 4, 8 or 16 pipes. This is relevant for Producer to System modes only. (CR-0000151585) 1’b1 - Enabled 1’b0 - Disable Available in BAM only
21	BAM_WB_CSW_ACK_IDL	Recommended value: 1 This bit allows the Writeback state machine to switch into idle state prior to visiting disabled state. This is needed when context switching from mode X to another pipe of mode X is well. This is required to fix a bug in the 2 pipes BAM. 1’b1 - Enable 1’b0 - Disable Available in BAM only
20	BAM_WB_BLK_CSW	Recommended value: 1 When Enabled, this bit does not allow context switch to happen in the Writeback state machine until it has created a descriptor. This is relevant when the descriptor fifo is becoming full and there’s no space to create a descriptor, while another pipe is context switching. This might result in the descriptor not to be created ever, if it was the last one for that pipe. Relevant for Producer BAM-to-BAM mode only. 1’b1 - Enable 1’b0 - Disable Available in BAM only

SDC4_BAM_CNFG_BITS (cont.)

Bits	Name	Description
19	BAM_WB_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Writeback state machine when performing pipe reset. 1'b1 - 1'b0 - Disable Available in BAM only
18	BAM_SI_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Sideband Inform state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
17	BAM_AU_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Ack Update state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
16	BAM_PSM_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Pipe state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
15	BAM_PSM_CSW_REQ	Recommended value: 1 This bit forces the context switch request from pipe state machine to RAM controller not to last longer than the slave requested. (2 Pipes BAM bug fix) 1'b1 - Enable 1'b0 - Disable Available in BAM only
14	BAM_SB_CLK_REQ	Recommended value: 1 This bit allows the clock request from the sideband block to propagate into the BAM's common clock request. 1'b1 - Propagate Sideband Clock Request 1'b0 - Disable Available in BAM only
13	BAM_IBC_DISABLE	Recommended value: 1 This bit helps to save power by allowing the BAM to keep the inactivity base counter in reset when BAM is disabled or when SW configures IBC_DISABLE bit high. 1'b1 - Enable Power Saving 1'b0 - Disable Power Saving

SDC4_BAM_CNFG_BITS (cont.)

Bits	Name	Description
12	BAM_NO_EXT_P_RST	Recommended value: 1 This bit allows the BAM / BAM Lite to ignore the externally connected blocks (eDML) when doing pipe reset. The BAM, once instructed to pipe reset, first thing lets the externally connected block know a reset is needed. Then it waits for the externally connected block to Acknowledge it is ready for the pipe reset (meaning it doesn't push any data for the reset pipe) and then the BAM Lite completes the pipe reset operation internally. When disabled, the BAM doesn't require any Acknowledge from the external block to perform pipe reset. 1’b1 - Enable external block pipe reset 1’b0 - Disable - ignore external block pipe reset
11	BAM_FULL_PIPE	Recommended value: 0 This enables the BAM support for a BAM to BAM Producer which insists to write to a full pipe. When 0, BAM might issue data overflow if producers write to a full pipe. When 1 BAM will not allow this and lower HReady when peripheral tries to do so. Once space is freed in the pipe, Hready will rise and the flow will continue. This functionality has been found to be buggy and was removed from APQ8064. Bit is currently unused. 1’b1 - Enable 1’b0 - Disable Available in BAM only
10:4	RESERVED_BITS10_4	Set to Zero (0)
3	BAM_ADML_SYNC_BRIDGE	0x1: Use a Synchronous Configuration bridge in aDML. 0x0: Use a Asynchronous Configuration bridge in aDML.
2	BAM_PIPE_CNFG	Recommended value: 1 Pipe SM upgrade for writing EOT bit to the previous descriptor. It’s invoked only when EOB arrives in the end of a descriptor. It is highly recommended to set this bit high. Leaving it low might cause incorrect Pipe Bytes Free value reported to peripheral in rare cases. 1’b1 - Enable 1’b0 - Disable Available in BAM only
1	BAM_ADML_DEEP_CONS_FIFO	0x1: Use a deep Consumer FIFO in aDML (16 dwords) 0x0: Use a shallow Consumer FIFO in aDML (8 dwords)
0	BAM_ADML_INCR4_EN_N	0x1: Don’t allow INCR4 aDML-BAM accesses. 0x0: Allow INCR 4 aDML-BAM accesses.

0x121C3800+ 128*n SDC4_BAM_IRQ_SRCS_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register has an alias - BAM_IRQ_SRCS register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

SDC4_BAM_IRQ_SRCS_EEn

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x121C3804+ 128*n SDC4_BAM_IRQ_SRCS_MSK_EEn, n=[0..3]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register has an alias - BAM_IRQ_SRCS_MSK register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

SDC4_BAM_IRQ_SRCS_MSK_EEn

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x121C3808+ 128*n SDC4_BAM_IRQ_SRCS_UNMASKED_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register has an alias - BAM_IRQ_SRCS_UNMASKED register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

SDC4_BAM_IRQ_SRCS_UNMASKED_EEn

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

20.21.2 BAM PIPE management registers

BAM Pipe management registers control each pipe's parameters. Those reside in physical registers.

0x121C2000+ 128*n SDC4_BAM_P_CTRLn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Control register provides various controls for the pipe.

SDC4_BAM_P_CTRLn

Bits	Name	Description
31:11	RESERVED_BITS31_11	Set to Zero (0)
10:9	P_PREFETCH_LIMIT	Bam Lite feature Selects the number of bytes to be pre-fetched by the Bam Lite, once a peripheral requests to read data from a pipe. This feature is relevant for Consumer modes only. 2'b00 - 32 bytes at most (INCR8) 2'b01 - 16 bytes at most (INCR4) 2'b10 - 4 bytes at most (SINGLE) Available in BAM-Lite only

SDC4_BAM_P_CTRLn (cont.)

Bits	Name	Description
8:7	P_AUTO_EOB_SEL	Bam Lite feature. Selects the number of bytes to be processed before creating End Of Block indication internally by the BAM. See P_AUTO_EOB. Descriptors generated by this feature (bam to bam producer mode) will always be of the chosen size, unless an End Of Transfer, causes a smaller descriptor to be created. 2'b00 - 512 Bytes 2'b01 - 256 Bytes 2'b10 - 128 Bytes 2'b11 - 64 Bytes Available in BAM-Lite only
6	P_AUTO_EOB	BAM Lite feature. When Enabled, the BAM Lite will ignore any incoming End Of Block indications from the peripheral (if any). Instead, the BAM Lite will generate it's own End Of Block indications internally, every P_AUTO_EOB_SEL bytes. This feature is relevant for Producer Bam 2 Bam modes only. It is a must for peripherals which are not able to produce End Of Block indications. 1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
5	P_SYS_MODE	This bit sets the pipe to work in System Mode, where the Software is the second side of the pipe. 1'b1 - System mode. 1'b0 - BAM to BAM mode.
4	P_SYS_STRM	Streaming Enable. Relevant to System Producer BAM mode only.When enabled, BAM will not close descriptors with End Of Transfer notifications received from peripheral, but continue writing the data to the same descriptor. 1'b1 - Enable Streaming Mode 1'b0 - None-Streaming Mode
3	P_DIRECTION	This bit denotes pipe direction. 1'b1 - The pipe can be written (producer mode) 1'b0 - The pipe can be read (consumer mode)
2	RESERVED_BITS2	Set to Zero (0)
1	P_EN	1'b1 - Enable Pipe 1'b0 - Disable Pipe
0	RESERVED_BITS0	Set to Zero (0)

0x121C2004+ 128*n SDC4_BAM_P_RSTn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Reset register provides Pipe Reset ability. Software needs to write 1 to this register to make the Pipe Reset. Writing 0 to this register will finish the Pipe Reset. Writing zero is needed prior to Peripheral reconfiguration for the same pipe.

SDC4_BAM_P_RSTn

Bits	Name	Description
31:1	RESERVED_BITS31_1	Set to Zero (0)
0	P_SW_RST	This resets the pipe and its' registers, (Both Flip-Flops and RAM). 1'b1 - Reset 1'b0 - Do Nothing

0x121C2008+ 128*n SDC4_BAM_P_HALTn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Halt register Enables/Disables the Halt Sequence.

This is a self-modifying register.

SDC4_BAM_P_HALTn

Bits	Name	Description
31:2	RESERVED_BITS31_2	Set to Zero (0)
1	P_PROD_HALTED	This bit is used to inform the Consumer about the Producer being in Halt mode now. This is a part of the Halt procedure. 1'b1 - Sets this bit to 1 1'b0 - Does Nothing This bit will be cleared by the HW.
0	P_HALT	When Enabled, the Pipe will enter Halt Mode. 1'b1 - Enable Halt 1'b0 - Disable Halt For B2B Producer pipes, this bit is self modifying. It doesn't need the SW to clear it..

0x121C2030+ 128*n SDC4_BAM_P_TRUST_REGn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

SDC4_BAM_P_TRUST_REGn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_P_VMID	Those bits indicate the VMID value to be used when performing Pipe type accesses to the bus. BAM Type accesses include Pipe MTI, Data and Descriptors.
7:2	RESERVED_BITS7_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_P_EE	This Field Indicates the EE (0,1,2,3) to which the Pipe Interrupt belongs to. The BAM interrupt will fire to the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x121C2010+ 128*n SDC4_BAM_P_IRQ_STTSn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only. It also has informative bits which are not interrupts.

Clearing the interrupt bits is done by writing to P_IRQ_CLR register.

SDC4_BAM_P_IRQ_STTSn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_IRQ	For producer this interrupt happens whenever the last AHB burst of a transfer happens For Consumer when ack_on_success closes a transfer
4	P_ERR_IRQ	Pipe Error interrupt indicates that an error has happened. TBD: Error reason is not yet defined. Interrupt not in use.
3	P_OUT_OF_DESC_IRQ	Out of descriptors interrupt has several meanings depending on the operation mode: Producer - no free space in the descriptors fifo for adding a descriptor Consumer - no descriptors in the descriptors fifo for processing IO Vectors Producer - No descriptors to read (and therefore no space for data to write to the pipe) IO Vectors Consumer - No descriptors to read (and therefore no data to read from pipe)
2	P_WAKE_IRQ	Wake peripheral interrupt signals the driver to wake up the peripheral (USB for example) for transmission via the current pipe. This interrupt is issued whenever an Event comes to the specific pipe.
1	P_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
0	P_PRCSD_DESC_IRQ	This Interrupt rises when BAM finishes processing an IO Vector which has INT bit selected

0x121C2014+ 128*n SDC4_BAM_P_IRQ_CLRn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

SDC4_BAM_P_IRQ_CLRn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_CLR	1’b1 - Clear 1’b0 - Unchanged
4	P_ERR_CLR	1’b1 - Clear 1’b0 - Unchanged
3	P_OUT_OF_DESC_CLR	1’b1 - Clear 1’b0 - Unchanged

SDC4_BAM_P_IRQ_CLRn (cont.)

Bits	Name	Description
2	P_WAKE_CLR	Clear Wake peripheral interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
1	P_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
0	P_PRCSD_DESC_CLR	Clear Descriptor Processed interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged

0x121C2018+ 128*n SDC4_BAM_P_IRQ_ENn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the Pipe Interrupt Status register.

SDC4_BAM_P_IRQ_ENn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_EN	1'b1 - Enable 1'b0 - Disable
4	P_ERR_EN	1'b1 - Enable 1'b0 - Disable
3	P_OUT_OF_DESC_EN	1'b1 - Enable 1'b0 - Disable
2	P_WAKE_EN	Enable Wake peripheral interrupt 1'b1 - Enable 1'b0 - Disable
1	P_TIMER_EN	Enable Inactivity timer Interrupt 1'b1 - Enable 1'b0 - Disable
0	P_PRCSD_DESC_EN	Enable Descriptor Processed Interrupt 1'b1 - Enable 1'b0 - Disable

0x121C201C+128*n SDC4_BAM_P_TIMERn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the pipe.

SDC4_BAM_P_TIMERn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x121C2020+128*n SDC4_BAM_P_TIMER_CTRLn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The resolution of the pipe inactivity timers are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the P_TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * P_TIMER_TRSHLD.

SDC4_BAM_P_TIMER_CTRLn

Bits	Name	Description
31	P_TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the P_TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	P_TIMER_RUN	Will be used along with P_TIMER_MODE Not implemented at this time. Set to zero(0)
29	P_TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	P_TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x121C2024+ 128*n SDC4_BAM_P_PRDCR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Producer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

SDC4_BAM_P_PRDCR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_producer
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	BAM_P_TOGGLE	Pipe Bytes Free Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Free Ctrl value
15:0	BAM_P_BYTES_FREE	Pipe Bytes Free value

0x121C2028+ 128*n SDC4_BAM_P_CNSMR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Consumer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

SDC4_BAM_P_CNSMR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_consumer
23	BAM_P_WAIT_4_ACK	waiting_for_ack_bytes_avail_r
22	BAM_P_ACK_TOGGLE	ack_bytes_avail_toggle
21	BAM_P_ACK_TOGGLE_R	ack_bytes_avail_toggle_r
20	BAM_P_TOGGLE	Pipe Bytes Avail Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Avail Ctrl value
15:0	BAM_P_BYTES_AVAIL	Pipe Bytes AVAIL value

20.21.3 BAM PIPE configuration registers (RAM)

BAM Pipe management registers configure each pipes' parameters.

Pipe Address span: currently defining each pipe to have 32 addresses, therefore inter pipe offset is 32*4=128=0x80 bytes.

0x121C302C+64*n SDC4_BAM_P_EVNT_DEST_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Event Destination Address which is the address of BAM_P_EVNT_REG in the BAM on the other side of the Pipe.

Producer BAM will send Write Events to this address.

Consumer BAM will send Read Events to this address.

This is relevant only for BAM to BAM modes. In System modes, BAM doesn't issue Write/Read events.

SDC4_BAM_P_EVNT_DEST_ADDRn

Bits	Name	Description
31:0	P_EVNT_DEST_ADDR	Address of the Event Register in the peer BAM (second end of the pipe). Driver will configure this when initializing the pipe.

0x121C3018+ 64*n SDC4_BAM_P_EVNT_REGn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register is where Read/Write events are sent to. If current BAM works as Producer, it will receive Read events into this register from the Consumer. If the Consumer is another BAM, it will write read events to this register. If the Consumer is the Software, it will prepare descriptors in the descriptor FIFO and update the DESC_FIFO_PEER_OFST value in this register.

If current BAM works as Consumer, opposite behavior is assumed.

SDC4_BAM_P_EVNT_REGn

Bits	Name	Description
31:16	P_BYTES_CONSUMED	This field is used only in the B2B mode. It indicates the number of bits consumed by the Consumer. Consumer sends this value to the Producer as a part of a read event, for the Producer to know how many bytes were consumed. When working in System mode, this value should be set to zero. BAM to BAM Producer writes zero in this value.
15:0	P_DESC_FIFO_PEER_OFST	This field indicates the Descriptor Fifo Offset Pointer of the Peer BAM (The BAM or the Software which creates descriptors). For example when current BAM works as consumer for the current pipe, Producer BAM (or the software) updates this value to let the current pipe know about the new descriptors added in the Descriptor Fifo.

0x121C3000+ 64*n SDC4_BAM_P_SW_OFSTSn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register denotes the pointer Offset of the first Not Acknowledged Descriptor. Meaning all Descriptors prior to this one have been processed by the BAM. This register is only used by the Software. After receiving an interrupt, software reads this register in order to know what descriptors has been processed.

When the BAM works as Producer, Software will usually read this value after Descriptor Processed Interrupt or after the End of Transfer Interrupt.

When the BAM works as Consumer, Software will usually read this value after Descriptor Processed Interrupt.

NOTE This is non relevant in BAM to BAM modes.

NOTE Although being Writable, Software should never write to this register.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC4_BAM_P_SW_OFSTSn

Bits	Name	Description
31:16	SW_OFST_IN_DESC	Offset inside the Descriptor. This value is used by the Software only when a BAM is working as System Producer. Then the SW can read this value to know how many Bytes were written to the current descriptor if it was not closed down. This is useful for Streaming mode.
15:0	SW_DESC_OFST	Descriptor FIFO offset.

0x121C3024+64*n SDC4_BAM_P_DATA_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Beginning of the Data Address space.

This register is non relevant in System Modes.

SDC4_BAM_P_DATA_FIFO_ADDRn

Bits	Name	Description
31:0	P_DATA_FIFO_ADDR	Data Address Space beginning.

0x121C301C+64*n SDC4_BAM_P_DESC_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Address of the Descriptor Fifo beginning.

NOTE This register is used by all modes.

SDC4_BAM_P_DESC_FIFO_ADDRn

Bits	Name	Description
31:0	P_DESC_FIFO_ADDR	Address of the Descriptors Fifo. This address must be 8 bytes aligned.

0x121C3028+ 64*n SDC4_BAM_P_EVNT_GEN_TRSHLDn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register configures the threshold value for Read/Write event generation by the BAM towards another BAM. When a BAM pushes/pops this number of bytes to/from the pipe an event to the other BAM will be generated. A counter summing up the bytes pushed/popped is reset when event is issued, thus restarting count for the threshold.

Events are also issued after End Of Transfer received from the peripheral (Producer case), non regarding whether the pushed bytes count has reached the threshold or not.

This register is non relevant in System Modes.

SDC4_BAM_P_EVNT_GEN_TRSHLDn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TRSHLD	Threshold value. The maximum allowed value is 32kByte.

0x121C3020+ 64*n SDC4_BAM_P_FIFO_SIZESn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

The least significant field is the Descriptor Fifo Size.

The most significant field is the Data Fifo Size.

NOTE This Descriptor Fifo Size is used by all modes. The Data Fifo Size is non relevant in System Modes.

SDC4_BAM_P_FIFO_SIZESn

Bits	Name	Description
31:16	P_DATA_FIFO_SIZE	Size of the Data Address Space.
15:0	P_DESC_FIFO_SIZE	Size of the Descriptors Fifo. Must be 8 byte aligned. Each descriptor is 8 bytes. Size of the descriptor fifo must contain an integer number of Descriptors.

20.21.4 BAM PIPE internal state registers (RAM)

BAM Pipe debug registers allow a software look inside on the internal parameters of the BAM State Machines stored in RAM.

Those shouldn't be normally used or altered by the software.

0x121C3034+ 64*n SDC4_BAM_P_RETR_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context stored for retransmission.

This is being stored by Ack Update state machine in consumer mode or by the Writeback state machine in producer mode.

This is being loaded by the Writeback state machine when retransmission happens.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC4_BAM_P_RETR_CNTXT_n

Bits	Name	Description
31:16	RETR_DESC_OFST	Descriptor Fifo Offset for retransmission.
15:0	RETR_OFST_IN_DESC	The Offset inside the Descriptor for retransmission.

0x121C3038+ 64*n SDC4_BAM_P_SI_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Sideband Inform state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC4_BAM_P_SI_CNTXT_n

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	SI_DESC_OFST	The Descriptor Fifo Offset pointer stored by the Sideband Inform state machine.

0x121C3004+ 64*n SDC4_BAM_P_AU_PSM_CNTXT_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Ack Update state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC4_BAM_P_AU_PSM_CNTXT_1_n

Bits	Name	Description
31:16	AU_PSM_ACCUMED	PSM: The acknowledged (EOB/T) number of bytes since last Write Event. AU: The accumulation of the descriptor sizes for the present ack_on_success event. This is never bigger than the ACKED field. Once the ACCUMED values are bigger than Event Threshold, an Event will be issued, the ACKED value will decrease by the ACCUMED size and this value will be zeroed. This also serves as the Bytes Consumed value in the Event.
15:0	AU_ACKED	AU: The left over of the number of bytes that were received via the ack_on_success, that did not cause a descriptor closure. This value is down counting upon issuing Read Event. PSM:

0x121C3008+ 64*n SDC4_BAM_P_PSM_CNTXT_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC4_BAM_P_PSM_CNTXT_2_n

Bits	Name	Description
31	PSM_DESC_VALID	The Descriptor Valid bit provided by the Writeback state machine to Pipe state machine.
30	PSM_DESC_IRQ	The Descriptor Interrupt bit provided by the Writeback state machine to pipe state machine.
29	PSM_DESC_IRQ_DONE	The Descriptor Interrupt needed selection bit.
28:25	PSM_GENERAL_BITS	General Context Switch Bits
24:22	PSM_CONS_STATE	State of the Pipe Consumer state machine.
21:19	PSM_PROD_SYS_STATE	State of the Pipe Producer System state machine.
18:16	PSM_PROD_B2B_STATE	State of the Pipe Producer BAM to BAM state machine.
15:0	PSM_DESC_SIZE	The Descriptor Size provided by the Writeback state machine to pipe state machine.

0x121C300C+64*n SDC4_BAM_P_PSM_CNTXT_3_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC4_BAM_P_PSM_CNTXT_3_n

Bits	Name	Description
31:0	PSM_DESC_ADDR	The Data Address provided in the current descriptor from the Writeback state machine.

0x121C3010+64*n SDC4_BAM_P_PSM_CNTXT_4_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC4_BAM_P_PSM_CNTXT_4_n

Bits	Name	Description
31:16	PSM_DESC_OFST	The running Descriptor Fifo Offset of the Writeback state machine
15:0	PSM_SAVED_ACCUMED_SIZE	The Saved Accumulated Size from the Pipe state machine.

0x121C3014+ 64*n SDC4_BAM_P_PSM_CNTXT_5_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC4_BAM_P_PSM_CNTXT_5_n

Bits	Name	Description
31:16	PSM_BLOCK_BYTE_CNT	The Byte count inside the current Block.
15:0	PSM_OFST_IN_DESC	The Offset inside a register. This is used by pipe state machine to compute offset inside a register after retransmission

0x121C3030+ 64*n SDC4_BAM_P_RESERVED_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

SDC4_BAM_P_RESERVED_1_n

Bits	Name	Description
31:0	BAM_P_RES_1	Set to zero (0) Reserved

0x121C303C+64*n SDC4_BAM_P_RESERVED_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

SDC4_BAM_P_RESERVED_2_n

Bits	Name	Description
31:0	BAM_P_RES_2	Set to zero (0) Obsolete Register: BAM_P_IRQ_DEST_ADDRn, n=[0..30]

20.22 BAM DMA Registers (0x12240000 BAM_DMA_BASE)

This section contains the BAM DMA registers.

The BAM registers may be accessed via a burst on AHB.

Registers in this file are offsets from zero. DMA_BASE_ADDRESS is allocated separately since DMA block in instantiated in a standalone BAM.

0x12240000 BAM_DMA_DMA_ENBL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000001

This register enables the BAM DMA.

BAM_DMA_DMA_ENBL

Bits	Name	Description
31:1	RESERVED_BITS31_1	Set to Zero (0)
0	DMA_ENABLE	When de-asserted - will stop any transaction in any channel of DMA

0x12240004+4*n BAM_DMA_DMA_CHNL_CONFIGn, n=[0..9]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000131

This register configures channel number n.

Bits [18:16] are read only.

BAM_DMA_DMA_CHNL_CONFIGn

Bits	Name	Description
31:19	RESERVED_BITS31_19	Set to Zero (0)
18	PRODUCER_PIPE_ENABLED	When 0x1 - Producer pipe (as received from BAM) is enabled)
17	CONSUMER_PIPE_ENABLED	When 0x1 - Consumer pipe (as received from BAM) is enabled
16	DMA_CHNL_HALT_DONE	Channel n has inserted halt functionality. Read only bit
15:13	RESERVED_BITS15_13	Set to Zero (0)

BAM_DMA_DMA_CHNL_CONFIGn (cont.)

Bits	Name	Description
12	DMA_CHNL_HALT	Halt channel n
11:9	RESERVED_BITS11_9	
8	DMA_CHNL_ENABLE	Enable channel n
7:6	RESERVED_BITS7_6	
5:4	DMA_CHNL_ACT_THRESH	This field sets the threshold value of the channel 2'b11 - 512 Bytes 2'b10 - 256 Bytes 2'b01 - 128 Bytes 2'b00 - 64 Bytes
3	RESERVED_BITS3	Set to Zero (0)
2:0	DMA_CHNL_WEIGHT	This field sets the weight of the channel. The higher the weight is the more successive transactions are allowed. 3'b111 - Weight is 7 3'b110 - Weight is 6 3'b101 - Weight is 5 3'b100 - Weight is 4 3'b011 - Weight is 3 3'b010 - Weight is 2 3'b001 - Weight is 1 3'b000 - Channel won't be invoked. If set to this value when this channel id currently active, it would finish its chunk as with former weight and then be disabled

0x1224003C BAM_DMA_DMA_REVISION

Type: Read
Clock: BAM_CLK
Reset State: 0X00000001

This register holds a hard coded revision of the DMA RTL.

BAM_DMA_DMA_REVISION

Bits	Name	Description
31:0	REVISION	This fields holds the RTL version of the DMA (hard-coded).

0x12240040 BAM_DMA_DMA_CONFIG

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This register selects the testbus bits of BAM DMA.

BAM_DMA_DMA_CONFIG

Bits	Name	Description
31:2	RESERVED_BITS31_2	Set to Zero (0)
1:0	TESTBUS_SELECT	0x3: All bits are zero. 0x2: BAM testbus is selected 0x1: BAM_DMA testbus is selected 0x0: All bits are zero (default.)

20.23 BAM DMA BAM Registers (0x12244000 BAM_DMA_BAM_BASE)

This section contains the BAM DMA BAM registers.

BAM supports only Word (4 byte) aligned writes and reads on the Configuration Bus interface.

BAM has MAX_PIPES hardware generic parameter defining the number of pipes it supports. Each BAM can have up to 31 pipes supported.

BAM has BAM_CONF_AHBS_ADDR_WIDTH hardware generic parameter defining the Bit Number for selecting BAM access or Peripheral access. Legal Ranges are 14 to 20. Count starts from 1, meaning a value of 17 will set BAM Base address as 0x0001_0000.

20.23.1 BAM control registers

BAM Control registers configure the BAM operational state, SW reset, interrupts and others.

0x12244F80 BAM_DMA_BAM_CTRL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

BAM Control register allows global controls for the BAM.

BAM_DMA_BAM_CTRL

Bits	Name	Description
31:17	RESERVED_BITS31_17	Set to Zero (0)
16	IBC_DISABLE	This Bit enables power saving by disabling the inactivity clock timer/counter. This is useful when: 1) The BAM is Enabled but idling for long periods. 2) The BAM is Enabled and running but the inactivity timers/counters are not required by the SW for operating the BAM. When the BAM is Disabled, it automatically shuts down those timers to save power. 1’b1 - Enable Power Saving Mode 1’b0 - Disable Power Saving Mode

BAM_DMA_BAM_CTRL (cont.)

Bits	Name	Description
15	BAM_CACHED_DESC_STORE	This Bit enables storage of a cached Descriptor into RAM when doing Context Switch and loading it back when returning to this pipe. This is relevant for System Modes Only. BAM to BAM Consumer mode doesn't have this option. Enabling this makes the Context Switch process slightly longer but reduces AHB Descriptor Fetch time later on. It also reduces the number of descriptor fetches done by the BAM if BAM is treating more than 2 pipes. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
14:13	BAM_DESC_CACHE_SEL	This Selector chooses which Descriptor Caching mode will be used. This is relevant for System Producer or Consumer modes only. 2’b00 - Cache when current descriptor has less than 64 bytes left. 2’b01 - Cache when current descriptor has less than 128 bytes left. 2’b10 - Immediate Auto cache - cache will happen whenever there are no descriptors cached. This might cause unnecessary descriptors reads when switching between more than 2 pipes. It is the most effective when each pipe processes more bytes than there are in an average descriptor (small descriptors, big block size), or when working with 2 or less pipes. 2’b11 - Cache when descriptor is needed only. This results in 1 descriptor present in cache at most. Available in BAM only
12	RESERVED_BITS12	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_SIC_SEL
11:5	BAM_TESTBUS_SEL	Set to Zero (0) Obsolete field: BAM_TESTBUS_SEL Test Bus selector. Supported until (including) bam_p3q3r29 (BlackBird). Moved to a dedicated register - BAM_TEST_BUS_SEL in the following releases.
4	BAM_EN_ACCUM	When Enabled, BAM will accumulate data written by the peripheral in Direct Mode into INCR8 Bursts. This is an optimization feature for Producer Direct Mode cases. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
3	RESERVED_BITS3	Set to Zero (0)
2	RESERVED_BITS2	Set to Zero (0)

BAM_DMA_BAM_CTRL (cont.)

Bits	Name	Description
1	BAM_EN	After reset the BAM wakes up in Disabled Mode. While Disabled, BAM operates in Legacy mode (all the transfers from the peripheral go around the BAM as if it doesn't exist) Software Enables this bit to allow BAM operation. This bit doesn't affect the PIPE enable bit in BAM_P_CTRL register. The only possibility to Disable the BAM after it has been enabled is by Hardware or Software reset. 1'b1 - Enabled 1'b0 - Disabled
0	BAM_SW_RST	This will reset the BAM & all Pipes. Software may use this to reset the BAM. As long as the bit remains high the BAM remains in reset state. Software should clear this bit 1'b1 - Reset state 1'b0 - Normal state

0x12244F84 BAM_DMA_BAM_REVISION

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a hard coded revision number of the BAM RTL. This corresponds to the BAM target number in the IMS. Also additional BAM settings are reflected here.

BAM_DMA_BAM_REVISION

Bits	Name	Description
31:24	INACTIV_TMR_BASE	This indicates the width of the inactivity timers base counter
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	NUM_INACTIV_TMRS	This bit is checked only if INACTIV_TMRS_EXST = 1. This bit indicates how many inactivity timers are implemented according to value of INACTIVITY_TIMERS_SUPPORTED generic: 1'b1 - One timer for global BAM activity (INACTIVITY_TIMERS_SUPPORTED = 1) 1'b0 - MAX_PIPES timers for each pipe activity (INACTIVITY_TIMERS_SUPPORTED = 2)
19	INACTIV_TMRS_EXST	This indicates BAM has inactivity timers. 1'b1 - Timers available (INACTIVITY_TIMERS_SUPPORTED = 1 or 2) 1'b0 - No timers available (INACTIVITY_TIMERS_SUPPORTED = 0)

BAM_DMA_BAM_REVISION (cont.)

Bits	Name	Description
18	HIGH_FREQUENCY_BAM	This indicates BAM has Double Sampling on the Ack On Success interface. 1'b1 - Ack On Success double sampled 1'b0 - No double sampling of Ack On Success
17	BAM_HAS_NO_BYPASS	This field indicates BAM has no bypass on the AHB Data bus, from the Peripheral AHB Master to the fabric. When Bypass is available, it is the default routing when BAM is disabled. 1'b1 - No Bypass 1'b0 - Bypass Exists
16	SECURED	This field indicates BAM/BAM-Lite has security support (APU inside) 1'b1 - Secured 1'b0 - Not Secured
15:12	RESERVED_BITS15_12	Set to Zero (0)
11:8	NUM_EES	This indicates the Number of Interrupt Lines (Execution Environments) supported by the BAM. When 1 EE is supported, only the BAM_IRQ_SRCS*_EE0 registers exist. When 4 EEs are supported, all BAM_IRQ_SRCS*_EEn registers exist for n=[0..3].
7:0	REVISION	This field contains the revision number of the core, Hard Coded. 8'h01 - Voyager (bam_p3q3r22 +) 8'h02 - BlackBird (bam_p3q3r27 +) 8'h03 - Waverider BAM (bam_p3q3r30 +) 8'h04 - Aurora BAM (bam_p3q2r43 +) 8'h05 - Shelby BAM (bam_p2q2r45 +) 8'h10 - Waverider BAM Lite (bam_lite_p1q1r0 +) 8'h11 - Aurora BAM Lite (bam_lite_p3q2r16 +) 8'h12 - Shelby BAM Lite (bam_lite_p2q2r18 +)

0x12244FBC BAM_DMA_BAM_NUM_PIPES

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a the hard coded number of pipes in the BAM. Since each BAM may have a different number of pipes instantiated in HW, this register allows the SW to know this parameter. The reset state value doesn't have any meaning in this register since it is a constant.

BAM_DMA_BAM_NUM_PIPES

Bits	Name	Description
31:24	BAM_NON_PIPE_GRP	This field contains the number of BAM Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
23:16	PERIPH_NON_PIPE_GRP	This field contains the number of Peripheral's Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
15:8	RESERVED_BITS15_8	Set to Zero (0)
7:0	BAM_NUM_PIPES	This field contains the number of pipes available in this BAM

0x12244FC0 BAM_DMA_BAM_TIMER

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the BAM (all the pipes are in idle state).

BAM_DMA_BAM_TIMER

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12244FC4 BAM_DMA_BAM_TIMER_CTRL

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The register can be written and read only when INACTIVITY_TIMERS_SUPPORTED generic equals to 1.

The resolution of the BAM inactivity timer are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define

the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * TIMER_TRSHLD.

BAM_DMA_BAM_TIMER_CTRL

Bits	Name	Description
31	TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1 to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	TIMER_RUN	Will be used along with TIMER_MODE Not implemented at this time. Set to zero(0)
29	TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12244F88 BAM_DMA_BAM_DESC_CNT_TRSHLD

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds a threshold value for the counter summing the Size of the Descriptors Provided. This value is Global for all pipes but it is relevant for System Producer BAM mode and Both Consumer modes, where Descriptors summing takes place in order to provide the information to the peripheral via pipe bytes free (producer) or pipe bytes available interfaces.

BAM_DMA_BAM_DESC_CNT_TRSHLD

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0).
15:0	CNT_TRSHLD	Threshold value. The maximum allowed value is 32kByte. Available in BAM only

0x12244F8C BAM_DMA_BAM_IRQ_SRCS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking out this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register points to the physical BAM_IRQ_SRCS_EE0 register.

BAM_DMA_BAM_IRQ_SRCS

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12244F90 BAM_DMA_BAM_IRQ_SRCS_MSK

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register points to the physical BAM_IRQ_SRCS_MSK_EE0 register.

BAM_DMA_BAM_IRQ_SRCS_MSK

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12244FB0 BAM_DMA_BAM_IRQ_SRCS_UNMASKED

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register points to the physical BAM_IRQ_SRCS_UNMASKED_EE0 register.

BAM_DMA_BAM_IRQ_SRCS_UNMASKED

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

0x12244F94 BAM_DMA_BAM_IRQ_STTS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only.

Clearing the interrupt bits is done by writing to BAM_IRQ_CLR register.

BAM_DMA_BAM_IRQ_STTS

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
3	BAM_EMPTY_IRQ	This interrupt is for DEBUG purpose only. It should not be used in normal SW flows. The interrupt indicates the BAMs buffer is empty. This bit can become high only when BAM_DATA_ERASE or BAM_DATA_FLUSH is high in BAM_TEST_BUS_SEL register.
2	BAM_ERROR_IRQ	This Indicates a Fatal Error has happened in the BAM. Currently this might happen due to an UnSuccessful Pipe Reset operation.

BAM_DMA_BAM_IRQ_STTS (cont.)

Bits	Name	Description
1	BAM_HRESP_ERR_IRQ	This interrupt Indicates that an Erroneous HResponse has been received by the AHB Master. Additional Information about the error may be read at BAM_AHB_MASTER_ERR_* Registers. Clearing this interrupt also clears the BAM_AHB_MASTER_ERR_* Registers. Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12244F98 BAM_DMA_BAM_IRQ_CLR

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

BAM_DMA_BAM_IRQ_CLR

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
3	BAM_EMPTY_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM-Lite only
2	BAM_ERROR_CLR	1'b1 - Clear 1'b0 - Unchanged
1	BAM_HRESP_ERR_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12244F9C BAM_DMA_BAM_IRQ_EN

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the BAM Interrupt Status register.

BAM_DMA_BAM_IRQ_EN

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_EN	Enables Inactivity timer interrupt by writing this bit 1'b1 - Enable 1'b0 - Disable
3	BAM_EMPTY_EN	1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
2	BAM_ERROR_EN	1'b1 - Enable 1'b0 - Disable
1	BAM_HRESP_ERR_EN	1'b1 - Enable 1'b0 - Disable Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12244FA0 BAM_DMA_BAM_RESERVED_1

Type: Read
Clock: BAM_CLK
Reset State: 0x00000000

BAM_DMA_BAM_RESERVED_1

Bits	Name	Description
31	RESERVED_BITS31	Set to Zero (0) Obsolete field: BAM_IRQ_SIC_SEL
30:0	RESERVED_BITS30_0	Set to Zero (0) Obsolete field: P_IRQ_SIC_SEL

0x12244FA4 BAM_DMA_BAM_AHB_MASTER_ERR_CTRLS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

BAM_DMA_BAM_AHB_MASTER_ERR_CTRLS

Bits	Name	Description
31:23	RESERVED_BITS31_16	Set to Zero (0)
22:18	BAM_ERR_HVMID	HVMID
17	BAM_ERR_DIRECT_MODE	DIRECT MODE
16:12	BAM_ERR_HCID	HCID
11:8	BAM_ERR_HPROT	HPROT
7:5	BAM_ERR_HBURST	HBURST
4:3	BAM_ERR_HSIZE	HSIZE
2	BAM_ERR_HWRITE	HWRITE
1:0	BAM_ERR_HTRANS	HTRANS

0x12244FA8 BAM_DMA_BAM_AHB_MASTER_ERR_ADDR

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

BAM_DMA_BAM_AHB_MASTER_ERR_ADDR

Bits	Name	Description
31:0	BAM_ERR_ADDR	HADDR

0x12244FAC BAM_DMA_BAM_AHB_MASTER_ERR_DATA

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

BAM_DMA_BAM_AHB_MASTER_ERR_DATA

Bits	Name	Description
31:0	BAM_ERR_DATA	HDATA

0x12244FB4 BAM_DMA_BAM_RESERVED_2

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

BAM_DMA_BAM_RESERVED_2

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_IRQ_DEST_ADDR

0x12244FB8 BAM_DMA_BAM_RESERVED_3

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

BAM_DMA_BAM_RESERVED_3

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_DEST_ADDR

0x12244FF0 BAM_DMA_BAM_TRUST_REG

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside - SECURED field in the BAM_REVISION register) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

BAM_DMA_BAM_TRUST_REG

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_VMID	Those bits indicate the VMID value to be used when performing BAM type accesses to the bus. BAM Type accesses include BAM MTI (or Direct Mode accesses, not applicable for BAM Lite)
7	BAM_RST_BLOCK	When enabled, the BAM Global SW reset will not be available for usage. This is in order to deny Global SW reset requests by the Global security group. 1'b1 - Enable 1'b0 - Disable
6:2	RESERVED_BITS6_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_EE	This Field Indicates the EE (0,1,2,3) to which the BAM Interrupt belongs to. The pipe interrupts will fire on the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12244FF4 BAM_DMA_BAM_TEST_BUS_SEL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This is the testbus selector register.

Supported in releases after bam_p3q3r29 (BlackBird).

BAM_DMA_BAM_TEST_BUS_SEL

Bits	Name	Description
31:19	RESERVED_BITS31_19	Set to Zero (0)
18	BAM_DATA_ERASE	When enabled, BAM will be instructed to erase all the data it currently has inside. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Erase 1'b0 - Disabled
17	BAM_DATA_FLUSH	When enabled, BAM will be instructed to flush all the data it currently has inside. BAM will only flush the data once it has enough data and a valid destination for it. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Flush 1'b0 - Disabled
16	BAM_CLK_ALWAYS_ON	This bit controls the BAM to issue 'always on' clock request. 1'b1 - Enable Always On clock request. 1'b0 - Disabled
15:7	RESERVED_BITS15_7	Set to Zero (0)
6:0	BAM_TESTBUS_SEL	Test Bus selector. Values with bit[11] set high are reserved for the BAM Lite integrator to provide testbus from outside of the BAM Lite. For example, eDML testbus may reside at X'100_0000' to X'111_1111' selector values. eDML has no registers thus has no test bus selector, so its test bus is combined with the BAM lite's. BAM provides zeroes on its testbus when external values selected. X'000_0000' - Zeros X'000_0001' - Slave test bus X'000_0010' - Pipe state machine test bus X'000_0011' - Buffer test bus X'000_0100' - Sideband test bus X'000_1101' - Bus Manager test bus X'001_0000' - Reg file test bus X'1''_''''' - BAM Lite sets zeroes on the test bus, leaving it for external use

0x12244FF8 BAM_DMA_BAM_TEST_BUS_REG

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the value being output to the testbus of the chip. It is not intended for SW usage but for lab debugging of the BAM. Values here can change every cycle.

BAM_DMA_BAM_TEST_BUS_REG

Bits	Name	Description
31:0	BAM_TESTBUS_REG	32 bit Testbus value. To select the Block in BAM to show here, use the BAM_TESTBUS_SEL field in BAM_CTRL register.

0x12244FFC BAM_DMA_BAM_CNFG_BITS

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM configuration bits for bug fixes. It is highly recommended to follow the directions for each bit and set it accordingly.

BAM_DMA_BAM_CNFG_BITS

Bits	Name	Description
31:27	RESERVED_BITS31_27	Set to Zero (0)
26	BAM_AU_ACCUMED	Recommended value: 1 This bit fixes a bug in the Ack Update state machine, where an overflow happened while counting descriptors and reaching more than 64kB of calculated sizes. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only
25	BAM_PSM_P_HD_DATA	Recommended value: 1 This bit allows pipe state machine to ignore retransmission requests if a pipe has just been initialized and process those as a regular fetch request. (consumer modes only). When this bit disabled, BAM could fetch descriptors for a pipe which was reset and no descriptors were added yet, if a retransmission request followed after the reset. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only

BAM_DMA_BAM_CNFG_BITS (cont.)

Bits	Name	Description
24	BAM_REG_P_EN	Recommended value: 1 This bit fixes the pipe configuration signals mux for the current active pipe in 2 pipes BAM. When disabled, internal state machines might get into enabled states while the pipe is disabled. This would typically happen after pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
23	BAM_WB_DSC_AVL_P_RST	Recommended value: 1 This bit allows the Writeback state machine to reset the vector indicating there are available descriptors when a pipe reset occurs. If disabled, BAM might fetch descriptors after resetting and reconfiguring a pipe, even though no Event (descriptors) was provided.. 1’b1 - Enable 1’b0 - Disable Available in BAM only
22	BAM_WB_RETR_SVPNT	Recommended value: 1 This bit fixes a bug where a pipe which was reset, still stored its retransmission savepoint, but into the illegal’s pipe address space, thus hurting the last pipe of the BAM if the BAM had a total 4, 8 or 16 pipes. This is relevant for Producer to System modes only. (CR-0000151585) 1’b1 - Enabled 1’b0 - Disable Available in BAM only
21	BAM_WB_CSW_ACK_IDL	Recommended value: 1 This bit allows the Writeback state machine to switch into idle state prior to visiting disabled state. This is needed when context switching from mode X to another pipe of mode X is well. This is required to fix a bug in the 2 pipes BAM. 1’b1 - Enable 1’b0 - Disable Available in BAM only
20	BAM_WB_BLK_CSW	Recommended value: 1 When Enabled, this bit does not allow context switch to happen in the Writeback state machine until it has created a descriptor. This is relevant when the descriptor fifo is becoming full and there’s no space to create a descriptor, while another pipe is context switching. This might result in the descriptor not to be created ever, if it was the last one for that pipe. Relevant for Producer BAM-to-BAM mode only. 1’b1 - Enable 1’b0 - Disable Available in BAM only

BAM_DMA_BAM_CNFG_BITS (cont.)

Bits	Name	Description
19	BAM_WB_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Writeback state machine when performing pipe reset. 1'b1 - 1'b0 - Disable Available in BAM only
18	BAM_SI_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Sideband Inform state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
17	BAM_AU_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Ack Update state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
16	BAM_PSM_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Pipe state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
15	BAM_PSM_CSW_REQ	Recommended value: 1 This bit forces the context switch request from pipe state machine to RAM controller not to last longer than the slave requested. (2 Pipes BAM bug fix) 1'b1 - Enable 1'b0 - Disable Available in BAM only
14	BAM_SB_CLK_REQ	Recommended value: 1 This bit allows the clock request from the sideband block to propagate into the BAM's common clock request. 1'b1 - Propagate Sideband Clock Request 1'b0 - Disable Available in BAM only
13	BAM_IBC_DISABLE	Recommended value: 1 This bit helps to save power by allowing the BAM to keep the inactivity base counter in reset when BAM is disabled or when SW configures IBC_DISABLE bit high. 1'b1 - Enable Power Saving 1'b0 - Disable Power Saving

BAM_DMA_BAM_CNFG_BITS (cont.)

Bits	Name	Description
12	BAM_NO_EXT_P_RST	Recommended value: 1 This bit allows the BAM / BAM Lite to ignore the externally connected blocks (eDML) when doing pipe reset. The BAM, once instructed to pipe reset, first thing lets the externally connected block know a reset is needed. Then it waits for the externally connected block to Acknowledge it is ready for the pipe reset (meaning it doesn't push any data for the reset pipe) and then the BAM Lite completes the pipe reset operation internally. When disabled, the BAM doesn't require any Acknowledge from the external block to perform pipe reset. 1’b1 - Enable external block pipe reset 1’b0 - Disable - ignore external block pipe reset
11	BAM_FULL_PIPE	Recommended value: 0 This enables the BAM support for a BAM to BAM Producer which insists to write to a full pipe. When 0, BAM might issue data overflow if producers write to a full pipe. When 1 BAM will not allow this and lower HReady when peripheral tries to do so. Once space is freed in the pipe, Hready will rise and the flow will continue. This functionality has been found to be buggy and was removed from APQ8064. Bit is currently unused. 1’b1 - Enable 1’b0 - Disable Available in BAM only
10:4	RESERVED_BITS10_4	Set to Zero (0)
3	BAM_ADML_SYNC_BRIDGE	0x1: Use a Synchronous Configuration bridge in aDML. 0x0: Use a Asynchronous Configuration bridge in aDML.
2	BAM_PIPE_CNFG	Recommended value: 1 Pipe SM upgrade for writing EOT bit to the previous descriptor. It’s invoked only when EOB arrives in the end of a descriptor. It is highly recommended to set this bit high. Leaving it low might cause incorrect Pipe Bytes Free value reported to peripheral in rare cases. 1’b1 - Enable 1’b0 - Disable Available in BAM only
1	BAM_ADML_DEEP_CONS_FIFO	0x1: Use a deep Consumer FIFO in aDML (16 dwords) 0x0: Use a shallow Consumer FIFO in aDML (8 dwords)
0	BAM_ADML_INCR4_EN_N	0x1: Don’t allow INCR4 aDML-BAM accesses. 0x0: Allow INCR 4 aDML-BAM accesses.

0x12245800+ 128*n BAM_DMA_BAM_IRQ_SRCS_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register has an alias - BAM_IRQ_SRCS register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

BAM_DMA_BAM_IRQ_SRCS_EEn

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12245804+ 128*n BAM_DMA_BAM_IRQ_SRCS_MSK_EEn, n=[0..3]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register has an alias - BAM_IRQ_SRCS_MSK register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

BAM_DMA_BAM_IRQ_SRCS_MSK_EEn

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12245808+ 128*n BAM_DMA_BAM_IRQ_SRCS_UNMASKED_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register has an alias - BAM_IRQ_SRCS_UNMASKED register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

BAM_DMA_BAM_IRQ_SRCS_UNMASKED_EEn

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

20.23.2 BAM PIPE management registers

BAM Pipe management registers control each pipe's parameters. Those reside in physical registers.

0x12244000+ 128*n BAM_DMA_BAM_P_CTRLn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Control register provides various controls for the pipe.

BAM_DMA_BAM_P_CTRLn

Bits	Name	Description
31:11	RESERVED_BITS31_11	Set to Zero (0)
10:9	P_PREFETCH_LIMIT	Bam Lite feature Selects the number of bytes to be pre-fetched by the Bam Lite, once a peripheral requests to read data from a pipe. This feature is relevant for Consumer modes only. 2'b00 - 32 bytes at most (INCR8) 2'b01 - 16 bytes at most (INCR4) 2'b10 - 4 bytes at most (SINGLE) Available in BAM-Lite only

BAM_DMA_BAM_P_CTRLn (cont.)

Bits	Name	Description
8:7	P_AUTO_EOB_SEL	Bam Lite feature. Selects the number of bytes to be processed before creating End Of Block indication internally by the BAM. See P_AUTO_EOB. Descriptors generated by this feature (bam to bam producer mode) will always be of the chosen size, unless an End Of Transfer, causes a smaller descriptor to be created. 2'b00 - 512 Bytes 2'b01 - 256 Bytes 2'b10 - 128 Bytes 2'b11 - 64 Bytes Available in BAM-Lite only
6	P_AUTO_EOB	BAM Lite feature. When Enabled, the BAM Lite will ignore any incoming End Of Block indications from the peripheral (if any). Instead, the BAM Lite will generate it's own End Of Block indications internally, every P_AUTO_EOB_SEL bytes. This feature is relevant for Producer Bam 2 Bam modes only. It is a must for peripherals which are not able to produce End Of Block indications. 1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
5	P_SYS_MODE	This bit sets the pipe to work in System Mode, where the Software is the second side of the pipe. 1'b1 - System mode. 1'b0 - BAM to BAM mode.
4	P_SYS_STRM	Streaming Enable. Relevant to System Producer BAM mode only.When enabled, BAM will not close descriptors with End Of Transfer notifications received from peripheral, but continue writing the data to the same descriptor. 1'b1 - Enable Streaming Mode 1'b0 - None-Streaming Mode
3	P_DIRECTION	This bit denotes pipe direction. 1'b1 - The pipe can be written (producer mode) 1'b0 - The pipe can be read (consumer mode)
2	RESERVED_BITS2	Set to Zero (0)
1	P_EN	1'b1 - Enable Pipe 1'b0 - Disable Pipe
0	RESERVED_BITS0	Set to Zero (0)

0x12244004+ 128*n BAM_DMA_BAM_P_RSTn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Reset register provides Pipe Reset ability. Software needs to write 1 to this register to make the Pipe Reset. Writing 0 to this register will finish the Pipe Reset. Writing zero is needed prior to Peripheral reconfiguration for the same pipe.

BAM_DMA_BAM_P_RSTn

Bits	Name	Description
31:1	RESERVED_BITS31_1	Set to Zero (0)
0	P_SW_RST	This resets the pipe and its' registers, (Both Flip-Flops and RAM). 1'b1 - Reset 1'b0 - Do Nothing

0x12244008+ 128*n BAM_DMA_BAM_P_HALTn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Halt register Enables/Disables the Halt Sequence.

This is a self-modifying register.

BAM_DMA_BAM_P_HALTn

Bits	Name	Description
31:2	RESERVED_BITS31_2	Set to Zero (0)
1	P_PROD_HALTED	This bit is used to inform the Consumer about the Producer being in Halt mode now. This is a part of the Halt procedure. 1'b1 - Sets this bit to 1 1'b0 - Does Nothing This bit will be cleared by the HW.
0	P_HALT	When Enabled, the Pipe will enter Halt Mode. 1'b1 - Enable Halt 1'b0 - Disable Halt For B2B Producer pipes, this bit is self modifying. It doesn't need the SW to clear it.

0x12244030+ 128*n BAM_DMA_BAM_P_TRUST_REGn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

BAM_DMA_BAM_P_TRUST_REGn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_P_VMID	Those bits indicate the VMID value to be used when performing Pipe type accesses to the bus. BAM Type accesses include Pipe MTI, Data and Descriptors.
7:2	RESERVED_BITS7_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_P_EE	This Field Indicates the EE (0,1,2,3) to which the Pipe Interrupt belongs to. The BAM interrupt will fire to the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12244010+ 128*n BAM_DMA_BAM_P_IRQ_STTSn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only. It also has informative bits which are not interrupts.

Clearing the interrupt bits is done by writing to P_IRQ_CLR register.

BAM_DMA_BAM_P_IRQ_STTSn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_IRQ	For producer this interrupt happens whenever the last AHB burst of a transfer happens For Consumer when ack_on_success closes a transfer
4	P_ERR_IRQ	Pipe Error interrupt indicates that an error has happened. TBD: Error reason is not yet defined. Interrupt not in use.
3	P_OUT_OF_DESC_IRQ	Out of descriptors interrupt has several meanings depending on the operation mode: Producer - no free space in the descriptors fifo for adding a descriptor Consumer - no descriptors in the descriptors fifo for processing IO Vectors Producer - No descriptors to read (and therefore no space for data to write to the pipe) IO Vectors Consumer - No descriptors to read (and therefore no data to read from pipe)
2	P_WAKE_IRQ	Wake peripheral interrupt signals the driver to wake up the peripheral (USB for example) for transmission via the current pipe. This interrupt is issued whenever an Event comes to the specific pipe.
1	P_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
0	P_PRCSD_DESC_IRQ	This Interrupt rises when BAM finishes processing an IO Vector which has INT bit selected

0x12244014+128*n BAM_DMA_BAM_P_IRQ_CLRn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

BAM_DMA_BAM_P_IRQ_CLRn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_CLR	1'b1 - Clear 1'b0 - Unchanged
4	P_ERR_CLR	1'b1 - Clear 1'b0 - Unchanged
3	P_OUT_OF_DESC_CLR	1'b1 - Clear 1'b0 - Unchanged

BAM_DMA_BAM_P_IRQ_CLRn (cont.)

Bits	Name	Description
2	P_WAKE_CLR	Clear Wake peripheral interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
1	P_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
0	P_PRCSD_DESC_CLR	Clear Descriptor Processed interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged

0x12244018+ 128*n BAM_DMA_BAM_P_IRQ_ENn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the Pipe Interrupt Status register.

BAM_DMA_BAM_P_IRQ_ENn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_EN	1'b1 - Enable 1'b0 - Disable
4	P_ERR_EN	1'b1 - Enable 1'b0 - Disable
3	P_OUT_OF_DESC_EN	1'b1 - Enable 1'b0 - Disable
2	P_WAKE_EN	Enable Wake peripheral interrupt 1'b1 - Enable 1'b0 - Disable
1	P_TIMER_EN	Enable Inactivity timer Interrupt 1'b1 - Enable 1'b0 - Disable
0	P_PRCSD_DESC_EN	Enable Descriptor Processed Interrupt 1'b1 - Enable 1'b0 - Disable

0x1224401C+ 128*n BAM_DMA_BAM_P_TIMERn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the pipe.

BAM_DMA_BAM_P_TIMERn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12244020+ 128*n BAM_DMA_BAM_P_TIMER_CTRLn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The resolution of the pipe inactivity timers are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the P_TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * P_TIMER_TRSHLD.

BAM_DMA_BAM_P_TIMER_CTRLn

Bits	Name	Description
31	P_TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the P_TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	P_TIMER_RUN	Will be used along with P_TIMER_MODE Not implemented at this time. Set to zero(0)
29	P_TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	P_TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12244024+ 128*n BAM_DMA_BAM_P_PRDCR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Producer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

BAM_DMA_BAM_P_PRDCR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_producer
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	BAM_P_TOGGLE	Pipe Bytes Free Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Free Ctrl value
15:0	BAM_P_BYTES_FREE	Pipe Bytes Free value

0x12244028+ 128*n BAM_DMA_BAM_P_CNSMR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Consumer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

BAM_DMA_BAM_P_CNSMR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_consumer
23	BAM_P_WAIT_4_ACK	waiting_for_ack_bytes_avail_r
22	BAM_P_ACK_TOGGLE	ack_bytes_avail_toggle
21	BAM_P_ACK_TOGGLE_R	ack_bytes_avail_toggle_r
20	BAM_P_TOGGLE	Pipe Bytes Avail Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Avail Ctrl value
15:0	BAM_P_BYTES_AVAIL	Pipe Bytes AVAIL value

20.23.3 BAM PIPE configuration registers (RAM)

BAM Pipe management registers configure each pipes' parameters.

Pipe Address span: currently defining each pipe to have 32 addresses, therefore inter pipe offset is 32*4=128=0x80 bytes.

0x1224502C+ 64*n BAM_DMA_BAM_P_EVNT_DEST_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Event Destination Address which is the address of BAM_P_EVNT_REG in the BAM on the other side of the Pipe.

Producer BAM will send Write Events to this address.

Consumer BAM will send Read Events to this address.

This is relevant only for BAM to BAM modes. In System modes, BAM doesn't issue Write/Read events.

BAM_DMA_BAM_P_EVNT_DEST_ADDRn

Bits	Name	Description
31:0	P_EVNT_DEST_ADDR	Address of the Event Register in the peer BAM (second end of the pipe). Driver will configure this when initializing the pipe.

0x12245018+64*n BAM_DMA_BAM_P_EVNT_REGn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register is where Read/Write events are sent to. If current BAM works as Producer, it will receive Read events into this register from the Consumer. If the Consumer is another BAM, it will write read events to this register. If the Consumer is the Software, it will prepare descriptors in the descriptor FIFO and update the DESC_FIFO_PEER_OFST value in this register.

If current BAM works as Consumer, opposite behavior is assumed.

BAM_DMA_BAM_P_EVNT_REGn

Bits	Name	Description
31:16	P_BYTES_CONSUMED	This field is used only in the B2B mode. It indicates the number of bits consumed by the Consumer. Consumer sends this value to the Producer as a part of a read event, for the Producer to know how many bytes were consumed. When working in System mode, this value should be set to zero. BAM to BAM Producer writes zero in this value.
15:0	P_DESC_FIFO_PEER_OFST	This field indicates the Descriptor Fifo Offset Pointer of the Peer BAM (The BAM or the Software which creates descriptors). For example when current BAM works as consumer for the current pipe, Producer BAM (or the software) updates this value to let the current pipe know about the new descriptors added in the Descriptor Fifo.

0x12245000+64*n BAM_DMA_BAM_P_SW_OFSTSn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register denotes the pointer Offset of the first Not Acknowledged Descriptor. Meaning all Descriptors prior to this one have been processed by the BAM. This register is only used by the Software. After receiving an interrupt, software reads this register in order to know what descriptors has been processed.

When the BAM works as Producer, Software will usually read this value after Descriptor Processed Interrupt or after the End of Transfer Interrupt.

When the BAM works as Consumer, Software will usually read this value after Descriptor Processed Interrupt.

NOTE This is non relevant in BAM to BAM modes.

NOTE Although being Writable, Software should never write to this register.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

BAM_DMA_BAM_P_SW_OFSTSn

Bits	Name	Description
31:16	SW_OFST_IN_DESC	Offset inside the Descriptor. This value is used by the Software only when a BAM is working as System Producer. Then the SW can read this value to know how many Bytes were written to the current descriptor if it was not closed down. This is useful for Streaming mode.
15:0	SW_DESC_OFST	Descriptor FIFO offset.

0x12245024+64*n BAM_DMA_BAM_P_DATA_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Beginning of the Data Address space.

This register is non relevant in System Modes.

BAM_DMA_BAM_P_DATA_FIFO_ADDRn

Bits	Name	Description
31:0	P_DATA_FIFO_ADDR	Data Address Space beginning.

0x1224501C+64*n BAM_DMA_BAM_P_DESC_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Address of the Descriptor Fifo beginning.

NOTE This register is used by all modes.

BAM_DMA_BAM_P_DESC_FIFO_ADDRn

Bits	Name	Description
31:0	P_DESC_FIFO_ADDR	Address of the Descriptors Fifo. This address must be 8 bytes aligned.

0x12245028+64*n BAM_DMA_BAM_P_EVNT_GEN_TRSHLDn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register configures the threshold value for Read/Write event generation by the BAM towards another BAM. When aBAM pushes/pops this number of bytes to/from the pipe an event to the other BAM will be generated. A counter summing up the bytes pushed/popped is reset when event is issued, thus restarting count for the threshold.

Events are also issued after End Of Transfer received from the peripheral (Producer case), non regarding whether the pushed bytes count has reached the threshold or not.

This register is non relevant in System Modes.

BAM_DMA_BAM_P_EVNT_GEN_TRSHLDn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TRSHLD	Threshold value. The maximum allowed value is 32kByte.

0x12245020+64*n BAM_DMA_BAM_P_FIFO_SIZESn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

The least significant field is the Descriptor Fifo Size.

The most significant field is the Data Fifo Size.

NOTE This Descriptor Fifo Size is used by all modes. The Data Fifo Size is non relevant in System Modes.

BAM_DMA_BAM_P_FIFO_SIZESn

Bits	Name	Description
31:16	P_DATA_FIFO_SIZE	Size of the Data Address Space.
15:0	P_DESC_FIFO_SIZE	Size of the Descriptors Fifo. Must be 8 byte aligned. Each descriptor is 8 bytes. Size of the descriptor fifo must contain an integer number of Descriptors.

20.23.4 BAM PIPE internal state registers (RAM)

BAM Pipe debug registers allow a software look inside on the internal parameters of the BAM State Machines stored in RAM.

Those shouldn't be normally used or altered by the software.

0x12245034+64*n BAM_DMA_BAM_P_RETR_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context stored for retransmission.

This is being stored by Ack Update state machine in consumer mode or by the Writeback state machine in producer mode.

This is being loaded by the Writeback state machine when retransmission happens.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

BAM_DMA_BAM_P_RETR_CNTXT_n

Bits	Name	Description
31:16	RETR_DESC_OFST	Descriptor Fifo Offset for retransmission.
15:0	RETR_OFST_IN_DESC	The Offset inside the Descriptor for retransmission.

0x12245038+64*n BAM_DMA_BAM_P_SI_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Sideband Inform state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

BAM_DMA_BAM_P_SI_CNTXT_n

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	SI_DESC_OFST	The Descriptor Fifo Offset pointer stored by the Sideband Inform state machine.

0x12245004+ 64*n BAM_DMA_BAM_P_AU_PSM_CNTXT_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Ack Update state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

BAM_DMA_BAM_P_AU_PSM_CNTXT_1_n

Bits	Name	Description
31:16	AU_PSM_ACCUMED	PSM: The acknowledged (EOB/T) number of bytes since last Write Event. AU: The accumulation of the descriptor sizes for the present ack_on_success event. This is never bigger than the ACKED field. Once the ACCUMED values are bigger than Event Threshold, an Event will be issued, the ACKED value will decrease by the ACCUMED size and this value will be zeroed. This also serves as the Bytes Consumed value in the Event.
15:0	AU_ACKED	AU: The left over of the number of bytes that were received via the ack_on_success, that did not cause a descriptor closure. This value is down counting upon issuing Read Event. PSM:

0x12245008+ 64*n BAM_DMA_BAM_P_PSM_CNTXT_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

BAM_DMA_BAM_P_PSM_CNTXT_2_n

Bits	Name	Description
31	PSM_DESC_VALID	The Descriptor Valid bit provided by the Writeback state machine to Pipe state machine.
30	PSM_DESC_IRQ	The Descriptor Interrupt bit provided by the Writeback state machine to pipe state machine.
29	PSM_DESC_IRQ_DONE	The Descriptor Interrupt needed selection bit.
28:25	PSM_GENERAL_BITS	General Context Switch Bits
24:22	PSM_CONS_STATE	State of the Pipe Consumer state machine.
21:19	PSM_PROD_SYS_STATE	State of the Pipe Producer System state machine.
18:16	PSM_PROD_B2B_STATE	State of the Pipe Producer BAM to BAM state machine.
15:0	PSM_DESC_SIZE	The Descriptor Size provided by the Writeback state machine to pipe state machine.

0x1224500C+64*n BAM_DMA_BAM_P_PSM_CNTXT_3_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

BAM_DMA_BAM_P_PSM_CNTXT_3_n

Bits	Name	Description
31:0	PSM_DESC_ADDR	The Data Address provided in the current descriptor from the Writeback state machine.

0x12245010+64*n BAM_DMA_BAM_P_PSM_CNTXT_4_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

BAM_DMA_BAM_P_PSM_CNTXT_4_n

Bits	Name	Description
31:16	PSM_DESC_OFST	The running Descriptor Fifo Offset of the Writeback state machine
15:0	PSM_SAVED_ACCUMED_SIZE	The Saved Accumulated Size from the Pipe state machine.

0x12245014+64*n BAM_DMA_BAM_P_PSM_CNTXT_5_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

BAM_DMA_BAM_P_PSM_CNTXT_5_n

Bits	Name	Description
31:16	PSM_BLOCK_BYTE_CNT	The Byte count inside the current Block.
15:0	PSM_OFST_IN_DESC	The Offset inside a register. This is used by pipe state machine to compute offset inside a register after retransmission

0x12245030+64*n BAM_DMA_BAM_P_RESERVED_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

BAM_DMA_BAM_P_RESERVED_1_n

Bits	Name	Description
31:0	BAM_P_RES_1	Set to zero (0) Reserved

0x1224503C+64*n BAM_DMA_BAM_P_RESERVED_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

BAM_DMA_BAM_P_RESERVED_2_n

Bits	Name	Description
31:0	BAM_P_RES_2	Set to zero (0) Obsolete Register: BAM_P_IRQ_DEST_ADDRn, n=[0..30]

20.24 BAM DMA XPU Registers (0x12246000 BAM_DMA_BAM_XPU_BASE)

This section contains the BAM DMA XPU registers.

0x12246000+4*n BAM_DMA_APU_RGn_ACR, n=[0..38]

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

(Read) Access Control Registers: This description is for the case when APU_IDR[MV, PT] = 10, i.e, a multi-VMID full access vs. no access permission type APU. These registers include a single bit per VMID granting full access

BAM_DMA_APU_RGn_ACR

Bits	Name	Description
31:0	RWE	Read/Write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the registers in the associated resource group.

0x12246F80 BAM_DMA_APU_CR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

APU Configuration Register: This register includes fields governing various APU behaviors.

BAM_DMA_APU_CR

Bits	Name	Description
31:4	RESERVED31_4	Reserved
3	DCDEE	Decode Error Enable: Governs whether or not configuration port decode errors (i.e., invalid addresses) are recorded as such. 0xDCDEE: 0 - do not record. Decode errors do not set APU_ESR. APU_EAR and APU_ESYNR0 not updated. 0xDCDEE: 1 - record. Decode errors set APU_ESR. APU_EAR and APU_ESYNR0 updated with address and syndrome of error.
2	APUEIE	APU Error Interrupt Enable. Governs whether the client port and the configuration port errors are reported directly to the interrupt controller via the interrupt output of the APU. Interrupt output is asserted if APU_CR[APUEIE] = 1 and any bit is set in APU_ESR

BAM_DMA_APU_CR (cont.)

Bits	Name	Description
1	APUERE	APU Error Report Enable. APUERE = 0 causes the APU to treat configuration port errors as RAZ/WI, and to simply pass client port errors through to the slave device. Errors are not reported to the requesting master APUERE = 1 enables client port and configuration port errors to be reported to the requesting master according to the particular bus protocol of the respective APU port. Errors from either port are terminated by the APU as RAZ/WI Both client and configuration port errors are recorded in APU_ESR, independent of the value of APU_CR[APUERE]
0	APUE	APU Enable. Governs whether APU checking occurs for both the client port and the configuration port. This bit is cleared (0) by reset. It is set (1) once SROT configures APU and the MID to VMID mapping tables.

0x12246F84 BAM_DMA_APU_EAR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Address Register. This register captures the address upon errors detected by the APU, for both the client port and the configuration port.

BAM_DMA_APU_EAR

Bits	Name	Description
31:0	PA	The physical address of the errant request.

0x12246F88 BAM_DMA_APU_ESR

Type: Read/Write-clear
Clock: XPU_CLK
Reset State: 0x00000000

Error Status Register. This register captures the status upon errors detected by the APU, for both the client port and the configuration port.

This register has read/write-clear access, meaning that reads simply read the value in the register, while writes are performed by clearing those bits corresponding to 1s in the written data, and leaving unchanged those bits corresponding to 0s in the written data. This prevents inadvertent clearing of new errors when writing the register to clear an old The presence of an asserted value on any bit in this register is what prompts the assertion of the APU's interrupt output (when enabled by APU_CR[IE]). Therefore, these bits must be cleared by the interrupt handler. This is

contrasted with the fields in the APU_ESYNRn registers, which are merely the "syndrome" of an error indicated by APU_ESR.

BAM_DMA_APU_ESR

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x12246F8C BAM_DMA_APU_ESRRESTORE

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error RestoreRegister: This is just an aliased address for APU_ESR, which provides direct write access (rather than write-clear) for restoration purposes.

BAM_DMA_APU_ESRRESTORE

Bits	Name	Description
31	MULTI	Multi-error: Indicates additional error occurred while APU_ESR[CFG, CLIENT] still non-zero. APU_EAR and APU_ESYNRn registers (and APU_ESR itself, except for the MULTI bit) "lock" upon first error, APU_ESR must be cleared to unlock.Status, address and syndrome of errors that occur while APU_ESR is non-zero are lost.
30:2	RESERVED30_2	Reserved
1	CLIENT	Client Port Error. Indicates error (access control is the only type) associated with a client port request.
0	CFG	Configuration Port Error. Indicates error (access control or decode) associated with a configuration port request.

0x12246F90 BAM_DMA_APU_ESYNR0

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

BAM_DMA_APU_ESYNR0

Bits	Name	Description
31:24	ATID	ATID field of errant request.
23:21	RESERVED23_21	Reserved
20:16	AVMID	AVMID field of errant request.
15:13	ABID	ABID field of errant request.
12:8	APID	APID field of errant request.
7:0	AMID	AMID field of errant request.

0x12246F94 BAM_DMA_APU_ESYNR1

Type: Read/Write
Clock: XPU_CLK
Reset State: 0x00000000

Error Syndrome Register. Captures the syndrome upon errors detected by the APU, for both the client port and the configuration port.

BAM_DMA_APU_ESYNR1

Bits	Name	Description
31	DCD	Decode. Indicates error due to invalid/unrecognized address (e.g., a reserved register address).
30	AC	Access Control. Indicates error due to lack of permission, as specified by the access control registers.
29:25	RESERVED29_25	Reserved
24	AFULL	AFULL field of errant request
23	RESERVED23	Reserved.
22	AOOO	AOOO field of errant request
21:20	ALOCK	ALOCK field of errant request
19	RESERVED19	Reserved

BAM_DMA_APU_ESYNR1 (cont.)

Bits	Name	Description
18:16	ASIZE	ASIZE field of errant request.
15:12	ALEN	ALEN field of errant request.
11	RESERVED11	Reserved.
10	ABURST	ABURST field of errant request.
9	RESERVED9	Reserved.
8	AWRITE	AWRITE field of errant request.
7	AINST	AINST field of errant request.
6	APROTNS	APROTNS field of errant request.
5	APRIV	APRIV field of errant request.
4	AINNERSHARED	AINNERSHARED field of errant request.
3	ASHARED	ASHARED field of errant request.
2:0	AMEMTYPE	AMEMTYPE field of errant request.

0x12246FF4 BAM_DMA_APU_REV

Type: Read
Clock: XPU_CLK
Reset State: 0x00000011

Revision Register. This register provides major/minor revision codes for the implementation.

BAM_DMA_APU_REV

Bits	Name	Description
31:8	RESERVED31_8	Reserved
7:4	MAJOR	Major variant field
3:0	MINOR	Minor variant field

0x12246FF8 BAM_DMA_APU_IDR

Type: Read
Clock: XPU_CLK
Reset State: 0x00001426

APU ID Register: Read-only register that defines various configuration attributes of the APU instance.

BAM_DMA_APU_IDR

Bits	Name	Description
31:29	RESERVED31_21	Reserved
28:24	MSB	Indicates most significant address bit number used to select a resource group
23:21	RESERVED23_21	Reserved
20:16	LSB	Indicates least significant address bit number used to select a resource group.
15:14	RESERVED15_14	Reserved
13:12	XPUT	Indicates type of xPU (hardwired to 0b00 for RPU 0x0: RPU 0x1: APU 0x2: MPU 0x3: reserved
11	PT	Permission type PT=0 : indicates full access vs. no access type. Only APU_RGn_ACR registers needed, and they specify which VMID(s) have full access (other VMIDs have no access) PT=1 : indicates read/write access type vs. read-only access type. For multi-VMID, separate APU_RGn_RACR and APU_RGn_WACR registers govern read vs. write access. For single VMID, APU_RGn_ACR registers include separate 5-bit read/write vs. read-only "owner" VMID fields
10	MV	Multi-VMID MV=0 : indicates single VMID type access control. APU_RGn_ACR registers indicate single 5 bit "owner" VMID field for governing access. MV=1 : indicates multi-VMID type access control. APU_RGn_xACR registers include separate bit per VMID (32 bits) for governing access.
9	RESERVED9	Reserved
8:0	NRG	Number of resource groups: Indicates number of resource groups (minus 1) supported by the APU. Value can range between 0 and 255 (1-256 resource groups).

0x12246FFC BAM_DMA_APU_APU_ACR

Type: Read/Write
Clock: XPU_CLK
Reset State: 0xFFFFFFFF

APU Access Control Register: This register includes a bit per VMID governing configuration port access to the registers of the APU (including the APU_APU_ACR itself).

BAM_DMA_APU_APU_ACR

Bits	Name	Description
31:0	RWE	Read/write enable. Each bit corresponds to a VMID, which when set to 1 grants that VMID read/write access to the entire block of registers within the APU's 4KB address region (including the APU_APU_ACR itself). For single VMID type APUs (APU_IDR[MV] = 0) the APU_APU_ACR is also used to identify the VMIDs. In practice, this register designates the ASID(s) that can act as SROT.

20.25 SDC1 Registers (0x12400000 SDC1_BASE)

This section contains the SDC1 base registers.

0x12400000 SDC1_MCI_POWER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x00000000

(ARM name: MCIPower)

SDC1_MCI_POWER

Bits	Name	Description
31:7	RESERVED_1	Always reads zero. Writes 'don't care' but by convention write zero.
6	OPEN_DRAIN	MCICMD Output Control. See Note 2 below
5:1	RESERVED_2	Always reads zero. Writes 'don't care' by convention write zero.
0	CONTROL	This register is used to control the operation of the memory controller. value 0: power-off value 1: power-on Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_POWER register and before accessing this register again. Note:2 - This bit is reserved for the use mentioned in the Description but it is not implemented in HW. The open drain mode is preserved such that when enabled, the command output is driven low when the logic is low and undriven (so that the pull up can pull high) when the logic is high. Whether this gets used in the system is up to SW/system but the HW does support this mode.

0x12400004 SDC1_MCI_CLK

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x01008000

(ARM name: MCIClock)

SDC1_MCI_CLK

Bits	Name	Description
31:27	RESERVED_1	Always reads zero. Writes ’don’t care’ but by convention write zero.
26	SDCC_CLK_EXT_EN	Value 0 (default) - sdcc_clkout is driven via the clock pad and external clock can’t be used for testing the cm_dll_sdc4. Value 1- External clock can be used as a test clock.
25	RX_FLOW_TIMING	Configuration bit which selects the cycle which RxFlowControl will be asserted when UHS mode is used Value 0 (default) - RxFlowControl is asserted one clock before the end bit is received in DPSM (NextBlkTCnt in DPSM equals to 1). Value 1 - RxFlowControl is asserted two clocks before the end bit is received in DPSM (NextBlkTCnt in DPSM equals to 2).
24:23	SDC4_MCLK_SEL	Selects the sdc4_mclk - input clock of cm_dll_sdc4 Value 0 - gated version of MCLK Value 1 - feedback clock from CLK pad Value 2 (default) - free running mclk (gated between the transactions)
22	CLK_INV	When set(1), the input clock which is inserted into the input macros is inverted.
21	IO_PAD_PWR_SWITCH	Indication to Pad that power has to be switched from 3.3V to 1.8V.
20	CLK_FB_DLY_SEL	Selects the source of feedback clock used by the controller. Value 1 - output of cm_dll_sdc4 is used as feedback clock Value 0 - feedback clock from CLK pad is used
19:18	SD_DEV_SEL	Select the active device if more than one device are connected in shared bus mode. (range: ’00’ - ’11’).
17	HCLKON_SW_EN	SW enable of AHB clock request of SDCC4. value 0: HW clock request mechanism is used value 1: clock request signal is always high
16:14	SELECT_IN	Select to latch data and command coming in: value 000: on the falling edge of internal MCLK. value 001: on the rising edge of internal MCLK. value 010: using feedback clock (default). value 011: DDR mode - In DDR mode, the SDC_CLK output will be SDCn_APPS_CLK divided by 2. value 100: UHS mode - MCLK is used internally. value 101: UHS mode - divided frequency (MCLK/2) is used internally.
13	INVERT_OUT	Clear (0) to change data and command going out on the falling edge. Set (1) to change data and command going out on the rising edge.
12	FLOW_ENA	Enable flow control: value 0: disable (default) value 1: enable

SDC1_MCI_CLK (cont.)

Bits	Name	Description
11:10	WIDEBUS	Enable wide bus mode: value 00: 1 bit mode value 10: 4 bit mode value 01 or 11: 8 bit mode
9	PWRSAVE	Disable Prime-Cell MCI clock output when bus is idle to save power. value 0: Power save disabled - always enabled if bit 8 is set. value 1: Power save enabled - clock enabled only when bus is active and bit 8 is set.
8	ENABLE	Enable Prime-Cell MCI bus clock: value 0: clock disabled value 1: clock enabled
7:0	RESERVED_2	Always reads zero. Writes 'don't care' but by convention write zero. Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_CLK register and before accessing this register again.

0x12400008 SDC1_MCI_ARGUMENT

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIArgument)

SDC1_MCI_ARGUMENT

Bits	Name	Description
31:0	CMD_ARG	Command argument.

0x1240000C SDC1_MCI_CMD

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x00000000

(ARM name: MMCCommand) CPSM: 'Command Path State Machine'.

SDC1_MCI_CMD

Bits	Name	Description
31:17	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
16	AUTO_CMD19	If set (1), CPSM sends CMD19 automatically before sending CMD17 or CMD18. This sequence is needed for CDR auto-calibration of cm_dll_sdc4.
15	CCS_DISABLE	If set (1), CPSM sends Command_Completion_Signal (CCS) disable sequence to the external CE-ATA device.
14	CCS_ENABLE	If set (1), CPSM waits for CCS from external card CE-ATA device.
13	MCIABORT	Signals the next command will be an abort (stop) command. This bit always read as (0) due to the hardware implementation. See note 2 below.
12	DAT_CMD	If set (1) indicates that this is a Command with Data. See note 2 below.
11	PROG_ENA	If set (1), PROG_DONE status bit will be asserted when busy is de-asserted. This bit is to be used with a stop or status command after a block write is performed. Does not effect CPSM.
10	ENABLE	The action of writing to this register (MCI_CMD) with this bit set (1), triggers CPSM to leave the ’Idle State’. .
9	PENDING	If set (1), CPSM waits for ’CmdPend’ from the DPSM before it starts sending a command. See note 3 below.
8	INTERRUPT	If set (1), CPSM disables command timer and waits for interrupt request (Card Response). See note 4 below.
7	LONGRSP	If set (1), receives a 136-bit long response.
6	RESPONSE	If set (1), CPSM waits for a response subject to INTERRUPT above.

SDC1_MCI_CMD (cont.)

Bits	Name	Description
5:0	CMD_INDEX	Command index. Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_CMD register and before accessing this register again. Note 2: These bits don't have any effect on the CPSM. They are used to signal the SDIO Interrupt state machine that a Multi Block (CMD18, CMD25, CMD53, etc.) data transaction is taking place. The DAT_CMD bit signals the start of the data transaction while the MCIABORT bit signals the end. For a pure SD Memory card, these bits are a 'don't care' and should be set to zero by convention. However, some software drivers may chose to manipulate the bits in order to maintain compatibility with Combo cards and/or pure SDIO cards. Note 3: This bit is designed to be used with SD CMD18 (READ_MULTIPLE_BLOCK) and SD CMD25 (WRITE_MULTIPLE_BLOCK) which must be terminated with a SD CMD12 (STOP_TRANSMISSION). After CMD18 or CMD25 is sent, the DPSM is enabled to send or receive data of amount MCI_DATA_LENGTH. After the DPSM finishes the transferring the data, it sends 'CmdPend' to the CPSM and goes idle. When the CPSM receives this signal, it sends the currently loaded command which software would normally establish as CMD12. Note 4: The START, CMD_INDEX, ARGUMENT, and CRC are a total of 48 bits in length. If the INTERRUPT bit is zero, the CPSM will wait (63-47) 16 MCLK ticks for a response before going back to IDLE. If the INTERRUP bit is set, the CPSM will wait indefinitely for a card response.

0x12400010 SDC1_MCI_RESP_CMD

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIRespCmd)

SDC1_MCI_RESP_CMD

Bits	Name	Description
31:6	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
5:0	RESPCMD	Response command index.

0x12400014+4*n SDC1_MCI_RESPn, n=[0..3]

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIResponse0-3). Note that MCIResponse3 has 31 bits; the other three (*RESP0, *RESP1, *RESP2) have 32 bits.

The card status size can be 32 or 127 bits, depending on the response type (see Table 1-2). The most significant bit of the card status is received first. The MCIResponse3 register LSB is always 0.

Table 20-8MCIResponse and card status size

Description	Short response	Long response
MCIResponse0	Card Status [31:0]	Card status [127:96]
MCIResponse1	Unused	Card status [95:64]
MCIResponse2	Unused	Card status [63:32]
MCIResponse3	Unused	Card status [31:1]

SDC1_MCI_RESPn

Bits	Name	Description
31:0	STATUS	Card status.

0x12400024 SDC1_MCI_DATA_TIMER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIDataTimer).

There is no way to disable this timer. The timer starts counting as soon as a transaction is initiated. The time counts in MCLK ticks.

SDC1_MCI_DATA_TIMER

Bits	Name	Description
31:0	DATA_TIME	Data timeout period.

0x12400028 SDC1_MCI_DATA_LENGTH

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIDataLength)

Total number of bytes in the transaction regardless of mode (stream or block). In block mode, must be an exact multiple of block size. During an infinite transfer the value of DATALENGTH should be programmed to 0.

SDC1_MCI_DATA_LENGTH

Bits	Name	Description
31:25	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
24:0	DATALENGTH	Data length value.

0x1240002C SDC1_MCI_DATA_CTL

Type: Read/Write
Clock: SAME_RATE_AS_HCLK_SEE_NOTE_1_BELOW_
Reset State: 0x00100000

(ARM name: MCIDataCtrl). Data Path State Machine (DPSM).

SDC1_MCI_DATA_CTL

Bits	Name	Description
31:22	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
21	SW_SDC4_CMD19	The input of cm_dll_sdc4 - sdc4_cmd19 can be driven by SW if AUTO_CMD19 (bit 16 in MCI_CMD) feature is not used. Value 1 - sdc4_cmd19 is driven by SW Value 0 (default) - sdc4_cmd19 is driven by HW
20	RX_DATA_PEND	If set (1), timeout counter will start counting only after the RX command (with data) was sent instead of counting from initialization of DPSM. The feature is enabled by default.

SDC1_MCI_DATA_CTL (cont.)

Bits	Name	Description
19	AUTO_PROG_DONE	If set (1), automatic detection of PROG_DONE condition is executed without sending CMD12, CMD13, CMD52 or any other 'dummy' command. SW should set this bit in the following cases only: 1. When sending CMD53 for SDIO write transaction. 2. When sending CMD24. 3. When sending CMD25 and CMD23 was issued before to inform card about the exact number of blocks to be written. 4. When sending CMD19 for testing bus procedure. CMD12 is not required in this case.
18	INFINITE_TRANSFER	If set (1), infinite transfer is enabled. MCI_DATA_LENGTH register should set to 0 during infinite transfer.
17	DATA_PEND	If set (1), DPSM waits for 'DataPend' from the CPSM before it enables the DPSM. See note 2 below.
16:4	BLOCKSIZE	Data block length in bytes (1 to 4096).
3	DM_ENABLE	Enable DM interface: 0: DM disabled 1: DM enabled
2	MODE	Data transfer mode: 0: block data transfer 1: stream data transfer
1	DIRECTION	Data transfer direction: 0: controller to card 1: card to controller
0	ENABLE	Data transfer enabled. If zero, DPSM unconditionally reset. Note:1 - This register must be updated to the MCLK domain so subsequent writes to this register will be ignored until 3 MCLK and 3 HCLK have passed. SW should wait until bit 0 (MCLK_REG_WR_ACTIVE) of MCI_STATUS2 register is 0, after writing to MCI_DATA_CTL register and before accessing this register again. Note 2: This bit is designed to be used with SD CMD24 and CMD25 (WRITE_SINGLE_BLOCK and WRITE_MULTIPLE_BLOCK) to automatically start the DPSM after a normal (non-error) response is received. This register should be written with the enable bit and the pending bit asserted before MCI_CMD is enabled.

0x12400030 SDC1_MCI_DATA_COUNT

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIDataCnt)

NOTE There is no mechanism to ensure that a read of this counter will be accurate as it is not synchronized. The reason being the value read is async to the clock domain in which the reading is done. It is only useful as a debug tool for diagnostic purposes only.

SDC1_MCI_DATA_COUNT

Bits	Name	Description
31:25	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
24:0	DATACOUNT	Value of data counter in MciDPSM block. Represents remaining data of transaction.

0x12400034 SDC1_MCI_STATUS

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x000C0000

(ARM name: MCIStatus)

This register may need exclusion for QCSR POR Test for bits 25 and 22.

Static[30:26], [24:23] and [10:0]

These remain asserted until they are cleared by writing to the appropriate bit in the Clear Register (see MCI_CLEAR)

XCIS

The means used to send the SDIO external-card-interrupt-signal (XCIS) to the SDCC depends on the transfer mode: 1-bit, 4-bit, or 8-bit. Under 1 bit transfer mode, the XCIS has a dedicated physical connection to the SDCC. Hence once it is asserted, it remain at a high level. Under 4 and 8 bit transfer modes, the XCIS is time multiplexed with physical connection data bit 1. The XCIS is recognized as valid during specific time slots on data bit 1 by the SDCC. How this 'recognition' takes places shows up as different behaviors on SDIO_INTR_OPER, SDIO_INTR, and the actual interrupt sent to the ARM through MCI_INT_MASKn.

Special[25]

The SDIO_INTR_OPER indicator reflects the true state of XCIS as it would be observed inside the external SDIO card. As such, there is no bit 25 in MCI_CLEAR. The only way to clear SDIO_INTR_OPER is to clear the appropriate bit in the external card Common Card Control Registers (CCCR). Like 'static' above and 'dynamic' below, bit 25 in MCI_INT_MASKn controls actually sending this indicator value to the ARM. This indicator of XCIS is used for normal SDCC operation.

Special[22]

The SDIO_INTR indicator reflects that there has been a low-to-high transition on the connection as explained under XCIS above. This indicator is cleared via bit 22 of MCI_CLEAR but any low-to-high transition on the connection will set this indicator again. Further note that this indicator is not routed through the MCI_INT_MASKn to the ARM. For bit 22, the raw value of the connection is routed through the MCI_INT_MASKn to the ARM. As this raw connection is not aware of 'specific time slots', the signal sent to the ARM generally toggles in an unpredictable fashion. This

is generally not useful during normal SDCC operation. However, for wake-up with clocks off, the raw connection is desirable.

Dynamic[21:11]

These change state depending on the state of the underlying logic (for example, FIFO full and empty flags are asserted and de-asserted as data while written to the FIFO).

SDC1_MCI_STATUS

Bits	Name	Description
31	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
30	AUTO_CMD19_TIMEOUT	Response or tuning pattern wasn't received after automatic CMD19's transmission. This status bit should be read only if AUTO_CMD19 (MCI_CMD(16)) was set.
29	BOOT_TIMEOUT	Data wasn't received within the valid time (according to MCI_CCS_TIMER) from the start of boot operation.
28	BOOT_ACK_ERR	Acknowledge pattern wasn't received correctly or not within the valid time (according to MCI_ACK_TIMER) from the start of boot operation.
27	BOOT_ACK_REC	Acknowledge pattern was received correctly.
26	CCS_TIMEOUT	CE-ATA Command Completion Signal timeout.
25	SDIO_INTR_OPER	SDIO interrupt indicator for normal operation.
24	ATA_CMD_COMPL	CE-ATA Command Completion Signal has been detected.
23	PROG_DONE	Programming done.
22	SDIO_INTR	SDIO interrupt indicator for wake-up.
21	RXDATA_AVLBL	Data available in receive FIFO. At least 1 word in the RX FIFO. SW can read 1 word only from the FIFO.
20	TXDATA_AVLBL	Data available in transmit FIFO. At least 1 word in the TX FIFO.
19	RXFIFO_EMPTY	Receive FIFO empty. SW can't read FIFO.
18	TXFIFO_EMPTY	Transmit FIFO empty. SW can write 8 words into the FIFO.
17	RXFIFO_FULL	Receive FIFO full. SW can read 8 words from the FIFO.
16	TXFIFO_FULL	Transmit FIFO full. TX FIFO contains 8 words. SW can't write to FIFO.
15	RXFIFO_HALF_FULL	Receive FIFO half full. SW can read 8 words from the FIFO.
14	TXFIFO_HALF_FULL	Transmit FIFO half full. SW can write 8 words into the FIFO.
13	RXACTIVE	Data receive in progress.
12	TXACTIVE	Data transmit in progress.
11	CMD_ACTIVE	Command transfer in progress.
10	DATA_BLK_END	Data block sent / received (CRC check passed).

SDC1_MCI_STATUS (cont.)

Bits	Name	Description
9	START_BIT_ERR	Start Bit Error flag
8	DATAEND	Data end (data counter is zero).
7	CMD_SENT	Command sent (no response required).
6	CMD_RESPONSE_END	Command response received (CRC check passed).
5	RX_OVERRUN	Receive FIFO overrun error.
4	TX_UNDERRUN	Transmit FIFO underrun error.
3	DATA_TIMEOUT	Data timeout.
2	CMD_TIMEOUT	Command response timeout.
1	DATA_CRC_FAIL	Data block sent / received (CRC check failed).
0	CMD_CRC_FAIL	Command response received (CRC check failed).

0x12400038 SDC1_MCI_CLEAR

Type: Write
Clock: SAME_RATE_AS_HCLK

(ARM name: MCIClear)

SDC1_MCI_CLEAR

Bits	Name	Description
31	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
30	AUTO_CMD19_TIMEOUT_CLR	Clears AUTO_CMD19_TIMEOUT flag.
29	BOOT_TIMEOUT_CLR	Clears BOOT_TIMEOUT flag.
28	BOOT_ACK_ERR_CLR	Clears BOOT_ACK_ERR flag.
27	BOOT_ACK_REC_CLR	Clears BOOT_ACK_REC flag.
26	CCS_TIMEOUT_CLR	Clears CCSTimeOut flag.
24	ATA_CMD_COMPL_CLR	Clears AtaCmdCompl flag.
23	PROG_DONE_CLR	Clears ProgDone flag.
22	SDIO_INTR_CLR	Clears SDIOInt flag.
10	DATA_BLK_END_CLR	Clears DataBlockEnd flag.
9	START_BIT_ERR_CLR	Clears StartBitErr flag.
8	DATA_END_CLR	Clears DataEnd flag.
7	CMD_SENT_CLR	Clears commandSent flag.

SDC1_MCI_CLEAR (cont.)

Bits	Name	Description
6	CMD_RESP_END_CLT	Clears CmdRespEnd flag.
5	RX_OVERRUN_CLR	Clears RxOverrunClr flag.
4	TX_UNDERRUN_CLR	Clears TxUnderrun flag.
3	DATA_TIMEOUT_CLR	Clears DataTimeOut flag.
2	CMD_TIMOUT_CLR	Clears CmdTimOutflag.
1	DATA_CRC_FAIL_CLR	Clears DataCrcFail flag.
0	CMD_CRC_FAIL_CLR	Clears CmdCrcFail flag.

0x1240003C+4*n SDC1_MCI_INT_MASKn, n=[0..1]

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

(ARM name: MCIMask0, MCIMask1)

SDC1_MCI_INT_MASKn

Bits	Name	Description
31	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
30	MASK30	MASK AUTO_CMD19_TIMEOUT flag.
29	MASK29	MASK BOOT_TIMEOUT flag.
28	MASK28	MASK BOOT_ACK_ERR flag.
27	MASK27	MASK BOOT_ACK_REC flag.
26	MASK26	MASK CCSTimeOut flag.
25	MASK25	MASK SDIOIntOper flag.
24	MASK24	MASK AtaCmdCompl flag.
23	MASK23	MASK ProgDone flag.
22	MASK22	MASK SDIOInt flag.
21	MASK21	MASK RxDataAvlbl flag.
20	MASK20	MASK TxDataAvlbl flag.
19	MASK19	MASK RxFifoEmpty flag.
18	MASK18	MASK TxFifoEmpty flag.
17	MASK17	MASK RxFifoFull flag.
16	MASK16	MASK TxFifoFull flag.

SDC1_MCI_INT_MASKn (cont.)

Bits	Name	Description
15	MASK15	MASK RxFifoHalfFull flag.
14	MASK14	MASK TxFifoHalfFull flag.
13	MASK13	MASK RxActive flag.
12	MASK12	MASK TxActive flag.
11	MASK11	MASK CmdActive flag.
10	MASK10	MASK DataBlockEnd flag.
9	MASK9	MASK StartBitErr
8	MASK8	MASK DataEnd flag.
7	MASK7	MASK CmdSent flag.
6	MASK6	MASK CmdRespEnd flag.
5	MASK5	MASK RxOverrun flag.
4	MASK4	MASK TxOverrun flag.
3	MASK3	MASK DataTimeOut flag.
2	MASK2	MASK CmdTimeOut flag.
1	MASK1	MASK DataCmdCrcFail flag.
0	MASK0	MASK CmdCrcFail flag.

0x12400044 SDC1_MCI_FIFO_COUNT

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

The SDCC core operates in two clock domains ’ MCLK and HCLK. The CPSM and DPSM operate in MCLK domain and MciFifoDmaCtl (FIFO/DMA Controller) operates in HCLK domain. The MCI_FIFO_COUNT is a counter of FIFO Controller that monitors how many words of data are still needed to be transferred through the FIFO. At the beginning of data transaction the MCI_FIFO_COUNT counter will be loaded with the (MCI_DATA_LENGTH / 4) value and then will count down during the data transaction until it reach zero. This register is only useful for debug purposes and should not be used for normal operation since it does not reflect data which may or may not be in the pipeline.

SDC1_MCI_FIFO_COUNT

Bits	Name	Description
31:24	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
23:0	DATA_COUNT	Remaining data.

0x12400048 SDC1_MCI_BOOT

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

Handling the boot operation.

SDC1_MCI_BOOT

Bits	Name	Description
31:3	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
2	BOOT_ACK_EN	If set to '1' then Host waits for acknowledge pattern after initiating the boot operation.
1	BOOT_EN	When this bit is asserted, the boot operation is initiated in both of the modes.
0	BOOT_MODE	If set to '1' then CMD line is low during the boot operation. If boot_mode = '0', then CMD0 with the argument 0xFFFFFFFA is sent.

0x1240004C SDC1_MCI_BOOT_ACK_TIMER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

Timer for boot operation - the time until receiving the acknowledge pattern.

SDC1_MCI_BOOT_ACK_TIMER

Bits	Name	Description
31:0	BOOT_ACK_TIMER	Timer for counting the cycles from initiating the boot operation until the acknowledge pattern is accepted.

0x12400050 SDC1_MCI_VERSION

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: see below

This register should be excluded for QCSR POR testing.

SDC1_MCI_VERSION

Bits	Name	Description
31:0	MCI_VERSION	SDCC4 core version. This value corresponds to Z according to core release tag: sdcc4_pXqYrZ.

0x12400054 SDC1_MCI_EMULATION_DLY_LINE

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

The register is responsible for handling DCM which is used in emulation supports 256 values of shift intervals so 8 bits are required (0:255). Bits [31:30] are used for emulation purposes only.

The procedure for activating the DCM is:

1. Setting bit 28 - DCM_RESET.
2. Clearing bit 28 - DCM_RESET.
3. Waiting until bit 29 DCM_LOCKED is high.
4. Writing a new phase in SD_CLK_DLY_CTRL field and setting the DCM_START bit (bit 30).

The clock's placement was executed by the DCM when DCM_DONE is asserted.

SDC1_MCI_EMULATION_DLY_LINE

Bits	Name	Description
31	DCM_DONE	The shift process was finished in DCM and CMD19 can be sent towards the card. This is a read-only bit.
30	DCM_START	A new value of SD_CLK_DLY_CTRL is ready. Clears the DCM_DONE bit.
29	DCM_LOCKED	Reading the status of the LOCKED DCM's output which indicates that the output clock is ready for use.
28	DCM_RESET	Driving reset to DCM.
27:8	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
7:0	SD_CLK_DLY_CTRL	Input to DCM block in FPGA (8 bits). Controlling the change of the delay interval. The value's range may be 0-255 in DCM block.

0x12400058 SDC1_MCI_CCS_TIMER

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

This register is used for operation with CE-ATA devices. The CCS timer starts to count at the end of SD transaction and it advances with every MCLK clock cycle. In boot operation this register is used for storing the number of cycles from initiating the boot operation until the first data is received.

SDC1_MCI_CCS_TIMER

Bits	Name	Description
31:0	CCS_TIMER	CE-ATA Command Completion Signal timeout period.

0x1240005C SDC1_MCI_RESPONSE_MASK

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC1_MCI_RESPONSE_MASK

Bits	Name	Description
31:0	RESPONSE_MASK	Mask used to verify the 32 status error bits. Active only when the data pending bit is set in the MCI_DATA_CTL register. When bit of this mask is set the corresponding bit from response [39:8] is checked to be 0, i.e., shows there is no error. If all bits from mask shows no error, the DPSM will be activated without waiting for software write.

0x12400060 SDC1_MCI_DLL_CONFIG

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x60006400

SDC1_MCI_DLL_CONFIG

Bits	Name	Description
31	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
30	DLL_RST	Setting this bit to 1 resets cm_dll_sdc4. cm_dll_sdc4 should be reset every time the MCLK frequency is changed.

SDC1_MCI_DLL_CONFIG (cont.)

Bits	Name	Description
29	PDN	Power Down Value 0 - analog blocks are enabled Value 1 - analog blocks are powered down (default)
28	CK_INTP_SEL	Selects interpolator output
27	CK_INTP_EN	Enable clock interpolation for finer resolution
26:24	MCLK_FREQ	Frequency of MCLK Value 000 -100 ’ 112 (MHz) Value 001 -112 ’ 125 Value 010 -125 ’ 137 Value 011 -137 ’ 150 Value 100 -150 ’ 162 Value 101 -162 ’ 175 Value 110 -175 ’ 187 Value 111 -187 ’ 200
23:20	CDR_SELEXT	CDR phase select (gray coded) Value 0000 - phase 0 Value 0001 - phase 1 Value 0011 - phase 2 Value 0010 - phase 3 Value 0110 - phase 4 Value 0111 - phase 5 Value 0101 - phase 6 Value 0100 - phase 7 Value 1000 - phase 8 Value 1001 - phase 9 Value 1011 - phase 10 Value 1010 - phase 11 Value 1110 - phase 12 Value 1111 - phase 13 Value 1101 - phase 14 Value 1100 - phase 15
19	CDR_EXT_EN	Enable external control of cdr phase select
18	CK_OUT_EN	Enable output clock (default value is ’1’)
17	CDR_EN	Enable CDR function
16	DLL_EN	Enable DLL function
15:14	CDR_UPD_RATE	CDR update rate, low pass filtering window of CDR Max update rate: Value 00 - 0.5 MCLK frequency Value 01 - 0.25 MCLK Frequency (default) Value 10 - 0.125 MCLK frequency Value 11 - 1/16 MCLK Frequency

SDC1_MCI_DLL_CONFIG (cont.)

Bits	Name	Description
13:12	DLL_UPD_RATE	DLL update rate Value 00 - sdc4_mclk/10 Value 01 - sdc4_mclk/20 Value 10 - sdc4_mclk/40 (default) Value 11 - sdc4_mclk/80
11:10	DLL_PHASE_DET	DLL phase detector low pass average window Value 00 - 4 cycles Value 01 - 8 cycles (default) Value 10 - 16 cycles Value 11 - 32 cycles
9:8	CDR_ALGORITHM_SEL	CDR algorithm select Value 00 - Edge 1 (default) Value 01 - Edge 2 Value 10 - level Value 11- Constant delay
7:6	CMUX0_SHIFT_PHASE	Clock mux0 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable
5:4	CMUX1_SHIFT_PHASE	Clock mux1 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable
3:2	CMUX2_SHIFT_PHASE	Clock mux2 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable
1:0	CMUX3_SHIFT_PHASE	Clock mux3 shift phase shift control Value 00 - Nominal (default) Value 01 - +1 Value 10 - -1 Value 11 - disable

0x12400064 SDC1_MCI_DLL_TEST_CTL

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC1_MCI_DLL_TEST_CTL

Bits	Name	Description
31:26	VTH_CTRL	Vth control: change current in delay cell. Higher number means less delay.
25:22	DELTA_VGS_CTRL	dVgs control: change current in delay cell. Higher number means less delay.
21	DLL_BIAS_EXT_EN	Enable dll bias external control Value 0 - disable external control (default) Value 1 - enable external control
20:19	CDR_TEST_CTRL	External input to increment or decrement CDR output phase by 1 step Phase is changed on rising edge of signal. Ex. To increment phase by 2 steps: 10 -> 00 -> 10 Value 00 - hold (default) Value 01 - decrement Value 10 - increment Value 11 - invalid
18	EXT_UP_DN	external control up/dn signal Value 0 - disable (default) Value 1 - enable
17	ATEST_CTRL	atest control Value 0 - disable (default) Value 1 - enable
16:14	ATEST_OUT_MUX_CTRL	Atest output mux control Value 000 - Avss (default) Value 001 - Vth current Value 010 - delta Vgs current Value 011 - Vthn Value 100- Pbias Value 101 - Nbias Value 110 - reserved Value 111 - External bias current
13	DTEST_CTRL	dtest control Value 0 - disable (default) Value 1 - enable

SDC1_MCI_DLL_TEST_CTL (cont.)

Bits	Name	Description
12:10	DTEST_OUT_MUX_CTRL	dtest output mux control. Output signals are paired for measurements Value 000 - sdc4_mclk, sdc4_mclk (default) Value 001 - da_ phout<0>, da_phout<7> Value 010 - da_ phout<3>, da_phout<4> Value 011 - da_phout<0>, da_phout<15> Value 100 - sd4_clk_out, sd4_data_out<0> Value 101 - sd4_clk_out, sd4_data_out<1> Value 110 - sd4_clk_out, sd4_data_out<2> Value 111 - sd4_clk_out, sd4_data_out<3>
9	DLL_TAP_CTRL	Delay line tap control - change number of unit delay cell in each tap Delay value Value 0 - 1 (default) Value 1 - 2
8:7	DLL_CUR_CTRL	Delay line current control - change current mirror ratio in each delay tap Delay value Value 00 - 1x (default) Value 01 - 2x Value 10 - 3x Value 11 - 4x
6	INT_REF_CLK	Value 0 (default) - use internal generated clock for delay line reference Value 1 - use sdc4_mclk for delay line reference
5	FEEDBACK_CLK_EN	Value 0 (default) - enable delay line feedback Value 1 - disable delay line feedback
4:0	RESERVED	These reserved bits can be accessed by the SW and connected to cm_dll_sdc4's input

0x12400068 SDC1_MCI_DLL_STATUS

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC1_MCI_DLL_STATUS

Bits	Name	Description
31:8	RESERVED_1	Always reads zero. Writes 'don't care' but by convention write zero.
7	DLL_LOCK	DLL lock status Value 0 - Not locked Value 1 - Locked

SDC1_MCI_DLL_STATUS (cont.)

Bits	Name	Description
6:3	CDR_PHASE	CDR phase select (gray coded) Value 0000 - phase 0 Value 0001 - phase 1 Value 0011 - phase 2 Value 0010 - phase 3 Value 0110 - phase 4 Value 0111 - phase 5 Value 0101 - phase 6 Value 0100 - phase 7 Value 1000 - phase 8 Value 1001 - phase 9 Value 1011 - phase 10 Value 1010 - phase 11 Value 1110 - phase 12 Value 1111 - phase 13 Value 1101 - phase 14 Value 1100 - phase 15
2	DDLL_COARSE_CAL	Value 1 - done Value 0 - not done
1:0	RESERVED_2	Connected to cm_dll_sdc4's output.

0x1240006C SDC1_MCI_STATUS2

Type: Read
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC1_MCI_STATUS2

Bits	Name	Description
31:1	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
0	MCLK_REG_WR_ACTIVE	Value 0 - No active register write to MCLK domain Value 1 - Active register write to MCLK domain. The bit indicates if a write operation to one of the following registers is in process (synchronization between HCLK and MCLK): MCI_POWER MCI_CLOCK MCI_CMD MCI_DATA_CTL

0x12400070 SDC1_MCI_GENERICS

Type: Read
Clock: SAME_RATE_AS_HCLK

SDC1_MCI_GENERICS

Bits	Name	Description
31:27	RESERVED	Always reads zero. Writes 'don't care' but by convention write zero.
26:23	SD_DATA_WIDTH	Number of DAT lines Value 4 - 4 DAT lines (SD, SDIO) Value 8 - 8 DAT lines (MMC, eMMC)
22:10	RAM_SIZE	Size of RAM size: Optional Values: 512, 1024, 2048 or 4096 bytes.
9	USE_SPS	Value 1 - BAM and DML are used and USB core is connected to SDCC4, Value 0 - BAM and DML are not used.
8:6	NUM_OF_DEV	Number of eSD or eSDIO devices supported on shared SD bus. Can be set from 1 to 4.
5:1	MAX_PIPES	Number of simultaneous parallel pipes supported by the BAM and attached peripheral pair. Can be set from 1 to 31.
0	USE_DLL_SDC4	Enables the instantiation of cm_dll_sdc4. Value 0 - cm_dll_sdc4 isn't integrated with SDCC4 Value 1 - cm_dll_sdc4 is used with SDCC4.

0x12400080 SDC1_MCI_FIFO

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

SDC1_MCI_FIFO

Bits	Name	Description
31:0	DATA	FIFO data. This register is aliased to 16 words, 0x080 - 0xBC. In SDCC3, an access to the FIFO was executed with 16 words so 16 addresses were defined. However, in SDCC4 only 8 words are used in each burst so only 8 addresses from the range should be used. When writing to the external SD_Card, writes to the data path FIFO. When reading from the external SD_Card, reads from the data path FIFO.

0x124000CC SDC1_MCI_TESTBUS_CONFIG

Type: Read/Write
Clock: SAME_RATE_AS_HCLK
Reset State: 0x00000000

NOTE mclk_mux is the selected internal mclk: the original mclk or divided mclk during divided frequency mode.

Table 20-9 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus0(0)	sdcc_crif_wr_en	hclk
test_bus0(1)	sdcc_crif_rd_en	hclk
test_bus0(2)	sdcc_crif_core_select	hclk
test_bus0(6 downto 3)	sdcc_crif_wr_data[3:0]	hclk
test_bus0(10 downto 7)	sdcc_crif_rd_data[3:0]	hclk
test_bus0(14 downto 11)	sdcc_crif_addr[5:2]	hclk
test_bus0(15)	sdcc_crif_ready	hclk
test_bus0(16)	adm_crci4_ack	-
test_bus0(17)	adm_crci4_req	hclk
test_bus0(18)	rx_fifo_rd_en	hclk
test_bus0(19)	tx_fifo_wr_en	hclk
test_bus0(20)	dm_cnt_rst	hclk
test_bus0(28 downto 21)	ram_addr	mclk_mux
test_bus0(29)	ram_we_n	mclk_mux
test_bus0(30)	ram_cs_n	mclk_mux
test_bus0(31)	rx_fifo_wr_en	mclk_mux
test_bus1(0)	sdcc_crif_wr_en	hclk
test_bus1(1)	sdcc_crif_rd_en	hclk
test_bus1(2)	sdcc_crif_core_select	hclk
test_bus1(6 downto 3)	sdcc_crif_addr[5:2]	hclk
test_bus1(7)	sdcc_crif_ready	hclk
test_bus1(8)	adm_crci4_ack	-
test_bus1(9)	adm_crci4_req	hclk
test_bus1(10)	rx_fifo_rd_en	hclk
test_bus1(11)	tx_fifo_wr_en	hclk
test_bus1(15 downto 12)	req_rw	hclk
test_bus1(16)	DATEnUpdPulse	hclk
test_bus1(17)	LastRxRdDone	hclk
test_bus1(25 downto 18)	ram_addr	mclk_mux

Table 20-9 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus1(26)	ram_we_n	mclk_mux
test_bus1(27)	ram_cs_n	mclk_mux
test_bus1(28)	rx_fifo_wr_en	mclk_mux
test_bus1(29)	ram_reset	mclk_mux
test_bus1(31 downto 30)	pipeline_fill	mclk_mux
test_bus2(2 downto 0)	CPSMState	mclk_mux
test_bus2(3)	CPSMEn	mclk_mux
test_bus2(4)	nIntCMDEN	mclk_mux
test_bus2(5)	iCMDCnt47	mclk_mux
test_bus2(6)	iCRspE	mclk_mux
test_bus2(7)	start_bit_first(CPSM)	mclk_mux
test_bus2(8)	DivLevelCo	mclk_mux
test_bus2(11 downto 9)	DPSMState	mclk_mux
test_bus2(12)	DPSMEn	mclk_mux
test_bus2(13)	inDAT0EN_sel	mclk_mux
test_bus2(14)	inDATEN_sel	mclk_mux
test_bus2(15)	StartBit	mclk_mux
test_bus2(16)	iDEndSet	mclk_mux
test_bus2(17)	iStopBit	mclk_mux
test_bus2(18)	TxFlowCtrlChk	mclk_mux
test_bus2(19)	iTxFlowControl	mclk_mux
test_bus2(27 downto 20)	ram_addr	mclk_mux
test_bus2(28)	ram_we_n	mclk_mux
test_bus2(29)	ram_cs_n	mclk_mux
test_bus2(30)	LastRxRdDoneL	mclk_mux
test_bus2(31)	start_bit_first(DPSM)	mclk_mux
test_bus3(7 downto 0)	DATIN[7:0]	mclk_mux
test_bus3(8)	Valid	mclk_mux
test_bus3(10 downto 9)	VSMState	mclk_mux
test_bus3(11)	CmdStopBit	mclk_mux
test_bus3(13 downto 12)	StopBitDelCnt	mclk_mux
test_bus3(15 downto 14)	CRspESetDelCnt	mclk_mux
test_bus3(16)	mclkenable	mclk_mux
test_bus3(18 downto 17)	isdcc_irq	-
test_bus3(21 downto 19)	DPSMState	mclk_mux
test_bus3(22)	DPSMEn	mclk_mux
test_bus3(23)	inDAT0EN_sel	mclk_mux
test_bus3(24)	inDATEN_sel	mclk_mux

Table 20-9 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus3(25)	StartBit	mclk_mux
test_bus3(26)	iDEndSet	mclk_mux
test_bus3(27)	iStopBit	mclk_mux
test_bus3(28)	TxFlowCtrlChk	mclk_mux
test_bus3(29)	iTxFlowControl	mclk_mux
test_bus3(31)	LastDataWord	mclk_mux
test_bus4(2 downto 0)	CPSMState	mclk_mux
test_bus4(3)	CPSMEn	mclk_mux
test_bus4(4)	nIntCMDEN	mclk_mux
test_bus4(5)	iCRspE	mclk_mux
test_bus4(13 downto 6)	CMDCNT	mclk_mux
test_bus4(14)	start_bit_first(CPSM)	mclk_mux
test_bus4(15)	DivLevelCo	mclk_mux
test_bus4(16)	async_fifo_out_valid	mclk_mux
test_bus4(18 downto 17)	CMDIN	mclk_mux
test_bus4(21 downto 19)	DPSMState	mclk_mux
test_bus4(22)	DPSMEn	mclk_mux
test_bus4(29 downto 23)	BLKTCnt(6 downto 0)	mclk_mux
test_bus4(30)	iCheckProgDone	mclk_mux
test_bus4(31)	iProgDone	mclk_mux
test_bus5(2 downto 0)	DPSMState	mclk_mux
test_bus5(3)	DPSMEn	mclk_mux
test_bus5(4)	inDAT0EN_sel	mclk_mux
test_bus5(5)	inDATEN_sel	mclk_mux
test_bus5(6)	StartBit	mclk_mux
test_bus5(7)	iDEndSet	mclk_mux
test_bus5(8)	iStopBit	mclk_mux
test_bus5(9)	TxFlowCtrlChk	mclk_mux
test_bus5(10)	iTxFlowControl	mclk_mux
test_bus5(11)	LdDataBuffer	mclk_mux
test_bus5(12)	iRxFlowControl	mclk_mux
test_bus5(13)	LastRxRdDone	mclk_mux
test_bus5(14)	inDATEN_high_sel	mclk_mux
test_bus5(15)	inDATEN_low_sel	mclk_mux
test_bus5(16)	async_fifo_out_valid	mclk_mux
test_bus5(17)	LastDataWord	mclk_mux
test_bus5(18)	pipeline_empty	mclk_mux
test_bus5(19)	ShiftNotE	mclk_mux

Table 20-9 TESTBUS signals

TESTBUS bits	Signal	Clock
test_bus5(20)	start_bit_first (DPSM)	mclk_mux
test_bus5(21)	DIVLevelCo	mclk_mux
test_bus5(28 downto 22)	BLKTCnt(6:0)	mclk_mux
test_bus5(29)	iCheckProgDone	mclk_mux
test_bus5(30)	iProgDone	mclk_mux
test_bus5(31)	start_bit_last	mclk_mux
test_bus6(7 downto 0)	ram_addr	mclk_mux
test_bus6(8)	ram_we_n	mclk_mux
test_bus6(9)	ram_cs_n	mclk_mux
test_bus6(11 downto 10)	pipeline_fill	mclk_mux
test_bus6(12)	ram_reset	mclk_mux
test_bus6(13)	rx_fifo_wr_en	mclk_mux
test_bus6(14)	rx_fifo_rd_en	hclk
test_bus6(15)	tx_fifo_wr_en	hclk
test_bus6(19 downto 16)	req_rw	hclk
test_bus6(20)	DATEnUpdPulse	hclk
test_bus6(21)	dm_cnt_rst	hclk
test_bus6(25 downto 22)	rx_fifo_rd_word_cnt	hclk
test_bus6(29 downto 26)	tx_fifo_wr_word_cnt	hclk
test_bus6(30)	iLastRxRdDone	hclk
test_bus6(31)	RxActive	hclk
test_bus7(1 downto 0)	CMDIN	mclk_mux
test_bus7(17 downto 2)	DATIN	mclk_mux
test_bus7(18)	div_freq_cnt_cmd_tx	mclk
test_bus7(19)	div_freq_cnt_dat_tx	mclk
test_bus7(20)	div_freq_cnt_rx	mclk
test_bus7(21)	async_fifo_out_valid	mclk
test_bus7(22)	Rising_DAT0EN_5d	mclk
test_bus7(31 downto 23)	async_fifo_rd_data	mclk

SDC1_MCI_TESTBUS_CONFIG

Bits	Name	Description
31:8	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
7:4	SPARE_FIELD	SW spare bits.
3	TESTBUS_ENA	0x1: Enable 0x0: Disable

SDC1_MCI_TESTBUS_CONFIG (cont.)

Bits	Name	Description
2:0	TESTBUS_SEL	These bits select from different test signals. Refer to Table 1-3 for a list of test signals. TESTBUS_SELBus testbus_sel = 0sdcc_test_bus <= test_bus0 testbus_sel = 1 sdcc_test_bus <= test_bus1 testbus_sel = 2sdcc_test_bus <= test_bus2 testbus_sel = 3sdcc_test_bus <= test_bus3 testbus_sel = 4sdcc_test_bus <= test_bus4 testbus_sel = 5sdcc_test_bus <= test_bus5 testbus_sel = 6sdcc_test_bus <= test_bus6 testbus_sel = 7sdcc_test_bus <= test_bus7

0x124000D0 SDC1_MCI_TEST_CTL

Type: Read/Write
Clock: PCLK
Reset State: 0x00000000

(ARM name: MCITCR)

SDC1_MCI_TEST_CTL

Bits	Name	Description
31:4	RESERVED_1	Always reads zero. Writes ’don’t care’ but by convention write zero.
3	REGTEST	Register Test Bit: Set 0: normal mode (default--accesses to the registers are controlled by the hardware protection circuitry) Set 1: test mode (the hardware protection circuitry is bypassed. Normal Write/Read/Write/ Read tests can be performed independently of the link side.
2:1	RESERVED_2	Always reads zero. Writes ’don’t care’ but by convention write zero.
0	ITEN	Integration Test Enable. This bit places PrimeCell MCI in the following modes: Set 0: normal mode Set 1: Integration test mode

0x124000D4 SDC1_MCI_TEST_INPUT

Type: Read
Clock: PCLK

(ARM name: MCIITIP)

SDC1_MCI_TEST_INPUT

Bits	Name	Description
31:10	RESERVED_1	Always reads zero. Writes ’don’t care’ but by convention write zero.
9:6	MCIDATIN_7_4	Reads return the value on the MCIDATIN[7:4] primary inputs.
5	MCICMDIN	Reads return the value on the MCICMDIN primary input.
4:1	MCIDATIN_3_0	Reads return the value on the MCIDATIN[3:0] primary inputs.
0	RESERVED_2	Always reads zero. Writes ’don’t care’ but by convention write zero.

0x124000D8 SDC1_MCI_TEST_OUT

Type: Read/Write
Clock: PCLK

(ARM name: MCIITOP)

SDC1_MCI_TEST_OUT

Bits	Name	Description
31:16	RESERVED	Always reads zero. Writes ’don’t care’ but by convention write zero.
15:12	MCIDATOUT_7_4	Primary output. Writes specify the value to be driven on the MCIDATOUT[7:4] primary output in the integration test mode. Reads return the value written into this field.
10	MCICMDOUT	Primary output. Writes specify the value to be driven on the MCICMDOUT primary output in the integration test mode. Reads return the value written into this field.
9:6	MCIDATOUT_3_0	Primary output. Writes specify the value to be driven on the MCIDATOUT[3:0] primary output in the integration test mode. Reads return the value written into this field.
1	MCIINTR1	Intra-chip output. Writes specify the value to be driven on the intra-chip MCIINTR1 output in the integration test mode. This bit is write-only.
0	MCIINTR0	Intra-chip output. Writes specify the value to be driven on the intra-chip MCIINTR0 output in the integration test mode. This bit is write-only.

20.26 USB1 HS OTG Registers (0x12500000 USB1_HS_BASE)

This section contains the USB OTG HS registers.

20.26.1 Identification registers

Identification registers are used to declare the slave interface presence and include a table of the hardware configuration parameters.

0x12500000 USB1_HS_USB_OTG_HS_ID

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0042FA05

The USB_OTG_HS_ID register is the identification register. It provides a simple way to determine if the USB-HS USB 2.0 core is provided in the system. The ID register identifies the USB-HS USB 2.0 core and its revision.

USB1_HS_USB_OTG_HS_ID

Bits	Name	Description
31:24	RESERVED_BITS31_24	These bits are reserved and should be set to zero.
23:16	REVISON_7_0	This field contains the revision number of the core - 0x42.
15:8	NID_5_0	This field contains the complement version of ID[7:0] - 0xFA.
7:0	ID_5_0	This field is the configuration number. This number is set to 0x05 and indicates that the peripheral is the USB-HS USB 2.0 core.

0x12500004 USB1_HS_USB_OTG_HS_HWGENERAL

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x5C2

The USB_OTG_HS_HWGENERAL register contains the general hardware parameters.

USB1_HS_USB_OTG_HS_HWGENERAL

Bits	Name	Description
31:10	RESERVED_BITS31_10	Clear (0) these bits.
9	SM	VUSB_HS_PHY_SERIAL = 2
8:6	PHYM	VUSB_HS_PHY_TYPE = 7
5:4	PHYW	VUSB_HS_PHY16_8 = 0

USB1_HS_USB_OTG_HS_HWGENERAL (cont.)

Bits	Name	Description
3	BWT	This bit is reserved for internal testing = 0
2:1	CLCK	VUSB_HS_CLOCK_CONFIGURATION = 1
0	RT	VUSB_HS_RESET_TYPE = 0

0x12500008 USB1_HS_USB_OTG_HS_HWHOST

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x10020001

The USB_OTG_HS_HWHOST register contains the host hardware parameters.

USB1_HS_USB_OTG_HS_HWHOST

Bits	Name	Description
31:24	TTPER	VUSB_HS_TT_PERIODIC_CONTEXTS
23:16	TTASY	VUSB_HS_TT_ASYNC_CONTEXTS
15:4	RESERVED_BITS15_4	Clear (0) these bits.
3:1	NPORT	VUSB_HS_NUM_PORT-1
0	HC	VUSB_HS_HOST

0x1250000C USB1_HS_USB_OTG_HS_HWDEVICE

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000021

The USB_OTG_HS_HWDEVICE register contains the device hardware parameters.

USB1_HS_USB_OTG_HS_HWDEVICE

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:1	DEVEP	VUSB_HS_DEV_EP
0	DC	Device capable; [VUSB_HS_DEV/=0]

0x12500010 USB1_HS_USB_OTG_HS_HWTXBUF

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x80070B08

The USB_OTG_HS_HWTXBUF register contains the Tx buffer hardware parameters.

USB1_HS_USB_OTG_HS_HWTXBUF

Bits	Name	Description
31	TXLCR	This bit is fixed to 1'b1 so that the local context register's are included in the design. This means that the DMA context is implemented in FlipFlops.
30:24	RESERVED_BITS30_24	Clear (0) these bits.
23:16	TXCHANADD	VUSB_HS_TX_CHAN_ADD - Defines the number of address lines needed per Endpoint per the TX latency buffer. It's reset value is taken from a GENERIC value passed to the core.
15:8	TXADD	VUSB_HS_TX_ADD - Defines the number of address lines needed per the entire TX latency buffer. It's reset value is taken from a GENERIC value passed to the core.
7:0	TXBURST	VUSB_HS_TX_BURST - Defines the data burst length of the AHB master interface in Quad-words (4-byte increments) of the TX data. It's reset value is taken from a GENERIC value passed to the core. Note that the actual burst length is will depend on the settings of USB_OTG_HS_AHB_MODE and USB_OTG_HS_AHB_BURST registers.

0x12500014 USB1_HS_USB_OTG_HS_HWRXBUF

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000808

The USB_OTG_HS_HWRXBUF register contains the Rx buffer hardware parameters.

USB1_HS_USB_OTG_HS_HWRXBUF

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits).
15:8	RX_ADD	VUSB_HS_RX_ADD - Defines the number of address lines needed per the entire RX latency buffer. It's reset value is taken from a GENERIC value passed to the core.

USB1_HS_USB_OTG_HS_HWRXBUF (cont.)

Bits	Name	Description
7:0	RX_BURST	VUSB_HS_RX_BURST - Defines the data burst length of the AHB master interface in Quad-words (4-byte increments) of the RX data. It's reset value is taken from a GENERIC value passed to the core. Note that the actual burst length is will depend on the settings of USB_OTG_HS_AHB_MODE and USB_OTG_HS_AHB_BURST registers.

0x12500040+ 4*n USB1_HS_USB_OTG_HS_SCRATCH_RAMn, n=[0..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

USB_OTG_HS_SCRATCH_RAMn registers are 16 32bit scratch registers.Required for passing USB software information between different images.

USB1_HS_USB_OTG_HS_SCRATCH_RAMn

Bits	Name	Description
31:0	SCRATCH_REGISTER	32 bit scratch register

20.26.2 Device/host timer registers

The host/device controller drivers can measure time related activities using these timer registers.

NOTE These registers are not part of the standard EHCI controller.

0x12500080 USB1_HS_USB_OTG_HS_GPTIMER0LD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER0LD register is the general purpose timer 0 load register. This register contains the timer duration or load value. See the GPTIMER0CTRL register for a description of the timer functions.

USB1_HS_USB_OTG_HS_GPTIMER0LD

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.

USB1_HS_USB_OTG_HS_GPTIMER0LD (cont.)

Bits	Name	Description
23:0	GPTLD	General purpose timer load value. This field is the value to be loaded into the GPTCNT countdown timer on a reset action. This value in this register represents the time in microseconds minus 1 for the timer duration. Example: for a one millisecond timer, load 1000-1=999 or 0x0003E7. Note: Max value is 0xFFFFFF or 16.777215 seconds

0x12500084 USB1_HS_USB_OTG_HS_GPTIMER0CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER0CTRL register is the general purpose timer 0 control register. This register contains the control for the timer and a data field can be queried to determine the running count value. This timer has a granularity of 1 ms and can be programmed to a little over 16 seconds. There are two modes supported by this timer: the first is a one-shot and the second is a looped count, which is described in the register table below. When the timer counter value transitions to zero, an interrupt can be generated though the use of the timer interrupts in the USBTS and USBINTR registers.

USB1_HS_USB_OTG_HS_GPTIMER0CTRL

Bits	Name	Description
31	GTPRUN	General purpose timer run Read/write value 0 = Timer stop value 1 = Timer run This bit enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.
30	GPTRST	General purpose timer reset Write-only value 0 = No action value 1 = Load counter value Writing a one to this bit will reload the GPTCNT with the value in GPTLD.
29:25	RESERVED_BITS29_25	Clear (0) these bits.

USB1_HS_USB_OTG_HS_GPTIMER0CTRL (cont.)

Bits	Name	Description
24	GPTMODE	General purpose timer mode Read/write value 0 = One shot value 1 = Repeat This bit selects between a single timer countdown and a looped count down. In the one-shot mode, the timer will count down to zero, generate an interrupt, and stop until the counter is reset by the software. In the repeat mode, the timer will count down to zero, generate an interrupt, and automatically reload the counter to begin again.
23:0	GPTCNT	General purpose timer counter Read-only This field is the value of the running timer.

0x12500088 USB1_HS_USB_OTG_HS_GPTIMER1LD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER1LD register is the general purpose timer 1 control register. This register contains the timer duration or load value. See the GPTIMER0LDregister for a description of the timer functions.

USB1_HS_USB_OTG_HS_GPTIMER1LD

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.
23:0	GPTLD	General purpose timer load value. This field is the value to be loaded into the GPTCNT countdown timer on a reset action. This value in this register represents the time in microseconds minus 1 for the timer duration. Example: for a one millisecond timer, load 1000-1=999 or 0x0003E7. Note: Max value is 0xFFFFFF or 16.777215 seconds.

0x1250008C USB1_HS_USB_OTG_HS_GPTIMER1CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER1CTRL register is the general purpose timer 1 control register. See the description of the USB_OTG_HS_GPTIMER0CTRL register for details about this register.

USB1_HS_USB_OTG_HS_GPTIMER1CTRL

Bits	Name	Description
31	GTPRUN	General purpose timer run Read/write value 0 = Timer stop value 1 = Timer run This bit enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.
30	GPTRST	General purpose timer reset Write-only value 0 = No action value 1 = Load counter value Writing a one to this bit will reload the GPTCNT with the value in GPTLD.
29:25	RESERVED_BITS29_25	Clear (0) these bits.
24	GPTMODE	General purpose timer mode Read/write value 0 = One shot value 1 = Repeat This bit selects between a single timer countdown and a looped count down. In the one-shot mode, the timer will count down to zero, generate an interrupt, and stop until the counter is reset by the software. In the repeat mode, the timer will count down to zero, generate an interrupt, and automatically reload the counter to begin again.
23:0	GPTCNT	General purpose timer counter Read-only This field is the value of the running timer.

20.26.3 Wrapper operational registers

0x12500090 USB1_HS_USB_OTG_HS_AHB_BURST

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_AHB_BURST register determines the AHB master mode of the USB HS Core.

NOTE If the USB_OTG_HS_AHB_MODE is configured to be 0x0 (the AHB Transactor is used), this register must be 0x0 as well, otherwise the AHB Master bus behavior is undefined. Use values other than 0x0 only if setting USB_OTG_HS_AHB_MODE to 0x1.

USB1_HS_USB_OTG_HS_AHB_BURST

Bits	Name	Description
31:3	RESERVED_BITS31_3	Should be set to zero.
2:0	AHB_BURST	AMBA AHB BURST. This is a r/w field that selects the following options for the m_hburst signal of the AMBA master interface: In all cases where the unspecified length burst is allowed, singles access may also occur, this is mostly true when the transaction is not 32-bit aligned. Two consecutive single accesses should not happen. When a INCRx burst size is selected and the transfer is not multiple of the INCRx burst, the burst is decomposed in the different ways. With AHBBRST[2] = 1, the smaller bursts will be unspecified length. with AHBBRST[2] = 0, the smaller bursts will be smaller INCRx or singles. For example, lets say that it's required at a given time, to transfer 22 words of information, for the following values of AHBBRST the master sequence will be: This field after reset is set to a default value that can be configured in the file vusb_hs_cfg.vhd. The AHBBRST field is only used if the AMBA-AHB system interface has been selected. It has no effect for cores featuring BVCI interface. In the later case the read will return zeros. When this field is different from zero, the value of the fields TXBURST /RXBURST in register BURSTSIZE 160h, will be ignored by the controller. Internally the BURSTSIZE will be set to the value of the INCRx AMBA burst. Since this has a direct relation with the burst sizes you must be careful with AHB burst selected. Although the TXBURST / RXBURST are bypassed, this register can still be written / read with no effect, while the AHBBRST field is non-zero. 0x0: INCR burst of unspecified length 0x1: INCR4, non-multiple transfers of INCR4 will be decomposed into singles 0x2: INCR8, non-multiple transfers of INCR8, will be decomposed into INCR4 or singles 0x3: INCR16, non-multiple transfers of INCR16, will be decomposed into INCR8, INCR4 or singles 0x4: This value is reserved and should not be used 0x5: INCR4, non-multiple transfers of INCR4 will be decomposed into smaller unspecified length bursts 0x6: INCR8, non-multiple transfers of INCR8 will be decomposed into smaller unspecified length bursts 0x7: INCR16, non-multiple transfers of INCR16 will be decomposed into smaller unspecified length bursts 0x5: INCR4+ INCR4 +INCR4+ INCR4 +INCR4+ INCR unspec. length 0x6: INCR8+INCR8+INCR4+ INCR unspec. length 0x7: INCR16+INCR4+ INCR unspec. length 0x1: INCR4+ INCR4 +INCR4+ INCR4 +INCR4+SINGLE+SINGLE 0x2: INCR8+INCR8+INCR4+SINGLE+SINGLE 0x3: INCR16+INCR4+SINGLE+SINGLE

0x12500094 USB1_HS_USB_OTG_HS_XTOR_STS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_XTOR_STS register is currently a placeholder for future status bits from the AHB2AHB Transactor.

USB1_HS_USB_OTG_HS_XTOR_STS

Bits	Name	Description
31:2	RESERVED_BITS31_2	Not used currently.
1	GRANT_STOLEN	Reports whether the arbiter removed the hgrant signal prior to completing a transaction. This is currently supported in WRITES ONLY. This bit can be cleared by writing a ’1’ to the GRANT_STOLEN_CLEAR bit in the USB_OTG_HS_AHB_MODE register. To enable this bit again, write a ’0’ to he GRANT_STOLEN_CLEAR bit in the USB_OTG_HS_AHB_MODE register.
0	RESERVED_BIT0	Not used currently.

0x12500098 USB1_HS_USB_OTG_HS_AHB_MODE

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1

USB1_HS_USB_OTG_HS_AHB_MODE

Bits	Name	Description
31	ASYNC_BRIDGES_BYPASS	Default is ’0’. When ’0’ the asynchronous bridge on the master AHB interface is used. When ’1’, it is bypassed. The bridge on the slave AHB is always used.
30:5	RESERVED_BITS30_5	Not used currently.
4	INCR_OVERRIDE	Valid only if the Transactor is bypassed: When ’1’, all INCR bursts from the USB Core will be internally transformed into SINGLE transfers. When ’0’, if the USB Core issues an INCR burst, it will propagate to the external master AHB port.

USB1_HS_USB_OTG_HS_AHB_MODE (cont.)

Bits	Name	Description
3:2	HPROT_MODE	When ’00’ the HPROT signal out of the USB Wrapper is ’0001’, and all transactions are non-posted. When ’01’ the HPROT signal out of the USB Wrapper is ’0101’, and all transactions are posted. When ’10’ the HPROT signal out of the USB Wrapper alternates according to the context of the AHB bus access. Control structures are non-posted while data transfer is posted. When ’11’, reserved value, but currently maps to non-posted (same as ’00’).
1	GRANT_STOLEN_CLEAR	Clears the grant stolen field of the USB_OTG_HS_XTOR_STS register. To enable this bit again, write ’0’ after clearing the GRANT_STOLEN (’1’).
0	XTOR_BYPASS	When this bit is set (1), the AHB Transactor is bypassed, and the USB HS Core’s AHB Master interface is directly connected to the AHB system. In this case, the USB_OTG_HS_AHB_BURST register value will determine the bus characteristics. When this bit is reset (0), the AHB Transactor is used to connect the USB HS Core to the AHB system.

0x1250009C USB1_HS_USB_OTG_HS_GEN_CONFIG

Type: Read/write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXX0830

The USB_OTG_HS_GEN_CONFIG register is used to configure various features that have been added to the HS USB Core.

USB1_HS_USB_OTG_HS_GEN_CONFIG

Bits	Name	Description
31:16	USB_OTG_HS_HW_QVERSION	HW revision of the USB OTG HS core. This version changes with every official release of USB_OTG_HS core.
15	SYS_CLK_SW_EN	This bit is applicable only in SPS Device mode. When this bit is set then USB core always voting for USB_SYSTEM_CLK. Default value is 0 - USB core doesn’t request USB_SYSTEM_CLK when in Low Power Mode.
14	TESTMUX_SEL_4	see TESTMUX_SEL_3_0 the first 4 bits of this register.
13	USB_BAM_DISABLE	This bit disables the bam logic inside the USB and makes him work in Legacy mode.
12	DMA_HPROT_CTRL	When this bit is set Link Controller always does non-posted dQH writes.
11	ISO_FIX_EN	This bit enables fix for Isochronous bug in CI core (CR--0000135251).

USB1_HS_USB_OTG_HS_GEN_CONFIG (cont.)

Bits	Name	Description
10	DSC_PE_RST_EN	This bit enables an automatic reset of Device PE State Machine on disconnection event when operating as device. This reset is a HW fix for CR-000940.
9	HOST_SIM_TIMERS_EN_SUSP	When this bit is set (1), the timers used for the USB suspend process short for faster simulation and ATE time. When this bit is clear(0), the timers used for the USB suspend process are according to the USB specification.
8	HOST_SIM_TIMERS_EN_STD	When this bit is set (1), the timers used for the USB reset on the ULPI are short for faster simulation and ATE time. When this bit is clear(0), the timers used for the USB reset on the ULPI are according to the USB specification.
7	PE_RX_BUF_PENDING_EN	This is only valid in Device Mode. Setting this bit will cause to store a Transaction Status Tag in the Pending register instead of RX Buffer if the RX Buffer is full. The Tag will move from Pending register to RX Buffer as soon as it becomes not full.
6	STREAM_RX_BYPASS_ENABLE	This is only valid in Device Mode. If SDIS bit is set (bit 4 of USB_OTG_HS_USBMODE (0x1A8)), i.e., streaming mode is disabled, setting this bit will cause the RX traffic to override the SDIS bit, and to receive in streaming mode. TX will still be in non-streaming mode.
5	ULPI_SERIAL_EN	This bit must be set to enable operation of ULPI Serial FS/LS mode. Default state is ’1’ - ULPI Serial mode is supported.
4	PE_DP_TXFIFO_IDLE_FORCE	This is only valid in Device Mode. Setting this bit to ’1’ forces the dp_tx_fifo_cmd_dev to be equal to PE_DP_TXFIFO_IDLE when Device PE state machine in REPORT_NAK state and the RX Buffer is full. This bit is used to enable fix of CR-001612. Reset value is ’1’.

USB1_HS_USB_OTG_HS_GEN_CONFIG (cont.)

Bits	Name	Description
3:0	TESTMUX_SEL_3_0	With TESTMUX_SEL_4 select one of the following test buses: Value 00001 Key state machines 01101 hsic_test_bus1 01110 hsic_test_bus2 10000 dma_eng_3 dma_dev_sm_2 10001 dma_eng_4 dma_traf others zeros 0x2: dma_eng_0 dma_dev_sm_1 0x3: dma_eng_1 dma_context 0x4: dma_eng_2 dma_mem_arb 0x5: prot_eng_0 0x6: prot_eng_1 0x7: prot_eng_2 0x8: port_ctrl_0 0x9: port_ctrl_1 0xA: tx_buffer 0xB: rx_buffer 0xC: otg

0x125000A0 USB1_HS_USB_OTG_HS_GEN_CONFIG_2

Type: Read/write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0001F60

Register for the chicken bits. The USB_OTG_HS_GEN_CONFIG_2 register is used to configure various features that have been added to the HS USB Core. By default, all chicken bits are off and the fix is applicable.

USB1_HS_USB_OTG_HS_GEN_CONFIG_2

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12	LINESTATE_DIFF_WAKEUP_EN	chicken bit for CR-0000155486.when this bit is set the USB enables the HW fix for Race condition between the attempt to enter LPM and USB bus reset.Default value is 1.
11	ULPI_LPM_PEND_EN	chicken bit for CR-0000153486.when this bit is set the USB enables the HW fix for Function Control and LPM race condition.Default value is 1.
10	RX_FULL_NAK_EN	chicken bit for CR-0000152878.when this bit is set the USB will respond with NAK's for Host Tokens with very slow AHB and when Streaming mode is enabled. Default value is 1.

USB1_HS_USB_OTG_HS_GEN_CONFIG_2 (cont.)

Bits	Name	Description
9	ENDLESS_TD_EN	chicken bit for CR-0000152976. When this bit is set Performance enhancements for 'infinite' Producer pipe (out endpoint with eTD that points to itself) are enabled. Default value is 1.
8	SCRATCH_RAM_EN	chicken bit for CR-0000149922. When this bis is set the use of scratch ram is enabled and the SW can read/write from addresses 0x040 - 0x07c. when this bit is clear SW can no longer access those registers. Default value is 1.
7	SESS_VLD_CTRL_EN	When this bit is set then bit 25 of USBCMD register controls sess_vld signal inside the Link Controller. When this bit is clear then Link Controller receives sess_vld directly from PHY. Default value is 0.
6	CI_T_WTSUSRSTHS_EN	When this bit is 0 then Device Port Control State Machine waits 2.5 us from USB Reset detection until starting driving Chirp K. When this bit is 1 then Device Port Control State Machine waits 1.5 ms from USB Reset detection until starting driving Chirp K. Default value is 1 - legacy behavior.
5	CI_T_UCH_EN	When this bit is 0 then Device Port Control State Machine drives Chirp K for 1 ms. When this bit is 1 then Device Port Control State Machine drives Chirp K for 2ms. Default value is 1 - legacy behavior.
4	DP_RESET	chicken bit for fix CI2687: When the OTG core is acting as a Host, and VBUS is turned off, and the attached Device attempts to perform a Session Request Protocol by using Data-line Pulsing, it will not be recognized by the Host. Also, when doing HNP and becoming a Host, a SE0 is forced in the line causing the OPT TD5.4 test to fail, without the software workaround.
3	ZLP_PRIME	chicken bit for fix CI2655: When using ISO IN endpoints with MULT=3 and low bandwidth system bus access, the controller may enter into a wait loop situation without warning the software. Due to the low bandwidth the last packet from a mult3 sequence may not be fetched in time before the last token IN is received (for that uframe/endpoint). This will cause the controller to reply with a zero length packet (ZLP), breaking the prime sequence.
2	NO_SOF_RX_FIFO_FULL	chicken bit for fix CI2581: During normal operation, if the RX Fifo becomes full and the protocol engine needs to send a command to the DMA state machine, it will wait in that state until the RX Fifo becomes not full. As the protocol state machine also handles the SOF generation, the SOFs will no longer be sent. If one SOF is missed, the Host controller will issue a false babble detection. If more than 3.125ms are elapsed without SOFs the peripheral will recognize the idle bus as a USB reset.
1	WRONG_OPMODE_SUSP	chicken bit for fix CI1274: When the Controller enters a Suspend state it asserts opmode with the wrong value, according to specifications 'UTMI+ Specification, Revision 1.0, Section 3.2' and 'UTMI+ Low Pin Interface Specification, Revision 1.1, Section 3.8.5.3'. This causes no issue in actual usage.

USB1_HS_USB_OTG_HS_GEN_CONFIG_2 (cont.)

Bits	Name	Description
0	RESUME_END_INTER	chicken bit for fix CI1179: Working as host, when doing resume a port change interrupt was fired at the end of resume. According to the EHCI spec no interrupt should be fired.

20.26.4 Device/host capability registers

0x12500100 USB1_HS_USB_OTG_HS_CAPLENGTH

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x01000040

The USB_OTG_HS_CAPLENGTH register is the capability register length. It is used to indicate which offset to add to the register base address at the beginning of the operational register.

USB1_HS_USB_OTG_HS_CAPLENGTH

Bits	Name	Description
31:16	HCIVERSION_15_0	BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.
7:0	CAPLENGTH_7_0	Offset at beginning of operational register

0x12500104 USB1_HS_USB_OTG_HS_HCSPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00010011

The USB_OTG_HS_HCSPARAMS register contains the host control structural parameters. The port steering logic capabilities are described in this register.

USB1_HS_USB_OTG_HS_HCSPARAMS

Bits	Name	Description
31:28	RESERVED_BITS31_28	Clear (0) these bits.
27:24	N_TT_3_0	Number of transaction translators This field indicates the number of embedded transaction translators associated with the USB2.0 host controller. For a multi-port host, this field will always equal 0001. For all other implementations, N_TT = 0000. This in a non-EHCI field to support embedded TT.

USB1_HS_USB_OTG_HS_HCSPARAMS (cont.)

Bits	Name	Description
23:20	N_PTT_3_0	Number of ports per transaction translator This field indicates the number of ports assigned to each transaction translator within the USB2.0 host controller. For a multi-port host this field will always equal N_PORTS. For all other implementations, N_PTT = 0000. This in a non-EHCI field to support embedded TT.
19:17	RESERVED_BITS19_17	Clear (0) these bits.
16	PI_3_0	Port indicator This bit indicates whether the ports support port indicator control. When set (1), the port status and control registers include a read/writable field for controlling the state of the port indicator. This field will always be set (1).
15:12	N_CC_3_0	Number of companion controllers This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no internal companion controllers. Port-ownership hand-off is not supported. A value larger than zero in this field indicates that there are companion USB1.1 host controller(s). Port-ownership hand-offs are supported. High-, full-, and low-speed devices are supported on the host controller root ports. In this implementation, this field will always be clear (0).
11:8	N_PCC_3_0	Number of ports per companion controller This field indicates the number of ports supported per internal companion controller. It is used to indicate the port routing configuration to the system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2, then N_PCC could have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, and so on. In the previous example, the N_PCC could have been 4, where the first 4 are routed to companion controller 1 and the last two are routed to companion controller 2. The number in this field must be consistent with N_PORTS and N_CC. In this implementation, this field will always be clear (0).
7:5	RESERVED_BITS7_5	Clear (0) these bits.
4	PPC	Port power control This field indicates whether the host controller implementation includes port power control. Set (1) indicates that the ports have port power switches. Clear (0) indicates that the ports do not have port power switches. The value of this field affects the functionality of the port power field in each port status and control register. This bit will always be clear (0) for a device only implementation.

USB1_HS_USB_OTG_HS_HCSPARAMS (cont.)

Bits	Name	Description
3:0	N_PORTS_3_0	Number of downstream ports This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the operational register. Valid values are in the range of 1h to Fh. A zero in this field is undefined. The number of ports for a host implementation is configurable from 1 to 8. This field will always be set (1) for device-only implementation.

0x12500108 USB1_HS_USB_OTG_HS_HCCPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0006

The USB_OTG_HS_HCCPARAMS register contains the host control capability parameters. This register identifies multiple mode control (time-base bit functionality) addressing capability.

USB1_HS_USB_OTG_HS_HCCPARAMS

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.
15:8	EECP_7_0	EHCI extended capabilities pointer Default = 0 This optional field indicates the existence of a capabilities list. A value of 00h indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capability. The pointer value must be 40h or greater if implemented to maintain the consistency of the PCI header defined for this class of device. For this implementation, all of these bits are clear (0).
7:4	IST_7_4	Isochronous scheduling threshold Default = implementation dependent This field indicates, relative to the current position of the executing host controller, where the software can reliably update the isochronous schedule. When bit [7] is clear (0), the value of the least significant 3 bits indicates the number of microframes a host controller can hold a set of isochronous data structures (one or more) before flushing the state. When bit [7] is set (1), then host software assumes the host controller may cache an isochronous data structure for an entire frame. All of the bits in this field will always be clear (0).
3	RESERVED_BIT3	Clear (0) this bit.

USB1_HS_USB_OTG_HS_HCCPARAMS (cont.)

Bits	Name	Description
2	ASP	Asynchronous schedule park capability Default = 1 If this bit is set (1), then the host controller supports the park feature for high-speed queue heads in the asynchronous schedule. The feature can be disabled, or enabled and set to a specific level by using the (ASPE) and (ASP[1:0]) fields in the USB_OTG_HS_USBCMD register. This field will always be set (1).
1	PFL	Programmable frame list flag If this bit is clear (0), then the system software must use a frame list length of 1024 elements with this host controller. The FS[2:0] field in the USBCMD register is read-only and must be cleared (0). If this bit is set (1), then the system software can specify and use a smaller frame list, and configure the host controller using the FS[2:0] field in the USBCMD register. The frame list must always be aligned on a 4k-page boundary. This requirement ensures that the frame list is always physically contiguous. This bit in this field will always be set (1).
0	ADC	64-bit addressing capability This field will always be clear (0). No 64-bit addressing capability is supported.

0x12500120 USB1_HS_USB_OTG_HS_DCIVERSION

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1

The USB_OTG_HS_DCIVERSION register contains the device interface version number. The device controller interface conforms to the two-byte BCD encoding of the interface version number contained in this register.

USB1_HS_USB_OTG_HS_DCIVERSION

Bits	Name	Description
15:0	DCIVERSION_15_0	Device interface version number

0x12500124 USB1_HS_USB_OTG_HS_DCCPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x190

The USB_OTG_HS_DCCPARAMS register contains the device control capability parameters. These fields describe the overall host/device capability of the controller.

USB1_HS_USB_OTG_HS_DCCPARAMS

Bits	Name	Description
31:9	RESERVED_BITS31_9	Clear (0) these bits.
8	HC	Host capable When this bit is set (1), this controller is capable of operating as an EHCI-compatible USB 2.0 host controller.
7	DC	Device capable When this bit is set (1), this controller is capable of operating as a USB 2.0 device.
6:5	RESERVED_BITS6_5	Clear (0) these bits.
4:0	DEN_4_0	Device endpoint number This field indicates the number of endpoints build into the device controller. If this controller is not device capable, then this field will be al zeroes. Valid values for this field are 0 through 16.

20.26.5 Device/host operational registers

0x12500140 USB1_HS_USB_OTG_HS_USBCMD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00080000

The USB_OTG_HS_USBCMD register is the USB command register. The serial bus host/device controller executes the command indicated in this register.

USB1_HS_USB_OTG_HS_USBCMD

Bits	Name	Description
31	RST_CTRL	Default value = 0. Set to 1 to block operational reset to xcvr (ser and ulpi) clock domains.
30	ULPI_STP_CTRL	Default value = 0. Set to 1 to block the ulpi_stp signal from going out to ULPI PHY
29	ASYNC_INTR_CTRL	Default value = 0. Set to 1 to allow the async interrupt out from the HS core.
28	SE0_GLITCH_FIX_CTRL	Default value = 0. Set to 1 to activate the SE0 glitch fix mechanism
27	FS_3_WIRE_2_WIRE_SELECT	Default value = 0. Set this bit for enabling the two wire interface on the fs_dat and fs_se0 pins

USB1_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
26	ULPI_SER3_NOT6_SEL	ULPI serial 3 bits select. Read/write Read: Current status of serial data bus wide Write: SW writes ’1’ to this bit to request 3 pins ULPI data wide, or ’0’ to request 6 bit data wide in FsLsSerial Mode.
25	SESS_VLD_CTRL	Default value = 0. Set this bit to enable Link Controller operation after switching interface from Serial to ULPI.
24	RESERVED_BIT24	Clear (0) these bit
23:16	ITC_7_0	Interrupt threshold control Read/write Default 08h The system software uses this field to set the maximum rate at which the host/device controller will issue interrupts. This field contains the maximum interrupt interval measured in micro-frames. Valid values are shown below. Value Maximum interrupt interval 00h Immediate (no threshold) 01h 1 micro-frame 02h 2 micro-frames 04h 4 micro-frames 08h 8 micro-frames 10h 16 micro-frames 20h 32 micro-frames 40h 64 micro-frames
15	FS2	This field is Read/Write only if Programmable Frame List Flag in the HCCPARAMS registers is set to one. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index. Note that this field is made up from USBCMD bits 15, 3 and 2. Values meaning 000 1024 elements (4096 bytes) Default value 001 512 elements (2048 bytes) 010 256 elements (1024 bytes) 011 128 elements (512 bytes) 100 64 elements (256 bytes) 101 32 elements (128 bytes) 110 16 elements (64 bytes) 111 8 elements (32 bytes) Only the host controller uses this field.

USB1_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
14	ATDTW	Add dTD tripwire Read/write (Device mode only) This bit is used as a semaphore to ensure the to proper addition of a new dTD to an active (primed) endpoint's linked list. This bit is set (1) and cleared (0) by the software. This bit shall also be cleared (0) by the hardware when the state machine is a hazard region for which adding a dTD to a primed endpoint may go unrecognized.
13	SUTW	Setup tripwire (device mode only) Read/write This bit is used as a semaphore to ensure that the setup data payload of 8 bytes is extracted from a QH by the DCD without being corrupted. If the setup lockout mode is off (see USBMODE) then there exists a hazard when new setup data arrives while the DCD is copying the setup data payload from the QH for a previous setup packet. This bit is set (1) and cleared (0) by software, and will be cleared (0) by hardware when a hazard exists.
12	RESERVED_BITS12	Clear (0) this bit
11	ASPE	Asynchronous schedule park mode enable (OPTIONAL) Read/write If the asynchronous park capability (ASP) bit in the HCCPARAMS register is set (1), then this bit defaults to a 1h and is R/W. Otherwise, the bit must be cleared (0) and is RO. The software uses this bit to enable or disable the park mode. value 1 = Park mode is enabled. value 0 = Park mode is disabled. This field is set (1) in this implementation.
10	RESERVED_BIT10	Clear (0) this bit.
9:8	ASP_1_0	Asynchronous schedule park mode count (OPTIONAL) Read/write If the Asynchronous park capability (ASP) bit in the HCCPARAMS register is set (1), then this field defaults to 3h and is R/W. Otherwise it defaults to zero and is RO. This field contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule before continuing traversal of the Asynchronous schedule. See Section 4.10.3.2 for full operational details. Valid values are 1h to 3h. The software must not clear (0) this bit when the ASPE bit in this register is set (1), as this will result in undefined behavior. This field is set to 3h in this implementation.
7	LR	Light host/device controller reset (OPTIONAL) Read only Not implemented. This bit will always be clear (0).

USB1_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
6	IAA	Interrupt on async advance doorbell Read/write This bit is used as a doorbell by the software to tell the host controller to issue an interrupt the next time it advances the asynchronous schedule. The software must set (1) this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule states, it sets (1) the interrupt on the async advance status (AAI) bit in the USBSTS register. If the interrupt on async advance enable (AAE) bit in the USBINTR register is set (1), then the host controller will assert an interrupt at the next interrupt threshold. The host controller clears (0) this bit after it has set (1) the interrupt on async advance status (AAI) bit in the USBSTS register. The software should not set (1) this bit when the asynchronous schedule is inactive. Doing so will yield undefined results. This bit is only used in the host mode. Setting (1) this bit when the device mode is selected will produce undefined results.
5	ASE	Asynchronous Schedule Enable Read/write Default = 0b This bit controls whether the host controller skips processing the asynchronous schedule. value 0 = Do not process the asynchronous schedule value 1 = Use the ASYNCLISTADDR register to access the asynchronous schedule. Only the host controller uses this bit.
4	PSE	Periodic schedule enable Read/write Default 0b This bit controls whether the host controller skips processing the periodic schedule. value 0 = Do not process the periodic schedule value 1 = Use the PERIODICLISTBASE register to access the periodic schedule. Only the host controller uses this bit.

USB1_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
3:2	FS_1_0	This field is Read/Write only if Programmable Frame List Flag in the HCCPARAMS registers is set to one. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index. Note that this field is made up from USBCMD bits 15, 3 and 2. Values meaning 000 1024 elements (4096 bytes) Default value 001 512 elements (2048 bytes) 010 256 elements (1024 bytes) 011 128 elements (512 bytes) 100 64 elements (256 bytes) 101 32 elements (128 bytes) 110 16 elements (64 bytes) 111 8 elements (32 bytes) Only the host controller uses this field.
1	RST	Controller reset (RESET) Read/write The software uses this bit to reset the controller. This bit is cleared (0) by the host/device controller when the reset process is complete. The software cannot terminate the reset process early by clearing (0) this bit. Host controller: When the software sets (1) this bit, the host controller resets its internal pipelines, timers, counters, state machines, and so on to their initial values. Any transaction currently in progress on the USB is immediately terminated. A USB reset is not driven on downstream ports. The software should not set (1) this bit when the HCHalted bit in the USBSTS register is clear (0). Attempting to reset an actively running host controller will result in undefined behavior. Device controller: When the software sets (1) this bit, the device controller resets its internal pipelines, timers, counters, state machines, and so on to their initial values. Setting this bit when the device is in the attached state is not recommended, since the effect on an attached host is undefined. In order to ensure that the device is not in an attached state before initiating a device controller reset, all primed endpoints should be flushed and the USBCMD run/stop bit should be cleared (0).

USB1_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
0	RS	Run/stop Read/Write Default 0b value 1 = Run value 0 = Stop Host controller: When this bit is set (1), the host controller proceeds with the execution of the schedule. The host controller continues execution as long as this bit remains set (1). When this bit is clear (0), the host controller completes the current transaction on the USB and then halts. The HC halted bit in the status register indicates when the host controller has finished the transaction and has entered the stopped state. The software should not set (1) this bit unless the host controller is in the halted state (that is, the HCHalted bit in the USBSTS register is set (1)). Device controller: Setting (1) this bit will cause the device controller to enable a pull-up on D+ and initiate an attach event. This control bit is not directly connected to the pull-up enable, as the pull-up will become disabled upon transitioning into high-speed mode. The software should use this bit to prevent an attach event before the device controller has been properly initialized. Clearing (0) this bit will cause a detach event.

0x12500144 USB1_HS_USB_OTG_HS_USBSTS

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_USBSTS register is the USB status register. This register indicates various states of the host/device controller and any pending interrupts. This register does not indicate status resulting from a transaction on the serial bus. The software clears certain bits in this register by setting (1) them.

USB1_HS_USB_OTG_HS_USBSTS

Bits	Name	Description
31	ULPI_INTR	Default value = 0.This bit is set when Interrupt during ULPI -Serial mode or ULPI Interrupt during LPM occurs. Writing a 1 to this bit will clear it.
30	PHY_SESS_VLD_CHG	This bit is set when PHY_SESS_VLD bit changes its value.
29	PHY_SESS_VLD	This bit presents the SESS_VLD status of PHY.
28	PHY_ALT_INT	This bit is asserted when a non-USB interrupt from PHY is detected. This interrupt is used for procedures like Battery Charging. This bit is set when bit 7 (alt_int) of RX CMD is high. Writing a 1 to this bit will clear it.

USB1_HS_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
27:26	RESERVED_BITS27_26	Clear (0) these bits.
25	TI1	General purpose timer interrupt 1 (GPTINT1) Read/write control This bit is set (1) when the counter in the GPTIMER1CTRL (non-EHCI) register transitions to zero. Setting (1) this bit will clear it.
24	TI0	General purpose timer interrupt 0 (GPTINT0) Read/write control This bit is set (1) when the counter in the GPTIMER0CTRL (non-EHCI) register transitions to zero. Setting (1) this bit will clear it.
23:20	RESERVED_BITS23_20	Clear (0) these bits.
19	UPI	USB host periodic interrupt (USBHSTPERINT) Read/write control This bit is set (1) by the host controller when the cause of an interrupt is a completion of a USB transaction, where the transfer descriptor (TD) has an interrupt on complete (IOC) bit set (1) and the TD was from the periodic schedule. This bit is also set (1) by the host controller when a short packet is detected AND the packet is on the periodic schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes. This bit is not used by the device controller and will always be clear (0).
18	UAI	USB host asynchronous interrupt (USBHSTASYNCINT) Read/write control This bit is set (1) by the host controller when the cause of an interrupt is a completion of a USB transaction, where the transfer descriptor (TD) has an interrupt on complete (IOC) bit set AND the TD was from the asynchronous schedule. This bit is also set (1) by the host when a short packet is detected AND the packet is on the asynchronous schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes. This bit is not used by the device controller and will always be clear (0).
17	RESERVED_BIT17	Clear (0) these bits.
16	NAKI	NAK interrupt bit Read only This bit is set (1) by the hardware when, for a particular endpoint, both the Tx/Rx endpoint NAK bit and the corresponding Tx/Rx endpoint NAK enable bit are set (1). This bit is automatically cleared (0) by the hardware when all of the enabled Tx/Rx endpoint NAK bits are cleared (0).

USB1_HS_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
15	AS	Asynchronous schedule status Read only Default = 0 This bit reports the current real status of the asynchronous schedule. When cleared (0), the asynchronous schedule status is disabled. And, if set (1), the status is enabled. The host controller is not required to immediately disable or enable the asynchronous schedule when software transitions the asynchronous schedule enable bit in the USBCMD register. When this bit and the asynchronous schedule enable bit are the same value, the asynchronous schedule is either enabled (1) or disabled (0). This bit is only used by the host controller.
14	PS	Periodic schedule status Read only Default = 0 This bit reports the current real status of the periodic schedule. When cleared (0), the periodic schedule is disabled. And, if set (1), the status is enabled. The host controller is not required to immediately disable or enable the periodic schedule when software transitions the periodic schedule enable bit in the USBCMD register. When this bit and the periodic schedule enable bit are the same value, the periodic schedule is either enabled (1) or disabled (0). This bit is only used by the host controller.
13	RCL	Reclamation Read only Default = 0 This is a read-only status bit that is used to detect an empty asynchronous schedule. This bit is only used by the host controller.
12	HCH	HC halted Read only Default = 1 This bit is a clear (0) whenever the run/stop bit is set (1). The host controller sets (1) this bit after it has stopped executing, because of the run/stop bit being cleared (0), either by the software or by the host controller hardware (for example, an internal error). This bit is only used by the host controller.
11	RESERVED_BIT11	Clear (0) this bit.
10	ULPII	ULPI interrupt Read/write control Default = 0 When the ULPI viewport is present in the design, an event completion will set (1) this interrupt. This bit is used by both the host and device controllers. It is only present in designs where the configuration constant VUSB_HS_PHY_ULPI = 1.

USB1_HS_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
9	RESERVED_BIT9	Clear (0) this bit.
8	SLI	DC suspend Read/write control Default = 0 When a device controller enters a suspend state from an active state, this bit will be set (1). The device controller clears (0) the bit upon exiting from a suspend state. This bit is only used by the device controller.
7	SRI	SOF received Read/write control Default = 0 When the device controller detects a start of (micro) frame, this bit will be set (1). When a SOF is extremely late, the device controller will automatically set (1) this bit to indicate that an SOF was expected. Therefore, this bit will be set (1) roughly every 1 ms in the device FS mode and every 125 ms in the HS mode, and will be synchronized to the actual SOF that is received. Since the device controller is initialized to FS before connect, this bit will be set (1) at an interval of 1 ms during the prelude to connect and chirp. In the host mode, this bit will be set (1) every 125 us and can be used by the host controller driver as a time base. The software writes a 1 to this bit to clear it. This is a non-EHCI status bit.
6	URI	USB reset received Read/write control Default = 0 When the device controller detects a USB reset and enters the default state, this bit will be set (1). The software can set (1) this bit to clear the USB reset received status bit. This bit is only used by the device controller.
5	AAI	Interrupt on async advance Read/write control Default = 0 The system software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by setting (1) the interrupt on async advance doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source. This bit is only used by the host controller.
4	SEI	System error Read/write control This interrupt is triggered when there is an AHB error (HRESP = ERROR) on the AHB Master interface.

USB1_HS_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
3	FRI	Frame list rollover Read/write control The host controller sets (1) this bit when the frame list index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the frame list size field of the USBCMD register) is 1024, the frame index register rolls over every time FRINDEX [1 3] toggles. Similarly, if the size is 512, the host controller sets (1) this bit to a one every time FHINDEX [12] toggles. This bit is only used by the host controller.
2	PCI	Port change detect Read/write control The host controller sets (1) this bit when a connect status occurs on any port, a port enable/disable change occurs on any port, or the force port resume bit is set (1) as the result of a J-K transition on the suspended port. The device controller sets (1) this bit when the port controller enters the full or high-speed operational state. When the port controller exits the full or high-speed operation states due to reset or suspend events, the notification mechanisms are the USB reset received bit and the DC suspend bits, respectively. This bit is not EHCI compatible.
1	UEI	USB error interrupt (USBERRINT) Read/write control When completion of a USB transaction results in an error condition, this bit is set (1) by the host/device controller. This bit is set (1) along with the USBINT bit, if the TD on which the error interrupt occurred also had its interrupt-on-complete (IOC) bit set (1). The device controller detects resume signaling only.
0	UI	USB interrupt (USBINT) Read/write control This bit is set (1) by the host/device controller when the cause of an interrupt is a completion of a USB transaction where the transfer descriptor (TD) has an interrupt-on-complete (IOC) bit set (1). This bit is also set (1) by the host/device controller when a short packet is detected. A short packet is when the actual number of bytes received was less than the expected number of bytes.

0x12500148

USB1_HS_USB_OTG_HS_USBINTR

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_USBINTR register is the USB interrupt enable register. The interrupts to the software are enabled with this register. An interrupt is generated when a bit is set (1) and the corresponding interrupt is active. The USB status register (USBSTS) still shows interrupt sources, even if they are disabled by the USBINTR register, which allows polling of interrupt events by the software.

USB1_HS_USB_OTG_HS_USBINTR

Bits	Name	Description
31	ULPI_INTR_EN	Default value =0.When this bit is a 1 and ULPI_INTR is a 1, the controller will issue an interrupt. The interrupt is acknowledged by software clearing the ULPI_INTR bit.
30	PHY_SESS_VLD_CHG_EN	Default value =0. When this bit is set then Link Controller will issue an interrupt when PHY_SESS_VLD changes its value.
29:26	RESERVED_BITS29_26	Clear (0) these bits.
25	TIE1	General purpose timer interrupt enable 1 When this bit is set (1), and the GPTINT1 bit in the USBSTS register is set (1), the controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the GPTINT1 bit.
24	TIE0	General purpose timer interrupt enable 0 When this bit is set (1), and the GPTINT0 bit in the USBSTS register is set (1), the controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the GPTINT0 bit.
23:20	RESERVED_BITS23_20	Clear (0) these bits.
19	UPIE	USB host periodic interrupt enable When this bit is set (1), and the USBHSTPERINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBHSTPERINT bit.
18	UAIE	USB host asynchronous interrupt enable When this bit is set (1), and the USBHSTASYNCINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBHSTASYNCINT bit.
17	RESERVED_BIT17	Clear (0) this bit.

USB1_HS_USB_OTG_HS_USBINTR (cont.)

Bits	Name	Description
16	NAKE	NAK interrupt enable This bit is set (1) by the software if it wants to enable the hardware interrupt for the NAK interrupt bit. If both this bit and the corresponding NAK interrupt bit are set (1), a hardware interrupt is generated.
15:11	RESERVED_BITS15_11	Clear (0) these bits.
10	ULPIE	ULPI enable When this bit is set (1), and the ULPI Interrupt bit in the USBSTS register transitions, the controller will issue and interrupt. The interrupt is acknowledged by the software setting (1) the ULPI interrupt bit. This bit is used by both the host and device controllers. It is only present in designs where configuration constant VUSB_HS_PHY_ULPI = 1.
9	RESERVED_BIT9	Clear (0) this bit.
8	SLE	Sleep enable When this bit is set (1) and the DC suspend bit in the USBSTS register transitions, the device controller will issue an interrupt. The interrupt is acknowledged by the software setting (1) the DC suspend bit. This bit is only used by the device controller.
7	SRE	SOF received enable When this bit is set (1) and the SOF received bit in the USBSTS register is set (1), the device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the SOF received bit.
6	URE	USB reset enable When this bit is set (1) and the USB reset received bit in the USBSTS register is set (1), the device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the USB reset received bit.
5	AAE	Interrupt on async advance enable When this bit is set (1) and the interrupt on async advance bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the interrupt on async advance bit. This bit is only used by the host controller.
4	SEE	System error enable When this bit is set (1) and the system error bit in the USBSTS register is set (1), the host/device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the system error bit.

USB1_HS_USB_OTG_HS_USBINTR (cont.)

Bits	Name	Description
3	FRE	Frame list rollover enable When this bit is set (1) and the frame list rollover bit in the USBSTS register is set (1), the host controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the frame list rollover bit. This bit is only used by the host controller.
2	PCE	Port change detect enable When this bit is set (1) and the port change detect bit in the USBSTS register is set (1), the host/device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the port change detect bit.
1	UEE	USB error interrupt enable When this bit is set (1) and the USBERRINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBERRINT bit in the USBSTS register.
0	UE	USB interrupt enable When this bit is set (1) and the USBINT bit in the USBSTS register is set (1), the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBINT bit.

0x1250014C USB1_HS_USB_OTG_HS_FRINDEX

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_FRINDEX register is the USB frame index register. This register is used by the host controller to index the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits [N:3] are used to select a particular entry in the periodic frame list during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by the system software in the frame list size field in the USBCMD register.

This register must be written as a DWord. Byte writes produce-undefined results. This register cannot be written unless the host controller is in the 'halted' state, as indicated by the HC halted bit. A write to this register while the run/stop bit is set (1) produces undefined results. Writes to this register also affect the SOF value.

In the device mode, this register is read-only and the device controller updates the FRINDEX [13:3] register from the frame number indicated by the SOF marker. Whenever a SOF is received by the USB bus, FRINDEX [13:3] will be checked against the SOF marker. If FRINDEX [13:3] is different from the SOF marker, FRINDEX [13:3] will be set to the SOF value and FRINDEX [2:0] will be cleared (0) (that is, SOF for a 1-ms frame). If FRINDEX [13:3] is equal to the SOF value, FRINDEX [2:0] will be incremented (that is, SOF for 125-ms micro-frame.

USB1_HS_USB_OTG_HS_FRINDEX

Bits	Name	Description
31:14	RESERVED_BITS31_14	Clear (0) these bits.
13:0	FRINDEX_13_0	Frame index The value in this register increments at the end of each time frame (for example, a micro-frame). Bits [N:3] are used for the frame list current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. The following data shows the values of N based on the value of the frame list size field in the USBCMD register when used in host mode. USBCMD [Frame list size] number Elements N 000b (1024) 12 001b (512) 11 010b (256) 10 011b (128) 9 100b (64) 8 101b (32) 7 110b (16) 6 111b (8) 5 In the device mode, the value is the current frame number of the last frame transmitted. It is not used as an index. In either mode, bits 2:0 indicate the current microframe.

0x12500154 USB1_HS_USB_OTG_HS_PERIODICLISTBASE

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_PERIODICLISTBASE register is the periodic list base address register. This 32-bit register contains the beginning address of the periodic frame list in the system memory. The HCD loads this register prior to starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the frame index register (FRINDEX) to enable the host controller to step through the periodic frame list in sequence.

NOTE This device is shared between the host controller and device controller operation. For host controller operation, this is the USB_OTG_HS_ PERIODICLISTBASE register. For device controller operation, this is the USB_OTG_HS_DEVICEADDR register.

USB1_HS_USB_OTG_HS_PERIODICLISTBASE

Bits	Name	Description
31:12	PERBASE_31_12	Base address (low) These bits correspond to memory address signals [31:12], respectively. Only used by the host controller.
11:0	RESERVED_BITS11_0	This field must be written as zeros. During runtime, the values of these bits are undefined.

0x12500154 USB1_HS_USB_OTG_HS_DEVICEADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_DEVICEADDR register is the USB device address register. The upper seven bits of this register represent the device address. After any controller reset or a USB reset, the device address is set to the default address (0). The default address will match all incoming addresses. The software shall reprogram the address after receiving a SET_ADDRESS descriptor.

The USBADRA is used to accelerate the SET_ADDRESS sequence by allowing the DCD to preset the USBADR register before the status phase of the SET_ADDRESS descriptor.

NOTE This device is shared between the host controller and device controller operations. For host controller operation, this is the USB_OTG_HS_ PERIODICLISTBASE register. For device controller operation, this is the USB_OTG_HS_DEVICEADDR register.

USB1_HS_USB_OTG_HS_DEVICEADDR

Bits	Name	Description
31:25	USBADR_31_25	Device address These bits correspond to the USB device address.

USB1_HS_USB_OTG_HS_DEVICEADDR (cont.)

Bits	Name	Description
24	USBADRA	Device address advance Default = 0 When this bit is clear (0), any writes to USBADR are instantaneous. When this bit is set (1) at the same time or before USBADR is written, the write to the USBADR field is staged and held in a hidden register. After an IN occurs on endpoint 0 and is ACKed, USBADR will be loaded from the holding register. The hardware will automatically clear (0) this bit on the following conditions: 1. IN is ACKed to endpoint 0 (USBADR is updated from staging register). 2. OUT/SETUP occur to endpoint 0 (USBADR is not updated). 3. Device reset occurs (USBADR is reset to 0). Note: After the status phase of the SET_ADDRESS descriptor, the DCD has 2 ms to program the USBADR field. This mechanism will ensure this specification is met when the DCD can not write of the device address within 2 ms from the SET_ADDRESS status phase. If the DCD writes the USBADR with USBADRA = 1 after the SET_ADDRESS data phase (before the prime of the status phase), the USBADR will be programmed instantly at the correct time and meet the 2-ms USB requirement.
23:0	RESERVED_BITS23_0	These bits must be written as zeros. During runtime, the values of these bits are undefined.

0x12500158 USB1_HS_USB_OTG_HS_ASYNCLISTADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ASYNCLISTADDR register is the next asynchronous list address register. This 32-bit register contains the address of the next asynchronous queue head to be executed by the host. Bits [4:0] of this register cannot be modified by the system software and will always return a zero when read.

NOTE The USB_OTG_HS_ASYNCLISTADDR register and the USB_OTG_HS_ENDPOINTLISTADDR register are shared between the host controller and device controller operations. For the host controller, this is the USB_OTG_HS_ASYNCLISTADDR register. For the device controller, this is the USB_OTG_HS_ENDPOINTLISTADDR register.

USB1_HS_USB_OTG_HS_ASYNCLISTADDR

Bits	Name	Description
31:5	ASYBASE_31_15	Link pointer low (LPL). These bits correspond to memory address signals [31:5], respectively. This field may only reference a queue head (OH). This field is only used by the host controller.
4:0	RESERVED_BITS4_0	The values of these bits has no effect on circuit operation.

0x12500158 USB1_HS_USB_OTG_HS_ENDPOINTLISTADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPOINTLISTADDR register is the endpointlist address register. In the device mode, this register contains the address of the top of the endpoint list in system memory. Bits [10:0] of this register cannot be modified by the system software and will always return a zero when read.

NOTE The USB_OTG_HS_ASYNCLISTADDR register and the USB_OTG_HS_ENDPOINTLISTADDR register are shared between the host controller and device controller operations. For the host controller, this is the USB_OTG_HS_ASYNCLISTADDR register. For the device controller, this is the USB_OTG_HS_ENDPOINTLISTADDR register.

USB1_HS_USB_OTG_HS_ENDPOINTLISTADDR

Bits	Name	Description
31:11	EPBASE_31_11	Endpoint list pointer (low) These bits correspond to memory address signals [31:11], respectively. This field will reference a list of up to 32 queue heads (QH). That is, one queue head per endpoint & direction.
10:0	RESERVED_BITS10_0	The values of these bits has no effect on circuit operation.

0x1250015C USB1_HS_USB_OTG_HS_TTCTRL

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_TTCTRL register is the TT status and control register. This register contains parameters needed for internal TT operations.

NOTE This register is not used in the device controller operation.

USB1_HS_USB_OTG_HS_TTCTRL

Bits	Name	Description
31	RESERVED_BIT31	Not used.
30:24	TTHA	Not used.
23:0	RESERVED_BITS23_0	Not used.

0x12500160 USB1_HS_USB_OTG_HS_BURSTSIZE

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1010

The USB_OTG_HS_BURSTSIZE register is the programmable burst size register. This register is used to control dynamically change the burst size used during data movement on the initiator (master) interface.

USB1_HS_USB_OTG_HS_BURSTSIZE

Bits	Name	Description
31:16	RESERVED_BITS31_16	The value of these bits has no effect on circuit operation.
15:8	TXPBURST	Programmable Tx burst length This register represents the maximum length of a the burst in 32-bit words while moving data from system memory to the USB bus.
7:0	RXPBURST	Programmable Rx burst length This register represents the maximum length of a the burst in 32-bit words while moving data from the USB bus to system memory.

0x12500164 USB1_HS_USB_OTG_HS_TXFILLTUNING

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_TXFILLTUNING register is the host transmit pre-buffer packet tuning register. The fields in this register control performance tuning associated with how the host controller posts data to the Tx latency FIFO before moving the data onto the USB bus. The specific areas of performance include the how much data to post into the FIFO and an estimate for how long that operation should take in the target system.

Definitions:

T0 = Standard packet overhead

T1 = Time to send data payload

Tff = Time to fetch packet into TX FIFO up to specified level.

Ts = Total packet flight time (send-only) packet

Ts = T0 + T1

Tp = Total packet time (fetch and send) packet

Tp = Tff + T0 + T1

Upon discovery of a transmit (OUT/SETUP) packet in the data structures, the host controller checks to ensure Tp remains before the end of the [micro] frame. If so it proceeds to pre-fill the TX FIFO. If at anytime during the pre-fill operation the time remaining the [micro] frame is < Ts, then the packet attempt ceases and the packet is tried at a later time. Although this is not an error condition and the host controller will eventually recover, a mark will be made the scheduler health counter to note the occurrence of a ’back-off’ event. When a back-off event is detected, the partial packet fetched may need to be discarded from the latency buffer to make room for periodic traffic that will begin after the next SOF. Too many back-off events can waste bandwidth and power on the system bus, and thus should be minimized (not necessarily eliminated). Back-offs can be minimized with use of the TSCHHEALTH (Tff), as described in the register table.

USB1_HS_USB_OTG_HS_TXFILLTUNING

Bits	Name	Description
31:22	RESERVED_BITS31_22	The value of these bits has no effect on circuit operation.
21:16	TXFIFOTHRES	FIFO burst threshold Default = 2 This register controls the number of data bursts that are posted to the TX latency FIFO in the host mode before the packet begins on to the bus. The minimum value is 2 and this value should be a low as possible to maximize USB performance. A higher value can be used in systems with unpredictable latency and/or insufficient bandwidth, where the FIFO may underrun because the data transferred from the latency FIFO to USB occurs before it can be replenished from system memory. This value is ignored if the stream disable bit in USBMODE register is set (1).
15:13	RESERVED_BITS15_13	The value of these bits has no effect on circuit operation.

USB1_HS_USB_OTG_HS_TXFILLTUNING (cont.)

Bits	Name	Description
12:8	TXSCHHEALTH	Scheduler health counter Read/write to clear Default = 0 This register increments when the host controller fails to fill the Tx latency FIFO to the level programmed by TXFIFOTHRES before running out of time to send the packet before the next start-of-frame. This health counter measures the number of times this occurs to provide feedback to selecting a proper TXSCHOH. Writing to this register will clear the counter and this counter will be at a maximum at 31.
7:0	TXSCHOH	Scheduler overhead Default = 0 This register adds an additional fixed offset to the schedule time estimator described above as Tff. As an approximation, the value chosen for this register should limit the number of back-off events captured in the TXSCHHEALTH to less than 10 per second in a highly-utilized bus. Choosing a value that is too high for this register is not desired, as it can needlessly reduce USB utilization. The time unit represented in this register is 1.267 ms when a device is connected in the high-speed mode for OTG and SPH. The time unit represented in this register is 6.333 ms when a device is connected in the low/full speed mode for OTG and SPH. The time unit represented in this register is always 1.267 times the MPH product.

0x12500170 USB1_HS_USB_OTG_HS_ULPI_VIEWPORT

Type: Read/write (unless otherwise indicated)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x08000000

The USB_OTG_HS_ULPI_VIEWPORT register provides indirect access to the ULPI PHY register set. Although the core performs access to the ULPI PHY register set, there may be extraordinary circumstances where software may need direct access.

CAUTION Writes to the ULPI through the viewport can substantially harm standard USB operations. Currently, no usage model has been defined where the software should need to execute writes directly to the ULPI - see the exception regarding optional features below.

Executing read operations though the ULPI viewport should have no harmful side effects to standard USB operations.

NOTE The ULPI viewport is only synthesized in the design if the constant VUSB_HS_PHY_ULPI is set (1). If the ULPI interface is not enabled, this register will always read zeros.

Two operations can be performed with the ULPI viewport: wake-up and read/write operations. The wake-up operation is used to put the ULPI interface into normal operation mode and re-enable the clock, if necessary. A wake-up operation is required before accessing the registers when the ULPI interface is operating in the low power mode, serial mode, or car kit mode.

The ULPI state can be determined by reading the sync state bit (ULPISS). If this bit is set (1), then the ULPI interface is running in the normal operation mode and can accept read/write operations. If the ULPISS is clear (0), then read/write operations will not be able to execute. Undefined behavior will result if ULPISS = 0, and a read or write operation is performed.

To execute a wake-up operation, write all 32-bits of the ULPI Viewport where ULPIPORT is constructed appropriately, and the ULPIWU bit is set (1) and the ULPIRUN bit is clear (0). Poll the ULPI viewport until ULPIWU is zero for the operation to complete.

To execute a read or write operation, write all 32-bits of the ULPI viewport where ULPIDATWR, ULPIADDR, ULPIPORT, and ULPIRW are constructed appropriately, and the ULPIRUN bit is set (1). Poll the ULPI viewport until ULPIRUN is zero for the operation to complete. Once ULPIRUN is zero, the ULPIDATRD will be valid if the operation was a read.

The polling method above could also be replaced and an interrupt driven using the ULPI interrupt defined in the USBTS and USBINTR registers. When a wake-up or read/write operation completes, the ULPI interrupt will be set (1).

Several optional features may need to be enabled or disabled by the system software as part of system configuration. These bits are contained in the interface and OTG control registers of the ULPI PHY register set. These registers also contain bits that are controlled by the link dynamically and, therefore, should only be modified by the system software using the set/clear access method. Direct writes to these registers could have harmful side effects to the standard USB operations. The following bits are optional bits:

- Bits 3 through 7 in the interface control register
- Bits 6 and 7 in the OTG control register.

Refer to the ULPI Specification Revision 1.1 for further information on the use of the optional features. For more information on the use of the optional features http://www.ulpi.org/documents.html.

USB1_HS_USB_OTG_HS_ULPI_VIEWPORT

Bits	Name	Description
31	ULPIWU	ULPI wake-up Setting (1) this bit begins the wake-up operation. The bit will automatically transition to 0 after the wake-up is complete. Once this bit is set (1), the driver can not clear it back to 0. Note: The driver must never execute a wake-up and a read/write operation at the same time.

USB1_HS_USB_OTG_HS_ULPI_VIEWPORT (cont.)

Bits	Name	Description
30	ULPIRUN	ULPI read/write run Setting (1) this bit will begin the read/write operation. The bit will automatically transition to 0 after the read/write is complete. Once this bit is set (1), the driver can not clear it back to 0. Note: The driver must never execute a wakeup and a read/write operation at the same time.
29	ULPIRW	ULPI read/write control This bit selects between running a read or write operation. value 0 = Read value 1 = Write
28	ULPIFORCE	ULPI read/write force This bit enables forcing register access during RX packet value 0 = register access is not forced during RX packet (default) value 1 = register access is forced during RX packet reception
27	ULPISS	ULPI sync state Read Only value 1 = Normal sync state value 0 = In another state (for example, car kit, serial, low power) This bit represents the state of the ULPI interface. Before reading this bit, the ULPIPORT field should be set accordingly if used with the multi-port host. Otherwise, this field should always remain 0.
26:24	ULPIPORT	ULPI port number For the wakeup or read/write operation to be executed, this value selects the port number the ULPI PHY is attached to in the multi-port host. The valid range is 0 to 7. This field should always be written as a 0 for the non-multi port products.
23:16	ULPIADDR	ULPI data address When a read or write operation is commanded, the address of the operation is written to this field.
15:8	ULPIDATRD	ULPI data read Read only After a read operation completes, the result is placed in this field.
7:0	ULPIDATWR	ULPI data write When a write operation is commanded, the data to be sent is written to this field.

0x12500178 USB1_HS_USB_OTG_HS_ENDPTNAK

Type: Read/write clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTNAK register is the endpoint NAK register.

USB1_HS_USB_OTG_HS_ENDPTNAK

Bits	Name	Description
31:16	EPTN_15_0	Tx endpoint NAK Each tx endpoint has 1 bit in this field. The bit is set (1) when the device sends a NAK handshake on a received IN token for the corresponding endpoint. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0
15:0	EPRN_15_0	Rx endpoint NAK Each rx endpoint has 1 bit in this field. The bit is set (1) when the device sends a NAK handshake on a received OUT or PING token for the corresponding endpoint. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x1250017C USB1_HS_USB_OTG_HS_ENDPTNAKEN

Type: Read/write clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTNAKEN register is the endpoint NAK enable register.

USB1_HS_USB_OTG_HS_ENDPTNAKEN

Bits	Name	Description
31:16	EPTNE_15_0	Tx endpoint NAK enable Each bit is an enable bit for the corresponding Tx endpoint NAK bit. If this bit is set (1) and the corresponding Tx endpoint NAK bit is set (1), the NAK Interrupt bit is set (1). Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0
15:0	EPRNE_15_0	Rx endpoint NAK enable Each bit is an enable bit for the corresponding Rx endpoint NAK bit. If this bit is set (1) and the corresponding Rx endpoint NAK bit is set (1), the NAK Interrupt bit is set (1). Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x12500184 USB1_HS_USB_OTG_HS_PORTSC

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xCC000004

This is the USB_OTG_HS_PORTSC register.

USB1_HS_USB_OTG_HS_PORTSC

Bits	Name	Description
31:30	PTS	Parallel transceiver select Read/write This register bit pair is used in conjunction with the configuration constant VUSB_HS_PHY_TYPE to control which parallel transceiver interface is selected. If VUSB_HS_PHY_ TYPE is set for 0, 1, 2, or 3, then this bit is read only. If VUSB_HS_PHY_TYPE is 4, 5, 6, or 7, then this bit is read/write. This field is reset to the following values: 00 if VUSB_HS_PHY_TYPE = 0,4 - UTMI/UTMI+ 01 if VUSB_HS_PHY_TYPE = 1,5 - Reserved 10 if VUSB_HS_PHY_TYPE = 2,6 - ULPI 11 if VUSB_HS_PHY_TYPE = 3,7 - Serial/1.1 PHY (FS only) This bit is not defined in the EHCI specification.
29	STS	Serial transceiver select Read/write This register bit is used in conjunction with the configuration constant VUSB_HS_PHY_SERIAL to control whether the parallel or serial transceiver interface is selected for FS and LS operation. The serial interface engine can be used in combination with the UTMI+ or ULPI physical interface to provide FS/LS signaling instead of the parallel interface. ’ If VUSB_HS_PHY_SERIAL is 0 or 1, then this bit is read only. ’ If VUSB_HS_PHY_SERIAL is 2 or 3, then this bit is read/write. This bit has no effect unless the parallel transceiver select is set to UTMI+ or ULPI. The Serial/1.1 physical interface will use the serial interface engine for FS/LS signaling regardless of this bit value. Note: This bit was reserved for future operation, and is now adding for dynamic use of the serial engine in accord with UMTI+ and ULPI characterization logic. This bit is not defined in the EHCI specification.

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
28	PTW	Parallel transceiver width Read/write This register bit is used in conjunction with the configuration constant VUSB_HS_PHY16_8 to control the data bus width of the UTMI transceiver interface. ' If VUSB_HS_PHY16_8 is 0 or 1, then this bit is read only. ' If VUSB_HS_PHY16_8 is 2 or 3, then this bit is read/write. This bit is reset to 1 if VUSB_HS_PHY16_8 selects a default UTMI interface width of 16-bits, else it is reset to 0. ' Writing this bit to 0 selects the 8-bit [60MHz] UTMI interface. ' Writing this bit to 1 selects the 16-bit [30MHz] UTMI interface. This bit has no effect if the serial interface is selected. This bit is not defined in the EHCI specification.
27:26	PSPD	Port speed Read only This register field indicates the speed at which the port is operating. For HS mode operation in the host controller and HS/FS operation in the device controller, the port routing steers data to the protocol engine. For FS and LS mode operation in the host controller, the port routing steers data to the protocol engine with the embedded transaction translator. value 00 = Full speed value 01 = Low speed value 10 = High speed This bit is not defined in the EHCI specification.
25	SPRT	Short Port Reset Time. shortens port reset time for simulation.
24	PFSC	Port force full speed connect Read/write Default = 0 Setting (1) this bit will force the port to only connect at full speed. It also disables the chirp sequence that allows the port to identify itself as high speed. This is useful for testing FS configurations with a HS host, hub or device. This bit is not defined in the EHCI specification. This bit is for debugging purposes.

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
23	PHCD	PHY low power suspend - clock disable (PLPSCD) Read/write Default = 0 value 1 = Disable the PHY clock. value 0 = Enable the PHY clock. Reading this bit will indicate the status of the PHY clock. Note: The PHY clock cannot be disabled if it is being used as the system clock. In the device mode, The PHY can be put into low power suspend - clock disable when the device is not running (USBCMD run/stop = 0) or the host has signaled suspend (PORTSC SUSPEND = 1). Low power suspend will be cleared automatically when the host has signaled resume. Before forcing a resume from the device, the device controller driver must clear this bit. In the host mode, the PHY can be put into low power suspend - clock disable when the downstream device has been put into the suspend mode or when no downstream device is connected. Low power suspend is completely under the control of the software. This bit is not defined in the EHCI specification.
22	WKOC	Wake on over-current enable (WKOC_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to over-current conditions as wake-up events. This bit is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0). This bit is output from the controller as signal pwrctl_wake_ ovrcurr_en (OTG/host core only) for use by an external power control circuit.
21	WKDS	Wake on disconnect enable (WKDSCNNT_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to device disconnects as wake-up events. This field is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0) or in the device mode. This bit is output from the controller as signal pwrctl_wake_ dscnnt_en (OTG/host core only) for use by an external power control circuit.

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
20	WKCN	Wake on connect enable (WKCNNT_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to device connects as wake-up events. This field is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0) or in the device mode. This bit is output from the controller as signal pwrctl_wake_ dscnnt_en (OTG/host core only) for use by an external power control circuit.

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
19:16	PTC_3_0	Port test control Read/write Default = 0000 Any other value than zero indicates that the port is operating in the test mode. Value Specific test The FORCE_ENABLE_FS and FORCE ENABLE_LS tests are extensions to the test mode support, as specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. Note: Low speed operations are not supported as a peripheral device. 0x0: TEST_MODE_DISABLE 0x1: J_ STATE 0x8: K_STATE 0x9: SE0 (host / NAK device) 0x40: Packet 0x41: FORCE_ENABLE_HS 0x48: FORCE_ENABLE_FS 0x49: FORCE_ENABLE_LS 0x3E8: Reserved_1 0x3E9: Reserved_2 0x3EA: Reserved_3 0x3EB: Reserved_4 0x3EC: Reserved_5 0x3ED: Reserved_6 0x3EE: Reserved_7 0x3EF: Reserved_8 0x3F0: Reserved_9 0x3F1: Reserved_10 0x3F2: Reserved_11 0x3F3: Reserved_12 0x3F4: Reserved_13 0x3F5: Reserved_14 0x3F6: Reserved_15 0x3F7: Reserved_16 0x3F8: Reserved_17 0x3F9: Reserved_18 0x3FA: Reserved_19 0x3FB: Reserved_20 0x3FC: Reserved_21 0x3FD: Reserved_22 0x3FE: Reserved_23 0x3FF: Reserved_24

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
19:16	PTC_3_0 (CONTINUED)	0x400: Reserved_25 0x401: Reserved_26 0x402: Reserved_27 0x403: Reserved_28 0x404: Reserved_29 0x405: Reserved_30 0x406: Reserved_31 0x407: Reserved_32 0x408: Reserved_33 0x409: Reserved_34 0x40A: Reserved_35 0x40B: Reserved_36 0x40C: Reserved_37 0x40D: Reserved_38 0x40E: Reserved_39 0x40F: Reserved_40 0x410: Reserved_41 0x411: Reserved_42 0x412: Reserved_43 0x413: Reserved_44 0x414: Reserved_45 0x415: Reserved_46 0x416: Reserved_47 0x417: Reserved_48 0x418: Reserved_49 0x419: Reserved_50 0x41A: Reserved_51 0x41B: Reserved_52 0x41C: Reserved_53 0x41D: Reserved_54 0x41E: Reserved_55 0x41F: Reserved_56 0x420: Reserved_57 0x421: Reserved_58 0x422: Reserved_59 0x423: Reserved_60 0x424: Reserved_61 0x425: Reserved_62 0x426: Reserved_63 0x427: Reserved_64 0x428: Reserved_65 0x429: Reserved_66 0x42A: Reserved_67 0x42B: Reserved_68

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
19:16	PTC_3_0 (CONTINUED)	0x42C: Reserved_69 0x42D: Reserved_70 0x42E: Reserved_71 0x42F: Reserved_72 0x430: Reserved_73 0x431: Reserved_74 0x432: Reserved_75 0x433: Reserved_76 0x434: Reserved_77 0x435: Reserved_78 0x436: Reserved_79 0x437: Reserved_80 0x438: Reserved_81 0x439: Reserved_82 0x43A: Reserved_83 0x43B: Reserved_84 0x43C: Reserved_85 0x43D: Reserved_86 0x43E: Reserved_87 0x43F: Reserved_88 0x440: Reserved_89 0x441: Reserved_90 0x442: Reserved_91 0x443: Reserved_92 0x444: Reserved_93 0x445: Reserved_94 0x446: Reserved_95 0x447: Reserved_96 0x448: Reserved_97 0x449: Reserved_98 0x44A: Reserved_99 0x44B: Reserved_100 0x44C: Reserved_101 0x44E: Reserved_103 0x44F: Reserved_104 0x450: Reserved_105 0x451: Reserved_106 0x452: Reserved_107 0x453: Reserved_108 0x44D: Reserved_102 0x454: Reserved_109 0x455: Reserved_110 0x456: Reserved_111 0x457: Reserved_112

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
15:14	PIC_1_0	Port indicator control Read/write Default = 0 Writing to this field has no effect if the P_INDICATOR bit in the HCSPARAMS register is a zero. If the P_INDICATOR bit is set (1), then this field has the following meanings: Bit value Meaning value 00 Port indicators are off value 01 Amber value 10 Green value 11 Undefined Refer to the USB Specification Revision 2.0 for a description on how these bits are to be used http://www.usb.org/developers/docs/ This field is output from the controller as signals port_ind_ctl_1 and port_ind_ctl_0 for use by an external LED driving circuit.
13	PO	Port owner Read only Port owner hand-off is not implemented in this design, therefore this bit will always read back as clear (0). Default = 0 The EHCI definition is include here for reference: ’ This bit unconditionally goes clear (0) when the configured bit in the CONFIGFLAG register makes a 0-to-1 transition. ’ This bit unconditionally goes set (1) whenever the configured bit is clear (0). The system software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). The software sets (1) this bit when the attached device is not a high-speed device. When this bit is set (1), it indicates that an internal companion controller owns and controls the port.

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
12	PP	Port power (PP) Read/write or read-only The function of this bit depends on the value of the port power switching (PPC) field in the HCSPARAMS register. ’ PPC = 0: PP is read-only. A device controller with no OTG capability does not have port power control switches. ’ PPC = 1: PP is read/write. The host/OTG controller requires port power control switches. This bit represents the current setting of the switch (0 = off, 1 = on). When power is not available on a port (and PP equals a 0), the port is non-functional and will not report attaches, detaches, and so on. When an over-current condition is detected on a powered port and PPC is set (1), the PP bit in each affected port may be transitioned by the host controller driver from a one to a zero, removing power from the port. This feature is implemented in the host/OTG controller (PPC = 1). In a device-only implementation, port power control is not necessary. So, PPC and PP = 0.
11:10	LS_1_0	Line status Read-only These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines: Value Meaning value 00 SE0 value 10 J-state value 01 K-state value 11 Undefined In the host mode, the use of line state by the host controller driver is not necessary (unlike EHCI), because the port controller state machine and the port routing manage the connection of LS and FS. In the device mode, the use of line state by the device controller driver is not necessary.
9	HSP	High-speed port Read-only Default = 0 When the bit is set (1), the host/device connected to the port is in the high-speed mode. When this bit is clear (0), the host/device connected to the port is not in a high-speed mode. Note: HSP is redundant with PSPD(27:26), but will remain in the design for compatibility. This bit is not defined in the EHCI specification.

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
8	PR	Port reset This bit is clear (0) if the port power (PP) bit (bit 12) of this register is clear (0). Host mode: ’ Read/write ’ Default = 0 When the software sets (1) this bit, the bus-reset sequence as defined in the USB Specification Revision 2.0 is started. This bit will automatically clear (go to 0) after the reset sequence is complete. Note: This behavior is different from EHCI, where the host controller driver is required to clear (0) this bit after the reset duration is timed in the driver. Device mode: This bit is a read-only status bit. Device reset from the USB bus is also indicated in the USBSTS register. 0x1: Port is in reset 0x0: Port is not in reset

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
7	SUSP	Suspend Host mode: ’ Read/write ’ Default = 0 The port enabled bit and suspend bit of this register define the port states: Bit value Port state value 0x Disable value 10 Enable value 11 Suspend When in the suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction if a transaction was in progress when this bit set (1). In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. The host controller will unconditionally clear (0) this bit when the software clears (0) the force port resume bit. The host controller ignores a write of zero to this bit. If the host software sets (1) this bit when the port is not enabled (port enabled bit is a zero), the results are undefined. This field is clear (0) if port power (PP) is clear (0) in the host mode. Device mode: ’ Read only ’ Default = 0 In the device mode, this bit is a read-only status bit. 0x1: Port in suspend state_1 0x0: Port not in suspend st_1 0x1: Port in suspend state_2 0x0: Port not in suspend st_2

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
6	FPR	Force port resume ’ Read/write ’ Default = 0 Host mode: The software sets (1) this bit to drive resume signaling. The host controller sets (1) this bit if a J-to-K transition is detected while the port is in the suspend state. When this bit transitions to a one because a J-to-K transition is detected, the port change detect bit in the USBSTS register is also set (1). This bit will automatically clear (go to 0) after the resume sequence is complete. This behavior is different from EHCI, where the host controller driver is required to clear (0) this bit after the resume duration is timed in the driver. Note that, when the host controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (full-speed 'K') is driven on the port as long as this bit remains set (1). This bit will remain set (1) until the port has switched to the high-speed idle. Clearing (0) this bit has no affect, because the port controller will time the resume operation and clear (0) the bit when the port control state switches to HS or FS idle. This bit is clear if the port power (PP) is clear (0) in the host mode. This bit is not-EHCI compatible. Device mode: After the device has been in the suspend state for 5 ms or more, the software must set (1) this bit to drive resume signaling before clearing. The device controller will set (1) this bit if a J-to-K transition is detected while the port is in the suspend state. The bit will be cleared (0) when the device returns to normal operation. Also, when this bit transitions to a one because a J-to-K transition was detected, the port change detect bit in the USBSTS register is also set (1). 0x1: Resume detected/driven on port 0x0: No resume (K-state detected/driven on port)
5	OCC	Over-current change Read/write control Default = 0 This bit gets is set (1) when there is a change to over-current active. The software clears this bit by setting (1) this bit position. For host/OTG implementations, the user can provide over-current detection to the vbus_pwr_fault input for this condition. For device-only implementations, this bit shall always be clear (0).

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
4	OCA	Over-current active Read-only Default = 0 value 1 = This port currently has an over-current condition. value 0 = This port does not have an over-current condition. This bit will automatically transition from set (1) to clear (0) when the over current condition is removed. For host/OTG implementations, the user can provide over-current detection to the vbus_pwr_fault input for this condition. For device-only implementations, this bit shall always be clear (0).
3	PEC	Port enable/disable change Read/write control value 1 = Port enabled/disabled status has changed value 0 = No change Default = 0 Host mode: For the root hub, this bit gets set (1) only when a port is disabled due to disconnect on the port or due to the appropriate conditions existing at the EOF2 point. The software clears this bit by writing a one to it. This field is clear (0) if the port power (PP) bit in the register is clear (0). Device mode: The device port is always enabled (this bit will be zero).
2	PE	Port enabled/disabled Read/write value 1 = Enable value 0 = Disable Default 0 Host mode: Ports can only be enabled by the host controller as a part of the reset and enable. The software cannot enable a port by setting (1) this field. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by the host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port, due to other host controller and bus events. When the port is disabled, (0) downstream propagation of data is blocked except for reset. This field is clear (0) if the port power (PP) bit is cleared (0) in the host mode. Device mode: The device port is always enabled (this bit will be set [1])

USB1_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
1	CSC	Connect status change Read/write control value 1 = Change in current connect status value 0 = No change Default = 0 Host mode: Indicates that a change has occurred in the port's current connect status. The host/device controller sets (1) this bit for all changes to the port device connect status, even if the system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, the hub hardware will be 'setting' an already-set bit (that is, the bit will remain set). The software clears this bit by writing a one to it. This field is zero if the port power (PP) bit in this register is zero in the host mode. Device mode: This bit is undefined in the device controller mode.
0	CCS	Current connect status Read-only Host mode: value 1 = Device is present on port value 0 = No device is present Default = 0 This value reflects the current state of the port, and may not correspond directly to the event that caused the connect status change bit (bit 1) to be set (1). This field is clear if the port power (PP) bit in this register is clear (0) in host mode. Device mode: value 1 = Attached value 0 = Not attached Default = 0 If this bit is set (1), this indicates that the device successfully attached, and is operating in either high speed or full speed, as indicated by the high speed port bit in this register. If this bit is clear (0), this indicates that the device did not attach successfully or was forcibly disconnected by the software clearing (0) the run bit in the USBCMD register. It does not state the device being disconnected or suspended.

0x125001A4 USB1_HS_USB_OTG_HS_OTGSC

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000E20

USB1_HS_USB_OTG_HS_OTGSC

Bits	Name	Description
31	RESERVED_BIT31	Clear (0) this bit.
30	DPIE	Data pulse interrupt enable
29	B_1MSE	1 millisecond timer interrupt enable - read/write
28	BSEIE	B session end interrupt enable Read/write Setting (1) this bit enables the B session end interrupt.
27	BSVIE	B session valid interrupt enable Read/write Setting (1) this bit enables the B session valid interrupt.
26	ASVIE	A session valid interrupt enable Read/write Setting (1) this bit enables the A session valid interrupt.
25	AVVIE	A Vbus valid interrupt enable Read/write Setting (1) this bit enables the A Vbus valid interrupt.
24	IDIE	USB ID interrupt enable Read/write Setting (1) this bit enables the USB ID interrupt.
23	RESERVED_BIT23	Clear (0) this bit.
22	DPIS	Data pulse interrupt status Read/write to clear This bit is set (1) when data bus pulsing occurs on DP or DM. Data bus pulsing is only detected when USBMODE.CM = Host (11) and PORTSC(0). PortPower = Off (0). The software must write a one to clear this bit.
21	B_1MSS	1 millisecond timer interrupt status Read/write to clear This bit is set (1) once every millisecond. The software must write a one to clear this bit.
20	BSEIS	B session end interrupt status Read/write to clear This bit is set (1) when the Vbus has fallen below the B session end threshold. The software must write a one to clear this bit
19	BSVIS	B session valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the B session valid threshold (0.8 VDC). The software must write a one to clear this bit.

USB1_HS_USB_OTG_HS_OTGSC (cont.)

Bits	Name	Description
18	ASVIS	A session valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the A session valid threshold (0.8 VDC). The software must write a one to clear this bit.
17	AVVIS	A Vbus valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the Vbus valid threshold (4.4 VDC) on an A device. The software must write a one to clear this bit.
16	IDIS	USB ID interrupt status Read/write This bit is set (1) when a change on the ID input has been detected. The software must write a one to clear this bit.
15	RESERVED_BIT15	Clear (0) this bit.
14	DPS	Data bus pulsing status Read-only If this bit is set (1), it indicates that the data bus pulsing is being detected on the port.
13	B_1MST	1 millisecond timer toggle Read-only This bit toggles once per millisecond.
12	BSE	B session end Read-only Indicates that the Vbus is below the B session end threshold.
11	BSV	B session valid Read-only Indicates that the Vbus is above the B session valid threshold.
10	ASV	A session valid Read-only Indicates that the Vbus is above the A session valid threshold.
9	AVV	A Vbus valid Read-only Indicates that the Vbus is above the A Vbus valid threshold.
8	ID	USB ID Read-only value 0 = A device value 1 = B device

USB1_HS_USB_OTG_HS_OTGSC (cont.)

Bits	Name	Description
7	HABA	Hardware assist B-disconnect to A-connect Read/write value 0 = Disabled value 1 = Enable automatic B-disconnect to A-connect sequence.
6	HADP	Hardware assist data-pulse Write to set
5	IDPU	ID pull-up Read/write This bit provides control over the ID pull-up register. value 0 = Off value 1 = On (default) When this bit is clear (0), the ID input will not be sampled.
4	DP	Data pulsing Read/write Setting (1) this bit causes the pull-up on DP to be asserted for data pulsing during SRP.
3	OT	OTG termination Read/write This bit must be set (1) when the OTG device is in the device mode. This controls the pull-down on DM.
2	HAAR	Hardware assist auto-reset Read/write value 0 = Disabled value 1 = Enable automatic reset after connect on host port.
1	VC	Vbus charge Read/write Setting (1) this bit causes the Vbus line to be charged. This is used for Vbus pulsing during SRP.
0	VD	Vbus discharge Read/write Setting (1) this bit causes the Vbus to discharge through a resistor.

0x125001A8 USB1_HS_USB_OTG_HS_USBMODE

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_USBMODE register is the USB device mode register.

USB1_HS_USB_OTG_HS_USBMODE

Bits	Name	Description
31:6	RESERVED_BITS31_6	Clear (0) these bits.
5	VBPS	Vbus power select value 0 - Output is 0 value 1 - Output is 1 This bit is connected to the vbus_pwr_select output and can be used for any generic control, but is named to be used by logic that selects between an on-chip Vbus power source (charge pump) and an off-chip source in systems when both are available.
4	SDIS	Stream disable mode value 0 = Inactive (default) value 1 = Active Device mode: Setting (1) this bit disables double priming on both the Rx and Tx for low bandwidth systems. This mode ensures that, when the Rx and Tx buffers are sufficient to contain an entire packet, the standard double buffering scheme is disabled to prevent overruns/underruns in bandwidth-limited systems. Note: In the high speed mode, a NYET handshake will respond to all packets received when the stream disable is active. Host mode: Setting (1) this bit ensures that overruns/underruns of the latency FIFO are eliminated for low bandwidth systems where the Rx and Tx buffers are sufficient to contain the entire packet. Enabling the stream disable also has the effect of ensuring that the Tx latency is filled to capacity before the packet is launched onto the USB. Note: Time duration to pre-fill the FIFO becomes significant when the stream disable is active. See TXFILLTUNING and TXTTFILLTUNING [MPH only] to characterize the adjustments needed for the scheduler when using this feature. Note: The use of this feature substantially limits of the overall USB performance.
3	SLOM	Setup lockout mode. In the device mode, this bit controls the behavior of the setup lock mechanism. value 0 = Setup lockouts on (default) value 1 = Setup lockouts off (DCD requires use of a setup data buffer tripwire in USBCMD)

USB1_HS_USB_OTG_HS_USBMODE (cont.)

Bits	Name	Description
2	ES	Endian select Read/write This bit can change the byte ordering of the transfer buffers to match the host microprocessor bus architecture. The bit fields in the microprocessor interface and the DMA data structures (including the setup buffer within the device QH) are unaffected by the value of this bit, because they are based upon 32-bit words. value 0 = Little endian (default) - first byte referenced in the least significant byte of a 32-bit word. value 1 = Big endian - first byte referenced in most significant byte of a 32-bit word.
1:0	CM	Controller mode Read/write once The controller mode is defaulted to the proper mode for host-only and device-only implementations. For those designs that contain both host and device capability, the controller will default to an idle state and will need to be initialized to the desired operating mode after reset. For combination host/device controllers, this register can only be written once after reset. If it is necessary to switch modes, the software must reset the controller by writing to the RESET bit in the USBCMD register before reprogramming this register. value 00 = Idle [default for combination host/device] value 01 = Reserved value 10 = Device controller [default for device only controller] value 11 = Host controller [default for host only controller]

0x125001AC USB1_HS_USB_OTG_HS_ENPDTSETUPSTAT

Type: Read/write control
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENPDTSETUPSTAT register is the endpoint set-up status register.

USB1_HS_USB_OTG_HS_ENPDTSETUPSTAT

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.

USB1_HS_USB_OTG_HS_ENPDTSETUPSTAT (cont.)

Bits	Name	Description
15:0	ENDPTSETUPSTAT_15_0	Set-up endpoint status For every set-up transaction that is received, a corresponding bit in this register is set (1). The software must clear or acknowledge the setup transfer by setting (1) a respective bit after it has read the setup data from the queue head. The response to a set-up packet as in the order of operations and total response time is crucial to limit bus time outs while the set-up lock-out mechanism is engaged. See Managing Endpoints in the Device Operational Model. This register is only used in the device mode.

0x125001B0 USB1_HS_USB_OTG_HS_ENDPTPRIME

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTPRIME register is the endpoint initialization register. This register is only used in the device mode.

USB1_HS_USB_OTG_HS_ENDPTPRIME

Bits	Name	Description
31:16	PETB_15_0	Prime endpoint transmit buffer For each endpoint, a corresponding bit is used to request that a buffer is prepared for a transmit operation in order to respond to a USB IN/INTERRUPT transaction. The software should set (1) the corresponding bit when posting a new transfer descriptor to an endpoint. The hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a transmit buffer. The hardware will clear (0) this bit when the associated endpoint(s) is (are) successfully primed. Note: These bits will be momentarily set (1) by the hardware during hardware re-priming operations when a dTD is retired, and the dQH is updated. PETB[15] - Endpoint 15 PETB[1] - Endpoint 1 PETB[0] - Endpoint 0

USB1_HS_USB_OTG_HS_ENDPTPRIME (cont.)

Bits	Name	Description
15:0	PERB_15_0	Prime endpoint receive buffer For each endpoint, a corresponding bit is used to request that a buffer is prepared for a receive operation for when a USB host initiates a USB OUT transaction. The software should set (1) the corresponding bit whenever posting a new transfer descriptor to an endpoint. The hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a receive buffer. The hardware will clear (0) this bit when the associated endpoint(s) is (are) successfully primed. Note: These bits will be momentarily set (1) by the hardware during hardware re-priming operations when a dTD is retired, and the dQH is updated. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x125001B4 USB1_HS_USB_OTG_HS_ENDPTFLUSH

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTFLUSH register is the endpoint de-initialize register. This register is only used in the device mode.

USB1_HS_USB_OTG_HS_ENDPTFLUSH

Bits	Name	Description
31:16	FETB_15_0	Flush endpoint transmit buffer Setting (1) a bit in this register will cause the associated endpoint to clear any primed buffers. If a packet is in progress for one of the associated endpoints, that transfer will continue until completion. The hardware will clear this register after the endpoint flush operation is successful. FETB[15] - Endpoint 15 FETB[1] - Endpoint 1 FETB[0] - Endpoint 0
15:0	FERB_15_0	Flush endpoint receive buffer Setting a bit (1) will cause the associated endpoint to clear any primed buffers. If a packet is in progress for one of the associated endpoints, that transfer will continue until completion. The hardware will clear this register after the endpoint flush operation is successful. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x125001B8 USB1_HS_USB_OTG_HS_ENDPTSTAT

Type: Read-only
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTSTAT register is the endpoint status register. This register is only used in the device mode.

USB1_HS_USB_OTG_HS_ENDPTSTAT

Bits	Name	Description
31:16	ETBR_15_0	Endpoint transmit buffer ready One bit for each endpoint indicates the status of the respective endpoint buffer. This bit is set (1) by the hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There will always be a delay between setting (1) a bit in the ENDPTPRIME register and the endpoint indicating that it is ready. This delay time varies based upon the current USB traffic and the number of bits set (1) in the ENDPTPRIME register. The buffer ready status is cleared by a USB reset, by the USB DMA system, or through the ENDPTFLUSH register. Note: These bits will be momentarily cleared by the hardware during hardware endpoint re-priming operations when a dTD is retired, and the dQH is updated. ETBR[15] - Endpoint 15 ETBR[1] - Endpoint 1 ETBR[0] - Endpoint 0
15:0	ERBR_15_0	Endpoint receive buffer ready One bit for each endpoint indicates the status of the respective endpoint buffer. This bit is set (1) by the hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There will always be a delay between setting (1) a bit in the ENDPTPRIME register and the endpoint indicating that it is ready. This delay time varies based upon the current USB traffic and the number of bits set (1) in the ENDPTPRIME register. The buffer ready status is cleared by a USB reset, by the USB DMA system, or through the ENDPTFLUSH register. Note: These bits will be momentarily cleared by the hardware during hardware endpoint re-priming operations when a dTD is retired, and the dQH is updated. ERBR[15] - Endpoint 15 ERBR[1] - Endpoint 1 ERBR[0] - Endpoint 0

0x125001BC USB1_HS_USB_OTG_HS_ENDPTCOMPLETE

Type: Read/write control
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The register is the endpoint complete register. This register is only used in the device mode.

USB1_HS_USB_OTG_HS_ENDPTCOMPLETE

Bits	Name	Description
31:16	ETCE_15_0	Endpoint transmit complete event Each bit indicates that a transmit event (IN/INTERRUPT) occurred and the software should read the corresponding endpoint queue to determine the endpoint status. If the corresponding IOC bit is set (1) in the transfer descriptor, then this bit will be set (1) simultaneously with the USBINT. Writing a one will clear the corresponding bit in this register. ETCE[15] - Endpoint 15 ETCE[1] - Endpoint 1 ETCE[0] - Endpoint 0
15:0	ERCE_15_0	Endpoint receive complete event Each bit indicates that a received event (OUT/SETUP) occurred and the software should read the corresponding endpoint queue to determine the transfer status. If the corresponding IOC bit is set (1) in the transfer descriptor, then this bit will be set (1) simultaneously with the USBINT. Writing a one will clear the corresponding bit in this register. ERCE[15] - Endpoint 15 ERCE[1] - Endpoint 1 ERCE[0] - Endpoint 0

0x125001C0 USB1_HS_USB_OTG_HS_ENDPTCTRL0

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00800080

The USB_OTG_HS_ENDPTCTRL0 register is the endpoint control 0 register. Every device will implement endpoint0 as a control endpoint.

USB1_HS_USB_OTG_HS_ENDPTCTRL0

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.

USB1_HS_USB_OTG_HS_ENDPTCTRL0 (cont.)

Bits	Name	Description
23	TXE	Tx endpoint enable value 1 = Enabled Endpoint0 is always enabled. Read only
22:20	RESERVED_BITS22_20	Clear (0) these bits.
19:18	TXT	Tx endpoint type Read only value 00 = Control Endpoint0 is fixed as a control end point.
17	RESERVED_BIT17	Clear (0) this bit.
16	TXS	Tx endpoint stall Read/write value 0 = End point OK (default) value 1 = End point stalled The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. It will continue returning STALL until the bit is cleared (0) by the software or it will automatically be cleared (0) upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). Note: There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. In most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15:8	RESERVED_BITS15_8	Clear (0) these bits.
7	RXE	Rx endpoint enable value 1 = Enabled Endpoint0 is always enabled. Read only
6:4	RESERVED_BITS6_4	Clear (0) these bits.
3:2	RXT	Rx endpoint type Read only value 00 = Control Endpoint0 is fixed as a control end point.
1	RESERVED_BIT1	Clear (0) this bit.

USB1_HS_USB_OTG_HS_ENDPTCTRL0 (cont.)

Bits	Name	Description
0	RXS	Rx endpoint stall Read/write value 0 = End point OK (default) value 1 = End point stalled The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. It will continue returning STALL until the bit is cleared (0) by the software or it will automatically be cleared (0) upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). Note: There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. In most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

0x125001C0+4*n USB1_HS_USB_OTG_HS_ENDPTCTRLn, n=[1..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTCTRLn register is the endpoint control n register. There is an ENDPTCTRLn register for each endpoint in a device.

CAUTION If one endpoint direction is enabled and the paired endpoint of the opposite direction is disabled, then the unused direction type must be changed from the default control-type to any other type (such as bulk-type). Leaving an unconfigured endpoint control will cause undefined behavior for the data PID tracking on the active endpoint/direction.

USB1_HS_USB_OTG_HS_ENDPTCTRLn

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.
23	TXE	Tx endpoint enable value 0 = Disabled (default) value 1 = Enabled An endpoint should be enabled only after it has been configured.

USB1_HS_USB_OTG_HS_ENDPTCTRLn (cont.)

Bits	Name	Description
22	TXR	Tx data toggle reset (WS) value 1 = Reset PID sequence Whenever a configuration event is received for this endpoint, the software must set (1) this bit in order to synchronize the data PIDs between the host and device.
21	TXI	Tx data toggle inhibit value 0 = PID sequencing enabled (default) value 1 = PID sequencing disabled This bit is only used for testing and should always be cleared (0). Setting (1) this bit will cause this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.
20	RESERVED_BIT20	Clear (0) this bit.
19:18	TXT	Tx endpoint type value 00 = Control value 01 = Isochronous value 10 = Bulk value 11 = Interrupt
17	TXD	Tx endpoint data source value 0 = Dual port memory buffer/DMA engine (default) This bit should always be cleared (0).
16	TXS	Tx endpoint stall value 0 = End point OK value 1 = End point stalled This bit will be cleared (0) automatically upon receipt of a SETUP request if this endpoint is configured as a control endpoint, and this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. This control will continue to STALL until this bit is either cleared (0) by the software or automatically cleared (0) as described above for control endpoints. Note (control endpoint types only): There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. in most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15:8	RESERVED_BITS15_8	Clear (0) these bits.
7	RXE	Rx endpoint enable value 0 = Disabled (default) value 1 = Enabled An endpoint should be enabled only after it has been configured.

USB1_HS_USB_OTG_HS_ENDPTCTRLn (cont.)

Bits	Name	Description
6	RXR	Rx data toggle reset (WS) Write 1 = Reset PID sequence Whenever a configuration event is received for this endpoint, the software must set (1) this bit in order to synchronize the data PIDs between the host and the device.
5	RXI	Rx data toggle inhibit value 0 = Disabled (default) value 1 = Enabled This bit is only used for testing and should always be cleared (0). Setting (1) this bit will cause this endpoint to ignore the data toggle sequence and always accept a data packet regardless of their data PID.
4	RESERVED_BIT4	Clear (0) this bit.
3:2	RXT	Rx endpoint type value 00 = Control value 01 = Isochronous value 10 = Bulk value 11 = Interrupt
1	RXD	Rx endpoint data sink value 0 = Dual port memory buffer/DMA engine (default) This bit should always be cleared (0).
0	RXS	Rx endpoint stall value 0 = End point OK value 1 = End point stalled This bit will be cleared (0) automatically upon receipt of a SETUP request if this endpoint is configured as a control endpoint, and this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. This control will continue to STALL until this bit is either cleared (0) by the software or automatically cleared (0) as described above for control endpoints. Note (control endpoint types only): There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. in most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

0x125001FC+4*n USB1_HS_USB_OTG_HS_ENDPT_PIPE_IDn, n=[1..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x001F001F

The USB_OTG_HS_ENDPT_PIPE_IDn register is the endpoint pipe number register. There is an USB_OTG_HS_ENDPT_PIPE_IDn register for each endpoint in a device.

NOTE reset value of TX_PIPE_ID and RX_PIPE_ID is 0x1F, which means that Endpoint is not mapped to any pipe.

USB1_HS_USB_OTG_HS_ENDPT_PIPE_IDn

Bits	Name	Description
31:21	RESERVED_BITS31_21	Clear (0) these bits.
20:16	TX_PIPE_ID	This field indicate the pipe number that this tx end point (n) will use in pipe mode.
15:5	RESERVED_BITS15_5	Clear (0) these bits.
4:0	RX_PIPE_ID	This field indicate the pipe number that this rx end point (n) will use in pipe mode.

0x12500240 USB1_HS_USB_OTG_HS_PHY_CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0b1110000111010

The USB_OTG_HS_PHY_CTRL register is used to configure various features in the Synopsys 28nm PHY.

USB1_HS_USB_OTG_HS_PHY_CTRL

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12	USB2_PHY_IDHV_CLAMP_EN	Clamp enable for IDHV interrupt level shifter from USB VDD180 domain to VDDCX domain. When set (1), VLS is active and IDHV interrupt is translated from 1.8V domain to Vddcx domain. When clear (0), VLS is clamped high. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.
11	USB2_PHY_OTGSESSVLDHV_CLAMP_EN	Clamp enable for OTGSESSVLDHV interrupt level shifter from USB VDD180 domain to VDDCX domain. When set (1), VLS is active and OTGSESSVLDHV interrupt is translated from 1.8V domain to Vddcx domain. When clear (0), VLS is clamped to zero. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.

USB1_HS_USB_OTG_HS_PHY_CTRL (cont.)

Bits	Name	Description
10	PHY_MPM_HV_CLAMP_EN	Clamp enable for HV interrupts level shifters from USB VDD180 domain to VDDPAD MPM in usb2 phy wrapper. When set (1), VLS is active and HV interrupts are translated from 1.8V domain to MPM Vdd domain. When clear (0), VLS is clamped to inactive state. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.
9	USB2_PHY_OTGSESSVLD HV_INTEN	Enable HV session valid interrupt from phy. This interrupt translated with level shifter for wakeup from retention when VDDCX is nominal and TCXO is running.
8	USB2_PHY_IDHV_INTEN	Enable HV id pin interrupt from phy. This interrupt translated with level shifter for wakeup from retention when VDDCX is nominal and TCXO is running.
7	USB2_PHY_ULPI_POR	Reset for ULPI PHY Wrapper and ULPI clock domain logic in usb2_phy_wrapper.
6:4	USB2_PHY_FSEL	Reference Clock Frequency Select 011 (Assumes 19.2MHz default)
3	HOST_PORTCTRL_FORCE _SUSEN	Chicken bit for CR-0000153908 - when this bit set the core will enter to low power mode when portctrl host sm enter to suspend mode. Default value is 1.
2	USB2_PHY_SIDDQ	IDDQ Test Enable.
1	USB2_PHY_RETEN	Retention mode enable/disable
0	USB2_PHY_POR	Power-On-Reset (Analog configuration needs to happen before POR is set to 0)

0x12500244 USB1_HS_USB_OTG_HS_GENERIC1

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

The USB_OTG_HS_GENERIC1 register.

USB1_HS_USB_OTG_HS_GENERIC1

Bits	Name	Description
31:16	USB_HS_TX_DEPTH	TX_DEPTH is the number of words in the TX buffer. This number is calculated by the number of bytes allocated per Endpoint divided by 4, times the number of endpoints. The RAM width is 36. In HS USB this value is usually 512 bytes per EP, and for FS ONLY USB it is usually 64 Bytes per EP.
15:0	USB_HS_RX_DEPTH	RX_DEPTH is the number of words in the RX buffer. This number is usually 256, but can support powers of 2 up to 4096. The RAM width is 36.

0x12500248 USB1_HS_USB_OTG_HS_GENERIC2

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

The USB_OTG_HS_GENERIC2 register.

USB1_HS_USB_OTG_HS_GENERIC2

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.
15	USE_SPS_AHB2AHB	USE_SPS_AHB2AHB generic specifies if AHB2AHB bridge is connected between BAM and SPS Fabric AHB.
14	LPM_SUPPORT	The LPM_SUPPORT generic specifies if USB support Link Power Management.
13:9	USB_HS_DEV_EP	The number of USB endpoints. Valid values for the number of Endpoints are 4, 8, and 16
8:3	MAX_PIPES	The number of simultaneous parallel pipes supported by the BAM. Supported values are 2 to 30
2	USE_SPS	The USE_SPS generic specifies if Bam is connected to USB core.
1	USE_HSIC	The USE_HSIC generic specifies if an HSIC is connected to USB core.
0	UTMI_PHY_SW_IF_EN	The UTMI_PHY_SW_IF_EN generic specifies if UTMI phy Register Interface is enabled

0x12500250 USB1_HS_USB_OTG_HS_L1_EP_CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0000FFFF

The USB_OTG_HS_L1_EP_CTRL register enables/disables transition to L1 and exit from L1 state when specific TX endpoints are primed.

USB1_HS_USB_OTG_HS_L1_EP_CTRL

Bits	Name	Description
31:16	TX_EP_PRIME_L1_EXIT	Those bit's enables Remote Wakeup in L1 state when SW starts Priming The specific Endpoint.
15:0	TX_EP_PRIME_L1_EN	Control bit's that enables/disables transition to L1 when the specific TX Endpoint is active.

0x12500254 USB1_HS_USB_OTG_HS_L1_CONFIG

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_L1_CONFIG register is used to configure various L1 features.

USB1_HS_USB_OTG_HS_L1_CONFIG

Bits	Name	Description
31:12	RESERVED_BITS31_12	Clear (0) these bits.
11	PLL_PWR_DWN_EN	Control bit that enables/disables power down of 480 MHZ PLL in L1 state.
10	PHY_LPM_EN	Control bit that enable/disables entering ULPI Low Power Mode in L1 state
9	GATE_AHB_CLK_EN	Control bit that enable/disables clock request signaling for usb_ahb_clk in L1 state
8	GATE_FS_XCVR_CLK_EN	Control bit that enable/disables clock gating of usb_fs_xcvr_clk in L1 state
7	GATE_SYS_CLK_EN	Control bit that enable/disables clock gating of usb_system_clk in L1 state
6	GATE_XCVR_CLK_EN	Control bit that enable/disables power-down of 480 MHz PLL in L1 state
5	L1_REMOTE_WAKEUP_EN	Control bit that enables/disables Remote Wakeup in L1 state. When this bit is low, then Link Controller never initiates Remote Wakeup in L1 state. When this bit is high, Link Controller can initiate Remote Wakeup.
4	LPM_EN	Control bit that enables/disables LPM support. When this bit is zero a full backward compatibility is ensured - no LPM support and no response for LPM Extended Transaction
3:0	PLL_TURNOFF_MIN_HIRD	Specifying a minimum expected HIRD value from Host that enables HW mechanism for turning off the 480 MHz PLL. The default value is 50us.

0x12500258 USB1_HS_USB_OTG_HS_LPM_DEBUG_1

Type: Read/Clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_DEBUG_1 register is for debug and testing purposes mostly.

USB1_HS_USB_OTG_HS_LPM_DEBUG_1

Bits	Name	Description
31:16	DEBUG_L1_LONG_ENT_CNT	Count number of exits from L1 where duration in L1 is > 200us. Writing to this register clears the counter.
15:0	DEBUG_L1_SHORT_ENT_CNT	Count number of exits from L1 where duration in L1 is <= 200us. Writing to this register clears the counter.

0x1250025C USB1_HS_USB_OTG_HS_LPM_DEBUG_2

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_DEBUG_2 register is for debug and testing purposes mostly.

USB1_HS_USB_OTG_HS_LPM_DEBUG_2

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12:9	L1_RMT_WKUP_TIME	Read/write Specifying How much time the device drives remote wakeup. The default Value is 50us for reset value. Add the value of this register (in us) to the remote wakeup time.
8	L1_FPR	Read/write L1 Force port resume, The software sets (1) this bit to drive resume signaling.
7	HSIC_CLK_PLL_BYPASSNL	Read only. Disables PLL analog logic. Active low. Connects to bypassnl input of NT_PLL.
6	HSIC_CLK_PLL_RESET	Read only. Resets all FF in PLL. Active low. Connects to reset_n input of NT_PLL.
5	HSIC_CLK_GATE	Read only. Clock gating of hsic_clk and ulpi_clk, without turning off HSIC PLL.
4	FS_XCVR_CLK_GATE	Read only. Clock gating of cc_usb_xcvr_fs_clk
3	SYS_CLK_GATE	Read only. Clock gating of cc_usb_system_clk
2	AHB_CLK_GATE	Read only. Clock gating of usb_ahb_clk

USB1_HS_USB_OTG_HS_LPM_DEBUG_2 (cont.)

Bits	Name	Description
1	L1_STATE	Read only. Status bit indicating if Device is in L1 state. When this bit high, Link Controller and HSIC PHY are in L1 state
0	DEBUG_L1_EN	Read/write Control bit that enable/disables DEBUG counters operation.

0x12500260 USB1_HS_USB_OTG_HS_LPM_ATTRIBUTES

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_ATTRIBUTES register store the bmAttribute Field of the LPM transaction.

USB1_HS_USB_OTG_HS_LPM_ATTRIBUTES

Bits	Name	Description
31:5	RESERVED_BITS31_5	Clear (0) these bits.
4	BREMOTEWAKE	A value of one (1B) in this field enables the addressed device to wake the host upon any meaningful application-specific event (e.g. an interrupt for a device with one or more interrupt endpoints). A value of zero (0B) disables the device from initiating remote wake.
3:0	HIRD	Host Initiated Resume Duration.

20.27 SDC1 DML Registers (0x12400800 SDC1_DML_BASE)

This section contains the SDC1 DML registers.

The address field is a relative address. A base will be supplied by the SOC team and documented at the start of the chip SW Manual.

0x12400800 SDC1_DML_CONFIG

Type: Read/Write
Clock: HCLK
Reset State: 0x00010000

SW has the responsibility to set the CRCI SEL fields correctly when both Consumer and Producer sides are enabled at the same time. For example, setting both to 01 or setting both to 10 is an invalid setting if both producer and consumer sides are kicked off. The DML does NOT assume responsibility for incorrect setting of CRCI SEL fields and hence its function is not defined in such cases.

SDC1_DML_CONFIG

Bits	Name	Description
31:19	RESERVED31	reserved
18	INFINITE_CONS_TRANS	If set, this bit means the consumer transaction is of infinite size. Hence the transaction_end_rec signal from BAM will be ignored.
17	DIRECT_MODE	If set, DML is assumed to directly MASTER the AHB bus, in essence, no BAM or BAM is bypassed. This bit value is also routed to the direct_mode hardware port on the DML to be connected to BAM. See Direct_mode_BASE_addr register.
16	BYPASS	If set, the CRCI pairs will be passed through for legacy central DM support. The config AHB slave interface will be directly accessing the peripheral core for config, command and data movement functions. NOTE: The reset value of this bit is `1' which means the DML come out of PoReset in BYPASS state.
15:6	RESERVED15	reserved
5	PRODUCER_BLOCK_END_HPROT2	If set, DML drives high hprot[2] to BAM when block_end is high, else DML drives low hprot[2] to BAM when block_end is high
4	PRODUCER_TRANS_END_EN	When set, transaction_end signal is asserted at the end of DML transaction. When cleared, transaction_end signal is NOT asserted at the end of DML transaction. This feature allows to divide one BAM transaction to two Peripheral transactions.
3:2	CONSUMER_CRCI_SEL	When set to 00, Consumer side is Disabled When set to 01, CRCI-x pair is the consumer CRCI When set to 10, CRCI-y pair is the consumerCRCI If set to 11, its a invalid setting.

SDC1_DML_CONFIG (cont.)

Bits	Name	Description
1:0	PRODUCER_CRCI_SEL	When set to 00, Producer side is Disabled When set to 01, CRCI-x pair is the producer CRCI When set to 10, CRCI-y pair is the producer CRCI If set to 11, its a invalid setting.

0x12400804 SDC1_DML_STATUS

Type: Read
Clock: HCLK
Reset State: 0x00010001

SDC1_DML_STATUS

Bits	Name	Description
31:17	RESERVED31	reserved
16	CONSUMER_IDLE	0x0: Consumer is busy 0x1: Consumer is IDLE
15:1	RESERVED15	reserved
0	PRODUCER_IDLE	0x0: Producer is busy 0x1: Producer is IDLE

0x12400808 SDC1_DML_SW_RESET

Type: Write
Clock: HCLK
Reset State: 0x00000000

A write to this register resets the DML core. All internal state information will be lost and all register values will be reset as well.

SDC1_DML_SW_RESET

Bits	Name	Description
31:0	RESERVED	reserved

0x1240080C SDC1_DML_PRODUCER_START

Type: Write
Clock: HCLK
Reset State: 0x00000000

A write to this register triggers the DML's Producer state machine. No SW register values will be altered. Only the internal counters and settings related to Producer activity will be reset and started afresh. This register should be written to after POR to kick off producer side. This register should also be used to restart the producer once it has reached IDLE state (as indicated by the STATUS register) after completing the current transaction.

SDC1_DML_PRODUCER_START

Bits	Name	Description
31:0	RESERVED	reserved

0x12400810 SDC1_DML_CONSUMER_START

Type: Write
Clock: HCLK
Reset State: 0x00000000

A write to this register triggers the DML's consumer state machine. No SW register values will be altered. Only the internal counters and settings related to consumer activity will be reset and started afresh. This register should be written to after POR to kick off consumer side. This register should also be used to restart the consumer once it has reached IDLE state (as indicated by the STATUS register) after completing the current transaction..

SDC1_DML_CONSUMER_START

Bits	Name	Description
31:0	RESERVED	reserved

0x12400814 SDC1_DML_PRODUCER_PIPE_LOGICAL_SIZE

Type: Write/Read
Clock: HCLK
Reset State: 0x00000000

This register holds the size of the producer pipe (in units of bytes) _to_ which the peripheral can keep writing data to when its the PRODUCER. The value of this register should be consistent with what the BAM registers are programmed with as well. The DML in response to producer side CRCI requests starts writing out data (generated by the Peripheral) from address 0x0 (on its AHB Master Interface). For subsequent Producer side data accesses, the DML keeps on incrementing the address. Upon reaching the max value as indicated by this register, the address rolls over back to 0x0. The address also rolls over back to 0x0 after reaching the end of a transaction.

This register value decides the range of addresses seen on the DML AHB Master address bus during Producer activity.

The value of this register is restricted to any power of two and greater than or equal to the Producer BAM Block Size setting. This is to avoid DML overwriting its own data in the pipe as the data is not committed until block_end is received by the BAM.

The recommended value for this register is 4096(decimal)

SDC1_DML_PRODUCER_PIPE_LOGICAL_SIZE

Bits	Name	Description
31:16	RESERVED31	reserved31
15:0	PRODUCER_LOGICAL_SIZE	The size of the producer pipe (in units of bytes) to which a producer peripheral can keep writing the data it produces.

0x12400818 SDC1_DML_CONSUMER_PIPE_LOGICAL_SIZE

Type: Write/Read
Clock: HCLK
Reset State: 0x00000000

This register holds the size of the consumer pipe (in units of bytes) _from_ which the peripheral can keep _reading_ data from when its the CONSUMER. The value of this register should be consistent with what the BAM registers are programmed with as well. The DML in response to consumer side CRCI requests starts reading out data (needed by the Peripheral) from address 0x0 (on its AHB Master Interface). For subsequent consumer side data accesses, the DML keeps on incrementing the address. Upon reaching the max value as indicated by this register, the address rolls over back to 0x0. The address also rolls over back to 0x0 after reaching the end of a transaction.

This register value decides the range of addresses seen on the DML AHB Master address bus during consumer activity.

The value of this register is restricted to any power of two and no smaller than 32 bytes, that is, no smaller than a "beat-8" burst on a 32 bit AHB.

The recommended value for this register is 4096(decimal)

SDC1_DML_CONSUMER_PIPE_LOGICAL_SIZE

Bits	Name	Description
31:16	RESERVED31	reserved31
15:0	CONSUMER_LOGICAL_SIZE	The size of the consumer pipe (in units of bytes) to which a consumer peripheral can keep reading the data from it needs.

0x1240081C SDC1_DML_PIPE_ID

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register holds pipe IDs that services the producer and consumer side of the peripheral.

- The producer pipe ID is fed to the BAM when servicing the producer side of the peripheral.
- The consumer pipe ID is fed to the BAM when servicing the consumer side of the peripheral.
- The DML also uses this ID value to look into the appropriate side band signals from BAM like pipe_empty, pipe_full etc before initiating the said AHB transaction.

SDC1_DML_PIPE_ID

Bits	Name	Description
31:21	RESERVED31	reserved
20:16	CONSUMER_PIPE_ID	consumer pipe ID
15:5	RESERVED15	reserved
4:0	PRODUCER_PIPE_ID	producer pipe ID

0x12400820 SDC1_DML_PRODUCER_TRACKERS

Type: Read
Clock: HCLK
Reset State: 0x00000000

.This register is for debug purposes only. They reflect the value of the producer block and transaction counters when read. The values may be dynamically changing when a transaction is in progress.

SDC1_DML_PRODUCER_TRACKERS

Bits	Name	Description
31:16	PROD_TRANS_CNT	Value of the 16bit tracker tracking the Producer Transaction Count for the current transaction. Should read 0 at the end of the transaction.
15:0	PROD_BLOCK_CNT	Value of the 16 bit tracker that tracks the Producer Block Count. Need not be zero at the end of transaction.

0x12400824 SDC1_DML_PRODUCER_BAM_BLOCK_SIZE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register holds the "block" size, in units of bytes, associated with the Producer BAM. The DML asserts the block_end side band signal to the BAM whenever the producer side of the peripheral has generated the said amount of data. This register value should be an integral multiple of the Producer CRCI Block Size.

Legal values for Producer BAM Block Size are 64, 128, 192, 256, 512, 1024, 2048 and 4096.

The recommended value for this register is 512(decimal)

SDC1_DML_PRODUCER_BAM_BLOCK_SIZE

Bits	Name	Description
31:16	RESERVED	reserved
15:0	PRODUCER_BLK_SIZE	Size of the one "block" on the producer side in units of bytes.

0x12400828 SDC1_DML_PRODUCER_BAM_TRANS_SIZE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register holds the "transaction" size, in units of bytes, associated with the Producer BAM. The DML asserts the transaction_end side band signal to the BAM whenever the producer side of the peripheral has generated the said amount of data. This signal is asserted only during the address phase of the AHB transaction that carries the last byte corresponding to the size mentioned in this register. Once this value is reached for a given transaction, the address for subsequent data access rolls back to 0x0 and all the block size, CRCI size and transaction size counters also get reset to 0 and start all over again. A value of zero in this register during a producer transaction start means infinite size transaction and hence transaction_end may not get asserted.

This value can be anything up to a maximum of 4294967295 bytes (4 GB -1). If this register value is zero when the DML is started, then an infinite transaction size is assumed. No transaction_end will be generated.

SDC1_DML_PRODUCER_BAM_TRANS_SIZE

Bits	Name	Description
31:0	PRODUCER_TRANS_SIZE	Size of the one "transaction" on the producer side in units of bytes or if zero, then infinite transaction size assumed.

0x1240082C SDC1_DML_DIRECT_MODE_BASE_ADDR

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

This register is used whenever the DIRECT_MODE bit in config register is set. The programmed 16bits will be used as DML AHB Master address bus MSBits for consumer (AHB read) and producer (AHB Write) operations. The lower 16bits would be dictated by the pipe logical size register.

SDC1_DML_DIRECT_MODE_BASE_ADDR

Bits	Name	Description
31:16	CONSUMER_BASE_ADDR	used as AHB Master address (31:16) when doing direct mode consumer operations if direct_mode bit is set.
15:0	PRODUCER_BASE_ADDR	used as AHB Master address (31:16) when doing direct mode producer operations if direct_mode bit is set.

0x12400830 SDC1_DML_DEBUG

Type: Write/Read
Clock: HCLK
Reset State: 0x00000000

Enables Test Bus of the DML and also selects which side signals to drive the test bus with.

SDC1_DML_DEBUG

Bits	Name	Description
31:2	RESERVED	reserved
1	STATUS_2_SEL	If set, selects the set of signals listed out in DML_BAM_SIDE_STATUS_2 register onto Test bus, else selects set of signals listed out in DML_BAM_SIDE_STATUS_1 register to be muxed onto test bus. Valid only if bit 0 is set.
0	TESTBUS_EN	0x0: Disable Test Bus 0x1: Enable Test Bus

0x12400834 SDC1_DML_BAM_SIDE_STATUS_1

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the instantaneous value of the side band signals with BAM.

SDC1_DML_BAM_SIDE_STATUS_1

Bits	Name	Description
31:24	RESERVED31	reserved
23	ACK_ON_SUCCESS_TOGGLE	for selected consumer pipe
22	ACK_BYTES_AVAIL_TOGGLE	for selected consumer pipe
21	PIPE_BYTES_AVAIL_TOGGLE	for selected consumer pipe
20	TRANSACTION_END_REC	transaction end received for selected consumer pipe.
19	PIPE_BYTES_FREE_TOGGLE	bytes free toggle signal for selected producer pipe
18:3	PIPE_BYTES_FREE	bytes free value for selected producer pipe
2	MESSAGING_ONLY	DML output status
1	TRANSACTION_END	DML output status
0	BLOCK_END	DML output status

0x12400838 SDC1_DML_BAM_SIDE_STATUS_2

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the instantaneous value of the side band signals with BAM.

SDC1_DML_BAM_SIDE_STATUS_2

Bits	Name	Description
31:16	ACK_ON_SUCCESS_TOGGLE_SIZE	for selected consumer pipe
15:0	PIPE_BYTES_AVAIL	for selected consumer pipe

0x1240083C SDC1_DML_RTL_GENERICS_1

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the value of the RTL Generics set during the integration of the DML into a SPS Wrapper or other entity.

SDC1_DML_RTL_GENERICS_1

Bits	Name	Description
31:17	RESERVED31	reserved
16:11	PERIPHERAL_ADDR_WIDTH	represents the width set (in binary format)
10:6	MAX_PIPES	represents the number of pipe value set (in binary format)
5:3	CONSUMER_CRCI_BLK	101:.256 bytes 0x0: 16 bytes 0x1: 32 bytes 0x2: 64 bytes 0x3: 128 bytes 0x4: 192 bytes
2:0	PRODUCER_CRCI_BLK	101:.256 bytes 0x0: 16 bytes 0x1: 32 bytes 0x2: 64 bytes 0x3: 128 bytes 0x4: 192 bytes

0x12400840 SDC1_DML_RTL_GENERICS_2

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the value of the PROD_DMR_RD_ADDR Generic set in RTL during the integration of the DML into a SPS Wrapper or other entity.

SDC1_DML_RTL_GENERICS_2

Bits	Name	Description
31:0	PROD_RD_DMR_ADDR	32bit Value of the PROD_DMR_RD_ADDR generic

0x12400844 SDC1_DML_RTL_GENERICS_3

Type: Read
Clock: HCLK
Reset State: 0xXXXXXXXX

Reflects the value of the CONS_DMR_WR_ADDR Generic set in RTL during the integration of the DML into a SPS Wrapper or other entity.

SDC1_DML_RTL_GENERICS_3

Bits	Name	Description
31:0	CONS_WR_DMR_ADDR	32bit Value of the CONS_DMR_WR_ADDR generic

0x12400848 SDC1_DML_INTERRUPT_ENABLE

Type: Read/Write
Clock: HCLK
Reset State: 0x00000000

SDC1_DML_INTERRUPT_ENABLE

Bits	Name	Description
31:1	RESERVED31	reserved
0	PROD_IDLE_START_INTR_EN	Enable DML to generate an interrupt when PRODUCER enters an IDLE state.

0x1240084C SDC1_DML_INTERRUPT_CLEAR

Type: Write
Clock: HCLK
Reset State: 0xXXXXXXXX

SDC1_DML_INTERRUPT_CLEAR

Bits	Name	Description
31:1	RESERVED31	reserved
0	PROD_IDLE_START_INTR_CLR	Clear PROD_IDLE_START_INTR interrupt.

20.28 SDC1 BAM Registers (0x12402000 SDC1_BAM_BASE)

BAM supports only Word (4 byte) aligned writes and reads on the Configuration Bus interface.

BAM has MAX_PIPES hardware generic parameter defining the number of pipes it supports. Each BAM can have up to 31 pipes supported.

BAM has BAM_CONF_AHBS_ADDR_WIDTH hardware generic parameter defining the Bit Number for selecting BAM access or Peripheral access. Legal Ranges are 14 to 20. Count starts from 1, meaning a value of 17 will set BAM Base address as 0x0001_0000.

20.28.1 BAM control registers

BAM Control registers configure the BAM operational state, SW reset, interrupts and others.

0x12402F80 SDC1_BAM_CTRL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

BAM Control register allows global controls for the BAM.

SDC1_BAM_CTRL

Bits	Name	Description
31:17	RESERVED_BITS31_17	Set to Zero (0)
16	IBC_DISABLE	This Bit enables power saving by disabling the inactivity clock timer/counter. This is useful when: 1) The BAM is Enabled but idling for long periods. 2) The BAM is Enabled and running but the inactivity timers/counters are not required by the SW for operating the BAM. When the BAM is Disabled, it automatically shuts down those timers to save power. 1’b1 - Enable Power Saving Mode 1’b0 - Disable Power Saving Mode
15	BAM_CACHED_DESC_STORE	This Bit enables storage of a cached Descriptor into RAM when doing Context Switch and loading it back when returning to this pipe. This is relevant for System Modes Only. BAM to BAM Consumer mode doesn't have this option. Enabling this makes the Context Switch process slightly longer but reduces AHB Descriptor Fetch time later on. It also reduces the number of descriptor fetches done by the BAM if BAM is treating more than 2 pipes. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only

SDC1_BAM_CTRL (cont.)

Bits	Name	Description
14:13	BAM_DESC_CACHE_SEL	This Selector chooses which Descriptor Caching mode will be used. This is relevant for System Producer or Consumer modes only. 2'b00 - Cache when current descriptor has less than 64 bytes left. 2'b01 - Cache when current descriptor has less than 128 bytes left. 2'b10 - Immediate Auto cache - cache will happen whenever there are no descriptors cached. This might cause unnecessary descriptors reads when switching between more than 2 pipes. It is the most effective when each pipe processes more bytes than there are in an average descriptor (small descriptors, big block size), or when working with 2 or less pipes. 2'b11 - Cache when descriptor is needed only. This results in 1 descriptor present in cache at most. Available in BAM only
12	RESERVED_BITS12	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_SIC_SEL
11:5	BAM_TESTBUS_SEL	Set to Zero (0) Obsolete field: BAM_TESTBUS_SEL Test Bus selector. Supported until (including) bam_p3q3r29 (BlackBird). Moved to a dedicated register - BAM_TEST_BUS_SEL in the following releases.
4	BAM_EN_ACCUM	When Enabled, BAM will accumulate data written by the peripheral in Direct Mode into INCR8 Bursts. This is an optimization feature for Producer Direct Mode cases. 1'b1 - Enabled 1'b0 - Disabled Available in BAM only
3	RESERVED_BITS3	Set to Zero (0)
2	RESERVED_BITS2	Set to Zero (0)
1	BAM_EN	After reset the BAM wakes up in Disabled Mode. While Disabled, BAM operates in Legacy mode (all the transfers from the peripheral go around the BAM as if it doesn't exist) Software Enables this bit to allow BAM operation. This bit doesn't affect the PIPE enable bit in BAM_P_CTRL register. The only possibility to Disable the BAM after it has been enabled is by Hardware or Software reset. 1'b1 - Enabled 1'b0 - Disabled

SDC1_BAM_CTRL (cont.)

Bits	Name	Description
0	BAM_SW_RST	This will reset the BAM & all Pipes. Software may use this to reset the BAM. As long as the bit remains high the BAM remains in reset state. Software should clear this bit 1'b1 - Reset state 1'b0 - Normal state

0x12402F84 SDC1_BAM_REVISION

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a hard coded revision number of the BAM RTL. This corresponds to the BAM target number in the IMS. Also additional BAM settings are reflected here.

SDC1_BAM_REVISION

Bits	Name	Description
31:24	INACTIV_TMR_BASE	This indicates the width of the inactivity timers base counter
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	NUM_INACTIV_TMRS	This bit is checked only if INACTIV_TMRS_EXST = 1. This bit indicates how many inactivity timers are implemented according to value of INACTIVITY_TIMERS_SUPPORTED generic: 1'b1 - One timer for global BAM activity (INACTIVITY_TIMERS_SUPPORTED = 1) 1'b0 - MAX_PIPES timers for each pipe activity (INACTIVITY_TIMERS_SUPPORTED = 2)
19	INACTIV_TMRS_EXST	This indicates BAM has inactivity timers. 1'b1 - Timers available (INACTIVITY_TIMERS_SUPPORTED = 1 or 2) 1'b0 - No timers available (INACTIVITY_TIMERS_SUPPORTED = 0)
18	HIGH_FREQUENCY_BAM	This indicates BAM has Double Sampling on the Ack On Success interface. 1'b1 - Ack On Success double sampled 1'b0 - No double sampling of Ack On Success
17	BAM_HAS_NO_BYPASS	This field indicates BAM has no bypass on the AHB Data bus, from the Peripheral AHB Master to the fabric. When Bypass is available, it is the default routing when BAM is disabled. 1'b1 - No Bypass 1'b0 - Bypass Exists

SDC1_BAM_REVISION (cont.)

Bits	Name	Description
16	SECURED	This field indicates BAM/BAM-Lite has security support (APU inside) 1'b1 - Secured 1'b0 - Not Secured
15:12	RESERVED_BITS15_12	Set to Zero (0)
11:8	NUM_EES	This indicates the Number of Interrupt Lines (Execution Environments) supported by the BAM. When 1 EE is supported, only the BAM_IRQ_SRCS*_EE0 registers exist. When 4 EEs are supported, all BAM_IRQ_SRCS*_EEn registers exist for n=[0..3].
7:0	REVISION	This field contains the revision number of the core, Hard Coded. 8'h01 - Voyager (bam_p3q3r22 +) 8'h02 - BlackBird (bam_p3q3r27 +) 8'h03 - Waverider BAM (bam_p3q3r30 +) 8'h04 - Aurora BAM (bam_p3q2r43 +) 8'h05 - Shelby BAM (bam_p2q2r45 +) 8'h10 - Waverider BAM Lite (bam_lite_p1q1r0 +) 8'h11 - Aurora BAM Lite (bam_lite_p3q2r16 +) 8'h12 - Shelby BAM Lite (bam_lite_p2q2r18 +)

0x12402FBC SDC1_BAM_NUM_PIPES

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a the hard coded number of pipes in the BAM. Since each BAM may have a different number of pipes instantiated in HW, this register allows the SW to know this parameter. The reset state value doesn't have any meaning in this register since it is a constant.

SDC1_BAM_NUM_PIPES

Bits	Name	Description
31:24	BAM_NON_PIPE_GRP	This field contains the number of BAM Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
23:16	PERIPH_NON_PIPE_GRP	This field contains the number of Peripheral's Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
15:8	RESERVED_BITS15_8	Set to Zero (0)
7:0	BAM_NUM_PIPES	This field contains the number of pipes available in this BAM

0x12402FC0 SDC1_BAM_TIMER

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the BAM (all the pipes are in idle state).

SDC1_BAM_TIMER

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12402FC4 SDC1_BAM_TIMER_CTRL

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The register can be written and read only when INACTIVITY_TIMERS_SUPPORTED generic equals to 1.

The resolution of the BAM inactivity timer are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * TIMER_TRSHLD.

SDC1_BAM_TIMER_CTRL

Bits	Name	Description
31	TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1 to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	TIMER_RUN	Will be used along with TIMER_MODE Not implemented at this time. Set to zero(0)
29	TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12402F88 SDC1_BAM_DESC_CNT_TRSHLD

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds a threshold value for the counter summing the Size of the Descriptors Provided. This value is Global for all pipes but it is relevant for System Producer BAM mode and Both Consumer modes, where Descriptors summing takes place in order to provide the information to the peripheral via pipe bytes free (producer) or pipe bytes available interfaces.

SDC1_BAM_DESC_CNT_TRSHLD

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0).
15:0	CNT_TRSHLD	Threshold value. The maximum allowed value is 32kByte. Available in BAM only

0x12402F8C SDC1_BAM_IRQ_SRCS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking out this register, SW

reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register points to the physical BAM_IRQ_SRCS_EE0 register.

SDC1_BAM_IRQ_SRCS

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12402F90 SDC1_BAM_IRQ_SRCS_MSK

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register points to the physical BAM_IRQ_SRCS_MSK_EE0 register.

SDC1_BAM_IRQ_SRCS_MSK

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12402FB0 SDC1_BAM_IRQ_SRCS_UNMASKED

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register points to the physical BAM_IRQ_SRCS_UNMASKED_EE0 register.

SDC1_BAM_IRQ_SRCS_UNMASKED

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

0x12402F94 SDC1_BAM_IRQ_STTS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only.

Clearing the interrupt bits is done by writing to BAM_IRQ_CLR register.

SDC1_BAM_IRQ_STTS

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
3	BAM_EMPTY_IRQ	This interrupt is for DEBUG purpose only. It should not be used in normal SW flows. The interrupt indicates the BAMs buffer is empty. This bit can become high only when BAM_DATA_ERASE or BAM_DATA_FLUSH is high in BAM_TEST_BUS_SEL register.
2	BAM_ERROR_IRQ	This Indicates a Fatal Error has happened in the BAM. Currently this might happen due to an UnSuccessful Pipe Reset operation.
1	BAM_HRESP_ERR_IRQ	This interrupt Indicates that an Erroneous HResponse has been received by the AHB Master. Additional Information about the error may be read at BAM_AHB_MASTER_ERR_* Registers. Clearing this interrupt also clears the BAM_AHB_MASTER_ERR_* Registers. Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12402F98 SDC1_BAM_IRQ_CLR

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

SDC1_BAM_IRQ_CLR

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
3	BAM_EMPTY_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM-Lite only
2	BAM_ERROR_CLR	1'b1 - Clear 1'b0 - Unchanged
1	BAM_HRESP_ERR_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12402F9C SDC1_BAM_IRQ_EN

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the BAM Interrupt Status register.

SDC1_BAM_IRQ_EN

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_EN	Enables Inactivity timer interrupt by writing this bit 1'b1 - Enable 1'b0 - Disable
3	BAM_EMPTY_EN	1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only

SDC1_BAM_IRQ_EN (cont.)

Bits	Name	Description
2	BAM_ERROR_EN	1'b1 - Enable 1'b0 - Disable
1	BAM_HRESP_ERR_EN	1'b1 - Enable 1'b0 - Disable Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12402FA0 SDC1_BAM_RESERVED_1

Type: Read
Clock: BAM_CLK
Reset State: 0x00000000

SDC1_BAM_RESERVED_1

Bits	Name	Description
31	RESERVED_BITS31	Set to Zero (0) Obsolete field: BAM_IRQ_SIC_SEL
30:0	RESERVED_BITS30_0	Set to Zero (0) Obsolete field: P_IRQ_SIC_SEL

0x12402FA4 SDC1_BAM_AHB_MASTER_ERR_CTRLS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

SDC1_BAM_AHB_MASTER_ERR_CTRLS

Bits	Name	Description
31:23	RESERVED_BITS31_16	Set to Zero (0)
22:18	BAM_ERR_HVMID	HVMID

SDC1_BAM_AHB_MASTER_ERR_CTRLS (cont.)

Bits	Name	Description
17	BAM_ERR_DIRECT_MODE	DIRECT MODE
16:12	BAM_ERR_HCID	HCID
11:8	BAM_ERR_HPROT	HPROT
7:5	BAM_ERR_HBURST	HBURST
4:3	BAM_ERR_HSIZE	HSIZE
2	BAM_ERR_HWRITE	HWRITE
1:0	BAM_ERR_HTRANS	HTRANS

0x12402FA8 SDC1_BAM_AHB_MASTER_ERR_ADDR

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

SDC1_BAM_AHB_MASTER_ERR_ADDR

Bits	Name	Description
31:0	BAM_ERR_ADDR	HADDR

0x12402FAC SDC1_BAM_AHB_MASTER_ERR_DATA

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

SDC1_BAM_AHB_MASTER_ERR_DATA

Bits	Name	Description
31:0	BAM_ERR_DATA	HDATA

0x12402FB4 SDC1_BAM_RESERVED_2

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

SDC1_BAM_RESERVED_2

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_IRQ_DEST_ADDR

0x12402FB8 SDC1_BAM_RESERVED_3

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

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SDC1_BAM_RESERVED_3

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_DEST_ADDR

0x12402FF0 SDC1_BAM_TRUST_REG

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside - SECURED field in the BAM_REVISION register) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

SDC1_BAM_TRUST_REG

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_VMID	Those bits indicate the VMID value to be used when performing BAM type accesses to the bus. BAM Type accesses include BAM MTI (or Direct Mode accesses, not applicable for BAM Lite)
7	BAM_RST_BLOCK	When enabled, the BAM Global SW reset will not be available for usage. This is in order to deny Global SW reset requests by the Global security group. 1'b1 - Enable 1'b0 - Disable
6:2	RESERVED_BITS6_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_EE	This Field Indicates the EE (0,1,2,3) to which the BAM Interrupt belongs to. The pipe interrupts will fire on the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12402FF4 SDC1_BAM_TEST_BUS_SEL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This is the testbus selector register.

Supported in releases after bam_p3q3r29 (BlackBird).

SDC1_BAM_TEST_BUS_SEL

Bits	Name	Description
31:19	RESERVED_BITS31_19	Set to Zero (0)
18	BAM_DATA_ERASE	When enabled, BAM will be instructed to erase all the data it currently has inside. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Erase 1'b0 - Disabled
17	BAM_DATA_FLUSH	When enabled, BAM will be instructed to flush all the data it currently has inside. BAM will only flush the data once it has enough data and a valid destination for it. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Flush 1'b0 - Disabled
16	BAM_CLK_ALWAYS_ON	This bit controls the BAM to issue 'always on' clock request. 1'b1 - Enable Always On clock request. 1'b0 - Disabled
15:7	RESERVED_BITS15_7	Set to Zero (0)
6:0	BAM_TESTBUS_SEL	Test Bus selector. Values with bit[11] set high are reserved for the BAM Lite integrator to provide testbus from outside of the BAM Lite. For example, eDML testbus may reside at X'100_0000' to X'111_1111' selector values. eDML has no registers thus has no test bus selector, so its test bus is combined with the BAM lite's. BAM provides zeroes on its testbus when external values selected. X'000_0000' - Zeros X'000_0001' - Slave test bus X'000_0010' - Pipe state machine test bus X'000_0011' - Buffer test bus X'000_0100' - Sideband test bus X'000_1101' - Bus Manager test bus X'001_0000' - Reg file test bus X'1''_''''' - BAM Lite sets zeroes on the test bus, leaving it for external use

0x12402FF8 SDC1_BAM_TEST_BUS_REG

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the value being output to the testbus of the chip. It is not intended for SW usage but for lab debugging of the BAM. Values here can change every cycle.

SDC1_BAM_TEST_BUS_REG

Bits	Name	Description
31:0	BAM_TESTBUS_REG	32 bit Testbus value. To select the Block in BAM to show here, use the BAM_TESTBUS_SEL field in BAM_CTRL register.

0x12402FFC SDC1_BAM_CNFG_BITS

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM configuration bits for bug fixes. It is highly recommended to follow the directions for each bit and set it accordingly.

SDC1_BAM_CNFG_BITS

Bits	Name	Description
31:27	RESERVED_BITS31_27	Set to Zero (0)
26	BAM_AU_ACCUMED	Recommended value: 1 This bit fixes a bug in the Ack Update state machine, where an overflow happened while counting descriptors and reaching more than 64kB of calculated sizes. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only
25	BAM_PSM_P_HD_DATA	Recommended value: 1 This bit allows pipe state machine to ignore retransmission requests if a pipe has just been initialized and process those as a regular fetch request. (consumer modes only). When this bit disabled, BAM could fetch descriptors for a pipe which was reset and no descriptors were added yet, if a retransmission request followed after the reset. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only

SDC1_BAM_CNFG_BITS (cont.)

Bits	Name	Description
24	BAM_REG_P_EN	Recommended value: 1 This bit fixes the pipe configuration signals mux for the current active pipe in 2 pipes BAM. When disabled, internal state machines might get into enabled states while the pipe is disabled. This would typically happen after pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
23	BAM_WB_DSC_AVL_P_RST	Recommended value: 1 This bit allows the Writeback state machine to reset the vector indicating there are available descriptors when a pipe reset occurs. If disabled, BAM might fetch descriptors after resetting and reconfiguring a pipe, even though no Event (descriptors) was provided.. 1'b1 - Enable 1'b0 - Disable Available in BAM only
22	BAM_WB_RETR_SVPNT	Recommended value: 1 This bit fixes a bug where a pipe which was reset, still stored its retransmission savepoint, but into the illegal's pipe address space, thus hurting the last pipe of the BAM if the BAM had a total 4, 8 or 16 pipes. This is relevant for Producer to System modes only. (CR-0000151585) 1'b1 - Enabled 1'b0 - Disable Available in BAM only
21	BAM_WB_CSW_ACK_IDL	Recommended value: 1 This bit allows the Writeback state machine to switch into idle state prior to visiting disabled state. This is needed when context switching from mode X to another pipe of mode X is well. This is required to fix a bug in the 2 pipes BAM. 1'b1 - Enable 1'b0 - Disable Available in BAM only
20	BAM_WB_BLK_CSW	Recommended value: 1 When Enabled, this bit does not allow context switch to happen in the Writeback state machine until it has created a descriptor. This is relevant when the descriptor fifo is becoming full and there's no space to create a descriptor, while another pipe is context switching. This might result in the descriptor not to be created ever, if it was the last one for that pipe. Relevant for Producer BAM-to-BAM mode only. 1'b1 - Enable 1'b0 - Disable Available in BAM only

SDC1_BAM_CNFG_BITS (cont.)

Bits	Name	Description
19	BAM_WB_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Writeback state machine when performing pipe reset. 1'b1 - 1'b0 - Disable Available in BAM only
18	BAM_SI_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Sideband Inform state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
17	BAM_AU_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Ack Update state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
16	BAM_PSM_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Pipe state machine when performing pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
15	BAM_PSM_CSW_REQ	Recommended value: 1 This bit forces the context switch request from pipe state machine to RAM controller not to last longer than the slave requested. (2 Pipes BAM bug fix) 1'b1 - Enable 1'b0 - Disable Available in BAM only
14	BAM_SB_CLK_REQ	Recommended value: 1 This bit allows the clock request from the sideband block to propagate into the BAM's common clock request. 1'b1 - Propagate Sideband Clock Request 1'b0 - Disable Available in BAM only
13	BAM_IBC_DISABLE	Recommended value: 1 This bit helps to save power by allowing the BAM to keep the inactivity base counter in reset when BAM is disabled or when SW configures IBC_DISABLE bit high. 1'b1 - Enable Power Saving 1'b0 - Disable Power Saving

SDC1_BAM_CNFG_BITS (cont.)

Bits	Name	Description
12	BAM_NO_EXT_P_RST	Recommended value: 1 This bit allows the BAM / BAM Lite to ignore the externally connected blocks (eDML) when doing pipe reset. The BAM, once instructed to pipe reset, first thing lets the externally connected block know a reset is needed. Then it waits for the externally connected block to Acknowledge it is ready for the pipe reset (meaning it doesn't push any data for the reset pipe) and then the BAM Lite completes the pipe reset operation internally. When disabled, the BAM doesn't require any Acknowledge from the external block to perform pipe reset. 1’b1 - Enable external block pipe reset 1’b0 - Disable - ignore external block pipe reset
11	BAM_FULL_PIPE	Recommended value: 0 This enables the BAM support for a BAM to BAM Producer which insists to write to a full pipe. When 0, BAM might issue data overflow if producers write to a full pipe. When 1 BAM will not allow this and lower HReady when peripheral tries to do so. Once space is freed in the pipe, Hready will rise and the flow will continue. This functionality has been found to be buggy and was removed from APQ8064. Bit is currently unused. 1’b1 - Enable 1’b0 - Disable Available in BAM only
10:4	RESERVED_BITS10_4	Set to Zero (0)
3	BAM_ADML_SYNC_BRIDGE	0x1: Use a Synchronous Configuration bridge in aDML. 0x0: Use a Asynchronous Configuration bridge in aDML.
2	BAM_PIPE_CNFG	Recommended value: 1 Pipe SM upgrade for writing EOT bit to the previous descriptor. It’s invoked only when EOB arrives in the end of a descriptor. It is highly recommended to set this bit high. Leaving it low might cause incorrect Pipe Bytes Free value reported to peripheral in rare cases. 1’b1 - Enable 1’b0 - Disable Available in BAM only
1	BAM_ADML_DEEP_CONS_FIFO	0x1: Use a deep Consumer FIFO in aDML (16 dwords) 0x0: Use a shallow Consumer FIFO in aDML (8 dwords)
0	BAM_ADML_INCR4_EN_N	0x1: Don’t allow INCR4 aDML-BAM accesses. 0x0: Allow INCR 4 aDML-BAM accesses.

0x12403800+ 128*n SDC1_BAM_IRQ_SRCS_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register has an alias - BAM_IRQ_SRCS register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

SDC1_BAM_IRQ_SRCS_EEn

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12403804+ 128*n SDC1_BAM_IRQ_SRCS_MSK_EEn, n=[0..3]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register has an alias - BAM_IRQ_SRCS_MSK register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

SDC1_BAM_IRQ_SRCS_MSK_EEn

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12403808+ 128*n SDC1_BAM_IRQ_SRCS_UNMASKED_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register has an alias - BAM_IRQ_SRCS_UNMASKED register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

SDC1_BAM_IRQ_SRCS_UNMASKED_EEn

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

20.28.2 BAM PIPE management registers

BAM Pipe management registers control each pipe's parameters. Those reside in physical registers.

0x12402000+ 128*n SDC1_BAM_P_CTRLn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Control register provides various controls for the pipe.

SDC1_BAM_P_CTRLn

Bits	Name	Description
31:11	RESERVED_BITS31_11	Set to Zero (0)
10:9	P_PREFETCH_LIMIT	Bam Lite feature Selects the number of bytes to be pre-fetched by the Bam Lite, once a peripheral requests to read data from a pipe. This feature is relevant for Consumer modes only. 2'b00 - 32 bytes at most (INCR8) 2'b01 - 16 bytes at most (INCR4) 2'b10 - 4 bytes at most (SINGLE) Available in BAM-Lite only

SDC1_BAM_P_CTRLn (cont.)

Bits	Name	Description
8:7	P_AUTO_EOB_SEL	Bam Lite feature. Selects the number of bytes to be processed before creating End Of Block indication internally by the BAM. See P_AUTO_EOB. Descriptors generated by this feature (bam to bam producer mode) will always be of the chosen size, unless an End Of Transfer, causes a smaller descriptor to be created. 2'b00 - 512 Bytes 2'b01 - 256 Bytes 2'b10 - 128 Bytes 2'b11 - 64 Bytes Available in BAM-Lite only
6	P_AUTO_EOB	BAM Lite feature. When Enabled, the BAM Lite will ignore any incoming End Of Block indications from the peripheral (if any). Instead, the BAM Lite will generate it's own End Of Block indications internally, every P_AUTO_EOB_SEL bytes. This feature is relevant for Producer Bam 2 Bam modes only. It is a must for peripherals which are not able to produce End Of Block indications. 1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
5	P_SYS_MODE	This bit sets the pipe to work in System Mode, where the Software is the second side of the pipe. 1'b1 - System mode. 1'b0 - BAM to BAM mode.
4	P_SYS_STRM	Streaming Enable. Relevant to System Producer BAM mode only.When enabled, BAM will not close descriptors with End Of Transfer notifications received from peripheral, but continue writing the data to the same descriptor. 1'b1 - Enable Streaming Mode 1'b0 - None-Streaming Mode
3	P_DIRECTION	This bit denotes pipe direction. 1'b1 - The pipe can be written (producer mode) 1'b0 - The pipe can be read (consumer mode)
2	RESERVED_BITS2	Set to Zero (0)
1	P_EN	1'b1 - Enable Pipe 1'b0 - Disable Pipe
0	RESERVED_BITS0	Set to Zero (0)

0x12402004+ 128*n SDC1_BAM_P_RSTn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Reset register provides Pipe Reset ability. Software needs to write 1 to this register to make the Pipe Reset. Writing 0 to this register will finish the Pipe Reset. Writing zero is needed prior to Peripheral reconfiguration for the same pipe.

SDC1_BAM_P_RSTn

Bits	Name	Description
31:1	RESERVED_BITS31_1	Set to Zero (0)
0	P_SW_RST	This resets the pipe and its' registers, (Both Flip-Flops and RAM). 1'b1 - Reset 1'b0 - Do Nothing

0x12402008+ 128*n SDC1_BAM_P_HALTn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Halt register Enables/Disables the Halt Sequence.

This is a self-modifying register.

SDC1_BAM_P_HALTn

Bits	Name	Description
31:2	RESERVED_BITS31_2	Set to Zero (0)
1	P_PROD_HALTED	This bit is used to inform the Consumer about the Producer being in Halt mode now. This is a part of the Halt procedure. 1'b1 - Sets this bit to 1 1'b0 - Does Nothing This bit will be cleared by the HW.
0	P_HALT	When Enabled, the Pipe will enter Halt Mode. 1'b1 - Enable Halt 1'b0 - Disable Halt For B2B Producer pipes, this bit is self modifying. It doesn't need the SW to clear it.

0x12402030+ 128*n SDC1_BAM_P_TRUST_REGn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

SDC1_BAM_P_TRUST_REGn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_P_VMID	Those bits indicate the VMID value to be used when performing Pipe type accesses to the bus. BAM Type accesses include Pipe MTI, Data and Descriptors.
7:2	RESERVED_BITS7_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_P_EE	This Field Indicates the EE (0,1,2,3) to which the Pipe Interrupt belongs to. The BAM interrupt will fire to the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12402010+ 128*n SDC1_BAM_P_IRQ_STTSn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only. It also has informative bits which are not interrupts.

Clearing the interrupt bits is done by writing to P_IRQ_CLR register.

SDC1_BAM_P_IRQ_STTSn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_IRQ	For producer this interrupt happens whenever the last AHB burst of a transfer happens For Consumer when ack_on_success closes a transfer
4	P_ERR_IRQ	Pipe Error interrupt indicates that an error has happened. TBD: Error reason is not yet defined. Interrupt not in use.
3	P_OUT_OF_DESC_IRQ	Out of descriptors interrupt has several meanings depending on the operation mode: Producer - no free space in the descriptors fifo for adding a descriptor Consumer - no descriptors in the descriptors fifo for processing IO Vectors Producer - No descriptors to read (and therefore no space for data to write to the pipe) IO Vectors Consumer - No descriptors to read (and therefore no data to read from pipe)
2	P_WAKE_IRQ	Wake peripheral interrupt signals the driver to wake up the peripheral (USB for example) for transmission via the current pipe. This interrupt is issued whenever an Event comes to the specific pipe.
1	P_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
0	P_PRCSD_DESC_IRQ	This Interrupt rises when BAM finishes processing an IO Vector which has INT bit selected

0x12402014+128*n SDC1_BAM_P_IRQ_CLRn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

SDC1_BAM_P_IRQ_CLRn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_CLR	1’b1 - Clear 1’b0 - Unchanged
4	P_ERR_CLR	1’b1 - Clear 1’b0 - Unchanged
3	P_OUT_OF_DESC_CLR	1’b1 - Clear 1’b0 - Unchanged

SDC1_BAM_P_IRQ_CLRn (cont.)

Bits	Name	Description
2	P_WAKE_CLR	Clear Wake peripheral interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
1	P_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
0	P_PRCSD_DESC_CLR	Clear Descriptor Processed interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged

0x12402018+ 128*n SDC1_BAM_P_IRQ_ENn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the Pipe Interrupt Status register.

SDC1_BAM_P_IRQ_ENn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_EN	1'b1 - Enable 1'b0 - Disable
4	P_ERR_EN	1'b1 - Enable 1'b0 - Disable
3	P_OUT_OF_DESC_EN	1'b1 - Enable 1'b0 - Disable
2	P_WAKE_EN	Enable Wake peripheral interrupt 1'b1 - Enable 1'b0 - Disable
1	P_TIMER_EN	Enable Inactivity timer Interrupt 1'b1 - Enable 1'b0 - Disable
0	P_PRCSD_DESC_EN	Enable Descriptor Processed Interrupt 1'b1 - Enable 1'b0 - Disable

0x1240201C+ 128*n SDC1_BAM_P_TIMERn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the pipe.

SDC1_BAM_P_TIMERn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12402020+ 128*n SDC1_BAM_P_TIMER_CTRLn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The resolution of the pipe inactivity timers are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the P_TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * P_TIMER_TRSHLD.

SDC1_BAM_P_TIMER_CTRLn

Bits	Name	Description
31	P_TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the P_TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	P_TIMER_RUN	Will be used along with P_TIMER_MODE Not implemented at this time. Set to zero(0)
29	P_TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	P_TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12402024+ 128*n SDC1_BAM_P_PRDCR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Producer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

SDC1_BAM_P_PRDCR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_producer
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	BAM_P_TOGGLE	Pipe Bytes Free Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Free Ctrl value
15:0	BAM_P_BYTES_FREE	Pipe Bytes Free value

0x12402028+ 128*n SDC1_BAM_P_CNSMR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Consumer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

SDC1_BAM_P_CNSMR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_consumer
23	BAM_P_WAIT_4_ACK	waiting_for_ack_bytes_avail_r
22	BAM_P_ACK_TOGGLE	ack_bytes_avail_toggle
21	BAM_P_ACK_TOGGLE_R	ack_bytes_avail_toggle_r
20	BAM_P_TOGGLE	Pipe Bytes Avail Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Avail Ctrl value
15:0	BAM_P_BYTES_AVAIL	Pipe Bytes AVAIL value

20.28.3 BAM PIPE configuration registers (RAM)

BAM Pipe management registers configure each pipes' parameters.

Pipe Address span: currently defining each pipe to have 32 addresses, therefore inter pipe offset is 32*4=128=0x80 bytes.

0x1240302C+ 64*n SDC1_BAM_P_EVNT_DEST_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Event Destination Address which is the address of BAM_P_EVNT_REG in the BAM on the other side of the Pipe.

Producer BAM will send Write Events to this address.

Consumer BAM will send Read Events to this address.

This is relevant only for BAM to BAM modes. In System modes, BAM doesn't issue Write/Read events.

SDC1_BAM_P_EVNT_DEST_ADDRn

Bits	Name	Description
31:0	P_EVNT_DEST_ADDR	Address of the Event Register in the peer BAM (second end of the pipe). Driver will configure this when initializing the pipe.

0x12403018+64*n SDC1_BAM_P_EVNT_REGn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register is where Read/Write events are sent to. If current BAM works as Producer, it will receive Read events into this register from the Consumer. If the Consumer is another BAM, it will write read events to this register. If the Consumer is the Software, it will prepare descriptors in the descriptor FIFO and update the DESC_FIFO_PEER_OFST value in this register.

If current BAM works as Consumer, opposite behavior is assumed.

SDC1_BAM_P_EVNT_REGn

Bits	Name	Description
31:16	P_BYTES_CONSUMED	This field is used only in the B2B mode. It indicates the number of bits consumed by the Consumer. Consumer sends this value to the Producer as a part of a read event, for the Producer to know how many bytes were consumed. When working in System mode, this value should be set to zero. BAM to BAM Producer writes zero in this value.
15:0	P_DESC_FIFO_PEER_OFST	This field indicates the Descriptor Fifo Offset Pointer of the Peer BAM (The BAM or the Software which creates descriptors). For example when current BAM works as consumer for the current pipe, Producer BAM (or the software) updates this value to let the current pipe know about the new descriptors added in the Descriptor Fifo.

0x12403000+64*n SDC1_BAM_P_SW_OFSTSn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register denotes the pointer Offset of the first Not Acknowledged Descriptor. Meaning all Descriptors prior to this one have been processed by the BAM. This register is only used by the Software. After receiving an interrupt, software reads this register in order to know what descriptors has been processed.

When the BAM works as Producer, Software will usually read this value after Descriptor Processed Interrupt or after the End of Transfer Interrupt.

When the BAM works as Consumer, Software will usually read this value after Descriptor Processed Interrupt.

NOTE This is non relevant in BAM to BAM modes.

NOTE Although being Writable, Software should never write to this register.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC1_BAM_P_SW_OFSTSn

Bits	Name	Description
31:16	SW_OFST_IN_DESC	Offset inside the Descriptor. This value is used by the Software only when a BAM is working as System Producer. Then the SW can read this value to know how many Bytes were written to the current descriptor if it was not closed down. This is useful for Streaming mode.
15:0	SW_DESC_OFST	Descriptor FIFO offset.

0x12403024+ 64*n SDC1_BAM_P_DATA_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Beginning of the Data Address space.

This register is non relevant in System Modes.

SDC1_BAM_P_DATA_FIFO_ADDRn

Bits	Name	Description
31:0	P_DATA_FIFO_ADDR	Data Address Space beginning.

0x1240301C+ 64*n SDC1_BAM_P_DESC_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Address of the Descriptor Fifo beginning.

NOTE This register is used by all modes.

SDC1_BAM_P_DESC_FIFO_ADDRn

Bits	Name	Description
31:0	P_DESC_FIFO_ADDR	Address of the Descriptors Fifo. This address must be 8 bytes aligned.

0x12403028+ 64*n SDC1_BAM_P_EVNT_GEN_TRSHLDn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register configures the threshold value for Read/Write event generation by the BAM towards another BAM. When a BAM pushes/pops this number of bytes to/from the pipe an event to the other BAM will be generated. A counter summing up the bytes pushed/popped is reset when event is issued, thus restarting count for the threshold.

Events are also issued after End Of Transfer received from the peripheral (Producer case), non regarding whether the pushed bytes count has reached the threshold or not.

This register is non relevant in System Modes.

SDC1_BAM_P_EVNT_GEN_TRSHLDn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TRSHLD	Threshold value. The maximum allowed value is 32kByte.

0x12403020+ 64*n SDC1_BAM_P_FIFO_SIZESn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

The least significant field is the Descriptor Fifo Size.

The most significant field is the Data Fifo Size.

NOTE This Descriptor Fifo Size is used by all modes. The Data Fifo Size is non relevant in System Modes.

SDC1_BAM_P_FIFO_SIZESn

Bits	Name	Description
31:16	P_DATA_FIFO_SIZE	Size of the Data Address Space.
15:0	P_DESC_FIFO_SIZE	Size of the Descriptors Fifo. Must be 8 byte aligned. Each descriptor is 8 bytes. Size of the descriptor fifo must contain an integer number of Descriptors.

20.28.4 BAM PIPE internal state registers (RAM)

BAM Pipe debug registers allow a software look inside on the internal parameters of the BAM State Machines stored in RAM.

Those shouldn't be normally used or altered by the software.

0x12403034+ 64*n SDC1_BAM_P_RETR_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context stored for retransmission.

This is being stored by Ack Update state machine in consumer mode or by the Writeback state machine in producer mode.

This is being loaded by the Writeback state machine when retransmission happens.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC1_BAM_P_RETR_CNTXT_n

Bits	Name	Description
31:16	RETR_DESC_OFST	Descriptor Fifo Offset for retransmission.
15:0	RETR_OFST_IN_DESC	The Offset inside the Descriptor for retransmission.

0x12403038+ 64*n SDC1_BAM_P_SI_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Sideband Inform state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC1_BAM_P_SI_CNTXT_n

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	SI_DESC_OFST	The Descriptor Fifo Offset pointer stored by the Sideband Inform state machine.

0x12403004+ 64*n SDC1_BAM_P_AU_PSM_CNTXT_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Ack Update state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC1_BAM_P_AU_PSM_CNTXT_1_n

Bits	Name	Description
31:16	AU_PSM_ACCUMED	PSM: The acknowledged (EOB/T) number of bytes since last Write Event. AU: The accumulation of the descriptor sizes for the present ack_on_success event. This is never bigger than the ACKED field. Once the ACCUMED values are bigger than Event Threshold, an Event will be issued, the ACKED value will decrease by the ACCUMED size and this value will be zeroed. This also serves as the Bytes Consumed value in the Event.
15:0	AU_ACKED	AU: The left over of the number of bytes that were received via the ack_on_success, that did not cause a descriptor closure. This value is down counting upon issuing Read Event. PSM:

0x12403008+ 64*n SDC1_BAM_P_PSM_CNTXT_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC1_BAM_P_PSM_CNTXT_2_n

Bits	Name	Description
31	PSM_DESC_VALID	The Descriptor Valid bit provided by the Writeback state machine to Pipe state machine.
30	PSM_DESC_IRQ	The Descriptor Interrupt bit provided by the Writeback state machine to pipe state machine.
29	PSM_DESC_IRQ_DONE	The Descriptor Interrupt needed selection bit.
28:25	PSM_GENERAL_BITS	General Context Switch Bits
24:22	PSM_CONS_STATE	State of the Pipe Consumer state machine.
21:19	PSM_PROD_SYS_STATE	State of the Pipe Producer System state machine.
18:16	PSM_PROD_B2B_STATE	State of the Pipe Producer BAM to BAM state machine.
15:0	PSM_DESC_SIZE	The Descriptor Size provided by the Writeback state machine to pipe state machine.

0x1240300C+ 64*n SDC1_BAM_P_PSM_CNTXT_3_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC1_BAM_P_PSM_CNTXT_3_n

Bits	Name	Description
31:0	PSM_DESC_ADDR	The Data Address provided in the current descriptor from the Writeback state machine.

0x12403010+ 64*n SDC1_BAM_P_PSM_CNTXT_4_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC1_BAM_P_PSM_CNTXT_4_n

Bits	Name	Description
31:16	PSM_DESC_OFST	The running Descriptor Fifo Offset of the Writeback state machine
15:0	PSM_SAVED_ACCUMED_SIZE	The Saved Accumulated Size from the Pipe state machine.

0x12403014+64*n SDC1_BAM_P_PSM_CNTXT_5_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

SDC1_BAM_P_PSM_CNTXT_5_n

Bits	Name	Description
31:16	PSM_BLOCK_BYTE_CNT	The Byte count inside the current Block.
15:0	PSM_OFST_IN_DESC	The Offset inside a register. This is used by pipe state machine to compute offset inside a register after retransmission

0x12403030+64*n SDC1_BAM_P_RESERVED_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

SDC1_BAM_P_RESERVED_1_n

Bits	Name	Description
31:0	BAM_P_RES_1	Set to zero (0) Reserved

0x1240303C+64*n SDC1_BAM_P_RESERVED_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

SDC1_BAM_P_RESERVED_2_n

Bits	Name	Description
31:0	BAM_P_RES_2	Set to zero (0) Obsolete Register: BAM_P_IRQ_DEST_ADDRn, n=[0..30]

20.29 USB1 HS BAM Registers (0x12502000 USB1_HS_BAM_BASE)

This section contains the USB1 BAM registers.

BAM supports only Word (4 byte) aligned writes and reads on the Configuration Bus interface.

BAM has MAX_PIPES hardware generic parameter defining the number of pipes it supports. Each BAM can have up to 31 pipes supported.

BAM has BAM_CONF_AHBS_ADDR_WIDTH hardware generic parameter defining the Bit Number for selecting BAM access or Peripheral access. Legal Ranges are 14 to 20. Count starts from 1, meaning a value of 17 will set BAM Base address as 0x0001_0000.

20.29.1 BAM control registers

BAM Control registers configure the BAM operational state, SW reset, interrupts and others.

0x12502F80 USB1_HS_BAM_CTRL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

BAM Control register allows global controls for the BAM.

USB1_HS_BAM_CTRL

Bits	Name	Description
31:17	RESERVED_BITS31_17	Set to Zero (0)
16	IBC_DISABLE	This Bit enables power saving by disabling the inactivity clock timer/counter. This is useful when: 1) The BAM is Enabled but idling for long periods. 2) The BAM is Enabled and running but the inactivity timers/counters are not required by the SW for operating the BAM. When the BAM is Disabled, it automatically shuts down those timers to save power. 1’b1 - Enable Power Saving Mode 1’b0 - Disable Power Saving Mode

USB1_HS_BAM_CTRL (cont.)

Bits	Name	Description
15	BAM_CACHED_DESC_STORE	This Bit enables storage of a cached Descriptor into RAM when doing Context Switch and loading it back when returning to this pipe. This is relevant for System Modes Only. BAM to BAM Consumer mode doesn't have this option. Enabling this makes the Context Switch process slightly longer but reduces AHB Descriptor Fetch time later on. It also reduces the number of descriptor fetches done by the BAM if BAM is treating more than 2 pipes. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
14:13	BAM_DESC_CACHE_SEL	This Selector chooses which Descriptor Caching mode will be used. This is relevant for System Producer or Consumer modes only. 2’b00 - Cache when current descriptor has less than 64 bytes left. 2’b01 - Cache when current descriptor has less than 128 bytes left. 2’b10 - Immediate Auto cache - cache will happen whenever there are no descriptors cached. This might cause unnecessary descriptors reads when switching between more than 2 pipes. It is the most effective when each pipe processes more bytes than there are in an average descriptor (small descriptors, big block size), or when working with 2 or less pipes. 2’b11 - Cache when descriptor is needed only. This results in 1 descriptor present in cache at most. Available in BAM only
12	RESERVED_BITS12	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_SIC_SEL
11:5	BAM_TESTBUS_SEL	Set to Zero (0) Obsolete field: BAM_TESTBUS_SEL Test Bus selector. Supported until (including) bam_p3q3r29 (BlackBird). Moved to a dedicated register - BAM_TEST_BUS_SEL in the following releases.
4	BAM_EN_ACCUM	When Enabled, BAM will accumulate data written by the peripheral in Direct Mode into INCR8 Bursts. This is an optimization feature for Producer Direct Mode cases. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
3	RESERVED_BITS3	Set to Zero (0)
2	RESERVED_BITS2	Set to Zero (0)

USB1_HS_BAM_CTRL (cont.)

Bits	Name	Description
1	BAM_EN	After reset the BAM wakes up in Disabled Mode. While Disabled, BAM operates in Legacy mode (all the transfers from the peripheral go around the BAM as if it doesn't exist) Software Enables this bit to allow BAM operation. This bit doesn't affect the PIPE enable bit in BAM_P_CTRL register. The only possibility to Disable the BAM after it has been enabled is by Hardware or Software reset. 1'b1 - Enabled 1'b0 - Disabled
0	BAM_SW_RST	This will reset the BAM & all Pipes. Software may use this to reset the BAM. As long as the bit remains high the BAM remains in reset state. Software should clear this bit 1'b1 - Reset state 1'b0 - Normal state

0x12502F84 USB1_HS_BAM_REVISION

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a hard coded revision number of the BAM RTL. This corresponds to the BAM target number in the IMS. Also additional BAM settings are reflected here.

USB1_HS_BAM_REVISION

Bits	Name	Description
31:24	INACTIV_TMR_BASE	This indicates the width of the inactivity timers base counter
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	NUM_INACTIV_TMRS	This bit is checked only if INACTIV_TMRS_EXST = 1. This bit indicates how many inactivity timers are implemented according to value of INACTIVITY_TIMERS_SUPPORTED generic: 1'b1 - One timer for global BAM activity (INACTIVITY_TIMERS_SUPPORTED = 1) 1'b0 - MAX_PIPES timers for each pipe activity (INACTIVITY_TIMERS_SUPPORTED = 2)
19	INACTIV_TMRS_EXST	This indicates BAM has inactivity timers. 1'b1 - Timers available (INACTIVITY_TIMERS_SUPPORTED = 1 or 2) 1'b0 - No timers available (INACTIVITY_TIMERS_SUPPORTED = 0)

USB1_HS_BAM_REVISION (cont.)

Bits	Name	Description
18	HIGH_FREQUENCY_BAM	This indicates BAM has Double Sampling on the Ack On Success interface. 1'b1 - Ack On Success double sampled 1'b0 - No double sampling of Ack On Success
17	BAM_HAS_NO_BYPASS	This field indicates BAM has no bypass on the AHB Data bus, from the Peripheral AHB Master to the fabric. When Bypass is available, it is the default routing when BAM is disabled. 1'b1 - No Bypass 1'b0 - Bypass Exists
16	SECURED	This field indicates BAM/BAM-Lite has security support (APU inside) 1'b1 - Secured 1'b0 - Not Secured
15:12	RESERVED_BITS15_12	Set to Zero (0)
11:8	NUM_EES	This indicates the Number of Interrupt Lines (Execution Environments) supported by the BAM. When 1 EE is supported, only the BAM_IRQ_SRCS*_EE0 registers exist. When 4 EEs are supported, all BAM_IRQ_SRCS*_EEn registers exist for n=[0..3].
7:0	REVISION	This field contains the revision number of the core, Hard Coded. 8'h01 - Voyager (bam_p3q3r22 +) 8'h02 - BlackBird (bam_p3q3r27 +) 8'h03 - Waverider BAM (bam_p3q3r30 +) 8'h04 - Aurora BAM (bam_p3q2r43 +) 8'h05 - Shelby BAM (bam_p2q2r45 +) 8'h10 - Waverider BAM Lite (bam_lite_p1q1r0 +) 8'h11 - Aurora BAM Lite (bam_lite_p3q2r16 +) 8'h12 - Shelby BAM Lite (bam_lite_p2q2r18 +)

0x12502FBC USB1_HS_BAM_NUM_PIPES

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a the hard coded number of pipes in the BAM. Since each BAM may have a different number of pipes instantiated in HW, this register allows the SW to know this parameter. The reset state value doesn't have any meaning in this register since it is a constant.

USB1_HS_BAM_NUM_PIPES

Bits	Name	Description
31:24	BAM_NON_PIPE_GRP	This field contains the number of BAM Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
23:16	PERIPH_NON_PIPE_GRP	This field contains the number of Peripheral's Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
15:8	RESERVED_BITS15_8	Set to Zero (0)
7:0	BAM_NUM_PIPES	This field contains the number of pipes available in this BAM

0x12502FC0 USB1_HS_BAM_TIMER

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the BAM (all the pipes are in idle state).

USB1_HS_BAM_TIMER

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12502FC4 USB1_HS_BAM_TIMER_CTRL

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The register can be written and read only when INACTIVITY_TIMERS_SUPPORTED generic equals to 1.

The resolution of the BAM inactivity timer are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define

the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * TIMER_TRSHLD.

USB1_HS_BAM_TIMER_CTRL

Bits	Name	Description
31	TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1 to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	TIMER_RUN	Will be used along with TIMER_MODE Not implemented at this time. Set to zero(0)
29	TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12502F88 USB1_HS_BAM_DESC_CNT_TRSHLD

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds a threshold value for the counter summing the Size of the Descriptors Provided. This value is Global for all pipes but it is relevant for System Producer BAM mode and Both Consumer modes, where Descriptors summing takes place in order to provide the information to the peripheral via pipe bytes free (producer) or pipe bytes available interfaces.

USB1_HS_BAM_DESC_CNT_TRSHLD

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0).
15:0	CNT_TRSHLD	Threshold value. The maximum allowed value is 32kByte. Available in BAM only

0x12502F8C USB1_HS_BAM_IRQ_SRCS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking out this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register points to the physical BAM_IRQ_SRCS_EE0 register.

USB1_HS_BAM_IRQ_SRCS

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12502F90 USB1_HS_BAM_IRQ_SRCS_MSK

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register points to the physical BAM_IRQ_SRCS_MSK_EE0 register.

USB1_HS_BAM_IRQ_SRCS_MSK

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12502FB0 USB1_HS_BAM_IRQ_SRCS_UNMASKED

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register points to the physical BAM_IRQ_SRCS_UNMASKED_EE0 register.

USB1_HS_BAM_IRQ_SRCS_UNMASKED

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

0x12502F94 USB1_HS_BAM_IRQ_STTS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only.

Clearing the interrupt bits is done by writing to BAM_IRQ_CLR register.

USB1_HS_BAM_IRQ_STTS

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
3	BAM_EMPTY_IRQ	This interrupt is for DEBUG purpose only. It should not be used in normal SW flows. The interrupt indicates the BAMs buffer is empty. This bit can become high only when BAM_DATA_ERASE or BAM_DATA_FLUSH is high in BAM_TEST_BUS_SEL register.
2	BAM_ERROR_IRQ	This Indicates a Fatal Error has happened in the BAM. Currently this might happen due to an UnSuccessful Pipe Reset operation.

USB1_HS_BAM_IRQ_STTS (cont.)

Bits	Name	Description
1	BAM_HRESP_ERR_IRQ	This interrupt Indicates that an Erroneous HResponse has been received by the AHB Master. Additional Information about the error may be read at BAM_AHB_MASTER_ERR_* Registers. Clearing this interrupt also clears the BAM_AHB_MASTER_ERR_* Registers. Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12502F98 USB1_HS_BAM_IRQ_CLR

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

USB1_HS_BAM_IRQ_CLR

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
3	BAM_EMPTY_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM-Lite only
2	BAM_ERROR_CLR	1'b1 - Clear 1'b0 - Unchanged
1	BAM_HRESP_ERR_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12502F9C USB1_HS_BAM_IRQ_EN

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the BAM Interrupt Status register.

USB1_HS_BAM_IRQ_EN

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_EN	Enables Inactivity timer interrupt by writing this bit 1'b1 - Enable 1'b0 - Disable
3	BAM_EMPTY_EN	1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
2	BAM_ERROR_EN	1'b1 - Enable 1'b0 - Disable
1	BAM_HRESP_ERR_EN	1'b1 - Enable 1'b0 - Disable Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12502FA0 USB1_HS_BAM_RESERVED_1

Type: Read
Clock: BAM_CLK
Reset State: 0x00000000

USB1_HS_BAM_RESERVED_1

Bits	Name	Description
31	RESERVED_BITS31	Set to Zero (0) Obsolete field: BAM_IRQ_SIC_SEL
30:0	RESERVED_BITS30_0	Set to Zero (0) Obsolete field: P_IRQ_SIC_SEL

0x12502FA4 USB1_HS_BAM_AHB_MASTER_ERR_CTRLS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

USB1_HS_BAM_AHB_MASTER_ERR_CTRLS

Bits	Name	Description
31:23	RESERVED_BITS31_16	Set to Zero (0)
22:18	BAM_ERR_HVMID	HVMID
17	BAM_ERR_DIRECT_MODE	DIRECT MODE
16:12	BAM_ERR_HCID	HCID
11:8	BAM_ERR_HPROT	HPROT
7:5	BAM_ERR_HBURST	HBURST
4:3	BAM_ERR_HSIZE	HSIZE
2	BAM_ERR_HWRITE	HWRITE
1:0	BAM_ERR_HTRANS	HTRANS

0x12502FA8 USB1_HS_BAM_AHB_MASTER_ERR_ADDR

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

USB1_HS_BAM_AHB_MASTER_ERR_ADDR

Bits	Name	Description
31:0	BAM_ERR_ADDR	HADDR

0x12502FAC USB1_HS_BAM_AHB_MASTER_ERR_DATA

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

USB1_HS_BAM_AHB_MASTER_ERR_DATA

Bits	Name	Description
31:0	BAM_ERR_DATA	HDATA

0x12502FB4 USB1_HS_BAM_RESERVED_2

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

USB1_HS_BAM_RESERVED_2

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_IRQ_DEST_ADDR

0x12502FB8 USB1_HS_BAM_RESERVED_3

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

USB1_HS_BAM_RESERVED_3

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_DEST_ADDR

0x12502FF0 USB1_HS_BAM_TRUST_REG

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside - SECURED field in the BAM_REVISION register) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

USB1_HS_BAM_TRUST_REG

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_VMID	Those bits indicate the VMID value to be used when performing BAM type accesses to the bus. BAM Type accesses include BAM MTI (or Direct Mode accesses, not applicable for BAM Lite)
7	BAM_RST_BLOCK	When enabled, the BAM Global SW reset will not be available for usage. This is in order to deny Global SW reset requests by the Global security group. 1'b1 - Enable 1'b0 - Disable
6:2	RESERVED_BITS6_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_EE	This Field Indicates the EE (0,1,2,3) to which the BAM Interrupt belongs to. The pipe interrupts will fire on the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12502FF4 USB1_HS_BAM_TEST_BUS_SEL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This is the testbus selector register.

Supported in releases after bam_p3q3r29 (BlackBird).

USB1_HS_BAM_TEST_BUS_SEL

Bits	Name	Description
31:19	RESERVED_BITS31_19	Set to Zero (0)
18	BAM_DATA_ERASE	When enabled, BAM will be instructed to erase all the data it currently has inside. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1’b1 - Enable Erase 1’b0 - Disabled
17	BAM_DATA_FLUSH	When enabled, BAM will be instructed to flush all the data it currently has inside. BAM will only flush the data once it has enough data and a valid destination for it. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1’b1 - Enable Flush 1’b0 - Disabled
16	BAM_CLK_ALWAYS_ON	This bit controls the BAM to issue ’always on’ clock request. 1’b1 - Enable Always On clock request. 1’b0 - Disabled
15:7	RESERVED_BITS15_7	Set to Zero (0)
6:0	BAM_TESTBUS_SEL	Test Bus selector. Values with bit[11] set high are reserved for the BAM Lite integrator to provide testbus from outside of the BAM Lite. For example, eDML testbus may reside at X’100_0000’ to X’111_1111’ selector values. eDML has no registers thus has no test bus selector, so its test bus is combined with the BAM lite’s. BAM provides zeroes on its testbus when external values selected. X’000_0000’ - Zeros X’000_0001’ - Slave test bus X’000_0010’ - Pipe state machine test bus X’000_0011’ - Buffer test bus X’000_0100’ - Sideband test bus X’000_1101’ - Bus Manager test bus X’001_0000’ - Reg file test bus X’1’’_’’’’ - BAM Lite sets zeroes on the test bus, leaving it for external use

0x12502FF8 USB1_HS_BAM_TEST_BUS_REG

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the value being output to the testbus of the chip. It is not intended for SW usage but for lab debugging of the BAM. Values here can change every cycle.

USB1_HS_BAM_TEST_BUS_REG

Bits	Name	Description
31:0	BAM_TESTBUS_REG	32 bit Testbus value. To select the Block in BAM to show here, use the BAM_TESTBUS_SEL field in BAM_CTRL register.

0x12502FFC USB1_HS_BAM_CNFG_BITS

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM configuration bits for bug fixes. It is highly recommended to follow the directions for each bit and set it accordingly.

USB1_HS_BAM_CNFG_BITS

Bits	Name	Description
31:27	RESERVED_BITS31_27	Set to Zero (0)
26	BAM_AU_ACCUMED	Recommended value: 1 This bit fixes a bug in the Ack Update state machine, where an overflow happened while counting descriptors and reaching more than 64kB of calculated sizes. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only
25	BAM_PSM_P_HD_DATA	Recommended value: 1 This bit allows pipe state machine to ignore retransmission requests if a pipe has just been initialized and process those as a regular fetch request. (consumer modes only). When this bit disabled, BAM could fetch descriptors for a pipe which was reset and no descriptors were added yet, if a retransmission request followed after the reset. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only

USB1_HS_BAM_CNFG_BITS (cont.)

Bits	Name	Description
24	BAM_REG_P_EN	Recommended value: 1 This bit fixes the pipe configuration signals mux for the current active pipe in 2 pipes BAM. When disabled, internal state machines might get into enabled states while the pipe is disabled. This would typically happen after pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
23	BAM_WB_DSC_AVL_P_RST	Recommended value: 1 This bit allows the Writeback state machine to reset the vector indicating there are available descriptors when a pipe reset occurs. If disabled, BAM might fetch descriptors after resetting and reconfiguring a pipe, even though no Event (descriptors) was provided.. 1'b1 - Enable 1'b0 - Disable Available in BAM only
22	BAM_WB_RETR_SVPNT	Recommended value: 1 This bit fixes a bug where a pipe which was reset, still stored its retransmission savepoint, but into the illegal's pipe address space, thus hurting the last pipe of the BAM if the BAM had a total 4, 8 or 16 pipes. This is relevant for Producer to System modes only. (CR-0000151585) 1'b1 - Enabled 1'b0 - Disable Available in BAM only
21	BAM_WB_CSW_ACK_IDL	Recommended value: 1 This bit allows the Writeback state machine to switch into idle state prior to visiting disabled state. This is needed when context switching from mode X to another pipe of mode X is well. This is required to fix a bug in the 2 pipes BAM. 1'b1 - Enable 1'b0 - Disable Available in BAM only
20	BAM_WB_BLK_CSW	Recommended value: 1 When Enabled, this bit does not allow context switch to happen in the Writeback state machine until it has created a descriptor. This is relevant when the descriptor fifo is becoming full and there's no space to create a descriptor, while another pipe is context switching. This might result in the descriptor not to be created ever, if it was the last one for that pipe. Relevant for Producer BAM-to-BAM mode only. 1'b1 - Enable 1'b0 - Disable Available in BAM only

USB1_HS_BAM_CNFG_BITS (cont.)

Bits	Name	Description
19	BAM_WB_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Writeback state machine when performing pipe reset. 1’b1 - 1’b0 - Disable Available in BAM only
18	BAM_SI_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Sideband Inform state machine when performing pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
17	BAM_AU_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Ack Update state machine when performing pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
16	BAM_PSM_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Pipe state machine when performing pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
15	BAM_PSM_CSW_REQ	Recommended value: 1 This bit forces the context switch request from pipe state machine to RAM controller not to last longer than the slave requested. (2 Pipes BAM bug fix) 1’b1 - Enable 1’b0 - Disable Available in BAM only
14	BAM_SB_CLK_REQ	Recommended value: 1 This bit allows the clock request from the sideband block to propagate into the BAM’s common clock request. 1’b1 - Propagate Sideband Clock Request 1’b0 - Disable Available in BAM only
13	BAM_IBC_DISABLE	Recommended value: 1 This bit helps to save power by allowing the BAM to keep the inactivity base counter in reset when BAM is disabled or when SW configures IBC_DISABLE bit high. 1’b1 - Enable Power Saving 1’b0 - Disable Power Saving

USB1_HS_BAM_CNFG_BITS (cont.)

Bits	Name	Description
12	BAM_NO_EXT_P_RST	Recommended value: 1 This bit allows the BAM / BAM Lite to ignore the externally connected blocks (eDML) when doing pipe reset. The BAM, once instructed to pipe reset, first thing lets the externally connected block know a reset is needed. Then it waits for the externally connected block to Acknowledge it is ready for the pipe reset (meaning it doesn't push any data for the reset pipe) and then the BAM Lite completes the pipe reset operation internally. When disabled, the BAM doesn't require any Acknowledge from the external block to perform pipe reset. 1’b1 - Enable external block pipe reset 1’b0 - Disable - ignore external block pipe reset
11	BAM_FULL_PIPE	Recommended value: 0 This enables the BAM support for a BAM to BAM Producer which insists to write to a full pipe. When 0, BAM might issue data overflow if producers write to a full pipe. When 1 BAM will not allow this and lower HReady when peripheral tries to do so. Once space is freed in the pipe, Hready will rise and the flow will continue. This functionality has been found to be buggy and was removed from APQ8064. Bit is currently unused. 1’b1 - Enable 1’b0 - Disable Available in BAM only
10:4	RESERVED_BITS10_4	Set to Zero (0)
3	BAM_ADML_SYNC_BRIDGE	0x1: Use a Synchronous Configuration bridge in aDML. 0x0: Use a Asynchronous Configuration bridge in aDML.
2	BAM_PIPE_CNFG	Recommended value: 1 Pipe SM upgrade for writing EOT bit to the previous descriptor. It’s invoked only when EOB arrives in the end of a descriptor. It is highly recommended to set this bit high. Leaving it low might cause incorrect Pipe Bytes Free value reported to peripheral in rare cases. 1’b1 - Enable 1’b0 - Disable Available in BAM only
1	BAM_ADML_DEEP_CONS_FIFO	0x1: Use a deep Consumer FIFO in aDML (16 dwords) 0x0: Use a shallow Consumer FIFO in aDML (8 dwords)
0	BAM_ADML_INCR4_EN_N	0x1: Don’t allow INCR4 aDML-BAM accesses. 0x0: Allow INCR 4 aDML-BAM accesses.

0x12503800+ 128*n USB1_HS_BAM_IRQ_SRCS_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register has an alias - BAM_IRQ_SRCS register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

USB1_HS_BAM_IRQ_SRCS_EEn

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12503804+ 128*n USB1_HS_BAM_IRQ_SRCS_MSK_EEn, n=[0..3]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register has an alias - BAM_IRQ_SRCS_MSK register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

USB1_HS_BAM_IRQ_SRCS_MSK_EEn

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12503808+ 128*n USB1_HS_BAM_IRQ_SRCS_UNMASKED_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register has an alias - BAM_IRQ_SRCS_UNMASKED register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

USB1_HS_BAM_IRQ_SRCS_UNMASKED_EEn

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

20.29.2 BAM PIPE management registers

BAM Pipe management registers control each pipe's parameters. Those reside in physical registers.

0x12502000+ 128*n USB1_HS_BAM_P_CTRLn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Control register provides various controls for the pipe.

USB1_HS_BAM_P_CTRLn

Bits	Name	Description
31:11	RESERVED_BITS31_11	Set to Zero (0)
10:9	P_PREFETCH_LIMIT	Bam Lite feature Selects the number of bytes to be pre-fetched by the Bam Lite, once a peripheral requests to read data from a pipe. This feature is relevant for Consumer modes only. 2'b00 - 32 bytes at most (INCR8) 2'b01 - 16 bytes at most (INCR4) 2'b10 - 4 bytes at most (SINGLE) Available in BAM-Lite only

USB1_HS_BAM_P_CTRLn (cont.)

Bits	Name	Description
8:7	P_AUTO_EOB_SEL	Bam Lite feature. Selects the number of bytes to be processed before creating End Of Block indication internally by the BAM. See P_AUTO_EOB. Descriptors generated by this feature (bam to bam producer mode) will always be of the chosen size, unless an End Of Transfer, causes a smaller descriptor to be created. 2'b00 - 512 Bytes 2'b01 - 256 Bytes 2'b10 - 128 Bytes 2'b11 - 64 Bytes Available in BAM-Lite only
6	P_AUTO_EOB	BAM Lite feature. When Enabled, the BAM Lite will ignore any incoming End Of Block indications from the peripheral (if any). Instead, the BAM Lite will generate it's own End Of Block indications internally, every P_AUTO_EOB_SEL bytes. This feature is relevant for Producer Bam 2 Bam modes only. It is a must for peripherals which are not able to produce End Of Block indications. 1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
5	P_SYS_MODE	This bit sets the pipe to work in System Mode, where the Software is the second side of the pipe. 1'b1 - System mode. 1'b0 - BAM to BAM mode.
4	P_SYS_STRM	Streaming Enable. Relevant to System Producer BAM mode only.When enabled, BAM will not close descriptors with End Of Transfer notifications received from peripheral, but continue writing the data to the same descriptor. 1'b1 - Enable Streaming Mode 1'b0 - None-Streaming Mode
3	P_DIRECTION	This bit denotes pipe direction. 1'b1 - The pipe can be written (producer mode) 1'b0 - The pipe can be read (consumer mode)
2	RESERVED_BITS2	Set to Zero (0)
1	P_EN	1'b1 - Enable Pipe 1'b0 - Disable Pipe
0	RESERVED_BITS0	Set to Zero (0)

0x12502004+ 128*n USB1_HS_BAM_P_RSTn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Reset register provides Pipe Reset ability. Software needs to write 1 to this register to make the Pipe Reset. Writing 0 to this register will finish the Pipe Reset. Writing zero is needed prior to Peripheral reconfiguration for the same pipe.

USB1_HS_BAM_P_RSTn

Bits	Name	Description
31:1	RESERVED_BITS31_1	Set to Zero (0)
0	P_SW_RST	This resets the pipe and its' registers, (Both Flip-Flops and RAM). 1'b1 - Reset 1'b0 - Do Nothing

0x12502008+ 128*n USB1_HS_BAM_P_HALTn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Halt register Enables/Disables the Halt Sequence.

This is a self-modifying register.

USB1_HS_BAM_P_HALTn

Bits	Name	Description
31:2	RESERVED_BITS31_2	Set to Zero (0)
1	P_PROD_HALTED	This bit is used to inform the Consumer about the Producer being in Halt mode now. This is a part of the Halt procedure. 1'b1 - Sets this bit to 1 1'b0 - Does Nothing This bit will be cleared by the HW.
0	P_HALT	When Enabled, the Pipe will enter Halt Mode. 1'b1 - Enable Halt 1'b0 - Disable Halt For B2B Producer pipes, this bit is self modifying. It doesn't need the SW to clear it

0x12502030+ 128*n USB1_HS_BAM_P_TRUST_REGn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

USB1_HS_BAM_P_TRUST_REGn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_P_VMID	Those bits indicate the VMID value to be used when performing Pipe type accesses to the bus. BAM Type accesses include Pipe MTI, Data and Descriptors.
7:2	RESERVED_BITS7_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_P_EE	This Field Indicates the EE (0,1,2,3) to which the Pipe Interrupt belongs to. The BAM interrupt will fire to the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12502010+ 128*n USB1_HS_BAM_P_IRQ_STTSn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only. It also has informative bits which are not interrupts.

Clearing the interrupt bits is done by writing to P_IRQ_CLR register.

USB1_HS_BAM_P_IRQ_STTSn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_IRQ	For producer this interrupt happens whenever the last AHB burst of a transfer happens For Consumer when ack_on_success closes a transfer
4	P_ERR_IRQ	Pipe Error interrupt indicates that an error has happened. TBD: Error reason is not yet defined. Interrupt not in use.
3	P_OUT_OF_DESC_IRQ	Out of descriptors interrupt has several meanings depending on the operation mode: Producer - no free space in the descriptors fifo for adding a descriptor Consumer - no descriptors in the descriptors fifo for processing IO Vectors Producer - No descriptors to read (and therefore no space for data to write to the pipe) IO Vectors Consumer - No descriptors to read (and therefore no data to read from pipe)
2	P_WAKE_IRQ	Wake peripheral interrupt signals the driver to wake up the peripheral (USB for example) for transmission via the current pipe. This interrupt is issued whenever an Event comes to the specific pipe.
1	P_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
0	P_PRCSD_DESC_IRQ	This Interrupt rises when BAM finishes processing an IO Vector which has INT bit selected

0x12502014+128*n USB1_HS_BAM_P_IRQ_CLRn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

USB1_HS_BAM_P_IRQ_CLRn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_CLR	1’b1 - Clear 1’b0 - Unchanged
4	P_ERR_CLR	1’b1 - Clear 1’b0 - Unchanged
3	P_OUT_OF_DESC_CLR	1’b1 - Clear 1’b0 - Unchanged

USB1_HS_BAM_P_IRQ_CLRn (cont.)

Bits	Name	Description
2	P_WAKE_CLR	Clear Wake peripheral interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
1	P_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
0	P_PRCSD_DESC_CLR	Clear Descriptor Processed interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged

0x12502018+128*n USB1_HS_BAM_P_IRQ_ENn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the Pipe Interrupt Status register.

USB1_HS_BAM_P_IRQ_ENn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_EN	1'b1 - Enable 1'b0 - Disable
4	P_ERR_EN	1'b1 - Enable 1'b0 - Disable
3	P_OUT_OF_DESC_EN	1'b1 - Enable 1'b0 - Disable
2	P_WAKE_EN	Enable Wake peripheral interrupt 1'b1 - Enable 1'b0 - Disable
1	P_TIMER_EN	Enable Inactivity timer Interrupt 1'b1 - Enable 1'b0 - Disable
0	P_PRCSD_DESC_EN	Enable Descriptor Processed Interrupt 1'b1 - Enable 1'b0 - Disable

0x1250201C+ 128*n USB1_HS_BAM_P_TIMERn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the pipe.

USB1_HS_BAM_P_TIMERn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12502020+ 128*n USB1_HS_BAM_P_TIMER_CTRLn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The resolution of the pipe inactivity timers are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the P_TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * P_TIMER_TRSHLD.

USB1_HS_BAM_P_TIMER_CTRLn

Bits	Name	Description
31	P_TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the P_TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	P_TIMER_RUN	Will be used along with P_TIMER_MODE Not implemented at this time. Set to zero(0)
29	P_TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	P_TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12502024+ 128*n USB1_HS_BAM_P_PRDCR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Producer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

USB1_HS_BAM_P_PRDCR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_producer
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	BAM_P_TOGGLE	Pipe Bytes Free Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Free Ctrl value
15:0	BAM_P_BYTES_FREE	Pipe Bytes Free value

0x12502028+ 128*n USB1_HS_BAM_P_CNSMR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Consumer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

USB1_HS_BAM_P_CNSMR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_consumer
23	BAM_P_WAIT_4_ACK	waiting_for_ack_bytes_avail_r
22	BAM_P_ACK_TOGGLE	ack_bytes_avail_toggle
21	BAM_P_ACK_TOGGLE_R	ack_bytes_avail_toggle_r
20	BAM_P_TOGGLE	Pipe Bytes Avail Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Avail Ctrl value
15:0	BAM_P_BYTES_AVAIL	Pipe Bytes AVAIL value

20.29.3 BAM PIPE configuration registers (RAM)

BAM Pipe management registers configure each pipes' parameters.

Pipe Address span: currently defining each pipe to have 32 addresses, therefore inter pipe offset is 32*4=128=0x80 bytes.

0x1250302C+ 64*n USB1_HS_BAM_P_EVNT_DEST_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Event Destination Address which is the address of BAM_P_EVNT_REG in the BAM on the other side of the Pipe.

Producer BAM will send Write Events to this address.

Consumer BAM will send Read Events to this address.

This is relevant only for BAM to BAM modes. In System modes, BAM doesn't issue Write/Read events.

USB1_HS_BAM_P_EVNT_DEST_ADDRn

Bits	Name	Description
31:0	P_EVNT_DEST_ADDR	Address of the Event Register in the peer BAM (second end of the pipe). Driver will configure this when initializing the pipe.

0x12503018+64*n USB1_HS_BAM_P_EVNT_REGn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register is where Read/Write events are sent to. If current BAM works as Producer, it will receive Read events into this register from the Consumer. If the Consumer is another BAM, it will write read events to this register. If the Consumer is the Software, it will prepare descriptors in the descriptor FIFO and update the DESC_FIFO_PEER_OFST value in this register.

If current BAM works as Consumer, opposite behavior is assumed.

USB1_HS_BAM_P_EVNT_REGn

Bits	Name	Description
31:16	P_BYTES_CONSUMED	This field is used only in the B2B mode. It indicates the number of bits consumed by the Consumer. Consumer sends this value to the Producer as a part of a read event, for the Producer to know how many bytes were consumed. When working in System mode, this value should be set to zero. BAM to BAM Producer writes zero in this value.
15:0	P_DESC_FIFO_PEER_OFST	This field indicates the Descriptor Fifo Offset Pointer of the Peer BAM (The BAM or the Software which creates descriptors). For example when current BAM works as consumer for the current pipe, Producer BAM (or the software) updates this value to let the current pipe know about the new descriptors added in the Descriptor Fifo.

0x12503000+64*n USB1_HS_BAM_P_SW_OFSTSn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register denotes the pointer Offset of the first Not Acknowledged Descriptor. Meaning all Descriptors prior to this one have been processed by the BAM. This register is only used by the Software. After receiving an interrupt, software reads this register in order to know what descriptors has been processed.

When the BAM works as Producer, Software will usually read this value after Descriptor Processed Interrupt or after the End of Transfer Interrupt.

When the BAM works as Consumer, Software will usually read this value after Descriptor Processed Interrupt.

NOTE This is non relevant in BAM to BAM modes.

NOTE Although being Writable, Software should never write to this register.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB1_HS_BAM_P_SW_OFSTSn

Bits	Name	Description
31:16	SW_OFST_IN_DESC	Offset inside the Descriptor. This value is used by the Software only when a BAM is working as System Producer. Then the SW can read this value to know how many Bytes were written to the current descriptor if it was not closed down. This is useful for Streaming mode.
15:0	SW_DESC_OFST	Descriptor FIFO offset.

0x12503024+ 64*n USB1_HS_BAM_P_DATA_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Beginning of the Data Address space.

This register is non relevant in System Modes.

USB1_HS_BAM_P_DATA_FIFO_ADDRn

Bits	Name	Description
31:0	P_DATA_FIFO_ADDR	Data Address Space beginning.

0x1250301C+ 64*n USB1_HS_BAM_P_DESC_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Address of the Descriptor Fifo beginning.

NOTE This register is used by all modes.

USB1_HS_BAM_P_DESC_FIFO_ADDRn

Bits	Name	Description
31:0	P_DESC_FIFO_ADDR	Address of the Descriptors Fifo. This address must be 8 bytes aligned.

0x12503028+64*n USB1_HS_BAM_P_EVNT_GEN_TRSHLDn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register configures the threshold value for Read/Write event generation by the BAM towards another BAM. When a BAM pushes/pops this number of bytes to/from the pipe an event to the other BAM will be generated. A counter summing up the bytes pushed/popped is reset when event is issued, thus restarting count for the threshold.

Events are also issued after End Of Transfer received from the peripheral (Producer case), non regarding whether the pushed bytes count has reached the threshold or not.

This register is non relevant in System Modes.

USB1_HS_BAM_P_EVNT_GEN_TRSHLDn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TRSHLD	Threshold value. The maximum allowed value is 32kByte.

0x12503020+64*n USB1_HS_BAM_P_FIFO_SIZESn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

The least significant field is the Descriptor Fifo Size.

The most significant field is the Data Fifo Size.

NOTE This Descriptor Fifo Size is used by all modes. The Data Fifo Size is non relevant in System Modes.

USB1_HS_BAM_P_FIFO_SIZESn

Bits	Name	Description
31:16	P_DATA_FIFO_SIZE	Size of the Data Address Space.
15:0	P_DESC_FIFO_SIZE	Size of the Descriptors Fifo. Must be 8 byte aligned. Each descriptor is 8 bytes. Size of the descriptor fifo must contain an integer number of Descriptors.

20.29.4 BAM PIPE internal state registers (RAM)

BAM Pipe debug registers allow a software look inside on the internal parameters of the BAM State Machines stored in RAM.

Those shouldn't be normally used or altered by the software.

0x12503034+64*n USB1_HS_BAM_P_RETR_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context stored for retransmission.

This is being stored by Ack Update state machine in consumer mode or by the Writeback state machine in producer mode.

This is being loaded by the Writeback state machine when retransmission happens.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB1_HS_BAM_P_RETR_CNTXT_n

Bits	Name	Description
31:16	RETR_DESC_OFST	Descriptor Fifo Offset for retransmission.
15:0	RETR_OFST_IN_DESC	The Offset inside the Descriptor for retransmission.

0x12503038+64*n USB1_HS_BAM_P_SI_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Sideband Inform state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB1_HS_BAM_P_SI_CNTXT_n

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	SI_DESC_OFST	The Descriptor Fifo Offset pointer stored by the Sideband Inform state machine.

0x12503004+ 64*n USB1_HS_BAM_P_AU_PSM_CNTXT_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Ack Update state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB1_HS_BAM_P_AU_PSM_CNTXT_1_n

Bits	Name	Description
31:16	AU_PSM_ACCUMED	PSM: The acknowledged (EOB/T) number of bytes since last Write Event. AU: The accumulation of the descriptor sizes for the present ack_on_success event. This is never bigger than the ACKED field. Once the ACCUMED values are bigger than Event Threshold, an Event will be issued, the ACKED value will decrease by the ACCUMED size and this value will be zeroed. This also serves as the Bytes Consumed value in the Event.
15:0	AU_ACKED	AU: The left over of the number of bytes that were received via the ack_on_success, that did not cause a descriptor closure. This value is down counting upon issuing Read Event. PSM:

0x12503008+ 64*n USB1_HS_BAM_P_PSM_CNTXT_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB1_HS_BAM_P_PSM_CNTXT_2_n

Bits	Name	Description
31	PSM_DESC_VALID	The Descriptor Valid bit provided by the Writeback state machine to Pipe state machine.
30	PSM_DESC_IRQ	The Descriptor Interrupt bit provided by the Writeback state machine to pipe state machine.
29	PSM_DESC_IRQ_DONE	The Descriptor Interrupt needed selection bit.
28:25	PSM_GENERAL_BITS	General Context Switch Bits
24:22	PSM_CONS_STATE	State of the Pipe Consumer state machine.
21:19	PSM_PROD_SYS_STATE	State of the Pipe Producer System state machine.
18:16	PSM_PROD_B2B_STATE	State of the Pipe Producer BAM to BAM state machine.
15:0	PSM_DESC_SIZE	The Descriptor Size provided by the Writeback state machine to pipe state machine.

0x1250300C+ 64*n USB1_HS_BAM_P_PSM_CNTXT_3_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB1_HS_BAM_P_PSM_CNTXT_3_n

Bits	Name	Description
31:0	PSM_DESC_ADDR	The Data Address provided in the current descriptor from the Writeback state machine.

0x12503010+ 64*n USB1_HS_BAM_P_PSM_CNTXT_4_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB1_HS_BAM_P_PSM_CNTXT_4_n

Bits	Name	Description
31:16	PSM_DESC_OFST	The running Descriptor Fifo Offset of the Writeback state machine
15:0	PSM_SAVED_ACCUMED_SIZE	The Saved Accumulated Size from the Pipe state machine.

0x12503014+64*n USB1_HS_BAM_P_PSM_CNTXT_5_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB1_HS_BAM_P_PSM_CNTXT_5_n

Bits	Name	Description
31:16	PSM_BLOCK_BYTE_CNT	The Byte count inside the current Block.
15:0	PSM_OFST_IN_DESC	The Offset inside a register. This is used by pipe state machine to compute offset inside a register after retransmission

0x12503030+64*n USB1_HS_BAM_P_RESERVED_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

USB1_HS_BAM_P_RESERVED_1_n

Bits	Name	Description
31:0	BAM_P_RES_1	Set to zero (0) Reserved

0x1250303C+64*n USB1_HS_BAM_P_RESERVED_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

USB1_HS_BAM_P_RESERVED_2_n

Bits	Name	Description
31:0	BAM_P_RES_2	Set to zero (0) Obsolete Register: BAM_P_IRQ_DEST_ADDRn, n=[0..30]

20.30 USB2 OTG HS Registers (0x12510000 USB2_HSIC_BASE)

This section contains USB2 OTG HS registers.

20.30.1 Identification registers

Identification registers are used to declare the slave interface presence and include a table of the hardware configuration parameters.

0x12510000 USB2_HSIC_USB_OTG_HS_ID

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0042FA05

The USB_OTG_HS_ID register is the identification register. It provides a simple way to determine if the USB-HS USB 2.0 core is provided in the system. The ID register identifies the USB-HS USB 2.0 core and its revision.

USB2_HSIC_USB_OTG_HS_ID

Bits	Name	Description
31:24	RESERVED_BITS31_24	These bits are reserved and should be set to zero.
23:16	REVISON_7_0	This field contains the revision number of the core - 0x42.
15:8	NID_5_0	This field contains the complement version of ID[7:0] - 0xFA.
7:0	ID_5_0	This field is the configuration number. This number is set to 0x05 and indicates that the peripheral is the USB-HS USB 2.0 core.

0x12510004 USB2_HSIC_USB_OTG_HS_HWGENERAL

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x5C2

The USB_OTG_HS_HWGENERAL register contains the general hardware parameters.

USB2_HSIC_USB_OTG_HS_HWGENERAL

Bits	Name	Description
31:10	RESERVED_BITS31_10	Clear (0) these bits.
9	SM	VUSB_HS_PHY_SERIAL = 2
8:6	PHYM	VUSB_HS_PHY_TYPE = 7
5:4	PHYW	VUSB_HS_PHY16_8 = 0

USB2_HSIC_USB_OTG_HS_HWGENERAL (cont.)

Bits	Name	Description
3	BWT	This bit is reserved for internal testing = 0
2:1	CLCK	VUSB_HS_CLOCK_CONFIGURATION = 1
0	RT	VUSB_HS_RESET_TYPE = 0

0x12510008 USB2_HSIC_USB_OTG_HS_HWHOST

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x10020001

The USB_OTG_HS_HWHOST register contains the host hardware parameters.

USB2_HSIC_USB_OTG_HS_HWHOST

Bits	Name	Description
31:24	TTPER	VUSB_HS_TT_PERIODIC_CONTEXTS
23:16	TTASY	VUSB_HS_TT_ASYNC_CONTEXTS
15:4	RESERVED_BITS15_4	Clear (0) these bits.
3:1	NPORT	VUSB_HS_NUM_PORT-1
0	HC	VUSB_HS_HOST

0x1251000C USB2_HSIC_USB_OTG_HS_HWDEVICE

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000021

The USB_OTG_HS_HWDEVICE register contains the device hardware parameters.

USB2_HSIC_USB_OTG_HS_HWDEVICE

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:1	DEVEP	VUSB_HS_DEV_EP
0	DC	Device capable; [VUSB_HS_DEV/=0]

0x12510010 USB2_HSIC_USB_OTG_HS_HWTXBUF

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x80070B08

The USB_OTG_HS_HWTXBUF register contains the Tx buffer hardware parameters.

USB2_HSIC_USB_OTG_HS_HWTXBUF

Bits	Name	Description
31	TXLCR	This bit is fixed to 1'b1 so that the local context register's are included in the design. This means that the DMA context is implemented in FlipFlops.
30:24	RESERVED_BITS30_24	Clear (0) these bits.
23:16	TXCHANADD	VUSB_HS_TX_CHAN_ADD - Defines the number of address lines needed per Endpoint per the TX latency buffer. It's reset value is taken from a GENERIC value passed to the core.
15:8	TXADD	VUSB_HS_TX_ADD - Defines the number of address lines needed per the entire TX latency buffer. It's reset value is taken from a GENERIC value passed to the core.
7:0	TXBURST	VUSB_HS_TX_BURST - Defines the data burst length of the AHB master interface in Quad-words (4-byte increments) of the TX data. It's reset value is taken from a GENERIC value passed to the core. Note that the actual burst length will depend on the settings of USB_OTG_HS_AHB_MODE and USB_OTG_HS_AHB_BURST registers.

0x12510014 USB2_HSIC_USB_OTG_HS_HWRXBUF

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000808

The USB_OTG_HS_HWRXBUF register contains the Rx buffer hardware parameters.

USB2_HSIC_USB_OTG_HS_HWRXBUF

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits).
15:8	RX_ADD	VUSB_HS_RX_ADD - Defines the number of address lines needed per the entire RX latency buffer. It's reset value is taken from a GENERIC value passed to the core.

USB2_HSIC_USB_OTG_HS_HWRXBUF (cont.)

Bits	Name	Description
7:0	RX_BURST	VUSB_HS_RX_BURST - Defines the data burst length of the AHB master interface in Quad-words (4-byte increments) of the RX data. It's reset value is taken from a GENERIC value passed to the core. Note that the actual burst length will depend on the settings of USB_OTG_HS_AHB_MODE and USB_OTG_HS_AHB_BURST registers.

0x12510040+4*n USB2_HSIC_USB_OTG_HS_SCRATCH_RAMn, n=[0..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

USB_OTG_HS_SCRATCH_RAMn registers are 16 32bit scratch registers.Required for passing USB software information between different images.

USB2_HSIC_USB_OTG_HS_SCRATCH_RAMn

Bits	Name	Description
31:0	SCRATCH_REGISTER	32 bit scratch register

20.30.2 Device/host timer registers

The host/device controller drivers can measure time related activities using these timer registers.

NOTE These registers are not part of the standard EHCI controller.

0x12510080 USB2_HSIC_USB_OTG_HS_GPTIMER0LD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER0LD register is the general purpose timer 0 load register. This register contains the timer duration or load value. See the GPTIMER0CTRL register for a description of the timer functions.

USB2_HSIC_USB_OTG_HS_GPTIMER0LD

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.

USB2_HSIC_USB_OTG_HS_GPTIMER0LD (cont.)

Bits	Name	Description
23:0	GPTLD	General purpose timer load value. This field is the value to be loaded into the GPTCNT countdown timer on a reset action. This value in this register represents the time in microseconds minus 1 for the timer duration. Example: for a one millisecond timer, load 1000-1=999 or 0x0003E7. Note: Max value is 0xFFFFFF or 16.777215 seconds

0x12510084 USB2_HSIC_USB_OTG_HS_GPTIMER0CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER0CTRL register is the general purpose timer 0 control register. This register contains the control for the timer and a data field can be queried to determine the running count value. This timer has a granularity of 1 ms and can be programmed to a little over 16 seconds. There are two modes supported by this timer: the first is a one-shot and the second is a looped count, which is described in the register table below. When the timer counter value transitions to zero, an interrupt can be generated though the use of the timer interrupts in the USBTS and USBINTR registers.

USB2_HSIC_USB_OTG_HS_GPTIMER0CTRL

Bits	Name	Description
31	GTPRUN	General purpose timer run Read/write value 0 = Timer stop value 1 = Timer run This bit enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.
30	GPTRST	General purpose timer reset Write-only value 0 = No action value 1 = Load counter value Writing a one to this bit will reload the GPTCNT with the value in GPTLD.
29:25	RESERVED_BITS29_25	Clear (0) these bits.

USB2_HSIC_USB_OTG_HS_GPTIMER0CTRL (cont.)

Bits	Name	Description
24	GPTMODE	General purpose timer mode Read/write value 0 = One shot value 1 = Repeat This bit selects between a single timer countdown and a looped count down. In the one-shot mode, the timer will count down to zero, generate an interrupt, and stop until the counter is reset by the software. In the repeat mode, the timer will count down to zero, generate an interrupt, and automatically reload the counter to begin again.
23:0	GPTCNT	General purpose timer counter Read-only This field is the value of the running timer.

0x12510088 USB2_HSIC_USB_OTG_HS_GPTIMER1LD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER1LD register is the general purpose timer 1 control register. This register contains the timer duration or load value. See the GPTIMER0LDregister for a description of the timer functions.

USB2_HSIC_USB_OTG_HS_GPTIMER1LD

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.
23:0	GPTLD	General purpose timer load value. This field is the value to be loaded into the GPTCNT countdown timer on a reset action. This value in this register represents the time in microseconds minus 1 for the timer duration. Example: for a one millisecond timer, load 1000-1=999 or 0x0003E7. Note: Max value is 0xFFFFFF or 16.777215 seconds.

0x1251008C USB2_HSIC_USB_OTG_HS_GPTIMER1CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER1CTRL register is the general purpose timer 1 control register. See the description of the USB_OTG_HS_GPTIMER0CTRL register for details about this register.

USB2_HSIC_USB_OTG_HS_GPTIMER1CTRL

Bits	Name	Description
31	GTPRUN	General purpose timer run Read/write value 0 = Timer stop value 1 = Timer run This bit enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.
30	GPTRST	General purpose timer reset Write-only value 0 = No action value 1 = Load counter value Writing a one to this bit will reload the GPTCNT with the value in GPTLD.
29:25	RESERVED_BITS29_25	Clear (0) these bits.
24	GPTMODE	General purpose timer mode Read/write value 0 = One shot value 1 = Repeat This bit selects between a single timer countdown and a looped count down. In the one-shot mode, the timer will count down to zero, generate an interrupt, and stop until the counter is reset by the software. In the repeat mode, the timer will count down to zero, generate an interrupt, and automatically reload the counter to begin again.
23:0	GPTCNT	General purpose timer counter Read-only This field is the value of the running timer.

20.30.3 Wrapper operational registers

0x12510090 USB2_HSIC_USB_OTG_HS_AHB_BURST

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_AHB_BURST register determines the AHB master mode of the USB HS Core.

NOTE If the USB_OTG_HS_AHB_MODE is configured to be 0x0 (the AHB Transactor is used), this register must be 0x0 as well, otherwise the AHB Master bus behavior is undefined. Use values other than 0x0 only if setting USB_OTG_HS_AHB_MODE to 0x1.

USB2_HSIC_USB_OTG_HS_AHB_BURST

Bits	Name	Description
31:3	RESERVED_BITS31_3	Should be set to zero.
2:0	AHB_BURST	AMBA AHB BURST. This is a r/w field that selects the following options for the m_hburst signal of the AMBA master interface: In all cases where the unspecified length burst is allowed, singles access may also occur, this is mostly true when the transaction is not 32-bit aligned. Two consecutive single accesses should not happen. When a INCRx burst size is selected and the transfer is not multiple of the INCRx burst, the burst is decomposed in the different ways. With AHBBRST[2] = 1, the smaller bursts will be unspecified length. with AHBBRST[2] = 0, the smaller bursts will be smaller INCRx or singles. For example, lets say that it's required at a given time, to transfer 22 words of information, for the following values of AHBBRST the master sequence will be: This field after reset is set to a default value that can be configured in the file vusb_hs_cfg.vhd. The AHBBRST field is only used if the AMBA-AHB system interface has been selected. It has no effect for cores featuring BVCI interface. In the later case the read will return zeros. When this field is different from zero, the value of the fields TXBURST /RXBURST in register BURSTSIZE 160h, will be ignored by the controller. Internally the BURSTSIZE will be set to the value of the INCRx AMBA burst. Since this has a direct relation with the burst sizes you must be careful with AHB burst selected. Although the TXBURST / RXBURST are bypassed, this register can still be written / read with no effect, while the AHBBRST field is non-zero. 0x0: INCR burst of unspecified length 0x1: INCR4, non-multiple transfers of INCR4 will be decomposed into singles 0x2: INCR8, non-multiple transfers of INCR8, will be decomposed into INCR4 or singles 0x3: INCR16, non-multiple transfers of INCR16, will be decomposed into INCR8, INCR4 or singles 0x4: This value is reserved and should not be used 0x5: INCR4, non-multiple transfers of INCR4 will be decomposed into smaller unspecified length bursts 0x6: INCR8, non-multiple transfers of INCR8 will be decomposed into smaller unspecified length bursts 0x7: INCR16, non-multiple transfers of INCR16 will be decomposed into smaller unspecified length bursts 0x5: INCR4+ INCR4 +INCR4+ INCR4 +INCR4+ INCR unspec. length 0x6: INCR8+INCR8+INCR4+ INCR unspec. length 0x7: INCR16+INCR4+ INCR unspec. length 0x1: INCR4+ INCR4 +INCR4+ INCR4 +INCR4+SINGLE+SINGLE 0x2: INCR8+INCR8+INCR4+SINGLE+SINGLE 0x3: INCR16+INCR4+SINGLE+SINGLE

0x12510094 USB2_HSIC_USB_OTG_HS_XTOR_STS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_XTOR_STS register is currently a placeholder for future status bits from the AHB2AHB Transactor.

USB2_HSIC_USB_OTG_HS_XTOR_STS

Bits	Name	Description
31:2	RESERVED_BITS31_2	Not used currently.
1	GRANT_STOLEN	Reports whether the arbiter removed the hgrant signal prior to completing a transaction. This is currently supported in WRITES ONLY. This bit can be cleared by writing a ’1’ to the GRANT_STOLEN_CLEAR bit in the USB_OTG_HS_AHB_MODE register. To enable this bit again, write a ’0’ to he GRANT_STOLEN_CLEAR bit in the USB_OTG_HS_AHB_MODE register.
0	RESERVED_BIT0	Not used currently.

0x12510098 USB2_HSIC_USB_OTG_HS_AHB_MODE

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1

USB2_HSIC_USB_OTG_HS_AHB_MODE

Bits	Name	Description
31	ASYNC_BRIDGES_BYPASS	Default is ’0’. When ’0’ the asynchronous bridge on the master AHB interface is used. When ’1’, it is bypassed. The bridge on the slave AHB is always used.
30:5	RESERVED_BITS30_5	Not used currently.
4	INCR_OVERRIDE	Valid only if the Transactor is bypassed: When ’1’, all INCR bursts from the USB Core will be internally transformed into SINGLE transfers. When ’0’, if the USB Core issues an INCR burst, it will propagate to the external master AHB port.

USB2_HSIC_USB_OTG_HS_AHB_MODE (cont.)

Bits	Name	Description
3:2	HPROT_MODE	When ’00’ the HPROT signal out of the USB Wrapper is ’0001’, and all transactions are non-posted. When ’01’ the HPROT signal out of the USB Wrapper is ’0101’, and all transactions are posted. When ’10’ the HPROT signal out of the USB Wrapper alternates according to the context of the AHB bus access. Control structures are non-posted while data transfer is posted. When ’11’, reserved value, but currently maps to non-posted (same as ’00’).
1	GRANT_STOLEN_CLEAR	Clears the grant stolen field of the USB_OTG_HS_XTOR_STS register. To enable this bit again, write ’0’ after clearing the GRANT_STOLEN (’1’).
0	XTOR_BYPASS	When this bit is set (1), the AHB Transactor is bypassed, and the USB HS Core’s AHB Master interface is directly connected to the AHB system. In this case, the USB_OTG_HS_AHB_BURST register value will determine the bus characteristics. When this bit is reset (0), the AHB Transactor is used to connect the USB HS Core to the AHB system.

0x1251009C USB2_HSIC_USB_OTG_HS_GEN_CONFIG

Type: Read/write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXX0830

The USB_OTG_HS_GEN_CONFIG register is used to configure various features that have been added to the HS USB Core.

USB2_HSIC_USB_OTG_HS_GEN_CONFIG

Bits	Name	Description
31:16	USB_OTG_HS_HW_QVERSION	HW revision of the USB OTG HS core. This version changes with every official release of USB_OTG_HS core.
15	SYS_CLK_SW_EN	This bit is applicable only in SPS Device mode. When this bit is set then USB core always voting for USB_SYSTEM_CLK. Default value is 0 - USB core doesn’t request USB_SYSTEM_CLK when in Low Power Mode.
14	TESTMUX_SEL_4	see TESTMUX_SEL_3_0 the first 4 bits of this register.
13	USB_BAM_DISABLE	This bit disables the bam logic inside the USB and makes him work in Legacy mode.
12	DMA_HPROT_CTRL	When this bit is set Link Controller always does non-posted dQH writes.
11	ISO_FIX_EN	This bit enables fix for Isochronous bug in CI core (CR--0000135251).

USB2_HSIC_USB_OTG_HS_GEN_CONFIG (cont.)

Bits	Name	Description
10	DSC_PE_RST_EN	This bit enables an automatic reset of Device PE State Machine on disconnection event when operating as device. This reset is a HW fix for CR-000940.
9	HOST_SIM_TIMERS_EN_SUSP	When this bit is set (1), the timers used for the USB suspend process short for faster simulation and ATE time. When this bit is clear(0), the timers used for the USB suspend process are according to the USB specification.
8	HOST_SIM_TIMERS_EN_STD	When this bit is set (1), the timers used for the USB reset on the ULPI are short for faster simulation and ATE time. When this bit is clear(0), the timers used for the USB reset on the ULPI are according to the USB specification.
7	PE_RX_BUF_PENDING_EN	This is only valid in Device Mode. Setting this bit will cause to store a Transaction Status Tag in the Pending register instead of RX Buffer if the RX Buffer is full. The Tag will move from Pending register to RX Buffer as soon as it becomes not full.
6	STREAM_RX_BYPASS_ENABLE	This is only valid in Device Mode. If SDIS bit is set (bit 4 of USB_OTG_HS_USBMODE (0x1A8)), i.e., streaming mode is disabled, setting this bit will cause the RX traffic to override the SDIS bit, and to receive in streaming mode. TX will still be in non-streaming mode.
5	ULPI_SERIAL_EN	This bit must be set to enable operation of ULPI Serial FS/LS mode. Default state is ’1’ - ULPI Serial mode is supported.
4	PE_DP_TXFIFO_IDLE_FORCE	This is only valid in Device Mode. Setting this bit to ’1’ forces the dp_tx_fifo_cmd_dev to be equal to PE_DP_TXFIFO_IDLE when Device PE state machine in REPORT_NAK state and the RX Buffer is full. This bit is used to enable fix of CR-001612. Reset value is ’1’.

USB2_HSIC_USB_OTG_HS_GEN_CONFIG (cont.)

Bits	Name	Description
3:0	TESTMUX_SEL_3_0	With TESTMUX_SEL_4 select one of the following test buses: Value 00001 Key state machines 01101 hsic_test_bus1 01110 hsic_test_bus2 10000 dma_eng_3 dma_dev_sm_2 10001 dma_eng_4 dma_traf others zeros 0x2: dma_eng_0 dma_dev_sm_1 0x3: dma_eng_1 dma_context 0x4: dma_eng_2 dma_mem_arb 0x5: prot_eng_0 0x6: prot_eng_1 0x7: prot_eng_2 0x8: port_ctrl_0 0x9: port_ctrl_1 0xA: tx_buffer 0xB: rx_buffer 0xC: otg

0x125100A0 USB2_HSIC_USB_OTG_HS_GEN_CONFIG_2

Type: Read/write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0001F60

Register for the chicken bits. The USB_OTG_HS_GEN_CONFIG_2 register is used to configure various features that have been added to the HS USB Core. By default, all chicken bits are off and the fix is applicable.

USB2_HSIC_USB_OTG_HS_GEN_CONFIG_2

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12	LINESTATE_DIFF_WAKEUP_EN	chicken bit for CR-0000155486.when this bit is set the USB enables the HW fix for Race condition between the attempt to enter LPM and USB bus reset.Default value is 1.
11	ULPI_LPM_PEND_EN	chicken bit for CR-0000153486.when this bit is set the USB enables the HW fix for Function Control and LPM race condition.Default value is 1.
10	RX_FULL_NAK_EN	chicken bit for CR-0000152878.when this bit is set the USB will respond with NAK's for Host Tokens with very slow AHB and when Streaming mode is enabled. Default value is 1.

USB2_HSIC_USB_OTG_HS_GEN_CONFIG_2 (cont.)

Bits	Name	Description
9	ENDLESS_TD_EN	chicken bit for CR-0000152976. When this bit is set Performance enhancements for 'infinite' Producer pipe (out endpoint with eTD that points to itself) are enabled. Default value is 1.
8	SCRATCH_RAM_EN	chicken bit for CR-0000149922. When this bit is set the use of scratch ram is enabled and the SW can read/write from addresses 0x040 - 0x07c. when this bit is clear SW can no longer access those registers. Default value is 1.
7	SESS_VLD_CTRL_EN	When this bit is set then bit 25 of USBCMD register controls sess_vld signal inside the Link Controller. When this bit is clear then Link Controller receives sess_vld directly from PHY. Default value is 0.
6	CI_T_WTSUSRSTHS_EN	When this bit is 0 then Device Port Control State Machine waits 2.5 us from USB Reset detection until starting driving Chirp K. When this bit is 1 then Device Port Control State Machine waits 1.5 ms from USB Reset detection until starting driving Chirp K. Default value is 1 - legacy behavior.
5	CI_T_UCH_EN	When this bit is 0 then Device Port Control State Machine drives Chirp K for 1 ms. When this bit is 1 then Device Port Control State Machine drives Chirp K for 2ms. Default value is 1 - legacy behavior.
4	DP_RESET	chicken bit for fix CI2687: When the OTG core is acting as a Host, and VBUS is turned off, and the attached Device attempts to perform a Session Request Protocol by using Data-line Pulsing, it will not be recognized by the Host. Also, when doing HNP and becoming a Host, a SE0 is forced in the line causing the OPT TD5.4 test to fail, without the software workaround.
3	ZLP_PRIME	chicken bit for fix CI2655: When using ISO IN endpoints with MULT=3 and low bandwidth system bus access, the controller may enter into a wait loop situation without warning the software. Due to the low bandwidth the last packet from a mult3 sequence may not be fetched in time before the last token IN is received (for that uframe/endpoint). This will cause the controller to reply with a zero length packet (ZLP), breaking the prime sequence.
2	NO_SOF_RX_FIFO_FULL	chicken bit for fix CI2581: During normal operation, if the RX Fifo becomes full and the protocol engine needs to send a command to the DMA state machine, it will wait in that state until the RX Fifo becomes not full. As the protocol state machine also handles the SOF generation, the SOFs will no longer be sent. If one SOF is missed, the Host controller will issue a false babble detection. If more than 3.125ms are elapsed without SOFs the peripheral will recognize the idle bus as a USB reset.
1	WRONG_OPMODE_SUSP	chicken bit for fix CI1274: When the Controller enters a Suspend state it asserts opmode with the wrong value, according to specifications 'UTMI+ Specification, Revision 1.0, Section 3.2' and 'UTMI+ Low Pin Interface Specification, Revision 1.1, Section 3.8.5.3'. This causes no issue in actual usage.

USB2_HSIC_USB_OTG_HS_GEN_CONFIG_2 (cont.)

Bits	Name	Description
0	RESUME_END_INTER	chicken bit for fix CI1179: Working as host, when doing resume a port change interrupt was fired at the end of resume. According to the EHCI spec no interrupt should be fired.

20.30.4 Device/host capability registers

0x12510100 USB2_HSIC_USB_OTG_HS_CAPLENGTH

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x01000040

The USB_OTG_HS_CAPLENGTH register is the capability register length. It is used to indicate which offset to add to the register base address at the beginning of the operational register.

USB2_HSIC_USB_OTG_HS_CAPLENGTH

Bits	Name	Description
31:16	HCIVERSION_15_0	BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.
7:0	CAPLENGTH_7_0	Offset at beginning of operational register

0x12510104 USB2_HSIC_USB_OTG_HS_HCSPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00010011

The USB_OTG_HS_HCSPARAMS register contains the host control structural parameters. The port steering logic capabilities are described in this register.

USB2_HSIC_USB_OTG_HS_HCSPARAMS

Bits	Name	Description
31:28	RESERVED_BITS31_28	Clear (0) these bits.
27:24	N_TT_3_0	Number of transaction translators This field indicates the number of embedded transaction translators associated with the USB2.0 host controller. For a multi-port host, this field will always equal 0001. For all other implementations, N_TT = 0000. This in a non-EHCI field to support embedded TT.

USB2_HSIC_USB_OTG_HS_HCSPARAMS (cont.)

Bits	Name	Description
23:20	N_PTT_3_0	Number of ports per transaction translator This field indicates the number of ports assigned to each transaction translator within the USB2.0 host controller. For a multi-port host this field will always equal N_PORTS. For all other implementations, N_PTT = 0000. This in a non-EHCI field to support embedded TT.
19:17	RESERVED_BITS19_17	Clear (0) these bits.
16	PI_3_0	Port indicator This bit indicates whether the ports support port indicator control. When set (1), the port status and control registers include a read/writable field for controlling the state of the port indicator. This field will always be set (1).
15:12	N_CC_3_0	Number of companion controllers This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no internal companion controllers. Port-ownership hand-off is not supported. A value larger than zero in this field indicates that there are companion USB1.1 host controller(s). Port-ownership hand-offs are supported. High-, full-, and low-speed devices are supported on the host controller root ports. In this implementation, this field will always be clear (0).
11:8	N_PCC_3_0	Number of ports per companion controller This field indicates the number of ports supported per internal companion controller. It is used to indicate the port routing configuration to the system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2, then N_PCC could have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, and so on. In the previous example, the N_PCC could have been 4, where the first 4 are routed to companion controller 1 and the last two are routed to companion controller 2. The number in this field must be consistent with N_PORTS and N_CC. In this implementation, this field will always be clear (0).
7:5	RESERVED_BITS7_5	Clear (0) these bits.
4	PPC	Port power control This field indicates whether the host controller implementation includes port power control. Set (1) indicates that the ports have port power switches. Clear (0) indicates that the ports do not have port power switches. The value of this field affects the functionality of the port power field in each port status and control register. This bit will always be clear (0) for a device only implementation.

USB2_HSIC_USB_OTG_HS_HCSPARAMS (cont.)

Bits	Name	Description
3:0	N_PORTS_3_0	Number of downstream ports This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the operational register. Valid values are in the range of 1h to Fh. A zero in this field is undefined. The number of ports for a host implementation is configurable from 1 to 8. This field will always be set (1) for device-only implementation.

0x12510108 USB2_HSIC_USB_OTG_HS_HCCPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0006

The USB_OTG_HS_HCCPARAMS register contains the host control capability parameters. This register identifies multiple mode control (time-base bit functionality) addressing capability.

USB2_HSIC_USB_OTG_HS_HCCPARAMS

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.
15:8	EECP_7_0	EHCI extended capabilities pointer Default = 0 This optional field indicates the existence of a capabilities list. A value of 00h indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capability. The pointer value must be 40h or greater if implemented to maintain the consistency of the PCI header defined for this class of device. For this implementation, all of these bits are clear (0).
7:4	IST_7_4	Isochronous scheduling threshold Default = implementation dependent This field indicates, relative to the current position of the executing host controller, where the software can reliably update the isochronous schedule. When bit [7] is clear (0), the value of the least significant 3 bits indicates the number of microframes a host controller can hold a set of isochronous data structures (one or more) before flushing the state. When bit [7] is set (1), then host software assumes the host controller may cache an isochronous data structure for an entire frame. All of the bits in this field will always be clear (0).
3	RESERVED_BIT3	Clear (0) this bit.

USB2_HSIC_USB_OTG_HS_HCCPARAMS (cont.)

Bits	Name	Description
2	ASP	Asynchronous schedule park capability Default = 1 If this bit is set (1), then the host controller supports the park feature for high-speed queue heads in the asynchronous schedule. The feature can be disabled, or enabled and set to a specific level by using the (ASPE) and (ASP[1:0]) fields in the USB_OTG_HS_USBCMD register. This field will always be set (1).
1	PFL	Programmable frame list flag If this bit is clear (0), then the system software must use a frame list length of 1024 elements with this host controller. The FS[2:0] field in the USBCMD register is read-only and must be cleared (0). If this bit is set (1), then the system software can specify and use a smaller frame list, and configure the host controller using the FS[2:0] field in the USBCMD register. The frame list must always be aligned on a 4k-page boundary. This requirement ensures that the frame list is always physically contiguous. This bit in this field will always be set (1).
0	ADC	64-bit addressing capability This field will always be clear (0). No 64-bit addressing capability is supported.

0x12510120 USB2_HSIC_USB_OTG_HS_DCIVERSION

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1

The USB_OTG_HS_DCIVERSION register contains the device interface version number. The device controller interface conforms to the two-byte BCD encoding of the interface version number contained in this register.

USB2_HSIC_USB_OTG_HS_DCIVERSION

Bits	Name	Description
15:0	DCIVERSION_15_0	Device interface version number

0x12510124 USB2_HSIC_USB_OTG_HS_DCCPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x190

The USB_OTG_HS_DCCPARAMS register contains the device control capability parameters. These fields describe the overall host/device capability of the controller.

USB2_HSIC_USB_OTG_HS_DCCPARAMS

Bits	Name	Description
31:9	RESERVED_BITS31_9	Clear (0) these bits.
8	HC	Host capable When this bit is set (1), this controller is capable of operating as an EHCI-compatible USB 2.0 host controller.
7	DC	Device capable When this bit is set (1), this controller is capable of operating as a USB 2.0 device.
6:5	RESERVED_BITS6_5	Clear (0) these bits.
4:0	DEN_4_0	Device endpoint number This field indicates the number of endpoints build into the device controller. If this controller is not device capable, then this field will be al zeroes. Valid values for this field are 0 through 16.

20.30.5 Device/host operational registers

0x12510140 USB2_HSIC_USB_OTG_HS_USBCMD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00080000

The USB_OTG_HS_USBCMD register is the USB command register. The serial bus host/device controller executes the command indicated in this register.

USB2_HSIC_USB_OTG_HS_USBCMD

Bits	Name	Description
31	RST_CTRL	Default value = 0. Set to 1 to block operational reset to xcvr (ser and ulpi) clock domains.
30	ULPI_STP_CTRL	Default value = 0. Set to 1 to block the ulpi_stp signal from going out to ULPI PHY
29	ASYNC_INTR_CTRL	Default value = 0. Set to 1 to allow the async interrupt out from the HS core.
28	SE0_GLITCH_FIX_CTRL	Default value = 0. Set to 1 to activate the SE0 glitch fix mechanism
27	FS_3_WIRE_2_WIRE_SELECT	Default value = 0. Set this bit for enabling the two wire interface on the fs_dat and fs_se0 pins

USB2_HSIC_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
26	ULPI_SER3_NOT6_SEL	ULPI serial 3 bits select. Read/write Read: Current status of serial data bus wide Write: SW writes ’1’ to this bit to request 3 pins ULPI data wide, or ’0’ to request 6 bit data wide in FsLsSerial Mode.
25	SESS_VLD_CTRL	Default value = 0. Set this bit to enable Link Controller operation after switching interface from Serial to ULPI.
24	RESERVED_BIT24	Clear (0) these bit
23:16	ITC_7_0	Interrupt threshold control Read/write Default 08h The system software uses this field to set the maximum rate at which the host/device controller will issue interrupts. This field contains the maximum interrupt interval measured in micro-frames. Valid values are shown below. Value Maximum interrupt interval 00h Immediate (no threshold) 01h 1 micro-frame 02h 2 micro-frames 04h 4 micro-frames 08h 8 micro-frames 10h 16 micro-frames 20h 32 micro-frames 40h 64 micro-frames
15	FS2	This field is Read/Write only if Programmable Frame List Flag in the HCCPARAMS registers is set to one. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index. Note that this field is made up from USBCMD bits 15, 3 and 2. Values meaning 000 1024 elements (4096 bytes) Default value 001 512 elements (2048 bytes) 010 256 elements (1024 bytes) 011 128 elements (512 bytes) 100 64 elements (256 bytes) 101 32 elements (128 bytes) 110 16 elements (64 bytes) 111 8 elements (32 bytes) Only the host controller uses this field.

USB2_HSIC_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
14	ATDTW	Add dTD tripwire Read/write (Device mode only) This bit is used as a semaphore to ensure the to proper addition of a new dTD to an active (primed) endpoint's linked list. This bit is set (1) and cleared (0) by the software. This bit shall also be cleared (0) by the hardware when the state machine is a hazard region for which adding a dTD to a primed endpoint may go unrecognized.
13	SUTW	Setup tripwire (device mode only) Read/write This bit is used as a semaphore to ensure that the setup data payload of 8 bytes is extracted from a QH by the DCD without being corrupted. If the setup lockout mode is off (see USBMODE) then there exists a hazard when new setup data arrives while the DCD is copying the setup data payload from the QH for a previous setup packet. This bit is set (1) and cleared (0) by software, and will be cleared (0) by hardware when a hazard exists.
12	RESERVED_BITS12	Clear (0) this bit
11	ASPE	Asynchronous schedule park mode enable (OPTIONAL) Read/write If the asynchronous park capability (ASP) bit in the HCCPARAMS register is set (1), then this bit defaults to a 1h and is R/W. Otherwise, the bit must be cleared (0) and is RO. The software uses this bit to enable or disable the park mode. value 1 = Park mode is enabled. value 0 = Park mode is disabled. This field is set (1) in this implementation.
10	RESERVED_BIT10	Clear (0) this bit.
9:8	ASP_1_0	Asynchronous schedule park mode count (OPTIONAL) Read/write If the Asynchronous park capability (ASP) bit in the HCCPARAMS register is set (1), then this field defaults to 3h and is R/W. Otherwise it defaults to zero and is RO. This field contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid values are 1h to 3h. The software must not clear (0) this bit when the ASPE bit in this register is set (1), as this will result in undefined behavior. This field is set to 3h in this implementation.
7	LR	Light host/device controller reset (OPTIONAL) Read only Not implemented. This bit will always be clear (0).

USB2_HSIC_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
6	IAA	Interrupt on async advance doorbell Read/write This bit is used as a doorbell by the software to tell the host controller to issue an interrupt the next time it advances the asynchronous schedule. The software must set (1) this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule states, it sets (1) the interrupt on the async advance status (AAI) bit in the USBSTS register. If the interrupt on async advance enable (AAE) bit in the USBINTR register is set (1), then the host controller will assert an interrupt at the next interrupt threshold. The host controller clears (0) this bit after it has set (1) the interrupt on async advance status (AAI) bit in the USBSTS register. The software should not set (1) this bit when the asynchronous schedule is inactive. Doing so will yield undefined results. This bit is only used in the host mode. Setting (1) this bit when the device mode is selected will produce undefined results.
5	ASE	Asynchronous Schedule Enable Read/write Default = 0b This bit controls whether the host controller skips processing the asynchronous schedule. value 0 = Do not process the asynchronous schedule value 1 = Use the ASYNCLISTADDR register to access the asynchronous schedule. Only the host controller uses this bit.
4	PSE	Periodic schedule enable Read/write Default 0b This bit controls whether the host controller skips processing the periodic schedule. value 0 = Do not process the periodic schedule value 1 = Use the PERIODICLISTBASE register to access the periodic schedule. Only the host controller uses this bit.

USB2_HSIC_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
3:2	FS_1_0	This field is Read/Write only if Programmable Frame List Flag in the HCCPARAMS registers is set to one. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index. Note that this field is made up from USBCMD bits 15, 3 and 2. Values meaning 000 1024 elements (4096 bytes) Default value 001 512 elements (2048 bytes) 010 256 elements (1024 bytes) 011 128 elements (512 bytes) 100 64 elements (256 bytes) 101 32 elements (128 bytes) 110 16 elements (64 bytes) 111 8 elements (32 bytes) Only the host controller uses this field.
1	RST	Controller reset (RESET) Read/write The software uses this bit to reset the controller. This bit is cleared (0) by the host/device controller when the reset process is complete. The software cannot terminate the reset process early by clearing (0) this bit. Host controller: When the software sets (1) this bit, the host controller resets its internal pipelines, timers, counters, state machines, and so on to their initial values. Any transaction currently in progress on the USB is immediately terminated. A USB reset is not driven on downstream ports. The software should not set (1) this bit when the HCHalted bit in the USBSTS register is clear (0). Attempting to reset an actively running host controller will result in undefined behavior. Device controller: When the software sets (1) this bit, the device controller resets its internal pipelines, timers, counters, state machines, and so on to their initial values. Setting this bit when the device is in the attached state is not recommended, since the effect on an attached host is undefined. In order to ensure that the device is not in an attached state before initiating a device controller reset, all primed endpoints should be flushed and the USBCMD run/stop bit should be cleared (0).

USB2_HSIC_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
0	RS	Run/stop Read/Write Default 0b value 1 = Run value 0 = Stop Host controller: When this bit is set (1), the host controller proceeds with the execution of the schedule. The host controller continues execution as long as this bit remains set (1). When this bit is clear (0), the host controller completes the current transaction on the USB and then halts. The HC halted bit in the status register indicates when the host controller has finished the transaction and has entered the stopped state. The software should not set (1) this bit unless the host controller is in the halted state (that is, the HCHalted bit in the USBSTS register is set (1)). Device controller: Setting (1) this bit will cause the device controller to enable a pull-up on D+ and initiate an attach event. This control bit is not directly connected to the pull-up enable, as the pull-up will become disabled upon transitioning into high-speed mode. The software should use this bit to prevent an attach event before the device controller has been properly initialized. Clearing (0) this bit will cause a detach event.

0x12510144 USB2_HSIC_USB_OTG_HS_USBSTS

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_USBSTS register is the USB status register. This register indicates various states of the host/device controller and any pending interrupts. This register does not indicate status resulting from a transaction on the serial bus. The software clears certain bits in this register by setting (1) them.

USB2_HSIC_USB_OTG_HS_USBSTS

Bits	Name	Description
31	ULPI_INTR	Default value = 0.This bit is set when Interrupt during ULPI -Serial mode or ULPI Interrupt during LPM occurs. Writing a 1 to this bit will clear it.
30	PHY_SESS_VLD_CHG	This bit is set when PHY_SESS_VLD bit changes its value.
29	PHY_SESS_VLD	This bit presents the SESS_VLD status of PHY.

USB2_HSIC_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
28	PHY_ALT_INT	This bit is asserted when a non-USB interrupt from PHY is detected. This interrupt is used for procedures like Battery Charging. This bit is set when bit 7 (alt_int) of RX CMD is high. Writing a 1 to this bit will clear it.
27:26	RESERVED_BITS27_26	Clear (0) these bits.
25	TI1	General purpose timer interrupt 1 (GPTINT1) Read/write control This bit is set (1) when the counter in the GPTIMER1CTRL (non-EHCI) register transitions to zero. Setting (1) this bit will clear it.
24	TI0	General purpose timer interrupt 0 (GPTINT0) Read/write control This bit is set (1) when the counter in the GPTIMER0CTRL (non-EHCI) register transitions to zero. Setting (1) this bit will clear it.
23:20	RESERVED_BITS23_20	Clear (0) these bits.
19	UPI	USB host periodic interrupt (USBHSTPERINT) Read/write control This bit is set (1) by the host controller when the cause of an interrupt is a completion of a USB transaction, where the transfer descriptor (TD) has an interrupt on complete (IOC) bit set (1) and the TD was from the periodic schedule. This bit is also set (1) by the host controller when a short packet is detected AND the packet is on the periodic schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes. This bit is not used by the device controller and will always be clear (0).
18	UAI	USB host asynchronous interrupt (USBHSTASYNCINT) Read/write control This bit is set (1) by the host controller when the cause of an interrupt is a completion of a USB transaction, where the transfer descriptor (TD) has an interrupt on complete (IOC) bit set AND the TD was from the asynchronous schedule. This bit is also set (1) by the host when a short packet is detected AND the packet is on the asynchronous schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes. This bit is not used by the device controller and will always be clear (0).
17	RESERVED_BIT17	Clear (0) these bits.
16	NAKI	NAK interrupt bit Read only This bit is set (1) by the hardware when, for a particular endpoint, both the Tx/Rx endpoint NAK bit and the corresponding Tx/Rx endpoint NAK enable bit are set (1). This bit is automatically cleared (0) by the hardware when all of the enabled Tx/Rx endpoint NAK bits are cleared (0).

USB2_HSIC_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
15	AS	Asynchronous schedule status Read only Default = 0 This bit reports the current real status of the asynchronous schedule. When cleared (0), the asynchronous schedule status is disabled. And, if set (1), the status is enabled. The host controller is not required to immediately disable or enable the asynchronous schedule when software transitions the asynchronous schedule enable bit in the USBCMD register. When this bit and the asynchronous schedule enable bit are the same value, the asynchronous schedule is either enabled (1) or disabled (0). This bit is only used by the host controller.
14	PS	Periodic schedule status Read only Default = 0 This bit reports the current real status of the periodic schedule. When cleared (0), the periodic schedule is disabled. And, if set (1), the status is enabled. The host controller is not required to immediately disable or enable the periodic schedule when software transitions the periodic schedule enable bit in the USBCMD register. When this bit and the periodic schedule enable bit are the same value, the periodic schedule is either enabled (1) or disabled (0). This bit is only used by the host controller.
13	RCL	Reclamation Read only Default = 0 This is a read-only status bit that is used to detect an empty asynchronous schedule. This bit is only used by the host controller.
12	HCH	HC halted Read only Default = 1 This bit is a clear (0) whenever the run/stop bit is set (1). The host controller sets (1) this bit after it has stopped executing, because of the run/stop bit being cleared (0), either by the software or by the host controller hardware (for example, an internal error). This bit is only used by the host controller.
11	RESERVED_BIT11	Clear (0) this bit.
10	ULPII	ULPI interrupt Read/write control Default = 0 When the ULPI viewport is present in the design, an event completion will set (1) this interrupt. This bit is used by both the host and device controllers. It is only present in designs where the configuration constant VUSB_HS_PHY_ULPI = 1.

USB2_HSIC_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
9	RESERVED_BIT9	Clear (0) this bit.
8	SLI	DC suspend Read/write control Default = 0 When a device controller enters a suspend state from an active state, this bit will be set (1). The device controller clears (0) the bit upon exiting from a suspend state. This bit is only used by the device controller.
7	SRI	SOF received Read/write control Default = 0 When the device controller detects a start of (micro) frame, this bit will be set (1). When a SOF is extremely late, the device controller will automatically set (1) this bit to indicate that an SOF was expected. Therefore, this bit will be set (1) roughly every 1 ms in the device FS mode and every 125 ms in the HS mode, and will be synchronized to the actual SOF that is received. Since the device controller is initialized to FS before connect, this bit will be set (1) at an interval of 1 ms during the prelude to connect and chirp. In the host mode, this bit will be set (1) every 125 us and can be used by the host controller driver as a time base. The software writes a 1 to this bit to clear it. This is a non-EHCI status bit.
6	URI	USB reset received Read/write control Default = 0 When the device controller detects a USB reset and enters the default state, this bit will be set (1). The software can set (1) this bit to clear the USB reset received status bit. This bit is only used by the device controller.
5	AAI	Interrupt on async advance Read/write control Default = 0 The system software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by setting (1) the interrupt on async advance doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source. This bit is only used by the host controller.
4	SEI	System error Read/write control This interrupt is triggered when there is an AHB error (HRESP = ERROR) on the AHB Master interface.

USB2_HSIC_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
3	FRI	Frame list rollover Read/write control The host controller sets (1) this bit when the frame list index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the frame list size field of the USBCMD register) is 1024, the frame index register rolls over every time FRINDEX [1 3] toggles. Similarly, if the size is 512, the host controller sets (1) this bit to a one every time FHINDEX [12] toggles. This bit is only used by the host controller.
2	PCI	Port change detect Read/write control The host controller sets (1) this bit when a connect status occurs on any port, a port enable/disable change occurs on any port, or the force port resume bit is set (1) as the result of a J-K transition on the suspended port. The device controller sets (1) this bit when the port controller enters the full or high-speed operational state. When the port controller exits the full or high-speed operation states due to reset or suspend events, the notification mechanisms are the USB reset received bit and the DC suspend bits, respectively. This bit is not EHCI compatible.
1	UEI	USB error interrupt (USBERRINT) Read/write control When completion of a USB transaction results in an error condition, this bit is set (1) by the host/device controller. This bit is set (1) along with the USBINT bit, if the TD on which the error interrupt occurred also had its interrupt-on-complete (IOC) bit set (1). The device controller detects resume signaling only.
0	UI	USB interrupt (USBINT) Read/write control This bit is set (1) by the host/device controller when the cause of an interrupt is a completion of a USB transaction where the transfer descriptor (TD) has an interrupt-on-complete (IOC) bit set (1). This bit is also set (1) by the host/device controller when a short packet is detected. A short packet is when the actual number of bytes received was less than the expected number of bytes.

0x12510148

USB2_HSIC_USB_OTG_HS_USBINTR

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_USBINTR register is the USB interrupt enable register. The interrupts to the software are enabled with this register. An interrupt is generated when a bit is set (1) and the corresponding interrupt is active. The USB status register (USBSTS) still shows interrupt sources, even if they are disabled by the USBINTR register, which allows polling of interrupt events by the software.

USB2_HSIC_USB_OTG_HS_USBINTR

Bits	Name	Description
31	ULPI_INTR_EN	Default value =0.When this bit is a 1 and ULPI_INTR is a 1, the controller will issue an interrupt. The interrupt is acknowledged by software clearing the ULPI_INTR bit.
30	PHY_SESS_VLD_CHG_EN	Default value =0. When this bit is set then Link Controller will issue an interrupt when PHY_SESS_VLD changes its value.
29:26	RESERVED_BITS29_26	Clear (0) these bits.
25	TIE1	General purpose timer interrupt enable 1 When this bit is set (1), and the GPTINT1 bit in the USBSTS register is set (1), the controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the GPTINT1 bit.
24	TIE0	General purpose timer interrupt enable 0 When this bit is set (1), and the GPTINT0 bit in the USBSTS register is set (1), the controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the GPTINT0 bit.
23:20	RESERVED_BITS23_20	Clear (0) these bits.
19	UPIE	USB host periodic interrupt enable When this bit is set (1), and the USBHSTPERINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBHSTPERINT bit.
18	UAIE	USB host asynchronous interrupt enable When this bit is set (1), and the USBHSTASYNCINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBHSTASYNCINT bit.
17	RESERVED_BIT17	Clear (0) this bit.

USB2_HSIC_USB_OTG_HS_USBINTR (cont.)

Bits	Name	Description
16	NAKE	NAK interrupt enable This bit is set (1) by the software if it wants to enable the hardware interrupt for the NAK interrupt bit. If both this bit and the corresponding NAK interrupt bit are set (1), a hardware interrupt is generated.
15:11	RESERVED_BITS15_11	Clear (0) these bits.
10	ULPIE	ULPI enable When this bit is set (1), and the ULPI Interrupt bit in the USBSTS register transitions, the controller will issue and interrupt. The interrupt is acknowledged by the software setting (1) the ULPI interrupt bit. This bit is used by both the host and device controllers. It is only present in designs where configuration constant VUSB_HS_PHY_ULPI = 1.
9	RESERVED_BIT9	Clear (0) this bit.
8	SLE	Sleep enable When this bit is set (1) and the DC suspend bit in the USBSTS register transitions, the device controller will issue an interrupt. The interrupt is acknowledged by the software setting (1) the DC suspend bit. This bit is only used by the device controller.
7	SRE	SOF received enable When this bit is set (1) and the SOF received bit in the USBSTS register is set (1), the device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the SOF received bit.
6	URE	USB reset enable When this bit is set (1) and the USB reset received bit in the USBSTS register is set (1), the device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the USB reset received bit.
5	AAE	Interrupt on async advance enable When this bit is set (1) and the interrupt on async advance bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the interrupt on async advance bit. This bit is only used by the host controller.
4	SEE	System error enable When this bit is set (1) and the system error bit in the USBSTS register is set (1), the host/device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the system error bit.

USB2_HSIC_USB_OTG_HS_USBINTR (cont.)

Bits	Name	Description
3	FRE	Frame list rollover enable When this bit is set (1) and the frame list rollover bit in the USBSTS register is set (1), the host controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the frame list rollover bit. This bit is only used by the host controller.
2	PCE	Port change detect enable When this bit is set (1) and the port change detect bit in the USBSTS register is set (1), the host/device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the port change detect bit.
1	UEE	USB error interrupt enable When this bit is set (1) and the USBERRINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBERRINT bit in the USBSTS register.
0	UE	USB interrupt enable When this bit is set (1) and the USBINT bit in the USBSTS register is set (1), the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBINT bit.

0x1251014C USB2_HSIC_USB_OTG_HS_FRINDEX

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_FRINDEX register is the USB frame index register. This register is used by the host controller to index the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits [N:3] are used to select a particular entry in the periodic frame list during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by the system software in the frame list size field in the USBCMD register.

This register must be written as a DWord. Byte writes produce-undefined results. This register cannot be written unless the host controller is in the 'halted' state, as indicated by the HC halted bit. A write to this register while the run/stop bit is set (1) produces undefined results. Writes to this register also affect the SOF value.

In the device mode, this register is read-only and the device controller updates the FRINDEX [13:3] register from the frame number indicated by the SOF marker. Whenever a SOF is received by the USB bus, FRINDEX [13:3] will be checked against the SOF marker. If FRINDEX [13:3] is different from the SOF marker, FRINDEX [13:3] will be set to the SOF value and FRINDEX [2:0] will be cleared (0) (that is, SOF for a 1-ms frame). If FRINDEX [13:3] is equal to the SOF value, FRINDEX [2:0] will be incremented (that is, SOF for 125-ms micro-frame.

USB2_HSIC_USB_OTG_HS_FRINDEX

Bits	Name	Description
31:14	RESERVED_BITS31_14	Clear (0) these bits.
13:0	FRINDEX_13_0	Frame index The value in this register increments at the end of each time frame (for example, a micro-frame). Bits [N:3] are used for the frame list current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. The following data shows the values of N based on the value of the frame list size field in the USBCMD register when used in host mode. USBCMD [Frame list size] number Elements N 000b (1024) 12 001b (512) 11 010b (256) 10 011b (128) 9 100b (64) 8 101b (32) 7 110b (16) 6 111b (8) 5 In the device mode, the value is the current frame number of the last frame transmitted. It is not used as an index. In either mode, bits 2:0 indicate the current microframe.

0x12510154 USB2_HSIC_USB_OTG_HS_PERIODICLISTBASE

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_PERIODICLISTBASE register is the periodic list base address register. This 32-bit register contains the beginning address of the periodic frame list in the system memory. The HCD loads this register prior to starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the frame index register (FRINDEX) to enable the host controller to step through the periodic frame list in sequence.

NOTE This device is shared between the host controller and device controller operation. For host controller operation, this is the USB_OTG_HS_ PERIODICLISTBASE register. For device controller operation, this is the USB_OTG_HS_DEVICEADDR register.

USB2_HSIC_USB_OTG_HS_PERIODICLISTBASE

Bits	Name	Description
31:12	PERBASE_31_12	Base address (low) These bits correspond to memory address signals [31:12], respectively. Only used by the host controller.
11:0	RESERVED_BITS11_0	This field must be written as zeros. During runtime, the values of these bits are undefined.

0x12510154 USB2_HSIC_USB_OTG_HS_DEVICEADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_DEVICEADDR register is the USB device address register. The upper seven bits of this register represent the device address. After any controller reset or a USB reset, the device address is set to the default address (0). The default address will match all incoming addresses. The software shall reprogram the address after receiving a SET_ADDRESS descriptor.

The USBADRA is used to accelerate the SET_ADDRESS sequence by allowing the DCD to preset the USBADR register before the status phase of the SET_ADDRESS descriptor.

NOTE This device is shared between the host controller and device controller operations. For host controller operation, this is the USB_OTG_HS_ PERIODICLISTBASE register. For device controller operation, this is the USB_OTG_HS_DEVICEADDR register.

USB2_HSIC_USB_OTG_HS_DEVICEADDR

Bits	Name	Description
31:25	USBADR_31_25	Device address These bits correspond to the USB device address.

USB2_HSIC_USB_OTG_HS_DEVICEADDR (cont.)

Bits	Name	Description
24	USBADRA	Device address advance Default = 0 When this bit is clear (0), any writes to USBADR are instantaneous. When this bit is set (1) at the same time or before USBADR is written, the write to the USBADR field is staged and held in a hidden register. After an IN occurs on endpoint 0 and is ACKed, USBADR will be loaded from the holding register. The hardware will automatically clear (0) this bit on the following conditions: 1. IN is ACKed to endpoint 0 (USBADR is updated from staging register). 2. OUT/SETUP occur to endpoint 0 (USBADR is not updated). 3. Device reset occurs (USBADR is reset to 0). Note: After the status phase of the SET_ADDRESS descriptor, the DCD has 2 ms to program the USBADR field. This mechanism will ensure this specification is met when the DCD can not write of the device address within 2 ms from the SET_ADDRESS status phase. If the DCD writes the USBADR with USBADRA = 1 after the SET_ADDRESS data phase (before the prime of the status phase), the USBADR will be programmed instantly at the correct time and meet the 2-ms USB requirement.
23:0	RESERVED_BITS23_0	These bits must be written as zeros. During runtime, the values of these bits are undefined.

0x12510158 USB2_HSIC_USB_OTG_HS_ASYNCLISTADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ASYNCLISTADDR register is the next asynchronous list address register. This 32-bit register contains the address of the next asynchronous queue head to be executed by the host. Bits [4:0] of this register cannot be modified by the system software and will always return a zero when read.

NOTE The USB_OTG_HS_ASYNCLISTADDR register and the USB_OTG_HS_ENDPOINTLISTADDR register are shared between the host controller and device controller operations. For the host controller, this is the USB_OTG_HS_ASYNCLISTADDR register. For the device controller, this is the USB_OTG_HS_ENDPOINTLISTADDR register.

USB2_HSIC_USB_OTG_HS_ASYNCLISTADDR

Bits	Name	Description
31:5	ASYBASE_31_15	Link pointer low (LPL). These bits correspond to memory address signals [31:5], respectively. This field may only reference a queue head (OH). This field is only used by the host controller.
4:0	RESERVED_BITS4_0	The values of these bits has no effect on circuit operation.

0x12510158 USB2_HSIC_USB_OTG_HS_ENDPOINTLISTADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPOINTLISTADDR register is the endpointlist address register. In the device mode, this register contains the address of the top of the endpoint list in system memory. Bits [10:0] of this register cannot be modified by the system software and will always return a zero when read.

NOTE The USB_OTG_HS_ASYNCLISTADDR register and the USB_OTG_HS_ENDPOINTLISTADDR register are shared between the host controller and device controller operations. For the host controller, this is the USB_OTG_HS_ASYNCLISTADDR register. For the device controller, this is the USB_OTG_HS_ENDPOINTLISTADDR register.

USB2_HSIC_USB_OTG_HS_ENDPOINTLISTADDR

Bits	Name	Description
31:11	EPBASE_31_11	Endpoint list pointer (low) These bits correspond to memory address signals [31:11], respectively. This field will reference a list of up to 32 queue heads (QH). That is, one queue head per endpoint & direction.
10:0	RESERVED_BITS10_0	The values of these bits has no effect on circuit operation.

0x1251015C USB2_HSIC_USB_OTG_HS_TTCTRL

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_TTCTRL register is the TT status and control register. This register contains parameters needed for internal TT operations.

NOTE This register is not used in the device controller operation.

USB2_HSIC_USB_OTG_HS_TTCTRL

Bits	Name	Description
31	RESERVED_BIT31	Not used.
30:24	TTHA	Not used.
23:0	RESERVED_BITS23_0	Not used.

0x12510160 USB2_HSIC_USB_OTG_HS_BURSTSIZE

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1010

The USB_OTG_HS_BURSTSIZE register is the programmable burst size register. This register is used to control dynamically change the burst size used during data movement on the initiator (master) interface.

USB2_HSIC_USB_OTG_HS_BURSTSIZE

Bits	Name	Description
31:16	RESERVED_BITS31_16	The value of these bits has no effect on circuit operation.
15:8	TXPBURST	Programmable Tx burst length This register represents the maximum length of a the burst in 32-bit words while moving data from system memory to the USB bus.
7:0	RXPBURST	Programmable Rx burst length This register represents the maximum length of a the burst in 32-bit words while moving data from the USB bus to system memory.

0x12510164 USB2_HSIC_USB_OTG_HS_TXFILLTUNING

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_TXFILLTUNING register is the host transmit pre-buffer packet tuning register. The fields in this register control performance tuning associated with how the host controller posts data to the Tx latency FIFO before moving the data onto the USB bus. The specific areas of performance include the how much data to post into the FIFO and an estimate for how long that operation should take in the target system.

Definitions:

T0 = Standard packet overhead

T1 = Time to send data payload

Tff = Time to fetch packet into TX FIFO up to specified level.

Ts = Total packet flight time (send-only) packet

Ts = T0 + T1

Tp = Total packet time (fetch and send) packet

Tp = Tff + T0 + T1

Upon discovery of a transmit (OUT/SETUP) packet in the data structures, the host controller checks to ensure Tp remains before the end of the [micro] frame. If so it proceeds to pre-fill the TX FIFO. If at anytime during the pre-fill operation the time remaining the [micro] frame is < Ts, then the packet attempt ceases and the packet is tried at a later time. Although this is not an error condition and the host controller will eventually recover, a mark will be made the scheduler health counter to note the occurrence of a ’back-off’ event. When a back-off event is detected, the partial packet fetched may need to be discarded from the latency buffer to make room for periodic traffic that will begin after the next SOF. Too many back-off events can waste bandwidth and power on the system bus, and thus should be minimized (not necessarily eliminated). Back-offs can be minimized with use of the TSCHHEALTH (Tff), as described in the register table.

USB2_HSIC_USB_OTG_HS_TXFILLTUNING

Bits	Name	Description
31:22	RESERVED_BITS31_22	The value of these bits has no effect on circuit operation.
21:16	TXFIFOTHRES	FIFO burst threshold Default = 2 This register controls the number of data bursts that are posted to the TX latency FIFO in the host mode before the packet begins on to the bus. The minimum value is 2 and this value should be a low as possible to maximize USB performance. A higher value can be used in systems with unpredictable latency and/or insufficient bandwidth, where the FIFO may underrun because the data transferred from the latency FIFO to USB occurs before it can be replenished from system memory. This value is ignored if the stream disable bit in USBMODE register is set (1).
15:13	RESERVED_BITS15_13	The value of these bits has no effect on circuit operation.

USB2_HSIC_USB_OTG_HS_TXFILLTUNING (cont.)

Bits	Name	Description
12:8	TXSCHHEALTH	Scheduler health counter Read/write to clear Default = 0 This register increments when the host controller fails to fill the Tx latency FIFO to the level programmed by TXFIFOTHRES before running out of time to send the packet before the next start-of-frame. This health counter measures the number of times this occurs to provide feedback to selecting a proper TXSCHOH. Writing to this register will clear the counter and this counter will be at a maximum at 31.
7:0	TXSCHOH	Scheduler overhead Default = 0 This register adds an additional fixed offset to the schedule time estimator described above as Tff. As an approximation, the value chosen for this register should limit the number of back-off events captured in the TXSCHHEALTH to less than 10 per second in a highly-utilized bus. Choosing a value that is too high for this register is not desired, as it can needlessly reduce USB utilization. The time unit represented in this register is 1.267 ms when a device is connected in the high-speed mode for OTG and SPH. The time unit represented in this register is 6.333 ms when a device is connected in the low/full speed mode for OTG and SPH. The time unit represented in this register is always 1.267 times the MPH product.

0x12510170 USB2_HSIC_USB_OTG_HS_ULPI_VIEWPORT

Type: Read/write (unless otherwise indicated)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x08000000

The USB_OTG_HS_ULPI_VIEWPORT register provides indirect access to the ULPI PHY register set. Although the core performs access to the ULPI PHY register set, there may be extraordinary circumstances where software may need direct access.

CAUTION Writes to the ULPI through the viewport can substantially harm standard USB operations. Currently, no usage model has been defined where the software should need to execute writes directly to the ULPI - see the exception regarding optional features below.

Executing read operations though the ULPI viewport should have no harmful side effects to standard USB operations.

NOTE The ULPI viewport is only synthesized in the design if the constant VUSB_HS_PHY_ULPI is set (1). If the ULPI interface is not enabled, this register will always read zeros.

Two operations can be performed with the ULPI viewport: wake-up and read/write operations. The wake-up operation is used to put the ULPI interface into normal operation mode and re-enable the clock, if necessary. A wake-up operation is required before accessing the registers when the ULPI interface is operating in the low power mode, serial mode, or car kit mode.

The ULPI state can be determined by reading the sync state bit (ULPISS). If this bit is set (1), then the ULPI interface is running in the normal operation mode and can accept read/write operations. If the ULPISS is clear (0), then read/write operations will not be able to execute. Undefined behavior will result if ULPISS = 0, and a read or write operation is performed.

To execute a wake-up operation, write all 32-bits of the ULPI Viewport where ULPIPORT is constructed appropriately, and the ULPIWU bit is set (1) and the ULPIRUN bit is clear (0). Poll the ULPI viewport until ULPIWU is zero for the operation to complete.

To execute a read or write operation, write all 32-bits of the ULPI viewport where ULPIDATWR, ULPIADDR, ULPIPORT, and ULPIRW are constructed appropriately, and the ULPIRUN bit is set (1). Poll the ULPI viewport until ULPIRUN is zero for the operation to complete. Once ULPIRUN is zero, the ULPIDATRD will be valid if the operation was a read.

The polling method above could also be replaced and an interrupt driven using the ULPI interrupt defined in the USBTS and USBINTR registers. When a wake-up or read/write operation completes, the ULPI interrupt will be set (1).

Several optional features may need to be enabled or disabled by the system software as part of system configuration. These bits are contained in the interface and OTG control registers of the ULPI PHY register set. These registers also contain bits that are controlled by the link dynamically and, therefore, should only be modified by the system software using the set/clear access method. Direct writes to these registers could have harmful side effects to the standard USB operations. The following bits are optional bits:

- Bits 3 through 7 in the interface control register
- Bits 6 and 7 in the OTG control register.

Refer to the ULPI Specification Revision 1.1 for further information on the use of the optional features.

USB2_HSIC_USB_OTG_HS_ULPI_VIEWPORT

Bits	Name	Description
31	ULPIWU	ULPI wake-up Setting (1) this bit begins the wake-up operation. The bit will automatically transition to 0 after the wake-up is complete. Once this bit is set (1), the driver can not clear it back to 0. Note: The driver must never execute a wake-up and a read/write operation at the same time.
30	ULPIRUN	ULPI read/write run Setting (1) this bit will begin the read/write operation. The bit will automatically transition to 0 after the read/write is complete. Once this bit is set (1), the driver can not clear it back to 0. Note: The driver must never execute a wakeup and a read/write operation at the same time.

USB2_HSIC_USB_OTG_HS_ULPI_VIEWPORT (cont.)

Bits	Name	Description
29	ULPIRW	ULPI read/write control This bit selects between running a read or write operation. value 0 = Read value 1 = Write
28	ULPIFORCE	ULPI read/write force This bit enables forcing register access during RX packet value 0 = register access is not forced during RX packet (default) value 1 = register access is forced during RX packet reception
27	ULPISS	ULPI sync state Read Only value 1 = Normal sync state value 0 = In another state (for example, car kit, serial, low power) This bit represents the state of the ULPI interface. Before reading this bit, the ULPIPORT field should be set accordingly if used with the multi-port host. Otherwise, this field should always remain 0.
26:24	ULPIPORT	ULPI port number For the wakeup or read/write operation to be executed, this value selects the port number the ULPI PHY is attached to in the multi-port host. The valid range is 0 to 7. This field should always be written as a 0 for the non-multi port products.
23:16	ULPIADDR	ULPI data address When a read or write operation is commanded, the address of the operation is written to this field.
15:8	ULPIDATRD	ULPI data read Read only After a read operation completes, the result is placed in this field.
7:0	ULPIDATWR	ULPI data write When a write operation is commanded, the data to be sent is written to this field.

0x12510178 USB2_HSIC_USB_OTG_HS_ENDPTNAK

Type: Read/write clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTNAK register is the endpoint NAK register.

USB2_HSIC_USB_OTG_HS_ENDPTNAK

Bits	Name	Description
31:16	EPTN_15_0	Tx endpoint NAK Each tx endpoint has 1 bit in this field. The bit is set (1) when the device sends a NAK handshake on a received IN token for the corresponding endpoint. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0
15:0	EPRN_15_0	Rx endpoint NAK Each rx endpoint has 1 bit in this field. The bit is set (1) when the device sends a NAK handshake on a received OUT or PING token for the corresponding endpoint. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x1251017C USB2_HSIC_USB_OTG_HS_ENDPTNAKEN

Type: Read/write clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTNAKEN register is the endpoint NAK enable register.

USB2_HSIC_USB_OTG_HS_ENDPTNAKEN

Bits	Name	Description
31:16	EPTNE_15_0	Tx endpoint NAK enable Each bit is an enable bit for the corresponding Tx endpoint NAK bit. If this bit is set (1) and the corresponding Tx endpoint NAK bit is set (1), the NAK Interrupt bit is set (1). Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0
15:0	EPRNE_15_0	Rx endpoint NAK enable Each bit is an enable bit for the corresponding Rx endpoint NAK bit. If this bit is set (1) and the corresponding Rx endpoint NAK bit is set (1), the NAK Interrupt bit is set (1). Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x12510184 USB2_HSIC_USB_OTG_HS_PORTSC

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xCC000004

This is the USB_OTG_HS_PORTSC register.

USB2_HSIC_USB_OTG_HS_PORTSC

Bits	Name	Description
31:30	PTS	Parallel transceiver select Read/write This register bit pair is used in conjunction with the configuration constant VUSB_HS_PHY_TYPE to control which parallel transceiver interface is selected. If VUSB_HS_PHY_ TYPE is set for 0, 1, 2, or 3, then this bit is read only. If VUSB_HS_PHY_TYPE is 4, 5, 6, or 7, then this bit is read/write. This field is reset to the following values: 00 if VUSB_HS_PHY_TYPE = 0,4 - UTMI/UTMI+ 01 if VUSB_HS_PHY_TYPE = 1,5 - Reserved 10 if VUSB_HS_PHY_TYPE = 2,6 - ULPI 11 if VUSB_HS_PHY_TYPE = 3,7 - Serial/1.1 PHY (FS only) This bit is not defined in the EHCI specification.
29	STS	Serial transceiver select Read/write This register bit is used in conjunction with the configuration constant VUSB_HS_PHY_SERIAL to control whether the parallel or serial transceiver interface is selected for FS and LS operation. The serial interface engine can be used in combination with the UTMI+ or ULPI physical interface to provide FS/LS signaling instead of the parallel interface. ’ If VUSB_HS_PHY_SERIAL is 0 or 1, then this bit is read only. ’ If VUSB_HS_PHY_SERIAL is 2 or 3, then this bit is read/write. This bit has no effect unless the parallel transceiver select is set to UTMI+ or ULPI. The Serial/1.1 physical interface will use the serial interface engine for FS/LS signaling regardless of this bit value. Note: This bit was reserved for future operation, and is now adding for dynamic use of the serial engine in accord with UMTI+ and ULPI characterization logic. This bit is not defined in the EHCI specification.

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
28	PTW	Parallel transceiver width Read/write This register bit is used in conjunction with the configuration constant VUSB_HS_PHY16_8 to control the data bus width of the UTMI transceiver interface. ' If VUSB_HS_PHY16_8 is 0 or 1, then this bit is read only. ' If VUSB_HS_PHY16_8 is 2 or 3, then this bit is read/write. This bit is reset to 1 if VUSB_HS_PHY16_8 selects a default UTMI interface width of 16-bits, else it is reset to 0. ' Writing this bit to 0 selects the 8-bit [60MHz] UTMI interface. ' Writing this bit to 1 selects the 16-bit [30MHz] UTMI interface. This bit has no effect if the serial interface is selected. This bit is not defined in the EHCI specification.
27:26	PSPD	Port speed Read only This register field indicates the speed at which the port is operating. For HS mode operation in the host controller and HS/FS operation in the device controller, the port routing steers data to the protocol engine. For FS and LS mode operation in the host controller, the port routing steers data to the protocol engine with the embedded transaction translator. value 00 = Full speed value 01 = Low speed value 10 = High speed This bit is not defined in the EHCI specification.
25	SPRT	Short Port Reset Time. shortens port reset time for simulation.
24	PFSC	Port force full speed connect Read/write Default = 0 Setting (1) this bit will force the port to only connect at full speed. It also disables the chirp sequence that allows the port to identify itself as high speed. This is useful for testing FS configurations with a HS host, hub or device. This bit is not defined in the EHCI specification. This bit is for debugging purposes.

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
23	PHCD	PHY low power suspend - clock disable (PLPSCD) Read/write Default = 0 value 1 = Disable the PHY clock. value 0 = Enable the PHY clock. Reading this bit will indicate the status of the PHY clock. Note: The PHY clock cannot be disabled if it is being used as the system clock. In the device mode, The PHY can be put into low power suspend - clock disable when the device is not running (USBCMD run/stop = 0) or the host has signaled suspend (PORTSC SUSPEND = 1). Low power suspend will be cleared automatically when the host has signaled resume. Before forcing a resume from the device, the device controller driver must clear this bit. In the host mode, the PHY can be put into low power suspend - clock disable when the downstream device has been put into the suspend mode or when no downstream device is connected. Low power suspend is completely under the control of the software. This bit is not defined in the EHCI specification.
22	WKOC	Wake on over-current enable (WKOC_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to over-current conditions as wake-up events. This bit is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0). This bit is output from the controller as signal pwrctl_wake_ ovrcurr_en (OTG/host core only) for use by an external power control circuit.
21	WKDS	Wake on disconnect enable (WKDSCNNT_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to device disconnects as wake-up events. This field is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0) or in the device mode. This bit is output from the controller as signal pwrctl_wake_ dscnnt_en (OTG/host core only) for use by an external power control circuit.

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
20	WKCN	Wake on connect enable (WKCNNT_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to device connects as wake-up events. This field is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0) or in the device mode. This bit is output from the controller as signal pwrctl_wake_ dscnnt_en (OTG/host core only) for use by an external power control circuit.

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
19:16	PTC_3_0	Port test control Read/write Default = 0000 Any other value than zero indicates that the port is operating in the test mode. Value Specific test The FORCE_ENABLE_FS and FORCE ENABLE_LS tests are extensions to the test mode support, as specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. Note: Low speed operations are not supported as a peripheral device. 0x0: TEST_MODE_DISABLE 0x1: J_ STATE 0x8: K_STATE 0x9: SE0 (host / NAK device) 0x40: Packet 0x41: FORCE_ENABLE_HS 0x48: FORCE_ENABLE_FS 0x49: FORCE_ENABLE_LS 0x3E8: Reserved_1 0x3E9: Reserved_2 0x3EA: Reserved_3 0x3EB: Reserved_4 0x3EC: Reserved_5 0x3ED: Reserved_6 0x3EE: Reserved_7 0x3EF: Reserved_8 0x3F0: Reserved_9 0x3F1: Reserved_10 0x3F2: Reserved_11 0x3F3: Reserved_12 0x3F4: Reserved_13 0x3F5: Reserved_14 0x3F6: Reserved_15 0x3F7: Reserved_16 0x3F8: Reserved_17 0x3F9: Reserved_18 0x3FA: Reserved_19 0x3FB: Reserved_20 0x3FC: Reserved_21 0x3FD: Reserved_22 0x3FE: Reserved_23 0x3FF: Reserved_24

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
19:16	PTC_3_0 (CONTINUED)	0x400: Reserved_25 0x401: Reserved_26 0x402: Reserved_27 0x403: Reserved_28 0x404: Reserved_29 0x405: Reserved_30 0x406: Reserved_31 0x407: Reserved_32 0x408: Reserved_33 0x409: Reserved_34 0x40A: Reserved_35 0x40B: Reserved_36 0x40C: Reserved_37 0x40D: Reserved_38 0x40E: Reserved_39 0x40F: Reserved_40 0x410: Reserved_41 0x411: Reserved_42 0x412: Reserved_43 0x413: Reserved_44 0x414: Reserved_45 0x415: Reserved_46 0x416: Reserved_47 0x417: Reserved_48 0x418: Reserved_49 0x419: Reserved_50 0x41A: Reserved_51 0x41B: Reserved_52 0x41C: Reserved_53 0x41D: Reserved_54 0x41E: Reserved_55 0x41F: Reserved_56 0x420: Reserved_57 0x421: Reserved_58 0x422: Reserved_59 0x423: Reserved_60 0x424: Reserved_61 0x425: Reserved_62 0x426: Reserved_63 0x427: Reserved_64 0x428: Reserved_65 0x429: Reserved_66 0x42A: Reserved_67 0x42B: Reserved_68 0x42C: Reserved_69

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
19:16	PTC_3_0 (CONTINUED)	0x42D: Reserved_70 0x42E: Reserved_71 0x42F: Reserved_72 0x430: Reserved_73 0x431: Reserved_74 0x432: Reserved_75 0x433: Reserved_76 0x434: Reserved_77 0x435: Reserved_78 0x436: Reserved_79 0x437: Reserved_80 0x438: Reserved_81 0x439: Reserved_82 0x43A: Reserved_83 0x43B: Reserved_84 0x43C: Reserved_85 0x43D: Reserved_86 0x43E: Reserved_87 0x43F: Reserved_88 0x440: Reserved_89 0x441: Reserved_90 0x442: Reserved_91 0x443: Reserved_92 0x444: Reserved_93 0x445: Reserved_94 0x446: Reserved_95 0x447: Reserved_96 0x448: Reserved_97 0x449: Reserved_98 0x44A: Reserved_99 0x44B: Reserved_100 0x44C: Reserved_101 0x44D: Reserved_102 0x44E: Reserved_103 0x44F: Reserved_104 0x450: Reserved_105 0x451: Reserved_106 0x452: Reserved_107 0x453: Reserved_108 0x454: Reserved_109 0x455: Reserved_110 0x456: Reserved_111 0x457: Reserved_112

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
15:14	PIC_1_0	Port indicator control Read/write Default = 0 Writing to this field has no effect if the P_INDICATOR bit in the HCSPARAMS register is a zero. If the P_INDICATOR bit is set (1), then this field has the following meanings: Bit value Meaning value 00 Port indicators are off value 01 Amber value 10 Green value 11 Undefined Refer to the USB Specification Revision 2.0 [3] for a description on how these bits are to be used. This field is output from the controller as signals port_ind_ctl_1 and port_ind_ctl_0 for use by an external LED driving circuit.
13	PO	Port owner Read only Port owner hand-off is not implemented in this design, therefore this bit will always read back as clear (0). Default = 0 The EHCI definition is include here for reference: ’ This bit unconditionally goes clear (0) when the configured bit in the CONFIGFLAG register makes a 0-to-1 transition. ’ This bit unconditionally goes set (1) whenever the configured bit is clear (0). The system software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). The software sets (1) this bit when the attached device is not a high-speed device. When this bit is set (1), it indicates that an internal companion controller owns and controls the port.

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
12	PP	Port power (PP) Read/write or read-only The function of this bit depends on the value of the port power switching (PPC) field in the HCSPARAMS register. ’ PPC = 0: PP is read-only. A device controller with no OTG capability does not have port power control switches. ’ PPC = 1: PP is read/write. The host/OTG controller requires port power control switches. This bit represents the current setting of the switch (0 = off, 1 = on). When power is not available on a port (and PP equals a 0), the port is non-functional and will not report attaches, detaches, and so on. When an over-current condition is detected on a powered port and PPC is set (1), the PP bit in each affected port may be transitioned by the host controller driver from a one to a zero, removing power from the port. This feature is implemented in the host/OTG controller (PPC = 1). In a device-only implementation, port power control is not necessary. So, PPC and PP = 0.
11:10	LS_1_0	Line status Read-only These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines: Value Meaning value 00 SE0 value 10 J-state value 01 K-state value 11 Undefined In the host mode, the use of line state by the host controller driver is not necessary (unlike EHCI), because the port controller state machine and the port routing manage the connection of LS and FS. In the device mode, the use of line state by the device controller driver is not necessary.
9	HSP	High-speed port Read-only Default = 0 When the bit is set (1), the host/device connected to the port is in the high-speed mode. When this bit is clear (0), the host/device connected to the port is not in a high-speed mode. Note: HSP is redundant with PSPD(27:26), but will remain in the design for compatibility. This bit is not defined in the EHCI specification.

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
8	PR	Port reset This bit is clear (0) if the port power (PP) bit (bit 12) of this register is clear (0). Host mode: ’ Read/write ’ Default = 0 When the software sets (1) this bit, the bus-reset sequence as defined in the USB Specification Revision 2.0 is started. This bit will automatically clear (go to 0) after the reset sequence is complete. Note: This behavior is different from EHCI, where the host controller driver is required to clear (0) this bit after the reset duration is timed in the driver. Device mode: This bit is a read-only status bit. Device reset from the USB bus is also indicated in the USBSTS register. 0x1: Port is in reset 0x0: Port is not in reset

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
7	SUSP	Suspend Host mode: ’ Read/write ’ Default = 0 The port enabled bit and suspend bit of this register define the port states: Bit value Port state value 0x Disable value 10 Enable value 11 Suspend When in the suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction if a transaction was in progress when this bit set (1). In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. The host controller will unconditionally clear (0) this bit when the software clears (0) the force port resume bit. The host controller ignores a write of zero to this bit. If the host software sets (1) this bit when the port is not enabled (port enabled bit is a zero), the results are undefined. This field is clear (0) if port power (PP) is clear (0) in the host mode. Device mode: ’ Read only ’ Default = 0 In the device mode, this bit is a read-only status bit. 0x1: Port in suspend state_1 0x0: Port not in suspend st_1 0x1: Port in suspend state_2 0x0: Port not in suspend st_2

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
6	FPR	Force port resume ’ Read/write ’ Default = 0 Host mode: The software sets (1) this bit to drive resume signaling. The host controller sets (1) this bit if a J-to-K transition is detected while the port is in the suspend state. When this bit transitions to a one because a J-to-K transition is detected, the port change detect bit in the USBSTS register is also set (1). This bit will automatically clear (go to 0) after the resume sequence is complete. This behavior is different from EHCI, where the host controller driver is required to clear (0) this bit after the resume duration is timed in the driver. Note that, when the host controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (full-speed 'K') is driven on the port as long as this bit remains set (1). This bit will remain set (1) until the port has switched to the high-speed idle. Clearing (0) this bit has no affect, because the port controller will time the resume operation and clear (0) the bit when the port control state switches to HS or FS idle. This bit is clear if the port power (PP) is clear (0) in the host mode. This bit is not-EHCI compatible. Device mode: After the device has been in the suspend state for 5 ms or more, the software must set (1) this bit to drive resume signaling before clearing. The device controller will set (1) this bit if a J-to-K transition is detected while the port is in the suspend state. The bit will be cleared (0) when the device returns to normal operation. Also, when this bit transitions to a one because a J-to-K transition was detected, the port change detect bit in the USBSTS register is also set (1). 0x1: Resume detected/driven on port 0x0: No resume (K-state detected/driven on port)
5	OCC	Over-current change Read/write control Default = 0 This bit gets is set (1) when there is a change to over-current active. The software clears this bit by setting (1) this bit position. For host/OTG implementations, the user can provide over-current detection to the vbus_pwr_fault input for this condition. For device-only implementations, this bit shall always be clear (0).

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
4	OCA	Over-current active Read-only Default = 0 value 1 = This port currently has an over-current condition. value 0 = This port does not have an over-current condition. This bit will automatically transition from set (1) to clear (0) when the over current condition is removed. For host/OTG implementations, the user can provide over-current detection to the vbus_pwr_fault input for this condition. For device-only implementations, this bit shall always be clear (0).
3	PEC	Port enable/disable change Read/write control value 1 = Port enabled/disabled status has changed value 0 = No change Default = 0 Host mode: For the root hub, this bit gets set (1) only when a port is disabled due to disconnect on the port or due to the appropriate conditions existing at the EOF2 point. The software clears this bit by writing a one to it. This field is clear (0) if the port power (PP) bit in the register is clear (0). Device mode: The device port is always enabled (this bit will be zero).
2	PE	Port enabled/disabled Read/write value 1 = Enable value 0 = Disable Default 0 Host mode: Ports can only be enabled by the host controller as a part of the reset and enable. The software cannot enable a port by setting (1) this field. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by the host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port, due to other host controller and bus events. When the port is disabled, (0) downstream propagation of data is blocked except for reset. This field is clear (0) if the port power (PP) bit is cleared (0) in the host mode. Device mode: The device port is always enabled (this bit will be set [1])

USB2_HSIC_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
1	CSC	Connect status change Read/write control value 1 = Change in current connect status value 0 = No change Default = 0 Host mode: Indicates that a change has occurred in the port's current connect status. The host/device controller sets (1) this bit for all changes to the port device connect status, even if the system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, the hub hardware will be 'setting' an already-set bit (that is, the bit will remain set). The software clears this bit by writing a one to it. This field is zero if the port power (PP) bit in this register is zero in the host mode. Device mode: This bit is undefined in the device controller mode.
0	CCS	Current connect status Read-only Host mode: value 1 = Device is present on port value 0 = No device is present Default = 0 This value reflects the current state of the port, and may not correspond directly to the event that caused the connect status change bit (bit 1) to be set (1). This field is clear if the port power (PP) bit in this register is clear (0) in host mode. Device mode: value 1 = Attached value 0 = Not attached Default = 0 If this bit is set (1), this indicates that the device successfully attached, and is operating in either high speed or full speed, as indicated by the high speed port bit in this register. If this bit is clear (0), this indicates that the device did not attach successfully or was forcibly disconnected by the software clearing (0) the run bit in the USBCMD register. It does not state the device being disconnected or suspended.

0x125101A4 USB2_HSIC_USB_OTG_HS_OTGSC

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000E20

USB2_HSIC_USB_OTG_HS_OTGSC

Bits	Name	Description
31	RESERVED_BIT31	Clear (0) this bit.
30	DPIE	Data pulse interrupt enable
29	B_1MSE	1 millisecond timer interrupt enable - read/write
28	BSEIE	B session end interrupt enable Read/write Setting (1) this bit enables the B session end interrupt.
27	BSVIE	B session valid interrupt enable Read/write Setting (1) this bit enables the B session valid interrupt.
26	ASVIE	A session valid interrupt enable Read/write Setting (1) this bit enables the A session valid interrupt.
25	AVVIE	A Vbus valid interrupt enable Read/write Setting (1) this bit enables the A Vbus valid interrupt.
24	IDIE	USB ID interrupt enable Read/write Setting (1) this bit enables the USB ID interrupt.
23	RESERVED_BIT23	Clear (0) this bit.
22	DPIS	Data pulse interrupt status Read/write to clear This bit is set (1) when data bus pulsing occurs on DP or DM. Data bus pulsing is only detected when USBMODE.CM = Host (11) and PORTSC(0). PortPower = Off (0). The software must write a one to clear this bit.
21	B_1MSS	1 millisecond timer interrupt status Read/write to clear This bit is set (1) once every millisecond. The software must write a one to clear this bit.
20	BSEIS	B session end interrupt status Read/write to clear This bit is set (1) when the Vbus has fallen below the B session end threshold. The software must write a one to clear this bit
19	BSVIS	B session valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the B session valid threshold (0.8 VDC). The software must write a one to clear this bit.

USB2_HSIC_USB_OTG_HS_OTGSC (cont.)

Bits	Name	Description
18	ASVIS	A session valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the A session valid threshold (0.8 VDC). The software must write a one to clear this bit.
17	AVVIS	A Vbus valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the Vbus valid threshold (4.4 VDC) on an A device. The software must write a one to clear this bit.
16	IDIS	USB ID interrupt status Read/write This bit is set (1) when a change on the ID input has been detected. The software must write a one to clear this bit.
15	RESERVED_BIT15	Clear (0) this bit.
14	DPS	Data bus pulsing status Read-only If this bit is set (1), it indicates that the data bus pulsing is being detected on the port.
13	B_1MST	1 millisecond timer toggle Read-only This bit toggles once per millisecond.
12	BSE	B session end Read-only Indicates that the Vbus is below the B session end threshold.
11	BSV	B session valid Read-only Indicates that the Vbus is above the B session valid threshold.
10	ASV	A session valid Read-only Indicates that the Vbus is above the A session valid threshold.
9	AVV	A Vbus valid Read-only Indicates that the Vbus is above the A Vbus valid threshold.
8	ID	USB ID Read-only value 0 = A device value 1 = B device

USB2_HSIC_USB_OTG_HS_OTGSC (cont.)

Bits	Name	Description
7	HABA	Hardware assist B-disconnect to A-connect Read/write value 0 = Disabled value 1 = Enable automatic B-disconnect to A-connect sequence.
6	HADP	Hardware assist data-pulse Write to set
5	IDPU	ID pull-up Read/write This bit provides control over the ID pull-up register. value 0 = Off value 1 = On (default) When this bit is clear (0), the ID input will not be sampled.
4	DP	Data pulsing Read/write Setting (1) this bit causes the pull-up on DP to be asserted for data pulsing during SRP.
3	OT	OTG termination Read/write This bit must be set (1) when the OTG device is in the device mode. This controls the pull-down on DM.
2	HAAR	Hardware assist auto-reset Read/write value 0 = Disabled value 1 = Enable automatic reset after connect on host port.
1	VC	Vbus charge Read/write Setting (1) this bit causes the Vbus line to be charged. This is used for Vbus pulsing during SRP.
0	VD	Vbus discharge Read/write Setting (1) this bit causes the Vbus to discharge through a resistor.

0x125101A8 USB2_HSIC_USB_OTG_HS_USBMODE

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_USBMODE register is the USB device mode register.

USB2_HSIC_USB_OTG_HS_USBMODE

Bits	Name	Description
31:6	RESERVED_BITS31_6	Clear (0) these bits.
5	VBPS	Vbus power select value 0 - Output is 0 value 1 - Output is 1 This bit is connected to the vbus_pwr_select output and can be used for any generic control, but is named to be used by logic that selects between an on-chip Vbus power source (charge pump) and an off-chip source in systems when both are available.
4	SDIS	Stream disable mode value 0 = Inactive (default) value 1 = Active Device mode: Setting (1) this bit disables double priming on both the Rx and Tx for low bandwidth systems. This mode ensures that, when the Rx and Tx buffers are sufficient to contain an entire packet, the standard double buffering scheme is disabled to prevent overruns/underruns in bandwidth-limited systems. Note: In the high speed mode, a NYET handshake will respond to all packets received when the stream disable is active. Host mode: Setting (1) this bit ensures that overruns/underruns of the latency FIFO are eliminated for low bandwidth systems where the Rx and Tx buffers are sufficient to contain the entire packet. Enabling the stream disable also has the effect of ensuring that the Tx latency is filled to capacity before the packet is launched onto the USB. Note: Time duration to pre-fill the FIFO becomes significant when the stream disable is active. See TXFILLTUNING and TXTTFILLTUNING [MPH only] to characterize the adjustments needed for the scheduler when using this feature. Note: The use of this feature substantially limits of the overall USB performance.
3	SLOM	Setup lockout mode. In the device mode, this bit controls the behavior of the setup lock mechanism. value 0 = Setup lockouts on (default) value 1 = Setup lockouts off (DCD requires use of a setup data buffer tripwire in USBCMD)

USB2_HSIC_USB_OTG_HS_USBMODE (cont.)

Bits	Name	Description
2	ES	Endian select Read/write This bit can change the byte ordering of the transfer buffers to match the host microprocessor bus architecture. The bit fields in the microprocessor interface and the DMA data structures (including the setup buffer within the device QH) are unaffected by the value of this bit, because they are based upon 32-bit words. value 0 = Little endian (default) - first byte referenced in the least significant byte of a 32-bit word. value 1 = Big endian - first byte referenced in most significant byte of a 32-bit word.
1:0	CM	Controller mode Read/write once The controller mode is defaulted to the proper mode for host-only and device-only implementations. For those designs that contain both host and device capability, the controller will default to an idle state and will need to be initialized to the desired operating mode after reset. For combination host/device controllers, this register can only be written once after reset. If it is necessary to switch modes, the software must reset the controller by writing to the RESET bit in the USBCMD register before reprogramming this register. value 00 = Idle [default for combination host/device] value 01 = Reserved value 10 = Device controller [default for device only controller] value 11 = Host controller [default for host only controller]

0x125101AC USB2_HSIC_USB_OTG_HS_ENPDTSETUPSTAT

Type: Read/write control
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENPDTSETUPSTAT register is the endpoint set-up status register.

USB2_HSIC_USB_OTG_HS_ENPDTSETUPSTAT

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.

USB2_HSIC_USB_OTG_HS_ENPDTSETUPSTAT (cont.)

Bits	Name	Description
15:0	ENDPTSETUPSTAT_15_0	Set-up endpoint status For every set-up transaction that is received, a corresponding bit in this register is set (1). The software must clear or acknowledge the setup transfer by setting (1) a respective bit after it has read the setup data from the queue head. The response to a set-up packet as in the order of operations and total response time is crucial to limit bus time outs while the set-up lock-out mechanism is engaged. See Managing Endpoints in the Device Operational Model. This register is only used in the device mode.

0x125101B0 USB2_HSIC_USB_OTG_HS_ENDPTPRIME

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTPRIME register is the endpoint initialization register. This register is only used in the device mode.

USB2_HSIC_USB_OTG_HS_ENDPTPRIME

Bits	Name	Description
31:16	PETB_15_0	Prime endpoint transmit buffer For each endpoint, a corresponding bit is used to request that a buffer is prepared for a transmit operation in order to respond to a USB IN/INTERRUPT transaction. The software should set (1) the corresponding bit when posting a new transfer descriptor to an endpoint. The hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a transmit buffer. The hardware will clear (0) this bit when the associated endpoint(s) is (are) successfully primed. Note: These bits will be momentarily set (1) by the hardware during hardware re-priming operations when a dTD is retired, and the dQH is updated. PETB[15] - Endpoint 15 PETB[1] - Endpoint 1 PETB[0] - Endpoint 0

USB2_HSIC_USB_OTG_HS_ENDPTPRIME (cont.)

Bits	Name	Description
15:0	PERB_15_0	Prime endpoint receive buffer For each endpoint, a corresponding bit is used to request that a buffer is prepared for a receive operation for when a USB host initiates a USB OUT transaction. The software should set (1) the corresponding bit whenever posting a new transfer descriptor to an endpoint. The hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a receive buffer. The hardware will clear (0) this bit when the associated endpoint(s) is (are) successfully primed. Note: These bits will be momentarily set (1) by the hardware during hardware re-priming operations when a dTD is retired, and the dQH is updated. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x125101B4 USB2_HSIC_USB_OTG_HS_ENDPTFLUSH

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTFLUSH register is the endpoint de-initialize register. This register is only used in the device mode.

USB2_HSIC_USB_OTG_HS_ENDPTFLUSH

Bits	Name	Description
31:16	FETB_15_0	Flush endpoint transmit buffer Setting (1) a bit in this register will cause the associated endpoint to clear any primed buffers. If a packet is in progress for one of the associated endpoints, that transfer will continue until completion. The hardware will clear this register after the endpoint flush operation is successful. FETB[15] - Endpoint 15 FETB[1] - Endpoint 1 FETB[0] - Endpoint 0
15:0	FERB_15_0	Flush endpoint receive buffer Setting a bit (1) will cause the associated endpoint to clear any primed buffers. If a packet is in progress for one of the associated endpoints, that transfer will continue until completion. The hardware will clear this register after the endpoint flush operation is successful. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x125101B8 USB2_HSIC_USB_OTG_HS_ENDPTSTAT

Type: Read-only
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTSTAT register is the endpoint status register. This register is only used in the device mode.

USB2_HSIC_USB_OTG_HS_ENDPTSTAT

Bits	Name	Description
31:16	ETBR_15_0	Endpoint transmit buffer ready One bit for each endpoint indicates the status of the respective endpoint buffer. This bit is set (1) by the hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There will always be a delay between setting (1) a bit in the ENDPTPRIME register and the endpoint indicating that it is ready. This delay time varies based upon the current USB traffic and the number of bits set (1) in the ENDPTPRIME register. The buffer ready status is cleared by a USB reset, by the USB DMA system, or through the ENDPTFLUSH register. Note: These bits will be momentarily cleared by the hardware during hardware endpoint re-priming operations when a dTD is retired, and the dQH is updated. ETBR[15] - Endpoint 15 ETBR[1] - Endpoint 1 ETBR[0] - Endpoint 0
15:0	ERBR_15_0	Endpoint receive buffer ready One bit for each endpoint indicates the status of the respective endpoint buffer. This bit is set (1) by the hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There will always be a delay between setting (1) a bit in the ENDPTPRIME register and the endpoint indicating that it is ready. This delay time varies based upon the current USB traffic and the number of bits set (1) in the ENDPTPRIME register. The buffer ready status is cleared by a USB reset, by the USB DMA system, or through the ENDPTFLUSH register. Note: These bits will be momentarily cleared by the hardware during hardware endpoint re-priming operations when a dTD is retired, and the dQH is updated. ERBR[15] - Endpoint 15 ERBR[1] - Endpoint 1 ERBR[0] - Endpoint 0

0x125101BC USB2_HSIC_USB_OTG_HS_ENDPTCOMPLETE

Type: Read/write control
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The register is the endpoint complete register. This register is only used in the device mode.

USB2_HSIC_USB_OTG_HS_ENDPTCOMPLETE

Bits	Name	Description
31:16	ETCE_15_0	Endpoint transmit complete event Each bit indicates that a transmit event (IN/INTERRUPT) occurred and the software should read the corresponding endpoint queue to determine the endpoint status. If the corresponding IOC bit is set (1) in the transfer descriptor, then this bit will be set (1) simultaneously with the USBINT. Writing a one will clear the corresponding bit in this register. ETCE[15] - Endpoint 15 ETCE[1] - Endpoint 1 ETCE[0] - Endpoint 0
15:0	ERCE_15_0	Endpoint receive complete event Each bit indicates that a received event (OUT/SETUP) occurred and the software should read the corresponding endpoint queue to determine the transfer status. If the corresponding IOC bit is set (1) in the transfer descriptor, then this bit will be set (1) simultaneously with the USBINT. Writing a one will clear the corresponding bit in this register. ERCE[15] - Endpoint 15 ERCE[1] - Endpoint 1 ERCE[0] - Endpoint 0

0x125101C0 USB2_HSIC_USB_OTG_HS_ENDPTCTRL0

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00800080

The USB_OTG_HS_ENDPTCTRL0 register is the endpoint control 0 register. Every device will implement endpoint0 as a control endpoint.

USB2_HSIC_USB_OTG_HS_ENDPTCTRL0

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.

USB2_HSIC_USB_OTG_HS_ENDPTCTRL0 (cont.)

Bits	Name	Description
23	TXE	Tx endpoint enable value 1 = Enabled Endpoint0 is always enabled. Read only
22:20	RESERVED_BITS22_20	Clear (0) these bits.
19:18	TXT	Tx endpoint type Read only value 00 = Control Endpoint0 is fixed as a control end point.
17	RESERVED_BIT17	Clear (0) this bit.
16	TXS	Tx endpoint stall Read/write value 0 = End point OK (default) value 1 = End point stalled The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. It will continue returning STALL until the bit is cleared (0) by the software or it will automatically be cleared (0) upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). Note: There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. In most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15:8	RESERVED_BITS15_8	Clear (0) these bits.
7	RXE	Rx endpoint enable value 1 = Enabled Endpoint0 is always enabled. Read only
6:4	RESERVED_BITS6_4	Clear (0) these bits.
3:2	RXT	Rx endpoint type Read only value 00 = Control Endpoint0 is fixed as a control end point.
1	RESERVED_BIT1	Clear (0) this bit.

USB2_HSIC_USB_OTG_HS_ENDPTCTRL0 (cont.)

Bits	Name	Description
0	RXS	Rx endpoint stall Read/write value 0 = End point OK (default) value 1 = End point stalled The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. It will continue returning STALL until the bit is cleared (0) by the software or it will automatically be cleared (0) upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). Note: There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. In most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

0x125101C0+4*n USB2_HSIC_USB_OTG_HS_ENDPTCTRLn, n=[1..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTCTRLn register is the endpoint control n register. There is an ENDPTCTRLn register for each endpoint in a device.

CAUTION If one endpoint direction is enabled and the paired endpoint of the opposite direction is disabled, then the unused direction type must be changed from the default control-type to any other type (such as bulk-type). Leaving an unconfigured endpoint control will cause undefined behavior for the data PID tracking on the active endpoint/direction.

USB2_HSIC_USB_OTG_HS_ENDPTCTRLn

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.
23	TXE	Tx endpoint enable value 0 = Disabled (default) value 1 = Enabled An endpoint should be enabled only after it has been configured.

USB2_HSIC_USB_OTG_HS_ENDPTCTRLn (cont.)

Bits	Name	Description
22	TXR	Tx data toggle reset (WS) value 1 = Reset PID sequence Whenever a configuration event is received for this endpoint, the software must set (1) this bit in order to synchronize the data PIDs between the host and device.
21	TXI	Tx data toggle inhibit value 0 = PID sequencing enabled (default) value 1 = PID sequencing disabled This bit is only used for testing and should always be cleared (0). Setting (1) this bit will cause this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.
20	RESERVED_BIT20	Clear (0) this bit.
19:18	TXT	Tx endpoint type value 00 = Control value 01 = Isochronous value 10 = Bulk value 11 = Interrupt
17	TXD	Tx endpoint data source value 0 = Dual port memory buffer/DMA engine (default) This bit should always be cleared (0).
16	TXS	Tx endpoint stall value 0 = End point OK value 1 = End point stalled This bit will be cleared (0) automatically upon receipt of a SETUP request if this endpoint is configured as a control endpoint, and this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. This control will continue to STALL until this bit is either cleared (0) by the software or automatically cleared (0) as described above for control endpoints. Note (control endpoint types only): There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. in most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15:8	RESERVED_BITS15_8	Clear (0) these bits.
7	RXE	Rx endpoint enable value 0 = Disabled (default) value 1 = Enabled An endpoint should be enabled only after it has been configured.

USB2_HSIC_USB_OTG_HS_ENDPTCTRLn (cont.)

Bits	Name	Description
6	RXR	Rx data toggle reset (WS) Write 1 = Reset PID sequence Whenever a configuration event is received for this endpoint, the software must set (1) this bit in order to synchronize the data PIDs between the host and the device.
5	RXI	Rx data toggle inhibit value 0 = Disabled (default) value 1 = Enabled This bit is only used for testing and should always be cleared (0). Setting (1) this bit will cause this endpoint to ignore the data toggle sequence and always accept a data packet regardless of their data PID.
4	RESERVED_BIT4	Clear (0) this bit.
3:2	RXT	Rx endpoint type value 00 = Control value 01 = Isochronous value 10 = Bulk value 11 = Interrupt
1	RXD	Rx endpoint data sink value 0 = Dual port memory buffer/DMA engine (default) This bit should always be cleared (0).
0	RXS	Rx endpoint stall value 0 = End point OK value 1 = End point stalled This bit will be cleared (0) automatically upon receipt of a SETUP request if this endpoint is configured as a control endpoint, and this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. This control will continue to STALL until this bit is either cleared (0) by the software or automatically cleared (0) as described above for control endpoints. Note (control endpoint types only): There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. in most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

0x125101FC+4*n USB2_HSIC_USB_OTG_HS_ENDPT_PIPE_IDn, n=[1..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x001F001F

The USB_OTG_HS_ENDPT_PIPE_IDn register is the endpoint pipe number register. There is an USB_OTG_HS_ENDPT_PIPE_IDn register for each endpoint in a device.

NOTE reset value of TX_PIPE_ID and RX_PIPE_ID is 0x1F, which means that Endpoint is not mapped to any pipe.

USB2_HSIC_USB_OTG_HS_ENDPT_PIPE_IDn

Bits	Name	Description
31:21	RESERVED_BITS31_21	Clear (0) these bits.
20:16	TX_PIPE_ID	This field indicate the pipe number that this tx end point (n) will use in pipe mode.
15:5	RESERVED_BITS15_5	Clear (0) these bits.
4:0	RX_PIPE_ID	This field indicate the pipe number that this rx end point (n) will use in pipe mode.

0x12510240 USB2_HSIC_USB_OTG_HS_PHY_CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0b1110000111010

The USB_OTG_HS_PHY_CTRL register is used to configure various features in the Synopsys 28nm PHY.

USB2_HSIC_USB_OTG_HS_PHY_CTRL

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12	USB2_PHY_IDHV_CLAMP_EN	Clamp enable for IDHV interrupt level shifter from USB VDD180 domain to VDDCX domain. When set (1), VLS is active and IDHV interrupt is translated from 1.8V domain to Vddcx domain. When clear (0), VLS is clamped high. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.
11	USB2_PHY_OTGSESSVLDHV_CLAMP_EN	Clamp enable for OTGSESSVLDHV interrupt level shifter from USB VDD180 domain to VDDCX domain. When set (1), VLS is active and OTGSESSVLDHV interrupt is translated from 1.8V domain to Vddcx domain. When clear (0), VLS is clamped to zero. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.

USB2_HSIC_USB_OTG_HS_PHY_CTRL (cont.)

Bits	Name	Description
10	PHY_MPM_HV_CLAMP_EN	Clamp enable for HV interrupts level shifters from USB VDD180 domain to VDDPAD MPM in usb2 phy wrapper. When set (1), VLS is active and HV interrupts are translated from 1.8V domain to MPM Vdd domain. When clear (0), VLS is clamped to inactive state. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.
9	USB2_PHY_OTGSESSVLD HV_INTEN	Enable HV session valid interrupt from phy. This interrupt translated with level shifter for wakeup from retention when VDDCX is nominal and TCXO is running.
8	USB2_PHY_IDHV_INTEN	Enable HV id pin interrupt from phy. This interrupt translated with level shifter for wakeup from retention when VDDCX is nominal and TCXO is running.
7	USB2_PHY_ULPI_POR	Reset for ULPI PHY Wrapper and ULPI clock domain logic in usb2_phy_wrapper.
6:4	USB2_PHY_FSEL	Reference Clock Frequency Select 011 (Assumes 19.2MHz default)
3	HOST_PORTCTRL_FORCE _SUSEN	Chicken bit for CR-0000153908 - when this bit set the core will enter to low power mode when portctrl host sm enter to suspend mode. Default value is 1.
2	USB2_PHY_SIDDQ	IDDQ Test Enable.
1	USB2_PHY_RETEN	Retention mode enable/disable
0	USB2_PHY_POR	Power-On-Reset (Analog configuration needs to happen before POR is set to 0)

0x12510244 USB2_HSIC_USB_OTG_HS_GENERIC1

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

The USB_OTG_HS_GENERIC1 register.

USB2_HSIC_USB_OTG_HS_GENERIC1

Bits	Name	Description
31:16	USB_HS_TX_DEPTH	TX_DEPTH is the number of words in the TX buffer. This number is calculated by the number of bytes allocated per Endpoint divided by 4, times the number of endpoints. The RAM width is 36. In HS USB this value is usually 512 bytes per EP, and for FS ONLY USB it is usually 64 Bytes per EP.
15:0	USB_HS_RX_DEPTH	RX_DEPTH is the number of words in the RX buffer. This number is usually 256, but can support powers of 2 up to 4096. The RAM width is 36.

0x12510248 USB2_HSIC_USB_OTG_HS_GENERIC2

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

The USB_OTG_HS_GENERIC2 register.

USB2_HSIC_USB_OTG_HS_GENERIC2

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.
15	USE_SPS_AHB2AHB	USE_SPS_AHB2AHB generic specifies if AHB2AHB bridge is connected between BAM and SPS Fabric AHB.
14	LPM_SUPPORT	The LPM_SUPPORT generic specifies if USB support Link Power Management.
13:9	USB_HS_DEV_EP	The number of USB endpoints. Valid values for the number of Endpoints are 4, 8, and 16
8:3	MAX_PIPES	The number of simultaneous parallel pipes supported by the BAM. Supported values are 2 to 30
2	USE_SPS	The USE_SPS generic specifies if Bam is connected to USB core.
1	USE_HSIC	The USE_HSIC generic specifies if an HSIC is connected to USB core.
0	UTMI_PHY_SW_IF_EN	The UTMI_PHY_SW_IF_EN generic specifies if UTMI phy Register Interface is enabled

0x12510250 USB2_HSIC_USB_OTG_HS_L1_EP_CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0000FFFF

The USB_OTG_HS_L1_EP_CTRL register enables/disables transition to L1 and exit from L1 state when specific TX endpoints are primed.

USB2_HSIC_USB_OTG_HS_L1_EP_CTRL

Bits	Name	Description
31:16	TX_EP_PRIME_L1_EXIT	Those bit's enables Remote Wakeup in L1 state when SW starts Priming The specific Endpoint.
15:0	TX_EP_PRIME_L1_EN	Control bit's that enables/disables transition to L1 when the specific TX Endpoint is active.

0x12510254 USB2_HSIC_USB_OTG_HS_L1_CONFIG

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_L1_CONFIG register is used to configure various L1 features.

USB2_HSIC_USB_OTG_HS_L1_CONFIG

Bits	Name	Description
31:12	RESERVED_BITS31_12	Clear (0) these bits.
11	PLL_PWR_DWN_EN	Control bit that enables/disables power down of 480 MHZ PLL in L1 state.
10	PHY_LPM_EN	Control bit that enable/disables entering ULPI Low Power Mode in L1 state
9	GATE_AHB_CLK_EN	Control bit that enable/disables clock request signaling for usb_ahb_clk in L1 state
8	GATE_FS_XCVR_CLK_EN	Control bit that enable/disables clock gating of usb_fs_xcvr_clk in L1 state
7	GATE_SYS_CLK_EN	Control bit that enable/disables clock gating of usb_system_clk in L1 state
6	GATE_XCVR_CLK_EN	Control bit that enable/disables power-down of 480 MHz PLL in L1 state
5	L1_REMOTE_WAKEUP_EN	Control bit that enables/disables Remote Wakeup in L1 state. When this bit is low, then Link Controller never initiates Remote Wakeup in L1 state. When this bit is high, Link Controller can initiate Remote Wakeup.
4	LPM_EN	Control bit that enables/disables LPM support. When this bit is zero a full backward compatibility is ensured - no LPM support and no response for LPM Extended Transaction
3:0	PLL_TURNOFF_MIN_HIRD	Specifying a minimum expected HIRD value from Host that enables HW mechanism for turning off the 480 MHz PLL. The default value is 50us.

0x12510258 USB2_HSIC_USB_OTG_HS_LPM_DEBUG_1

Type: Read/Clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_DEBUG_1 register is for debug and testing purposes mostly.

USB2_HSIC_USB_OTG_HS_LPM_DEBUG_1

Bits	Name	Description
31:16	DEBUG_L1_LONG_ENT_CNT	Count number of exits from L1 where duration in L1 is > 200us. Writing to this register clears the counter.
15:0	DEBUG_L1_SHORT_ENT_CNT	Count number of exits from L1 where duration in L1 is <= 200us. Writing to this register clears the counter.

0x1251025C USB2_HSIC_USB_OTG_HS_LPM_DEBUG_2

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_DEBUG_2 register is for debug and testing purposes mostly.

USB2_HSIC_USB_OTG_HS_LPM_DEBUG_2

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12:9	L1_RMT_WKUP_TIME	Read/write Specifying How much time the device drives remote wakeup. The default Value is 50us for reset value. Add the value of this register (in us) to the remote wakeup time.
8	L1_FPR	Read/write L1 Force port resume, The software sets (1) this bit to drive resume signaling.
7	HSIC_CLK_PLL_BYPASSNL	Read only. Disables PLL analog logic. Active low. Connects to bypassnl input of NT_PLL.
6	HSIC_CLK_PLL_RESET	Read only. Resets all FF in PLL. Active low. Connects to reset_n input of NT_PLL.
5	HSIC_CLK_GATE	Read only. Clock gating of hsic_clk and ulpi_clk, without turning off HSIC PLL.
4	FS_XCVR_CLK_GATE	Read only. Clock gating of cc_usb_xcvr_fs_clk
3	SYS_CLK_GATE	Read only. Clock gating of cc_usb_system_clk
2	AHB_CLK_GATE	Read only. Clock gating of usb_ahb_clk

USB2_HSIC_USB_OTG_HS_LPM_DEBUG_2 (cont.)

Bits	Name	Description
1	L1_STATE	Read only. Status bit indicating if Device is in L1 state. When this bit high, Link Controller and HSIC PHY are in L1 state
0	DEBUG_L1_EN	Read/write Control bit that enable/disables DEBUG counters operation.

0x12510260 USB2_HSIC_USB_OTG_HS_LPM_ATTRIBUTES

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_ATTRIBUTES register store the bmAttribute Field of the LPM transaction.

USB2_HSIC_USB_OTG_HS_LPM_ATTRIBUTES

Bits	Name	Description
31:5	RESERVED_BITS31_5	Clear (0) these bits.
4	BREMOTEWAKE	A value of one (1B) in this field enables the addressed device to wake the host upon any meaningful application-specific event (e.g. an interrupt for a device with one or more interrupt endpoints). A value of zero (0B) disables the device from initiating remote wake.
3:0	HIRD	Host Initiated Resume Duration.

20.31 USB3 OTG HS Registers (0x12520000 USB3_HS_BASE)

This section contains USB3 OTG HS registers.

20.31.1 Identification registers

Identification registers are used to declare the slave interface presence and include a table of the hardware configuration parameters.

0x12520000 USB3_HS_USB_OTG_HS_ID

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0042FA05

The USB_OTG_HS_ID register is the identification register. It provides a simple way to determine if the USB-HS USB 2.0 core is provided in the system. The ID register identifies the USB-HS USB 2.0 core and its revision.

USB3_HS_USB_OTG_HS_ID

Bits	Name	Description
31:24	RESERVED_BITS31_24	These bits are reserved and should be set to zero.
23:16	REVISON_7_0	This field contains the revision number of the core - 0x42.
15:8	NID_5_0	This field contains the complement version of ID[7:0] - 0xFA.
7:0	ID_5_0	This field is the configuration number. This number is set to 0x05 and indicates that the peripheral is the USB-HS USB 2.0 core.

0x12520004 USB3_HS_USB_OTG_HS_HWGENERAL

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x5C2

The USB_OTG_HS_HWGENERAL register contains the general hardware parameters.

USB3_HS_USB_OTG_HS_HWGENERAL

Bits	Name	Description
31:10	RESERVED_BITS31_10	Clear (0) these bits.
9	SM	VUSB_HS_PHY_SERIAL = 2
8:6	PHYM	VUSB_HS_PHY_TYPE = 7
5:4	PHYW	VUSB_HS_PHY16_8 = 0

USB3_HS_USB_OTG_HS_HWGENERAL (cont.)

Bits	Name	Description
3	BWT	This bit is reserved for internal testing = 0
2:1	CLCK	VUSB_HS_CLOCK_CONFIGURATION = 1
0	RT	VUSB_HS_RESET_TYPE = 0

0x12520008 USB3_HS_USB_OTG_HS_HWHOST

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x10020001

The USB_OTG_HS_HWHOST register contains the host hardware parameters.

USB3_HS_USB_OTG_HS_HWHOST

Bits	Name	Description
31:24	TTPER	VUSB_HS_TT_PERIODIC_CONTEXTS
23:16	TTASY	VUSB_HS_TT_ASYNC_CONTEXTS
15:4	RESERVED_BITS15_4	Clear (0) these bits.
3:1	NPORT	VUSB_HS_NUM_PORT-1
0	HC	VUSB_HS_HOST

0x1252000C USB3_HS_USB_OTG_HS_HWDEVICE

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000021

The USB_OTG_HS_HWDEVICE register contains the device hardware parameters.

USB3_HS_USB_OTG_HS_HWDEVICE

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:1	DEVEP	VUSB_HS_DEV_EP
0	DC	Device capable; [VUSB_HS_DEV/=0]

0x12520010 USB3_HS_USB_OTG_HS_HWTXBUF

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x80070B08

The USB_OTG_HS_HWTXBUF register contains the Tx buffer hardware parameters.

USB3_HS_USB_OTG_HS_HWTXBUF

Bits	Name	Description
31	TXLCR	This bit is fixed to 1'b1 so that the local context register's are included in the design. This means that the DMA context is implemented in FlipFlops.
30:24	RESERVED_BITS30_24	Clear (0) these bits.
23:16	TXCHANADD	VUSB_HS_TX_CHAN_ADD - Defines the number of address lines needed per Endpoint per the TX latency buffer. It's reset value is taken from a GENERIC value passed to the core.
15:8	TXADD	VUSB_HS_TX_ADD - Defines the number of address lines needed per the entire TX latency buffer. It's reset value is taken from a GENERIC value passed to the core.
7:0	TXBURST	VUSB_HS_TX_BURST - Defines the data burst length of the AHB master interface in Quad-words (4-byte increments) of the TX data. It's reset value is taken from a GENERIC value passed to the core. Note that the actual burst length will depend on the settings of USB_OTG_HS_AHB_MODE and USB_OTG_HS_AHB_BURST registers.

0x12520014 USB3_HS_USB_OTG_HS_HWRXBUF

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000808

The USB_OTG_HS_HWRXBUF register contains the Rx buffer hardware parameters.

USB3_HS_USB_OTG_HS_HWRXBUF

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits).
15:8	RX_ADD	VUSB_HS_RX_ADD - Defines the number of address lines needed per the entire RX latency buffer. It's reset value is taken from a GENERIC value passed to the core.

USB3_HS_USB_OTG_HS_HWRXBUF (cont.)

Bits	Name	Description
7:0	RX_BURST	VUSB_HS_RX_BURST - Defines the data burst length of the AHB master interface in Quad-words (4-byte increments) of the RX data. It's reset value is taken from a GENERIC value passed to the core. Note that the actual burst length will depend on the settings of USB_OTG_HS_AHB_MODE and USB_OTG_HS_AHB_BURST registers.

0x12520040+4*n USB3_HS_USB_OTG_HS_SCRATCH_RAMn, n=[0..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

USB_OTG_HS_SCRATCH_RAMn registers are 16 32bit scratch registers.Required for passing USB software information between different images.

USB3_HS_USB_OTG_HS_SCRATCH_RAMn

Bits	Name	Description
31:0	SCRATCH_REGISTER	32 bit scratch register

20.31.2 Device/host timer registers

The host/device controller drivers can measure time related activities using these timer registers.

NOTE These registers are not part of the standard EHCI controller.

0x12520080 USB3_HS_USB_OTG_HS_GPTIMER0LD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER0LD register is the general purpose timer 0 load register. This register contains the timer duration or load value. See the GPTIMER0CTRL register for a description of the timer functions.

USB3_HS_USB_OTG_HS_GPTIMER0LD

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.

USB3_HS_USB_OTG_HS_GPTIMER0LD (cont.)

Bits	Name	Description
23:0	GPTLD	General purpose timer load value. This field is the value to be loaded into the GPTCNT countdown timer on a reset action. This value in this register represents the time in microseconds minus 1 for the timer duration. Example: for a one millisecond timer, load 1000-1=999 or 0x0003E7. Note: Max value is 0xFFFFFF or 16.777215 seconds

0x12520084 USB3_HS_USB_OTG_HS_GPTIMER0CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER0CTRL register is the general purpose timer 0 control register. This register contains the control for the timer and a data field can be queried to determine the running count value. This timer has a granularity of 1 ms and can be programmed to a little over 16 seconds. There are two modes supported by this timer: the first is a one-shot and the second is a looped count, which is described in the register table below. When the timer counter value transitions to zero, an interrupt can be generated though the use of the timer interrupts in the USBTS and USBINTR registers.

USB3_HS_USB_OTG_HS_GPTIMER0CTRL

Bits	Name	Description
31	GTPRUN	General purpose timer run Read/write value 0 = Timer stop value 1 = Timer run This bit enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.
30	GPTRST	General purpose timer reset Write-only value 0 = No action value 1 = Load counter value Writing a one to this bit will reload the GPTCNT with the value in GPTLD.
29:25	RESERVED_BITS29_25	Clear (0) these bits.

USB3_HS_USB_OTG_HS_GPTIMER0CTRL (cont.)

Bits	Name	Description
24	GPTMODE	General purpose timer mode Read/write value 0 = One shot value 1 = Repeat This bit selects between a single timer countdown and a looped count down. In the one-shot mode, the timer will count down to zero, generate an interrupt, and stop until the counter is reset by the software. In the repeat mode, the timer will count down to zero, generate an interrupt, and automatically reload the counter to begin again.
23:0	GPTCNT	General purpose timer counter Read-only This field is the value of the running timer.

0x12520088 USB3_HS_USB_OTG_HS_GPTIMER1LD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER1LD register is the general purpose timer 1 control register. This register contains the timer duration or load value. See the GPTIMER0LDregister for a description of the timer functions.

USB3_HS_USB_OTG_HS_GPTIMER1LD

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.
23:0	GPTLD	General purpose timer load value. This field is the value to be loaded into the GPTCNT countdown timer on a reset action. This value in this register represents the time in microseconds minus 1 for the timer duration. Example: for a one millisecond timer, load 1000-1=999 or 0x0003E7. Note: Max value is 0xFFFFFF or 16.777215 seconds.

0x1252008C USB3_HS_USB_OTG_HS_GPTIMER1CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER1CTRL register is the general purpose timer 1 control register. See the description of the USB_OTG_HS_GPTIMER0CTRL register for details about this register.

USB3_HS_USB_OTG_HS_GPTIMER1CTRL

Bits	Name	Description
31	GTPRUN	General purpose timer run Read/write value 0 = Timer stop value 1 = Timer run This bit enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.
30	GPTRST	General purpose timer reset Write-only value 0 = No action value 1 = Load counter value Writing a one to this bit will reload the GPTCNT with the value in GPTLD.
29:25	RESERVED_BITS29_25	Clear (0) these bits.
24	GPTMODE	General purpose timer mode Read/write value 0 = One shot value 1 = Repeat This bit selects between a single timer countdown and a looped count down. In the one-shot mode, the timer will count down to zero, generate an interrupt, and stop until the counter is reset by the software. In the repeat mode, the timer will count down to zero, generate an interrupt, and automatically reload the counter to begin again.
23:0	GPTCNT	General purpose timer counter Read-only This field is the value of the running timer.

20.31.3 Wrapper operational registers

0x12520090 USB3_HS_USB_OTG_HS_AHB_BURST

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_AHB_BURST register determines the AHB master mode of the USB HS Core.

NOTE If the USB_OTG_HS_AHB_MODE is configured to be 0x0 (the AHB Transactor is used), this register must be 0x0 as well, otherwise the AHB Master bus behavior is undefined. Use values other than 0x0 only if setting USB_OTG_HS_AHB_MODE to 0x1.

USB3_HS_USB_OTG_HS_AHB_BURST

Bits	Name	Description
31:3	RESERVED_BITS31_3	Should be set to zero.
2:0	AHB_BURST	AMBA AHB BURST. This is a r/w field that selects the following options for the m_hburst signal of the AMBA master interface: In all cases where the unspecified length burst is allowed, singles access may also occur, this is mostly true when the transaction is not 32-bit aligned. Two consecutive single accesses should not happen. When a INCRx burst size is selected and the transfer is not multiple of the INCRx burst, the burst is decomposed in the different ways. With AHBBRST[2] = 1, the smaller bursts will be unspecified length. with AHBBRST[2] = 0, the smaller bursts will be smaller INCRx or singles. For example, lets say that it's required at a given time, to transfer 22 words of information, for the following values of AHBBRST the master sequence will be: This field after reset is set to a default value that can be configured in the file vusb_hs_cfg.vhd. The AHBBRST field is only used if the AMBA-AHB system interface has been selected. It has no effect for cores featuring BVCI interface. In the later case the read will return zeros. When this field is different from zero, the value of the fields TXBURST /RXBURST in register BURSTSIZE 160h, will be ignored by the controller. Internally the BURSTSIZE will be set to the value of the INCRx AMBA burst. Since this has a direct relation with the burst sizes you must be careful with AHB burst selected. Although the TXBURST / RXBURST are bypassed, this register can still be written / read with no effect, while the AHBBRST field is non-zero. 0x0: INCR burst of unspecified length 0x1: INCR4, non-multiple transfers of INCR4 will be decomposed into singles 0x2: INCR8, non-multiple transfers of INCR8, will be decomposed into INCR4 or singles 0x3: INCR16, non-multiple transfers of INCR16, will be decomposed into INCR8, INCR4 or singles 0x4: This value is reserved and should not be used 0x5: INCR4, non-multiple transfers of INCR4 will be decomposed into smaller unspecified length bursts 0x6: INCR8, non-multiple transfers of INCR8 will be decomposed into smaller unspecified length bursts 0x7: INCR16, non-multiple transfers of INCR16 will be decomposed into smaller unspecified length bursts 0x5: INCR4+ INCR4 +INCR4+ INCR4 +INCR4+ INCR unspec. length 0x6: INCR8+INCR8+INCR4+ INCR unspec. length 0x7: INCR16+INCR4+ INCR unspec. length 0x1: INCR4+ INCR4 +INCR4+ INCR4 +INCR4+SINGLE+SINGLE 0x2: INCR8+INCR8+INCR4+SINGLE+SINGLE 0x3: INCR16+INCR4+SINGLE+SINGLE

0x12520094 USB3_HS_USB_OTG_HS_XTOR_STS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_XTOR_STS register is currently a placeholder for future status bits from the AHB2AHB Transactor.

USB3_HS_USB_OTG_HS_XTOR_STS

Bits	Name	Description
31:2	RESERVED_BITS31_2	Not used currently.
1	GRANT_STOLEN	Reports whether the arbiter removed the hgrant signal prior to completing a transaction. This is currently supported in WRITES ONLY. This bit can be cleared by writing a ’1’ to the GRANT_STOLEN_CLEAR bit in the USB_OTG_HS_AHB_MODE register. To enable this bit again, write a ’0’ to he GRANT_STOLEN_CLEAR bit in the USB_OTG_HS_AHB_MODE register.
0	RESERVED_BIT0	Not used currently.

0x12520098 USB3_HS_USB_OTG_HS_AHB_MODE

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1

USB3_HS_USB_OTG_HS_AHB_MODE

Bits	Name	Description
31	ASYNC_BRIDGES_BYPASS	Default is ’0’. When ’0’ the asynchronous bridge on the master AHB interface is used. When ’1’, it is bypassed. The bridge on the slave AHB is always used.
30:5	RESERVED_BITS30_5	Not used currently.
4	INCR_OVERRIDE	Valid only if the Transactor is bypassed: When ’1’, all INCR bursts from the USB Core will be internally transformed into SINGLE transfers. When ’0’, if the USB Core issues an INCR burst, it will propagate to the external master AHB port.

USB3_HS_USB_OTG_HS_AHB_MODE (cont.)

Bits	Name	Description
3:2	HPROT_MODE	When ’00’ the HPROT signal out of the USB Wrapper is ’0001’, and all transactions are non-posted. When ’01’ the HPROT signal out of the USB Wrapper is ’0101’, and all transactions are posted. When ’10’ the HPROT signal out of the USB Wrapper alternates according to the context of the AHB bus access. Control structures are non-posted while data transfer is posted. When ’11’, reserved value, but currently maps to non-posted (same as ’00’).
1	GRANT_STOLEN_CLEAR	Clears the grant stolen field of the USB_OTG_HS_XTOR_STS register. To enable this bit again, write ’0’ after clearing the GRANT_STOLEN (’1’).
0	XTOR_BYPASS	When this bit is set (1), the AHB Transactor is bypassed, and the USB HS Core’s AHB Master interface is directly connected to the AHB system. In this case, the USB_OTG_HS_AHB_BURST register value will determine the bus characteristics. When this bit is reset (0), the AHB Transactor is used to connect the USB HS Core to the AHB system.

0x1252009C USB3_HS_USB_OTG_HS_GEN_CONFIG

Type: Read/write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXX0830

The USB_OTG_HS_GEN_CONFIG register is used to configure various features that have been added to the HS USB Core.

USB3_HS_USB_OTG_HS_GEN_CONFIG

Bits	Name	Description
31:16	USB_OTG_HS_HW_QVERSION	HW revision of the USB OTG HS core. This version changes with every official release of USB_OTG_HS core.
15	SYS_CLK_SW_EN	This bit is applicable only in SPS Device mode. When this bit is set then USB core always voting for USB_SYSTEM_CLK. Default value is 0 - USB core doesn’t request USB_SYSTEM_CLK when in Low Power Mode.
14	TESTMUX_SEL_4	see TESTMUX_SEL_3_0 the first 4 bits of this register.
13	USB_BAM_DISABLE	This bit disables the bam logic inside the USB and makes him work in Legacy mode.
12	DMA_HPROT_CTRL	When this bit is set Link Controller always does non-posted dQH writes.
11	ISO_FIX_EN	This bit enables fix for Isochronous bug in CI core (CR--0000135251).

USB3_HS_USB_OTG_HS_GEN_CONFIG (cont.)

Bits	Name	Description
10	DSC_PE_RST_EN	This bit enables an automatic reset of Device PE State Machine on disconnection event when operating as device. This reset is a HW fix for CR-000940.
9	HOST_SIM_TIMERS_EN_SUSP	When this bit is set (1), the timers used for the USB suspend process short for faster simulation and ATE time. When this bit is clear(0), the timers used for the USB suspend process are according to the USB specification.
8	HOST_SIM_TIMERS_EN_STD	When this bit is set (1), the timers used for the USB reset on the ULPI are short for faster simulation and ATE time. When this bit is clear(0), the timers used for the USB reset on the ULPI are according to the USB specification.
7	PE_RX_BUF_PENDING_EN	This is only valid in Device Mode. Setting this bit will cause to store a Transaction Status Tag in the Pending register instead of RX Buffer if the RX Buffer is full. The Tag will move from Pending register to RX Buffer as soon as it becomes not full.
6	STREAM_RX_BYPASS_ENABLE	This is only valid in Device Mode. If SDIS bit is set (bit 4 of USB_OTG_HS_USBMODE (0x1A8)), i.e., streaming mode is disabled, setting this bit will cause the RX traffic to override the SDIS bit, and to receive in streaming mode. TX will still be in non-streaming mode.
5	ULPI_SERIAL_EN	This bit must be set to enable operation of ULPI Serial FS/LS mode. Default state is ’1’ - ULPI Serial mode is supported.
4	PE_DP_TXFIFO_IDLE_FORCE	This is only valid in Device Mode. Setting this bit to ’1’ forces the dp_tx_fifo_cmd_dev to be equal to PE_DP_TXFIFO_IDLE when Device PE state machine in REPORT_NAK state and the RX Buffer is full. This bit is used to enable fix of CR-001612. Reset value is ’1’.

USB3_HS_USB_OTG_HS_GEN_CONFIG (cont.)

Bits	Name	Description
3:0	TESTMUX_SEL_3_0	With TESTMUX_SEL_4 select one of the following test buses: Value 00001 Key state machines 01101 hsic_test_bus1 01110 hsic_test_bus2 10000 dma_eng_3 dma_dev_sm_2 10001 dma_eng_4 dma_traf others zeros 0x2: dma_eng_0 dma_dev_sm_1 0x3: dma_eng_1 dma_context 0x4: dma_eng_2 dma_mem_arb 0x5: prot_eng_0 0x6: prot_eng_1 0x7: prot_eng_2 0x8: port_ctrl_0 0x9: port_ctrl_1 0xA: tx_buffer 0xB: rx_buffer 0xC: otg

0x125200A0 USB3_HS_USB_OTG_HS_GEN_CONFIG_2

Type: Read/write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0001F60

Register for the chicken bits. The USB_OTG_HS_GEN_CONFIG_2 register is used to configure various features that have been added to the HS USB Core. By default, all chicken bits are off and the fix is applicable.

USB3_HS_USB_OTG_HS_GEN_CONFIG_2

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12	LINESTATE_DIFF_WAKEUP_EN	chicken bit for CR-0000155486.when this bit is set the USB enables the HW fix for Race condition between the attempt to enter LPM and USB bus reset.Default value is 1.
11	ULPI_LPM_PEND_EN	chicken bit for CR-0000153486.when this bit is set the USB enables the HW fix for Function Control and LPM race condition.Default value is 1.
10	RX_FULL_NAK_EN	chicken bit for CR-0000152878.when this bit is set the USB will respond with NAK's for Host Tokens with very slow AHB and when Streaming mode is enabled. Default value is 1.

USB3_HS_USB_OTG_HS_GEN_CONFIG_2 (cont.)

Bits	Name	Description
9	ENDLESS_TD_EN	chicken bit for CR-0000152976. When this bit is set Performance enhancements for 'infinite' Producer pipe (out endpoint with eTD that points to itself) are enabled. Default value is 1.
8	SCRATCH_RAM_EN	chicken bit for CR-0000149922. When this bit is set the use of scratch ram is enabled and the SW can read/write from addresses 0x040 - 0x07c. when this bit is clear SW can no longer access those registers. Default value is 1.
7	SESS_VLD_CTRL_EN	When this bit is set then bit 25 of USBCMD register controls sess_vld signal inside the Link Controller. When this bit is clear then Link Controller receives sess_vld directly from PHY. Default value is 0.
6	CI_T_WTSUSRSTHS_EN	When this bit is 0 then Device Port Control State Machine waits 2.5 us from USB Reset detection until starting driving Chirp K. When this bit is 1 then Device Port Control State Machine waits 1.5 ms from USB Reset detection until starting driving Chirp K. Default value is 1 - legacy behavior.
5	CI_T_UCH_EN	When this bit is 0 then Device Port Control State Machine drives Chirp K for 1 ms. When this bit is 1 then Device Port Control State Machine drives Chirp K for 2ms. Default value is 1 - legacy behavior.
4	DP_RESET	chicken bit for fix CI2687: When the OTG core is acting as a Host, and VBUS is turned off, and the attached Device attempts to perform a Session Request Protocol by using Data-line Pulsing, it will not be recognized by the Host. Also, when doing HNP and becoming a Host, a SE0 is forced in the line causing the OPT TD5.4 test to fail, without the software workaround.
3	ZLP_PRIME	chicken bit for fix CI2655: When using ISO IN endpoints with MULT=3 and low bandwidth system bus access, the controller may enter into a wait loop situation without warning the software. Due to the low bandwidth the last packet from a mult3 sequence may not be fetched in time before the last token IN is received (for that uframe/endpoint). This will cause the controller to reply with a zero length packet (ZLP), breaking the prime sequence.
2	NO_SOF_RX_FIFO_FULL	chicken bit for fix CI2581: During normal operation, if the RX Fifo becomes full and the protocol engine needs to send a command to the DMA state machine, it will wait in that state until the RX Fifo becomes not full. As the protocol state machine also handles the SOF generation, the SOFs will no longer be sent. If one SOF is missed, the Host controller will issue a false babble detection. If more than 3.125ms are elapsed without SOFs the peripheral will recognize the idle bus as a USB reset.
1	WRONG_OPMODE_SUSP	chicken bit for fix CI1274: When the Controller enters a Suspend state it asserts opmode with the wrong value, according to specifications 'UTMI+ Specification, Revision 1.0, Section 3.2' and 'UTMI+ Low Pin Interface Specification, Revision 1.1, Section 3.8.5.3'. This causes no issue in actual usage.

USB3_HS_USB_OTG_HS_GEN_CONFIG_2 (cont.)

Bits	Name	Description
0	RESUME_END_INTER	chicken bit for fix CI1179: Working as host, when doing resume a port change interrupt was fired at the end of resume. According to the EHCI spec no interrupt should be fired.

20.31.4 Device/host capability registers

0x12520100 USB3_HS_USB_OTG_HS_CAPLENGTH

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x01000040

The USB_OTG_HS_CAPLENGTH register is the capability register length. It is used to indicate which offset to add to the register base address at the beginning of the operational register.

USB3_HS_USB_OTG_HS_CAPLENGTH

Bits	Name	Description
31:16	HCIVERSION_15_0	BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.
7:0	CAPLENGTH_7_0	Offset at beginning of operational register

0x12520104 USB3_HS_USB_OTG_HS_HCSPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00010011

The USB_OTG_HS_HCSPARAMS register contains the host control structural parameters. The port steering logic capabilities are described in this register.

USB3_HS_USB_OTG_HS_HCSPARAMS

Bits	Name	Description
31:28	RESERVED_BITS31_28	Clear (0) these bits.
27:24	N_TT_3_0	Number of transaction translators This field indicates the number of embedded transaction translators associated with the USB2.0 host controller. For a multi-port host, this field will always equal 0001. For all other implementations, N_TT = 0000. This in a non-EHCI field to support embedded TT.

USB3_HS_USB_OTG_HS_HCSPARAMS (cont.)

Bits	Name	Description
23:20	N_PTT_3_0	Number of ports per transaction translator This field indicates the number of ports assigned to each transaction translator within the USB2.0 host controller. For a multi-port host this field will always equal N_PORTS. For all other implementations, N_PTT = 0000. This in a non-EHCI field to support embedded TT.
19:17	RESERVED_BITS19_17	Clear (0) these bits.
16	PI_3_0	Port indicator This bit indicates whether the ports support port indicator control. When set (1), the port status and control registers include a read/writable field for controlling the state of the port indicator. This field will always be set (1).
15:12	N_CC_3_0	Number of companion controllers This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no internal companion controllers. Port-ownership hand-off is not supported. A value larger than zero in this field indicates that there are companion USB1.1 host controller(s). Port-ownership hand-offs are supported. High-, full-, and low-speed devices are supported on the host controller root ports. In this implementation, this field will always be clear (0).
11:8	N_PCC_3_0	Number of ports per companion controller This field indicates the number of ports supported per internal companion controller. It is used to indicate the port routing configuration to the system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2, then N_PCC could have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, and so on. In the previous example, the N_PCC could have been 4, where the first 4 are routed to companion controller 1 and the last two are routed to companion controller 2. The number in this field must be consistent with N_PORTS and N_CC. In this implementation, this field will always be clear (0).
7:5	RESERVED_BITS7_5	Clear (0) these bits.
4	PPC	Port power control This field indicates whether the host controller implementation includes port power control. Set (1) indicates that the ports have port power switches. Clear (0) indicates that the ports do not have port power switches. The value of this field affects the functionality of the port power field in each port status and control register. This bit will always be clear (0) for a device only implementation.

USB3_HS_USB_OTG_HS_HCSPARAMS (cont.)

Bits	Name	Description
3:0	N_PORTS_3_0	Number of downstream ports This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the operational register. Valid values are in the range of 1h to Fh. A zero in this field is undefined. The number of ports for a host implementation is configurable from 1 to 8. This field will always be set (1) for device-only implementation.

0x12520108 USB3_HS_USB_OTG_HS_HCCPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0006

The USB_OTG_HS_HCCPARAMS register contains the host control capability parameters. This register identifies multiple mode control (time-base bit functionality) addressing capability.

USB3_HS_USB_OTG_HS_HCCPARAMS

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.
15:8	EECP_7_0	EHCI extended capabilities pointer Default = 0 This optional field indicates the existence of a capabilities list. A value of 00h indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capability. The pointer value must be 40h or greater if implemented to maintain the consistency of the PCI header defined for this class of device. For this implementation, all of these bits are clear (0).
7:4	IST_7_4	Isochronous scheduling threshold Default = implementation dependent This field indicates, relative to the current position of the executing host controller, where the software can reliably update the isochronous schedule. When bit [7] is clear (0), the value of the least significant 3 bits indicates the number of microframes a host controller can hold a set of isochronous data structures (one or more) before flushing the state. When bit [7] is set (1), then host software assumes the host controller may cache an isochronous data structure for an entire frame. All of the bits in this field will always be clear (0).
3	RESERVED_BIT3	Clear (0) this bit.

USB3_HS_USB_OTG_HS_HCCPARAMS (cont.)

Bits	Name	Description
2	ASP	Asynchronous schedule park capability Default = 1 If this bit is set (1), then the host controller supports the park feature for high-speed queue heads in the asynchronous schedule. The feature can be disabled, or enabled and set to a specific level by using the (ASPE) and (ASP[1:0]) fields in the USB_OTG_HS_USBCMD register. This field will always be set (1).
1	PFL	Programmable frame list flag If this bit is clear (0), then the system software must use a frame list length of 1024 elements with this host controller. The FS[2:0] field in the USBCMD register is read-only and must be cleared (0). If this bit is set (1), then the system software can specify and use a smaller frame list, and configure the host controller using the FS[2:0] field in the USBCMD register. The frame list must always be aligned on a 4k-page boundary. This requirement ensures that the frame list is always physically contiguous. This bit in this field will always be set (1).
0	ADC	64-bit addressing capability This field will always be clear (0). No 64-bit addressing capability is supported.

0x12520120 USB3_HS_USB_OTG_HS_DCIVERSION

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1

The USB_OTG_HS_DCIVERSION register contains the device interface version number. The device controller interface conforms to the two-byte BCD encoding of the interface version number contained in this register.

USB3_HS_USB_OTG_HS_DCIVERSION

Bits	Name	Description
15:0	DCIVERSION_15_0	Device interface version number

0x12520124 USB3_HS_USB_OTG_HS_DCCPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x190

The USB_OTG_HS_DCCPARAMS register contains the device control capability parameters. These fields describe the overall host/device capability of the controller.

USB3_HS_USB_OTG_HS_DCCPARAMS

Bits	Name	Description
31:9	RESERVED_BITS31_9	Clear (0) these bits.
8	HC	Host capable When this bit is set (1), this controller is capable of operating as an EHCI-compatible USB 2.0 host controller.
7	DC	Device capable When this bit is set (1), this controller is capable of operating as a USB 2.0 device.
6:5	RESERVED_BITS6_5	Clear (0) these bits.
4:0	DEN_4_0	Device endpoint number This field indicates the number of endpoints build into the device controller. If this controller is not device capable, then this field will be al zeroes. Valid values for this field are 0 through 16.

20.31.5 Device/host operational registers

0x12520140 USB3_HS_USB_OTG_HS_USBCMD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00080000

The USB_OTG_HS_USBCMD register is the USB command register. The serial bus host/device controller executes the command indicated in this register.

USB3_HS_USB_OTG_HS_USBCMD

Bits	Name	Description
31	RST_CTRL	Default value = 0. Set to 1 to block operational reset to xcvr (ser and ulpi) clock domains.
30	ULPI_STP_CTRL	Default value = 0. Set to 1 to block the ulpi_stp signal from going out to ULPI PHY
29	ASYNC_INTR_CTRL	Default value = 0. Set to 1 to allow the async interrupt out from the HS core.
28	SE0_GLITCH_FIX_CTRL	Default value = 0. Set to 1 to activate the SE0 glitch fix mechanism
27	FS_3_WIRE_2_WIRE_SELECT	Default value = 0. Set this bit for enabling the two wire interface on the fs_dat and fs_se0 pins

USB3_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
26	ULPI_SER3_NOT6_SEL	ULPI serial 3 bits select. Read/write Read: Current status of serial data bus wide Write: SW writes ’1’ to this bit to request 3 pins ULPI data wide, or ’0’ to request 6 bit data wide in FsLsSerial Mode.
25	SESS_VLD_CTRL	Default value = 0. Set this bit to enable Link Controller operation after switching interface from Serial to ULPI.
24	RESERVED_BIT24	Clear (0) these bit
23:16	ITC_7_0	Interrupt threshold control Read/write Default 08h The system software uses this field to set the maximum rate at which the host/device controller will issue interrupts. This field contains the maximum interrupt interval measured in micro-frames. Valid values are shown below. Value Maximum interrupt interval 00h Immediate (no threshold) 01h 1 micro-frame 02h 2 micro-frames 04h 4 micro-frames 08h 8 micro-frames 10h 16 micro-frames 20h 32 micro-frames 40h 64 micro-frames
15	FS2	This field is Read/Write only if Programmable Frame List Flag in the HCCPARAMS registers is set to one. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index. Note that this field is made up from USBCMD bits 15, 3 and 2. Values meaning 000 1024 elements (4096 bytes) Default value 001 512 elements (2048 bytes) 010 256 elements (1024 bytes) 011 128 elements (512 bytes) 100 64 elements (256 bytes) 101 32 elements (128 bytes) 110 16 elements (64 bytes) 111 8 elements (32 bytes) Only the host controller uses this field.

USB3_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
14	ATDTW	Add dTD tripwire Read/write (Device mode only) This bit is used as a semaphore to ensure the to proper addition of a new dTD to an active (primed) endpoint's linked list. This bit is set (1) and cleared (0) by the software. This bit shall also be cleared (0) by the hardware when the state machine is a hazard region for which adding a dTD to a primed endpoint may go unrecognized.
13	SUTW	Setup tripwire (device mode only) Read/write This bit is used as a semaphore to ensure that the setup data payload of 8 bytes is extracted from a QH by the DCD without being corrupted. If the setup lockout mode is off (see USBMODE) then there exists a hazard when new setup data arrives while the DCD is copying the setup data payload from the QH for a previous setup packet. This bit is set (1) and cleared (0) by software, and will be cleared (0) by hardware when a hazard exists.
12	RESERVED_BITS12	Clear (0) this bit
11	ASPE	Asynchronous schedule park mode enable (OPTIONAL) Read/write If the asynchronous park capability (ASP) bit in the HCCPARAMS register is set (1), then this bit defaults to a 1h and is R/W. Otherwise, the bit must be cleared (0) and is RO. The software uses this bit to enable or disable the park mode. value 1 = Park mode is enabled. value 0 = Park mode is disabled. This field is set (1) in this implementation.
10	RESERVED_BIT10	Clear (0) this bit.
9:8	ASP_1_0	Asynchronous schedule park mode count (OPTIONAL) Read/write If the Asynchronous park capability (ASP) bit in the HCCPARAMS register is set (1), then this field defaults to 3h and is R/W. Otherwise it defaults to zero and is RO. This field contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid values are 1h to 3h. The software must not clear (0) this bit when the ASPE bit in this register is set (1), as this will result in undefined behavior. This field is set to 3h in this implementation.
7	LR	Light host/device controller reset (OPTIONAL) Read only Not implemented. This bit will always be clear (0).

USB3_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
6	IAA	Interrupt on async advance doorbell Read/write This bit is used as a doorbell by the software to tell the host controller to issue an interrupt the next time it advances the asynchronous schedule. The software must set (1) this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule states, it sets (1) the interrupt on the async advance status (AAI) bit in the USBSTS register. If the interrupt on async advance enable (AAE) bit in the USBINTR register is set (1), then the host controller will assert an interrupt at the next interrupt threshold. The host controller clears (0) this bit after it has set (1) the interrupt on async advance status (AAI) bit in the USBSTS register. The software should not set (1) this bit when the asynchronous schedule is inactive. Doing so will yield undefined results. This bit is only used in the host mode. Setting (1) this bit when the device mode is selected will produce undefined results.
5	ASE	Asynchronous Schedule Enable Read/write Default = 0b This bit controls whether the host controller skips processing the asynchronous schedule. value 0 = Do not process the asynchronous schedule value 1 = Use the ASYNCLISTADDR register to access the asynchronous schedule. Only the host controller uses this bit.
4	PSE	Periodic schedule enable Read/write Default 0b This bit controls whether the host controller skips processing the periodic schedule. value 0 = Do not process the periodic schedule value 1 = Use the PERIODICLISTBASE register to access the periodic schedule. Only the host controller uses this bit.

USB3_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
3:2	FS_1_0	This field is Read/Write only if Programmable Frame List Flag in the HCCPARAMS registers is set to one. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index. Note that this field is made up from USBCMD bits 15, 3 and 2. Values meaning 000 1024 elements (4096 bytes) Default value 001 512 elements (2048 bytes) 010 256 elements (1024 bytes) 011 128 elements (512 bytes) 100 64 elements (256 bytes) 101 32 elements (128 bytes) 110 16 elements (64 bytes) 111 8 elements (32 bytes) Only the host controller uses this field.
1	RST	Controller reset (RESET) Read/write The software uses this bit to reset the controller. This bit is cleared (0) by the host/device controller when the reset process is complete. The software cannot terminate the reset process early by clearing (0) this bit. Host controller: When the software sets (1) this bit, the host controller resets its internal pipelines, timers, counters, state machines, and so on to their initial values. Any transaction currently in progress on the USB is immediately terminated. A USB reset is not driven on downstream ports. The software should not set (1) this bit when the HCHalted bit in the USBSTS register is clear (0). Attempting to reset an actively running host controller will result in undefined behavior. Device controller: When the software sets (1) this bit, the device controller resets its internal pipelines, timers, counters, state machines, and so on to their initial values. Setting this bit when the device is in the attached state is not recommended, since the effect on an attached host is undefined. In order to ensure that the device is not in an attached state before initiating a device controller reset, all primed endpoints should be flushed and the USBCMD run/stop bit should be cleared (0).

USB3_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
0	RS	Run/stop Read/Write Default 0b value 1 = Run value 0 = Stop Host controller: When this bit is set (1), the host controller proceeds with the execution of the schedule. The host controller continues execution as long as this bit remains set (1). When this bit is clear (0), the host controller completes the current transaction on the USB and then halts. The HC halted bit in the status register indicates when the host controller has finished the transaction and has entered the stopped state. The software should not set (1) this bit unless the host controller is in the halted state (that is, the HCHalted bit in the USBSTS register is set (1)). Device controller: Setting (1) this bit will cause the device controller to enable a pull-up on D+ and initiate an attach event. This control bit is not directly connected to the pull-up enable, as the pull-up will become disabled upon transitioning into high-speed mode. The software should use this bit to prevent an attach event before the device controller has been properly initialized. Clearing (0) this bit will cause a detach event.

0x12520144 USB3_HS_USB_OTG_HS_USBSTS

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_USBSTS register is the USB status register. This register indicates various states of the host/device controller and any pending interrupts. This register does not indicate status resulting from a transaction on the serial bus. The software clears certain bits in this register by setting (1) them.

USB3_HS_USB_OTG_HS_USBSTS

Bits	Name	Description
31	ULPI_INTR	Default value = 0.This bit is set when Interrupt during ULPI -Serial mode or ULPI Interrupt during LPM occurs. Writing a 1 to this bit will clear it.
30	PHY_SESS_VLD_CHG	This bit is set when PHY_SESS_VLD bit changes its value.
29	PHY_SESS_VLD	This bit presents the SESS_VLD status of PHY.

USB3_HS_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
28	PHY_ALT_INT	This bit is asserted when a non-USB interrupt from PHY is detected. This interrupt is used for procedures like Battery Charging. This bit is set when bit 7 (alt_int) of RX CMD is high. Writing a 1 to this bit will clear it.
27:26	RESERVED_BITS27_26	Clear (0) these bits.
25	TI1	General purpose timer interrupt 1 (GPTINT1) Read/write control This bit is set (1) when the counter in the GPTIMER1CTRL (non-EHCI) register transitions to zero. Setting (1) this bit will clear it.
24	TI0	General purpose timer interrupt 0 (GPTINT0) Read/write control This bit is set (1) when the counter in the GPTIMER0CTRL (non-EHCI) register transitions to zero. Setting (1) this bit will clear it.
23:20	RESERVED_BITS23_20	Clear (0) these bits.
19	UPI	USB host periodic interrupt (USBHSTPERINT) Read/write control This bit is set (1) by the host controller when the cause of an interrupt is a completion of a USB transaction, where the transfer descriptor (TD) has an interrupt on complete (IOC) bit set (1) and the TD was from the periodic schedule. This bit is also set (1) by the host controller when a short packet is detected AND the packet is on the periodic schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes. This bit is not used by the device controller and will always be clear (0).
18	UAI	USB host asynchronous interrupt (USBHSTASYNCINT) Read/write control This bit is set (1) by the host controller when the cause of an interrupt is a completion of a USB transaction, where the transfer descriptor (TD) has an interrupt on complete (IOC) bit set AND the TD was from the asynchronous schedule. This bit is also set (1) by the host when a short packet is detected AND the packet is on the asynchronous schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes. This bit is not used by the device controller and will always be clear (0).
17	RESERVED_BIT17	Clear (0) these bits.
16	NAKI	NAK interrupt bit Read only This bit is set (1) by the hardware when, for a particular endpoint, both the Tx/Rx endpoint NAK bit and the corresponding Tx/Rx endpoint NAK enable bit are set (1). This bit is automatically cleared (0) by the hardware when all of the enabled Tx/Rx endpoint NAK bits are cleared (0).

USB3_HS_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
15	AS	Asynchronous schedule status Read only Default = 0 This bit reports the current real status of the asynchronous schedule. When cleared (0), the asynchronous schedule status is disabled. And, if set (1), the status is enabled. The host controller is not required to immediately disable or enable the asynchronous schedule when software transitions the asynchronous schedule enable bit in the USBCMD register. When this bit and the asynchronous schedule enable bit are the same value, the asynchronous schedule is either enabled (1) or disabled (0). This bit is only used by the host controller.
14	PS	Periodic schedule status Read only Default = 0 This bit reports the current real status of the periodic schedule. When cleared (0), the periodic schedule is disabled. And, if set (1), the status is enabled. The host controller is not required to immediately disable or enable the periodic schedule when software transitions the periodic schedule enable bit in the USBCMD register. When this bit and the periodic schedule enable bit are the same value, the periodic schedule is either enabled (1) or disabled (0). This bit is only used by the host controller.
13	RCL	Reclamation Read only Default = 0 This is a read-only status bit that is used to detect an empty asynchronous schedule. This bit is only used by the host controller.
12	HCH	HC halted Read only Default = 1 This bit is a clear (0) whenever the run/stop bit is set (1). The host controller sets (1) this bit after it has stopped executing, because of the run/stop bit being cleared (0), either by the software or by the host controller hardware (for example, an internal error). This bit is only used by the host controller.
11	RESERVED_BIT11	Clear (0) this bit.
10	ULPII	ULPI interrupt Read/write control Default = 0 When the ULPI viewport is present in the design, an event completion will set (1) this interrupt. This bit is used by both the host and device controllers. It is only present in designs where the configuration constant VUSB_HS_PHY_ULPI = 1.

USB3_HS_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
9	RESERVED_BIT9	Clear (0) this bit.
8	SLI	DC suspend Read/write control Default = 0 When a device controller enters a suspend state from an active state, this bit will be set (1). The device controller clears (0) the bit upon exiting from a suspend state. This bit is only used by the device controller.
7	SRI	SOF received Read/write control Default = 0 When the device controller detects a start of (micro) frame, this bit will be set (1). When a SOF is extremely late, the device controller will automatically set (1) this bit to indicate that an SOF was expected. Therefore, this bit will be set (1) roughly every 1 ms in the device FS mode and every 125 ms in the HS mode, and will be synchronized to the actual SOF that is received. Since the device controller is initialized to FS before connect, this bit will be set (1) at an interval of 1 ms during the prelude to connect and chirp. In the host mode, this bit will be set (1) every 125 us and can be used by the host controller driver as a time base. The software writes a 1 to this bit to clear it. This is a non-EHCI status bit.
6	URI	USB reset received Read/write control Default = 0 When the device controller detects a USB reset and enters the default state, this bit will be set (1). The software can set (1) this bit to clear the USB reset received status bit. This bit is only used by the device controller.
5	AAI	Interrupt on async advance Read/write control Default = 0 The system software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by setting (1) the interrupt on async advance doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source. This bit is only used by the host controller.
4	SEI	System error Read/write control This interrupt is triggered when there is an AHB error (HRESP = ERROR) on the AHB Master interface.

USB3_HS_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
3	FRI	Frame list rollover Read/write control The host controller sets (1) this bit when the frame list index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the frame list size field of the USBCMD register) is 1024, the frame index register rolls over every time FRINDEX [1 3] toggles. Similarly, if the size is 512, the host controller sets (1) this bit to a one every time FHINDEX [12] toggles. This bit is only used by the host controller.
2	PCI	Port change detect Read/write control The host controller sets (1) this bit when a connect status occurs on any port, a port enable/disable change occurs on any port, or the force port resume bit is set (1) as the result of a J-K transition on the suspended port. The device controller sets (1) this bit when the port controller enters the full or high-speed operational state. When the port controller exits the full or high-speed operation states due to reset or suspend events, the notification mechanisms are the USB reset received bit and the DC suspend bits, respectively. This bit is not EHCI compatible.
1	UEI	USB error interrupt (USBERRINT) Read/write control When completion of a USB transaction results in an error condition, this bit is set (1) by the host/device controller. This bit is set (1) along with the USBINT bit, if the TD on which the error interrupt occurred also had its interrupt-on-complete (IOC) bit set (1). The device controller detects resume signaling only.
0	UI	USB interrupt (USBINT) Read/write control This bit is set (1) by the host/device controller when the cause of an interrupt is a completion of a USB transaction where the transfer descriptor (TD) has an interrupt-on-complete (IOC) bit set (1). This bit is also set (1) by the host/device controller when a short packet is detected. A short packet is when the actual number of bytes received was less than the expected number of bytes.

0x12520148

USB3_HS_USB_OTG_HS_USBINTR

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_USBINTR register is the USB interrupt enable register. The interrupts to the software are enabled with this register. An interrupt is generated when a bit is set (1) and the corresponding interrupt is active. The USB status register (USBSTS) still shows interrupt sources, even if they are disabled by the USBINTR register, which allows polling of interrupt events by the software.

USB3_HS_USB_OTG_HS_USBINTR

Bits	Name	Description
31	ULPI_INTR_EN	Default value =0.When this bit is a 1 and ULPI_INTR is a 1, the controller will issue an interrupt. The interrupt is acknowledged by software clearing the ULPI_INTR bit.
30	PHY_SESS_VLD_CHG_EN	Default value =0. When this bit is set then Link Controller will issue an interrupt when PHY_SESS_VLD changes its value.
29:26	RESERVED_BITS29_26	Clear (0) these bits.
25	TIE1	General purpose timer interrupt enable 1 When this bit is set (1), and the GPTINT1 bit in the USBSTS register is set (1), the controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the GPTINT1 bit.
24	TIE0	General purpose timer interrupt enable 0 When this bit is set (1), and the GPTINT0 bit in the USBSTS register is set (1), the controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the GPTINT0 bit.
23:20	RESERVED_BITS23_20	Clear (0) these bits.
19	UPIE	USB host periodic interrupt enable When this bit is set (1), and the USBHSTPERINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBHSTPERINT bit.
18	UAIE	USB host asynchronous interrupt enable When this bit is set (1), and the USBHSTASYNCINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBHSTASYNCINT bit.
17	RESERVED_BIT17	Clear (0) this bit.

USB3_HS_USB_OTG_HS_USBINTR (cont.)

Bits	Name	Description
16	NAKE	NAK interrupt enable This bit is set (1) by the software if it wants to enable the hardware interrupt for the NAK interrupt bit. If both this bit and the corresponding NAK interrupt bit are set (1), a hardware interrupt is generated.
15:11	RESERVED_BITS15_11	Clear (0) these bits.
10	ULPIE	ULPI enable When this bit is set (1), and the ULPI Interrupt bit in the USBSTS register transitions, the controller will issue and interrupt. The interrupt is acknowledged by the software setting (1) the ULPI interrupt bit. This bit is used by both the host and device controllers. It is only present in designs where configuration constant VUSB_HS_PHY_ULPI = 1.
9	RESERVED_BIT9	Clear (0) this bit.
8	SLE	Sleep enable When this bit is set (1) and the DC suspend bit in the USBSTS register transitions, the device controller will issue an interrupt. The interrupt is acknowledged by the software setting (1) the DC suspend bit. This bit is only used by the device controller.
7	SRE	SOF received enable When this bit is set (1) and the SOF received bit in the USBSTS register is set (1), the device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the SOF received bit.
6	URE	USB reset enable When this bit is set (1) and the USB reset received bit in the USBSTS register is set (1), the device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the USB reset received bit.
5	AAE	Interrupt on async advance enable When this bit is set (1) and the interrupt on async advance bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the interrupt on async advance bit. This bit is only used by the host controller.
4	SEE	System error enable When this bit is set (1) and the system error bit in the USBSTS register is set (1), the host/device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the system error bit.

USB3_HS_USB_OTG_HS_USBINTR (cont.)

Bits	Name	Description
3	FRE	Frame list rollover enable When this bit is set (1) and the frame list rollover bit in the USBSTS register is set (1), the host controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the frame list rollover bit. This bit is only used by the host controller.
2	PCE	Port change detect enable When this bit is set (1) and the port change detect bit in the USBSTS register is set (1), the host/device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the port change detect bit.
1	UEE	USB error interrupt enable When this bit is set (1) and the USBERRINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBERRINT bit in the USBSTS register.
0	UE	USB interrupt enable When this bit is set (1) and the USBINT bit in the USBSTS register is set (1), the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBINT bit.

0x1252014C USB3_HS_USB_OTG_HS_FRINDEX

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_FRINDEX register is the USB frame index register. This register is used by the host controller to index the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits [N:3] are used to select a particular entry in the periodic frame list during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by the system software in the frame list size field in the USBCMD register.

This register must be written as a DWord. Byte writes produce-undefined results. This register cannot be written unless the host controller is in the 'halted' state, as indicated by the HC halted bit. A write to this register while the run/stop bit is set (1) produces undefined results. Writes to this register also affect the SOF value.

In the device mode, this register is read-only and the device controller updates the FRINDEX [13:3] register from the frame number indicated by the SOF marker. Whenever a SOF is received by the USB bus, FRINDEX [13:3] will be checked against the SOF marker. If FRINDEX [13:3] is different from the SOF marker, FRINDEX [13:3] will be set to the SOF value and FRINDEX [2:0] will be cleared (0) (that is, SOF for a 1-ms frame). If FRINDEX [13:3] is equal to the SOF value, FRINDEX [2:0] will be incremented (that is, SOF for 125-ms micro-frame.

USB3_HS_USB_OTG_HS_FRINDEX

Bits	Name	Description
31:14	RESERVED_BITS31_14	Clear (0) these bits.
13:0	FRINDEX_13_0	Frame index The value in this register increments at the end of each time frame (for example, a micro-frame). Bits [N:3] are used for the frame list current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. The following data shows the values of N based on the value of the frame list size field in the USBCMD register when used in host mode. USBCMD [Frame list size] number Elements N 000b (1024) 12 001b (512) 11 010b (256) 10 011b (128) 9 100b (64) 8 101b (32) 7 110b (16) 6 111b (8) 5 In the device mode, the value is the current frame number of the last frame transmitted. It is not used as an index. In either mode, bits 2:0 indicate the current microframe.

0x12520154 USB3_HS_USB_OTG_HS_PERIODICLISTBASE

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_PERIODICLISTBASE register is the periodic list base address register. This 32-bit register contains the beginning address of the periodic frame list in the system memory. The HCD loads this register prior to starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the frame index register (FRINDEX) to enable the host controller to step through the periodic frame list in sequence.

NOTE This device is shared between the host controller and device controller operation. For host controller operation, this is the USB_OTG_HS_ PERIODICLISTBASE register. For device controller operation, this is the USB_OTG_HS_DEVICEADDR register.

USB3_HS_USB_OTG_HS_PERIODICLISTBASE

Bits	Name	Description
31:12	PERBASE_31_12	Base address (low) These bits correspond to memory address signals [31:12], respectively. Only used by the host controller.
11:0	RESERVED_BITS11_0	This field must be written as zeros. During runtime, the values of these bits are undefined.

0x12520154 USB3_HS_USB_OTG_HS_DEVICEADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_DEVICEADDR register is the USB device address register. The upper seven bits of this register represent the device address. After any controller reset or a USB reset, the device address is set to the default address (0). The default address will match all incoming addresses. The software shall reprogram the address after receiving a SET_ADDRESS descriptor.

The USBADRA is used to accelerate the SET_ADDRESS sequence by allowing the DCD to preset the USBADR register before the status phase of the SET_ADDRESS descriptor.

NOTE This device is shared between the host controller and device controller operations. For host controller operation, this is the USB_OTG_HS_ PERIODICLISTBASE register. For device controller operation, this is the USB_OTG_HS_DEVICEADDR register.

USB3_HS_USB_OTG_HS_DEVICEADDR

Bits	Name	Description
31:25	USBADR_31_25	Device address These bits correspond to the USB device address.

USB3_HS_USB_OTG_HS_DEVICEADDR (cont.)

Bits	Name	Description
24	USBADRA	Device address advance Default = 0 When this bit is clear (0), any writes to USBADR are instantaneous. When this bit is set (1) at the same time or before USBADR is written, the write to the USBADR field is staged and held in a hidden register. After an IN occurs on endpoint 0 and is ACKed, USBADR will be loaded from the holding register. The hardware will automatically clear (0) this bit on the following conditions: 1. IN is ACKed to endpoint 0 (USBADR is updated from staging register). 2. OUT/SETUP occur to endpoint 0 (USBADR is not updated). 3. Device reset occurs (USBADR is reset to 0). Note: After the status phase of the SET_ADDRESS descriptor, the DCD has 2 ms to program the USBADR field. This mechanism will ensure this specification is met when the DCD can not write of the device address within 2 ms from the SET_ADDRESS status phase. If the DCD writes the USBADR with USBADRA = 1 after the SET_ADDRESS data phase (before the prime of the status phase), the USBADR will be programmed instantly at the correct time and meet the 2-ms USB requirement.
23:0	RESERVED_BITS23_0	These bits must be written as zeros. During runtime, the values of these bits are undefined.

0x12520158 USB3_HS_USB_OTG_HS_ASYNCLISTADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ASYNCLISTADDR register is the next asynchronous list address register. This 32-bit register contains the address of the next asynchronous queue head to be executed by the host. Bits [4:0] of this register cannot be modified by the system software and will always return a zero when read.

NOTE The USB_OTG_HS_ASYNCLISTADDR register and the USB_OTG_HS_ENDPOINTLISTADDR register are shared between the host controller and device controller operations. For the host controller, this is the USB_OTG_HS_ASYNCLISTADDR register. For the device controller, this is the USB_OTG_HS_ENDPOINTLISTADDR register.

USB3_HS_USB_OTG_HS_ASYNCLISTADDR

Bits	Name	Description
31:5	ASYBASE_31_15	Link pointer low (LPL). These bits correspond to memory address signals [31:5], respectively. This field may only reference a queue head (OH). This field is only used by the host controller.
4:0	RESERVED_BITS4_0	The values of these bits has no effect on circuit operation.

0x12520158 USB3_HS_USB_OTG_HS_ENDPOINTLISTADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPOINTLISTADDR register is the endpointlist address register. In the device mode, this register contains the address of the top of the endpoint list in system memory. Bits [10:0] of this register cannot be modified by the system software and will always return a zero when read.

NOTE The USB_OTG_HS_ASYNCLISTADDR register and the USB_OTG_HS_ENDPOINTLISTADDR register are shared between the host controller and device controller operations. For the host controller, this is the USB_OTG_HS_ASYNCLISTADDR register. For the device controller, this is the USB_OTG_HS_ENDPOINTLISTADDR register.

USB3_HS_USB_OTG_HS_ENDPOINTLISTADDR

Bits	Name	Description
31:11	EPBASE_31_11	Endpoint list pointer (low) These bits correspond to memory address signals [31:11], respectively. This field will reference a list of up to 32 queue heads (QH). That is, one queue head per endpoint & direction.
10:0	RESERVED_BITS10_0	The values of these bits has no effect on circuit operation.

0x1252015C USB3_HS_USB_OTG_HS_TTCTRL

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_TTCTRL register is the TT status and control register. This register contains parameters needed for internal TT operations.

NOTE This register is not used in the device controller operation.

USB3_HS_USB_OTG_HS_TTCTRL

Bits	Name	Description
31	RESERVED_BIT31	Not used.
30:24	TTHA	Not used.
23:0	RESERVED_BITS23_0	Not used.

0x12520160 USB3_HS_USB_OTG_HS_BURSTSIZE

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1010

The USB_OTG_HS_BURSTSIZE register is the programmable burst size register. This register is used to control dynamically change the burst size used during data movement on the initiator (master) interface.

USB3_HS_USB_OTG_HS_BURSTSIZE

Bits	Name	Description
31:16	RESERVED_BITS31_16	The value of these bits has no effect on circuit operation.
15:8	TXPBURST	Programmable Tx burst length This register represents the maximum length of a the burst in 32-bit words while moving data from system memory to the USB bus.
7:0	RXPBURST	Programmable Rx burst length This register represents the maximum length of a the burst in 32-bit words while moving data from the USB bus to system memory.

0x12520164 USB3_HS_USB_OTG_HS_TXFILLTUNING

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_TXFILLTUNING register is the host transmit pre-buffer packet tuning register. The fields in this register control performance tuning associated with how the host controller posts data to the Tx latency FIFO before moving the data onto the USB bus. The specific areas of performance include the how much data to post into the FIFO and an estimate for how long that operation should take in the target system.

Definitions:

T0 = Standard packet overhead

T1 = Time to send data payload

Tff = Time to fetch packet into TX FIFO up to specified level.

Ts = Total packet flight time (send-only) packet

Ts = T0 + T1

Tp = Total packet time (fetch and send) packet

Tp = Tff + T0 + T1

Upon discovery of a transmit (OUT/SETUP) packet in the data structures, the host controller checks to ensure Tp remains before the end of the [micro] frame. If so it proceeds to pre-fill the TX FIFO. If at anytime during the pre-fill operation the time remaining the [micro] frame is < Ts, then the packet attempt ceases and the packet is tried at a later time. Although this is not an error condition and the host controller will eventually recover, a mark will be made the scheduler health counter to note the occurrence of a ’back-off’ event. When a back-off event is detected, the partial packet fetched may need to be discarded from the latency buffer to make room for periodic traffic that will begin after the next SOF. Too many back-off events can waste bandwidth and power on the system bus, and thus should be minimized (not necessarily eliminated). Back-offs can be minimized with use of the TSCHHEALTH (Tff), as described in the register table.

USB3_HS_USB_OTG_HS_TXFILLTUNING

Bits	Name	Description
31:22	RESERVED_BITS31_22	The value of these bits has no effect on circuit operation.
21:16	TXFIFOTHRES	FIFO burst threshold Default = 2 This register controls the number of data bursts that are posted to the TX latency FIFO in the host mode before the packet begins on to the bus. The minimum value is 2 and this value should be a low as possible to maximize USB performance. A higher value can be used in systems with unpredictable latency and/or insufficient bandwidth, where the FIFO may underrun because the data transferred from the latency FIFO to USB occurs before it can be replenished from system memory. This value is ignored if the stream disable bit in USBMODE register is set (1).
15:13	RESERVED_BITS15_13	The value of these bits has no effect on circuit operation.

USB3_HS_USB_OTG_HS_TXFILLTUNING (cont.)

Bits	Name	Description
12:8	TXSCHHEALTH	Scheduler health counter Read/write to clear Default = 0 This register increments when the host controller fails to fill the Tx latency FIFO to the level programmed by TXFIFOTHRES before running out of time to send the packet before the next start-of-frame. This health counter measures the number of times this occurs to provide feedback to selecting a proper TXSCHOH. Writing to this register will clear the counter and this counter will be at a maximum at 31.
7:0	TXSCHOH	Scheduler overhead Default = 0 This register adds an additional fixed offset to the schedule time estimator described above as Tff. As an approximation, the value chosen for this register should limit the number of back-off events captured in the TXSCHHEALTH to less than 10 per second in a highly-utilized bus. Choosing a value that is too high for this register is not desired, as it can needlessly reduce USB utilization. The time unit represented in this register is 1.267 ms when a device is connected in the high-speed mode for OTG and SPH. The time unit represented in this register is 6.333 ms when a device is connected in the low/full speed mode for OTG and SPH. The time unit represented in this register is always 1.267 times the MPH product.

0x12520170 USB3_HS_USB_OTG_HS_ULPI_VIEWPORT

Type: Read/write (unless otherwise indicated)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x08000000

The USB_OTG_HS_ULPI_VIEWPORT register provides indirect access to the ULPI PHY register set. Although the core performs access to the ULPI PHY register set, there may be extraordinary circumstances where software may need direct access.

CAUTION Writes to the ULPI through the viewport can substantially harm standard USB operations. Currently, no usage model has been defined where the software should need to execute writes directly to the ULPI - see the exception regarding optional features below.

Executing read operations though the ULPI viewport should have no harmful side effects to standard USB operations.

NOTE The ULPI viewport is only synthesized in the design if the constant VUSB_HS_PHY_ULPI is set (1). If the ULPI interface is not enabled, this register will always read zeros.

Two operations can be performed with the ULPI viewport: wake-up and read/write operations. The wake-up operation is used to put the ULPI interface into normal operation mode and re-enable the clock, if necessary. A wake-up operation is required before accessing the registers when the ULPI interface is operating in the low power mode, serial mode, or car kit mode.

The ULPI state can be determined by reading the sync state bit (ULPISS). If this bit is set (1), then the ULPI interface is running in the normal operation mode and can accept read/write operations. If the ULPISS is clear (0), then read/write operations will not be able to execute. Undefined behavior will result if ULPISS = 0, and a read or write operation is performed.

To execute a wake-up operation, write all 32-bits of the ULPI Viewport where ULPIPORT is constructed appropriately, and the ULPIWU bit is set (1) and the ULPIRUN bit is clear (0). Poll the ULPI viewport until ULPIWU is zero for the operation to complete.

To execute a read or write operation, write all 32-bits of the ULPI viewport where ULPIDATWR, ULPIADDR, ULPIPORT, and ULPIRW are constructed appropriately, and the ULPIRUN bit is set (1). Poll the ULPI viewport until ULPIRUN is zero for the operation to complete. Once ULPIRUN is zero, the ULPIDATRD will be valid if the operation was a read.

The polling method above could also be replaced and an interrupt driven using the ULPI interrupt defined in the USBTS and USBINTR registers. When a wake-up or read/write operation completes, the ULPI interrupt will be set (1).

Several optional features may need to be enabled or disabled by the system software as part of system configuration. These bits are contained in the interface and OTG control registers of the ULPI PHY register set. These registers also contain bits that are controlled by the link dynamically and, therefore, should only be modified by the system software using the set/clear access method. Direct writes to these registers could have harmful side effects to the standard USB operations. The following bits are optional bits:

- Bits 3 through 7 in the interface control register
- Bits 6 and 7 in the OTG control register.

Refer to the ULPI Specification Revision 1.1 for further information on the use of the optional features.

USB3_HS_USB_OTG_HS_ULPI_VIEWPORT

Bits	Name	Description
31	ULPIWU	ULPI wake-up Setting (1) this bit begins the wake-up operation. The bit will automatically transition to 0 after the wake-up is complete. Once this bit is set (1), the driver can not clear it back to 0. Note: The driver must never execute a wake-up and a read/write operation at the same time.
30	ULPIRUN	ULPI read/write run Setting (1) this bit will begin the read/write operation. The bit will automatically transition to 0 after the read/write is complete. Once this bit is set (1), the driver can not clear it back to 0. Note: The driver must never execute a wakeup and a read/write operation at the same time.

USB3_HS_USB_OTG_HS_ULPI_VIEWPORT (cont.)

Bits	Name	Description
29	ULPIRW	ULPI read/write control This bit selects between running a read or write operation. value 0 = Read value 1 = Write
28	ULPIFORCE	ULPI read/write force This bit enables forcing register access during RX packet value 0 = register access is not forced during RX packet (default) value 1 = register access is forced during RX packet reception
27	ULPISS	ULPI sync state Read Only value 1 = Normal sync state value 0 = In another state (for example, car kit, serial, low power) This bit represents the state of the ULPI interface. Before reading this bit, the ULPIPORT field should be set accordingly if used with the multi-port host. Otherwise, this field should always remain 0.
26:24	ULPIPORT	ULPI port number For the wakeup or read/write operation to be executed, this value selects the port number the ULPI PHY is attached to in the multi-port host. The valid range is 0 to 7. This field should always be written as a 0 for the non-multi port products.
23:16	ULPIADDR	ULPI data address When a read or write operation is commanded, the address of the operation is written to this field.
15:8	ULPIDATRD	ULPI data read Read only After a read operation completes, the result is placed in this field.
7:0	ULPIDATWR	ULPI data write When a write operation is commanded, the data to be sent is written to this field.

0x12520178 USB3_HS_USB_OTG_HS_ENDPTNAK

Type: Read/write clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTNAK register is the endpoint NAK register.

USB3_HS_USB_OTG_HS_ENDPTNAK

Bits	Name	Description
31:16	EPTN_15_0	Tx endpoint NAK Each tx endpoint has 1 bit in this field. The bit is set (1) when the device sends a NAK handshake on a received IN token for the corresponding endpoint. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0
15:0	EPRN_15_0	Rx endpoint NAK Each rx endpoint has 1 bit in this field. The bit is set (1) when the device sends a NAK handshake on a received OUT or PING token for the corresponding endpoint. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x1252017C USB3_HS_USB_OTG_HS_ENDPTNAKEN

Type: Read/write clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTNAKEN register is the endpoint NAK enable register.

USB3_HS_USB_OTG_HS_ENDPTNAKEN

Bits	Name	Description
31:16	EPTNE_15_0	Tx endpoint NAK enable Each bit is an enable bit for the corresponding Tx endpoint NAK bit. If this bit is set (1) and the corresponding Tx endpoint NAK bit is set (1), the NAK Interrupt bit is set (1). Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0
15:0	EPRNE_15_0	Rx endpoint NAK enable Each bit is an enable bit for the corresponding Rx endpoint NAK bit. If this bit is set (1) and the corresponding Rx endpoint NAK bit is set (1), the NAK Interrupt bit is set (1). Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x12520184 USB3_HS_USB_OTG_HS_PORTSC

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xCC000004

This is the USB_OTG_HS_PORTSC register.

USB3_HS_USB_OTG_HS_PORTSC

Bits	Name	Description
31:30	PTS	Parallel transceiver select Read/write This register bit pair is used in conjunction with the configuration constant VUSB_HS_PHY_TYPE to control which parallel transceiver interface is selected. If VUSB_HS_PHY_ TYPE is set for 0, 1, 2, or 3, then this bit is read only. If VUSB_HS_PHY_TYPE is 4, 5, 6, or 7, then this bit is read/write. This field is reset to the following values: 00 if VUSB_HS_PHY_TYPE = 0,4 - UTMI/UTMI+ 01 if VUSB_HS_PHY_TYPE = 1,5 - Reserved 10 if VUSB_HS_PHY_TYPE = 2,6 - ULPI 11 if VUSB_HS_PHY_TYPE = 3,7 - Serial/1.1 PHY (FS only) This bit is not defined in the EHCI specification.
29	STS	Serial transceiver select Read/write This register bit is used in conjunction with the configuration constant VUSB_HS_PHY_SERIAL to control whether the parallel or serial transceiver interface is selected for FS and LS operation. The serial interface engine can be used in combination with the UTMI+ or ULPI physical interface to provide FS/LS signaling instead of the parallel interface. ’ If VUSB_HS_PHY_SERIAL is 0 or 1, then this bit is read only. ’ If VUSB_HS_PHY_SERIAL is 2 or 3, then this bit is read/write. This bit has no effect unless the parallel transceiver select is set to UTMI+ or ULPI. The Serial/1.1 physical interface will use the serial interface engine for FS/LS signaling regardless of this bit value. Note: This bit was reserved for future operation, and is now adding for dynamic use of the serial engine in accord with UMTI+ and ULPI characterization logic. This bit is not defined in the EHCI specification.

USB3_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
28	PTW	Parallel transceiver width Read/write This register bit is used in conjunction with the configuration constant VUSB_HS_PHY16_8 to control the data bus width of the UTMI transceiver interface. ' If VUSB_HS_PHY16_8 is 0 or 1, then this bit is read only. ' If VUSB_HS_PHY16_8 is 2 or 3, then this bit is read/write. This bit is reset to 1 if VUSB_HS_PHY16_8 selects a default UTMI interface width of 16-bits, else it is reset to 0. ' Writing this bit to 0 selects the 8-bit [60MHz] UTMI interface. ' Writing this bit to 1 selects the 16-bit [30MHz] UTMI interface. This bit has no effect if the serial interface is selected. This bit is not defined in the EHCI specification.
27:26	PSPD	Port speed Read only This register field indicates the speed at which the port is operating. For HS mode operation in the host controller and HS/FS operation in the device controller, the port routing steers data to the protocol engine. For FS and LS mode operation in the host controller, the port routing steers data to the protocol engine with the embedded transaction translator. value 00 = Full speed value 01 = Low speed value 10 = High speed This bit is not defined in the EHCI specification.
25	SPRT	Short Port Reset Time. shortens port reset time for simulation.
24	PFSC	Port force full speed connect Read/write Default = 0 Setting (1) this bit will force the port to only connect at full speed. It also disables the chirp sequence that allows the port to identify itself as high speed. This is useful for testing FS configurations with a HS host, hub or device. This bit is not defined in the EHCI specification. This bit is for debugging purposes.

USB3_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
23	PHCD	PHY low power suspend - clock disable (PLPSCD) Read/write Default = 0 value 1 = Disable the PHY clock. value 0 = Enable the PHY clock. Reading this bit will indicate the status of the PHY clock. Note: The PHY clock cannot be disabled if it is being used as the system clock. In the device mode, The PHY can be put into low power suspend - clock disable when the device is not running (USBCMD run/stop = 0) or the host has signaled suspend (PORTSC SUSPEND = 1). Low power suspend will be cleared automatically when the host has signaled resume. Before forcing a resume from the device, the device controller driver must clear this bit. In the host mode, the PHY can be put into low power suspend - clock disable when the downstream device has been put into the suspend mode or when no downstream device is connected. Low power suspend is completely under the control of the software. This bit is not defined in the EHCI specification.
22	WKOC	Wake on over-current enable (WKOC_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to over-current conditions as wake-up events. This bit is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0). This bit is output from the controller as signal pwrctl_wake_ ovrcurr_en (OTG/host core only) for use by an external power control circuit.
21	WKDS	Wake on disconnect enable (WKDSCNNT_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to device disconnects as wake-up events. This field is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0) or in the device mode. This bit is output from the controller as signal pwrctl_wake_ dscnnt_en (OTG/host core only) for use by an external power control circuit.

USB3_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
20	WKCN	Wake on connect enable (WKCNNT_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to device connects as wake-up events. This field is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0) or in the device mode. This bit is output from the controller as signal pwrctl_wake_ dscnnt_en (OTG/host core only) for use by an external power control circuit.

USB3_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
19:16	PTC_3_0	Port test control Read/write Default = 0000 Any other value than zero indicates that the port is operating in the test mode. Value Specific test The FORCE_ENABLE_FS and FORCE ENABLE_LS tests are extensions to the test mode support, as specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. Note: Low speed operations are not supported as a peripheral device. 0x0: TEST_MODE_DISABLE 0x1: J_ STATE 0x8: K_STATE 0x9: SE0 (host / NAK device) 0x40: Packet 0x41: FORCE_ENABLE_HS 0x48: FORCE_ENABLE_FS 0x49: FORCE_ENABLE_LS 0x3E8: Reserved_1 0x3E9: Reserved_2 0x3EA: Reserved_3 0x3EB: Reserved_4 0x3EC: Reserved_5 0x3ED: Reserved_6 0x3EE: Reserved_7 0x3EF: Reserved_8 0x3F0: Reserved_9 0x3F1: Reserved_10 0x3F2: Reserved_11 0x3F3: Reserved_12 0x3F4: Reserved_13 0x3F5: Reserved_14 0x3F6: Reserved_15 0x3F7: Reserved_16 0x3F8: Reserved_17 0x3F9: Reserved_18 0x3FA: Reserved_19 0x3FB: Reserved_20 0x3FC: Reserved_21 0x3FD: Reserved_22 0x3FE: Reserved_23 0x3FF: Reserved_24 0x400: Reserved_25 0x401: Reserved_26 0x402: Reserved_27 0x403: Reserved_28 0x404: Reserved_29 0x405: Reserved_30 0x406: Reserved_31 0x407: Reserved_32 0x408: Reserved_33 0x409: Reserved_34 0x40A: Reserved_35

USB3_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
19:16	PTC_3_0 (CONTINUED)	0x40B: Reserved_36 0x40C: Reserved_37 0x40D: Reserved_38 0x40E: Reserved_39 0x40F: Reserved_40 0x410: Reserved_41 0x411: Reserved_42 0x412: Reserved_43 0x413: Reserved_44 0x414: Reserved_45 0x415: Reserved_46 0x416: Reserved_47 0x417: Reserved_48 0x418: Reserved_49 0x419: Reserved_50 0x41A: Reserved_51 0x41B: Reserved_52 0x41C: Reserved_53 0x41D: Reserved_54 0x41E: Reserved_55 0x41F: Reserved_56 0x420: Reserved_57 0x421: Reserved_58 0x422: Reserved_59 0x423: Reserved_60 0x424: Reserved_61 0x425: Reserved_62 0x426: Reserved_63 0x427: Reserved_64 0x428: Reserved_65 0x429: Reserved_66 0x42A: Reserved_67 0x42B: Reserved_68 0x42C: Reserved_69 0x42D: Reserved_70 0x42E: Reserved_71 0x42F: Reserved_72 0x430: Reserved_73 0x431: Reserved_74 0x432: Reserved_75 0x433: Reserved_76 0x434: Reserved_77 0x435: Reserved_78 0x436: Reserved_79 0x437: Reserved_80 0x438: Reserved_81 0x439: Reserved_82 0x43A: Reserved_83 0x43B: Reserved_84 0x43C: Reserved_85 0x43D: Reserved_86 0x43E: Reserved_87 0x43F: Reserved_88 0x440: Reserved_89 0x441: Reserved_90 0x442: Reserved_91 0x443: Reserved_92 0x444: Reserved_93 0x445: Reserved_94 0x446: Reserved_95 0x447: Reserved_96 0x448: Reserved_97 0x449: Reserved_98 0x44A: Reserved_99 0x44B: Reserved_100

USB3_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
19:16	PTC_3_0 (CONTINUED)	0x44C: Reserved_101 0x44D: Reserved_102 0x44E: Reserved_103 0x44F: Reserved_104 0x450: Reserved_105 0x451: Reserved_106 0x452: Reserved_107 0x453: Reserved_108 0x454: Reserved_109 0x455: Reserved_110 0x456: Reserved_111 0x457: Reserved_112
15:14	PIC_1_0	Port indicator control Read/write Default = 0 Writing to this field has no effect if the P_INDICATOR bit in the HCSPARAMS register is a zero. If the P_INDICATOR bit is set (1), then this field has the following meanings: Bit value Meaning value 00 Port indicators are off value 01 Amber value 10 Green value 11 Undefined Refer to the USB Specification Revision 2.0 [3] for a description on how these bits are to be used. This field is output from the controller as signals port_ind_ctl_1 and port_ind_ctl_0 for use by an external LED driving circuit.
13	PO	Port owner Read only Port owner hand-off is not implemented in this design, therefore this bit will always read back as clear (0). Default = 0 The EHCI definition is include here for reference: ’ This bit unconditionally goes clear (0) when the configured bit in the CONFIGFLAG register makes a 0-to-1 transition. ’ This bit unconditionally goes set (1) whenever the configured bit is clear (0). The system software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). The software sets (1) this bit when the attached device is not a high-speed device. When this bit is set (1), it indicates that an internal companion controller owns and controls the port.

USB3_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
12	PP	Port power (PP) Read/write or read-only The function of this bit depends on the value of the port power switching (PPC) field in the HCSPARAMS register. ’ PPC = 0: PP is read-only. A device controller with no OTG capability does not have port power control switches. ’ PPC = 1: PP is read/write. The host/OTG controller requires port power control switches. This bit represents the current setting of the switch (0 = off, 1 = on). When power is not available on a port (and PP equals a 0), the port is non-functional and will not report attaches, detaches, and so on. When an over-current condition is detected on a powered port and PPC is set (1), the PP bit in each affected port may be transitioned by the host controller driver from a one to a zero, removing power from the port. This feature is implemented in the host/OTG controller (PPC = 1). In a device-only implementation, port power control is not necessary. So, PPC and PP = 0.
11:10	LS_1_0	Line status Read-only These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines: Value Meaning value 00 SE0 value 10 J-state value 01 K-state value 11 Undefined In the host mode, the use of line state by the host controller driver is not necessary (unlike EHCI), because the port controller state machine and the port routing manage the connection of LS and FS. In the device mode, the use of line state by the device controller driver is not necessary.
9	HSP	High-speed port Read-only Default = 0 When the bit is set (1), the host/device connected to the port is in the high-speed mode. When this bit is clear (0), the host/device connected to the port is not in a high-speed mode. Note: HSP is redundant with PSPD(27:26), but will remain in the design for compatibility. This bit is not defined in the EHCI specification.

USB3_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
8	PR	Port reset This bit is clear (0) if the port power (PP) bit (bit 12) of this register is clear (0). Host mode: ’ Read/write ’ Default = 0 When the software sets (1) this bit, the bus-reset sequence as defined in the USB Specification Revision 2.0 is started. This bit will automatically clear (go to 0) after the reset sequence is complete. Note: This behavior is different from EHCI, where the host controller driver is required to clear (0) this bit after the reset duration is timed in the driver. Device mode: This bit is a read-only status bit. Device reset from the USB bus is also indicated in the USBSTS register. 0x1: Port is in reset 0x0: Port is not in reset

USB3_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
7	SUSP	Suspend Host mode: ' Read/write ' Default = 0 The port enabled bit and suspend bit of this register define the port states: Bit value Port state value 0x Disable value 10 Enable value 11 Suspend When in the suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction if a transaction was in progress when this bit set (1). In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. The host controller will unconditionally clear (0) this bit when the software clears (0) the force port resume bit. The host controller ignores a write of zero to this bit. If the host software sets (1) this bit when the port is not enabled (port enabled bit is a zero), the results are undefined. This field is clear (0) if port power (PP) is clear (0) in the host mode. Device mode: ' Read only ' Default = 0 In the device mode, this bit is a read-only status bit. 0x1: Port in suspend state_1 0x0: Port not in suspend st_1 0x1: Port in suspend state_2 0x0: Port not in suspend st_2

USB3_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
6	FPR	Force port resume ’ Read/write ’ Default = 0 Host mode: The software sets (1) this bit to drive resume signaling. The host controller sets (1) this bit if a J-to-K transition is detected while the port is in the suspend state. When this bit transitions to a one because a J-to-K transition is detected, the port change detect bit in the USBSTS register is also set (1). This bit will automatically clear (go to 0) after the resume sequence is complete. This behavior is different from EHCI, where the host controller driver is required to clear (0) this bit after the resume duration is timed in the driver. Note that, when the host controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (full-speed 'K') is driven on the port as long as this bit remains set (1). This bit will remain set (1) until the port has switched to the high-speed idle. Clearing (0) this bit has no affect, because the port controller will time the resume operation and clear (0) the bit when the port control state switches to HS or FS idle. This bit is clear if the port power (PP) is clear (0) in the host mode. This bit is not-EHCI compatible. Device mode: After the device has been in the suspend state for 5 ms or more, the software must set (1) this bit to drive resume signaling before clearing. The device controller will set (1) this bit if a J-to-K transition is detected while the port is in the suspend state. The bit will be cleared (0) when the device returns to normal operation. Also, when this bit transitions to a one because a J-to-K transition was detected, the port change detect bit in the USBSTS register is also set (1). 0x1: Resume detected/driven on port 0x0: No resume (K-state detected/driven on port)
5	OCC	Over-current change Read/write control Default = 0 This bit gets is set (1) when there is a change to over-current active. The software clears this bit by setting (1) this bit position. For host/OTG implementations, the user can provide over-current detection to the vbus_pwr_fault input for this condition. For device-only implementations, this bit shall always be clear (0).

USB3_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
4	OCA	Over-current active Read-only Default = 0 value 1 = This port currently has an over-current condition. value 0 = This port does not have an over-current condition. This bit will automatically transition from set (1) to clear (0) when the over current condition is removed. For host/OTG implementations, the user can provide over-current detection to the vbus_pwr_fault input for this condition. For device-only implementations, this bit shall always be clear (0).
3	PEC	Port enable/disable change Read/write control value 1 = Port enabled/disabled status has changed value 0 = No change Default = 0 Host mode: For the root hub, this bit gets set (1) only when a port is disabled due to disconnect on the port or due to the appropriate conditions existing at the EOF2 point. The software clears this bit by writing a one to it. This field is clear (0) if the port power (PP) bit in the register is clear (0). Device mode: The device port is always enabled (this bit will be zero).
2	PE	Port enabled/disabled Read/write value 1 = Enable value 0 = Disable Default 0 Host mode: Ports can only be enabled by the host controller as a part of the reset and enable. The software cannot enable a port by setting (1) this field. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by the host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port, due to other host controller and bus events. When the port is disabled, (0) downstream propagation of data is blocked except for reset. This field is clear (0) if the port power (PP) bit is cleared (0) in the host mode. Device mode: The device port is always enabled (this bit will be set [1])

USB3_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
1	CSC	Connect status change Read/write control value 1 = Change in current connect status value 0 = No change Default = 0 Host mode: Indicates that a change has occurred in the port's current connect status. The host/device controller sets (1) this bit for all changes to the port device connect status, even if the system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, the hub hardware will be 'setting' an already-set bit (that is, the bit will remain set). The software clears this bit by writing a one to it. This field is zero if the port power (PP) bit in this register is zero in the host mode. Device mode: This bit is undefined in the device controller mode.
0	CCS	Current connect status Read-only Host mode: value 1 = Device is present on port value 0 = No device is present Default = 0 This value reflects the current state of the port, and may not correspond directly to the event that caused the connect status change bit (bit 1) to be set (1). This field is clear if the port power (PP) bit in this register is clear (0) in host mode. Device mode: value 1 = Attached value 0 = Not attached Default = 0 If this bit is set (1), this indicates that the device successfully attached, and is operating in either high speed or full speed, as indicated by the high speed port bit in this register. If this bit is clear (0), this indicates that the device did not attach successfully or was forcibly disconnected by the software clearing (0) the run bit in the USBCMD register. It does not state the device being disconnected or suspended.

0x125201A4 USB3_HS_USB_OTG_HS_OTGSC

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000E20

USB3_HS_USB_OTG_HS_OTGSC

Bits	Name	Description
31	RESERVED_BIT31	Clear (0) this bit.
30	DPIE	Data pulse interrupt enable
29	B_1MSE	1 millisecond timer interrupt enable - read/write
28	BSEIE	B session end interrupt enable Read/write Setting (1) this bit enables the B session end interrupt.
27	BSVIE	B session valid interrupt enable Read/write Setting (1) this bit enables the B session valid interrupt.
26	ASVIE	A session valid interrupt enable Read/write Setting (1) this bit enables the A session valid interrupt.
25	AVVIE	A Vbus valid interrupt enable Read/write Setting (1) this bit enables the A Vbus valid interrupt.
24	IDIE	USB ID interrupt enable Read/write Setting (1) this bit enables the USB ID interrupt.
23	RESERVED_BIT23	Clear (0) this bit.
22	DPIS	Data pulse interrupt status Read/write to clear This bit is set (1) when data bus pulsing occurs on DP or DM. Data bus pulsing is only detected when USBMODE.CM = Host (11) and PORTSC(0). PortPower = Off (0). The software must write a one to clear this bit.
21	B_1MSS	1 millisecond timer interrupt status Read/write to clear This bit is set (1) once every millisecond. The software must write a one to clear this bit.
20	BSEIS	B session end interrupt status Read/write to clear This bit is set (1) when the Vbus has fallen below the B session end threshold. The software must write a one to clear this bit
19	BSVIS	B session valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the B session valid threshold (0.8 VDC). The software must write a one to clear this bit.

USB3_HS_USB_OTG_HS_OTGSC (cont.)

Bits	Name	Description
18	ASVIS	A session valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the A session valid threshold (0.8 VDC). The software must write a one to clear this bit.
17	AVVIS	A Vbus valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the Vbus valid threshold (4.4 VDC) on an A device. The software must write a one to clear this bit.
16	IDIS	USB ID interrupt status Read/write This bit is set (1) when a change on the ID input has been detected. The software must write a one to clear this bit.
15	RESERVED_BIT15	Clear (0) this bit.
14	DPS	Data bus pulsing status Read-only If this bit is set (1), it indicates that the data bus pulsing is being detected on the port.
13	B_1MST	1 millisecond timer toggle Read-only This bit toggles once per millisecond.
12	BSE	B session end Read-only Indicates that the Vbus is below the B session end threshold.
11	BSV	B session valid Read-only Indicates that the Vbus is above the B session valid threshold.
10	ASV	A session valid Read-only Indicates that the Vbus is above the A session valid threshold.
9	AVV	A Vbus valid Read-only Indicates that the Vbus is above the A Vbus valid threshold.
8	ID	USB ID Read-only value 0 = A device value 1 = B device

USB3_HS_USB_OTG_HS_OTGSC (cont.)

Bits	Name	Description
7	HABA	Hardware assist B-disconnect to A-connect Read/write value 0 = Disabled value 1 = Enable automatic B-disconnect to A-connect sequence.
6	HADP	Hardware assist data-pulse Write to set
5	IDPU	ID pull-up Read/write This bit provides control over the ID pull-up register. value 0 = Off value 1 = On (default) When this bit is clear (0), the ID input will not be sampled.
4	DP	Data pulsing Read/write Setting (1) this bit causes the pull-up on DP to be asserted for data pulsing during SRP.
3	OT	OTG termination Read/write This bit must be set (1) when the OTG device is in the device mode. This controls the pull-down on DM.
2	HAAR	Hardware assist auto-reset Read/write value 0 = Disabled value 1 = Enable automatic reset after connect on host port.
1	VC	Vbus charge Read/write Setting (1) this bit causes the Vbus line to be charged. This is used for Vbus pulsing during SRP.
0	VD	Vbus discharge Read/write Setting (1) this bit causes the Vbus to discharge through a resistor.

0x125201A8 USB3_HS_USB_OTG_HS_USBMODE

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_USBMODE register is the USB device mode register.

USB3_HS_USB_OTG_HS_USBMODE

Bits	Name	Description
31:6	RESERVED_BITS31_6	Clear (0) these bits.
5	VBPS	Vbus power select value 0 - Output is 0 value 1 - Output is 1 This bit is connected to the vbus_pwr_select output and can be used for any generic control, but is named to be used by logic that selects between an on-chip Vbus power source (charge pump) and an off-chip source in systems when both are available.
4	SDIS	Stream disable mode value 0 = Inactive (default) value 1 = Active Device mode: Setting (1) this bit disables double priming on both the Rx and Tx for low bandwidth systems. This mode ensures that, when the Rx and Tx buffers are sufficient to contain an entire packet, the standard double buffering scheme is disabled to prevent overruns/underruns in bandwidth-limited systems. Note: In the high speed mode, a NYET handshake will respond to all packets received when the stream disable is active. Host mode: Setting (1) this bit ensures that overruns/underruns of the latency FIFO are eliminated for low bandwidth systems where the Rx and Tx buffers are sufficient to contain the entire packet. Enabling the stream disable also has the effect of ensuring that the Tx latency is filled to capacity before the packet is launched onto the USB. Note: Time duration to pre-fill the FIFO becomes significant when the stream disable is active. See TXFILLTUNING and TXTTFILLTUNING [MPH only] to characterize the adjustments needed for the scheduler when using this feature. Note: The use of this feature substantially limits of the overall USB performance.
3	SLOM	Setup lockout mode. In the device mode, this bit controls the behavior of the setup lock mechanism.. value 0 = Setup lockouts on (default) value 1 = Setup lockouts off (DCD requires use of a setup data buffer tripwire in USBCMD)

USB3_HS_USB_OTG_HS_USBMODE (cont.)

Bits	Name	Description
2	ES	Endian select Read/write This bit can change the byte ordering of the transfer buffers to match the host microprocessor bus architecture. The bit fields in the microprocessor interface and the DMA data structures (including the setup buffer within the device QH) are unaffected by the value of this bit, because they are based upon 32-bit words. value 0 = Little endian (default) - first byte referenced in the least significant byte of a 32-bit word. value 1 = Big endian - first byte referenced in most significant byte of a 32-bit word.
1:0	CM	Controller mode Read/write once The controller mode is defaulted to the proper mode for host-only and device-only implementations. For those designs that contain both host and device capability, the controller will default to an idle state and will need to be initialized to the desired operating mode after reset. For combination host/device controllers, this register can only be written once after reset. If it is necessary to switch modes, the software must reset the controller by writing to the RESET bit in the USBCMD register before reprogramming this register. value 00 = Idle [default for combination host/device] value 01 = Reserved value 10 = Device controller [default for device only controller] value 11 = Host controller [default for host only controller]

0x125201AC USB3_HS_USB_OTG_HS_ENPDTSETUPSTAT

Type: Read/write control
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENPDTSETUPSTAT register is the endpoint set-up status register.

USB3_HS_USB_OTG_HS_ENPDTSETUPSTAT

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.

USB3_HS_USB_OTG_HS_ENPDTSETUPSTAT (cont.)

Bits	Name	Description
15:0	ENDPTSETUPSTAT_15_0	Set-up endpoint status For every set-up transaction that is received, a corresponding bit in this register is set (1). The software must clear or acknowledge the setup transfer by setting (1) a respective bit after it has read the setup data from the queue head. The response to a set-up packet as in the order of operations and total response time is crucial to limit bus time outs while the set-up lock-out mechanism is engaged. See Managing Endpoints in the Device Operational Model. This register is only used in the device mode.

0x125201B0 USB3_HS_USB_OTG_HS_ENDPTPRIME

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTPRIME register is the endpoint initialization register. This register is only used in the device mode.

USB3_HS_USB_OTG_HS_ENDPTPRIME

Bits	Name	Description
31:16	PETB_15_0	Prime endpoint transmit buffer For each endpoint, a corresponding bit is used to request that a buffer is prepared for a transmit operation in order to respond to a USB IN/INTERRUPT transaction. The software should set (1) the corresponding bit when posting a new transfer descriptor to an endpoint. The hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a transmit buffer. The hardware will clear (0) this bit when the associated endpoint(s) is (are) successfully primed. Note: These bits will be momentarily set (1) by the hardware during hardware re-priming operations when a dTD is retired, and the dQH is updated. PETB[15] - Endpoint 15 PETB[1] - Endpoint 1 PETB[0] - Endpoint 0

USB3_HS_USB_OTG_HS_ENDPTPRIME (cont.)

Bits	Name	Description
15:0	PERB_15_0	Prime endpoint receive buffer For each endpoint, a corresponding bit is used to request that a buffer is prepared for a receive operation for when a USB host initiates a USB OUT transaction. The software should set (1) the corresponding bit whenever posting a new transfer descriptor to an endpoint. The hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a receive buffer. The hardware will clear (0) this bit when the associated endpoint(s) is (are) successfully primed. Note: These bits will be momentarily set (1) by the hardware during hardware re-priming operations when a dTD is retired, and the dQH is updated. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x125201B4 USB3_HS_USB_OTG_HS_ENDPTFLUSH

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTFLUSH register is the endpoint de-initialize register. This register is only used in the device mode.

USB3_HS_USB_OTG_HS_ENDPTFLUSH

Bits	Name	Description
31:16	FETB_15_0	Flush endpoint transmit buffer Setting (1) a bit in this register will cause the associated endpoint to clear any primed buffers. If a packet is in progress for one of the associated endpoints, that transfer will continue until completion. The hardware will clear this register after the endpoint flush operation is successful. FETB[15] - Endpoint 15 FETB[1] - Endpoint 1 FETB[0] - Endpoint 0
15:0	FERB_15_0	Flush endpoint receive buffer Setting a bit (1) will cause the associated endpoint to clear any primed buffers. If a packet is in progress for one of the associated endpoints, that transfer will continue until completion. The hardware will clear this register after the endpoint flush operation is successful. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x125201B8 USB3_HS_USB_OTG_HS_ENDPTSTAT

Type: Read-only
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTSTAT register is the endpoint status register. This register is only used in the device mode.

USB3_HS_USB_OTG_HS_ENDPTSTAT

Bits	Name	Description
31:16	ETBR_15_0	Endpoint transmit buffer ready One bit for each endpoint indicates the status of the respective endpoint buffer. This bit is set (1) by the hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There will always be a delay between setting (1) a bit in the ENDPTPRIME register and the endpoint indicating that it is ready. This delay time varies based upon the current USB traffic and the number of bits set (1) in the ENDPTPRIME register. The buffer ready status is cleared by a USB reset, by the USB DMA system, or through the ENDPTFLUSH register. Note: These bits will be momentarily cleared by the hardware during hardware endpoint re-priming operations when a dTD is retired, and the dQH is updated. ETBR[15] - Endpoint 15 ETBR[1] - Endpoint 1 ETBR[0] - Endpoint 0
15:0	ERBR_15_0	Endpoint receive buffer ready One bit for each endpoint indicates the status of the respective endpoint buffer. This bit is set (1) by the hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There will always be a delay between setting (1) a bit in the ENDPTPRIME register and the endpoint indicating that it is ready. This delay time varies based upon the current USB traffic and the number of bits set (1) in the ENDPTPRIME register. The buffer ready status is cleared by a USB reset, by the USB DMA system, or through the ENDPTFLUSH register. Note: These bits will be momentarily cleared by the hardware during hardware endpoint re-priming operations when a dTD is retired, and the dQH is updated. ERBR[15] - Endpoint 15 ERBR[1] - Endpoint 1 ERBR[0] - Endpoint 0

0x125201BC USB3_HS_USB_OTG_HS_ENDPTCOMPLETE

Type: Read/write control
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The register is the endpoint complete register. This register is only used in the device mode.

USB3_HS_USB_OTG_HS_ENDPTCOMPLETE

Bits	Name	Description
31:16	ETCE_15_0	Endpoint transmit complete event Each bit indicates that a transmit event (IN/INTERRUPT) occurred and the software should read the corresponding endpoint queue to determine the endpoint status. If the corresponding IOC bit is set (1) in the transfer descriptor, then this bit will be set (1) simultaneously with the USBINT. Writing a one will clear the corresponding bit in this register. ETCE[15] - Endpoint 15 ETCE[1] - Endpoint 1 ETCE[0] - Endpoint 0
15:0	ERCE_15_0	Endpoint receive complete event Each bit indicates that a received event (OUT/SETUP) occurred and the software should read the corresponding endpoint queue to determine the transfer status. If the corresponding IOC bit is set (1) in the transfer descriptor, then this bit will be set (1) simultaneously with the USBINT. Writing a one will clear the corresponding bit in this register. ERCE[15] - Endpoint 15 ERCE[1] - Endpoint 1 ERCE[0] - Endpoint 0

0x125201C0 USB3_HS_USB_OTG_HS_ENDPTCTRL0

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00800080

The USB_OTG_HS_ENDPTCTRL0 register is the endpoint control 0 register. Every device will implement endpoint0 as a control endpoint.

USB3_HS_USB_OTG_HS_ENDPTCTRL0

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.

USB3_HS_USB_OTG_HS_ENDPTCTRL0 (cont.)

Bits	Name	Description
23	TXE	Tx endpoint enable value 1 = Enabled Endpoint0 is always enabled. Read only
22:20	RESERVED_BITS22_20	Clear (0) these bits.
19:18	TXT	Tx endpoint type Read only value 00 = Control Endpoint0 is fixed as a control end point.
17	RESERVED_BIT17	Clear (0) this bit.
16	TXS	Tx endpoint stall Read/write value 0 = End point OK (default) value 1 = End point stalled The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. It will continue returning STALL until the bit is cleared (0) by the software or it will automatically be cleared (0) upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). Note: There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. In most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15:8	RESERVED_BITS15_8	Clear (0) these bits.
7	RXE	Rx endpoint enable value 1 = Enabled Endpoint0 is always enabled. Read only
6:4	RESERVED_BITS6_4	Clear (0) these bits.
3:2	RXT	Rx endpoint type Read only value 00 = Control Endpoint0 is fixed as a control end point.
1	RESERVED_BIT1	Clear (0) this bit.

USB3_HS_USB_OTG_HS_ENDPTCTRL0 (cont.)

Bits	Name	Description
0	RXS	Rx endpoint stall Read/write value 0 = End point OK (default) value 1 = End point stalled The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. It will continue returning STALL until the bit is cleared (0) by the software or it will automatically be cleared (0) upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). Note: There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. In most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

0x125201C0+4*n USB3_HS_USB_OTG_HS_ENDPTCTRLn, n=[1..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTCTRLn register is the endpoint control n register. There is an ENDPTCTRLn register for each endpoint in a device.

CAUTION If one endpoint direction is enabled and the paired endpoint of the opposite direction is disabled, then the unused direction type must be changed from the default control-type to any other type (such as bulk-type). Leaving an unconfigured endpoint control will cause undefined behavior for the data PID tracking on the active endpoint/direction.

USB3_HS_USB_OTG_HS_ENDPTCTRLn

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.
23	TXE	Tx endpoint enable value 0 = Disabled (default) value 1 = Enabled An endpoint should be enabled only after it has been configured.

USB3_HS_USB_OTG_HS_ENDPTCTRLn (cont.)

Bits	Name	Description
22	TXR	Tx data toggle reset (WS) value 1 = Reset PID sequence Whenever a configuration event is received for this endpoint, the software must set (1) this bit in order to synchronize the data PIDs between the host and device.
21	TXI	Tx data toggle inhibit value 0 = PID sequencing enabled (default) value 1 = PID sequencing disabled This bit is only used for testing and should always be cleared (0). Setting (1) this bit will cause this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.
20	RESERVED_BIT20	Clear (0) this bit.
19:18	TXT	Tx endpoint type value 00 = Control value 01 = Isochronous value 10 = Bulk value 11 = Interrupt
17	TXD	Tx endpoint data source value 0 = Dual port memory buffer/DMA engine (default) This bit should always be cleared (0).
16	TXS	Tx endpoint stall value 0 = End point OK value 1 = End point stalled This bit will be cleared (0) automatically upon receipt of a SETUP request if this endpoint is configured as a control endpoint, and this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. This control will continue to STALL until this bit is either cleared (0) by the software or automatically cleared (0) as described above for control endpoints. Note (control endpoint types only): There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. in most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15:8	RESERVED_BITS15_8	Clear (0) these bits.
7	RXE	Rx endpoint enable value 0 = Disabled (default) value 1 = Enabled An endpoint should be enabled only after it has been configured.

USB3_HS_USB_OTG_HS_ENDPTCTRLn (cont.)

Bits	Name	Description
6	RXR	Rx data toggle reset (WS) Write 1 = Reset PID sequence Whenever a configuration event is received for this endpoint, the software must set (1) this bit in order to synchronize the data PIDs between the host and the device.
5	RXI	Rx data toggle inhibit value 0 = Disabled (default) value 1 = Enabled This bit is only used for testing and should always be cleared (0). Setting (1) this bit will cause this endpoint to ignore the data toggle sequence and always accept a data packet regardless of their data PID.
4	RESERVED_BIT4	Clear (0) this bit.
3:2	RXT	Rx endpoint type value 00 = Control value 01 = Isochronous value 10 = Bulk value 11 = Interrupt
1	RXD	Rx endpoint data sink value 0 = Dual port memory buffer/DMA engine (default) This bit should always be cleared (0).
0	RXS	Rx endpoint stall value 0 = End point OK value 1 = End point stalled This bit will be cleared (0) automatically upon receipt of a SETUP request if this endpoint is configured as a control endpoint, and this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. This control will continue to STALL until this bit is either cleared (0) by the software or automatically cleared (0) as described above for control endpoints. Note (control endpoint types only): There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. in most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

0x125201FC+4*n USB3_HS_USB_OTG_HS_ENDPT_PIPE_IDn, n=[1..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x001F001F

The USB_OTG_HS_ENDPT_PIPE_IDn register is the endpoint pipe number register. There is an USB_OTG_HS_ENDPT_PIPE_IDn register for each endpoint in a device.

NOTE reset value of TX_PIPE_ID and RX_PIPE_ID is 0x1F, which means that Endpoint is not mapped to any pipe.

USB3_HS_USB_OTG_HS_ENDPT_PIPE_IDn

Bits	Name	Description
31:21	RESERVED_BITS31_21	Clear (0) these bits.
20:16	TX_PIPE_ID	This field indicate the pipe number that this tx end point (n) will use in pipe mode.
15:5	RESERVED_BITS15_5	Clear (0) these bits.
4:0	RX_PIPE_ID	This field indicate the pipe number that this rx end point (n) will use in pipe mode.

0x12520240 USB3_HS_USB_OTG_HS_PHY_CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0b1110000111010

The USB_OTG_HS_PHY_CTRL register is used to configure various features in the Synopsys 28nm PHY.

USB3_HS_USB_OTG_HS_PHY_CTRL

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12	USB2_PHY_IDHV_CLAMP_EN	Clamp enable for IDHV interrupt level shifter from USB VDD180 domain to VDDCX domain. When set (1), VLS is active and IDHV interrupt is translated from 1.8V domain to Vddcx domain. When clear (0), VLS is clamped high. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.
11	USB2_PHY_OTGSESSVLDHV_CLAMP_EN	Clamp enable for OTGSESSVLDHV interrupt level shifter from USB VDD180 domain to VDDCX domain. When set (1), VLS is active and OTGSESSVLDHV interrupt is translated from 1.8V domain to Vddcx domain. When clear (0), VLS is clamped to zero. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.

USB3_HS_USB_OTG_HS_PHY_CTRL (cont.)

Bits	Name	Description
10	PHY_MPM_HV_CLAMP_EN	Clamp enable for HV interrupts level shifters from USB VDD180 domain to VDDPAD MPM in usb2 phy wrapper. When set (1), VLS is active and HV interrupts are translated from 1.8V domain to MPM Vdd domain. When clear (0), VLS is clamped to inactive state. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.
9	USB2_PHY_OTGSESSVLD HV_INTEN	Enable HV session valid interrupt from phy. This interrupt translated with level shifter for wakeup from retention when VDDCX is nominal and TCXO is running.
8	USB2_PHY_IDHV_INTEN	Enable HV id pin interrupt from phy. This interrupt translated with level shifter for wakeup from retention when VDDCX is nominal and TCXO is running.
7	USB2_PHY_ULPI_POR	Reset for ULPI PHY Wrapper and ULPI clock domain logic in usb2_phy_wrapper.
6:4	USB2_PHY_FSEL	Reference Clock Frequency Select 011 (Assumes 19.2MHz default)
3	HOST_PORTCTRL_FORCE _SUSEN	Chicken bit for CR-0000153908 - when this bit set the core will enter to low power mode when portctrl host sm enter to suspend mode. Default value is 1.
2	USB2_PHY_SIDDQ	IDDQ Test Enable.
1	USB2_PHY_RETEN	Retention mode enable/disable
0	USB2_PHY_POR	Power-On-Reset (Analog configuration needs to happen before POR is set to 0)

0x12520244 USB3_HS_USB_OTG_HS_GENERIC1

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

The USB_OTG_HS_GENERIC1 register.

USB3_HS_USB_OTG_HS_GENERIC1

Bits	Name	Description
31:16	USB_HS_TX_DEPTH	TX_DEPTH is the number of words in the TX buffer. This number is calculated by the number of bytes allocated per Endpoint divided by 4, times the number of endpoints. The RAM width is 36. In HS USB this value is usually 512 bytes per EP, and for FS ONLY USB it is usually 64 Bytes per EP.
15:0	USB_HS_RX_DEPTH	RX_DEPTH is the number of words in the RX buffer. This number is usually 256, but can support powers of 2 up to 4096. The RAM width is 36.

0x12520248 USB3_HS_USB_OTG_HS_GENERIC2

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

The USB_OTG_HS_GENERIC2 register.

USB3_HS_USB_OTG_HS_GENERIC2

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.
15	USE_SPS_AHB2AHB	USE_SPS_AHB2AHB generic specifies if AHB2AHB bridge is connected between BAM and SPS Fabric AHB.
14	LPM_SUPPORT	The LPM_SUPPORT generic specifies if USB support Link Power Management.
13:9	USB_HS_DEV_EP	The number of USB endpoints. Valid values for the number of Endpoints are 4, 8, and 16
8:3	MAX_PIPES	The number of simultaneous parallel pipes supported by the BAM. Supported values are 2 to 30
2	USE_SPS	The USE_SPS generic specifies if Bam is connected to USB core.
1	USE_HSIC	The USE_HSIC generic specifies if an HSIC is connected to USB core.
0	UTMI_PHY_SW_IF_EN	The UTMI_PHY_SW_IF_EN generic specifies if UTMI phy Register Interface is enabled

0x12520250 USB3_HS_USB_OTG_HS_L1_EP_CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0000FFFF

The USB_OTG_HS_L1_EP_CTRL register enables/disables transition to L1 and exit from L1 state when specific TX endpoints are primed.

USB3_HS_USB_OTG_HS_L1_EP_CTRL

Bits	Name	Description
31:16	TX_EP_PRIME_L1_EXIT	Those bit's enables Remote Wakeup in L1 state when SW starts Priming The specific Endpoint.
15:0	TX_EP_PRIME_L1_EN	Control bit's that enables/disables transition to L1 when the specific TX Endpoint is active.

0x12520254 USB3_HS_USB_OTG_HS_L1_CONFIG

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_L1_CONFIG register is used to configure various L1 features.

USB3_HS_USB_OTG_HS_L1_CONFIG

Bits	Name	Description
31:12	RESERVED_BITS31_12	Clear (0) these bits.
11	PLL_PWR_DWN_EN	Control bit that enables/disables power down of 480 MHZ PLL in L1 state.
10	PHY_LPM_EN	Control bit that enable/disables entering ULPI Low Power Mode in L1 state
9	GATE_AHB_CLK_EN	Control bit that enable/disables clock request signaling for usb_ahb_clk in L1 state
8	GATE_FS_XCVR_CLK_EN	Control bit that enable/disables clock gating of usb_fs_xcvr_clk in L1 state
7	GATE_SYS_CLK_EN	Control bit that enable/disables clock gating of usb_system_clk in L1 state
6	GATE_XCVR_CLK_EN	Control bit that enable/disables power-down of 480 MHz PLL in L1 state
5	L1_REMOTE_WAKEUP_EN	Control bit that enables/disables Remote Wakeup in L1 state. When this bit is low, then Link Controller never initiates Remote Wakeup in L1 state. When this bit is high, Link Controller can initiate Remote Wakeup.
4	LPM_EN	Control bit that enables/disables LPM support. When this bit is zero a full backward compatibility is ensured - no LPM support and no response for LPM Extended Transaction
3:0	PLL_TURNOFF_MIN_HIRD	Specifying a minimum expected HIRD value from Host that enables HW mechanism for turning off the 480 MHz PLL. The default value is 50us.

0x12520258 USB3_HS_USB_OTG_HS_LPM_DEBUG_1

Type: Read/Clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_DEBUG_1 register is for debug and testing purposes mostly.

USB3_HS_USB_OTG_HS_LPM_DEBUG_1

Bits	Name	Description
31:16	DEBUG_L1_LONG_ENT_CNT	Count number of exits from L1 where duration in L1 is > 200us. Writing to this register clears the counter.
15:0	DEBUG_L1_SHORT_ENT_CNT	Count number of exits from L1 where duration in L1 is <= 200us. Writing to this register clears the counter.

0x1252025C USB3_HS_USB_OTG_HS_LPM_DEBUG_2

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_DEBUG_2 register is for debug and testing purposes mostly.

USB3_HS_USB_OTG_HS_LPM_DEBUG_2

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12:9	L1_RMT_WKUP_TIME	Read/write Specifying How much time the device drives remote wakeup. The default Value is 50us for reset value. Add the value of this register (in us) to the remote wakeup time.
8	L1_FPR	Read/write L1 Force port resume, The software sets (1) this bit to drive resume signaling.
7	HSIC_CLK_PLL_BYPASSNL	Read only. Disables PLL analog logic. Active low. Connects to bypassnl input of NT_PLL.
6	HSIC_CLK_PLL_RESET	Read only. Resets all FF in PLL. Active low. Connects to reset_n input of NT_PLL.
5	HSIC_CLK_GATE	Read only. Clock gating of hsic_clk and ulpi_clk, without turning off HSIC PLL.
4	FS_XCVR_CLK_GATE	Read only. Clock gating of cc_usb_xcvr_fs_clk
3	SYS_CLK_GATE	Read only. Clock gating of cc_usb_system_clk
2	AHB_CLK_GATE	Read only. Clock gating of usb_ahb_clk

USB3_HS_USB_OTG_HS_LPM_DEBUG_2 (cont.)

Bits	Name	Description
1	L1_STATE	Read only. Status bit indicating if Device is in L1 state. When this bit high, Link Controller and HSIC PHY are in L1 state
0	DEBUG_L1_EN	Read/write Control bit that enable/disables DEBUG counters operation.

0x12520260 USB3_HS_USB_OTG_HS_LPM_ATTRIBUTES

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_ATTRIBUTES register store the bmAttribute Field of the LPM transaction.

USB3_HS_USB_OTG_HS_LPM_ATTRIBUTES

Bits	Name	Description
31:5	RESERVED_BITS31_5	Clear (0) these bits.
4	BREMOTEWAKE	A value of one (1B) in this field enables the addressed device to wake the host upon any meaningful application-specific event (e.g. an interrupt for a device with one or more interrupt endpoints). A value of zero (0B) disables the device from initiating remote wake.
3:0	HIRD	Host Initiated Resume Duration.

20.32 USB3 HS BAM Registers (0x12522000 USB3_HS_BAM_BASE)

This section contains the USB3 BAM registers.

BAM supports only Word (4 byte) aligned writes and reads on the Configuration Bus interface.

BAM has MAX_PIPES hardware generic parameter defining the number of pipes it supports. Each BAM can have up to 31 pipes supported.

BAM has BAM_CONF_AHBS_ADDR_WIDTH hardware generic parameter defining the Bit Number for selecting BAM access or Peripheral access. Legal Ranges are 14 to 20. Count starts from 1, meaning a value of 17 will set BAM Base address as 0x0001_0000.

20.32.1 BAM control registers

BAM Control registers configure the BAM operational state, SW reset, interrupts and others.

0x12522F80 USB3_HS_BAM_CTRL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

BAM Control register allows global controls for the BAM.

USB3_HS_BAM_CTRL

Bits	Name	Description
31:17	RESERVED_BITS31_17	Set to Zero (0)
16	IBC_DISABLE	This Bit enables power saving by disabling the inactivity clock timer/counter. This is useful when: 1) The BAM is Enabled but idling for long periods. 2) The BAM is Enabled and running but the inactivity timers/counters are not required by the SW for operating the BAM. When the BAM is Disabled, it automatically shuts down those timers to save power. 1’b1 - Enable Power Saving Mode 1’b0 - Disable Power Saving Mode

USB3_HS_BAM_CTRL (cont.)

Bits	Name	Description
15	BAM_CACHED_DESC_STORE	This Bit enables storage of a cached Descriptor into RAM when doing Context Switch and loading it back when returning to this pipe. This is relevant for System Modes Only. BAM to BAM Consumer mode doesn't have this option. Enabling this makes the Context Switch process slightly longer but reduces AHB Descriptor Fetch time later on. It also reduces the number of descriptor fetches done by the BAM if BAM is treating more than 2 pipes. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
14:13	BAM_DESC_CACHE_SEL	This Selector chooses which Descriptor Caching mode will be used. This is relevant for System Producer or Consumer modes only. 2’b00 - Cache when current descriptor has less than 64 bytes left. 2’b01 - Cache when current descriptor has less than 128 bytes left. 2’b10 - Immediate Auto cache - cache will happen whenever there are no descriptors cached. This might cause unnecessary descriptors reads when switching between more than 2 pipes. It is the most effective when each pipe processes more bytes than there are in an average descriptor (small descriptors, big block size), or when working with 2 or less pipes. 2’b11 - Cache when descriptor is needed only. This results in 1 descriptor present in cache at most. Available in BAM only
12	RESERVED_BITS12	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_SIC_SEL
11:5	BAM_TESTBUS_SEL	Set to Zero (0) Obsolete field: BAM_TESTBUS_SEL Test Bus selector. Supported until (including) bam_p3q3r29 (BlackBird). Moved to a dedicated register - BAM_TEST_BUS_SEL in the following releases.
4	BAM_EN_ACCUM	When Enabled, BAM will accumulate data written by the peripheral in Direct Mode into INCR8 Bursts. This is an optimization feature for Producer Direct Mode cases. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
3	RESERVED_BITS3	Set to Zero (0)
2	RESERVED_BITS2	Set to Zero (0)

USB3_HS_BAM_CTRL (cont.)

Bits	Name	Description
1	BAM_EN	After reset the BAM wakes up in Disabled Mode. While Disabled, BAM operates in Legacy mode (all the transfers from the peripheral go around the BAM as if it doesn't exist) Software Enables this bit to allow BAM operation. This bit doesn't affect the PIPE enable bit in BAM_P_CTRL register. The only possibility to Disable the BAM after it has been enabled is by Hardware or Software reset. 1'b1 - Enabled 1'b0 - Disabled
0	BAM_SW_RST	This will reset the BAM & all Pipes. Software may use this to reset the BAM. As long as the bit remains high the BAM remains in reset state. Software should clear this bit 1'b1 - Reset state 1'b0 - Normal state

0x12522F84 USB3_HS_BAM_REVISION

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a hard coded revision number of the BAM RTL. This corresponds to the BAM target number in the IMS. Also additional BAM settings are reflected here.

USB3_HS_BAM_REVISION

Bits	Name	Description
31:24	INACTIV_TMR_BASE	This indicates the width of the inactivity timers base counter
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	NUM_INACTIV_TMRS	This bit is checked only if INACTIV_TMRS_EXST = 1. This bit indicates how many inactivity timers are implemented according to value of INACTIVITY_TIMERS_SUPPORTED generic: 1'b1 - One timer for global BAM activity (INACTIVITY_TIMERS_SUPPORTED = 1) 1'b0 - MAX_PIPES timers for each pipe activity (INACTIVITY_TIMERS_SUPPORTED = 2)
19	INACTIV_TMRS_EXST	This indicates BAM has inactivity timers. 1'b1 - Timers available (INACTIVITY_TIMERS_SUPPORTED = 1 or 2) 1'b0 - No timers available (INACTIVITY_TIMERS_SUPPORTED = 0)

USB3_HS_BAM_REVISION (cont.)

Bits	Name	Description
18	HIGH_FREQUENCY_BAM	This indicates BAM has Double Sampling on the Ack On Success interface. 1'b1 - Ack On Success double sampled 1'b0 - No double sampling of Ack On Success
17	BAM_HAS_NO_BYPASS	This field indicates BAM has no bypass on the AHB Data bus, from the Peripheral AHB Master to the fabric. When Bypass is available, it is the default routing when BAM is disabled. 1'b1 - No Bypass 1'b0 - Bypass Exists
16	SECURED	This field indicates BAM/BAM-Lite has security support (APU inside) 1'b1 - Secured 1'b0 - Not Secured
15:12	RESERVED_BITS15_12	Set to Zero (0)
11:8	NUM_EES	This indicates the Number of Interrupt Lines (Execution Environments) supported by the BAM. When 1 EE is supported, only the BAM_IRQ_SRCS*_EE0 registers exist. When 4 EEs are supported, all BAM_IRQ_SRCS*_EEn registers exist for n=[0..3].
7:0	REVISION	This field contains the revision number of the core, Hard Coded. 8'h01 - Voyager (bam_p3q3r22 +) 8'h02 - BlackBird (bam_p3q3r27 +) 8'h03 - Waverider BAM (bam_p3q3r30 +) 8'h04 - Aurora BAM (bam_p3q2r43 +) 8'h05 - Shelby BAM (bam_p2q2r45 +) 8'h10 - Waverider BAM Lite (bam_lite_p1q1r0 +) 8'h11 - Aurora BAM Lite (bam_lite_p3q2r16 +) 8'h12 - Shelby BAM Lite (bam_lite_p2q2r18 +)

0x12522FBC USB3_HS_BAM_NUM_PIPES

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a the hard coded number of pipes in the BAM. Since each BAM may have a different number of pipes instantiated in HW, this register allows the SW to know this parameter. The reset state value doesn't have any meaning in this register since it is a constant.

USB3_HS_BAM_NUM_PIPES

Bits	Name	Description
31:24	BAM_NON_PIPE_GRP	This field contains the number of BAM Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
23:16	PERIPH_NON_PIPE_GRP	This field contains the number of Peripheral's Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
15:8	RESERVED_BITS15_8	Set to Zero (0)
7:0	BAM_NUM_PIPES	This field contains the number of pipes available in this BAM

0x12522FC0 USB3_HS_BAM_TIMER

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the BAM (all the pipes are in idle state).

USB3_HS_BAM_TIMER

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12522FC4 USB3_HS_BAM_TIMER_CTRL

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The register can be written and read only when INACTIVITY_TIMERS_SUPPORTED generic equals to 1.

The resolution of the BAM inactivity timer are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define

the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * TIMER_TRSHLD.

USB3_HS_BAM_TIMER_CTRL

Bits	Name	Description
31	TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1 to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	TIMER_RUN	Will be used along with TIMER_MODE Not implemented at this time. Set to zero(0)
29	TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12522F88 USB3_HS_BAM_DESC_CNT_TRSHLD

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds a threshold value for the counter summing the Size of the Descriptors Provided. This value is Global for all pipes but it is relevant for System Producer BAM mode and Both Consumer modes, where Descriptors summing takes place in order to provide the information to the peripheral via pipe bytes free (producer) or pipe bytes available interfaces.

USB3_HS_BAM_DESC_CNT_TRSHLD

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0).
15:0	CNT_TRSHLD	Threshold value. The maximum allowed value is 32kByte. Available in BAM only

0x12522F8C USB3_HS_BAM_IRQ_SRCS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking out this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register points to the physical BAM_IRQ_SRCS_EE0 register.

USB3_HS_BAM_IRQ_SRCS

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12522F90 USB3_HS_BAM_IRQ_SRCS_MSK

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register points to the physical BAM_IRQ_SRCS_MSK_EE0 register.

USB3_HS_BAM_IRQ_SRCS_MSK

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12522FB0 USB3_HS_BAM_IRQ_SRCS_UNMASKED

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register points to the physical BAM_IRQ_SRCS_UNMASKED_EE0 register.

USB3_HS_BAM_IRQ_SRCS_UNMASKED

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

0x12522F94 USB3_HS_BAM_IRQ_STTS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only.

Clearing the interrupt bits is done by writing to BAM_IRQ_CLR register.

USB3_HS_BAM_IRQ_STTS

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
3	BAM_EMPTY_IRQ	This interrupt is for DEBUG purpose only. It should not be used in normal SW flows. The interrupt indicates the BAMs buffer is empty. This bit can become high only when BAM_DATA_ERASE or BAM_DATA_FLUSH is high in BAM_TEST_BUS_SEL register.
2	BAM_ERROR_IRQ	This Indicates a Fatal Error has happened in the BAM. Currently this might happen due to an UnSuccessful Pipe Reset operation.

USB3_HS_BAM_IRQ_STTS (cont.)

Bits	Name	Description
1	BAM_HRESP_ERR_IRQ	This interrupt Indicates that an Erroneous HResponse has been received by the AHB Master. Additional Information about the error may be read at BAM_AHB_MASTER_ERR_* Registers. Clearing this interrupt also clears the BAM_AHB_MASTER_ERR_* Registers. Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12522F98 USB3_HS_BAM_IRQ_CLR

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

USB3_HS_BAM_IRQ_CLR

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
3	BAM_EMPTY_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM-Lite only
2	BAM_ERROR_CLR	1'b1 - Clear 1'b0 - Unchanged
1	BAM_HRESP_ERR_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12522F9C USB3_HS_BAM_IRQ_EN

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the BAM Interrupt Status register.

USB3_HS_BAM_IRQ_EN

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_EN	Enables Inactivity timer interrupt by writing this bit 1'b1 - Enable 1'b0 - Disable
3	BAM_EMPTY_EN	1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
2	BAM_ERROR_EN	1'b1 - Enable 1'b0 - Disable
1	BAM_HRESP_ERR_EN	1'b1 - Enable 1'b0 - Disable Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12522FA0 USB3_HS_BAM_RESERVED_1

Type: Read
Clock: BAM_CLK
Reset State: 0x00000000

USB3_HS_BAM_RESERVED_1

Bits	Name	Description
31	RESERVED_BITS31	Set to Zero (0) Obsolete field: BAM_IRQ_SIC_SEL
30:0	RESERVED_BITS30_0	Set to Zero (0) Obsolete field: P_IRQ_SIC_SEL

0x12522FA4 USB3_HS_BAM_AHB_MASTER_ERR_CTRLS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

USB3_HS_BAM_AHB_MASTER_ERR_CTRLS

Bits	Name	Description
31:23	RESERVED_BITS31_16	Set to Zero (0)
22:18	BAM_ERR_HVMID	HVMID
17	BAM_ERR_DIRECT_MODE	DIRECT MODE
16:12	BAM_ERR_HCID	HCID
11:8	BAM_ERR_HPROT	HPROT
7:5	BAM_ERR_HBURST	HBURST
4:3	BAM_ERR_HSIZE	HSIZE
2	BAM_ERR_HWRITE	HWRITE
1:0	BAM_ERR_HTRANS	HTRANS

0x12522FA8 USB3_HS_BAM_AHB_MASTER_ERR_ADDR

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

USB3_HS_BAM_AHB_MASTER_ERR_ADDR

Bits	Name	Description
31:0	BAM_ERR_ADDR	HADDR

0x12522FAC USB3_HS_BAM_AHB_MASTER_ERR_DATA

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

USB3_HS_BAM_AHB_MASTER_ERR_DATA

Bits	Name	Description
31:0	BAM_ERR_DATA	HDATA

0x12522FB4 USB3_HS_BAM_RESERVED_2

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

USB3_HS_BAM_RESERVED_2

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_IRQ_DEST_ADDR

0x12522FB8 USB3_HS_BAM_RESERVED_3

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

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USB3_HS_BAM_RESERVED_3

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_DEST_ADDR

0x12522FF0 USB3_HS_BAM_TRUST_REG

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside - SECURED field in the BAM_REVISION register) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

USB3_HS_BAM_TRUST_REG

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_VMID	Those bits indicate the VMID value to be used when performing BAM type accesses to the bus. BAM Type accesses include BAM MTI (or Direct Mode accesses, not applicable for BAM Lite)
7	BAM_RST_BLOCK	When enabled, the BAM Global SW reset will not be available for usage. This is in order to deny Global SW reset requests by the Global security group. 1'b1 - Enable 1'b0 - Disable
6:2	RESERVED_BITS6_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_EE	This Field Indicates the EE (0,1,2,3) to which the BAM Interrupt belongs to. The pipe interrupts will fire on the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12522FF4 USB3_HS_BAM_TEST_BUS_SEL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This is the testbus selector register.

Supported in releases after bam_p3q3r29 (BlackBird).

USB3_HS_BAM_TEST_BUS_SEL

Bits	Name	Description
31:19	RESERVED_BITS31_19	Set to Zero (0)
18	BAM_DATA_ERASE	When enabled, BAM will be instructed to erase all the data it currently has inside. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1’b1 - Enable Erase 1’b0 - Disabled
17	BAM_DATA_FLUSH	When enabled, BAM will be instructed to flush all the data it currently has inside. BAM will only flush the data once it has enough data and a valid destination for it. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1’b1 - Enable Flush 1’b0 - Disabled
16	BAM_CLK_ALWAYS_ON	This bit controls the BAM to issue ’always on’ clock request. 1’b1 - Enable Always On clock request. 1’b0 - Disabled
15:7	RESERVED_BITS15_7	Set to Zero (0)
6:0	BAM_TESTBUS_SEL	Test Bus selector. Values with bit[11] set high are reserved for the BAM Lite integrator to provide testbus from outside of the BAM Lite. For example, eDML testbus may reside at X’100_0000’ to X’111_1111’ selector values. eDML has no registers thus has no test bus selector, so its test bus is combined with the BAM lite’s. BAM provides zeroes on its testbus when external values selected. X’000_0000’ - Zeros X’000_0001’ - Slave test bus X’000_0010’ - Pipe state machine test bus X’000_0011’ - Buffer test bus X’000_0100’ - Sideband test bus X’000_1101’ - Bus Manager test bus X’001_0000’ - Reg file test bus X’1’’_’’’’ - BAM Lite sets zeroes on the test bus, leaving it for external use

0x12522FF8 USB3_HS_BAM_TEST_BUS_REG

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the value being output to the testbus of the chip. It is not intended for SW usage but for lab debugging of the BAM. Values here can change every cycle.

USB3_HS_BAM_TEST_BUS_REG

Bits	Name	Description
31:0	BAM_TESTBUS_REG	32 bit Testbus value. To select the Block in BAM to show here, use the BAM_TESTBUS_SEL field in BAM_CTRL register.

0x12522FFC USB3_HS_BAM_CNFG_BITS

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM configuration bits for bug fixes. It is highly recommended to follow the directions for each bit and set it accordingly.

USB3_HS_BAM_CNFG_BITS

Bits	Name	Description
31:27	RESERVED_BITS31_27	Set to Zero (0)
26	BAM_AU_ACCUMED	Recommended value: 1 This bit fixes a bug in the Ack Update state machine, where an overflow happened while counting descriptors and reaching more than 64kB of calculated sizes. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only
25	BAM_PSM_P_HD_DATA	Recommended value: 1 This bit allows pipe state machine to ignore retransmission requests if a pipe has just been initialized and process those as a regular fetch request. (consumer modes only). When this bit disabled, BAM could fetch descriptors for a pipe which was reset and no descriptors were added yet, if a retransmission request followed after the reset. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only

USB3_HS_BAM_CNFG_BITS (cont.)

Bits	Name	Description
24	BAM_REG_P_EN	Recommended value: 1 This bit fixes the pipe configuration signals mux for the current active pipe in 2 pipes BAM. When disabled, internal state machines might get into enabled states while the pipe is disabled. This would typically happen after pipe reset. 1'b1 - Enable 1'b0 - Disable Available in BAM only
23	BAM_WB_DSC_AVL_P_RST	Recommended value: 1 This bit allows the Writeback state machine to reset the vector indicating there are available descriptors when a pipe reset occurs. If disabled, BAM might fetch descriptors after resetting and reconfiguring a pipe, even though no Event (descriptors) was provided.. 1'b1 - Enable 1'b0 - Disable Available in BAM only
22	BAM_WB_RETR_SVPNT	Recommended value: 1 This bit fixes a bug where a pipe which was reset, still stored its retransmission savepoint, but into the illegal's pipe address space, thus hurting the last pipe of the BAM if the BAM had a total 4, 8 or 16 pipes. This is relevant for Producer to System modes only. (CR-0000151585) 1'b1 - Enabled 1'b0 - Disable Available in BAM only
21	BAM_WB_CSW_ACK_IDL	Recommended value: 1 This bit allows the Writeback state machine to switch into idle state prior to visiting disabled state. This is needed when context switching from mode X to another pipe of mode X is well. This is required to fix a bug in the 2 pipes BAM. 1'b1 - Enable 1'b0 - Disable Available in BAM only
20	BAM_WB_BLK_CSW	Recommended value: 1 When Enabled, this bit does not allow context switch to happen in the Writeback state machine until it has created a descriptor. This is relevant when the descriptor fifo is becoming full and there's no space to create a descriptor, while another pipe is context switching. This might result in the descriptor not to be created ever, if it was the last one for that pipe. Relevant for Producer BAM-to-BAM mode only. 1'b1 - Enable 1'b0 - Disable Available in BAM only

USB3_HS_BAM_CNFG_BITS (cont.)

Bits	Name	Description
19	BAM_WB_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Writeback state machine when performing pipe reset. 1’b1 - 1’b0 - Disable Available in BAM only
18	BAM_SI_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Sideband Inform state machine when performing pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
17	BAM_AU_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Ack Update state machine when performing pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
16	BAM_PSM_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Pipe state machine when performing pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
15	BAM_PSM_CSW_REQ	Recommended value: 1 This bit forces the context switch request from pipe state machine to RAM controller not to last longer than the slave requested. (2 Pipes BAM bug fix) 1’b1 - Enable 1’b0 - Disable Available in BAM only
14	BAM_SB_CLK_REQ	Recommended value: 1 This bit allows the clock request from the sideband block to propagate into the BAM’s common clock request. 1’b1 - Propagate Sideband Clock Request 1’b0 - Disable Available in BAM only
13	BAM_IBC_DISABLE	Recommended value: 1 This bit helps to save power by allowing the BAM to keep the inactivity base counter in reset when BAM is disabled or when SW configures IBC_DISABLE bit high. 1’b1 - Enable Power Saving 1’b0 - Disable Power Saving

USB3_HS_BAM_CNFG_BITS (cont.)

Bits	Name	Description
12	BAM_NO_EXT_P_RST	Recommended value: 1 This bit allows the BAM / BAM Lite to ignore the externally connected blocks (eDML) when doing pipe reset. The BAM, once instructed to pipe reset, first thing lets the externally connected block know a reset is needed. Then it waits for the externally connected block to Acknowledge it is ready for the pipe reset (meaning it doesn't push any data for the reset pipe) and then the BAM Lite completes the pipe reset operation internally. When disabled, the BAM doesn't require any Acknowledge from the external block to perform pipe reset. 1’b1 - Enable external block pipe reset 1’b0 - Disable - ignore external block pipe reset
11	BAM_FULL_PIPE	Recommended value: 0 This enables the BAM support for a BAM to BAM Producer which insists to write to a full pipe. When 0, BAM might issue data overflow if producers write to a full pipe. When 1 BAM will not allow this and lower HReady when peripheral tries to do so. Once space is freed in the pipe, Hready will rise and the flow will continue. This functionality has been found to be buggy and was removed from APQ8064. Bit is currently unused. 1’b1 - Enable 1’b0 - Disable Available in BAM only
10:4	RESERVED_BITS10_4	Set to Zero (0)
3	BAM_ADML_SYNC_BRIDGE	0x1: Use a Synchronous Configuration bridge in aDML. 0x0: Use a Asynchronous Configuration bridge in aDML.
2	BAM_PIPE_CNFG	Recommended value: 1 Pipe SM upgrade for writing EOT bit to the previous descriptor. It’s invoked only when EOB arrives in the end of a descriptor. It is highly recommended to set this bit high. Leaving it low might cause incorrect Pipe Bytes Free value reported to peripheral in rare cases. 1’b1 - Enable 1’b0 - Disable Available in BAM only
1	BAM_ADML_DEEP_CONS_FIFO	0x1: Use a deep Consumer FIFO in aDML (16 dwords) 0x0: Use a shallow Consumer FIFO in aDML (8 dwords)
0	BAM_ADML_INCR4_EN_N	0x1: Don’t allow INCR4 aDML-BAM accesses. 0x0: Allow INCR 4 aDML-BAM accesses.

0x12523800+ 128*n USB3_HS_BAM_IRQ_SRCS_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register has an alias - BAM_IRQ_SRCS register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

USB3_HS_BAM_IRQ_SRCS_EEn

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12523804+ 128*n USB3_HS_BAM_IRQ_SRCS_MSK_EEn, n=[0..3]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register has an alias - BAM_IRQ_SRCS_MSK register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

USB3_HS_BAM_IRQ_SRCS_MSK_EEn

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12523808+ 128*n USB3_HS_BAM_IRQ_SRCS_UNMASKED_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register has an alias - BAM_IRQ_SRCS_UNMASKED register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

USB3_HS_BAM_IRQ_SRCS_UNMASKED_EEn

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

20.32.2 BAM PIPE management registers

BAM Pipe management registers control each pipe's parameters. Those reside in physical registers.

0x12522000+ 128*n USB3_HS_BAM_P_CTRLn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Control register provides various controls for the pipe.

USB3_HS_BAM_P_CTRLn

Bits	Name	Description
31:11	RESERVED_BITS31_11	Set to Zero (0)
10:9	P_PREFETCH_LIMIT	Bam Lite feature Selects the number of bytes to be pre-fetched by the Bam Lite, once a peripheral requests to read data from a pipe. This feature is relevant for Consumer modes only. 2'b00 - 32 bytes at most (INCR8) 2'b01 - 16 bytes at most (INCR4) 2'b10 - 4 bytes at most (SINGLE) Available in BAM-Lite only

USB3_HS_BAM_P_CTRLn (cont.)

Bits	Name	Description
8:7	P_AUTO_EOB_SEL	Bam Lite feature. Selects the number of bytes to be processed before creating End Of Block indication internally by the BAM. See P_AUTO_EOB. Descriptors generated by this feature (bam to bam producer mode) will always be of the chosen size, unless an End Of Transfer, causes a smaller descriptor to be created. 2'b00 - 512 Bytes 2'b01 - 256 Bytes 2'b10 - 128 Bytes 2'b11 - 64 Bytes Available in BAM-Lite only
6	P_AUTO_EOB	BAM Lite feature. When Enabled, the BAM Lite will ignore any incoming End Of Block indications from the peripheral (if any). Instead, the BAM Lite will generate it's own End Of Block indications internally, every P_AUTO_EOB_SEL bytes. This feature is relevant for Producer Bam 2 Bam modes only. It is a must for peripherals which are not able to produce End Of Block indications. 1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
5	P_SYS_MODE	This bit sets the pipe to work in System Mode, where the Software is the second side of the pipe. 1'b1 - System mode. 1'b0 - BAM to BAM mode.
4	P_SYS_STRM	Streaming Enable. Relevant to System Producer BAM mode only.When enabled, BAM will not close descriptors with End Of Transfer notifications received from peripheral, but continue writing the data to the same descriptor. 1'b1 - Enable Streaming Mode 1'b0 - None-Streaming Mode
3	P_DIRECTION	This bit denotes pipe direction. 1'b1 - The pipe can be written (producer mode) 1'b0 - The pipe can be read (consumer mode)
2	RESERVED_BITS2	Set to Zero (0)
1	P_EN	1'b1 - Enable Pipe 1'b0 - Disable Pipe
0	RESERVED_BITS0	Set to Zero (0)

0x12522004+ 128*n USB3_HS_BAM_P_RSTn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Reset register provides Pipe Reset ability. Software needs to write 1 to this register to make the Pipe Reset. Writing 0 to this register will finish the Pipe Reset. Writing zero is needed prior to Peripheral reconfiguration for the same pipe.

USB3_HS_BAM_P_RSTn

Bits	Name	Description
31:1	RESERVED_BITS31_1	Set to Zero (0)
0	P_SW_RST	This resets the pipe and its' registers, (Both Flip-Flops and RAM). 1'b1 - Reset 1'b0 - Do Nothing

0x12522008+ 128*n USB3_HS_BAM_P_HALTn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Halt register Enables/Disables the Halt Sequence.

This is a self-modifying register.

USB3_HS_BAM_P_HALTn

Bits	Name	Description
31:2	RESERVED_BITS31_2	Set to Zero (0)
1	P_PROD_HALTED	This bit is used to inform the Consumer about the Producer being in Halt mode now. This is a part of the Halt procedure. 1'b1 - Sets this bit to 1 1'b0 - Does Nothing This bit will be cleared by the HW.
0	P_HALT	When Enabled, the Pipe will enter Halt Mode. 1'b1 - Enable Halt 1'b0 - Disable Halt For B2B Producer pipes, this bit is self modifying. It doesn't need the SW to clear it.

0x12522030+ 128*n USB3_HS_BAM_P_TRUST_REGn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29 (BlackBird).

USB3_HS_BAM_P_TRUST_REGn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_P_VMID	Those bits indicate the VMID value to be used when performing Pipe type accesses to the bus. BAM Type accesses include Pipe MTI, Data and Descriptors.
7:2	RESERVED_BITS7_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_P_EE	This Field Indicates the EE (0,1,2,3) to which the Pipe Interrupt belongs to. The BAM interrupt will fire to the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12522010+ 128*n USB3_HS_BAM_P_IRQ_STTSn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only. It also has informative bits which are not interrupts.

Clearing the interrupt bits is done by writing to P_IRQ_CLR register.

USB3_HS_BAM_P_IRQ_STTSn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_IRQ	For producer this interrupt happens whenever the last AHB burst of a transfer happens For Consumer when ack_on_success closes a transfer
4	P_ERR_IRQ	Pipe Error interrupt indicates that an error has happened. TBD: Error reason is not yet defined. Interrupt not in use.
3	P_OUT_OF_DESC_IRQ	Out of descriptors interrupt has several meanings depending on the operation mode: Producer - no free space in the descriptors fifo for adding a descriptor Consumer - no descriptors in the descriptors fifo for processing IO Vectors Producer - No descriptors to read (and therefore no space for data to write to the pipe) IO Vectors Consumer - No descriptors to read (and therefore no data to read from pipe)
2	P_WAKE_IRQ	Wake peripheral interrupt signals the driver to wake up the peripheral (USB for example) for transmission via the current pipe. This interrupt is issued whenever an Event comes to the specific pipe.
1	P_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
0	P_PRCSD_DESC_IRQ	This Interrupt rises when BAM finishes processing an IO Vector which has INT bit selected

0x12522014+128*n USB3_HS_BAM_P_IRQ_CLRn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

USB3_HS_BAM_P_IRQ_CLRn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_CLR	1'b1 - Clear 1'b0 - Unchanged
4	P_ERR_CLR	1'b1 - Clear 1'b0 - Unchanged
3	P_OUT_OF_DESC_CLR	1'b1 - Clear 1'b0 - Unchanged

USB3_HS_BAM_P_IRQ_CLRn (cont.)

Bits	Name	Description
2	P_WAKE_CLR	Clear Wake peripheral interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
1	P_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
0	P_PRCSD_DESC_CLR	Clear Descriptor Processed interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged

0x12522018+ 128*n USB3_HS_BAM_P_IRQ_ENn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the Pipe Interrupt Status register.

USB3_HS_BAM_P_IRQ_ENn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_EN	1'b1 - Enable 1'b0 - Disable
4	P_ERR_EN	1'b1 - Enable 1'b0 - Disable
3	P_OUT_OF_DESC_EN	1'b1 - Enable 1'b0 - Disable
2	P_WAKE_EN	Enable Wake peripheral interrupt 1'b1 - Enable 1'b0 - Disable
1	P_TIMER_EN	Enable Inactivity timer Interrupt 1'b1 - Enable 1'b0 - Disable
0	P_PRCSD_DESC_EN	Enable Descriptor Processed Interrupt 1'b1 - Enable 1'b0 - Disable

0x1252201C+ 128*n USB3_HS_BAM_P_TIMERn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the pipe.

USB3_HS_BAM_P_TIMERn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12522020+ 128*n USB3_HS_BAM_P_TIMER_CTRLn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The resolution of the pipe inactivity timers are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the P_TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * P_TIMER_TRSHLD.

USB3_HS_BAM_P_TIMER_CTRLn

Bits	Name	Description
31	P_TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the P_TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	P_TIMER_RUN	Will be used along with P_TIMER_MODE Not implemented at this time. Set to zero(0)
29	P_TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	P_TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12522024+ 128*n USB3_HS_BAM_P_PRDCR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Producer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

USB3_HS_BAM_P_PRDCR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_producer
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	BAM_P_TOGGLE	Pipe Bytes Free Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Free Ctrl value
15:0	BAM_P_BYTES_FREE	Pipe Bytes Free value

0x12522028+ 128*n USB3_HS_BAM_P_CNSMR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Consumer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

USB3_HS_BAM_P_CNSMR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_consumer
23	BAM_P_WAIT_4_ACK	waiting_for_ack_bytes_avail_r
22	BAM_P_ACK_TOGGLE	ack_bytes_avail_toggle
21	BAM_P_ACK_TOGGLE_R	ack_bytes_avail_toggle_r
20	BAM_P_TOGGLE	Pipe Bytes Avail Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Avail Ctrl value
15:0	BAM_P_BYTES_AVAIL	Pipe Bytes AVAIL value

20.32.3 BAM PIPE configuration registers (RAM)

BAM Pipe management registers configure each pipes' parameters.

Pipe Address span: currently defining each pipe to have 32 addresses, therefore inter pipe offset is 32*4=128=0x80 bytes.

0x1252302C+ 64*n USB3_HS_BAM_P_EVNT_DEST_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Event Destination Address which is the address of BAM_P_EVNT_REG in the BAM on the other side of the Pipe.

Producer BAM will send Write Events to this address.

Consumer BAM will send Read Events to this address.

This is relevant only for BAM to BAM modes. In System modes, BAM doesn't issue Write/Read events.

USB3_HS_BAM_P_EVNT_DEST_ADDRn

Bits	Name	Description
31:0	P_EVNT_DEST_ADDR	Address of the Event Register in the peer BAM (second end of the pipe). Driver will configure this when initializing the pipe.

0x12523018+64*n USB3_HS_BAM_P_EVNT_REGn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register is where Read/Write events are sent to. If current BAM works as Producer, it will receive Read events into this register from the Consumer. If the Consumer is another BAM, it will write read events to this register. If the Consumer is the Software, it will prepare descriptors in the descriptor FIFO and update the DESC_FIFO_PEER_OFST value in this register.

If current BAM works as Consumer, opposite behavior is assumed.

USB3_HS_BAM_P_EVNT_REGn

Bits	Name	Description
31:16	P_BYTES_CONSUMED	This field is used only in the B2B mode. It indicates the number of bits consumed by the Consumer. Consumer sends this value to the Producer as a part of a read event, for the Producer to know how many bytes were consumed. When working in System mode, this value should be set to zero. BAM to BAM Producer writes zero in this value.
15:0	P_DESC_FIFO_PEER_OFST	This field indicates the Descriptor Fifo Offset Pointer of the Peer BAM (The BAM or the Software which creates descriptors). For example when current BAM works as consumer for the current pipe, Producer BAM (or the software) updates this value to let the current pipe know about the new descriptors added in the Descriptor Fifo.

0x12523000+64*n USB3_HS_BAM_P_SW_OFSTSn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register denotes the pointer Offset of the first Not Acknowledged Descriptor. Meaning all Descriptors prior to this one have been processed by the BAM. This register is only used by the Software. After receiving an interrupt, software reads this register in order to know what descriptors has been processed.

When the BAM works as Producer, Software will usually read this value after Descriptor Processed Interrupt or after the End of Transfer Interrupt.

When the BAM works as Consumer, Software will usually read this value after Descriptor Processed Interrupt.

NOTE This is non relevant in BAM to BAM modes.

NOTE Although being Writable, Software should never write to this register.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB3_HS_BAM_P_SW_OFSTSn

Bits	Name	Description
31:16	SW_OFST_IN_DESC	Offset inside the Descriptor. This value is used by the Software only when a BAM is working as System Producer. Then the SW can read this value to know how many Bytes were written to the current descriptor if it was not closed down. This is useful for Streaming mode.
15:0	SW_DESC_OFST	Descriptor FIFO offset.

0x12523024+ 64*n USB3_HS_BAM_P_DATA_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Beginning of the Data Address space.

This register is non relevant in System Modes.

USB3_HS_BAM_P_DATA_FIFO_ADDRn

Bits	Name	Description
31:0	P_DATA_FIFO_ADDR	Data Address Space beginning.

0x1252301C+ 64*n USB3_HS_BAM_P_DESC_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Address of the Descriptor Fifo beginning.

NOTE This register is used by all modes.

USB3_HS_BAM_P_DESC_FIFO_ADDRn

Bits	Name	Description
31:0	P_DESC_FIFO_ADDR	Address of the Descriptors Fifo. This address must be 8 bytes aligned.

0x12523028+64*n USB3_HS_BAM_P_EVNT_GEN_TRSHLDn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register configures the threshold value for Read/Write event generation by the BAM towards another BAM. When aBAM pushes/pops this number of bytes to/from the pipe an event to the other BAM will be generated. A counter summing up the bytes pushed/popped is reset when event is issued, thus restarting count for the threshold.

Events are also issued after End Of Transfer received from the peripheral (Producer case), non regarding whether the pushed bytes count has reached the threshold or not.

This register is non relevant in System Modes.

USB3_HS_BAM_P_EVNT_GEN_TRSHLDn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TRSHLD	Threshold value. The maximum allowed value is 32kByte.

0x12523020+64*n USB3_HS_BAM_P_FIFO_SIZESn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

The least significant field is the Descriptor Fifo Size.

The most significant field is the Data Fifo Size.

NOTE This Descriptor Fifo Size is used by all modes. The Data Fifo Size is non relevant in System Modes.

USB3_HS_BAM_P_FIFO_SIZESn

Bits	Name	Description
31:16	P_DATA_FIFO_SIZE	Size of the Data Address Space.
15:0	P_DESC_FIFO_SIZE	Size of the Descriptors Fifo. Must be 8 byte aligned. Each descriptor is 8 bytes. Size of the descriptor fifo must contain an integer number of Descriptors.

20.32.4 BAM PIPE internal state registers (RAM)

BAM Pipe debug registers allow a software look inside on the internal parameters of the BAM State Machines stored in RAM.

Those shouldn't be normally used or altered by the software.

0x12523034+64*n USB3_HS_BAM_P_RETR_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context stored for retransmission.

This is being stored by Ack Update state machine in consumer mode or by the Writeback state machine in producer mode.

This is being loaded by the Writeback state machine when retransmission happens.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB3_HS_BAM_P_RETR_CNTXT_n

Bits	Name	Description
31:16	RETR_DESC_OFST	Descriptor Fifo Offset for retransmission.
15:0	RETR_OFST_IN_DESC	The Offset inside the Descriptor for retransmission.

0x12523038+64*n USB3_HS_BAM_P_SI_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Sideband Inform state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB3_HS_BAM_P_SI_CNTXT_n

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	SI_DESC_OFST	The Descriptor Fifo Offset pointer stored by the Sideband Inform state machine.

0x12523004+ 64*n USB3_HS_BAM_P_AU_PSM_CNTXT_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Ack Update state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB3_HS_BAM_P_AU_PSM_CNTXT_1_n

Bits	Name	Description
31:16	AU_PSM_ACCUMED	PSM: The acknowledged (EOB/T) number of bytes since last Write Event. AU: The accumulation of the descriptor sizes for the present ack_on_success event. This is never bigger than the ACKED field. Once the ACCUMED values are bigger than Event Threshold, an Event will be issued, the ACKED value will decrease by the ACCUMED size and this value will be zeroed. This also serves as the Bytes Consumed value in the Event.
15:0	AU_ACKED	AU: The left over of the number of bytes that were received via the ack_on_success, that did not cause a descriptor closure. This value is down counting upon issuing Read Event. PSM:

0x12523008+ 64*n USB3_HS_BAM_P_PSM_CNTXT_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB3_HS_BAM_P_PSM_CNTXT_2_n

Bits	Name	Description
31	PSM_DESC_VALID	The Descriptor Valid bit provided by the Writeback state machine to Pipe state machine.
30	PSM_DESC_IRQ	The Descriptor Interrupt bit provided by the Writeback state machine to pipe state machine.
29	PSM_DESC_IRQ_DONE	The Descriptor Interrupt needed selection bit.
28:25	PSM_GENERAL_BITS	General Context Switch Bits
24:22	PSM_CONS_STATE	State of the Pipe Consumer state machine.
21:19	PSM_PROD_SYS_STATE	State of the Pipe Producer System state machine.
18:16	PSM_PROD_B2B_STATE	State of the Pipe Producer BAM to BAM state machine.
15:0	PSM_DESC_SIZE	The Descriptor Size provided by the Writeback state machine to pipe state machine.

0x1252300C+64*n USB3_HS_BAM_P_PSM_CNTXT_3_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB3_HS_BAM_P_PSM_CNTXT_3_n

Bits	Name	Description
31:0	PSM_DESC_ADDR	The Data Address provided in the current descriptor from the Writeback state machine.

0x12523010+64*n USB3_HS_BAM_P_PSM_CNTXT_4_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB3_HS_BAM_P_PSM_CNTXT_4_n

Bits	Name	Description
31:16	PSM_DESC_OFST	The running Descriptor Fifo Offset of the Writeback state machine
15:0	PSM_SAVED_ACCUMED_SIZE	The Saved Accumulated Size from the Pipe state machine.

0x12523014+64*n USB3_HS_BAM_P_PSM_CNTXT_5_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB3_HS_BAM_P_PSM_CNTXT_5_n

Bits	Name	Description
31:16	PSM_BLOCK_BYTE_CNT	The Byte count inside the current Block.
15:0	PSM_OFST_IN_DESC	The Offset inside a register. This is used by pipe state machine to compute offset inside a register after retransmission

0x12523030+64*n USB3_HS_BAM_P_RESERVED_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

USB3_HS_BAM_P_RESERVED_1_n

Bits	Name	Description
31:0	BAM_P_RES_1	Set to zero (0) Reserved

0x1252303C+64*n USB3_HS_BAM_P_RESERVED_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

USB3_HS_BAM_P_RESERVED_2_n

Bits	Name	Description
31:0	BAM_P_RES_2	Set to zero (0) Obsolete Register: BAM_P_IRQ_DEST_ADDRn, n=[0..30]

20.33 USB4 OTG HS Registers (0x12530000 USB4_HS_BASE)

This section contains USB4 OTG HS registers.

20.33.1 Identification registers

Identification registers are used to declare the slave interface presence and include a table of the hardware configuration parameters.

0x12530000 USB4_HS_USB_OTG_HS_ID

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0042FA05

The USB_OTG_HS_ID register is the identification register. It provides a simple way to determine if the USB-HS USB 2.0 core is provided in the system. The ID register identifies the USB-HS USB 2.0 core and its revision.

USB4_HS_USB_OTG_HS_ID

Bits	Name	Description
31:24	RESERVED_BITS31_24	These bits are reserved and should be set to zero.
23:16	REVISON_7_0	This field contains the revision number of the core - 0x42.
15:8	NID_5_0	This field contains the complement version of ID[7:0] - 0xFA.
7:0	ID_5_0	This field is the configuration number. This number is set to 0x05 and indicates that the peripheral is the USB-HS USB 2.0 core.

0x12530004 USB4_HS_USB_OTG_HS_HWGENERAL

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x5C2

The USB_OTG_HS_HWGENERAL register contains the general hardware parameters.

USB4_HS_USB_OTG_HS_HWGENERAL

Bits	Name	Description
31:10	RESERVED_BITS31_10	Clear (0) these bits.
9	SM	VUSB_HS_PHY_SERIAL = 2
8:6	PHYM	VUSB_HS_PHY_TYPE = 7
5:4	PHYW	VUSB_HS_PHY16_8 = 0

USB4_HS_USB_OTG_HS_HWGENERAL (cont.)

Bits	Name	Description
3	BWT	This bit is reserved for internal testing = 0
2:1	CLCK	VUSB_HS_CLOCK_CONFIGURATION = 1
0	RT	VUSB_HS_RESET_TYPE = 0

0x12530008 USB4_HS_USB_OTG_HS_HWHOST

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x10020001

The USB_OTG_HS_HWHOST register contains the host hardware parameters.

USB4_HS_USB_OTG_HS_HWHOST

Bits	Name	Description
31:24	TTPER	VUSB_HS_TT_PERIODIC_CONTEXTS
23:16	TTASY	VUSB_HS_TT_ASYNC_CONTEXTS
15:4	RESERVED_BITS15_4	Clear (0) these bits.
3:1	NPORT	VUSB_HS_NUM_PORT-1
0	HC	VUSB_HS_HOST

0x1253000C USB4_HS_USB_OTG_HS_HWDEVICE

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000021

The USB_OTG_HS_HWDEVICE register contains the device hardware parameters.

USB4_HS_USB_OTG_HS_HWDEVICE

Bits	Name	Description
31:6	RESERVED_BITS31_6	
5:1	DEVEP	VUSB_HS_DEV_EP
0	DC	Device capable; [VUSB_HS_DEV/=0]

0x12530010 USB4_HS_USB_OTG_HS_HWTXBUF

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x80070B08

The USB_OTG_HS_HWTXBUF register contains the Tx buffer hardware parameters.

USB4_HS_USB_OTG_HS_HWTXBUF

Bits	Name	Description
31	TXLCR	This bit is fixed to 1'b1 so that the local context register's are included in the design. This means that the DMA context is implemented in FlipFlops.
30:24	RESERVED_BITS30_24	Clear (0) these bits.
23:16	TXCHANADD	VUSB_HS_TX_CHAN_ADD - Defines the number of address lines needed per Endpoint per the TX latency buffer. It's reset value is taken from a GENERIC value passed to the core.
15:8	TXADD	VUSB_HS_TX_ADD - Defines the number of address lines needed per the entire TX latency buffer. It's reset value is taken from a GENERIC value passed to the core.
7:0	TXBURST	VUSB_HS_TX_BURST - Defines the data burst length of the AHB master interface in Quad-words (4-byte increments) of the TX data. It's reset value is taken from a GENERIC value passed to the core. Note that the actual burst lengthis will depend on the settings of USB_OTG_HS_AHB_MODE and USB_OTG_HS_AHB_BURST registers.

0x12530014 USB4_HS_USB_OTG_HS_HWRXBUF

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000808

The USB_OTG_HS_HWRXBUF register contains the Rx buffer hardware parameters.

USB4_HS_USB_OTG_HS_HWRXBUF

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits).
15:8	RX_ADD	VUSB_HS_RX_ADD - Defines the number of address lines needed per the entire RX latency buffer. It's reset value is taken from a GENERIC value passed to the core.

USB4_HS_USB_OTG_HS_HWRXBUF (cont.)

Bits	Name	Description
7:0	RX_BURST	VUSB_HS_RX_BURST - Defines the data burst length of the AHB master interface in Quad-words (4-byte increments) of the RX data. It's reset value is taken from a GENERIC value passed to the core. Note that the actual burst length will depend on the settings of USB_OTG_HS_AHB_MODE and USB_OTG_HS_AHB_BURST registers.

0x12530040+ 4*n USB4_HS_USB_OTG_HS_SCRATCH_RAMn, n=[0..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

USB_OTG_HS_SCRATCH_RAMn registers are 16 32bit scratch registers.Required for passing USB software information between different images.

USB4_HS_USB_OTG_HS_SCRATCH_RAMn

Bits	Name	Description
31:0	SCRATCH_REGISTER	32 bit scratch register

20.33.2 Device/host timer registers

The host/device controller drivers can measure time related activities using these timer registers.

NOTE These registers are not part of the standard EHCI controller.

0x12530080 USB4_HS_USB_OTG_HS_GPTIMER0LD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER0LD register is the general purpose timer 0 load register. This register contains the timer duration or load value. See the GPTIMER0CTRL register for a description of the timer functions.

USB4_HS_USB_OTG_HS_GPTIMER0LD

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.

USB4_HS_USB_OTG_HS_GPTIMER0LD (cont.)

Bits	Name	Description
23:0	GPTLD	General purpose timer load value. This field is the value to be loaded into the GPTCNT countdown timer on a reset action. This value in this register represents the time in microseconds minus 1 for the timer duration. Example: for a one millisecond timer, load 1000-1=999 or 0x0003E7. Note: Max value is 0xFFFFFF or 16.777215 seconds

0x12530084 USB4_HS_USB_OTG_HS_GPTIMER0CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER0CTRL register is the general purpose timer 0 control register. This register contains the control for the timer and a data field can be queried to determine the running count value. This timer has a granularity of 1 ms and can be programmed to a little over 16 seconds. There are two modes supported by this timer: the first is a one-shot and the second is a looped count, which is described in the register table below. When the timer counter value transitions to zero, an interrupt can be generated though the use of the timer interrupts in the USBTS and USBINTR registers.

USB4_HS_USB_OTG_HS_GPTIMER0CTRL

Bits	Name	Description
31	GTPRUN	General purpose timer run Read/write value 0 = Timer stop value 1 = Timer run This bit enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.
30	GPTRST	General purpose timer reset Write-only value 0 = No action value 1 = Load counter value Writing a one to this bit will reload the GPTCNT with the value in GPTLD.
29:25	RESERVED_BITS29_25	Clear (0) these bits.

USB4_HS_USB_OTG_HS_GPTIMER0CTRL (cont.)

Bits	Name	Description
24	GPTMODE	General purpose timer mode Read/write value 0 = One shot value 1 = Repeat This bit selects between a single timer countdown and a looped count down. In the one-shot mode, the timer will count down to zero, generate an interrupt, and stop until the counter is reset by the software. In the repeat mode, the timer will count down to zero, generate an interrupt, and automatically reload the counter to begin again.
23:0	GPTCNT	General purpose timer counter Read-only This field is the value of the running timer.

0x12530088 USB4_HS_USB_OTG_HS_GPTIMER1LD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER1LD register is the general purpose timer 1 control register. This register contains the timer duration or load value. See the GPTIMER0LDregister for a description of the timer functions.

USB4_HS_USB_OTG_HS_GPTIMER1LD

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.
23:0	GPTLD	General purpose timer load value. This field is the value to be loaded into the GPTCNT countdown timer on a reset action. This value in this register represents the time in microseconds minus 1 for the timer duration. Example: for a one millisecond timer, load 1000-1=999 or 0x0003E7. Note: Max value is 0xFFFFFF or 16.777215 seconds.

0x1253008C USB4_HS_USB_OTG_HS_GPTIMER1CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_GPTIMER1CTRL register is the general purpose timer 1 control register. See the description of the USB_OTG_HS_GPTIMER0CTRL register for details about this register.

USB4_HS_USB_OTG_HS_GPTIMER1CTRL

Bits	Name	Description
31	GTPRUN	General purpose timer run Read/write value 0 = Timer stop value 1 = Timer run This bit enables the general-purpose timer to run. Setting or clearing this bit will not have an effect on the GPTCNT.
30	GPTRST	General purpose timer reset Write-only value 0 = No action value 1 = Load counter value Writing a one to this bit will reload the GPTCNT with the value in GPTLD.
29:25	RESERVED_BITS29_25	Clear (0) these bits.
24	GPTMODE	General purpose timer mode Read/write value 0 = One shot value 1 = Repeat This bit selects between a single timer countdown and a looped count down. In the one-shot mode, the timer will count down to zero, generate an interrupt, and stop until the counter is reset by the software. In the repeat mode, the timer will count down to zero, generate an interrupt, and automatically reload the counter to begin again.
23:0	GPTCNT	General purpose timer counter Read-only This field is the value of the running timer.

20.33.3 Wrapper operational registers

0x12530090 USB4_HS_USB_OTG_HS_AHB_BURST

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_AHB_BURST register determines the AHB master mode of the USB HS Core.

NOTE If the USB_OTG_HS_AHB_MODE is configured to be 0x0 (the AHB Transactor is used), this register must be 0x0 as well, otherwise the AHB Master bus behavior is undefined. Use values other than 0x0 only if setting USB_OTG_HS_AHB_MODE to 0x1.

USB4_HS_USB_OTG_HS_AHB_BURST

Bits	Name	Description
31:3	RESERVED_BITS31_3	Should be set to zero.
2:0	AHB_BURST	AMBA AHB BURST. This is a r/w field that selects the following options for the m_hburst signal of the AMBA master interface: In all cases where the unspecified length burst is allowed, singles access may also occur, this is mostly true when the transaction is not 32-bit aligned. Two consecutive single accesses should not happen. When a INCRx burst size is selected and the transfer is not multiple of the INCRx burst, the burst is decomposed in the different ways. With AHBBRST[2] = 1, the smaller bursts will be unspecified length. with AHBBRST[2] = 0, the smaller bursts will be smaller INCRx or singles. For example, lets say that it's required at a given time, to transfer 22 words of information, for the following values of AHBBRST the master sequence will be: This field after reset is set to a default value that can be configured in the file vusb_hs_cfg.vhd. The AHBBRST field is only used if the AMBA-AHB system interface has been selected. It has no effect for cores featuring BVCI interface. In the later case the read will return zeros. When this field is different from zero, the value of the fields TXBURST /RXBURST in register BURSTSIZE 160h, will be ignored by the controller. Internally the BURSTSIZE will be set to the value of the INCRx AMBA burst. Since this has a direct relation with the burst sizes you must be careful with AHB burst selected. Although the TXBURST / RXBURST are bypassed, this register can still be written / read with no effect, while the AHBBRST field is non-zero. 0x0: INCR burst of unspecified length 0x1: INCR4, non-multiple transfers of INCR4 will be decomposed into singles 0x2: INCR8, non-multiple transfers of INCR8, will be decomposed into INCR4 or singles 0x3: INCR16, non-multiple transfers of INCR16, will be decomposed into INCR8, INCR4 or singles 0x4: This value is reserved and should not be used 0x5: INCR4, non-multiple transfers of INCR4 will be decomposed into smaller unspecified length bursts 0x6: INCR8, non-multiple transfers of INCR8 will be decomposed into smaller unspecified length bursts 0x7: INCR16, non-multiple transfers of INCR16 will be decomposed into smaller unspecified length bursts 0x5: INCR4+ INCR4 +INCR4+ INCR4 +INCR4+ INCR unspec. length 0x6: INCR8+INCR8+INCR4+ INCR unspec. length 0x7: INCR16+INCR4+ INCR unspec. length 0x1: INCR4+ INCR4 +INCR4+ INCR4 +INCR4+SINGLE+SINGLE 0x2: INCR8+INCR8+INCR4+SINGLE+SINGLE 0x3: INCR16+INCR4+SINGLE+SINGLE

0x12530094 USB4_HS_USB_OTG_HS_XTOR_STS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_XTOR_STS register is currently a placeholder for future status bits from the AHB2AHB Transactor.

USB4_HS_USB_OTG_HS_XTOR_STS

Bits	Name	Description
31:2	RESERVED_BITS31_2	Not used currently.
1	GRANT_STOLEN	Reports whether the arbiter removed the hgrant signal prior to completing a transaction. This is currently supported in WRITES ONLY. This bit can be cleared by writing a ’1’ to the GRANT_STOLEN_CLEAR bit in the USB_OTG_HS_AHB_MODE register. To enable this bit again, write a ’0’ to he GRANT_STOLEN_CLEAR bit in the USB_OTG_HS_AHB_MODE register.
0	RESERVED_BIT0	Not used currently.

0x12530098 USB4_HS_USB_OTG_HS_AHB_MODE

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1

USB4_HS_USB_OTG_HS_AHB_MODE

Bits	Name	Description
31	ASYNC_BRIDGES_BYPASS	Default is ’0’. When ’0’ the asynchronous bridge on the master AHB interface is used. When ’1’, it is bypassed. The bridge on the slave AHB is always used.
30:5	RESERVED_BITS30_5	Not used currently.
4	INCR_OVERRIDE	Valid only if the Transactor is bypassed: When ’1’, all INCR bursts from the USB Core will be internally transformed into SINGLE transfers. When ’0’, if the USB Core issues an INCR burst, it will propagate to the external master AHB port.

USB4_HS_USB_OTG_HS_AHB_MODE (cont.)

Bits	Name	Description
3:2	HPROT_MODE	When ’00’ the HPROT signal out of the USB Wrapper is ’0001’, and all transactions are non-posted. When ’01’ the HPROT signal out of the USB Wrapper is ’0101’, and all transactions are posted. When ’10’ the HPROT signal out of the USB Wrapper alternates according to the context of the AHB bus access. Control structures are non-posted while data transfer is posted. When ’11’, reserved value, but currently maps to non-posted (same as ’00’).
1	GRANT_STOLEN_CLEAR	Clears the grant stolen field of the USB_OTG_HS_XTOR_STS register. To enable this bit again, write ’0’ after clearing the GRANT_STOLEN (’1’).
0	XTOR_BYPASS	When this bit is set (1), the AHB Transactor is bypassed, and the USB HS Core’s AHB Master interface is directly connected to the AHB system. In this case, the USB_OTG_HS_AHB_BURST register value will determine the bus characteristics. When this bit is reset (0), the AHB Transactor is used to connect the USB HS Core to the AHB system.

0x1253009C USB4_HS_USB_OTG_HS_GEN_CONFIG

Type: Read/write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXX0830

The USB_OTG_HS_GEN_CONFIG register is used to configure various features that have been added to the HS USB Core.

USB4_HS_USB_OTG_HS_GEN_CONFIG

Bits	Name	Description
31:16	USB_OTG_HS_HW_QVERSION	HW revision of the USB OTG HS core. This version changes with every official release of USB_OTG_HS core.
15	SYS_CLK_SW_EN	This bit is applicable only in SPS Device mode. When this bit is set then USB core always voting for USB_SYSTEM_CLK. Default value is 0 - USB core doesn’t request USB_SYSTEM_CLK when in Low Power Mode.
14	TESTMUX_SEL_4	see TESTMUX_SEL_3_0 the first 4 bits of this register.
13	USB_BAM_DISABLE	This bit disables the bam logic inside the USB and makes him work in Legacy mode.
12	DMA_HPROT_CTRL	When this bit is set Link Controller always does non-posted dQH writes.
11	ISO_FIX_EN	This bit enables fix for Isochronous bug in CI core (CR--0000135251).

USB4_HS_USB_OTG_HS_GEN_CONFIG (cont.)

Bits	Name	Description
10	DSC_PE_RST_EN	This bit enables an automatic reset of Device PE State Machine on disconnection event when operating as device. This reset is a HW fix for CR-000940.
9	HOST_SIM_TIMERS_EN_SUSP	When this bit is set (1), the timers used for the USB suspend process short for faster simulation and ATE time. When this bit is clear(0), the timers used for the USB suspend process are according to the USB specification.
8	HOST_SIM_TIMERS_EN_STD	When this bit is set (1), the timers used for the USB reset on the ULPI are short for faster simulation and ATE time. When this bit is clear(0), the timers used for the USB reset on the ULPI are according to the USB specification.
7	PE_RX_BUF_PENDING_EN	This is only valid in Device Mode. Setting this bit will cause to store a Transaction Status Tag in the Pending register instead of RX Buffer if the RX Buffer is full. The Tag will move from Pending register to RX Buffer as soon as it becomes not full.
6	STREAM_RX_BYPASS_ENABLE	This is only valid in Device Mode. If SDIS bit is set (bit 4 of USB_OTG_HS_USBMODE (0x1A8)), i.e., streaming mode is disabled, setting this bit will cause the RX traffic to override the SDIS bit, and to receive in streaming mode. TX will still be in non-streaming mode.
5	ULPI_SERIAL_EN	This bit must be set to enable operation of ULPI Serial FS/LS mode. Default state is ’1’ - ULPI Serial mode is supported.
4	PE_DP_TXFIFO_IDLE_FORCE	This is only valid in Device Mode. Setting this bit to ’1’ forces the dp_tx_fifo_cmd_dev to be equal to PE_DP_TXFIFO_IDLE when Device PE state machine in REPORT_NAK state and the RX Buffer is full. This bit is used to enable fix of CR-001612. Reset value is ’1’.

USB4_HS_USB_OTG_HS_GEN_CONFIG (cont.)

Bits	Name	Description
3:0	TESTMUX_SEL_3_0	With TESTMUX_SEL_4 select one of the following test buses: Value 00001 Key state machines 01101 hsic_test_bus1 01110 hsic_test_bus2 10000 dma_eng_3 dma_dev_sm_2 10001 dma_eng_4 dma_traf others zeros 0x2: dma_eng_0 dma_dev_sm_1 0x3: dma_eng_1 dma_context 0x4: dma_eng_2 dma_mem_arb 0x5: prot_eng_0 0x6: prot_eng_1 0x7: prot_eng_2 0x8: port_ctrl_0 0x9: port_ctrl_1 0xA: tx_buffer 0xB: rx_buffer 0xC: otg

0x125300A0 USB4_HS_USB_OTG_HS_GEN_CONFIG_2

Type: Read/write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0001F60

Register for the chicken bits. The USB_OTG_HS_GEN_CONFIG_2 register is used to configure various features that have been added to the HS USB Core. By default, all chicken bits are off and the fix is applicable.

USB4_HS_USB_OTG_HS_GEN_CONFIG_2

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12	LINESTATE_DIFF_WAKEUP_EN	chicken bit for CR-0000155486.when this bit is set the USB enables the HW fix for Race condition between the attempt to enter LPM and USB bus reset.Default value is 1.
11	ULPI_LPM_PEND_EN	chicken bit for CR-0000153486.when this bit is set the USB enables the HW fix for Function Control and LPM race condition.Default value is 1.
10	RX_FULL_NAK_EN	chicken bit for CR-0000152878.when this bit is set the USB will respond with NAK's for Host Tokens with very slow AHB and when Streaming mode is enabled. Default value is 1.

USB4_HS_USB_OTG_HS_GEN_CONFIG_2 (cont.)

Bits	Name	Description
9	ENDLESS_TD_EN	chicken bit for CR-0000152976. When this bit is set Performance enhancements for 'infinite' Producer pipe (out endpoint with eTD that points to itself) are enabled. Default value is 1.
8	SCRATCH_RAM_EN	chicken bit for CR-0000149922. When this bit is set the use of scratch ram is enabled and the SW can read/write from addresses 0x040 - 0x07c. when this bit is clear SW can no longer access those registers. Default value is 1.
7	SESS_VLD_CTRL_EN	When this bit is set then bit 25 of USBCMD register controls sess_vld signal inside the Link Controller. When this bit is clear then Link Controller receives sess_vld directly from PHY. Default value is 0.
6	CI_T_WTSUSRSTHS_EN	When this bit is 0 then Device Port Control State Machine waits 2.5 us from USB Reset detection until starting driving Chirp K. When this bit is 1 then Device Port Control State Machine waits 1.5 ms from USB Reset detection until starting driving Chirp K. Default value is 1 - legacy behavior.
5	CI_T_UCH_EN	When this bit is 0 then Device Port Control State Machine drives Chirp K for 1 ms. When this bit is 1 then Device Port Control State Machine drives Chirp K for 2ms. Default value is 1 - legacy behavior.
4	DP_RESET	chicken bit for fix CI2687: When the OTG core is acting as a Host, and VBUS is turned off, and the attached Device attempts to perform a Session Request Protocol by using Data-line Pulsing, it will not be recognized by the Host. Also, when doing HNP and becoming a Host, a SE0 is forced in the line causing the OPT TD5.4 test to fail, without the software workaround.
3	ZLP_PRIME	chicken bit for fix CI2655: When using ISO IN endpoints with MULT=3 and low bandwidth system bus access, the controller may enter into a wait loop situation without warning the software. Due to the low bandwidth the last packet from a mult3 sequence may not be fetched in time before the last token IN is received (for that uframe/endpoint). This will cause the controller to reply with a zero length packet (ZLP), breaking the prime sequence.
2	NO_SOF_RX_FIFO_FULL	chicken bit for fix CI2581: During normal operation, if the RX Fifo becomes full and the protocol engine needs to send a command to the DMA state machine, it will wait in that state until the RX Fifo becomes not full. As the protocol state machine also handles the SOF generation, the SOFs will no longer be sent. If one SOF is missed, the Host controller will issue a false babble detection. If more than 3.125ms are elapsed without SOFs the peripheral will recognize the idle bus as a USB reset.
1	WRONG_OPMODE_SUSP	chicken bit for fix CI1274: When the Controller enters a Suspend state it asserts opmode with the wrong value, according to specifications 'UTMI+ Specification, Revision 1.0, Section 3.2' and 'UTMI+ Low Pin Interface Specification, Revision 1.1, Section 3.8.5.3'. This causes no issue in actual usage.

USB4_HS_USB_OTG_HS_GEN_CONFIG_2 (cont.)

Bits	Name	Description
0	RESUME_END_INTER	chicken bit for fix CI1179: Working as host, when doing resume a port change interrupt was fired at the end of resume. According to the EHCI spec no interrupt should be fired.

20.33.4 Device/host capability registers

0x12530100 USB4_HS_USB_OTG_HS_CAPLENGTH

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x01000040

The USB_OTG_HS_CAPLENGTH register is the capability register length. It is used to indicate which offset to add to the register base address at the beginning of the operational register.

USB4_HS_USB_OTG_HS_CAPLENGTH

Bits	Name	Description
31:16	HCIVERSION_15_0	BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.
7:0	CAPLENGTH_7_0	Offset at beginning of operational register

0x12530104 USB4_HS_USB_OTG_HS_HCSPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00010011

The USB_OTG_HS_HCSPARAMS register contains the host control structural parameters. The port steering logic capabilities are described in this register.

USB4_HS_USB_OTG_HS_HCSPARAMS

Bits	Name	Description
31:28	RESERVED_BITS31_28	Clear (0) these bits.
27:24	N_TT_3_0	Number of transaction translators This field indicates the number of embedded transaction translators associated with the USB2.0 host controller. For a multi-port host, this field will always equal 0001. For all other implementations, N_TT = 0000. This in a non-EHCI field to support embedded TT.

USB4_HS_USB_OTG_HS_HCSPARAMS (cont.)

Bits	Name	Description
23:20	N_PTT_3_0	Number of ports per transaction translator This field indicates the number of ports assigned to each transaction translator within the USB2.0 host controller. For a multi-port host this field will always equal N_PORTS. For all other implementations, N_PTT = 0000. This in a non-EHCI field to support embedded TT.
19:17	RESERVED_BITS19_17	Clear (0) these bits.
16	PI_3_0	Port indicator This bit indicates whether the ports support port indicator control. When set (1), the port status and control registers include a read/writable field for controlling the state of the port indicator. This field will always be set (1).
15:12	N_CC_3_0	Number of companion controllers This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no internal companion controllers. Port-ownership hand-off is not supported. A value larger than zero in this field indicates that there are companion USB1.1 host controller(s). Port-ownership hand-offs are supported. High-, full-, and low-speed devices are supported on the host controller root ports. In this implementation, this field will always be clear (0).
11:8	N_PCC_3_0	Number of ports per companion controller This field indicates the number of ports supported per internal companion controller. It is used to indicate the port routing configuration to the system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2, then N_PCC could have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, and so on. In the previous example, the N_PCC could have been 4, where the first 4 are routed to companion controller 1 and the last two are routed to companion controller 2. The number in this field must be consistent with N_PORTS and N_CC. In this implementation, this field will always be clear (0).
7:5	RESERVED_BITS7_5	Clear (0) these bits.
4	PPC	Port power control This field indicates whether the host controller implementation includes port power control. Set (1) indicates that the ports have port power switches. Clear (0) indicates that the ports do not have port power switches. The value of this field affects the functionality of the port power field in each port status and control register. This bit will always be clear (0) for a device only implementation.

USB4_HS_USB_OTG_HS_HCSPARAMS (cont.)

Bits	Name	Description
3:0	N_PORTS_3_0	Number of downstream ports This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the operational register. Valid values are in the range of 1h to Fh. A zero in this field is undefined. The number of ports for a host implementation is configurable from 1 to 8. This field will always be set (1) for device-only implementation.

0x12530108 USB4_HS_USB_OTG_HS_HCCPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0006

The USB_OTG_HS_HCCPARAMS register contains the host control capability parameters. This register identifies multiple mode control (time-base bit functionality) addressing capability.

USB4_HS_USB_OTG_HS_HCCPARAMS

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.
15:8	EECP_7_0	EHCI extended capabilities pointer Default = 0 This optional field indicates the existence of a capabilities list. A value of 00h indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capability. The pointer value must be 40h or greater if implemented to maintain the consistency of the PCI header defined for this class of device. For this implementation, all of these bits are clear (0).
7:4	IST_7_4	Isochronous scheduling threshold Default = implementation dependent This field indicates, relative to the current position of the executing host controller, where the software can reliably update the isochronous schedule. When bit [7] is clear (0), the value of the least significant 3 bits indicates the number of microframes a host controller can hold a set of isochronous data structures (one or more) before flushing the state. When bit [7] is set (1), then host software assumes the host controller may cache an isochronous data structure for an entire frame. All of the bits in this field will always be clear (0).
3	RESERVED_BIT3	Clear (0) this bit.

USB4_HS_USB_OTG_HS_HCCPARAMS (cont.)

Bits	Name	Description
2	ASP	Asynchronous schedule park capability Default = 1 If this bit is set (1), then the host controller supports the park feature for high-speed queue heads in the asynchronous schedule. The feature can be disabled, or enabled and set to a specific level by using the (ASPE) and (ASP[1:0]) fields in the USB_OTG_HS_USBCMD register. This field will always be set (1).
1	PFL	Programmable frame list flag If this bit is clear (0), then the system software must use a frame list length of 1024 elements with this host controller. The FS[2:0] field in the USBCMD register is read-only and must be cleared (0). If this bit is set (1), then the system software can specify and use a smaller frame list, and configure the host controller using the FS[2:0] field in the USBCMD register. The frame list must always be aligned on a 4k-page boundary. This requirement ensures that the frame list is always physically contiguous. This bit in this field will always be set (1).
0	ADC	64-bit addressing capability This field will always be clear (0). No 64-bit addressing capability is supported.

0x12530120 USB4_HS_USB_OTG_HS_DCIVERSION

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1

The USB_OTG_HS_DCIVERSION register contains the device interface version number. The device controller interface conforms to the two-byte BCD encoding of the interface version number contained in this register.

USB4_HS_USB_OTG_HS_DCIVERSION

Bits	Name	Description
15:0	DCIVERSION_15_0	Device interface version number

0x12530124 USB4_HS_USB_OTG_HS_DCCPARAMS

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x190

The USB_OTG_HS_DCCPARAMS register contains the device control capability parameters. These fields describe the overall host/device capability of the controller.

USB4_HS_USB_OTG_HS_DCCPARAMS

Bits	Name	Description
31:9	RESERVED_BITS31_9	Clear (0) these bits.
8	HC	Host capable When this bit is set (1), this controller is capable of operating as an EHCI-compatible USB 2.0 host controller.
7	DC	Device capable When this bit is set (1), this controller is capable of operating as a USB 2.0 device.
6:5	RESERVED_BITS6_5	Clear (0) these bits.
4:0	DEN_4_0	Device endpoint number This field indicates the number of endpoints build into the device controller. If this controller is not device capable, then this field will be al zeroes. Valid values for this field are 0 through 16.

20.33.5 Device/host operational registers

0x12530140 USB4_HS_USB_OTG_HS_USBCMD

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00080000

The USB_OTG_HS_USBCMD register is the USB command register. The serial bus host/device controller executes the command indicated in this register.

USB4_HS_USB_OTG_HS_USBCMD

Bits	Name	Description
31	RST_CTRL	Default value = 0. Set to 1 to block operational reset to xcvr (ser and ulpi) clock domains.
30	ULPI_STP_CTRL	Default value = 0. Set to 1 to block the ulpi_stp signal from going out to ULPI PHY
29	ASYNC_INTR_CTRL	Default value = 0. Set to 1 to allow the async interrupt out from the HS core.
28	SE0_GLITCH_FIX_CTRL	Default value = 0. Set to 1 to activate the SE0 glitch fix mechanism
27	FS_3_WIRE_2_WIRE_SELECT	Default value = 0. Set this bit for enabling the two wire interface on the fs_dat and fs_se0 pins

USB4_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
26	ULPI_SER3_NOT6_SEL	ULPI serial 3 bits select. Read/write Read: Current status of serial data bus wide Write: SW writes ’1’ to this bit to request 3 pins ULPI data wide, or ’0’ to request 6 bit data wide in FsLsSerial Mode.
25	SESS_VLD_CTRL	Default value = 0. Set this bit to enable Link Controller operation after switching interface from Serial to ULPI.
24	RESERVED_BIT24	Clear (0) these bit
23:16	ITC_7_0	Interrupt threshold control Read/write Default 08h The system software uses this field to set the maximum rate at which the host/device controller will issue interrupts. This field contains the maximum interrupt interval measured in micro-frames. Valid values are shown below. Value Maximum interrupt interval 00h Immediate (no threshold) 01h 1 micro-frame 02h 2 micro-frames 04h 4 micro-frames 08h 8 micro-frames 10h 16 micro-frames 20h 32 micro-frames 40h 64 micro-frames
15	FS2	This field is Read/Write only if Programmable Frame List Flag in the HCCPARAMS registers is set to one. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index. Note that this field is made up from USBCMD bits 15, 3 and 2. Values meaning 000 1024 elements (4096 bytes) Default value 001 512 elements (2048 bytes) 010 256 elements (1024 bytes) 011 128 elements (512 bytes) 100 64 elements (256 bytes) 101 32 elements (128 bytes) 110 16 elements (64 bytes) 111 8 elements (32 bytes) Only the host controller uses this field.

USB4_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
14	ATDTW	Add dTD tripwire Read/write (Device mode only) This bit is used as a semaphore to ensure the to proper addition of a new dTD to an active (primed) endpoint's linked list. This bit is set (1) and cleared (0) by the software. This bit shall also be cleared (0) by the hardware when the state machine is a hazard region for which adding a dTD to a primed endpoint may go unrecognized.
13	SUTW	Setup tripwire (device mode only) Read/write This bit is used as a semaphore to ensure that the setup data payload of 8 bytes is extracted from a QH by the DCD without being corrupted. If the setup lockout mode is off (see USBMODE) then there exists a hazard when new setup data arrives while the DCD is copying the setup data payload from the QH for a previous setup packet. This bit is set (1) and cleared (0) by software, and will be cleared (0) by hardware when a hazard exists.
12	RESERVED_BITS12	Clear (0) this bit
11	ASPE	Asynchronous schedule park mode enable (OPTIONAL) Read/write If the asynchronous park capability (ASP) bit in the HCCPARAMS register is set (1), then this bit defaults to a 1h and is R/W. Otherwise, the bit must be cleared (0) and is RO. The software uses this bit to enable or disable the park mode. value 1 = Park mode is enabled. value 0 = Park mode is disabled. This field is set (1) in this implementation.
10	RESERVED_BIT10	Clear (0) this bit.
9:8	ASP_1_0	Asynchronous schedule park mode count (OPTIONAL) Read/write If the Asynchronous park capability (ASP) bit in the HCCPARAMS register is set (1), then this field defaults to 3h and is R/W. Otherwise it defaults to zero and is RO. This field contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule before continuing traversal of the Asynchronous schedule. See Section 4.10.3.2 for full operational details. Valid values are 1h to 3h. The software must not clear (0) this bit when the ASPE bit in this register is set (1), as this will result in undefined behavior. This field is set to 3h in this implementation.
7	LR	Light host/device controller reset (OPTIONAL) Read only Not implemented. This bit will always be clear (0).

USB4_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
6	IAA	Interrupt on async advance doorbell Read/write This bit is used as a doorbell by the software to tell the host controller to issue an interrupt the next time it advances the asynchronous schedule. The software must set (1) this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule states, it sets (1) the interrupt on the async advance status (AAI) bit in the USBSTS register. If the interrupt on async advance enable (AAE) bit in the USBINTR register is set (1), then the host controller will assert an interrupt at the next interrupt threshold. The host controller clears (0) this bit after it has set (1) the interrupt on async advance status (AAI) bit in the USBSTS register. The software should not set (1) this bit when the asynchronous schedule is inactive. Doing so will yield undefined results. This bit is only used in the host mode. Setting (1) this bit when the device mode is selected will produce undefined results.
5	ASE	Asynchronous Schedule Enable Read/write Default = 0b This bit controls whether the host controller skips processing the asynchronous schedule. value 0 = Do not process the asynchronous schedule value 1 = Use the ASYNCLISTADDR register to access the asynchronous schedule. Only the host controller uses this bit.
4	PSE	Periodic schedule enable Read/write Default 0b This bit controls whether the host controller skips processing the periodic schedule. value 0 = Do not process the periodic schedule value 1 = Use the PERIODICLISTBASE register to access the periodic schedule. Only the host controller uses this bit.

USB4_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
3:2	FS_1_0	This field is Read/Write only if Programmable Frame List Flag in the HCCPARAMS registers is set to one. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index. Note that this field is made up from USBCMD bits 15, 3 and 2. Values meaning 000 1024 elements (4096 bytes) Default value 001 512 elements (2048 bytes) 010 256 elements (1024 bytes) 011 128 elements (512 bytes) 100 64 elements (256 bytes) 101 32 elements (128 bytes) 110 16 elements (64 bytes) 111 8 elements (32 bytes) Only the host controller uses this field.
1	RST	Controller reset (RESET) Read/write The software uses this bit to reset the controller. This bit is cleared (0) by the host/device controller when the reset process is complete. The software cannot terminate the reset process early by clearing (0) this bit. Host controller: When the software sets (1) this bit, the host controller resets its internal pipelines, timers, counters, state machines, and so on to their initial values. Any transaction currently in progress on the USB is immediately terminated. A USB reset is not driven on downstream ports. The software should not set (1) this bit when the HCHalted bit in the USBSTS register is clear (0). Attempting to reset an actively running host controller will result in undefined behavior. Device controller: When the software sets (1) this bit, the device controller resets its internal pipelines, timers, counters, state machines, and so on to their initial values. Setting this bit when the device is in the attached state is not recommended, since the effect on an attached host is undefined. In order to ensure that the device is not in an attached state before initiating a device controller reset, all primed endpoints should be flushed and the USBCMD run/stop bit should be cleared (0).

USB4_HS_USB_OTG_HS_USBCMD (cont.)

Bits	Name	Description
0	RS	Run/stop Read/Write Default 0b value 1 = Run value 0 = Stop Host controller: When this bit is set (1), the host controller proceeds with the execution of the schedule. The host controller continues execution as long as this bit remains set (1). When this bit is clear (0), the host controller completes the current transaction on the USB and then halts. The HC halted bit in the status register indicates when the host controller has finished the transaction and has entered the stopped state. The software should not set (1) this bit unless the host controller is in the halted state (that is, the HCHalted bit in the USBSTS register is set (1)). Device controller: Setting (1) this bit will cause the device controller to enable a pull-up on D+ and initiate an attach event. This control bit is not directly connected to the pull-up enable, as the pull-up will become disabled upon transitioning into high-speed mode. The software should use this bit to prevent an attach event before the device controller has been properly initialized. Clearing (0) this bit will cause a detach event.

0x12530144 USB4_HS_USB_OTG_HS_USBSTS

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_USBSTS register is the USB status register. This register indicates various states of the host/device controller and any pending interrupts. This register does not indicate status resulting from a transaction on the serial bus. The software clears certain bits in this register by setting (1) them.

USB4_HS_USB_OTG_HS_USBSTS

Bits	Name	Description
31	ULPI_INTR	Default value = 0.This bit is set when Interrupt during ULPI -Serial mode or ULPI Interrupt during LPM occurs. Writing a 1 to this bit will clear it.
30	PHY_SESS_VLD_CHG	This bit is set when PHY_SESS_VLD bit changes its value.
29	PHY_SESS_VLD	This bit presents the SESS_VLD status of PHY.

USB4_HS_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
28	PHY_ALT_INT	This bit is asserted when a non-USB interrupt from PHY is detected. This interrupt is used for procedures like Battery Charging. This bit is set when bit 7 (alt_int) of RX CMD is high. Writing a 1 to this bit will clear it.
27:26	RESERVED_BITS27_26	Clear (0) these bits.
25	TI1	General purpose timer interrupt 1 (GPTINT1) Read/write control This bit is set (1) when the counter in the GPTIMER1CTRL (non-EHCI) register transitions to zero. Setting (1) this bit will clear it.
24	TI0	General purpose timer interrupt 0 (GPTINT0) Read/write control This bit is set (1) when the counter in the GPTIMER0CTRL (non-EHCI) register transitions to zero. Setting (1) this bit will clear it.
23:20	RESERVED_BITS23_20	Clear (0) these bits.
19	UPI	USB host periodic interrupt (USBHSTPERINT) Read/write control This bit is set (1) by the host controller when the cause of an interrupt is a completion of a USB transaction, where the transfer descriptor (TD) has an interrupt on complete (IOC) bit set (1) and the TD was from the periodic schedule. This bit is also set (1) by the host controller when a short packet is detected AND the packet is on the periodic schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes. This bit is not used by the device controller and will always be clear (0).
18	UAI	USB host asynchronous interrupt (USBHSTASYNCINT) Read/write control This bit is set (1) by the host controller when the cause of an interrupt is a completion of a USB transaction, where the transfer descriptor (TD) has an interrupt on complete (IOC) bit set AND the TD was from the asynchronous schedule. This bit is also set (1) by the host when a short packet is detected AND the packet is on the asynchronous schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes. This bit is not used by the device controller and will always be clear (0).
17	RESERVED_BIT17	Clear (0) these bits.
16	NAKI	NAK interrupt bit Read only This bit is set (1) by the hardware when, for a particular endpoint, both the Tx/Rx endpoint NAK bit and the corresponding Tx/Rx endpoint NAK enable bit are set (1). This bit is automatically cleared (0) by the hardware when all of the enabled Tx/Rx endpoint NAK bits are cleared (0).

USB4_HS_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
15	AS	Asynchronous schedule status Read only Default = 0 This bit reports the current real status of the asynchronous schedule. When cleared (0), the asynchronous schedule status is disabled. And, if set (1), the status is enabled. The host controller is not required to immediately disable or enable the asynchronous schedule when software transitions the asynchronous schedule enable bit in the USBCMD register. When this bit and the asynchronous schedule enable bit are the same value, the asynchronous schedule is either enabled (1) or disabled (0). This bit is only used by the host controller.
14	PS	Periodic schedule status Read only Default = 0 This bit reports the current real status of the periodic schedule. When cleared (0), the periodic schedule is disabled. And, if set (1), the status is enabled. The host controller is not required to immediately disable or enable the periodic schedule when software transitions the periodic schedule enable bit in the USBCMD register. When this bit and the periodic schedule enable bit are the same value, the periodic schedule is either enabled (1) or disabled (0). This bit is only used by the host controller.
13	RCL	Reclamation Read only Default = 0 This is a read-only status bit that is used to detect an empty asynchronous schedule. This bit is only used by the host controller.
12	HCH	HC halted Read only Default = 1 This bit is a clear (0) whenever the run/stop bit is set (1). The host controller sets (1) this bit after it has stopped executing, because of the run/stop bit being cleared (0), either by the software or by the host controller hardware (for example, an internal error). This bit is only used by the host controller.
11	RESERVED_BIT11	Clear (0) this bit.
10	ULPII	ULPI interrupt Read/write control Default = 0 When the ULPI viewport is present in the design, an event completion will set (1) this interrupt. This bit is used by both the host and device controllers. It is only present in designs where the configuration constant VUSB_HS_PHY_ULPI = 1.

USB4_HS_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
9	RESERVED_BIT9	Clear (0) this bit.
8	SLI	DC suspend Read/write control Default = 0 When a device controller enters a suspend state from an active state, this bit will be set (1). The device controller clears (0) the bit upon exiting from a suspend state. This bit is only used by the device controller.
7	SRI	SOF received Read/write control Default = 0 When the device controller detects a start of (micro) frame, this bit will be set (1). When a SOF is extremely late, the device controller will automatically set (1) this bit to indicate that an SOF was expected. Therefore, this bit will be set (1) roughly every 1 ms in the device FS mode and every 125 ms in the HS mode, and will be synchronized to the actual SOF that is received. Since the device controller is initialized to FS before connect, this bit will be set (1) at an interval of 1 ms during the prelude to connect and chirp. In the host mode, this bit will be set (1) every 125 us and can be used by the host controller driver as a time base. The software writes a 1 to this bit to clear it. This is a non-EHCI status bit.
6	URI	USB reset received Read/write control Default = 0 When the device controller detects a USB reset and enters the default state, this bit will be set (1). The software can set (1) this bit to clear the USB reset received status bit. This bit is only used by the device controller.
5	AAI	Interrupt on async advance Read/write control Default = 0 The system software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by setting (1) the interrupt on async advance doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source. This bit is only used by the host controller.
4	SEI	System error Read/write control This interrupt is triggered when there is an AHB error (HRESP = ERROR) on the AHB Master interface.

USB4_HS_USB_OTG_HS_USBSTS (cont.)

Bits	Name	Description
3	FRI	Frame list rollover Read/write control The host controller sets (1) this bit when the frame list index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the frame list size field of the USBCMD register) is 1024, the frame index register rolls over every time FRINDEX [1 3] toggles. Similarly, if the size is 512, the host controller sets (1) this bit to a one every time FHINDEX [12] toggles. This bit is only used by the host controller.
2	PCI	Port change detect Read/write control The host controller sets (1) this bit when a connect status occurs on any port, a port enable/disable change occurs on any port, or the force port resume bit is set (1) as the result of a J-K transition on the suspended port. The device controller sets (1) this bit when the port controller enters the full or high-speed operational state. When the port controller exits the full or high-speed operation states due to reset or suspend events, the notification mechanisms are the USB reset received bit and the DC suspend bits, respectively. This bit is not EHCI compatible.
1	UEI	USB error interrupt (USBERRINT) Read/write control When completion of a USB transaction results in an error condition, this bit is set (1) by the host/device controller. This bit is set (1) along with the USBINT bit, if the TD on which the error interrupt occurred also had its interrupt-on-complete (IOC) bit set (1). The device controller detects resume signaling only.
0	UI	USB interrupt (USBINT) Read/write control This bit is set (1) by the host/device controller when the cause of an interrupt is a completion of a USB transaction where the transfer descriptor (TD) has an interrupt-on-complete (IOC) bit set (1). This bit is also set (1) by the host/device controller when a short packet is detected. A short packet is when the actual number of bytes received was less than the expected number of bytes.

0x12530148

USB4_HS_USB_OTG_HS_USBINTR

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_USBINTR register is the USB interrupt enable register. The interrupts to the software are enabled with this register. An interrupt is generated when a bit is set (1) and the corresponding interrupt is active. The USB status register (USBSTS) still shows interrupt sources, even if they are disabled by the USBINTR register, which allows polling of interrupt events by the software.

USB4_HS_USB_OTG_HS_USBINTR

Bits	Name	Description
31	ULPI_INTR_EN	Default value =0.When this bit is a 1 and ULPI_INTR is a 1, the controller will issue an interrupt. The interrupt is acknowledged by software clearing the ULPI_INTR bit.
30	PHY_SESS_VLD_CHG_EN	Default value =0. When this bit is set then Link Controller will issue an interrupt when PHY_SESS_VLD changes its value.
29:26	RESERVED_BITS29_26	Clear (0) these bits.
25	TIE1	General purpose timer interrupt enable 1 When this bit is set (1), and the GPTINT1 bit in the USBSTS register is set (1), the controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the GPTINT1 bit.
24	TIE0	General purpose timer interrupt enable 0 When this bit is set (1), and the GPTINT0 bit in the USBSTS register is set (1), the controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the GPTINT0 bit.
23:20	RESERVED_BITS23_20	Clear (0) these bits.
19	UPIE	USB host periodic interrupt enable When this bit is set (1), and the USBHSTPERINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBHSTPERINT bit.
18	UAIE	USB host asynchronous interrupt enable When this bit is set (1), and the USBHSTASYNCINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBHSTASYNCINT bit.
17	RESERVED_BIT17	Clear (0) this bit.

USB4_HS_USB_OTG_HS_USBINTR (cont.)

Bits	Name	Description
16	NAKE	NAK interrupt enable This bit is set (1) by the software if it wants to enable the hardware interrupt for the NAK interrupt bit. If both this bit and the corresponding NAK interrupt bit are set (1), a hardware interrupt is generated.
15:11	RESERVED_BITS15_11	Clear (0) these bits.
10	ULPIE	ULPI enable When this bit is set (1), and the ULPI Interrupt bit in the USBSTS register transitions, the controller will issue and interrupt. The interrupt is acknowledged by the software setting (1) the ULPI interrupt bit. This bit is used by both the host and device controllers. It is only present in designs where configuration constant VUSB_HS_PHY_ULPI = 1.
9	RESERVED_BIT9	Clear (0) this bit.
8	SLE	Sleep enable When this bit is set (1) and the DC suspend bit in the USBSTS register transitions, the device controller will issue an interrupt. The interrupt is acknowledged by the software setting (1) the DC suspend bit. This bit is only used by the device controller.
7	SRE	SOF received enable When this bit is set (1) and the SOF received bit in the USBSTS register is set (1), the device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the SOF received bit.
6	URE	USB reset enable When this bit is set (1) and the USB reset received bit in the USBSTS register is set (1), the device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the USB reset received bit.
5	AAE	Interrupt on async advance enable When this bit is set (1) and the interrupt on async advance bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the interrupt on async advance bit. This bit is only used by the host controller.
4	SEE	System error enable When this bit is set (1) and the system error bit in the USBSTS register is set (1), the host/device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the system error bit.

USB4_HS_USB_OTG_HS_USBINTR (cont.)

Bits	Name	Description
3	FRE	Frame list rollover enable When this bit is set (1) and the frame list rollover bit in the USBSTS register is set (1), the host controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the frame list rollover bit. This bit is only used by the host controller.
2	PCE	Port change detect enable When this bit is set (1) and the port change detect bit in the USBSTS register is set (1), the host/device controller will issue an interrupt. The interrupt is acknowledged by the software clearing (0) the port change detect bit.
1	UEE	USB error interrupt enable When this bit is set (1) and the USBERRINT bit in the USBSTS register is set (1), the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBERRINT bit in the USBSTS register.
0	UE	USB interrupt enable When this bit is set (1) and the USBINT bit in the USBSTS register is set (1), the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by the software clearing (0) the USBINT bit.

0x1253014C USB4_HS_USB_OTG_HS_FRINDEX

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_FRINDEX register is the USB frame index register. This register is used by the host controller to index the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits [N:3] are used to select a particular entry in the periodic frame list during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by the system software in the frame list size field in the USBCMD register.

This register must be written as a DWord. Byte writes produce-undefined results. This register cannot be written unless the host controller is in the 'halted' state, as indicated by the HC halted bit. A write to this register while the run/stop bit is set (1) produces undefined results. Writes to this register also affect the SOF value.

In the device mode, this register is read-only and the device controller updates the FRINDEX [13:3] register from the frame number indicated by the SOF marker. Whenever a SOF is received by the USB bus, FRINDEX [13:3] will be checked against the SOF marker. If FRINDEX [13:3] is different from the SOF marker, FRINDEX [13:3] will be set to the SOF value and FRINDEX [2:0] will be cleared (0) (that is, SOF for a 1-ms frame). If FRINDEX [13:3] is equal to the SOF value, FRINDEX [2:0] will be incremented (that is, SOF for 125-ms micro-frame.

USB4_HS_USB_OTG_HS_FRINDEX

Bits	Name	Description
31:14	RESERVED_BITS31_14	Clear (0) these bits.
13:0	FRINDEX_13_0	Frame index The value in this register increments at the end of each time frame (for example, a micro-frame). Bits [N:3] are used for the frame list current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. The following data shows the values of N based on the value of the frame list size field in the USBCMD register when used in host mode. USBCMD [Frame list size] number Elements N 000b (1024) 12 001b (512) 11 010b (256) 10 011b (128) 9 100b (64) 8 101b (32) 7 110b (16) 6 111b (8) 5 In the device mode, the value is the current frame number of the last frame transmitted. It is not used as an index. In either mode, bits 2:0 indicate the current microframe.

0x12530154 USB4_HS_USB_OTG_HS_PERIODICLISTBASE

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_PERIODICLISTBASE register is the periodic list base address register. This 32-bit register contains the beginning address of the periodic frame list in the system memory. The HCD loads this register prior to starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the frame index register (FRINDEX) to enable the host controller to step through the periodic frame list in sequence.

NOTE This device is shared between the host controller and device controller operation. For host controller operation, this is the USB_OTG_HS_ PERIODICLISTBASE register. For device controller operation, this is the USB_OTG_HS_DEVICEADDR register.

USB4_HS_USB_OTG_HS_PERIODICLISTBASE

Bits	Name	Description
31:12	PERBASE_31_12	Base address (low) These bits correspond to memory address signals [31:12], respectively. Only used by the host controller.
11:0	RESERVED_BITS11_0	This field must be written as zeros. During runtime, the values of these bits are undefined.

0x12530154 USB4_HS_USB_OTG_HS_DEVICEADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_DEVICEADDR register is the USB device address register. The upper seven bits of this register represent the device address. After any controller reset or a USB reset, the device address is set to the default address (0). The default address will match all incoming addresses. The software shall reprogram the address after receiving a SET_ADDRESS descriptor.

The USBADRA is used to accelerate the SET_ADDRESS sequence by allowing the DCD to preset the USBADR register before the status phase of the SET_ADDRESS descriptor.

NOTE This device is shared between the host controller and device controller operations. For host controller operation, this is the USB_OTG_HS_ PERIODICLISTBASE register. For device controller operation, this is the USB_OTG_HS_DEVICEADDR register.

USB4_HS_USB_OTG_HS_DEVICEADDR

Bits	Name	Description
31:25	USBADR_31_25	Device address These bits correspond to the USB device address.

USB4_HS_USB_OTG_HS_DEVICEADDR (cont.)

Bits	Name	Description
24	USBADRA	Device address advance Default = 0 When this bit is clear (0), any writes to USBADR are instantaneous. When this bit is set (1) at the same time or before USBADR is written, the write to the USBADR field is staged and held in a hidden register. After an IN occurs on endpoint 0 and is ACKed, USBADR will be loaded from the holding register. The hardware will automatically clear (0) this bit on the following conditions: 1. IN is ACKed to endpoint 0 (USBADR is updated from staging register). 2. OUT/SETUP occur to endpoint 0 (USBADR is not updated). 3. Device reset occurs (USBADR is reset to 0). Note: After the status phase of the SET_ADDRESS descriptor, the DCD has 2 ms to program the USBADR field. This mechanism will ensure this specification is met when the DCD can not write of the device address within 2 ms from the SET_ADDRESS status phase. If the DCD writes the USBADR with USBADRA = 1 after the SET_ADDRESS data phase (before the prime of the status phase), the USBADR will be programmed instantly at the correct time and meet the 2-ms USB requirement.
23:0	RESERVED_BITS23_0	These bits must be written as zeros. During runtime, the values of these bits are undefined.

0x12530158 USB4_HS_USB_OTG_HS_ASYNCLISTADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ASYNCLISTADDR register is the next asynchronous list address register. This 32-bit register contains the address of the next asynchronous queue head to be executed by the host. Bits [4:0] of this register cannot be modified by the system software and will always return a zero when read.

NOTE The USB_OTG_HS_ASYNCLISTADDR register and the USB_OTG_HS_ENDPOINTLISTADDR register are shared between the host controller and device controller operations. For the host controller, this is the USB_OTG_HS_ASYNCLISTADDR register. For the device controller, this is the USB_OTG_HS_ENDPOINTLISTADDR register.

USB4_HS_USB_OTG_HS_ASYNCLISTADDR

Bits	Name	Description
31:5	ASYBASE_31_15	Link pointer low (LPL). These bits correspond to memory address signals [31:5], respectively. This field may only reference a queue head (OH). This field is only used by the host controller.
4:0	RESERVED_BITS4_0	The values of these bits has no effect on circuit operation.

0x12530158 USB4_HS_USB_OTG_HS_ENDPOINTLISTADDR

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPOINTLISTADDR register is the endpointlist address register. In the device mode, this register contains the address of the top of the endpoint list in system memory. Bits [10:0] of this register cannot be modified by the system software and will always return a zero when read.

NOTE The USB_OTG_HS_ASYNCLISTADDR register and the USB_OTG_HS_ENDPOINTLISTADDR register are shared between the host controller and device controller operations. For the host controller, this is the USB_OTG_HS_ASYNCLISTADDR register. For the device controller, this is the USB_OTG_HS_ENDPOINTLISTADDR register.

USB4_HS_USB_OTG_HS_ENDPOINTLISTADDR

Bits	Name	Description
31:11	EPBASE_31_11	Endpoint list pointer (low) These bits correspond to memory address signals [31:11], respectively. This field will reference a list of up to 32 queue heads (QH). That is, one queue head per endpoint & direction.
10:0	RESERVED_BITS10_0	The values of these bits has no effect on circuit operation.

0x1253015C USB4_HS_USB_OTG_HS_TTCTRL

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_TTCTRL register is the TT status and control register. This register contains parameters needed for internal TT operations.

NOTE This register is not used in the device controller operation.

USB4_HS_USB_OTG_HS_TTCTRL

Bits	Name	Description
31	RESERVED_BIT31	Not used.
30:24	TTHA	Not used.
23:0	RESERVED_BITS23_0	Not used.

0x12530160 USB4_HS_USB_OTG_HS_BURSTSIZE

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x1010

The USB_OTG_HS_BURSTSIZE register is the programmable burst size register. This register is used to control dynamically change the burst size used during data movement on the initiator (master) interface.

USB4_HS_USB_OTG_HS_BURSTSIZE

Bits	Name	Description
31:16	RESERVED_BITS31_16	The value of these bits has no effect on circuit operation.
15:8	TXPBURST	Programmable Tx burst length This register represents the maximum length of a the burst in 32-bit words while moving data from system memory to the USB bus.
7:0	RXPBURST	Programmable Rx burst length This register represents the maximum length of a the burst in 32-bit words while moving data from the USB bus to system memory.

0x12530164 USB4_HS_USB_OTG_HS_TXFILLTUNING

Type: Read/write (writes must be DWord writes)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_TXFILLTUNING register is the host transmit pre-buffer packet tuning register. The fields in this register control performance tuning associated with how the host controller posts data to the Tx latency FIFO before moving the data onto the USB bus. The specific areas of performance include the how much data to post into the FIFO and an estimate for how long that operation should take in the target system.

Definitions:

T0 = Standard packet overhead

T1 = Time to send data payload

Tff = Time to fetch packet into TX FIFO up to specified level.

Ts = Total packet flight time (send-only) packet

Ts = T0 + T1

Tp = Total packet time (fetch and send) packet

Tp = Tff + T0 + T1

Upon discovery of a transmit (OUT/SETUP) packet in the data structures, the host controller checks to ensure Tp remains before the end of the [micro] frame. If so it proceeds to pre-fill the TX FIFO. If at anytime during the pre-fill operation the time remaining the [micro] frame is < Ts, then the packet attempt ceases and the packet is tried at a later time. Although this is not an error condition and the host controller will eventually recover, a mark will be made the scheduler health counter to note the occurrence of a ’back-off’ event. When a back-off event is detected, the partial packet fetched may need to be discarded from the latency buffer to make room for periodic traffic that will begin after the next SOF. Too many back-off events can waste bandwidth and power on the system bus, and thus should be minimized (not necessarily eliminated). Back-offs can be minimized with use of the TSCHHEALTH (Tff), as described in the register table.

USB4_HS_USB_OTG_HS_TXFILLTUNING

Bits	Name	Description
31:22	RESERVED_BITS31_22	The value of these bits has no effect on circuit operation.
21:16	TXFIFOTHRES	FIFO burst threshold Default = 2 This register controls the number of data bursts that are posted to the TX latency FIFO in the host mode before the packet begins on to the bus. The minimum value is 2 and this value should be a low as possible to maximize USB performance. A higher value can be used in systems with unpredictable latency and/or insufficient bandwidth, where the FIFO may underrun because the data transferred from the latency FIFO to USB occurs before it can be replenished from system memory. This value is ignored if the stream disable bit in USBMODE register is set (1).
15:13	RESERVED_BITS15_13	The value of these bits has no effect on circuit operation.

USB4_HS_USB_OTG_HS_TXFILLTUNING (cont.)

Bits	Name	Description
12:8	TXSCHHEALTH	Scheduler health counter Read/write to clear Default = 0 This register increments when the host controller fails to fill the Tx latency FIFO to the level programmed by TXFIFOTHRES before running out of time to send the packet before the next start-of-frame. This health counter measures the number of times this occurs to provide feedback to selecting a proper TXSCHOH. Writing to this register will clear the counter and this counter will be at a maximum at 31.
7:0	TXSCHOH	Scheduler overhead Default = 0 This register adds an additional fixed offset to the schedule time estimator described above as Tff. As an approximation, the value chosen for this register should limit the number of back-off events captured in the TXSCHHEALTH to less than 10 per second in a highly-utilized bus. Choosing a value that is too high for this register is not desired, as it can needlessly reduce USB utilization. The time unit represented in this register is 1.267 ms when a device is connected in the high-speed mode for OTG and SPH. The time unit represented in this register is 6.333 ms when a device is connected in the low/full speed mode for OTG and SPH. The time unit represented in this register is always 1.267 times the MPH product.

0x12530170 USB4_HS_USB_OTG_HS_ULPI_VIEWPORT

Type: Read/write (unless otherwise indicated)
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x08000000

The USB_OTG_HS_ULPI_VIEWPORT register provides indirect access to the ULPI PHY register set. Although the core performs access to the ULPI PHY register set, there may be extraordinary circumstances where software may need direct access.

CAUTION Writes to the ULPI through the viewport can substantially harm standard USB operations. Currently, no usage model has been defined where the software should need to execute writes directly to the ULPI - see the exception regarding optional features below.

Executing read operations though the ULPI viewport should have no harmful side effects to standard USB operations.

NOTE The ULPI viewport is only synthesized in the design if the constant VUSB_HS_PHY_ULPI is set (1). If the ULPI interface is not enabled, this register will always read zeros.

Two operations can be performed with the ULPI viewport: wake-up and read/write operations. The wake-up operation is used to put the ULPI interface into normal operation mode and re-enable the clock, if necessary. A wake-up operation is required before accessing the registers when the ULPI interface is operating in the low power mode, serial mode, or car kit mode.

The ULPI state can be determined by reading the sync state bit (ULPISS). If this bit is set (1), then the ULPI interface is running in the normal operation mode and can accept read/write operations. If the ULPISS is clear (0), then read/write operations will not be able to execute. Undefined behavior will result if ULPISS = 0, and a read or write operation is performed.

To execute a wake-up operation, write all 32-bits of the ULPI Viewport where ULPIPORT is constructed appropriately, and the ULPIWU bit is set (1) and the ULPIRUN bit is clear (0). Poll the ULPI viewport until ULPIWU is zero for the operation to complete.

To execute a read or write operation, write all 32-bits of the ULPI viewport where ULPIDATWR, ULPIADDR, ULPIPORT, and ULPIRW are constructed appropriately, and the ULPIRUN bit is set (1). Poll the ULPI viewport until ULPIRUN is zero for the operation to complete. Once ULPIRUN is zero, the ULPIDATRD will be valid if the operation was a read.

The polling method above could also be replaced and an interrupt driven using the ULPI interrupt defined in the USBTS and USBINTR registers. When a wake-up or read/write operation completes, the ULPI interrupt will be set (1).

Several optional features may need to be enabled or disabled by the system software as part of system configuration. These bits are contained in the interface and OTG control registers of the ULPI PHY register set. These registers also contain bits that are controlled by the link dynamically and, therefore, should only be modified by the system software using the set/clear access method. Direct writes to these registers could have harmful side effects to the standard USB operations. The following bits are optional bits:

- Bits 3 through 7 in the interface control register
- Bits 6 and 7 in the OTG control register.

Refer to the ULPI Specification Revision 1.1 for further information on the use of the optional features.

USB4_HS_USB_OTG_HS_ULPI_VIEWPORT

Bits	Name	Description
31	ULPIWU	ULPI wake-up Setting (1) this bit begins the wake-up operation. The bit will automatically transition to 0 after the wake-up is complete. Once this bit is set (1), the driver can not clear it back to 0. Note: The driver must never execute a wake-up and a read/write operation at the same time.
30	ULPIRUN	ULPI read/write run Setting (1) this bit will begin the read/write operation. The bit will automatically transition to 0 after the read/write is complete. Once this bit is set (1), the driver can not clear it back to 0. Note: The driver must never execute a wakeup and a read/write operation at the same time.

USB4_HS_USB_OTG_HS_ULPI_VIEWPORT (cont.)

Bits	Name	Description
29	ULPIRW	ULPI read/write control This bit selects between running a read or write operation. value 0 = Read value 1 = Write
28	ULPIFORCE	ULPI read/write force This bit enables forcing register access during RX packet value 0 = register access is not forced during RX packet (default) value 1 = register access is forced during RX packet reception
27	ULPISS	ULPI sync state Read Only value 1 = Normal sync state value 0 = In another state (for example, car kit, serial, low power) This bit represents the state of the ULPI interface. Before reading this bit, the ULPIPORT field should be set accordingly if used with the multi-port host. Otherwise, this field should always remain 0.
26:24	ULPIPORT	ULPI port number For the wakeup or read/write operation to be executed, this value selects the port number the ULPI PHY is attached to in the multi-port host. The valid range is 0 to 7. This field should always be written as a 0 for the non-multi port products.
23:16	ULPIADDR	ULPI data address When a read or write operation is commanded, the address of the operation is written to this field.
15:8	ULPIDATRD	ULPI data read Read only After a read operation completes, the result is placed in this field.
7:0	ULPIDATWR	ULPI data write When a write operation is commanded, the data to be sent is written to this field.

0x12530178 USB4_HS_USB_OTG_HS_ENDPTNAK

Type: Read/write clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTNAK register is the endpoint NAK register.

USB4_HS_USB_OTG_HS_ENDPTNAK

Bits	Name	Description
31:16	EPTN_15_0	Tx endpoint NAK Each tx endpoint has 1 bit in this field. The bit is set (1) when the device sends a NAK handshake on a received IN token for the corresponding endpoint. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0
15:0	EPRN_15_0	Rx endpoint NAK Each rx endpoint has 1 bit in this field. The bit is set (1) when the device sends a NAK handshake on a received OUT or PING token for the corresponding endpoint. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x1253017C USB4_HS_USB_OTG_HS_ENDPTNAKEN

Type: Read/write clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTNAKEN register is the endpoint NAK enable register.

USB4_HS_USB_OTG_HS_ENDPTNAKEN

Bits	Name	Description
31:16	EPTNE_15_0	Tx endpoint NAK enable Each bit is an enable bit for the corresponding Tx endpoint NAK bit. If this bit is set (1) and the corresponding Tx endpoint NAK bit is set (1), the NAK Interrupt bit is set (1). Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0
15:0	EPRNE_15_0	Rx endpoint NAK enable Each bit is an enable bit for the corresponding Rx endpoint NAK bit. If this bit is set (1) and the corresponding Rx endpoint NAK bit is set (1), the NAK Interrupt bit is set (1). Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x12530184 USB4_HS_USB_OTG_HS_PORTSC

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xCC000004

This is the USB_OTG_HS_PORTSC register.

USB4_HS_USB_OTG_HS_PORTSC

Bits	Name	Description
31:30	PTS	Parallel transceiver select Read/write This register bit pair is used in conjunction with the configuration constant VUSB_HS_PHY_TYPE to control which parallel transceiver interface is selected. If VUSB_HS_PHY_ TYPE is set for 0, 1, 2, or 3, then this bit is read only. If VUSB_HS_PHY_TYPE is 4, 5, 6, or 7, then this bit is read/write. This field is reset to the following values: 00 if VUSB_HS_PHY_TYPE = 0,4 - UTMI/UTMI+ 01 if VUSB_HS_PHY_TYPE = 1,5 - Reserved 10 if VUSB_HS_PHY_TYPE = 2,6 - ULPI 11 if VUSB_HS_PHY_TYPE = 3,7 - Serial/1.1 PHY (FS only) This bit is not defined in the EHCI specification.
29	STS	Serial transceiver select Read/write This register bit is used in conjunction with the configuration constant VUSB_HS_PHY_SERIAL to control whether the parallel or serial transceiver interface is selected for FS and LS operation. The serial interface engine can be used in combination with the UTMI+ or ULPI physical interface to provide FS/LS signaling instead of the parallel interface. ’ If VUSB_HS_PHY_SERIAL is 0 or 1, then this bit is read only. ’ If VUSB_HS_PHY_SERIAL is 2 or 3, then this bit is read/write. This bit has no effect unless the parallel transceiver select is set to UTMI+ or ULPI. The Serial/1.1 physical interface will use the serial interface engine for FS/LS signaling regardless of this bit value. Note: This bit was reserved for future operation, and is now adding for dynamic use of the serial engine in accord with UMTI+ and ULPI characterization logic. This bit is not defined in the EHCI specification.

USB4_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
28	PTW	Parallel transceiver width Read/write This register bit is used in conjunction with the configuration constant VUSB_HS_PHY16_8 to control the data bus width of the UTMI transceiver interface. ' If VUSB_HS_PHY16_8 is 0 or 1, then this bit is read only. ' If VUSB_HS_PHY16_8 is 2 or 3, then this bit is read/write. This bit is reset to 1 if VUSB_HS_PHY16_8 selects a default UTMI interface width of 16-bits, else it is reset to 0. ' Writing this bit to 0 selects the 8-bit [60MHz] UTMI interface. ' Writing this bit to 1 selects the 16-bit [30MHz] UTMI interface. This bit has no effect if the serial interface is selected. This bit is not defined in the EHCI specification.
27:26	PSPD	Port speed Read only This register field indicates the speed at which the port is operating. For HS mode operation in the host controller and HS/FS operation in the device controller, the port routing steers data to the protocol engine. For FS and LS mode operation in the host controller, the port routing steers data to the protocol engine with the embedded transaction translator. value 00 = Full speed value 01 = Low speed value 10 = High speed This bit is not defined in the EHCI specification.
25	SPRT	Short Port Reset Time. shortens port reset time for simulation.
24	PFSC	Port force full speed connect Read/write Default = 0 Setting (1) this bit will force the port to only connect at full speed. It also disables the chirp sequence that allows the port to identify itself as high speed. This is useful for testing FS configurations with a HS host, hub or device. This bit is not defined in the EHCI specification. This bit is for debugging purposes.

USB4_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
23	PHCD	PHY low power suspend - clock disable (PLPSCD) Read/write Default = 0 value 1 = Disable the PHY clock. value 0 = Enable the PHY clock. Reading this bit will indicate the status of the PHY clock. Note: The PHY clock cannot be disabled if it is being used as the system clock. In the device mode, The PHY can be put into low power suspend - clock disable when the device is not running (USBCMD run/stop = 0) or the host has signaled suspend (PORTSC SUSPEND = 1). Low power suspend will be cleared automatically when the host has signaled resume. Before forcing a resume from the device, the device controller driver must clear this bit. In the host mode, the PHY can be put into low power suspend - clock disable when the downstream device has been put into the suspend mode or when no downstream device is connected. Low power suspend is completely under the control of the software. This bit is not defined in the EHCI specification.
22	WKOC	Wake on over-current enable (WKOC_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to over-current conditions as wake-up events. This bit is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0). This bit is output from the controller as signal pwrctl_wake_ ovrcurr_en (OTG/host core only) for use by an external power control circuit.
21	WKDS	Wake on disconnect enable (WKDSCNNT_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to device disconnects as wake-up events. This field is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0) or in the device mode. This bit is output from the controller as signal pwrctl_wake_ dscnnt_en (OTG/host core only) for use by an external power control circuit.

USB4_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
20	WKCN	Wake on connect enable (WKCNNT_E) Read/write Default = 0 Setting (1) this bit enables the port to be sensitive to device connects as wake-up events. This field is clear (0) if the port power (PP) bit (bit 12) in this register is clear (0) or in the device mode. This bit is output from the controller as signal pwrctl_wake_ dscnnt_en (OTG/host core only) for use by an external power control circuit.

USB4_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
19:16	PTC_3_0	Port test control Read/write Default = 0000 Any other value than zero indicates that the port is operating in the test mode. Value Specific test The FORCE_ENABLE_FS and FORCE ENABLE_LS tests are extensions to the test mode support, as specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. Note: Low speed operations are not supported as a peripheral device. 0x0: TEST_MODE_DISABLE 0x1: J_ STATE 0x8: K_STATE 0x9: SE0 (host / NAK device) 0x40: Packet 0x41: FORCE_ENABLE_HS 0x48: FORCE_ENABLE_FS 0x49: FORCE_ENABLE_LS 0x3E8: Reserved_1 0x3E9: Reserved_2 0x3EA: Reserved_3 0x3EB: Reserved_4 0x3EC: Reserved_5 0x3ED: Reserved_6 0x3EE: Reserved_7 0x3EF: Reserved_8 0x3F0: Reserved_9 0x3F1: Reserved_10 0x3F2: Reserved_11 0x3F3: Reserved_12 0x3F4: Reserved_13 0x3F5: Reserved_14 0x3F6: Reserved_15 0x3F7: Reserved_16 0x3F8: Reserved_17 0x3F9: Reserved_18 0x3FA: Reserved_19 0x3FB: Reserved_20 0x3FC: Reserved_21 0x3FD: Reserved_22 0x3FE: Reserved_23 0x3FF: Reserved_24 0x400: Reserved_25 0x401: Reserved_26 0x402: Reserved_27 0x403: Reserved_28 0x404: Reserved_29 0x405: Reserved_30 0x406: Reserved_31

USB4_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
15:14	PIC_1_0	Port indicator control Read/write Default = 0 Writing to this field has no effect if the P_INDICATOR bit in the HCSPARAMS register is a zero. If the P_INDICATOR bit is set (1), then this field has the following meanings: Bit value Meaning value 00 Port indicators are off value 01 Amber value 10 Green value 11 Undefined Refer to the USB Specification Revision 2.0 [3] for a description on how these bits are to be used. This field is output from the controller as signals port_ind_ctl_1 and port_ind_ctl_0 for use by an external LED driving circuit.
13	PO	Port owner Read only Port owner hand-off is not implemented in this design, therefore this bit will always read back as clear (0). Default = 0 The EHCI definition is include here for reference: ’ This bit unconditionally goes clear (0) when the configured bit in the CONFIGFLAG register makes a 0-to-1 transition. ’ This bit unconditionally goes set (1) whenever the configured bit is clear (0). The system software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). The software sets (1) this bit when the attached device is not a high-speed device. When this bit is set (1), it indicates that an internal companion controller owns and controls the port.

USB4_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
12	PP	Port power (PP) Read/write or read-only The function of this bit depends on the value of the port power switching (PPC) field in the HCSPARAMS register. ’ PPC = 0: PP is read-only. A device controller with no OTG capability does not have port power control switches. ’ PPC = 1: PP is read/write. The host/OTG controller requires port power control switches. This bit represents the current setting of the switch (0 = off, 1 = on). When power is not available on a port (and PP equals a 0), the port is non-functional and will not report attaches, detaches, and so on. When an over-current condition is detected on a powered port and PPC is set (1), the PP bit in each affected port may be transitioned by the host controller driver from a one to a zero, removing power from the port. This feature is implemented in the host/OTG controller (PPC = 1). In a device-only implementation, port power control is not necessary. So, PPC and PP = 0.
11:10	LS_1_0	Line status Read-only These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines: Value Meaning value 00 SE0 value 10 J-state value 01 K-state value 11 Undefined In the host mode, the use of line state by the host controller driver is not necessary (unlike EHCI), because the port controller state machine and the port routing manage the connection of LS and FS. In the device mode, the use of line state by the device controller driver is not necessary.
9	HSP	High-speed port Read-only Default = 0 When the bit is set (1), the host/device connected to the port is in the high-speed mode. When this bit is clear (0), the host/device connected to the port is not in a high-speed mode. Note: HSP is redundant with PSPD(27:26), but will remain in the design for compatibility. This bit is not defined in the EHCI specification.

USB4_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
8	PR	Port reset This bit is clear (0) if the port power (PP) bit (bit 12) of this register is clear (0). Host mode: ’ Read/write ’ Default = 0 When the software sets (1) this bit, the bus-reset sequence as defined in the USB Specification Revision 2.0 is started. This bit will automatically clear (go to 0) after the reset sequence is complete. Note: This behavior is different from EHCI, where the host controller driver is required to clear (0) this bit after the reset duration is timed in the driver. Device mode: This bit is a read-only status bit. Device reset from the USB bus is also indicated in the USBSTS register. 0x1: Port is in reset 0x0: Port is not in reset

USB4_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
7	SUSP	Suspend Host mode: ' Read/write ' Default = 0 The port enabled bit and suspend bit of this register define the port states: Bit value Port state value 0x Disable value 10 Enable value 11 Suspend When in the suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction if a transaction was in progress when this bit set (1). In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. The host controller will unconditionally clear (0) this bit when the software clears (0) the force port resume bit. The host controller ignores a write of zero to this bit. If the host software sets (1) this bit when the port is not enabled (port enabled bit is a zero), the results are undefined. This field is clear (0) if port power (PP) is clear (0) in the host mode. Device mode: ' Read only ' Default = 0 In the device mode, this bit is a read-only status bit. 0x1: Port in suspend state_1 0x0: Port not in suspend st_1 0x1: Port in suspend state_2 0x0: Port not in suspend st_2

USB4_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
6	FPR	Force port resume ’ Read/write ’ Default = 0 Host mode: The software sets (1) this bit to drive resume signaling. The host controller sets (1) this bit if a J-to-K transition is detected while the port is in the suspend state. When this bit transitions to a one because a J-to-K transition is detected, the port change detect bit in the USBSTS register is also set (1). This bit will automatically clear (go to 0) after the resume sequence is complete. This behavior is different from EHCI, where the host controller driver is required to clear (0) this bit after the resume duration is timed in the driver. Note that, when the host controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (full-speed 'K') is driven on the port as long as this bit remains set (1). This bit will remain set (1) until the port has switched to the high-speed idle. Clearing (0) this bit has no affect, because the port controller will time the resume operation and clear (0) the bit when the port control state switches to HS or FS idle. This bit is clear if the port power (PP) is clear (0) in the host mode. This bit is not-EHCI compatible. Device mode: After the device has been in the suspend state for 5 ms or more, the software must set (1) this bit to drive resume signaling before clearing. The device controller will set (1) this bit if a J-to-K transition is detected while the port is in the suspend state. The bit will be cleared (0) when the device returns to normal operation. Also, when this bit transitions to a one because a J-to-K transition was detected, the port change detect bit in the USBSTS register is also set (1). 0x1: Resume detected/driven on port 0x0: No resume (K-state detected/driven on port)
5	OCC	Over-current change Read/write control Default = 0 This bit gets is set (1) when there is a change to over-current active. The software clears this bit by setting (1) this bit position. For host/OTG implementations, the user can provide over-current detection to the vbus_pwr_fault input for this condition. For device-only implementations, this bit shall always be clear (0).

USB4_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
4	OCA	Over-current active Read-only Default = 0 value 1 = This port currently has an over-current condition. value 0 = This port does not have an over-current condition. This bit will automatically transition from set (1) to clear (0) when the over current condition is removed. For host/OTG implementations, the user can provide over-current detection to the vbus_pwr_fault input for this condition. For device-only implementations, this bit shall always be clear (0).
3	PEC	Port enable/disable change Read/write control value 1 = Port enabled/disabled status has changed value 0 = No change Default = 0 Host mode: For the root hub, this bit gets set (1) only when a port is disabled due to disconnect on the port or due to the appropriate conditions existing at the EOF2 point. The software clears this bit by writing a one to it. This field is clear (0) if the port power (PP) bit in the register is clear (0). Device mode: The device port is always enabled (this bit will be zero).
2	PE	Port enabled/disabled Read/write value 1 = Enable value 0 = Disable Default 0 Host mode: Ports can only be enabled by the host controller as a part of the reset and enable. The software cannot enable a port by setting (1) this field. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by the host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port, due to other host controller and bus events. When the port is disabled, (0) downstream propagation of data is blocked except for reset. This field is clear (0) if the port power (PP) bit is cleared (0) in the host mode. Device mode: The device port is always enabled (this bit will be set [1])

USB4_HS_USB_OTG_HS_PORTSC (cont.)

Bits	Name	Description
1	CSC	Connect status change Read/write control value 1 = Change in current connect status value 0 = No change Default = 0 Host mode: Indicates that a change has occurred in the port's current connect status. The host/device controller sets (1) this bit for all changes to the port device connect status, even if the system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, the hub hardware will be 'setting' an already-set bit (that is, the bit will remain set). The software clears this bit by writing a one to it. This field is zero if the port power (PP) bit in this register is zero in the host mode. Device mode: This bit is undefined in the device controller mode.
0	CCS	Current connect status Read-only Host mode: value 1 = Device is present on port value 0 = No device is present Default = 0 This value reflects the current state of the port, and may not correspond directly to the event that caused the connect status change bit (bit 1) to be set (1). This field is clear if the port power (PP) bit in this register is clear (0) in host mode. Device mode: value 1 = Attached value 0 = Not attached Default = 0 If this bit is set (1), this indicates that the device successfully attached, and is operating in either high speed or full speed, as indicated by the high speed port bit in this register. If this bit is clear (0), this indicates that the device did not attach successfully or was forcibly disconnected by the software clearing (0) the run bit in the USBCMD register. It does not state the device being disconnected or suspended.

0x125301A4 USB4_HS_USB_OTG_HS_OTGSC

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000E20

USB4_HS_USB_OTG_HS_OTGSC

Bits	Name	Description
31	RESERVED_BIT31	Clear (0) this bit.
30	DPIE	Data pulse interrupt enable
29	B_1MSE	1 millisecond timer interrupt enable - read/write
28	BSEIE	B session end interrupt enable Read/write Setting (1) this bit enables the B session end interrupt.
27	BSVIE	B session valid interrupt enable Read/write Setting (1) this bit enables the B session valid interrupt.
26	ASVIE	A session valid interrupt enable Read/write Setting (1) this bit enables the A session valid interrupt.
25	AVVIE	A Vbus valid interrupt enable Read/write Setting (1) this bit enables the A Vbus valid interrupt.
24	IDIE	USB ID interrupt enable Read/write Setting (1) this bit enables the USB ID interrupt.
23	RESERVED_BIT23	Clear (0) this bit.
22	DPIS	Data pulse interrupt status Read/write to clear This bit is set (1) when data bus pulsing occurs on DP or DM. Data bus pulsing is only detected when USBMODE.CM = Host (11) and PORTSC(0). PortPower = Off (0). The software must write a one to clear this bit.
21	B_1MSS	1 millisecond timer interrupt status Read/write to clear This bit is set (1) once every millisecond. The software must write a one to clear this bit.
20	BSEIS	B session end interrupt status Read/write to clear This bit is set (1) when the Vbus has fallen below the B session end threshold. The software must write a one to clear this bit
19	BSVIS	B session valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the B session valid threshold (0.8 VDC). The software must write a one to clear this bit.

USB4_HS_USB_OTG_HS_OTGSC (cont.)

Bits	Name	Description
18	ASVIS	A session valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the A session valid threshold (0.8 VDC). The software must write a one to clear this bit.
17	AVVIS	A Vbus valid interrupt status Read/write to clear This bit is set (1) when Vbus has either risen above or fallen below the Vbus valid threshold (4.4 VDC) on an A device. The software must write a one to clear this bit.
16	IDIS	USB ID interrupt status Read/write This bit is set (1) when a change on the ID input has been detected. The software must write a one to clear this bit.
15	RESERVED_BIT15	Clear (0) this bit.
14	DPS	Data bus pulsing status Read-only If this bit is set (1), it indicates that the data bus pulsing is being detected on the port.
13	B_1MST	1 millisecond timer toggle Read-only This bit toggles once per millisecond.
12	BSE	B session end Read-only Indicates that the Vbus is below the B session end threshold.
11	BSV	B session valid Read-only Indicates that the Vbus is above the B session valid threshold.
10	ASV	A session valid Read-only Indicates that the Vbus is above the A session valid threshold.
9	AVV	A Vbus valid Read-only Indicates that the Vbus is above the A Vbus valid threshold.
8	ID	USB ID Read-only value 0 = A device value 1 = B device

USB4_HS_USB_OTG_HS_OTGSC (cont.)

Bits	Name	Description
7	HABA	Hardware assist B-disconnect to A-connect Read/write value 0 = Disabled value 1 = Enable automatic B-disconnect to A-connect sequence.
6	HADP	Hardware assist data-pulse Write to set
5	IDPU	ID pull-up Read/write This bit provides control over the ID pull-up register. value 0 = Off value 1 = On (default) When this bit is clear (0), the ID input will not be sampled.
4	DP	Data pulsing Read/write Setting (1) this bit causes the pull-up on DP to be asserted for data pulsing during SRP.
3	OT	OTG termination Read/write This bit must be set (1) when the OTG device is in the device mode. This controls the pull-down on DM.
2	HAAR	Hardware assist auto-reset Read/write value 0 = Disabled value 1 = Enable automatic reset after connect on host port.
1	VC	Vbus charge Read/write Setting (1) this bit causes the Vbus line to be charged. This is used for Vbus pulsing during SRP.
0	VD	Vbus discharge Read/write Setting (1) this bit causes the Vbus to discharge through a resistor.

0x125301A8 USB4_HS_USB_OTG_HS_USBMODE

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_USBMODE register is the USB device mode register.

USB4_HS_USB_OTG_HS_USBMODE

Bits	Name	Description
31:6	RESERVED_BITS31_6	Clear (0) these bits.
5	VBPS	Vbus power select value 0 - Output is 0 value 1 - Output is 1 This bit is connected to the vbus_pwr_select output and can be used for any generic control, but is named to be used by logic that selects between an on-chip Vbus power source (charge pump) and an off-chip source in systems when both are available.
4	SDIS	Stream disable mode value 0 = Inactive (default) value 1 = Active Device mode: Setting (1) this bit disables double priming on both the Rx and Tx for low bandwidth systems. This mode ensures that, when the Rx and Tx buffers are sufficient to contain an entire packet, the standard double buffering scheme is disabled to prevent overruns/underruns in bandwidth-limited systems. Note: In the high speed mode, a NYET handshake will respond to all packets received when the stream disable is active. Host mode: Setting (1) this bit ensures that overruns/underruns of the latency FIFO are eliminated for low bandwidth systems where the Rx and Tx buffers are sufficient to contain the entire packet. Enabling the stream disable also has the effect of ensuring that the Tx latency is filled to capacity before the packet is launched onto the USB. Note: Time duration to pre-fill the FIFO becomes significant when the stream disable is active. See TXFILLTUNING and TXTTFILLTUNING [MPH only] to characterize the adjustments needed for the scheduler when using this feature. Note: The use of this feature substantially limits of the overall USB performance.
3	SLOM	Setup lockout mode. In the device mode, this bit controls the behavior of the setup lock mechanism. value 0 = Setup lockouts on (default) value 1 = Setup lockouts off (DCD requires use of a setup data buffer tripwire in USBCMD)

USB4_HS_USB_OTG_HS_USBMODE (cont.)

Bits	Name	Description
2	ES	Endian select Read/write This bit can change the byte ordering of the transfer buffers to match the host microprocessor bus architecture. The bit fields in the microprocessor interface and the DMA data structures (including the setup buffer within the device QH) are unaffected by the value of this bit, because they are based upon 32-bit words. value 0 = Little endian (default) - first byte referenced in the least significant byte of a 32-bit word. value 1 = Big endian - first byte referenced in most significant byte of a 32-bit word.
1:0	CM	Controller mode Read/write once The controller mode is defaulted to the proper mode for host-only and device-only implementations. For those designs that contain both host and device capability, the controller will default to an idle state and will need to be initialized to the desired operating mode after reset. For combination host/device controllers, this register can only be written once after reset. If it is necessary to switch modes, the software must reset the controller by writing to the RESET bit in the USBCMD register before reprogramming this register. value 00 = Idle [default for combination host/device] value 01 = Reserved value 10 = Device controller [default for device only controller] value 11 = Host controller [default for host only controller]

0x125301AC USB4_HS_USB_OTG_HS_ENPDTSETUPSTAT

Type: Read/write control
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENPDTSETUPSTAT register is the endpoint set-up status register.

USB4_HS_USB_OTG_HS_ENPDTSETUPSTAT

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.

USB4_HS_USB_OTG_HS_ENPDTSETUPSTAT (cont.)

Bits	Name	Description
15:0	ENDPTSETUPSTAT_15_0	Set-up endpoint status For every set-up transaction that is received, a corresponding bit in this register is set (1). The software must clear or acknowledge the setup transfer by setting (1) a respective bit after it has read the setup data from the queue head. The response to a set-up packet as in the order of operations and total response time is crucial to limit bus time outs while the set-up lock-out mechanism is engaged. See Managing Endpoints in the Device Operational Model. This register is only used in the device mode.

0x125301B0 USB4_HS_USB_OTG_HS_ENDPTPRIME

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTPRIME register is the endpoint initialization register. This register is only used in the device mode.

USB4_HS_USB_OTG_HS_ENDPTPRIME

Bits	Name	Description
31:16	PETB_15_0	Prime endpoint transmit buffer For each endpoint, a corresponding bit is used to request that a buffer is prepared for a transmit operation in order to respond to a USB IN/INTERRUPT transaction. The software should set (1) the corresponding bit when posting a new transfer descriptor to an endpoint. The hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a transmit buffer. The hardware will clear (0) this bit when the associated endpoint(s) is (are) successfully primed. Note: These bits will be momentarily set (1) by the hardware during hardware re-priming operations when a dTD is retired, and the dQH is updated. PETB[15] - Endpoint 15 PETB[1] - Endpoint 1 PETB[0] - Endpoint 0

USB4_HS_USB_OTG_HS_ENDPTPRIME (cont.)

Bits	Name	Description
15:0	PERB_15_0	Prime endpoint receive buffer For each endpoint, a corresponding bit is used to request that a buffer is prepared for a receive operation for when a USB host initiates a USB OUT transaction. The software should set (1) the corresponding bit whenever posting a new transfer descriptor to an endpoint. The hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a receive buffer. The hardware will clear (0) this bit when the associated endpoint(s) is (are) successfully primed. Note: These bits will be momentarily set (1) by the hardware during hardware re-priming operations when a dTD is retired, and the dQH is updated. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x125301B4 USB4_HS_USB_OTG_HS_ENDPTFLUSH

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTFLUSH register is the endpoint de-initialize register. This register is only used in the device mode.

USB4_HS_USB_OTG_HS_ENDPTFLUSH

Bits	Name	Description
31:16	FETB_15_0	Flush endpoint transmit buffer Setting (1) a bit in this register will cause the associated endpoint to clear any primed buffers. If a packet is in progress for one of the associated endpoints, that transfer will continue until completion. The hardware will clear this register after the endpoint flush operation is successful. FETB[15] - Endpoint 15 FETB[1] - Endpoint 1 FETB[0] - Endpoint 0
15:0	FERB_15_0	Flush endpoint receive buffer Setting a bit (1) will cause the associated endpoint to clear any primed buffers. If a packet is in progress for one of the associated endpoints, that transfer will continue until completion. The hardware will clear this register after the endpoint flush operation is successful. Bit 15 - Endpoint 15 Bit 1 - Endpoint 1 Bit 0 - Endpoint 0

0x125301B8 USB4_HS_USB_OTG_HS_ENDPTSTAT

Type: Read-only
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTSTAT register is the endpoint status register. This register is only used in the device mode.

USB4_HS_USB_OTG_HS_ENDPTSTAT

Bits	Name	Description
31:16	ETBR_15_0	Endpoint transmit buffer ready One bit for each endpoint indicates the status of the respective endpoint buffer. This bit is set (1) by the hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There will always be a delay between setting (1) a bit in the ENDPTPRIME register and the endpoint indicating that it is ready. This delay time varies based upon the current USB traffic and the number of bits set (1) in the ENDPTPRIME register. The buffer ready status is cleared by a USB reset, by the USB DMA system, or through the ENDPTFLUSH register. Note: These bits will be momentarily cleared by the hardware during hardware endpoint re-priming operations when a dTD is retired, and the dQH is updated. ETBR[15] - Endpoint 15 ETBR[1] - Endpoint 1 ETBR[0] - Endpoint 0
15:0	ERBR_15_0	Endpoint receive buffer ready One bit for each endpoint indicates the status of the respective endpoint buffer. This bit is set (1) by the hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There will always be a delay between setting (1) a bit in the ENDPTPRIME register and the endpoint indicating that it is ready. This delay time varies based upon the current USB traffic and the number of bits set (1) in the ENDPTPRIME register. The buffer ready status is cleared by a USB reset, by the USB DMA system, or through the ENDPTFLUSH register. Note: These bits will be momentarily cleared by the hardware during hardware endpoint re-priming operations when a dTD is retired, and the dQH is updated. ERBR[15] - Endpoint 15 ERBR[1] - Endpoint 1 ERBR[0] - Endpoint 0

0x125301BC USB4_HS_USB_OTG_HS_ENDPTCOMPLETE

Type: Read/write control
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The register is the endpoint complete register. This register is only used in the device mode.

USB4_HS_USB_OTG_HS_ENDPTCOMPLETE

Bits	Name	Description
31:16	ETCE_15_0	Endpoint transmit complete event Each bit indicates that a transmit event (IN/INTERRUPT) occurred and the software should read the corresponding endpoint queue to determine the endpoint status. If the corresponding IOC bit is set (1) in the transfer descriptor, then this bit will be set (1) simultaneously with the USBINT. Writing a one will clear the corresponding bit in this register. ETCE[15] - Endpoint 15 ETCE[1] - Endpoint 1 ETCE[0] - Endpoint 0
15:0	ERCE_15_0	Endpoint receive complete event Each bit indicates that a received event (OUT/SETUP) occurred and the software should read the corresponding endpoint queue to determine the transfer status. If the corresponding IOC bit is set (1) in the transfer descriptor, then this bit will be set (1) simultaneously with the USBINT. Writing a one will clear the corresponding bit in this register. ERCE[15] - Endpoint 15 ERCE[1] - Endpoint 1 ERCE[0] - Endpoint 0

0x125301C0 USB4_HS_USB_OTG_HS_ENDPTCTRL0

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00800080

The USB_OTG_HS_ENDPTCTRL0 register is the endpoint control 0 register. Every device will implement endpoint0 as a control endpoint.

USB4_HS_USB_OTG_HS_ENDPTCTRL0

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.

USB4_HS_USB_OTG_HS_ENDPTCTRL0 (cont.)

Bits	Name	Description
23	TXE	Tx endpoint enable value 1 = Enabled Endpoint0 is always enabled. Read only
22:20	RESERVED_BITS22_20	Clear (0) these bits.
19:18	TXT	Tx endpoint type Read only value 00 = Control Endpoint0 is fixed as a control end point.
17	RESERVED_BIT17	Clear (0) this bit.
16	TXS	Tx endpoint stall Read/write value 0 = End point OK (default) value 1 = End point stalled The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. It will continue returning STALL until the bit is cleared (0) by the software or it will automatically be cleared (0) upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). Note: There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. In most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15:8	RESERVED_BITS15_8	Clear (0) these bits.
7	RXE	Rx endpoint enable value 1 = Enabled Endpoint0 is always enabled. Read only
6:4	RESERVED_BITS6_4	Clear (0) these bits.
3:2	RXT	Rx endpoint type Read only value 00 = Control Endpoint0 is fixed as a control end point.
1	RESERVED_BIT1	Clear (0) this bit.

USB4_HS_USB_OTG_HS_ENDPTCTRL0 (cont.)

Bits	Name	Description
0	RXS	Rx endpoint stall Read/write value 0 = End point OK (default) value 1 = End point stalled The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. It will continue returning STALL until the bit is cleared (0) by the software or it will automatically be cleared (0) upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). Note: There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. In most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

0x125301C0+4*n USB4_HS_USB_OTG_HS_ENDPTCTRLn, n=[1..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_ENDPTCTRLn register is the endpoint control n register. There is an ENDPTCTRLn register for each endpoint in a device.

CAUTION If one endpoint direction is enabled and the paired endpoint of the opposite direction is disabled, then the unused direction type must be changed from the default control-type to any other type (such as bulk-type). Leaving an unconfigured endpoint control will cause undefined behavior for the data PID tracking on the active endpoint/direction.

USB4_HS_USB_OTG_HS_ENDPTCTRLn

Bits	Name	Description
31:24	RESERVED_BITS31_24	Clear (0) these bits.
23	TXE	Tx endpoint enable value 0 = Disabled (default) value 1 = Enabled An endpoint should be enabled only after it has been configured.

USB4_HS_USB_OTG_HS_ENDPTCTRLn (cont.)

Bits	Name	Description
22	TXR	Tx data toggle reset (WS) value 1 = Reset PID sequence Whenever a configuration event is received for this endpoint, the software must set (1) this bit in order to synchronize the data PIDs between the host and device.
21	TXI	Tx data toggle inhibit value 0 = PID sequencing enabled (default) value 1 = PID sequencing disabled This bit is only used for testing and should always be cleared (0). Setting (1) this bit will cause this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.
20	RESERVED_BIT20	Clear (0) this bit.
19:18	TXT	Tx endpoint type value 00 = Control value 01 = Isochronous value 10 = Bulk value 11 = Interrupt
17	TXD	Tx endpoint data source value 0 = Dual port memory buffer/DMA engine (default) This bit should always be cleared (0).
16	TXS	Tx endpoint stall value 0 = End point OK value 1 = End point stalled This bit will be cleared (0) automatically upon receipt of a SETUP request if this endpoint is configured as a control endpoint, and this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. This control will continue to STALL until this bit is either cleared (0) by the software or automatically cleared (0) as described above for control endpoints. Note (control endpoint types only): There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. in most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.
15:8	RESERVED_BITS15_8	Clear (0) these bits.
7	RXE	Rx endpoint enable value 0 = Disabled (default) value 1 = Enabled An endpoint should be enabled only after it has been configured.

USB4_HS_USB_OTG_HS_ENDPTCTRLn (cont.)

Bits	Name	Description
6	RXR	Rx data toggle reset (WS) Write 1 = Reset PID sequence Whenever a configuration event is received for this endpoint, the software must set (1) this bit in order to synchronize the data PIDs between the host and the device.
5	RXI	Rx data toggle inhibit value 0 = Disabled (default) value 1 = Enabled This bit is only used for testing and should always be cleared (0). Setting (1) this bit will cause this endpoint to ignore the data toggle sequence and always accept a data packet regardless of their data PID.
4	RESERVED_BIT4	Clear (0) this bit.
3:2	RXT	Rx endpoint type value 00 = Control value 01 = Isochronous value 10 = Bulk value 11 = Interrupt
1	RXD	Rx endpoint data sink value 0 = Dual port memory buffer/DMA engine (default) This bit should always be cleared (0).
0	RXS	Rx endpoint stall value 0 = End point OK value 1 = End point stalled This bit will be cleared (0) automatically upon receipt of a SETUP request if this endpoint is configured as a control endpoint, and this bit will continue to be cleared (0) by the hardware until the associated ENDPTSETUPSTAT bit is cleared (0). The software can set (1) this bit to force the endpoint to return a STALL handshake to the host. This control will continue to STALL until this bit is either cleared (0) by the software or automatically cleared (0) as described above for control endpoints. Note (control endpoint types only): There is a slight delay (50 clocks maximum) between the ENDPTSETUPSTAT being cleared (0) and the hardware continuing to clear (0) this bit. in most systems, it is unlikely that the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set (1) after writing a one to it, then continually write this stall bit until it is set (1) or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

0x125301FC+4*n USB4_HS_USB_OTG_HS_ENDPT_PIPE_IDn, n=[1..15]

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x001F001F

The USB_OTG_HS_ENDPT_PIPE_IDn register is the endpoint pipe number register. There is an USB_OTG_HS_ENDPT_PIPE_IDn register for each endpoint in a device.

NOTE reset value of TX_PIPE_ID and RX_PIPE_ID is 0x1F, which means that Endpoint is not mapped to any pipe.

USB4_HS_USB_OTG_HS_ENDPT_PIPE_IDn

Bits	Name	Description
31:21	RESERVED_BITS31_21	Clear (0) these bits.
20:16	TX_PIPE_ID	This field indicate the pipe number that this tx end point (n) will use in pipe mode.
15:5	RESERVED_BITS15_5	Clear (0) these bits.
4:0	RX_PIPE_ID	This field indicate the pipe number that this rx end point (n) will use in pipe mode.

0x12530240 USB4_HS_USB_OTG_HS_PHY_CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0b1110000111010

The USB_OTG_HS_PHY_CTRL register is used to configure various features in the Synopsys 28nm PHY.

USB4_HS_USB_OTG_HS_PHY_CTRL

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12	USB2_PHY_IDHV_CLAMP_EN	Clamp enable for IDHV interrupt level shifter from USB VDD180 domain to VDDCX domain. When set (1), VLS is active and IDHV interrupt is translated from 1.8V domain to Vddcx domain. When clear (0), VLS is clamped high. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.
11	USB2_PHY_OTGSESSVLDHV_CLAMP_EN	Clamp enable for OTGSESSVLDHV interrupt level shifter from USB VDD180 domain to VDDCX domain. When set (1), VLS is active and OTGSESSVLDHV interrupt is translated from 1.8V domain to Vddcx domain. When clear (0), VLS is clamped to zero. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.

USB4_HS_USB_OTG_HS_PHY_CTRL (cont.)

Bits	Name	Description
10	PHY_MPM_HV_CLAMP_EN	Clamp enable for HV interrupts level shifters from USB VDD180 domain to VDDPAD MPM in usb2 phy wrapper. When set (1), VLS is active and HV interrupts are translated from 1.8V domain to MPM Vdd domain. When clear (0), VLS is clamped to inactive state. Default value is 1. SW should clear this bit before power collapse of 1.8V domain of PHY.
9	USB2_PHY_OTGSESSVLD HV_INTEN	Enable HV session valid interrupt from phy. This interrupt translated with level shifter for wakeup from retention when VDDCX is nominal and TCXO is running.
8	USB2_PHY_IDHV_INTEN	Enable HV id pin interrupt from phy. This interrupt translated with level shifter for wakeup from retention when VDDCX is nominal and TCXO is running.
7	USB2_PHY_ULPI_POR	Reset for ULPI PHY Wrapper and ULPI clock domain logic in usb2_phy_wrapper.
6:4	USB2_PHY_FSEL	Reference Clock Frequency Select 011 (Assumes 19.2MHz default)
3	HOST_PORTCTRL_FORCE _SUSEN	Chicken bit for CR-0000153908 - when this bit set the core will enter to low power mode when portctrl host sm enter to suspend mode. Default value is 1.
2	USB2_PHY_SIDDQ	IDDQ Test Enable.
1	USB2_PHY_RETEN	Retention mode enable/disable
0	USB2_PHY_POR	Power-On-Reset (Analog configuration needs to happen before POR is set to 0)

0x12530244 USB4_HS_USB_OTG_HS_GENERIC1

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

The USB_OTG_HS_GENERIC1 register.

USB4_HS_USB_OTG_HS_GENERIC1

Bits	Name	Description
31:16	USB_HS_TX_DEPTH	TX_DEPTH is the number of words in the TX buffer. This number is calculated by the number of bytes allocated per Endpoint divided by 4, times the number of endpoints. The RAM width is 36. In HS USB this value is usually 512 bytes per EP, and for FS ONLY USB it is usually 64 Bytes per EP.
15:0	USB_HS_RX_DEPTH	RX_DEPTH is the number of words in the RX buffer. This number is usually 256, but can support powers of 2 up to 4096. The RAM width is 36.

0x12530248 USB4_HS_USB_OTG_HS_GENERIC2

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0xXXXXXXXX

The USB_OTG_HS_GENERIC2 register.

USB4_HS_USB_OTG_HS_GENERIC2

Bits	Name	Description
31:16	RESERVED_BITS31_16	Clear (0) these bits.
15	USE_SPS_AHB2AHB	USE_SPS_AHB2AHB generic specifies if AHB2AHB bridge is connected between BAM and SPS Fabric AHB.
14	LPM_SUPPORT	The LPM_SUPPORT generic specifies if USB support Link Power Management.
13:9	USB_HS_DEV_EP	The number of USB endpoints. Valid values for the number of Endpoints are 4, 8, and 16
8:3	MAX_PIPES	The number of simultaneous parallel pipes supported by the BAM. Supported values are 2 to 30
2	USE_SPS	The USE_SPS generic specifies if Bam is connected to USB core.
1	USE_HSIC	The USE_HSIC generic specifies if an HSIC is connected to USB core.
0	UTMI_PHY_SW_IF_EN	The UTMI_PHY_SW_IF_EN generic specifies if UTMI phy Register Interface is enabled

0x12530250 USB4_HS_USB_OTG_HS_L1_EP_CTRL

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0000FFFF

The USB_OTG_HS_L1_EP_CTRL register enables/disables transition to L1 and exit from L1 state when specific TX endpoints are primed.

USB4_HS_USB_OTG_HS_L1_EP_CTRL

Bits	Name	Description
31:16	TX_EP_PRIME_L1_EXIT	Those bit's enables Remote Wakeup in L1 state when SW starts Priming The specific Endpoint.
15:0	TX_EP_PRIME_L1_EN	Control bit's that enables/disables transition to L1 when the specific TX Endpoint is active.

0x12530254 USB4_HS_USB_OTG_HS_L1_CONFIG

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x00000000

The USB_OTG_HS_L1_CONFIG register is used to configure various L1 features.

USB4_HS_USB_OTG_HS_L1_CONFIG

Bits	Name	Description
31:12	RESERVED_BITS31_12	Clear (0) these bits.
11	PLL_PWR_DWN_EN	Control bit that enables/disables power down of 480 MHZ PLL in L1 state.
10	PHY_LPM_EN	Control bit that enable/disables entering ULPI Low Power Mode in L1 state
9	GATE_AHB_CLK_EN	Control bit that enable/disables clock request signaling for usb_ahb_clk in L1 state
8	GATE_FS_XCVR_CLK_EN	Control bit that enable/disables clock gating of usb_fs_xcvr_clk in L1 state
7	GATE_SYS_CLK_EN	Control bit that enable/disables clock gating of usb_system_clk in L1 state
6	GATE_XCVR_CLK_EN	Control bit that enable/disables power-down of 480 MHz PLL in L1 state
5	L1_REMOTE_WAKEUP_EN	Control bit that enables/disables Remote Wakeup in L1 state. When this bit is low, then Link Controller never initiates Remote Wakeup in L1 state. When this bit is high, Link Controller can initiate Remote Wakeup.
4	LPM_EN	Control bit that enables/disables LPM support. When this bit is zero a full backward compatibility is ensured - no LPM support and no response for LPM Extended Transaction
3:0	PLL_TURNOFF_MIN_HIRD	Specifying a minimum expected HIRD value from Host that enables HW mechanism for turning off the 480 MHz PLL. The default value is 50us.

0x12530258 USB4_HS_USB_OTG_HS_LPM_DEBUG_1

Type: Read/Clear
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_DEBUG_1 register is for debug and testing purposes mostly.

USB4_HS_USB_OTG_HS_LPM_DEBUG_1

Bits	Name	Description
31:16	DEBUG_L1_LONG_ENT_CNT	Count number of exits from L1 where duration in L1 is > 200us. Writing to this register clears the counter.
15:0	DEBUG_L1_SHORT_ENT_CNT	Count number of exits from L1 where duration in L1 is <= 200us. Writing to this register clears the counter.

0x1253025C USB4_HS_USB_OTG_HS_LPM_DEBUG_2

Type: Read/Write
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_DEBUG_2 register is for debug and testing purposes mostly.

USB4_HS_USB_OTG_HS_LPM_DEBUG_2

Bits	Name	Description
31:13	RESERVED_BITS31_13	Clear (0) these bits.
12:9	L1_RMT_WKUP_TIME	Read/write Specifying How much time the device drives remote wakeup. The default Value is 50us for reset value. Add the value of this register (in us) to the remote wakeup time.
8	L1_FPR	Read/write L1 Force port resume, The software sets (1) this bit to drive resume signaling.
7	HSIC_CLK_PLL_BYPASSNL	Read only. Disables PLL analog logic. Active low. Connects to bypassnl input of NT_PLL.
6	HSIC_CLK_PLL_RESET	Read only. Resets all FF in PLL. Active low. Connects to reset_n input of NT_PLL.
5	HSIC_CLK_GATE	Read only. Clock gating of hsic_clk and ulpi_clk, without turning off HSIC PLL.
4	FS_XCVR_CLK_GATE	Read only. Clock gating of cc_usb_xcvr_fs_clk
3	SYS_CLK_GATE	Read only. Clock gating of cc_usb_system_clk
2	AHB_CLK_GATE	Read only. Clock gating of usb_ahb_clk

USB4_HS_USB_OTG_HS_LPM_DEBUG_2 (cont.)

Bits	Name	Description
1	L1_STATE	Read only. Status bit indicating if Device is in L1 state. When this bit high, Link Controller and HSIC PHY are in L1 state
0	DEBUG_L1_EN	Read/write Control bit that enable/disables DEBUG counters operation.

0x12530260 USB4_HS_USB_OTG_HS_LPM_ATTRIBUTES

Type: Read
Clock: CC_USB_OTG_HS_CLK
Reset State: 0x0

The USB_OTG_HS_LPM_ATTRIBUTES register store the bmAttribute Field of the LPM transaction.

USB4_HS_USB_OTG_HS_LPM_ATTRIBUTES

Bits	Name	Description
31:5	RESERVED_BITS31_5	Clear (0) these bits.
4	BREMOTEWAKE	A value of one (1B) in this field enables the addressed device to wake the host upon any meaningful application-specific event (e.g. an interrupt for a device with one or more interrupt endpoints). A value of zero (0B) disables the device from initiating remote wake.
3:0	HIRD	Host Initiated Resume Duration.

20.34 USB4 HS BAM Registers (0x12532000 USB4_HS_BAM_BASE)

This section contains the USB4 BAM registers.

BAM supports only Word (4 byte) aligned writes and reads on the Configuration Bus interface.

BAM has MAX_PIPES hardware generic parameter defining the number of pipes it supports. Each BAM can have up to 31 pipes supported.

BAM has BAM_CONF_AHBS_ADDR_WIDTH hardware generic parameter defining the Bit Number for selecting BAM access or Peripheral access. Legal Ranges are 14 to 20. Count starts from 1, meaning a value of 17 will set BAM Base address as 0x0001_0000.

20.34.1 BAM control registers

BAM Control registers configure the BAM operational state, SW reset, interrupts and others.

0x12532F80 USB4_HS_BAM_CTRL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

BAM Control register allows global controls for the BAM.

USB4_HS_BAM_CTRL

Bits	Name	Description
31:17	RESERVED_BITS31_17	Set to Zero (0)
16	IBC_DISABLE	This Bit enables power saving by disabling the inactivity clock timer/counter. This is useful when: 1) The BAM is Enabled but idling for long periods. 2) The BAM is Enabled and running but the inactivity timers/counters are not required by the SW for operating the BAM. When the BAM is Disabled, it automatically shuts down those timers to save power. 1’b1 - Enable Power Saving Mode 1’b0 - Disable Power Saving Mode

USB4_HS_BAM_CTRL (cont.)

Bits	Name	Description
15	BAM_CACHED_DESC_STORE	This Bit enables storage of a cached Descriptor into RAM when doing Context Switch and loading it back when returning to this pipe. This is relevant for System Modes Only. BAM to BAM Consumer mode doesn't have this option. Enabling this makes the Context Switch process slightly longer but reduces AHB Descriptor Fetch time later on. It also reduces the number of descriptor fetches done by the BAM if BAM is treating more than 2 pipes. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
14:13	BAM_DESC_CACHE_SEL	This Selector chooses which Descriptor Caching mode will be used. This is relevant for System Producer or Consumer modes only. 2’b00 - Cache when current descriptor has less than 64 bytes left. 2’b01 - Cache when current descriptor has less than 128 bytes left. 2’b10 - Immediate Auto cache - cache will happen whenever there are no descriptors cached. This might cause unnecessary descriptors reads when switching between more than 2 pipes. It is the most effective when each pipe processes more bytes than there are in an average descriptor (small descriptors, big block size), or when working with 2 or less pipes. 2’b11 - Cache when descriptor is needed only. This results in 1 descriptor present in cache at most. Available in BAM only
12	RESERVED_BITS12	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_SIC_SEL
11:5	BAM_TESTBUS_SEL	Set to Zero (0) Obsolete field: BAM_TESTBUS_SEL Test Bus selector. Supported until (including) bam_p3q3r29. Moved to a dedicated register - BAM_TEST_BUS_SEL in the following releases.
4	BAM_EN_ACCUM	When Enabled, BAM will accumulate data written by the peripheral in Direct Mode into INCR8 Bursts. This is an optimization feature for Producer Direct Mode cases. 1’b1 - Enabled 1’b0 - Disabled Available in BAM only
3	RESERVED_BITS3	Set to Zero (0)
2	RESERVED_BITS2	Set to Zero (0)

USB4_HS_BAM_CTRL (cont.)

Bits	Name	Description
1	BAM_EN	After reset the BAM wakes up in Disabled Mode. While Disabled, BAM operates in Legacy mode (all the transfers from the peripheral go around the BAM as if it doesn't exist) Software Enables this bit to allow BAM operation. This bit doesn't affect the PIPE enable bit in BAM_P_CTRL register. The only possibility to Disable the BAM after it has been enabled is by Hardware or Software reset. 1'b1 - Enabled 1'b0 - Disabled
0	BAM_SW_RST	This will reset the BAM & all Pipes. Software may use this to reset the BAM. As long as the bit remains high the BAM remains in reset state. Software should clear this bit 1'b1 - Reset state 1'b0 - Normal state

0x12532F84 USB4_HS_BAM_REVISION

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a hard coded revision number of the BAM RTL. This corresponds to the BAM target number in the IMS. Also additional BAM settings are reflected here.

USB4_HS_BAM_REVISION

Bits	Name	Description
31:24	INACTIV_TMR_BASE	This indicates the width of the inactivity timers base counter
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	NUM_INACTIV_TMRS	This bit is checked only if INACTIV_TMRS_EXST = 1. This bit indicates how many inactivity timers are implemented according to value of INACTIVITY_TIMERS_SUPPORTED generic: 1'b1 - One timer for global BAM activity (INACTIVITY_TIMERS_SUPPORTED = 1) 1'b0 - MAX_PIPES timers for each pipe activity (INACTIVITY_TIMERS_SUPPORTED = 2)
19	INACTIV_TMRS_EXST	This indicates BAM has inactivity timers. 1'b1 - Timers available (INACTIVITY_TIMERS_SUPPORTED = 1 or 2) 1'b0 - No timers available (INACTIVITY_TIMERS_SUPPORTED = 0)

USB4_HS_BAM_REVISION (cont.)

Bits	Name	Description
18	HIGH_FREQUENCY_BAM	This indicates BAM has Double Sampling on the Ack On Success interface. 1'b1 - Ack On Success double sampled 1'b0 - No double sampling of Ack On Success
17	BAM_HAS_NO_BYPASS	This field indicates BAM has no bypass on the AHB Data bus, from the Peripheral AHB Master to the fabric. When Bypass is available, it is the default routing when BAM is disabled. 1'b1 - No Bypass 1'b0 - Bypass Exists
16	SECURED	This field indicates BAM/BAM-Lite has security support (APU inside) 1'b1 - Secured 1'b0 - Not Secured
15:12	RESERVED_BITS15_12	Set to Zero (0)
11:8	NUM_EES	This indicates the Number of Interrupt Lines (Execution Environments) supported by the BAM. When 1 EE is supported, only the BAM_IRQ_SRCS*_EE0 registers exist. When 4 EEs are supported, all BAM_IRQ_SRCS*_EEn registers exist for n=[0..3].
7:0	REVISION	This field contains the revision number of the core, Hard Coded. 8'h01 - (bam_p3q3r22 +) 8'h02 - (bam_p3q3r27 +) 8'h03 - BAM (bam_p3q3r30 +) 8'h04 - BAM (bam_p3q2r43 +) 8'h05 - BAM (bam_p2q2r45 +) 8'h10 - BAM Lite (bam_lite_p1q1r0 +) 8'h11 - BAM Lite (bam_lite_p3q2r16 +) 8'h12 - BAM Lite (bam_lite_p2q2r18 +)

0x12532FBC USB4_HS_BAM_NUM_PIPES

Type: Read
Clock: BAM_CLK
Reset State: 0XUUUUUUUU

This Register holds a the hard coded number of pipes in the BAM. Since each BAM may have a different number of pipes instantiated in HW, this register allows the SW to know this parameter. The reset state value doesn't have any meaning in this register since it is a constant.

USB4_HS_BAM_NUM_PIPES

Bits	Name	Description
31:24	BAM_NON_PIPE_GRP	This field contains the number of BAM Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
23:16	PERIPH_NON_PIPE_GRP	This field contains the number of Peripheral's Non Pipe security groups (APU Entries). Zeroes when Non-Secured BAM
15:8	RESERVED_BITS15_8	Set to Zero (0)
7:0	BAM_NUM_PIPES	This field contains the number of pipes available in this BAM

0x12532FC0 USB4_HS_BAM_TIMER

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the BAM (all the pipes are in idle state).

USB4_HS_BAM_TIMER

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12532FC4 USB4_HS_BAM_TIMER_CTRL

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The register can be written and read only when INACTIVITY_TIMERS_SUPPORTED generic equals to 1.

The resolution of the BAM inactivity timer are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define

the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * TIMER_TRSHLD.

USB4_HS_BAM_TIMER_CTRL

Bits	Name	Description
31	TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1 to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	TIMER_RUN	Will be used along with TIMER_MODE Not implemented at this time. Set to zero(0)
29	TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12532F88 USB4_HS_BAM_DESC_CNT_TRSHLD

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds a threshold value for the counter summing the Size of the Descriptors Provided. This value is Global for all pipes but it is relevant for System Producer BAM mode and Both Consumer modes, where Descriptors summing takes place in order to provide the information to the peripheral via pipe bytes free (producer) or pipe bytes available interfaces.

USB4_HS_BAM_DESC_CNT_TRSHLD

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0).
15:0	CNT_TRSHLD	Threshold value. The maximum allowed value is 32kByte. Available in BAM only

0x12532F8C USB4_HS_BAM_IRQ_SRCS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking out this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register points to the physical BAM_IRQ_SRCS_EE0 register.

USB4_HS_BAM_IRQ_SRCS

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12532F90 USB4_HS_BAM_IRQ_SRCS_MSK

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register points to the physical BAM_IRQ_SRCS_MSK_EE0 register.

USB4_HS_BAM_IRQ_SRCS_MSK

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12532FB0 USB4_HS_BAM_IRQ_SRCS_UNMASKED

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register points to the physical BAM_IRQ_SRCS_UNMASKED_EE0 register.

USB4_HS_BAM_IRQ_SRCS_UNMASKED

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

0x12532F94 USB4_HS_BAM_IRQ_STTS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only.

Clearing the interrupt bits is done by writing to BAM_IRQ_CLR register.

USB4_HS_BAM_IRQ_STTS

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
3	BAM_EMPTY_IRQ	This interrupt is for DEBUG purpose only. It should not be used in normal SW flows. The interrupt indicates the BAMs buffer is empty. This bit can become high only when BAM_DATA_ERASE or BAM_DATA_FLUSH is high in BAM_TEST_BUS_SEL register.
2	BAM_ERROR_IRQ	This Indicates a Fatal Error has happened in the BAM. Currently this might happen due to an UnSuccessful Pipe Reset operation.

USB4_HS_BAM_IRQ_STTS (cont.)

Bits	Name	Description
1	BAM_HRESP_ERR_IRQ	This interrupt Indicates that an Erroneous HResponse has been received by the AHB Master. Additional Information about the error may be read at BAM_AHB_MASTER_ERR_* Registers. Clearing this interrupt also clears the BAM_AHB_MASTER_ERR_* Registers. Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12532F98 USB4_HS_BAM_IRQ_CLR

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

USB4_HS_BAM_IRQ_CLR

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
3	BAM_EMPTY_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM-Lite only
2	BAM_ERROR_CLR	1'b1 - Clear 1'b0 - Unchanged
1	BAM_HRESP_ERR_CLR	1'b1 - Clear 1'b0 - Unchanged Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12532F9C USB4_HS_BAM_IRQ_EN

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the BAM Interrupt Status register.

USB4_HS_BAM_IRQ_EN

Bits	Name	Description
31:5	RESERVED_BITS31_5	Set to Zero (0)
4	BAM_TIMER_EN	Enables Inactivity timer interrupt by writing this bit 1'b1 - Enable 1'b0 - Disable
3	BAM_EMPTY_EN	1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
2	BAM_ERROR_EN	1'b1 - Enable 1'b0 - Disable
1	BAM_HRESP_ERR_EN	1'b1 - Enable 1'b0 - Disable Available in BAM only
0	RESERVED_BITS0	Set to Zero (0)

0x12532FA0 USB4_HS_BAM_RESERVED_1

Type: Read
Clock: BAM_CLK
Reset State: 0x00000000

USB4_HS_BAM_RESERVED_1

Bits	Name	Description
31	RESERVED_BITS31	Set to Zero (0) Obsolete field: BAM_IRQ_SIC_SEL
30:0	RESERVED_BITS30_0	Set to Zero (0) Obsolete field: P_IRQ_SIC_SEL

0x12532FA4 USB4_HS_BAM_AHB_MASTER_ERR_CTRLS

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

USB4_HS_BAM_AHB_MASTER_ERR_CTRLS

Bits	Name	Description
31:23	RESERVED_BITS31_16	Set to Zero (0)
22:18	BAM_ERR_HVMID	HVMID
17	BAM_ERR_DIRECT_MODE	DIRECT MODE
16:12	BAM_ERR_HCID	HCID
11:8	BAM_ERR_HPROT	HPROT
7:5	BAM_ERR_HBURST	HBURST
4:3	BAM_ERR_HSIZE	HSIZE
2	BAM_ERR_HWRITE	HWRITE
1:0	BAM_ERR_HTRANS	HTRANS

0x12532FA8 USB4_HS_BAM_AHB_MASTER_ERR_ADDR

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

USB4_HS_BAM_AHB_MASTER_ERR_ADDR

Bits	Name	Description
31:0	BAM_ERR_ADDR	HADDR

0x12532FAC USB4_HS_BAM_AHB_MASTER_ERR_DATA

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the information about the data error in the AHB Buffer during bus Access.

The value stored is the value of the first error occurred.

Clear the BAM_HRESP_ERR_IRQ interrupt to clear the recorded error.

Available in BAM only

USB4_HS_BAM_AHB_MASTER_ERR_DATA

Bits	Name	Description
31:0	BAM_ERR_DATA	HDATA

0x12532FB4 USB4_HS_BAM_RESERVED_2

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

USB4_HS_BAM_RESERVED_2

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_IRQ_DEST_ADDR

0x12532FB8 USB4_HS_BAM_RESERVED_3

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

USB4_HS_BAM_RESERVED_3

Bits	Name	Description
31:0	RESERVED_BITS31_0	Set to Zero (0) Obsolete field: BAM_PERIPH_IRQ_DEST_ADDR

0x12532FF0 USB4_HS_BAM_TRUST_REG

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside - SECURED field in the BAM_REVISION register) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29.

USB4_HS_BAM_TRUST_REG

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_VMID	Those bits indicate the VMID value to be used when performing BAM type accesses to the bus. BAM Type accesses include BAM MTI (or Direct Mode accesses, not applicable for BAM Lite)
7	BAM_RST_BLOCK	When enabled, the BAM Global SW reset will not be available for usage. This is in order to deny Global SW reset requests by the Global security group. 1'b1 - Enable 1'b0 - Disable
6:2	RESERVED_BITS6_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_EE	This Field Indicates the EE (0,1,2,3) to which the BAM Interrupt belongs to. The pipe interrupts will fire on the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12532FF4 USB4_HS_BAM_TEST_BUS_SEL

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This is the testbus selector register.

Supported in releases after bam_p3q3r29.

USB4_HS_BAM_TEST_BUS_SEL

Bits	Name	Description
31:19	RESERVED_BITS31_19	Set to Zero (0)
18	BAM_DATA_ERASE	When enabled, BAM will be instructed to erase all the data it currently has inside. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Erase 1'b0 - Disabled
17	BAM_DATA_FLUSH	When enabled, BAM will be instructed to flush all the data it currently has inside. BAM will only flush the data once it has enough data and a valid destination for it. This is a DEBUG feature and should not be used in normal SW flows. Use with extreme care after consulting with HW representative. BAM_IRQ_STTS register has an interrupt bit indicating the BAM has no data buffered inside. 1'b1 - Enable Flush 1'b0 - Disabled
16	BAM_CLK_ALWAYS_ON	This bit controls the BAM to issue 'always on' clock request. 1'b1 - Enable Always On clock request. 1'b0 - Disabled
15:7	RESERVED_BITS15_7	Set to Zero (0)
6:0	BAM_TESTBUS_SEL	Test Bus selector. Values with bit[11] set high are reserved for the BAM Lite integrator to provide testbus from outside of the BAM Lite. For example, eDML testbus may reside at X'100_0000' to X'111_1111' selector values. eDML has no registers thus has no test bus selector, so its test bus is combined with the BAM lite's. BAM provides zeroes on its testbus when external values selected. X'000_0000' - Zeros X'000_0001' - Slave test bus X'000_0010' - Pipe state machine test bus X'000_0011' - Buffer test bus X'000_0100' - Sideband test bus X'000_1101' - Bus Manager test bus X'001_0000' - Reg file test bus X'1''_''''' - BAM Lite sets zeroes on the test bus, leaving it for external use

0x12532FF8 USB4_HS_BAM_TEST_BUS_REG

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the value being output to the testbus of the chip. It is not intended for SW usage but for lab debugging of the BAM. Values here can change every cycle.

USB4_HS_BAM_TEST_BUS_REG

Bits	Name	Description
31:0	BAM_TESTBUS_REG	32 bit Testbus value. To select the Block in BAM to show here, use the BAM_TESTBUS_SEL field in BAM_CTRL register.

0x12532FFC USB4_HS_BAM_CNFG_BITS

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM configuration bits for bug fixes. It is highly recommended to follow the directions for each bit and set it accordingly.

USB4_HS_BAM_CNFG_BITS

Bits	Name	Description
31:27	RESERVED_BITS31_27	Set to Zero (0)
26	BAM_AU_ACCUMED	Recommended value: 1 This bit fixes a bug in the Ack Update state machine, where an overflow happened while counting descriptors and reaching more than 64kB of calculated sizes. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only
25	BAM_PSM_P_HD_DATA	Recommended value: 1 This bit allows pipe state machine to ignore retransmission requests if a pipe has just been initialized and process those as a regular fetch request. (consumer modes only). When this bit disabled, BAM could fetch descriptors for a pipe which was reset and no descriptors were added yet, if a retransmission request followed after the reset. 1’b1 - Enable Fix 1’b0 - Disable Available in BAM only

USB4_HS_BAM_CNFG_BITS (cont.)

Bits	Name	Description
24	BAM_REG_P_EN	Recommended value: 1 This bit fixes the pipe configuration signals mux for the current active pipe in 2 pipes BAM. When disabled, internal state machines might get into enabled states while the pipe is disabled. This would typically happen after pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
23	BAM_WB_DSC_AVL_P_RST	Recommended value: 1 This bit allows the Writeback state machine to reset the vector indicating there are available descriptors when a pipe reset occurs. If disabled, BAM might fetch descriptors after resetting and reconfiguring a pipe, even though no Event (descriptors) was provided.. 1’b1 - Enable 1’b0 - Disable Available in BAM only
22	BAM_WB_RETR_SVPNT	Recommended value: 1 This bit fixes a bug where a pipe which was reset, still stored its retransmission savepoint, but into the illegal’s pipe address space, thus hurting the last pipe of the BAM if the BAM had a total 4, 8 or 16 pipes. This is relevant for Producer to System modes only. (CR-0000151585) 1’b1 - Enabled 1’b0 - Disable Available in BAM only
21	BAM_WB_CSW_ACK_IDL	Recommended value: 1 This bit allows the Writeback state machine to switch into idle state prior to visiting disabled state. This is needed when context switching from mode X to another pipe of mode X is well. This is required to fix a bug in the 2 pipes BAM. 1’b1 - Enable 1’b0 - Disable Available in BAM only
20	BAM_WB_BLK_CSW	Recommended value: 1 When Enabled, this bit does not allow context switch to happen in the Writeback state machine until it has created a descriptor. This is relevant when the descriptor fifo is becoming full and there’s no space to create a descriptor, while another pipe is context switching. This might result in the descriptor not to be created ever, if it was the last one for that pipe. Relevant for Producer BAM-to-BAM mode only. 1’b1 - Enable 1’b0 - Disable Available in BAM only

USB4_HS_BAM_CNFG_BITS (cont.)

Bits	Name	Description
19	BAM_WB_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Writeback state machine when performing pipe reset. 1’b1 - 1’b0 - Disable Available in BAM only
18	BAM_SI_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Sideband Inform state machine when performing pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
17	BAM_AU_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Ack Update state machine when performing pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
16	BAM_PSM_P_RES	Recommended value: 1 This bit allows to reset all internal registers of the Pipe state machine when performing pipe reset. 1’b1 - Enable 1’b0 - Disable Available in BAM only
15	BAM_PSM_CSW_REQ	Recommended value: 1 This bit forces the context switch request from pipe state machine to RAM controller not to last longer than the slave requested. (2 Pipes BAM bug fix) 1’b1 - Enable 1’b0 - Disable Available in BAM only
14	BAM_SB_CLK_REQ	Recommended value: 1 This bit allows the clock request from the sideband block to propagate into the BAM’s common clock request. 1’b1 - Propagate Sideband Clock Request 1’b0 - Disable Available in BAM only
13	BAM_IBC_DISABLE	Recommended value: 1 This bit helps to save power by allowing the BAM to keep the inactivity base counter in reset when BAM is disabled or when SW configures IBC_DISABLE bit high. 1’b1 - Enable Power Saving 1’b0 - Disable Power Saving

USB4_HS_BAM_CNFG_BITS (cont.)

Bits	Name	Description
12	BAM_NO_EXT_P_RST	Recommended value: 1 This bit allows the BAM / BAM Lite to ignore the externally connected blocks (eDML) when doing pipe reset. The BAM, once instructed to pipe reset, first thing lets the externally connected block know a reset is needed. Then it waits for the externally connected block to Acknowledge it is ready for the pipe reset (meaning it doesn't push any data for the reset pipe) and then the BAM Lite completes the pipe reset operation internally. When disabled, the BAM doesn't require any Acknowledge from the external block to perform pipe reset. 1’b1 - Enable external block pipe reset 1’b0 - Disable - ignore external block pipe reset
11	BAM_FULL_PIPE	Recommended value: 0 This enables the BAM support for a BAM to BAM Producer which insists to write to a full pipe. When 0, BAM might issue data overflow if producers write to a full pipe. When 1 BAM will not allow this and lower HReady when peripheral tries to do so. Once space is freed in the pipe, Hready will rise and the flow will continue. This functionality has been found to be buggy and was removed from APQ8064. Bit is currently unused. 1’b1 - Enable 1’b0 - Disable Available in BAM only
10:4	RESERVED_BITS10_4	Set to Zero (0)
3	BAM_ADML_SYNC_BRIDGE	0x1: Use a Synchronous Configuration bridge in aDML. 0x0: Use a Asynchronous Configuration bridge in aDML.
2	BAM_PIPE_CNFG	Recommended value: 1 Pipe SM upgrade for writing EOT bit to the previous descriptor. It’s invoked only when EOB arrives in the end of a descriptor. It is highly recommended to set this bit high. Leaving it low might cause incorrect Pipe Bytes Free value reported to peripheral in rare cases. 1’b1 - Enable 1’b0 - Disable Available in BAM only
1	BAM_ADML_DEEP_CONS_FIFO	0x1: Use a deep Consumer FIFO in aDML (16 dwords) 0x0: Use a shallow Consumer FIFO in aDML (8 dwords)
0	BAM_ADML_INCR4_EN_N	0x1: Don’t allow INCR4 aDML-BAM accesses. 0x0: Allow INCR 4 aDML-BAM accesses.

0x12533800+ 128*n USB4_HS_BAM_IRQ_SRCS_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Interrupt Status Register provides a single interrupt bit per each pipe in the BAM and a single bit for the BAM (not pipe related) interrupt. This register is read only and provides fast indication for the software to decide which pipe triggered the interrupt. After checking this register, SW reads the BAM_P_IRQ_STTSn register for the pipe interrupt reason and BAM_IRQ_STTS for the BAM interrupt reason.

This register has an alias - BAM_IRQ_SRCS register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

USB4_HS_BAM_IRQ_SRCS_EEn

Bits	Name	Description
31	BAM_IRQ	BAM Global interrupt
30:0	P_IRQ	An interrupt bit per each pipe in the BAM.

0x12533804+ 128*n USB4_HS_BAM_IRQ_SRCS_MSK_EEn, n=[0..3]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Interrupt Sources Mask register allows to mask the interrupts by their source, whether BAM or a specific pipe.

This register has an alias - BAM_IRQ_SRCS_MSK register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

USB4_HS_BAM_IRQ_SRCS_MSK_EEn

Bits	Name	Description
31	BAM_IRQ_MSK	BAM Global Interrupt Mask 0x1: Enable BAM interrupt 0x0: Disable BAM interrupt
30:0	P_IRQ_MSK	An Interrupt Mask bit per each pipe in the BAM. 0x1: Enable Pipe interrupt 0x0: Disable Pipe interrupt

0x12533808+ 128*n USB4_HS_BAM_IRQ_SRCS_UNMASKED_EEn, n=[0..3]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

The register shows the interrupts sources like (BAM_IRQ_SRCS) although the interrupts from the BAM and the pipes are not masked on the lower level.

This register has an alias - BAM_IRQ_SRCS_UNMASKED register.

Registers with n=[1..3] exist only when the BAM supports multiple EEs (NUM_EES field in the BAM_REVISION register).

USB4_HS_BAM_IRQ_SRCS_UNMASKED_EEn

Bits	Name	Description
31	BAM_IRQ_UNMASKED	BAM Global Interrupt after Mask
30:0	P_IRQ_UNMASKED	An Interrupt bit per each pipe in the BAM, after Mask

20.34.2 BAM PIPE management registers

BAM Pipe management registers control each pipe's parameters. Those reside in physical registers.

0x12532000+ 128*n USB4_HS_BAM_P_CTRLn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Control register provides various controls for the pipe.

USB4_HS_BAM_P_CTRLn

Bits	Name	Description
31:11	RESERVED_BITS31_11	Set to Zero (0)
10:9	P_PREFETCH_LIMIT	Bam Lite feature Selects the number of bytes to be pre-fetched by the Bam Lite, once a peripheral requests to read data from a pipe. This feature is relevant for Consumer modes only. 2'b00 - 32 bytes at most (INCR8) 2'b01 - 16 bytes at most (INCR4) 2'b10 - 4 bytes at most (SINGLE) Available in BAM-Lite only

USB4_HS_BAM_P_CTRLn (cont.)

Bits	Name	Description
8:7	P_AUTO_EOB_SEL	Bam Lite feature. Selects the number of bytes to be processed before creating End Of Block indication internally by the BAM. See P_AUTO_EOB. Descriptors generated by this feature (bam to bam producer mode) will always be of the chosen size, unless an End Of Transfer, causes a smaller descriptor to be created. 2'b00 - 512 Bytes 2'b01 - 256 Bytes 2'b10 - 128 Bytes 2'b11 - 64 Bytes Available in BAM-Lite only
6	P_AUTO_EOB	BAM Lite feature. When Enabled, the BAM Lite will ignore any incoming End Of Block indications from the peripheral (if any). Instead, the BAM Lite will generate it's own End Of Block indications internally, every P_AUTO_EOB_SEL bytes. This feature is relevant for Producer Bam 2 Bam modes only. It is a must for peripherals which are not able to produce End Of Block indications. 1'b1 - Enable 1'b0 - Disable Available in BAM-Lite only
5	P_SYS_MODE	This bit sets the pipe to work in System Mode, where the Software is the second side of the pipe. 1'b1 - System mode. 1'b0 - BAM to BAM mode.
4	P_SYS_STRM	Streaming Enable. Relevant to System Producer BAM mode only.When enabled, BAM will not close descriptors with End Of Transfer notifications received from peripheral, but continue writing the data to the same descriptor. 1'b1 - Enable Streaming Mode 1'b0 - None-Streaming Mode
3	P_DIRECTION	This bit denotes pipe direction. 1'b1 - The pipe can be written (producer mode) 1'b0 - The pipe can be read (consumer mode)
2	RESERVED_BITS2	Set to Zero (0)
1	P_EN	1'b1 - Enable Pipe 1'b0 - Disable Pipe
0	RESERVED_BITS0	Set to Zero (0)

0x12532004+ 128*n USB4_HS_BAM_P_RSTn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Reset register provides Pipe Reset ability. Software needs to write 1 to this register to make the Pipe Reset. Writing 0 to this register will finish the Pipe Reset. Writing zero is needed prior to Peripheral reconfiguration for the same pipe.

USB4_HS_BAM_P_RSTn

Bits	Name	Description
31:1	RESERVED_BITS31_1	Set to Zero (0)
0	P_SW_RST	This resets the pipe and its' registers, (Both Flip-Flops and RAM). 1'b1 - Reset 1'b0 - Do Nothing

0x12532008+ 128*n USB4_HS_BAM_P_HALTn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Halt register Enables/Disables the Halt Sequence.

This is a self-modifying register.

USB4_HS_BAM_P_HALTn

Bits	Name	Description
31:2	RESERVED_BITS31_2	Set to Zero (0)
1	P_PROD_HALTED	This bit is used to inform the Consumer about the Producer being in Halt mode now. This is a part of the Halt procedure. 1'b1 - Sets this bit to 1 1'b0 - Does Nothing This bit will be cleared by the HW.
0	P_HALT	When Enabled, the Pipe will enter Halt Mode. 1'b1 - Enable Halt 1'b0 - Disable Halt For B2B Producer pipes, this bit is self modifying. It doesn't need the SW to clear it.

0x12532030+ 128*n USB4_HS_BAM_P_TRUST_REGn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register holds the BAM Trusted configurations. The BAM APU needs to protect this register at the highest security level.

This register cannot be reset by any SW reset. Only HW reset applies. When using a secured BAM (APU integrated inside) it is reset by the XPU HW Reset. When using a non-secured BAM, it is reset by the BAM HW Reset.

Supported in releases after bam_p3q3r29.

USB4_HS_BAM_P_TRUST_REGn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:13	RESERVED_BITS15_13	Set to Zero (0) Reserved for possible BAM_VMID field expansion
12:8	BAM_P_VMID	Those bits indicate the VMID value to be used when performing Pipe type accesses to the bus. BAM Type accesses include Pipe MTI, Data and Descriptors.
7:2	RESERVED_BITS7_2	Set to Zero (0). Reserved for BAM_EE field expansion
1:0	BAM_P_EE	This Field Indicates the EE (0,1,2,3) to which the Pipe Interrupt belongs to. The BAM interrupt will fire to the EE set at BAM_P_TRUST_REGn registers. The number of supported EEs is reflect in the NUM_EES field in the BAM_REVISION register. 2'b00 - EE0 2'b01 - EE1 2'b10 - EE2 2'b11 - EE3

0x12532010+ 128*n USB4_HS_BAM_P_IRQ_STTSn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

Pipe Interrupt status register describing the reason for the ongoing interrupt. This is an informative only register and therefore read only. It also has informative bits which are not interrupts.

Clearing the interrupt bits is done by writing to P_IRQ_CLR register.

USB4_HS_BAM_P_IRQ_STTSn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_IRQ	For producer this interrupt happens whenever the last AHB burst of a transfer happens For Consumer when ack_on_success closes a transfer
4	P_ERR_IRQ	Pipe Error interrupt indicates that an error has happened. TBD: Error reason is not yet defined. Interrupt not in use.
3	P_OUT_OF_DESC_IRQ	Out of descriptors interrupt has several meanings depending on the operation mode: Producer - no free space in the descriptors fifo for adding a descriptor Consumer - no descriptors in the descriptors fifo for processing IO Vectors Producer - No descriptors to read (and therefore no space for data to write to the pipe) IO Vectors Consumer - No descriptors to read (and therefore no data to read from pipe)
2	P_WAKE_IRQ	Wake peripheral interrupt signals the driver to wake up the peripheral (USB for example) for transmission via the current pipe. This interrupt is issued whenever an Event comes to the specific pipe.
1	P_TIMER_IRQ	Inactivity timer has reached its threshold value Interrupt
0	P_PRCSD_DESC_IRQ	This Interrupt rises when BAM finishes processing an IO Vector which has INT bit selected

0x12532014+128*n USB4_HS_BAM_P_IRQ_CLRn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

Writing to this register causes the interrupt to clear.

USB4_HS_BAM_P_IRQ_CLRn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_CLR	1’b1 - Clear 1’b0 - Unchanged
4	P_ERR_CLR	1’b1 - Clear 1’b0 - Unchanged
3	P_OUT_OF_DESC_CLR	1’b1 - Clear 1’b0 - Unchanged

USB4_HS_BAM_P_IRQ_CLRn (cont.)

Bits	Name	Description
2	P_WAKE_CLR	Clear Wake peripheral interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
1	P_TIMER_CLR	Clear Inactivity timer interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged
0	P_PRCSD_DESC_CLR	Clear Descriptor Processed interrupt by writing this bit 1'b1 - Clear 1'b0 - Unchanged

0x12532018+ 128*n USB4_HS_BAM_P_IRQ_ENn, n=[0..30]

Type: Read/Write
Clock: BAM_CLK
Reset State: 0X00000000

Enable bits for the Interrupts in the Pipe Interrupt Status register.

USB4_HS_BAM_P_IRQ_ENn

Bits	Name	Description
31:6	RESERVED_BITS31_5	Set to Zero (0)
5	P_TRNSFR_END_EN	1'b1 - Enable 1'b0 - Disable
4	P_ERR_EN	1'b1 - Enable 1'b0 - Disable
3	P_OUT_OF_DESC_EN	1'b1 - Enable 1'b0 - Disable
2	P_WAKE_EN	Enable Wake peripheral interrupt 1'b1 - Enable 1'b0 - Disable
1	P_TIMER_EN	Enable Inactivity timer Interrupt 1'b1 - Enable 1'b0 - Disable
0	P_PRCSD_DESC_EN	Enable Descriptor Processed Interrupt 1'b1 - Enable 1'b0 - Disable

0x1253201C+ 128*n USB4_HS_BAM_P_TIMERn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This register counts the idle time of the pipe.

USB4_HS_BAM_P_TIMERn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TIMER	Inactivity timer counter. 16 bits = 64k*0.1ms

0x12532020+ 128*n USB4_HS_BAM_P_TIMER_CTRLn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register sets various controls and the threshold of the inactivity for interrupt triggering after long idle time.

The resolution of the pipe inactivity timers are in units set by a common counter. This common counter is controlled by GENERIC values to the BAM, and uses a separate clock, the nactivity_timers_clk.This clock can be slower than the bam_clk. The intent of the design is to use the sleep_clk, which is an always on 32 KHz clock. This allows the bam_clk to be turned off, while the base counter keeps counting. The width of this counter, as well of the rollover value are set using BAM GENERIC inputs. These values, taking the inactivity_timers_clk frequency define the pulse frequency that the base counter gives, and the threshold value can be calculated and set to interrupt after a specific time, regardless of the bam_clk frequency, and independent of clock power save features of the bam_clk. The timers continue counting even if the clock is turned off due to BAM dynamic hardware clock request voting

The timer configuration is based on the inactivity_timers_clk period and the INACTIVITY_TIMER_WIDTH generic constant. These parameters should be taken into account when setting this register. For example for inactivity_timer_clk period is 1us and the generic is 3 and the P_TIMER_THRSHLD is 10 will indicate the 2^3*1us*10 which is 80us of inactivity in a pipe before sending an interrupt. The general formula is 2^INACTIVITY_TIMER_WIDTH * clock period * P_TIMER_TRSHLD.

USB4_HS_BAM_P_TIMER_CTRLn

Bits	Name	Description
31	P_TIMER_RST	To begin using the inactivity timer the SW should write the threshold and write 1to this bit. writing the value 0 will hold the timer reset until value 1 is written again. Then the timer will start down counting from the P_TIMER_THRESOLD value 1'b1 - Active 1'b0 - Reset
30	P_TIMER_RUN	Will be used along with P_TIMER_MODE Not implemented at this time. Set to zero(0)
29	P_TIMER_MODE	Not implemented at this time. Set to zero(0)
28:16	RESERVED_BITS28_16	Set to zero(0)
15:0	P_TIMER_TRSHLD	Inactivity timer threshold for interrupt generation.

0x12532024+ 128*n USB4_HS_BAM_P_PRDCR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Producer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

USB4_HS_BAM_P_PRDCR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_producer
23:21	RESERVED_BITS23_21	Set to Zero (0)
20	BAM_P_TOGGLE	Pipe Bytes Free Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Free Ctrl value
15:0	BAM_P_BYTES_FREE	Pipe Bytes Free value

0x12532028+ 128*n USB4_HS_BAM_P_CNSMR_SDBNDn, n=[0..30]

Type: Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register reflects the current status of the Consumer Sideband interface as the peripheral sees it and some additional internal bits related to its management.

USB4_HS_BAM_P_CNSMR_SDBNDn

Bits	Name	Description
31:25	RESERVED_BITS31_25	Set to Zero (0)
24	BAM_P_SB_UPDATED	sideband_inform_bytes_avail_updated_consumer
23	BAM_P_WAIT_4_ACK	waiting_for_ack_bytes_avail_r
22	BAM_P_ACK_TOGGLE	ack_bytes_avail_toggle
21	BAM_P_ACK_TOGGLE_R	ack_bytes_avail_toggle_r
20	BAM_P_TOGGLE	Pipe Bytes Avail Toggle value
19:16	BAM_P_CTRL	Pipe Bytes Avail Ctrl value
15:0	BAM_P_BYTES_AVAIL	Pipe Bytes AVAIL value

20.34.3 BAM PIPE configuration registers (RAM)

BAM Pipe management registers configure each pipes' parameters.

Pipe Address span: currently defining each pipe to have 32 addresses, therefore inter pipe offset is 32*4=128=0x80 bytes.

0x1253302C+64*n USB4_HS_BAM_P_EVNT_DEST_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Event Destination Address which is the address of BAM_P_EVNT_REG in the BAM on the other side of the Pipe.

Producer BAM will send Write Events to this address.

Consumer BAM will send Read Events to this address.

This is relevant only for BAM to BAM modes. In System modes, BAM doesn't issue Write/Read events.

USB4_HS_BAM_P_EVNT_DEST_ADDRn

Bits	Name	Description
31:0	P_EVNT_DEST_ADDR	Address of the Event Register in the peer BAM (second end of the pipe). Driver will configure this when initializing the pipe.

0x12533018+64*n USB4_HS_BAM_P_EVNT_REGn, n=[0..30]

Type: Write
Clock: BAM_CLK
Reset State: 0X00000000

This Register is where Read/Write events are sent to. If current BAM works as Producer, it will receive Read events into this register from the Consumer. If the Consumer is another BAM, it will write read events to this register. If the Consumer is the Software, it will prepare descriptors in the descriptor FIFO and update the DESC_FIFO_PEER_OFST value in this register.

If current BAM works as Consumer, opposite behavior is assumed.

USB4_HS_BAM_P_EVNT_REGn

Bits	Name	Description
31:16	P_BYTES_CONSUMED	This field is used only in the B2B mode. It indicates the number of bits consumed by the Consumer. Consumer sends this value to the Producer as a part of a read event, for the Producer to know how many bytes were consumed. When working in System mode, this value should be set to zero. BAM to BAM Producer writes zero in this value.
15:0	P_DESC_FIFO_PEER_OFST	This field indicates the Descriptor Fifo Offset Pointer of the Peer BAM (The BAM or the Software which creates descriptors). For example when current BAM works as consumer for the current pipe, Producer BAM (or the software) updates this value to let the current pipe know about the new descriptors added in the Descriptor Fifo.

0x12533000+64*n USB4_HS_BAM_P_SW_OFSTSn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register denotes the pointer Offset of the first Not Acknowledged Descriptor. Meaning all Descriptors prior to this one have been processed by the BAM. This register is only used by the Software. After receiving an interrupt, software reads this register in order to know what descriptors has been processed.

When the BAM works as Producer, Software will usually read this value after Descriptor Processed Interrupt or after the End of Transfer Interrupt.

When the BAM works as Consumer, Software will usually read this value after Descriptor Processed Interrupt.

NOTE This is non relevant in BAM to BAM modes.

NOTE Although being Writable, Software should never write to this register.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB4_HS_BAM_P_SW_OFSTSn

Bits	Name	Description
31:16	SW_OFST_IN_DESC	Offset inside the Descriptor. This value is used by the Software only when a BAM is working as System Producer. Then the SW can read this value to know how many Bytes were written to the current descriptor if it was not closed down. This is useful for Streaming mode.
15:0	SW_DESC_OFST	Descriptor FIFO offset.

0x12533024+ 64*n USB4_HS_BAM_P_DATA_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Beginning of the Data Address space.

This register is non relevant in System Modes.

USB4_HS_BAM_P_DATA_FIFO_ADDRn

Bits	Name	Description
31:0	P_DATA_FIFO_ADDR	Data Address Space beginning.

0x1253301C+ 64*n USB4_HS_BAM_P_DESC_FIFO_ADDRn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register stores the Address of the Descriptor Fifo beginning.

NOTE This register is used by all modes.

USB4_HS_BAM_P_DESC_FIFO_ADDRn

Bits	Name	Description
31:0	P_DESC_FIFO_ADDR	Address of the Descriptors Fifo. This address must be 8 bytes aligned.

0x12533028+64*n USB4_HS_BAM_P_EVNT_GEN_TRSHLDn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This register configures the threshold value for Read/Write event generation by the BAM towards another BAM. When a BAM pushes/pops this number of bytes to/from the pipe an event to the other BAM will be generated. A counter summing up the bytes pushed/popped is reset when event is issued, thus restarting count for the threshold.

Events are also issued after End Of Transfer received from the peripheral (Producer case), non regarding whether the pushed bytes count has reached the threshold or not.

This register is non relevant in System Modes.

USB4_HS_BAM_P_EVNT_GEN_TRSHLDn

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	P_TRSHLD	Threshold value. The maximum allowed value is 32kByte.

0x12533020+64*n USB4_HS_BAM_P_FIFO_SIZESn, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

The least significant field is the Descriptor Fifo Size.

The most significant field is the Data Fifo Size.

NOTE This Descriptor Fifo Size is used by all modes. The Data Fifo Size is non relevant in System Modes.

USB4_HS_BAM_P_FIFO_SIZESn

Bits	Name	Description
31:16	P_DATA_FIFO_SIZE	Size of the Data Address Space.
15:0	P_DESC_FIFO_SIZE	Size of the Descriptors Fifo. Must be 8 byte aligned. Each descriptor is 8 bytes. Size of the descriptor fifo must contain an integer number of Descriptors.

20.34.4 BAM PIPE internal state registers (RAM)

BAM Pipe debug registers allow a software look inside on the internal parameters of the BAM State Machines stored in RAM.

Those shouldn't be normally used or altered by the software.

0x12533034+64*n USB4_HS_BAM_P_RETR_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context stored for retransmission.

This is being stored by Ack Update state machine in consumer mode or by the Writeback state machine in producer mode.

This is being loaded by the Writeback state machine when retransmission happens.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB4_HS_BAM_P_RETR_CNTXT_n

Bits	Name	Description
31:16	RETR_DESC_OFST	Descriptor Fifo Offset for retransmission.
15:0	RETR_OFST_IN_DESC	The Offset inside the Descriptor for retransmission.

0x12533038+64*n USB4_HS_BAM_P_SI_CNTXT_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Sideband Inform state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB4_HS_BAM_P_SI_CNTXT_n

Bits	Name	Description
31:16	RESERVED_BITS31_16	Set to Zero (0)
15:0	SI_DESC_OFST	The Descriptor Fifo Offset pointer stored by the Sideband Inform state machine.

0x12533004+ 64*n USB4_HS_BAM_P_AU_PSM_CNTXT_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Ack Update state machine.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB4_HS_BAM_P_AU_PSM_CNTXT_1_n

Bits	Name	Description
31:16	AU_PSM_ACCUMED	PSM: The acknowledged (EOB/T) number of bytes since last Write Event. AU: The accumulation of the descriptor sizes for the present ack_on_success event. This is never bigger than the ACKED field. Once the ACCUMED values are bigger than Event Threshold, an Event will be issued, the ACKED value will decrease by the ACCUMED size and this value will be zeroed. This also serves as the Bytes Consumed value in the Event.
15:0	AU_ACKED	AU: The left over of the number of bytes that were received via the ack_on_success, that did not cause a descriptor closure. This value is down counting upon issuing Read Event. PSM:

0x12533008+ 64*n USB4_HS_BAM_P_PSM_CNTXT_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB4_HS_BAM_P_PSM_CNTXT_2_n

Bits	Name	Description
31	PSM_DESC_VALID	The Descriptor Valid bit provided by the Writeback state machine to Pipe state machine.
30	PSM_DESC_IRQ	The Descriptor Interrupt bit provided by the Writeback state machine to pipe state machine.
29	PSM_DESC_IRQ_DONE	The Descriptor Interrupt needed selection bit.
28:25	PSM_GENERAL_BITS	General Context Switch Bits
24:22	PSM_CONS_STATE	State of the Pipe Consumer state machine.
21:19	PSM_PROD_SYS_STATE	State of the Pipe Producer System state machine.
18:16	PSM_PROD_B2B_STATE	State of the Pipe Producer BAM to BAM state machine.
15:0	PSM_DESC_SIZE	The Descriptor Size provided by the Writeback state machine to pipe state machine.

0x1253300C+64*n USB4_HS_BAM_P_PSM_CNTXT_3_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB4_HS_BAM_P_PSM_CNTXT_3_n

Bits	Name	Description
31:0	PSM_DESC_ADDR	The Data Address provided in the current descriptor from the Writeback state machine.

0x12533010+64*n USB4_HS_BAM_P_PSM_CNTXT_4_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB4_HS_BAM_P_PSM_CNTXT_4_n

Bits	Name	Description
31:16	PSM_DESC_OFST	The running Descriptor Fifo Offset of the Writeback state machine
15:0	PSM_SAVED_ACCUMED_SIZE	The Saved Accumulated Size from the Pipe state machine.

0x12533014+64*n USB4_HS_BAM_P_PSM_CNTXT_5_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

Internal Context of Pipe & Writeback state machines.

NOTE When using 2 pipes BAM, REVISION 0x03, this registers is Read Only.

USB4_HS_BAM_P_PSM_CNTXT_5_n

Bits	Name	Description
31:16	PSM_BLOCK_BYTE_CNT	The Byte count inside the current Block.
15:0	PSM_OFST_IN_DESC	The Offset inside a register. This is used by pipe state machine to compute offset inside a register after retransmission

0x12533030+64*n USB4_HS_BAM_P_RESERVED_1_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

USB4_HS_BAM_P_RESERVED_1_n

Bits	Name	Description
31:0	BAM_P_RES_1	Set to zero (0) Reserved

0x1253303C+64*n USB4_HS_BAM_P_RESERVED_2_n, n=[0..30]

Type: Write/Read
Clock: BAM_CLK
Reset State: 0X00000000

This Register indicates reserved space.

USB4_HS_BAM_P_RESERVED_2_n

Bits	Name	Description
31:0	BAM_P_RES_2	Set to zero (0) Obsolete Register: BAM_P_IRQ_DEST_ADDRn, n=[0..30]

20.35 SPS GSBI1Registers (0x12440000 SPS_GSBI1_BASE)

This section contains GSBI 1 registers.

20.35.1 GSBI CTRL Registers

0x12440000 SPS_GSBI1_GSBI_CTRL_REG

Type: Read/write
Clock: HCLK
Reset State: 0x00000000

SPS_GSBI1_GSBI_CTRL_REG

Bits	Name	Description
15:12	RESERVED	reserved
11:8	WRAPPER_CTRL	This field has no predefined use. When a wrapper is constructed around one or more GSBIs there may be a need to configure it. E.g., to select which of several GSBIs will be connected to a particular I2S block. All bits of this field emerge from GSBI as output ports which can be used for any such configuration task.
7	RESERVED_7	Reserved. The host can write and read this field, but its state has no effect on anything.
6:4	PROTOCOL_CODE	This field controls which protocol, if any, is applied to the GSBI's four I/O ports. Most codes assign a single protocol, but codes of "001" and "110" assigns I2C to two of the ports and UART (without flow control signals) or SIM to the other two. 0x0: Idle (null values are applied to all four GSBI I/Os) 0x1: I2C on 2 ports, SIM/R-UIM on other 2 0x2: I2C 0x3: SPI 0x4: UART with flow control (or IRDA) 0x5: SIM/R-UIM 0x6: I2C on 2 ports, UART (without HS flow ctrl on other 2) 0x7: Undefined
3:1	RESERVED_3_1	Reserved. The host can write and read this field, but its state has no effect on anything.
0	CRCI_MUX_CTRL	While this bit is low QUP CRCI ports are connected to the GSBI ports nominally for QUP and UART_DM CRCI ports are connected to the GSBI ports nominally for UART_DM. While this bit is high QUP CRCI ports are connected to the GSBI ports nominally for UART_DM and UART_DM CRCI ports are connected to nothing.

0x12440004 SPS_GSBI1_GSBI_DBG0_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

SPS_GSBI1_GSBI_DBG0_REG

Bits	Name	Description
1:0	GSBI_PLAY0	This field has no function beyond the fact that the ARM can write to it and read from it.

0x12440008 SPS_GSBI1_GSBI_DBG1_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

SPS_GSBI1_GSBI_DBG1_REG

Bits	Name	Description
1:0	GSBI_PLAY1	This field has no function beyond the fact that the ARM can write to it and read from it.

0x1244000C SPS_GSBI1_GSBI_DBG2_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

SPS_GSBI1_GSBI_DBG2_REG

Bits	Name	Description
1:0	GSBI_PLAY2	This field has no function beyond the fact that the ARM can write to it and read from it.

0x12440010 SPS_GSBI1_GSBI_DBG3_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

SPS_GSBI1_GSBI_DBG3_REG

Bits	Name	Description
1:0	GSBI_PLAY3	This field has no function beyond the fact that the ARM can write to it and read from it.

20.36 SPS GSBI1 UART DM Registers (0x12450000 SPS_UART1_DM_BASE)

This section contains Smart Peripheral System GSBI 1 UART DM registers.

UART_DM registers are accessible only by the ARM

This section contains the read and write registers for UART1.

20.36.1 Write and read/write registers

0x12450000 SPS_GSBI1_UART_DM_MR1

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_MR1 register is the UART mode register 1. It is used, along with UART_DM_MR2, to configure the operational mode of the UART.

SPS_GSBI1_UART_DM_MR1

Bits	Name	Description
31:8	AUTO_RFR_LEVEL1	These bits are used, along with bits 5:0 (AUTO_RFR_LEVEL0) to program the level in the receive FIFO at which the RFR_N signal is de-asserted, if programmed to do so (see RX_RDY_CTL field of this register). The level counts the number of words inside the RX FIFO. It doesn't count the character that is being received (shift register) or characters in the packing buffer. This value is programmed from 1 to 2^RAM_ADDR_WIDTH. The RFR_N signal is de-asserted when the RX FIFO level (the number of characters remaining in the RX FIFO) is greater than the level that is programmed into this register. · Only RAM_ADDR_WIDTH +1:8 bits are generated.
7	RX_RDY_CTL	Setting (1) this bit enables the automatic ready-for-receiving (RFR_N) control for the receiver. RFR_N is turned off, or set (1), when a valid start bit is received and the channel FIFO is at the level programmed in bits 4 through 0 of this mode register. When the FIFO level falls back to the programmed level, the RFR_N signal is turned on, or clear (0). When this feature is off, the RFR_N signal can be used by normal signal port bit manipulation (see UART_DM_CR register).

SPS_GSBI1_UART_DM_MR1 (cont.)

Bits	Name	Description
6	CTS_CTL	When this bit is set(1), the transmitter checks the CTS_N input to determine whether to begin transmission of a new character. If CTS_N is low, the character is sent. Otherwise the transmitter continues marking until CTS_N goes low, then the next character is transmitted. A change on CTS_N during the transmission of a character has no effect on that character. When this bit is clear(0), the CTS_N input for the channel has no effect on the transmitter.
5:0	AUTO_RFR_LEVEL0	See the description of bit 8 (AUTO_RFR_LEVEL1).

0x12450004 SPS_GSBI1_UART_DM_MR2

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI1_UART_DM_MR2

Bits	Name	Description
9	RX_ERROR_CHAR_OFF	When this bit is asserted, characters with parity or framing errors don't enter RX FIFO. Otherwise they enter RX FIFO.
8	RX_BREAK_ZERO_CHAR_OFF	When this bit is asserted, the zero character received at rx_break doesn't enter RX FIFO. Otherwise it enters RX FIFO.
7	LOOPBACK	Internal use only
6	ERROR_MODE	This bit controls the operation of the two FIFO status bits for the channel (parity or framing error and received break). · When clear (0), the UART operates in character mode and the status bits apply only to the character at the top of the FIFO. · When set (1), the UART operates in block mode and both bits are the "OR" of the status for all previously received characters arriving after the last `reset error status' command was issued (see CR register).
5:4	BITS_PER_CHAR	These bits determine how many bits are transmitted or received per character, not including the start, stop, and parity bits. 0x0: 5 bits 0x1: 6 bits 0x2: 7 bits 0x3: 8 bits

SPS_GSBI1_UART_DM_MR2 (cont.)

Bits	Name	Description
3:2	STOP_BIT_LEN	This field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 9/16, 1, 1+ 9/16, and 2 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. 0x0: 0.563 (9/16 bit times) 0x1: 1.000 bit time 0x2: 1.563 (1+9/16 bit times) 0x3: 2.000 bit times
1:0	PARITY_MODE	These bits determine which parity mode is used. The user can select between odd, even, space, or no parity. 0x0: no parity 0x1: odd parity 0x2: even parity 0x3: space parity

0x12450008 SPS_GSBI1_UART_DM_CSR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_CSR register is the UART clock selection register. This register is used in conjunction with the UART M/N counter registers to determine the bit rate for the transmitter and receiver. The transmitter and receiver can be clocked at different rates.

The rates below are based on a uart_dm_clk rate of 1.8432 MHz (115.2 * 16).

Table 28-12 lists the hexadecimal values for the clock select field and the corresponding data rates.

Table 20-10 Hexadecimal values for clock select field and corresponding data rates

CLK SEL value	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Bit rate (b/sec)	75	150	300	600	1200	2400	3600	4800	7200	9600	14.4k	19.2k	28.8k	38.4k	57.6k	115.2k

SPS_GSBI1_UART_DM_CSR

Bits	Name	Description
7:4	UART_RX_CLK_SEL	Use the CLK SEL values in Table 28-12 to select the appropriate receive and transmit bit rates.
3:0	UART_TX_CLK_SEL	

0x12450070 SPS_GSBI1_UART_DM_TF

Type: Write
Clock: AHB_CLK
Reset State: Undefined

In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM TX FIFO.

SPS_GSBI1_UART_DM_TF

Bits	Name	Description
31:0	UART_TF	The UART_TF register is the UART transmit FIFO register. This register is used to access the channel transmit FIFO. If the FIFO is full at the time of writing, the character is lost and an interrupt is generated (see UART_DM_IMR register).

0x12450074 SPS_GSBI1_UART_DM_TF_2

Type: Write
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_TF_2

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x12450078 SPS_GSBI1_UART_DM_TF_3

Type: Write
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_TF_3

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x1245007C SPS_GSBI1_UART_DM_TF_4

Type: Write
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_TF_4

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x12450010 SPS_GSBI1_UART_DM_CR

Type: Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_CR register is the UART command register. This register is used to issue specific commands to the UART subsystem. This register is updated asynchronously.

CAUTION Do not reset the transmitter and disable it at the same time. Do not reset the receiver and disable it at the same time.

Table 20-11 UART DM command values

Value	Description	Result
0	Null command	Does nothing.
1	Reset receiver	Resets the receiver as if a hardware reset were issued. The receiver is disabled and the FIFO, packing buffer and shift registers are flushed.
2	Reset transmitter	Resets the transmitter as if a hardware reset were issued. The transmitter signal goes high (marking) and the FIFO, unpacking register and shift register are flushed.
3	Reset error status	Clears the overrun error and hunt char received status bits in both the character and block error modes. In the block error mode, it clears the error status and received break.
4	Reset break change interrupt	Clears the break change interrupt status bit.
5	Start break	Forces the transmitter signal low. The transmitter must be enabled. If the transmitter is busy, the break is started when all characters in the transmit FIFO and the transmit shift register have been completely sent.
6	Stop break	If executed while channel is breaking, this command causes the transmitter signal to go high. The signal remains high for at least one bit time before sending out a new character.
7	Reset CTS_N	Clears ISR bit 5.
8	Reset stale interrupt	Clears the stale interrupt.

Table 20-11 UART DM command values

Value	Description	Result
9	Packet mode	Turns on the sample data mode, which causes the receiver to sample the receive data stream at 16 times the programmed baud rate. The data is sampled with the start of the start bit, or the first data bit, and continued until the marking state. To exit this state, write 1100 in the command field.
A	test_parity_on	Internal use only.
B	test_frame_on	Internal use only.
C	Mode reset	Turns off the sample data mode.
D	Set RFR_N	Asserts the ready for receiving signal (active low).
E	Reset RFR_N	De-asserts the ready for receiving signal.
F	uart_reset_int	Internal use only.
10	Reset TX_ERROR	Clears TX_ERROR
11	Clear TX_DONE	Clears the TX_DONE interrupt (ISR bit 9)
12	Reset break start interrupt	Clears the break start interrupt status bit.
13	Reset break end interrupt	Clears the break end interrupt status bit.
14	Reset par_frame_err interrupt	Clears the par_frame_err interrupt status bit.

Table 20-12 UART DM command values

Value	Description	Result
0	Null command	Does nothing.
1	CR Protection Enable	Enables CR HW protection. When two consecutive writes to the CR are detected, the second write is delayed until the command of the first write is finished. The delay is done by de-asserting the AHB ready and this ensures that the first command completes and the second one will be executed right afterward.
2	CR Protection Disable	Disables CR HW protection. SW is responsible for managing delay between writes to the CR register.
3	Reset TX-Ready interrupt	Clears the TX_READY interrupt.
5	Enable Stale Event	Enables the `stale event' mechanism. See Software Procedures.
6	Disable Stale Event	Disables the `stale event' mechanism. See Software Procedures.
4	SW Force Stale	Causes a `stale event' (even if `stale event' is disabled). See Software Procedures.
7	RESERVED	

SPS_GSBI1_UART_DM_CR

Bits	Name	Description
11	CHANNEL_COMMAND_MSB	This is the msb of the CHANNEL_COMMAND bit field.
10:8	GENERAL_COMMAND	Writing the appropriate value to these bits executes the commands that are listed in Table.
7:4	CHANNEL_COMMAND_LSB	Writing the appropriate value to these bits along with bit 11,executes the commands that are listed in Table 28-13.
3	UART_TX_DISABLE	This command terminates the operation of the transmitter after any character in the transmit shift register is sent.
2	UART_TX_EN	This command enables the operation of the transmitter.
1	UART_RX_DISABLE	This command immediately terminates the operation of the channel receiver and any incoming characters are lost. None of the receiver status bits are affected by this command and characters that are already in the receive FIFO remain there.
0	UART_RX_EN	This command enables the channel receiver.

0x12450014 SPS_GSBI1_UART_DM_IMR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IMR register is the UART interrupt mask register. This register is used to enable the corresponding functions in the UART_DM_ISR register. Setting (1) a bit in the UART_DM_IMR register causes an interrupt to be generated, if the corresponding bit in the UART_DM_ISR register is set. Clearing (0) a bit in the UART_DM_IMR register causes the setting of the corresponding bit in the UART_DM_ISR register to have no effect on the interrupt signal.

Bit 6 of the UART_DM_IMR register, CURRENT_CTS, is slightly different. If the current value of the CTS is one (1), no interrupt is generated. However, the user can use bit 6 in this register to mask the CTS value when reading the UART_DM_MISR register or as a general-purpose bit.

SPS_GSBI1_UART_DM_IMR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	This bit is asserted in the same condition at which PAR_FRAME_ERR status bit is asserted. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x14.
11	RXBREAK_END	This bit is set (1) if the end of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x13.

SPS_GSBI1_UART_DM_IMR (cont.)

Bits	Name	Description
10	RXBREAK_START	This bit is set (1) if the start of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x12.
9	TX_DONE	This bit is used only in UIM/SIM_IF mode. Set (1) this bit when the last byte in the transmitter has been sent. · This bit is generated only when SIM_GLUE_GEN generic equals 1.
8	TX_ERROR	Only used in UIM_IF mode. Set (1) this bit to indicate that there has been parity error during transmission. To clear the detection logic associated with this function, write CR[11;7:4]=0x10. · This bit is generated only when SIM_GLUE_GEN generic equals 1.
7	TX_READY	This bit, when set(1), indicates that: 1. TX FIFO is empty. 2. The value written in NO_CHARS_FOR_TX register equals the number of bytes written to the TX FIFO since the register was updated. Note: There may be characters in the unpack buffer or in the shift register. This bit is cleared by issuing `clear TX ready' command (see UART_DM_CR register).
6	CURRENT_CTS	This bit indicates the current state of the CTS input. It never generates an interrupt.
5	DELTA_CTS	This bit, when set (1), indicates that the CTS input has changed states. To clear the detection logic associated with this function, write CR[7:4]=0x7.
4	RXLEV	This bit is set when a character is loaded into the receive FIFO that brings the total number of characters in the FIFO above the programmed watermark level in the FIFO watermark register (RFWR). This bit is cleared after enough characters have been read to bring the level equal to or below the programmed watermark level.
3	RXSTALE	This bit indicates that a `stale event' occurred. See Software procedures for the exact timing of this interrupt. It is cleared by issuing a reset-stale command (see CR register).
2	RXBREAK_CHANGE	This bit is set (1) if the start or end of a break condition is detected. The logic associated with this condition is cleared (0) by writing CR[7:4]=0x4. A detected break is defined as an all-zeros character with an invalid stop bit AND LOW PARITY. The end of a break is defined as a mark condition (1) at least 1/2 bit width. A detected break occupies one position in the Rx FIFO.
1	RXHUNT	This bit is set (1) when an incoming character matches the value programmed into the UART_DM_HCR register. This condition is cleared (0) by issuing a reset error status command (CR[7:4]=0x3).

SPS_GSBI1_UART_DM_IMR (cont.)

Bits	Name	Description
0	TXLEV	This bit is set (1) when a character which is transferred from the transmit FIFO to the transmit shift register brings the total number of characters in the FIFO below or equal to the programmed watermark level in the UART_DM_TFWR register. This bit is cleared (0) after enough characters have been written to the FIFO to bring the level above the programmed watermark level.

0x12450018 SPS_GSBI1_UART_DM_IPR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0xffffff9f

The UART_DM_IPR register is the UART interrupt programming register.

SPS_GSBI1_UART_DM_IPR

Bits	Name	Description
31:7	STALE_TIMEOUT_MSB	These bits are the STALE_TIMEOUT bit field. The stale character time-out duration field contains a number from 1 to 2^30 -1. This number determines how many character times must elapse before a `stale event' is generated. This character time is defined as 10 times the bit rate. It is reset whenever a data bit is received. Do not clear (0) this register if the stale character time-out interrupt is enabled. Note the discontinuity in the bit assignments.
6	SAMPLE_DATA	Setting (1) this bit enables the new sample data mode, which means that the start bit is sampled as well as the rest, when in sample data mode. See the CR register, CHANNEL_COMMAND bit for more information.
5	RESERVED	
4:0	STALE_TIMEOUT_LSB	This bit field is the LSbits of the STALE_TIMEOUT bit field.

0x1245001C SPS_GSBI1_UART_DM_TFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_TFWR register is the UART transmit FIFO watermark register.

SPS_GSBI1_UART_DM_TFWR

Bits	Name	Description
31:0	TFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the transmit FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of TX words in the FIFO) is less than or equal to the value in TFWR. See UART_DM_IMR register. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x12450020 SPS_GSBI1_UART_DM_RFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RFWR register is the UART receive FIFO watermark register.

SPS_GSBI1_UART_DM_RFWR

Bits	Name	Description
31:0	RFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the receive FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of words in the RX FIFO) is greater than the value in RFWR. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x12450024 SPS_GSBI1_UART_DM_HCR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI1_UART_DM_HCR

Bits	Name	Description
7:0	DATA	The UART_DM_HCR register is the UART hunt character register, which contains the character for which the receiver looks to assert a hunt character received interrupt.

0x12450034 SPS_GSBI1_UART_DM_DMRX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI1_UART_DM_DMRX

Bits	Name	Description
24:0	RX_DM_CRCI_CHARS	In the DM mode, the number of chars in the Rx FIFO that are used for CRCI handshake with the DM. The written value of RX_DM_CRCI_ CHARS must be a multiple of 16(bits [3:0] are treated as 0x0). After a value is written, the UART will generate CRCI requests as long as RX_DM_CRCI_CHARS is non zero. Read of DMRX register gives the number of characters that were received since the end of the last transfer. It is reset at the end of each Rx transfer Also is used by the software to indicate `transfer initialization'. See Software procedures.

0x12450038 SPS_GSBI1_UART_DM_IRDA

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IRDA register enables the IRDA function, selects a loopback, and allows inversion of RX and TX data. This register also controls the IRDA transceiver that optionally interfaces between the UART and the DP_RX_DATA and DP_TX_DATA pins.

The UART proper is a standard RX/TX configuration that converts the serial pin input and output lines to 8-bit data for the microprocessor. The configuration contains receive and transmit blocks, a control block, a bit rate generator for RX and TX, and FIFO interfaces with the microprocessor data bus. The IRDA register provides the means of switching IRDA circuits into the serial I/O lines and the IRDA function is normally switched out. The IRDA modulator/demodulator may be enabled or disabled under microprocessor control. When enabled, the RX and TX data paths have individual inversion select bits, so external true or inverted drivers may be used in the signal path.

- The register is generated only when IRDA_IFC_GEN generic equals 1.

SPS_GSBI1_UART_DM_IRDA

Bits	Name	Description
4	MEDIUM_RATE_EN	· Set (1) for 1/4 bit-time pulse length (Medium rate) · Clear (0) for 3/16 bit-time pulse length (Low rate)
3	IRDA_LOOPBACK	· This bit loops the IRDA modulated TX line back into the IRDA RX line. The normal UART loopback mode must be off in order to see this effect.

SPS_GSBI1_UART_DM_IRDA (cont.)

Bits	Name	Description
2	INVERT_IRDA_TX	This bit inverts the polarity of the IRDA modulated signal on the DP_TX_DATA pin. · Set (1) this bit for an inverted polarity. · Clear (0) this bit for a non-inverted polarity.
1	INVERT_IRDA_RX	This bit inverts the polarity of the IRDA received signal on the DP_RX_DATA pin. · Set (1) this bit for inverted the polarity. · Clear (0) this bit for non-inverted polarity.
0	IRDA_EN	· Set (1) this bit to enable the IRDA transceiver. · Clear (0) this bit to bypass the IRDA transceiver and ignore the other bits of this register.

0x1245003C SPS_GSBI1_UART_DM_DMEN

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_DMEN register indicates if Data Mover is enabled for TX and RX channels.

SPS_GSBI1_UART_DM_DMEN

Bits	Name	Description
1	RX_DM_EN	· Set (1) this bit to enable RX DM interface. · Clear (0) this bit to disable RX DM interface. Clearing this bit requires resetting the receiver (see UART_DM_CR register).
0	TX_DM_EN	Set (1) this bit to enable TX DM interface. Clear (0) this bit to disable TX DM interface.

0x12450040 SPS_GSBI1_UART_DM_NO_CHARS_FOR_TX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI1_UART_DM_NO_CHARS_FOR_TX

Bits	Name	Description
23:0	TX_TOTAL_TRANS_LEN	The total number of characters for transmission. Before writing a new value, the TX FIFO must be empty (as indicated by TX_READY interrupt in IMR register or after a reset). It is used by the transmitter to calculate how many characters to transmit in the last word. In DM mode, it is also used for the CRCI mechanism. Any additional writes to the TX FIFO above TX_TOTAL_TRANS_LEN will be discarded. A TX_READY interrupt is triggered after TX_TOTAL_TRANS_LEN number of characters were moved from the TX FIFO to the unpacking register (not all may have been sent).

0x12450044 SPS_GSBI1_UART_DM_BADR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_BADR

Bits	Name	Description
31:2	RX_BASE_ADDR	RX FIFO base address. Both FIFOs use the same RAM (2^RAM_ADDR_WIDTH, 32-bit entries). This register controls the division of the memory to the RX and TX FIFOs. The division is a multiple of 4 entries, since the DM's burst length is 4. The size of the TX FIFO equals RX_BASE_ADDR. The size of the RX FIFO is 2^RAM_ADDR_WIDTH - RX_BASE_ADDR. ® The default is RX_BASE_ADDR = 2^(RAM_ADDR_WIDTH - 1) ® Only RAM_ADDR_WIDTH -1:2 bits are generated.
1:0	UNUSED	

0x12450048 SPS_GSBI1_UART_DM_TESTSL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI1_UART_DM_TESTSL

Bits	Name	Description
4	TEST_EN	Test bus enable
3:0	TEST_SEL	Test bus selector

0x12450060 SPS_GSBI1_UART_DM_MISR_MODE

Type: Read/Write
Clock: WR_CLK

SPS_GSBI1_UART_DM_MISR_MODE

Bits	Name	Description
31:2	RESERVED	unused.
1:0	MODE	0x0: Disabled 0x1: Enabled,TX test 0x2: Enabled, RX test

0x12450064 SPS_GSBI1_UART_DM_MISR_RESET

Type: Write
Clock: WR_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_MISR_RESET

Bits	Name	Description
31:1	RESERVED	unused.
0	RESET	

0x12450068 SPS_GSBI1_UART_DM_MISR_EXPORT

Type: Read/Write
Clock: WR_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_MISR_EXPORT

Bits	Name	Description
31:1	RESERVED	unused.
0	EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., what is the result of the muxing of all the input data streams with <BLOCK>_TEST_MODE) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x1245006C SPS_GSBI1_UART_DM_MISR_VAL

Type: Read
Clock: WR_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_MISR_VAL

Bits	Name	Description
9:0	VAL	Current MISR state

0x12450080 SPS_GSBI1_UART_DM_SIM_CFG

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_SIM_CFG register is used to configure the SIM interface for the UART.

- The register is generated only when SIM_GLUE_GEN generic equals 1.

SPS_GSBI1_UART_DM_SIM_CFG

Bits	Name	Description
17	UIM_TX_MODE	When this bit is set (1), the transmission portion of the SIM interface operates in block mode (T=1). When clear (0), the transmission portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.
16	UIM_RX_MODE	When this bit is set (1), the receive portion of the SIM interface operates in block mode (T=1). When clear (0), the receive portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.
15:8	SIM_STOP_BIT_LEN	In UIM_IF mode, this field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 1 to 254 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. ..... 11 111110: 254 bit times 0x1: 1 bit times 0x2: 2 bit times
7	SIM_CLK_ON	When this bit is set(1), the UIM_CLK is turned on at either the TD8 or TD4 frequency, as indicated by bit6(UIM_CLK_TD8_SEL). When this bit is cleared, the UIM_CLK is stopped either LOW or HIGH, as indicated by bit 5(UIM_CLK_STOP_HIGH).

SPS_GSBI1_UART_DM_SIM_CFG (cont.)

Bits	Name	Description
6	SIM_CLK_TD8_SEL	This bit selects the UIM_CLK frequency at which the UIM_CLK is turned on. 0x1: TD8 (the UIM_CLK runs at the TD8 frequency) 0x0: TD4 (the UIM_CLK runs at the TD4 frequency)
5	SIM_CLK_STOP_HIGH	This bit indicates at what point - high or low - the UIM_CLK will stop. 0x1: high 0x0: low
4	SIM_CLK_SEL	unused
3	MASK_RX	Setting (1) this bit masks off any 0 on the RX line, which prevents the receiver from seeing the START bit. Set (1) this bit if you do not want to receive the data you transmit.
2	SWAP_D	Setting (1) this bit causes the UIM_IF to swap the 8 data bits (making MSB into LSB, bit 6 into bit1, and so on) before it is read by the microprocessor.
1	INV_D	Set (1) this bit to cause the UIM_IF to invert the 8 data bit before it is read by the microprocessor.
0	SIM_SEL	Set (1) this bit to designate the UIM_IF mode of operation.

0x12450084 SPS_GSBI1_UART_DM_TEST_WR_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI1_UART_DM_TEST_WR_ADDR

Bits	Name	Description
31:0	TEST_WR_ADDR	RAM address at which to write the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x12450088 SPS_GSBI1_UART_DM_TEST_WR_DATA

Type: Write
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_TEST_WR_DATA

Bits	Name	Description
31:0	TEST_WR_DATA	The test data to be written to the RAM. Write to this register triggers the write to the RAM, to TEST_WR_ADDR address.

0x1245008C SPS_GSBI1_UART_DM_TEST_RD_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI1_UART_DM_TEST_RD_ADDR

Bits	Name	Description
31:0	TEST_RD_ADDR	RAM address from which to read the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

20.36.2 Read registers

NOTE The addresses of the read-only registers are mapped into the same addresses of the four write-only registers in the section above this one. They are: UART_DM_CSR, UART_DM_TF, UART_DM_CR, and UART_DM_IMR, respectively.

0x12450008 SPS_GSBI1_UART_DM_SR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_SR register is the UART status register. This register is used to obtain the current state of the UART subsystem. This register is updated asynchronously.

SPS_GSBI1_UART_DM_SR

Bits	Name	Description
8	RX_BREAK_START_LAST	When break start is detected, this bit is set (1). When break end was detected, this bit is reset (0).
7	HUNT_CHAR	When set (1), this bit indicates that the programmed character in the UART_DM_HCR register was received. If programmed, this condition causes the RXHUNT bit to be set (1) in the UART_DM_ISR register. This bit is cleared by issuing a reset error status command.
6	RX_BREAK	When set (1), this bit indicates that an all-zero character of the programmed length was received without a stop bit. If a break begins in the middle of a character, it is detected if the condition remains until the end of the next character time. Only one all zero character is written into the FIFO upon receiving the break. After the RX input returns high for at least half a bit time, then more characters are accepted by the receiver. Whenever the break condition starts or stops as defined above, the RXBREAK bit is set (1) in the UART_DM_ISR register. This bit is appended to the character in the receive FIFO.

SPS_GSBI1_UART_DM_SR (cont.)

Bits	Name	Description
5	PAR_FRAME_ERR	A parity error occurs if parity is programmed to be checked and an incoming character is received with incorrect parity. A framing error occurs when the RX input is low while the stop bit is being sampled. This bit is sampled in the middle of the first stop bit position, regardless of the programmed length of the stop bit. This error bit is appended to the character in the receive FIFO.
4	UART_OVERRUN	An overrun error occurs if one or more incoming characters are lost. This happens when the receive FIFO is full, the packing buffer is full and another character has been received in the shift register. The character in the receive shift register is lost. Upon overrun, this status bit remains high until cleared by a reset error status command.
3	TXEMT	This bit is set (1) when the transmitter under-runs. It is set after the transmission of the stop bit at the end of a character, if there are no characters waiting to be sent. It is reset when a character is written to the transmit FIFO.
2	TXRDY	This bit indicates that the transmit FIFO has space in it. It is reset when the FIFO becomes full and set when space becomes available again. Any characters that are written to the FIFO while this bit is low is lost.
1	RXFULL	This bit is set (1) when the receive FIFO becomes full. It is reset when the CPU reads a word.
0	RXRDY	This bit is set (1) when there is a word in the receive FIFO waiting to be read. It is reset when the last word currently stored in the FIFO is read.

0x12450070 SPS_GSBI1_UART_DM_RF

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RF register is the UART receive FIFO register, which is used to access the channel receive FIFO. In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM RX FIFO.

SPS_GSBI1_UART_DM_RF

Bits	Name	Description
31:0	UART_RF	This register returns the next value in the receive FIFO. After the read is completed, the FIFO read pointer is updated to make the next character available.

0x12450074 SPS_GSBI1_UART_DM_RF_2

Type: Read
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_RF_2

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x12450078 SPS_GSBI1_UART_DM_RF_3

Type: Read
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_RF_3

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x1245007C SPS_GSBI1_UART_DM_RF_4

Type: Read
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_RF_4

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x12450010 SPS_GSBI1_UART_DM_MISR

Type: Read
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI1_UART_DM_MISR

Bits	Name	Description
12:0	UART_MISR	The UART_DM_MISR register is the masked interrupt status register. A read from this register returns the "AND" of the UART_DM_ISR and the UART_DM_IMR registers. This register is updated asynchronously. This bit field is misr <= (isr(12 DOWNTO 7) AND imr(12 DOWNTO 7)) & '0' & (isr(5 DOWNTO 0) AND imr(5 DOWNTO 0)).

0x12450014 SPS_GSBI1_UART_DM_ISR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_ISR register is the UART interrupt status register. This register provides the current status of the possible interrupt conditions. If one of these bits is set (1), and the corresponding bit in the UART_DM_IMR register is set (1), an interrupt is generated (with the exception of bit 6, CURRENT_CTS - see the description of the UART_DM_IMR register). If the corresponding bit in the UART_DM_IMR register is clear (0), setting one of these bits has no effect on the UART interrupt request signal. This register is updated asynchronously.

SPS_GSBI1_UART_DM_ISR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	· See UART_DM_IMR on page 28-9
11	RXBREAK_END	· See UART_DM_IMR on page 28-9
10	RXBREAK_START	· See UART_DM_IMR on page 28-9
9	TX_DONE	· Bit 9 generated only when SIM_GLUE_GEN generic equals 1
8	TX_ERROR	· Bit 9 generated only when SIM_GLUE_GEN generic equals 1
7	TX_READY	See UART_DM_IMR on page 28-9, for descriptions of the UART_DM_ISR bits.
6	CURRENT_CTS	
5	DELTA_CTS	
4	RXLEV	
3	RXSTALE	
2	RXBREAK	
1	RXHUNT	
0	TXLEV	

0x12450038 SPS_GSBI1_UART_DM_RX_TOTAL_SNAP

Type: Read
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI1_UART_DM_RX_TOTAL_SNAP

Bits	Name	Description
23:0	RX_TOTAL_BYTES	'RX_TOTAL_SNAP register holds the number of characters received since the end of last Rx transfer. It is updated at the end of an Rx transfer (see Software procedures). Rx transfer ends when one of the conditions is met: · The number of characters which were received since the end of the previous transfer equals the value which was written to DMRX at "Transfer initialization". · A stale event occurred (flush operation already performed if was needed).

0x1245004C SPS_GSBI1_UART_DM_TXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_TXFS

Bits	Name	Description
31:14	TX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bit field. · Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	TX_ASYNC_FIFO_STATE	TX asynchronous fifo status - number of characters in the TX asynchronous FIFO.
9:7	TX_BUFFER_STATE	TX unpacking buffer status - number of bytes in the unpacking buffer
6:0	TX_FIFO_STATE_LSB	TX FIFO status - number of words in the TX FIFO

0x12450050 SPS_GSBI1_UART_DM_RXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_RXFS

Bits	Name	Description
31:14	RX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bit field. Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	RX_ASYNC_FIFO_STATE	RX asynchronous fifo status - number of characters in the RX asynchronous FIFO.
9:7	RX_BUFFER_STATE	RX packing buffer status - number of bytes in the packing buffer
6:0	RX_FIFO_STATE_LSB	The number of entries in the RX FIFO that have at least one valid character. It is incremented each time a word is moved from the packing register to the RX FIFO. It is decremented each time a word is read from the RX FIFO. Note: The Uart does not keep track of non-valid characters in each word. (See Software procedures).

0x12450090 SPS_GSBI1_UART_DM_TEST_RD_DATA

Type: Read
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI1_UART_DM_TEST_RD_DATA

Bits	Name	Description
31:0	TEST_RD_DATA	Read from this register triggers the read from the RAM. The register will hold, after read access, data which is found at TEST_RD_ADDR address in the RAM.

20.37 SPS GSBI1 QUP Registers (0x12460000 SPS_QUP1_BASE)

This section contain Smart Peripheral System GBSI 1 QUP registers.

20.37.1 QUP core registers

0x12460000 SPS_GSBI1_QUP_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

a. The contents of this register should only be changed when in the RESET_STATE (see the QUP_STATE register).

b. The value written to the QUP output FIFO, is shifted left toward the MSB before passing it to the mini-core as follows:

- N equals 8 or less - shift 24
- N equals 16 to 9 - shift 16
- N equals 24 to 17 - shift 8
- N equals 32 to 25 - no shift

The MINI_CORE clock selected is as follows:

Null: cc_qup_core_clk

SPI: cc_spi_master_clk

SPS_GSBI1_QUP_CONFIG

Bits	Name	Description
31:14	RESERVED_1	reserved
13	CORE_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).
12	APP_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).

SPS_GSBI1_QUP_CONFIG (cont.)

Bits	Name	Description
11:8	MINI_CORE	value: 0000 Null core value: 0001 SPI core value: 0010 I2C master controller value: 0011 I2C slave controller value: 0100 Reserved (I2C master & slave for loop back operation) value: 0101 Reserved (map to null core) value: 0110 Reserved (map to null core value: 0111 Reserved (map to null core) See Note 1.
7	NO_INPUT	qup_data_in is not used and the value is a "don't care". The QUP input FIFO is always empty. The input service interrupt and INPUT_SERVICE_FLAG bit are never set. See notes (a) and (b) above.
6	NO_OUTPUT	qup_data_out is not used and is held at the value zero. The QUP output FIFO is always empty. The output service flag and OUTPUT_SERVICE_FLAG bit are never set. qup_data_out is still driven when SPI_CS _N is asserted. The setting for NO_TRI_STATE still applies. See notes (a) and (b) above.
5	RESERVED_2	Reserved.
4:0	N	Number of logical bits N in the mini-core that constitutes a single transfer. The value zero indicates N equals one. The value of all ones indicates N equals 32. The value in this register must be 3 (i.e., N is 4 or higher in order for the STATE field to be set to RUN_STATE). See note (a) above.

0x12460004 SPS_GSBI1_QUP_STATE

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b0000000000000000_00000000000XX100

SPS_GSBI1_QUP_STATE

Bits	Name	Description
31:5	RESERVED	reserved.
4	I2C_MAST_GEN	Read only. Reflects the RTL generic setting for GEN_I2C_MASTER_MINI_CORE.
3	SPI_GEN	Read only. Reflects the RTL generic setting for GEN_SPI_MINI_CORE.
2	STATE_VALID	Read only. If and only if set to one, writes to the STATE field is allowed or reads from the STATE field is valid. Writes to this bit is ignored.

SPS_GSBI1_QUP_STATE (cont.)

Bits	Name	Description
1:0	STATE	When clear (00), the mini-core and related logic is held in RESET_STATE. When set to "01", the mini-core and related logic is released from reset and enters the RUN_STATE. When set to "11", the mini-core and related logic enters the PAUSE_STATE at the next appropriate point in time. Writing (10) to this field clears these two bits. For PAUSE_STATE to RESET_STATE transition, two writes of (10) are required for the transition to complete. See notes 1 and 2. Note 1: SPI - the "next appropriate point in time" is the next time SPI_CS _N de-asserts. If SPI_CS _N is not asserted when the PAUSE_STATE is entered, the SPI_CS _N is maintained in the not asserted state. The PAUSE_STATE is not available for SLAVE operation. Note 2: I2C -

0x12460008 SPS_GSBI1_QUP_IO_MODES

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b0000000000000000_00000000XXXXXXXX

Unless otherwise stated, register bits written return the value when read.

Notes:

a. "Packing" occurs as follows:

- N equals 8 or less - pack four values into each QUP input FIFO word.
- N equals 16 to 9 - pack two values into each QUP input FIFO word.
- N equals 32 to 17 - no packing. Each mini-core value is moved to an QUP input FIFO word.

b. "UnPacking" occurs as follows:

- N equals 8 or less - unpack four values from each QUP output FIFO word.
- N equals 16 to 9 - unpack two values from each QUP output FIFO word.
- N equals 32 to 17 - no packing. Each QUP output FIFO value is moved to the mini-core.

SPS_GSBI1_QUP_IO_MODES

Bits	Name	Description
31:17	RESERVED	reserved
16	OUTPUT_BIT_SHIFT_EN	If set, enables the QUP output FIFO block to do bit shifting on the output data.

SPS_GSBI1_QUP_IO_MODES (cont.)

Bits	Name	Description
15	PACK_EN	Indicates data values from the mini-core are to be packed before placement in the QUP input FIFO. See note (a) above.
14	UNPACK_EN	Indicates data values taken from the QUP output FIFO should be unpacked before passing to the mini-core. See note (b) above.
13:12	INPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_INPUT = 0, then only FIFO_Mode is available)
11:10	OUTPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_OUTPUT = 0, then only FIFO_Mode is available)
9:7	INPUT_FIFO_SIZE	Read only, actual value set by RTL generic. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 6x BLOCK_SIZE
6:5	INPUT_BLOCK_SIZE	Read only. Actual value set by RTL generic. Indicates the block size associated with Block_Mode and Data_Mover_Mode for input. Value 00: 4 Bytes (FIFO_Mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved
4:2	OUTPUT_FIFO_SIZE	Read only. Actual value set by RTL GENERIC. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 16 BLOCK_SIZE
1:0	OUTPUT_BLOCK_SIZE	Read only. Actual value set by RTL GENERIC. Value 00: 04 Bytes (FIFO mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved

0x1246000C SPS_GSBI1_QUP_SW_RESET

Type: Write/cmd
Clock: CRIF_CLK
Reset State: 0x0000

A write to this register resets the entire QUP core and all mini-cores. The internal registers are brought back to their reset values. Reading of this register returns zero.

SPS_GSBI1_QUP_SW_RESET

Bits	Name	Description
31:0	RESERVED	NA

0x12460010 SPS_GSBI1_QUP_TIME_OUT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies if the QUP_MX_OUTPUT_COUNT register and/or QUP_MX_INPUT_COUNT register are enabled. Additionally, this register only applies to Block_Mode and Data_Mover_Mode. The timer starts "ticking" when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The timer pauses for the PAUSE_STATE. If the timer expires before the QUP_MX_OUTPUT_COUNT and/or QUP_MX_INPUT_COUNT are exhausted, then the TIME_OUT_ERR flag is set in the QUP_ERROR_FLAGS register and the interrupt gsbi_qup_irq may be asserted.

SPS_GSBI1_QUP_TIME_OUT

Bits	Name	Description
15:0	TIME_OUT_VALUE	Specifies time out value in units of cc_qup_app clock ticks. A value of zero indicates the timer function is not enabled for use. See QUP_CONFIG register for information on clocks.

0x12460014 SPS_GSBI1_QUP_TIME_OUT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

SPS_GSBI1_QUP_TIME_OUT_CURRENT

Bits	Name	Description
31:0	TIME_OUT_CURRENT	Current value of time-out counter.

0x12460018 SPS_GSBI1_QUP_OPERATIONAL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0080

SPS_GSBI1_QUP_OPERATIONAL

Bits	Name	Description
31:10	RESERVED_1	reserved.
13	IN_BLOCK_READ_REQ	Read only. When set by hardware, indicates QUP input FIFO has BLOCK_SIZE_INPUT amount of data ready for reading. Valid only in Block_Mode.
12	OUT_BLOCK_WRITE_REQ	Read only. When set by hardware, indicates QUP output FIFO needs BLOCK_SIZE_OUTPUT amount of data to be written. Valid only in Block_Mode.
11	MAX_INPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP input FIFO has reached the programmed QUP_MX_INPUT_COUNT value. Valid in FIFO_Mode (only if MX_READ_COUNT is non-zero), Block_Mode and Data_Mover_Mode.
10	MAX_OUTPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP output FIFO has reached the programmed QUP_MX_OUTPUT_COUNT value. Valid in Block_Mode and Data_Mover_Mode.
9	INPUT_SERVICE_FLAG	When set by hardware, indicates QUP input FIFO has an outstanding input service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowledges software has or will read the data. Valid only in all modes.
8	OUTPUT_SERVICE_FLAG	When set by hardware, indicates QUP output FIFO has an outstanding output service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowledges software has or will read the data. Valid only in all modes.
7	INPUT_FIFO_FULL	Read only. When set, indicates the input FIFO is full and can accept no more data from the QUP mini-core.
6	OUTPUT_FIFO_FULL	Read only. When set, indicates the output FIFO is full and can accept no more CRIF writes.
5	INPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the input FIFO has at least one value in it to be read. When clear, indicates the input FIFO is empty.
4	OUTPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the output FIFO has at least one value in it to be shifted out. When clear, indicates the output FIFO is empty.
3:0	RESERVED_2	reserved.

0x1246001C SPS_GSBI1_QUP_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

SPS_GSBI1_QUP_ERROR_FLAGS

Bits	Name	Description
31:7	RESERVED_1	reserved.
6	TIME_OUT_ERR	The time out limit for a given transfer has been reached.
5	OUTPUT_OVER_RUN_ERR	Indicates the output FIFO was full when a CRIF write was attempted to the FIFO. The write is discarded.
4	INPUT_UNDER_RUN_ERR	Indicates the input FIFO was empty when a CRIF read was attempted to the FIFO. The read value returns is indeterminate.
3	OUTPUT_UNDER_RUN_ER R	Indicates the output FIFO was empty when an output shift operation required a value.
2	INPUT_OVER_RUN_ERR	Indicates the input FIFO was full when an input shift operation provided a new value. When this happens, the new value is discarded.
1:0	RESERVED_2	reserved

0x12460020 SPS_GSBI1_QUP_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x007C

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of gsbi_qup_irq and the setting of the corresponding error flag in the QUP_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

SPS_GSBI1_QUP_ERROR_FLAGS_EN

Bits	Name	Description
31:7	RESERVED_1	reserved
6	TIME_OUT_ERR_EN	If set, enables time out error generation.
5	OUTPUT_OVER_RUN_ERR _EN	If set, enables output over run error generation.

SPS_GSBI1_QUP_ERROR_FLAGS_EN (cont.)

Bits	Name	Description
4	INPUT_UNDER_RUN_ERR_EN	If set, enables input under run error generation.
3	OUTPUT_UNDER_RUN_ERR_EN	If set, enables output under run error generation.
2	INPUT_OVER_RUN_ERR_EN	If set, enables input over run error generation.
1:0	RESERVED_2	reserved

0x12460024 SPS_GSBI1_QUP_TEST_CTRL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register enables QUP test bus to be actively driven by QUP core signals.

SPS_GSBI1_QUP_TEST_CTRL

Bits	Name	Description
31:1	RESERVED	reserved
0	QUP_TEST_BUS_EN	If set, enables QUP core to actively drive test bus. If zero, the core drives the test bus to all zeros.

20.37.2 QUP output FIFO registers

0x12460100 SPS_GSBI1_QUP_MX_OUTPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each output transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not effect the count.

Notes:

a. Allows the total number of Mini Core transfers to be less than an exact multiple of OUTPUT_BLOCK_SIZE. Any additional outputs are discarded.

SPS_GSBI1_QUP_MX_OUTPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_COUNT	Number of writes of size N to the mini-core per RUN_STATE. A value of zero indicates the output count function is not enabled for use. See note (a) above.

0x12460104 SPS_GSBI1_QUP_MX_OUTPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

SPS_GSBI1_QUP_MX_OUTPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_CNT_CURRENT	Current value of QUP_MX_OUTPUT_COUNT.

0x12460108 SPS_GSBI1_QUP_OUTPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

This register holds the output data hanging out of the QUP output FIFO ready be loaded into the mini-core for the next load operation. This corresponds to signal qup_data_out going into the mini-core block.

SPS_GSBI1_QUP_OUTPUT_DEBUG

Bits	Name	Description
31:0	OUTPUT_DEBUG_DATA	Value waiting at the exit of output FIFO.

0x1246010C SPS_GSBI1_QUP_OUTPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the output FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the

value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

SPS_GSBI1_QUP_OUTPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	OUTPUT_FIFO_WORD_CNT	Number of words in the output FIFO.

0x12460110+4*c SPS_GSBI1_QUP_OUTPUT_FIFOc, c=[0..15]

Type: Write
Clock: CRIF_CLK
Reset State: 0x0000

Note that consecutive writes to this address keeps filling up the output FIFO. The max address to address the output FIFO is 0x14C.

SPS_GSBI1_QUP_OUTPUT_FIFOc

Bits	Name	Description
31:0	OUTPUT	Value to be shifted out.

0x12460150 SPS_GSBI1_QUP_MX_WRITE_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_OUTPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the gsbi_qup_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_OUTPUT_COUNT register case, the SW should not program the QUP_MX_WRITE_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_OUTPUT * FIFO_SIZE_OUTPUT).

SPS_GSBI1_QUP_MX_WRITE_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_COUNT	The number of "writes" of size N. This is used only if the core is in FIFO_Mode.

0x12460154 SPS_GSBI1_QUP_MX_WRITE_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

SPS_GSBI1_QUP_MX_WRITE_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_CNT_CURRENT	Current value of QUP_MX_WRITE_COUNT counter.

20.37.3 QUP input FIFO registers

0x12460200 SPS_GSBI1_QUP_MX_INPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each input transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not affect the count.

Notes:

a. Allows the number of shift register transfers to be less than an exact multiple of INPUT_BLOCK_SIZE. When count reached, remainder of INPUT_BLOCK_SIZE is filled with zeroes.

SPS_GSBI1_QUP_MX_INPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_COUNT	Number of reads of size N from the mini-core per RUN_STATE. A value of zero indicates the input count function is not enabled for use. See note (a) above.

0x12460204 SPS_GSBI1_QUP_MX_INPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

SPS_GSBI1_QUP_MX_INPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_CNT_CURRENT	Current value of QUP_MX_INPUT_COUNT.

0x12460208 SPS_GSBI1_QUP_MX_READ_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_INPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the qup_input_service_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_INPUT_COUNT register case, the SW should not program the QUP_MX_READ_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_INPUT * FIFO_SIZE_INPUT). If the SPI mini-core and slave operation is enabled, then an InputOverRun error will result.

SPS_GSBI1_QUP_MX_READ_COUNT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_COUNT	The number of "reads" of size N. This is used only if the core is in FIFO_Mode.

0x1246020C SPS_GSBI1_QUP_MX_READ_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

SPS_GSBI1_QUP_MX_READ_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_CNT_CURRENT	Current value of QUP_MX_READ_COUNT counter.

0x12460210 SPS_GSBI1_QUP_INPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the value of the last loaded in known-good-data into the QUP input FIFO. May be different from what the actual read of input FIFO will return because of packing enabled at the input side. This corresponds to signal qup_data_in coming from the mini-core block synchronized to the crif_clk.

SPS_GSBI1_QUP_INPUT_DEBUG

Bits	Name	Description
31:0	INPUT_DEBUG_DATA	Last known good value shifted into the input FIFO.

0x12460214 SPS_GSBI1_QUP_INPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the input FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

SPS_GSBI1_QUP_INPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	INPUT_FIFO_WORD_CNT	Number of words in the input FIFO.

0x12460218+4*c SPS_GSBI1_QUP_INPUT_FIFOc, c=[0..15]

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

Consecutive reads to this address reads the input FIFO contents on a FIFO basis.The max address to read the input FIFO is 0x254.

SPS_GSBI1_QUP_INPUT_FIFOc

Bits	Name	Description
31:0	INPUT	Value shifted in.

20.37.4 SPI mini-core registers

0x12460300 SPS_GSBI1_SPI_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register. Both NO_OUTPUT and NO_INPUT set to zero provides default full duplex operation. Setting both these bits to one is not a legal operational state.

SPS_GSBI1_SPI_CONFIG

Bits	Name	Description
31:11	RESERVED_1	Reserved.
10	HS_MODE	When set, SPI HS_MODE is enabled. When clear, SPI HS_MODE is disabled.
9	INPUT_FIRST	When set, INPUT FIRST SPI protocol is used. When clear, OUTPUT FIRST SPI protocol is used.
8	LOOP_BACK	Loopback is only valid in non-HS mode. Always clear for normal operation. If set, loop back on SPI_DATA_MO_SI under MASTER operation or SPI_DATA_MI_SO under SLAVE operation.
7:6	RESERVED_2	Reserved.
5	SLAVE_OPERATION	This register is writable only when the hardware signal spi_slave_en is asserted. When set, the SPI is configured for SLAVE operation. Zero indicates MASTER operation.
4:0	RESERVED	Reserved.

0x12460304 SPS_GSBI1_SPI_IO_CONTROL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register.

Unless otherwise stated, register bits written return the value when read.

SPS_GSBI1_SPI_IO_CONTROL

Bits	Name	Description
31:11	RESERVED	Reserved.
10	CLK_IDLE_HIGH	Use SPI_CLK_IDLE_HIGH when set.
9	CLK_ALWAYS_ON	When MASTER operation is used, run SPI_CLK during IDLE.
8	MX_CS_MODE	If this bit is set, then for a given RUN state, the associated chip select will be asserted for the first N-bit transfer and will be kept asserted till the last programmed transfer. Applies only in MASTER mode. The number of transfers is determined by SPI_MX_OUTPUT_COUNT and/or SPI_MX_INPUT_COUNT registers.
7:4	CS_N_POLARITY	These four bits control the polarity of four SPI_CS _N respectively. Setting any of this bit to '1', makes the associated SPI_CS _N active HIGH. This field is a "don't care" in SLAVE operation.
3:2	CS_SELECT	When MASTER operation is used, controls the assertion of SPI_CS_ N pins. Selects SPI_CS_N if 00, SPI_CS1_N if 01, SPI_CS2_N if 10, or SPI_CS3_N if 11. The deselected ChipSelects will be driven to inactive state dictated by the field CS_N_POLARITY. This field is a "don't care" in SLAVE operation.
1	TRISTATE_CS	When set, drives Z on all SPI_CS _N lines. When clear, enables normal functionality on these lines. This bit can be used to support deployment of the core as one of the masters in a multi-master configuration.
0	NO_TRI_STATE	When set, spi_data_out is not taken tri-state when SPI_CS _N is de-asserted. This bit is normally set for MASTER operation but may be optionally left cleared.

0x12460308 SPS_GSBI1_SPI_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

SPS_GSBI1_SPI_ERROR_FLAGS

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.

SPS_GSBI1_SPI_ERROR_FLAGS (cont.)

Bits	Name	Description
1	SPI_SLV_CLK_OVER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was greater than the programmed value of N. When this happens, only the first N bits are passed to the SPI input FIFO and the output shift value is held at zero.
0	SPI_SLV_CLK_UNDER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was less than the programmed value of N. When this occurs, the bits which were received are passed to the SPI input FIFO and the CURRENT output bit is forced to zero.

0x1246030C SPS_GSBI1_SPI_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0003

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of spi_error_irq and the setting of the corresponding error flag in the SPI_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

SPS_GSBI1_SPI_ERROR_FLAGS_EN

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.
1	SPI_SLV_CLK_OVER_RUN_ERR_EN	If set, enables clock over run error generation.
0	SPI_SLV_CLK_UNDER_RUN_ERR_EN	If set, enables clock under run error generation.

0x12460310 SPS_GSBI1_SPI_DEASSERT_WAIT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the de-assertion wait time of SPI_CS _N between consecutive N-bit transfers in MASTER operation. The wait time is specified in number of cycles of cc_spi_master_clk.

SPS_GSBI1_SPI_DEASSERT_WAIT

Bits	Name	Description
31:6	RESERVED	Reserved.

SPS_GSBI1_SPI_DEASSERT_WAIT (cont.)

Bits	Name	Description
5:0	DEASSERT_WAIT	Number cc_spi_master_clk ticks associated with the de-asserted time of SPI_CS _N. Only applies to MASTER operation. For SLAVE operation, this field is a "don't care". A value of zero indicates SPI_CS _N remains de-asserted for exactly one clock tick. A value of one, indicates two ticks, etc. All ones indicates 64 ticks.

20.37.5 I2C master mini-core registers

0x12460400 SPS_GSBI1_I2C_MASTER_CLK_CTL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_CLK_CTL register is a read/write register that controls clock divider values. This register should only be written to after it is confirmed that the I2C master mini-core is not longer in RESET state (QUP_STATE register).

SPS_GSBI1_I2C_MASTER_CLK_CTL

Bits	Name	Description
31:11	RESERVED	Reserved.
10:8	HS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in high-speed (HS) mode. The minimum value should be 3 hex (4 I2C_clk clocks per period) to ensure proper sampling of the bus. For a maximum high speed bit rate of 3.4 Mb/s (high speed mode), this would require a minimum 40.8 MHz I2C_clk clock. The maximum I2C_clk is 81.6 MHz. This register is reset to a maximum value of 7 hex. I2C_HS_CLK = I2C_CLK/(3*(HS_DIVIDER_VALUE+1)
7:0	FS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in fast/standard (FS) mode. The minimum value should be 3 hex to ensure proper sampling of the bus. For a maximum bit rate of 400 kb/s (fast mode), this would require a 4.8 MHz I2C_clk clock. For a maximum bit rate of 100 kb/s (standard mode), this would require a 1.2 MHz I2C_clk clock. Maximum I2C_clk for fast and standard modes are 206.4 MHz and 51.6 MHz respectively. This register is reset to a maximum value of 255 hex. I2C_FS_CLK = I2C_CLK/(2*(FS_DIVIDER_VALUE+3)

0x12460404 SPS_GSBI1_I2C_MASTER_STATUS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_STATUS is a status register. Writing a one clears the status bits.

SPS_GSBI1_I2C_MASTER_STATUS

Bits	Name	Description
31:26	RESERVED_1	Reserved.
25	INVALID_READ_SEQ	This bit is set (1) when a MI_REC tag does not follow a START tag for an I2C READ. Not applicable for Halcyon.
24	INVALID_READ_ADDR	This bit is set (1) when the I2C controller is trying to receive data from a non-existent I2C slave (address).
23	INVALID_TAG	This bit is set (1) when the I2C controller is trying to process data from the output FIFO that is improperly tagged.
22:20	INPUT_FSM_STATE	This 3-bit field informs the microprocessor of the state of the I2C MASTER INPUT FSM block. Reset, read_last_byte, mi_rec, dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: READ_LAST_BYTE_STATE Value 0x3: MI_REC_STATE Value 0x4: DEC_STATE Value 0x5: STORE_STATE
19:16	OUTPUT_FSM_STATE	This 4-bit field informs the microprocessor of the state of the I2C MASTER OUTPUT FSM block. Reset, decode, send, mi_red, nop, nop_dec, invalid, invalid_dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: DECODE_STATE Value 0x3: SEND_STATE Value 0x4: MI_REC_STATE Value 0x5: NOP_STATE Value 0x6: INVALID_STATE Value 0x7: PEEK_STATE Value 0x8: SEND_R_STATE

SPS_GSBI1_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
15:13	CLK_STATE	This 3-bit field informs the microprocessor of the state of the I2C clk_control block. Reset_busidle, not_master, high, low, high_wait, forced_low, hs_addr_low or double_buffer_wait. Value 0x0: RESET_BUSIDLE_STATE Value 0x1: NOT_MASTER_STATE Value 0x2: HIGH_STATE Value 0x3: LOW_STATE Value 0x4: HIGH_WAIT_STATE Value 0x5: FORCED_LOW_STATE Value 0x6: HS_ADDR_LOW_STATE Value 0x7: DOUBLE_BUFFER_WAIT_STATE
12:10	DATA_STATE	This 3-bit field informs the microprocessor of the state of the I2C data_control block. Reset, Tx addr, Tx HS addr, Tx 10-bit addr, Tx 2nd 10-bit addr byte, Tx data and Rx data. Value 0x0: RESET_WAIT_STATE Value 0x1: TX_ADDR_STATE Value 0x2: TX_DATA_STATE Value 0x3: TX_HS_ADDR_STATE Value 0x4: TX_10_BIT_ADDR_STATE Value 0x5: TX_2ND_BYTE_STATE Value 0x6: RX_DATA_STATE
9	BUS_MASTER	This bit is set (1) when the I2C controller is the present bus master.
8	BUS_ACTIVE	This bit is set (1) when the bus is in use by this, or any other controller.
7:6	FAILED	This 2-bit field contains the failure information of the present I2C transfers. If transmitting, failed[1] contains the information regarding the byte that has been transmitted. Failed[0] contains the information of the byte awaiting transmission if there is a byte pipelined. If no byte is pipelined, ignore this bit. If receiving, failed[1] contains the information of the byte received and stored in the buffer, and failed[0] should be ignored. For example: Value 00: Byte n transmitted successfully, byte n+1 to begin transmission Value 01: Byte n transmitted successfully, byte n+1 errored: type of error indicated in other STATUS bits. (queued invalid write, for example) Value 10: Byte n errored: type of error indicated in other STATUS bits, byte n+1 to begin transmission (byte n+1 would have to be a valid address byte for this condition to occur) Value 11: Byte n errored: type of error indicated in other STATUS bits, byte n+1 discarded as well (if the byte was a data byte destined for a NACKed address, data is useless, therefore discarded)
5	INVALID_WRITE	This bit is set (1) when software writes data to the I2C_DATA register that should be flagged as an address but is not.

SPS_GSBI1_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
4	ARB_LOST	This bit is set (1) when the controller loses arbitration for the bus. If this bit gets set (1) during the transmission, all data has been lost, and the microprocessor must re-request its transmission.
3	PACKET_NACKED	This bit is set high when a NACK is received from a slave. If a high speed master code is sent and there is an ACK from a slave, then this bit is set (1) to indicate that the high speed mode can not be entered. If the high speed mode is accepted by the slave, then a NACK is performed and this bit is not set (1).
2	BUS_ERROR	This bit is set (1) when an unexpected START or STOP condition is detected. This returns the controller to its reset state.
1:0	RESERVED_2	Reserved.

20.38 SPS GSBI2 Registers (0x12480000 SPS_GSBI2_BASE)

This section contains Smart Peripheral System GSBI 2 registers.

20.38.1 GSBI CTRL Registers

0x12480000 SPS_GSBI2_GSBI_CTRL_REG

Type: Read/write
Clock: HCLK
Reset State: 0x00000000

SPS_GSBI2_GSBI_CTRL_REG

Bits	Name	Description
15:12	RESERVED	reserved
11:8	WRAPPER_CTRL	This field has no predefined use. When a wrapper is constructed around one or more GSBIs there may be a need to configure it. E.g., to select which of several GSBIs will be connected to a particular I2S block. All bits of this field emerge from GSBI as output ports which can be used for any such configuration task.
7	RESERVED_7	Reserved. The host can write and read this field, but its state has no effect on anything.
6:4	PROTOCOL_CODE	This field controls which protocol, if any, is applied to the GSBI's four I/O ports. Most codes assign a single protocol, but codes of "001" and "110" assigns I2C to two of the ports and UART (without flow control signals) or SIM to the other two. 0x0: Idle (null values are applied to all four GSBI I/Os) 0x1: I2C on 2 ports, SIM/R-UIM on other 2 0x2: I2C 0x3: SPI 0x4: UART with flow control (or IRDA) 0x5: SIM/R-UIM 0x6: I2C on 2 ports, UART (without HS flow ctrl on other 2) 0x7: Undefined
3:1	RESERVED_3_1	Reserved. The host can write and read this field, but its state has no effect on anything.
0	CRCI_MUX_CTRL	While this bit is low QUP CRCI ports are connected to the GSBI ports nominally for QUP and UART_DM CRCI ports are connected to the GSBI ports nominally for UART_DM. While this bit is high QUP CRCI ports are connected to the GSBI ports nominally for UART_DM and UART_DM CRCI ports are connected to nothing.

0x12480004 SPS_GSBI2_GSBI_DBG0_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

SPS_GSBI2_GSBI_DBG0_REG

Bits	Name	Description
1:0	GSBI_PLAY0	This field has no function beyond the fact that the ARM can write to it and read from it.

0x12480008 SPS_GSBI2_GSBI_DBG1_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

SPS_GSBI2_GSBI_DBG1_REG

Bits	Name	Description
1:0	GSBI_PLAY1	This field has no function beyond the fact that the ARM can write to it and read from it.

0x1248000C SPS_GSBI2_GSBI_DBG2_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

SPS_GSBI2_GSBI_DBG2_REG

Bits	Name	Description
1:0	GSBI_PLAY2	This field has no function beyond the fact that the ARM can write to it and read from it.

0x12480010 SPS_GSBI2_GSBI_DBG3_REG

Type: Read/write
Clock: HCLK
Reset State: 0x0

SPS_GSBI2_GSBI_DBG3_REG

Bits	Name	Description
1:0	GSBI_PLAY3	This field has no function beyond the fact that the ARM can write to it and read from it.

20.39 SPS GSBI2 UART DM Registers (0x12490000 SPS_UART2_DM_BASE)

This section contains Smart Peripheral System GSBI 2 UART DM registers.

UART_DM registers are accessible only by the ARM

This section contains the read and write registers for UART1.

20.39.1 Write and read/write registers

0x12490000 SPS_GSBI2_UART_DM_MR1

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_MR1 register is the UART mode register 1. It is used, along with UART_DM_MR2, to configure the operational mode of the UART.

SPS_GSBI2_UART_DM_MR1

Bits	Name	Description
31:8	AUTO_RFR_LEVEL1	These bits are used, along with bits 5:0 (AUTO_RFR_LEVEL0) to program the level in the receive FIFO at which the RFR_N signal is de-asserted, if programmed to do so (see RX_RDY_CTL field of this register). The level counts the number of words inside the RX FIFO. It doesn't count the character that is being received (shift register) or characters in the packing buffer. This value is programmed from 1 to 2^RAM_ADDR_WIDTH. The RFR_N signal is de-asserted when the RX FIFO level (the number of characters remaining in the RX FIFO) is greater than the level that is programmed into this register. · Only RAM_ADDR_WIDTH +1:8 bits are generated.
7	RX_RDY_CTL	Setting (1) this bit enables the automatic ready-for-receiving (RFR_N) control for the receiver. RFR_N is turned off, or set (1), when a valid start bit is received and the channel FIFO is at the level programmed in bits 4 through 0 of this mode register. When the FIFO level falls back to the programmed level, the RFR_N signal is turned on, or clear (0). When this feature is off, the RFR_N signal can be used by normal signal port bit manipulation (see UART_DM_CR register).

SPS_GSBI2_UART_DM_MR1 (cont.)

Bits	Name	Description
6	CTS_CTL	When this bit is set(1), the transmitter checks the CTS_N input to determine whether to begin transmission of a new character. If CTS_N is low, the character is sent. Otherwise the transmitter continues marking until CTS_N goes low, then the next character is transmitted. A change on CTS_N during the transmission of a character has no effect on that character. When this bit is clear(0), the CTS_N input for the channel has no effect on the transmitter.
5:0	AUTO_RFR_LEVEL0	See the description of bit 8 (AUTO_RFR_LEVEL1).

0x12490004 SPS_GSBI2_UART_DM_MR2

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI2_UART_DM_MR2

Bits	Name	Description
9	RX_ERROR_CHAR_OFF	When this bit is asserted, characters with parity or framing errors don't enter RX FIFO. Otherwise they enter RX FIFO.
8	RX_BREAK_ZERO_CHAR_OFF	When this bit is asserted, the zero character received at rx_break doesn't enter RX FIFO. Otherwise it enters RX FIFO.
7	LOOPBACK	Internal use only
6	ERROR_MODE	This bit controls the operation of the two FIFO status bits for the channel (parity or framing error and received break). · When clear (0), the UART operates in character mode and the status bits apply only to the character at the top of the FIFO. · When set (1), the UART operates in block mode and both bits are the "OR" of the status for all previously received characters arriving after the last `reset error status' command was issued (see CR register).
5:4	BITS_PER_CHAR	These bits determine how many bits are transmitted or received per character, not including the start, stop, and parity bits. 0x0: 5 bits 0x1: 6 bits 0x2: 7 bits 0x3: 8 bits

SPS_GSBI2_UART_DM_MR2 (cont.)

Bits	Name	Description
3:2	STOP_BIT_LEN	This field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 9/16, 1, 1+ 9/16, and 2 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. 0x0: 0.563 (9/16 bit times) 0x1: 1.000 bit time 0x2: 1.563 (1+9/16 bit times) 0x3: 2.000 bit times
1:0	PARITY_MODE	These bits determine which parity mode is used. The user can select between odd, even, space, or no parity. 0x0: no parity 0x1: odd parity 0x2: even parity 0x3: space parity

0x12490008 SPS_GSBI2_UART_DM_CSR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_CSR register is the UART clock selection register. This register is used in conjunction with the UART M/N counter registers to determine the bit rate for the transmitter and receiver. The transmitter and receiver can be clocked at different rates.

The rates below are based on a uart_dm_clk rate of 1.8432 MHz (115.2 * 16).

Table 20-13 lists the hexadecimal values for the clock select field and the corresponding data rates.

Table 20-13 Hexadecimal values for clock select field and corresponding data rates

CLK SEL value	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Bit rate (b/sec)	75	150	300	600	1200	2400	3600	4800	7200	9600	14.4k	19.2k	28.8k	38.4k	57.6k	115.2k

SPS_GSBI2_UART_DM_CSR

Bits	Name	Description
7:4	UART_RX_CLK_SEL	Use the CLK SEL values in Table 28-12 to select the appropriate receive and transmit bit rates.
3:0	UART_TX_CLK_SEL	

0x12490070 SPS_GSBI2_UART_DM_TF

Type: Write
Clock: AHB_CLK
Reset State: Undefined

In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM TX FIFO.

SPS_GSBI2_UART_DM_TF

Bits	Name	Description
31:0	UART_TF	The UART_TF register is the UART transmit FIFO register. This register is used to access the channel transmit FIFO. If the FIFO is full at the time of writing, the character is lost and an interrupt is generated (see UART_DM_IMR register).

0x12490074 SPS_GSBI2_UART_DM_TF_2

Type: Write
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_TF_2

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x12490078 SPS_GSBI2_UART_DM_TF_3

Type: Write
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_TF_3

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x1249007C SPS_GSBI2_UART_DM_TF_4

Type: Write
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_TF_4

Bits	Name	Description
31:0	UART_TF	See UART_DM_TF register.

0x12490010 SPS_GSBI2_UART_DM_CR

Type: Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_CR register is the UART command register. This register is used to issue specific commands to the UART subsystem. This register is updated asynchronously.

CAUTION Do not reset the transmitter and disable it at the same time. Do not reset the receiver and disable it at the same time.

Table 20-14 UART DM command values

Value	Description	Result
0	Null command	Does nothing.
1	Reset receiver	Resets the receiver as if a hardware reset were issued. The receiver is disabled and the FIFO, packing buffer and shift registers are flushed.
2	Reset transmitter	Resets the transmitter as if a hardware reset were issued. The transmitter signal goes high (marking) and the FIFO, unpacking register and shift register are flushed.
3	Reset error status	Clears the overrun error and hunt char received status bits in both the character and block error modes. In the block error mode, it clears the error status and received break.
4	Reset break change interrupt	Clears the break change interrupt status bit.
5	Start break	Forces the transmitter signal low. The transmitter must be enabled. If the transmitter is busy, the break is started when all characters in the transmit FIFO and the transmit shift register have been completely sent.
6	Stop break	If executed while channel is breaking, this command causes the transmitter signal to go high. The signal remains high for at least one bit time before sending out a new character.
7	Reset CTS_N	Clears ISR bit 5.
8	Reset stale interrupt	Clears the stale interrupt.

Table 20-14 UART DM command values

Value	Description	Result
9	Packet mode	Turns on the sample data mode, which causes the receiver to sample the receive data stream at 16 times the programmed baud rate. The data is sampled with the start of the start bit, or the first data bit, and continued until the marking state. To exit this state, write 1100 in the command field.
A	test_parity_on	Internal use only.
B	test_frame_on	Internal use only.
C	Mode reset	Turns off the sample data mode.
D	Set RFR_N	Asserts the ready for receiving signal (active low).
E	Reset RFR_N	De-asserts the ready for receiving signal.
F	uart_reset_int	Internal use only.
10	Reset TX_ERROR	Clears TX_ERROR
11	Clear TX_DONE	Clears the TX_DONE interrupt (ISR bit 9)
12	Reset break start interrupt	Clears the break start interrupt status bit.
13	Reset break end interrupt	Clears the break end interrupt status bit.
14	Reset par_frame_err interrupt	Clears the par_frame_err interrupt status bit.

Table 20-15 UART DM command values

Value	Description	Result
0	Null command	Does nothing.
1	CR Protection Enable	Enables CR HW protection. When two consecutive writes to the CR are detected, the second write is delayed until the command of the first write is finished. The delay is done by de-asserting the AHB ready and this ensures that the first command completes and the second one will be executed right afterward.
2	CR Protection Disable	Disables CR HW protection. SW is responsible for managing delay between writes to the CR register.
3	Reset TX-Ready interrupt	Clears the TX_READY interrupt.
5	Enable Stale Event	Enables the `stale event' mechanism. See Software Procedures.
6	Disable Stale Event	Disables the `stale event' mechanism. See Software Procedures.
4	SW Force Stale	Causes a `stale event' (even if `stale event' is disabled). See Software Procedures.
7	RESERVED	

SPS_GSBI2_UART_DM_CR

Bits	Name	Description
11	CHANNEL_COMMAND_MSB	This is the msb of the CHANNEL_COMMAND bit field.
10:8	GENERAL_COMMAND	Writing the appropriate value to these bits executes the commands that are listed in Table.
7:4	CHANNEL_COMMAND_LSB	Writing the appropriate value to these bits along with bit 11,executes the commands that are listed in Table 28-13.
3	UART_TX_DISABLE	This command terminates the operation of the transmitter after any character in the transmit shift register is sent.
2	UART_TX_EN	This command enables the operation of the transmitter.
1	UART_RX_DISABLE	This command immediately terminates the operation of the channel receiver and any incoming characters are lost. None of the receiver status bits are affected by this command and characters that are already in the receive FIFO remain there.
0	UART_RX_EN	This command enables the channel receiver.

0x12490014 SPS_GSBI2_UART_DM_IMR

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IMR register is the UART interrupt mask register. This register is used to enable the corresponding functions in the UART_DM_ISR register. Setting (1) a bit in the UART_DM_IMR register causes an interrupt to be generated, if the corresponding bit in the UART_DM_ISR register is set. Clearing (0) a bit in the UART_DM_IMR register causes the setting of the corresponding bit in the UART_DM_ISR register to have no effect on the interrupt signal.

Bit 6 of the UART_DM_IMR register, CURRENT_CTS, is slightly different. If the current value of the CTS is one (1), no interrupt is generated. However, the user can use bit 6 in this register to mask the CTS value when reading the UART_DM_MISR register or as a general-purpose bit.

SPS_GSBI2_UART_DM_IMR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	This bit is asserted in the same condition at which PAR_FRAME_ERR status bit is asserted. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x14.
11	RXBREAK_END	This bit is set (1) if the end of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x13.

SPS_GSBI2_UART_DM_IMR (cont.)

Bits	Name	Description
10	RXBREAK_START	This bit is set (1) if the start of a break condition is detected. The logic associated with this condition is cleared (0) by issuing CHANNEL_COMMAN = 0x12.
9	TX_DONE	This bit is used only in UIM/SIM_IF mode. Set (1) this bit when the last byte in the transmitter has been sent. · This bit is generated only when SIM_GLUE_GEN generic equals 1.
8	TX_ERROR	Only used in UIM_IF mode. Set (1) this bit to indicate that there has been parity error during transmission. To clear the detection logic associated with this function, write CR[11;7:4]=0x10. · This bit is generated only when SIM_GLUE_GEN generic equals 1.
7	TX_READY	This bit, when set(1), indicates that: 1. TX FIFO is empty. 2. The value written in NO_CHARS_FOR_TX register equals the number of bytes written to the TX FIFO since the register was updated. Note: There may be characters in the unpack buffer or in the shift register. This bit is cleared by issuing `clear TX ready' command (see UART_DM_CR register).
6	CURRENT_CTS	This bit indicates the current state of the CTS input. It never generates an interrupt.
5	DELTA_CTS	This bit, when set (1), indicates that the CTS input has changed states. To clear the detection logic associated with this function, write CR[7:4]=0x7.
4	RXLEV	This bit is set when a character is loaded into the receive FIFO that brings the total number of characters in the FIFO above the programmed watermark level in the FIFO watermark register (RFWR). This bit is cleared after enough characters have been read to bring the level equal to or below the programmed watermark level.
3	RXSTALE	This bit indicates that a `stale event' occurred. See Software procedures for the exact timing of this interrupt. It is cleared by issuing a reset-stale command (see CR register).
2	RXBREAK_CHANGE	This bit is set (1) if the start or end of a break condition is detected. The logic associated with this condition is cleared (0) by writing CR[7:4]=0x4. A detected break is defined as an all-zeros character with an invalid stop bit AND LOW PARITY. The end of a break is defined as a mark condition (1) at least 1/2 bit width. A detected break occupies one position in the Rx FIFO.
1	RXHUNT	This bit is set (1) when an incoming character matches the value programmed into the UART_DM_HCR register. This condition is cleared (0) by issuing a reset error status command (CR[7:4]=0x3).

SPS_GSBI2_UART_DM_IMR (cont.)

Bits	Name	Description
0	TXLEV	This bit is set (1) when a character which is transferred from the transmit FIFO to the transmit shift register brings the total number of characters in the FIFO below or equal to the programmed watermark level in the UART_DM_TFWR register. This bit is cleared (0) after enough characters have been written to the FIFO to bring the level above the programmed watermark level.

0x12490018 SPS_GSBI2_UART_DM_IPR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0xffffff9f

The UART_DM_IPR register is the UART interrupt programming register.

SPS_GSBI2_UART_DM_IPR

Bits	Name	Description
31:7	STALE_TIMEOUT_MSB	These bits are the STALE_TIMEOUT bit field. The stale character time-out duration field contains a number from 1 to 2^30 -1. This number determines how many character times must elapse before a `stale event' is generated. This character time is defined as 10 times the bit rate. It is reset whenever a data bit is received. Do not clear (0) this register if the stale character time-out interrupt is enabled. Note the discontinuity in the bit assignments.
6	SAMPLE_DATA	Setting (1) this bit enables the new sample data mode, which means that the start bit is sampled as well as the rest, when in sample data mode. See the CR register, CHANNEL_COMMAND bit for more information.
5	RESERVED	
4:0	STALE_TIMEOUT_LSB	This bit field is the LSbits of the STALE_TIMEOUT bit field.

0x1249001C SPS_GSBI2_UART_DM_TFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_TFWR register is the UART transmit FIFO watermark register.

SPS_GSBI2_UART_DM_TFWR

Bits	Name	Description
31:0	TFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the transmit FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of TX words in the FIFO) is less than or equal to the value in TFWR. See UART_DM_IMR register. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x12490020 SPS_GSBI2_UART_DM_RFWR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RFWR register is the UART receive FIFO watermark register.

SPS_GSBI2_UART_DM_RFWR

Bits	Name	Description
31:0	RFW	These bits contain a number, between 0 and 2^RAM_ADDR_WIDTH - 1, that determines the level of the receive FIFO at which an interrupt is generated. The interrupt is generated when the FIFO level (number of words in the RX FIFO) is greater than the value in RFWR. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x12490024 SPS_GSBI2_UART_DM_HCR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI2_UART_DM_HCR

Bits	Name	Description
7:0	DATA	The UART_DM_HCR register is the UART hunt character register, which contains the character for which the receiver looks to assert a hunt character received interrupt.

0x12490034 SPS_GSBI2_UART_DM_DMRX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI2_UART_DM_DMRX

Bits	Name	Description
24:0	RX_DM_CRCI_CHARS	In the DM mode, the number of chars in the Rx FIFO that are used for CRCI handshake with the DM. The written value of RX_DM_CRCI_ CHARS must be a multiple of 16(bits [3:0] are treated as 0x0). After a value is written, the UART will generate CRCI requests as long as RX_DM_CRCI_CHARS is non zero. Read of DMRX register gives the number of characters that were received since the end of the last transfer. It is reset at the end of each Rx transfer Also is used by the software to indicate `transfer initialization'. See Software procedures.

0x12490038 SPS_GSBI2_UART_DM_IRDA

Type: Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_IRDA register enables the IRDA function, selects a loopback, and allows inversion of RX and TX data. This register also controls the IRDA transceiver that optionally interfaces between the UART and the DP_RX_DATA and DP_TX_DATA pins.

The UART proper is a standard RX/TX configuration that converts the serial pin input and output lines to 8-bit data for the microprocessor. The configuration contains receive and transmit blocks, a control block, a bit rate generator for RX and TX, and FIFO interfaces with the microprocessor data bus. The IRDA register provides the means of switching IRDA circuits into the serial I/O lines and the IRDA function is normally switched out. The IRDA modulator/demodulator may be enabled or disabled under microprocessor control. When enabled, the RX and TX data paths have individual inversion select bits, so external true or inverted drivers may be used in the signal path.

- The register is generated only when IRDA_IFC_GEN generic equals 1.

SPS_GSBI2_UART_DM_IRDA

Bits	Name	Description
4	MEDIUM_RATE_EN	· Set (1) for 1/4 bit-time pulse length (Medium rate) · Clear (0) for 3/16 bit-time pulse length (Low rate)
3	IRDA_LOOPBACK	· This bit loops the IRDA modulated TX line back into the IRDA RX line. The normal UART loopback mode must be off in order to see this effect.

SPS_GSBI2_UART_DM_IRDA (cont.)

Bits	Name	Description
2	INVERT_IRDA_TX	This bit inverts the polarity of the IRDA modulated signal on the DP_TX_DATA pin. · Set (1) this bit for an inverted polarity. · Clear (0) this bit for a non-inverted polarity.
1	INVERT_IRDA_RX	This bit inverts the polarity of the IRDA received signal on the DP_RX_DATA pin. · Set (1) this bit for inverted the polarity. · Clear (0) this bit for non-inverted polarity.
0	IRDA_EN	· Set (1) this bit to enable the IRDA transceiver. · Clear (0) this bit to bypass the IRDA transceiver and ignore the other bits of this register.

0x1249003C SPS_GSBI2_UART_DM_DMEN

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_DMEN register indicates if Data Mover is enabled for TX and RX channels.

SPS_GSBI2_UART_DM_DMEN

Bits	Name	Description
1	RX_DM_EN	· Set (1) this bit to enable RX DM interface. · Clear (0) this bit to disable RX DM interface. Clearing this bit requires resetting the receiver (see UART_DM_CR register).
0	TX_DM_EN	Set (1) this bit to enable TX DM interface. Clear (0) this bit to disable TX DM interface.

0x12490040 SPS_GSBI2_UART_DM_NO_CHARS_FOR_TX

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI2_UART_DM_NO_CHARS_FOR_TX

Bits	Name	Description
23:0	TX_TOTAL_TRANS_LEN	The total number of characters for transmission. Before writing a new value, the TX FIFO must be empty (as indicated by TX_READY interrupt in IMR register or after a reset). It is used by the transmitter to calculate how many characters to transmit in the last word. In DM mode, it is also used for the CRCI mechanism. Any additional writes to the TX FIFO above TX_TOTAL_TRANS_LEN will be discarded. A TX_READY interrupt is triggered after TX_TOTAL_TRANS_LEN number of characters were moved from the TX FIFO to the unpacking register (not all may have been sent).

0x12490044 SPS_GSBI2_UART_DM_BADR

Type: Read/Write
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_BADR

Bits	Name	Description
31:2	RX_BASE_ADDR	RX FIFO base address. Both FIFOs use the same RAM (2^RAM_ADDR_WIDTH, 32-bit entries). This register controls the division of the memory to the RX and TX FIFOs. The division is a multiple of 4 entries, since the DM's burst length is 4. The size of the TX FIFO equals RX_BASE_ADDR. The size of the RX FIFO is 2^RAM_ADDR_WIDTH - RX_BASE_ADDR. ® The default is RX_BASE_ADDR = 2^(RAM_ADDR_WIDTH - 1) ® Only RAM_ADDR_WIDTH -1:2 bits are generated.
1:0	UNUSED	

0x12490048 SPS_GSBI2_UART_DM_TESTSL

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI2_UART_DM_TESTSL

Bits	Name	Description
4	TEST_EN	Test bus enable
3:0	TEST_SEL	Test bus selector

0x12490060 SPS_GSBI2_UART_DM_MISR_MODE

Type: Read/Write
Clock: WR_CLK

SPS_GSBI2_UART_DM_MISR_MODE

Bits	Name	Description
31:2	RESERVED	unused.
1:0	MODE	0x0: Disabled 0x1: Enabled,TX test 0x2: Enabled, RX test

0x12490064 SPS_GSBI2_UART_DM_MISR_RESET

Type: Write
Clock: WR_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_MISR_RESET

Bits	Name	Description
31:1	RESERVED	unused.
0	RESET	

0x12490068 SPS_GSBI2_UART_DM_MISR_EXPORT

Type: Read/Write
Clock: WR_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_MISR_EXPORT

Bits	Name	Description
31:1	RESERVED	unused.
0	EXPORT	When clear (0), testbus is driven by what is sent into the MISR. (i.e., what is the result of the muxing of all the input data streams with <BLOCK>_TEST_MODE) When set (1), testbus is driven by the current state of the MISR. (debug typically)

0x1249006C SPS_GSBI2_UART_DM_MISR_VAL

Type: Read
Clock: WR_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_MISR_VAL

Bits	Name	Description
9:0	VAL	Current MISR state

0x12490080 SPS_GSBI2_UART_DM_SIM_CFG

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

The UART_DM_SIM_CFG register is used to configure the SIM interface for the UART.

- The register is generated only when SIM_GLUE_GEN generic equals 1.

SPS_GSBI2_UART_DM_SIM_CFG

Bits	Name	Description
17	UIM_TX_MODE	When this bit is set (1), the transmission portion of the SIM interface operates in block mode (T=1). When clear (0), the transmission portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.
16	UIM_RX_MODE	When this bit is set (1), the receive portion of the SIM interface operates in block mode (T=1). When clear (0), the receive portion of the SIM interface operates in asynchronous transfer mode (T=0). Note that the operation of this function is conditional upon UART_SIM_CFG[0] being set (1) to designate the UIM_IF mode of operation.
15:8	SIM_STOP_BIT_LEN	In UIM_IF mode, this field programs the duration of the stop bit that is appended to each transmitted character. The stop bit duration can be 1 to 254 bit times. The receiver only samples the stop bit once, regardless of the programmed stop bit length. ..... 11 111110: 254 bit times 0x1: 1 bit times 0x2: 2 bit times
7	SIM_CLK_ON	When this bit is set(1), the UIM_CLK is turned on at either the TD8 or TD4 frequency, as indicated by bit6(UIM_CLK_TD8_SEL). When this bit is cleared, the UIM_CLK is stopped either LOW or HIGH, as indicated by bit 5(UIM_CLK_STOP_HIGH).

SPS_GSBI2_UART_DM_SIM_CFG (cont.)

Bits	Name	Description
6	SIM_CLK_TD8_SEL	This bit selects the UIM_CLK frequency at which the UIM_CLK is turned on. 0x1: TD8 (the UIM_CLK runs at the TD8 frequency) 0x0: TD4 (the UIM_CLK runs at the TD4 frequency)
5	SIM_CLK_STOP_HIGH	This bit indicates at what point - high or low - the UIM_CLK will stop. 0x1: high 0x0: low
4	SIM_CLK_SEL	unused
3	MASK_RX	Setting (1) this bit masks off any 0 on the RX line, which prevents the receiver from seeing the START bit. Set (1) this bit if you do not want to receive the data you transmit.
2	SWAP_D	Setting (1) this bit causes the UIM_IF to swap the 8 data bits (making MSB into LSB, bit 6 into bit1, and so on) before it is read by the microprocessor.
1	INV_D	Set (1) this bit to cause the UIM_IF to invert the 8 data bit before it is read by the microprocessor.
0	SIM_SEL	Set (1) this bit to designate the UIM_IF mode of operation.

0x12490084 SPS_GSBI2_UART_DM_TEST_WR_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI2_UART_DM_TEST_WR_ADDR

Bits	Name	Description
31:0	TEST_WR_ADDR	RAM address at which to write the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

0x12490088 SPS_GSBI2_UART_DM_TEST_WR_DATA

Type: Write
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_TEST_WR_DATA

Bits	Name	Description
31:0	TEST_WR_DATA	The test data to be written to the RAM. Write to this register triggers the write to the RAM, to TEST_WR_ADDR address.

0x1249008C SPS_GSBI2_UART_DM_TEST_RD_ADDR

Type: Read/Write
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI2_UART_DM_TEST_RD_ADDR

Bits	Name	Description
31:0	TEST_RD_ADDR	RAM address from which to read the test data. · Only RAM_ADDR_WIDTH -1:0 bits are generated.

20.39.2 Read registers

NOTE The addresses of the read-only registers are mapped into the same addresses of the four write-only registers in the section above this one. They are: UART_DM_CSR, UART_DM_TF, UART_DM_CR, and UART_DM_IMR, respectively.

0x12490008 SPS_GSBI2_UART_DM_SR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_SR register is the UART status register. This register is used to obtain the current state of the UART subsystem. This register is updated asynchronously.

SPS_GSBI2_UART_DM_SR

Bits	Name	Description
8	RX_BREAK_START_LAST	When break start is detected, this bit is set (1). When break end was detected, this bit is reset (0).
7	HUNT_CHAR	When set (1), this bit indicates that the programmed character in the UART_DM_HCR register was received. If programmed, this condition causes the RXHUNT bit to be set (1) in the UART_DM_ISR register. This bit is cleared by issuing a reset error status command.
6	RX_BREAK	When set (1), this bit indicates that an all-zero character of the programmed length was received without a stop bit. If a break begins in the middle of a character, it is detected if the condition remains until the end of the next character time. Only one all zero character is written into the FIFO upon receiving the break. After the RX input returns high for at least half a bit time, then more characters are accepted by the receiver. Whenever the break condition starts or stops as defined above, the RXBREAK bit is set (1) in the UART_DM_ISR register. This bit is appended to the character in the receive FIFO.

SPS_GSBI2_UART_DM_SR (cont.)

Bits	Name	Description
5	PAR_FRAME_ERR	A parity error occurs if parity is programmed to be checked and an incoming character is received with incorrect parity. A framing error occurs when the RX input is low while the stop bit is being sampled. This bit is sampled in the middle of the first stop bit position, regardless of the programmed length of the stop bit. This error bit is appended to the character in the receive FIFO.
4	UART_OVERRUN	An overrun error occurs if one or more incoming characters are lost. This happens when the receive FIFO is full, the packing buffer is full and another character has been received in the shift register. The character in the receive shift register is lost. Upon overrun, this status bit remains high until cleared by a reset error status command.
3	TXEMT	This bit is set (1) when the transmitter under-runs. It is set after the transmission of the stop bit at the end of a character, if there are no characters waiting to be sent. It is reset when a character is written to the transmit FIFO.
2	TXRDY	This bit indicates that the transmit FIFO has space in it. It is reset when the FIFO becomes full and set when space becomes available again. Any characters that are written to the FIFO while this bit is low is lost.
1	RXFULL	This bit is set (1) when the receive FIFO becomes full. It is reset when the CPU reads a word.
0	RXRDY	This bit is set (1) when there is a word in the receive FIFO waiting to be read. It is reset when the last word currently stored in the FIFO is read.

0x12490070 SPS_GSBI2_UART_DM_RF

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_RF register is the UART receive FIFO register, which is used to access the channel receive FIFO. In order to support bursts of 4, 0x70-0x7C address space is reserved for the UART_DM RX FIFO.

SPS_GSBI2_UART_DM_RF

Bits	Name	Description
31:0	UART_RF	This register returns the next value in the receive FIFO. After the read is completed, the FIFO read pointer is updated to make the next character available.

0x12490074 SPS_GSBI2_UART_DM_RF_2

Type: Read
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_RF_2

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x12490078 SPS_GSBI2_UART_DM_RF_3

Type: Read
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_RF_3

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x1249007C SPS_GSBI2_UART_DM_RF_4

Type: Read
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_RF_4

Bits	Name	Description
31:0	UART_RF	see UART_DM_RF register.

0x12490010 SPS_GSBI2_UART_DM_MISR

Type: Read
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI2_UART_DM_MISR

Bits	Name	Description
12:0	UART_MISR	The UART_DM_MISR register is the masked interrupt status register. A read from this register returns the "AND" of the UART_DM_ISR and the UART_DM_IMR registers. This register is updated asynchronously. This bit field is misr <= (isr(12 DOWNTO 7) AND imr(12 DOWNTO 7)) & '0' & (isr(5 DOWNTO 0) AND imr(5 DOWNTO 0)).

0x12490014 SPS_GSBI2_UART_DM_ISR

Type: Read
Clock: AHB_CLK
Reset State: Undefined

The UART_DM_ISR register is the UART interrupt status register. This register provides the current status of the possible interrupt conditions. If one of these bits is set (1), and the corresponding bit in the UART_DM_IMR register is set (1), an interrupt is generated (with the exception of bit 6, CURRENT_CTS - see the description of the UART_DM_IMR register). If the corresponding bit in the UART_DM_IMR register is clear (0), setting one of these bits has no effect on the UART interrupt request signal. This register is updated asynchronously.

SPS_GSBI2_UART_DM_ISR

Bits	Name	Description
12	PAR_FRAME_ERR_IRQ	· See UART_DM_IMR on page 28-9
11	RXBREAK_END	· See UART_DM_IMR on page 28-9
10	RXBREAK_START	· See UART_DM_IMR on page 28-9
9	TX_DONE	· Bit 9 generated only when SIM_GLUE_GEN generic equals 1
8	TX_ERROR	· Bit 9 generated only when SIM_GLUE_GEN generic equals 1
7	TX_READY	See UART_DM_IMR for descriptions of the UART_DM_ISR bits.
6	CURRENT_CTS	
5	DELTA_CTS	
4	RXLEV	
3	RXSTALE	
2	RXBREAK	

SPS_GSBI2_UART_DM_ISR (cont.)

Bits	Name	Description
1	RXHUNT	
0	TXLEV	

0x12490038 SPS_GSBI2_UART_DM_RX_TOTAL_SNAP

Type: Read
Clock: AHB_CLK
Reset State: 0x0

SPS_GSBI2_UART_DM_RX_TOTAL_SNAP

Bits	Name	Description
23:0	RX_TOTAL_BYTES	'RX_TOTAL_SNAP register holds the number of characters received since the end of last Rx transfer. It is updated at the end of an Rx transfer (see Software procedures). Rx transfer ends when one of the conditions is met: · The number of characters which were received since the end of the previous transfer equals the value which was written to DMRX at "Transfer initialization". · A stale event occurred (flush operation already performed if was needed).

0x1249004C SPS_GSBI2_UART_DM_TXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_TXFS

Bits	Name	Description
31:14	TX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bit field. · Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	TX_ASYNC_FIFO_STATE	TX asynchronous fifo status - number of characters in the TX asynchronous FIFO.
9:7	TX_BUFFER_STATE	TX unpacking buffer status - number of bytes in the unpacking buffer
6:0	TX_FIFO_STATE_LSB	TX FIFO status - number of words in the TX FIFO

0x12490050 SPS_GSBI2_UART_DM_RXFS

Type: Read
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_RXFS

Bits	Name	Description
31:14	RX_FIFO_STATE_MSB	The msb of TX_FIFO_STATE bit field. Only RAM_ADDR_WIDTH +4 +3 -1:14 bits are generated.
13:10	RX_ASYNC_FIFO_STATE	RX asynchronous fifo status - number of characters in the RX asynchronous FIFO.
9:7	RX_BUFFER_STATE	RX packing buffer status - number of bytes in the packing buffer
6:0	RX_FIFO_STATE_LSB	The number of entries in the RX FIFO that have at least one valid character. It is incremented each time a word is moved from the packing register to the RX FIFO. It is decremented each time a word is read from the RX FIFO. Note: The Uart does not keep track of non-valid characters in each word. (See Software procedures).

0x12490090 SPS_GSBI2_UART_DM_TEST_RD_DATA

Type: Read
Clock: AHB_CLK
Reset State: Undefined

SPS_GSBI2_UART_DM_TEST_RD_DATA

Bits	Name	Description
31:0	TEST_RD_DATA	Read from this register triggers the read from the RAM. The register will hold, after read access, data which is found at TEST_RD_ADDR address in the RAM.

20.40 SPS GSBI2 QUP Registers (0x124A0000 SPS_QUP2_BASE)

This section contain Smart Peripheral System GBSI 2 QUP registers.

20.40.1 QUP core registers

0x124A0000 SPS_GSBI2_QUP_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

a. The contents of this register should only be changed when in the RESET_STATE (see the QUP_STATE register).

b. The value written to the QUP output FIFO, is shifted left toward the MSB before passing it to the mini-core as follows:

- N equals 8 or less - shift 24
- N equals 16 to 9 - shift 16
- N equals 24 to 17 - shift 8
- N equals 32 to 25 - no shift

The MINI_CORE clock selected is as follows:

Null: cc_qup_core_clk

SPI: cc_spi_master_clk

SPS_GSBI2_QUP_CONFIG

Bits	Name	Description
31:14	RESERVED_1	reserved
13	CORE_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).
12	APP_CLK_ON_EN	When set to 0, clock on is turned off and driven high unconditionally. When set to 1, dynamic clock on is turned on and driven high conditionally (not applicable for Halcyon).

SPS_GSBI2_QUP_CONFIG (cont.)

Bits	Name	Description
11:8	MINI_CORE	value: 0000 Null core value: 0001 SPI core value: 0010 I2C master controller value: 0011 I2C slave controller value: 0100 Reserved (I2C master & slave for loop back operation) value: 0101 Reserved (map to null core) value: 0110 Reserved (map to null core value: 0111 Reserved (map to null core) See Note 1.
7	NO_INPUT	qup_data_in is not used and the value is a "don't care". The QUP input FIFO is always empty. The input service interrupt and INPUT_SERVICE_FLAG bit are never set. See notes (a) and (b) above.
6	NO_OUTPUT	qup_data_out is not used and is held at the value zero. The QUP output FIFO is always empty. The output service flag and OUTPUT_SERVICE_FLAG bit are never set. qup_data_out is still driven when SPI_CS _N is asserted. The setting for NO_TRI_STATE still applies. See notes (a) and (b) above.
5	RESERVED_2	Reserved.
4:0	N	Number of logical bits N in the mini-core that constitutes a single transfer. The value zero indicates N equals one. The value of all ones indicates N equals 32. The value in this register must be 3 (i.e., N is 4 or higher in order for the STATE field to be set to RUN_STATE). See note (a) above.

0x124A0004 SPS_GSBI2_QUP_STATE

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b0000000000000000_00000000000XX100

SPS_GSBI2_QUP_STATE

Bits	Name	Description
31:5	RESERVED	reserved.
4	I2C_MAST_GEN	Read only. Reflects the RTL generic setting for GEN_I2C_MASTER_MINI_CORE.
3	SPI_GEN	Read only. Reflects the RTL generic setting for GEN_SPI_MINI_CORE.
2	STATE_VALID	Read only. If and only if set to one, writes to the STATE field is allowed or reads from the STATE field is valid. Writes to this bit is ignored.

SPS_GSBI2_QUP_STATE (cont.)

Bits	Name	Description
1:0	STATE	When clear (00), the mini-core and related logic is held in RESET_STATE. When set to "01", the mini-core and related logic is released from reset and enters the RUN_STATE. When set to "11", the mini-core and related logic enters the PAUSE_STATE at the next appropriate point in time. Writing (10) to this field clears these two bits. For PAUSE_STATE to RESET_STATE transition, two writes of (10) are required for the transition to complete. See notes 1 and 2. Note 1: SPI - the "next appropriate point in time" is the next time SPI_CS _N de-asserts. If SPI_CS _N is not asserted when the PAUSE_STATE is entered, the SPI_CS _N is maintained in the not asserted state. The PAUSE_STATE is not available for SLAVE operation. Note 2: I2C -

0x124A0008 SPS_GSBI2_QUP_IO_MODES

Type: Read/write
Clock: CRIF_CLK
Reset State: 0b0000000000000000_00000000XXXXXXXX

Unless otherwise stated, register bits written return the value when read.

Notes:

a. "Packing" occurs as follows:

- N equals 8 or less - pack four values into each QUP input FIFO word.
- N equals 16 to 9 - pack two values into each QUP input FIFO word.
- N equals 32 to 17 - no packing. Each mini-core value is moved to an QUP input FIFO word.

b. "UnPacking" occurs as follows:

- N equals 8 or less - unpack four values from each QUP output FIFO word.
- N equals 16 to 9 - unpack two values from each QUP output FIFO word.
- N equals 32 to 17 - no packing. Each QUP output FIFO value is moved to the mini-core.

SPS_GSBI2_QUP_IO_MODES

Bits	Name	Description
31:17	RESERVED	reserved
16	OUTPUT_BIT_SHIFT_EN	If set, enables the QUP output FIFO block to do bit shifting on the output data.

SPS_GSBI2_QUP_IO_MODES (cont.)

Bits	Name	Description
15	PACK_EN	Indicates data values from the mini-core are to be packed before placement in the QUP input FIFO. See note (a) above.
14	UNPACK_EN	Indicates data values taken from the QUP output FIFO should be unpacked before passing to the mini-core. See note (b) above.
13:12	INPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_INPUT = 0, then only FIFO_Mode is available)
11:10	OUTPUT_MODE	Value 00: FIFO_Mode Value 01: Block_Mode Value 10: Data_Mover_Mode Value 11: Reserved (note if the RTL generic BLOCK_SIZE_OUTPUT = 0, then only FIFO_Mode is available)
9:7	INPUT_FIFO_SIZE	Read only, actual value set by RTL generic. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 6x BLOCK_SIZE
6:5	INPUT_BLOCK_SIZE	Read only. Actual value set by RTL generic. Indicates the block size associated with Block_Mode and Data_Mover_Mode for input. Value 00: 4 Bytes (FIFO_Mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved
4:2	OUTPUT_FIFO_SIZE	Read only. Actual value set by RTL GENERIC. Value 000: 2X BLOCK_SIZE Value 001: 4X BLOCK_SIZE Value 010: 8X BLOCK_SIZE Value 011: 16 BLOCK_SIZE
1:0	OUTPUT_BLOCK_SIZE	Read only. Actual value set by RTL GENERIC. Value 00: 04 Bytes (FIFO mode only) Value 01: 16 Bytes Value 10: 32 Bytes Value 11: Reserved

0x124A000C SPS_GSBI2_QUP_SW_RESET

Type: Write/cmd
Clock: CRIF_CLK
Reset State: 0x0000

A write to this register resets the entire QUP core and all mini-cores. The internal registers are brought back to their reset values. Reading of this register returns zero.

SPS_GSBI2_QUP_SW_RESET

Bits	Name	Description
31:0	RESERVED	NA

0x124A0010 SPS_GSBI2_QUP_TIME_OUT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies if the QUP_MX_OUTPUT_COUNT register and/or QUP_MX_INPUT_COUNT register are enabled. Additionally, this register only applies to Block_Mode and Data_Mover_Mode. The timer starts "ticking" when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The timer pauses for the PAUSE_STATE. If the timer expires before the QUP_MX_OUTPUT_COUNT and/or QUP_MX_INPUT_COUNT are exhausted, then the TIME_OUT_ERR flag is set in the QUP_ERROR_FLAGS register and the interrupt gsbi_qup_irq may be asserted.

SPS_GSBI2_QUP_TIME_OUT

Bits	Name	Description
15:0	TIME_OUT_VALUE	Specifies time out value in units of cc_qup_app clock ticks. A value of zero indicates the timer function is not enabled for use. See QUP_CONFIG register for information on clocks.

0x124A0014 SPS_GSBI2_QUP_TIME_OUT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

SPS_GSBI2_QUP_TIME_OUT_CURRENT

Bits	Name	Description
31:0	TIME_OUT_CURRENT	Current value of time-out counter.

0x124A0018 SPS_GSBI2_QUP_OPERATIONAL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0080

SPS_GSBI2_QUP_OPERATIONAL

Bits	Name	Description
31:10	RESERVED_1	reserved.
13	IN_BLOCK_READ_REQ	Read only. When set by hardware, indicates QUP input FIFO has BLOCK_SIZE_INPUT amount of data ready for reading. Valid only in Block_Mode.
12	OUT_BLOCK_WRITE_REQ	Read only. When set by hardware, indicates QUP output FIFO needs BLOCK_SIZE_OUTPUT amount of data to be written. Valid only in Block_Mode.
11	MAX_INPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP input FIFO has reached the programmed QUP_MX_INPUT_COUNT value. Valid in FIFO_Mode (only if MX_READ_COUNT is non-zero), Block_Mode and Data_Mover_Mode.
10	MAX_OUTPUT_DONE_FLAG	Read only. When set by hardware, indicates QUP output FIFO has reached the programmed QUP_MX_OUTPUT_COUNT value. Valid in Block_Mode and Data_Mover_Mode.
9	INPUT_SERVICE_FLAG	When set by hardware, indicates QUP input FIFO has an outstanding input service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowledges software has or will read the data. Valid only in all modes.
8	OUTPUT_SERVICE_FLAG	When set by hardware, indicates QUP output FIFO has an outstanding output service request. At the point in time this bit is set, the hardware also asserts qup_gsbi_irq. Writing a "zero" to this bit does nothing. Writing a "one" to this bit clears it and acknowledges software has or will read the data. Valid only in all modes.
7	INPUT_FIFO_FULL	Read only. When set, indicates the input FIFO is full and can accept no more data from the QUP mini-core.
6	OUTPUT_FIFO_FULL	Read only. When set, indicates the output FIFO is full and can accept no more CRIF writes.
5	INPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the input FIFO has at least one value in it to be read. When clear, indicates the input FIFO is empty.
4	OUTPUT_FIFO_NOT_EMPTY	Read only. When set, indicates the output FIFO has at least one value in it to be shifted out. When clear, indicates the output FIFO is empty.
3:0	RESERVED_2	reserved.

0x124A001C SPS_GSBI2_QUP_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

SPS_GSBI2_QUP_ERROR_FLAGS

Bits	Name	Description
31:7	RESERVED_1	reserved.
6	TIME_OUT_ERR	The time out limit for a given transfer has been reached.
5	OUTPUT_OVER_RUN_ERR	Indicates the output FIFO was full when a CRIF write was attempted to the FIFO. The write is discarded.
4	INPUT_UNDER_RUN_ERR	Indicates the input FIFO was empty when a CRIF read was attempted to the FIFO. The read value returns is indeterminate.
3	OUTPUT_UNDER_RUN_ER R	Indicates the output FIFO was empty when an output shift operation required a value.
2	INPUT_OVER_RUN_ERR	Indicates the input FIFO was full when an input shift operation provided a new value. When this happens, the new value is discarded.
1:0	RESERVED_2	reserved

0x124A0020 SPS_GSBI2_QUP_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x007C

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of gsbi_qup_irq and the setting of the corresponding error flag in the QUP_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

SPS_GSBI2_QUP_ERROR_FLAGS_EN

Bits	Name	Description
31:7	RESERVED_1	reserved
6	TIME_OUT_ERR_EN	If set, enables time out error generation.
5	OUTPUT_OVER_RUN_ERR _EN	If set, enables output over run error generation.

SPS_GSBI2_QUP_ERROR_FLAGS_EN (cont.)

Bits	Name	Description
4	INPUT_UNDER_RUN_ERR_EN	If set, enables input under run error generation.
3	OUTPUT_UNDER_RUN_ERR_EN	If set, enables output under run error generation.
2	INPUT_OVER_RUN_ERR_EN	If set, enables input over run error generation.
1:0	RESERVED_2	reserved

0x124A0024 SPS_GSBI2_QUP_TEST_CTRL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register enables QUP test bus to be actively driven by QUP core signals.

SPS_GSBI2_QUP_TEST_CTRL

Bits	Name	Description
31:1	RESERVED	reserved
0	QUP_TEST_BUS_EN	If set, enables QUP core to actively drive test bus. If zero, the core drives the test bus to all zeros.

20.40.2 QUP output FIFO registers

0x124A0100 SPS_GSBI2_QUP_MX_OUTPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each output transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not effect the count.

Notes:

a. Allows the total number of Mini Core transfers to be less than an exact multiple of OUTPUT_BLOCK_SIZE. Any additional outputs are discarded.

SPS_GSBI2_QUP_MX_OUTPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_COUNT	Number of writes of size N to the mini-core per RUN_STATE. A value of zero indicates the output count function is not enabled for use. See note (a) above.

0x124A0104 SPS_GSBI2_QUP_MX_OUTPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

SPS_GSBI2_QUP_MX_OUTPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_OUTPUT_CNT_CURRENT	Current value of QUP_MX_OUTPUT_COUNT.

0x124A0108 SPS_GSBI2_QUP_OUTPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

This register holds the output data hanging out of the QUP output FIFO ready be loaded into the mini-core for the next load operation. This corresponds to signal qup_data_out going into the mini-core block.

SPS_GSBI2_QUP_OUTPUT_DEBUG

Bits	Name	Description
31:0	OUTPUT_DEBUG_DATA	Value waiting at the exit of output FIFO.

0x124A010C SPS_GSBI2_QUP_OUTPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the output FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the

value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

SPS_GSBI2_QUP_OUTPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	OUTPUT_FIFO_WORD_CNT	Number of words in the output FIFO.

0x124A0110+4*c SPS_GSBI2_QUP_OUTPUT_FIFOc, c=[0..15]

Type: Write
Clock: CRIF_CLK
Reset State: 0x0000

Note that consecutive writes to this address keeps filling up the output FIFO. The max address to address the output FIFO is 0x14C.

SPS_GSBI2_QUP_OUTPUT_FIFOc

Bits	Name	Description
31:0	OUTPUT	Value to be shifted out.

0x124A0150 SPS_GSBI2_QUP_MX_WRITE_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_OUTPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the gsbi_qup_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_OUTPUT_COUNT register case, the SW should not program the QUP_MX_WRITE_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_OUTPUT * FIFO_SIZE_OUTPUT).

SPS_GSBI2_QUP_MX_WRITE_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_COUNT	The number of "writes" of size N. This is used only if the core is in FIFO_Mode.

0x124A0154 SPS_GSBI2_QUP_MX_WRITE_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

SPS_GSBI2_QUP_MX_WRITE_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_WRITE_CNT_CURRENT	Current value of QUP_MX_WRITE_COUNT counter.

20.40.3 QUP input FIFO registers

0x124A0200 SPS_GSBI2_QUP_MX_INPUT_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read. This register only applies to Block_Mode and Data_Mover_Mode. The counter decrements for each input transfer when the STATE field (see QUP_STATE register) is moved from the RESET_STATE to the RUN_STATE. The PAUSE_STATE doe not affect the count.

Notes:

a. Allows the number of shift register transfers to be less than an exact multiple of INPUT_BLOCK_SIZE. When count reached, remainder of INPUT_BLOCK_SIZE is filled with zeroes.

SPS_GSBI2_QUP_MX_INPUT_COUNT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_COUNT	Number of reads of size N from the mini-core per RUN_STATE. A value of zero indicates the input count function is not enabled for use. See note (a) above.

0x124A0204 SPS_GSBI2_QUP_MX_INPUT_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

SPS_GSBI2_QUP_MX_INPUT_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved.
15:0	MX_INPUT_CNT_CURRENT	Current value of QUP_MX_INPUT_COUNT.

0x124A0208 SPS_GSBI2_QUP_MX_READ_COUNT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

What the QUP_MX_INPUT_COUNT register means to Block_Mode and Data_Mover_Mode, this register means the same to FIFO_mode. If this register is non-zero, then the qup_input_service_irq is asserted after shifting in the number of shifts specified by this register.

Unlike the QUP_MX_INPUT_COUNT register case, the SW should not program the QUP_MX_READ_COUNT value to be more than the "actual depth" of the FIFO (BLOCK_SIZE_INPUT * FIFO_SIZE_INPUT). If the SPI mini-core and slave operation is enabled, then an InputOverRun error will result.

SPS_GSBI2_QUP_MX_READ_COUNT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_COUNT	The number of "reads" of size N. This is used only if the core is in FIFO_Mode.

0x124A020C SPS_GSBI2_QUP_MX_READ_CNT_CURRENT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

SPS_GSBI2_QUP_MX_READ_CNT_CURRENT

Bits	Name	Description
31:16	RESERVED	reserved
15:0	MX_READ_CNT_CURRENT	Current value of QUP_MX_READ_COUNT counter.

0x124A0210 SPS_GSBI2_QUP_INPUT_DEBUG

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the value of the last loaded in known-good-data into the QUP input FIFO. May be different from what the actual read of input FIFO will return because of packing enabled at the input side. This corresponds to signal qup_data_in coming from the mini-core block synchronized to the crif_clk.

SPS_GSBI2_QUP_INPUT_DEBUG

Bits	Name	Description
31:0	INPUT_DEBUG_DATA	Last known good value shifted into the input FIFO.

0x124A0214 SPS_GSBI2_QUP_INPUT_FIFO_WORD_CNT

Type: Read
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the number of words in the input FIFO at a given time. Note the fields in this register are dynamically updated hence when this register is read during a FIFO operation, the value of this register could have been altered by the time SW gets the read value. Recommended for debug purposes.

SPS_GSBI2_QUP_INPUT_FIFO_WORD_CNT

Bits	Name	Description
31:9	RESERVED	reserved
8:0	INPUT_FIFO_WORD_CNT	Number of words in the input FIFO.

0x124A0218+4*c SPS_GSBI2_QUP_INPUT_FIFOc, c=[0..15]

Type: Read
Clock: CRIF_CLK
Reset State: 0xXXXX

Consecutive reads to this address reads the input FIFO contents on a FIFO basis.The max address to read the input FIFO is 0x254.

SPS_GSBI2_QUP_INPUT_FIFOc

Bits	Name	Description
31:0	INPUT	Value shifted in.

20.40.4 SPI mini-core registers

0x124A0300 SPS_GSBI2_SPI_CONFIG

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

Unless otherwise stated, register bits written return the value when read.

The contents of this register should only be changed when in the RESET_STATE. See the QUP_STATE register. Both NO_OUTPUT and NO_INPUT set to zero provides default full duplex operation. Setting both these bits to one is not a legal operational state.

SPS_GSBI2_SPI_CONFIG

Bits	Name	Description
31:11	RESERVED_1	Reserved.
10	HS_MODE	When set, SPI HS_MODE is enabled. When clear, SPI HS_MODE is disabled.
9	INPUT_FIRST	When set, INPUT FIRST SPI protocol is used. When clear, OUTPUT FIRST SPI protocol is used.
8	LOOP_BACK	Loopback is only valid in non-HS mode. Always clear for normal operation. If set, loop back on SPI_DATA_MO_SI under MASTER operation or SPI_DATA_MI_SO under SLAVE operation.
7:6	RESERVED_2	Reserved.
5	SLAVE_OPERATION	This register is writable only when the hardware signal spi_slave_en is asserted. When set, the SPI is configured for SLAVE operation. Zero indicates MASTER operation.
4:0	RESERVED	Reserved.

0x124A0304 SPS_GSBI2_SPI_IO_CONTROL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The contents of this register should only be changed when in the RESET_STATE.

Unless otherwise stated, register bits written return the value when read.

SPS_GSBI2_SPI_IO_CONTROL

Bits	Name	Description
31:11	RESERVED	Reserved.
10	CLK_IDLE_HIGH	Use SPI_CLK_IDLE_HIGH when set.
9	CLK_ALWAYS_ON	When MASTER operation is used, run SPI_CLK during IDLE.
8	MX_CS_MODE	If this bit is set, then for a given RUN state, the associated chip select will be asserted for the first N-bit transfer and will be kept asserted till the last programmed transfer. Applies only in MASTER mode. The number of transfers is determined by SPI_MX_OUTPUT_COUNT and/or SPI_MX_INPUT_COUNT registers.
7:4	CS_N_POLARITY	These four bits control the polarity of four SPI_CS _N respectively. Setting any of this bit to '1', makes the associated SPI_CS _N active HIGH. This field is a "don't care" in SLAVE operation.
3:2	CS_SELECT	When MASTER operation is used, controls the assertion of SPI_CS_ N pins. Selects SPI_CS_N if 00, SPI_CS1_N if 01, SPI_CS2_N if 10, or SPI_CS3_N if 11. The deselected ChipSelects will be driven to inactive state dictated by the field CS_N_POLARITY. This field is a "don't care" in SLAVE operation.
1	TRISTATE_CS	When set, drives Z on all SPI_CS _N lines. When clear, enables normal functionality on these lines. This bit can be used to support deployment of the core as one of the masters in a multi-master configuration.
0	NO_TRI_STATE	When set, spi_data_out is not taken tri-state when SPI_CS _N is de-asserted. This bit is normally set for MASTER operation but may be optionally left cleared.

0x124A0308 SPS_GSBI2_SPI_ERROR_FLAGS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

All bits in this register are set by hardware and remain set until cleared by software. Writing a "one" to a bit clears it while writing a "zero" leaves the bit unchanged.

SPS_GSBI2_SPI_ERROR_FLAGS

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.

SPS_GSBI2_SPI_ERROR_FLAGS (cont.)

Bits	Name	Description
1	SPI_SLV_CLK_OVER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was greater than the programmed value of N. When this happens, only the first N bits are passed to the SPI input FIFO and the output shift value is held at zero.
0	SPI_SLV_CLK_UNDER_RUN_ERR	Number of SPI_CLK ticks which occurred while SPI_CS _N was asserted was less than the programmed value of N. When this occurs, the bits which were received are passed to the SPI input FIFO and the CURRENT output bit is forced to zero.

0x124A030C SPS_GSBI2_SPI_ERROR_FLAGS_EN

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0003

Each bit in this register controls the setting of a corresponding error flag. If set, each bit enables generation of spi_error_irq and the setting of the corresponding error flag in the SPI_ERROR_FLAGS register for the specified error case. At reset, all error enable bits are set to `1'.

SPS_GSBI2_SPI_ERROR_FLAGS_EN

Bits	Name	Description
31:2	RESERVED	Reserved. Writes are a "don't care" but by convention always write zero. Reads always return the value zero.
1	SPI_SLV_CLK_OVER_RUN_ERR_EN	If set, enables clock over run error generation.
0	SPI_SLV_CLK_UNDER_RUN_ERR_EN	If set, enables clock under run error generation.

0x124A0310 SPS_GSBI2_SPI_DEASSERT_WAIT

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

This register holds the de-assertion wait time of SPI_CS _N between consecutive N-bit transfers in MASTER operation. The wait time is specified in number of cycles of cc_spi_master_clk.

SPS_GSBI2_SPI_DEASSERT_WAIT

Bits	Name	Description
31:6	RESERVED	Reserved.

SPS_GSBI2_SPI_DEASSERT_WAIT (cont.)

Bits	Name	Description
5:0	DEASSERT_WAIT	Number cc_spi_master_clk ticks associated with the de-asserted time of SPI_CS _N. Only applies to MASTER operation. For SLAVE operation, this field is a "don't care". A value of zero indicates SPI_CS _N remains de-asserted for exactly one clock tick. A value of one, indicates two ticks, etc. All ones indicates 64 ticks.

20.40.5 I2C master mini-core registers

0x124A0400 SPS_GSBI2_I2C_MASTER_CLK_CTL

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_CLK_CTL register is a read/write register that controls clock divider values. This register should only be written to after it is confirmed that the I2C master mini-core is not longer in RESET state (QUP_STATE register).

SPS_GSBI2_I2C_MASTER_CLK_CTL

Bits	Name	Description
31:11	RESERVED	Reserved.
10:8	HS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in high-speed (HS) mode. The minimum value should be 3 hex (4 I2C_clk clocks per period) to ensure proper sampling of the bus. For a maximum high speed bit rate of 3.4 Mb/s (high speed mode), this would require a minimum 40.8 MHz I2C_clk clock. The maximum I2C_clk is 81.6 MHz. This register is reset to a maximum value of 7 hex. I2C_HS_CLK = I2C_CLK/(3*(HS_DIVIDER_VALUE+1)
7:0	FS_DIVIDER_VALUE	The value in this register represents the clock period multiplier in fast/standard (FS) mode. The minimum value should be 3 hex to ensure proper sampling of the bus. For a maximum bit rate of 400 kb/s (fast mode), this would require a 4.8 MHz I2C_clk clock. For a maximum bit rate of 100 kb/s (standard mode), this would require a 1.2 MHz I2C_clk clock. Maximum I2C_clk for fast and standard modes are 206.4 MHz and 51.6 MHz respectively. This register is reset to a maximum value of 255 hex. I2C_FS_CLK = I2C_CLK/(2*(FS_DIVIDER_VALUE+3)

0x124A0404 SPS_GSBI2_I2C_MASTER_STATUS

Type: Read/write
Clock: CRIF_CLK
Reset State: 0x0000

The I2C_STATUS is a status register. Writing a one clears the status bits.

SPS_GSBI2_I2C_MASTER_STATUS

Bits	Name	Description
31:26	RESERVED_1	Reserved.
25	INVALID_READ_SEQ	This bit is set (1) when a MI_REC tag does not follow a START tag for an I2C READ. Not applicable for Halcyon.
24	INVALID_READ_ADDR	This bit is set (1) when the I2C controller is trying to receive data from a non-existent I2C slave (address).
23	INVALID_TAG	This bit is set (1) when the I2C controller is trying to process data from the output FIFO that is improperly tagged.
22:20	INPUT_FSM_STATE	This 3-bit field informs the microprocessor of the state of the I2C MASTER INPUT FSM block. Reset, read_last_byte, mi_rec, dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: READ_LAST_BYTE_STATE Value 0x3: MI_REC_STATE Value 0x4: DEC_STATE Value 0x5: STORE_STATE
19:16	OUTPUT_FSM_STATE	This 4-bit field informs the microprocessor of the state of the I2C MASTER OUTPUT FSM block. Reset, decode, send, mi_red, nop, nop_dec, invalid, invalid_dec. Value 0x0: RESET_STATE Value 0x1: IDLE_STATE Value 0x2: DECODE_STATE Value 0x3: SEND_STATE Value 0x4: MI_REC_STATE Value 0x5: NOP_STATE Value 0x6: INVALID_STATE Value 0x7: PEEK_STATE Value 0x8: SEND_R_STATE

SPS_GSBI2_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
15:13	CLK_STATE	This 3-bit field informs the microprocessor of the state of the I2C clk_control block. Reset_busidle, not_master, high, low, high_wait, forced_low, hs_addr_low or double_buffer_wait. Value 0x0: RESET_BUSIDLE_STATE Value 0x1: NOT_MASTER_STATE Value 0x2: HIGH_STATE Value 0x3: LOW_STATE Value 0x4: HIGH_WAIT_STATE Value 0x5: FORCED_LOW_STATE Value 0x6: HS_ADDR_LOW_STATE Value 0x7: DOUBLE_BUFFER_WAIT_STATE
12:10	DATA_STATE	This 3-bit field informs the microprocessor of the state of the I2C data_control block. Reset, Tx addr, Tx HS addr, Tx 10-bit addr, Tx 2nd 10-bit addr byte, Tx data and Rx data. Value 0x0: RESET_WAIT_STATE Value 0x1: TX_ADDR_STATE Value 0x2: TX_DATA_STATE Value 0x3: TX_HS_ADDR_STATE Value 0x4: TX_10_BIT_ADDR_STATE Value 0x5: TX_2ND_BYTE_STATE Value 0x6: RX_DATA_STATE
9	BUS_MASTER	This bit is set (1) when the I2C controller is the present bus master.
8	BUS_ACTIVE	This bit is set (1) when the bus is in use by this, or any other controller.
7:6	FAILED	This 2-bit field contains the failure information of the present I2C transfers. If transmitting, failed[1] contains the information regarding the byte that has been transmitted. Failed[0] contains the information of the byte awaiting transmission if there is a byte pipelined. If no byte is pipelined, ignore this bit. If receiving, failed[1] contains the information of the byte received and stored in the buffer, and failed[0] should be ignored. For example: Value 00: Byte n transmitted successfully, byte n+1 to begin transmission Value 01: Byte n transmitted successfully, byte n+1 errored: type of error indicated in other STATUS bits. (queued invalid write, for example) Value 10: Byte n errored: type of error indicated in other STATUS bits, byte n+1 to begin transmission (byte n+1 would have to be a valid address byte for this condition to occur) Value 11: Byte n errored: type of error indicated in other STATUS bits, byte n+1 discarded as well (if the byte was a data byte destined for a NACKed address, data is useless, therefore discarded)
5	INVALID_WRITE	This bit is set (1) when software writes data to the I2C_DATA register that should be flagged as an address but is not.

SPS_GSBI2_I2C_MASTER_STATUS (cont.)

Bits	Name	Description
4	ARB_LOST	This bit is set (1) when the controller loses arbitration for the bus. If this bit gets set (1) during the transmission, all data has been lost, and the microprocessor must re-request its transmission.
3	PACKET_NACKED	This bit is set high when a NACK is received from a slave. If a high speed master code is sent and there is an ACK from a slave, then this bit is set (1) to indicate that the high speed mode can not be entered. If the high speed mode is accepted by the slave, then a NACK is performed and this bit is not set (1).
2	BUS_ERROR	This bit is set (1) when an unexpected START or STOP condition is detected. This returns the controller to its reset state.
1:0	RESERVED_2	Reserved.

20.41 PP SS Interrupt Controller Registers (0x12080000 PPSS_BASE)

This section contains Peripheral Process Subsystem (PPSS) Interrupt Controller registers.

-- The interrupt sources (irq/fiq_source) are defined as:

-- intsource(15) is controlled by a software register within the interrupt controller.

intsource(14 DOWNTO 12) <=

ppss_int_cntl; -- PPSS top-level inputs

intsource(11 DOWNTO 0) <=

'0' & -- Spare input bit 11

rpm_dsps_gp_high_irq & -- RPM bit 10

rpm_dsps_gp_med_irq & -- RPM bit 9

rpm_dsps_gp_low_irq & -- RPM bit 8

rpm_dsps_wakeup_irq & -- RPM bit 7

ppss_wdog_bark_irq_loc & -- Watchdog bit 6

int_gp1 & -- General Purpose Outputs bit 5

int_gp0 & -- General Purpose Inputs bit 4

ppss_tmr11_irq & -- Sleep Timer 1 bit 3

ppss_tmr10_irq & -- Sleep Timer 0 bit 2

ppss_tmr01_irq & -- XO Timer 1 bit 1

ppss_tmr00_irq; -- XO Timer O bit 0

0x12080000 IRQSTATUSA

Type: Read
Clock: PPSS_PCLK
Reset State: 0x0000

IRQSTATUSA

Bits	Name	Description
15:0	STATUS	Returns the state of the interrupt sources after they have been masked by the bits stored in the IRQENABLESETA register. IRQSTATUSA <= IRQRAWSTATUSA AND IRQENABLESETA

0x12080004 IRQRAWSTATUSA

Type: Read
Clock: PPSS_PCLK
Reset State: 0x0000

IRQRAWSTATUSA

Bits	Name	Description
15:0	RAWSTATUS	Returns the state of the internal IRQSOFTA register bit concatenated with the 15 interrupt inputs. IRQRAWSTATUSA <= IRQSOFTA & irq_source

0x12080008 IRQENABLESETA

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x0000

16 interrupts are formed by concatenating the internal IRQSOFTA register bit with the 15 interrupt inputs listed at the start of this section.

irq_interrupts <= IRQSOFTA & irq_source(14 DOWNTO 0).

By default all 16 interrupts are masked out. To enable a particular interrupt, the corresponding bit within the IRQENABLESETA register must be set to logic `1'. Writing 0xFFFF to this register enables all irq_interrupts.

Each input bit of this register is ORed with the corresponding register output bit.

This is done so that the state of any set bit is automatically maintained and does not need to be rewritten. This saves processor time as it prevents the software from having to perform a read modify write cycle when updating this register.

Once an interrupt bit has been enabled, it cannot be disabled by writing a `0' to this register due to the ORed feedback connections. To disable an interrupt, the IRQENABLECLEARA register must be used, i.e., writing to the IRQENABLESETA address sets bits within the interrupt enable register while writing to the IRQENABLECLEARA address clears them.

After the 16 irq_interrupts have been masked they are NORed together and output as a single internal active low interrupt request (irq_n).

IRQENABLESETA

Bits	Name	Description
15:0	ENABLESET	To enable an interrupt, set the corresponding bit within this register to a `1'. Writing zeros to this address does not change the state of the register output. Write to the IRQENABLECLEARA address to clear bits within this register

0x1208000C IRQENABLECLEARA

Type: Write
Clock: PPSS_PCLK
Reset State: 0x0000

IRQENABLECLEARA

Bits	Name	Description
15:0	ENABLECLEAR	To understand the function of the ENABLECLEAR bits, the IRQENABLESETA register description must be read first. Writing a logic `1' to any of the 16 data bits at this address clears the corresponding data bit within the IRQENABLESETA register. Writing 0xFFFF to this address clears the entire IRQENABLESETA register and thereby masks all irq_interrupts.

0x12080010 IRQSOFTA

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x0

IRQSOFTA

Bits	Name	Description
0	SOFT	Software programmable test interrupt. Sets the upper irq_interrupt bit, i.e., bit 15.

0x12080100 FIQSTATUSA

Type: Read
Clock: PPSS_PCLK
Reset State: 0x0000

FIQSTATUSA

Bits	Name	Description
15:0	STATUS	Returns the state of the interrupt sources after they have been masked by the bits stored in the FIQENABLESETA register. FIQSTATUSA <= FIQRAWSTATUSA AND FIQENABLESETA

0x12080104 FIQRAWSTATUSA

Type: Read
Clock: PPSS_PCLK
Reset State: 0x0000

FIQRAWSTATUSA

Bits	Name	Description
15:0	RAWSTATUS	Returns the state of the internal FIQSOFTA register bit concatenated with the 15 interrupt inputs. FIQRAWSTATUSA <= FIQSOFTA & fiq_source

0x12080108 FIQENABLESETA

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x0000

16 interrupts are formed by concatenating the internal FIQSOFTA register bit with the 15 interrupt inputs listed at the start of this section.

fiq_interrupts <= FIQSOFTA & fiq_source(14 DOWNTO 0).

By default all 16 interrupts are masked out. To enable a particular interrupt, the corresponding bit within this register must be set to logic `1'. Writing 0xFFFF to this register enables all fiq_interrupts.

Each input bit of this register is ORed with the corresponding register output bit.

This is done so that the state of any set bit is automatically maintained and does not need to be rewritten. This saves processor time as it prevents the software from having to perform a read modify write cycle when updating this register.

Once an interrupt bit has been enabled, it cannot be disabled by writing a `0' to this register due to the ORed feedback connections. To disable an interrupt the FIQENABLECLEARA register must

be used, i.e., writing to the FIQENABLESETA address sets bits within the interrupt enable register while writing to the IRQENABLECLEARA address clears them.

After the 16 fiq_interrupts have been masked they are NORed together and output as a single internal active low interrupt request (fiq_n).

FIQENABLESETA

Bits	Name	Description
15:0	ENABLESET	To enable an interrupt, set the corresponding bit within this register to a `1'. Writing zeros to this address does not change the state of the register output. Write to the FIQENABLECLEARA address to clear bits within this register..

0x1208010C FIQENABLECLEARA

Type: Write
Clock: PPSS_PCLK
Reset State: 0x0000

FIQENABLECLEARA

Bits	Name	Description
15:0	ENABLECLEAR	To understand the function of the ENABLECLEAR bits, the FIQENABLESETA register description must be read first. Writing logic `1' to any of the 16 data bits at this address clears the corresponding data bit within the FIQENABLESETA register. Writing 0xFFFF to this address clears the entire FIQENABLESETA register and thereby masks all fiq_interrupts.

0x12080110 FIQSOFTA

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x0

FIQSOFTA

Bits	Name	Description
0	SOFT	Software programmable test interrupt. Sets the upper fiq_interrupt bit, i.e., bit 15.

20.42 PP SS Timer Registers (0x12080000 PPSS_BASE)

This section contains Peripheral Process Subsystem (PPSS) Timer registers.

The Timer Blocks run at different frequencies. Timer Block 0 is clocked by a XO (approximately 20MHz), whilst Timer Block 1 is clocked at 32KHz (referred to as SLP (sleep) in the register name prefixes). Hence, there are a total of 4 counters available in the PPSS, with 2 counters running at the Timer Block 0 frequency and another 2 counters running at the Timer Block 1 frequency.

Each of the two PPSS Timers Blocks have two duplicate sets of registers, one for each of the two 32-bit counters. Rather than repeat identical descriptions for each entry, the following list uses notation that defines the register as belonging to TMRn, where n represents either 0 or 1.

0x12080800+ 0x18*n XO_TMRn_MATCH_VAL, n=[0..1]

Type: Read/Write
Clock: PPSS_TIMER0_CLK_24_576_OR_27MHZ_
Reset State: 0x00000000

XO_TMRn_MATCH_VAL

Bits	Name	Description
31:0	MATCH_VAL	An interrupt is generated when the counter output equals the value stored in the match value register Reading this register returns the value of the Match register located in the APB clock domain rather than the XO clock domain..

0x12080804+ 0x18*n XO_TMRn_COUNT_VAL, n=[0..1]

Type: Read/Write
Clock: PPSS_TIMER0_CLK_24_576_OR_27MHZ_
Reset State: 0x00000000

Count Write

The count value is writable as a test/debug only feature. The value written to this address is loaded into the XO_TMRn_MATCH_VAL register due to HW reuse. The procedure for writing the XO_TMRn_COUNT_VAL is as follows:

1. Write to the XO_TMRn_CONTROL register to set the required mode and pre-scale counter frequency.
2. Set the timer ON/OFF control bit 5 to `1' and prevent the timer from counting by setting the timer enable (EN) bit 4 to `0'.

The XO_TMRn_STATUS register bit 2 (CONTROL_UPDATE) returns low once the data written to the control register has been synchronized to the XO clock domain.

3. Read this status bit and do not proceed until it is low.
4. Write the required counter value to the XO_TMRn_COUNT_VAL address.

NOTE This value is loaded into the XO_TMRn_MATCH register.

XO_TMRn_STATUS register bit 3(COUNT_UPDATE) returns low once the written value has been loaded into the counter.

5. If required the original Match value can now be restored by writing directly to the XO_TMRn_MATCH_VAL address.

Count Read

The counter increments at the pre-scaled timer clock rate set within the XO_TMRn_Control register. The AHB clock is used to detect the rising edge of the slower pre-scaled XO clock. Each time a rising edge is detected, the XO counter output is copied to a 32-bit register within the APB clock domain. Constantly updating this register ensures that the processor does not have to be stalled each time the counter value is read, i.e., the synchronization delay is eliminated. The disadvantage of this synchronization technique is that it takes time for the counter value to be synchronized when the timer is initially enabled. In addition, if the AHB clock is switched off to save power the counter value becomes stale or invalid when the AHB clock is first restored. To overcome these limitations the software must either allow time for the counter value to be synchronized or take repeated readings and wait for the counter value to be updated.

XO_TMRn_COUNT_VAL

Bits	Name	Description
31:0	COUNT	The current counter value.

0x12080808+ 0x18*n XO_TMRn_CONTROL, n=[0..1]

Type: Read/Write
Clock: PPSS_TIMER0_CLK_24_576_OR_27MHZ_
Reset State: 0x00

The software should not write to the CONTROL register while the CONTROL_UPDATE status register bit is set. If this occur, the XO timer circuitry delays the second write cycle until the first write has completed. The insertion of wait states ensures that the control register cannot be updated while the contents are being copied from the APB to XO clock domain.

Three modes of operation are provided. The mode of operation determines how the timer behaves once the counter reaches the value stored in the match register:

- FREE_RUN - the counter continues counting. Once the up-counter reaches the maximum value the counter resets to zero and counting then continues.
- ONE_SHOT - the counter resets to zero and stops counting.

- PERIODIC - the counter resets to zero and counting then continues. This periodic process continues until the timer register settings are changed. When using this mode, the match value register must not be loaded with too low a value as it is impossible to clear the interrupt output before the next interrupt is generated.

Reading this register returns the value of the Control register located in the APB clock domain rather than the XO clock domain.

NOTE Due to the synchronization scheme used in the XO timers, the prescale counter must be set so that the timer clock always runs at least 4x slower than the AHB clock. The prescale clock frequency must be set and the timer switched ON before any of the other registers associated with the timer can be used.

XO_TMRn_CONTROL

Bits	Name	Description
5	ON	Timer ON/OFF When the timer is not in use, it should be switched OFF. This holds the prescale counter in reset which stops the clock and saves power. 0x0: OFF 0x1: ON
4	EN	Timer Enable, When set to (1) the timer counts at the prescale clock rate. 0x0: Disable 0x1: Enable
3:2	MODE	Timer Mode, 0x0: FREE_RUN 0x1: ONE_SHOT 0x2: PERIODIC 0x3: RESERVED
1:0	PRESCALE	Pre_scale clock frequency The division ratio must be set so that the pre-scale clock frequency is always at least 4x slower than the AHB clock frequency. Unless greater timer accuracy is required the division ratio should be left at the default setting of DIV32 as this saves power. 0x0: DIV32 0x1: DIV8 0x2: DIV4 0x3: DIV2

0x1208080C+ 0x18*n XO_TMRn_CLEAR_INT, n=[0..1]

Type: Write (command)
Clock: PPSS_TIMER0_CLK_24_576_OR_27MHZ_
Reset State: 0x0

XO_TMRn_CLEAR_INT

Bits	Name	Description
0	CLEAR_INT	This register is a one-shot command register that, when written with any value, resets the interrupt.

0x12080810+ 0x18*n XO_TMRn_CLEAR_CNT, n=[0..1]

Type: Write (command)
Clock: PPSS_TIMER0_CLK_24_576_OR_27MHZ_
Reset State: 0x0

XO_TMRn_CLEAR_CNT

Bits	Name	Description
0	CLEAR_CNT	This register is a one-shot command register that, when written with any value, resets the COUNT_VAL to 0. This occurs regardless of the state of the EN bit within the TMR0/1_CONTROL register.

0x12080814+ 0x18*n XO_TMRn_STATUS, n=[0..1]

Type: Read
Clock: PPSS_TIMER0_CLK_24_576_27MHZ_
Reset State: 0x00

As the advanced peripheral bus (APB) runs at a different clock frequency to the XO timers, it takes time to synchronize data between the two clock domains. The actual synchronization delay depends on the pre-scale timer setting. The TMRn_STATUS register allows the software to track the progress of each synchronized write command.

The XO Control register can synchronize faster than the other registers so it is important that the software checks this status information to ensure the timer registers are written in the correct sequence. Note that if the Match or Control registers are read, the values are returned from the registers located within the APB clock domain rather than the sleep clock domain. As a result, the status register must be used to determine when the Match or Control registers within the sleep clock domain have been updated.

XO_TMRn_STATUS

Bits	Name	Description
4	MATCH_UPDATE	0x0: Register write completed 0x1: Register updating
3	COUNT_UPDATE	0x0: Register write completed 0x1: Register updating
2	CONTROL_UPDATE	0x0: Register write completed 0x1: Register updating
1	CLR_INT_UPDATE	0x0: Register write completed 0x1: Register updating
0	CLR_CNT_UPDATE	0x0: Register write completed 0x1: Register updating

0x12081000+ 0x18*n SLP_TMRn_MATCH_VAL, n=[0..1]

Type: Read/Write
Clock: PPSS_TIMER1_CLK_32KHZ_
Reset State: 0x00000000

SLP_TMRn_MATCH_VAL

Bits	Name	Description
31:0	MATCH_VAL	An interrupt is generated when the counter output equals the value stored in the match value register. Reading this register returns the value of the Match register located in the APB clock domain rather than the sleep clock domain.

0x12081004+ 0x18*n SLP_TMRn_COUNT_VAL, n=[0..1]

Type: Read/Write
Clock: PPSS_TIMER1_CLK_32KHZ_
Reset State: 0x00000000

Count Write

The count value is writable as a test/debug only feature. The value written to this address is loaded into the SLP_TMRn_MATCH_VAL register due to HW reuse. The procedure for writing the TMRn_COUNT_VAL is as follows:

1. Disable the timer by clearing the EN bit within the SLP_TMRn_CONTROL register.

The SLP_TMRn_STATUS register bit 2 (CONTROL_UPDATE) returns low once the data written to the control register has been synchronized to the SLP clock domain.

2. Read this status bit and do not proceed until it is low.
3. Write the required counter value to the SLP_TMRn_COUNT_VAL address.

Note that this value is loaded into the SLP_TMRn_MATCH register.

SLP_TMRn_STATUS register bit 3 (COUNT_UPDATE) returns low once the written value has been loaded into the counter.

4. If required the original Match value can now be restored by writing directly to the SLP_TMRn_MATCH_VAL register.

Count Read

The counter increments at the sleep clock rate. The AHB clock is used to detect the falling edge of the slower sleep clock. Each time a falling edge is detected, the SLP counter output is copied to a 32-bit register within the APB clock domain. Constantly updating this register ensures that the processor does not have to be stalled each time the counter value is read, i.e., the synchronization delay is eliminated. The disadvantage of this synchronization technique is that it takes time for the counter value to be synchronized when the timer is initially enabled. In addition, if the AHB clock is switched off to save power, the counter value becomes stale or invalid when the AHB clock is first restored. To overcome these limitations, the software must either allow time for the counter value to be synchronized or take repeated readings and wait for the counter value to be updated.

SLP_TMRn_COUNT_VAL

Bits	Name	Description
31:0	COUNT	The current counter value.

0x12081008+ 0x18*n SLP_TMRn_CONTROL, n=[0..1]

Type: Read/Write
Clock: PPSS_TIMER1_CLK_32KHZ_
Reset State: 0x00

Three modes of operation are provided. The mode of operation determines how the timer behaves once the counter reaches the value stored in the match register:

- FREE_RUN - the counter continues counting.

Once the up-counter reaches the maximum value, the count resets to zero and counting then continues.

- ONE_SHOT - the counter resets to zero and stops counting.
- PERIODIC - the count resets to zero and counting then continues.

This periodic process continues until the timer register settings are changed. When using this mode, the match value register must not be loaded with too low a value as it is impossible to clear the interrupt output before the next interrupt is generated.

Reading this register returns the value of the Control register located in the APB clock domain rather than the sleep clock domain.

SLP_TMRn_CONTROL

Bits	Name	Description
4	EN	Timer Enable, 0x0: Disable 0x1: Enable
3:2	MODE	Timer Mode, 0x0: FREE_RUN 0x1: ONE_SHOT 0x2: PERIODIC 0x3: RESERVE
1:0	RESERVED_2	The sleep timers do not provide a pre-scale counter facility.

0x1208100C+ 0x18*n SLP_TMRn_CLEAR_INT, n=[0..1]

Type: Write (command)
Clock: PPSS_TIMER1_CLK_32KHZ_
Reset State: 0x0

SLP_TMRn_CLEAR_INT

Bits	Name	Description
0	CLEAR_INT	This register is a one-shot command register that, when written with any value, resets the interrupt.

0x12081010+ 0x18*n SLP_TMRn_CLEAR_CNT, n=[0..1]

Type: Write (command)
Clock: PPSS_TIMER1_CLK_32KHZ_
Reset State: 0x0

SLP_TMRn_CLEAR_CNT

Bits	Name	Description
0	CLEAR_CNT	This register is a one-shot command register that, when written with any value, resets the COUNT_VAL to 0. This occurs regardless of the state of the EN bit within the SLP_TMRn_CONTROL register.

0x12081014+0x18*n SLP_TMRn_STATUS, n=[0..1]

Type: Read
Clock: PPSS_TIMER1_CLK_32KHZ_
Reset State: 0x00

As the advanced peripheral bus (APB) runs at a different clock frequency to the sleep timers ,it takes time to synchronize data between the two clock domains. The actual synchronization delay depends on which register is being synchronized (refer to the HDD for timing details). The SLP_TMRn_STATUS register allows the software to track the progress of each synchronized write command. Note that if the Match or Control registers are read, the values are returned from the registers located within the APB clock domain rather than the sleep clock domain. As a result the status register must be used to determine when the Match or Control registers within the sleep clock domain have been updated.

SLP_TMRn_STATUS

Bits	Name	Description
4	MATCH_UPDATE	0x0: Register write completed 0x1: Register updating
3	COUNT_UPDATE	0x0: Register write completed 0x1: Register updating
2	CONTROL_UPDATE	0x0: Register write completed 0x1: Register updating
1	CLR_INT_UPDATE	0x0: Register write completed 0x1: Register updating
0	CLR_CNT_UPDATE	0x0: Register write completed 0x1: Register updating

0x12081800 PPSS_WDOG_RESET

Type: Write
Clock: PPSS_PCLK
Reset State: 0x0

The PPSS_WDOG_RESET register resets the watch dog counter. In normal operation, the microprocessor should periodically write this command register to reset watchdog. This command register also disables the watchdog freeze.

PPSS_WDOG_RESET

Bits	Name	Description
0	WDOG_RESET	This bit generates the WDOG_STB during the non-sleep mode. A pulse is generated on WDOG_STB when this bit is written with a `1'.

0x12081804 PPSS_WDOG_FREEZE

Type: Write/Command
Clock: PPSS_PCLK
Reset State: 0x0

NOTE This register is only needed for backward compatible power-on sleep, not for power-collapsed sleep.

The PPSS_WDOG_FREEZE register freezes the watchdog timer at count 0. The microprocessor should write this register before it goes to power-on sleep to avoid a watchdog timeout during sleep. This register is reset by setting the PPSS_WDOG_RESET register.

PPSS_WDOG_FREEZE

Bits	Name	Description
0	WDOG_FREEZE	This bit is used to freeze the watchdog timer at count 0. To enable the watchdog timer auto-kicker, write a '1'.

0x12081808 PPSS_WDOG_UNMASKED_INT_EN

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x0

The PPSS_WDOG_UNMASKED_INT_EN register enables unmasked IRQs and FIQs to enable the watch dog.

PPSS_WDOG_UNMASKED_INT_EN

Bits	Name	Description
1	ENABLE	Enable wdog timer Do not enable wdog timer 0x1: enable 0x0: don't enable
0	UNMASKED_INT_ENABLE	Unmasked IRQ or FIQ enables wdog timer Unmasked IRQ or FIQ does not enable wdog timer 0x1: enable 0x0: don't enable

0x1208180C PPSS_WDOG_STATUS

Type: Read
Clock: PPSS_PCLK
Reset State: 0x4

The PPSS_WDOG_STATUS register is the watchdog status register.

PPSS_WDOG_STATUS

Bits	Name	Description
16:3	WDOG_COUNT	Counter value [13:0] of watch dog counter. NOTE The sleep counter value is synchronized to the APB clock domain by transferring data on the falling edge of the sleep clock.
2	WDOG_CNT_RESET_STATUS	Show the status of wdog_res signal (for test).
1	WDOG_FROZEN	This bit indicates whether wdog is frozen at count `0'. 0x1: frozen 0x0: not frozen
0	WDOG_EXPIRED_STATUS	Watchdog timer has expired. Wdog timer has not expired. 0x1: expired 0x0: not expired

0x12081810 PPSS_WDOG_EXPIRED_WIDTH

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0xC7C

The PPSS_WDOG_EXPIRED_WIDTH register defines the width of the wdog_expired pulse in the number of sleep_clk cycles. The default value is 0x0C7C = 3196.

PPSS_WDOG_EXPIRED_WIDTH

Bits	Name	Description
14	SYNC_STATUS	When set (1), the wdog expired width data is synchronizing to SLEEP_CLK. The data value is not guaranteed until the SYNC_STATUS bit is clear (0). This bit is read only.
13:0	DATA	Wdog counter value to de-assert the wdog_expired pulse. The wdog counter is14 bits.

0x12081814 PPSS_WDOG_BARK_TIME

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x3FFF

The PPSS_WDOG_BARK_TIME register defines the time in sleep_clk when to assert the watchdog ("bark") interrupts. The value can be between 1and 12787 (the time when the watchdog times out). The default value is 0x3FFF, which is larger than the watchdog timeout of 0x31F3, effectively disabling the watchdog ("bark") interrupt.

NOTE A bark time of 0x0 is not allowed.

PPSS_WDOG_BARK_TIME

Bits	Name	Description
14	SYNC_STATUS	When set (1), the wdog bark time is synchronizing to the SLEEP_CLK. The data value is not guaranteed until the SYNC_STATUS bit is clear (0). This bit is read only.
13:0	DATA	The wdog counter value on which to trigger the bark interrupt

0x12081818 PPSS_WDOG_TEST_LOAD_STATUS

Type: Read
Reset State: 0x0

The PPSS_WDOG_TEST_LOAD_STATUS register indicates when the watchdog test load is synchronizing to sleep_clk

PPSS_WDOG_TEST_LOAD_STATUS

Bits	Name	Description
0	SYNC_STATUS	When set (1) wdog test load is synchronizing to SLEEP_XTAL_CLK. Data value is not guaranteed until sync_status bit is clear (0).

0x1208181C PPSS_WDOG_TEST_LOAD

Type: Write (Command)
Clock: PPSS_PCLK
Reset State: 0x0

The PPSS_WDOG_TEST_LOAD register loads the PPSS_WDOG_TEST register value into the watchdog counter. Any write to this register, irrespective of the value written, creates a load pulse.

The watchdog counter must be enabled before the counter can be loaded. A watchdog counter load has a lower priority than a reset condition.

PPSS_WDOG_TEST_LOAD

Bits	Name	Description
0	LOAD	

0x12081820 PPSS_WDOG_TEST

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x0

The PPSS_WDOG_TEST register indicates that the watchdog test is synchronizing to sleep_clk and contains the watchdog counter test load value.

PPSS_WDOG_TEST

Bits	Name	Description
14	SYNC_STATUS	When set (1), the watchdog test is synchronizing to SLEEP_ XTAL_CLK. The data value is not guaranteed until the SYNC_STATUS bit is clear (0).
13:0	LOAD_VALUE	The watchdog counter test load value [13:0]. The watchdog counter is 14 bits.

0x12081824 TIMER_CLK_CNTL

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x0000_0000

The TIMER_CLK_CNTL register provides a means of saving power by turning off the clocks to the Sleep and Watchdog timers when they are not in use.

TIMER_CLK_CNTL

Bits	Name	Description
1	WDOG_TIMER_CLK_ON	When the watchdog timer is not in use, the clock should be switched OFF to save power. 0x0: Clock OFF 0x1: Clock ON

TIMER_CLK_CNTL (cont.)

Bits	Name	Description
0	SLP_TIMER_CLKS_ON	When both sleep timers are not in use, the clocks should be switched OFF to save power. 0x0: Clocks OFF 0x1: Clocks ON

20.43 PPS SS Master Controller Registers (0x12080000 PPSS_BASE)

This section contains Peripheral Process Subsystem (PPSS) Master Controller registers.

0x12082004 PAUSE

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x0

PAUSE

Bits	Name	Description
0	PAUSE	Signal to halt the ARM7 clock Note that negative edge or active low interrupt will not cause the PPSS Processor to automatically wake-up. 0x0: Do not halt 0x1: Halt

0x1208200C PROC_TYPE

Type: Read
Clock: PPSS_PCLK
Reset State: 0x1

PROC_TYPE

Bits	Name	Description
2:0	PROC_TYPE	The type of CPU in PPSS. Default is ARM7. 0x0: No CPU 0x1: ARM7 0x2: IO Proc 0x3: Reserved_1 0x4: Reserved_2 0x5: Reserved_3 0x6: Reserved_4 0x7: Reserved_5

0x12082010 RAM_SIZE

Type: Read
Clock: PPSS_PCLK
Reset State: 0x30

RAM_SIZE

Bits	Name	Description
7:0	RAM_SIZE	This 8-bit register output gives the size of the PPSS Code RAM in 16 kilobytes multiples, e.g., RAM_SIZE of 0xA0 is equivalent to 160 kilobytes (16 x A), where the lower nibble is ignored. The memory size may be configured by setting a generic where the PPSS core is instantiated.

0x12082014 BUFFER_SIZE

Type: Read
Clock: PPSS_PCLK
Reset State: 0x10

BUFFER_SIZE

Bits	Name	Description
7:0	BUFFER_SIZE	This 8-bit register output gives the size of the PPSS Buffer RAM in 16 kilobytes multiples, e.g., BUFFER_SIZE of x10 is equivalent to 16 kilobytes (16 x 1), where the lower nibble is ignored. The memory size may be configured by setting a generic where the PPSS core is instantiated.

0x12082018 ROM_SIZE

Type: Read
Clock: PPSS_PCLK
Reset State: 0x00

ROM_SIZE

Bits	Name	Description
7:0	ROM_SIZE	Size of the ROM in kilobytes 0x0: No ROM

0x1208201C RAM_SHORTCUT_ENABLE

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x1

RAM_SHORTCUT_ENABLE

Bits	Name	Description
0	RAM_SHORTCUT_ENABLE	PPSS Code RAM Shortcut Enable. The PPSS processor (ARM7) can have a direct connection, via the PPSS Code RAM Shortcut, to the PPSS Code RAM bank, mapping the memory to address 0x0000_0000 to support the ARM7 exception vectors. The direct connection also provides single-cycle access time, which is critical as the ARM7 has no internal cache. On power-up, the PPSS Code RAM shortcut is enabled. It is recommended to leave the shortcut enabled unless the PPSS Processor needs to access the lower end of the chip address space (0x0000_0000 to RAM_SIZE*16*1024 - 4). If it is necessary to access PPSS Code RAM while the Code RAM Shortcut is disabled, the memory address must be modified by SW to reflect the PPSS Memory Map (i.e., PPSS HW does not automatically modify the address). 0x0: Disable Code RAM shortcut 0x1: Enable Code RAM shortcut

0x12082020 BUFFER_SHORTCUT_ENABLE

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x1

BUFFER_SHORTCUT_ENABLE

Bits	Name	Description
0	BUFFER_SHORTCUT_ENABLE	PPSS Buffer RAM Shortcut Enable. The PPSS processor (ARM7) can have a direct connection, via the PPSS Buffer RAM Shortcut, to the PPSS Buffer RAM bank, mapping the memory (to address RAM_SIZE*16*1024) to be contiguous with Code RAM and thus supporting instruction storage in Buffer RAM. The direct connection also provides single-cycle access time. On power-up, the PPSS Buffer RAM shortcut is enabled. It is recommended to leave the shortcut enabled unless the PPSS processor needs to access the lower end of the chip address space (RAM_SIZE*16*1024 to ((RAM_SIZE + BUFFER_SIZE)*16*1024 - 4)). If it is necessary to access PPSS Buffer RAM while the Buffer RAM Shortcut is disabled, the memory address must be modified by SW to reflect the PPSS Memory Map (i.e., PPSS HW does not automatically modify the address). 0x0: Disable Buffer RAM shortcut 0x1: Enable Buffer RAM shortcut

0x12082024 PERIPHERAL_SHORTCUT_ENABLE

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x1

PERIPHERAL_SHORTCUT_ENABLE

Bits	Name	Description
0	PERIPHERAL_SHORTCUT_ENABLE	PPSS Peripheral shortcut enable. The PPSS processor (ARM7) can have a direct connection, via the PPSS Peripheral shortcut, to the PPSS Peripheral Block bypassing the Fabric thus providing a low latency path, to PPSS Interrupt, GPI, GPO, Timers, and watchdog registers. On power-up, the PPSS Peripheral shortcut is enabled, and it is recommended to leave the shortcut enabled. 0x0: Disable Peripheral shortcut 0x1: Enable Peripheral shortcut

0x12082028 INTERRUPT_MODE

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x00

The INTERRUPT_MODE register controls the source of IRQ and FIQ within PPSS to be from either the internal Interrupt Controller within PPSS or from an external Secondary Interrupt Controller (SIC) at chip level.

INTERRUPT_MODE

Bits	Name	Description
1:0	INTERRUPT_MODE	Defines the PPSS interrupt mode 0x0: IRQ External and FIQ External 0x1: IRQ External and FIQ Internal 0x2: IRQ Internal and FIQ External 0x3: IRQ Internal and FIQ Internal

0x1208202C PPSS_RAM_ARB_CFG

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x1

The PPSS_RAM_ARB_CFG register controls the selection of the arbitration mode for the PPSS RAM slave arbiter: fair round robin or programmable priority. It is also used to set the priority level for each master for programmable priority mode.

NOTE the default arbitration mode is set to fair round robin mode and SHOULD NOT BE CHANGED.

The programmable priority mode is for future use ONLY.

PPSS_RAM_ARB_CFG

Bits	Name	Description
1	PRIORITY_0	SW: RW, HW: R First priority level (highest) Note that there is no need for a PRIORITY_1 register bit because Priority 1 is simply the opposite binary bit to the Priority 0 value in a two master arbiter system such as this one. Therefore, Priority 1 is calculated in the RTL code. Power-up value is 0 (ARM7). It is recommended to leave ARM7 as the high priority master. 0x0: ARM7 0x1: FABRIC AHB
0	ARB_TYPE	Stores arbiter type: Power-up value is 1 (fair round robin mode) and SHOULD NOT BE CHANGED. Programmable priority mode is for future use ONLY. 0x1: Fair Round Robin Mode

0x12082030 PPSS_BUFFER_ARB_CFG

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x1

The PPSS_BUFFER_ARB_CFG register controls the selection of the arbitration mode for the PPSS buffer slave arbiter: fair round robin or programmable priority. It is also used to set the priority level for each master for programmable priority mode.

NOTE the default arbitration mode is set to fair round robin mode and SHOULD NOT BE CHANGED.

The programmable priority mode is for future use ONLY.

PPSS_BUFFER_ARB_CFG

Bits	Name	Description
1	PRIORITY_0	SW: RW, HW: R First priority level (highest) The PRIORITY_0 bit is used in the design whether the ARB_TYPE bit is set as programmable priority or round robin mode. Note that there is no need for a PRIORITY_1 register bit because Priority 1 is simply the opposite binary bit to the Priority 0 value in a two master arbiter system such as this one. Therefore, Priority 1 is calculated in the RTL code. Power-up value is 0 (ARM7). It is recommended to leave ARM7 as the high priority master. 0x0: ARM7 0x1: FABRIC AHB
0	ARB_TYPE	Stores arbiter type: Power-up value is 1 (fair round robin mode) and SHOULD NOT BE CHANGED. Programmable priority mode is for future use ONLY 0x1: Fair Round Robin Mode

0x12082034 PPSS_DEBUG_BUS_SEL

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x0

PPSS_DEBUG_BUS_SEL

Bits	Name	Description
3:0	SEL	Select value for the PPSS Debug Bus MUX. When the value in this register is zero, the output on the PPSS Debug Bus will be a 32-bit zero vector. The MUX select values and associated signal group outputs on the debug bus are: 0000 --> 32-bit zero vector 0001 --> Clock and reset signals 0010 --> Slave 0 (S0) AHB and internal APB signals 0011 --> Slave 0 (S0) AHB 0100 --> Internal APB signals 0101 --> Slave 1 (S1) AHB signals 0110 --> PPSS Code RAM signals 0111 --> Slave 2 (S2) AHB signals 1000 --> PPSS Buffer RAM signals 1001 --> Master (PPSS Processor) signals 1010 --> JTAG and PPSS Processor debug signals 1011 --> Interrupts and 8-bit GPIO output 1100 --> PPSS Code Memory and AHB Subsystem selected ports and internal signals 1101 --> PPSS Buffer Memory and AHB Subsystem selected ports and internal signals 1110 --> Unused 1111 --> Unused

0x12082038 PPSS_CLZ_IN

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x00000000

PPSS_CLZ_IN

Bits	Name	Description
31:0	PPSS_CLZ_IN	32-bit input to the HW Count Leading Zeros (CLZ) functionality of the PPSS master control block. The result of the HW CLZ functionality appears as the contents of the PPSS_CLZ_OUT register.

0x1208203C PPSS_CLZ_OUT

Type: Read
Clock: PPSS_PCLK
Reset State: 0x00

PPSS_CLZ_OUT

Bits	Name	Description
5:0	PPSS_CLZ_OUT	6-bit output of the HW Count Leading Zeros (CLZ) functionality of the PPSS master control block. The input to the HW CLZ functionality should be specified via the PPSS_CLZ_IN register.

0x12082040 PPSS_ACC

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x0

PPSS_ACC

Bits	Name	Description
31:0	RESERVED	

0x12082044 PPSS_RPM_SPM_BYPASS

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x0

PPSS_RPM_SPM_BYPASS

Bits	Name	Description
0	PPSS_RPM_SPM_BYPASS	Selects control of processor bring up from halt state to be either dependent on the RPM SPM or not. When RPM_SPM_BYPASS is enabled, processor bring up from halt is only dependent on PAUSE register setting. When RPM_SPM_BYPASS is disabled, processor bring up from halt is dependent on status of the PAUSE register and the RPM SPM bringup_ack signal. If the bringup_ack is low the processor will be halted, even if the PAUSE register is cleared. 0x0: RPM_SPM_BYPASS_ENABLE 0x1: RPM_SPM_BYPASS_DISABLE

0x12082048 PPSS_RPM_SPM_HANDSHAKE

Type: Read
Clock: PPSS_PCLK
Reset State: 0xA

The PPSS_RPM_SPM_HANDSHAKE register shows the RPM_SPM handshake signals.

PPSS_RPM_SPM_HANDSHAKE

Bits	Name	Description
3	BRINGUP_REQ	bringup request sent from PPSS to RPM
2	SHUTDOWN_REQ	shutdown request sent from PPSS to RPM
1	BRINGUP_ACK	bringup acknowledgement returned by RPM
0	SHUTDOWN_ACK	shutdown acknowledgement returned by RPM

0x1208204C PPSS_RPM_SPM_FSM_RESET

Type: Write
Clock: PPSS_PCLK
Reset State: 0x0

PPSS_RPM_SPM_FSM_RESET

Bits	Name	Description
0	PPSS_RPM_SPM_FSM_RESET	Any write to this resgister will reset the RPM_SPM FSM to default state

20.44 PP SS GPIO Registers (0x12080000 PPSS_BASE)

This section contains Peripheral Process Subsystem (PPSS) GPIO registers.

The following section describes the GPIO settings.

The notation n is used to differentiate between the two GPIO blocks.

0x12082800+ 0x800*n GPIO_n_DIR, n=[0..1]

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x00

GPIO_n_DIR

Bits	Name	Description
7:0	DIR	Direction Register: Each bit within this register controls the corresponding bit within the GPIO block. The Direction register is used to select whether the internal GPIO logic monitors the eight external input lines or the outputs from the internal WDATA register. NOTE In GPIO_1 the WDATA register outputs are permanently connected to the external inputs so this register is not required. 0x0: External input 0x1: Internal input

0x12082804+ 0x800*n GPIO_n_IS, n=[0..1]

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x00

GPIO_n_IS

Bits	Name	Description
7:0	IS	Interrupt Sense Register: Each bit within this register controls the corresponding bit within the GPIO block. 0x0: Edge detection 0x1: Level detection

0x12082808+ 0x800*n GPIO_n_IBE, n=[0..1]

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x00

GPIO_n_IBE

Bits	Name	Description
7:0	IBE	Interrupt Both Edge Register: Each bit within this register controls the corresponding bit within the GPIO block. If Single edge detection is selected, the IEV register determines whether a rising or falling edge is required. If Both edge detection is selected, the circuit triggers on both a rising and falling edge. 0x0: Single edge detection 0x1: Both edge detection

0x1208280C+ 0x800*n GPIO_n_IEV, n=[0..1]

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x00

GPIO_n_IEV

Bits	Name	Description
7:0	IEV	Interrupt Event Register: Each bit within this register controls the corresponding bit within the GPIO block. The Interrupt Event Register performs two different functions depending upon whether the corresponding bit within the Interrupt Sense Register has been set for edge or logic level detection. Low selects a falling edge or logic '0' detection High selects a rising edge or logic '1' detection 0x0: Neg edge or low level 0x1: Pos edge or high level

0x12082810+ 0x800*n GPIO_n_IE, n=[0..1]

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x00

GPIO_n_IE

Bits	Name	Description
7:0	IE	Interrupt Enable Register: Each bit within this register controls the corresponding bit within the GPIO block. 0x0: Interrupt disabled 0x1: Interrupt enabled

0x12082814+ 0x800*n GPIO_n_RIS, n=[0..1]

Type: Read
Clock: PPSS_PCLK
Reset State: 0x00

GPIO_n_RIS

Bits	Name	Description
7:0	RIS	Raw Interrupt Status Register: Allows the output state of each of the eight edge/ level interrupt detection circuits to be read.

0x12082818+ 0x800*n GPIO_n_MIS, n=[0..1]

Type: Read
Clock: PPSS_PCLK
Reset State: 0x00

GPIO_n_MIS

Bits	Name	Description
7:0	MIS	Masked Interrupt Status Register: Performs an identical function to the Raw Interrupt Status Register except the inputs to this register are ANDed with the outputs from the Interrupt Enable Register, i.e., only the status of the bits that can cause an interrupt are read.

0x1208281C+ 0x800*n GPIO_n_IC, n=[0..1]

Type: Write
Clock: PPSS_PCLK
Reset State: 0x00

GPIO_n_IC

Bits	Name	Description
7:0	IC	Interrupt Clear: Each bit controls the corresponding bit within the GPIO block. Note: logic level interrupts are not latched and, therefore, cannot be cleared by means of this register. 0x0: Do not clear 0x1: Clear edge triggered interrupt

0x12082820+ 0x800*n GPIO_n_WDATA, n=[0..1]

Type: Read/Write
Clock: PPSS_PCLK
Reset State: 0x00

GPIO_n_WDATA

Bits	Name	Description
7:0	WDATA	Write Data Register: The outputs of this register connect to the eight GPIO data output lines. Only the output lines from GPIO block 1 are used. GPIO Block 1 Output Connections: The upper 5 bits are routed to the PPSS top level for general use. The top level signal names are ppss_gp1_out, i.e., ppss_gp1_out (4:0) <= ppss_gpio_out(7:3) The lower 3 bits are routed to the PPSS top level and externally routed to the RPM interrupt inputs listed below: dsps_rpm_gp_high_irq <= ppss_gpio_out(2) dsps_rpm_gp_medium_irq <= ppss_gpio_out(1) dsps_rpm_gp_low_irq <= ppss_gpio_out(0)

0x12082824+ 0x800*n GPIO_n_WDSET, n=[0..1]

Type: Write
Clock: PPSS_PCLK
Reset State: 0x00

GPIO_n_WDSET

Bits	Name	Description
7:0	WDSET	Write Data Set: Each bit sets the corresponding bit within the Write Data Register. Note that writing a zero has no effect. 0x0: Do not set 0x1: Set

0x12082828+ 0x800*n GPIO_n_WDCLR, n=[0..1]

Type: Write
Clock: PPSS_PCLK
Reset State: 0x00

GPIO_n_WDCLR

Bits	Name	Description
7:0	WDCLR	Write Data Clear: Each bit clears the corresponding bit within the Write Data Register. 0x0: Do not clear 0x1: Clear

0x1208282C+ 0x800*n GPIO_n_RPIND, n=[0..1]

Type: Read
Clock: PPSS_PCLK
Reset State: 0x00

GPIO_n_RPIND

Bits	Name	Description
7:0	RRPIND	Read Pin Data: The data applied to each of the eight external inputs is fed through a two stage synchronization circuit clocked at the PCLK frequency. RPIND returns the value of the data as it appears at the output of the synchronization circuits.

Index of Registers

A Exhibit 1

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1.4 **WARRANTY DISCLAIMER**. YOU EXPRESSLY ACKNOWLEDGE AND AGREE THAT THE USE OF THE MATERIALS IS AT YOUR SOLE RISK. THE MATERIALS AND TECHNICAL SUPPORT, IF ANY, ARE PROVIDED "AS IS" AND WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS OR IMPLIED. QTI ITS LICENSORS AND AFFILIATES MAKE NO WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THE MATERIALS OR ANY OTHER INFORMATION OR DOCUMENTATION PROVIDED UNDER THIS AGREEMENT, INCLUDING BUT NOT LIMITED TO ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR AGAINST INFRINGEMENT, OR ANY EXPRESS OR IMPLIED WARRANTY ARISING OUT OF TRADE USAGE OR OUT OF A COURSE OF DEALING OR COURSE OF PERFORMANCE. NOTHING CONTAINED IN THIS AGREEMENT SHALL BE CONSTRUED AS (I) A WARRANTY OR REPRESENTATION BY QTI, ITS LICENSORS OR AFFILIATES AS TO THE VALIDITY OR SCOPE OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT OR (II) A WARRANTY OR REPRESENTATION BY QTI THAT ANY MANUFACTURE OR USE WILL BE FREE FROM INFRINGEMENT OF PATENTS, COPYRIGHTS OR OTHER INTELLECTUAL PROPERTY RIGHTS OF OTHERS, AND IT SHALL BE THE SOLE RESPONSIBILITY OF YOU TO MAKE SUCH DETERMINATION AS IS NECESSARY WITH RESPECT TO THE ACQUISITION OF LICENSES UNDER PATENTS AND OTHER INTELLECTUAL PROPERTY OF THIRD PARTIES.

1.5 **LIMITATION OF LIABILITY**. IN NO EVENT SHALL QTI, QTI’S AFFILIATES OR ITS LICENSORS BE LIABLE TO YOU FOR ANY INCIDENTAL, CONSEQUENTIAL OR SPECIAL DAMAGES, INCLUDING BUT NOT LIMITED TO ANY LOST PROFITS, LOST SAVINGS, OR OTHER INCIDENTAL DAMAGES, ARISING OUT OF THE USE OR INABILITY TO USE, OR THE DELIVERY OR FAILURE TO DELIVER, ANY OF THE MATERIALS, OR ANY BREACH OF ANY OBLIGATION UNDER THIS AGREEMENT, EVEN IF QTI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. THE FOREGOING LIMITATION OF LIABILITY SHALL REMAIN IN FULL FORCE AND EFFECT REGARDLESS OF WHETHER YOUR REMEDIES HEREUNDER ARE DETERMINED TO HAVE FAILED OF THEIR ESSENTIAL PURPOSE. THE ENTIRE LIABILITY OF QTI, QTI’s AFFILIATES AND ITS LICENSORS, AND THE SOLE AND EXCLUSIVE REMEDY OF YOU, FOR ANY CLAIM OR CAUSE OF ACTION ARISING HEREUNDER (WHETHER IN CONTRACT, TORT, OR OTHERWISE) SHALL NOT EXCEED US$10.

2. **COMPLIANCE WITH LAWS; APPLICABLE LAW**. You agree to comply with all applicable local, international and national laws and regulations and with U.S. Export Administration Regulations, as they apply to the subject matter of this Agreement. This Agreement is governed by the laws of the State of California, excluding California's choice of law rules.

3. C**ONTRACTING PARTIES**. If the Materials are downloaded on any computer owned by a corporation or other legal entity, then this Agreement is formed by and between QTI and such entity. The individual accepting the terms of this Agreement represents and warrants to QTI that they have the authority to bind such entity to the terms and conditions of this Agreement.

4. **MISCELLANEOUS PROVISIONS**. This Agreement, together with all exhibits attached hereto, which are incorporated herein by this reference, constitutes the entire agreement between QTI and You and supersedes all prior negotiations, representations and agreements between the parties with respect to the subject matter hereof. No addition or modification of this Agreement shall be effective unless made in writing and signed by the respective representatives of QTI and You. The restrictions, limitations, exclusions and conditions set forth in this Agreement shall apply even if QTI or any of its affiliates becomes aware of or fails to act in a manner to address any violation or failure to comply therewith. You hereby acknowledge and agree that the restrictions, limitations, conditions and exclusions imposed in this Agreement on the rights granted in this Agreement are not a derogation of the benefits of such rights. You further acknowledges that, in the absence of such restrictions, limitations, conditions and exclusions, QTI would not have entered into this Agreement with You. Each party shall be responsible for and shall bear its own expenses in connection with this Agreement. If any of the provisions of this Agreement are determined to be invalid, illegal, or otherwise unenforceable, the remaining provisions shall remain in full force and effect. This Agreement is entered into solely in the English language, and if for any reason any other language version is prepared by any party, it shall be solely for convenience and the English version shall govern and control all aspects. If You are located in the province of Quebec, Canada, the following applies: The Parties hereby confirm they have requested this Agreement and all related documents be prepared in English.